IntelliStation Z Pro Type 6866

Technical Information Manual

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Note

Before using this information and the product it supports, be sure to read the information in “Appendix E. Notices and trademarks” on page 47.

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Contents

Preface

This *Technical Information Manual* provides information for the IBM® Z Pro Professional Type 6866 computer. The manual is intended for developers who want to provide hardware and software products to operate with this IBM computer. It provides an in-depth view of how this IBM computer works. Users of this publication should have an understanding of computer architecture and programming concepts.

Related publications

In addition to this manual, the following IBM publications provide information related to the operation of the IBM IntelliStation Z Pro Professional Workstation:

- *IntelliStation Z Pro User Guide*

  This publication, also available on the *Software Selections CD*, contains information about setting up your computer, configuring hardware and software, operating and maintaining your computer, and installing options. Also included are warranty information, instructions for diagnosing and solving problems, and information on how to obtain help and service.

- *Understanding Your Personal Computer*

  This online document includes general information about using computers and detailed information about the features of the IntelliStation Z Pro Professional Workstation.

- *Hardware Maintenance Manual*

  This publication contains information for trained service technicians. It is available at http://www.ibm.com/pc/support on the World Wide Web, and it can also be ordered from IBM. To purchase a copy, see the ″Getting help, service, and information″ section in the *IntelliStation Z Pro User Guide*.

- *Adaptec Technical Reference*

  This documentation is provided on the *Software Selections CD* that comes with the IntelliStation Z Pro Type 6866 computer. It includes instructions for installing and configuring Small Computer Systems Interface (SCSI) devices.

Terminology usage

Attention: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

In this manual, some signals are represented in an all-capital-letter format (−ACK). A minus sign in front of the signal indicates that the signal is active low. No sign in front of the signal indicates that the signal is active high.

The use of the term hex indicates a hexadecimal number.

When numerical modifiers such as K, M, and G are used, they typically indicate powers of 2, not powers of 10. For example, 1 KB equals 1 024 bytes (2^{10}), and 1 GB equals 1 073 824 bytes (2^{30}). However, when expressing storage capacity, powers of 10 are used. 1 MB equals approximately 1 000 KB (1 000 000 bytes).

Note: Depending on the operating system and other system requirements, the storage capacity available to the user might vary.

Chapter 1. System overview

IntelliStation Z Pro Type 6866 computer systems provide state-of-the-art computing power with room for future growth.

Major features

The major features are:

- An Intel® Pentium® III Xeon® microprocessor with MMX™ technology, streaming single-instruction multiple data (SIMD) extensions and 256 KB advanced transfer cache memory
- Up to 2 Gigabytes (GB) of system memory
- Dual microprocessor support
- Integrated drive electronics (IDE) bus master controller, Ultra DMA-66 capable
- Integrated SCSI controller, Ultra 160M capable
- System management
-
  - Wake on LAN® support
  - Desktop Management Interface (DMI) BIOS and DMI software
  - Integrated network protocols
  - Enablement for Remote Administration
  - Wake on Ring support
- IDE CD-ROM drive, standard
- Asset security
  - Security settings provided by the Configuration/Setup Utility program
    - Power-on and administrator password protection
    - Startup sequence control
    - Hard disk drive and diskette drive access control
    - I/O port control
  - Cover key lock
  - U-bolt and security cabling
  - Operating system security
  - Alert on LAN® support
  - Tamper-detection switch on the chassis
- Accelerated graphics port (AGP) adapter
- Integrated 16-bit stereo audio controller and built-in high-quality speaker (supports SoundBlaster, Adlib, and Microsoft® Windows® Sound System applications)
- IBM 10/100 megabits-per-second (Mbps) Ethernet subsystem with Wake on LAN support
- Expansion
  - Nine drive bays
  - Two 64-bit PCI connectors
  - Four 32-bit PCI connectors
  - One AGP Pro connector
- PCI version 2.2 I/O bus compatibility

- 3.5-inch, 1.44 MB diskette drive
- Input/Output features
  - One 25-pin parallel port with Extended Capabilities Port (ECP)/Extended Parallel Port (EPP) support
  - Two 9-pin universal asynchronous receiver/transmitter (UART) serial ports
  - Two 4-pin Universal Serial Bus ports
  - One 6-pin keyboard port
  - One 6-pin mouse port
  - One 15-pin DD2CB-compliant monitor port on the AGP adapter
  - Three 3.5-mm audio jacks (line out/headphone, line-in, microphone)

Other features

The IntelliStation Z Pro Type 6866 computer supports the following features.

Network support

The IntelliStation Z Pro Type 6866 computer is enabled to support management over a network. The following is a list of supported functions:

- Selectable primary startup sequence
- Selectable automatic power-on startup sequence
- Selectable error startup sequence
- POST/BIOS update from network
- Wake on LAN
- CMOS Save/Restore utility program
- CMOS setup over LAN
- Wake on Ring

Wake on LAN

The power supply of the computer supports the Wake on LAN feature. You can use the Wake on LAN feature to turn on the computer by passing a specific LAN frame to the computer over the LAN. You can find the menu for setting the Wake on LAN feature in the Configuration/Setup Utility program. For more information, see the *IntelliStation Z Pro User Guide*.

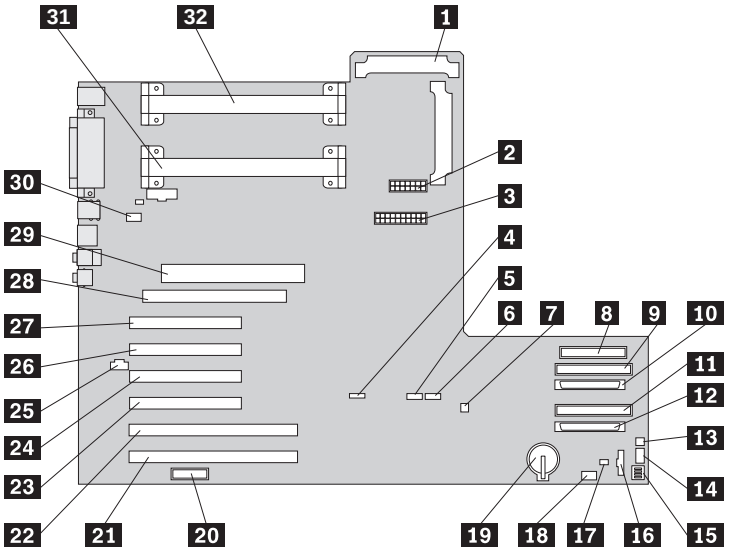
Chapter 2. System board features

This section includes information about system board features.

System board layout

The system board might look slightly different from the one shown.

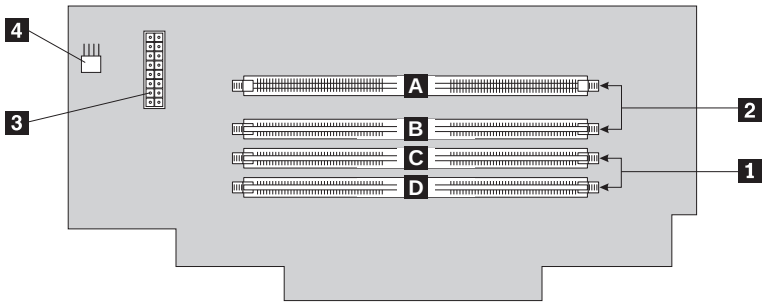
Note: A diagram of the system board, including switch and jumper settings, is attached to the computer cover.



1	Second CPU VRM	17	Tamper detection switch connector
2	Power connector 2	18	Radio frequency antenna connector
3	Power connector 1	19	Battery
4	Hard disk LED	20	MIDI/joystick connector
5	Wake on LAN connector	21	Slot 7 (64-bit PCI connector)
6	Alert on LAN connector	22	Slot 6 (64-bit PCI connector)
7	Wake on modem connector	23	Slot 5 (32-bit PCI connector)
8	Diskette drive connector	24	Slot 4 (32-bit PCI connector)
9	Secondary IDE connector	25	CD audio connector
10	SCSI channel B connector	26	Slot 3 (32-bit PCI connector)
11	Primary IDE connector	27	Slot 2 (32-bit PCI connector)
12	SCSI channel A connector	28	Slot 1 (AGP connector)
13	Internal speaker connector	29	Memory card connector
14	Front fan connector	30	Rear fan connector
15	Rocker switch	31	Microprocessor 1
16	Front panel connector	32	Microprocessor 2

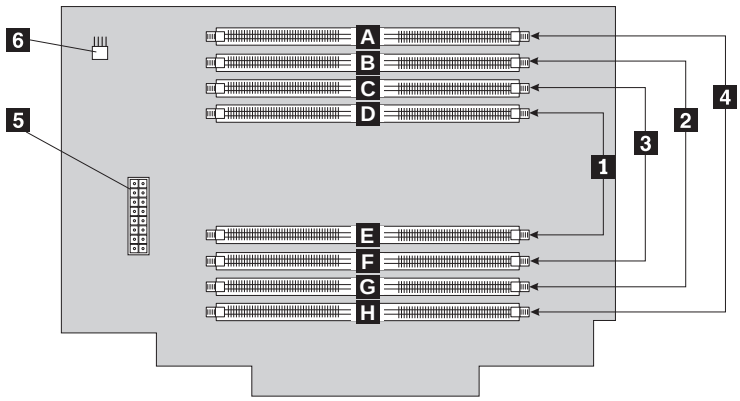
Memory card layout

The following illustration shows the layout of the four- RIMM memory card:



1	RIMM pair 1	A	RIMM connector 1
2	RIMM pair 2	B	RIMM connector 2
3	Power connector	C	RIMM connector 3
4	Hard disk drive fan connector	D	RIMM connector 4

The following illustration shows the layout of the eight-RIMM memory card:



1	RIMM pair 1	A	RIMM connector 1
2	RIMM pair 2	B	RIMM connector 2
3	RIMM pair 3	C	RIMM connector 3
4	RIMM pair 4	D	RIMM connector 4
5	Power connector	E	RIMM connector 5
6	Hard disk drive fan connector	F	RIMM connector 6
		G	RIMM connector 7
		H	RIMM connector 8

Pentium III Xeon microprocessor with MMX technology

IntelliStation Z Pro Type 6866 computer comes with an Intel Pentium III Xeon microprocessor. The microprocessor, which has an attached heat sink, plugs directly into a connector on the system board.

The features of the microprocessor are as follows:

- Optimization for 32-bit software
- 64-bit microprocessor data bus

- 133 MHz front-side bus (FSB)
- 256 KB full-speed advanced transfer cache memory integrated into the microprocessor
  - 4-way set associative
  - Nonblocking
- 36-bit microprocessor address bus
- Math coprocessor
- MMX technology, which boosts the processing of graphic, video, and audio data

Chip set control

The Intel 840 chip set is the interface between the microprocessor and the following:

- Memory subsystem
- PCI buses
- IDE bus master connection
- SCSI buses
- USB ports
- SMBus
- Enhanced DMA controller
- Real-time clock (RTC)
- Serial ports
- Parallel port
- Ethernet
- Audio

Memory subsystem

The system memory interface is controlled by the Intel 840 chip set. System memory is Rambus dynamic random access memory (RDRAM).

The maximum amount of system memory is 2 GB. For memory expansion, the memory card provides Rambus inline memory module (RIMM) connectors.

There are two available memory cards for the IntelliStation Z Pro Type 6866 computer. One is a four-connector memory card, and one is an eight-connector memory card. The four-connector memory card is divided into two RIMM pairs. The eight-connector memory card is divided into four RIMM pairs.

The memory card supports PC600 and PC800 memory RIMMs in sizes of 64 MB, 128 MB, and 256 MB. Memory must be installed in matched pairs. The amount of preinstalled memory varies by model.

The following information applies to system memory:

- RIMMs must be installed in pairs. The RIMMs installed in a RIMM connector pair must be the same speed and size.
- If the memory card in your computer has four RIMM connectors, any connector that does not have a RIMM installed must have a *continuity RIMM* (C-RIMM), a module that looks like a RIMM but has no memory on it. A C-RIMM is used to continue the connection on a RIMM connector that does not have memory installed in it.

- If the memory card in the computer has eight RIMM connectors, pairs 1 and 3 must have RIMMs or C-RIMMs installed in them. If RIMMs are installed in pair 2, RIMMs or C-RIMMs must be installed in pair 4 for optimal performance. For the arrangement of the RIMM connector pairs on your computer memory card, see the illustrations on page 4.
- Error checking and correction (ECC) or non-ECC RDRAM is supported. Install only ECC RIMMs to enable ECC. If you use ECC and non-ECC memory together, all installed memory will function as non-ECC memory.
- The maximum height of memory modules is 3.465 cm (1.375 in.).
- RIMM connectors do not support dual inline memory modules (DIMMs).
- Use PC600 or PC800 RIMMs only.
- System memory is auto-detected and auto-configured using serial presence detect.

The following tables show the possible configuration of RIMMs and C-RIMMs that can be used in the IntelliStation Z Pro Type 6866 computer.

Memory placement for 4-RIMM Memory Card

	Pair 1		Pair 2	
	3	**4**	**1**	**2**
2 RIMMs	RIMM	RIMM	C-RIMM	C-RIMM
4 RIMMs	RIMM	RIMM	RIMM	RIMM

Note: Memory must be installed in matched pairs.

Memory placement for 8-RIMM Memory Card

	Pair 4	Pair 2	Pair 3	Pair 1				
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
2 RIMMs	(1)	(1)	C-RIMM	RIMM	RIMM	C-RIMM	(1)	(1)
4 RIMMs	C-RIMM	RIMM	C-RIMM	RIMM	RIMM	C-RIMM	RIMM	C-RIMM
4 RIMMs*	(1)	(1)	RIMM	RIMM	RIMM	RIMM	(1)	(1)
6 RIMMs	C-RIMM	RIMM	RIMM	RIMM	RIMM	RIMM	RIMM	C-RIMM
8 RIMMs	RIMM	RIMM	RIMM	RIMM	RIMM	RIMM	RIMM	RIMM

Note: Memory must be installed in matched pairs.
***** Non-optimal performance configuration
(1) These connectors may either be left empty or used to store c-rimms.

Notes:

1. PC600 RIMM runs at 300 MHz
2. PC800 RIMM runs at 400 MHz

For information on the pin assignments for the memory module connectors, see “Memory connectors” on page 27.

PCI bus

The fully synchronous 32-bit 33 MHz PCI bus and the 64-bit 66 MHz PCI bus originate in the chip set. Features of these PCI buses are:

- Integrated arbiter with multitransaction, PCI-arbitration, acceleration hooks
- Zero-wait-state, microprocessor-to-PCI write interface for high-performance graphics
- Built-in PCI bus arbiter with support for all PCI devices and connectors
- Microprocessor-to-PCI memory write posting
- Conversion of back-to-back, sequential, microprocessor-to-PCI memory write to PCI burst write
- PCI-to-DRAM memory up to 528 megabytes per second (MBps) speed

- PCI 2.2 compliant
- Delayed transaction
- PCI parity checking and generation support

IDE bus master interface

The system board incorporates a PCI-to-IDE interface that complies with the *AT Attachment Interface with Extensions* standard.

The bus master for the IDE interface is integrated into the Intel 840 chip set. The chip set is PCI 2.2 compliant. It connects directly to the PCI bus and is designed to allow concurrent operations on the PCI bus and the IDE bus. The chip set is capable of supporting PIO mode 0-4 devices and IDE DMA mode 0-3 devices, and ATA 66 transfers of up to 66 Mbps.

The IDE devices receive their power through a four-position power cable containing +5 v dc, +12 v dc, and ground voltage. When devices are added to the IDE interface, one device is designated as the master (primary) device and another is designated as the slave (secondary) device. These designations are determined by jumpers on each device. Two connectors are provided on the system board for the IDE interface. One is designated Primary and the other Secondary, allowing up to four devices to be attached. For information on the connector pin assignments, see “IDE connectors” on page 26.

For the IDE interface, no resource assignments are given in the system memory or the direct memory access (DMA) channels. For information on the resource assignments, see Table 39 on page 43.

USB interface

Universal Serial Bus (USB) technology is a standard feature of the computer. The system board provides the USB interface with two channels integrated into the chip set. A USB-enabled device can attach to a connector, and if that device is a hub, multiple peripheral devices can attach to the hub and be used by the system. The USB connectors use Plug and Play technology for installed devices. The speed of the USB is up to 12 MBps with a maximum of 127 peripheral devices. The USB is compliant with *Universal Host Controller Interface Guide 1.0*.

Features provided by USB technology include:

- Support for hot-pluggable devices
- Support for concurrent operation of multiple devices
- Suitability for different device speeds
- Support for cable length of up to five meters (16 ft. 5 in) from host to hub or from hub to hub
- Wide range of packet sizes
- Limited power to hubs

For information on the connector pin assignments for the USB interface, see “USB port connectors” on page 23.

Low pin-count bus

The low-pin-count (LPC) bus enables device connections to the Super I/O without ISA or X-Bus. The IntelliStation Z Pro Type 6866 computer uses the National Semiconductor PC87363 Super I/O chip. The PC87363 includes the following:

- Diskette drive controller
- Keyboard and mouse controller
- IEEE 1284 parallel port
- Two UART serial ports
- Wake on LAN support
- MIDI/joystick port
- PC99 compliance
- ACPI compliance

A setting in the Configuration/Setup Utility program enables or disables diskette write protection.

Video subsystem

The IntelliStation Z Pro Type 6866 computer comes with one of the following graphics adapter:

- Matrox Millennium G400 AGP adapter with 16 MB synchronous graphics RAM (SGRAM)
- IBM Fire GL1 AGP adapter with 32 MB SGRAM and a display device driver that supports up to four screens
- Intense3D 4110 AGP adapter

Features of the Matrox Millennium G400 AGP adapter

The Matrox Millennium G400 AGP adapter is a 2D/3D video adapter that includes the Matrox MGA G400D video chip, 16 MB of 166 MHz SGRAM, a 300 MHz random access memory and digital-to-analog converter (RAMDAC), an EEPROM module with video POST and BIOS code, video support for various hardware multimedia upgrades, and a DDC2B monitor connector.

The Matrox MGA G400D video chip is compatible with VGA function, supports all VGA video modes, and contains the following advanced features:

- Integrated video subsystem on the chip including 2D, 3D, and a video port
- AGP 4x system bus interface
- Command list bus-mastering support for fast 2D performance
- 128-bit, 166 MHz SGRAM interface with block write and write-per-bit support
- 256-bit internal data bus
- OpenGL MCD and Direct3D optimized 3D engine
- High-resolution support up to 2048 x 1536
- 300 MHz, internal RAMDAC that supports up to 75 Hz refresh rate at 1920 x 1440 resolution
- Second display output port capable of running at 136 MHz (1280 x 1024 at 75 Hz), which can support a TV, a second monitor, or a flat-panel display
- Multiple monitor and adapter support (up to 16) in one computer
- Compliance with the following standards:
  - PC99
  - AGP 2.0
  - VESA VBE V2.0
  - DDC2B
- Advanced power-management support

- Complete Plug and Play support

Features of the IBM Fire GL1 AGP adapter

The IBM Fire GL1 AGP adapter includes the IBM Oasis video chip, 32 MB of 100 MHz SGRAM, an EEPROM module that contains video POST and BIOS code, and a DDC2B monitor connector.

The IBM Oasis chip uses CMOS technology and is compatible with VGA function and supports all VGA modes. The IBM Oasis chip also contains the following hardware features:

- Integrated video subsystem on a chip including 2D engine, 3D engine, and a 250 MHz, internal RAMDAC that supports up to 85 Hz refresh at 1600 x 1200 or 75 Hz at 1920 x 1200
- AGP 2x capable system bus interface
- 256-bit, 2-way interleaved 100 MHz SGRAM interface with block write and write-per-bit support and bandwidth up to 8.4 GB/second.
- Dual DMA units used for BitBLITs, rendering operations, and texture operations
- Overlay support on a per-window basis
- OpenGL MCD and Direct3D optimized 3D engine
- Pentium III single instruction multiple data (SIMD) and multiprocessor optimization in the OpenGL ICD for high quality video playback
- Multiple monitor and adapter support (up to 4) in one computer
- Complete Plug and Play support, including the monitor

Features of the Intense3D 4110 AGP adapter

The Intense3D 4110 AGP adapter is a 2D/3D video adapter with 128 MB 66.6 MHz SGRAM that includes:

- AGP 2x DMA transfer rates
- AGP 2x fast write transfers from host microprocessor
- 8 MB SDRAM DirectBurst memory
- 64 MB frame buffer supporting SuperScene, full-scene, multi sampled anti aliasing
- Onboard texture memory with full bit-mapped trilinear interpolated texture processing
- Maximum resolution of 1280 x 1024, 75 Hz vertical refresh for the Windows NT Workstation operating system (VGA) startup
- Two video lookup tables
- 16- and 32-bit color depths
- 10-bit gamma correction
- Stereoscopic views support - interlaced or frame sequential
- DDC monitor support
- Digital Visual Interface (DVI-I) flat-panel display support
- Advanced power-management support
- Complete Plug and Pla y support

Monitor support

The video subsystem provides a 15-pin analog monitor connector on the preinstalled graphics adapter. For information on connector pin assignments, see “Monitor connector” on page 23.

Audio subsystem

The IntelliStation Z Pro Type 6866 computer comes with an integrated audio controller. These models are capable of playing and recording sounds and support SoundBlaster, Adlib, and Microsoft Windows Sound System applications.

The device drivers are on the hard disk and are also available on the *Product Recovery CD* or *Device Driver and IBM Enhanced Diagnostics CD* that comes with the computer.

If you connect an optional device to the audio connectors, follow the instructions provided by the manufacturer. (Note that device drivers might be required. If necessary, contact the manufacturer for information on these device drivers.)

The following connectors are available on the integrated audio controller:

- *Line/headphone out* connector for connecting headphones or powered speakers. To hear audio from the adapter you must connect headphones or a set of speakers to the Line out port. These speakers must be powered with a built-in amplifier. In general, powered speakers are available with a wide range of features and power outputs.
- *Line in* connector for connecting musical devices, such as a portable CD player or stereo system.
- *Microphone* connector for attaching a microphone.

Super input/output controller

Control of the integrated input/output (I/O) and diskette drive controllers is provided by a single module. This module, which supports Plug and Play, controls the following features:

- Diskette drive interface
- Serial port
- Parallel port
- Keyboard and mouse ports
- MIDI/joystick port

Diskette drive interface

The IntelliStation Z Pro Type 6866 computer diskette drive subsystem supports the following devices:

- 1.44 MB, 3.5-inch diskette drive
- 1.44 MB, 3.5-inch 3-mode drive for Japan (no BIOS support for 3-mode drive)
- 1.2 MB, 5.25-inch diskette drive
- 1 Mbps, 500 Kbps, or 250 Kbps internal tape drive

Note: A 2.88 MB 3.5-inch diskette drive is not supported.

One 34-pin connector is provided on the system board for diskette drive support. For information about the connector pin assignments, see “Diskette drive connector” on page 26.

Serial ports

Two universal asynchronous receiver/transmitter (UART) serial ports are integrated into the system board. The serial ports include 16-byte data, first-in first-out (FIFO) buffers and have programmable baud rate generators. The serial ports are NS16450 and PC16550A compatible.

For information on the connector pin assignments, see “Serial connector” on page 24.

Note: The current loop interface is not supported.

The following figure shows the default serial port assignments in the configuration.

Table 1. Default serial port assignments

Port assignment	Address range (hex)	IRQ level
Serial 1	03F8–03FF	IRQ 4
Serial 2	02F8–02FF	IRQ 3

Parallel port

Integrated into the system board is support for extended capabilities port (ECP), enhanced parallel port (EPP), and standard parallel port (SPP) modes. The modes of operation are selected through the Configuration/Setup Utility program with the default mode set to SPP. The ECP and EPP modes are compliant with IEEE 1284.

The following table shows the possible parallel port assignments used in the configuration.

Table 2. Parallel port assignments

Port assignment	Address range (hex)	IRQ level
Parallel 1	03BC–03BE	IRQ 7
Parallel 2	0378–037F	IRQ 5
Parallel 3	0278–027F	IRQ 5

The default setting for the parallel port is Parallel 1.

The system board has one connector for the parallel port. For information about the connector pin assignments, see “Parallel connector” on page 24.

Keyboard and mouse ports

The keyboard and mouse subsystem is controlled by a general purpose 8-bit microcontroller that is compatible with 8043AH and PC87911. The controller consists of 256 bytes of data memory and 2 KB of read-only memory (ROM).

The controller has two logical devices: one controls the keyboard, and the other controls the mouse. The keyboard has two fixed I/O addresses and a fixed IRQ line and can operate without the mouse. The mouse cannot operate without the keyboard because, although it has a fixed IRQ line, the mouse relies on assignments given in the system memory addresses or DMA channels. For information on the resource assignments, see Table 38 on page 43 and Table 39 on page 43.

The system board has one connector for the keyboard port and one connector for the mouse port. For information on the connector pin assignments, see Table 39 on page 43.

Network connection

The IntelliStation Z Pro Type 6866 computer has an integrated Ethernet controller.

Features of the Etherne t controller are:

- Operates in shared 10BASE-T or 100BASE-TX environment
- Transmits and receives data at 10 Mbps or 100 Mbps
- Has a RJ-45 connector for LAN attachment
- Supports Wake on LAN
- Supports Alert on LAN
- Supports Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP)

Real-time clock and CMOS

The real-time clock is a low-power clock that provides a time-of-day clock and a calendar. The clock settings are maintained by the battery when the power cord is removed.

The system uses 242 bytes of complementary metal-oxide semiconductor (CMOS) memory to store data. The CMOS memory is erased if rocker switch 3 is switched to the on position.

To locate the battery, see “System board layout” on page 3.

Flash EEPROM

The system board uses 4 megabits (Mb) of flash electrically erasable, programmable, read-only memory (EEPROM) to store the basic input/output system (BIOS), IBM logo, Configuration/Setup Utility, and Plug and Play data.

If necessary, the EEPROM can be easily updated using a stand-alone program that is available on a 3.5-inch diskette. For information to obtain the latest version of the Flash Update Utility program, see the *IntelliStation Z Pro User Guide*.

Expansion adapters

Four expansion connectors on the IntelliStation Z Pro Type 6866 computer are 32-bit 33 MHz slots. These connectors support the 5 V signaling environment that is defined in *PCI Local Bus Specification 2.2*. Two expansion connectors on the IntelliStation Z Pro Type 6866 computer are 64-bit, 66 MHz slots. These connectors support the 3.3 V signaling environment that is defined in *PCI Local Bus Specification 2.1*.

The IntelliStation Z Pro Type 6866 computer has a 3-pin connector on the system board that provides the auxiliary 5 volts (AUX5) and wake-up signal connections. Some Wake on LAN adapters have two connectors: a 3-pin, right-angle header for AUX5, and a 2-pin straight connector for the wake-up signal. These Wake on LAN connector options include a Y-cable that has a 3-pin system-board connector on one end and splits into the 3-pin and 2-pin connectors that connect to the adapter.

For information on installing adapters, see the *IntelliStation Z Pro User Guide*.

For information on the connector pin assignments, see “32-bit PCI connectors” on page 28 and “64-bit PCI connectors” on page 30.

Rocker switches

The following table shows the functions of the rocker switches on the system board. For the location of the rocker switches on the system board, see “System board layout” on page 3.

Table 3. Rocker switch functions

Switch	Function
1	Reset microprocessor frequency to minimum value
2	Reserved
3	CMOS clear/recovery
4	Reserved

Cable connectors

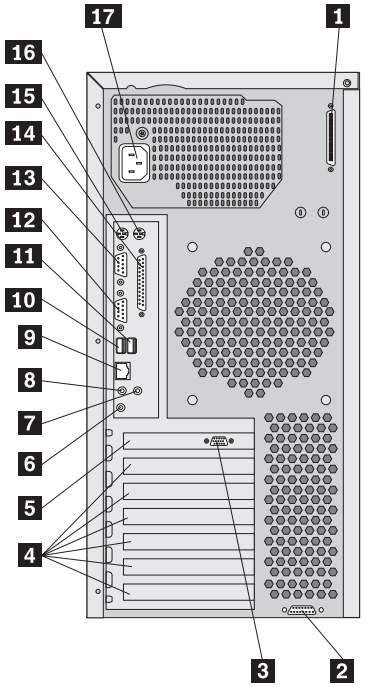
Connectors for attaching peripheral devices are provided on the back of the computer. The connectors are:

- Monitor (SVGA or DVI)
- Keyboard
- Mouse
- Serial (2)
- Parallel
- USB (2)
- Audio connectors for line in, line/headphone out, and microphone
- MIDI/joystick
- SCSI
- Ethernet

For pin assignment details on connectors, see “Appendix A. Connector-pin assignments” on page 23.

Connectors for features integrated into the system board can be identified by an icon directly below each connector. A connector located on an adapter might not have an identifying icon.

The following illustration shows the connector panel for the IntelliStation Z Pro Type 6866 computer.



1 External SCSI connector

2 MIDI/joystick connector

3 Monitor connector

4 PCI expansion slots

5 AGP adapter slot

6 Microphone line in connector

7 Audio line in connector

8 Headphone line out connector

9 Ethernet connector

10 USB 1

11 USB 2

12 Serial connector 2

13 Serial connector 1

14 Parallel connector

15 Keyboard

16 Mouse

17 Power connector

Chapter 3. Physical specifications

This section lists the physical specifications for the IntelliStation Z Pro Type 6866 computer. The IntelliStation Z Pro Type 6866 computer has four 32-bit PCI expansion slots, two 64-bit PCI expansion slots, one AGP slot, and nine drive bays.

Note: The computer is classified as a Class A digital device. See the *IntelliStation Z Pro User Guide* for further information about this classification.

Dimensions
- Height: 440 mm (17.3 in.)
- Width: 216 mm (8.5 in.)
- Depth: 606 mm (23.9 in.)

Weight
- Minimum configuration as shipped: 25.0 kg (55 lb)
- Maximum configuration: 29.5 kg (65 lb)

Environment
- Air temperature:
  - System on: 10° to 35°C (50° to 95° F)
  - Maximum altitude: 2134 m (7000 ft)
  - **Note:** The maximum altitude, 2134 m (7000 ft), is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.
- Humidity:
  - System on: 8% to 80%
  - System off: 8% to 80%

Electrical input
- Input voltage:
  - Low range:
    - Minimum: 90 V ac
    - Maximum: 137 V ac
    - Input frequency range: 57–63 Hz
    - Voltage switch setting: 115 V ac
  - High range:
    - Minimum: 180 V ac
    - Maximum: 265 V ac
    - Input frequency range: 47–53 Hz
    - Voltage switch setting: 230 V ac
- Input kilovolt-amperes (kVA) (approximate):
  - Minimum configuration as shipped: 0.52 kVA
  - Maximum configuration: 1.50 kVA

Note: Power consumption and heat output vary depending on the number and type of optional features installed and the power management optional features in use.

Heat output (approximate in British thermal units (Btu) per hour:
- Minimum configuration: 341 Btu/hr (100 watts)
- Maximum configuration: 2385 Btu/hr (700 watts)

Airflow
- Approximately 0.56 cubic meters per minute (20 cubic feet per minute) maximum

Acoustical noise-emission values
- Average sound-pressure levels:
  - At operator position:
    - Idle: 43 dBA
    - Operating: 45 dBA
  - At bystander position - 1 meter (3.3 ft):
    - Idle: 39 dBA
    - Operating: 40 dBA
- Declared (upper limit) sound-power levels:
  - Idle: 5.3 bels
  - Operating: 5.5 bels

Note: These levels were measured in controlled acoustical environments according to the procedures specified by the American National Standards Institute (ANSI) S12.10 and ISO 7779 and are reported in accordance with ISO 9296. Actual sound-pressure levels in a given location might exceed the average values stated because of room reflections and other nearby noise sources. The declared sound-power levels indicate an upper limit, below which a large number of computers will operate.

Chapter 4. Power supply

The IntelliStation Z Pro Type 6866 computer uses a 490-watt power supply. This power supply provides power for the Pentium III Xeon microprocessor, core chip set, and PCI adapters. Also included is an auxiliary 5-volt (AUX 5) supply to provide power to power-management circuitry and the Wake on LAN feature. The power supply converts the ac input voltage into five dc output voltages and provides power for the following:

- System board
- Memory card
- Adapters
- Internal drives
- Keyboard and auxiliary devices
- USB devices

A logic signal on the power connector controls the power supply; the front panel switch is not directly connected to the power supply.

The power supply connects to the system board with a 2-pin by 10-pin connector and a 2-pin by 7-pin connector, and to the memory card with a 2-pin by 8-pin connector.

Power input

The following table shows the power-input specifications. The power supply automatically selects the correct input voltage.

Table 4. Power input requirements

Specification	Measurements
Input voltage, low range	90 (min) to 137 (max) V ac
Input voltage, high range	180 (min) to 265 (max) V ac
Input frequency	50 Hz ± 3 or 60 Hz ± 3 Hz

Power output

The power supply outputs shown in the following figure include the current-supply capability of all the connectors, including system board, DASD, PCI, and auxiliary outputs.

Table 5. Power output (490 watts)

Output voltage	Regulation	Minimum current	Maximum current
+5 volts	+5% to−4%	1.5 A	44.0 A
+12 volts	+5% to −5%	0.2 A	18.0 A
+3.3 volts	±5%	0.0 A	50.0 A
+2.5 volts	±5%	1.5 A	30.0 A
+5 volts (auxiliary	+5% to -5%	0.005 A	1.20 A

Note: The total combined 3.3 V, 5 V, and 12 V power must not exceed 395 watts.

Component outputs

The power supply provides separate voltage sources for the system board and internal storage devices. The following figures show the approximate power that is provided for specific system components. Many components draw less current than the maximum shown.

Table 6. Keyboard port power

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	275 mA	+5.0% to −4.0%

Table 7. Mouse port power

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	275 mA	+5.0% to –4.0%

Table 8. USB port power

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	500 mA	+5.0% to −4.0%

Output protection

The power supply protects against output overcurrent, overvoltage, and short circuits. See the power supply specifications on “Chapter 4. Power supply” on page 17 for details.

An overload that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply. If this shutdown state occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Internal device connectors

The power supply for the IntelliStation Z Pro Professional Workstation has four 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in “Component outputs”. For connector pin assignments, see “Power supply connectors” on page 33.

Chapter 5. System software

This section briefly describes some of the system software included with the computer.

BIOS

The IntelliStation Z Pro Type 6866 computer uses the IBM basic input/output system (BIOS), which is stored in flash electrically erasable programmable read-only memory (EEPROM). Some of the features of the BIOS are:

- PCI support in accordance with *PCI BIOS Specification 2.2*
- Microsoft PCI IRQ Routing Table
- Plug and Play support in accordance with *Plug and Play Specification 1.1a*
- Wake on LAN support
- Wake on Ring support
- Alert on LAN support
- Asset ID support
- Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP)
- Startable CD-ROM support
- Alternate startup sequence support
- IBM look and feel, such as screen arrangements
- *Advanced Configuration and Power Interface* (*ACPI*) 1.0b
- IDE logical block addressing (LBA) support
- LS 120 support
- Desktop Management (DM) BIOS 2.0 (DMI compliant)
- PC99 compliance

Plug and Play

Support for Plug and Play conforms to the following:

- *Plug and Play BIOS Specification 1.0a*
- *Plug and Play BIOS Extension Design Guide 1.0*
- *Plug and Play BIOS Specification, Errata, and Clarifications 1.0a*
- *Guide to Integrating the Plug and Play BIOS Extensions with system BIOS 1.2*
- Plug and Play kit for DOS and Windows

POST

IBM power-on self-test (POST) code is used. Also, initialization code is included for the on-board system devices and controllers.

POST error codes include text messages for determining the cause of an error. For more information, see the *IntelliStation Z Pro User Guide* or the *IntelliStation Z ProHardware Maintenance Manual*.

Configuration/Setup Utility program

The Configuration/Setup Utility program provides menus for selecting options for devices, I/O ports, date and time, system security, start options, advanced setup, and power management.

More information on using the Configuration/Setup Utility program is provided in *IntelliStation Z Pro User Guide*.

Advanced Power Management (APM)

The IntelliStation Z Pro Type 6866 computer comes with built-in energy-saving capabilities. Advanced Power Management (APM) is a feature that reduces the power consumption of systems when they are not being used. When enabled, APM initiates reduced-power modes for the monitor, microprocessor, and hard disk drive after a specified period of inactivity.

The BIOS supports APM 1.2. This enables the system to enter a power-managed state, which reduces the power drawn from the ac electrical outlet. Advanced Power Management is enabled and controlled through the Configuration/Setup Utility program.

For more information on APM, see *IntelliStation Z Pro User Guide* and *Understanding Your Personal Computer*.

Advanced Configuration and Power Interface (ACPI)

Advanced Configuration and Power Interface (ACPI) BIOS mode enables the operating system to control the power-management features of the computer. Not all operating systems support ACPI BIOS mode. See the operating system documentation to determine if ACPI is supported.

Flash update utility program

The flash update utility program is a stand-alone program to support flash updates. This utility program updates the BIOS code and can change the machine readable information (MRI) to different languages.

The flash update utility program is available at http://www.ibm.com/pc/support on the World Wide Web. Type the machine type and model number in the **Quick Path** field and look for the **Downloadable Files** link. Use the menu choices to narrow the links to the applicable file for your computer.

Diagnostic program

The diagnostic program that comes with the IntelliStation Z Pro computer, IBM Enhanced Diagnostics, is provided on the *Device Driver and IBM Enhanced Diagnostics CD*. It runs independently of the operating system. You can use IBM Enhanced Diagnostics to diagnose and repair problems with the computer. You can download the latest version from http://www.ibm.com/pc/support on the World Wide Web. Type the machine type and model number in the **Quick Path** field and look for the **Downloadable Files** link. Use the menu choices to narrow the links to the applicable file for your computer. For more information on this diagnostic program, see *IntelliStation Z Pro User Guide*.

Chapter 6. System compatibility

This chapter discusses some of the hardware, software, and BIOS compatibility issues that must be considered when designing application programs for the computer.

Hardware compatibility

The functional interfaces are compatible with the following interfaces:

- Intel 8259 interrupt controllers (edge-triggered mode)
- National Semiconductor NS16450 and NS16550A serial communication controllers
- Motorola MC146818 Time of Day Clock command and status (CMOS reorganized)
- Intel 8254 timer, driven from a 1.193 MHz clock (channels 0,1, and 2)
- Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions; the Mode register is partially supported
- Intel 8272 or 82077 diskette drive controllers
- Intel 8042 keyboard controller at addresses hex 0060 and hex 0064
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes
- Parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode

Use this information to develop application programs. Whenever possible, use the BIOS as an interface to hardware to provide maximum compatibility and portability of applications among systems.

Hardware interrupts

Hardware interrupts are level-sensitive for PCI interrupts. The interrupt controller clears the in-service register bit when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI command is sent regardless of whether the incoming interrupt request to the controller is active or inactive.

The interrupt-in-progress latch is readable at an I/O address bit position. This latch is read during the interrupt service routine and might be reset by the read operation or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

With level-sensitive interrupts, the interrupt controller requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler does the following:

1. Clears the interrupt
2. Waits one I/O delay
3. Enables the interrupt through the Set Interrupt Enable Flag command

Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt

hex 0A. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.
2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.
3. When the interrupt occurs, the system microprocessor passes control to IRQ9 (interrupt hex 71) interrupt handler.
4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt hex 0A) interrupt handler.
5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

Hard disk drives and controller

Reading from and writing to the hard disk is initiated in the same way as in IBM Personal Computer products; however, new functions are supported.

Software compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02F*x* or 06F*x*, where *x* is the interrupt level) does not create interference.

Software interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-sensitive programs

Programs can select machine-specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return Configuration Parameters function (AH)=(C0H).

Appendix A. Connector-pin assignments

The following figures show the pin assignments for various system board connectors.

External connectors

The following information shows the pin assignments for external connectors.

Monitor connector

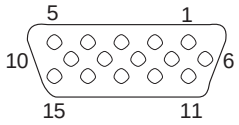


Table 9. Monitor connector-pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Red	O	9	+5 V dc, used by DDC2B	
2	Green	I	10	Ground	
3	Blue	O	11	Monitor ID 0 - not used	
4	Monitor ID 2 - not used	I	12	DDC2B data	I/O
5	Ground		13	Horizontal sync	O
6	Red ground		14	Vertical sync	O
7	Green ground		15	DDC2B clock	I/O
8	Blue ground				

USB port connectors

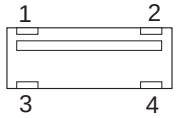


Table 10. USB port connector-pin assignments

Pin	Connector
1	VCC
2	−Data
3	+Data
4	Ground

Keyboard and mouse connectors

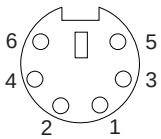


Table 11. Keyboard connector-pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Data	I/O	4	+5 V dc	
2	Reserved	I/O	5	Clock	I/O
3	Ground		6	Reserved	I/O

Table 12. Mouse connector-pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Data	I/O	4	+5 V dc	
2	Reserved	I/O	5	Clock	I/O
3	Ground		6	Reserved	

Serial connector

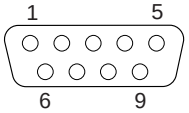


Table 13. Serial connector-pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Data carrier detect	I	6	Data set ready	I
2	Receive data#	I	7	Request to send	O
3	Transmit data#	O	8	Clear to send	I
4	Data terminal read	O	9	Ring indicator	I
5	Ground				

Parallel connector

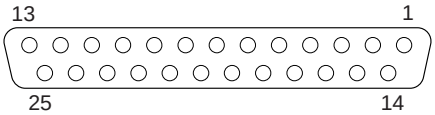


Table 14. Parallel connector-pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	STROBE#	I/O	14	AUTO FD XT#	O
2	Data bit 0	I/O	15	ERROR#	I
3	Data bit 1	I/O	16	INIT#	O
4	Data bit 2	I/O	17	SLCT IN#	O
5	Data bit 3	I/O	18	Ground	
6	Data bit 4	I/O	19	Ground	
7	Data bit 5	I/O	20	Ground	
8	Data bit 6	I/O	21	Ground	
9	Data bit 7	I/O	22	Ground	
10	ACK#	I	23	Ground	

Table 14. Parallel connector-pin assignments (continued)

Pin	Signal	I/O	Pin	Signal	I/O
11	BUSY	I	24	Ground	
12	PE	I	25	Ground	
13	SLCT	I			

Ethernet connector

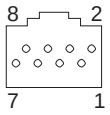


Table 15. Ethernet connector- pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	TxD+	O	5	Ground	
2	TxD−	O	6	RxD−	I
3	RxD+	I	7	Ground	
4	Ground		8	Ground	

MIDI/joystick external connector

The external MIDI/joystick connector attaches to the system board through a signal cable that connects to an internal connector on the system board. The following illustration shows the external connector.

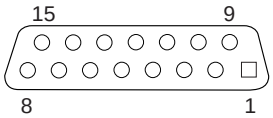


Table 16. MIDI/Joystick external connector-pin assignments

Pin	Signal	Pin	Signal
1	+5 v dc	9	+5 v dc
2	JAB1	10	JBB1
3	JACX	11	JBCX
4	Ground	12	MIDI out
5	Ground	13	JBCY
6	JACY	14	JBB2
7	JAB2	15	MIDI in
8	+5		

Internal connectors

The following figures show the connector-pin assignments for various internal connectors on the system board and memory card.

Diskette drive connector

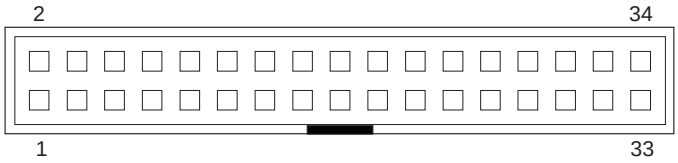


Table 17. Diskette drive connector-pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Ground	I	18	Direction in#	
2	High density select	O	19	Ground	
3	Ground		20	Step#	O
4	Not connected		21	Ground	
5	Ground		22	Write data#	O
6	Data rate 0		23	Ground	
7	Ground		24	Write enable#	O
8	Index#		25	Ground	
9	Reserved		26	Track0#	I
10	Motor enable 0#	O	27	Ground	
11	Ground		28	Write protect#	I
12	Drive select 1#	O	29	Ground	I
13	Ground		30	Read data#	I
14	Drive select 0#	O	31	Ground	
15	Ground		32	Head 1 select#	O
16	Motor enable 1#	O	33	Ground	O
17	N/C	I	34	Diskette change#	I

IDE connectors

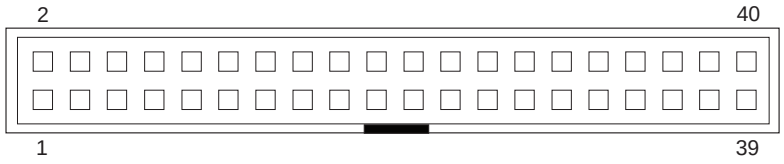


Table 18. IDE connector-pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	N/C	O	21	SDDREQ	
2	Ground		22	Ground	
3	Data bus bit 7	I/O	23	I/O write	O
4	Data bus bit 8	I/O	24	Ground	
5	Data bus bit 6	I/O	25	I/O read	O
6	Data bus bit 9	I/O	26	Ground	
7	Data bus bit 5	I/O	27	I/O channel ready	I

Table 18. IDE connector-pin assignments (continued)

Pin	Signal	I/O	Pin	Signal	I/O
8	Data bus bit 10	I/O	28	Ground	O
9	Data bus bit 4	I/O	29	DMAACK	
10	Data bus bit 11	I/O	30	Ground	
11	Data bus bit 3	I/O	31	IRQ	I
12	Data bus bit 12	I/O	32	CS16#	I
13	Data bus bit 2	I/O	33	SA1	O
14	Data bus bit 13	I/O	34	IDE66 detect	I
15	Data bus bit 1	I/O	35	SA0	O
16	Data bus bit 14	I/O	36	SA2	O
17	Data bus bit 0	I/O	37	CS0#	O
18	Data bus bit 15	I/O	38	CS1	O
19	Ground		39	Active#	I
20	Key (Reserved)		40	Ground	

Memory connectors

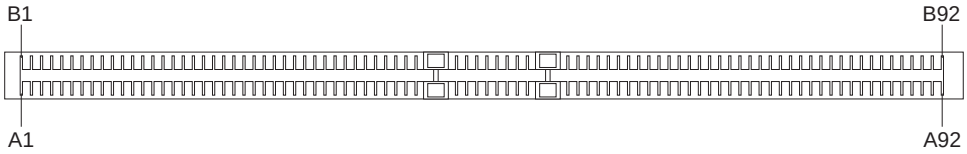


Table 19. System memory connector-pin assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Gnd	B1	Gnd	A47	NC	B47	NC
A2	LDQA8	B2	LDQA7	A48	NC	B48	NC
A3	Gnd	B3	Gnd	A49	NC	N49	NC
A4	LDQA6	B4	LDQA5	A50	NC	B50	NC
A5	Gnd	B5	Gnd	A51	Vref	B51	Vref
A6	LDQA4	B6	LDQA3	A52	Gnd	B52	Gnd
A7	Gnd	B7	Gnd	A53	SCL	B53	SA0
A8	LdQA2	B8	LDQA1	A54	Vdd	B54	Vdd
A9	Gnd	B9	Gnd	A55	SDA	B55	SA1
A10	LDQA1	B10	LCFM	A56	SVdd	B56	SVdd
A11	Gnd	B11	Gnd	A57	SWP	B57	SA2
A12	LCTMN	B12	LCFMN	A58	Vdd	B58	Vdd
A13	Gnd	B13	Gnd	A59	RSCK	B59	RCMD
A14	LCTM	B14	NC	A60	Gnd	B60	Gnd
A15	Gnd	B15	Gnd	A61	RDQB7	B61	RDQB8
A16	NC	B16	LROW2	A62	Gnd	B62	Gnd
A17	Gnd	B17	Gnd	A63	RDQB5	B63	RDQB6
A18	LROW1	B18	LROW0	A64	Gnd	B64	Gnd

Table 19. System memory connector-pin assignments (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A19	Gnd	B19	Gnd	A65	RDQB3	B65	RDQB4
A20	LCOL4	B20	LCOL3	A66	Gnd	B66	Gnd
A21	Gnd	B21	Gnd	A67	RDQB1	B67	RDQB0
A22	LCOL2	B22	LCOL1	A68	Gnd	B68	Gnd
A23	Gnd	B23	Gnd	A69	RCOL0	B69	RDQB0
A24	LCOL0	B24	LDQB0	A70	Gnd	B70	Gnd
A25	Gnd	B25	Gnd	A71	RCOL2	B71	RCOL1
A26	LDQB5	B26	LDQB2	A72	Gnd	B72	Gnd
A27	Gnd	B27	Gnd	A73	RDOL4	B73	RCOL3
A28	LDQB3	B28	LDQB4	A74	Gnd	B74	Gnd
A29	Gnd	B29	Gnd	A75	RROW1	B75	RROW0
A30	LDQB5	B30	LDQB8	A76	Gnd	B76	Gnd
A31	Gnd	B31	Gnd	A77	NC	B77	RROW2
A32	LDQB7	B32	LDQB8	A78	Gnd	B78	Gnd
A33	Gnd	B33	Gnd	A79	RCTM	B79	NC
A34	LSCK	B34	LCMD	A80	Gnd	B80	Gnd
A35	Vcmos	B35	Vcmos	A81	RCTMN	B81	RCFMN
A36	SOUT	B36	SIN	A82	Gnd	B82	Gnd
A37	Vcmos	B37	Vcmos	A83	RDQA0	B83	RCFM
A38	NC	B38	NC	A84	Gnd	B84	Gnd
A39	Gnd	B39	Gnd	A85	RDQA2	B85	RDQA1
A40	NC	B40	NC	A86	Gnd	B86	Gnd
A41	Vdd	B41	Vdd	A87	RDQA4	B87	RDQA3
A42	Vdd	B42	Vdd	A88	Gnd	B88	Gnd
A43	NC	B43	NC	A89	RDQA6	B89	RDQA5
A44	NC	B44	NC	A90	Gnd	B90	Gnd
A45	NC	B45	NC	A91	RDQA8	B91	RDQA7
A46	NC	B46	NC	A92	Gnd	B92	Gnd

32-bit PCI connectors

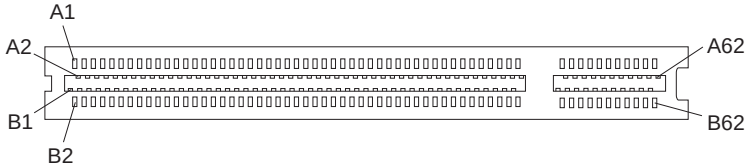


Table 20. PCI connector-pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
A1	TRST#	O	B1	−12 V dc	
A2	+12 V dc		B2	TCK	O

Table 20. PCI connector-pin assignments (continued)

Pin	Signal	I/O	Pin	Signal	I/O
A3	TMS	O	B3	Ground	
A4	TDI	O	B4	TDO	I
A5	+5 V dc		B5	+5 V dc	
A6	INTA#	I	B6	+5 V dc	
A7	INTC#	I	B7	INTB#	I
A8	+5 V dc		B8	INTD#	I
A9	Reserved		B9	PRSNT1#	I
A10	+5 V dc		B10	Reserved	
A11	Reserved		B11	PRSNT2#	I
A12	Ground		B12	Ground	
A13	Ground		B13	Ground	
A14	3.3 V AUX		B14	3.3 V AUX	
A15	RST#	O	B15	Ground	
A16	+5 V dc (I/O)		B16	CLK	O
A17	GNT#	O	B17	Ground	
A18	Ground		B18	REQ#	I
A19	PCI PME		B19	+5 V dc	
A20	Address/data 30	I/O	B20	Address/data 31	I/O
A21	+3.3 V dc		B21	Address/data 29	I/O
A22	Address/data 28	I/O	B22	Ground	
A23	Address/data 26	I/O	B23	Address/data 27	I/O
A24	Ground	I/O	B24	Address/data 25	
A25	Address/data 24	I/O	B25	+3.3 V dc	
A26	IDSEL	O	B26	C/BE 3#	I/O
A27	+3.3 V dc		B27	Address/data 23	I/O
A28	Address/data 22	I/O	B28	Ground	
A29	Address/data 20	I/O	B29	Address/data 21	I/O
A30	Ground	I/O	B30	Address/data 19	
A31	Address/data 18	I/O	B31	+3.3 V dc	
A32	Address/data 16	I/O	B32	Address/data 17	I/O
A33	+3.3 V dc		B33	C/BE 2#	I/O
A34	FRAME#	I/O	B34	Ground	
A35	Ground		B35	IRDY#	I/O
A36	TRDY#	I/O	B36	+3.3 V dc	
A37	Ground		B37	DEVSEL#	I/O
A38	STOP#	I/O	B38	Ground	
A39	+3.3 V dc		B39	LOCK#	I/O
A40	SMBCLK1	I/O	B40	PERR#	I/O
A41	SMBDATA1	I/O	B41	+3.3 V dc	
A42	Ground		B42	SERR#	I/O

Table 20. PCI connector-pin assignments (continued)

Pin	Signal	I/O	Pin	Signal	I/O
A43	PAR		B43	+3.3 V dc	
A44	Address/data 15	I/O	B44	C/BE 1#	I/O
A45	+3.3 V dc	I/O	B45	Address/data 14	I/O
A46	Address/data 13		B46	Ground	
A47	Address/data 11	I/O	B47	Address/data 12	I/O
A48	Ground	I/O	B48	Address/data 10	I/O
A49	Address/data 9		B49	Ground	
A50	Key		B50	Key	
A51	Key		B51	Key	
A52	C/BE(0)#	I/O	B52	Address/data 8	I/O
A53	+3.3 V dc	I/O	B53	Address/data 7	I/O
A54	Address/data 6		B54	+3.3 V dc	
A55	Address/data 4	I/O	B55	Address/data 5	I/O
A56	Ground	I/O	B56	Address/data 3	I/O
A57	Address/data 2		B57	Ground	
A58	Address/data 0	I/O	B58	Address/data 1	I/O
A59	+5 V dc		B59	+5 V dc	
A60	ACK64#	I/O	B60	ACK64#	I/O
A61	+5 V dc		B61	+5 V dc	
A62	+5 V dc		B62	+5 V dc	

64-bit PCI connectors

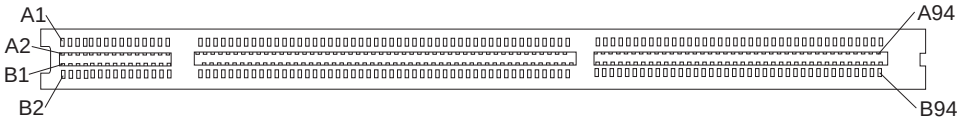


Table 21. 64-bit PCI connector-pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
A1	TRST#	O	B1	−12 V dc	
A2	+12 V dc		B2	TCK	O
A3	TMS	O	B3	Ground	
A4	TDI	O	B4	TDO	I
A5	+5 V dc		B5	+5 V dc	
A6	INTA#	I	B6	+5 V dc	
A7	INTC#	I	B7	INTB#	I
A8	+5 V dc		B8	INTD#	I
A9	Reserved		B9	PRSNT1#	I
A10	+5 V dc		B10	Reserved	
A11	Reserved		B11	PRSNT2#	I

Table 21. 64-bit PCI connector-pin assignments (continued)

Pin	Signal	I/O	Pin	Signal	I/O
A12	Ground		B12	Ground	
A13	Ground		B13	Ground	
A14	3.3 V AUX		B14	3.3 V AUX	
A15	RST#	O	B15	Ground	
A16	+5 V dc (I/O)		B16	CLK	O
A17	GNT#	O	B17	Ground	
A18	Ground		B18	REQ#	I
A19	PCI		B19	+5 V dc	
A20	Address/data 30	I/O	B20	Address/data 31	I/O
A21	+3.3 V dc		B21	Address/data 29	I/O
A22	Address/data 28	I/O	B22	Ground	
A23	Address/data 26	I/O	B23	Address/data 27	I/O
A24	Ground	I/O	B24	Address/data 25	
A25	Address/data 24	I/O	B25	+3.3 V dc	
A26	IDSEL	O	B26	C/BE 3#	I/O
A27	+3.3 V dc		B27	Address/data 23	I/O
A28	Address/data 22	I/O	B28	Ground	
A29	Address/data 20	I/O	B29	Address/data 21	I/O
A30	Ground	I/O	B30	Address/data 19	
A31	Address/data 18	I/O	B31	+3.3 V dc	
A32	Address/data 16	I/O	B32	Address/data 17	I/O
A33	+3.3 V dc		B33	C/BE 2#	I/O
A34	FRAME#	I/O	B34	Ground	
A35	Ground		B35	IRDY#	I/O
A36	TRDY#	I/O	B36	+3.3 V dc	
A37	Ground		B37	DEVSEL#	I/O
A38	STOP#	I/O	B38	Ground	
A39	+3.3 V dc		B39	LOCK#	I/O
A40	SMBCLK1	I/O	B40	PERR#	I/O
A41	SMBDATA1	I/O	B41	+3.3 V dc	
A42	Ground		B42	SERR#	I/O
A43	PAR		B43	+3.3 V dc	
A44	Address/data 15	I/O	B44	C/BE 1#	I/O
A45	+3.3 V dc	I/O	B45	Address/data 14	I/O
A46	Address/data 13		B46	Ground	
A47	Address/data 11	I/O	B47	Address/data 12	I/O
A48	Ground	I/O	B48	Address/data 10	I/O
A49	Address/data 9		B49	Ground	
A50	Key		B50	Key	
A51	Key		B51	Key	

Table 21. 64-bit PCI connector-pin assignments (continued)

Pin	Signal	I/O	Pin	Signal	I/O
A52	C/BE(0)#	I/O	B52	Address/data 8	I/O
A53	+3.3 V dc	I/O	B53	Address/data 7	I/O
A54	Address/data 6		B54	+3.3 V dc	
A55	Address/data 4	I/O	B55	Address/data 5	I/O
A56	Ground	I/O	B56	Address/data 3	I/O
A57	Address/data 2		B57	Ground	
A58	Address/data 0	I/O	B58	Address/data 1	I/O
A59	+5 V dc		B59	+5 V dc	
A60	ACK64#	I/O	B60	ACK64#	I/O
A61	+5 V dc		B61	+5 V dc	
A62	+5 V dc		B62	+5 V dc	
A63	Ground		B63	Reserved	
A64	C/BE[7]#		B64	Ground	
A65	C/BE[5]#		B65	C/BE[6]#	
A66	+3.3 V dc	I/O	B66	C/BE[4]#	
A67	PAR64		B67	Ground	
A68	Address/data 62		B68	Address/data 63	
A69	Ground		B69	Address/data 61	
A70	Address/data 60		B70	+3.3 V dc	I/O
A71	Address/data 58		B71	Address/data 59	
A72	Ground		B72	Address/data 57	
A73	Address/data 56		B73	Ground	
A74	Address/data 54		B74	Address/data 55	
A75	+3.3 V dc	I/O	B75	Address/data 53	
A76	Address/data 52		B76	Ground	
A77	Address/data 50		B77	Address/data 51	
A78	Ground		B78	Address/data 49	
A79	Address/data 48		B79	+3.3 V dc	I/O
A80	Address/data 46		B80	Address/data 47	
A81	Ground		B81	Address/data 45	
A82	Address/data 44		B82	Ground	
A83	Address/data 42		B83	Address/data 43	
A84	+3.3 V dc	I/O	B84	Address/data 41	
A85	Address/data 40		B85	Ground	
A86	Address/data 38		B86	Address/data 39	
A87	Ground		B87	Address/data37	
A88	Address/data 36		B88	+3.3 V dc	I/O
A89	Address/data 34		B89	Address/data 35	
A90	Ground		B90	Address/data 33	
A91	Address/data 32		B91	Ground	

Table 21. 64-bit PCI connector-pin assignments (continued)

Pin	Signal	I/O	Pin	Signal	I/O
A92	Reserved		B92	Reserved	
A93	Ground		B93	Reserved	
A94	Reserved		B94	Ground	

Power supply connectors

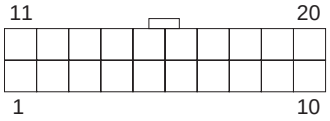


Table 22. Power supply (P1) connector-pin assignments

Pin	Signal name	Pin	Signal name
1	+3.3 V dc	11	+3.3 V dc
2	+3.3 V dc	12	−12 V dc
3	Ground	13	Ground
4	+ 5 V dc	14	On/Off
5	Ground	15	Ground
6	+5 V dc	16	Ground
7	Ground	17	Ground
8	PWR GOOD	18	−5 V dc
9	+5 V dc standby	19	+5 V dc
10	+12 V dc	20	+5 V dc

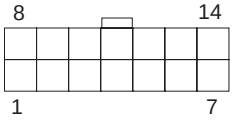


Table 23. Power supply (P2) connector-pin assignments

Pin	Signal name	Pin	Signal name
1	+3.3 v dc	8	Ground
2	+3.3 v dc	9	Ground
3	+3.3 v dc	10	Ground
4	+3.3 v dc	11	Ground
5	+5 v dc	12	Ground
6	+12 v dc	13	+5 v dc
7	System sense	14	System sense

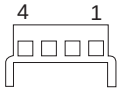


Table 24. Diskette drive power supply (P3) connector-pin assignments

Pin	Signal name	Pin	Signal name
1	+5 v dc	3	Ground
2	Ground	4	+12 v dc

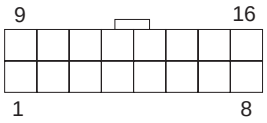


Table 25. Memory card power supply (P4) connector-pin assignments

Pin	Signal name	Pin	Signal name
1	+2.5 v dc	9	Ground
2	+2.5 v dc	10	Ground
3	+2.5 v dc	11	Ground
4	+2.5 v dc	12	Ground
5	+2.5 v dc	13	Ground
6	+2.5 v dc	14	Ground
7	+2.5 v dc	15	Ground
8	System sense	16	System sense

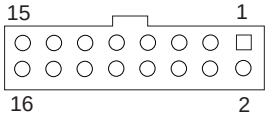


Table 26. IDE device p ower supply (P5, P6, P7, P8, P9, P10, P11, P12) connector-pin assignments

Pin	Signal name	Pin	Signal name
1	+12 v dc	3	Ground
2	Ground	4	+5 v dc

Wake on LAN connector

Table 27. Wake on LAN connector-pin assignments

Pin	Description
1	+5 V dc standby
2	Ground
3	Wake on LAN

Alert on LAN connectors

Table 28. Alert on LAN connector- pin assignments

Pin	Description
1	SMB data

Table 28. Alert on LAN connector- pin assignments (continued)

Pin	Description
2	SMB clock
3	Intrusion

Tamper detection switch

Table 29. Tamper detection switch pin assignments

Pin	Description
1	Tamper switch
2	Ground

Radio frequency ID

Table 30. Radio frequency identification (RFID) pin assignments

Pin	Description
1	RFID Ant 1
2	Key
3	Ground
4	RFID Ant 2

CD audio connector

Table 31. CD audio connector-pin assignments

Pin	Description
1	CD-in Left
2	CD-in Ground
3	CD-in Ground
4	CD-in Right

SCSI/ IDE LED connectors

Table 32. SCSI/IDE LED connector-pin assignments

Pin	Description
1	Not connected
2	to LED
3	to LED
4	Not connected

MIDI/joystick internal connector

The MIDI/joystick internal connector connects to the external connector through a ribbon signal cable. The following illustration shows the internal connector.

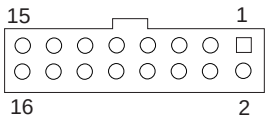


Table 33. MIDI/joystick internal connector-pin assignments

Pin	Signal	Pin	Signal
1	+5 v dc	9	Ground
2	+5 v dc	10	JBCY
3	JAB1	11	JACY
4	JBB1	12	JBB2
5	JACX	13	JBB2
6	JBCX	14	MIDI in
7	Ground	15	+5 v dc
8	MIDI out	16	N/C

SCSI connectors

There are two SCSI connectors on the system board of the IntelliStation Z Pro Type 6866 computer. One SCSI connector attaches to internal drives. The other connector attaches to an external connector on the back of the computer. The internal and external connectors have identical pin assignments.

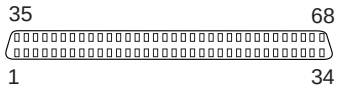


Table 34. SCSI connector pin assignments

Pin	Signal	Pin	Signal
1	+DB (12)	35	−DB (12)
2	+DB (13)	36	−DB (13)
3	+DB (14)	37	−DB (14)
4	+DB (15)	38	−DB (15)
5	+DB (P1)	39	−DB (P1)
6	+DB (0)	40	−DB (0)
7	+DB (1)	41	−DB (1)
8	+DB (2)	42	−DB (2)
9	+DB (3)	43	−DB (3)
10	+DB (4)	44	−DB (4)
11	+DB (5)	45	−DB (5)
12	+DB (6)	46	−DB (6)
13	+DB (7)	47	−DB (7)
14	+DB (P)	48	−DB (P)

Table 34. SCSI connector pin assignments (continued)

Pin	Signal	Pin	Signal
15	GROUND	49	GROUND
16	DIFFSENS	50	GROUND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	RESERVED	53	GROUND
20	GROUND	54	GROUND
21	+ATN	55	−ATN
22	GROUND	56	GROUND
23	+BSY	57	−BSY
24	+ACK	58	−ACK
25	+RST	59	−RST
26	+MSG	60	−MSG
27	+SEL	61	−SEL
28	+C/D	62	−C/D
29	REQ	63	−REQ
30	+I/O	64	−I/O
31	+DB (8)	65	−DB (8)
32	+DB (9)	66	−DB (9)
33	+DB (10)	67	−DB (10)
34	+DB (11)	68	−DB (11)

Appendix B. System address maps

The following charts represent how the hard disk stores different types of information. Address ranges and byte sizes are approximate.

System memory map

The first 640 KB of system board RAM is mapped starting at address hex 00000000. A 256 byte area and a 1 KB area of this RAM are reserved for BIOS data. Memory can be mapped differently if POST detects an error.

Table 35. System memory map

Address range (decimal)	Address range (hex)	Size	Description
0 K – 512 KB	00000 – 7FFFF	512 KB	Conventional
512 K – 639 KB	80000 – 9FBFF	127 KB	Extended conventional
639 K – 640 KB	9FC00 – 9FFFF	1 KB	Extended BIOS data
640 K – 767 KB	A0000 – BFFFF	128 KB	Dynamic video memory display cache
768 K – 800 KB	C0000 – C7FFF	32 KB	Video ROM BIOS (shadowed)
800 K – 896 KB	C8000 – DFFFF	96 KB	PCI space, available to adapter ROMs
896 K – 1 MB	E0000 – FFFFF	128 KB	System ROM BIOS (main memory shadowed)
1 MB – 16 MB	1000000 – FFFFFF	15 MB	PCI space
16 MB – 4096 MB	10000000 – FFDFFFFF	4080 MB	PCI space (positive decode)
	FFFE0000 – FFFFFFFF	128 KB	System ROM BIOS

Input/output address map

The following figure lists resource assignments for the I/O address map. Any addresses that are not shown are reserved.

Table 36. I/O address map

Address (hex)	Size (bytes)	Description
0000 – 000F	16	DMA 1
0010 – 001F	16	General I/O locations, available to PCI bus
0020 – 0021	2	Interrupt controller 1
0022 – 003F	30	General I/0 locations, available to PCI bus
0040 – 0043	4	Counter/timer 1
0044 – 00FF	28	General I/O locations, available to PCI bus
0060	1	Keyboard controller byte, reset IRQ
0061	1	System port B
0064	1	Keyboard controller, CMD/ATAT byte
0070, bit 7	1 bit	Enable NMI
0070, bits 6:0	6 bits	Real-time clock, address
0071	1 byte	Real-time clock, data
0072	1 bit	Enable NMI

Table 36. I/O address map (continued)

Address (hex)	Size (bytes)	Description
0072, bits 6:0	6 bits	RTC address
0073	1 byte	RTC data
0080	1	POST checkpoint register during POST only
008F	1	Refresh page register
0080 – 008F	16	DMA page registers
0090 – 0091	15	General I/O locations, available to PCI bus
0092	1	PS/2 keyboard controller registers
0093 – 009F	15	General I/O locations
00A0 – 00A1	2	Interrupt controller 2
00A2 – 00BF	30	APM control
00C0 – 00DF	31	DMA 2
00E0 – 00EF	16	General I/O locations, available to PCI bus
00F0	1	Coprocessor Error register
00F1 – 016F	127	General I/O locations, available to PCI bus
0170 – 0177	8	Secondary IDE channel
01F0 – 01F7	8	Primary IDE channel
0200 – 0207	8	MIDI/joystick port
0220 – 0227	8	Serial port 3 or 4
0228 – 0277	80	General I/O locations, available to PCI bus
0278 – 027F	8	LPT3
0280 – 02E7	102	Available
02E8 – 02EF	8	Serial port 3 or 4
02F8 – 02FF	8	COM2
0338 – 033F	8	Serial port 3 or 4
0340 – 036F	48	Available
0370 – 0371	2	IDE channel 1 command
0378 – 037F	8	LPT2
0380 – 03B3	52	Available
03B4 – 03B7	4	Video
03BA	1	Video
03BC – 03BE	16	LPT1
03C0 – 03CF	52	Video
03D4 – 03D7	16	Video
03DA	1	Video
03D0 – 03DF	11	Available
03E0 – 03E7	8	Available
03E8 – 03EF	8	COM3 or COM4
03F0 – 03F5	6	Diskette channel 1
03F6	1	Primary IDE channel command port
03F7 (Write)	1	Diskette channel 1 command

Table 36. I/O address map (continued)

Address (hex)	Size (bytes)	Description
03F7, bit 7	1 bit	Diskette disk change channel
03F7, bits 6:0	7 bits	Primary IDE channel status port
03F8 – 03FF	8	COM1
0400 – 047F	128	Available
0480 – 048F	16	DMA channel high page registers
0490 – 0CF7	1912	Available
0CF8 – 0CFB	4	PCI configuration address register
0CFC – 0CFF	4	PCI configuration data register
LPTn + 400h	8	ECP port, LPTn base address + hex 400
OCF9	1	Turbo and reset control register
0D00 – FFFF	62207	Available

DMA I/O address map

The following figure lists resource assignments for the DMA address map. Any addresses that are not shown are reserved.

Table 37. DMA I/O address map

Address (hex)	Description	Bits	Byte pointer
0000	Channel 0, memory address register	00 – 15	Yes
0001	Channel 0, transfer count register	00 – 15	Yes
0002	Channel 1, memory address register	00 – 15	Yes
0003	Channel 1, transfer count register	00 – 15	Yes
0004	Channel 2, memory address register	00 – 15	Yes
0005	Channel 2, transfer count register	00 – 15	Yes
0006	Channel 3, memory address register	00 – 15	Yes
0007	Channel 3, transfer count register	00 – 15	Yes
0008	Channels 0–3, read status/write command register	00 – 07	
0009	Channels 0–3, write request register	00 – 02	
000A	Channels 0–3, write single mas register bits	00 – 02	
000B	Channels 0–3, mode register (write)	00 – 07	
000C	Channels 0–3, clear byte pointer (write)	A	
000D	Channels 0–3, master clear (write)/temp (read)	00 – 07	
000E	Channels 0-3, clear mask register (write)	00 – 03	
000F	Channels 0-3, write all mask register bits	00 – 03	
0081	Channel 2, page table address register	00 – 07	
0082	Channel 3, page table address register	00 – 07	
0083	Channel 1, page table address register	00 – 07	
0087	Channel 0, page table address register	00 – 07	
0089	Channel 6, page table address register	00 – 07	

Table 37. DMA I/O address map (continued)

Address (hex)	Description	Bits	Byte pointer
008A	Channel 7, page table address register	00 – 07	
008B	Channel 5, page table address register	00 – 07	
008F	Channel 4, page table address/refresh register	00 – 07	
00C0	Channel 4, memory address register	00 – 15	Yes
00C2	Channel 4, transfer count register	00 – 15	Yes
00C4	Channel 5, memory address register	00 – 15	Yes
00C6	Channel 5, transfer count register	00 – 15	Yes
00C8	Channel 6, memory address register	00 – 15	Yes
00CA	Channel 6, transfer count register	00 – 15	Yes
00CC	Channel 7, memory address register	00 – 15	Yes
00CE	Channel 7, transfer count register	00 – 15	Yes
00D0	Channels 4–7, read status/write command register	00 – 07	
00D2	Channels 4–7, write request register	00 – 02	
00D4	Channels 4–7, write single mask register bit	00 – 02	
00D6	Channels 4–7, mode register (write)	00 – 07	
00D8	Channels 4–7, clear byte pointer (write)		
00DA	Channels 4–7, master clear (write)/temp (read)	00 – 07	
00DC	Channels 4–7, clear mask register (write)	00 – 03	
00DE	Channels 4–7, write all mask register bits	00 – 03	
00DF	Channels 5–7, 8- or 16-bit mode select	00 – 07	

Appendix C. IRQ and DMA channel assignments

The following figures list the interrupt request (IRQ) and direct memory access (DMA) channel assignments.

Table 38. IRQ channel assignments

IRQ	System resource
NMI	Critical system error
SMI	System-management interrupt for power management
0	Timer
1	Keyboard
2	Cascade interrupt from slave PIC
3	COM2
4	COM1
5	LPT2/audio (if present)
6	Diskette controller
7	LPT1
8	Real-time clock
9	Video, ACPI
10	Available to user
11	Available to user
12	Mouse port
13	Math coprocessor
14	Primary IDE (if present)
15	Secondary IDE (if present)

Note: The default settings for COM 1 (IRQ 4), COM 2 (IRQ 3), and LPT 1 (IRQ 7) can be changed to another IRQ.

Table 39. DMA channel assignments

DMA channel	Data width	System resource
0	8 bits	Open
1	8 bits	Open
2	8 bits	Diskette drive
3	8 bits	Parallel port (for ECP or EPP)
4		Reserved (cascade channel)
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

Appendix D. Error codes

The *IntelliStation Z Pro User Guide*and the *Hardware Maintenance Manual* provide complete lists of error and beep codes.

POST error codes

POST error messages appear when, during startup, POST finds problems with the hardware or a change in the hardware configuration. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages.

Beep codes

Beep codes are a series of tones in sets of two or three that sound when there are POST errors. The beep pattern represents numeric values and provide further information about the location of a potential problem.

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