Intel® Pentium® III Processor/840

Development Kit Manual

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Revision History

Date	Revision	Description
April 2001	003	Updated for 866 MHz Pentium® III processor; BOM format changed; Key components BOM expanded to include all kit components.
April 2000	002	Updated for 733 MHz Pentium® III processor
Feb. 2000	001	First release of this document

About this Manual 1

This manual tells you how to set up and use the evaluation board and processor assembly included in your Intel® Pentium® III processor/840 Development Kit.

1.1 Content Overview

Chapter 1, “About This Manual” - This chapter contains a description of conventions used in this manual. The last few sections tell you how to obtain literature and contact customer support.

Chapter 2, “Getting Started” - This chapter provides complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3, “Theory of Operation” - This chapter provides information on the system design.

Chapter 4, “Hardware Reference” - This chapter provides a description of jumper settings and functions, and pinout information for each connector.

Chapter 5, “BIOS Quick Reference” - This chapter describes how to configure the BIOS for your system. A summary of all BIOS menu options is provided.

Appendix A, “Using Different Processors in the Board” - This appendix provides instructions for installing and using a Pentium III Processor with a 100 MHz processor side bus in your kit.

Appendix B, “Termination Chip for Uniprocessor Systems” - This appendix provides contact information for obtaining a termination chip to insert in an unpopulated processor socket (for uniprocessor designs).

Appendix C, “PLD Code Listing” - This appendix includes a sample code listing for the Post Code Debugger.

Appendix D, “Bill of Materials” - This appendix contains the bill of materials for the evaluation board.

Appendix E, “Schematics” - This appendix contains schematics for selected connectors and subsystems for the evaluation board.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either uppercase or lowercase.
Numbers	Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)
Units of Measure	The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
Kbyte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Technical Support

1.3.1 Electronic Support

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

Product documentation is provided online in a variety of web-friendly formats at: http://developer.intel.com/design/litcentr/index.htm.

1.3.2 Telephone Technical Support

In the U.S. and Canada, technical support representatives are available to answer your questions between 5 a.m. and 5 p.m. PST. You can also fax your questions to us. (Please include your voice telephone number and indicate whether you prefer a response by phone or by fax.) Outside the U.S. and Canada, please contact your local distributor.

1-800-628-8686	U.S. and Canada
916-356-7599	U.S. and Canada
916-356-6100 (fax)	U.S. and Canada

1.4 Product Literature

You can order product literature from the following Intel literature centers.

1-800-548-4725	U.S. and Canada
708-296-9333	U.S. (from overseas)
44(0)1793-431155	Europe (U.K.)
44(0)1793-421333	Germany
44(0)1793-421777	France
81(0)120-47-88-32	Japan (fax only)

1.5 Related Documents

Table 1-1. Related Documents

Document Title	Order Number
Pentium® III Processor for the PGA370 Socket at 500 MHz to 1 GHz datasheet	245264
Intel® Pentium® III Processor Specification Update	244453
Intel® Pentium® III Processor Thermal Design Guide	273325
Intel® 840 Chipset: 82840 Memory Controller Hub (MCH) datasheet	298020
Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub datasheet	290655
Intel® 82802AB/82802AC Firmware Hub (FWH) datasheet	290658
Dual FC-PGA Intel® Pentium® III Processor and Intel® 840 Chipset Design Guide	273332
VRM 8.4 DC–DC Converter Design Guidelines	245335
P6 Family of Processors Hardware Developer's Manual	244001
Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture	243190
Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference	243191
Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide	243192
Intel Processor Serial Number application note	245125

Table 1-2. Related Specifications

Document Title	Location
WTX Workstation System Specification Version 1.02	http://www.wtx.org/
PCI Local Bus Specification Rev. 2.1	*http://www.pcisig.com*
Accelerated Graphics Port Interface Specification Rev. 2.0	*http://www.intel.com/technology/agp/agp_index.htm*
Advanced Configuration And Power Interface Specification Rev. 1.0b	*http://www.intel.com/technology/IAPC/tech.htm*

Getting Started 2

This chapter identifies the Intel® Pentium® III Processor/840 Development Kit's key components, features and specifications, and tells you how to set up the board for operation.

2.1 Overview

The evaluation board consists of a baseboard with two Intel Pentium III processors, the 840 chipset, and other system board components and peripheral connectors.

Note: The evaluation board is shipped as an open system, allowing for maximum flexibility in changing hardware configuration and peripherals. Because the board is not in a protective chassis, the user must observe extra precautions when handling and operating the system.

2.1.1 Baseboard Features

The evaluation board features are summarized below:

- Full support for two Intel® Pentium® III processors with 256 Kbytes of on-die L2 Cache at up to 866 MHz core bus speed. The baseboard supports a 100 or 133 MHz Processor System Bus.
- Intel® 840 chipset:
  - 82840 Memory Controller Hub (MCH)
  - 82801AA I/O Controller Hub (ICH)
  - 82802AB/82802AC Firmware Hub (FWH)
  - 82806AA PCI 64 Hub (P64H)
- 300 or 400 MHz memory interface:
  - Four Rambus RDRAM* (RIMM) connectors
  - Two 64-Mbyte, PC-800 RDRAM RIMMs included
  - Support for up to 2 Gbytes of memory with 256-Mbit technology
- Accelerated Graphics Port (AGP) Support:
  - AGP Interface Specification Rev. 2.0 compliant
  - Backward compatible with the AGP 1.0
  - Single AGP 1X, 2X, 4X, 66 MHz, 3.3 V/1.5 V device support
- Two PCI 64 slots
  - 64-bit, 66 MHz
- Four PCI 32 slots
  - 32-bit, 33 MHz
  - PCI Specification Rev 2.1 compliant

- Integrated on-board Intel® 82559ER LAN controller
  - — Support for Wired for Management (WfM)
  - — 10/100-Mbit Ethernet controller
- Integrated Audio Subsystem
  - — On-board AC'97
  - — Game port and MIDI port
- Flash system BIOS ROM
  - — FWH with security
  - — General Software system BIOS
  - — In-circuit BIOS upgradability
- Legacy I/O support
  - — SMSC LPC47B272 Super I/O Controller
  - — Legacy I/O ports
- Supports the Advanced Configuration and Power Interface (ACPI) 1.0 specification (S1, S3 and S5 power states only)
- Supports the Advanced Power Management (APM) 1.2 specification
- Plug-in voltage regulator module (VRM) connectors
- In-target probe (ITP) connector to interface to an ITP debugger

Note: Note: the ITP connector used on this board requires a 1.5 V supply voltage

- Integrated WTX form factor
- User-accessible on-board connectors include:
  - — Four RDRAM* RIMM connectors. Note that the evaluation board does not support SDRAM.
  - — Two serial RS-232 ports (COM1, COM2)
  - — One EPP/ECP parallel port
  - — PS/2-style (6-pin mini-DIN) keyboard and mouse connectors
  - — Two Universal Serial Bus (USB) ports
  - — Two IDE bus connectors
  - — One floppy connector
  - — Two PCI 64 expansion slots and four PCI 32 expansion slots
  - — One AGP connector
  - — Standard WTX power supply connectors
  - — RDRAM DC to DC Voltage Regulator Module
  - — ITP port
  - — On board 82559ER Ethernet LAN controller
  - — Audio jacks — Audio MIC, Audio line in, Audio line out

  - — Audio Headers — Aux line in, CD audio in
- Miscellaneous features include:
  - — On-board post-code display (Port 80H)
  - — Reset switch and power push button
  - — Stand-off feet for table-top operation
- Debug hooks
  - — SMA header site (for external function generator to drive the CK133-WS clock input)
  - — Jumper to overwrite the Voltage ID (VID) of each processors
  - — Major power supply voltage test points
  - — Clear CMOS jumper
  - — Single or dual processing ITP mode jumper

2.2 Included Hardware

- Evaluation board (baseboard)
- Two Intel® Pentium® III processors at 866 MHz with 133 MHz processor system bus
- Attached fansinks
- Two VRM 8.4 modules for processor voltage regulation
- Two 64-Mbyte, PC-800 RDRAM RIMMs
- Two Continuity RIMM modules
- One DC-to-DC voltage regulator module for memory subsystems voltage regulation
- PCI video graphics adapter
- 4.3-Gbyte hard disk drive pre-loaded with a target copy of Microsoft Windows* NT Embedded distributed by VenturCom
- IDE cable for the hard disk drive
- WTX power supply
- Mounting hardware

2.3 Software Key Features

The software in the kit was chosen to facilitate development of real-time applications based on the components used on the evaluation board. The software tools included in your kit are described in this section.

Refer to the letter included in your kit for up-to-date information on other vendors offering development software for this kit.

Note: Software in the kit is provided free by the vendor and is licensed only for evaluation purposes. Refer to the documentation in your evaluation kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using the tools that work with Microsoft products must have licensed those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third party vendors.

2.3.1 Embedded BIOS* for the Intel® Pentium® III Processor/840 Development Kit

The Intel Pentium III Processor/840 Development Kit ships pre-installed with Embedded BIOS* pre-boot firmware from General Software. Embedded BIOS provides an industry-standard BIOS platform to run any standard operating system, including DOS*, Windows* NT, NT Embedded*, Windows 95/98, Windows CE, QNX*, VxWorks*, and Linux*, among others. The Embedded BIOS Adaptation Kit (available separately) includes complete source code, a reference manual, and a Window's-based expert system, BIOStart* to enable easy and rapid configuration of customized firmware for your Intel Pentium III processor/840 development kit.

The following features of Embedded BIOS have been enabled in the Intel Pentium III Processor/840 Development Kit:

- SMP BIOS supports dual Pentium III processors (up to 866 MHz)
- RDRAM detection, configuration, and initialization with ECC
- Intel 840 chipset (MCH, ICH, and P64H) configuration
- Firmware Hub with security
- POST codes displayed to POST code monitor
- Two serial ports, one EPP/ECP parallel port
- PCI bus and device enumeration and configuration
- AGP configuration and initialization
- SMC LPC Super I/O programming
- Integrated Debugger
- Burn-In Diagnostics
- Console Redirection
- Manufacturing Mode

2.3.2 Microsoft Windows Embedded NT

While the business world welcomed Windows NT into their MIS and IT environments, Microsoft introduced Windows NT as an embedded operating system. Target Designer*, a new tool from Microsoft, enables Windows NT to be scaled for embedded applications. Target sizes can range from 10 Mbytes to 30 Mbytes. Although not small by most embedded standards, Embedded NT can be well suited to many demanding applications.

A relatively small footprint alone is not enough to allow Windows NT to address the demands of the control application world. But the attraction of a powerful, ubiquitous, general-purpose operating system is creating demand for Windows NT for use in industrial automation computing. Windows NT, as a platform to build on, fosters continuous improvement and leverages the skills of the average user. For automation system designers, Windows NT makes it easy to add tasks, improve the system incrementally, and upgrade different components at different times.

Windows NT includes significant and unique features. These include: RAM based operation (no disk based page file), ROM booting and CD ROM booting, Headless operation (no keyboard, mouse, or display), and remote administration. Windows Embedded NT also supports the VenturCom RTX scheduling enhancements for Real-time and deterministic application performance.

An embedded system developer would use Target Designer to configure a device-specific OS using Windows NT binaries, embedded-enabling technologies and an application. If necessary, Component Designer* is used to create reusable components that were not included in the product (i.e., some device drivers, applications, etc.) Once created, new components can be imported into Target Designer where they can then be incorporated into the device OS. Once an OS has been configured in Target Designer, dependencies are checked and a runnable image is produced which can then be loaded onto the device.

The target image provided was created with Target Designer based on a “standard” configuration model, with optimized drivers for the on-board Ethernet controller and the add-in PCI video adapter on the Intel Pentium III processor/840 evaluation board. Also included on the target image is VenturCom’s Platform Evaluator, a real-time performance evaluation tool for Windows NT and Windows NT Embedded. The sample image is a semi-functional Microsoft Windows NT system, which contains enough NT components to adequately provide a basic functional system with a keyboard, mouse, CD-ROM, floppy, COM ports, PCI graphic card and the on-board networking. The created image provides the following components:

- Workstation system with a uniprocessor or a multiprocessor HAL
- Storage device support for floppy, fixed disk, CD-ROM, and file system support (NTFS, FAT, and CDFS)
- SCSI support — USB support, parallel ports, RDRAM, etc.
- COM1/COM2 serial ports and LPT1 parallel port support
- Networking support for TCP/IP and workgroup participation
- Windows Explorer

Note: The graphics and network interface card drivers are for the add-in video card included in your kit and the on-board Ethernet controller.

VenturCom’s Platform Evaluator* application is also provided and is an easy-to-use tool for determining the right hardware platform for your real-time application. It allows you to vary the system loads, select the measurement criteria, and determine an accurate measurement of the real-

time capabilities of any reference platform. Performance measurements and related configuration information is tracked and saved for comparison purposes. Hardware selection for RTX-based applications can easily be performed by System Integrators, OEMs, and Developers. Users who often need to test one or more computers to evaluate the real-time performance that can be delivered for an RTX application will benefit from the easy to use controls. Platform Evaluator, while making the test cases easy to perform, also summarizes the test results and logs them to a simple text file. Real-time response can vary dramatically between what may appear to be similar hardware platforms.

Platform Evaluator is a standard tool for comparing hardware and software configurations in a simple and accurate manner which:

- Measures and displays timing statistics:
  - — Timer response latencies
  - — Thread context switch times
  - — Critical Win32 call execution times
- Evaluates Win32 API performance
- Offers basic loads for evaluating the suitability of device drivers
- Graphically and numerically displays performance results
- Collects hardware and Windows system configuration information

2.4 Before You Begin

Before you set up and configure your evaluation board, you may want to gather some additional hardware.

VGA Monitor	You can use any standard VGA or multi-resolution monitor. The setup instructions in this chapter assume that you are using a standard VGA monitor.
Power Supply	You must use a WTX-type PC power supply. One has been provided with your development kit for added convenience.
Keyboard	You need a keyboard with a PS/2-style connector or adapter.
Mouse	Optional. You can use a mouse with a PS/2-style connector or adapter.
Floppy Drives	You can connect up to two floppy drives to the evaluation board. You must provide the floppy drives and cables; they are not included in the evaluation kit.
Hard Drives and/or CD-ROM	You can connect up to four IDE drives to the evaluation board. Two devices (master and slave) can be attached to each IDE connector. Only one hard drive is included in your kit so you will need to provide the cables for any additional drives. You can have all of these storage devices attached to the board at the same time.
Video Adapter	You can use the video adapter supplied with your kit, or another adapter. The evaluation board supports AGP and PCI video cards.

Network Adapter An Intel 82559ER Ethernet controller is integrated into the baseboard design. You may use a different network card (not included in the kit) however, you are responsible for installing the correct drivers for such a network card. The evaluation board supports all standard PCI compatible network cards.

No network cable is provided. You will need a network cable to connect to your network.

Other Devices and Adapters The evaluation board behaves much like a standard desktop computer board. Most PC compatible peripherals can be attached and configured to work with the evaluation board.

Uni-Processor Configuration The evaluation board is by default shipped to operate in a dual-processor configuration. If your application is designed for uni-processor (UP) operation then it will simply not take advantage of the second processor. In this case the secondary processor is not recognized by your application/ OS. Even if you are taking advantage of only one processor, **do not remove the secondary processor** from the processor Socket 370 labeled P1. Either a processor or a termination chip is required at all times for proper signal termination. See Appendix B, “Termination Chip for Uniprocessor Systems” for additional information.

2.5 Setting up the Evaluation Board

Once you have gathered the hardware described in the last section, follow the steps below to set up your evaluation board. This manual assumes you are familiar with the basic concepts involved in installing and configuring computer hardware. Refer to Figure 2-1 for locations of connectors, jumpers, etc.

Note: Connecting the wrong cable or reversing the cable can damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

1. Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electro-static discharge damage; such damage may cause product failure or unpredictable operation.
2. Inspect the contents of your kit. Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Figure 2-1. Evaluation Board Jumpers

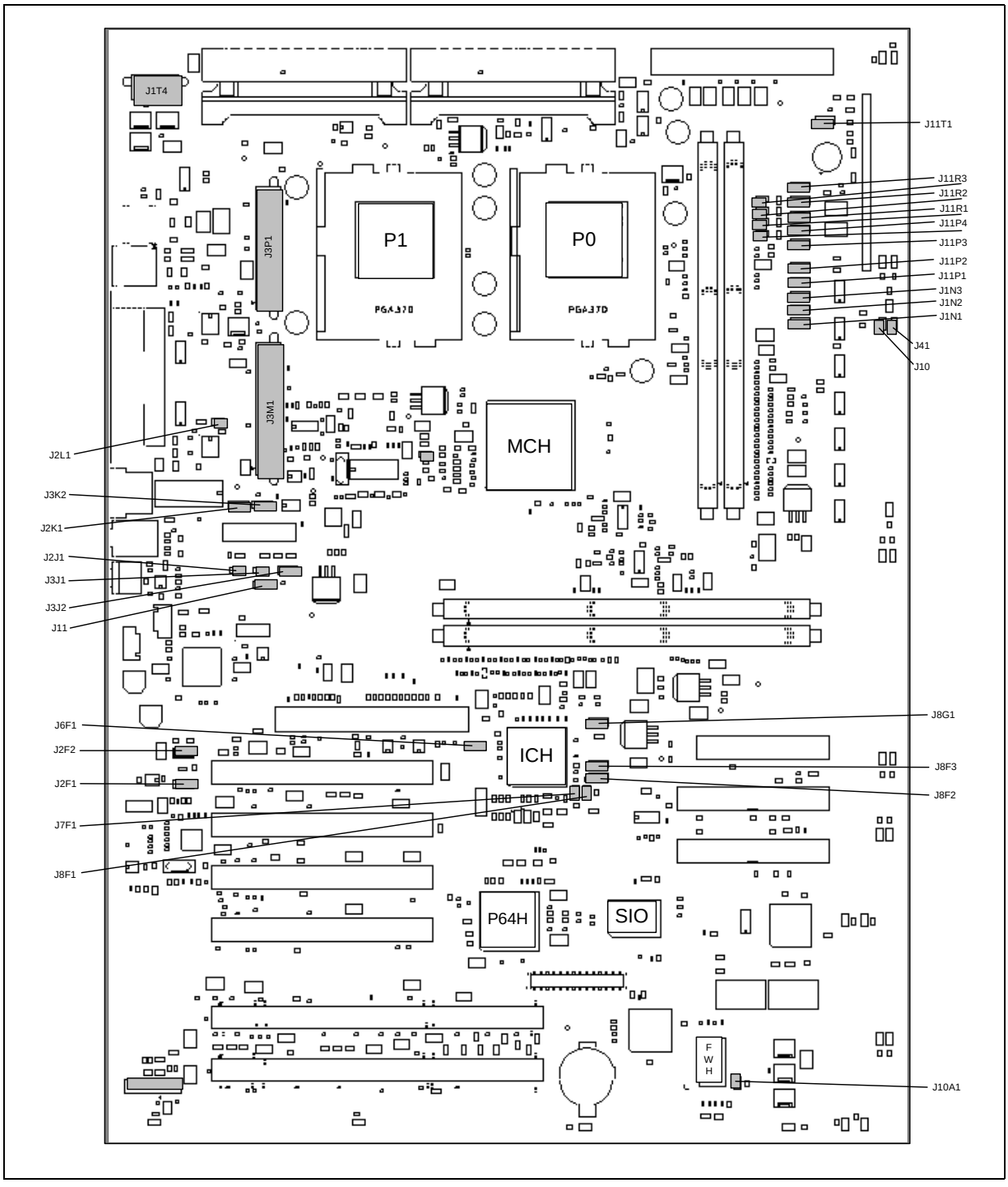
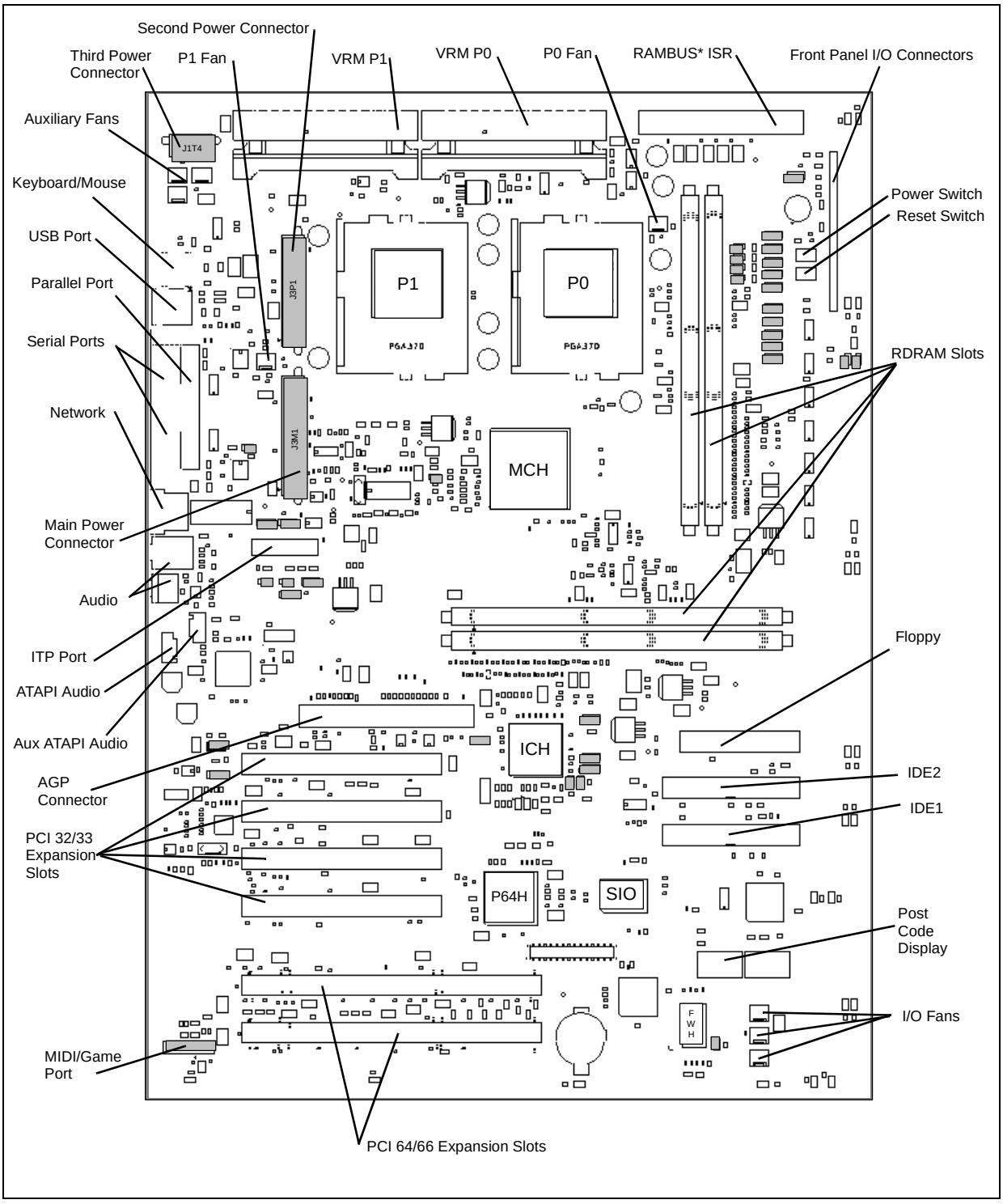


Figure 2-2. Evaluation Board Connectors



3. Check the jumper settings:
   Make sure the board's jumpers are set to the default locations shown in Table 2-1:

Table 2-1. Default Jumper Settings

Jumper	Connection
J10	OUT
J42	OUT
J11	2-3
J2L1, J2K1	OUT, OUT
J6R2	OUT
J2F1	1-2
J7F1	OUT
J8F1	IN
J6F1	1-2
J10A1	IN
J11T1	2-3
J11N1	1-2
J11N2	1-2
J11P2	1-2
J11P1	1-2
J11N3	2-3
J11P4	1-2
J11P3	1-2
J11R3	1-2
J11R2	1-2
J11R1	2-3

4. Mount the hardware:

- Table-top Operation: The evaluation board is shipped with standoff feet for use in a table-top environment. These feet are installed on the evaluation board to raise it off the table surface. Your kit contains a bag of mounting hardware with 13 screws, 13 standoff feet, and 13 washers. It is recommended that you install all 13 screws, standoffs, and washers to ensure proper support across the baseboard.
  - — To mount the ten standoff feet, insert a washer onto a screw, then push the screw through the top of the board. From below the board, thread one of the standoff feet onto the screw.
  - — It is recommended that you install the mounting hardware in the mounting hole locations listed below. This is to ensure an even support to the baseboard:
    A1, A7, A12, F1, F11, M2, K9, H3, U1 and T11, G11, M11, D2
    (Refer to the grid labeled on the baseboard to find the above locations).
- The evaluation board is a standard WTX form factor. A WTX chassis may be used to install the board if a protected environment is desired.

5. Connect storage devices:

   Connect the desired storage devices to the evaluation board: The evaluation board supports Primary and Secondary IDE interfaces that can each host one or two devices (master/slave). When you are using multiple devices, such as a hard disk and a CD-ROM drive, make sure the hard disk drive has a jumper in the master position and the CD-ROM has a jumper in the slave position. When using a single IDE device with the evaluation board, ensure that the jumpers are set correctly for single drive operation. For jumper settings for different configurations, consult the drive's documentation.

Note: The evaluation board BIOS only supports hard drives of 16 Gbytes or less.

Note: The hard disk is already formatted and is pre-loaded with a customized target image of Microsoft Windows Embedded NT Operating System distributed by VenturCom. You may have to make changes to the system BIOS to enable this hard disk. See Chapter 5, "BIOS Quick Reference" for more information.

- Install the IDE hard disk drive included in your kit:
  - — Connect the hard drive's IDE cable connector to the J10E1 connector on the evaluation board. Be sure to align Pin 1 of the cable connector with pin 1 of J10E1.
  - — Connect the other end of the cable to the hard disk drive.
  - — Connect the power cable to the hard drive.

Caution: Make sure the tracer on the ribbon cable is aligned with pin 1 on both the hard disk and the IDE connector header. Connecting the cable backwards can damage the evaluation board or the hard disk.

  - — Connect the power supply to the hard drive.

6. Connect a floppy drive (optional):

- Insert floppy cable into J10F2 (be sure to orient Pin 1 correctly).
- Connect the other end of the ribbon cable to the floppy drive.
- Connect a power cable to the floppy drive.

Note: You must make changes to the system BIOS to enable this floppy disk drive. See Chapter 5, "BIOS Quick Reference" for more information.

7. Connect the keyboard and mouse:

   Connect a PS/2 mouse and keyboard to their respective connectors. See Figure 2-1 for connector locations. J1P2 (on the baseboard) is a stacked PS/2 connector. The bottom connector is for the mouse and the top is for the keyboard. See Figure 3-2 for the correct connector.

8. Connect the Ethernet adapter (optional):

   Connect the network cable (not included) to the LAN port, J1K2, on the evaluation board. Ensure that the jumper J2F1 is set to 1-2 position in order to enable the on-board 82559ER LAN controller.

9. Connect the Audio (Optional):

   Please note that the Windows NT does not support AC'97.

10. Install the video adapter:

    Insert the PCI video adapter into one of the available PCI slots. Connect the monitor cable to the VGA port on the card.

11. Connect the power supply:

    Connect the WTX power supply provided with the evaluation kit.

    Note: Some WTX power supplies do not have an on/off switch. In this case, ensure that the power supply is unplugged from the wall prior to plugging in the WTX power connectors.

    Connect the power supply cables to the power headers as indicated below:

- Install the P1 connector of the power supply into 'WTX Main Pwr', connector J3M1 on the board.
- Install the P2 connector of the power supply into the 'Aux Power Supply', connector J3P1 on the board.
- Install the P3 connector of the power supply into the 'WTX DIG 12V', connector J1T4 on the board.

12. Power up the board: Turn on the power to the monitor and evaluation board. When the power is on you should see two power-indicator LEDs light up (located next to reset switch, see Figure 2-1). Ensure that the fansinks on both the processors are operating.

- Power Switch: The red push-button switch labeled S11R1 is the power switch to the baseboard. Push it once to turn the power on or off.

  Please note that when the system is powered down using the S11R1 switch, the standby voltages are still present on the board. Power can be completely removed from the board only by removing AC power from the WTX power supply or by removing the WTX power supply connector from the baseboard.

- Reset Switch: The black push-button switch labeled S11P1 is the reset switch. When pushed once, this switch will provide a hard reset to the baseboard.

Note: S11R1 is the power switch that should be used to turn the system on and off. Please note that this switch may be in the on position when you first apply power through the WTX power supply.

2.6 Configuring the BIOS

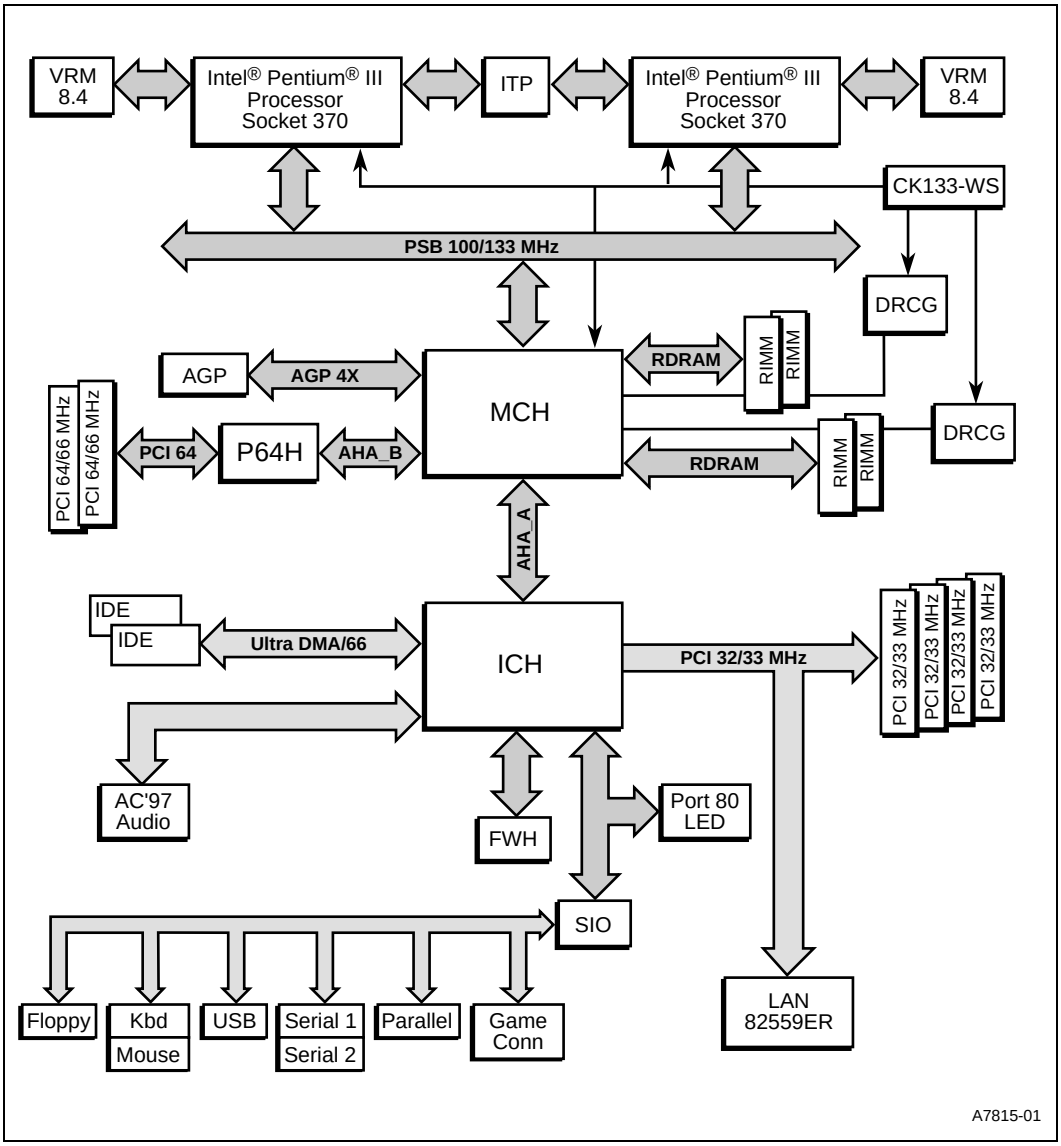
General Software's BIOS is pre-loaded on the evaluation board. You will need to make changes to the BIOS to enable hard disks, floppy disks and other supported features. You can use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface. Chapter 5, "BIOS Quick Reference" contains a description of BIOS options. BIOS updates may periodically be posted to Intel's Developers' web site at:

http://developer.intel.com/design/intarch/devkits

Theory of Operation 3

3.1 Evaluation Board Block Diagram

Figure 3-1. Pentium® III Processor/840 Evaluation Board Block Diagram



3.2 Mechanical Design

The evaluation board conforms to the WTX form factor. For extra protection in a development environment, users may want to install the evaluation board in a WTX chassis. The evaluation board has four 32-bit/33-MHz PCI connectors, two 64-bit/66-MHz PCI connectors, one AGP connector, and four RDRAM RIMM connectors. The I/O connectors reside in the defined WTX I/O window.

3.3 System Operation

The Intel® Pentium® III processor/840 evaluation board is a full-featured system board with two Pentium III processors with 256 Kbytes of on-die L2 cache in a PGA370 socket, and the Intel 840 Chipset. The supported core and processor side bus frequencies are up to 866 MHz/133 MHz. The 840 chipset includes the MCH, ICH, P64H and the FWH. The board also supports RDRAM and other system and I/O peripherals.

In addition, the evaluation kit supports other horizontal technologies from Intel that are commonly used in customer applications. These include 82559ER Ethernet controller (on board) and an add-in PCI video adapter.

3.3.1 Pentium® III Processor

The Pentium III processor/840 evaluation board is designed to support two Pentium III processors at 866/133 MHz with 256-Kbyte on-die L2 Cache, 32-Kbyte L1 instruction and data caches in the Flip Chip – Pin Grid Array (FC-PGA) package.

The Pentium III processor is the next member of the P6 family, in the Intel IA-32 processor line. Like the Pentium II processor, the Pentium III processor implements the Dynamic Execution microarchitecture - a unique combination of multiple branch prediction, data flow analysis, and speculative execution. This enables these processors to deliver higher performance than the Pentium processor, while maintaining binary compatibility with all previous Intel Architecture processors. The Pentium III processor also executes MMX™ technology instructions for enhanced media and communication performance just as its predecessor, the Pentium II processor. The Pentium III processor executes Internet Streaming SIMD Extensions for enhanced floating-point and 3-D application performance. The Pentium III processor extends the concept of processor identification with the addition of a processor serial number. Refer to the *Intel Processor Serial Number* application note (order number 245125) for more detailed information. The Pentium III processor utilizes multiple low-power states such as Auto HALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

3.3.2 On-Board Voltage Regulators

The Pentium III processor/840 evaluation board has up to seven types of on-board voltage regulators that support all required voltages.

- Two voltage regulator modules that are compliant with the VRM 8.4 specification.
- 1.5 V (GTL, Processor CMOS pull up)
- 2.5 V (Direct-RDRAM, ICH, CK133-WS)
- 1.8 V (RSL termination, MCH, AHA)

- 3.3 V/1.5 V (AGP, I/O Signals)
- 3.3 V standby
- 5 V I/O

3.3.2.1 Voltage Regulator Module (VRM)

Processors require many different voltage levels to operate properly. Voltage regulators are used to convert the voltage supplied by the power source to levels usable by the processor. The Voltage Regulator Module (VRM 8.4) is a voltage regulator that plugs into the motherboard, instead of being integrated into the design.

3.3.3 840 Chipset

The Intel 840 chipset supports the Pentium III processor architecture and it utilizes the new modular design of the 800 family of chipsets. Like other 800 series chipsets, the 840 chipset has three core components:

- Memory Controller Hub (MCH)
- I/O Controller Hub
- Firmware Hub (FWH)

In addition to providing high performance, the Intel 840 chipset was designed for scalability. Three components may be used with the core components listed above:

- The 64-bit PCI Controller Hub (P64H)
- RDRAM-based Memory Repeater Hub (MRH-R). The MRH-R is *not* implemented on this board.
- SDRAM-based Memory Repeater Hub (MRH-S). This board does *not* support SDRAM, and the MRH-S is not implemented.

The following features of the Intel 840 Chipset help maximize its performance.

- Dual memory channels, operating in lock-step, provide up to 3.2 Gbyte/s of either RDRAM or SDRAM (Repeater Hub required) memory bandwidth.
- A 16-bit wide implementation of Accelerated Hub Architecture allows high performance concurrent PCI I/O with a P64H.
- The Direct AGP port provides up to 1 Gbyte/s of graphics bandwidth.
- Supports processors using a 100/133-MHz system bus.
- A prefetch cache, unique to the Intel 840 chipset, allows highly efficient data flow and helps maximize system concurrency.

3.3.3.1 Memory Controller Hub (MCH)

The Memory Controller Hub (MCH) differentiates the Intel 840 chipset from other Intel 800 series chipsets. The MCH provides graphics support for AGP 1X/2X/4X, dual RDRAM memory channels, and multiple PCI segments for high performance I/O.

MCH features:

- 544-pin micro Ball Grid Array (micro-BGA) package
- Supports 32- or 36-bit host bus addressing
- 8-deep in-order-queue
- ECC protection on PSB data signals
- Parity protection on address and response signals
- Dual Direct RDRAM channels in lock step
- AGP 2.0 graphics port capable of 1X/2X/4X transfers
- 266-Mbyte/s AHA_A interface to ICH
- 533-Mbyte/s AHA_B interface between MCH and P64H
- ACPI 1.0 and APM 1.2 compliant

3.3.3.2 I/O Controller Hub (ICH)

The I/O Controller Hub (ICH) utilizes Intel Accelerated Hub Architecture to make a direct connection to the MCH. The ICH supports 32-bit PCI, IDE controllers and dual USB ports. The ICH is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of the functions needed in today's applied computing platforms. The ICH communicates with the host controller over a dedicated hub interface. There are two versions of the ICH (82801AA: ICH and 82801AB: ICH0). This provides added flexibility in designing cost-effective system solutions. These devices are pin-compatible and are in 241-pin packages. This evaluation kit implements the 82801AA version of the ICH.

ICH features:

- 241-pin BGA package
- IDE Accelerator supports four independent IDE devices
- Dual channel Fast IDE interface, supports mode 4 and Ultra DMA drives; also supports DMA bus mastering drives and ATAPI CD-ROMs.
- Dual Universal Serial Bus channels
- 5 V PCI interface, Rev 2.2 compliant
- Supports up to six PCI masters
- LPC Bus Support
- Integrated system power management supporting APM 1.2 and ACPI 1.0
- Integrated Real Time Clock
- CMOS battery-backed RAM, 128 bytes
- Nine Dedicated GPIO bits, 20 Multiplexed GPIO bits

3.3.3.3 Firmware Hub (FWH)

Firmware Hub (FWH) stores system BIOS and video BIOS, as well as an Intel Random Number Generator (RNG). The Intel RNG provides truly random numbers to enable stronger encryption, digital signing and security protocols. The FWH is key to enabling future security and manageability infrastructures for the applied computing platform.

3.3.3.4 The 64-bit PCI Controller Hub (P64H)

The 64-bit PCI Controller Hub (P64H) supports 64-bit PCI slots at speeds of either 33 or 66 MHz. The P64H connects directly to the MCH using Intel Accelerated Hub Architecture, providing a dedicated path for high performance I/O. The Intel 82806AA PCI-64 Hub (P64H) is a multi-function PCI device that provides a PCI bridging function and an I/O Advanced Peripheral Interrupt Controller (APIC) function. The P64H is an integral part of the Intel 840 chipset and has been implemented in this evaluation board design.

3.3.3.5 RDRAM-based Memory Repeater Hub (MRH-R)

For systems needing high RDRAM capacity, an RDRAM-based memory repeater hub (MRH-R) may be utilized. The MRH-R converts each memory channel into two memory channels for expanded memory capacity. MRH-R has not been implemented in this evaluation board.

3.3.3.6 SDRAM-based Memory Repeater Hub (MRH-S)

For systems needing high SDRAM capacity, an SDRAM-based memory repeater hub (MRH-S) may be utilized. The MRH-S efficiently translates the RDRAM protocol into SDRAM-based signals for system memory flexibility. The Pentium III processor/840 Development Kit does not provide support for SDRAM and the MRH-S has not been implemented on the evaluation board.

3.3.4 System Memory RDRAM

The MCH on the evaluation board provides support for RDRAM.

Memory features include:

- Up to 1 Gbyte with 128-Mbit technology
- Up to 2 Gbyte with 256-Mbit technology
- Dual Lock Step Direct RDRAM channel
- Maximum 32 RDRAM-D devices per channel
- SPD driven configuration of the 840 chipset for optimal memory operation
- Support for ECC single- and multiple-bit detection (single- or double-bit correction), using ECC RIMMs (ECC can be disabled via BIOS set-up).
- Empty RIMM slots require a continuity RIMM card, (C-RIMM).

Both banks of memory must have identical configurations. A slot in bank 0 must have the same size RIMM as the corresponding slot in bank 1. This is due to the lockstep feature, which means the MCH reads and writes data to each bank simultaneously.

3.3.5 Boot ROM

The system boot ROM installed at U10B1 is the Intel E82802AC Firmware Hub. The system is set up for in-circuit reprogramming of the BIOS (using BIOS update software), but the FWH is also socketed. This device is addressable on the LPC bus off of the ICH.

3.3.6 Expansion Slots and I/O Connectors

The evaluation board has the following expansion slots and I/O connectors:

- One AGP 4x slot
- Two PCI 64/66 slots
- Four PCI 32/33 slots
- AC97 audio jacks (LI, LO, MIC)
- On-board LAN connector
- Single Floppy connector
- Serial Ports
- One Parallel Port
- Two USB Ports
- IDE Ports
- PS/2 Keyboard and mouse ports

3.3.7 AGP Connector

AGP support is provided through the 82840 MCH. One industry standard 1.5 V/3.3 V AGP connector (J4G1) is provided on the evaluation board.

AGP Features include:

- AGP 1x, 2x, and 4x transfer rates
- AGP 2x/4x Fast Write Protocol
- 32-deep AGP request queue

AGP add-in cards must comply with the Rev. 2.0 *Accelerated Graphics Port Specification.*

3.3.8 64-Bit/66-MHz PCI Connectors

Two industry standard 64-bit, 5V/3.3 V PCI connectors (J4A1 & J4B1) are provided on the evaluation board.

3.3.9 32-Bit/33-MHz PCI Connectors

Four industry standard 32-bit, 5 V/3.3 V PCI connectors (J4D1, J4D2, J4E1 & J4F1) are provided on the evaluation board.

3.3.10 Audio Subsystem

The evaluation board has an integrated (on-board) AC'97-compliant audio subsystem, including three analog line-level stereo inputs for connection from LINE IN, CD, AUX.

Audio Subsystem features:

- Microphone input (back panel)
- Stereo line-level (1.7 Vrms) output
- Power management support

3.3.11 Speaker

Integrated low-cost Piezo speaker (stuffing option for 8 ohm chassis speaker).

3.3.12 82559ER LAN Controller

The evaluation board has an integrated (on-board) 82559ER LAN Controller.

82559ER Features:

- Support of Wired for Management (WfM)
- 10/100-Mbit Ethernet controller

3.3.13 Legacy I/O

Support for legacy I/O functions is provided by the SMSC Super I/O controller.

3.3.14 Floppy Drive Support

Floppy disk drive support is provided by the SMSC Super I/O controller. One 34-pin floppy connector is provided on the evaluation board.

3.3.15 RS-232 Ports

Two serial I/O ports provided by the SMSC Super I/O controller. Two 9-pin RS232 connectors are provided on a single stacked connector (J1M1 & J1N1).

3.3.16 IEEE 1284 Port

One parallel port connector controlled by the SMSC Super I/O controller device is provided (J1L1).

3.3.17 USB Port

USB support is provided through the ICH and can be used through connector J1P1.

3.3.18 IDE Support

The evaluation board supports both a primary and secondary IDE interface through two 40-pin IDE connectors. The connector labeled IDE1 (J10E1) is the primary interface and the connector labeled IDE2 (J10F1) is the secondary interface.

3.3.19 Keyboard/Mouse

Keyboard and mouse support are provided by the SMSC Super I/O controller. The keyboard and mouse connectors (J1P2) are PS/2-style, 6-pin stacked miniature DIN connectors. The top connector is for the keyboard and the bottom connector is for the mouse.

3.3.20 POST Code Display

The evaluation board has an on-board POST code display. Data from any program that performs an I/O write to 0080H is latched and displayed on the two LEDs (U10C1 and U11C1). During BIOS startup, codes are posted to these LEDs, to indicate what the BIOS is doing. Application programs can post their own data to these LEDs by writing to I/O address 0080H.

3.3.21 Clock Generation

The CK133W devices on the baseboard generate and distribute the clocks used by the entire system.

3.3.21.1 System Clocks

The CK133W, clock synthesizer is the primary source of clock generation for most of the clocks on the baseboard. The following clock groups are found on the Pentium III processor/840 evaluation board.

Host	100 MHz/133 MHz
PCI	66 MHz
PCI	33 MHz
Memory	DRCG - 300 MHz/400 MHz
AHA	66 MHz
USB	48 MHz
LPC	33 MHz
SIO	14 MHz
RTC	32.768 KHz
APIC	16.6 MHz
AC97	24.576 MHz

3.3.22 Interrupt Map

Table 3-1 indicates the IRQ interrupts and corresponding system resources.

Table 3-1. Interrupts and System Resources

IRQ	System Resources
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	Parallel Port (PNP0 option)
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	IRQ2 Redirect
10	Reserved. Not supported
11	Reserved. Not supported
12	On-board mouse port if present, else user available
13	Reserved for math coprocessor
14	Primary IDE if present, else user available
15	Reserved. Not supported

3.3.23 Memory Map

Table 3-2 indicates memory address ranges and corresponding memory size and description.

Table 3-2. Memory Map

Address Range (Hex)	Size (bytes)	Description
100000-8000000	127.25 M	Extended Memory
E0000-FFFFF	128 K	BIOS
C8000-DFFFF		Available expansion BIOS area (Flash disk memory window)
A0000-C7FFF		Off-board video memory and BIOS
9FC00-9FFFF	1K	Extended BIOS Data (movable by QEMM, 386MAX)
80000-9FBFF	127K	Extended conventional
00000-7FFFF	512K	Conventional

3.4 Power Management Features

Two power management modes are supported with a BIOS option: Advanced Configuration and Power Interface (ACPI 1.0) or Advanced Power Management (APM 1.2).

3.4.1 ACPI 1.0 Support

The evaluation board will support the ACPI 1.0 specification with the following features:

- Single power/sleep button user model (Normal switch depress (< 2 s) puts system in sleep mode, 4 seconds or greater switch depress turns system off)
- OS can turn system off (Soft Off feature)
- Suspend all devices that support power down modes
- Fan control for thermals and quiet operation (speeds = On/Off)
- Supports ACPI S0, S1, S3, S5 System States, no S4 Suspend to disk, no S2 for dual-processor designs

3.4.2 ACPI 1.0 System States and Power States

Note: All possible ACPI system states are listed in Table 3-3. Shaded states are not supported on the Pentium III processor/840 evaluation board.

Table 3-3. ACPI 1.0 System States and Power States

Global States	Sleep States	CPU States	Device States	Targeted System Power
G0/S0-working state	N/A	C0-working	D0-working state	Full power> Depends on system config.
G1-sleeping state	S1-CPU stopped	C1-stop grant	D1,D2,D3-device specification specific	5W<power<30W
G1-sleeping state†	S2-Power on suspend	C2-clock stopped	D2,D3-device specification specified	Not supported
G1-sleeping state	S3-Suspend to RAM. Context saved to disk.	No power	D3-no power except for wake-up logic	5W<power††
G1-sleeping state†	S4BIOS-Suspend to disk. Context saved to disk.	No power	D3-no power except for wake-up logic	Not supported
G2/S5	S5-soft off. Context not saved. Cold boot is required.	No power	D3-no power except for wake-up logic	5W<power††
G3-mechanical off. The power supply cord is unplugged from the system.	No power to the system.	No power	D3-no power. No power for wake-up logic, except when provided by a battery or external source.	No power to the system so that service can be performed.

† Not supported on the evaluation board.

†† Assumes limited number of wake-up devices.

3.4.3 ACPI 1.0 Wake-Up Events

The ability for the system to wake up is described in Table 3-4. Please note that sleeping states S3, S4 and S5 are the same (no power to CPU) for the wake up events.

Table 3-4. ACPI 1.0 Wake-Up Events

Wake-up Event	From State
Power button	S1,S3,S5
Real Time Clock alarm	S1,S3,S5
LAN†	S1,S3,S5
Modem†	S1,S3,S5
USB†	S1
Keyboard	S1
PCI PME	S1,S3,S5
Mouse	S1

† Feature requires additional 5 VSB current; use a power supply capable of 720mA minimum, 5 VSB current.

3.5 APM 1.2 Support

Legacy power management (APM1.2) will be supported for non-ACPI aware operating systems (Windows 3.x, Windows 95-retail and OSR2, Windows NT 4.x).

3.6 Label Requirements

This is not a production board and does not meet FCC regulations. It is intended for use in lab environments only.

3.7 Battery Requirements

A Type 2032, socketed, 3 V lithium coin-cell battery is used on this evaluation board. The battery has a shelf life of greater than three years.

3.8 Mechanical Considerations

3.8.1 Motherboard Dimensions

The actual size of the evaluation board is 12 inches wide by 17 inches long.

3.8.2 Board Layout

The board layout is determined by the standard WTX locations for I/O and card slots. The RDRAM RIMM connectors are positioned so that the two channels are at a right angle to each other. This allows the straightest connection from the MCH to each RIMM. For the dual-processor FC-PGA processor system bus, a T-topology using the on-die termination of the Pentium III processor has been used.

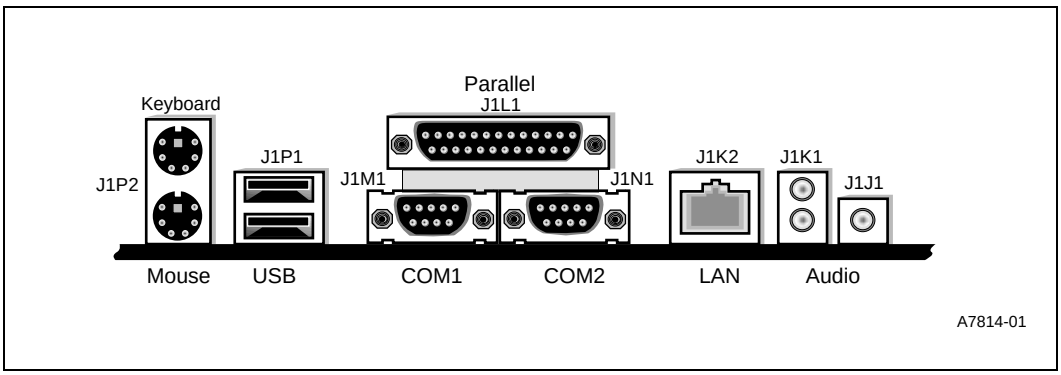
3.8.3 Mounting Hole Location Considerations

The board mounting hole locations are consistent with the WTX 1.02 specification.

3.8.4 Back Panel I/O Connector Layout

The back panel I/O connector layout is consistent with the WTX 1.02 specification, as shown in Figure 3-2.

Figure 3-2. Back Panel I/O Connector Layout



3.9 Power LED Status

Table 3-5 indicates the supported front panel Power LED states as they correspond to the system states.

Table 3-5. PWR System State and LED State

System State	LED State
OFF	OFF
Running	Steady Green
Running with message	Blinking Green
Sleeping	Steady Yellow
Sleeping with message	Blinking Yellow

NOTE: PWR_LED(0:1) are driven by GP0 signals to control the front panel Power LED states when the system is powered on.

Hardware Reference 4

This section provides reference information on the system hardware, including connector pinout information and jumper settings.

4.1 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance and cause reliability problems.

The Intel® Pentium® III processor/840 Development Kit is shipped with two heatsink/fan thermal solutions pre-installed on the primary and secondary processors using metallic clips. These thermal solutions have been tested in an open air environment at room temperature and are sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

4.2 In-Target Probe (ITP) Debugger Port

The evaluation platform is populated with a 1.5-V In-Target Probe (ITP) debugger port. The ITP port provides a path for debugger tools like emulators, in-target probes, and logic analyzers to gain access to the processor's registers and signals without affecting high speed operation. This allows the system to operate at full speed with the debugger attached.

Caution: The ITP connector used on this board requires a 1.5-V supply voltage.

4.3 Post Code Display

The evaluation board has an on-board Post Code Display. Data from any code that does an I/O write to 80H is latched on the two LED displays (U10C1 upper nibble/U11C1 lower nibble). During BIOS startup, code is posted to these LEDs to indicate what the BIOS is doing. Application code can post its own data to these LEDs by performing an I/O write to address 80H. The Altera EPM7064S PLD code used to implement this function is included in Appendix C, "PLD Code Listing."

4.4 WTX Power Supply

WTX is a new form factor developed for the mid-range workstation market. The WTX specification goes beyond standard form factor specifications to specify the size and shape of the board and the interface between the board and chassis.

For more information on the WTX form factor, go to www.WTX.org.

4.5 PCI Expansion Slots

The evaluation platform has four PCI 32-bit/33-MHz expansion slots (J4D1, J4D2, J4E1, J4F1) and two PCI 64-bit/66-MHz expansion slots (J4A1, J4B1).

4.6 PCI Device Mapping

On the evaluation platform the PCI devices are mapped to PCI device numbers by connecting an address line to the IDSEL signal of each PCI device. Table 4-1 shows the mapping of PCI devices.

Table 4-1. PCI Device Mapping

Device	Address Line	PCI Device Number
LAN	AD23	7
PCI Slot 1	AD24	8
PCI Slot 2	AD25	9
PCI Slot 3	AD26	10
PCI Slot 4	AD27	11

4.7 PCI64 Device Mapping

Table 4-2 shows the mapping of 64-bit/66-MHz PCI devices off of the P64H. The P64H does not use PCI device numbers; they are dynamically assigned.

Table 4-2. PCI64 Device Mapping

Device	Address Line
PCI64 Slot 1	P64AD28
PCI64 Slot 2	P64AD29

4.8 Connector Pinouts

4.8.1 WTX Power Connector

Table 4-3 shows the signals assigned to the WTX-style main power connector (J3M1).

Table 4-3. Main Power Connector Pinout (J3M1)

Pin	Signal Name	Function
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	3.3 V	3.3 V
4	3.3 V	3.3 V
5	3.3 V	3.3 V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	5 V	5 V VVC
12	5 V	5 V VVC
13	3.3 V	3.3 V
14	3.3 V	3.3 V
15	3.3 V	3.3 V
16	3.3 V	3.3 V
17	3.3 V_SB	Standby 3.3 V
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	5 V_SB	Standby 5 V
23	5 V	5 V VCC
24	5 V	5 V VCC

Table 4-4 shows the signals assigned to the WTX-style secondary power connector (J3P1).

Table 4-4. Secondary Power Connector Pinout (J3P1)

Pin	Signal Name	Function
1	5 V Sense	5 V Remote Sense
2	3.3 V Sense	3.3 V Remote Sense
3	RES	No Connection
4	GND	Ground
5	GND	Ground
6	12 V	12 V
7	-12 V	-12 V
8	I2C Clock	No Connection
9	Fan C	No Connection
10	PS-OK	Voltages within acceptable ranges
11	1394	No Connection
12	5 V Rtn	5 V Sense Return
13	3.3 V Rtn	3.3 V Sense Return
14	RES	No Connection
15	GND	Ground
16	12 V	12 V
17	12 V	12 V
18	Sleep	Sleep Control
19	I2C Date	No Connection
20	Fan M	No Connection
21	PS-ON#	Remote ON/OFF Control
22	1394 Rtn	No Connection

Table 4-4 shows the signals assigned to the third WTX-style power connector (J1T4).

Table 4-5. Third Power Connector Pinout (J1T4)

Pin	Signal Name	Function
1	12 V_DIG	D2D 12 V supply
2	12 V_DIG	D2D 12 V supply
3	12 V_DIG	D2D 12 V supply
4	No Connection	Reserved
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	No Connection	Reserved

4.8.2 ITP Debugger Connector

Table 4-6 shows the signals assigned to the ITP debugger connector (J3K1).

Table 4-6. ITP Debugger Connector Pinout (J3K1)

Pin	Signal Name	Pin	Signal Name
1	GND	2	RESET#
3	GND	4	DBRESET#
5	GND	6	TCLK
7	TDI_P0	8	TMS
9	TD0_P1	10	POWERON
11	TRST#	12	NC
13	NC	14	GND
15	PREQ0#	16	GND
17	PRDY0#	18	GND
19	PREQ1#	20	GND
21	PRDY1#	22	GND
23	NC	24	GND
25	NC	26	GND
27	NC	28	GND
29	NC	30	CPUCLK

4.8.3 Dual Stacked USB Connector

Table 4-7 shows the signals assigned to the dual stacked USB connector (J1P1).

Table 4-7. USB Connector Pinout (J1P1)

Pin	Signal Name
1,5	Power (fused)
2,6	USBP0# [USBP1#]
3,7	USBP0 [USBP1]
4,8	GND

4.8.4 PS/2-Style Mouse and Keyboard Connectors

Table 4-8 shows the signals assigned to the keyboard and mouse connector (J1P2). The keyboard port is on top. The mouse port is on the bottom.

Table 4-8. Keyboard and Mouse Connector Pinouts (J1P2)

Pin	Signal Name
1	Data
2	No Connect
3	GND
4	+5 V (fused)
5	Clock
6	No Connect

4.8.5 Parallel Port Connector

Table 4-9 shows the signals assigned to the parallel port connector (J1L1).

Table 4-9. DB25 Parallel Port Connector Pinout (J1L1)

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data Bit 0	15	Fault#
3	Data Bit 1	16	INIT#
4	Data Bit 2	17	SLCT IN#
5	Data Bit 3	18	GND
6	Data Bit 4	19	GND
7	Data Bit 5	20	GND
8	Data Bit 6	21	GND
9	Data Bit 7	22	GND
10	ACK#	23	GND
11	Busy	24	GND
12	Paper end	25	GND
13	SLCT		

4.8.6 Serial Ports

Table 4-10 shows the signals assigned to the serial port connectors (J1M1 and J1N1). When looking at the external side of the connectors, COM1 is the connector on the left (J1M1) and COM2 is connector on the right (J1N1).

Table 4-10. Serial Port Connector Pinout (J1M1 and J1N1)

Pin	Signal Name
1	DCD
2	Serial In (SIN)
3	Serial Out (SOUT)
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

4.8.7 Audio/MIDI/Game Port Connectors

Table 4-11 shows the signals assigned to the audio mic-in connector (J1J1).

Table 4-11. Audio Mic-In Connector Pinouts (J1J1)

Pin	Signal Name
Sleeve	GND
Tip	Mono In
Ring	Mic bias voltage

Table 4-12 shows the signals assigned to the audio line-in connector (J1K1 top).

Table 4-12. Audio Line-In Connector Pinouts (J1K1)

Pin	Signal Name
Sleeve	GND
Tip	Audio Left In
Ring	Audio Right In

Table 4-13 shows the signals assigned to the audio line-out connector (J1K1 bottom).

Table 4-13. Audio Line-Out Connector Pinouts (J1K1)

Pin	Signal Name
Sleeve	GND
Tip	Audio Left Out
Ring	Audio Right Out

Table 4-14 shows the signals assigned to the MIDI/game port connector (J1A1).

Table 4-14. MIDI/Game Port Connector Pinouts (J1A1)

Pin	Signal Name	Pin	Signal Name
1	+5 V (fused)	9	+5 V (fused)
2	GP4	10	GP6
3	GP0	11	GP2
4	GND	12	MIDI-OUTR
5	GND	13	GP3
6	GP1	14	GP7
7	GP5	15	MIDI-INR
8	+5 V (fused)	16	NC

4.8.8 LAN Connector

Table 4-15 shows the signals assigned to the Wake-On LAN (WOL) connector (J2F2).

Table 4-15. Wake-On LAN Connector Pinouts (J2F2, Not Populated)

Pin	Signal Name
1	5 VSB
2	Ground
3	WOL

Table 4-16 shows the signals assigned to the RJ45 connector (J1K2).

Table 4-16. RJ45 LAN Connector Pinouts (J1K2)

Pin	Signal Name
1	IO1
2	IO2
3	IO3
4	IO4
5	IO5
6	IO6
7	IO7
8	IO8

4.8.9 Front Panel I/O Connectors

Table 4-17 shows the signals assigned to the front panel I/O connector (J12R1).

Table 4-17. Front Panel I/O Connector Pinouts (J12R1)

Pin	Signal Name	Pin	Signal Name
1	SW_ON	15	HD Active#
2	Ground	16	HD PWR
3	NC	17	Key
4	NC	18	PWR_LED0 (Yellow)
5	Key	19	Key
6	+5 V (option for WOIR)	20	PWR_LED1 (Green)
7	Key	21	Key
8	IR_RX	22	Ground
9	Ground	23	FP_RESET
10	IR_TX	24	PC_SPKR#
11	+5 V	25	Key
12	Key	26	Onboard Spkr enable connect 26 - 27
13	+5 V	27	+5 V
14	Key		

Table 4-18 shows the pins in the front panel connector that control reset and ON/OFF.

Table 4-18. Reset and ON/OFF Connector Pinouts

Pin	Signal Name
1	SW_ON
2	Ground
22	Ground
23	FP_RESET

Table 4-19 shows the system state changes with contact closure between SW_ON and FPPWR_ON. Momentary contact closure between FP_RESET and Ground will initiate a complete system reset.

Table 4-19. System State Changes Between SW-ON and FPPWR_ON

System State	Contact Closure SW_ON to Ground	Result
Off	Any duration	System Power On
On	<4 seconds	System sleep
On	>4 seconds	System Power Off
Sleep	<4 seconds	System Wake-up

NOTE: Power management must be enabled in the BIOS setup. Operating System Power Management features may change the functionality listed above.

4.8.10 Processor Fans

Connections for thermal solution fans for the processors are located at J2N1 and J2R1.

Table 4-21 shows the signals assigned for the auxiliary fan connectors.

Table 4-20. Processor Fan Connector Pinouts (J2N1, J2R1)

Pin	Signal Name
1	Ground
2	+12 (FAN_CTL)
3	Tachometer (FAN_M)

NOTE: Fan_CTL gates the +12 V allowing each fan to be turned on and off by ACPI software for power management and noise reduction purposes.

4.8.11 Chassis Fans

There are six headers provided for additional chassis fans. The fan connectors are: J11A1, J11A2, J11B1, J1T1, J1T2, J1T3.

Table 4-21 shows the signals assigned for the chassis fan connectors.

Table 4-21. Auxiliary Fan Connector Pinouts (J11A1, J11A2, J11B1, J1T1, J1T2, J1T3)

Pin	Signal Name
1	Ground
2	+12 (FAN_CTL)
3	Tachometer (FAN_M)

NOTE: Fan_CTL gates the +12 V allowing each fan to be turned on and off by ACPI software for power management and noise reduction purposes.

4.8.12 ATAPI Audio Connectors

The ATAPI connectors are used with CD-ROM Drives, have four pins in one row, and mate with a polarized latching-type receptacle. There are several AMP (vendor) numbers; use 103961-1 as a reference. Table 4-22 shows the signals assigned to ATAPI connector (J1H1).

Table 4-22. ATAPI Audio Connector Pinouts (J1H1)

Pin	Signal Name
1	CD-Left
2	Ground
3	Ground
4	CD-Right

Table 4-23 shows the signals assigned to ATAPI connector (J1H2). This connector is used for auxiliary line input signals.

Table 4-23. ATAPI Audio (Auxiliary Line-In) Connector Pinouts (J1H2)

Pin	Signal Name
1	LLINE_IN
2	Ground
3	Ground
4	RLINE_IN

4.8.13 IDE Connector

The IDE connectors have 40 pins; two rows with twenty pins per row. Table 4-24 shows the signals assigned to connectors IDE1 (J10E1) and IDE2 (J10F1).

Table 4-24. IDE Connector Pinouts for IDE1 (J10E1) and IDE2 (J10F1) (Sheet 1 of 2)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	21	DRQ3
2	Ground	22	Ground
3	Host Data 7	23	I/O Write#
4	Host Data 8	24	Ground
5	Host Data 6	25	I/0 Read#
6	Host Data 9	26	Ground
7	Host Data 5	27	IOCHRDY
8	Host Data 10	28	BALE
9	Host Data 4	29	DACK3#
10	Host Data 11	30	Ground
11	Host Data 3	31	IRQ14
12	Host Data 12	32	IOCS16#

Table 4-24. IDE Connector Pinouts for IDE1 (J10E1) and IDE2 (J10F1) (Sheet 2 of 2)

Pin	Signal Name	Pin	Signal Name
13	Host Data 2	33	Addr 1
14	Host Data 13	34	Ground
15	Host Data 1	35	Addr 0
16	Host Data 14	36	Addr 2
17	Host Data 0	37	Chip Select 0#
18	Host Data 15	38	Chip Select 1#
19	Ground	39	Activity
20	Key	40	Ground

4.8.14 Floppy Drive Connector

The floppy drive connector has 34 pins. Table 4-25 shows the signals assigned to connector (J10F2).

Table 4-25. Floppy Drive Connector Pinouts (J10F2)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	FDHDIN
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	Index
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	Ground	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	Ground	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

4.8.15 32-Bit PCI Slot Connector

Table 4-26 shows the signals assigned to the 32-Bit PCI slot connector (J4F1, J4E1, J4D2, and J4D1).

Table 4-26. 32-Bit PCI Slot Connector Pinouts

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	VCC	B1	- 12V	A32	AD16	B32	AD17
A2	+ 12V	B2	GND	A33	3.3V	B33	CBE2#
A3	VCC	B3	GND	A34	FRAME#	B34	GND
A4	VCC	B4	No Connect	A35	GND	B35	IRDY#
A5	VCC	B5	VCC	A36	TRDY#	B36	3.3 V
A6	PIRQ1#	B6	VCC	A37	GND	B37	DEVSEL#
A7	PIRQ3#	B7	PIRQ2#	A38	STOP#	B38	GND
A8	VCC	B8	PIRQ0	A39	3.3 V	B39	LOCK#
A9	No Connect	B9	PRSNT1B#	A40	SDONE	B40	PERR#
A10	VCC	B10	No Connect	A41	SBO#	B41	3.3 V
A11	No Connect	B11	PRSNT2B#	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	3.3V
A13	GND	B13	GND	A44	AD15	B44	CBE1#
A14	No Connect	B14	No Connect	A45	3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	VCC	B16	PCLK3	A47	AD11	B47	AD12
A17	GNT1#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	Reserved	B19	VCC	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	3.3V	B21	AD29	A52	CBEO#	B52	AD8
A22	AD28	B22	GND	A53	3.3 V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	3.3 V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	3.3 V	A56	GND	B56	AD3
A26	IDSEL	B26	CBE3#	A57	AD2	B57	GND
A27	3.3V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	VCC	B59	VCC
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	GND	B30	AD19	A61	VCC	B61	VCC
A31	AD18	B31	3.3 V	A62	VCC	B62	VCC

4.8.16 64-Bit PCI Slot Connector

Table 4-27 shows the signals assigned to the 64-Bit PCI slot connector (J4A1 and J4B1).

Table 4-27. 64-Bit PCI Slot Connector Pinouts (Sheet 1 of 2)

Pins	A	B	Pins	A	B
1	TRST#	-12 V	48	GND	AD10
2	12 V	TCLK	49	AD9	M66EN
3	TMS	GND	50	GND	GND
4	TDI	TDO	51	GND	GND
5	+5 V	+5 V	52	CBE0#	AD8
6	P64IRQ0	+5 V	53	3.3 V	AD7
7	P64IRQ2	P64IRQ1	54	AD6	3.3 V
8	+5 V	+5 V	55	AD4	AD5
9	No Connect	PRSNT1#	56	GND	AD3
10	3.3 V	No Connect	57	AD2	GND
11	No Connect	PRSNT2#	58	AD0	AD10
12	KEY	KEY	59	3.3 V	3.3 V
13	KEY	KEY	60	REQ64#	ACK64#
14	3.3 V AUX	No Connect	61	+5 V	+5 V
15	RST#	GND	62	+5 V	+5 V
16	3.3 V	CLK	63	GND	No Connect
17	GNT#	GND	64	CBE7#	GND
18	GND	REQ#	65	CBE5#	CBE6#
19	PME#	3.3 V	66	3.3 V	CBE4#
20	AD30	AD31	67	PAR64	GND
21	3.3 V	AD29	68	AD62	AD63
22	AD28	GND	69	GND	AD61
23	AD26	AD27	70	AD60	3.3 V
24	GND	AD25	71	AD58	AD59
25	AD24	3.3 V	72	GND	AD57
26	IDSEL	CBE3#	73	AD56	GND
27	3.3 V	AD23	74	AD54	AD55
28	AD22	GND	75	3.3 V	AD53
29	AD20	AD21	76	AD52	GND
30	GND	AD19	77	AD50	AD51
31	AD18	3.3 V	78	GND	AD49
32	AD16	AD17	79	AD48	3.3 V
33	3.3 V	CBE2#	80	AD46	AD47
34	FRAME#	GND	81	GND	AD45

Table 4-27. 64-Bit PCI Slot Connector Pinouts (Sheet 2 of 2)

Pins	A	B	Pins	A	B
35	GND	IRDY#	82	AD44	GND
36	TRDY#	3.3 V	83	AD42	AD43
37	GND	DEVSEL#	84	3.3 V	AD41
38	STOP#	GND	85	AD40	GND
39	3.3 V	LOCK#	86	AD38	AD39
40	SDONE	PERR#	87	GND	AD37
41	SBO#	3.3 V	88	AD36	3.3 V
42	GND	SERR#	89	AD34	AD35
43	PAR	3.3 V	90	GND	AD33
44	AD15	CBE1#	91	AD32	GND
45	3.3 V	AD14	92	No Connect	No Connect
46	AD13	GND	93	GND	No Connect
47	AD11	AD12	94	No Connect	GND

4.9 AGP Connector

Table 4-28 shows the signals assigned to the AGP connector (J4G1).

Table 4-28. AGP Connector Pinouts (Sheet 1 of 2)

Pin	A	B	Pin	A	B
1	12 V	OVRCNT#	34	3.3 Vddq	3.3 Vddq
2	TYPEDET#	5.0V	35	AD22	AD21
3	Reserved	5.0V	36	AD20	AD19
4	USB-	USB+	37	GND	GND
5	GND	GND	38	AD18	AD17
6	INTA#	INTB#	39	AD16	C/BE2#
7	RST#	CLK	40	3.3 Vddq	3.3 Vddq
8	GNT#	REQ#	41	FRAME#	IRDY#
9	3.3 VCC	3.3 VCC	42	Reserved	3.3Vaux
10	ST1	ST0	43	GND	GND
11	Reserved	ST2	44	Reserved	Reserved
12	PIPE#	RBF#	45	3.3 VCC	3.3 VCC
13	GND	GND	46	TRDY#	DEVSEL#
14	Reserved	Reserved	47	STOP#	3.3 Vddq

NOTES:
1. Reserved pins are only for future use by the AGP interface specification.
2. IDSEL# is not a pin on the AGP connector. AGP graphics components should connect the AD16 signal to the 3. 3 volt IDSEL# function internal to the component.
3. All 3.3 volt cards leave the TYPEDET signal open. All 1.5 volt cards tie this signal hard to ground.

Table 4-28. AGP Connector Pinouts (Sheet 2 of 2)

15	SBA1	SBA0	48	PME#	PERR#
16	3.3 VCC	3.3 VCC	49	GND	GND
17	SBA3	SBA2	50	PAR	SERR#
18	Reserved	SB_STB	51	AD15	C/BE1#
19	GND	GND	52	3.3 Vddq	3.3 Vddq
20	SBA5	SBA4	53	AD13	AD14
21	SBA7	SBA6	54	AD11	AD12
22	KEY	KEY	55	GND	GND
23	KEY	KEY	56	AD9	AD10
24	KEY	KEY	57	C/BE0#	AD8
25	KEY	KEY	58	3.3 Vddq	3.3 Vddq
26	AD30	AD31	59	Reserved	AD_STB0
27	AD28	AD29	60	AD6	AD7
28	3.3 VCC	3.3 VCC	61	GND	GND
29	AD26	AD27	62	AD4	AD5
30	AD24	AD25	63	AD2	AD3
31	GND	GND	64	3.3 Vddq	3.3 Vddq
32	Reserved	AD_STB1	65	AD0	AD1
33	C/BE3#	AD23	66	Reserved	Reserved

NOTES:
1. Reserved pins are only for future use by the AGP interface specification.
2. IDSEL# is not a pin on the AGP connector. AGP graphics components should connect the AD16 signal to the 3. 3 volt IDSEL# function internal to the component.
3. All 3.3 volt cards leave the TYPEDET signal open. All 1.5 volt cards tie this signal hard to ground.

4.10 Jumpers

Table 4-29 shows default jumper settings.

Table 4-29. Default Jumper Settings (Sheet 1 of 2)

Jumper Name	Jumper	Connection	Function	Default
P1 Present Override	J10	IN	CPU Present Disabled	
2-pin (1x2) Header, J10		OUT	Normal Operation	X
P0 Present Override	J42	IN	CPU Present Disabled	
2-pin (1x2) Header, J10		OUT	Normal Operation	X
Single CPU ITP pass	J11	1-2	UPITP	
3-pin (1x3) Header		2-3	DPITP	X
PSB Select	J2L1, J2K1	IN, 2-3	PSB=100 MHz	
2-pin (1x2) Header		OUT, OUT	PSB=133 MHz	X
3-pin (1x3) Header		OUT, 1-2	Reserved	
IOQ	J6R2	IN	IOQ=1	
2-pin (1x2) Header		OUT	CHIPSET	X
82559	J2F1	1-2	Enable	X
3-pin (1x3) Header		2-3	Disable	
PSB STRAP	J7F1	IN	SAFE MODE (1111)	
2-pin (1x2) Header		OUT	NORMAL MODE	X
2nd WD TIMEOUT	J8F1	IN	NO REBOOT	X
2-pin (1x2) Header		OUT	REBOOT	
CMOS	J6F1	1-2	NORMAL	X
2-pin (1x2) Header		2-3	CLEAR	
FHW TBL	J10A1	IN	UNLOCKED	X
2-pin (1x2) Header		OUT	LOCKED	
SPEAKER	J11T1	1-2	AC'97	
3-pin (1x3) Header		2-3	ON-BOARD/FP	X
P0 VRM VID	J11N1	1-2	P0_VID0	X
3-pin (1x3) Header		2-3	0	
		OUT	1	
	J11N2	1-2	P0_VID1	X
		2-3	0	
		OUT	1	
	J11P2	1-2	P0_VID2	X
		2-3	0	
		OUT	1	
	J11P1	1-2	P0_VID3	X
		2-3	0	
		OUT	1	
	J11N3	1-2	P0_VID4	
		2-3	0	X

Table 4-29. Default Jumper Settings (Sheet 2 of 2)

Jumper Name	Jumper	Connection	Function	Default
		OUT	1	
P1 VRM VID	J11P4	1-2	P1_VID0	X
3-pin (1x3) Header		2-3	0	
		OUT	1	
	J11P3	1-2	P1_VID1	X
		2-3	0	
		OUT	1	
	J11R3	1-2	P1_VID2	X
		2-3	0	
		OUT	1	
	J11R2	1-2	P1_VID3	X
		2-3	0	
		OUT	1	
	J11R1	1-2	P1_VID4	
		2-3	0	X
		OUT	1	

4.10.1 P1/P0 Present Override (J10/J42)

The Intel Pentium III processor/840 evaluation board will not power on if both processors are not installed. To override this function (for board testing), install jumpers on J10 and J42.

During a boot up sequence, the hardware checks whether the processors are present. To boot the board without the hardware recognizing a processor, the jumper must be set to the IN position. To override the CPU detection for P0, jumper J42 must be set to the IN position. To override P1, J10 must be set to the IN position. To boot the board without either processor being enabled, both jumpers must be set. When operating in uni-processor mode, the jumper need not be set to ignore the processor. The terminator in the second socket will inform the hardware that no processor is present.

4.10.2 Single Processor ITP Pass (J11)

This jumper allows the TDO of CPU P0 to connect to the TDI of P1 (DP mode, default) or to connect directly to the ITP connector (UP mode).

4.10.3 Processor System Bus Select (J2L1, J2K1)

These two jumpers work together to select the processor system bus frequency. A 133 MHz processor side bus frequency is selected by default (J2L1 OUT and J2K1 OUT).

Caution: You will only need to change the default setting if you are replacing the processors provided in the kit with processors that use a 100 MHz processor system bus. Before changing these settings, read Appendix A, "Using Different Processors in the Board." Setting this jumper incorrectly could damage the evaluation board or the processors.

4.10.4 PSMI P0 (J3J2), PSMI P1 (J3K2) (Not used)

This jumper controls the processor SMI configuration. By default, the processors' SMIs are enabled.

4.10.5 In Order Queue (J6R2)

If this jumper is installed, the In Order Queue (IOQ) is set to 1. Otherwise the IOQ is set to 8.

4.10.6 82559 Ethernet Controller Enable (J2F1)

This jumper is used to enable/disable the 82559ER LAN Controller. By default, this jumper is set to 1-2 to enable the 82559ER.

4.10.7 Reserved Jumper (J7F1)

Reserved. Do not change the default setting.

4.10.8 Second WD Timeout (J8F1)

If enabled, the ICH resets the CPU after the TCO times out, if an instruction is not fetched after reset.

4.10.9 CMOS (J6F1)

This jumper controls the power to the battery backed-up CMOS RAM. This RAM stores system information required by the BIOS during startup. For normal operation, short pins 1 and 2. To clear the CMOS RAM, perform the following steps:

1. Remove power from the board by pushing the power switch (S11R1).
2. Move J6F1 to the 2-3 position.
3. Disconnect the power supply (J3M1, J3P1, J1T4).
4. Move J6F1 back to the 1-2 position.
5. Reconnect the power supply (J3M1, J3P1, J1T4).
6. Boot the system and enter the BIOS setup screen to reconfigure the system.

4.10.10 FWH TBL (J10A1)

This jumper provides write protection for the top block of memory in the FWH.

4.10.11 Speaker (J11T1)

The speaker jumper allows the system speaker output (PC Beep) to be routed to the on-board transducer or to the AC'97 Codec.

4.10.12 P0 Voltage Regulator Module Voltage ID (J11N3, J11N2, J11N1, J11P2, J11P1)

The P0 VID jumpers allow the CPU's core voltage to be altered. Do not modify this jumper setting; the processor core voltage is selected by the processor.

Warning: Incorrectly setting the VID jumpers can result in permanent damage to the processor.

4.10.13 P1 Voltage Regulator Module Voltage ID (J11P4, J11P3, J11R3, J11R2, J11R1)

The P1 VID jumpers allow the CPU's core voltage to be altered. Do not modify this jumper setting; the processor core voltage is selected by the processor.

Warning: Incorrectly setting the VID jumpers can result in permanent damage to the processor.

4.10.14 Push Button Switches

There are two push button switches on the evaluation board, labeled S11P1 and S11R1.

- S11P1 is the reset switch.
- S11R1 is the power switch.

Depending on the BIOS configuration the power switch may need to be held down for approximately five seconds before the board powers down. When powered down, the board will still have Standby power supplied by the WTX power supply.

BIOS Quick Reference 5

The evaluation board is licensed with a single copy of Embedded BIOS and Embedded DOS software from General Software, Inc.[1] This software is provided for demonstration purposes only and must be licensed directly from General Software, Inc. for integration with new designs. General Software may be reached at (800) 850-5755, on the web at http://www.gensw.com, or via email at sales@gensw.com.

BIOS updates may periodically be posted to the Intel Developers' web site at http://developer.intel.com/.

5.1 Overview

The system's pre-boot environment is managed with an adaptation of Embedded BIOS from General Software. The pre-boot environment includes POST, Setup Screen System, Manufacturing Mode, Console Redirection, Windows CE Loader (CE Ready), and Integrated BIOS Debugger. A REFLASH tool is also available to update the BIOS image with new builds of Embedded BIOS that may be obtained from General Software.

Before using the system, please read the following to properly configure CMOS settings, and learn how to use the embedded features of the pre-boot firmware, Embedded BIOS.

The last two sections of this chapter provide the BIOS POST Codes and Beep codes.

5.2 Power-On Self-Test (POST)

When the system is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components. During this time, POST progress codes are written by the system BIOS to I/O port 80H, allowing the user to monitor the progress with a special monitor. "Embedded BIOS POST Codes" on page 5-13 lists the POST codes and their meanings.

During early POST, no video is available to display error messages should a critical error be encountered; therefore, POST uses beeps on the speaker to indicate the failure of a critical system component during this time. Consult "Embedded BIOS Beep Codes" on page 5-16 for a list of Beep codes used by the system's BIOS.

5.3 The BIOS User Interface

The system BIOS can use the standard keyboard and video device, or use console redirection to demonstrate headless operation. For headless operation, remove the standard keyboard and screen devices and the system will boot unattended. If an RS232 cable is attached to COM1, a PC/AT-style character-based POST is available from HyperTerminal, PROCOMM, or any other terminal emulator software that supports VT100 emulation.

1. General Software™, the GS Logo, Embedded BIOS™, BIOStart™, CE-Ready™, and Embedded DOS™ are trademarks or registered trademarks of General Software, Inc.

When a keyboard and video device are attached, system can display either a traditional character-based PC BIOS display with memory count-up, or it can display a graphical POST with splash screen and progress icons. Both POST displays accept a <DEL> key press to enter the setup screen, and both display boot-time progress activity displays. The graphical display shows the status of file system devices and even OEM-defined devices (when the OEM adapts the BIOS to a particular OEM platform), but omits character-based PCI resource display. The text-based POST displays the memory count-up and the PCI resource assignment table.

Figure 5-1 shows the format of the text-based POST display. The display is very similar if console redirection through a COM port is used instead.

Figure 5-1. BIOS POST Pre-Boot Environment

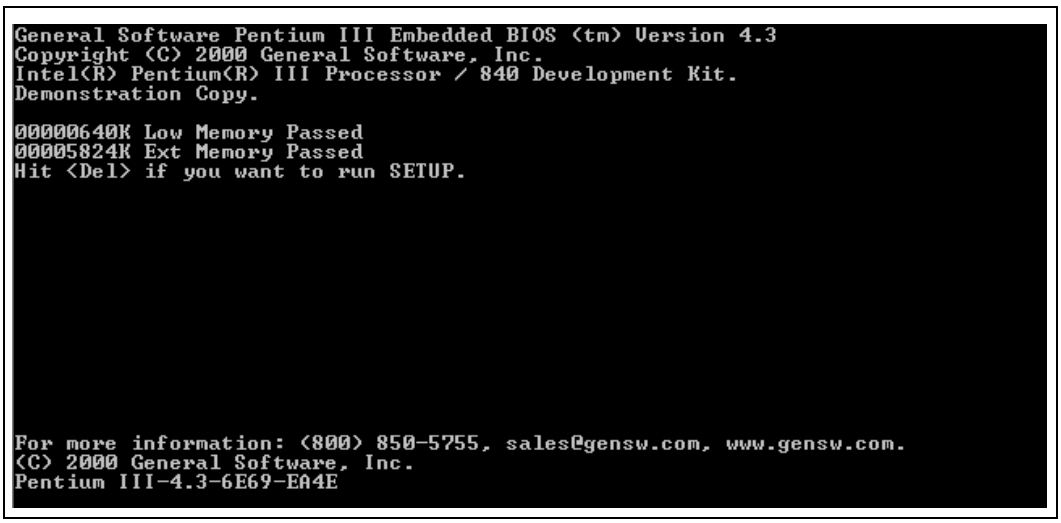
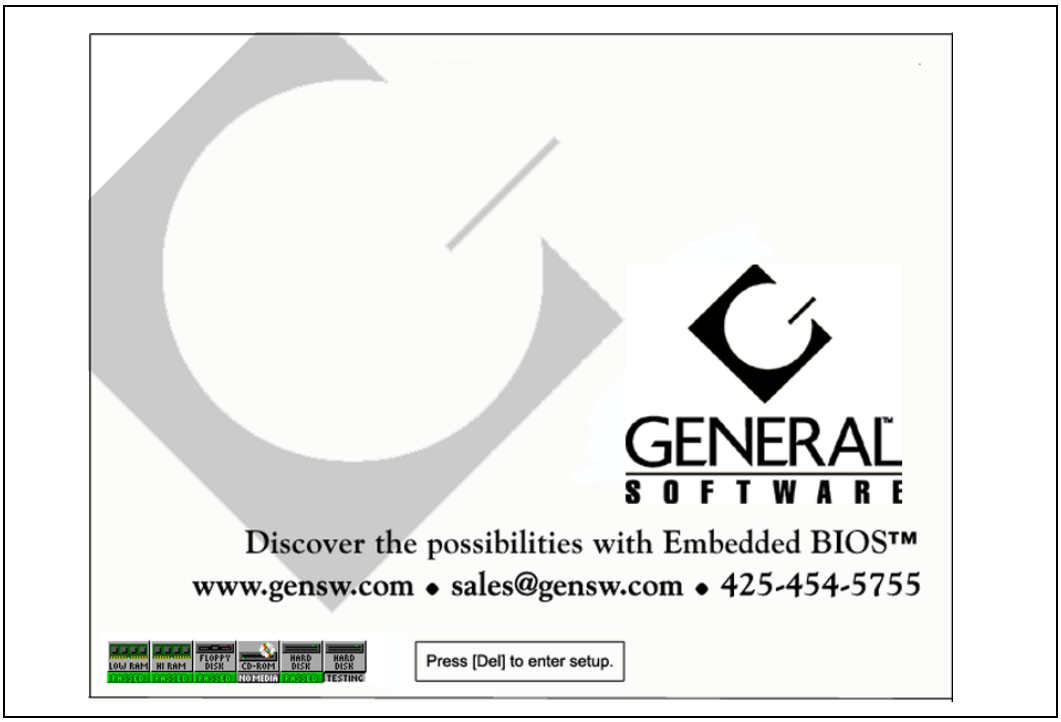


Figure 5-2 shows the graphical version of POST. The BIOS decompresses the main image, and can display multiple overlaid graphics at various points in POST. The OEM can define the entire sequence and control the timing of the system for an embedded application, and can arrange to have different graphics displayed on each successive boot of the system. This feature is ideal for embedded systems that must show evidence of operation during startup, while the application loads underneath the splash screen. Once the application begins writing to the screen, the splash screen relinquishes control, providing a seamless graphical progression for the end user.

Figure 5-2. Graphical POST



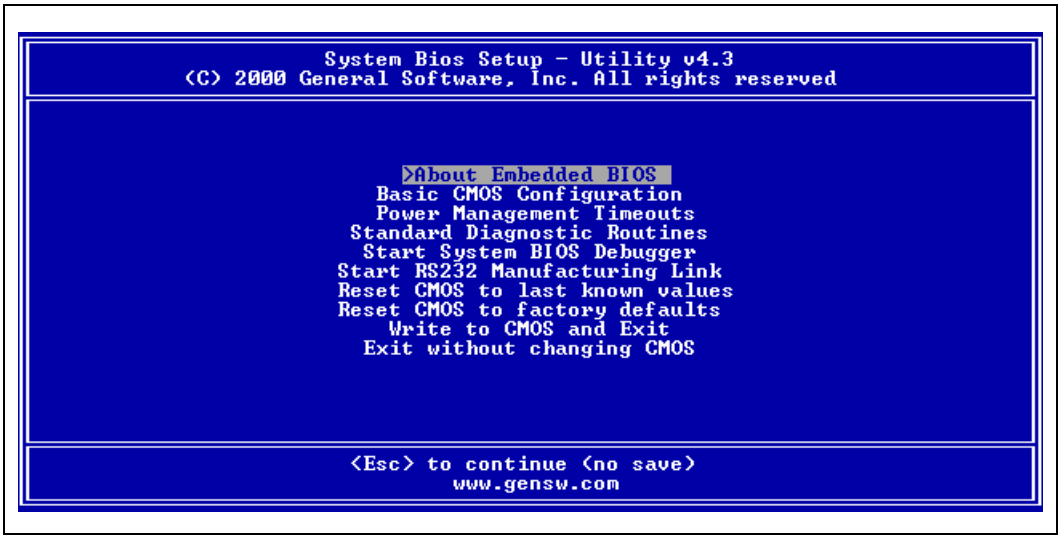
When the system is powered on for the first time, you'll need to configure the system through the Setup Screen System (described later) before peripherals, such as disk drives, are recognized by the BIOS. The information is written to battery-backed CMOS RAM on the board's Real Time Clock. Should the board's battery fail, this information will be lost and the board will need to be reconfigured.

The Basic Setup Screen provides an option to disable the graphical POST and switch to the legacy text-based version. This feature may not permanently disable the graphical POST if the BIOS adaptation calls for reverting to the graphical form after so many boots. If you find that the graphical POST comes back after several boots, it is because this option is enabled for this platform. The OEM can use the Embedded BIOS Adaptation Kit to control whether Setup can be used to dictate the policy, and whether it is permanent or temporary.

5.4 Setup Screen System

The system is configured from within the Setup Screen System, which is a series of menus that can be invoked from POST by pressing the <DEL> key if the main keyboard is being used, or by pressing Ctrl+C if the console is being redirected to a terminal program.

Figure 5-3. Embedded BIOS Setup Screen Menu

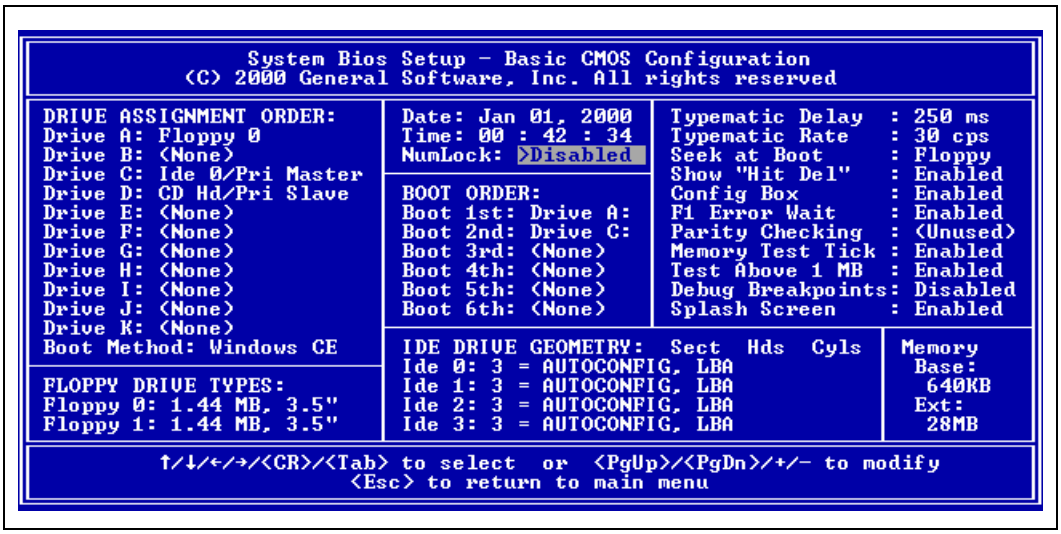


Once in the Setup Screen System (Figure 5-3), the user can navigate with the UP and DOWN arrow keys from the main console, or use the Ctrl+E and Ctrl+X keys from the remote terminal program to accomplish the same thing. TAB and ENTER are used to advance to the next field, and '+' and '-' keys cycle through values, such as those in the Basic Setup Screen, or the Diagnostics Setup Screen.

5.4.1 Basic CMOS Configuration Screen

The system's drive types, boot activities, and POST optimizations are configured from the Basic Setup Screen (Figure 5-4). In order to use disk drives with your system, you must select appropriate assignments of drive types in the left-hand column. Then, if you are using true floppy and IDE drives (not memory disks that emulate these drives), you need to configure the drive types themselves in the Floppy Drive Types and IDE Drive Geometry sections. Finally, you'll need to configure the boot sequence in the middle of the screen. Once these selections have been made, your system is ready to use.

Figure 5-4. Embedded BIOS Basic Setup Screen



5.4.2 Configuring Drive Assignments

Embedded BIOS allows the user to map a different file system to each drive letter. The BIOS allows file systems for each floppy (Floppy0 and Floppy1), each IDE drive (Ide0, Ide1, Ide2, and Ide3), and memory disks when configured (Flash0, ROM0, RAM0, etc.) Figure 5-4 shows how the first floppy drive (Floppy0) is assigned to drive A: in the system, and then how the first IDE drive (Ide0) is assigned to drive C: in the system.

To switch two floppy disks around or two hard disks around, just map Floppy0 to B: and Floppy1 to A:, and for hard disks map Ide0 to D: and Ide1 to C:.

Caution: Take care to not skip drive A: when making floppy disk assignments, as well as drive C: when making hard disk assignments. The first floppy should be A:, and the first hard drive should be C:. Also, do not assign the same file system to more than one drive letter. Thus, Floppy0 should not be used for both A: and B:. The BIOS permits this to allow embedded devices to alias drives, but desktop operating systems may not be able to maintain cache coherency with such a mapping in place.

A special field in this section entitled “Boot Method: (Windows CE/Boot Sector)” is used to configure the CE Ready feature of the BIOS. For normal booting (DOS, Windows NT, etc.), select “Boot Sector” or “Unused”.

5.4.2.1 Configuring Floppy Drive Types

If true floppy drive file systems (and not their emulators, such as ROM, RAM, or flash disks) are mapped to drive letters, then the floppy drives themselves must be configured in this section. Floppy0 refers to the first floppy disk drive on the drive ribbon cable (normally drive A:), and Floppy1 refers to the second drive (drive B:).

5.4.3 Configuring IDE Drive Types

If true IDE disk file systems (and not their emulators, such as ROM, RAM, or flash disks) are mapped to drive letters, then the IDE drives themselves must be configured in this section. The following table shows the drive assignments for Ide0-Ide3:

Table 5-1. IDE0-IDE3 Drive Assignments

File System Name	Controller	Master/Slave
Ide0	Primary (1f0h)	Master
Ide1	Primary (1f0h)	Slave
Ide2	Secondary (170h)	Master
Ide3	Secondary (170h)	Slave

To use the primary master IDE drive in your system (the typical case), just configure Ide0 in this section, and map Ide0 to drive C: in the Configuring Drive Assignments section.

The IDE Drive Types section lets you select the type for each of the four IDE drives: None, User, Physical, LBA, or CHS.

User This type allows the user to select the maximum cylinders, heads, and sectors per track associated with the IDE drive. This method is now rarely used since LBA is now in common use.

Physical This type instructs the BIOS to query the drive's geometry from the controller on each POST. No translation on the drive's geometry is performed, so this type is limited to drives of 512 Mbytes or less. Commonly, this is used with embedded ATA PC Cards.

LBA This type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the industry-standard LBA convention. This supports up to 16-Gbyte drives. *Use this method for all new drives.*

CHS This type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the Phoenix CHS convention. Using this type on a drive previously formatted with LBA or Physical geometry might show data as being missing or corrupted.

5.5 Configuring Boot Actions

Embedded BIOS supports up to six different user-defined steps in the boot sequence. When the entire system has been initialized, POST executes these steps in order until an operating system successfully loads. In addition, other pre-boot features can be run before, after, or between operating system load attempts. The following actions can be used:

Drive A: - K: Boot operating system from specified drive. If “Loader” is set to “BootRecord” or “Unused”, then the standard boot record will be invoked, causing DOS, Windows95/98, Windows NT, or other industry-standard operating systems to load. If “Boot Method” is set to “Windows CE”, then the boot drive’s boot record will not be used, and instead the BIOS will attempt to load and execute the Windows CE Kernel file, NK.BIN, from the root directory of each boot device.

Debugger Launch the Integrated BIOS Debugger. To return to the boot process from the debugger environment, type “G” at the debugger prompt and press ENTER.

MFGMODE Initiate Manufacturing Mode, allowing the system to be configured remotely via an RS232 connect to a host computer.

WindowsCE Execute a ROM-resident copy of Windows CE, if available. This feature is not applicable unless properly configured by the OEM in the BIOS adaptation.

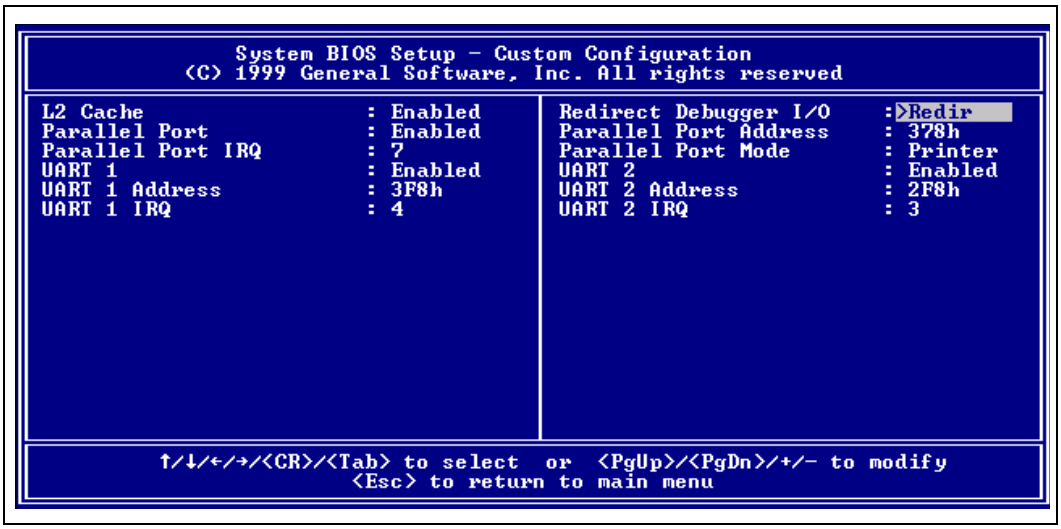
DOS in ROM Execute a ROM-resident copy of DOS, if available. This feature is not applicable unless an XIP copy of DOS, such as Embedded DOS-ROM, has been stored in the BIOS boot ROM. Copies of Embedded DOS-ROM may be obtained from General Software.

None No action; POST proceeds to the next activity in the sequence.

5.6 Custom Configuration Setup Screen

The system’s hardware-specific features are configured with the Custom Setup Screen (Figure 5-5). All features are straightforward except for the Redirect Debugger I/O option, which is an extra embedded feature that allows the user to select whether the Integrated BIOS Debugger should use standard keyboard and video or RS232 console redirection for interaction with the user. If no video is available, the debugger is always redirected.

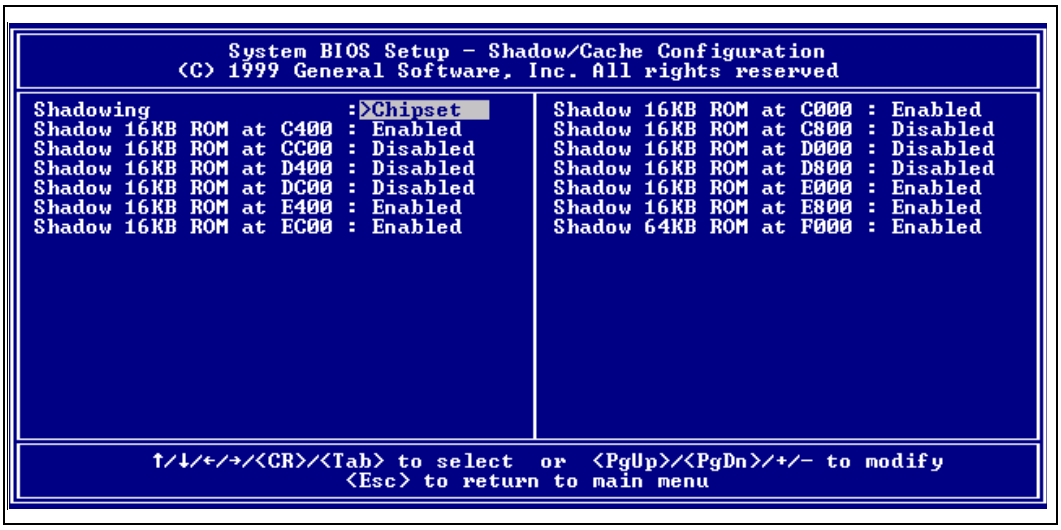
Figure 5-5. Embedded BIOS Custom Setup Screen



5.7 Shadow Configuration Setup Screen

The system's Shadow Configuration Setup Screen (Figure 5-6) allows the selective enabling and disabling of shadowing in 16 Kbyte sections, except for the top 64 Kbytes of the BIOS ROM, which is shadowed as a unit. Normally, shadowing should be enabled at C000/C400 (to enhance VGA ROM BIOS performance), and then E000-F000 should be shadowed to maximize system ROM BIOS performance.

Figure 5-6. Embedded BIOS Shadow Setup Screen



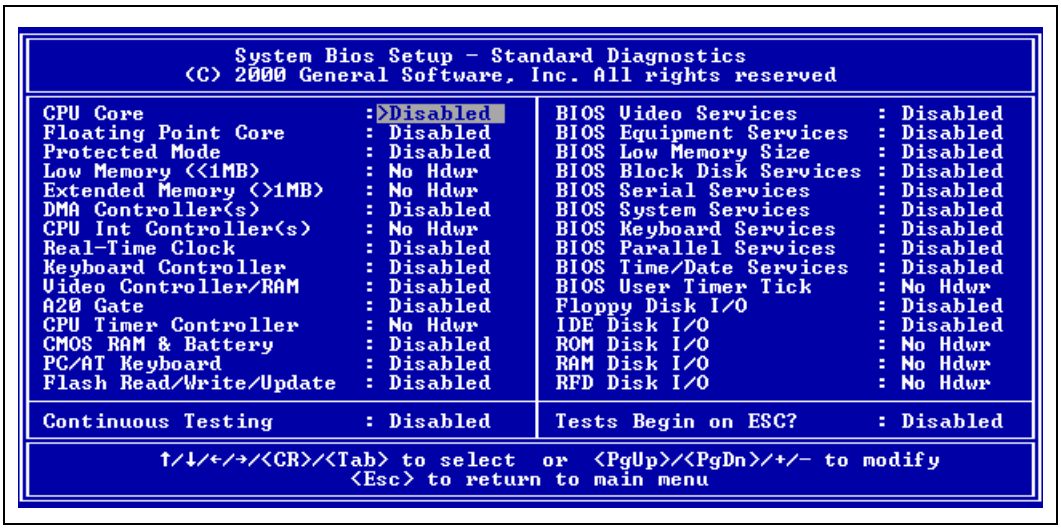
5.8 Standard Diagnostics Routines Setup Screen

Embedded systems may require automated burn-in testing in the development cycle. This facility is provided directly in the system's system BIOS through the Standard Diagnostics Routines Setup Screen (Figure 5-7). To use the system, selectively enable or disable features to be tested, and then enable the "Tests Begin on ESC?" option to cause the system test suite to be invoked. To repeat the system test battery continuously, you should also enable the "Continuous Testing" option. When continuous testing is started, the system will continue until an error is encountered.

Caution: The disk I/O diagnostics perform write operations on those drives; therefore, only spare drives should be used which do not contain data that could be harmed by the test.

Caution: The keyboard test may fail when in fact the hardware is operating within reasonable limits. This is because although the device may produce occasional errors, the BIOS retries operations when failures occur during normal operation of the system.

Figure 5-7. Standard Diagnostic Routines Setup Screen



5.9 Start System BIOS Debugger Setup Screen

The Embedded BIOS Integrated Debugger may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, the debugger will display the debugger prompt:

EB43DBG:

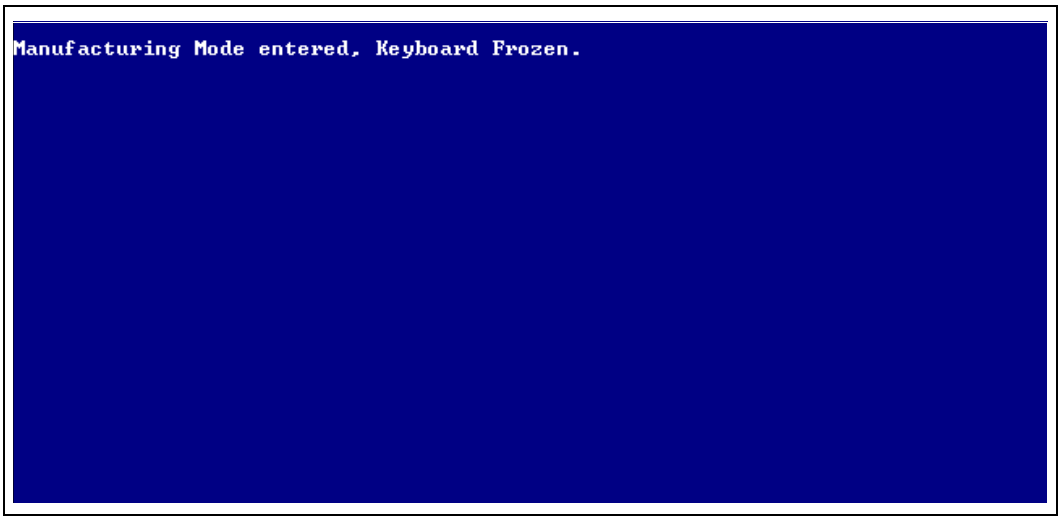
and await debugger commands. To resume back to the Setup Screen main menu, type the following command, which instructs the debugger to "go":

EB43DBG: **G** <ENTER>

5.10 Start RS232 Manufacturing Link Setup Screen

The Embedded BIOS Manufacturing Mode may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, Manufacturing Mode takes over the system and freezes the console of the system (Figure 5-8). The host can resume operation of the system and give control back to the system Setup Screen system with special control software.

Figure 5-8. Start RS232 Manufacturing Link Setup Screen



5.11 Manufacturing Mode

The system's BIOS provides a special mode, called Manufacturing Mode, that allows the target to be controlled by a host computer such as a laptop or desktop PC. Running special software supplied by General Software, the host can access the target's drives and manage the file systems on the target, reprogram flash memories, and test target hardware.

A full discussion of the uses of Manufacturing Mode is beyond the scope of this chapter. Complete documentation and host-side software is available directly from General Software. For more information, visit the General Software web site at http://www.gensw.com.

5.11.1 Console Redirection

The system can operate either with a standard PC/AT or PS/2 keyboard and VGA video monitor, or with a special emulation of a console over an RS232 cable connected to a host computer running a terminal program. To see an example session with HYPERTERMINAL, see the debugger section's screen display (Figure 5-10).

To use the Console Redirection feature, simply remove the video display card from the system so that no video ROM is available for the BIOS to detect. In the absence of any video support, the BIOS automatically switches its keyboard and screen functions to serial I/O over COM1 on the board. The hardware connection to the host computer requires a null modem cable.

The software on the target can be any terminal emulation program that supports ANSI terminal mode, using 9600 baud, no parity, and one stop bit (Note: This can be modified by the OEM during BIOS adaptation.) The program must be set to not use flow control, or the console may seem to stall or not accept input.

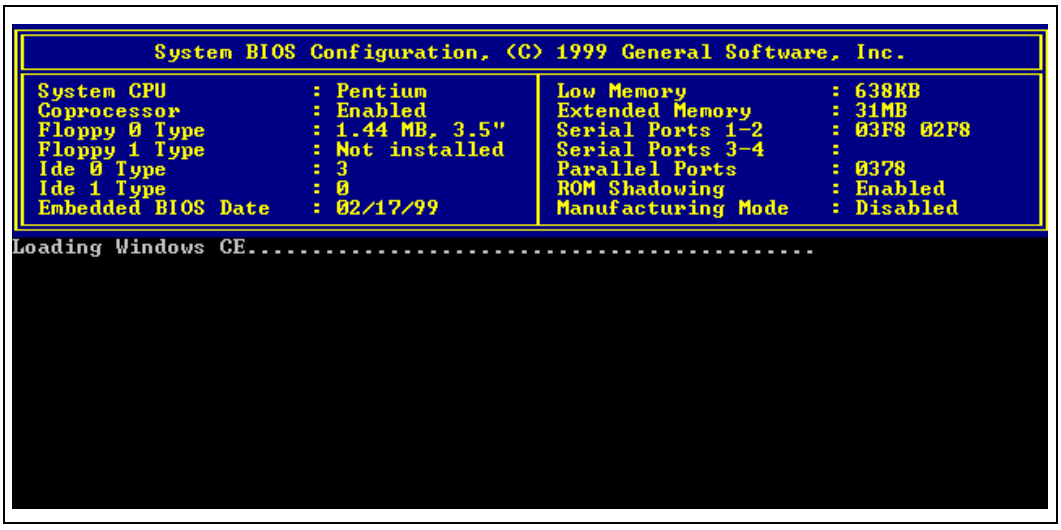
Caution: HYPERTERMINAL's default setting is to use flow control, which will render the console inoperative. To change this, create a new session, change the flow control setting to "none", save the session, and exit HYPERTERMINAL. Then reinvoke HYPERTERMINAL with the session and it will operate with the new flow control setting.

5.11.2 CE-Ready Windows CE Loader

Your system's BIOS is "CE-Ready" and can directly boot Windows CE* without loading an intermediate operating system such as DOS and LOADCEPC. Instead, the NK.BIN file can be placed on a disk drive or drive emulator, and then the BIOS can be configured through the Basic CMOS Configuration Setup Screen to boot the NK.BIN file from the boot drives instead of the boot records on those drives.

To configure your system to boot Windows CE natively from a disk drive, set the "Boot Method" field to "Windows CE" in the Basic CMOS Configuration Setup Screen. Then, place a copy of NK.BIN suitable for execution by LOADCEPC in the root directory of your normal boot drive, such as drive C:. Then, reboot the system. The configuration box should be displayed (Figure 5-9), and immediately following should be the message "Loading Windows CE…" followed by a series of dots, indicating that the loading process is continuing. Once fully loaded, Windows CE takes over the system and runs using the standard PC keyboard, screen, and PS/2 mouse.

Figure 5-9. CE-Ready Boot Feature

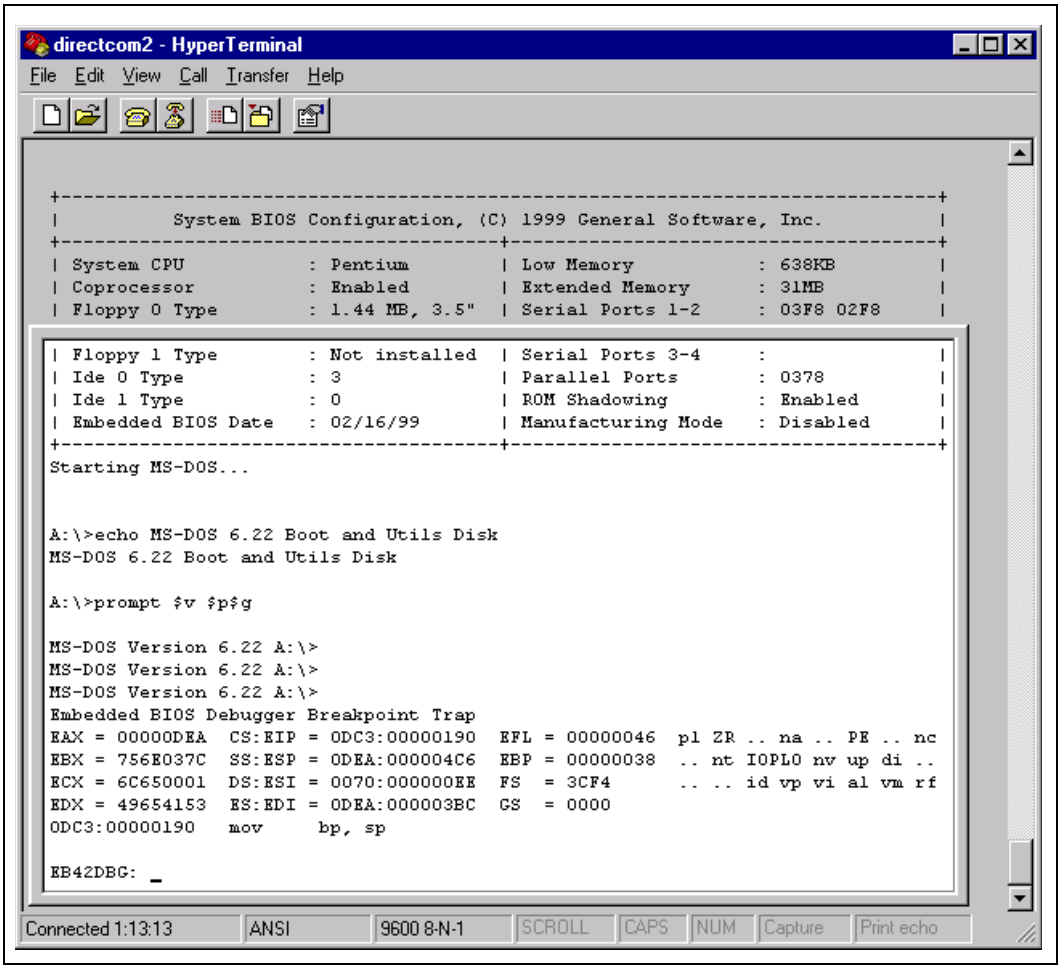


5.11.3 Integrated BIOS Debugger

The system's BIOS contains a built-in debugger that can be a valuable tool to aid the board bring-up process on new designs similar to the evaluation board. It supports a DOS SYMDEB-style command line interface, and can be used on the main console's keyboard and screen, or over a redirected connection to a terminal program (see "Console Redirection" on page 5-10).

To activate the debugger at any time from the main console, press the left shift and the control keys together. A display similar to the one in the HYPERTERMINAL session below (Figure 5-10) will appear, containing the title, “Embedded BIOS Debugger Breakpoint Trap” and a snapshot of the processor general registers.

Figure 5-10. Integrated BIOS Debugger Running Over a Remote Terminal



To leave the debugger and resume the interrupted activity (whether POST, BIOS, DOS, Windows, or an application program), enter the “G” command (short for “go”) and press ENTER. If you were at a DOS prompt when you entered the debugger, then DOS will still be waiting for its command, and will not prompt again until you press ENTER again.

The debugger can also be entered from the Setup Screen System, and as a boot activity (see “Basic CMOS Configuration Screen” on page 5-4), as a last ditch effort during board bring-up and development if no bootable device is available.

If your version of DOS, an application, or any OEM-supplied BIOS extensions have debugging code (i.e., “INT 3” instructions) remaining, then these will invoke the debugger automatically, although this is not an error. To continue, use the “G” command. When Embedded BIOS is adapted by the OEM, the debugger can be removed from the final production BIOS, and superfluous debugging code in the application will not cause the debugger to be invoked.

A complete discussion of the debugger is beyond the scope of this chapter; however, complete documentation is available from General Software via the web at http://www.gensw.com.

5.12 Embedded BIOS POST Codes

Embedded BIOS writes progress codes, also known as POST codes, to I/O port 80H during POST, in order to provide information to OEM developers about system faults. These POST codes may be monitored on the on-board Post Code Debugger located at U12 and U13. They are not displayed on the screen. For more information about POST codes, contact General Software.

Mnemonic Code	Code	System Progress Report
POST_STATUS_START	00h	Start POST (BIOS is executing).
POST_STATUS_CPUTEST	01h	Start CPU register test.
POST_STATUS_DELAY	02h	Start power-on delay.
POST_STATUS_DELAYDONE	03h	Power-on delay finished.
POST_STATUS_KBDBATRDY	04h	Keyboard BAT finished.
POST_STATUS_DISABSHADOW	05h	Disable shadowing & cache.
POST_STATUS_CALCCKSUM	06h	Compute ROM CRC, wait for KBC.
POST_STATUS_CKSUMGOOD	07h	CRC okay, KBC ready.
POST_STATUS_BATVRFY	08h	Verifying BAT command to KB.
POST_STATUS_KBDCMD	09h	Start KBC command.
POST_STATUS_KBDDATA	0ah	Start KBC data.
POST_STATUS_BLKUNBLK	0bh	Start pin 23,24 blocking & unblocking.
POST_STATUS_KBDNOP	0ch	Start KBC NOP command.
POST_STATUS_SHUTTEST	0dh	Test CMOS RAM shutdown register.
POST_STATUS_CMOSDIAG	0eh	Check CMOS checksum.
POST_STATUS_CMOSINIT	0fh	Initialize CMOS contents.
POST_STATUS_CMOSSTATUS	10h	Initialize CMOS status for date/time.
POST_STATUS_DISABDMAINT	11h	Disable DMA, PICs.
POST_STATUS_DISABPORTB	12h	Disable Port B, video display.
POST_STATUS_BOARD	13h	Initialize board, start memory bank detection.
POST_STATUS_TESTTIMER	14h	Start timer tests.
POST_STATUS_TESTTIMER2	15h	Test 8254 T2, for speaker, port B.
POST_STATUS_TESTTIMER1	16h	Test 8254 T1, for refresh.
POST_STATUS_TESTTIMER0	17h	Test 8254 T0, for 18.2Hz.
POST_STATUS_MEMREFRESH	18h	Start memory refresh.
POST_STATUS_TESTREFRESH	19h	Test memory refresh.
POST_STATUS_TEST15US	1ah	Test 15usec refresh ON/OFF time.
POST_STATUS_TEST64KB	1bh	Test base 64KB memory.
POST_STATUS_TESTDATA	1ch	Test data lines.
POST_STATUS_TESTADDR	20h	Test address lines.
POST_STATUS_TESTPARITY	21h	Test parity (toggling).
POST_STATUS_TESTMEMRDWR	22h	Test Base 64KB memory.
POST_STATUS_SYSINIT	23h	Prepare system for IVT initialization.
POST_STATUS_INITVECTORS	24h	Initialize vector table.
POST_STATUS_8042TURBO	25h	Read 8042 for turbo switch setting.
POST_STATUS_POSTTURBO	26h	Initialize turbo data.
POST_STATUS_POSTVECTORS	27h	Modification of IVT.
POST_STATUS_MONOMODE	28h	Video in monochrome mode verified.
POST_STATUS_COLORMODE	29h	Video in color mode verified.
POST_STATUS_TOGGLEPARITY	2ah	Toggle parity before video ROM test.
POST_STATUS_INITBEFOREVIDEO	2bh	Initialize before video ROM check.

POST_STATUS_VIDEOROM	2ch	Passing control to video ROM.
POST_STATUS_POSTVIDEO	2dh	Control returned from video ROM.
POST_STATUS_CHECKEGAVGA	2eh	Check for EGA/VGA adapter.
POST_STATUS_TESTVIDEOMEMORY	2fh	No EGA/VGA found, test video memory.
POST_STATUS_RETRACE	30h	Scan for video retrace signal.
POST_STATUS_ALTDISPLAY	31h	Primary retrace failed.
POST_STATUS_ALTRETRACE	32h	Alternate found.
POST_STATUS_VRFYSWADAPTER	33h	Verify video switches.
POST_STATUS_SETDISPMODE	34h	Establish display mode.
POST_STATUS_CHECKSEG40A	35h	Initialize ROM BIOS data area.
POST_STATUS_SETCURSOR	36h	Set cursor for power-on msg.
POST_STATUS_PWRONDISPLAY	37h	Display power-on message.
POST_STATUS_SAVECURSOR	38h	Save cursor position.
POST_STATUS_BIOSIDENT	39h	Display BIOS identification string.
POST_STATUS_HITDEL	3ah	Display "Hit <DEL> to ..." message.
POST_STATUS_VIRTUAL	40h	Prepare protected mode test.
POST_STATUS_DESCR	41h	Prepare descriptor tables.
POST_STATUS_ENTERVM	42h	Enter virtual mode for memory test.
POST_STATUS_ENABINT	43h	Enable interrupts for diagnostics mode.
POST_STATUS_CHECKWRAP1	44h	Initialize data for memory wrap test.
POST_STATUS_CHECKWRAP2	45h	Test for wrap, find total memory size.
POST_STATUS_HIGHPATTERNS	46h	Write extended memory test patterns.
POST_STATUS_LOWPATTERNS	47h	Write conventional memory test patterns.
POST_STATUS_FINDLOWMEM	48h	Find low memory size from patterns.
POST_STATUS_FINDHIMEM	49h	Find high memory size from patterns.
POST_STATUS_CHECKSEG40B	4ah	Verify ROM BIOS data area again.
POST_STATUS_CHECKDEL	4bh	Check for <DEL> pressed.
POST_STATUS_CLREXTMEM	4ch	Clear extended memory for soft reset.
POST_STATUS_SAVEMEMSIZE	4dh	Save memory size.
POST_STATUS_COLD64TEST	4eh	Cold boot: Display 1st 64KB memtest.
POST_STATUS_COLDLOWTEST	4fh	Cold boot: Test all of low memory.
POST_STATUS_ADJUSTLOW	50h	Adjust memory size for EBDA usage.
POST_STATUS_COLDHITEST	51h	Cold boot: Test high memory.
POST_STATUS_REALMODETEST	52h	Prepare for shutdown to real mode.
POST_STATUS_ENTERREAL	53h	Return to real mode.
POST_STATUS_SHUTDOWN	54h	Shutdown successful.
POST_STATUS_DISABA20	55h	Disable A20 line.
POST_STATUS_CHECKSEG40C	56h	Check ROM BIOS data area again.
POST_STATUS_CHECKSEG40D	57h	Check ROM BIOS data area again.
POST_STATUS_CLRHITDEL	58h	Clear "Hit <DEL>" message.
POST_STATUS_TESTDMAPAGE	59h	Test DMA page register file.
POST_STATUS_VRFYDISPMEM	60h	Verify from display memory.
POST_STATUS_TESTDMA0BASE	61h	Test DMA0 base register.
POST_STATUS_TESTDMA1BASE	62h	Test DMA1 base register.
POST_STATUS_CHECKSEG40E	63h	Checking ROM BIOS data area again.
POST_STATUS_CHECKSEG40F	64h	Checking ROM BIOS data area again.
POST_STATUS_PROGDMA	65h	Program DMA controllers.
POST_STATUS_INITINTCTRL	66h	Initialize PICs.
POST_STATUS_STARTKBDTEST	67h	Start keyboard test.
POST_STATUS_KBDRESET	80h	Issue KB reset command.
POST_STATUS_CHECKSTUCKKEYS	81h	Check for stuck keys.
POST_STATUS_INITCIRCBUFFER	82h	Initialize circular buffer.
POST_STATUS_CHECKLOCKEDKEYS	83h	Check for locked keys.
POST_STATUS_MEMSIZEMISMATCH	84h	Check for memory size mismatch.
POST_STATUS_PASSWORD	85h	Check for password or bypass setup.

```
POST_STATUS_BEFORESETUP      86h  Password accepted.
POST_STATUS_CALLSETUP        87h  Entering setup system.
POST_STATUS_POSTSETUP        88h  Setup system exited.
POST_STATUS_DISPPWRON        89h  Display power-on screen message.
POST_STATUS_DISPWAIT         8ah  Display "Wait..." message.
POST_STATUS_ENABSHADOW       8bh  Shadow system & video BIOS.
POST_STATUS_STDCMOSSETUP     8ch  Load standard setup values from CMOS.
POST_STATUS_MOUSE            8dh  Test and initialize mouse.
POST_STATUS_FLOPPY           8eh  Test floppy disks.
POST_STATUS_CONFIGFLOPPY     8fh  Configure floppy drives.
POST_STATUS_IDE              90h  Test hard disks.
POST_STATUS_CONFIGIDE        91h  Configure IDE drives.
POST_STATUS_CHECKSEG40G      92h  Checking ROM BIOS data area.
POST_STATUS_CHECKSEG40H      93h  Checking ROM BIOS data area.
POST_STATUS_SETMEMSIZE       94h  Set base & extended memory sizes.
POST_STATUS_SIZEADJUST       95h  Adjust low memory size for EBDA.
POST_STATUS_INITC8000        96h  Initialize before calling C800h ROM.
POST_STATUS_CALLC8000        97h  Call ROM BIOS extension at C800h.
POST_STATUS_POSTC8000        98h  ROM C800h extension returned.
POST_STATUS_TIMERPRNBASE     99h  Configure timer/printer data.
POST_STATUS_SERIALBASE       9ah  Configure serial port base addresses.
POST_STATUS_INITBEFORENPX    9bh  Prepare to initialize coprocessor.
POST_STATUS_INITNPX          9ch  Initialize numeric coprocessor.
POST_STATUS_POSTNPX          9dh  Numeric coprocessor initialized.
POST_STATUS_CHECKLOCKS       9eh  Check KB settings.
POST_STATUS_ISSUEKBDID       9fh  Issue keyboard ID command.
POST_STATUS_RESETID          0a0h KB ID flag reset.
POST_STATUS_TESTCACHE        0a1h Test cache memory.
POST_STATUS_DISPSOFTERR      0a2h Display soft errors.
POST_STATUS_TYPEMATIC        0a3h Set keyboard typematic rate.
POST_STATUS_MEMWAIT          0a4h Program memory wait states.
POST_STATUS_CLRSCR           0a5h Clear screen.
POST_STATUS_ENABPTYNMI       0a6h Enable parity and NMIs.
POST_STATUS_INITE000         0a7h Initialize before calling ROM at E000h.
POST_STATUS_CALLE000         0a8h Call ROM BIOS extension at E000h.
POST_STATUS_POSTE000         0a9h ROM extension returned.
POST_STATUS_DISPCONFIG       0b0h Display system configuration box.
POST_STATUS_INT19BOOT        00h  Call INT 19h bootstrap loader.
POST_STATUS_LOWMEMEXH        0b1h Test low memory exhaustively.
POST_STATUS_EXTMEMEXH        0b2h Test extended memory exhaustively.
POST_STATUS_PCIENUM          0b3h Enumerate PCI busses.
```

5.13 Embedded BIOS Beep Codes

Embedded BIOS tests much of the system hardware early in POST before messages can be displayed on the screen. When system failures are encountered at these early stages, POST uses beep codes (a sequence of tones on the speaker) to identify the source of the error.

The following is a comprehensive list of POST beep codes for the system BIOS. BIOS extensions, such as VGA ROMs and SCSI adapter ROMs, may use their own beep codes, including short/long sequences, or possibly beep codes that sound like the ones below. When diagnosing a system failure, remove these adapters if possible before making a final determination of the actual POST test that failed.

Mnemonic Code	Beep Count	Description of Problem
POST_BEEP_REFRESH	1	Memory refresh is not working.
POST_BEEP_PARITY	2	Parity error found in 1st 64KB of memory.
POST_BEEP_BASE64KB	3	Memory test of 1st 64KB failed.
POST_BEEP_TIMER	4	T1 timer test failed.
POST_BEEP_CPU	5	CPU test failed.
POST_BEEP_GATEA20	6	Gate A20 test failed.
POST_BEEP_DMA	7	DMA page/base register test failed.
POST_BEEP_VIDEO	8	Video controller test failed.
POST_BEEP_KEYBOARD	9	Keyboard test failed.
POST_BEEP_SHUTDOWN	10	CMOS shutdown register test failed.
POST_BEEP_CACHE	11	External cache test failed.
POST_BEEP_BOARD	12	General board initialization failed.
POST_BEEP_LOWMEM	13	Exhaustive low memory test failed.
POST_BEEP_EXTMEM	14	Exhaustive extended memory test failed.
POST_BEEP_CMOS	15	CMOS restart byte test failed.
POST_BEEP_ADDRESS_LINE	16	Address line test failed.
POST_BEEP_DATA_LINE	17	Data line test failed.
POST_BEEP_INTERRUPT	18	Interrupt controller test failed.
POST_BEEP_PASSWORD	1	Incorrect password used to access SETUP.

Using Different Processors in the Board A

The Intel Pentium® III Processor/840 Development Kit board supports processor side bus (PSB) frequencies of 100 MHz and 133 MHz (with processor speeds up to 866 MHz). By default, the board's PSB operates at 133 MHz. Follow these steps to configure the board to support a 100 MHz PSB:

1. Completely remove power from the board.
2. **Obtain 100 MHz PSB processors.** The processors included with the kit operate at 133 MHz. You must obtain processors that operate at 100 MHz.
3. **Remove the 133 MHz PSB processors.** To do this, remove the fans from each processor. Lift the bar on the side of the PGA370 sockets to release the processors. Carefully lift the processors out of their sockets.
4. **Install the 100 MHz PSB processors on the motherboard.** Insert the 100 MHz PSB processors into the sockets. Be sure to align the pins correctly. Secure the bar on the side of the socket and replace the fans.
5. **Reconfigure jumpers.** Place a jumper across pins 1 and 2 on jumper J2L1. Place another jumper across pins 2 and 3 on jumper J2K1. See Figure 2-1 on page 2-8 for jumper locations. This configures the board to run at 100 MHz.
6. **Power up the system.** The system will now operate with a PSB frequency of 100 MHz.

To order processors with a 100 MHz PSB frequency, contact your local Intel field representative.

Termination Chip for Uniprocessor Systems B

If the system is designed as a dual-processor system, but only one processor is implemented (for testing purposes or for applications that require only one processor), a termination chip is required in the unpopulated socket. The following are third-party suppliers of termination chip solutions:

FCI Electronics
Contact: Scott Beardsley
(510) 651-2700 x479
beardssb@bergelect.com

Methode
Contact: Jackie Muller
(708) 867-9600
jmuller@methode.com

PLD Code Listing C

```
--********************************************
-- Altera design file
--********************************************

TITLE  "port80";
SUBDESIGN port80
(
   LFRAME_N, PCI_RST_N,HEX_CLK  : input;
   AGP_CLK,SERR_N   : input;
   LAD[3..0]                      : bidir;
   LO_OUT[6..0]                  : output;
   HI_OUT[6..0]                  : output;
   LSERR_N              : bidir;
   LED_RESET          : output;

)

variable
 LED_SEL[1..0] : wire;
 PRE_LED[1..0] : wire;
 pre_LSERR_N : wire;
 PRE_LO_OUT[6..0] : wire;
 PRE_HI_OUT[6..0] : wire;
 dlad : dff;
 control : dff;
 dout : dff;
 data_low[3..0]: dff;
 data_high[3..0] : dff;
 hex : machine with states
(my_reset,IDLE,ADDR3,ADDR2,ADDR1,ADDR0,DIN_LOW,DIN_HIGH,
                TARIN1,TARIN2,TAROUT1,TAROUT2,SYNC_RDY
                );
ss: MACHINE WITH STATES ( s1,s2,s3,s4);

begin
 ss.clk = AGP_clk;
CASE ss IS
      WHEN s1 =>
         if SERR_N == GND
             THEN ss = s2;
         else ss = s1;
         end if;
        pre_LSERR_N = VCC;
      WHEN s2 =>
         ss = s3;
         pre_LSERR_N = GND;
      WHEN s3 =>
         ss = s4;
         pre_LSERR_N = GND;
      WHEN s4 =>
         ss = s1;
         pre_LSERR_N = GND;
```

```
      WHEN others =>
         ss = s1;
        pre_LSERR_N = GND;
  end case;
LSERR_N = OPNDRN(pre_LSERR_N);
LO_OUT[6]=OPNDRN(PRE_LO_OUT[6]);
LO_OUT[5]=OPNDRN(PRE_LO_OUT[5]);
LO_OUT[4]=OPNDRN(PRE_LO_OUT[4]);
LO_OUT[3]=OPNDRN(PRE_LO_OUT[3]);
LO_OUT[2]=OPNDRN(PRE_LO_OUT[2]);
LO_OUT[1]=OPNDRN(PRE_LO_OUT[1]);
LO_OUT[0]=OPNDRN(PRE_LO_OUT[0]);

HI_OUT[6]=OPNDRN(PRE_HI_OUT[6]);
HI_OUT[5]=OPNDRN(PRE_HI_OUT[5]);
HI_OUT[4]=OPNDRN(PRE_HI_OUT[4]);
HI_OUT[3]=OPNDRN(PRE_HI_OUT[3]);
HI_OUT[2]=OPNDRN(PRE_HI_OUT[2]);
HI_OUT[1]=OPNDRN(PRE_HI_OUT[1]);
HI_OUT[0]=OPNDRN(PRE_HI_OUT[0]);

-- **********************************
-- ADDED TO CONTROL FLASHING ACPI LEDS
-- BWF 11/18/98
-- Removed 6/23 for Tioga B0

#LED_SEL[1]=SLP_S3;
#LED_SEL[0]=SLP_S5_N;
#LED_S3=PRE_LED[1];
#LED_S5=PRE_LED[0];


#CASE LED_SEL[1..0] IS
 # WHEN B"00" => PRE_LED[1..0] = B"11";
 # WHEN B"01" => PRE_LED[1..0] = B"11";
 # WHEN B"10" => PRE_LED[1..0] = B"10";
 # WHEN B"11" => PRE_LED[1..0] = B"01";
#END CASE;
--************************************


-- **********************************
-- ADDED TO CONTROL PCI_Reset to LEDs
-- BWF 01/13/99
-- Made chnges to acf file for correct pin out
LED_RESET=not PCI_RST_N;
--************************************


CASE data_low[3..0] IS
    WHEN H"0" => PRE_LO_OUT[6..0] = B"0111111";
    WHEN H"1" => PRE_LO_OUT[6..0] = B"0000110";
    WHEN H"2" => PRE_LO_OUT[6..0] = B"1011011";
    WHEN H"3" => PRE_LO_OUT[6..0] = B"1001111";
    WHEN H"4" => PRE_LO_OUT[6..0] = B"1100110";
    WHEN H"5" => PRE_LO_OUT[6..0] = B"1101101";
    WHEN H"6" => PRE_LO_OUT[6..0] = B"1111101";
```

```
    WHEN H"7" => PRE_LO_OUT[6..0] = B"0000111";
    WHEN H"8" => PRE_LO_OUT[6..0] = B"1111111";
    WHEN H"9" => PRE_LO_OUT[6..0] = B"1101111";
    WHEN H"a" => PRE_LO_OUT[6..0] = B"1110111";
    WHEN H"b" => PRE_LO_OUT[6..0] = B"1011110";
    WHEN H"c" => PRE_LO_OUT[6..0] = B"0111001";
    WHEN H"d" => PRE_LO_OUT[6..0] = B"1111100";
    WHEN H"e" => PRE_LO_OUT[6..0] = B"1111001";
    WHEN H"f" => PRE_LO_OUT[6..0] = B"1110001";
 end case;

CASE data_high[3..0] IS
    WHEN H"0" => PRE_HI_OUT[6..0] = B"0111111";
    WHEN H"1" => PRE_HI_OUT[6..0] = B"0000110";
    WHEN H"2" => PRE_HI_OUT[6..0] = B"1011011";
    WHEN H"3" => PRE_HI_OUT[6..0] = B"1001111";
    WHEN H"4" => PRE_HI_OUT[6..0] = B"1100110";
    WHEN H"5" => PRE_HI_OUT[6..0] = B"1101101";
    WHEN H"6" => PRE_HI_OUT[6..0] = B"1111101";
    WHEN H"7" => PRE_HI_OUT[6..0] = B"0000111";
    WHEN H"8" => PRE_HI_OUT[6..0] = B"1111111";
    WHEN H"9" => PRE_HI_OUT[6..0] = B"1101111";
    WHEN H"a" => PRE_HI_OUT[6..0] = B"1110111";
    WHEN H"b" => PRE_HI_OUT[6..0] = B"1111111";
    WHEN H"c" => PRE_HI_OUT[6..0] = B"0111001";
    WHEN H"d" => PRE_HI_OUT[6..0] = B"0111111";
    WHEN H"e" => PRE_HI_OUT[6..0] = B"1111001";
    WHEN H"f" => PRE_HI_OUT[6..0] = B"1110001";
 end case;
%   0/a
     __
5/f |  | 1/b   Center is 6/g
     --
4/e |  | 2/c
     --
     3/d
%

LAD[0] = TRI(DOUT,control);
LAD[1] = TRI(DOUT,control);
LAD[2] = TRI(DOUT,control);
LAD[3] = TRI(DOUT,control);
control.clk = hex_clk;
dout.clk = hex_clk;
data_low[3..0].clk = hex_clk;
data_high[3..0].clk = hex_clk;
%
BLNK   = LE_POS;
LE_POS = GND;
%
dlad.clk = hex_clk;
dlad = lad[0]
     # lad[1]
     # lad[2]
     # lad[3]
     # lframe_n;
hex.clk = hex_clk;
```

```
hex.reset = !PCI_RST_N;
case hex IS
when my_reset =>
   if ( (LFRAME_N == vcc)  ) THEN
     hex = my_reset;  -- No cycle
    else hex = IDLE;   -- Cycle is going to start
   end if;
   control = gnd;
   DOUT = DOUT;
   data_low[3..0] = data_low[3..0];
   data_high[3..0] = data_high[3..0];
when IDLE =>
  if  (PCI_RST_N == gnd) THEN
      hex = my_reset;    -- my_reset. Go back to my_reset state
  elsif  (LFRAME_N == gnd) THEN
      hex = IDLE; -- wait for start of a cycle.
  elsif  ( (LFRAME_N == vcc) and ( DLAD == gnd) ) THmEN
              if (  (LAD[3 .. 1] == H"1")  )THEN
                    hex = ADDR3; -- start of a cycle and  cycle is i/o write cycle.
             else hex = my_reset;  -- i/o read cycle OR start of a cycle but cycle
is not i/o cycle.
              end if;
  else hex =  my_reset; -- LFRAME_N went high but not 'start'.MAy be  'reserved', '
bus master grant' etc.
  end if;

      control = gnd;
      DOUT = DOUT;
      data_low[3..0] = data_low[3..0];
      data_high[3..0] = data_high[3..0];

when ADDR3 =>
   if  (LFRAME_N == gnd)  THEN
      hex = my_reset;
   else hex = ADDR2; -- go to next phase of address latching
   end if;

      control = gnd;
      DOUT = DOUT;
      data_low[3..0] = data_low[3..0];
      data_high[3..0] = data_high[3..0];

  when ADDR2 =>
   if  (LFRAME_N == gnd)  THEN
      hex = my_reset;
   else hex = ADDR1; -- go to next phase of address latching
   end if;

      control = gnd;
      DOUT = DOUT; -- dummy
      data_low[3..0] = data_low[3..0];
      data_high[3..0] = data_high[3..0];

  when ADDR1 =>
   if  (LFRAME_N == gnd) THEN
      hex = my_reset;
   elsif (LAD[3 .. 0] == H"8") THEN
```

```
          hex = ADDR0;   -- write cycle at XX2Xh. Go to latch data phase
   else hex = my_reset;
   end if;
control = gnd;
      DOUT = DOUT; -- dummy
      data_low[3..0] = data_low[3..0];
      data_high[3..0] = data_high[3..0];


  when ADDR0 =>
    if  (LFRAME_N == gnd)  THEN
          hex  = my_reset;
    elsif (LAD[3 .. 0] == H"0") THEN
          hex = DIN_LOW;   -- write cycle at XX2Eh. Go to latch data phase
    else hex = my_reset;
    end if;
      control = gnd;
      DOUT = DOUT; -- dummy
      data_low[3..0] = data_low[3..0];
      data_high[3..0] = data_high[3..0];
  when DIN_LOW =>
  if  (LFRAME_N == gnd)  THEN
      hex = my_reset;
  else hex = DIN_HIGH;  -- next phase of latching data
  end if;
control = gnd;
      DOUT = DOUT; -- dummy
      data_low[3..0] = LAD[3..0];
      data_high[3..0] = data_high[3..0];

  when DIN_HIGH =>
  if  (LFRAME_N == gnd)  THEN
      hex = my_reset;
  else hex = TARIN1;
  end if;
data_low[3..0] = data_low[3..0];
      data_high[3..0] = LAD[3..0];
      control = gnd;
      DOUT = DOUT; -- dummy


  when TARIN1 =>
   if  (LFRAME_N == gnd)  THEN
      hex = my_reset;
   else hex = TARIN2;   -- second turnaround phase
   end if;
data_high[3..0] = data_high[3..0];
      data_low[3..0] = data_low[3..0];
      control = gnd;
      DOUT = DOUT; -- dummy


  when TARIN2 =>
   if  (LFRAME_N == gnd)  THEN
        hex = my_reset;
   else hex = SYNC_RDY; -- No wait required in write cycle
   end if;
```

```
control = vcc;
    DOUT = gnd; -- dummy
    data_low[3..0] = data_low[3..0];
    data_high[3..0] = data_high[3..0];



when  SYNC_RDY =>
   if  (LFRAME_N == gnd)  THEN
      hex = my_reset;
    else hex = TAROUT1;
   end if;
control = vcc;
       DOUT = vcc;
       data_low[3..0] = data_low[3..0];
       data_high[3..0] = data_high[3..0];

when TAROUT1 =>
   if  (LFRAME_N == gnd)  THEN
       hex = my_reset;
   else hex = TAROUT2;  -- same flow for read / write
   end if;
control = gnd;
    DOUT = DOUT;
    data_low[3..0] = data_low[3..0];
    data_high[3..0] = data_high[3..0];


when TAROUT2 =>
if  (LFRAME_N == gnd)  THEN
       hex = my_reset;
   else    hex = IDLE;
end if;
 control = gnd;
    DOUT = DOUT; -- dummy
    data_low[3..0] = data_low[3..0];
    data_high[3..0] = data_high[3..0];


when others =>
   if  (LFRAME_N == gnd)  THEN
     hex = my_reset;
   else hex = my_reset;
   end if;
control = gnd;
    DOUT = DOUT; -- dummy
    data_low[3..0] = data_low[3..0];
    data_high[3..0] = data_high[3..0];

 end case;
end;
```

Bill of Materials D

Note: Although Intel has made every effort to select components with a long life expectancy for this reference kit, the availability of any component cannot be guaranteed. Periodic reviews on availability are performed on all components and the product Bill of Materials is updated accordingly. As a result, alternative components may be recommended. Please refer to the Intel Developer website for the latest reference kit update. All product updates (documentation, bill of materials, software releases, etc.), can be found under the product specific websites.

Table D-1 is the bill of materials for the baseboard. Table D-2 is the bill of materials for the system.

Table D-1. Board Bill of Materials (Sheet 1 of 8)

Rev. 1.6

Reference Designator	Description	Manufacturer	Manufacturer Part Number	Alternate Manufacturing Info	All Changes
BH8A1	BATT_HLDR_3PIN, 665005-001	RENATA	HU2032-1		
C1A1,C1A2,C2A1,C2B3,C2B4,C2C3, C2D1-C2D3,C2E2,C2F5,C2L3,C2L4,C 2L6,C2N1,C3C1,C3C2,C3F6,C3F10,C 4C1,C4G1,C4G2,C5A1,C5B4-C5B6,C 5C3,C5C4,C6A1,C6C3,C6F3,C6K1,C6 L2,C6L4,C6M3,C7D1,C7D7,C7G3,C7 G4,C7G7,C7J1,C7K3,C7L2,C8F3,C8G 1,C8H4,C8H5,C8J2,C9E2,C9E3,C9H1 ,C9H3,C9H5,C9J1,C9J3,C9J6,C9M2, C9M3,C9N2,C9P3,C9P4,C10M6,C10 M7,C10P1,C10P2,C10P4	SMC103P_0603, 0.01U, SMC0603, 50V	KEMET	C0603C103K3RAC	KEMET - C0603C103J5RAC	
C1D1,C4P2,C4P3,C5L6,C5L7,C7E1	SMC105P_1206, 1.0U, SMC1206, 16V	TDK	C3216X7R1C105K		
C1D2,C1E6,C1E11,C1E14,C1E15,C1 F2,C1G4,C1H2,C1J1,C1J5,C1K1,C1R 2,C1T2,C1T3,C2A3,C2B2,C2C1,C2C2 ,C2C5,C2D4,C2D5,C2E3,C2F4,C2F6, C2G1-C2G4,C2H2,C2H3,C2H5-C2H7, C2M2,C2R2,C3A3,C3B5,C3D1,C3E1, C3F2,C3F9,C3G1-C3G3,C3L1,C3L4,C 3L5,C3M4,C3M5,C3P2,C3P3,C3R1,C 4A1,C4B2,C4B3,C4F1,C4H3,C4K2,C4 K3,C4L4,C4L6,C4L8,C4R2,C5A2,C5B 1,C5C1,C5D1,C5F2-C5F4,C5G1-C5G 3,C5H1,C5H2,C5K1-C5K3,C5K5,C5L1 ,C5L3,C5L4,C6B1,C6B2,C6F6-C6F8, C6G2,C6G4,C6G5,C6H2-C6H8,C6L1, C6L7,C6L8,C6M1,C6M2,C6M4,C7B1, C7C1,C7D2,C7D5,C7D8,C7F2,C7G1, C7G2,C7G5,C7G6,C7H1-C7H8,C7K1, C7K2,C7K4,C7L3,C7L8,C7T1,C7T2,C 8B1,C8B2,C8C2,C8D1-C8D3,C8H1-C 8H3,C8J1,C8K1-C8K3,C8K5-C8K8,C8 L1,C8L2,C8M1,C8M2,C8N1,C8N2,C8 P1,C8R1-C8R3,C8T1,C8T3,C9A1,C9 B1,C9D1,C9G2,C9H2,C9H4,C9H6,C9 J2,C9J5,C9J7-C9J11,C9K1,C9M4,C9 N1,C9N3,C9P1,C9P5,C9U1,C10A1-C 10A4,C10B1-C10B3,C10J2,C10K2-C1 0K4,C10L1,C10L2,C10L4-C10L8,C10 M1-C10M5,C10M8,C10N2,C10P5,C10 U1-C10U3,C11-12,C12R1,C13-20,C10 0,C102,C104-107,C128-131	SMC104P_0603, 0.1U, SMC0603, 16V	KEMET	C0603C104K4RACTM		
C1D3,C1P1,C1P2,C1R1,C2L5,CN2N, C2R1,C3L2,C3L3,C4R1,C4R4,C5K4,C 6G1,C6L3,C6L5,C6L9,C7D3,C7D4,C7 G8	SMC471P_0805, 470PF, SMC0805, 50V	TDK	C2012C0G1H471K1J		

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C1E2-C1E5,C1E7-C1E10,C1E12,C1E13,C1J2,C1J4,C2D6,C2E5,C2E6,C6L6,C8C1	SMC105P_603, 1.0U, SMC0603, 10V	TDK	C1608Y5V1A105Z		
C1F1,C1F6,C1H1,C2E4,C2H1,C3B1,C3B2,C4B1,C4D1,C4E1,C4K1,C4L12,C5B2,C5B3,C5C2,C5E1,C5F1,C5L2,C5L10,C6C1,C6C2,C6F4,C7D6,C8F2,C8J4,C8K9,C8T2,C8U1,C10G1,C11K1	SMC106P_6032, 10U, SMC6032, 16V	KEMET	T491C106M016A	KEMET - T491C106K016AS	
C1G1,C4J2,C4N2,C12T1	SMC102P_0805, 0.001U, SMC0805, 50V	KEMET	C0805C102K5RAC		
C1G2,C1G3	SMC225_1206, 220UF, SMC_8MM, 10V	PANASONIC	ECEV1AA221P		
C1J3	SMC47P_805, 47PF, SMC0805, 50V	TDK	C2012C0G1H470J		
C6E1	SMC223P_805, 2200PF, SMC0805, 50V	KEMET	C0805C222J5GAC	SYFER - 0805J0500222JXT	
C1L1	SMC152P_1808, 1500PF, SMC1808, 2KV	MURATA	GRM43X7R152K2KV	MURATA - GRM43X7R152KXKVA, AVX - 1808GC152KAT3A	
C1T1,C2A2,C2B1,C2C4,C2F1,C3C3,C3F8,C3P1,C3T1,C6T1,C7C2,C11B1	SMC226P_7343, 22UF, SMC7343, 25V	KEMET	T491D226M025AS	KEMET - T491C226M016AS	
C2E9	SMC474P_1206, 0.47U, SMC1206, 16V	KEMET	C1206C473K5RAC		
C2F2,C2F3	SMC390P_0805, 390P, SMC0805, 50V	TDK	C2012C0G1H391J		
C2H4,C2H9,C6F1,C6F2	SMC220P_805, 22P, SMC0805, 50V	MURATA	GRM39COG220J050A		
C2H8	SMC8_20_0805, 8.2P, SMC0805, 50V	MURATA	GRM40COG8R2C050AD		
C2L1,C2M1,C3F3,C3F7,C4H2,C6J1,C8G3,C8G4,C8J3,C9J4,C9M1,C9M5,C9P2,C10H1,C10J1,C10M9,C10P3,C11M2,C7L5	SMC226P_T6032, 22UF, SMC6032, 16V	KEMET	T491C226M016AS7454		
C2L2, C143	SMC104P_0805, 0.1U, SMC0805, 16V	KEMET	C0805C104K4RACTM		
C2P1,C4H1,C4J1,C4N1,C4N3,C4P1,C5M2,C6G3,C6L10,C7G9,C8G2,C9G1,C10K1,C11L1,C11L2	SMC107P_6032, 100U, SMC7343, 25V	KEMET	T491X107MO16AS		
C2U1,C9T3,C10N1,C10T1-C10T4	SMC107P_7343, 100U, SMC7343, 10V	KEMET	T491D107M010AS7454	KEMET - T491D107K016AS	
C3A1,C3A2,C3B3,C3B4,C3C4,C3C5,C3D2,C3D3,C3E2,C3F1,C3F4,C3F5,C4L1,C4L2	SMC100_0603, 10P, SMC0603, 50V	MURATA	GRM39COG100K050A		
C4K4,C4L5,C4L7,C5L5	SMC220P_603, 22P, SMC0603, 50V	MURATA	GRM39COG220J050A		
C4M1,C4M2,C98,C99	SMC56P_805, 56PF, SMC0805, 50V	TDK	C2012C0G1H560J		
C4R3,C5M1,C5R1,C6M5,C6R1,C7M1,C7R2,C8M3	SMC106P_1210, 10U, SMC1210_35, 16V	MURATA	GRM235Y5V106Z016		
C5N1,C5P1,C6N1,C6P1,C7N1,C7P1,C8N3,C8P2,C9T1,C9T2	SMC827_RDL, 820U, 628955-006, 4V	SANYO	4SP820MB+C3		
C6D1,C137-C140	SMC105P_805, 1.0U, SMC0805, 10V	TDK	C1608Y5V1A105Z		
C6H1,C10L3	FDTHRCAP, 0.1UF, LOWESL_120	TDK	CKD310X7R1C104ST		
C7F1,C9D2,C11M1	SMC225_0805, 2.2UF, SMC0805, 10V	TDK	C2012Y5V1C225ZT		
C8J6,C9E1,C9F1,C9K2,C141	SMC10_1P_0805, 100P, SMC0805	KEMET	C0805C101J5GAC		

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C11E1,C11F1	SMC475P_805, 0.047U, SMC0805, 50V	KEMET	C0805C473K5RAC		
C21,C22	SMC336P_7454, 33UF, SMC7454, 16V	KEMET	T491D336K016AS		
C108-C127,C132-C135,C142	SMC475P_1206, 4.7U, SMC1206, 10V	MURATA	GRM42-6X5R475K016 AL		
CP1A1	SCP1_03P, 1000PF, SMRA1206, 50V	KEMET	C1632C102M5RAC90 45		
CP1B1	SCP5_63P, 5600PF, SMRA1206, 50V	KEMET	C1632C562M5RAC90 45		
CP1J1,CP1L1,CP1L2,CP1N1,CP1N2, CP2P2,CP12R1,CP12R2	SCP4_72P, 470PF, SMRA1206, 50V	KEMET	C1632C471M5RAC90 45		
CP2P1,CP7F1	SCP4_71P, 47PF, SMRA1206, 50V	KEMET	C1632C470M5RAC90 45		
CR1R1	TVS6_2V, 6.2V, SMDA6	MOTOROLA	MMQA6V2T1	MOTOROLA - MMQA6C2T3, PHILIPS - BZA462A, PHILIPS - BZA462A125	
CR2P1,CR10D1,CR12T1	1N4148, SOT23	PHILIPS	PMBD914		
CR7E1,CR7E2	MBRA130LT3, SMD1811	MOTOROLA	MBRA130LT3		
D11N1	LED-RED, LED805	HP	HSMS-H670		
D11P1	LED-GRN, LED805	HP	HSMG-H670		
D12N1	LED-YEL, LED805	HP	HSMY-H670		
FB1E1,FB1J1,FB1J2,FB1K1,FB1K2,F B1P1	FB30OHM3A, 30_OHM, SMF0805	MURATA	BLM21P300SPT		
FB2P1,FB2P2,FB3L1,FB4K1,FB8K1,F B9J1	FB60OHM6A, 60_OHM, SMF1806	MURATA	BLM41P600SPT1		
FP1P1,FP1P2	ACA3216M4-060-, 60_OHM, SMFA1206	TDK	ACA3216M4-060-TL		
J1A1	2X8HDR7	FOXCONN	HC1908G-P8		
J1H1,J1H2	1X4HDR, 663573-001	AMP	104450-3		
J1J1	STEREOJACK, 202205-004	FOXCONN	JA1333L-100		
J1K1	AUDIO2STACK, 202205-003	HOSIDEN	HSJ1001-01-1010		
J1K2	RJ45_CONN	AMP	406549-4		
J1L1,J1N1	DSUB9,302921-001	AMP	787650-2	AMP - 787650-4	
J1M1	DSUB25TALL, 201591-005	FOXCONN	DM1 1356-R1		
J1P1	CONUSB, 642575-001	AMP	787745-1	AMP - 787745-2	
J1P2	PS2STACK, 201377-001	AMP	84405-1		
J1T1-J1T3,J2N1,J2R1,J11A1,J11A2,J1 1B1	HDR1X3FAN, 201581-103	FOXCONN	HF08030-P1		
J1T4	WTX_DIG, CONN8_6505	MOLEX	39-29-9082		
J2F1,J2K1,J6F1,J8F2,J8F3,J8G1,J11, J11N1-J11N3,J11P1-J11P4,J11R1-J11 R3,J11T1	HDR1X3DP, 102276-003	AMP	146225-3		
J2L1,J5L1,J6R2,J7F1,J8F1,J10,J10A1 ,J42	HDR1X2DP, 102276-001	FOXCON	HB1902G		
J3K1	2X15_ITP_1_5V , 509635-030	AMP	104078-4		
J3M1	WTX_MAIN_PWR, CONN24_650	MOLEX	39-28-1243		
J3P1	WTX_PWR, CONN22	MOLEX	39-28-1223		

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J3T1,J7T1	VRM_8_2, VRM8	AMP	146315-1		
J4A1,J4B1	PCI64, 201082-292	AMP	1-145168-2	AMP - 145168-4	
J4D1,J4D2,J4E1,J4F1	CON120_PCI-5V, CONN120_PC	AMP	145154-4		
J4G1	CON_AGP_UNIV, CONAGPU132	AMP	145376-2		
J8H1,J8J1,J10N1,J10N2	RIMM, FM1A_184_T	MOLEX	73811-0301	AMP - 390217-1, MOLEX - 0738111303, FOXCONN - AR09217-S1N	
J10E1,J10F1	2X20HDR20, IDE_2X20, 201418-040	AMP	111971-8	SAMTEC - TST-120-01-L-D-20, FOXCONN - HL09207-D2, AMP - 111685-8, MOLEX - 0872564056	
J10F2	2X17HDR, 201418-234	FOXCONN	HL16176-P4		
J10U1	CONN_2X25_44, AMP_2X25	AMP	146315-1		
J12R1	1X27HDR, 109728-127	FOXCONN	HB1127G-KU7		
L1,L2	COIL, 4.7UH	TDK	MLF2012A4R7K		
L3,L4,L5,L6				Change from Revision 001: Primary part number has been changed from an inductor to a resistor (see item 127.0)	
Q2F1,Q4F1,Q6K1	MMBF170, SOT23	MOTOROLA	MMBF170L		
Q2N1,Q2R1	MMBT2222, SOT23	MOTOROLA	MMBT2222ALT1		
Q4J1,Q4P1,Q5M1,Q8G1,Q9G1,Q11K1	EZ1585CM, TO263F1	SEMTECH	EZ1585CM	SEMTECH - EZ1585ACM	
Q5F1,Q5F2	MOSFETN, SOI8	SILICONIX	SI4410DY-T		
Q7R1	FDV301N, SOT23	FAIRCHILD	FDV301N		
Q8J1,Q8J2,Q8K1,Q8M1,Q9M1,Q9N1, Q11T1	MMBT3904, SOT23	MOTOROLA	MMBT3904L		
R1B1,R1B3	SMR4_71_805, 47, SMR0805	ROHM	MCR10EZH470		
R1B2,R1B4,R1J2,R1J3,R2D4,R2N1,R2N4,R2N9,R2N10,R2R1,R2T1,R3R1,R3R2,R6R1,R6T1,R7F3,R8B1,R8B2,R8F1-R8F3,R8K1-R8K3,R8R1,R9B1,R9C1,R9D2,R9E2,R9E3,R9J3,R9J7,R9N2,R9T1,R9U1,R10P1,R11D4,R11E4	SMR103_805, 10K, SMR0805	ROHM	MCR10EZH103		
R1D1	SMR2_22_1P_805, 220, SMR0805	ROHM	MCR10EZH221		
R1D2	SMR6_812_805, 681, SMR0805	ROHM	MCR10EZHF6810		
R1D3,R2N2,R5L6,R6F1,R7F1,R8J4,R9N1,R10F1,R11C1,R11D1-R11D3,R11E3	SMR102_0805, 1K, SMR0805	ROHM	MCR10EZH102		
R1G1,R3C2,R3D3,R3E1,R3E2,R6D1-R6D3,R34-37,R67	SMR3_31_805, 33, SMR805	ROHM	MCR10EZH330		
R1H1	SMR6_192_805, 619, SMR0805	ROHM	MCR10EZHF6190		
R1H2	SMR5_492_805, 549, SMR0805	ROHM	MCR10EZHF5490		
R1J1,R1J4	SMR11_805, 10, SMR0805	ROHM	MCR10EZH100		
R1J5,R12T2	SMR23_805, 2K, SMR0805	ROHM	MCR10EZH222		

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R1J6,R1K1,R8C1,R11P1,R66,R12N1, R21,R22,R4M3,R5M3	SMR3_32_805, 330, SMR0805	ROHM	MCR10EZH330		
R1N3,R1N4,R2D1-R2D3,R2N5-R2N7, R3D1,R3D2,R3J1,R3K1,R3L2,R3L5,R 3M1,R3N1,R3N2,R3T1,R6T2,R7G2,R 7G6,R8E1,R8G1,R8G2,R8R2,R9C2,R 11L1,R11L4,R11M2,R11M4,R11T1	SMR00_603, 0, SMR0603	ROHM	MCR03EZHJ000		
R2F1,R3E3,R8J1,R8M1,R9D3,R10A1, R10A2	SMR4_73_805, 4.7K, SMR0805	ROHM	MCR10EZH472	ROHM - MCR10EZHJ472	
R2G1	SMR104_805, 100K, SMR0805	ROHM	MCR10EZH104		
R2H1,R2H2,R4J2,R4N1,R7K1,R8L1	SMR1_002_805, 100, SMR0805	ROHM	MCR10EZHF101	ROM - MCR10EZHF1000	
R2J1,R3B1,R3C1,R5L9	SMR2_22_805, 220, SMR0805	ROHM	MCR10EZH221		
R2N3,R2R2	SMR3_574_805, 35.7K, SMR0805	ROHM	MCR10EZHF3572		
R3G1,R3G2,R4G2-R4G8,R5F1,R5G1-R5G9	SMR8_230_805, 8.25K, SMR0805	PANASONIC	ERK-3ELF8251V	DALE - CRCW08058251FT	
R3G3,R4H1,R64	SMR2_23_603, 2.2K, SMR0603	ROHM	MCR03EZH222	Change from Revision 001: Primary part number has been changed from a 2.2K to an 8.2 K resistor for location R3H1 (see item 224.0)	R3H1 part # changed in Rev 1.5, see below
R4F1,R4G1	SMR473_805, 47K, SMR0805	ROHM	MCR10EZH473		
R4J1,R4N2	SMR5_112_805, 511, SMR0805	ROHM	MCR10EZHF5110		
R4K1,R4K2,R4R1,R4R2	SMR2_672_805, 267, SMR0805	ROHM	MCR10EZHF2670		
R4M1,R7T1,R29-R32	SMR3_32_603, 330, SMR0603	ROHM	MCR03EZH331		
R4N3,R40,R41	SMR1_52_805, 150, SMR805	ROHM	MCR10EZH151		
R5H1,R6H1-R6H13,R7H1-R7H7,R7H 9-R7H15,R10K1-R10K5,R10L1-R10L1 6,R10M1-R10M7	SMR2_81_603, 28, SMR0603	ROHM	MCR03EZHF280	ROHM - MCR03EZHF28R0	
R5L1,R5M1,R6L1,R9F2,R10G1,R11K 1	SMR4_222_805, 422, SMR0805	ROHM	MCR10EZHF4220		
R5L2	SMR2_002_603, 200, SMR0603	ROHM	MCR03EZH201		
R5L3,R5L4,R6G1,R7D1,R7D2,R7G3, R7G5,R7G7,R8G3,R8G4,R11L2,R11L 3,R11M1,R11M3	SMR5_621_805, 56.2, SMR0805	ROHM	MCR10EZHF56B2	ROHM - MCR10EZHF56R2	
R5L5,R6L2, R65,L3,L4,L5,L6	SMR5_61_805, 56, SMR0805	ROHM	MCR10EZH560	Change from Revision 001: Locations L3-L6 have been added (these locations were previously populated with a 100 nH inductor)	L3-L6 resistors added in Rev 1.5 (previously populated with 100nH inductor)
R5L7,R5L8,R6G2,R7G4	SMR3_322_805, 332, SMR0805	ROHM	MCR10EZHF3320		
R5M2,R9F3,R10G2,R11K2	SMR9_092_805, 909, SMR0805	ROHM	MCR10EZHF9090		
R6C1,R10D1,R10E1	SMR5_63_805, 5.6K, SMR0805	ROHM	MCR10EZH562		
R6E1,R6E2	SMR106_805, 10M, SMR0805	ROHM	MCR10EZH106		
R6K1,R8K6	SMR4_021_805, 40.2, SMR0805	ROHM	MCR10EZHF40B2		

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R6K2	SMR3_012_805, 301, SMR0805	ROHM	MCR10EZHF3010		
R6L3,R7D5	SMR3_01_603, 30, SMR0805	ROHM	MCR10EZHF31		
R7D3	SMR6_82_603, 680, SMR0603	ROHM	MCR03EZH681		
R7F2,R9C3,R9J1	SMR8_23_805, 8.2K, SMR0805	ROHM	MCR10EZH822		
R18,R20,R7G1	SMR1_12_603, 110, SMR0603	ROHM	MCR03EZH111		
R7H8,R11M5	SMR2_23_805, 2.2K, SMR0805	ROHM	MCR10EZH222		
R8D1	SMR7_501_603, 75.1, SMR0603	ROHM	MCR03EZHF751		
R8D2	SMR1_502_603, 150, SMR0603	ROHM	MCR03EZH151		
R8H1,R9B2,R10M8	SMR1_02_805, 100, SMR0805	ROHM	MCR10EZHF101	ROHM - MCR10EZHF1000	
R8H2,R10M9	SMR3_91_805, 39, SMR0805	ROHM	MCR10EZHF39		
R8J2,R8J5,R8K4,R8K5	SMR3_91_603, 39, SMR0603	ROHM	MCR03EZHF390		
R8J3,R8J6,R9K1,R9K2,R26-R28	SMR5_11_603, 51, SMR0603	ROHM	MCR03EZHF510		
R9D1,R9E1,R9F1,R12R1	SMR2_22_603, 220, SMR0603	ROHM	MCR03EZH221		
R9G1,R10J1	SMR5_622_805, 562, SMR0805	ROHM	MCR10EZHF5620	ROHM - MCR10EZHF56520	
R9G3,R10J3	SMR1_622_805, 162, SMR0805	ROHM	MCR10EZHF1620		
R9J2	SMR1_53_805, 15K, SMR0805	ROHM	MCR10EZH153		
R11E1,R11F1,R12T1	SMR4_72_805, 470, SMR0805	ROHM	MCR10EZH471		
R11M6,R11R1	SMR5103_805, 510K, SMR0805	ROHM	MCR10EZH514		
R38,R39	SMR0_805, 0, SMR0805	ROHM	MCR10EZHF31		
RP1A1	SRP2_23, 2.2K, SMRA1206	ROHM	MNR14EOABJ222		
RP1B1,RP1R1,RP3G1,RP5L1,RP5L2, RP8E1,RP8G1	SRP4_73, 4.7K, SMRA1206	ROHM	MNR14EOABJ472		
RP1K1,RP3J4,RP4M1,RP11D1,RP12 T1	SRP3_32, 330, SMRA1206	ROHM	MNR14EOABJ331		
RP1L1,RP6M1,RP8M1,RP45,RP46	SRP7_51, 75, SMRA1206	ROHM	MNR14EOABJ750		
RP2B1-RP2B3,RP4B1-RP4B3,RP5A1, RP6B1-RP6B6,RP6D1,RP6E1,RP7B1 -RP7B3,RP7D1,RP7E1,RP7E2,RP9A1 ,RP9D1	SRP8_23, 8.2K, SMRA1206, 202474-071	CTS	7440803822J	KOA - CNK1J4T822J, KOA - CNK1J4TDD822J, DALE - CRA06S0803822JR T5, ROHM - MNR14$OABJ822, ROHM - MNR14FOABJ822, PANASONIC - EXB38V822JA	
RP2F1,RP2G1,RP3E1,RP3F1,RP4F1- RP4F3,RP5E1,RP7E5	SRP2_73, 2.7K, SMRA1206	ROHM	MNR14EOABJ272		
RP2H1	SRP6_24, 62K, SMRA1206	ROHM	MNR14EOABJ623		
RP2H2	SRP3_33, 3.3K, SMRA1206	ROHM	MNR14EOABJ332		

Table D-1. Board Bill of Materials (Sheet 7 of 8)

RP2J1,RP10C1,RP10C2,RP11C1,RP11C2,RP11F1	SRP102, 1K, SMRA1206	ROHM	MNR14EOABJ102		
RP2L1	SRP2_02, 220, SMRA1206	ROHM	MNR14EOABJ221	Change from Revision 001: Location RP3J3 has been changed - it will no longer be populated with this part (see item 223.0)	RP3J3 part # changed in Rev 1.5, see below
RP3J2,RP4M2,RP4M3	SRP1_52, 150, SMRA1206	ROHM	MNR14EOABJ151		
RP4K1,RP4K2,RP4L1,RP5K1,RP5K2,RP9F1	SRP2_21, 22, SMRA1206	ROHM	MNR14EOABJ220		
RP7E3,RP10A1	SRP1_54, 15K, SMRA1206	ROHM	MNR14EOABJ153		
RP7E4	SRP1_51, 15, SMRA1206	PANASONIC	EXB-38V150JV		
RP8T1,RP8T2	SRP5_12, 510, SMRA1206	ROHM	MNR14EOABJ511		
RP11E1	SRP3_31, 33, SMRA1206	ROHM	MNR14EOABJ330		
S11P1	SW_PB_SPST_BLK, 2PIN-SW	ALCO	TP11CGPC0		
S11R1	SW_PB_SPST_RED, 2PIN-SW	ALCO	TP11CGPC2		
SP11R1	SPKR, 201826-001	DB	DBX-05A	RDI - DMT-1206, RDI - DMT-1206(I), CHALLENGE ELECTRONICS - DBX-05A	
TH1A1	THRMSTR1_1A, 1.1AMP, SMRT1812	RAYCHEM CO	Mini SMDC-110-2		
TH2P1	THRMSTR, 1.1AMP, SMRT1208	RAYCHEM CO	SMD100-2		
TH2P2	THRMSTR2_5A, 2.5AMP, SMRT3525	RAYCHEM CO	SMD250-X	RAYCHEM - SMD250-2	
TP1-TP8,TP11,TP12	TEST_POINT_SM				
TP9,TP10,TP13-TP25	TEST_POINT				
U1E1,U3L1	LM317LM, SOI8	NATIONAL S	LM317LM		
U1F1	AUDIONET, SSOP28_25I	CA MICRO DEVICES	PRN406A	CA MICRO DEVICES - PRN406A/R, CA MICRO DEVICES - PACAC97, IRC - QS013	
U1F2	LM4880, SOI8	NATIONAL S	LM4880M		
U1J1	LF353, SOI8	NATIONAL S	LF353M		
U2E1	AD1881, PQFP48_5MM	ANALOG DEV	AD1881JST		
U2H1	82559, BGA196	INTEL	GD82559ER		
U2K1	XFMR, 644839-001	PULSE ENG	PE68515		
U2L1,U2N1	75LPE185, SSOP24_65M	TEXAS INST	SN75LPE185DBR		
U2L2,U2M1	RCNETWK, 220PF, SSOP24_25I	IRC	QRC1284-232-K-M	CMD - PAC1284-02Q/R	
U2R1	LM324, SOI14	NATIONAL SEMI	LM324AD	NATIONAL SEMI - LM324	
U3H1	AT93C46A, SOI8	ATMEL	AT93C46A-10SC		
U4L1	CK133W, SSOP56_25I	ICS	9250BF-12		
U6D1	P64H, BGA241	INTEL	FW82806AA		

Table D-1. Board Bill of Materials (Sheet 8 of 8)

U7F1	CAMINO_ICH, BGA241	INTEL	FW82801AA		
U7L1	MCH, BGA544	INTEL	FW82840		
U7R1	74LVC74, SOI14	PHILIPS	74LVC74D		
U7T1	NC7SZ125M5, SOT23_5	FAIRCHILD	NC7SZ125M5		
U8D1	SMC_LPC47B27X, PQFP100R_6	SMSC	LPC47B272		
U8J1,U8K1	DRCG, SSOP24_25I	CYPRESS/ICW	W134BH		
U9,U10	CUMINE370_P0, SOCKET, FCPGA370	AMP	916783-2	AMP - 916783-3	
U9B1	GLUECHIP3, SOCKET, PLCC44	AMP-SKT	822275-1		
U9E1	CY2308-2, SOI16	CYPRESS	CY2308SC-2		
U10B1	FWH_40PIN_TSOP, SOCKET, TSOP40_FMS	MERITEC-SK	980020-40-01		
U10C1,U11C1	7SEGDISP, LED14P_FM	HP	HDSP-E103		
U10D1	QS3384, SSOP24_25I	QUALITY SE	QS3384Q		
U11D1	SOCKET	AMP-SKT	822275-1		
U12K1,U12N2	74LVC32, SOI14	TEXAS INST	SN74LVC32D		
U12L1,U12L2	74HC04, SOI14	MOTOROLA	MC74C04AD		
U12M1	74LVC14D, SOI14	PHILIPS	SN74LVC14D	PHILIPS - SN74LVC14A-D	
U12M2	74LVC08, SOI14	TEXAS INST	SN74LVC08D		
U12N1	SN74F07, SOI14	SIGNETICS	N74F07D		
Y1E1	XTAL24_576, 24.576MHZ, SMY49S	CARDINAL C	CSM1A1B2C25024.576	ECLIPTEK - EC25M-24.596M	
Y3H1	XTAL25MHZ , 25MHZ, 673436-003	RALTRON	TT-SMDC-25.00-20-T		
Y4L1	XTAL14_3, 14.318MHZ, SMY49S	RALTRON	630770-003	ECLIPTEK - EC2SM-14.31818M, CITIZEN ELECTRONICS - HCM49-14.31818MBBK	
Y6F1	XTAL4P, 32.768KHZ, 619601-001	EPSON	MC-405-32.768K		
R17,R19	68.1	ROHM	MCR03EZH68B1		
RP3J3	SRP2_02, 62, SMRA1206	ROHM	MNR14EOABJ620	Change from Revision 001: Primary part number for this location has been changed	part # changed in Rev 1.5
R3H1	SMR2_23_603, 8.2K, SMR0603	ROHM	MCR03EZH822	Change from Revision 001: Primary part number for this location has been changed	part # changed in Rev 1.5

Table D-2. Key Components Bill of Materials

Rev. 1.0

Description	Manufacturer	Part #
840 Scalable Performance Board Development Kit baseboard	Intel	EIAP3840DEVBD
Intel® Pentium® III Processor at 866 MHz with 256K L2 (Qty2)	Intel	RB80526PZ866256
Thermal Solution (Qty 2)	Agilent Technologies	Arcti-Cooler HACA-0001
400MHZ RIMM, PC-800 (Qty 2)	Samsung	KMMR18R84AC1-RK8
Continuity Module (CRIMMs) (Qty 2)	Samsung	KMMR18CNTY1
Glue Chip	Mitel	GSC90031
BIOS Flash Memory (8Mbit)	Intel	E82802AC
PLD for port 80h display	Altera	EPM7064SLC44-7
Voltage Regulator Module (Qty 2)	Celestica	073-20772-01
Memory D2D	Delta	2S2522A 1
4.3GB Hard disk drive (blank, no OS)	Western Digital	WD153AA
69000 Video Card	Densitron	PCIX690LP

NOTE: *This BOM does not include items such as mounting hardware, packaging material, documentation, etc.

Schematics E

Schematics are provided for the following items listed below. Schematics are available from the Intel Developer's web site in PDF format.

- Block Diagram
- Boot Processor
- Application Processor
- ITP
- VRM
- MCH 1
- MCH 2
- MCH 3
- MCH Support
- Clock Distribution
- Clock Generation
- DRCG
- RIMM CHA Connectors
- RIMM CHB Connectors
- RIMM CHA Term + Decoupling
- RIMM CHB Term + Decoupling
- Power Management Map
- Power Distribution Map
- Power Connectors / Power Good
- Power Management Logic
- 1.5 V/1.8 V Regulators
- VCC_CMOS / 2.5 V / 3.3 V Regulators
- Temp / Voltage Monitoring
- WOL / FAN Headers
- AGP 4X
- PCI / Interrupt Diagram
- ICH
- ICH Support / Decoupling
- PCI Slot #1
- PCI Slot #2

- PCI Slot #3
- PCI Slot #4
- PCI Pullups
- P64H
- PCI64 Slot #1
- PCI64 Slot #2
- PCI64 Pullups and Decoupling
- Ethernet 82559ER
- Ethernet 82559ER Connector and Decoupling
- IDE
- USB
- FWH
- LPC/Gameport
- Floppy/KBD/Mouse
- Serial Parallel Ports
- Front Panel I/O
- HL Debug/Port 80
- Spare Logic
- Audio Codec 97
- Audio Net
- Audio Line In/Line Out/Mic In
- PCB Mounting Holes

Intel (R) Pentium (R) III Processor / 840 Development Board Schematics

REV B
2000

Contents

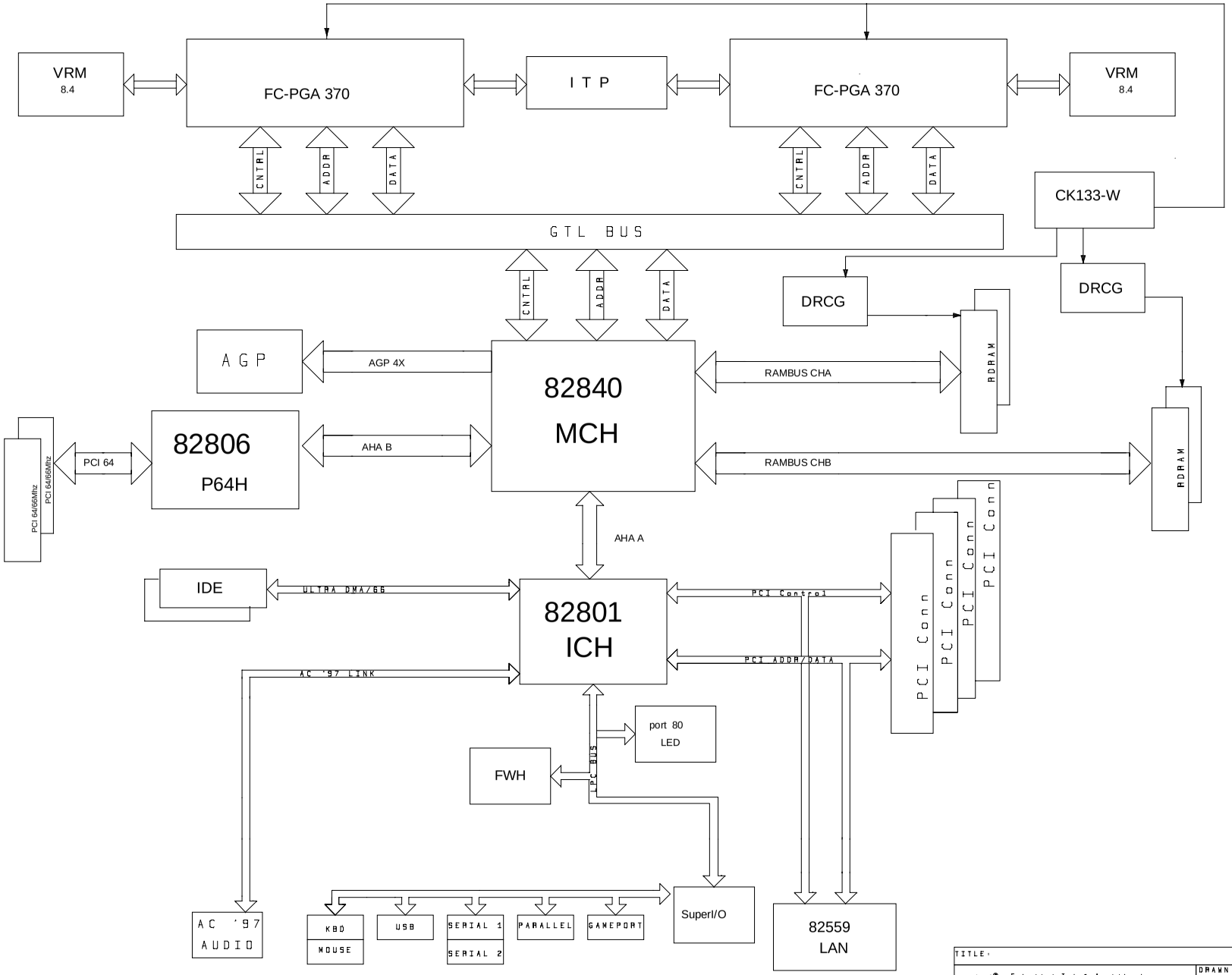
PAGE	DESCRIPTION		
1	Title Page	42	USB
2	Block Diagram	43	FWH
3	Boot Processor	44	LPC / Gameport
4	Application Processor	45	Floppy / KBD / Mouse
5	ITP	46	Serial Parallel Ports
6	VRM	47	Front Panel I/O
7	MCH 1	48	Port 80
8	MCH 2	49	Spare Logic
9	MCH 3	50	Audio Codec 97
10	MCH Support	51	Audio Net
11	Clock Distribution	52	Audio Line in/line out/Mic in
12	Clock Generation		
13	DRCG		
14	RIMM CHA Connectors		
15	RIMM CHB Connectors		
16	RIMM CHA Term + Decoupling		
17	RIMM CHb Term + Decoupling		
18	Power Management Map		
19	Power Distribution Map		
20	Power Connectors/Power Good		
21	Power Management Logic		
22	1.5v/1.8v Regulators		
23	VCC_CMOS / 2.5v/3.3v Regulators		
24	Temp / Voltage Monitoring		
25	WOL/FAN Headers		
26	AGP 4X		
27	PCI / Interupt Diagram		
28	ICH		
29	ICH Support / Decoupling		
30	PCI Slot #1		
31	PCI Slot #2		
32	PCI Slot #3		
33	PCI Slot #4		
34	PCI Pullups		
35	P64H		
36	PCI64 Slot #1		
37	PCI64 Slot #2		
38	PCI64 Pullups and Decoupling		
39	Ethernet 82559ER		
40	Ethernet 82559ER Connector and Decoupling		
41	IDE		

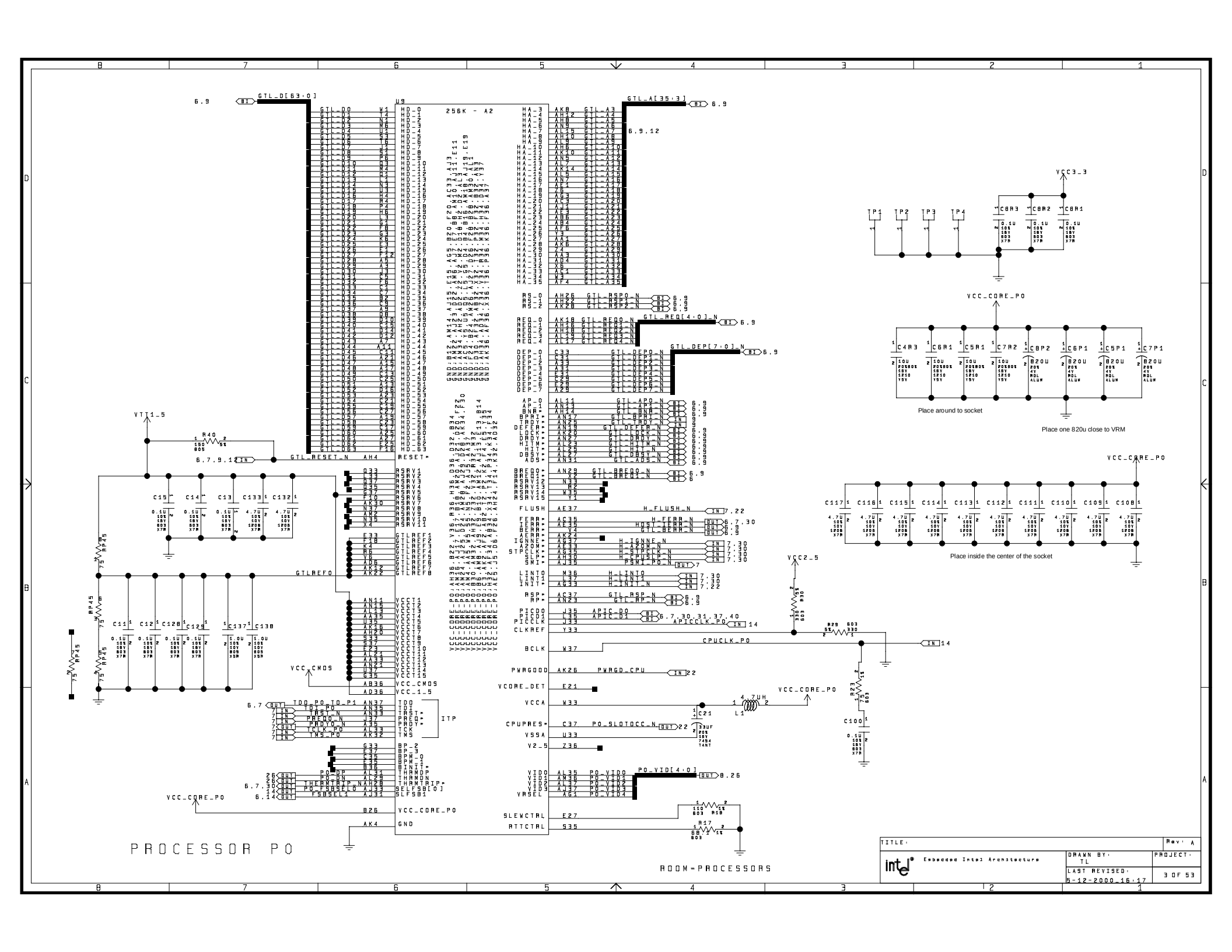
Revision History

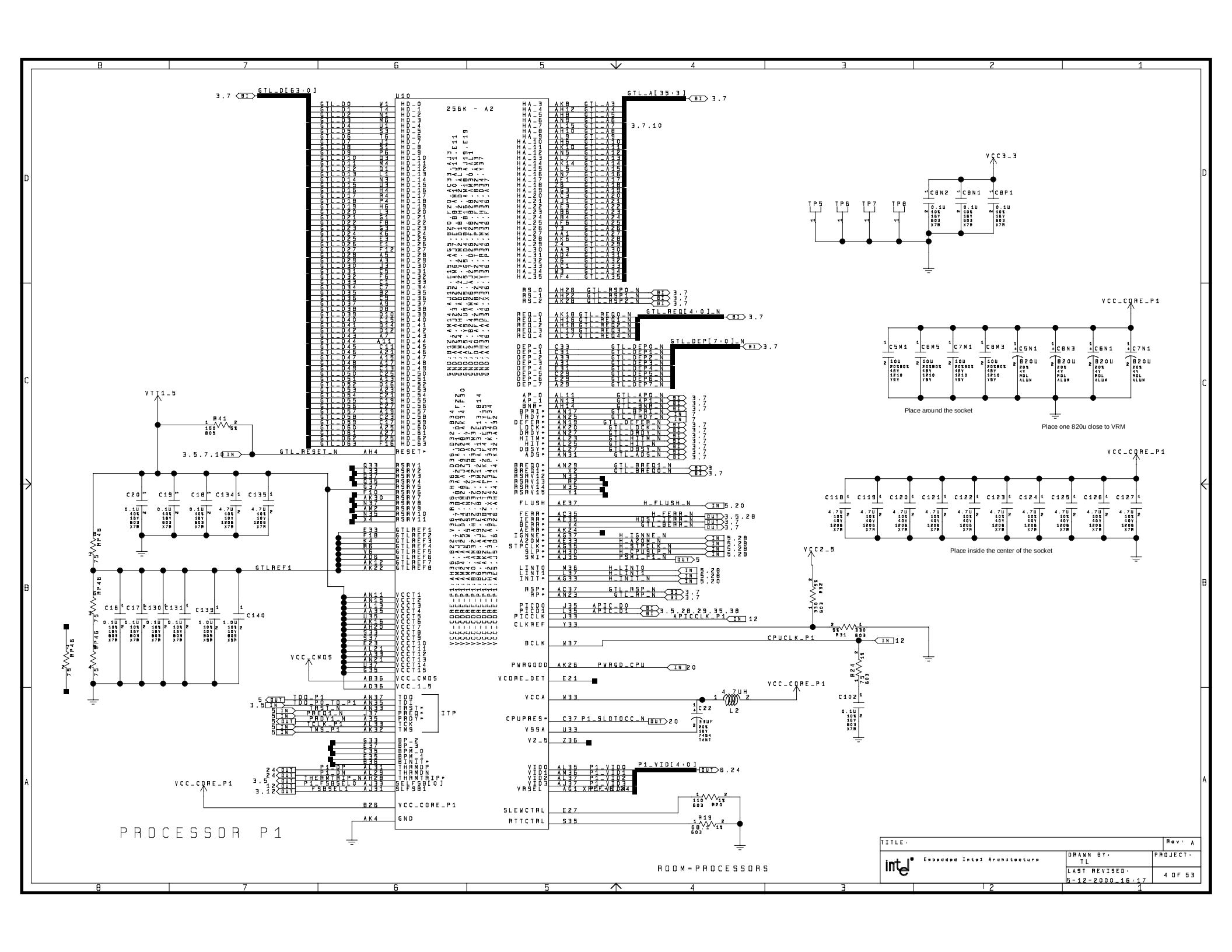
Rev A - Initial release
Rev B - Change ITP to work with American Arium
Change PSB ECC enable

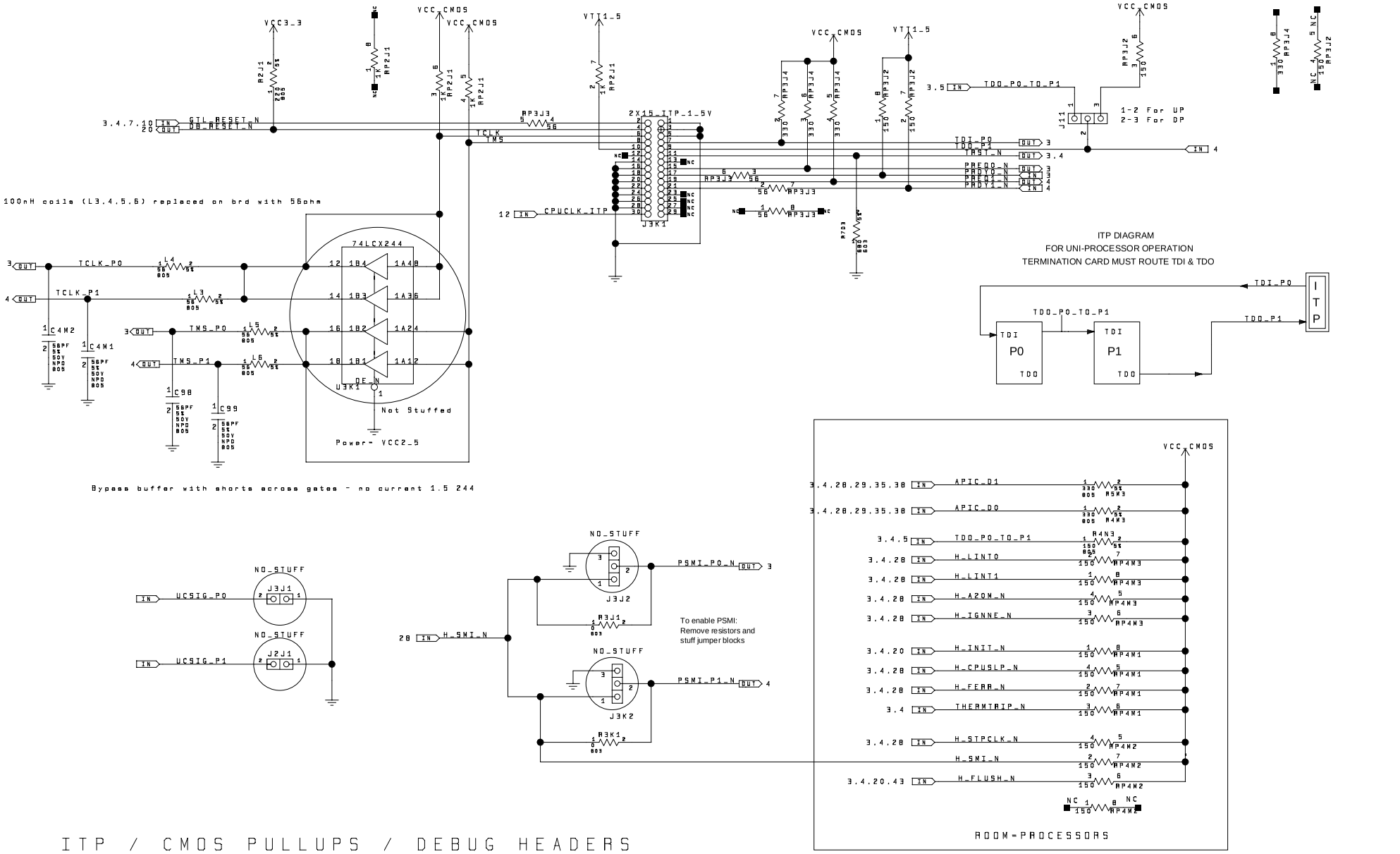
GTLREFA = 2/3 * 1.5V = 1.125V
GTLREFB = 2/3 * 1.5V = 1.125V
HUBREF_ICH= 1/2 * 1.8V = 0.9V
HUBREF_MCH= 1/2 * 1.8V = 0.9V
HUBREF_P64H= 2/3 * 1.8V = 1.35V
CHA_R_VREF= 0.777* 1.8V = 1.4V
CHB_R_VREF=0.777 * 1.8V = 1.4V

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 4-13-2000_11:59	1 OF 53


VRM
8.4
FC-PGA 370
I T P
FC-PGA 370
VRM
8.4
CNTRL
ADDR
DATA
CNTRL
ADDR
DATA
CK133-W
GTL BUS
CNTRL
ADDR
DATA
DRCG
DRCG
RDRAM
A G P
AGP 4X
82840
MCH
RAMBUS CHA
RDRAM
PCI 64/66Mhz
PCI 64/66Mhz
PCI 64
82806
P64H
AHA B
RAMBUS CHB
AHA A
IDE
ULTRA DMA/66
82801
ICH
PCI Control
PCI ADDR/DATA
PCI Conn
PCI Conn
PCI Conn
PCI Conn
AC '97 LINK
port 80
LED
FWH
LPC BUS
AC '97
AUDIO
KBD
MOUSE
USB
SERIAL 1
SERIAL 2
PARALLEL
GAMEPORT
SuperI/O
82559
LAN
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY:
TL
PROJECT:
LAST REVISED:
5-12-2000_16:04
2 OF 53

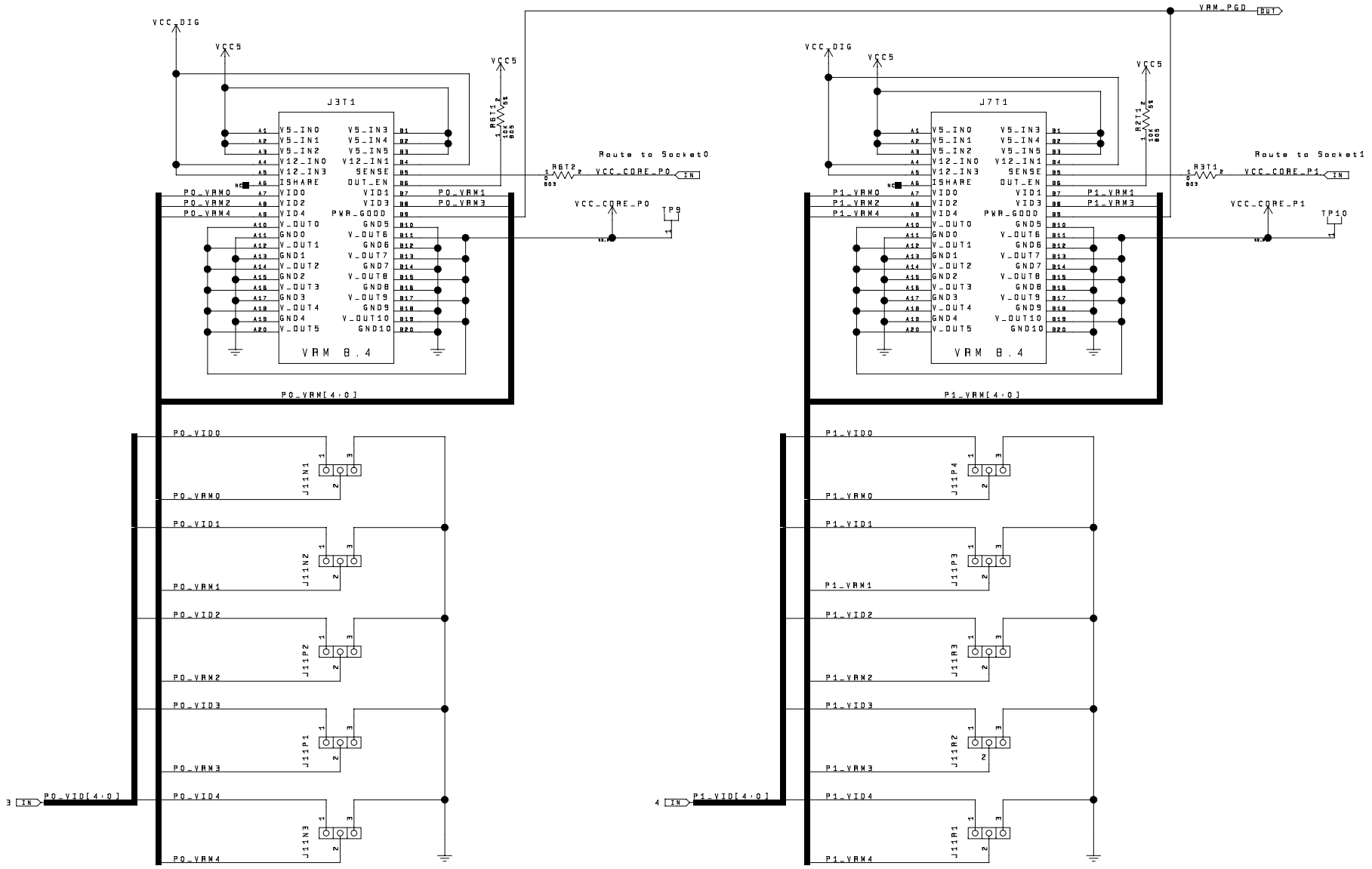

PROCESSOR PO
ROOM=PROCESSORS
Place around to socket
Place one 820u close to VRM
Place inside the center of the socket
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 5-12-2000_16:17
3 OF 53


PROCESSOR P1
Place around the socket
Place one 820u close to VRM
Place inside the center of the socket
ROOM=PROCESSORS
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 5-12-2000_16:17
4 OF 53



ITP / CMOS PULLUPS / DEBUG HEADERS

TITLE:	Rev: A
Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	5 OF 53



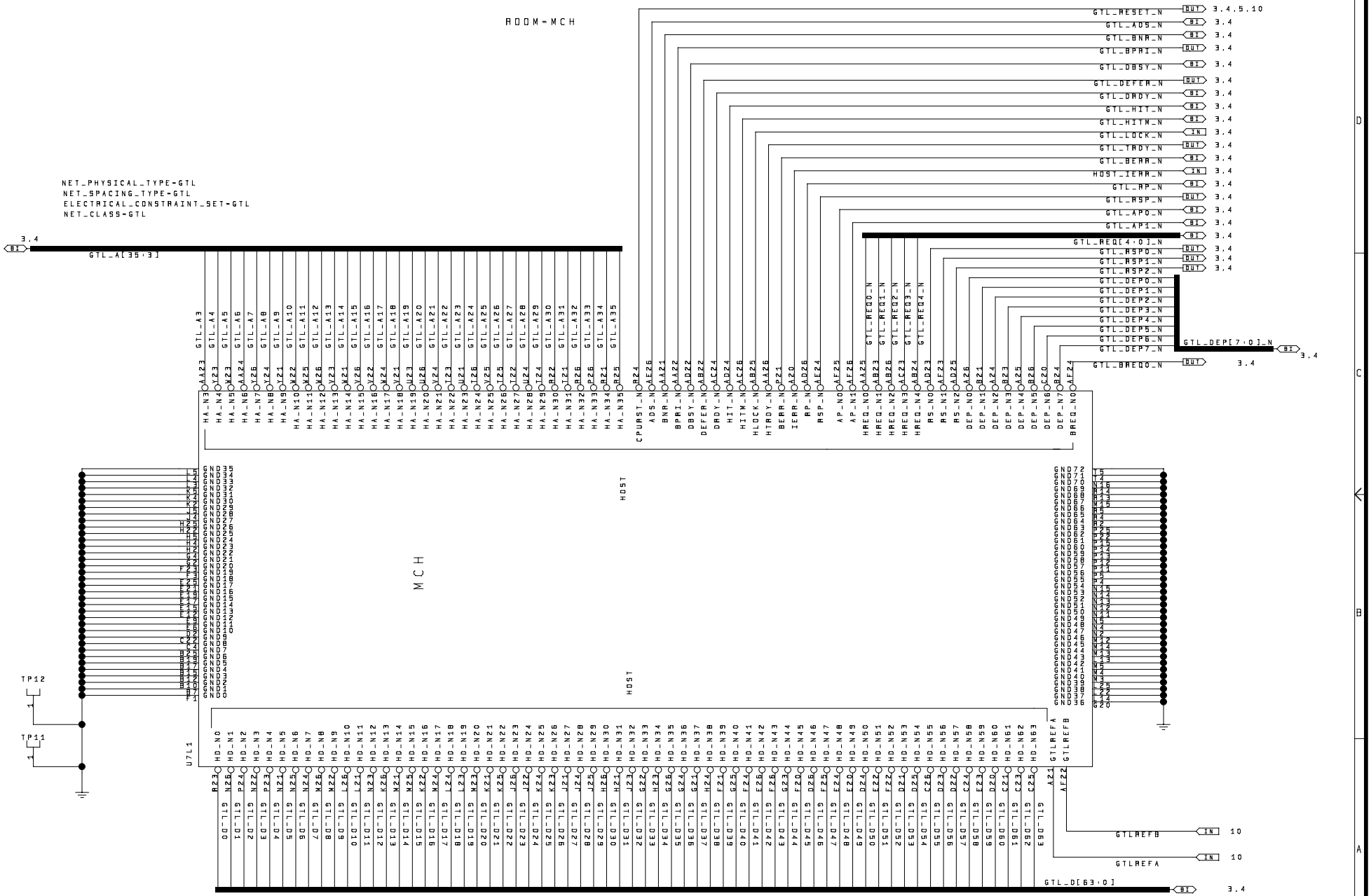
VID4 Must be grounded for production FC_PGA

Jumper position	1-2	2-3	No jumper
VRM VID[4:0]	CPU VID[4:0]	0	1

VRM HEADERS FOR PROCESSOR SOCKETS

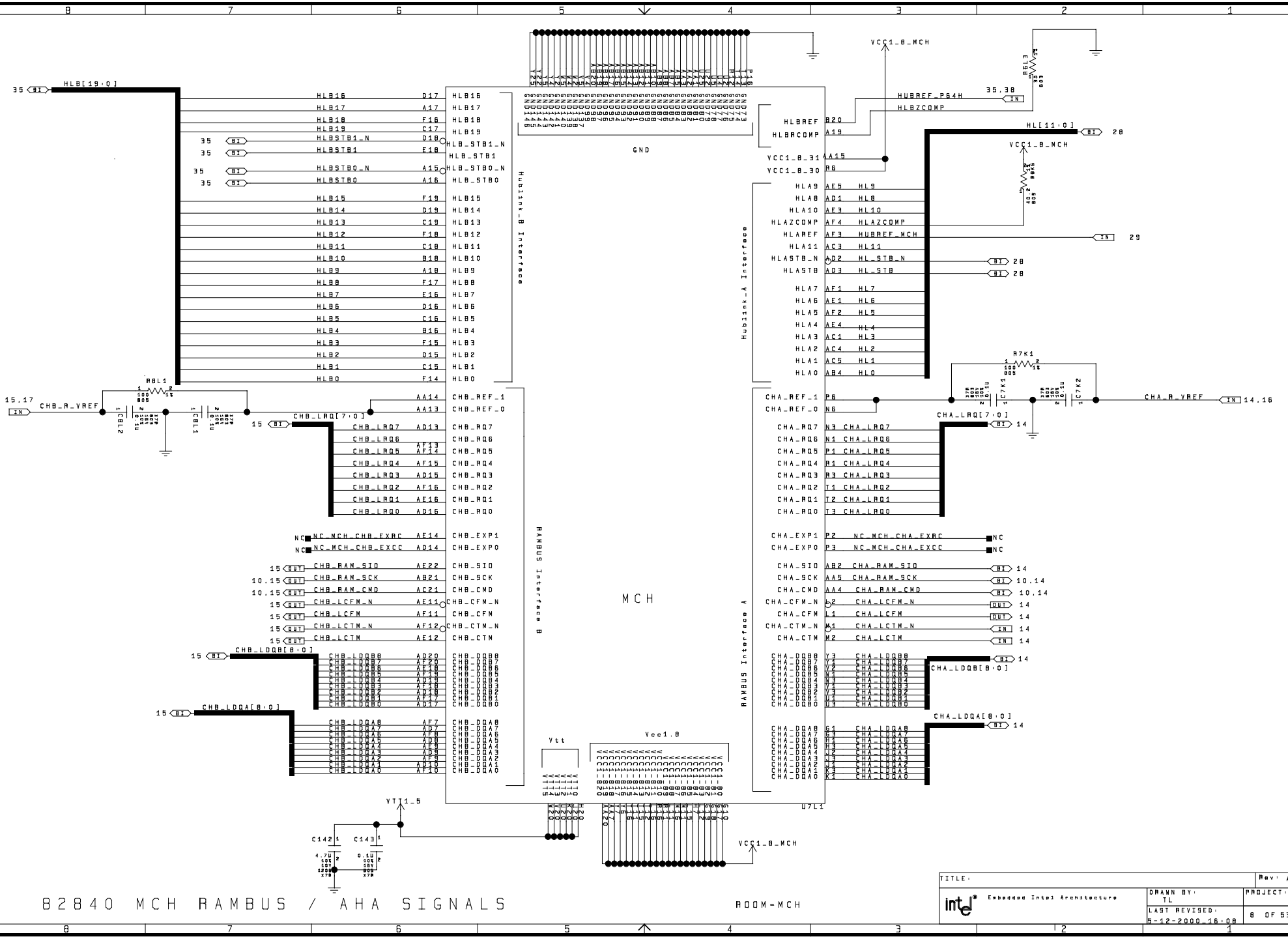
ROOM=VRM

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	6 OF 53



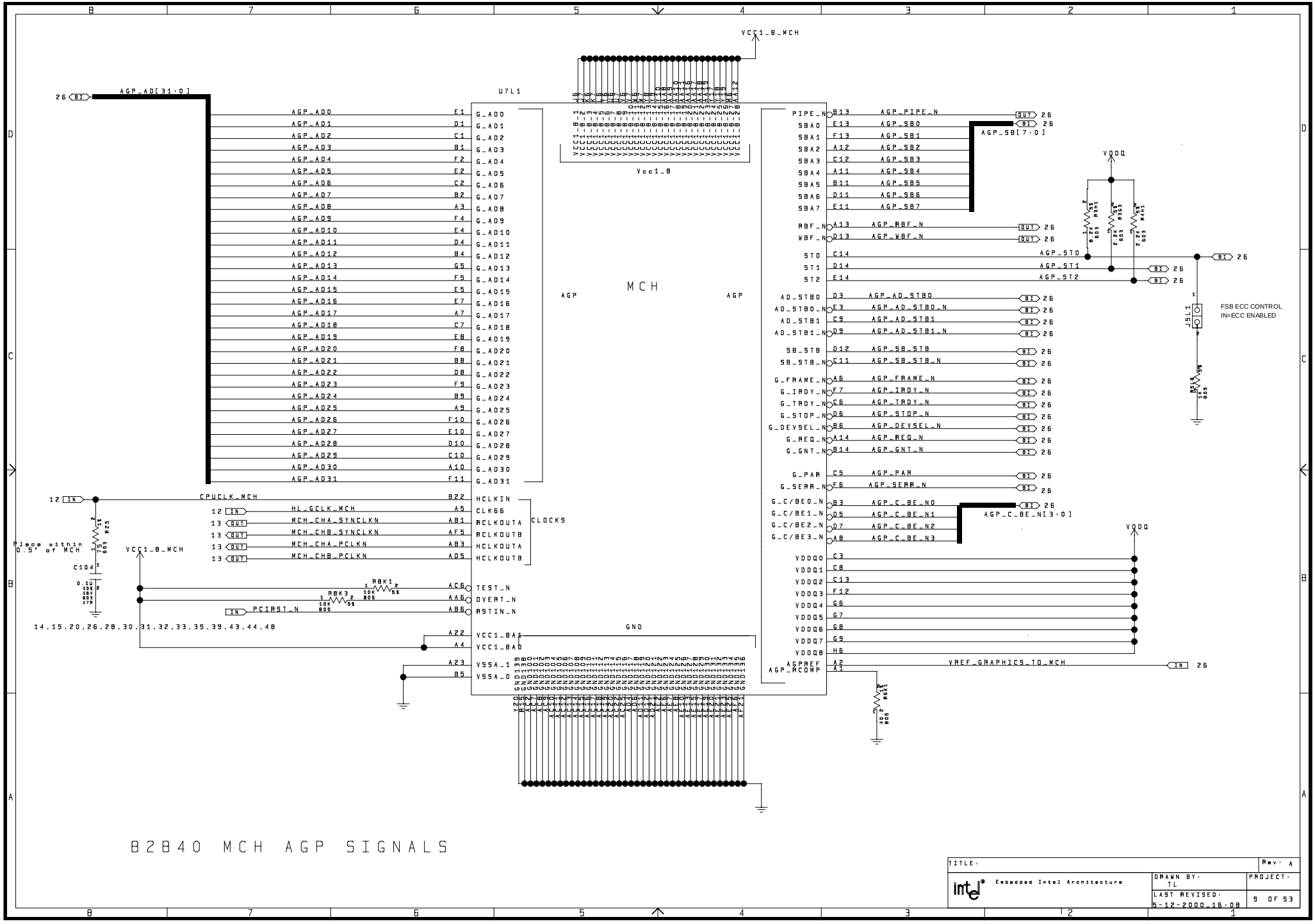
82840 MCH PSB SIGNALS

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:08
	7 OF 53



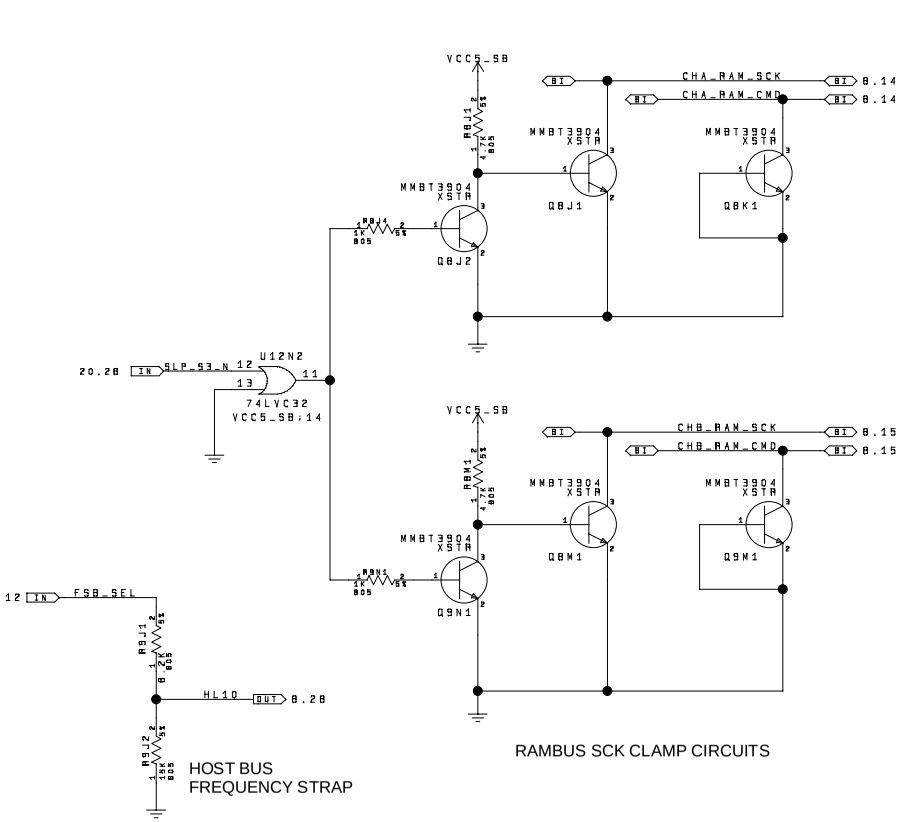
82840 MCH RAMBUS / AHA SIGNALS

TITLE:	Rev: A
intel Embedded Intel Architecture	PROJECT:
DRAWN BY: TL	
LAST REVISED: 5-12-2000_16:08	8 OF 53

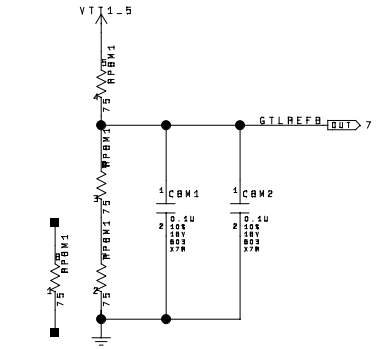


82840 MCH AGP SIGNALS

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	9 OF 53

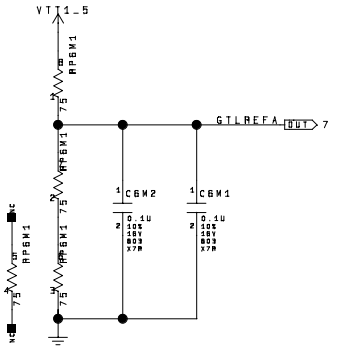


RAMBUS SCK CLAMP CIRCUITS



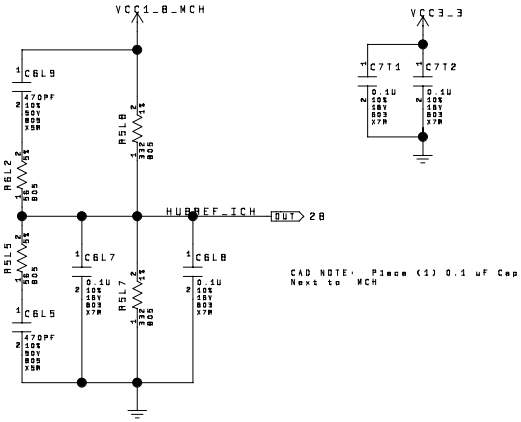
MCH GTLREFB GENERATION

Place close to MCH



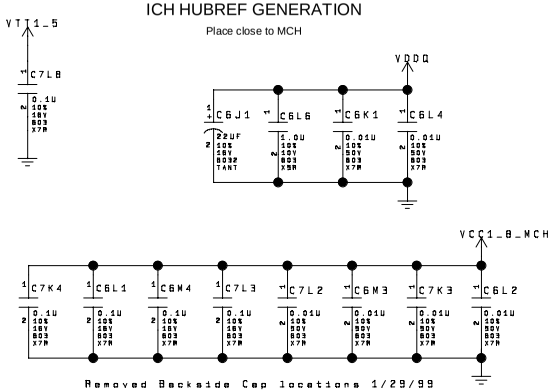
MCH GTLREFA GENERATION

Place close to MCH



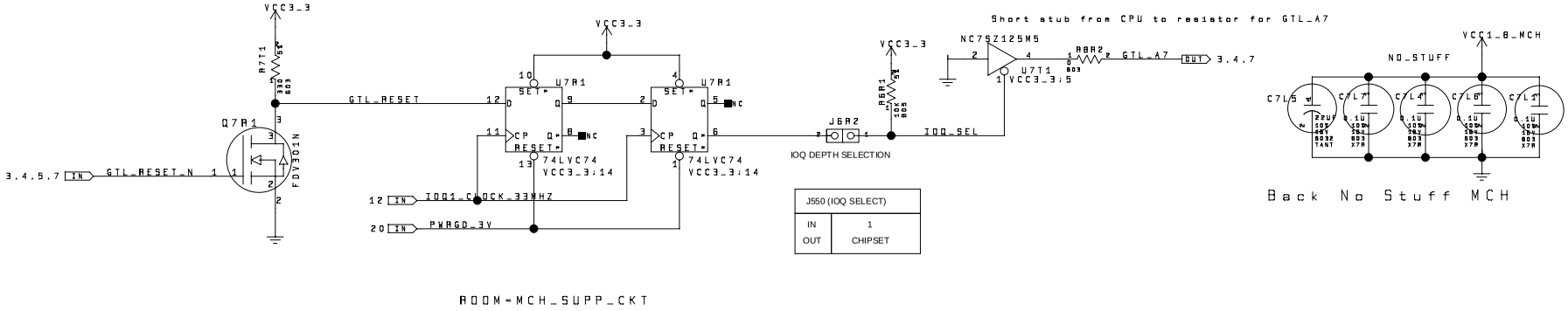
ICH HUBREF GENERATION

Place close to MCH



MCH DECOUPLING

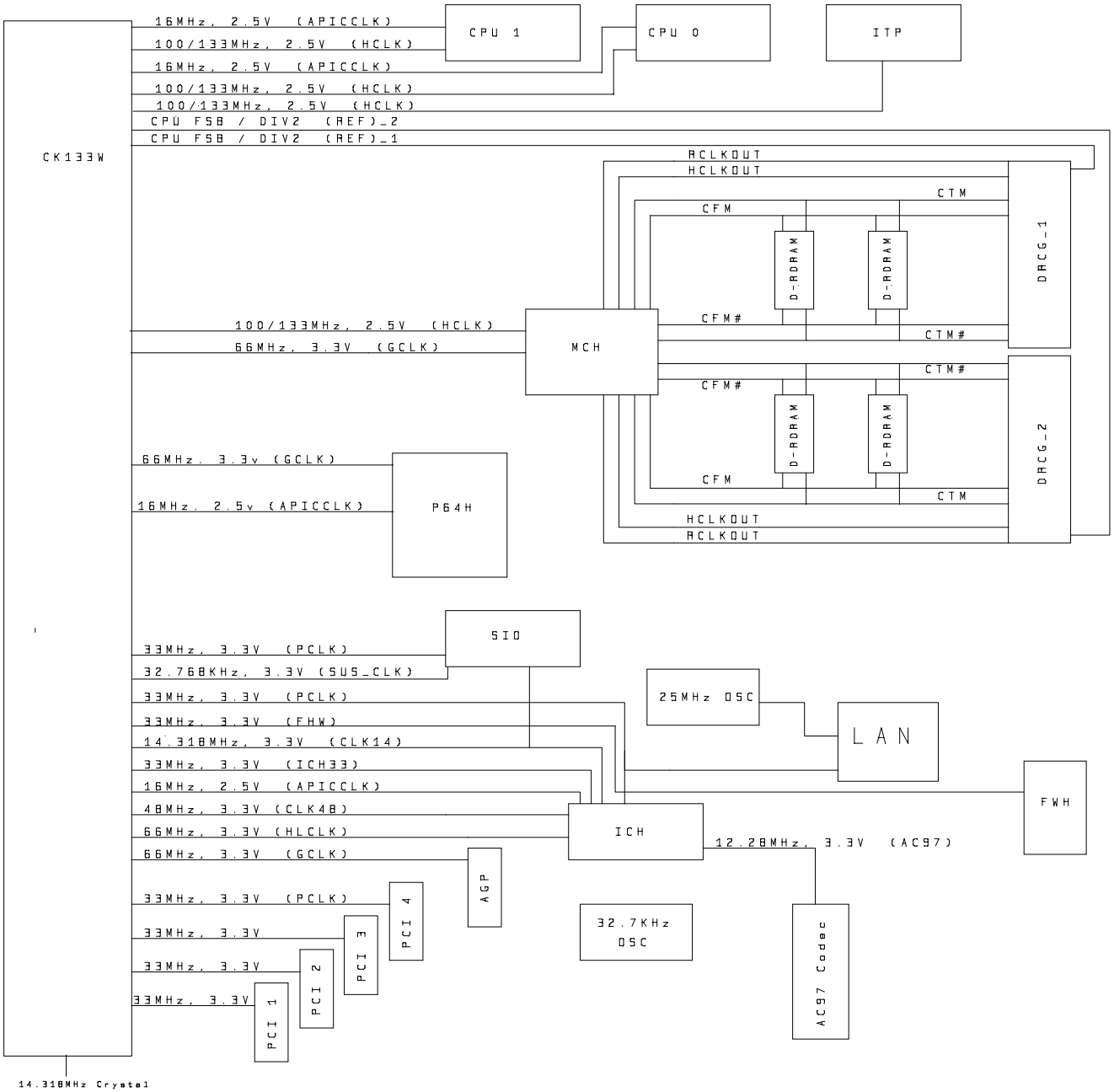
ROOM=MCH



ROOM=MCH_SUPP_CKT

82840 MCH DECOUPLING AND SUPPORT CIRCUITRY

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	10 OF 53



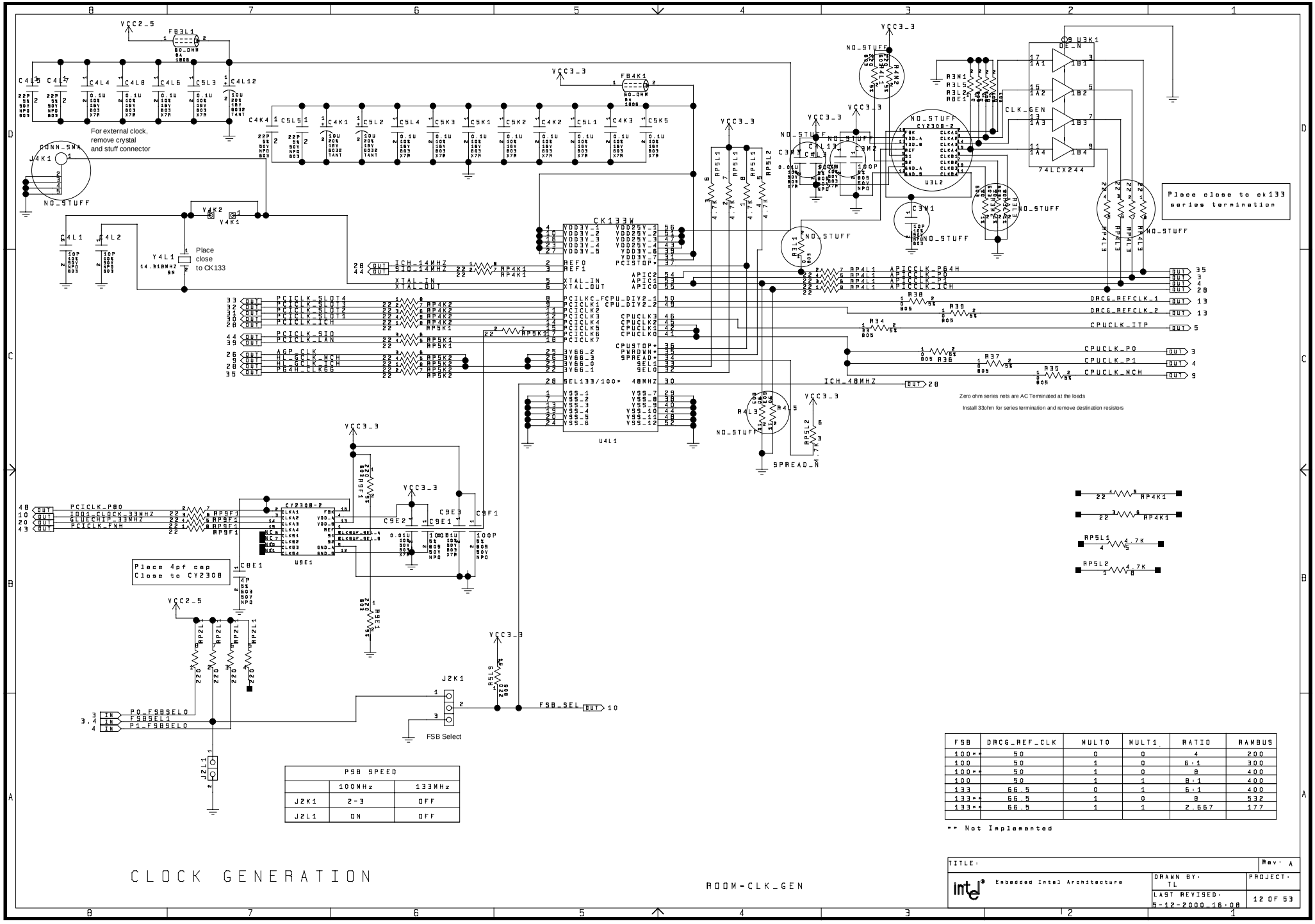
CLOCK DISTRIBUTION

5-12-2000_16:07

NOTES:

HCLK: 100/133MHz Processor & MCH FSB
GCLK: 66MHz, AGP, AHA, P64H
CTM/CFM: 300/400MHz, RDRAM-D, MCH RAC
APICCLK: 16.67MHz, APIC BUS
PCLK: 33MHz, PCI Bus & LPC Bus
CLK48: 48MHz, USB & SIO
CLK14: 14.318MHz, 8254 Timers
RTC: 32.768MHz, ICH
OSC: 14.318, ICH (ACPI Timer)
AC97: 12.288MHz, AC97 Audio Codec
ICH33: 33MHz, ICH (Free Running PCI)

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:07	11 OF 53

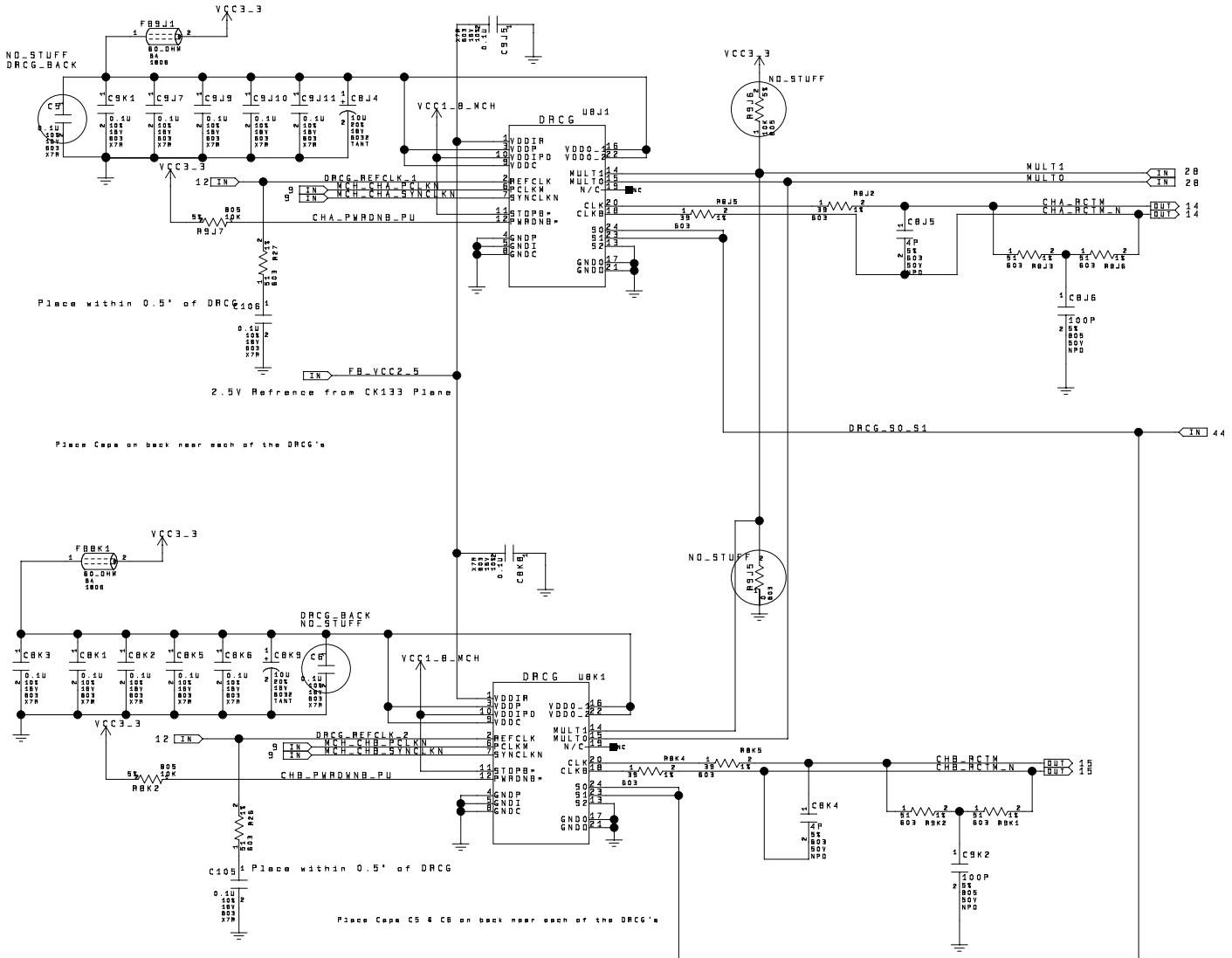


PSB SPEED		
	100MHz	133MHz
J2K1	2-3	OFF
J2L1	ON	OFF

FSB	DACG_REF_CLK	MULT0	MULT1	RATIO	RAMBUS
100**	50	0	0	4	200
100	50	1	0	6:1	300
100**	50	1	0	8	400
100	50	1	1	8:1	400
133	66.5	0	1	6:1	400
133**	66.5	1	0	8	532
133**	66.5	1	1	2.667	177

** Not Implemented

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	12 OF 53



RAMBUS FREQUENCY SELECTION

FSB	DRCG_REF_CLK	MULT0	MULT1	RATIO	RAMBUS
100**	50	0	0	4	200
100	50	0	1	6	300
100**	50	1	0	8	400
100	50	1	1	8:1	400
133	66.5	0	1	6	400
133**	66.5	1	0	8	532
133**	66.5	1	1	2.667	177

** Not Implemented

RAMBUS DRCG MODE CONTROL

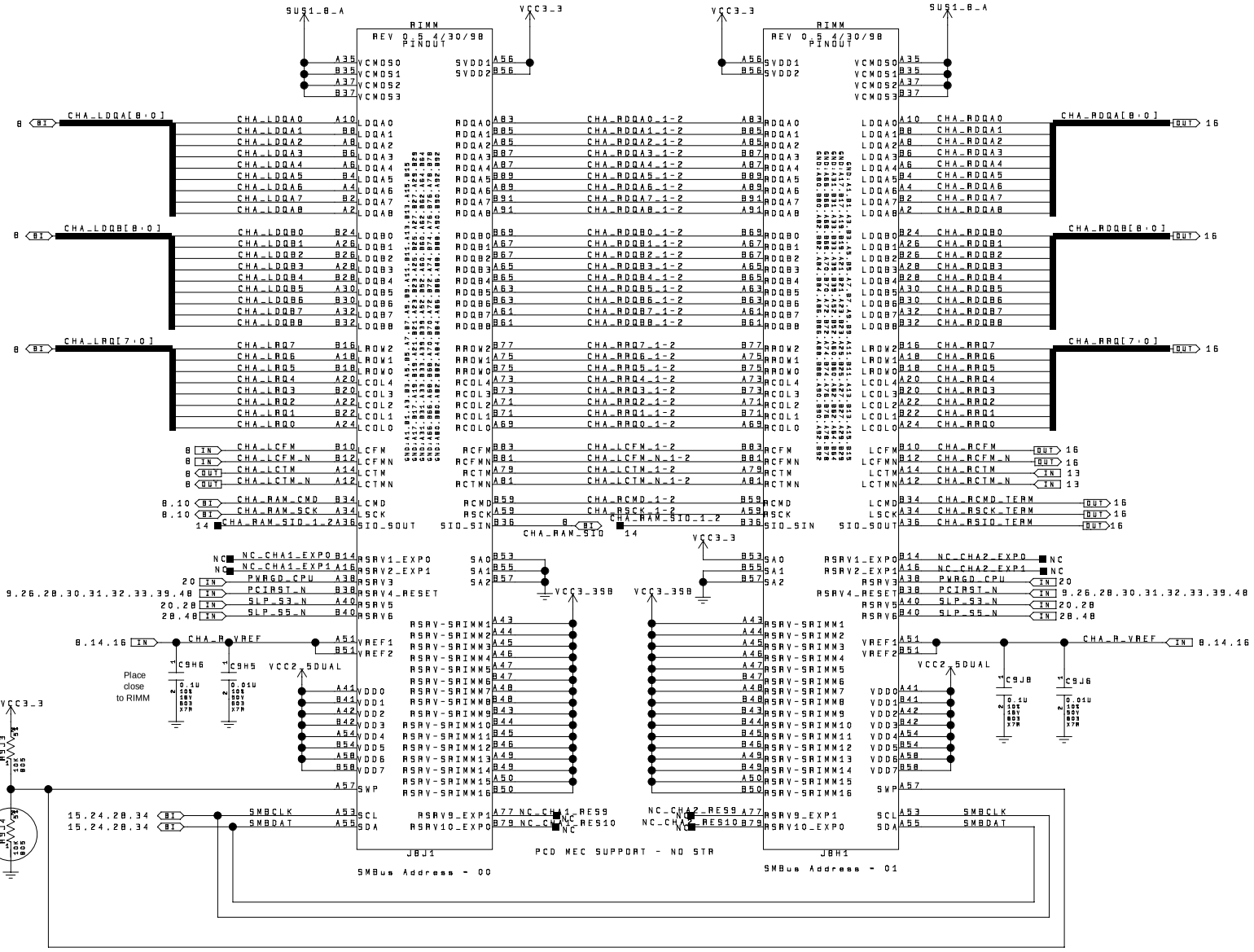
S0	S1	MODE
0	0	Normal
0	1	Output Enable Test
1	0	Bypass
1	1	Test

In Test Mode, Refclk is passed to the outputs

DRCG

ROOM=DRCG

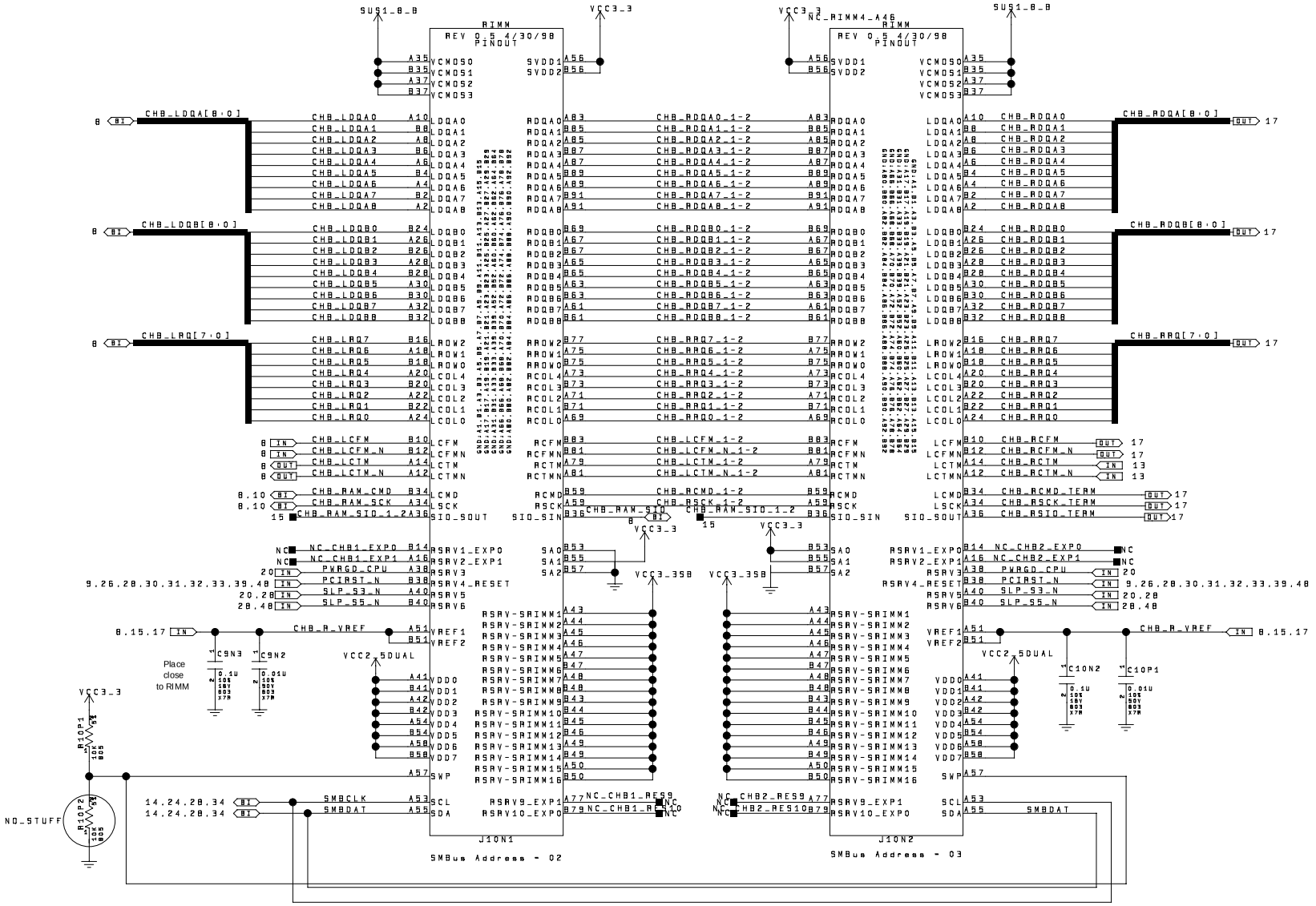
TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	13 OF 53



RIMM CHA CONNECTORS

ROOM=RIMM_CHA

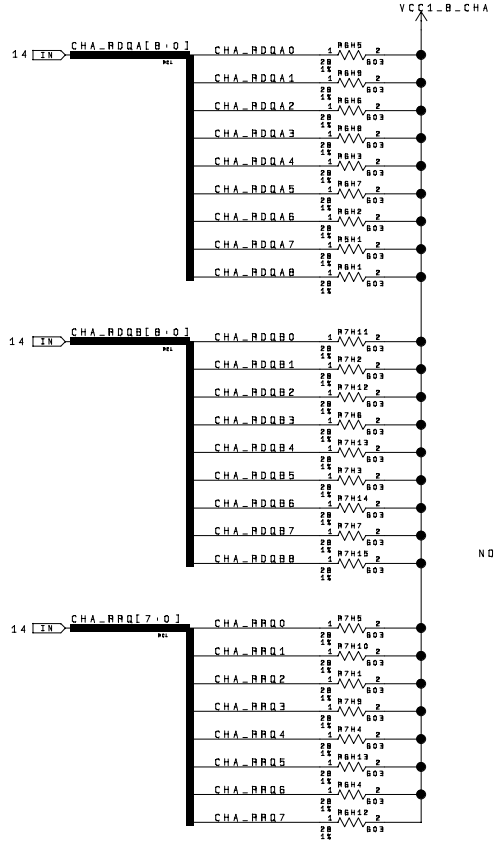
TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:08
	14 OF 53

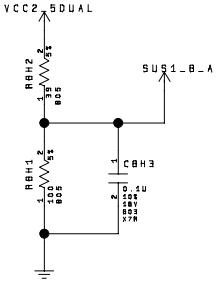


RIMM CHB CONNECTORS

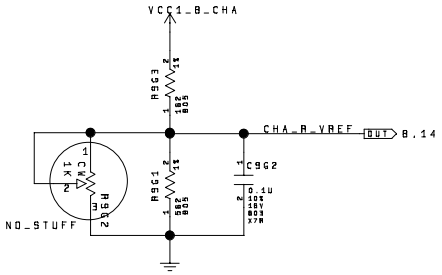
ROOM=RIMM_CHB

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	15 OF 53

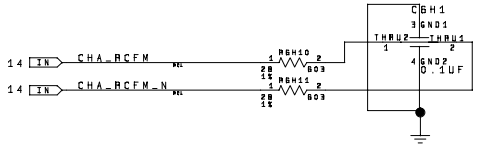


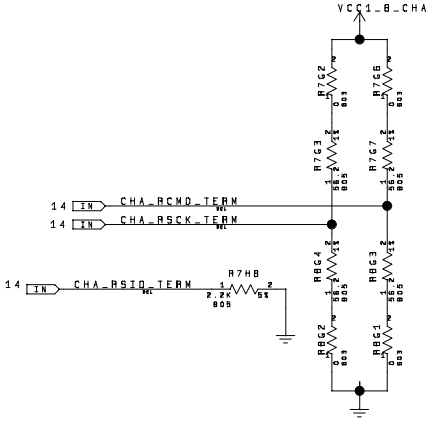


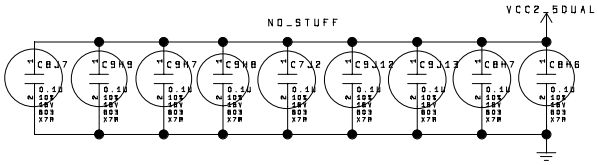
RAMBUS SUS1.8V GENERATION



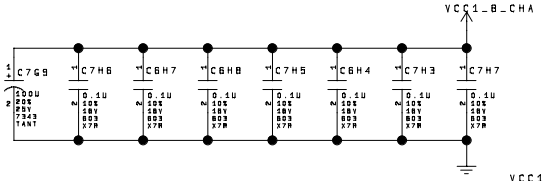
RAMBUS VREF GENERATION

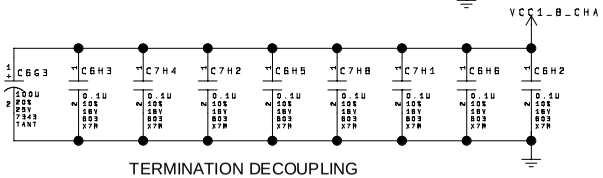


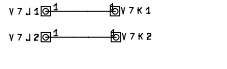




Back No Stuff Decouple

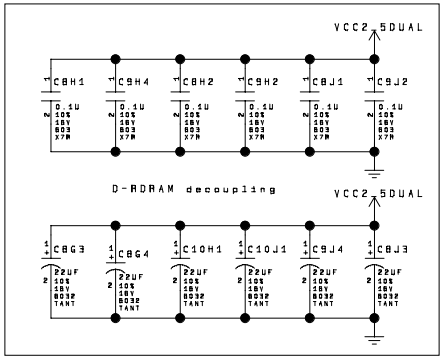


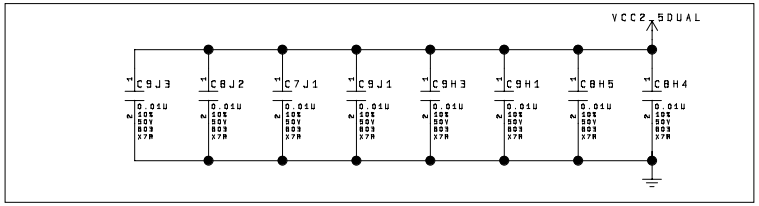




Vias for RSL test traces

TERMINATION DECOUPLING
(one 0.1uF cap per 2 RSL lines)



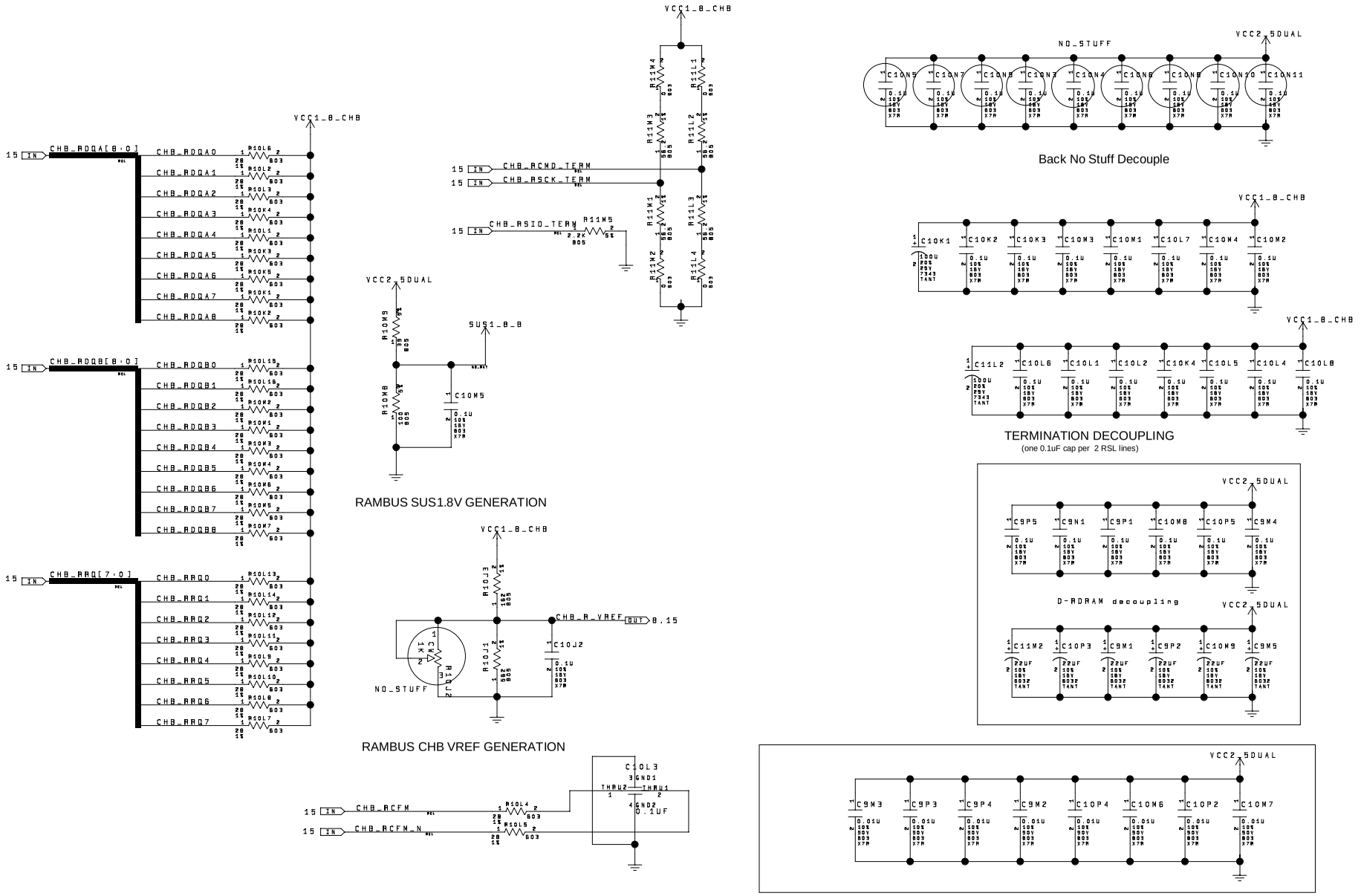


RIMM DECOUPLING

ROOM=RIMM_CHA

RDRAM CHA TERMINATION AND DECOUPLING

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	16 OF 53



RDRAM CHB TERMINATION AND DECOUPLING

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	17 OF 53

WTX POWER SUPPLY

VCC3_3SB

82559 LOM
SRIMMs
ADM1024
ICH, SIO
PCI32,PCI64, AMR

p.22

VCC5

CPUs,
VRMs,
AGP, PCI32, PCI64
AMR, Port 80,
USB, KBD/MS

VCC5_SB

WAKE ON LAN
COM1

VCC_DIG

VRM P0
VRM P1
RAMBUS ISR 2.5V

p.22

VCC3_3

CPUs,
CK133,
DRCG,
RIMMs,
AGP,ICH,
FWH,SIO,P64H
PCI32, PCI64, AMR
GAMEPORT

VCC12

VRMs, FANs,
AGP, PCI32, AMR,
MIC AMP,PCI64
COM PORTs

VCC-12

PCI32, PCI64, AMR
MIC AMP,
COM PORTs

VOLTAGE REGULATORS

VTT1_5

CPUs

p.21

AGP1_5

AGP

p.21

VCC1_8

ICH, P64H

p.21

VCC1_8_MCH

MCH
DRCG

p.21

VCC2_5DUAL

RIMMs

p.22

VCC2_5

CK133
DRCG
ITP CLK BUFFER

p.22

VCC_CMOS

CMOS PULLUPS

2.5V

p.22

AUDVCC5

AD1881 AUDIO
LM4880 AMP

p.38

SUS1_8A

RIMMs

p.16

SUS1_8B

RIMMs

p.17

VCC1_8_CHA
VCC1_8_CHB

RIMM TERM

p.17

VRMs

VCC_CORE_P0

CPU0

p.9

VCC_CORE_P1

CPU1

p.9

SWITCHED VOLTAGE PLANES

VDDQ

VCC3_3 / AGP1_5

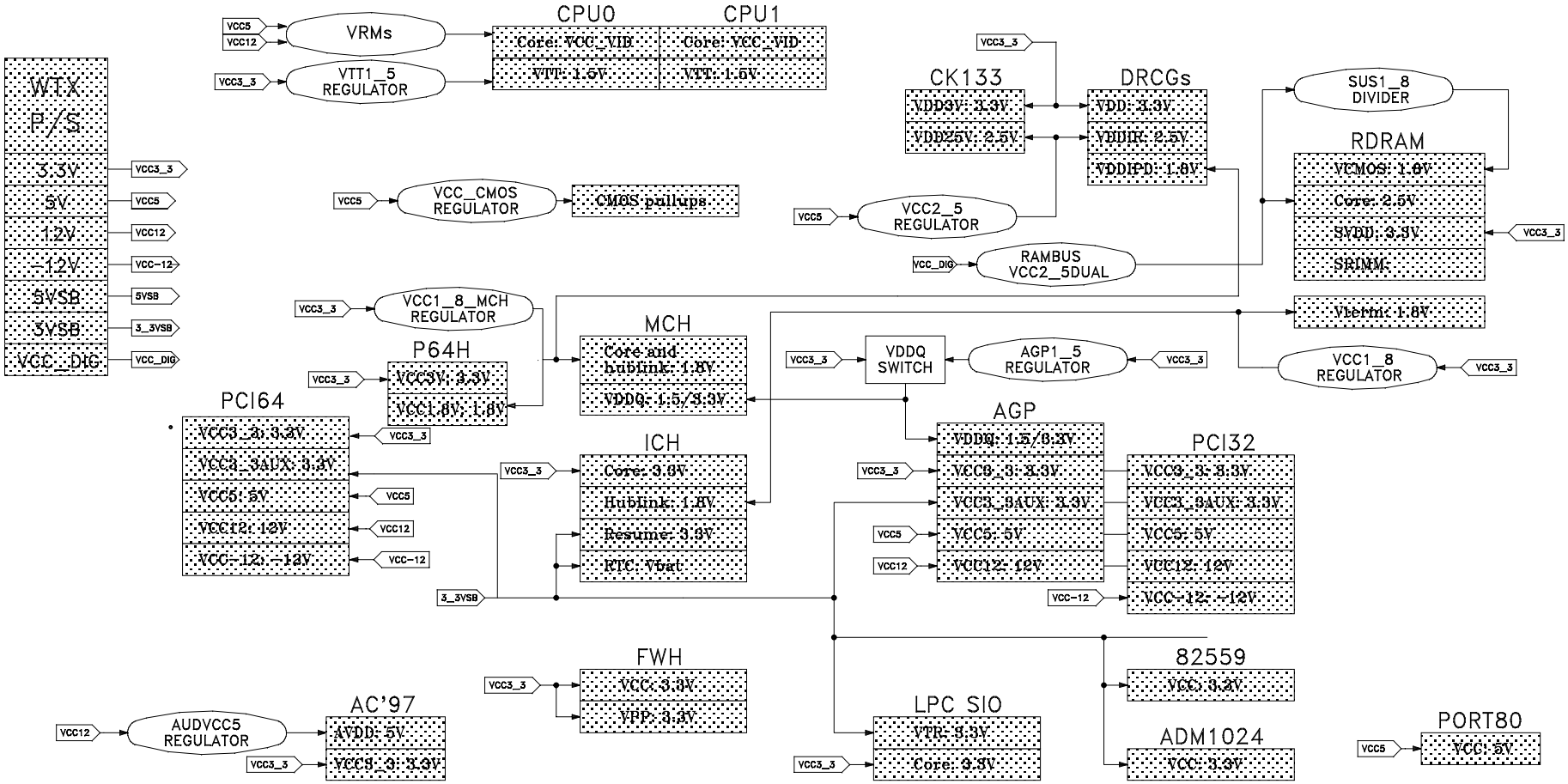
AGP
MCH

p.25

Note: Only major devices are listed in this diagram

POWER MANAGEMENT MAP

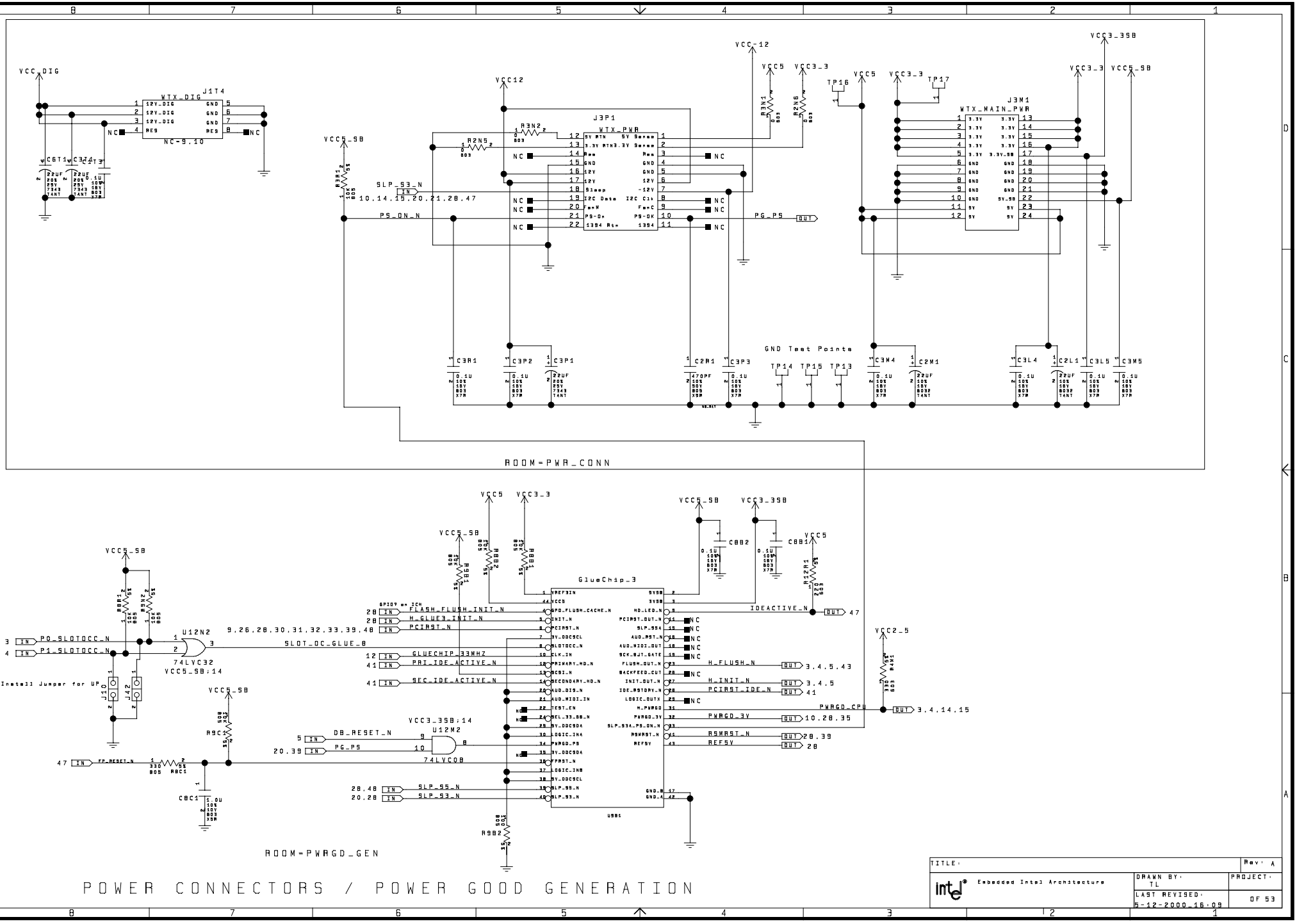
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	0F 53



AHA: Vdd = 1.8V, Vref = 0.5 Vdd
RSL: Vtt=1.8V, Vref = 2/3 Vtt
GTL: Vtt=1.5V, Vref = 2/3 Vtt
AGP: Vdd= 1.5V or 3.3V, Vref= 0.5 Vagpdd (1.5V) or 0.4 Vagpdd (3.3V)

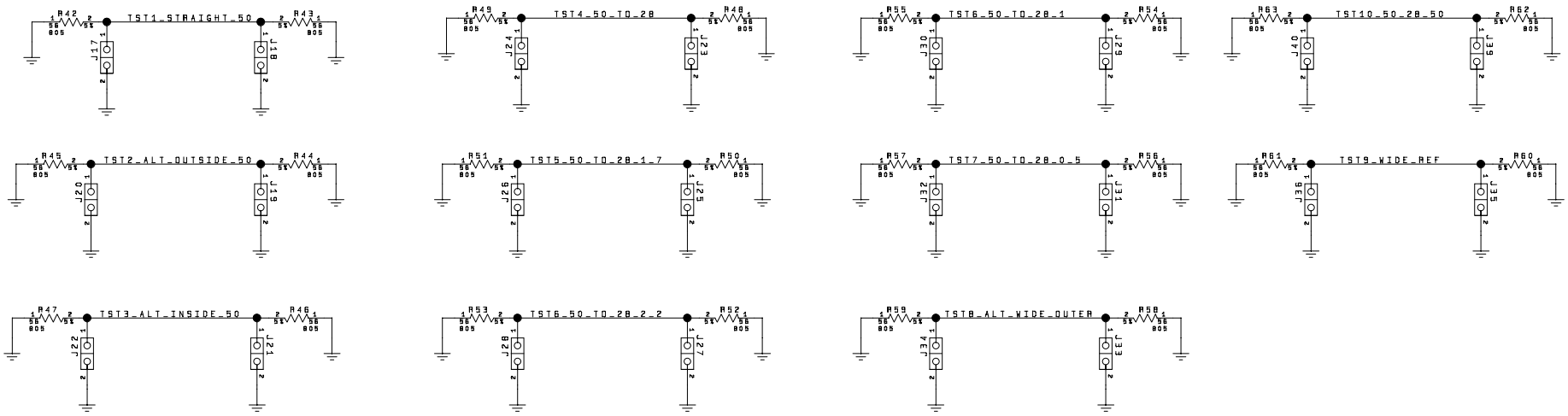
POWER DISTRIBUTION MAP

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	19 OF 53

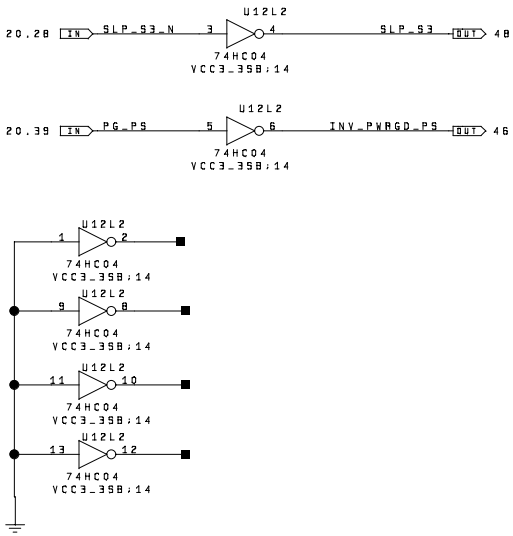


POWER CONNECTORS / POWER GOOD GENERATION

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	OF 53



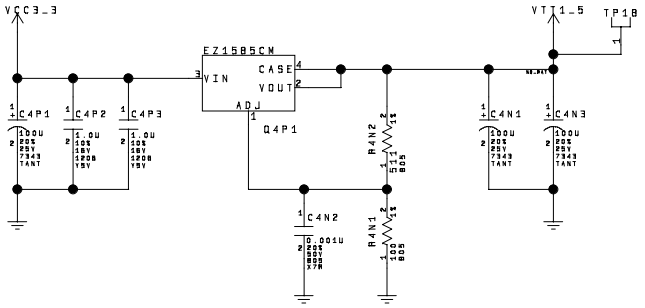
Impeadance Test Traces



POWER MANAGEMENT LOGIC

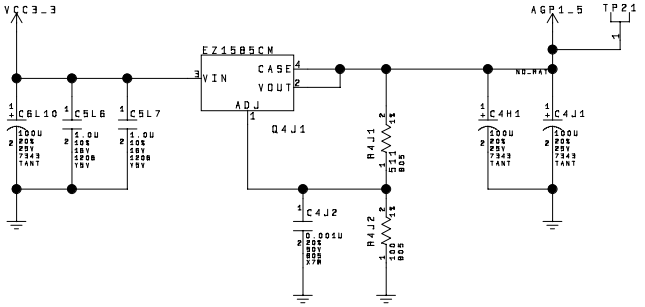
ROOM=PWR_MGMT_LOGIC

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	21 OF 53



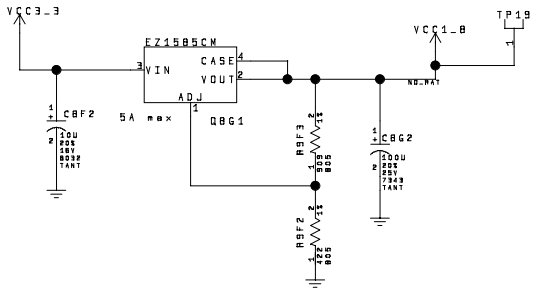
VTT 1.5V GENERATION

ROOM=VTT_1.5V_GEN



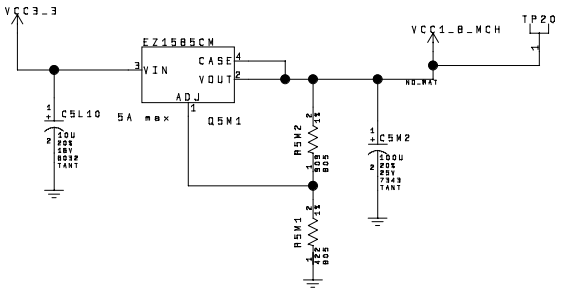
AGP 1.5V GENERATION

ROOM=AGP_1.5V_GEN



1.8V GENERATION

ROOM=1.8V_GEN

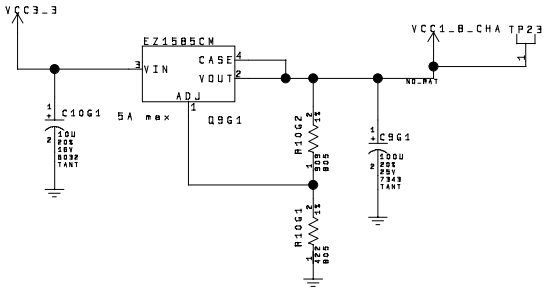


MCH 1.8V GENERATION

ROOM=MCH_1.8V_GEN

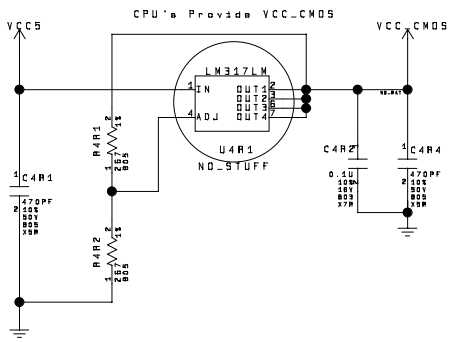
1.5V / 1.8V REGULATORS

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	22 OF 53



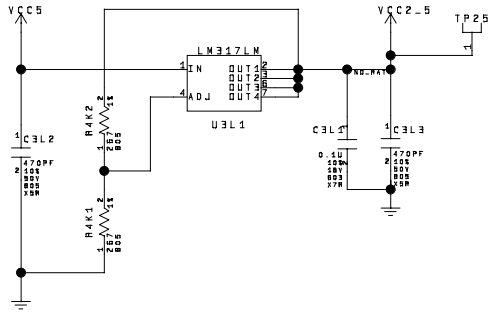
1.8V GENERATION FOR RAMBUS CHA TERM

ROOM=1.8V_GEN



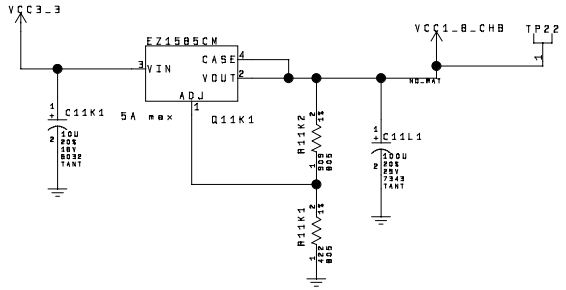
FSB CMOS VOLTAGE GENERATION

ROOM=FSB_CMOSV_GEN



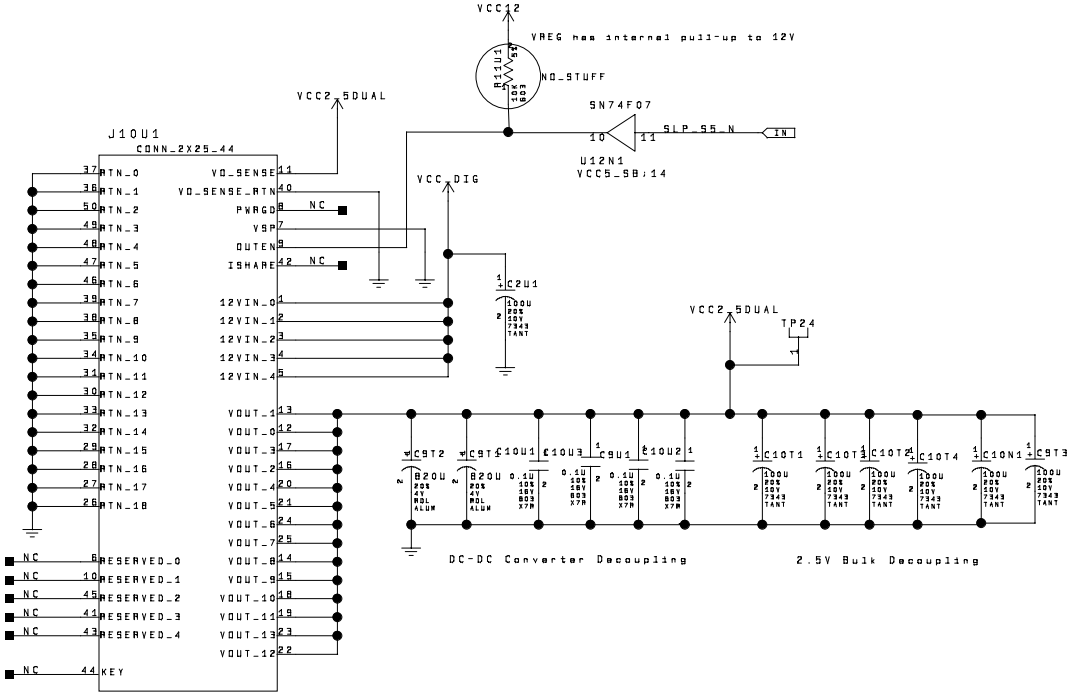
2.5V GENERATION

ROOM=2.5V_GEN



1.8V GENERATION FOR RAMBUS CHB TERM

ROOM=1.8V_GEN

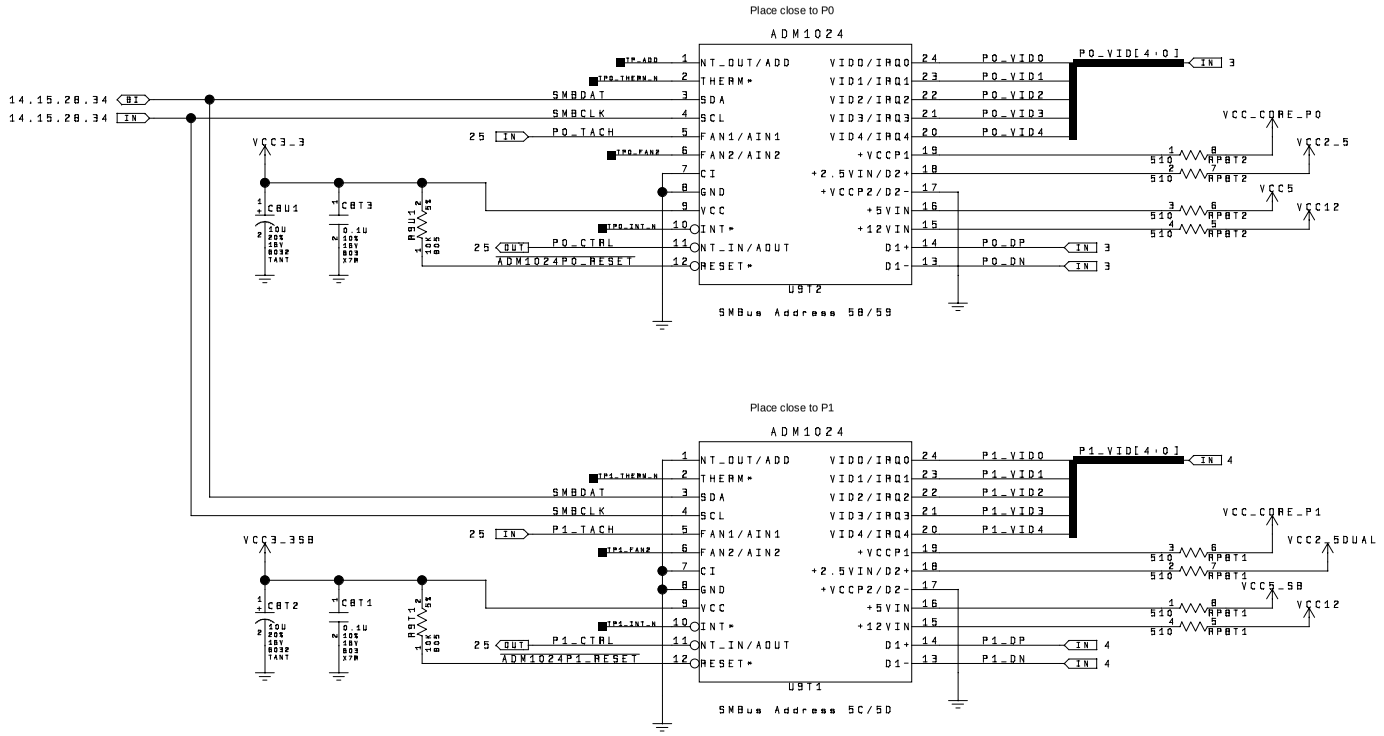


RAMBUS 2.5V DUAL GENERATION

ROOM=RAMBUS_25_GEN

VCC_CMOS / 2.5V / 3.3V REGULATORS

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	OF 53

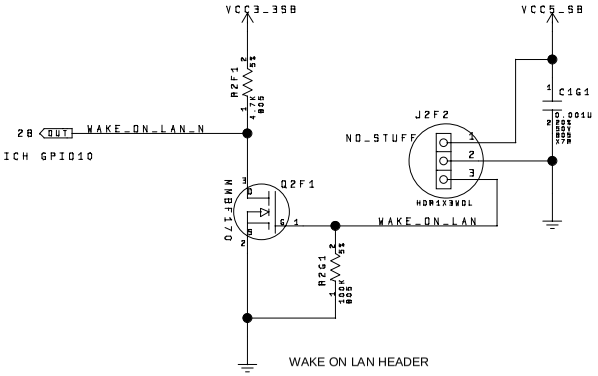


Not Populated

TEMP / VOLTAGE MONITORING

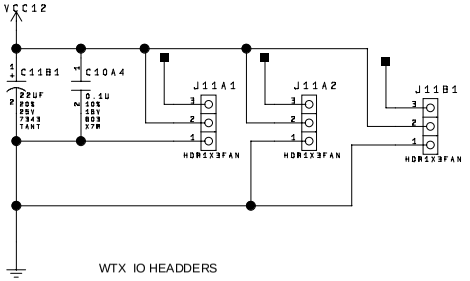
ROOM=PROCESSORS

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	OF 53

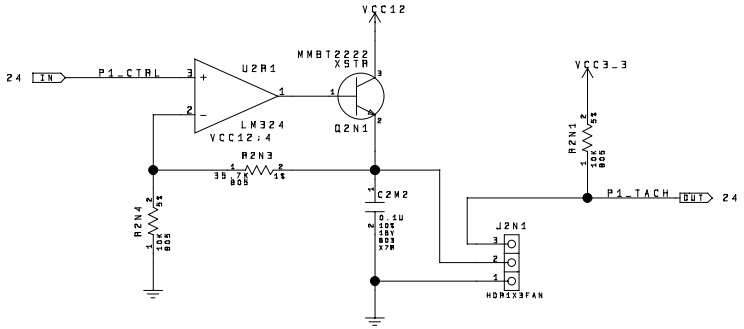


WAKE ON LAN HEADER

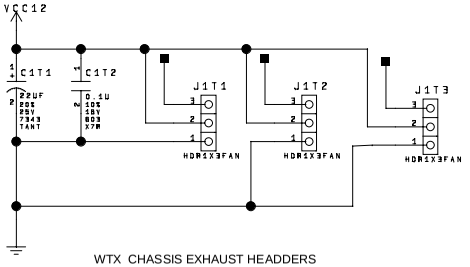
ROOM=82559



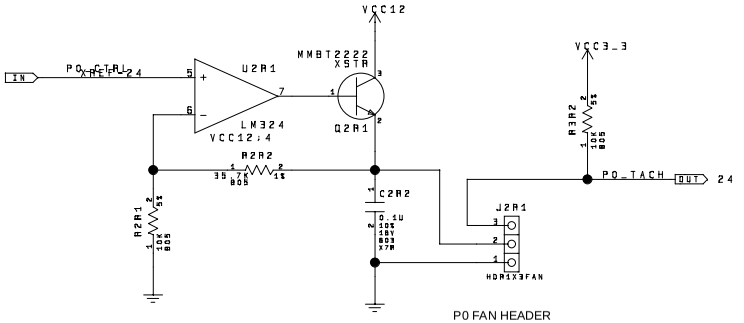
WTX IO HEADDERS



P1 FAN HEADER



WTX CHASSIS EXHAUST HEADDERS

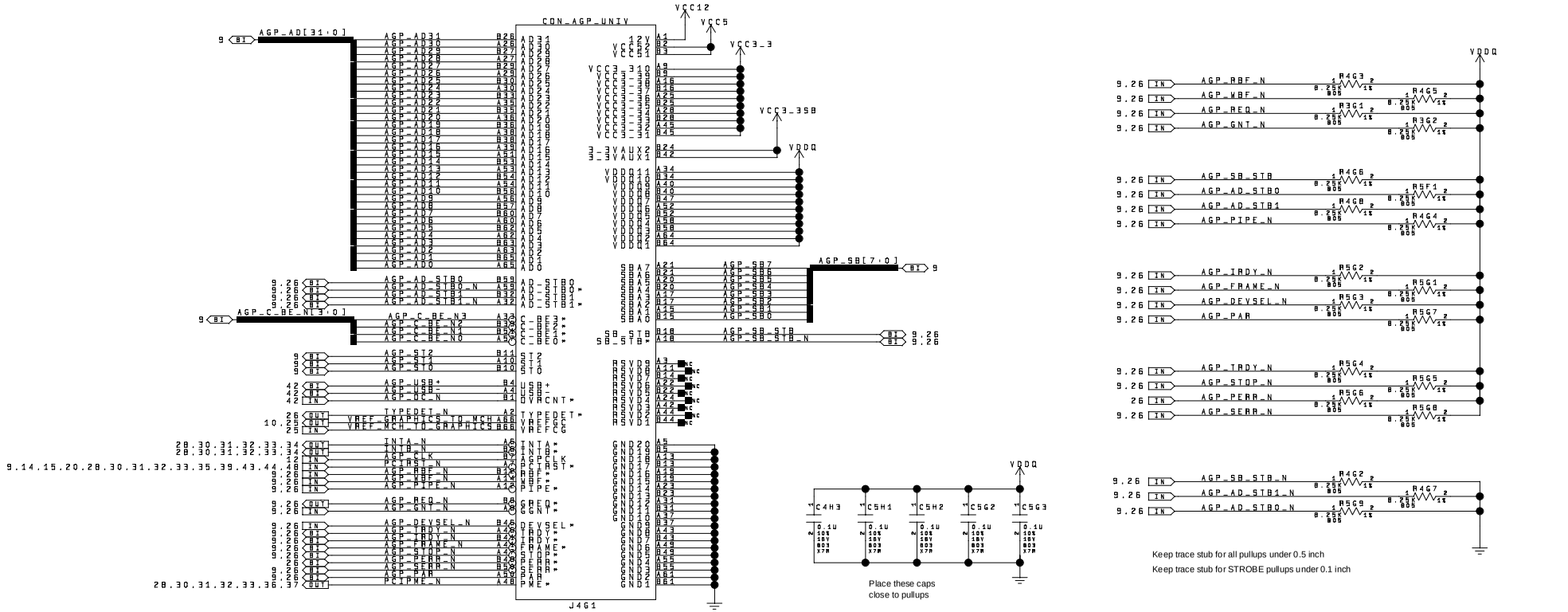


P0 FAN HEADER

ROOM=PROCESSORS

WOL / FAN HEADERS

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	OF 53



AGP VDDQ SWITCH

AGP DECOUPLING

AGP VREF GENERATION

ROOM=MCH

ROOM=AGP4X

AGP 4X

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
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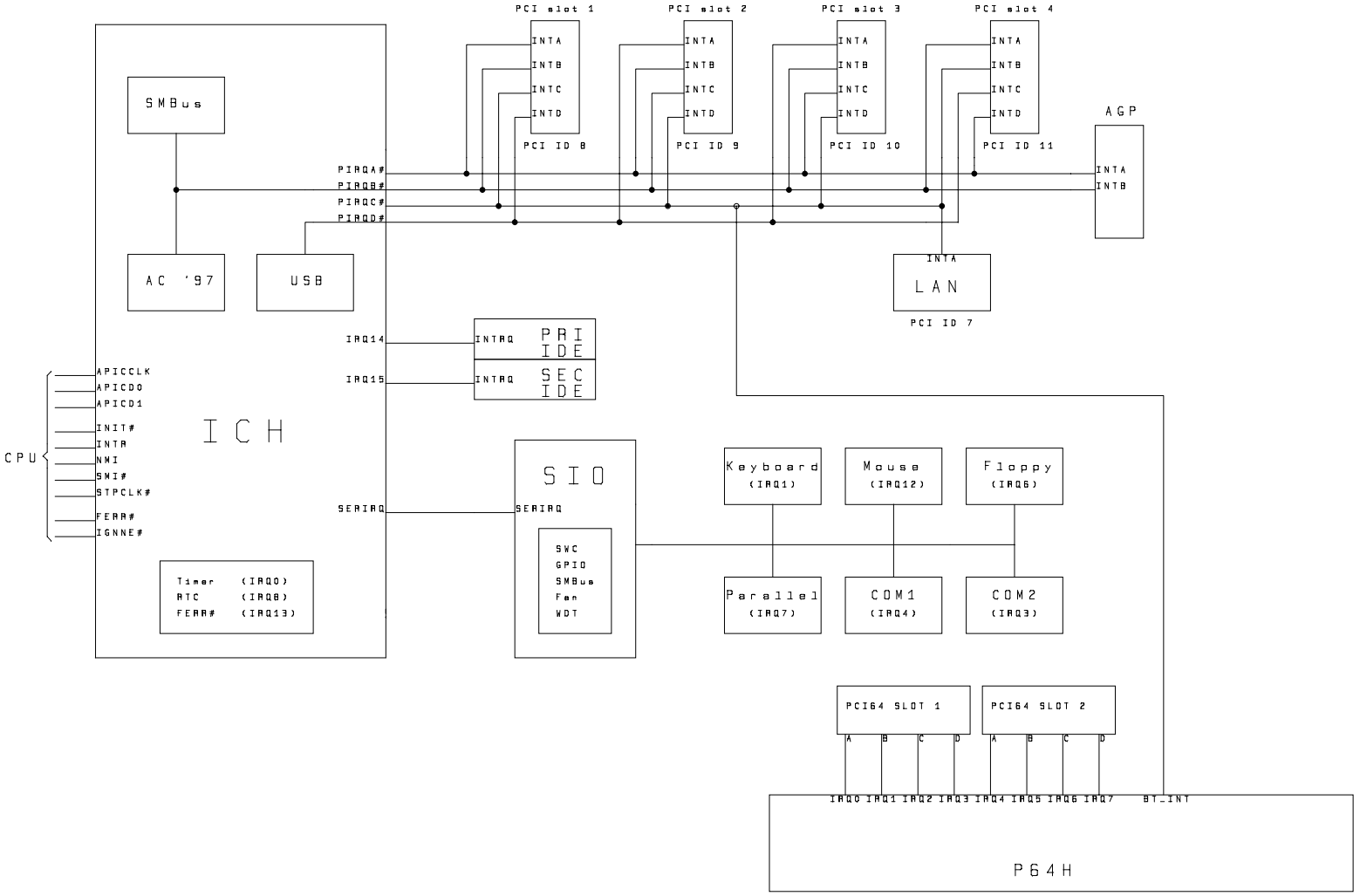
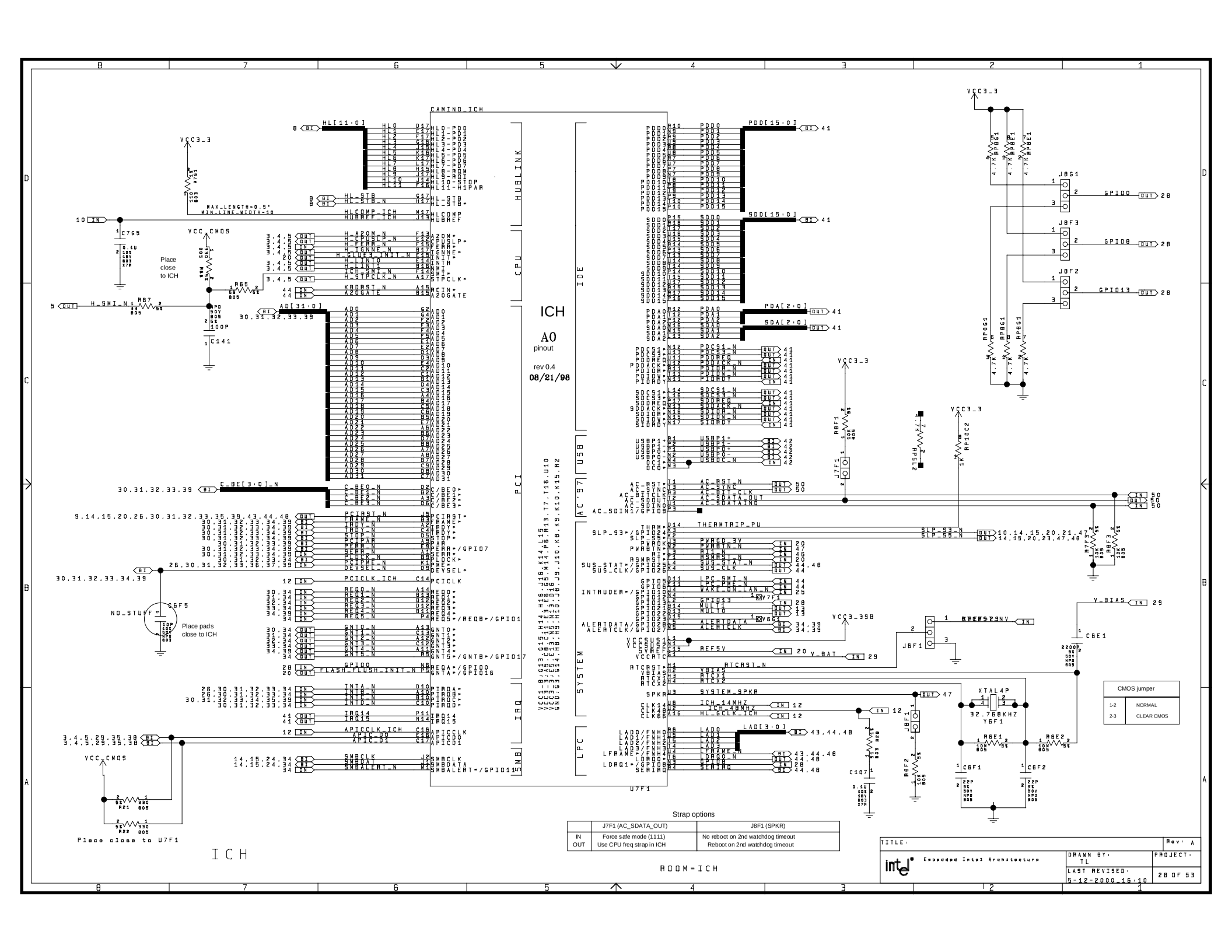
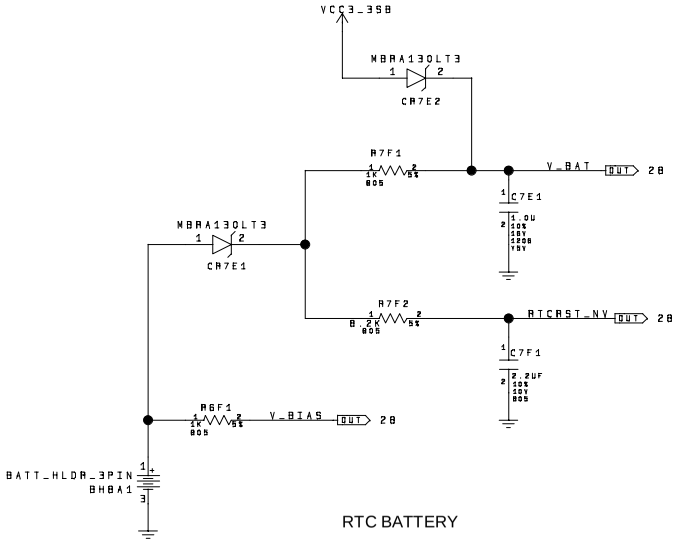
Interrupt Diagram



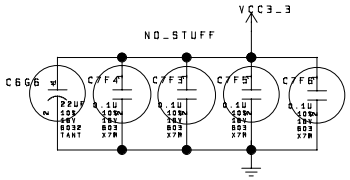
PCI / INTERRUPT DIAGRAM

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	OF 53

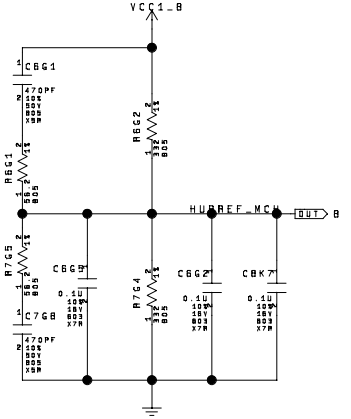

ICH
A0
pinout
rev 0.4
08/21/98
CAMINO_ICH
HUBLINK
CPU
IDE
PCI
USB
AC'97
SYSTEM
IRQ
SMB
LPC
HL[11:0]
AD[31:0]
C_BE[3:0]_N
PDD[15:0]
SDD[15:0]
PDA[2:0]
SDA[2:0]
VCC3_3
VCC_CMOS
Place close to ICH
Place pads close to ICH
NO_STUFF
Place close to U7F1
CMOS jumper
1-2 NORMAL
2-3 CLEAR CMOS
32.768KHZ
Y6F1
Strap options
J7F1 (AC_SDATA_OUT)
J8F1 (SPKR)
IN Force safe mode (1111)
No reboot on 2nd watchdog timeout
OUT Use CPU freq strap in ICH
Reboot on 2nd watchdog timeout
ROOM=ICH
ICH
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 5-12-2000.16:10
28 OF 53



RTC BATTERY

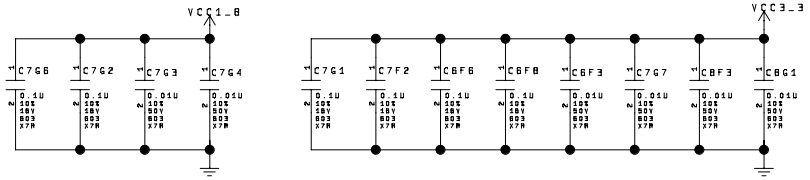


Back No Stuff ICH

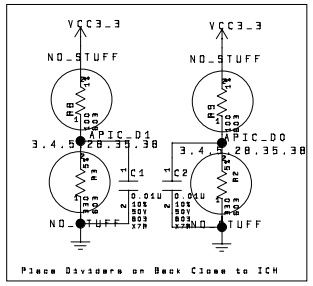


MCH HUBREF GENERATION

Place close to ICH



ICH DECOUPLING

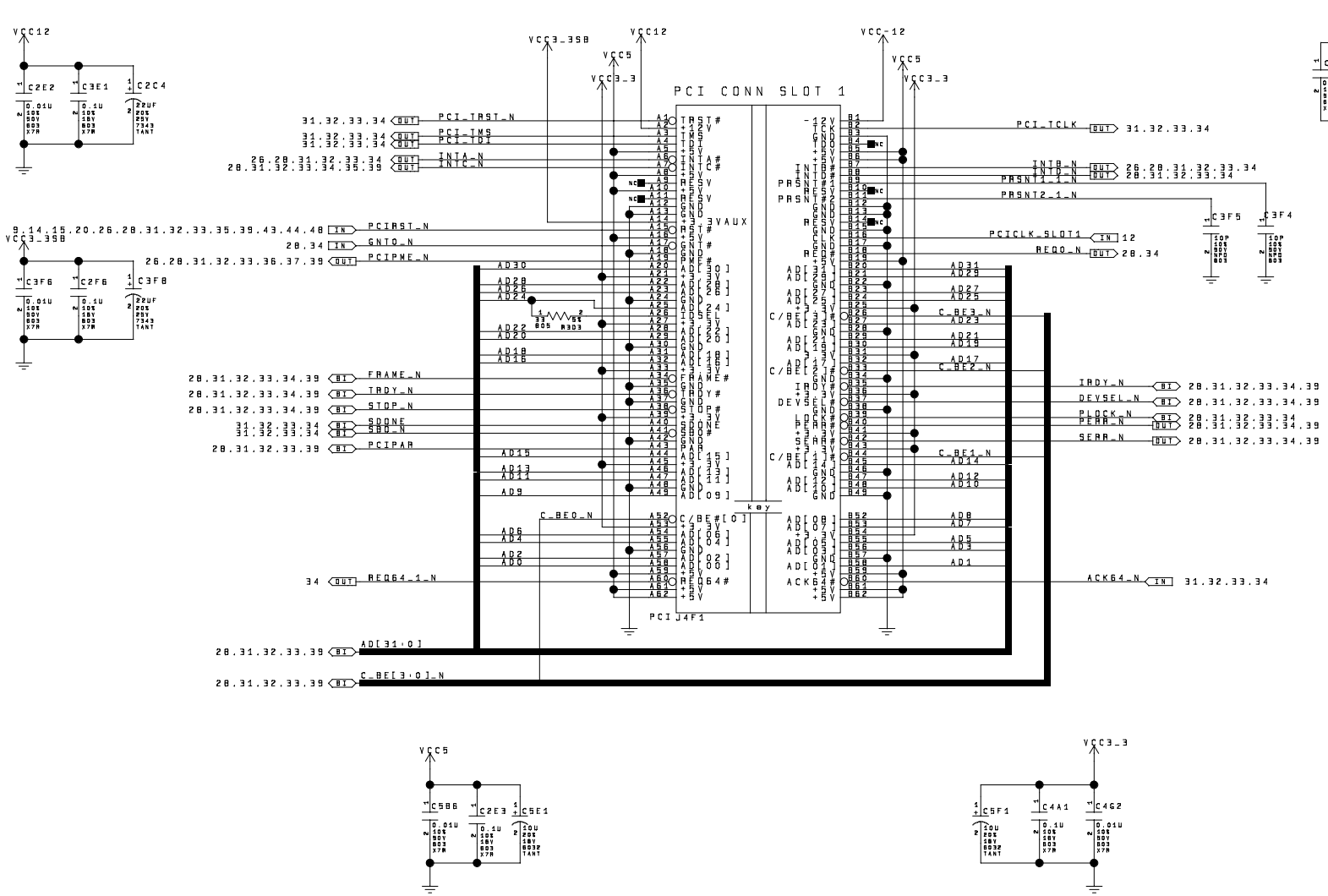


Place Dividers on Back Close to ICH

ROOM=ICH

ICH DECOUPLING AND SUPPORT CIRCUITRY

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	29 OF 53



PCI CONN SLOT 1

ROOM=PCI

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
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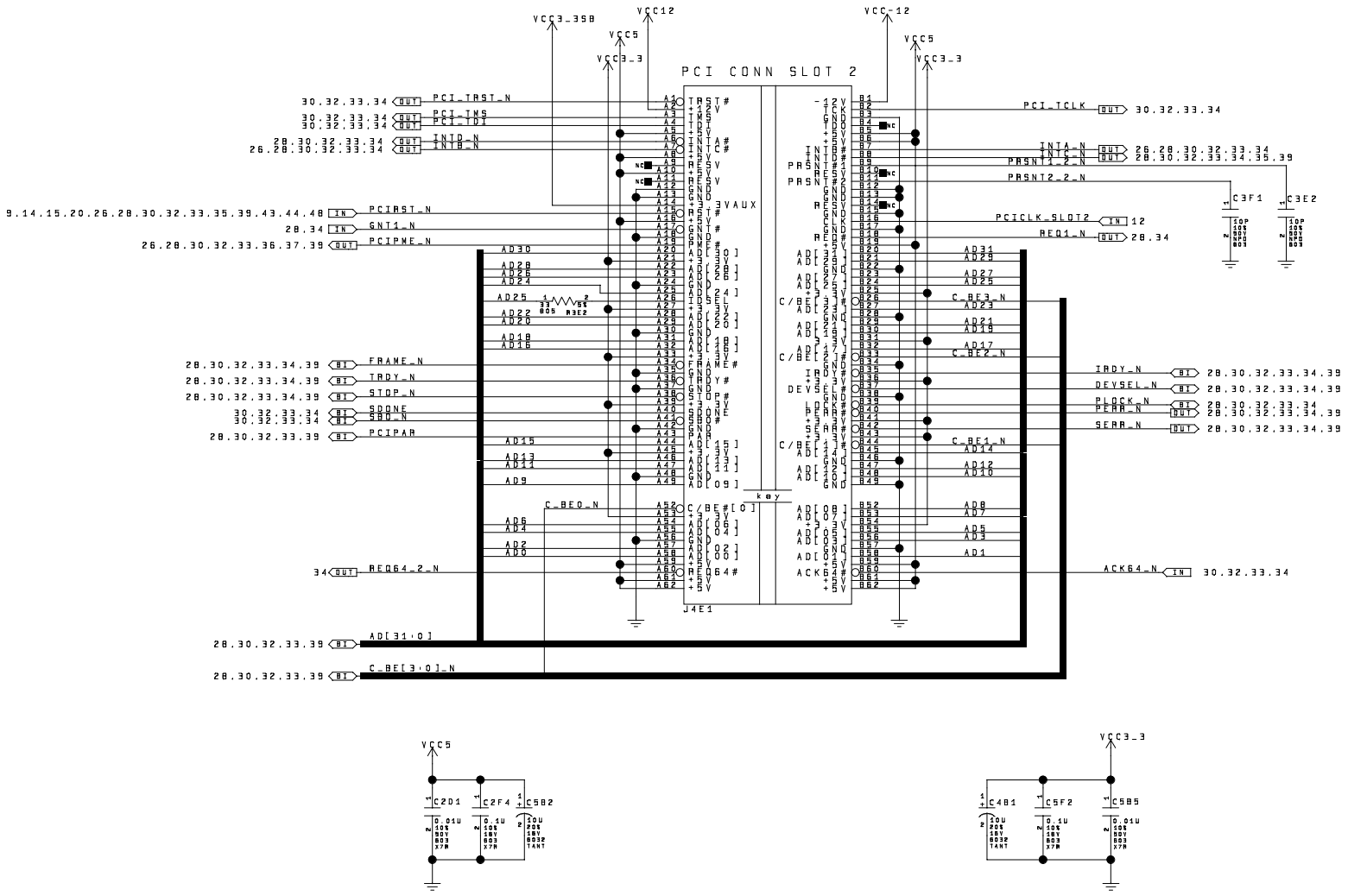

PCI CONN SLOT 2

ROOM=PCI

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
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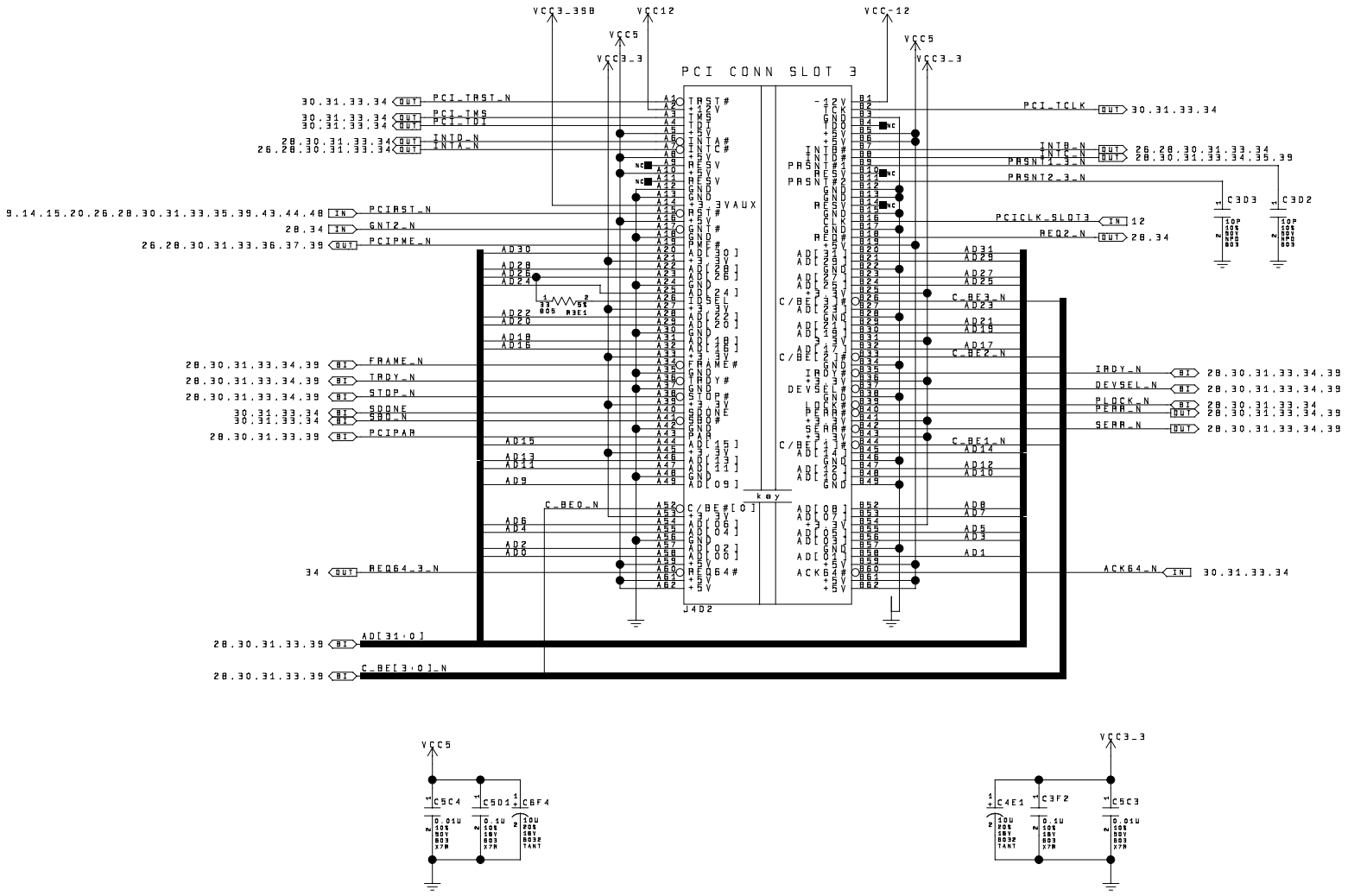

PCI CONN SLOT 3

ROOM=PCI

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
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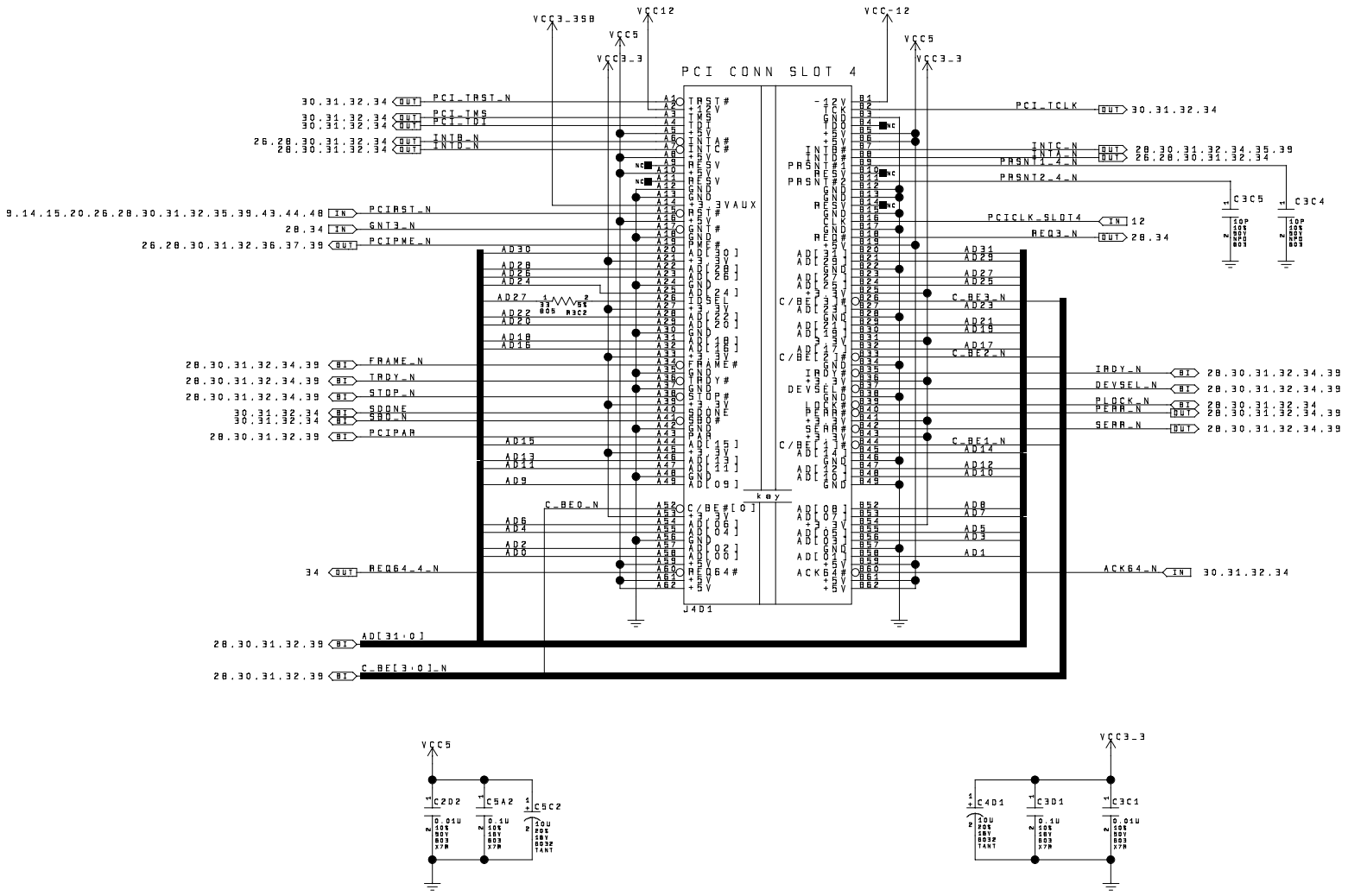

PCI CONN SLOT 4

ROOM=PCI

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
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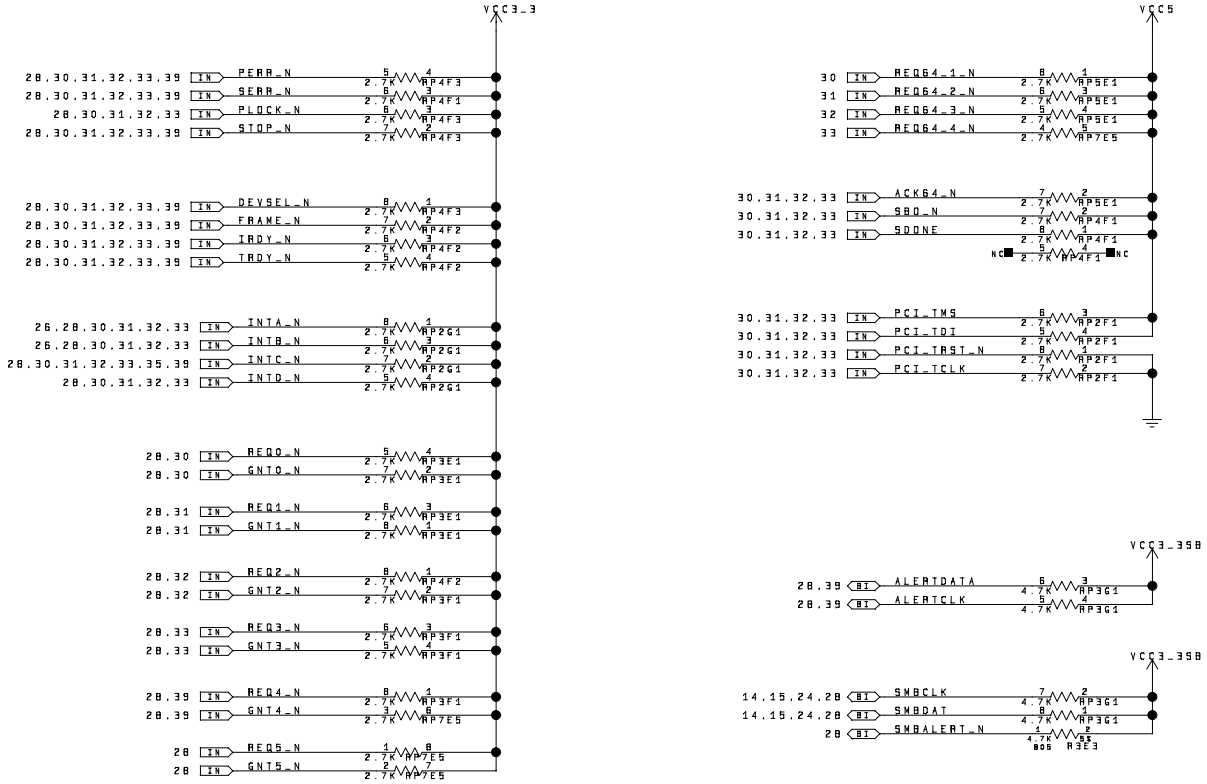

PCI PULLUPS

ROOM=PCI

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
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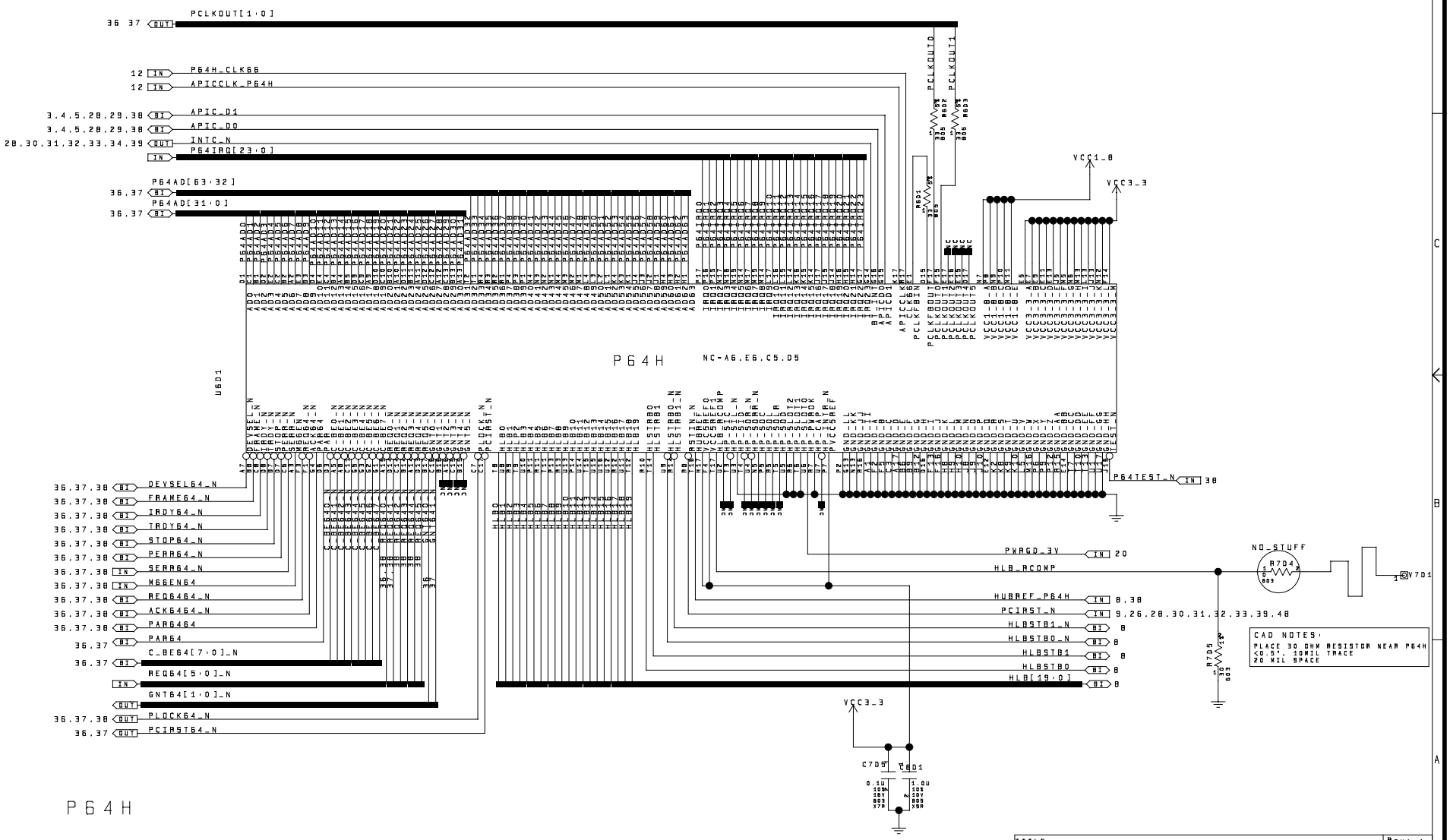
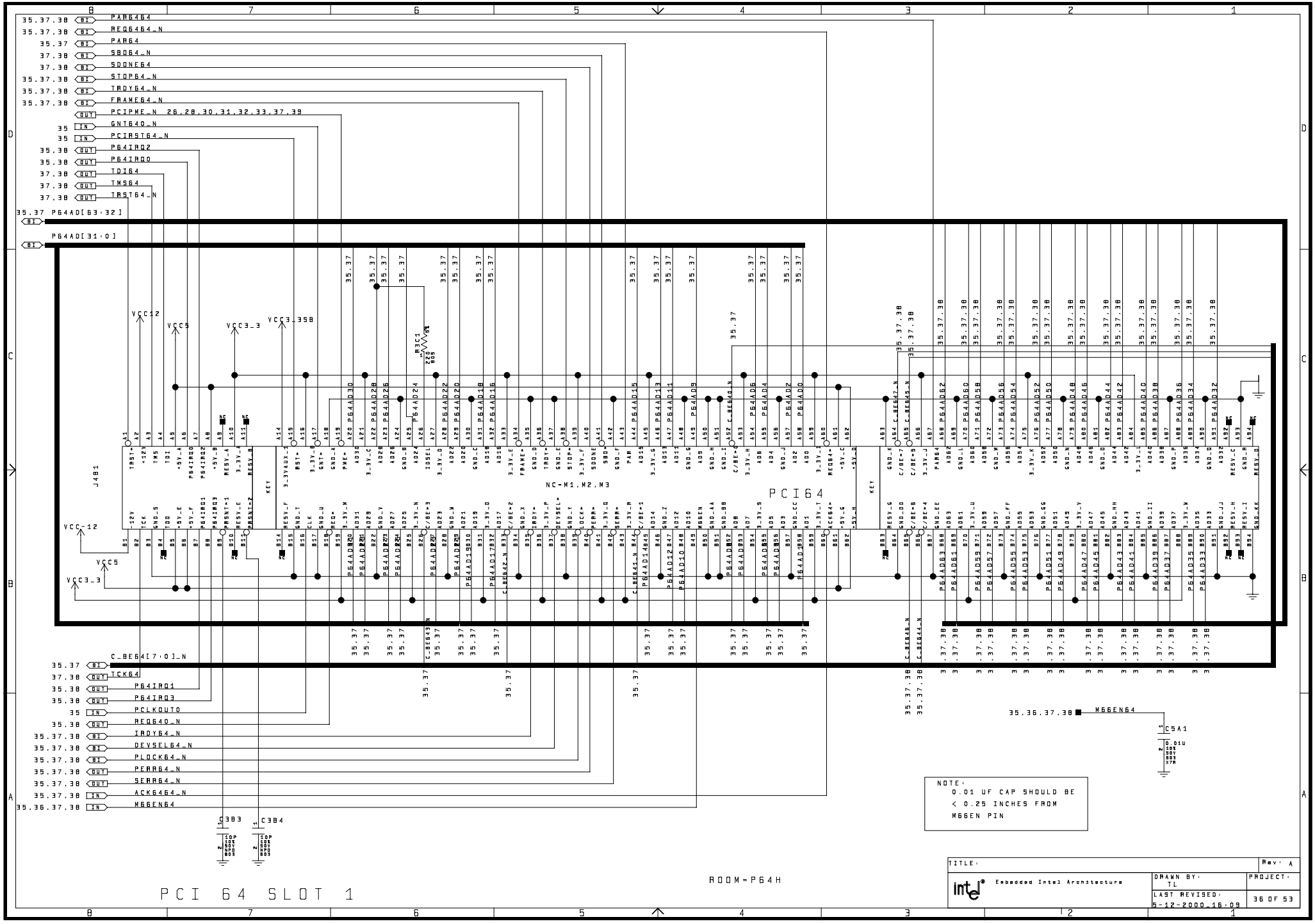


TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	35 OF 53


PCI 64 SLOT 1
PCI64
NC-M1,M2,M3
J4B1
KEY
VCC12
VCC5
VCC3_3
VCC3_3SB
VCC-12
PAR64
REQ64_N
SBO64_N
SDONE64
STOP64_N
TRDY64_N
FRAME64_N
PCIPME_N 26,28,30,31,32,33,37,39
GNT64_N
PCIRST64_N
P64IRQ2
P64IRQ0
TDI64
TMS64
TRST64_N
P64AD[63:32]
P64AD[31:0]
C_BE64[7:0]_N
TCK64
P64IRQ1
P64IRQ3
PCLKOUT0
REQ64_N
IRDY64_N
DEVSEL64_N
PLOCK64_N
PERR64_N
SERR64_N
ACK64_N
M66EN64
C3B3
C3B4
C5A1
NOTE:
0.01 UF CAP SHOULD BE
< 0.25 INCHES FROM
M66EN PIN
ROOM=P64H
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 5-12-2000_16:09
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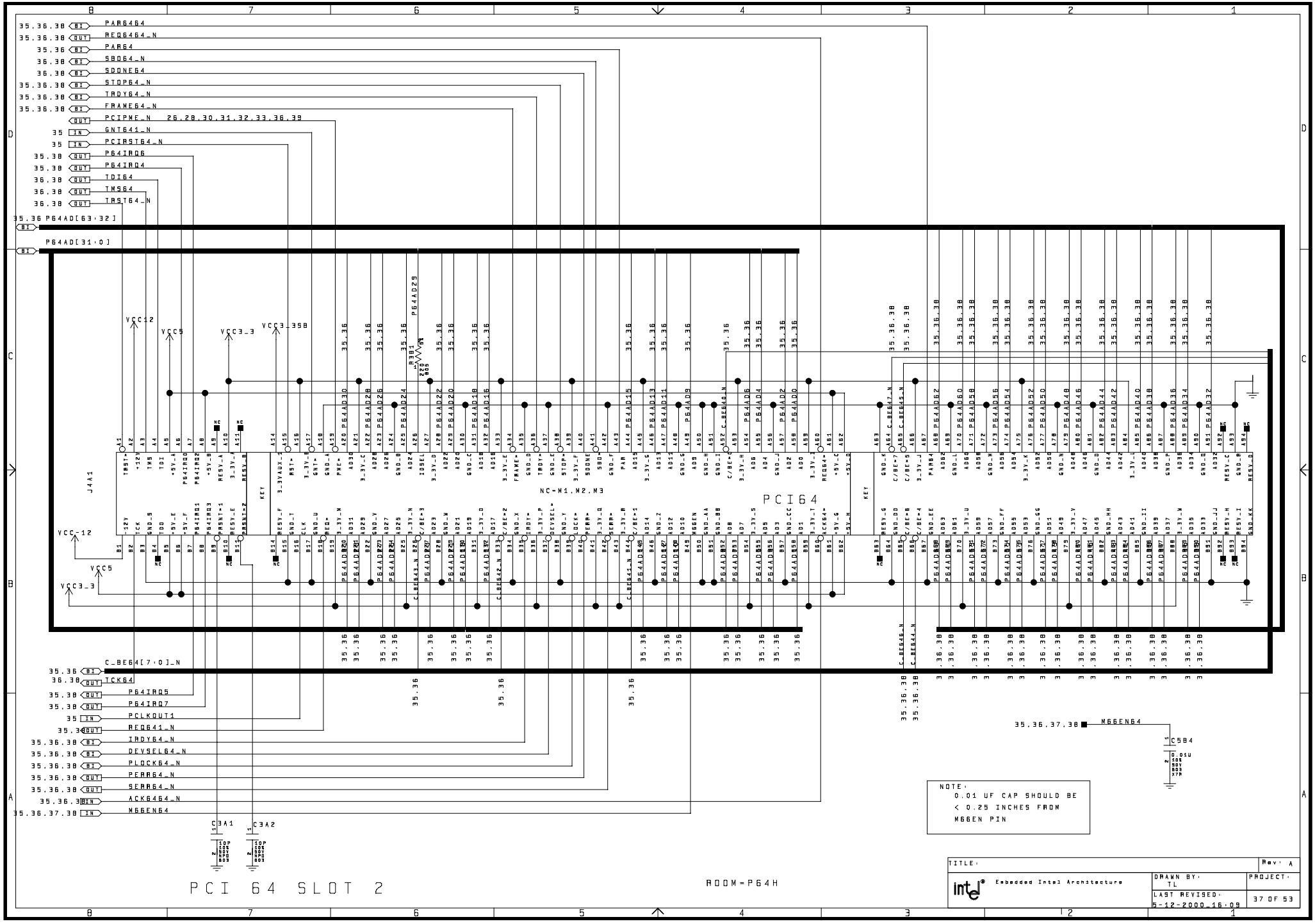
PAR6464
REQ6464_N
PAR64
SB064_N
SDONE64
STOP64_N
TRDY64_N
FRAME64_N
PCIPME_N
GNT641_N
PCIRST64_N
P64IRQ6
P64IRQ4
TDI64
TMS64
TRST64_N
P64AD[63:32]
P64AD[31:0]
C_BE64[7:0]_N
TCK64
P64IRQ5
P64IRQ7
PCLKOUT1
REQ641_N
IRDY64_N
DEVSEL64_N
PLOCK64_N
PERR64_N
SERR64_N
ACK6464_N
M66EN64
J4A1
KEY
PCI64
NC-M1,M2,M3
M66EN64
C584
0.01U
NOTE:
0.01 UF CAP SHOULD BE
< 0.25 INCHES FROM
M66EN PIN
C3A1
C3A2
PCI 64 SLOT 2
ROOM=P64H
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY:
TL
PROJECT:
LAST REVISED:
5-12-2000 16:09
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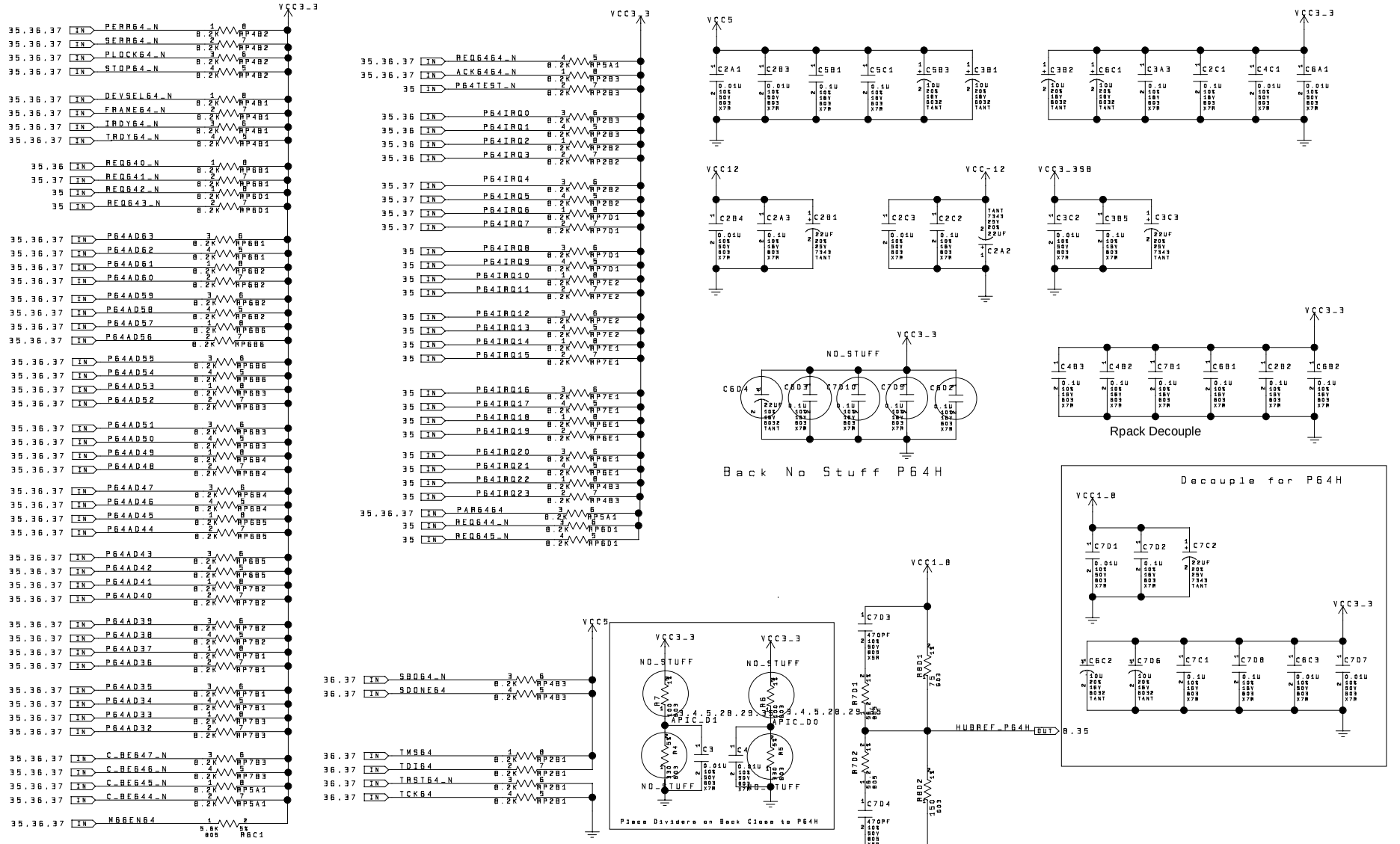
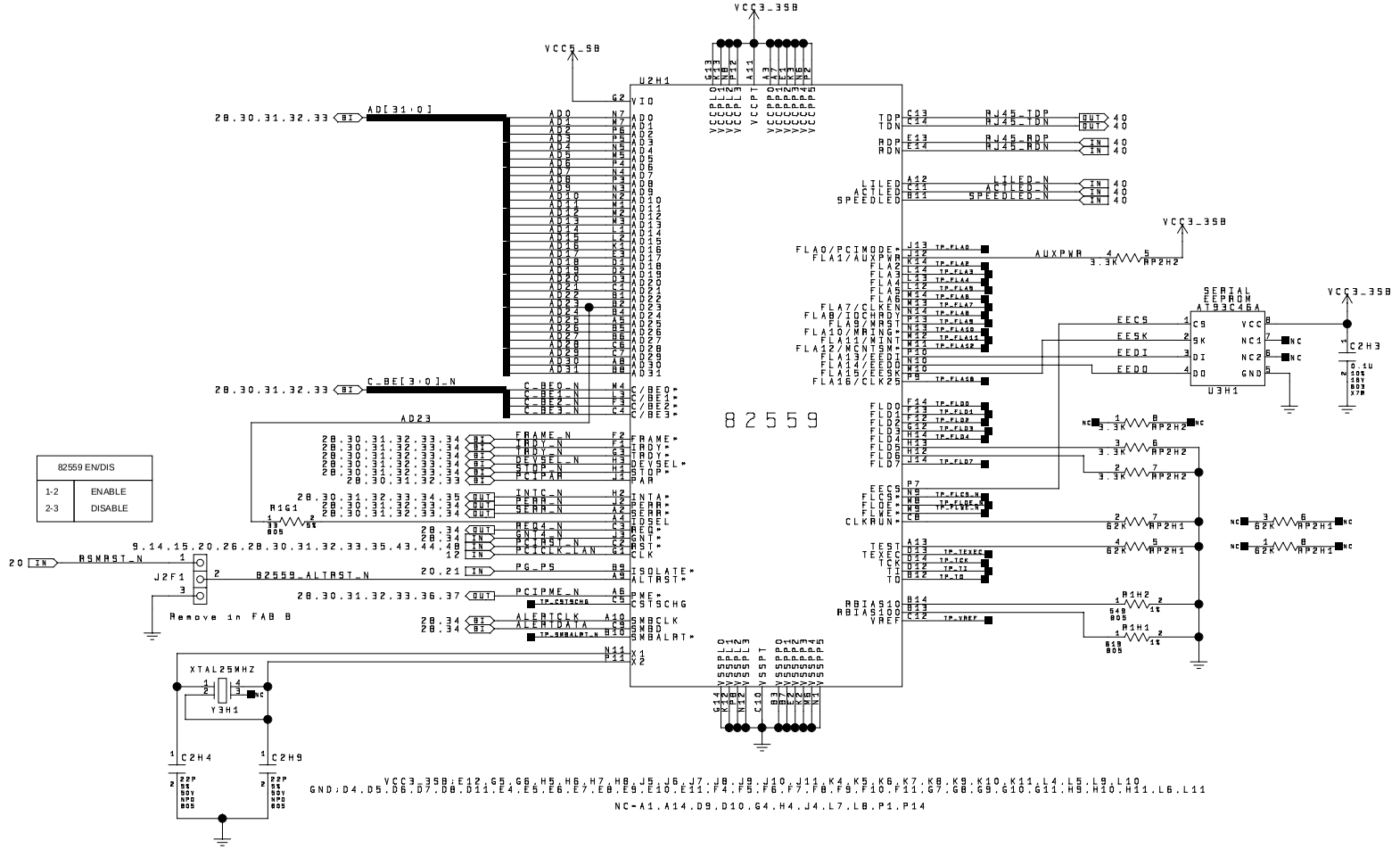


TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	38 OF 53



ETHERNET 82559ER

ROOM=82559

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
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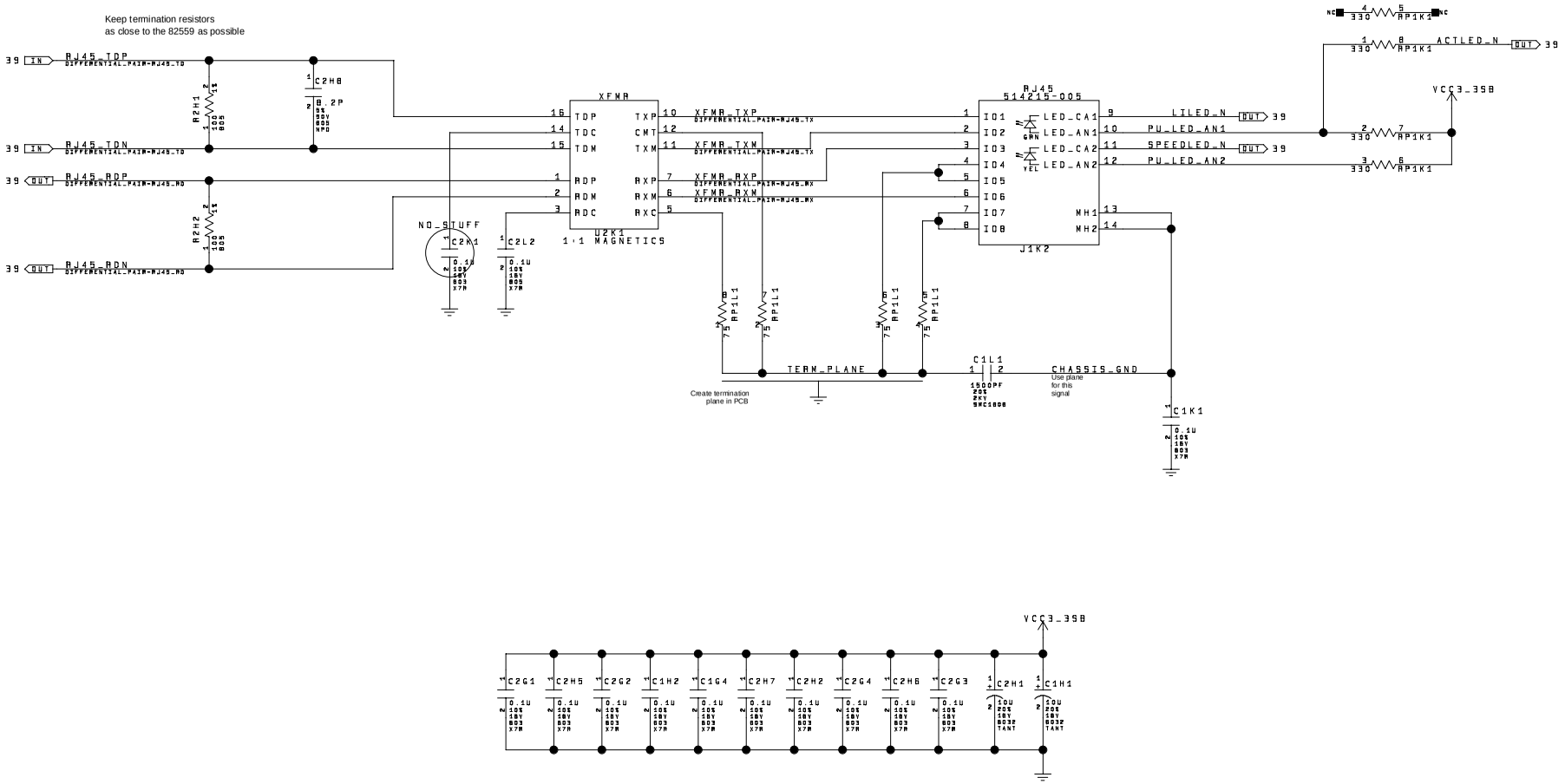

ETHERNET CONNECTOR / DECOUPLING

ROOM=82559

TITLE:	Rev: A
Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
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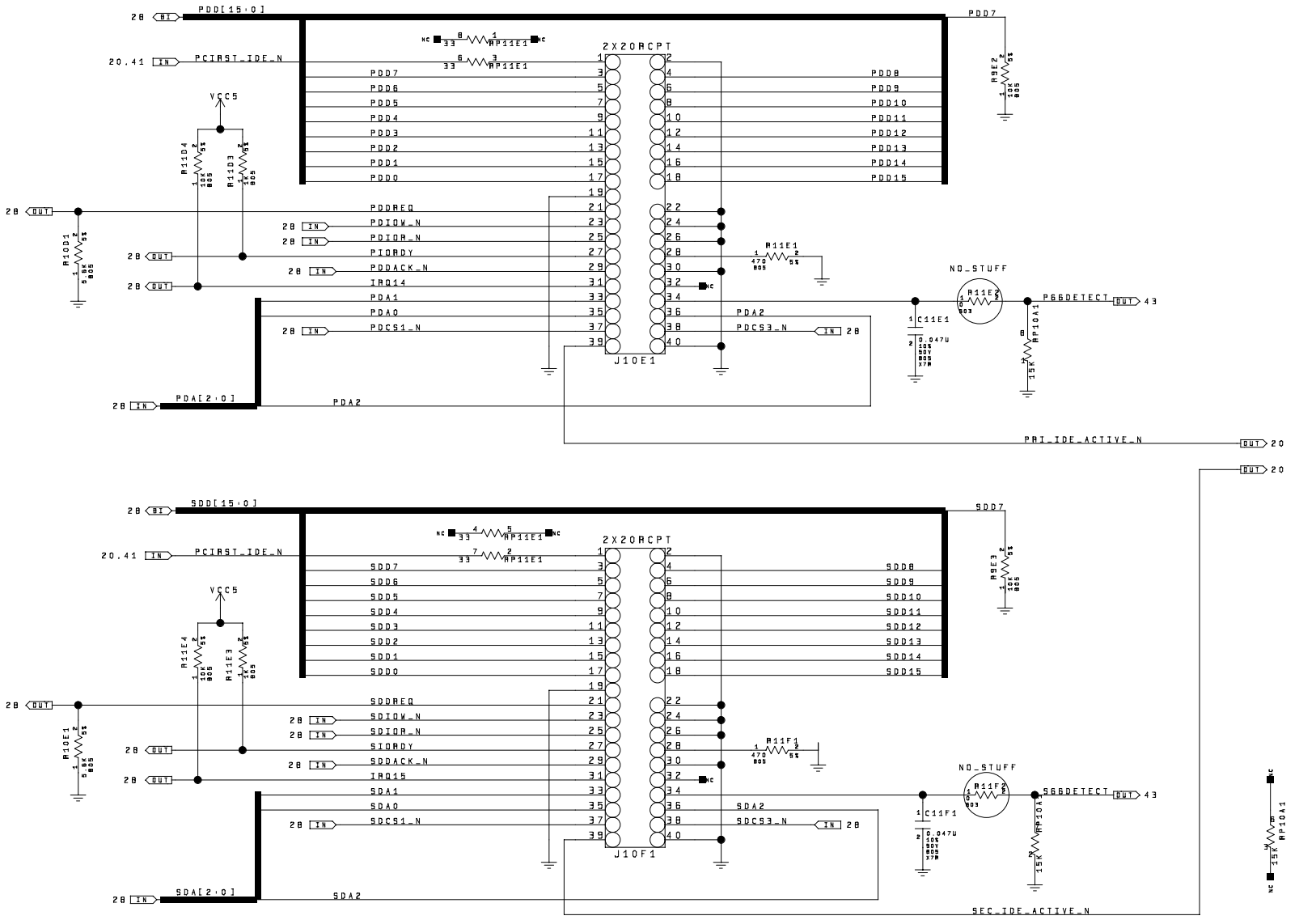

IDE CONNECTORS

ROOM=IDE_CONN

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
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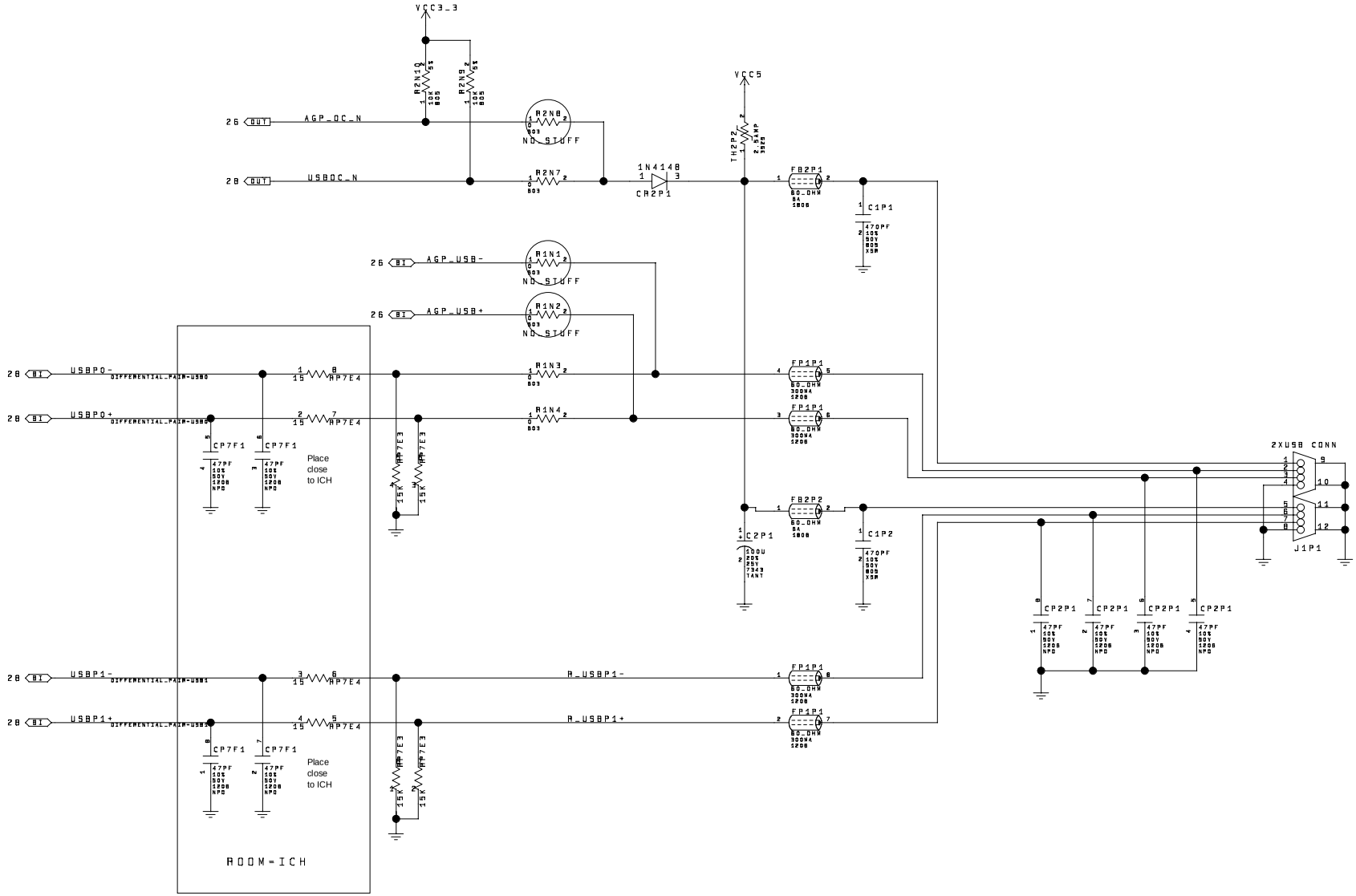

USB CONNECTORS

ROOM=USB_CONN

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
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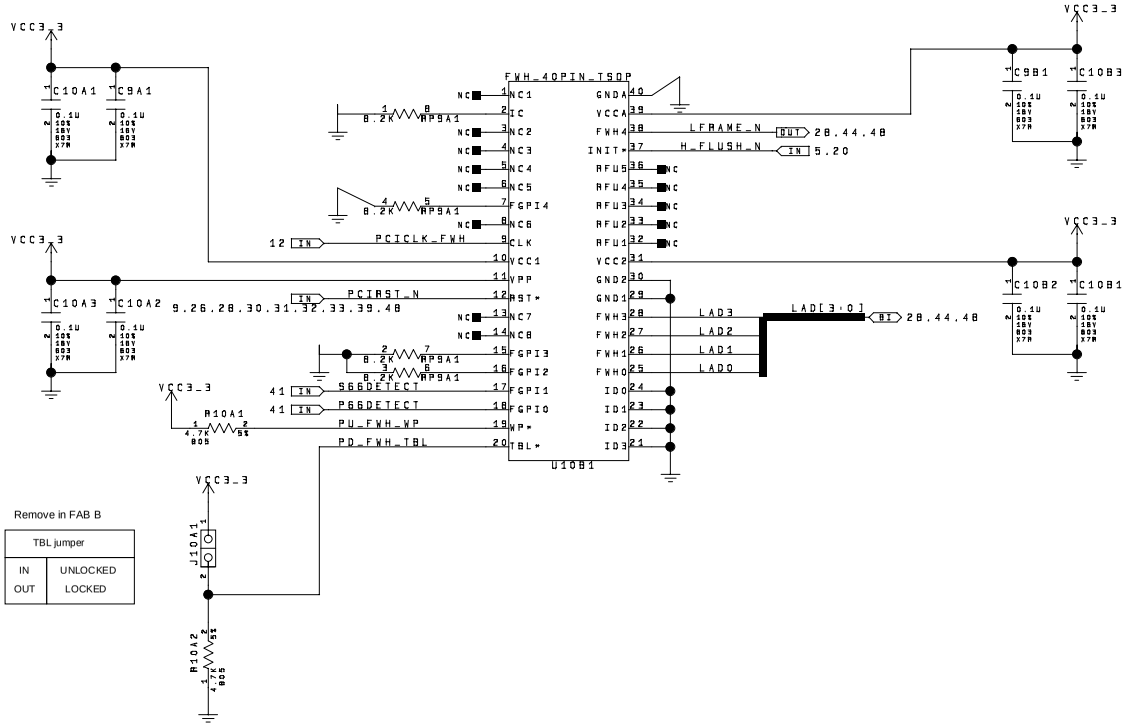
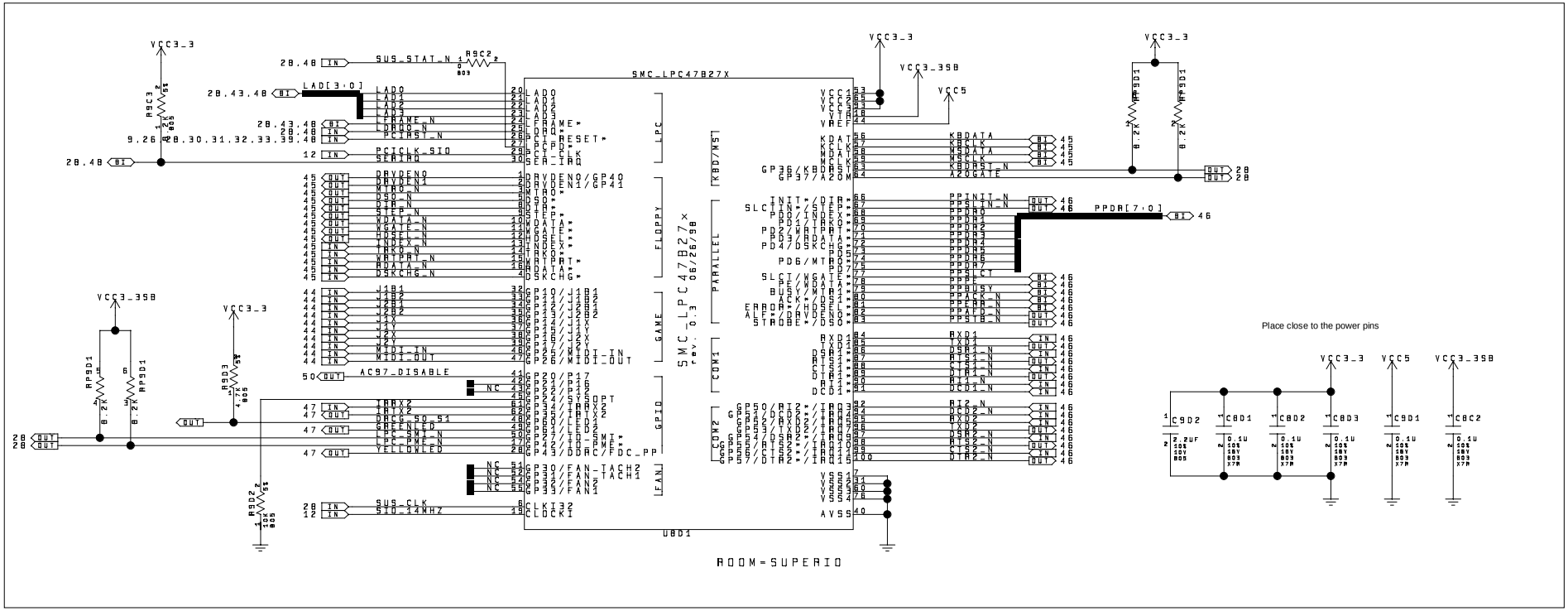


FWH

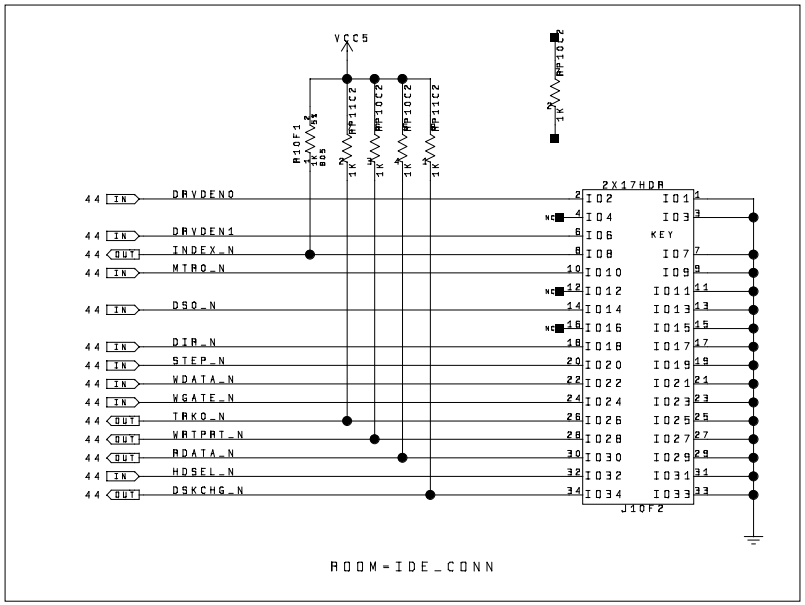
ROOM=FWH

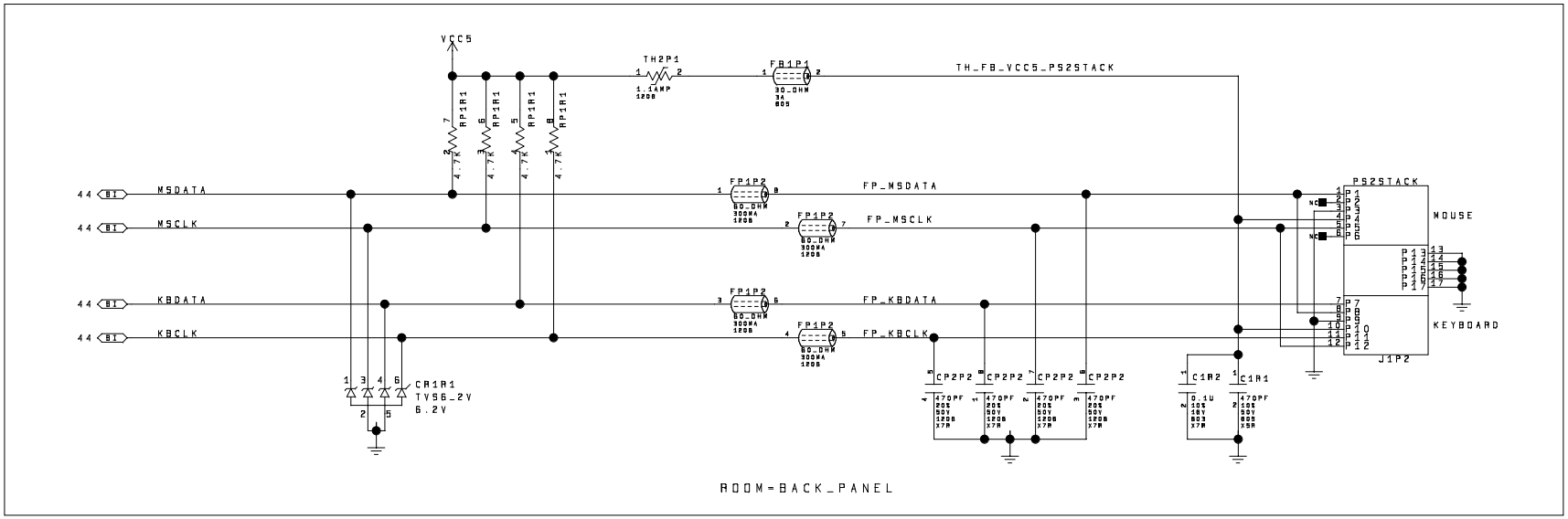
TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	43 OF 53



LPC SIO / GAMEPORT HEADER

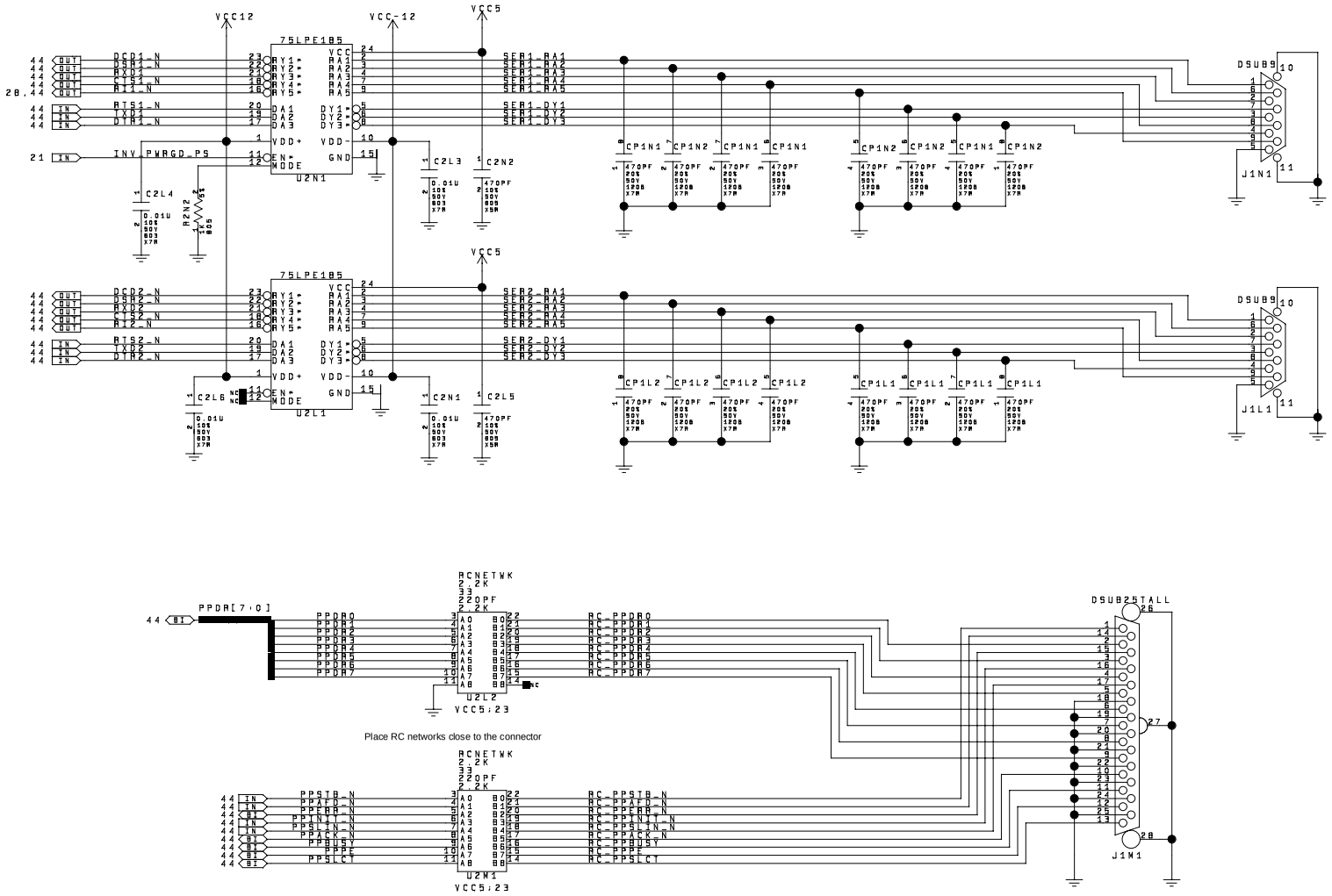
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	44 OF 53





FLOPPY / KBD / MOUSE CONN

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	45 OF 53

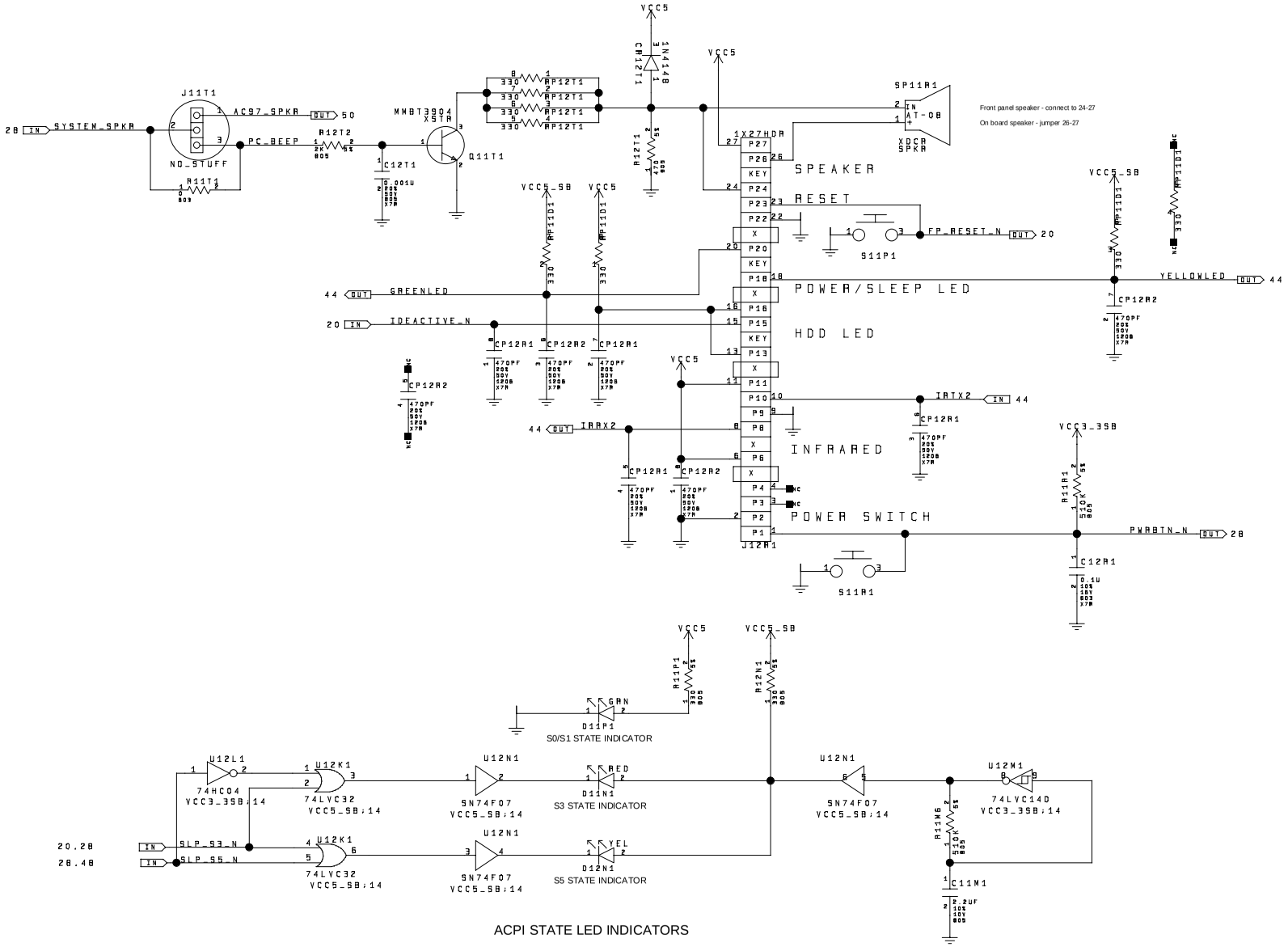


Place RC networks close to the connector

SERIAL / PARALLEL CONN

ROOM=BACK_PANEL

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	46 OF 53



ACPI STATE LED INDICATORS

ROOM=FRONT_PANEL

FRONT PANEL CONNECTOR / SPEAKER / ACPI LEDS

TITLE:		Rev: A
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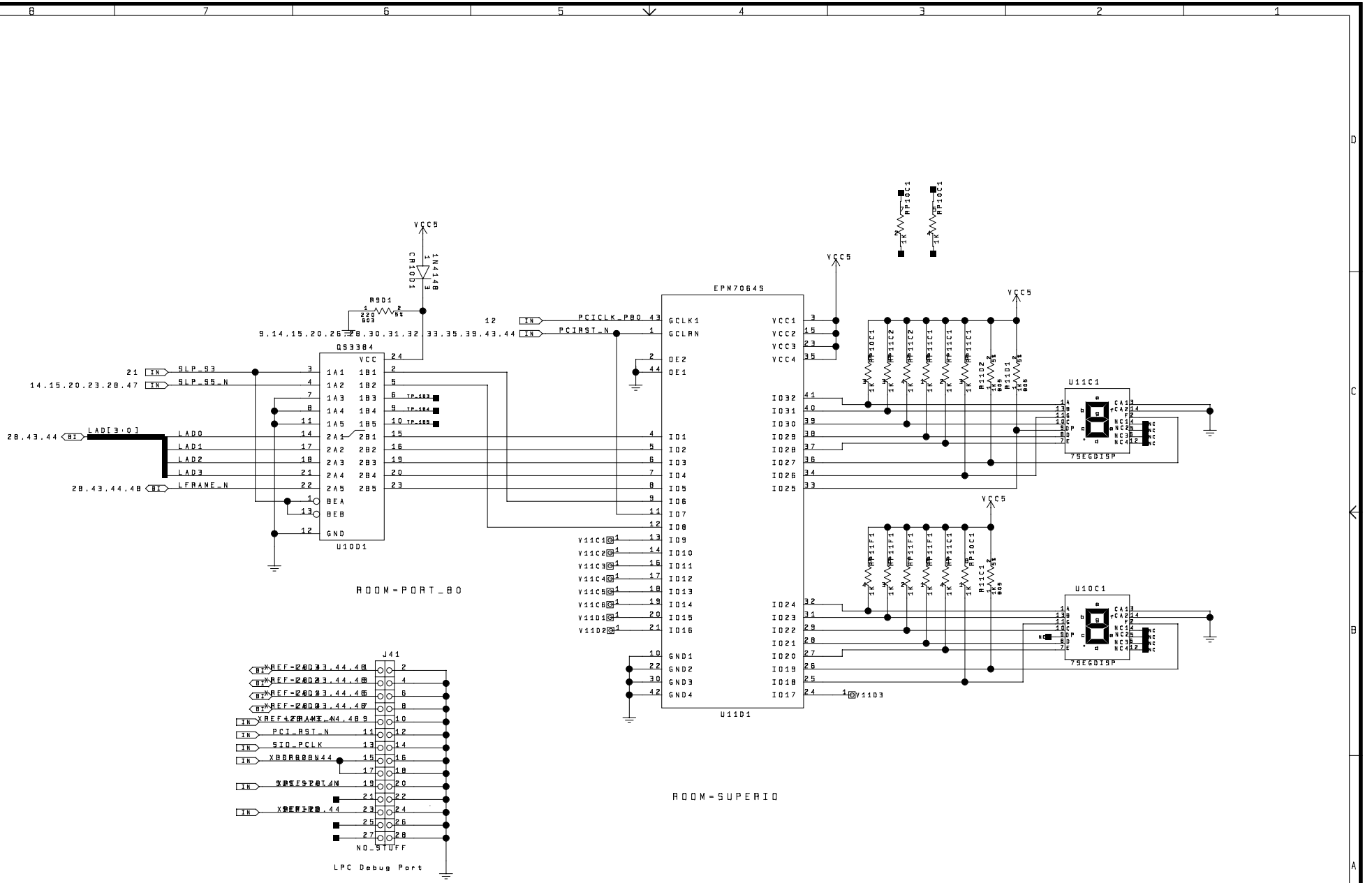

LPC / PORT 80 DISPLAY

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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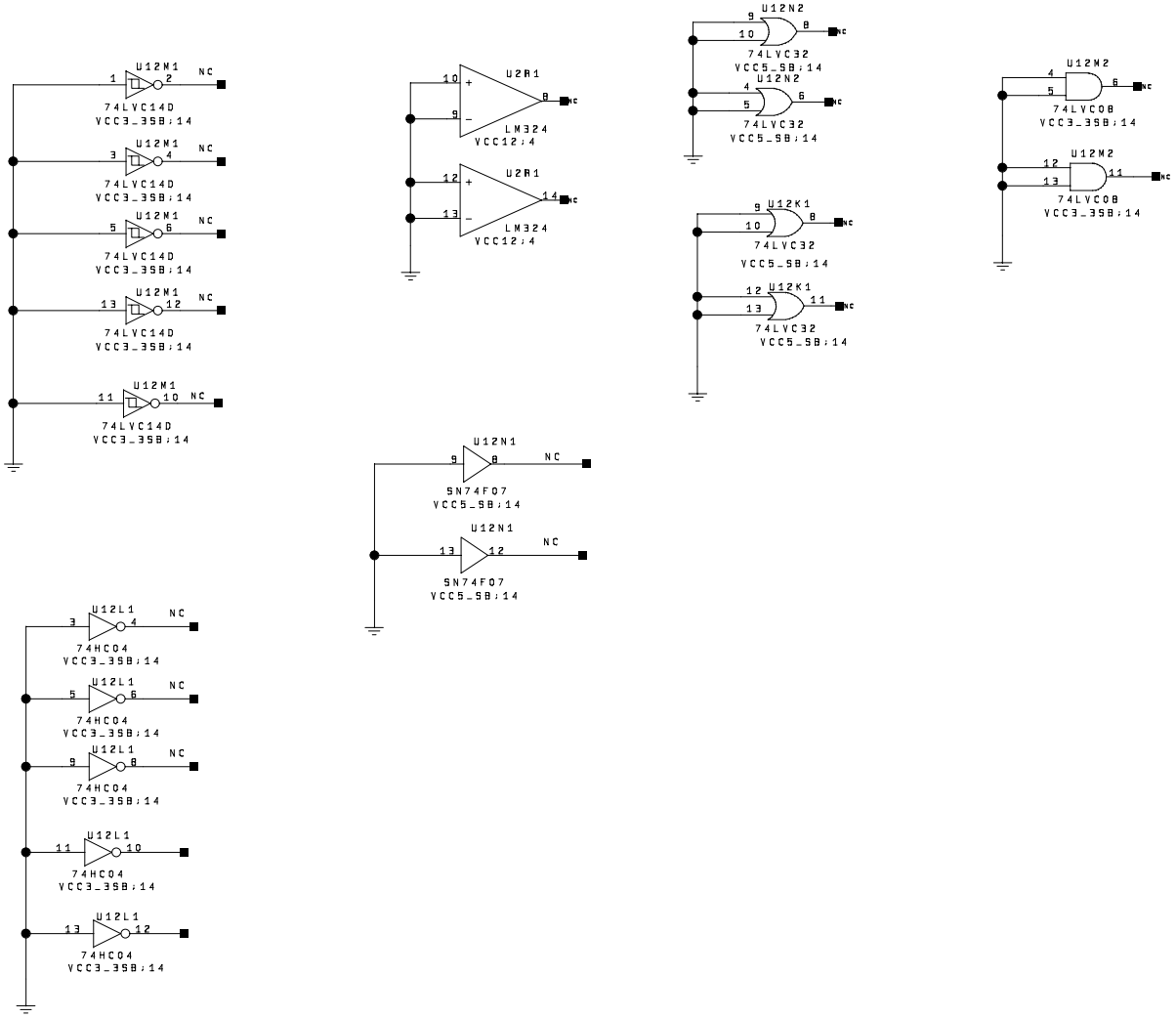

SPARE LOGIC

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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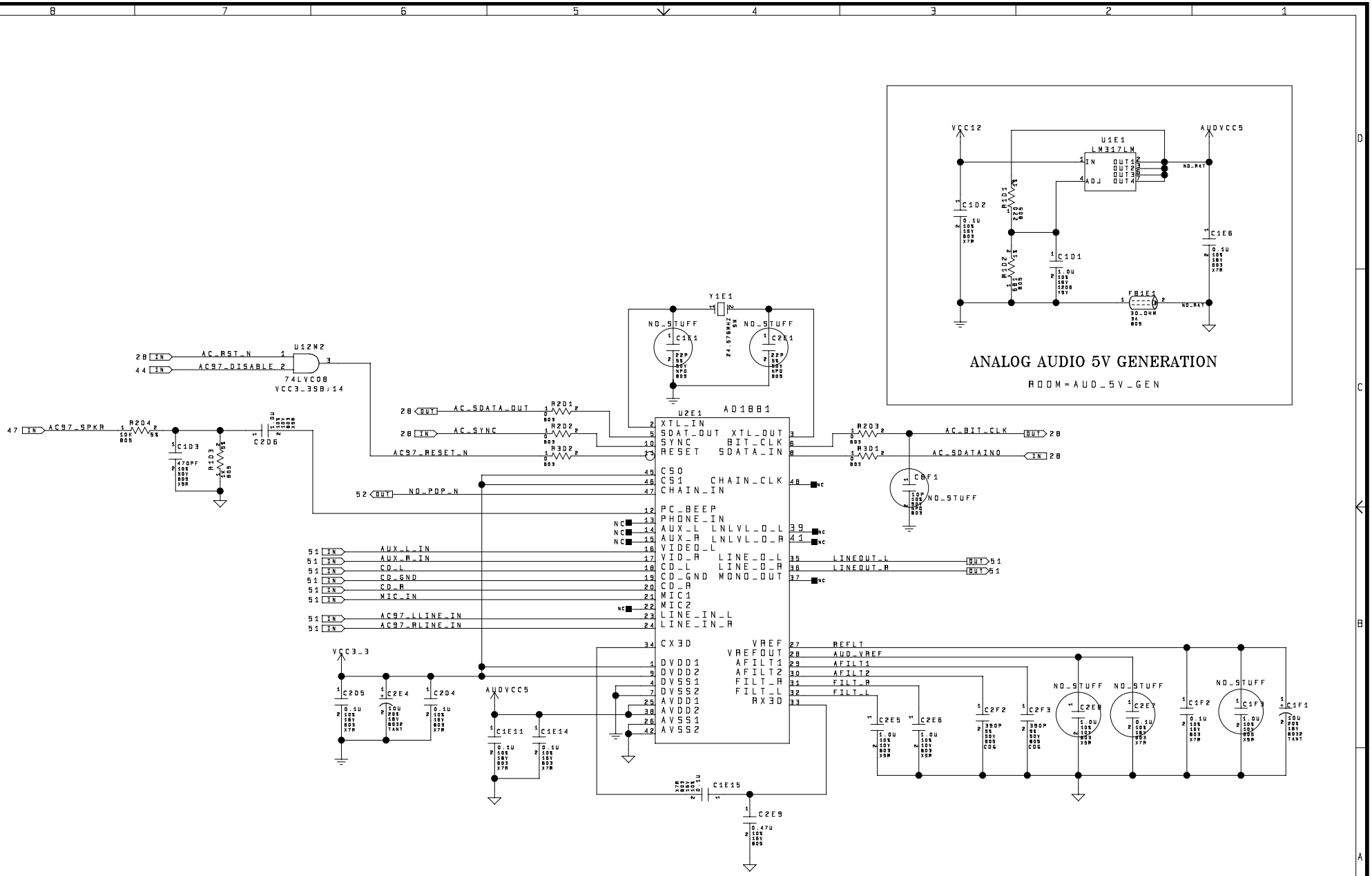
ANALOG AUDIO 5V GENERATION
ROOM=AUD_5V_GEN
VCC12
AUDVCC5
U1E1
LM317LM
R1D1
220
R1D2
C1D1
C1D2
C1E6
FB1E1
30_OHM
NO_RA1
AC_RST_N
AC97_DISABLE_2
U12M2
74LVC08
VCC3_3SB;14
Y1E1
24.576MHZ
NO_STUFF
C1E1
C2E1
U2E1
AD1881
AC_SDATA_OUT
AC_SYNC
AC97_RESET_N
R2D1
R2D2
R3D2
AC97_SPKR
R2D4
C1D3
C2D6
R1D3
NO_POP_N
R2D3
R3D1
AC_BIT_CLK
AC_SDATAINO
C8F1
XTL_IN
SDAT_OUT
SYNC
RESET
XTL_OUT
BIT_CLK
SDATA_IN
CS0
CS1
CHAIN_CLK
CHAIN_IN
PC_BEEP
PHONE_IN
AUX_L
AUX_R
VIDEO_L
VID_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
LNLVL_O_L
LNLVL_O_R
LINE_O_L
LINE_O_R
MONO_OUT
CX3D
DVDD1
DVDD2
DVSS1
DVSS2
AVDD1
AVDD2
AVSS1
AVSS2
VREF
VREFOUT
AFILT1
AFILT2
FILT_R
FILT_L
RX3D
AUX_L_IN
AUX_R_IN
CD_L
CD_GND
CD_R
MIC_IN
AC97_LLINE_IN
AC97_RLINE_IN
LINEOUT_L
LINEOUT_R
REFLT
AUD_VREF
AFILT1
AFILT2
FILT_R
FILT_L
VCC3_3
AUDVCC5
C2D5
C2E4
C2D4
C1E11
C1E14
C1E15
C2E9
C2E5
C2E6
C2F2
C2F3
C2E8
C2E7
C1F2
C1F3
C1F1
NO_STUFF
AUDIO CODEC 97
ROOM=AUD_CODEC
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 5-12-2000_16:09
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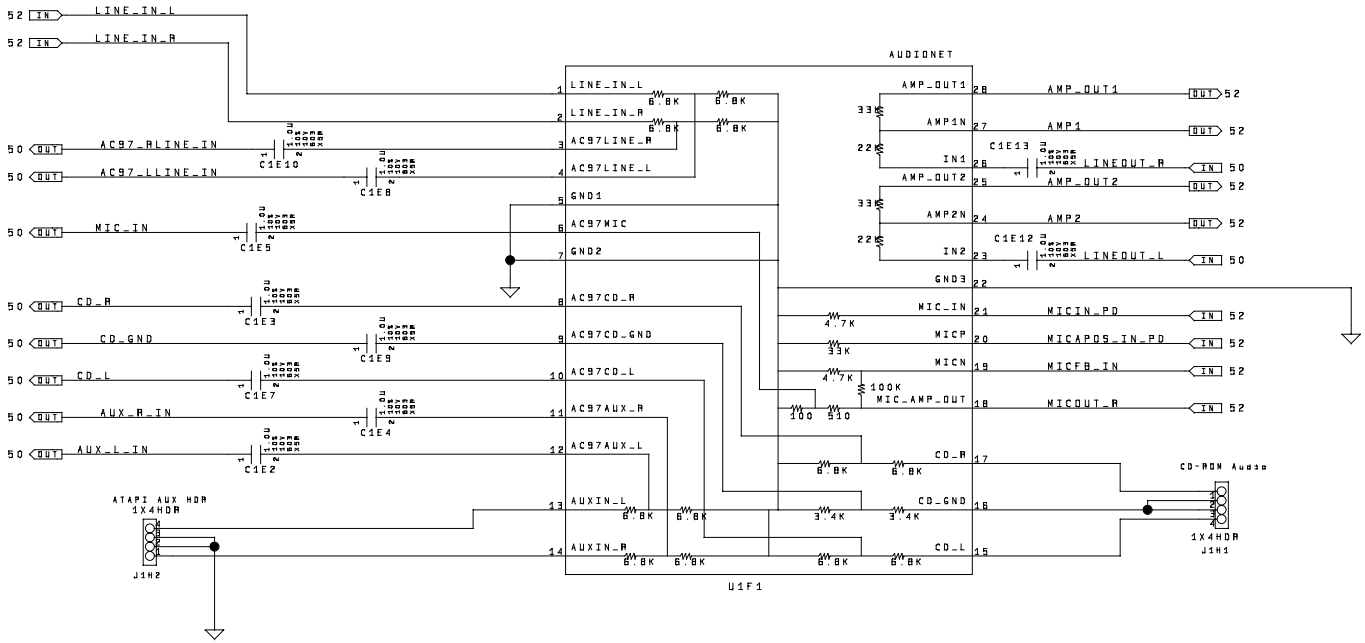

AUDIO NET

ROOM=AUD_CODEC

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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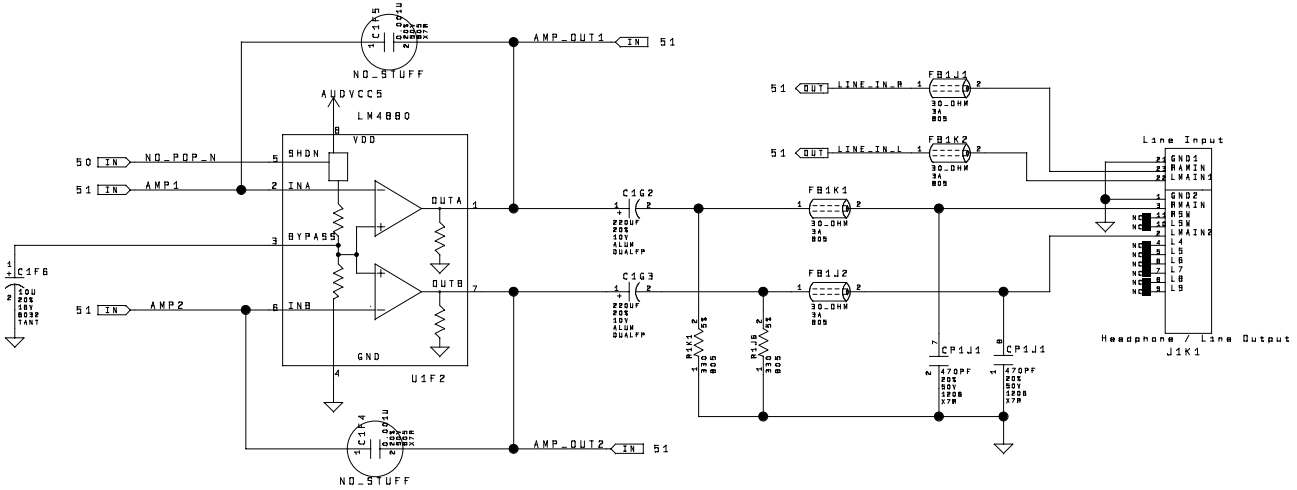

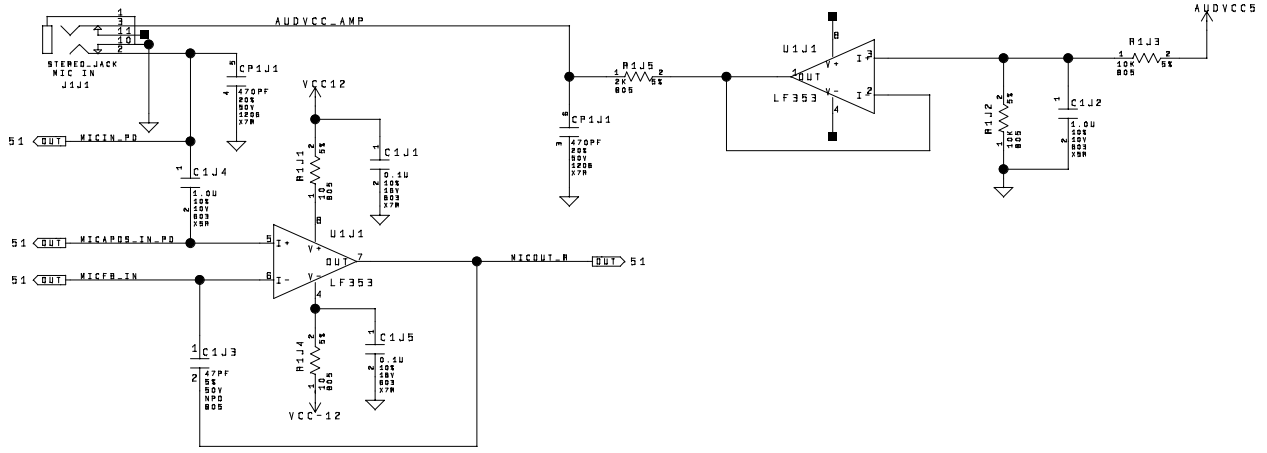

ROOM=BACK_PANEL

AUDIO LINE IN / LINE OUT / MIC IN

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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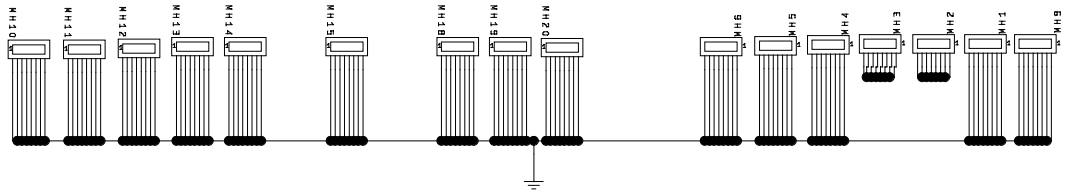

PCB MOUNTING HOLES

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