Intel® Celeron™ Processor at 266 MHz, 300 MHz, 300A MHz, and 333 MHz

Datasheet

Product Features

- Available at 266 MHz and 300 MHz core frequencies without cache; 300 MHz and 333 MHz core frequencies with cache
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Dynamic execution micro architecture
- Operates on a 66 MHz, transaction-oriented system bus
- Intel's first processor designed for the Basic PC: based on the same P6 micro architecture used in the Pentium® II processor with the capabilities of MMX™ technology
- Power Management capabilities
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Uses cost-reduced Single Edge Processor (S.E.P.) Package technology while maintaining compatibility with SC 242
- Integrated high performance 32 KB instruction and data, nonblocking, level one cache: separate 16 KB instruction and 16 KB data caches
- Integrated thermal diode

The Intel® Celeron™ processor is designed for Basic PC desktops, and is binary compatible with previous generation Intel architecture processors. The Intel® Celeron processor provides good performance for applications running on advanced operating systems such as Windows* 95, Windows NT and UNIX*. This is achieved by integrating the best attributes of Intel processors—the dynamic execution performance of the P6 microarchitecture plus the capabilities of MMX™ technology—bringing a balanced level of performance to the Basic PC buyers. The Intel® Celeron processor offers the dependability you expect from Intel at an exceptional value. Systems based on Intel® Celeron processors also include the latest features to simplify system management and lower the cost of ownership for small business and home environments.

Order Number: 243658-003
August 1998

Datasheet

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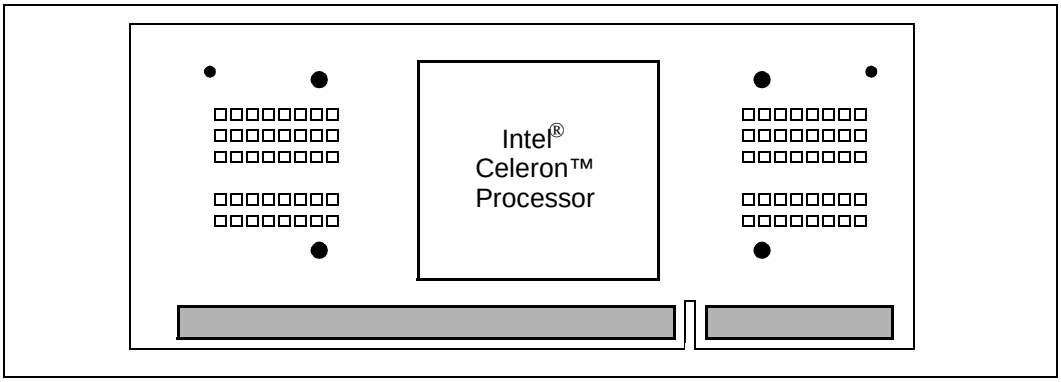
1.0 Introduction

The Intel® Celeron™ processor is the next addition to the P6 micro achitecture processor product lines. The Intel® Celeron™ processor, like the Pentium® Pro and Pentium® II processor, features a Dynamic Execution microarchitecture and also executes MMX media technology instructions for enhanced media and communication performance. The Intel processor also utilizes multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

The Intel® Celeron™ processor is capable of running today's most common PC applications. The Intel® Celeron™ processor is intended for Basic PC Systems. Support for multiprocessor based systems is not provided with the Intel® Celeron™ processor. The Pentium II processor should be used for dual-processor system designs.

To enable cost-reduction at both the processor and system level, the Intel® Celeron™ processor will utilize a new cost-reduced packaging technology, named S.E.P. Package (Single-edge Processor Package). This design lacks the thermal plate, cover, and latch arms of the Single Edge Contact (S.E.C.) cartridge currently used on the Pentium II processor. Different heatsink attachment and processor retention solutions are required to support this packaging technology, with design emphasis centered on cost-reduction. This design and associated heatsink attachment and retention solutions provide a low-cost medium for future Intel® Celeron™ processors targeted for cost-reduced systems.

Figure 1. Intel® Celeron™ Processor



1.1 Terminology

In this document, a '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D#[3:0] = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term "system bus" refers to the interface between the processor, system core logic (a.k.a. the AGPset components), and other bus agents. The system bus is an interface to the processor, memory, and I/O.

1.1.1 Package Terminology

The following terms are used often in this document and are explained here for clarification:

- **Intel® Celeron™ processor**—The entire product including internal components, substrate and core.
- **Processor substrate**—The structure on which components are mounted (with or without components attached).
- **Processor core**—The processor's execution engine.
- **S.E.P. Package**—Single-Edge Processor Package, differs from the S.E.C. cartridge as this processor has no external plastic cover, thermal plate or latch arms.

Additional terms referred to in this and other related documentation:

- **SC 242**—The 242-contact slot connector that the S.E.P. Package plugs into, just as the Pentium® Pro processor uses Socket 8.
- **Retention mechanism**—An enabled mechanical assembly which holds the package in the SC 242 connector.

1.2 References

The reader of this specification should also be familiar with material and concepts presented in the following documents:

- Intel® Celeron™ Processor Enabling Components Supplier Guide Rev 1.1
- AP-485, *Intel Processor Identification and the CPUID Instruction* (Order Number 241618)
- AP-585, *Pentium® II Processor GTL+ Guidelines* (Order Number 243330)
- AP-586, *Pentium® II Processor Thermal Design Guidelines* (Order Number 243331)
- AP-587, *Pentium® II Processor Power Distribution Guidelines* (Order Number 243332)
- AP-589, *Pentium® II Processor Electro-Magnetic Interference* (Order Number 243334)
- *Pentium® II Processor at 233, 266, 300, and 333 MHz* (Order Number 243335)
- *Intel® Celeron™ Processor Specification Update* (Order Number 243337)
- *Slot 1 Connector Specification* (Order Number 243397)
- *Pentium® II Processor Developer's Manual* (Order Number 243502)
- *Intel Architecture Software Developer's Manual* (Order Number 243193)
  - *Volume I: Basic Architecture* (Order Number 243190)
  - *Volume II: Instruction Set Reference* (Order Number 243191)
  - *Volume III: System Programming Guide* (Order Number 243192)
- *Pentium® II Processor I/O Buffer Models*, Quad Format (Electronic Form)

2.0 Electrical Specifications

2.1 The Intel® Celeron™ Processor System Bus and V_{REF}

Most Intel® Celeron processor signals use a variation of the low voltage Gunning Transceiver Logic (GTL) signaling technology.

The Intel Celeron processor system bus specification is similar to the GTL specification, but has been enhanced to provide larger noise margins and reduced ringing. The improvements are accomplished by increasing the termination voltage level and controlling the edge rates. Because this specification is different from the standard GTL specification, it is referred to as **GTL+** in this document. For more information on GTL+ specifications, see AP-585, *Pentium® II Processor GTL+ Guidelines* (Order Number 243330).

The GTL+ signals are open-drain and require termination to a supply that provides the high signal level. The GTL+ inputs use differential receivers which require a reference signal (V_{REF}). V_{REF} is used by the receivers to determine if a signal is a logical 0 or a logical 1, and is generated on the S.E.P Package for the processor core. Local V_{REF} copies should be generated on the motherboard for all other devices on the GTL+ system bus. Termination (usually a resistor at each end of the signal trace, however, if careful attention is paid to controlling trace lengths and layout, it may be possible to achieve single ended termination) is used to pull the bus up to the high voltage level and to control reflections on the transmission line. The processor contains termination resistors that provide termination for one end of the Intel Celeron processor system bus. These specifications assume another resistor at the end of each signal trace to ensure adequate signal quality for the GTL+ signals; see Table 9 for the bus termination voltage specifications for GTL+ and the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the GTL+ bus specification. Solutions exist for single-ended termination as well, though solution space is affected.

The GTL+ bus depends on incident wave switching. Therefore timing calculations for GTL+ signals are based on **flight time** as opposed to capacitive deratings. Analog signal simulation of the Intel Celeron processor system bus including trace lengths is highly recommended when designing a system, especially for systems using a single set of termination resistors (i.e., those on the processor substrate only) with the Intel 440LX, or 440EX AGPset. Such designs **will not** match the solution space allowed for by installation of termination resistors on the motherboard. See the *Pentium® II Processor GTL+ Layout Guidelines* and the *Pentium® II Processor I/O Buffer Models*, Quad Format (Electronic Form) for details.

2.2 Clock Control and Low Power States

Intel® Celeron processors allow the use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 2 for a visual representation of the Intel Celeron processor low power states.

For the processor to fully realize the low current consumption of the Stop-Grant, Sleep, and Deep Sleep states, a Model Specific Register (MSR) bit must be set. For the MSR at 02AH (Hex), bit 26 must be set to a '1' (this is the power on default setting) for the processor to stop all internal clocks during these modes. For more information, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

2.2.1 Normal State—State 1

This is the normal operating state for the processor.

2.2.2 AutoHALT Power Down State—State 2

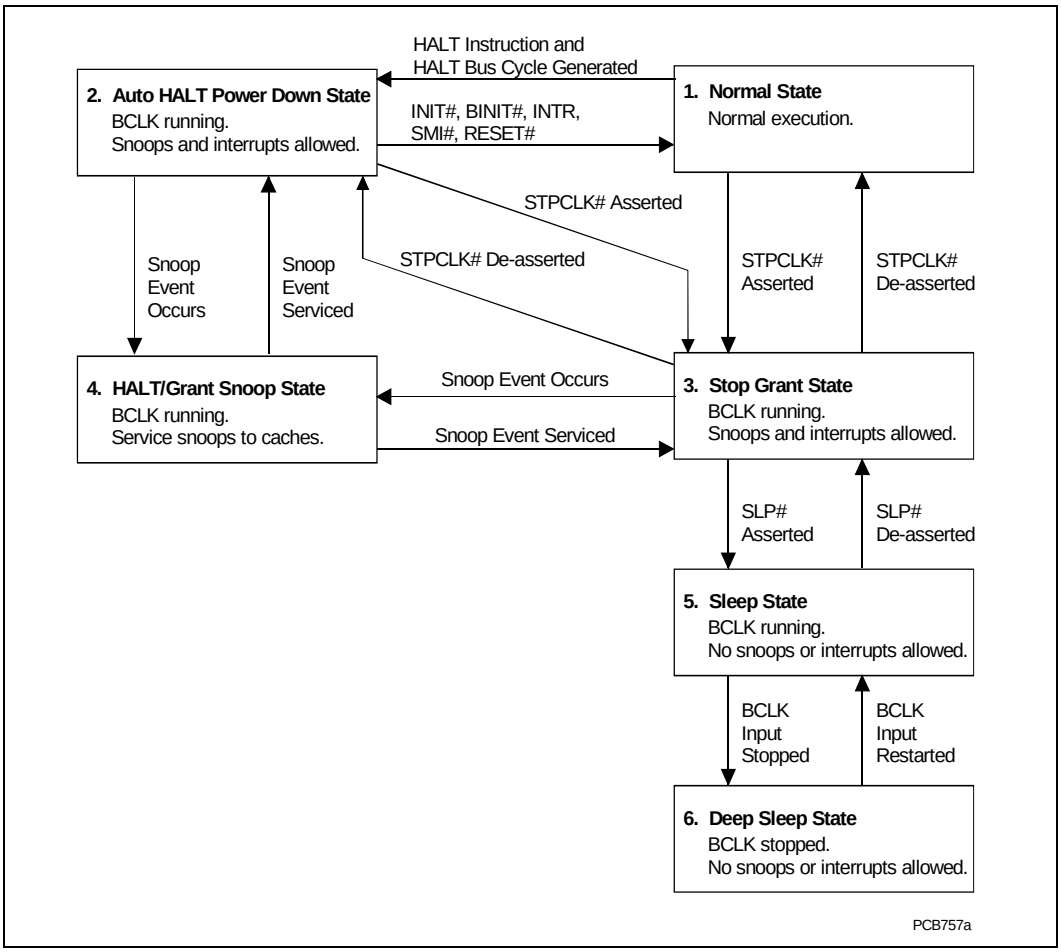
AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* (Order Number 243192) for more information.

FLUSH# will be serviced during the AutoHALT state, and the processor will return to the AutoHALT state.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

Figure 2. Clock Control State Machine



2.2.3 Stop-Grant State—State 3

The Stop-Grant state on the processor is entered when the STPCLK# signal is asserted.

Since the GTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will be recognized while the processor is in Stop-Grant state. If STPCLK# is still asserted at the completion of the BINIT# bus initialization, the processor will remain in Stop-Grant mode. If the STPCLK# is not asserted at the completion of the BINIT# bus initialization, the processor will return to Normal state.

FLUSH# will be serviced during Stop-Grant state, and the processor will return to the Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 2.2.4). A transition to the Sleep state (see Section 2.2.4) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

2.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the Intel® Celeron processor system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the Intel Celeron processor system bus has been serviced (whether by the processor or another agent on the Intel Celeron processor system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

2.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the SLP# pin can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK input. (See Section 2.2.6.) Once in the Sleep state, the SLP# pin can be deasserted if another asynchronous system bus event occurs. The SLP# pin has a minimum assertion of one BCLK period.

2.2.6 Deep Sleep State—State 6

The Deep Sleep state is the lowest power state the processor can enter while maintaining context. The Deep Sleep state is entered by stopping the BCLK input (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BLCK is stopped. It is recommended that the BLCK input be held low during the Deep Sleep State. Stopping of the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BLCK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep State. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.2.7 Clock Control

When the processor is in the Sleep or Deep Sleep states, it will not respond to interrupts or snoop transactions. PICCLK should not be removed during the AutoHALT Power Down or Stop-Grant states. PICCLK can be removed during the Sleep or Deep Sleep states. When transitioning from the Deep Sleep state to the Sleep state, PICCLK must be restarted with BCLK.

2.3 Power and Ground Pins

There are five pins defined on the package for voltage identification (VID). These pins specify the voltage required by the processor core. These have been added to cleanly support voltage specification variations on current and future Intel® Celeron processors.

For clean on-chip power distribution, Intel Celeron processors have 27 V_{CC} (power) and 30 V_{SS} (ground) inputs. The 27 V_{CC} pins are further divided to provide the different voltage levels to the components. $V_{CC_{CORE}}$ inputs for the processor core account for 19 of the V_{CC} pins, while 4 V_{TT} inputs (1.5 V) are used to provide a GTL+ termination voltage to the processor. One V_{CC5} pin is provided for use by the Slot 1 Test Kit. V_{CC5}, and $V_{CC_{CORE}}$ must remain electrically separated from each other. On the circuit board, all $V_{CC_{CORE}}$ pins must be connected to a voltage island. Similarly, all V_{SS} pins must be connected to a system ground plane.

2.4 Decoupling Guidelines

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This causes voltages on power planes to sag below their nominal values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 6, failure to do so can result in timing violations or a reduced lifetime of the component.

2.4.1 Intel® Celeron™ Processor $V_{CC_{CORE}}$ Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep an interconnect resistance from the regulator (or VRM pins) to the SC 242 connector of less than 0.3 mΩ. This can be accomplished by keeping a maximum distance of 1.0 inches between the regulator output and SC 242 connector. The recommended $V_{CC_{CORE}}$ interconnect is a 2.0 inch wide (the width of the VRM 8.2 connector) by 1.0 inch long (maximum distance between the SC 242 connector and the VRM connector) plane segment with a standard 1-ounce plating. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, is provided on the voltage regulation module (VRM). The $V_{CC_{CORE}}$ input should be capable of delivering a recommended minimum $dI_{CC_{CORE}}/dt$ (defined in Table 6) while maintaining the required tolerances (also defined in Table 6).

2.4.2 Intel® Celeron™ Processor System Bus GTL+ Decoupling

The Intel Celeron processor contains high frequency decoupling capacitance on the processor substrate; bulk decoupling must be provided for by the system motherboard for proper GTL+ bus operation. See AP-585, *Pentium® II Processor GTL+ Guidelines* (Order Number 243330), AP-587, *Pentium® II Processor Power Distribution Guidelines* (Order Number 243332), and the *Pentium® II Processor Developer's Manual* (Order Number 243502) for more information.

2.5 Intel® Celeron™ Processor System Bus Clock and Processor Clocking

The BCLK input directly controls the operating speed of the Intel® Celeron processor system bus interface. All Intel Celeron processor system bus timing parameters are specified with respect to the rising edge of the BCLK input. The Intel Celeron processor core frequency must be configured during Reset by using the A20M#, IGNNE#, LINT[1]/NMI, and LINT[0]/INTR pins (see Table 1). The value on these pins during Reset determines the multiplier that the PLL will use for the internal core clock. See the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the definition of these pins during Reset and the operation of the pins after Reset.

Table 1. Core Frequency to System Bus Multiplier Configuration

Multiplication of Processor Core Frequency to System Bus Frequency	LINT[1]	LINT[0]	A20M#	IGNNE#
1/4	L	L	H	L
2/9	L	H	H	L
safe	L	L	L	L
safe	H	H	H	H
1/5	L	H	H	H

See Figure 3 for the timing relationship between the system bus multiplier signals, RESET#, CRESET#, and normal processor operation. Using CRESET# (CMOS Reset) and the timing shown in Figure 3, the circuit in Figure 4 can be used to share these configuration signals. The component used as the multiplexer must not have outputs that drive higher than 2.5 V in order to meet the processor's 2.5 V tolerant buffer specifications. The multiplexer output current should be limited to 200 mA maximum, in case the $V_{CC_{CORE}}$ supply to the processor ever fails.

As shown in Figure 4, the 330 ohm pull-up resistors between the multiplexer and the processor (see Table 3 for appropriate values) force a "safe" ratio into the processor in the event that the processor powers up before the multiplexer and/or core logic. This prevents the processor from ever seeing a ratio higher than the final ratio.

If the multiplexer were powered by 2.5 V, a pull-down could be used on CRESET# instead of the four between the multiplexer and the Intel Celeron processor. In this case, the multiplexer must be designed such that the compatibility inputs are truly ignored, as their state is unknown.

In any case, the compatibility inputs to the multiplexer must meet the input specifications of the multiplexer. This may require a level translation before the multiplexer inputs unless the inputs and the signals driving them are already compatible.

Multiplying the bus clock frequency is required to increase performance while allowing for cost effective distribution of signals within a system. The system bus frequency multipliers supported are shown in Table 12; **other combinations will not be validated**.

Clock multiplying within the processor is provided by the internal Phase Lock Loop (PLL), which requires a constant frequency BCLK input. The system bus frequency ratio cannot be changed dynamically during normal operation, nor can it be changed during any low power modes. The system bus frequency ratio can be changed when RESET# is active, assuming that all Reset specifications are met.

Figure 3. Timing Diagram of Clock Ratio Signals

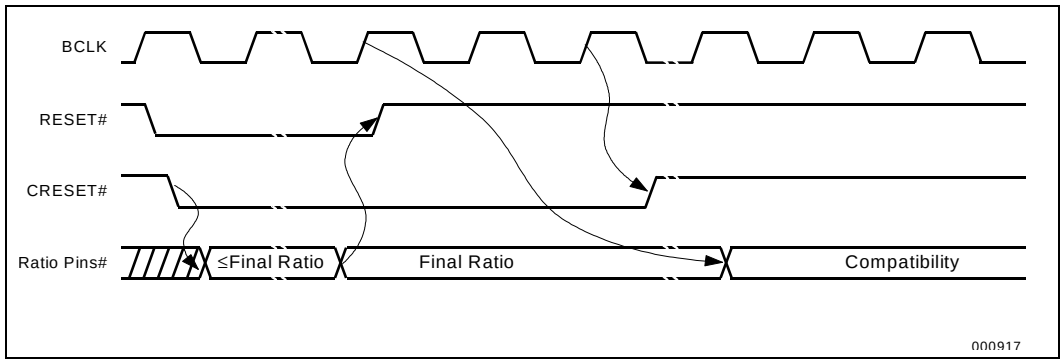
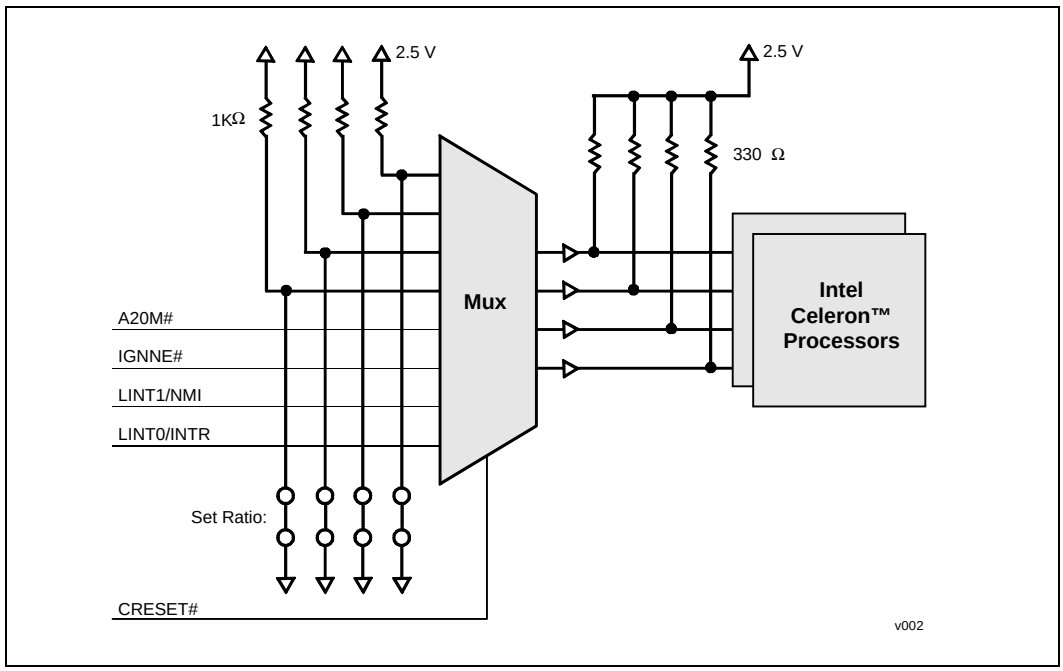


Figure 4. Example Schematic for Forcing a Safe Bus Fraction Ratio



2.6 Voltage Identification

There are five voltage identification pins on the SC 242 connector. These pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to V_{SS} on the processor. The combination of opens and shorts defines the voltage required by the processor core. The VID pins are needed to cleanly support voltage specification variations on current and future Intel® Celeron processors. These pins (VID[0] through VID[4]) are defined in Table 2. A '1' in this table refers to an open pin and a '0' refers to a short to ground. The definition provided in Table 2 is a superset of the definition previously defined for the Pentium Pro processor. The power supply must supply the voltage that is requested or disable itself.

Table 2. Voltage Identification Definition [1, 2, 3]

Processor Pins					
VID4	VID3	VID2	VID1	VID0	$V_{CC_{CORE}}$
01111 - 00110					Reserved
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00[4]
0	0	0	0	0	2.05
1	1	1	1	1	No Core
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

NOTES:
1. 0 = Processor pin connected to V_{SS}.
2. 1 = Open on processor; may be pulled up to TTL V_{IH} on motherboard.
3. VRM output should be disabled for $V_{CC_{CORE}}$ values less than 1.80 V.
4. The Intel® Celeron™ processor core will be powered off 2.0 V.

Note that the ‘11111’ (all opens) ID can be used to detect the absence of a processor core in a given slot as long as the power supply used does not affect these lines. Detection logic and pull-ups should not affect VID inputs at the power source (see Section 7.0).

The VID pins should be pulled up to a TTL-compatible level with external resistors to the power source of the regulator only if required by the regulator or external logic monitoring the VID[4:0] signals. The power source chosen must be guaranteed to be stable whenever the supply to the voltage regulator is stable. This will prevent the possibility of the processor supply going above the specified $V_{CC_{CORE}}$ in the event of a failure in the supply for the VID lines. In the case of a DC-to-DC converter, this can be accomplished by using the input voltage to the converter for the VID line pull-ups. A resistor of greater than or equal to 10 kΩ may be used to connect the VID signals to the converter input.

2.7 Intel® Celeron™ Processor System Bus Unused Pins

All RESERVED pins must remain unconnected. Connection of these pins to $V_{CC_{CORE}}$, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Intel Celeron products. See Section 5.2 for a pin listing of the processor and the location of each RESERVED pin.

The TESTHI pin must be connected to 2.5 V via a pull-up resistor of between 1 kΩ and 100 kΩ value.

PICCLK must be driven with a valid clock input and the PICD[1:0] lines must be pulled-up to 2.5 V even when the APIC will not be used. A separate pull-up resistor must be provided for each PICD line (see Table 3 for recommended values).

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused GTL+ inputs should be left as no connects; GTL+ termination is provided on the processor. Unused active low CMOS inputs should be connected to 2.5 V. Unused active high inputs should be connected to ground (V_{SS}). Unused outputs can be left unconnected. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused pins, it is suggested that ~10 kΩ resistors be used for pull-ups (except for PICD[1:0] discussed above), and ~1 kΩ resistors be used as pull-downs.

2.8 Intel® Celeron™ Processor System Bus Signal Groups

In order to simplify the following discussion, the Intel® Celeron processor system bus signals have been combined into groups by buffer type. **All Intel Celeron processor system bus outputs are open drain** and require a high-level source provided externally by the termination or pull-up resistor.

GTL+ input signals have differential input buffers, which use V_{REF} as a reference signal. GTL+ output signals require termination to 1.5 V. In this document, the term “GTL+ Input” refers to the GTL+ input group as well as the GTL+ I/O group when receiving. Similarly, “GTL+ Output” refers to the GTL+ output group as well as the GTL+ I/O group when driving.

EMI pins should be connected to motherboard ground and/or to chassis ground through zero ohm (0Ω) resistors. The zero ohm resistors should be placed in close proximity to the SC 242 connector. The path to chassis ground should be short in length and have a low impedance.

The CMOS, Clock, APIC, and TAP inputs can each be driven from ground to 2.5 V. The CMOS, APIC, and TAP outputs are open drain and should be pulled high to 2.5 V. This ensures not only correct operation for current Intel Celeron processors, but compatibility for future Intel Celeron products as well. See Table 3 for recommended pull-up resistor values on each CMOS signal. ~150Ω resistors are expected on the PICD[1:0] lines; other values in Table 3 are specified for proper logic analyzer and test mode operation only.

Table 3. Recommended Pull-up Resistor Values (Approximate) for CMOS Signals [1, 2, 3]

Recommended Resistor Value (Approximate)	CMOS Signal
150	TDI, TDO, TMS, PICD[0], PICD[1]
150–220	FERR#, IERR#, THERMTRIP#
150–330	A20M#, IGNNE#, INIT#, LINT[1]/NMI, LINT[0]/INTR, PWRGOOD, SLP#, PREQ#
410	STPCLK#, SMI#
500	FLUSH#
1KΩ–100KΩ	TESTHI

NOTES:
1. These resistor values are recommended for system implementations using open-drain CMOS buffers.
2. ~150Ω resistors are expected for these signals. This value may vary by system and should be correlated with the output drive characteristics of the devices generating the input signals. Other approximate values are recommended for proper operation with the Pentium® II processor LAI.
3. TRST# must be pulled to ground via a 680Ω resistor or driven low at power on with the assertion of RESET# (see Table 20).

The groups and the signals contained within each group are shown in Table 4. Refer to Section 7.0 for descriptions of these signals.

Table 4. Intel® Celeron™ Processor System Bus Signal Groups

Group Name	Signals
GTL+ Input	BPRI#, DEFER#, RESET#, RS[2:0]#, TRDY#
GTL+ Output	PRDY#
GTL+ I/O	A[31:3]#, ADS#, BERR#, BNR#, BP[3:2]#, BPM[1:0]#, D[63:0]#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#,
CMOS Input[4]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD[1], SMI#, SLP#[2], STPCLK#
CMOS Output[4]	FERR#, IERR#, THERMTRIP#[3]
System Bus Clock	BCLK
APIC Clock	PICCLK
APIC I/O[4]	PICD[1:0]
TAP Input[4]	TCK, TDI, TMS, TRST#
TAP Output[4]	TDO
Power/Other[5]	$V_{CC_{CORE}}$, V_{CC5}, VID[4:0], V_{TT}, V_{SS}, SLOTOCC#, BSEL#, EMI, V_{CC_L2}

NOTES:
1. See Section 7.0 for information on the PWRGOOD signal.
2. See Section 7.0 for information on the SLP# signal.
3. See Section 7.0 for information on the THERMTRIP# signal.
4. These signals are specified for 2.5 V operation. See Table 3 for recommended pull-up resistor values.
5. $V_{CC_{CORE}}$ is the power supply for the processor core.
   VID[4:0] is described in Section 2.0.
   V_{TT} is used to terminate the system bus and generate VREF on the processor substrate.
   V_{SS} is system ground.
   TESTHI should be connected to 2.5 V with a 1–100 kΩ resistor.
   V_{CC5} is not connected to the Intel® Celeron™ processor. This supply is used for the Slot 1 Test Kit.
   SLOTOCC# is described in Section 7.0.
   BSEL# is described in Section 2.8.2 and Section 7.0.
   EMI pins are described in Section 7.0.
   V_{CC_L2} is a Pentium® II processor reserved signal provided to maintain compatibility with the Pentium® II processor and may be left as a no contect for Intel Celeron™ processor only designs.

2.8.1 Asynchronous Vs. Synchronous for System Bus Signals

All GTL+ signals are synchronous to BCLK. All of the CMOS, APIC, and TAP signals can be applied asynchronously to BCLK. All APIC signals are synchronous to PICCLK. All TAP signals are synchronous to TCK.

2.8.2 Host Bus Frequency Select Signal (BSEL#)

This signal will be asserted a logic low by the Intel Celeron processor to denote 66 MHz system bus operation. On motherboards which support operation at either 66 or 100 MHz, this signal should force the clock synthesizer into 66 MHz operation.

2.9 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Intel Celeron processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting a 2.5 V input. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

A Debug Port may be placed at the start and end of the TAP chain with the TDI of the first component coming from the Debug Port and the TDO from the last component going to the Debug Port.

2.10 Maximum Ratings

Table 5 contains the Intel Celeron processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 5. Intel® Celeron™ Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	
T_{CASE}	Processor case temperature	5.0	85	°C	
$V_{CC(All)}$	Any processor supply voltage with respect to V_{SS}	–0.5	Operating voltage + 1.0	V	1, 2
V_{inGTL}	GTL+ buffer DC input voltage with respect to V_{SS}	–0.3	$V_{CC_{CORE}}$ + 0.7	V	
V_{inCMOS}	CMOS buffer DC input voltage with respect to V_{SS}	–0.3	3.3	V	3
I_{VID}	Max VID pin current		5	mA	
$I_{SLOTOCC}$	Max SLOTOCC# pin current		5	mA	
Mech Max Edge Fingers	Mechanical integrity of processor edge fingers		50	Insertions/ Extractions	4, 5

NOTES:
1. Operating voltage is the voltage to which the component is designed to operate. See Table 6.
2. This rating applies to the $V_{CC_{CORE}}$, V_{CC5}, and any input (except as noted below) to the processor.
3. Parameter applies to CMOS, APIC, and TAP bus signal groups only.
4. The electrical and mechanical integrity of the processor edge fingers are specified to last for 50 insertion/ extraction cycles.
5. Intel has performed internal testing showing functionality of the substrate after 5000 insertions. While insertion/extraction cycling above 50 insertions will cause an increase in the contact resistance (above 0.1Ω) and a degradation in the material integrity of the edge finger gold plating, it is possible to have processor functionality above the specified limit. The S.E.P. Package has been qualified to exceed the 50 insertion/ extractions. The actual number of insertions before processor failure will vary based upon system configuration and environmental conditions.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the Intel Celeron processor edge fingers. See Section 7.0 for the processor edge finger signal definitions and Section 5.0 for the signal listing.

Most of the signals on the Intel Celeron processor system bus are in the GTL+ signal group. These signals are specified to be terminated to 1.5 V. The DC specifications for these signals are listed in Table 7.

To allow connection with other devices, the Clock, CMOS, APIC, and TAP signals are designed to interface at non-GTL+ levels. The DC specifications for these pins are listed in Table 8.

Table 6 through Table 9 list the DC specifications for Intel Celeron processors operating at 66 MHz Intel Celeron processor system bus frequencies. Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 6. Intel® Celeron™ Processor Voltage and Current Specifications [1]

Symbol	Parameter	Core Freq	Min	Typ	Max	Unit	Notes
$V_{CC_{CORE}}$	V_{CC} for processor core			2.00		V	2, 3, 4
V_{TT}	GTL+ bus termination voltage		1.365	1.50	1.635	V	1.5 ±9% [5]
Baseboard Tolerance, Static	Processor core voltage static tolerance level at SC 242 pins		–0.070		0.100	V	6
Baseboard Tolerance, Transient	Processor core voltage transient tolerance level at SC 242 pins		–0.120		0.120	V	6
$V_{CC_{CORE}}$ Tolerance, Static	Processor core voltage static tolerance level at edge fingers		–0.085		0.100	V	7
$V_{CC_{CORE}}$ Tolerance, Transient	Processor core voltage transient tolerance level at edge fingers		–0.140		0.140	V	7
$I_{CC_{CORE}}$	I_{CC} for processor core	266 MHz 300 MHz 300A MHz 333 MHz			7.05 7.89 9.21 10.13	A	8, 9, 10
I_{VTT}	Termination voltage supply current				2.7	A	11
I_{SGnt}	I_{CC} Stop-Grant for processor core	266 MHz 300 MHz 300A MHz 333 MHz			0.605 0.820 0.820 0.900	A	12
I_{SLP}	I_{CC} Sleep for processor core	266 MHz 300 MHz 300A MHz 333 MHz			0.609 0.700 0.700 0.800	A	
I_{DSLP}	I_{CC} Deep Sleep for processor core				0.366	A	
$dI_{CC_{CORE}}/dt$	Power supply current slew rate				20	A/µs	13, 14, 15
$dI_{CC_{VTT}}/dt$	Termination current slew rate				8	A/µs	See Table 9, Table 17, Table 18
V_{CC5}	5 V supply voltage		4.75	5.00	5.25	V	5 V ±5% [16]
I_{CC5}	I_{CC} for 5 V supply voltage			1.0		A	16

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. $V_{CC_{CORE}}$ and $I_{CC_{CORE}}$ supply the processor core.

3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.5 and Table 2 for more information.
4. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
5. V_{TT} must be held to 1.5 V ±9%. It is recommended that V_{TT} be held to 1.5 V ±3% while the Intel® Celeron™ processor system bus is idle. This is measured at the processor edge fingers.
6. These are the tolerance requirements, across a 20 MHz bandwidth, **at the** SC 242 **connector pin on the bottom side of the baseboard.** The requirements at the SC 242 connector pins account for voltage drops (and impedance discontinuities) across the connector, processor edge fingers, and to the processor core. Vcc_{CORE} must return to within the static voltage specification within 100 µs after a transient event.
7. These are the tolerance requirements, across a 20 MHz bandwidth, **at the processor edge fingers.** The requirements at the processor edge fingers account for voltage drops (and impedance discontinuities) at the processor edge fingers and to the processor core. $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event.
8. The typical $I_{CC_{CORE}}$ measurements are an average current draw during the execution of Winstone* 96 under the Windows* 95 operating system. These numbers are meant as a guideline only, not a guaranteed specification. Actual measurements will vary based upon system environmental conditions, configuration, and software.
9. Max ICC measurements are measured at VCC max voltage, under maximum signal loading conditions.
10. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of $V_{CC_{CORE}}$ ($V_{CC_{CORE\_TYP}}$). In this case, the maximum current level for the regulator, $I_{CC_{CORE\_REG}}$, can be reduced from the specified maximum current $I_{CC_{CORE\_MAX}}$ and is calculated by the equation:
    $I_{CC_{CORE\_REG}} = I_{CC_{CORE\_MAX}} \times V_{CC_{CORE\_TYP}} / (V_{CC_{CORE\_TYP}} + V_{CC_{CORE}}$ Tolerance, Transient)
11. The current specified is the current required for a single Intel Celeron processor. A similar amount of current is drawn through the termination resistors on the opposite end of the GTL+ bus, unless single-ended termination is used (see Section 2.1).
12. The current specified is also for AutoHALT state.
13. Maximum values are specified by design/characterization at nominal $V_{CC_{CORE}}$.
14. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
15. dI_{CC}/dt specifications are measured and specified at the SC 242 connector pins.
16. V_{CC_5} and I_{CC_5} are not used by the Intel Celeron processor. This supply is used for the Slot 1 Test Kit.

Table 7. GTL+ Signal Groups DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.82	V	
V_{IH}	Input High Voltage	1.22	V_{TT}	V	2, 3
Ron	Buffer On Resistance		16.67	Ω	8
I_L	Leakage Current		±100	µA	6
I_{LO}	Output Leakage Current		±15	µA	7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies and cache sizes.
2. V_{IH} and V_{OH} for the Intel Celeron processor may experience excursions of up to 200 mV above V_{TT} for a single system bus clock. However, input signal drivers must comply with the signal quality specifications in Section 3.0.
3. Minimum and maximum V_{TT} are given in Table 9.
4. Parameter correlated to measurement into a 25Ω resistor terminated to 1.5 V.
5. I_{OH} for the Intel Celeron processor may experience excursions of up to 12 mA for a single system bus clock.
6. ($0 \le V_{IN} \le 2.0$ V +5%).
7. ($0 \le V_{OUT} \le 2.0$ V +5%).
8. Refer to the IO Buffer Models for IV characteristics.

Table 8. Non-GTL+ Signal Group DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.7	V	
V_{IH}	Input High Voltage	1.7	2.625	V	2.5 V +5% maximum
V_{OL}	Output Low Voltage		0.4	V	2
V_{OH}	Output High Voltage	N/A	2.625	V	All outputs are open-drain to 2.5 V +5%
I_{OL}	Output Low Current	14		mA	
I_{LI}	Input Leakage Current		±100	µA	3
I_{LO}	Output Leakage Current		±15	µA	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Parameter measured at 14 mA (for use with TTL inputs).
3. ($0 \le V_{IN} \le 2.5$ V +5%).
4. ($0 \le V_{OUT} \le 2.5$ V +5%).

2.12 GTL+ System Bus Specifications

It is recommended that the GTL+ bus be routed in a daisy-chain fashion with termination resistors to V_{TT} at each end of the signal trace. These termination resistors are placed electrically between the ends of the signal traces and the V_{TT} voltage supply and generally are chosen to approximate the substrate impedance. The valid high and low levels are determined by the input buffers using a reference voltage called V_{REF}. Single ended termination may be possible if trace lengths are tightly controlled, see the *440LX Single Ended Termination Design Guidelines* for more information.

Table 9 below lists the nominal specification for the GTL+ termination voltage (V_{TT}). The GTL+ reference voltage (V_{REF}) is generated on the processor substrate for the processor core, but should be set to 2/3 V_{TT} for other GTL+ logic using a voltage divider on the motherboard. It is important that the motherboard impedance be specified and held to a ±20% tolerance, and that the intrinsic trace capacitance for the GTL+ signal group traces is known and well-controlled. For more details on GTL+, see the *Pentium® II Processor Developer's Manual* (Order Number 243502) and AP-585, *Pentium® II Processor GTL+ Guidelines* (Order Number 243330).

Table 9. Intel® Celeron™ Processor GTL+ Bus Specifications [1, 2]

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{TT}	Bus Termination Voltage	1.365	1.50	1.635	V	1.5 V ±9% [3]
R_{TT}	Termination Resistor		56		Ohms	±5%
V_{REF}	Bus Reference Voltage		2/3 V_{TT}		V	±2% [4]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Intel Celeron processors contain GTL+ termination resistors at the end of each signal trace on the processor substrate. Intel Celeron processors generate V_{REF} on the processor substrate by using a voltage divider on V_{TT} supplied through the SC 242 connector.
3. V_{TT} must be held to 1.5 V ±9%; dI_{CCVTT}/dt is specified in Table 6. It is recommended that V_{TT} be held to 1.5 V ±3% while the Intel Celeron processor system bus is idle. This is measured at the processor edge fingers.
4. V_{REF} is generated on the processor substrate to be 2/3 V_{TT} nominally.

2.13 Intel® Celeron™ Processor System Bus AC Specifications

The Intel® Celeron processor system bus timings specified in this section are defined at the Intel Celeron processor edge fingers and the processor core pads. Unless otherwise specified, timings are tested at the processor core during manufacturing. Timings at the processor edge fingers are specified by design characterization. See Section 7.0 for the Intel Celeron processor edge connector signal definitions. **Note that at 66 MHz system bus operation, the Intel Celeron processor timings at the processor edge fingers are identical to the Pentium II processor processor timings at the edge fingers.** See the *Pentium® II Processor at 233, 266, 300, and 333 MHz* (Order Number 243335) for more detail.

Table 10 through Table 21 list the AC specifications associated with the Intel Celeron processor system bus. These specifications are broken into the following categories: Table 10 through Table 12 contain the system bus clock specifications, Table 13 and Table 14 contain the GTL+ specifications, Table 15 and Table 16 are the CMOS signal group specifications, Table 17 contains timings for the Reset conditions, Table 18 and Table 19 cover APIC bus timing, and Table 20 and Table 21 cover TAP timing. For each pair of tables, the first table contains timing specifications for measurement or simulation at the processor edge fingers. The second table contains specifications for simulation at the processor core pads.

All Intel Celeron processor system bus AC specifications for the GTL+ signal group are relative to the rising edge of the BCLK input. All GTL+ timings are referenced to V_{REF} for both ‘0’ and ‘1’ logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Pentium II processor in Quad format as the *Pentium® II Processor I/O Buffer Models*, Quad Format (Electronic Form). GTL+ layout guidelines are also available in AP-585, *Pentium® II Processor GTL+ Guidelines* (Order Number 243330).

Care should be taken to read all notes associated with a particular timing parameter.

Table 10. Intel® Celeron™ Processor System Bus AC Specifications (Clock) at the Processor Edge Fingers [1, 2, 3]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		66.67		MHz		
T1’: BCLK Period	15.0			ns	6	4, 5, 6
T1B’: SC 242 to Core Logic BCLK Offset		0.78		ns	6	Absolute Value [7,8]
T2’: BCLK Period Stability				±300ps		See Table 11
T3’: BCLK High Time	3.99			ns	6	@>2.0 V [6]
T4’: BCLK Low Time	4.39			ns	6	@<0.5 V [6]
T5’: BCLK Rise Time	1.02		2.68	ns	6	(0.5 V–2.0 V) [6, 9]
T6’: BCLK Fall Time	1.02		2.68	ns	6	(2.0 V–0.5 V) [6, 9]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the GTL+ signals are referenced to the BCLK rising edge at 0.70 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All GTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.70 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the

processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
4. The internal core clock frequency is derived from the Intel Celeron processor system bus clock. The system bus clock to core clock ratio is determined during initialization as described in Section 2.5. Table 12 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. This specification applies to Intel Celeron processors when operating at a system bus frequency of 66 MHz.
7. The BCLK offset time is the absolute difference needed between the BCLK signal arriving at the Intel Celeron processor edge finger at 0.5 V vs. arriving at the core logic at 1.25 V. The positive offset is needed to account for the delay between the SC 242 connector and processor core. The positive offset ensures both the processor core and the core logic receive the BCLK edge concurrently.
8. See Section 3.1 for Intel Celeron processor system bus clock signal quality specifications.
9. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 11. Intel® Celeron™ Processor System Bus AC Specifications (Clock) at the Processor Core Pins [1, 2, 3]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		66.67		MHz		
T1: BCLK Period	15.0			ns	6	4, 5, 6
T2: BCLK Period Stability			±300	ps	6	6, 8, 9
T3: BCLK High Time	4.94			ns	6	@>2.0 V [6]
T4: BCLK Low Time	4.94			ns	6	@<0.5 V [6]
T5: BCLK Rise Time	0.34		1.0	ns	6	(0.5 V–2.0 V) [6, 10]
T6: BCLK Fall Time	0.34		1.0	ns	6	(2.0 V–0.5 V) [6, 10]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the GTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All GTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor core pins.
4. The internal core clock frequency is derived from the Intel Celeron processor system bus clock. The system bus clock to core clock ratio is determined during initialization as described in Section 2.5. Table 12 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. This specification applies to the Intel Celeron processor when operating at a system bus frequency of 66 MHz.
7. See Section 3.1 for Intel Celeron processor system bus clock signal quality specifications.
8. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25 V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
9. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer.
10. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 12. Valid Intel® Celeron™ Processor System Bus, Core Frequency [1, 2]

Core Frequency (MHz)	BCLK Frequency (MHz)	Frequency Multiplier
266.67	66.67	4
300	66.67	4.5
333	66.67	5

NOTES:
1. Contact your local Intel representative for the latest information on processor frequencies and/or frequency multipliers.
2. While other bus ratios are defined, operation at frequencies other than those listed are not supported.

Table 13. Intel® Celeron™ Processor System Bus AC Specifications (GTL+ Signal Group) at the Processor Edge Fingers [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T7': GTL+ Output Valid Delay	1.07	6.37	ns	7	4, 5
T8': GTL+ Input Setup Time	1.96		ns	8	4, 6, 7, 8
T9': GTL+ Input Hold Time	1.53		ns	8	4, 9
T10': RESET# Pulse Width	1.00		ms	10	10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the GTL+ signals are referenced to the BCLK rising edge at 0.50 V at the processor edge fingers. All GTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor edge fingers.
4. This specification applies to Intel Celeron processors operating with a 66-MHz Intel Celeron processor system bus only.
5. Valid delay timings for these signals are specified into 50Ω to 1.5 V and with V_{REF} at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40 V swing.
9. Specification is for a maximum 1.0 V swing.
10. After Vcc_{CORE}, and BCLK become stable.

Table 14. Intel® Celeron™ Processor System Bus AC Specifications (GTL+ Signal Group) at the Processor Core Pins [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T7: GTL+ Output Valid Delay	0.17	5.16	ns	7	5
T8: GTL+ Input Setup Time	2.10		ns	8	5, 6, 7, 8
T9: GTL+ Input Hold Time	0.77		ns	8	9
T10: RESET# Pulse Width	1.00		ms	10	7, 10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the GTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All GTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor core pins.
4. This specification applies to the Intel Celeron processor operating with a 66-MHz Intel Celeron processor system bus only.
5. Valid delay timings for these signals are specified into 25Ω to 1.5 V and with V_{REF} at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40 V swing.
9. Specification is for a maximum 1.0 V swing.
10. After V_{CCCORE} and BCLK become stable.

Table 15. Intel® Celeron™ Processor System Bus AC Specifications (CMOS Signal Group) at the Processor Edge Fingers [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T11': CMOS Output Valid Delay	1.00	10.5	ns	7	5
T12': CMOS Input Setup Time	4.50		ns	8	6, 7, 8
T13': CMOS Input Hold Time	1.50		ns	8	6, 7
T14': CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	7	Active and Inactive states
T14B: LINT[1:0] Input Pulse Width	6		BCLKs	7	9
T15': PWRGOOD Inactive Pulse Width	10		BCLKs	7, 10	10, 11

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.50 V at the processor edge fingers. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. Valid delay timings for these signals are specified to 2.5 V +5%. See Table 3 for pull-up resistor values.
6. This specification applies to Intel Celeron processors operating with a 66-MHz Intel Celeron processor system bus only.
7. To ensure recognition on a specific clock, the setup and hold times with respect to BCLK must be met.
8. INTR and NMI are only valid when the local APIC is disabled. LINT[1:0] are only valid when the local APIC is enabled.
9. This specification only applies when the APIC is enabled and the LINT1 or LINT0 pin is confiugred as an edge-triggered interrupt with fixed delivery; otherwise, specification T14 applies.

   PWRGOOD must remain below $V_{IL,max}$ (Table 7) until all the voltage planesmeet the voltage tolerance specifications in Table 6 and BCLK has met the BCLK AC specifications in Table 11 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5 V.
10. When driven inactive or after Vcc_{CORE}, and BCLK become stable.
11. If the BCLK signal meets its AC specification within 150 ns of turning on, then the PWRGOOD inactive pulse width spcification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL,max}$ until all the vlotage planes meet the voltage tolerance specificaions.

Table 16. Intel® Celeron™ Processor System Bus AC Specifications (CMOS Signal Group) at the Processor Core Pins [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T11: CMOS Output Valid Delay	0.00	8.00	ns	7	5
T12: CMOS Input Setup Time	4.00		ns	8	6, 7, 8
T13: CMOS Input Hold Time	1.30		ns	8	6, 7
T14: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	7	Active and Inactive states
T14B: LINT[1:0] Input Pulse Width	6		BCLKs	7	9
T15: PWRGOOD Inactive Pulse Width	10		BCLKs	7 10	10, 11

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pins. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. Valid delay timings for these signals are specified to 2.5 V +5%. See Table 3 for pull-up resistor values.
6. This specification applies to Intel Celeron processors operating with a 66-MHz Intel Celeron processor system bus only.
7. To ensure recognition on a specific clock, the setup and hold times with respect to BCLK must be met.
8. INTR and NMI are only valid when the local APIC is disabled. LINT[1:0] are only valid when the local APIC is enabled.
9. This specification only applies when the APIC is enabled and the LINT1 or LINT0 pin is confiugred as an edge-triggered interrupt with fixed delivery; otherwise, specification T14 applies.
10. When driven inactive or after Vcc_{CORE}, and BCLK become stable.
11. If the BCLK signal meets its AC specification within 150 ns of turning on, then the PWRGOOD inactive pulse width spcification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL,max}$ until all the vlotage planes meet the voltage tolerance specificaions.

    PWRGOOD must remain below $V_{IL,max}$ (Table 7) until all the voltage planesmeet the voltage tolerance specifications in Table 6 and BCLK has met the BCLK AC specifications in Table 11 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5 V.

Table 17. Intel® Celeron™ Processor System Bus AC Specifications (Reset Conditions) [1]

T# Parameter	Min	Max	Unit	Figure	Notes
T16: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time	4		BCLKs	9	Before deassertion of RESET#
T17: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time	2	20	BCLKs	9	After clock that deasserts RESET#
T18: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Setup Time	1		ms	9	Before deassertion of RESET#
T19: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Delay Time		5	BCLKs	9	After assertion of RESET# [2]
T20: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Hold Time	2	20	BCLKs	9 10	After clock that deasserts RESET#

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. For a Reset, the clock ratio defined by these signals must be a safe value (their final or a lower multiplier) within this delay unless PWRGOOD is being driven inactive.

Table 18. Intel® Celeron™ Processor System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Edge Fingers [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T21': PICCLK Frequency	2.0	33.3	MHz		
T22': PICCLK Period	30.0	500.0	ns	6	
T23': PICCLK High Time	12.0		ns	6	
T24': PICCLK Low Time	12.0		ns	6	
T25': PICCLK Rise Time	0.25	3.0	ns	6	
T26': PICCLK Fall Time	0.25	3.0	ns	6	
T27': PICD[1:0] Setup Time	8.5		ns	8	5
T28': PICD[1:0] Hold Time	3.0		ns	8	5
T29': PICD[1:0] Valid Delay	3.0	12.0	ns	7	5, 6, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 0.7 V at the processor edge fingers. All APIC I/O signal timings are referenced at 1.25 V at the processor edge fingers.
4. This specification applies to Intel Celeron processors operating with a 66-MHz Intel Celeron processor system bus only.
5. Referenced to PICCLK rising edge.
6. For open drain signals, valid delay is synonymous with float delay.
7. Valid delay timings for these signals are specified to 2.5 V +5%. See Table 3 for recommended pull-up resistor values.

Table 19. Intel® Celeron™ Processor System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Core Pins [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T21: PICCLK Frequency	2.0	33.3	MHz		
T22: PICCLK Period	30.0	500.0	ns	6	
T23: PICCLK High Time	12.0		ns	6	
T24: PICCLK Low Time	12.0		ns	6	
T25: PICCLK Rise Time	0.25	3.0	ns	6	
T26: PICCLK Fall Time	0.25	3.0	ns	6	
T27: PICD[1:0] Setup Time	8.0		ns	8	5
T28: PICD[1:0] Hold Time	2.5		ns	8	5
T29: PICD[1:0] Valid Delay	1.5	10.0	ns	7	5, 6, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 1.25 V at the processor core pins. All APIC I/O signal timings are referenced at 1.25 V at the processor core pins.
4. This specification applies to Intel Celeron processors operating with a 66-MHz Intel Celeron processor system bus only.
5. Referenced to PICCLK rising edge.
6. For open drain signals, valid delay is synonymous with float delay.
7. Valid delay timings for these signals are specified to 2.5 V +5%. See Table 3 for recommended pull-up resistor values.

Table 20. Intel® Celeron™ Processor System Bus AC Specifications (TAP Connection) at the Processor Edge Fingers [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T30': TCK Frequency		16.667	MHz		
T31': TCK Period	60.0		ns	6	
T32': TCK High Time	25.0		ns	6	@1.7 V
T33': TCK Low Time	25.0		ns	6	@0.7 V
T34': TCK Rise Time		5.0	ns	6	(0.7 V–1.7 V) [4]
T35': TCK Fall Time		5.0	ns	6	(1.7 V–0.7 V) [4]
T36': TRST# Pulse Width	40.0		ns	12	Asynchronous
T37': TDI, TMS Setup Time	5.5		ns	11	5
T38': TDI, TMS Hold Time	14.5		ns	11	5
T39': TDO Valid Delay	2.0	13.5	ns	11	6, 7
T40': TDO Float Delay		28.5	ns	11	6, 7
T41': All Non-Test Outputs Valid Delay	2.0	27.5	ns	11	6, 8, 9
T42': All Non-Test Inputs Setup Time		27.5	ns	11	6, 8, 9
T43': All Non-Test Inputs Setup Time	5.5		ns	11	5, 8, 9
T44': All Non-Test Inputs Hold Time	14.5		ns	11	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 0.70 V at the processor edge fingers. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor edge fingers.
3. Not 100% tested. Specified by design characterization.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%. See Table 3 for pull-up resistor values.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.

Table 21. Intel® Celeron™ Processor System Bus AC Specifications (TAP Connection) at the Processor Core Pins [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T30: TCK Frequency		16.667	MHz		
T31: TCK Period	60.0		ns	6	
T32: TCK High Time	25.0		ns	6	@1.7 V [10]
T33: TCK Low Time	25.0		ns	6	@0.7 V [10]
T34: TCK Rise Time		5.0	ns	6	(0.7 V–1.7 V) [4, 10]
T35: TCK Fall Time		5.0	ns	6	(1.7 V–0.7 V) [4, 10]
T36: TRST# Pulse Width	40.0		ns	12	Asynchronous [10]
T37: TDI, TMS Setup Time	5.0		ns	11	5
T38: TDI, TMS Hold Time	14.0		ns	11	5
T39: TDO Valid Delay	1.0	10.0	ns	11	6, 7
T40: TDO Float Delay		25.0	ns	11	6, 7, 10
T41: All Non-Test Outputs Valid Delay	2.0	25.0	ns	11	6, 8, 9
T42: All Non-Test Inputs Setup Time		25.0	ns	11	6, 8, 9, 10
T43: All Non-Test Inputs Setup Time	5.0		ns	11	5, 8, 9
T44: All Non-Test Inputs Hold Time	13.0		ns	11	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 1.25 V at the processor core pins. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor core pins.
3. These specifications are tested during manufacturing, unless otherwise noted.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%. See Table 3 for pull-up resistor values.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.
10. Not 100% tested. Specified by design characterization.

Note: For Figure 6 through Figure 12, the following apply:

1. Figure 6 through Figure 12 are to be used in conjunction with Table 10 through Table 21.
2. All AC timings for the GTL+ signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All GTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the GTL+ signals at the processor core pins are referenced to the BCLK rising edge at 1.25 V. All GTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
4. All AC timings for the CMOS signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
5. All AC timings for the APIC I/O signals at the processor edge fingers are referenced to the PICCLK rising edge at 0.7 V. All APIC I/O signal timings are referenced at 1.25 V at the processor edge fingers.
6. All AC timings for the TAP signals at the processor edge fingers are referenced to the TCK rising edge at 0.70 V. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor edge fingers.

Figure 5. BCLK to Core Logic Offset

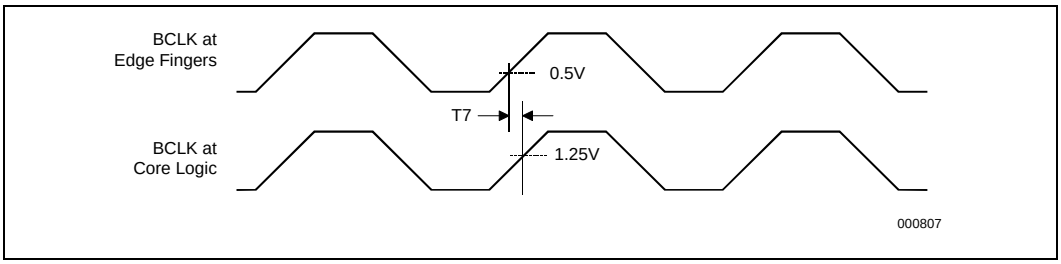


Figure 6. BCLK*, PICCLK, and TCK Generic Clock Waveform

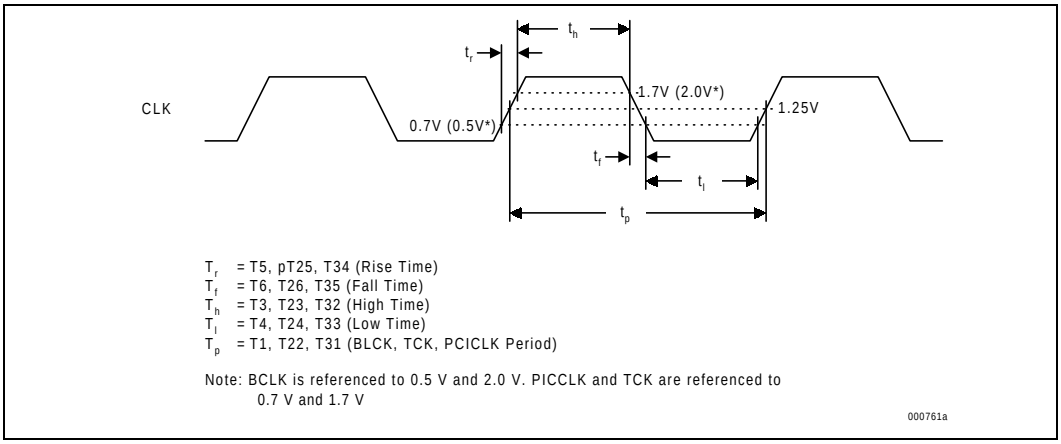
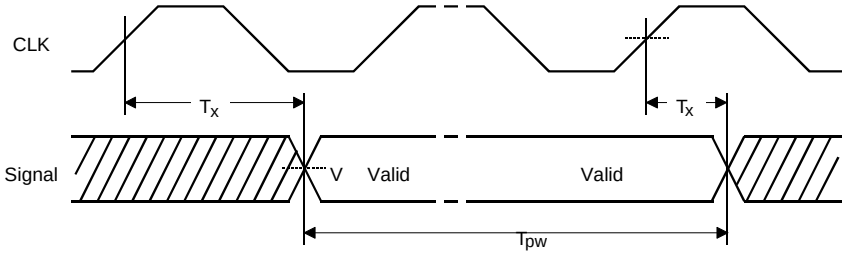


Figure 7. Intel® Celeron™ Processor System Bus Valid Delay Timings



T_x = T7, T11, T29 (Valid Delay)

T_{pw} = T14, T15 (Pulse Wdith)

V = 1.0V for GTL+ signal group; 1.25V for CMOS, APIC and JTAG signal groups

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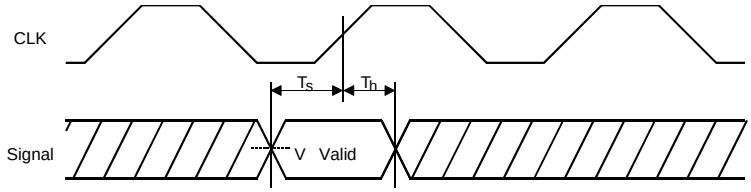
Figure 8. Intel® Celeron™ Processor System Bus Setup and Hold Timings



T_S = T8, T12, T27 (Setup Time)

T_h = T9, T13, T28 (Hold Time)

V = 1.0V for GTL+ signal group; 1.25V for CMOS, APIC and JTAG signal groups

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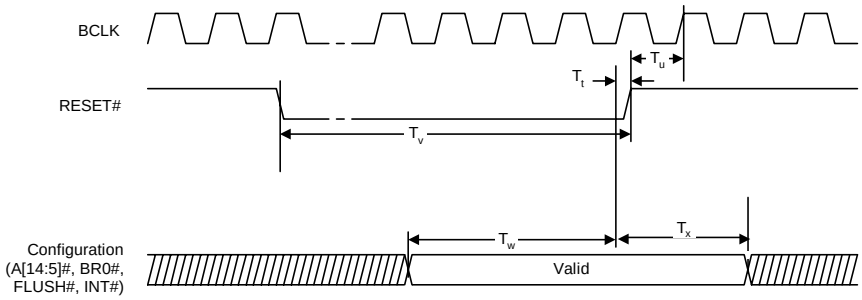
Figure 9. Intel® Celeron™ Processor System Bus Reset and Configuration Timings



T_t = T9 (GTL+ Input Hold Time)
T_u = T8 (GTL+ Input Setup Time)
T_v = T10 (RESET# Pulse Width)
T_w = T16 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup
T_x = T17 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold

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Figure 10. Power-On Reset and Configuration Timings

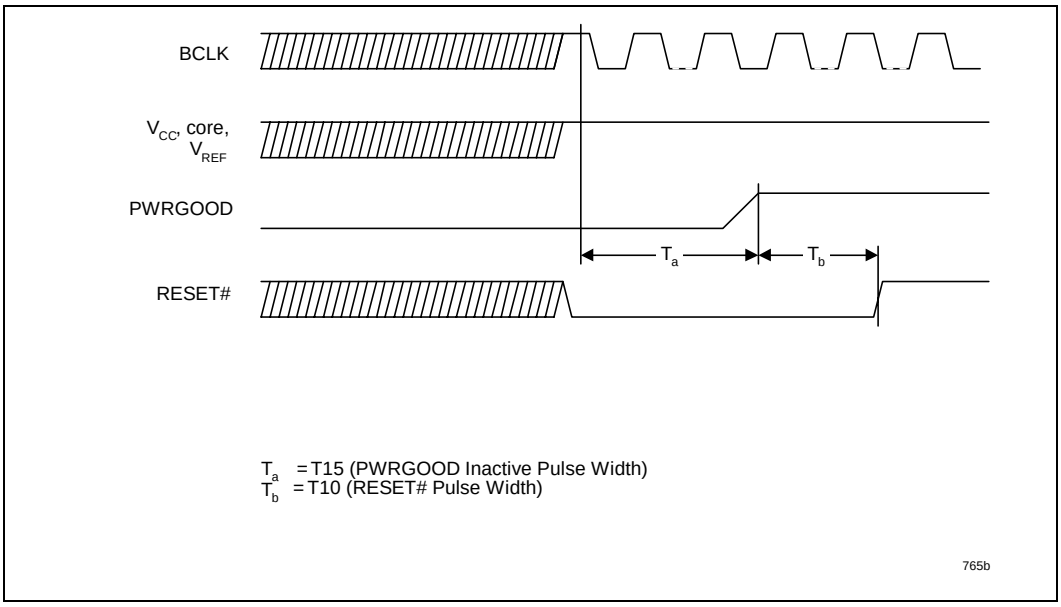


Figure 11. Test Timings (TAP Connection)

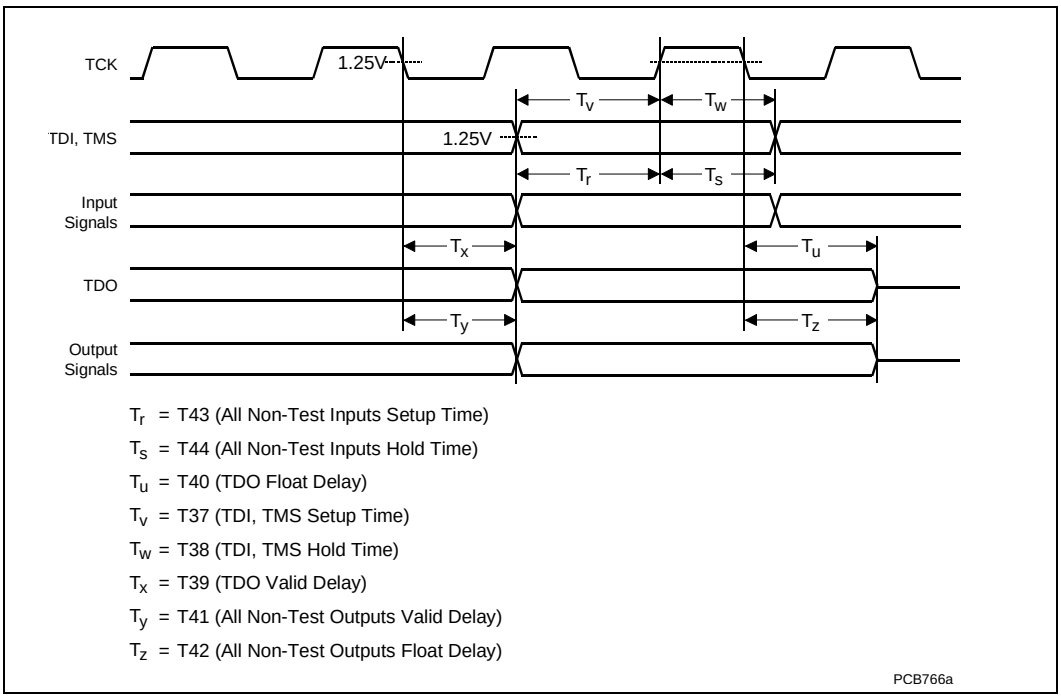
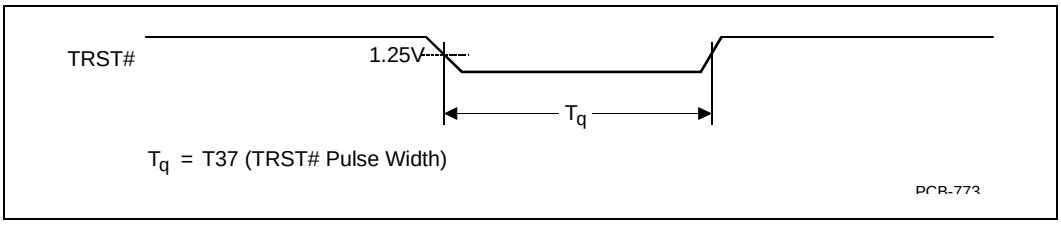


Figure 12. Test Reset Timings



3.0 System Bus Signal Simulations

Signals driven on the Intel® Celeron processor system bus should meet signal quality specifications to ensure that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. Specifications are provided for simulation at the processor core; guidelines are provided for correlation to the processor edge fingers. These edge finger guidelines are intended for use during testing and measurement of system signal integrity. Violations of these guidelines are permitted, but if they occur, simulation of signal quality at the processor core should be performed to ensure that no violations of signal quality specifications occur. Meeting the specifications at the processor core in Table 22, Table 24, and Table 26 ensures that signal quality effects will not adversely affect processor operation, but does not necessarily guarantee that the guidelines in Table 23, Table 25, and Table 27 will be met.

3.1 Intel® Celeron™ Processor System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines

Table 22 describes the signal quality specifications at the processor core for the Intel® Celeron processor system bus clock (BCLK) signal. Table 23 describes guidelines for signal quality measurement at the processor edge fingers. Figure 13 describes the signal quality waveform for the system bus clock at the processor core pins; Figure 14 describes the signal quality waveform for the system bus clock at the processor edge fingers.

Table 22. BCLK Signal Quality Specifications for Simulation at the Processor Core [1]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1: BCLK V_{IL}			0.5	V	14	
V2: BCLK V_{IH}	2.0			V	14	2
V3: V_{IN} Absolute Voltage Range	–0.7		3.5	V	14	2
V4: Rising Edge Ringback	1.7			V	14	3
V5: Falling Edge Ringback			0.7	V	14	3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. This is the Intel Celeron processor system bus clock overshoot and undershoot specification for 66-MHz system bus operation.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 13. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Core Pins

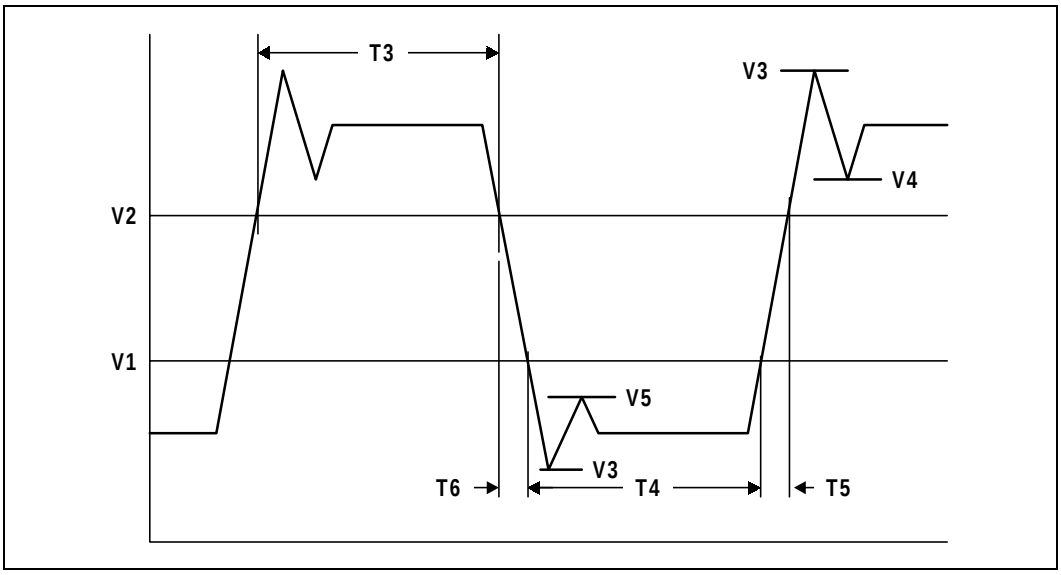
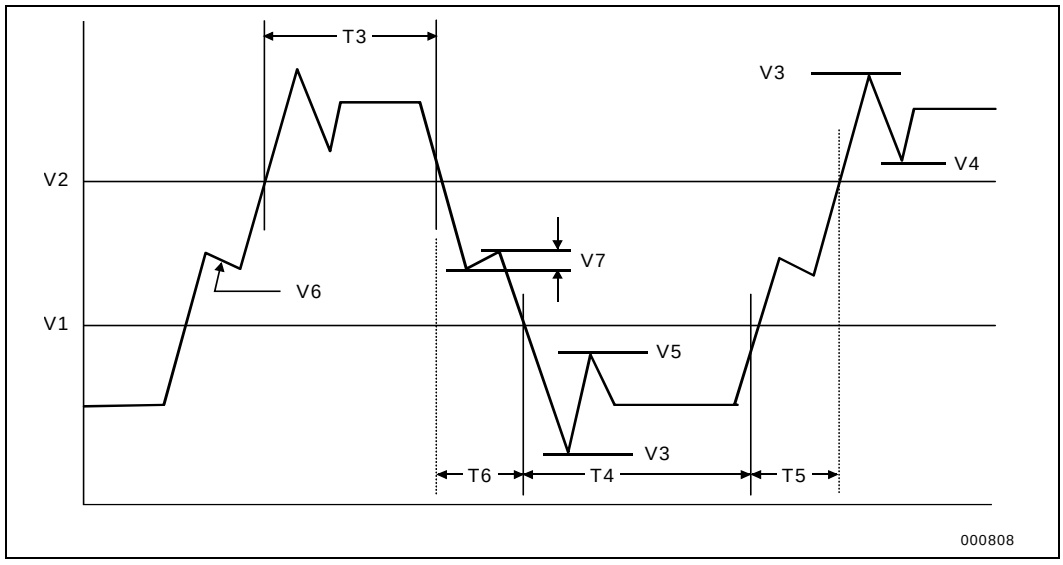


Table 23. BCLK Signal Quality Guidelines for Edge Finger Measurement [1]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1': BCLK V_{IL}			0.5	V	14	
V2': BCLK V_{IH}	2.0			V	14	
V3': V_{IN} Absolute Voltage Range	–0.5		3.3	V	14	2
V4': Rising Edge Ringback	2.0			V	14	3
V5': Falling Edge Ringback			0.5	V	14	3
V6': T_{line} Ledge Voltage	1.0		1.7	V	14	At Ledge Midpoint [4]
V7': T_{line} Ledge Oscillation			0.2	V	14	Peak-to-Peak [5]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel Celeron™ processor frequencies.
2. This is the Intel Celeron processor system bus clock overshoot and undershoot measurement guideline.
3. The rising and falling edge ringback voltage guideline is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal may dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This guideline is an absolute value.
4. The BCLK at the processor edge fingers may have a dip or ledge midway on the rising or falling edge. The midpoint voltage level of this ledge should be within the range of the guideline.
5. The ledge (V7) is allowed to have peak-to-peak oscillation as given in the guideline.

Figure 14. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Edge Fingers



3.2 GTL+ Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of GTL+ layout guidelines which are available in AP-585, *Pentium® II Processor GTL+ Guidelines* (Order Number 243330). Refer to the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the GTL+ buffer specification.

Table 24 provides the GTL+ signal quality specifications for Intel Celeron processors for use in simulating signal quality at the processor core. Table 25 provides GTL+ signal quality guidelines for measuring and testing signal quality at the processor edge fingers. Figure 15 describes the signal quality waveform for GTL+ signals at the processor core and edge fingers. For more information on the GTL+ interface, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

Table 24. GTL+ Signal Groups Ringback Tolerance Specifications at the Processor Core [1, 2, 3]

T# Parameter	Min	Unit	Figure	Notes
α: Overshoot	100	mV	15	4
τ: Minimum Time at High	1.00	ns	15	4
ρ: Amplitude of Ringback	–100	mV	15	4, 5
ϕ: Final Settling Voltage	100	mV	15	4
δ: Duration of Squarewave Ringback	N/A	ns	15	

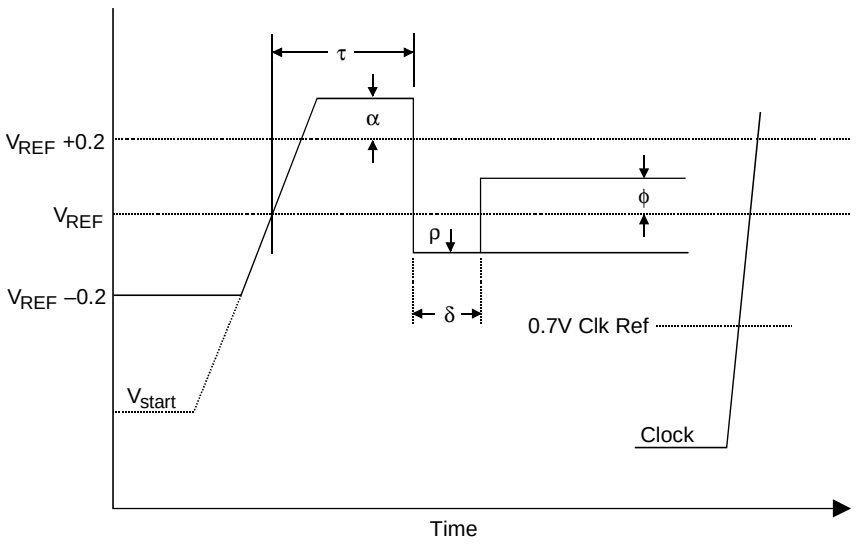
NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel Celeron™ processor frequencies.
2. Specifications are for the edge rate of 0.3 - 0.8 V/ns. See Figure 15 for the generic waveform.
3. All values specified by design characterization.
4. This specification applies to Intel Celeron processors operating with a 66-MHz Intel Celeron processor system bus only.
5. Ringback below V_{REF} + 20 mV is not supported.

Table 25. GTL+ Signal Groups Ringback Tolerance Guidelines for Edge Finger Measurement [1, 2, 3]

T# Parameter	Min	Unit	Figure	Notes
α': Overshoot	100	mV	15	
τ': Minimum Time at High	1.5	ns	15	4
ρ': Amplitude of Ringback	–250	mV	15	4, 5
ϕ': Final Settling Voltage	250	mV	15	4
δ': Duration of Squarewave Ringback	N/A	ns	15	

NOTES:
1. Unless otherwise noted, all guidelines in this table apply to all Intel Celeron™ processor frequencies.
2. Guidelines are for the edge rate of 0.3 - 0.8 V/ns. See Figure 15 for the generic waveform.
3. All values specified by design characterization.
4. This guideline applies to Intel Celeron processors operating with a 66-MHz system bus only.
5. Ringback below V_{REF} + 250 mV is not supported.

Figure 15. Low to High GTL+ Receiver Ringback Tolerance



Note: High to Low case is analogous.

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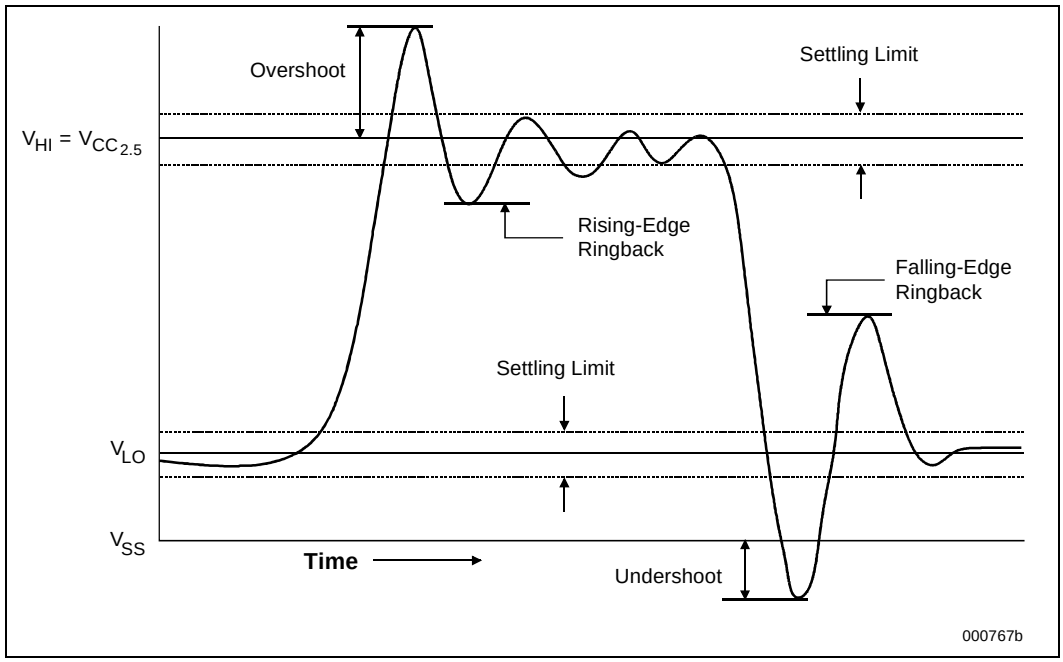
3.3 Non-GTL+ Signal Quality Specifications and Measurement Guidelines

There are three signal quality parameters defined for non-GTL+ signals: overshoot/undershoot, ringback, and settling limit. All three signal quality parameters are shown in Figure 16 for the non-GTL+ signal group.

Figure 16. Non-GTL+ Overshoot/Undershoot, Settling Limit, and Ringback



3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below V_{SS}. The overshoot/undershoot guideline limits transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. (See Figure 16 for non-GTL+ signals.) The processor can be damaged by repeated overshoot events on 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). However, excessive ringback is the dominant detrimental system timing effect resulting from overshoot/undershoot (i.e., violating the overshoot/undershoot guideline will make satisfying the ringback specification difficult). **The overshoot/undershoot guideline is 0.7 V** and assumes the absence of diodes on the input. These guidelines should be verified in simulations **without the on-chip ESD protection diodes present** because the diodes will begin clamping the 2.5 V tolerant signals beginning at approximately 0.7 V above the 2.5 V supply and 0.7 V below V_{SS}. If signals are not reaching the clamping voltage, this will not be an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

3.3.2 Ringback Specification

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is **the voltage that the signal rings back to after achieving its maximum absolute value**. (See Figure 16 for an illustration of ringback.) Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal ringback specification are not allowed under any circumstances for non-GTL+ signals.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table 26 for the signal ringback specifications for non-GTL+ signals for simulations at the processor core, and Table 27 for guidelines on measuring ringback at the edge fingers.

Table 26. Signal Ringback Specifications for Non-GTL+ Signal Simulation at the Processor Core [1]

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
Non-GTL+ Signals	0 → 1	1.7	V	16	
Non-GTL+ Signals	1 → 0	0.7	V	16	

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all Intel Celeron™ processor frequencies.

Table 27. Signal Ringback Guidelines for Non-GTL+ Signal Edge Finger Measurement [1]

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
Non-GTL+ Signals	0 → 1	2.0	V	16	
Non-GTL+ Signals	1 → 0	0.7	V	16	

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.

3.3.3 Settling Limit Guideline

Settling limit defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. The amount allowed is 10 percent of the total signal swing ($V_{HI} - V_{LO}$) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before it transitions again.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

4.0 Thermal Specifications and Design Considerations

The Intel® Celeron processor does not use a thermal plate. The heatsink for this processor is attached directly to the processor's heatslug.

4.1 Thermal Specifications

Table 28 provides the thermal design power dissipation for Intel Celeron processors. The processor core dissipates the majority of the thermal power. Systems should design for the highest possible thermal power, even if a processor with a lower thermal dissipation is planned. The processor's heatslug is the attach location for all thermal solutions. The maximum and minimum case temperatures are specified in Table 28. A thermal solution should be designed to ensure the temperature of the case never exceeds these specifications.

The processor power is a result of heat dissipated through the case. The overall system chassis thermal design must comprehend the entire processor power.

Table 28. Intel® Celeron™ Processor Thermal Design Power [1]

Processor Core Frequency (MHz)	L2 Cache Size (Kbytes)	Processor Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)
266	0	16.59	5	85
300	0	18.48	5	85
300A	128	19.05	0	85
333	128	20.94	0	85

NOTE:
1. These values are specified at nominal Vcc_{CORE} for the processor core.

4.1.1 Thermal Diode

The Intel Celeron Processor incorporates an on-die diode that can be used to monitor the die temperature. A thermal sensor located on the motherboard may monitor the die temperature of the Intel Celeron processor for thermal management purposes. Table 29 and Table 30 provide the diode parameter and interface specifications.

Table 29. Thermal Diode Parameters[4]

Symbol	Min	Typ	Max	Unit	Notes
$I_{forward\ bias}$	5		500	uA	1
n_ideality	1.0000	1.0065	1.0173		2,3

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. At room temperature with a forward bias of 630 mV.
3. n_ideality is the diode ideality factor parameter, as represented by the diode equation: I-Io(e (Vd*q)/(nkT) - 1).
4. Not 100% tested. Specified by design characterization.

Table 30. Thermal Diode Interface

Pin Name	SC 242 Connector Signal #	Pin Description
THERMDP	B14	diode anode (p junction)
THERMDN	B15	diode cathode (n junction)

4.2 Thermal Parameters

This section defines the terms used for Intel Celeron processor S.E.P. Package thermal analysis.

4.2.1 Ambient Temperature

Ambient temperature, TA, is the temperature of the ambient air surrounding the package. The design recommendation of TA is 45 °C. In a system environment, ambient temperature is the temperature of the air upstream from the package and in its close vicinity; or in an active cooling system, it is the inlet air to the active cooling device.

4.2.2 Thermal Resistance

The thermal resistance value for the case to ambient, Θ_{CA} is used as a measure of the cooling solution's performance. Θ_{CA} is comprised of the case to sink thermal, Θ_{CS} and the sink to ambient thermal resistance, Θ_{SA}. Θ_{CS} is a measure of the thermal resistance along the heat flow path from the top of the heatslug to the bottom of the cooling solution. This value is strongly dependent on the material, conductivity, and thickness of the thermal interface used. Θ_{SA} is a measure of the thermal resistance from the top of the cooling solution to the local ambient air. Θ_{SA} values depend on the material, thermal conductivity, and geometry of the thermal cooling solution as well as on the airflow rates.

4.2.3 Thermal Solution Performance

All processor thermal solutions should attach to the processor's heatslug.

The thermal solution must adequately control the processor's case temperatures below the maximum and above the minimum specified in Table 28. The performance of any thermal solution is defined as the thermal resistance between the case temperature and the ambient air around the processor (Θ_{CA}). The lower the thermal resistance between the case and the ambient air, the more efficient the thermal solution is. The required Θ_{CA} is dependent upon the maximum allowed case temperature (T_{CASE}), the local ambient temperature (T_{LA}) and the maximum power dissipation of the processor.

$$\Theta_{CA} = (T_{CASE} - T_{LA})/P_D$$

The case temperature and device power is listed in Table 28. T_{LA} is a function of the system design. Table 31 provides an example of the resulting thermal solution performance required for a 266-MHz Intel Celeron processor at different ambient air temperatures around the processor.

Table 31. Example Thermal Solution Performance for 266 MHz Intel® Celeron™ Processor at Power of 16.59 Watts

	Local Ambient Temperature (T_{LA})		
	35 °C	40 °C	45 °C
Θ_{CA} (°C/Watt)	3.01	2.71	2.41

A critical but controllable factor to decrease the value of Θ_{CS} is management of the thermal interface between the case and heatsink. The other controllable factor (Θ_{SA}) is determined by the design of the heatsink and airflow around the heatsink.

4.3 Thermal Solution Attach Methods

It is recommended that the Intel Celeron processor be integrated with an Intel designed heatsink and clip. These components are available from major manufacturers .

5.0 Mechanical Specifications

Intel® Celeron processors use a new cost-reduced package technology called S.E.P. Package (Single-Edge Processor Package). The Intel Celeron processor contains the processor core, and passive components. The Intel Celeron processor connects to the motherboard through an edge connector.

The processor edge connector defined in this document is referred to as the “SC 242 connector.” See the *Slot 1 Connector Specification* (Order Number 243397) for further details on the edge connector.

5.1 Intel® Celeron™ Processor Materials Information

The Intel® Celeron processor requires a retention mechanism. This retention mechanism may require motherboard hole dimensions to be 0.159" diameter holes if low cost plastic fasteners are used to secure the retention mechanisms in place. The larger diameter holes are necessary to provide a robust structural design that can guarantee stringent shock and vibe testing. If captive nuts are used in place of the plastic fasteners, then either the 0.159" or the 0.140" diameter holes will suffice as long as the corresponding sized attached mount is used.

Figure 17 with substrate dimensions is provided to aid in the design of a heatsink and clip. In Figure 18 all area on the secondary side of the substrate is zoned “keep out”, except for 25 mils around the tooling holes and the top and side edges of the substrate.

Figure 17. Intel® Celeron™ Processor Substrate Dimensions

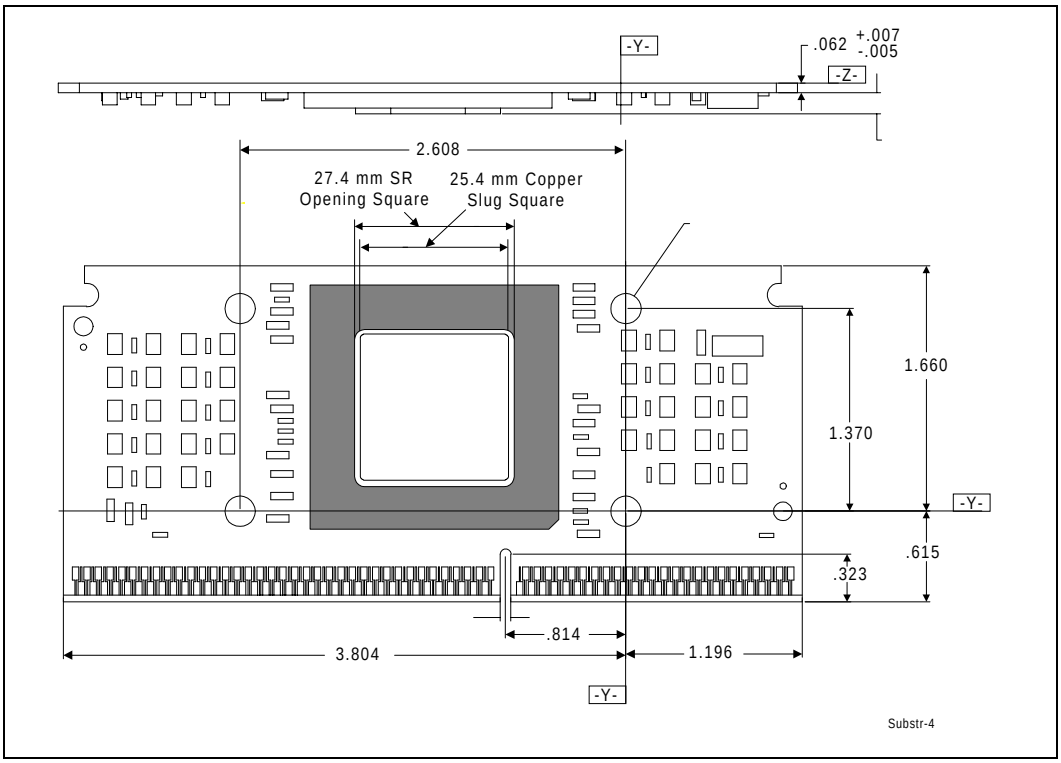
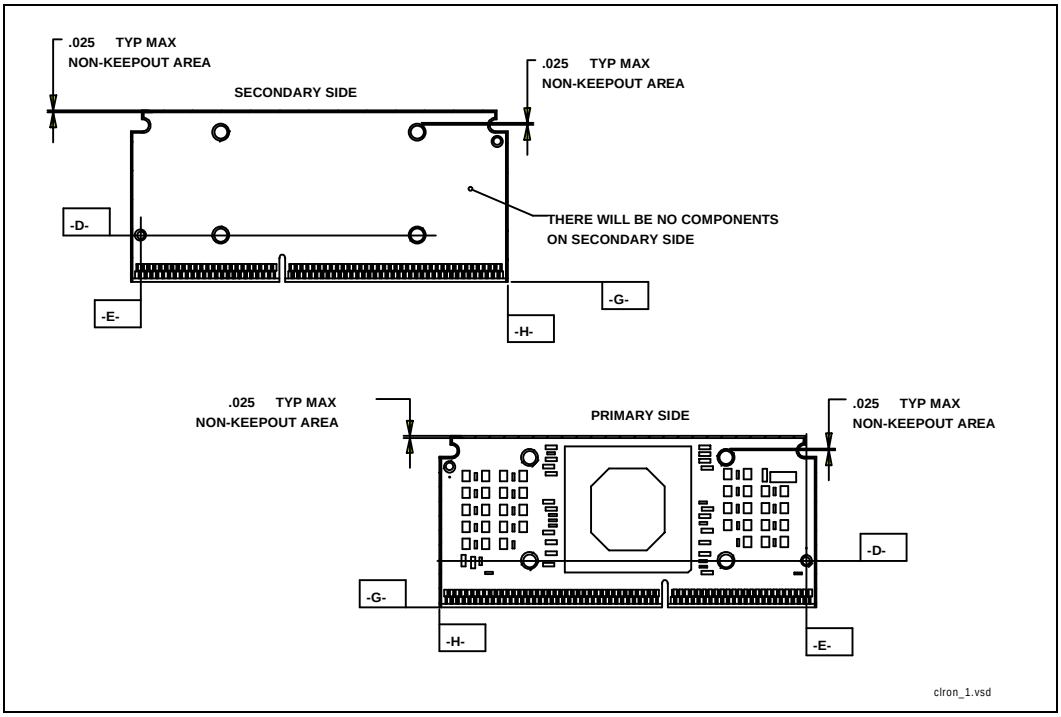


Figure 18. Intel Celeron™ Processor Substrate Primary/Secondary Side Dimensions



5.2 Intel® Celeron™ Processor Signal Listing

Table 32 and Table 33 provide the processor edge finger and SC 242 connector signal definitions for Intel® Celeron processor. The signal locations on the SC 242 edge connector are to be used for signal routing, simulation, and component placement on the motherboard.

Table 32 is the Intel Celeron processor substrate edge finger listing in order by pin number.

Table 32. Signal Listing in Order by Pin Number (Sheet 1 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A1	VCC_VTT	GTL+ VTT Supply	B1	EMI	EMI Management
A2	GND	VSS	B2	FLUSH#	CMOS Input
A3	VCC_VTT	GTL+ VTT Supply	B3	SMI#	CMOS Input
A4	IERR#	CMOS Output	B4	INIT#	CMOS Input
A5	A20M#	CMOS Input	B5	VCC_VTT	GTL+ VTT Supply
A6	GND	VSS	B6	STPCLK#	CMOS Input
A7	FERR#	CMOS Output	B7	TCK	JTAG Input
A8	IGNNE#	CMOS Input	B8	SLP#	CMOS Input
A9	TDI	JTAG Input	B9	VCC_VTT	GTL+ VTT Supply
A10	GND	VSS	B10	TMS	JTAG Input
A11	TDO	JTAG Output	B11	TRST#	JTAG Input
A12	PWRGOOD	CMOS Input	B12	Reserved	Reserved for Future Use
A13	TESTHI	CMOS Test Input	B13	VCC_CORE	Processor core VCC
A14	GND	VSS	B14	THERMDP	Diode Anode (p junction)
A15	THERMTRIP#	CMOS Output	B15	THERMDN	Diode Cathode (n junction)
A16	Reserved	Reserved for Future Use	B16	LINT[1]/NMI	CMOS Input
A17	LINT[0]/INTR	CMOS Input	B17	VCC_CORE	Processor core VCC
A18	GND	VSS	B18	PICCLK	APIC Clock Input
A19	PICD[0]	CMOS I/O	B19	BP#[2]	GTL+ I/O
A20	PREQ#	CMOS Input	B20	Reserved	Reserved for Future Use
A21	BP#[3]	GTL+ I/O	B21	BSEL#	VSS
A22	GND	VSS	B22	PICD[1]	CMOS I/O
A23	BPM#[0]	GTL+ I/O	B23	PRDY#	GTL+ Output
A24	Reserved	Reserved for Pentium II processor	B24	BPM#[1]	GTL+ I/O
A25	Reserved	Reserved for Pentium II processor	B25	VCC_CORE	Processor core VCC
A26	GND	VSS	B26	Reserved	Reserved for Pentium II processor
A27	Reserved	Reserved for Pentium II processor	B27	Reserved	Reserved for Pentium II processor
A28	Reserved	Reserved for Pentium II processor	B28	Reserved	Reserved for Pentium II processor
A29	Reserved	Reserved for Pentium II processor	B29	VCC_CORE	Processor core VCC

Table 32. Signal Listing in Order by Pin Number (Sheet 2 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A30	GND	Vss	B30	D#[62]	GTL+ I/O
A31	Reserved	Reserved for Pentium II processor	B31	D#[58]	GTL+ I/O
A32	D#[61]	GTL+ I/O	B32	D#[63]	GTL+ I/O
A33	D#[55]	GTL+ I/O	B33	VCC_CORE	Processor core Vcc
A34	GND	Vss	B34	D#[56]	GTL+ I/O
A35	D#[60]	GTL+ I/O	B35	D#[50]	GTL+ I/O
A36	D#[53]	GTL+ I/O	B36	D#[54]	GTL+ I/O
A37	D#[57]	GTL+ I/O	B37	VCC_CORE	Processor core Vcc
A38	GND	Vss	B38	D#[59]	GTL+ I/O
A39	D#[46]	GTL+ I/O	B39	D#[48]	GTL+ I/O
A40	D#[49]	GTL+ I/O	B40	D#[52]	GTL+ I/O
A41	D#[51]	GTL+ I/O	B41	EMI	EMI Management
A42	GND	Vss	B42	D#[41]	GTL+ I/O
A43	D#[42]	GTL+ I/O	B43	D#[47]	GTL+ I/O
A44	D#[45]	GTL+ I/O	B44	D#[44]	GTL+ I/O
A45	D#[39]	GTL+ I/O	B45	VCC_CORE	Processor core Vcc
A46	GND	Vss	B46	D#[36]	GTL+ I/O
A47	Reserved	Reserved for Future Use	B47	D#[40]	GTL+ I/O
A48	D#[43]	GTL+ I/O	B48	D#[34]	GTL+ I/O
A49	D#[37]	GTL+ I/O	B49	VCC_CORE	Processor core Vcc
A50	GND	Vss	B50	D#[38]	GTL+ I/O
A51	D#[33]	GTL+ I/O	B51	D#[32]	GTL+ I/O
A52	D#[35]	GTL+ I/O	B52	D#[28]	GTL+ I/O
A53	D#[31]	GTL+ I/O	B53	VCC_CORE	Processor core Vcc
A54	GND	Vss	B54	D#[29]	GTL+ I/O
A55	D#[30]	GTL+ I/O	B55	D#[26]	GTL+ I/O
A56	D#[27]	GTL+ I/O	B56	D#[25]	GTL+ I/O
A57	D#[24]	GTL+ I/O	B57	VCC_CORE	Processor core Vcc
A58	GND	Vss	B58	D#[22]	GTL+ I/O
A59	D#[23]	GTL+ I/O	B59	D#[19]	GTL+ I/O
A60	D#[21]	GTL+ I/O	B60	D#[18]	GTL+ I/O
A61	D#[16]	GTL+ I/O	B61	EMI	EMI Management
A62	GND	Vss	B62	D#[20]	GTL+ I/O
A63	D#[13]	GTL+ I/O	B63	D#[17]	GTL+ I/O
A64	D#[11]	GTL+ I/O	B64	D#[15]	GTL+ I/O
A65	D#[10]	GTL+ I/O	B65	VCC_CORE	Processor core Vcc
A66	GND	Vss	B66	D#[12]	GTL+ I/O
A67	D#[14]	GTL+ I/O	B67	D#[7]	GTL+ I/O
A68	D#[9]	GTL+ I/O	B68	D#[6]	GTL+ I/O

Table 32. Signal Listing in Order by Pin Number (Sheet 3 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A69	D#[8]	GTL+ I/O	B69	VCC_CORE	Processor core VCC
A70	GND	VSS	B70	D#[4]	GTL+ I/O
A71	D#[5]	GTL+ I/O	B71	D#[2]	GTL+ I/O
A72	D#[3]	GTL+ I/O	B72	D#[0]	GTL+ I/O
A73	D#[1]	GTL+ I/O	B73	VCC_CORE	Processor core VCC
A74	GND	VSS	B74	RESET#	GTL+ Input
A75	BCLK	Processor Clock Input	B75	Reserved	Reserved for future use
A76	Reserved	Reserved for Pentium II processor	B76	Reserved	Reserved for future use
A77	BERR#	GTL+ I/O	B77	VCC_CORE	Processor core VCC
A78	GND	VSS	B78	Reserved	Reserved for Pentium II processor
A79	Reserved	Reserved for Pentium II processor	B79	Reserved	Reserved for Pentium II processor
A80	Reserved	Reserved for Pentium II processor	B80	A#[29]	GTL+ I/O
A81	A#[30]	GTL+ I/O	B81	EMI	EMI Management
A82	GND	VSS	B82	A#[26]	GTL+ I/O
A83	A#[31]	GTL+ I/O	B83	A#[24]	GTL+ I/O
A84	A#[27]	GTL+ I/O	B84	A#[28]	GTL+ I/O
A85	A#[22]	GTL+ I/O	B85	VCC_CORE	Processor core VCC
A86	GND	VSS	B86	A#[20]	GTL+ I/O
A87	A#[23]	GTL+ I/O	B87	A#[21]	GTL+ I/O
A88	Reserved	Reserved for Future Use	B88	A#[25]	GTL+ I/O
A89	A#[19]	GTL+ I/O	B89	VCC_CORE	Processor core VCC
A90	GND	VSS	B90	A#[15]	GTL+ I/O
A91	A#[18]	GTL+ I/O	B91	A#[17]	GTL+ I/O
A92	A#[16]	GTL+ I/O	B92	A#[11]	GTL+ I/O
A93	A#[13]	GTL+ I/O	B93	VCC_CORE	Processor core VCC
A94	GND	VSS	B94	A#[12]	GTL+ I/O
A95	A#[14]	GTL+ I/O	B95	A#[8]	GTL+ I/O
A96	A#[10]	GTL+ I/O	B96	A#[7]	GTL+ I/O
A97	A#[5]	GTL+ I/O	B97	VCC_CORE	Processor core VCC
A98	GND	VSS	B98	A#[3]	GTL+ I/O
A99	A#[9]	GTL+ I/O	B99	A#[6]	GTL+ I/O
A100	A#[4]	GTL+ I/O	B100	EMI	EMI Management
A101	BNR#	GTL+ I/O	B101	SLOTOCC#	SC 242 Occupied
A102	GND	VSS	B102	REQ#[0]	GTL+ I/O
A103	BPRI#	GTL+ Input	B103	REQ#[1]	GTL+ I/O
A104	TRDY#	GTL+ Input	B104	REQ#[4]	GTL+ I/O
A105	DEFER#	GTL+ Input	B105	VCC_CORE	Processor core VCC

Table 32. Signal Listing in Order by Pin Number (Sheet 4 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A106	GND	VSS	B106	LOCK#	GTL+ I/O
A107	REQ#[2]	GTL+ I/O	B107	DRDY#	GTL+ I/O
A108	REQ#[3]	GTL+ I/O	B108	RS#[0]	GTL+ Input
A109	HITM#	GTL+ I/O	B109	VCC5	Other VCC
A110	GND	VSS	B110	HIT#	GTL+ I/O
A111	DBSY#	GTL+ I/O	B111	RS#[2]	GTL+ Input
A112	RS#[1]	GTL+ Input	B112	Reserved	Reserved for Future Use
A113	Reserved	Reserved for Future Use	B113	Reserved	Reserved for Pentium II processor
A114	GND	VSS	B114	Reserved	Reserved for Pentium II processor
A115	ADS#	GTL+ I/O	B115	Reserved	Reserved for Pentium II processor
A116	Reserved	Reserved for Future Use	B116	Reserved	Reserved for Pentium II processor
A117	Reserved	Reserved for Pentium II processor	B117	Reserved	Reserved for Pentium II processor
A118	GND	VSS	B118	Reserved	Reserved for Pentium II processor
A119	VID[2]	Voltage Identification	B119	VID[3]	Voltage Identification
A120	VID[1]	Voltage Identification	B120	VID[0]	Voltage Identification
A121	VID[4]	Voltage Identification	B121	Reserved	Reserved for Pentium II processor

Table 33 is the Intel Celeron processor substrate edge connector listing in order by signal name.

Table 33. Signal Listing in Order by Signal Name (Sheet 1 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
B98	A#[3]	GTL+ I/O	B19	BP#[2]	GTL+ I/O
A100	A#[4]	GTL+ I/O	A21	BP#[3]	GTL+ I/O
A97	A#[5]	GTL+ I/O	A23	BPM#[0]	GTL+ I/O
B99	A#[6]	GTL+ I/O	B24	BPM#[1]	GTL+ I/O
B96	A#[7]	GTL+ I/O	A103	BPRI#	GTL+ Input
B95	A#[8]	GTL+ I/O	B21	BSEL#	VSS
A99	A#[9]	GTL+ I/O	B72	D#[0]	GTL+ I/O
A96	A#[10]	GTL+ I/O	A73	D#[1]	GTL+ I/O
B92	A#[11]	GTL+ I/O	B71	D#[2]	GTL+ I/O
B94	A#[12]	GTL+ I/O	A72	D#[3]	GTL+ I/O
A93	A#[13]	GTL+ I/O	B70	D#[4]	GTL+ I/O
A95	A#[14]	GTL+ I/O	A71	D#[5]	GTL+ I/O
B90	A#[15]	GTL+ I/O	B68	D#[6]	GTL+ I/O
A92	A#[16]	GTL+ I/O	B67	D#[7]	GTL+ I/O
B91	A#[17]	GTL+ I/O	A69	D#[8]	GTL+ I/O
A91	A#[18]	GTL+ I/O	A68	D#[9]	GTL+ I/O
A89	A#[19]	GTL+ I/O	A65	D#[10]	GTL+ I/O
B86	A#[20]	GTL+ I/O	A64	D#[11]	GTL+ I/O
B87	A#[21]	GTL+ I/O	B66	D#[12]	GTL+ I/O
A85	A#[22]	GTL+ I/O	A63	D#[13]	GTL+ I/O
A87	A#[23]	GTL+ I/O	A67	D#[14]	GTL+ I/O
B83	A#[24]	GTL+ I/O	B64	D#[15]	GTL+ I/O
B88	A#[25]	GTL+ I/O	A61	D#[16]	GTL+ I/O
B82	A#[26]	GTL+ I/O	B63	D#[17]	GTL+ I/O
A84	A#[27]	GTL+ I/O	B60	D#[18]	GTL+ I/O
B84	A#[28]	GTL+ I/O	B59	D#[19]	GTL+ I/O
B80	A#[29]	GTL+ I/O	B62	D#[20]	GTL+ I/O
A81	A#[30]	GTL+ I/O	A60	D#[21]	GTL+ I/O
A83	A#[31]	GTL+ I/O	B58	D#[22]	GTL+ I/O
A5	A20M#	CMOS Input	A59	D#[23]	GTL+ I/O
A115	ADS#	GTL+ I/O	A57	D#[24]	GTL+ I/O
A75	BCLK	Processor Clock Input	B56	D#[25]	GTL+ I/O
A77	BERR#	GTL+ I/O	B55	D#[26]	GTL+ I/O
A101	BNR#	GTL+ I/O	A56	D#[27]	GTL+ I/O

Table 33. Signal Listing in Order by Signal Name (Sheet 2 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
B52	D#[28]	GTL+ I/O	B32	D#[63]	GTL+ I/O
B54	D#[29]	GTL+ I/O	A111	DBSY#	GTL+ I/O
A55	D#[30]	GTL+ I/O	A105	DEFER#	GTL+ Input
A53	D#[31]	GTL+ I/O	B107	DRDY#	GTL+ I/O
B51	D#[32]	GTL+ I/O	B1	EMI	EMI Management
A51	D#[33]	GTL+ I/O	B41	EMI	EMI Management
B48	D#[34]	GTL+ I/O	B61	EMI	EMI Management
A52	D#[35]	GTL+ I/O	B81	EMI	EMI Management
B46	D#[36]	GTL+ I/O	B100	EMI	EMI Management
A49	D#[37]	GTL+ I/O	A7	FERR#	CMOS Output
B50	D#[38]	GTL+ I/O	B2	FLUSH#	CMOS Input
A45	D#[39]	GTL+ I/O	A38	GND	Vss
B47	D#[40]	GTL+ I/O	A42	GND	Vss
B42	D#[41]	GTL+ I/O	A50	GND	Vss
A43	D#[42]	GTL+ I/O	A54	GND	Vss
A48	D#[43]	GTL+ I/O	A58	GND	Vss
B44	D#[44]	GTL+ I/O	A62	GND	Vss
A44	D#[45]	GTL+ I/O	A66	GND	Vss
A39	D#[46]	GTL+ I/O	A70	GND	Vss
B43	D#[47]	GTL+ I/O	A74	GND	Vss
B39	D#[48]	GTL+ I/O	A78	GND	Vss
A40	D#[49]	GTL+ I/O	A82	GND	Vss
B35	D#[50]	GTL+ I/O	A86	GND	Vss
A41	D#[51]	GTL+ I/O	A2	GND	Vss
B40	D#[52]	GTL+ I/O	A6	GND	Vss
A36	D#[53]	GTL+ I/O	A10	GND	Vss
B36	D#[54]	GTL+ I/O	A14	GND	Vss
A33	D#[55]	GTL+ I/O	A18	GND	Vss
B34	D#[56]	GTL+ I/O	A22	GND	Vss
A37	D#[57]	GTL+ I/O	A26	GND	Vss
B31	D#[58]	GTL+ I/O	A30	GND	Vss
B38	D#[59]	GTL+ I/O	A34	GND	Vss
A35	D#[60]	GTL+ I/O	A98	GND	Vss
A32	D#[61]	GTL+ I/O	A102	GND	Vss
B30	D#[62]	GTL+ I/O	A106	GND	Vss

Table 33. Signal Listing in Order by Signal Name (Sheet 3 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A110	GND	Vss	A88	Reserved	Reserved for Future Use
A114	GND	Vss	A116	Reserved	Reserved for Future Use
A118	GND	Vss	B12	Reserved	Reserved for Future Use
A46	GND	Vss	A113	Reserved	Reserved for Future Use
B110	HIT#	GTL+ I/O	B20	Reserved	Reserved for Future Use
A109	HITM#	GTL+ I/O	B76	Reserved	Reserved for Future Use
A4	IERR#	CMOS Output	B112	Reserved	Reserved for Future Use
A8	IGNNE#	CMOS Input	B79	Reserved	Reserved for Pentium II processor
B4	INIT#	CMOS Input	B114	Reserved	Reserved for Pentium II processor
A17	LINT[0]/INTR	CMOS Input	B115	Reserved	Reserved for Pentium II processor
B16	LINT[1]/NMI	CMOS Input	A117	Reserved	Reserved for Pentium II processor
B106	LOCK#	GTL+ I/O	B116	Reserved	Reserved for Pentium II processor
B18	PICCLK	APIC Clock Input	A24	Reserved	Reserved for Pentium II processor
A19	PICD[0]	CMOS I/O	A76	Reserved	Reserved for Pentium II processor
B22	PICD[1]	CMOS I/O	B75	Reserved	Reserved for Future Use
B23	PRDY#	GTL+ Output	A79	Reserved	Reserved for Pentium II processor
A20	PREQ#	CMOS Input	A80	Reserved	Reserved for Pentium II processor
A12	PWRGOOD	CMOS Input	B78	Reserved	Reserved for Pentium II processor
B102	REQ#[0]	GTL+ I/O	B118	Reserved	Reserved for Pentium II processor
B103	REQ#[1]	GTL+ I/O	A25	Reserved	Reserved for Pentium II processor
A107	REQ#[2]	GTL+ I/O	A27	Reserved	Reserved for Pentium II processor
A108	REQ#[3]	GTL+ I/O	B26	Reserved	Reserved for Pentium II processor
B104	REQ#[4]	GTL+ I/O	A28	Reserved	Reserved for Pentium II processor
A16	Reserved	Reserved for Future Use	B27	Reserved	Reserved for Pentium II processor
A47	Reserved	Reserved for Future Use	A29	Reserved	Reserved for Pentium II processor

Table 33. Signal Listing in Order by Signal Name (Sheet 4 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A31	Reserved	Reserved for Pentium II processor	B45	VCC_CORE	Processor core VCC
B28	Reserved	Reserved for Pentium II processor	B49	VCC_CORE	Processor core VCC
B74	RESET#	GTL+ Input	B53	VCC_CORE	Processor core VCC
B108	RS#[0]	GTL+ Input	B57	VCC_CORE	Processor core VCC
A112	RS#[1]	GTL+ Input	B65	VCC_CORE	Processor core VCC
B111	RS#[2]	GTL+ Input	B69	VCC_CORE	Processor core VCC
B101	SLOTOCC#	SC 242 Occupied	B73	VCC_CORE	Processor core VCC
B8	SLP#	CMOS Input	B77	VCC_CORE	Processor core VCC
B3	SMI#	CMOS Input	B85	VCC_CORE	Processor core VCC
B6	STPCLK#	CMOS Input	B89	VCC_CORE	Processor core VCC
B7	TCK	JTAG Input	B93	VCC_CORE	Processor core VCC
A9	TDI	JTAG Input	B97	VCC_CORE	Processor core VCC
A11	TDO	JTAG Output	B105	VCC_CORE	Processor core VCC
A13	TESTHI	CMOS Test Input	B113	VCC_L2	Reserved for Pentium II processor
B14	THERMDP	Diode Anode (p junction)	B117	VCC_L2	Reserved for Pentium II processor
B15	THERMDN	Diode Cathode (n junction)	B121	VCC_L2	Reserved for Pentium II processor
A15	THERMTRIP#	CMOS Output	A1	VCC_VTT	GTL+ VTT Supply
B10	TMS	JTAG Input	A3	VCC_VTT	GTL+ VTT Supply
A104	TRDY#	GTL+ Input	B5	VCC_VTT	GTL+ VTT Supply
B11	TRST#	JTAG Input	B9	VCC_VTT	GTL+ VTT Supply
B13	VCC_CORE	Processor core VCC	B109	VCC5	Other VCC
B17	VCC_CORE	Processor core VCC	B120	VID[0]	Voltage Identification
B25	VCC_CORE	Processor core VCC	A120	VID[1]	Voltage Identification
B29	VCC_CORE	Processor core VCC	A119	VID[2]	Voltage Identification
B33	VCC_CORE	Processor core VCC	B119	VID[3]	Voltage Identification
B37	VCC_CORE	Processor core VCC	A121	VID[4]	Voltage Identification

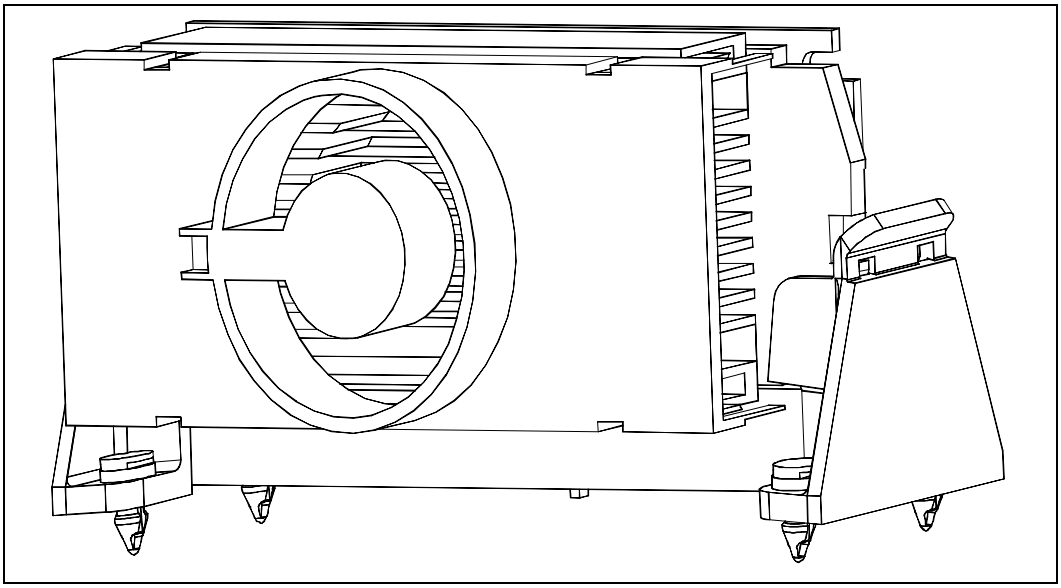
6.0 Boxed Processor Specifications

6.1 Introduction

The Intel® Celeron processor is also offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Intel Celeron processor will be supplied with an attached fan heatsink. This section documents motherboard and system requirements for the fan heatsink that will be supplied with the boxed Intel Celeron processor. This section is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches. Figure 19 shows a mechanical representation of the boxed Intel Celeron processor in a S.E.P. Package retention mechanism, which is not shipped with the boxed Intel Celeron processor.

Note: The airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

Figure 19. Conceptual Boxed Intel® Celeron™ Processor in Retention Mechanism



6.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed Intel Celeron processor fan heatsink.

The boxed processor ships with an attached fan heatsink. Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The space requirements and dimensions for the boxed Processor with integrated fan heatsink are shown in Figure 19, Figure 20, and Figure 21. All dimensions are in inches. Note that these drawings show a conceptual attachement interface to a S.E.P. Package low profile retention mechanism.

Figure 20. Side View Space Requirements for the Boxed Processor

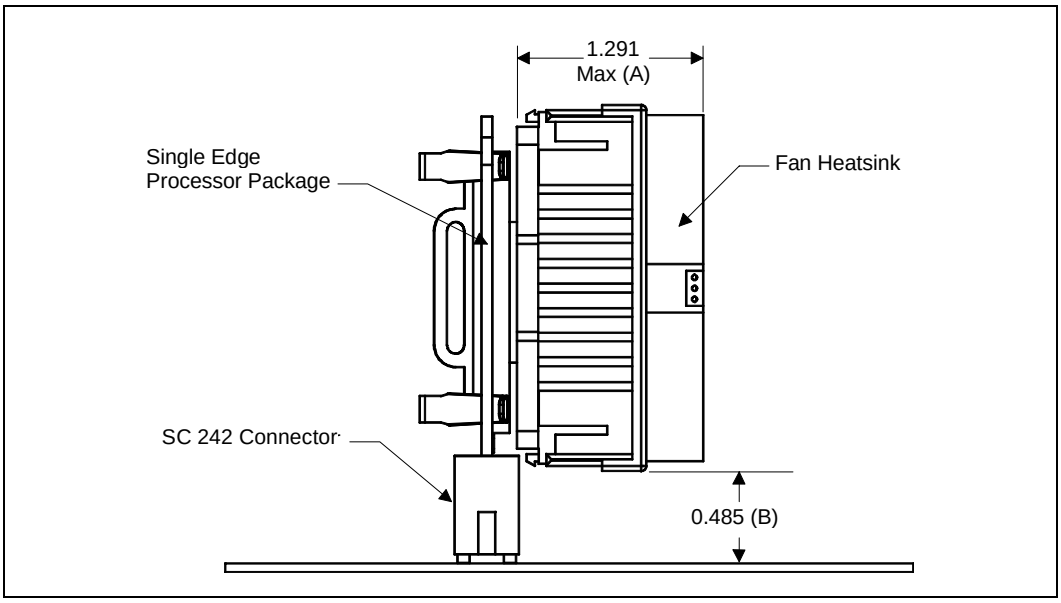


Figure 21. Front View Space Requirements for the Boxed Processor

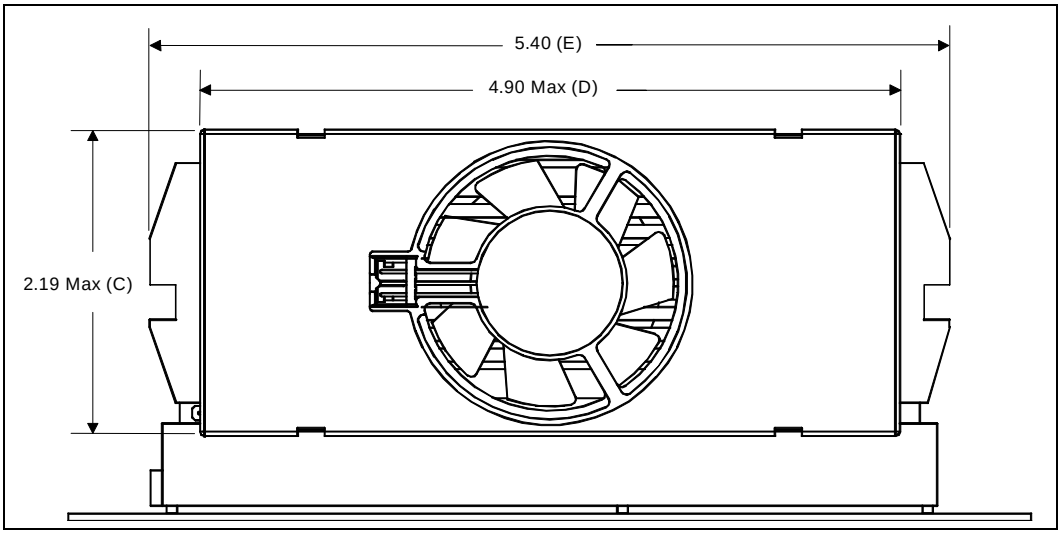
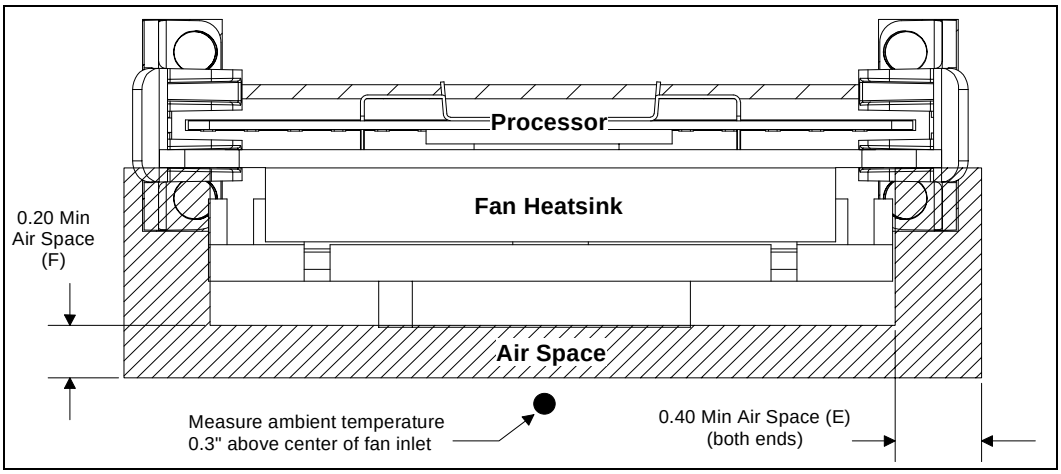


Figure 22. Top View Space Requirements for the Boxed Processor



6.2.1 Boxed Processor Heatsink Dimensions

Table 34. Boxed Processor Fan Heatsink Spatial Dimensions

Fig. Ref. Label	Dimensions (Inches)	Min	Typ	Max
A	Fan Heatsink Depth (off heatsink attach point)			1.291
B	Fan Heatsink Height (above motherboard)		0.485	
C	Fan Heatsink Height (see front view)			2.19
D	Fan Heatsink Width (see front view)			4.90
E	Fan Heatsink Base Width (see front view)		5.40	
F	Airflow keepout zones from end of fan featsink	0.40		
G	Airflow keepout zones from face of fan heatsink	0.20		

6.2.2 Boxed Processor Heatsink Weight

The boxed processor heatsink will not weigh more than 225 grams.

6.2.3 Boxed Processor Retention Mechanism

The boxed Intel Celeron processor requires a S.E.P. Package retention mechanism to secure the processor in the SC 242 connector. A S.E.P. Package retention mechanism will not be provided with the boxed processor. Motherboards designed for use by system integrators should include a retention mechanism and appropriate installation instructions.

The boxed Intel Celeron processor does not require additional fan heatsink supports. Fan heatsink supports will not be shipped with the boxed Intel Celeron processor.

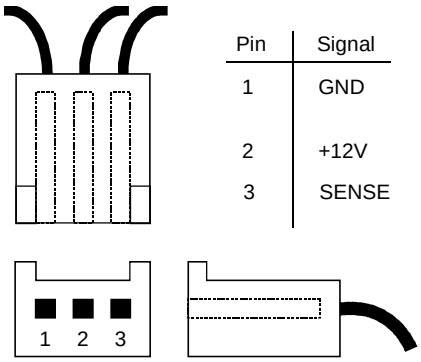
Motherboards designed for flexible use by system integrators must still recognize the boxed Pentium II processor's fan heatsink clearance requirements, which are described in *Pentium® II Processor at 233, 266, 300, and 333 MHz* (Order Number 243335).

6.3 Boxed Processor Requirements

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable is shipped with the boxed processor to draw power from a power header on the motherboard. The power cable connector and pinout are shown in Figure 22. Motherboards must provide a matched power header to support the boxed processor. Table 35 contains specifications for the input and output signals at the fan heatsink connector. The cable length is 7.0 inches (±0.25"). The fan heatsink outputs a SENSE signal, which is an open-collector output, that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides VOH to match the motherboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the motherboard documentation or on the motherboard. Figure 23 shows the recommended location of the fan power connector relative to the SC 242 connector. The motherboard power header should be positioned within 4.75 inches (lateral) of the fan power connector.

Figure 23. Boxed Processor Fan Heatsink Power Cable Connector Description



Pin	Signal	
1	GND	Straight square pin, 3-pin terminal housing with polarizing ribs and friction locking ramp.
2	+12V	0.100" pin pitch, 0.025" square pin width.
3	SENSE	Waldom*/Molex* P/N 22-01-3037 or equivalent.

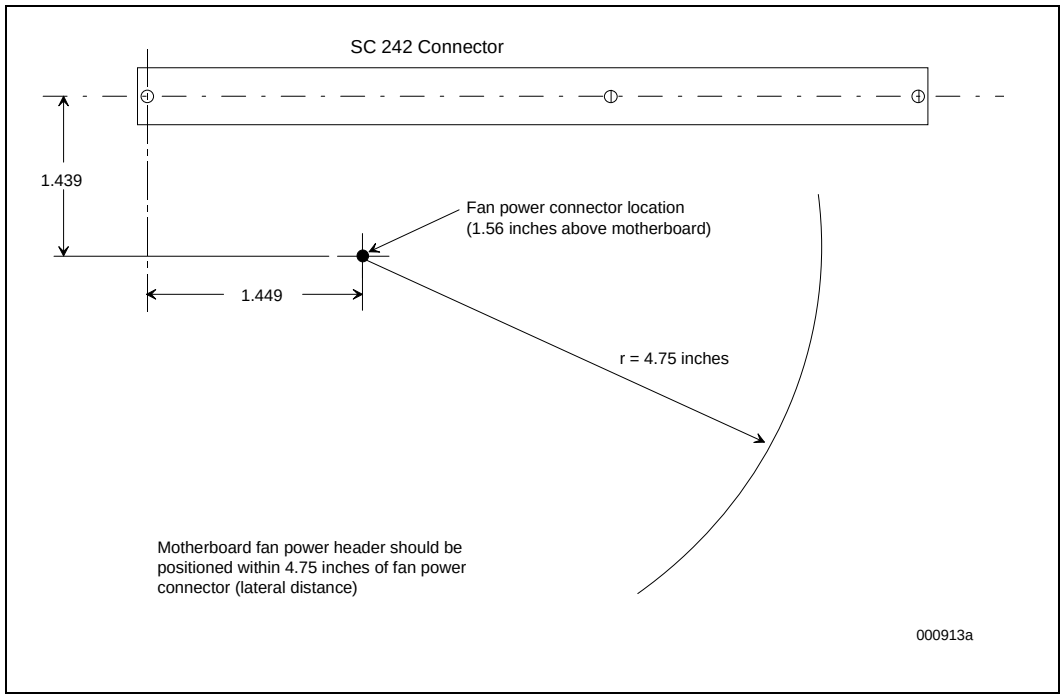
Match with straight pin, friction lock header on motherboard Waldom/Molex P/N 22-23-2031, AMP* P/N 640456-3, or equivalent.

000888

Table 35. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max
+12 V: 12 volt fan power supply	7 V	12 V	13.8 V
IC: Fan current draw			100 mA
SENSE: SENSE frequency (motherboard should pull this pin up to appropriate V_{CC} with resistor)		2 pulses per fan revolution	

Figure 24. Motherboard Power Header Placement Relative to Fan Power Connector and SC 242



6.4 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processor.

6.4.1 Boxed Processor Cooling Requirements

The boxed processor is cooled with a fan heatsink. The boxed processor fan heatsink will keep the processor core case temperature, TCASE, within the specifications (see Table 28), provided airflow through the fan heatsink is unimpeded and the air temperature entering the fan is below 45 °C (see Figure 21 for measurement location).

Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 21 illustrates an acceptable airspace clearance for the fan heatsink.

7.0 Intel® Celeron™ Processor Signal Description

Table 36 provides an alphabetical listing of all Intel® Celeron processor signals. The tables at the end of this section summarize the signals by direction: output, input, and I/O.

Table 36. Alphabetical Signal Reference (Sheet 1 of 7)

Signal	Type	Description
A[31:3]#	I/O	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel® Celeron™ processor system bus. The A[35:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[35:3]# pins to determine their power-on configuration. See the *Pentium® II Processor Developer's Manual* (Order Number 243502) for details.
A20M#	I	If the A20M# (Address-20 Mask) input signal is asserted, the Intel Celeron processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. During active RESET#, each processor begins sampling the A20M#, IGNNE# , and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. On the active-to-inactive transition of RESET#, each processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.
ADS#	I/O	The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[35:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.
BCLK	I	The BCLK (Bus Clock) signal determines the bus frequency. All Intel Celeron processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.
BERR#	I/O	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all Intel Celeron processor system bus agents, and must connect the appropriate pins of all such agents, if used. However, Intel Celeron processors do not observe assertions of the BERR# signal. BERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted optionally for internal errors along with IERR#. • Asserted optionally by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction.

Table 36. Alphabetical Signal Reference (Sheet 2 of 7)

Signal	Type	Description
BNR#	I/O	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all Intel Celeron processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O	The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.
BPRI#	I	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the Intel Celeron processor system bus. It must connect the appropriate pins of all Intel Celeron processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BSEL#	I/O	This bidirectional signal is used to select a host bus frequency of 66 MHz.
D[63:0]#	I/O	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the Intel Celeron processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
DBSY#	I/O	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the Intel Celeron processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.
DEFER#	I	The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.
DRDY#	I/O	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multicycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.
EMI	I	EMI pins should be connected to motherboard ground and/or to chassis ground through zero ohm (0Ω) resistors. The zero ohm resistors should be placed in close proximity to the Intel Celeron connector. The path to chassis ground should be short in length and have a low impedance. These pins are used for EMI management purposes.
FERR#	O	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.

Table 36. Alphabetical Signal Reference (Sheet 3 of 7)

Signal	Type	Description
FLUSH#	I	When the FLUSH# input signal is asserted, the processor writes back all data in the Modified state from the internal cache and invalidates all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, the processor samples FLUSH# to determine its power-on configuration. See *Pentium® Pro Family Developer's Manual, Volume 1: Specifications* (Order Number 242690) for details.
HIT#, HITM#	I/O	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all Intel Celeron processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the Intel Celeron processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. During active RESET#, the Intel Celeron processor begins sampling the A20M#, IGNNE#, and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Table 10. On the active-to-inactive transition of RESET#, the Intel Celeron processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation; see Figure 4 for an example implementation of this logic.
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all Intel Celeron processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).

Table 36. Alphabetical Signal Reference (Sheet 4 of 7)

Signal	Type	Description
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration. During active RESET#, the Intel Celeron processor begins sampling the A20M#, IGNNE#, and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency (See Table 1). On the active-to-inactive transition of RESET#, the Intel Celeron processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation; see Figure 4 for an example implementation of this logic.
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the Intel Celeron processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the Intel Celeron processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of the Intel Celeron processor for proper initialization.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.

Table 36. Alphabetical Signal Reference (Sheet 5 of 7)

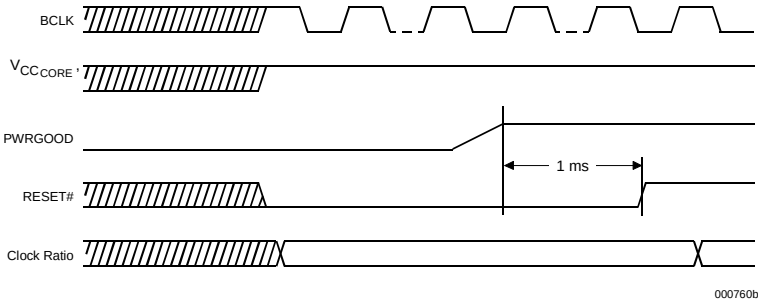
Signal	Type	Description
PWRGOOD	I	The PWRGOOD (Power Good) signal is a 2.5 V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies ($V_{CC_{CORE}}$, etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high (2.5 V) state. Figure 24 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 15 and Table 16, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. **PWRGOOD Relationship at Power-On** 
REQ[4:0]#	I/O	The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all Intel Celeron processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 cache without writing back any of the contents. RESET# must remain active for one microsecond for a “warm” Reset; for a power-on Reset, RESET# must stay active for at least one millisecond after $V_{CC_{CORE}}$ and CLK have reached their proper specifications. On observing active RESET#, all Intel Celeron processor system bus agents will deassert their outputs within two clocks. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the *Pentium® Pro Family Developer's Manual, Volume 1: Specifications* (Order Number 242690). The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all Intel Celeron processor system bus agents.
RS[2:0]#	I	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all Intel Celeron processor system bus agents.

Table 36. Alphabetical Signal Reference (Sheet 6 of 7)

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>SLOTOCC#</td><td>O</td><td>The SLOTOCC# signal is defined to allow a system design to detect the presence of a terminator card or processor in a SC 242 connector. Combined with the VID combination of VID[4:0]= 11111 (see Section 2.6), a system can determine if a SC 242 connector is occupied, and whether a processor core is present. The states and values for determining the type of cartridge in the SC 242 connector is shown below.

SC 242 Occupation Truth Table
<table><tr><th>Signal</th><th>Value</th><th>Status</th></tr><tr><td>SLOTOCC#
VID[4:0]</td><td>0
Anything other than ‘11111’</td><td>Processor with core in SC 242 connector.</td></tr><tr><td>SLOTOCC#
VID[4:0]</td><td>0
11111</td><td>Terminator cartridge in SC 242 connector (i.e., no core present).</td></tr><tr><td>SLOTOCC#
VID[4:0]</td><td>1
Any value</td><td>SC 242 connector not occupied.</td></tr></table></td></tr>
<tr><td>SLP#</td><td>I</td><td>The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.</td></tr>
<tr><td>SMI#</td><td>I</td><td>The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.</td></tr>
<tr><td>STPCLK#</td><td>I</td><td>The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.</td></tr>
<tr><td>TCK</td><td>I</td><td>The TCK (Test Clock) signal provides the clock input for the Intel Celeron processor Test Access Port.</td></tr>
<tr><td>TDI</td><td>I</td><td>The TDI (Test Data In) signal transfers serial test data into the Intel Celeron processor. TDI provides the serial input needed for JTAG specification support.</td></tr>
<tr><td>TDO</td><td>O</td><td>The TDO (Test Data Out) signal transfers serial test data out of the Intel Celeron processor. TDO provides the serial output needed for JTAG specification support.</td></tr>
<tr><td>TESTHI</td><td>I</td><td>The TESTHI signal must be connected to a 2.5 V power source through a 1kΩ –100 kΩ resistor for proper processor operation.</td></tr>
<tr><td>THERMDN</td><td>O</td><td>Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1.</td></tr>
<tr><td>THERMDP</td><td>I</td><td>Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1.</td></tr>
</table>

Table 36. Alphabetical Signal Reference (Sheet 7 of 7)

Signal	Type	Description
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 °C. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP# and remain stopped.
TMS	I	The TMS (Test Mode Select) signal is a JTAG specification support signal used by debug tools.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all Intel Celeron processor system bus agents.
TRST#	I	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. Intel Celeron processors require this signal to be driven low during power on Reset. A 680 ohm resistor is the suggested value for a pull down resistor on TRST#.
VID[4:0]	O	The VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on Intel Celeron processors. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.

7.1 Signal Summaries

Table 37 through Table 40 list attributes of the Intel Celeron processor output, input, and I/O signals.

Table 37. Output Signals

Name	Active Level	Clock	Signal Group
FERR#	Low	Asynch	CMOS Output
IERR#	Low	Asynch	CMOS Output
PRDY#	Low	BCLK	GTL+ Output
SLOTOCC#	Low	Asynch	Power/Other
TDO	High	TCK	JTAG Output
THERMTRIP#	Low	Asynch	CMOS Output
VID[4:0]	High	Asynch	Power/Other

Table 38. Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS Input	Always [1]
BPRI#	Low	BCLK	GTL+ Input	Always
BCLK	High	—	Clock	Always
DEFER#	Low	BCLK	GTL+ Input	Always
FLUSH#	Low	Asynch	CMOS Input	Always [1]
IGNNE#	Low	Asynch	CMOS Input	Always [1]
INIT#	Low	Asynch	CMOS Input	Always [1]
INTR	High	Asynch	CMOS Input	APIC disabled mode
LINT[1:0]	High	Asynch	CMOS Input	APIC enabled mode
NMI	High	Asynch	CMOS Input	APIC disabled mode
PICCLK	High	—	APIC Clock	Always
PREQ#	Low	Asynch	CMOS Input	Always
PWRGOOD	High	Asynch	CMOS Input	Always
RESET#	Low	BCLK	GTL+ Input	Always
RS[2:0]#	Low	BCLK	GTL+ Input	Always
SLP#	Low	Asynch	CMOS Input	During Stop-Grant state
SMI#	Low	Asynch	CMOS Input	
STPCLK#	Low	Asynch	CMOS Input	
TCK	High	—	JTAG Input	
TDI	High	TCK	JTAG Input	
TESTHI	High	Asynch	Power/Other	Always
TMS	High	TCK	JTAG Input	
TRST#	Low	Asynch	JTAG Input	
TRDY#	Low	BCLK	GTL+ Input	

NOTE:
1. Synchronous assertion with active TRDY# ensures synchronization.

Table 39. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
BSEL#	Low	Asynch	Power/Other	Always
A[31:3]#	Low	BCLK	GTL+ I/O	ADS#, ADS#+1
ADS#	Low	BCLK	GTL+ I/O	Always
BPM[1:0]#	Low	BCLK	GTL+ I/O	Always
D[63:0]#	Low	BCLK	GTL+ I/O	DRDY#
DBSY#	Low	BCLK	GTL+ I/O	Always
DRDY#	Low	BCLK	GTL+ I/O	Always
LOCK#	Low	BCLK	GTL+ I/O	Always
REQ[4:0]#	Low	BCLK	GTL+ I/O	ADS#, ADS#+1

Table 40. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
BERR#	Low	BCLK	GTL+ I/O	Always
BNR#	Low	BCLK	GTL+ I/O	Always
HIT#	Low	BCLK	GTL+ I/O	Always
HITM#	Low	BCLK	GTL+ I/O	Always
PICD[1:0]	High	PICCLK	APIC I/O	Always

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