intel® Technical Advisory

TA-0615-1

5200 NE Elam Young Parkway
Hillsboro, OR 97124

December 30, 2002

The SE7500WV2 may experience VBAT, POST 8300 errors or RTC time loss when contact between the CMOS battery and the server board battery holder is not adequate

Products Affected

PBA	TA	MM#	Prod Code
A81418-402	A88237-001	847596	SWV2ATA
A81418-402	A88237-002	847596	SWV2ATA
A81417-402	A88241-001	847597	SWV2SCSI
A81417-402	A88241-002	847597	SWV2SCSI
A81418-403	A88237-003	847596	SWV2ATA
A81417-403	A88241-003	847597	SWV2SCSI
A81418-404	A88237-004	847596	SWV2ATA
A81417-404	A88241-004	847597	SWV2SCSI
A81417-402	A93358-402	847684	BWVSBB
A81417-403	A93358-403	850383	BWVSBB
A81417-404	A93358-404	851849	BWVSBB

Description

Instances of infrequent "VBAT" and "POST 8300" events, and RTC time loss have been observed on the SE7500WV2 server board. The VBAT sensor monitors voltage from the CMOS battery (coin sized battery on the baseboard) and logs an error in the System Event Log (SEL) if the voltage drops below the threshold in the Sensor Data Record (SDR) file. The "POST 8300" error indicates that the Baseboard Management Controller (BMC) has failed its self-test during initialization.

Root Cause

Intel has root caused the failures to poor contact between the CMOS battery and the baseboard battery holder. Intel has determined that poor contact (excessive resistance) between the battery and the baseboard battery holder can result in "VBAT" or "POST 8300" events being logged. In addition, Intel has determined that Real-Time Clock (RTC) time loss can also occur in this situation. The Heceta chip is used by the BMC to monitor various system conditions, including the battery voltage. To monitor the battery voltage, the Heceta chip periodically samples the battery voltage. During this sampling time there is a momentary surge in current being drawn from the battery. If the battery is not properly seated and the resistance between the battery and the baseboard battery holder is very high (>3K Ohm), the battery voltage on the board can momentarily drop low enough to result in a low battery voltage (VBAT) error. During its initialization at POST, the BMC checks the bus to the Heceta for status and response. If the BMC can't fully communicate with the Heceta chip, it will report to the BIOS that it has failed its self-test, resulting in the POST 8300 event being logged in the SEL. In addition, when the battery voltage drops below the normal range, due to the battery seating, the ICH3-S chip can momentarily lose clock cycles, which can cause RTC time loss. Intel has had the CMOS battery holders from failing

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boards analyzed for possible corrosion or manufacturing anomalies or other excursions, and no issues were found. Extensive focused testing has been completed on failing baseboards after reseating the CMOS battery and subsequent failures have not been observed.

Corrective Action / Resolution

Intel is in the process of implementing manufacturing improvements with the addition of an automated test to measure resistance between the battery and the baseboard battery holder to insure that the battery has been properly seated. Intel has identified a design modification that will add additional margin to the affected circuit on the baseboard. This change will be cut in to the factory baseboard builds starting in December 2002. The value of the decoupling capacitor on the battery monitoring circuit will be changed from 0.1uF to 1.0uF, which significantly decreases the susceptibility of the board to poor CMOS battery contact. With this change, the minimum resistance required to induce a failure increases from 3K Ohm to 60K Ohm. This change will reduce the susceptibility of failures if the battery is replaced in the field and not properly reseated. Customers are asked to add a step to their manufacturing process to verify that CMOS batteries are seated corrected in the baseboard battery holder before shipment.

Please contact your Intel Sales Representative if you require more specific information about this issue.

Enterprise Platforms & Services Division
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