N440BX Server Board Specification Update

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The NA440BX and NC440BX DP Server systems may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

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REVISION HISTORY

Date of Revision	Description
June, 1998	This document is the first Specification Update for the NA440BX / NC440BX DP Server system.
July , 1998	Reformatted document. Included reference to Intel Columbus II chassis. Added General Information section. Added errata items
July, 1998	Issue # 3 plans changed to no-fix.
July, 1998	Modified issue # 15 to include resolution.
August, 1998	Modified issue “Speedo IV driver for integrated NIC will not load in Windows 95. Issue status is resolved.
August, 1998	Fixed: Issue #5 The BIOS does not honor PCI disable bit in ESCD.
August, 1998	Fixed: Issue #9 N440BX Server freezes with Windows NT 4.0 display drivers and some hardware RAID cards on the production Country Kit.
September, 1998	Fixed: Issue #22 Version 3.49 of TestView does not contain a VGA or hotswap backplane test package.
October, 1998	NoFix: Issue # 26 Systems may automatically power up if a PCI card is inserted without removing AC power. Not a bug.
November, 1998	NoFix Doc Issue # 9 N440BX Incorrectly calls out Functionality of Diskette Access Security
December, 1998	No Fix: Issue #21 PCI add-in card failure when configured in Slot 4.
January, 1999	No Fix: Issue #21 PCI add-in card wording change about type of PCI add-in card.
February 1999	Issue # 6 When selecting BIOS Boot Order, it is impossible to determine boot drive if models are identical. Due to issues discovered with new bios this fix had to be removed.
March 1999	No changes.
April, 1999	Fixed: Issue # 4
April, 1999	Fixed: Issue # 5
April, 1999	Fix: Issue # 6
April, 1999	NoFix: Normal operation. Issue # 16
April, 1999	Fixed: Issue # 17
April, 1999	NoFix: Issue # 19
April, 1999	Fixed: Issue # 23
April, 1999	NoFix: Normal operation. Issue # 24

Date of Revision (Continued)	Description
May, 1999	Errata incorporated into Appendix of the N440BX Technical Product Specification. Document changes incorporated into the TPS.
June, 1999	Fix: Issue # 26
June, 1999	NoFix: Issue # 27
July, 1999	No Changes
August, 1999	No Changes
September, 1999	BIOS speed selection for 600MHz Pentium® III Processor
October, 1999	Issue # 28 Fixed
November, 1999	No Changes
December, 1999	Updated the General Information section and updated the status on Errata #26.
January, 2000	Added Issue # 29, and Document Change # 1.
February, 2000	No Changes
March, 2000	Updated the General Information section.
April, 2000	Updated the General Information section.
May, 2000	No Changes
June, 2000	No Changes
July, 2000	Corrected the current “681234” revision number in the General Information section.

PREFACE

This document is an update to the specifications contained in the *N440BX DP Server Technical Product Specification* (Order Number 243701), the *Intel Columbus II Chassis Technical Product Specification* (Order Number 282957), and the *Intel Astor Chassis Technical Product Specification* (Order Number 243628). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Specification Clarifications, Errata, and Document Changes.

Refer to the *Pentium® II Processor Specification Update* (Order Number 243337) for specification updates concerning the Pentium II processor. Items contained in the Pentium II Processor Specification Update that either do not apply to the NA440BX DP Server system or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the latest *Intel 82440BX PCIset Specification Update* for specification updates concerning the Intel 82440BX PCIset. Items contained in these Specification Updates that either do not apply to the NA440BX DP Server system or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications for the NA440BX or NC440BX DP Server systems. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the NA440BX and NC440BX DP Server's behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

Specification Update for the N440BX DP Server Board

GENERAL INFORMATION

Identification Information

Below are the specific boards, BIOS and components covered by this update.

Baseboard Fab #	Baseboard PBA #	BIOS	SSU	Processor Stepping	Chipset Stepping (82440BX)
1.3	681234-503	Release 1.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1	B1
1.3	703861-203	Release 1.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1	B1
1.3	681234-504	Release 4.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1	B1
1.3	703861-204	Release 4.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1	B1
1.3	681234-505	Release 4.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1	B1
1.3	703861-205	Release 4.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1	B1
1.3	681234-506	Release 4.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1	B1
1.3	703861-206	Release 4.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1	B1
1.3	681234-507	Release 4.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	703861-207	Release 4.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	681234-508	Release 6.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	703861-208	Release 6.0	Release 1	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	681234-509	Release 6.0	Release 2	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	703861-209	Release 6.0	Release 2	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	681234-520	Release 9.0	Release 3	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1

Baseboard Fab # (Continued)	Baseboard PBA #	BIOS	SSU	Processor Stepping	Chipset Stepping (82440BX)
1.3	703861-220	Release 9.0	Release 3	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	681234-522	Release 11.0	Release 4	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	703861-222	Release 11.0	Release 4	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	681234-523	Release 12.0	Release 4	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	703861-223	Release 12.0	Release 4	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	681234-524	Release 13.0	Release 4	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	703861-224	Release 13.0	Release 4	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	681234-525	Release 13.0	Release 4	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1
1.3	703861-225	Release 13.0	Release 4	Pentium® II processor: A0, A1, B0, B1, C0, C1 Pentium® III processor: B0, C0	C1

Summary Table of Changes

The following tables indicate the Errata and the Document Changes that apply to the NA440BX and/or NC440BX DP Server system. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Intel intends to update the appropriate documentation in a future revision.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	Plans	ERRATA
26	**Fixed**	Boot Block Code to be updated in order to resolve BIOS recovery issue
27	**NoFix**	PERR # events are not logged in the Server Event Log (SEL)
28	**Fixed**	600MHz is not an option in BIOS setup in revisions 11.x and prior
29	**NoFix**	(S1) Sleep State not supported in the dual processor configuration

NO.	Plans	DOCUMENT CHANGES
1	**Fix**	BIOS Setup option listed in the N440BX TPS, but not available in the BIOS Setup

Errata

26. BIOS recovery fails using some single sided DIMMS

PROBLEM: Certain double sided DIMMs do not function correctly when only a single side of their memory is initialized. This causes the BIOS recovery to not complete.
IMPLICATION: BIOS recovery may not complete successfully.
WORKAROUND: If BIOS recovery has failed, try using different memory. Once the recovery process has been successful you can place the original DIMMs back in the system.
STATUS: Fixed. A new memory initialization algorithm that detects whether a DIMM is single or double sided was implemented into the BIOS 12 Boot Block at the Intel factory. This new initialization scheme that is only used during BIOS recovery will detect the DIMM type. If it is a double-sided DIMM it will simultaneously initialize the first 8MB of each side thus ensuring successful BIOS recovery. This fix was cut into the baseboards built with BIOS 12 at the Intel factory. These boards contain a PBA #681234-523 or PBA #703861-223.

27. PERR # events are not logged in the Server Event Log (SEL)

PROBLEM: PCI Parity error is not supported by the 440BX PCIset. On the N440BX the (PERR#) signal is not connected to the basic utility device (BUD). PERR# is connected between the PCI slots and onboard PCI devices on the N440BX baseboard.
IMPLICATION: PERR# events will not be logged in the SEL.
WORKAROUND: None identified.
STATUS: NoFix.

28. BIOS support for 600MHz Pentiumâ III Processor on N440BX Products

PROBLEM: N440BX BIOS revisions 11.X and prior do not list the 600MHz Pentium® III Processor as a possible speed selection in BIOS setup. Despite not being an option, production versions of the 600MHz Pentium® III processor will be recognized and function normally by BIOS revisions 11.X and newer.
IMPLICATION: If not running a production level processor it will be impossible to set clock frequency to 600MHz.
WORKAROUND: NONE
STATUS: Fixed: BIOS 12 may be downloaded from the web at:

http://support.intel.com/support/motherboards/server/n440bx/software.htm

29. (S1) Sleep State not supported in the dual processor configuration

PROBLEM: After Windows* 2000 is installed on an N440BX running with a dual processor configuration, the (S1) Sleep state is not available in Windows* 2000. This issue is due to the PIIX4E implemented on the N440BX baseboard. If Windows* 2000 is installed on an N440BX running with a single processor configuration, the (S1) Sleep state will be available and function correctly in Windows* 2000.
IMPLICATION: When Windows* 2000 is installed with a dual processor configuration, the S1 Sleep State option is not available.
WORKAROUND: NONE
STATUS: NoFix

Document Changes

1. BIOS Setup option listed in the N440BX TPS, but not available in the BIOS Setup

In Revision 2 of the N440BX Technical Product Specification, on page 104 in Table 5-15 System Management Sub-menu Selections, an option to enable/disable the System Management Mode is listed. This option was never implemented in the N440BX BIOS and this reference needs to be removed from the N440BX Technical Product Specification.
STATUS: This will be fixed in the next revision of the N440BX Technical Product Specification.