Intel ISP2150 Internet Server

2U Rack Mount Server System

Technical Product Specification

Revision 1.0
Order Number: A11373

Features:

- High Density 2U Rack Server
- 3.46” (88mm) H x 18.90” (480mm) W x 24.10” (612mm) L with front bezel
- 4 hot swappable Ultra 2 SCSI drive bays capable of supporting two 1” and two 1.6” or four 1” LVD SCSI Hard Drives
- One 3.5” floppy disk
- One bay for an ATAPI Slimline CD-Rom drive with drive tray and attached IDE adapter card
- 275 Watts PFC power supply with custom form factor
- Two system fans and one power supply for cooling
- Volume server platform based on the Intel® Pentium® II and Intel Pentium® III Processor. On the ISP2150, this processor operates with a 100MHz front side bus. The L440GX+ provides two 100MHz 242-contact slot connectors
- Using dual processors, the system is fully MPS (Multi-Processor Specification) 1.4 compliant (with appropriate Pentium® II and Pentium® III extensions). In addition, support is provided for MP operating systems that may not be fully MPS 1.4 compliant
- System design based on Intel® 440GX AGPset, PIIX4e, and I/O APIC devices.
- 100MHz main memory interface supporting up to 2GB of PC/100-compliant commodity SDRAM DIMMs. (ECC and Non-ECC)
- PCI I/O system, compliant with revision 2.1 of the PCI specification.
- Integrated Adaptec* 7896 PCI dual-port SCSI controller providing separate Ultra2 and Ultra wide SCSI channels
- Integrated Intel® EtherExpress™ PRO100+ 10/100Mbit PCI Ethernet controller with integrated physical layer (Intel® 82559)
- Cirrus Logic* GD5480 high performance 2D PCI video controller with 2MB of SGRAM on board
- Two 32 bit, 33 MHz 5 Volt PCI expansion slots
- PCI IDE controller (in PIIX4E) providing dual independent Ultra DMA/33 IDE interfaces, each able to support two IDE drives
- Emergency Management Port (EMP)
- Platform Event Paging (PEP)
- Flash BIOS support for all of the above

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1.0 System Overview

This chapter provides an overview of the ISP2150 2U Rack Server System, showing functional blocks, system diagrams, etc.

1.1. System Level Block Diagram

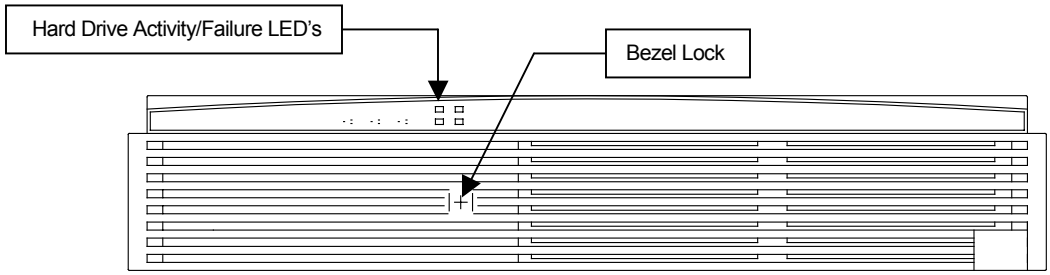


Figure 1. ISP2150 Front Bezel

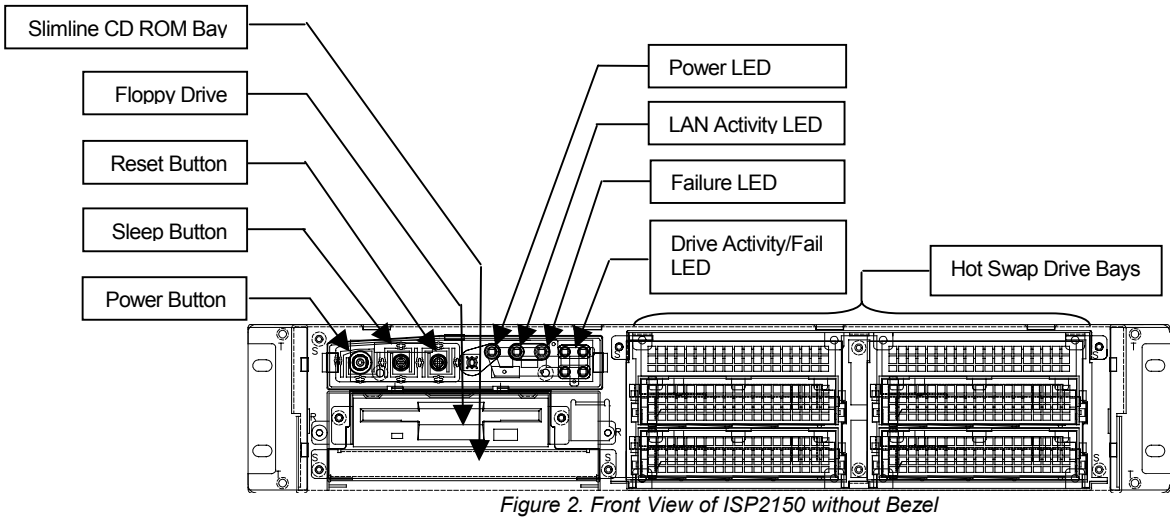


Figure 2. Front View of ISP2150 without Bezel

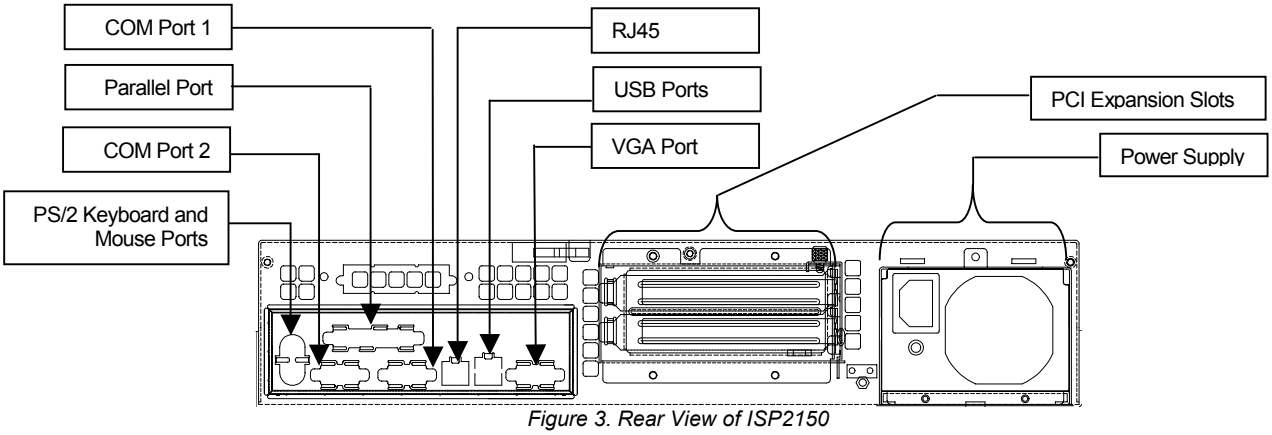


Figure 3. Rear View of ISP2150

1.2. L440GX+ Board Level Block Diagram

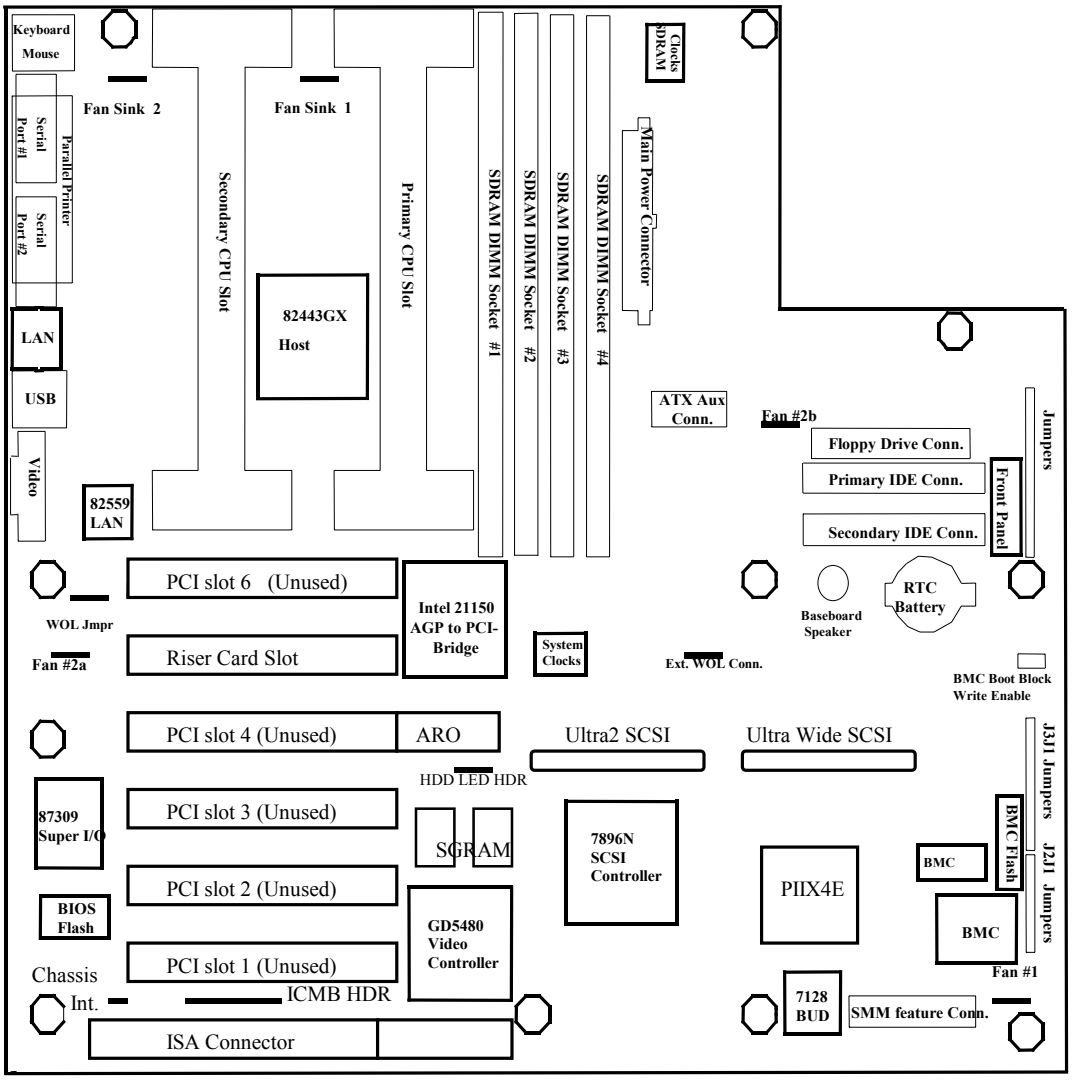


Figure 4. L440GX+ Block Diagram

2.0 ISP2150 Chassis

This section describes the ISP2150 chassis, its various features and functions. This specification details the feature set of the ISP2150 server chassis, an ATX compatible server chassis designed for the Intel® L440GX+ Server board.

2.1. Front Bezel Features

The standard front bezel is molded plastic. The bezel is fog coated in black. The bezel can be folded down to reveal the floppy, CD-ROM and SCSI drive bays, as well as the power, sleep, and reset switches. The front bezel displays the various indicator LED's (see section 1.1). The front bezel also contains a key lock which can be used to prevent opening of the bezel.

Figure 5. ISP2150 with Front Bezel Closed

2.1.1. Locking and Unlocking the Front Bezel

The bezel can be locked and unlocked to prevent unwanted access to the system.
To lock the bezel:

1. Remove the keys from the bezel (they should be taped to the bezel).
2. Close the bezel and insert the key into the lock. Turn the lock counterclockwise until it stops (about a quarter turn). The bezel is now locked and cannot be opened.

To unlock the bezel, insert the key into the lock and turn the lock clockwise until it stops（about a quarter turn). The bezel is now unlocked and can be opened again.

2.1.2. Attaching and Removing the Front Bezel

The front bezel can be installed or removed from the system.
To attach the bezel:

1. With the LED light tunnels located at the top of the bezel, push in the arms on either side of the bezel far enough so that the tabs on the ends of the arms can be inserted into the holes in the handles attached to the chassis.
2. Insert the tabs into the holes in the handles on the chassis. Make sure the tabs on each side of the bezel are completely in the holes in the handles.

To remove the bezel:

1. With the bezel opened, gently push the metal hinge arms located on each side of the bezel in towards the middle of the unit.
2. Push the arms far enough in so that the tabs on the end of the arms are completely out of the holes in the handles on the chassis. The bezel should now be able to be removed.

The bezel should now be able to open and close easily and completely.

2.2. Front Panel

The front panel is located behind the front bezel above the floppy drive. It provides four buttons and seven LEDs. The buttons are Power, Reset, Sleep and NMI. The LEDs are one green for power, one green for NIC activity, one yellow for System Fail and four bi-color (green – disk activity, yellow – disk fail) for the SCSI drives. These LED's are visible from the front bezel through the light pipe.

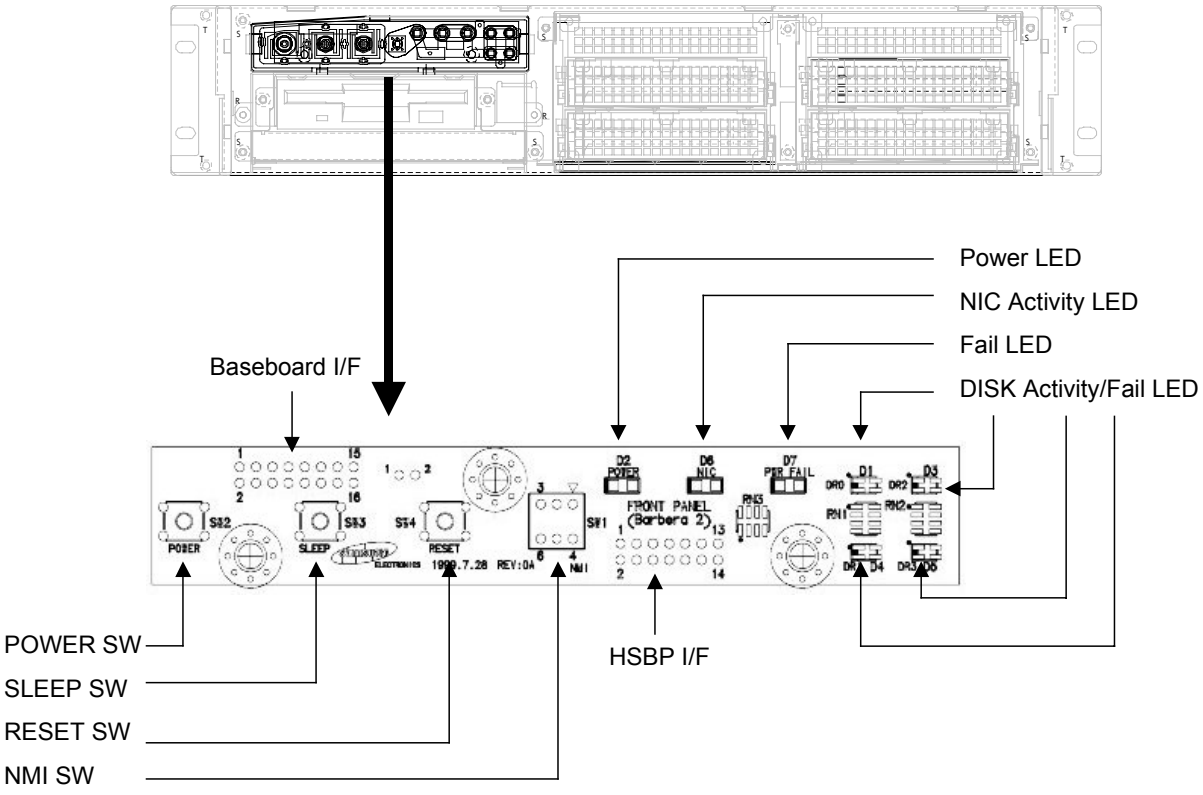


Figure 6. Front Panel and Functions

2.3. Security

The key lock on the front bezel can be used to prevent extraction of the 5.25" peripherals. An alarm switch is provided for the chassis side cover that may be connected directly to the server board, where server management software, such as Intel Server Control can process alarm switch activity as desired.

2.4. I/O panel

All input/output connectors are accessible on the rear of the chassis and an ATX 2.03 compatible cutout is provided for I/O shield installation. A metal I/O shield with appropriate EMI gasget must be installed in the cutout in order to maintain Electromagnetic Interference (EMI) compliance levels. The I/O cutout dimensions are shown in the figure below.

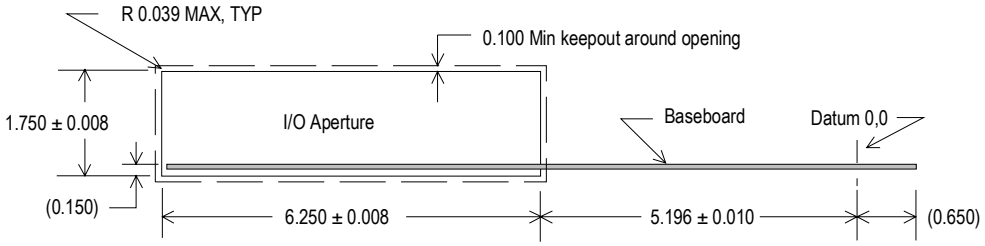


Figure 7. ATX 2.03 I/O Aperture

2.5. Power Supply

The ISP2150 chassis uses a custom form factor power supply. The form factor was chosen to optimize the overall chassis dimensions. The remote enable feature can be used. The remote enable feature permits the chassis power to be activated from a variety of sources, allowing the implementation of "Wake On LAN*" (WOL) or other remote management features. The 275 watt PFC (Power Factor Correction) power supply features an ATX 24 pin main power connector.

2.5.1. Power Supply/Chassis Configuration

The ISP2150 server chassis can only be configured with the Lite-On 275-Watt PFC power supply. For a more detailed specification on the power supply, see the specification for the Lite-On 275-Watt PFC Power Supply (Intel part number 751913).

2.5.2. Mechanical Outline

The mechanical outline and dimensions of the power supply adhere to optimize the overall chassis dimensions. The approximate dimensions of the power supply are: 3.85" (97.8mm) high X 2.5" (63.5mm) wide X 9.5" (241.3mm) deep.

2.5.3. Fan Requirements

The power system incorporates a 60mm low noise fan to exhaust air. The fan voltage and speed vary with power supply loading. In the event of a fan failure, the power supply will shut down, and attempt to auto restart every 10 – 20 seconds.

2.5.4. DC Outputs Rating

The power supply regulates properly over the following load ranges. During the manufacture of the power supply, enough configurations are tested to show functionality over these ranges.

Table 1: Output Current Ratings

	Load Range		
Voltage	MINIMUM CONTINUOUS	MAXIMUM CONTINUOUS	PEAK
+5V	1.00 A	20A	
+3.3V	0A	14A	
+12V	0A	14A	14A
-5V	0A	0.2A	
-12V	0A	0.2A	
+5V STANDBY	0.00A	2.0A	

* The individual outputs cannot exceed the individual maximums shown, and the total combined wattage of all channels must not exceed 275 Watts.

2.5.5. Power Supply Edge Connector Interface

The chassis comes supplied with a power distribution board. The power supply edge connector plugs into the power distribution board. The power distribution board converts the power supply connector into a standard ATX power connector and drive power connectors.

Table 2: Edge Connector Pin Assignments

Signal	Pin	Pin	Signal
N/C	1	2	N/C
N/C	3	4	N/C
N/C	5	6	N/C
N/C	7	8	N/C
RTN	9	10	RTN
RTN	11	12	RTN
RTN	13	14	RTN
RTN	15	16	RTN
N/C	17	18	N/C
N/C	19	20	N/C
POWER GOOD	21	22	N/C
READY SIGNAL	23	24	HARD BOOT
PS ON ACTIVE LOW	25	26	INTERLOCK
PRESENCE	27	28	N/C
+12V	29	30	N/C
+12V	31	32	+12V
+12V	33	34	+12V
-12V	35	36	-5V
+5 V	37	38	+5 V
+5 V	39	40	+5 V
+5 V	41	42	+5 V
+5 V	43	44	N/C
5V remote sense RTN	45	46	5V remote sense
RTN	47	48	RTN
RTN	49	50	RTN
RTN	51	52	RTN
RTN	53	54	RTN
RTN	55	56	RTN
RTN	57	58	RTN
RTN	59	60	RTN
5V STANDBY	61	62	+5 V
3.3V remote sense RTN	63	64	+3.3V remote sense
+3.3V	65	66	+3.3V
+3.3V	67	68	+3.3V
+3.3V	69	70	+3.3V

2.6. Chassis Cooling

Chassis cooling is accomplished using two 80mm system fans mounted in the middle of the chassis. There is also a power supply fan. Removal of the top cover gives access to the fans, which can then be easily changed with the system powered down.

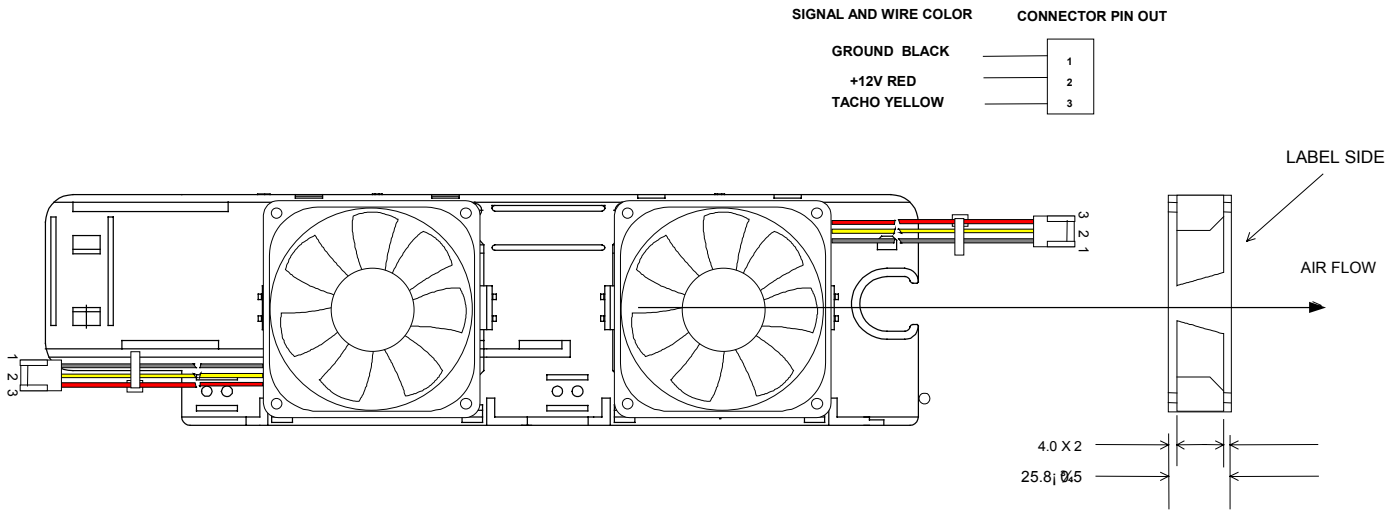


Figure 8. 80mm Mid System Fan

2.7. Chassis Peripheral Bays

2.7.1. 3.5" Floppy Drive Bay

The chassis provides for the installation of a 3.5“ floppy drive above the slimline CD-ROM drive. Removal of the front bezel and top cover provides access for replacement of the floppy drive, and insertion and removal of floppy disk media. A 3.5” 1.44M floppy drive is included with the system.

2.7.2. Slim CD-ROM Drive Bay

The chassis can support 1/2” (12.7mm) Slimline CD-ROM drives. The Slimline CD-Rom tray is exposed by pulling down the front bezel. When installed, the tray resides directly under the floppy drive.

2.7.3. LVD SCSI Hot Swap Drive Bay

The ISP2150 server chassis supports up to four (two 1” high and two 1.6” high) 3.5" SCA2 LVDS hard drives. The drives are accessible in the front of the chassis with the bezel open. The four drive carriers are provided with the chassis to mount hard drives in.

The system was designed to allow the user to install a Redundant Array of Independent Disks (RAID). An add-in RAID controller card, or software implementation can be used to set up RAID configurations.

2.8. Hot-Swap SCSI Sub-System with Saf-Te

The Hot-swap SCSI Sub-system supports the following features:

- Enclosure management and monitoring functions conforming to the *SCSI-Accessed Fault-Tolerant Enclosure Specification* (SAF-TE), Revision 1.00.
- Four Single Connector Assembly (SCA2) connectors for SCA2-compatible SCSI drives
- Hot swapping of SCSI drives, that allows connection of SCSI devices while the power is on and automatic slot power down upon drive removal.
- Full dual mode LVD/SE operation, compliant with Fast, Ultra, and Ultra-2 SCSI bus operation.
- Internal Intelligent Management Bus (IMB)
- Active termination on SCSI bus (SCSI-2 compatible)

The SCSI hot-swap backplane provides control signals and power for four Ultra2/LVD 3.5 inch SCA2 SCSI hard disk drives. The backplane receives control signals from the SCSI controller on the server board through a cable connected to the wide SCSI connector on the backplane. The backplane is powered through the cables connected to the power connector. Drives get their control signals and power from the SCA2 connectors on the backplane.

The SAF-TE specified features supported by the Hot-swap SCSI Backplane include monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include activating a drive fault indicator and powering down a drive that has failed.

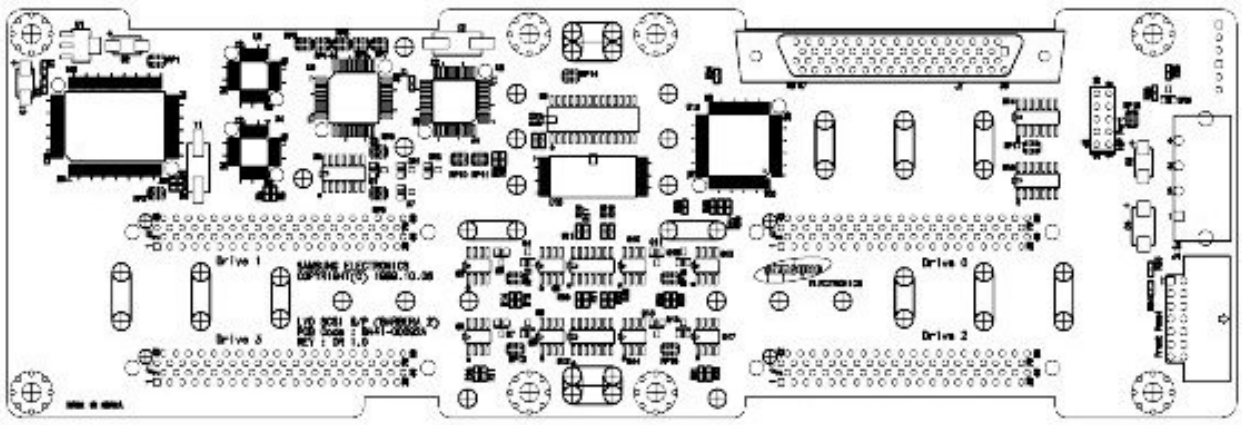
2.8.1. Abstract

The ISP2150 Hot-Swap SCSI Backplane is made up of the following functional blocks:

- SCSI Bus with SCA (Single Connector Attach) drive connectors, and active LVDS terminators
- Micro controller with programmable Flash and RAM
- SCSI interface that allows the micro controller to respond as a SCSI target
- Fault indicator support
- SCSI drive power control
- Configuration jumpers

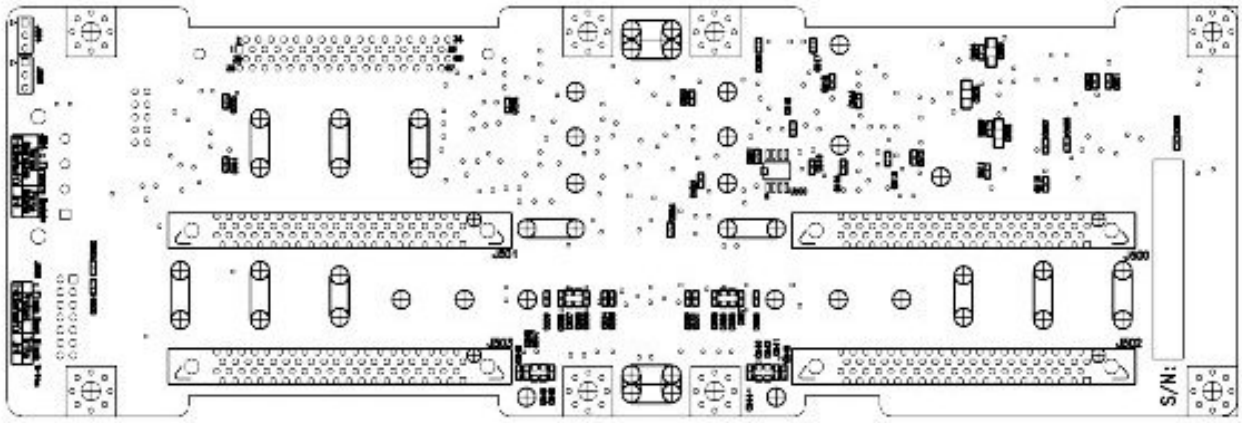
2.8.2. Hot-Swap Backplane Board Layout

The Hot-Swap SCSI Backplane resides in the hot-swap drive bay of the ISP2150 server chassis.The following diagrams show the layout of components and connectors on the Hot-swap SCSI backplane printed circuit board. The ovals in the diagram below represent ventilation holes for the hard drive bay.



< Component Side >

Figure 9. ISP2150 Hot-Swap SCSI Backplane Component and Connector Placement



< SCA 2 Connector Side >

Figure 10. ISP2150 Hot-Swap SCSI Backplane Component and Connector Placement

2.8.3. Configuration Options

The following table describes the various configuration options on the ISP2150 Hot-Swap SCSI backplane along with their function and intended usage.

Option Jumper ID Description

Option	Location	Description
Firmware Update	J504	Placing this jumper in the “FORCE UPDATE” position forces external firmware update of the program code stored in Flash memory. Placing this jumper in the “NORMAL OPERATION” position allows normal operation.
Flash Boot Block Write	J505	This jumper allows the boot block of the program flash to be updated. “PROTECT” does not allow the boot block to be written to. “WRITE” allows updating of the boot block.

Table 3: HSBP Configuration Jumpers

2.8.4. Functional Description

This section defines the architecture of the ISP2150 Hot-swap SCSI Backplane, including descriptions of functional blocks and how they operate. The following figure shows the functional blocks of the Hot-swap SCSI Backplane. An overview of each block follows.

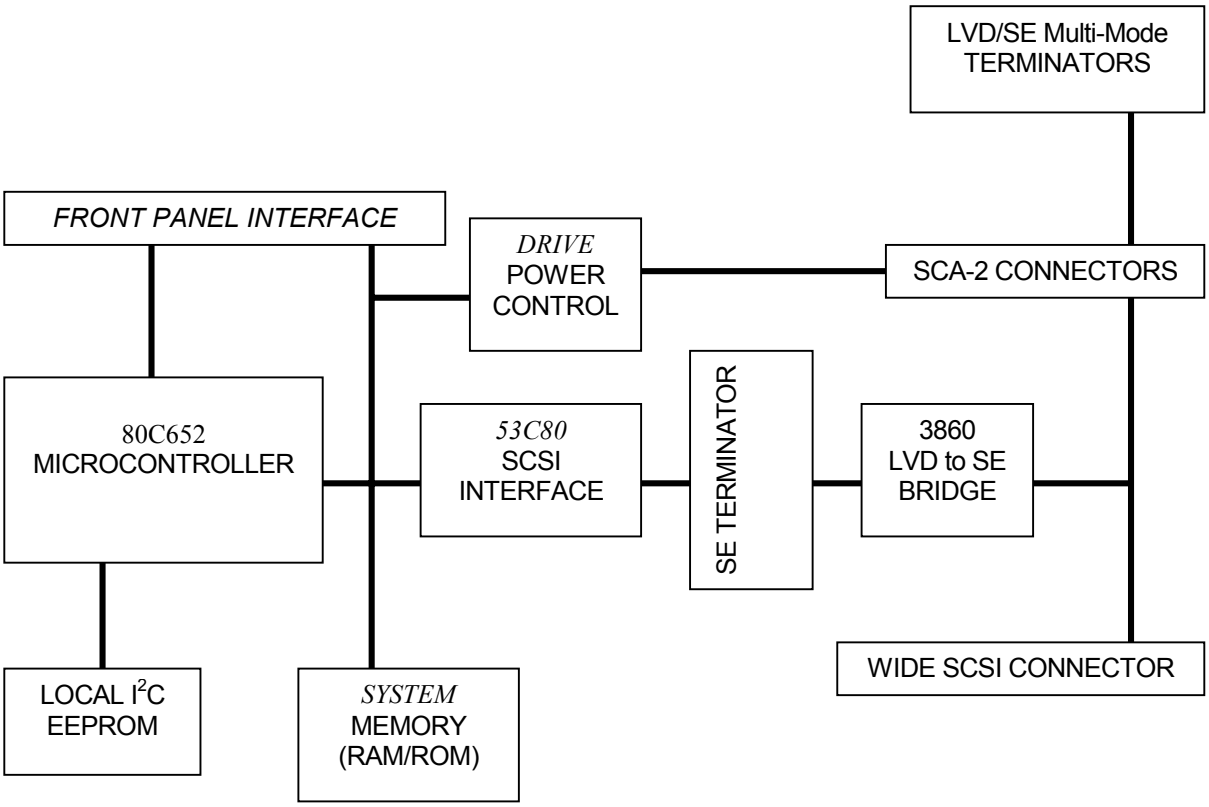


Figure 11. Hot Swap Backplane Block Diagram

2.8.5. SCA2 Hot-Swap Connectors

The ISP2150 Hot-swap SCSI Backplane provides four hot-swap SCA2 connectors that Ultra2 SCSI drives can connect to. These SCA2 connectors provide power and SCSI signals using a single connector. Each SCA drive attaches to the backplane using one of these connectors.

2.8.6. SCSI Interface

The SCSI interface on the ISP2150 Hot-swap SCSI Backplane provides the required circuitry between the SCSI bus and the micro controller, which contains the intelligence for the backplane. This allows the micro controller to respond as a SCSI target. The interface consists of a Symbios* 53C80S SCSI interface Chip, which functions as translator between the SCSI bus and the micro controller. The 53C80S is a single-ended, narrow device.

2.8.7. LVD to SE Bridge

Since the 53C80S is a single-ended, narrow device, an Adaptec* AIC-3860 LVD-to-SE Transceiver (Bridge) is used to create a single-ended extension of the LVD bus. This allows the 53C80S to communicate with the LVD bus.

2.8.8. SE Termination

Passive SE termination is used for the single-ended extension of the SCSI bus that the 53C80S is on.

2.8.9. Power Control

Power control on the ISP2150 Hot-swap SCSI Backplane supports the following features. Power-down if a drive when failure is detected and reported (using enclosure services messages) via the SCSI bus. This decreases the likelihood that the drive, which may be under warranty, is damaged during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a small amount of time for the drive to be fully seated, and then applies power to the drive in preparation for operation.

- If system power is on, the Hot-swap SCSI Backplane immediately powers off a drive slot when it detects that a drive has been removed. This prevents possible damage to the drive when it is partially removed and re-inserted while full power is available, and disruption of the entire SCSI array from possible sags in supply voltage and resultant current spikes.
- Hot-spare drive support, where spare drives are kept in the hot-swap bay, but are left un-powered until a drive is determined to have failed. In this case, the hot spare can be powered up and put into service automatically without requiring immediate operator intervention to replace the drive.
- The Hot-swap SCSI Backplane will automatically bypass the power control circuitry if a shorted drive is inserted or if a drive develops a short during operation. This prevents the Hot-swap SCSI Backplane from being damaged by a drive that draws excessive current.

2.8.10. Micro controller and Memory

The micro controller provides the intelligence for the ISP2150 Hot-swap SCSI Backplane. It is implemented with a Phillips 80C652 micro controller, with a built-in I^2C interface. The micro controller uses a 2 Megabit FLASH EEPROM for program code storage, and a 32 KB SRAM for program execution.

2.8.11. Front Panel Drive Fault LED's

The Drive Fault Indicators are not physically part of the ISP2150 Hot-swap SCSI Backplane, but rather located on the system front panel. They are referenced here because the driving circuitry is entirely contained on the backplane. The drive fault LEDs are activated by the micro controller, and indicate failure status for each drive. A front panel interface connector is provided for an electrical path between the Hot-swap SCSI Backplane, drive fault LEDs, and front panel drive activity indication. During initialization, the micro controller flashes the LEDs for 1 second as part of the POST.

2.8.12. IMB Bus

The IMB bus is a system-wide server management bus, based on the Phillips I^2C bus specification. It provides a way for various system components to communicate independently of the standard system interfaces (e.g., PCI bus or processor/memory bus). The I^2C bus controller is integrated into the micro controller. IMB connectivity is provided to the Backplane via the front panel connector.

2.8.13. Local I 2 C EEPROM & Temperature Sensor

An I^2C bus temperature sensor is connected to the micro controller on a Private I^2C bus. Micro controller programming implements the private I^2C connection by explicitly setting and clearing appropriate clock and data signals, to emulate an I^2C-like interface to the sensor. Temperature information is made available to other devices in the chassis using Enclosure Services messages. A Dallas DS1624 Serial EEPROM/Temperature Sensor implements this function. The EEPROM stores the Field Replaceable Unit (FRU) information for the Backplane.

2.9. 2-Slot Active PCI Riser Card

The Intel® ISP2150 employs a dual-slot PCI riser, which provides two full-length 32-bit/33Mhz PCI slots. The riser is an active riser due to the extra PCI Bus Bridge on the card. The riser resides in PCI slot number 2 of the Intel® L440GX+ server board.

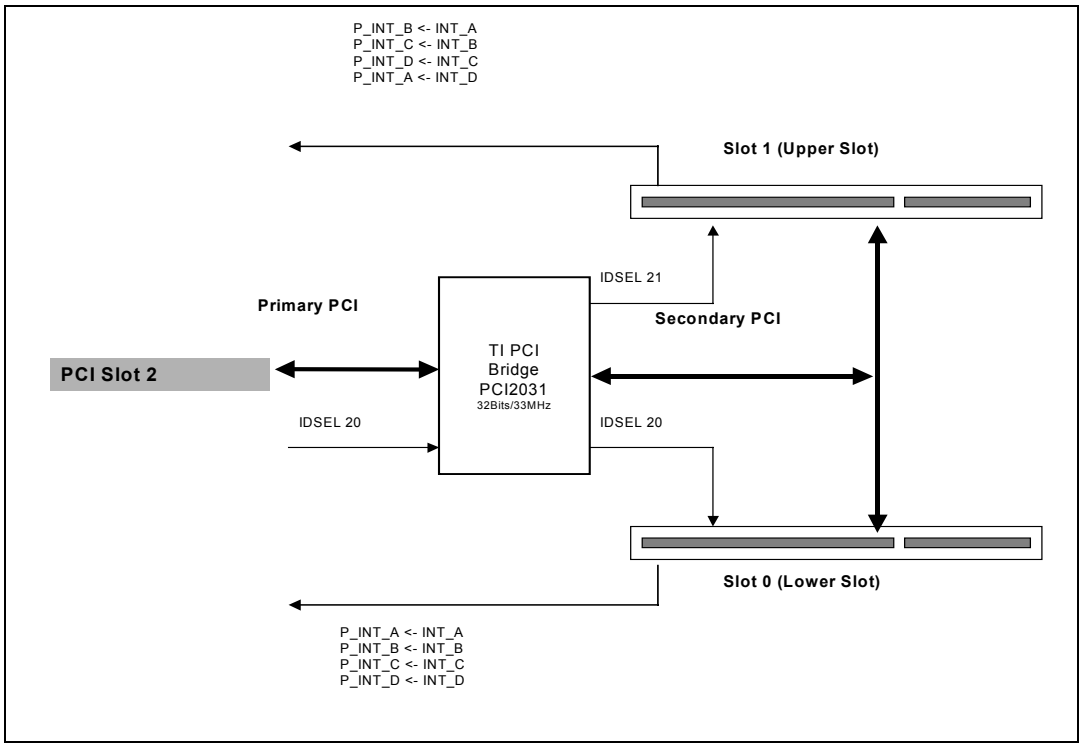


Figure 12. Active PCI Riser Block Diagram

Note: The Intel® L440GX+ baseboard provided in the Intel® LB440GX system contains 6 PCI slots and 1 ISA slot. PCI Slot 2 contains the PCI Riser Card. The other slots are inactive and should not be used. Any (up to two) PCI cards in the system should be inserted in the slots on the PCI Riser card, and not on the server board.

2.10. Slimline CD-ROM IDE Interface Board

The ISP2150 provides a drive tray to install a slimline CD-Rom. On the back of the CD-Rom tray is an interface board that allows the ATAPI connector on the slimline CD-Rom to attach to the tray, and the interface board then attaches to the IDE connector on the L440GX+ server board using an IDE cable.

2.11. Chassis Internal Cables

2.11.1. Front Panel to Hot-swap Backplane

A 14-pin connector cable connects the Front Panel board to the Hot-swap backplane to transfer the drive activities to LED indicators and provide the IMB bus path..

Table 4: Front Panel to Hot-swap Backplane Connector Pinout

Pin #	I/O	Description
1	I/O	I^2C SCL (Serial Clock)
2	PWR	GND
3	PWR	+5V
4	I/O	I^2C Data (Serial Data)
5	-	NC
6	-	NC
7	I	Drive0 Fault LED Cathode
8	I	Drive0 Activity LED Cathode
9	I	Drive1 Fault LED Cathode
10	I	Drive1 Activity LED Cathode
11	I	Drive2 Fault LED Cathode
12	I	Drive2 Activity LED Cathode
13	I	Drive3 Fault LED Cathode
14	I	Drive3 Activity LED Cathode

Baseboard to Front Panel

A 16-pin connector for flat cable is used for connecting baseboard and front panel board. The functions of the each signal are in the table.

Table 5: Front Panel to Baseboard connector Pinout

Pin #	I/O	Description
1	PWR	GND
2	-	NC
3	O	Reset Switch
4	O	Power Switch
5	PWR	+5V
6	-	NC
7	O	NMI Switch
8	I	Power LED Anode
9	-	NC
10	-	NC
11	I	Power fault LED Cathode
12	PWR	+5V standby
13	I/O	IMB Data line
14	I	NIC Activity LED Cathode
15	I/O	IMB Clock line
16	PWR	GND

2.11.2. Server board to SCSI devices

A Wide SCSI cable (68 pin) is provided to interface from the installed baseboard to the Hot-Swap backplane. Four SCA2 connectors in backplane provide interface between the Hot-Swap SCSI backplane and hot-swap SCSI devices.

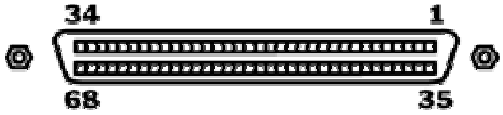


Figure 13. 68 Pin Wide SCSI Cable

Table 6: Ultra Wide (SE) & Ultra2 (LVD) SCSI Connector Pinout

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+DB(12)	18	TERMPWR	35	-DB(12)	52	TERMPWR
2	+DB(13)	19	RESERVED	36	-DB(13)	53	RESERVED
3	+DB(14)	20	GROUND	37	-DB(14)	54	GROUND
4	+DB(15)	21	+ATN	38	-DB(15)	55	-ATN
5	+DB(P1)	22	GROUND	39	-DB(P1)	56	GROUND
6	+DB(0)	23	+BSY	40	-DB(0)	57	-BSY
7	+DB(1)	24	+ACK	41	-DB(1)	58	-ACK
8	+DB(2)	25	+RST	42	-DB(2)	59	-RST
9	+DB(3)	26	+MSG	43	-DB(3)	60	-MSG
10	+DB(4)	27	+SEL	44	-DB(4)	61	-SEL
11	+DB(5)	28	+C/D	45	-DB(5)	62	-C/D
12	+DB(6)	29	+REQ	46	-DB(6)	63	-REQ
13	+DB(7)	30	+I/O	47	-DB(7)	64	-I/O
14	+DB(P)	31	+DB(8)	48	-DB(P)	65	-DB(8)
15	GROUND	32	+DB(9)	49	GROUND	66	-DB(9)
16	DIFFSENS	33	+DB(10)	50	GROUND	67	-DB(10)
17	TERMPWR	34	+DB(11)	51	TERMPWR	68	-DB(11)

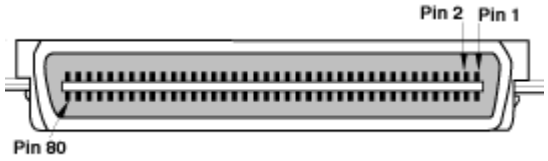
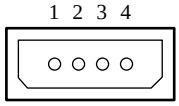


Figure 14. 80 Pin SCA2 Connector

2.12. Connector Interfaces

2.12.1. Hot-Swap Backplane and Peripheral Power Connectors

The Hot-swap backplane power connector and peripheral power connectors are a standard four-pin shrouded plastic PC power connectors with mechanical keying. Connector pinout is shown below.



OM04656

Figure 15. Peripheral power connector

Table 7: Peripheral power connectors

Name	Pin	Description
+12V	1	+12 Volt power supply (yellow wire)
GND	2	0V Electrical ground (black wire)
GND	3	0V Electrical ground (black wire)
+5V	4	+5 Volt power supply (red wire)

2.13. Front/Center Mount Brackets

The ISP2150 has brackets that allow the chassis to be mounted in either front or center mount relay racks, or regular server cabinets. The brackets can be attached at the front of the chassis for front mounting, or in the middle of the chassis for center mounting.

For mounting in a regular server cabinet attach the front mount brackets to the front of the chassis, and an included set of rear support brackets are attached to the back end of the cabinet. This distributes the weight of the server evenly to prevent the mounting rails on the cabinet from bending.

An optional rail kit can be used to mount the server in 19” wide server cabinets (up to 30” deep). This rail kit is available as an accessory.

3.0 L440GX+ Server Board

3.1. Server Board Architectural Overview

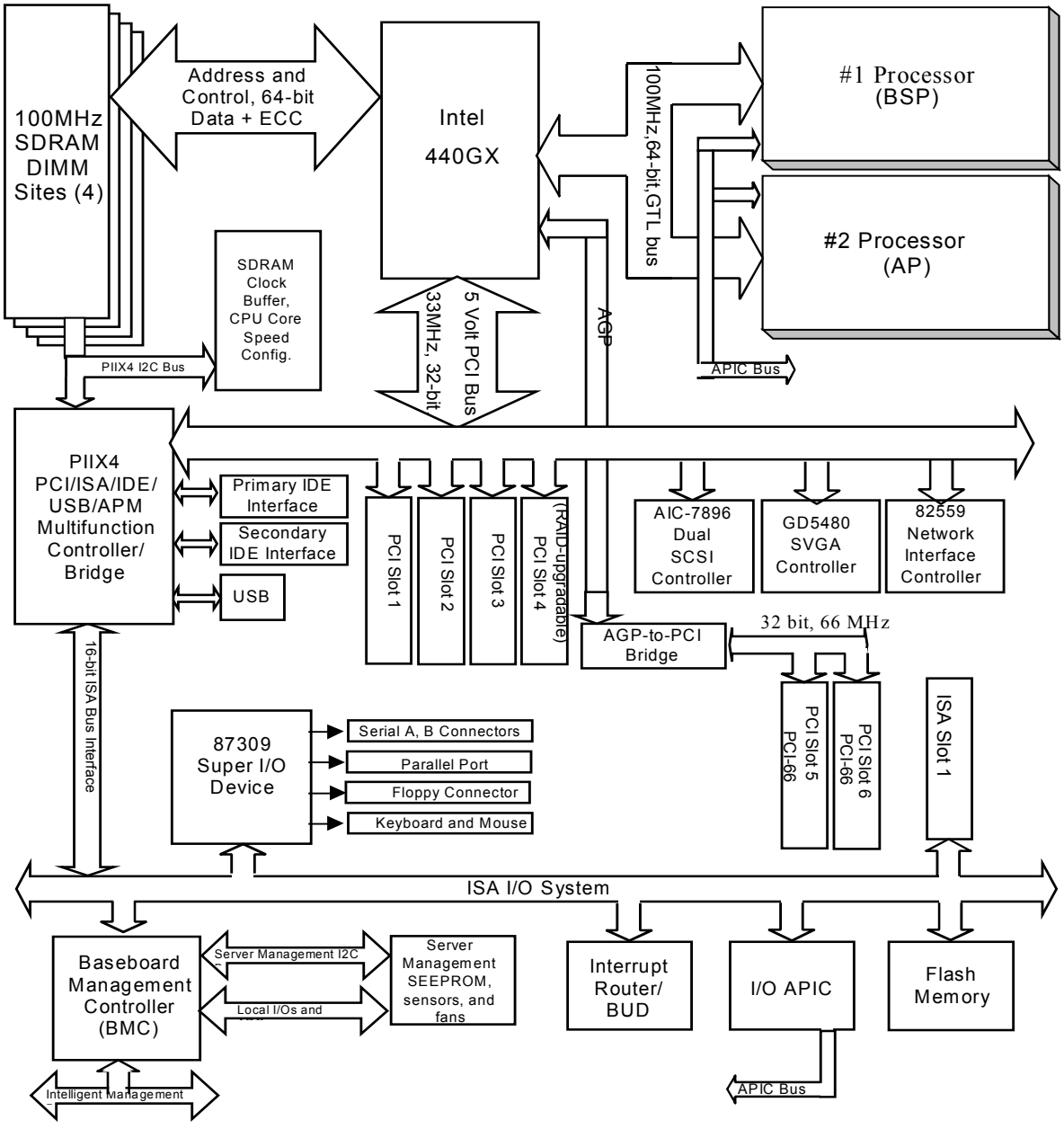


Figure 16. L440GX+ Server Board Architecture Overview

The architecture of the L440GX+ server board is based on a design supporting dual processor operation using Intel Pentium® II or Pentium® III processor cards, and the Intel® 82440GX AGP-set. The L440GX+ provides a PCI-based I/O subsystem containing embedded devices for video, NIC, SCSI, and IDE, along with an ISA bridge to support compatibility devices. The server board also provides support for Server Management and monitoring hardware, as well as interrupt control that supports dual processor and PC/AT compatible operation. This section provides an overview of these L440GX+ subsystems:

- Support for the Pentium® II or Pentium® III processors.
- Intel 440GX AGP-set
- Memory
- PCI support
- BMC Server management controller

3.1.1. Intel® Pentium® II and Pentium® III Processor Support

The L440GX+ server board will only function with the Pentium® II or Pentium® III processor card operating with a 100MHz front side bus. The processor packaging must be the SECC 2 type package. Older Pentium® II processors with SECC 1 packaging will not fit correctly in the Grounded Retention Mechanism on the server board.

The Pentium® II and Pentium® III processor core/L1 cache appears on one side of a pre-assembled printed circuit board, approximately 2.5" x 5" in size, with 256KB or 512KB L2 cache on the backside. The L2 cache and processor core/L1 cache connect using a private bus isolated from the processor host bus and operates at half of the processor core frequency. To compensate for the cache bus speed, the L1 data and code caches are 16KB. The processor supports memory cache of up to 4GB of addressable memory space.

The Pentium® III internal core can operate at frequencies of 500MHz, 533MHz, 550MHz, 600MHz, 650MHz, 667MHz, and 700MHz. While the Pentium® II can operate at frequencies starting up to 450MHz. The Pentium® II and Pentium® III processor's external interface is designed to be MP-ready. Each processor contains a local APIC section for interrupt handling. When two processors are installed, the pair must be of identical revision, core voltage, and bus/core speeds. If only one processor is installed, the other 242-contact slot connector must have a terminator card installed.

3.1.2. Voltage Regulation Modules (VRM)

The L440GX+ server board provides two embedded VRM 8.2-compliant voltage regulators (DC-to-DC converters) to provide VCC_P to each installed processor. One VRM is powered from the 5V supply and the other by the 12V supply. Each VRM automatically determines the proper output voltage as required by each processor.

3.1.3. 82440GX AGPset

The L440GX+ server board architecture is designed around the Intel® 82440GX host bridge controller (440GX). This device provides 100MHz processor host bus interface support, DRAM controller, PCI bus interface, and power management functions. The host bus/memory interface in the 440GX is optimized for 100MHz operation, using 100MHz SDRAM main memory. The PCI interface is PCI 2.1-compliant, providing a 33 MHz / 5V signaling environment for embedded controllers and slots in the single PCI segment on L440GX+ server board. The 440GX memory controller supports up to 2 GB of ECC or non-ECC memory, using PC/100 compliant Synchronous DRAM (SDRAM) devices on DIMM plug-in modules. ECC can detect and correct single-bit errors, and detect multiple-bit errors.

3.1.4. Memory

The L440GX+ server board only supports 100MHz, PC/100-compliant SDRAM DIMMs. **EDO DIMMs cannot be used.** Two types of memory devices on the DIMMs are supported: registered or unbuffered.

Four DIMM slots are provided and are capable of supporting 168 pin JEDEC, 3.3 Volt, 72-bit Registered or Unbuffered ECC DIMMs or 64-bit Unbuffered Non-ECC DIMMs. The minimum supported memory size is 32MB. The maximum memory size configurable is 2GB. Memory can be installed in one, two, three, or four sockets and must be populated starting with the lowest numbered slot first and filling slots in consecutive order. Empty memory slots between DIMMs is not supported. You can mix various sizes of DIMMs, but cannot mix unbuffered and registered DIMMs. Best performance is obtained using unbuffered DIMMs. Registered DIMMs require additional time (1 clock) for memory accesses.

The PIIX4E provides a local Intelligent Management Bus (IMB) interface to SDRAM DIMM information, SDRAM clock buffer control, and processor core speed configuration. BIOS code uses this interface during auto-configuration of the processor/memory subsystem, as part of the overall server management scheme.

3.1.5. PCI I/O Subsystem

The primary I/O bus for the L440GX+ is PCI, compliant with revision 2.1 of the PCI specification. The primary PCI bus supports embedded SCSI, network control, video, and a multi-function device that provides a PCI-to-ISA bridge, bus master IDE controller, Universal Serial Bus (USB) controller, and power management controller. The primary PCI bus also supports the two slots on the PCI Riser for full-length PCI add-in cards.

PCI SCSI Subsystem

The embedded SCSI controller on the L440GX+ is the Adaptec AIC-7896 dual function controller. This device provides both Ultra2 and Ultra wide SCSI interfaces as two independent PCI functions[1]. The four hot swappable drive bays operate off of the Ultra2 channel of the Adaptec AIC-7896 controller.

PCI Network Interface Subsystem

The network interface on the L440GX+ is implemented using an Intel 82559 network controller, which provides a 10/100Mbit Ethernet interface supporting 10baseT and 100baseTX, integrated with an RJ45 physical interface. The 82559 network controller also provides Wake-On-LAN functionality if the power supply used supports a minimum of 720mA of 5V standby current (configurable via baseboard jumper).

PCI Video Subsystem

The embedded SVGA-compatible video controller on the L440GX+ is a Cirrus Logic* GD5480 SGRAM GUI Accelerator. The SVGA subsystem also contains 2MB of SGRAM (synchronous graphics RAM).

[1] The PIIX4E and AIC-7896 are “Multi-function” PCI devices that provide separate sets of configuration registers for each function, while sharing a single PCI hardware connection. Refer to the PCI specification for further details.

PCI-to-ISA Bridge, IDE/USB/PM Controller (PIIX4e)

The PIIX4E is a multi-function PCI device, with four distinct PCI controllers onboard: PCI-to-ISA bridge, PCI bus master IDE interface, USB host controller, and enhanced power management. The PIIX4E also integrates a real-time clock (RTC), 82C54 Timer/Counter, two 82C59 interrupt controllers, and dual 82C37 DMA controllers on-chip that support "distributed DMA" transfers as well as compatibility operation. The PIIX4E also provides general purpose chip select decoding for BIOS, external RTC, keyboard controller and Intel I/O APIC. The integrated IDE controller supports up to four IDE devices in Bus Master mode at speeds up to 33MB/s (Ultra DMA/33 operation). The USB controller is Universal Host Controller Interface (UHCI) compatible.

3.1.6. ISA I/O Subsystem

The L440GX+ contains a full-featured ISA I/O subsystem with local ISA bus interface to embedded Super I/O, I/O APIC, Flash BIOS, Basic Utility Device (BUD), and server management features.

National Semiconductor* 87309 Super I/O Device

Compatibility I/O on the L440GX+ is implemented using a National PC87309VLJ component. This device integrates a floppy disk controller, keyboard and mouse controller, two enhanced UARTs, full IEEE 1284 parallel port, and support for power management. The chip provides separate configuration register sets for each supported function. Connectors are provided for all compatible I/O devices.

I/O APIC

The L440GX+ server board incorporates an Intel S82093AA Advanced Programmable Interrupt Controller to handle interrupts in accordance with Multiprocessor Specification 1.4.

Flash BIOS

The BIOS for the L440GX+ server board resides in an Intel 28F008S5 FlashFile Memory Family, 8Mbit, symmetrically blocked (64KB) flash device.

Server Management Subsystem

The L440GX+ server board incorporates a Dallas* 82CH10 micro-controller as the baseboard management controller (BMC). The BMC controls and monitors server management features on the server board, and provides the ISA interface to two independent IMB-based serial buses. The power supply on/off control, hard reset control, video blanking, watchdog timers, Fault Resilient Booting (FRB) functionality, and all temperature, voltage, fan and chassis intrusion monitoring are integrated into the BMC. The BMC can be polled for current status, or configured to automatically send an alert message when an error condition is detected either manually or by software. In addition, the L440GX+ server board provides an Emergency Management Port (EMP). With an external modem connected to serial port 2, this feature provides remote reset, power up/down control, and access to the event log, or run-time information. This port also supports console redirection.

Basic Utility Device

The L440GX+ provides the Basic Utility Device (BUD) for ISA and PCI interrupt routing, SMI/NMI routing, and PCI arbitration expansion. The physical device is an Altera* 7128 CPLD.

3.2. L440GX+ Functional Architecture

This chapter provides high level descriptions of functionality distributed between functional blocks (e.g., interrupt structure, clocks, resets, and server management).

3.2.1. Processor / PCI Host Bridge / Memory Subsystem

The processor/PCI bridge/memory subsystem consists of support for 1 to 2 identical Pentium® II or Pentium® III processor card(s), and up to 4 PC/100 SDRAM DIMMs. This support circuitry on the baseboard consists of the following:

- Intel 82440GX (440GX) PCI host bridge, memory, and power management controller chip.
- Dual 100MHz FSB 242-contact slot connectors accepting identical Pentium® II or Pentium® III processor cards (if using 1 processor, a GTL+ terminator card must be inserted into the empty slot).
- Four 168-pin DIMM connectors for interface to SDRAM memory.
- Processor host bus GTL+ support circuitry, including termination power supply.
- Embedded DC-to-DC voltage converters for processor power.
- APIC bus.
- Miscellaneous logic for reset configuration and processor card presence detection.

3.2.2. 82440GX Host Bridge

The 82440GX host bridge is a 492-pin BGA device with a 3.3V core and mixed 5V, 3.3V, and GTL+ signal interface pins. The PCI host bridge in the 440GX provides the sole pathway between processor and I/O systems, performing control signal translations and managing the data path in transactions with PCI resources onboard. This includes translation of 64-bit operations in the GTL+ signaling environment at 100MHz, to a 32-bit PCI Rev. 2.1 compliant, 5V signaling environment at 33MHz. The 440GX also handles arbitration for PCI bus master access. For more information on L440GX+ arbitration specifics, refer to “PCI Arbitration” later in this chapter. Although the 440GX is capable of being clocked to operate with multiple processor FSB frequencies, on L440GX+ the host bridge only supports a 100MHz FSB. The device also features 32-bit addressing (not 36-bit), 4 or 1 deep in-order and request queue (IOQ), dynamic deferred transaction support, and Desktop Optimized (DTO) GTL bus driver support (gated transceivers for reduced power operation). The PCI interface provides greater than 100 MB/s data streamlining for PCI to SDRAM accesses (120 MB/s for writes), while supporting concurrent processor host bus and PCI transactions to main memory. This is accomplished using extensive data buffering, with processor-to-SDRAM and PCI-to-SDRAM write data buffering and write-combining support for processor-to-PCI burst writes.

440GX Memory Controller

The 440GX performs the function of memory controller for the L440GX+. Total memory of 32MB to 2GB is supported. Although the memory controller supports a variety of memory devices, the L440GX+ implementation only supports PC/100 compliant, 72-bit, unbuffered or registered ECC SDRAM DIMMs or PC/100 Compliant 64-bit, unbuffered Non-ECC SDRAM DIMMs.

The 440GX provides ECC that can detect and correct single-bit errors (SED/SEC), and detect all double-bit and some multiple-bit errors (DED). Parity checking and ECC can be configured under software control; higher performance is possible if ECC is disabled (1 clock savings). At initial power-up, ECC and parity checking are disabled.

3.2.3. Processor sub-system

The L440GX+ provides two 242 pin connectors providing support for dual Pentium® II or Pentium® III processors. The primary processor slot is located at location J9D1 and the secondary processor is located at location J9B1 on the baseboard.

Processor Termination/Regulation/Power

The termination circuitry required by the processor bus signaling environment (GTL+), and the circuitry to set the GTL+ reference voltage are implemented directly on the processor card. The baseboard provides 1.5V GTL+ termination power, and two VRM 8.2-compliant DC-to-DC converters to provide processor VCC_P power at each connector. Power for processor 1 is derived from the 12V supply, using an embedded DC-DC converter onboard. A second DC-DC converter is also embedded for processor 2, which derives power from the 5V supply. Each VRM looks at the VID bits for its respective processor to automatically determine proper output voltage.

Termination Card

If only one processor card is installed on the board, a termination card *must* be installed in the empty processor slot to start the system. The L440GX+ server board contains circuitry that will hold off the deassertion of reset if a processor slot is left vacant. The server will not boot in this condition. The termination card contains GTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector.

APIC Bus

Interrupt notification and generation for dual processors is accomplished with an independent path between local APICs in each processor and the Intel I/O APIC located on the server board. This simple bus consists of 2 data signals and one clock line. PC-compatible interrupt handling is accomplished by using the PIIX4e, with all interrupts delivered to the processor via the INTR line. However, reduced interrupt latency is possible when the APIC bus delivers interrupts in uni-processor operation (if supported by the OS). Refer to “Interrupts and I/O APIC” later in this chapter for more information.

Miscellaneous Processor/Memory Subsystem Circuitry

In addition to the circuitry described above, the processor subsystem contains the following:

Processor Core Frequency and Memory Configuration Logic

The PIIX4e provides an independent IMB segment, the PIIX4e System Management Bus (PIIX4e SMB), supporting an IMB EEMUX device (PCF8550) for configuration of processor core speed. The PIIX4e IMB segment also provides access to information stored in IMB ROMs on installed DIMMs, and control of the SDRAM clock buffer that gates synchronous clocks to each DIMM. This feature allows a defective DIMM to be disabled and total memory resized automatically. BIOS code controls these features using IMB operations performed by the PIIX4e.

Processor Card Presence Detection

Logic is provided on the server board to detect the presence and identity of installed processor or termination cards. A termination card *must* be installed in a vacant processor card slot to ensure reliable system operation. If the logic senses an empty connector, the installed processor will not be allowed to leave the reset state, preventing operation of the system with an improperly terminated GTL+ processor bus.

3.3. PCI I/O Subsystem

All I/O for the L440GX+, including PCI and PC-compatible I/O, is directed through the PCI interface. On the L440GX+, the primary PCI bus supports the following embedded devices and connectors:

- Two 120-pin, 32-bit, 5 Volt, PCI expansion slot connectors on the Active PCI Riser attached to slot 2 on the server board
- PIIX4e PCI-to-ISA bridge / IDE / USB / Power Management (and PIIX4e SMB) controller
- PCI video controller, Cirrus Logic CL-GD5480
- PCI Ultra2/Ultra Wide SCSI Controller, Adaptec AIC-7896
- PCI Network Interface Controller, Intel 82559

Each device under the PCI host bridge has its IDSEL signal connected to one bit out of the PCI Address/Data lines AD[31::11], which acts as a device select on the PCI bus. This determines a unique PCI device ID value for use in configuration cycles.

3.3.1. PCI Arbitration

The L440GX+ primary PCI bus supports 8 PCI masters: NIC, PCI slots 1(unused) and 2, SCSI, PIIX4e, and 440GX host bridge (video is always a slave). All PCI masters must arbitrate for PCI access, using resources supplied by both the 440GX and custom arbitration logic. The 440GX uses internal arbitration connections within its host interface, and the PCI interface on the 440GX provides 5 REQ_L/GNT_L pairs for external devices or bridges. Logic in the BUD provides support for an additional master on a “Round Robin” basis.

One of the arbitration extensions goes to the SCSI controller, which contains an internal arbiter for bus master access to each SCSI interface (LVDS and SE).

The PIIX4e operates with a private arbitration scheme so that access time capability for ISA masters is guaranteed.

3.3.2. PCI Bus Termination

Certain PCI signals on the L440GX+ have “functional” termination, i.e., either pull-up or pull-down resistors. In addition, certain PCI signals may require additional termination to meet signal quality requirements.

3.3.3. PIIX4e

The PIIX4e is a multi-function PCI device, providing four PCI functions in a single package: PCI-to-ISA bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the PIIX4e has its own set of configuration registers and once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus

interface. The PIIX4e is packaged as a 324-pin BGA device. On L440GX+, its primary role is to provide the gateway to all PC-compatible I/O devices and features.

L440GX+ uses the following PIIX4e features:

- PCI interface
- ISA bus interface
- Dual IDE interfaces
- USB interface
- Power management control
- System reset control
- ISA-compatible interrupt control
- PC-compatible timer/counters and DMA controllers
- Baseboard plug-n-play support
- General purpose I/O
- Real-time Clock and CMOS configuration RAM.

3.3.4. SCSI Subsystem

The L440GX+ provides an embedded dual-function, PCI SCSI host adapter: Adaptec AIC-7896. The AIC-7896 contains two independent SCSI controllers that share a single PCI bus master interface as a multi-function device, packaged in a 352-pin BGA. Internally, each controller is identical, capable of operations using either 16-bit Ultra Wide SCSI providing 40 MB/s or Ultra2 SCSI providing 80 MB/s. In the L440GX+ implementation, controller A (Location J3E2) attaches to a 68-pin 16-bit differential Ultra2 SCSI connector and controller B (Location J3G1) attaches to a 68-pin 16-bit single ended Ultra Wide SCSI connector interface. Each controller has its own set of PCI configuration registers and SCSI I/O registers. As a PCI 2.1 bus master, the AIC-7896 supports burst data transfers on PCI up to the maximum rate of 133 MB/sec using on-chip buffers.

Adaptec* AIC-7896 PCI Signals

The Adaptec AIC-7896 supports all of the required 32-bit PCI signals including the PERR_L and SERR_L functions. Full PCI parity is maintained on the entire data path through the chip. The device also takes advantage of PCI interrupt signaling capability, using PCI_INTB_L (for controller A, Ultra2 SCSI) and PCI_INTC_L (for controller B, Ultra Wide) on the L440GX+ baseboard.

Adaptec* AIC-7896 Supported PCI Commands

The AIC-7896 supports PCI commands as shown in the following table:

Table 8: Embedded SCSI Supported PCI Commands

C/BE [3::0] _L	Command	AIC-7896 Support	
		Target	Master
0000	Interrupt Acknowledge	No[1]	No
0001	Special Cycle	No[1]	No
0010	I/O Read	Yes[2]	No
0011	I/O Write	Yes[2]	No
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes[2,3]	Yes[4]
0111	Memory Write	Yes[2,3]	Yes[4]
1000	Reserved	No[1]	No
1001	Reserved	No[1]	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	Yes[5]	Yes
1101	Dual Address Cycle	Yes[6]	Yes
1110	Memory Read Line	Yes[5]	Yes
1111	Memory Write and Invalidate	Yes[7]	Yes

Notes:

1. Ignored after checking address parity.
2. Support for 8-bit transfers only for all registers in its device register space.
3. Support for 32-bit transfers only for the external ROM/ EEPROM.
4. Support for transfers from system memory.
5. Defaults to Memory Read.
6. Will respond to DAC if PCI Address matches the MBAR[63:12].
7. Defaults to Memory Write.

The extensions to memory commands (memory read multiple, memory read line, and memory write and invalidate) work with the cache line size register to give the cache controller advance knowledge of the minimum amount of data to expect. The decision to use either the memory read line or memory read multiple commands is determined by a bit in the configuration space command register for this device.

SCSI Interfaces

Each SCSI interface on L440GX+ offers active negation outputs, controls for external differential transceivers, a disk activity output, and a SCSI terminator power down control. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48mA single-ended SCSI bus with no additional drivers (the SCSI segment can handle up to 15 devices). SCSI termination power is always on, regardless of the register settings for AIC-7896 SCSI termination power control features.

SCSI Bus

The SCSI data bus is 8- or 16-bits wide with odd parity generated per byte. SCSI control signals are the same for either bus width. To accommodate 8-bit devices on the 16-bit Wide SCSI connector, the AIC-7896 assigns the highest arbitration priority to the low byte of the 16-bit word. This way, 16-bit targets can be mixed with 8-bit if the 8-bit devices are placed on the low data byte. For 8-bit mode, the unused high data byte is self-terminated and need not be connected. During chip power down, all inputs are disabled to reduce power consumption. The following table shows the pin out for the Single-Ended (SE) and LVD SCSI connectors.

Table 9: Ultra Wide (SE) & Ultra2 (LVD) SCSI Connector Pinout

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+DB(12)	18	TERMPWR	35	-DB(12)	52	TERMPWR
2	+DB(13)	19	RESERVED	36	-DB(13)	53	RESERVED
3	+DB(14)	20	GROUND	37	-DB(14)	54	GROUND
4	+DB(15)	21	+ATN	38	-DB(15)	55	-ATN
5	+DB(P1)	22	GROUND	39	-DB(P1)	56	GROUND
6	+DB(0)	23	+BSY	40	-DB(0)	57	-BSY
7	+DB(1)	24	+ACK	41	-DB(1)	58	-ACK
8	+DB(2)	25	+RST	42	-DB(2)	59	-RST
9	+DB(3)	26	+MSG	43	-DB(3)	60	-MSG
10	+DB(4)	27	+SEL	44	-DB(4)	61	-SEL
11	+DB(5)	28	+C/D	45	-DB(5)	62	-C/D
12	+DB(6)	29	+REQ	46	-DB(6)	63	-REQ
13	+DB(7)	30	+I/O	47	-DB(7)	64	-I/O
14	+DB(P)	31	+DB(8)	48	-DB(P)	65	-DB(8)
15	GROUND	32	+DB(9)	49	GROUND	66	-DB(9)
16	DIFFSENS	33	+DB(10)	50	GROUND	67	-DB(10)
17	TERMPWR	34	+DB(11)	51	TERMPWR	68	-DB(11)

3.3.5. PCI Video

The L440GX+ provides a Cirrus* Logic CL-GD5480 video controller, along with 2MB video SGRAM and support circuitry for an embedded SVGA video subsystem. The CL-GD5480 64-bit VGA Graphics Accelerator chip contains an SVGA video controller, clock generator, BitBLT engine, and RAMDAC in a 208-pin PQFP. 256K x 32 SGRAM chips provide 2 MB of 10ns video memory. The SVGA subsystem supports a variety of modes: up to 1600 x 1200 resolution, and up to 16.7 M colors. It also supports analog VGA monitors, single- and multi-frequency, interlaced and non-interlaced, up to 100 Hz vertical retrace frequency. The L440GX+ baseboard also provides a standard 15pin VGA connector, and external video blanking logic for Server Management Console Redirection support.

Video Chip PCI Signals

The CL-GD5480 supports a minimal set of 32-bit PCI signals since it never acts as a PCI master. As a PCI slave, the device requires no arbitration or interrupt connections.

Video Controller PCI Commands

The CL-GD5480 supports the following PCI commands:

Table 10: Video Chip Supported PCI Commands

		CL-GD5480 Support	
C/BE[3::0]_L	Command Type	Target	Master
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	No
0111	Memory Write	Yes	No
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	No
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	No
1111	Memory Write and Invalidate	No	No

Video Modes

The CL-GD5480 supports all standard IBM* VGA modes. Using 2 MB of SGRAM, L440GX+ supports special Cirrus Logic extended modes. The following tables show the standard and extended modes that this implementation supports, including the number of colors and palette size (e.g., 16 colors out of 256 K colors), resolution, pixel frequency, and scan frequencies.

Table 11: Standard VGA Modes

Mode(s) in Hex	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	16/256K	360 X 400	14	31.5	70
2, 3	16/256K	720 X 400	28	31.5	70
4, 5	4/256K	320 X 200	12.5	31.5	70
6	2/256K	640 X 200	25	31.5	70
7	Mono	720 X 400	28	31.5	70
D	16/256K	320 X 200	12.5	31.5	70
E	16/256K	640 X 200	25	31.5	70
F	Mono	640 X 350	25	31.5	70
10	16/256K	640 X 350	25	31.5	70
11	2/256K	640 X 480	25	31.5	60
12	16/256K	640 X 480	25	31.5	60
12+	16/256K	640 X 480	31.5	37.5	75
13	256/256K	320 X 200	12.5	31.5	70

Table 12: Extended VGA Modes

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Video Memory Rqmnts
58, 6A	16/256K	800 X 600	36	35.2	56	1MB
58, 6A	16/256K	800 X 600	40	37.8	60	1MB
58, 6A	16/256K	800 X 600	50	48.1	72	1MB
58, 6A	16/256K	800 X 600	49.5	46.9	75	1MB
5C	256/256K	800 X 600	36	35.2	56	1MB
5C	256/256K	800 X 600	40	37.9	60	1MB
5C	256/256K	800 X 600	50	48.1	72	1MB
5C	256/256K	800 X 600	49.5	46.9	75	1MB
5C	256/256K	800 X 600	56.25	53.7	85	1MB
5C	256/256K	800 X 600	68.2	63.6	100	1MB
5D	16/256K (interlaced)	1024 X 768	44.9	35.5	43	1MB
5D	16/256K	1024 X 768	65	48.3	60	1MB
5D	16/256K	1024 X 768	75	56	70	1MB
5D	16/256K	1024 X 768	78.7	60	75	1MB
5E	256/256K	640 X 400	25	31.5	70	1MB
5F	256/256K	640 X 480	25	31.5	60	1MB
5F	256/256K	640 X 480	31.5	37.9	72	1MB
5F	256/256K	640 X 480	31.5	37.5	75	1MB
5F	256/256K	640 X 480	36	43.3	85	1MB
5F	256/256K	640 X 480	43.2	50.9	100	1MB
60	256/256K (interlaced)	1024 X 768	44.9	35.5	43	1MB
60	256/256K	1024 X 768	65	48.3	60	1MB
60	256/256K	1024 X 768	75	56	70	1MB
60	256/256K	1024 X 768	78.7	60	75	1MB
60	256/256K	1024 X 768	94.5	68.3	85	1MB
60	256/256K	1024 X 768	113.3	81.4	100	1MB
64	64K	640 X 480	25	31.5	60	1MB
64	64K	640 X 480	31.5	37.9	72	1MB
64	64K	640 X 480	31.5	37.5	75	1MB
64	64K	640 X 480	36	43.3	85	1MB
64	64K	640 X 480	43.2	50.9	100	1MB
65	64K	800 X 600	36	35.2	56	1MB
65	64K	800 X 600	40	37.8	60	1MB
65	64K	800 X 600	50	48.1	72	1MB
65	64K	800 X 600	49.5	46.9	75	1MB
65	64K	800 X 600	56.25	53.7	85	1MB
65	64K	800 X 600	68.2	63.6	100	1MB
66	32K	640 X 480	25	31.5	60	1MB
66	32K	640 X 480	31.5	37.9	72	1MB
66	32K	640 X 480	31.5	37.5	75	1MB
66	32K	640 X 480	36	43.3	85	1MB
66	32K	640 X 480	43.2	50.9	100	1MB
67	32K	800 X 600	36	35.2	56	1MB
67	32K	800 X 600	40	37.8	60	1MB
67	32K	800 X 600	50	48.1	72	1MB
67	32K	800 X 600	49.5	46.9	75	1MB
67	32K	800 X 600	56.25	53.7	85	1MB

VGA connector

The following table shows the pinout of the VGA connector:

Table 13: Video Port Connector Pinout

Pin	Signal	Description
1	RED	Analog color signal R
2	GREEN	Analog color signal G
3	BLUE	Analog color signal B
4	nc	No connect
5	GND	Video ground (shield)
6	GND	Video ground (shield)
7	GND	Video ground (shield)
8	GND	Video ground (shield)
9	nc	No connect
10	GND	Video ground
11	nc	No connect
12	DDCDAT	Monitor ID data
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync
15	DDCCLK	Monitor ID clock

3.3.6. Network Interface Controller (NIC)

The L440GX+ supports a 10BASE-T/100BASE-TX network subsystem based on the Intel 82559 Fast Ethernet PCI Bus Controller. No external devices are required to implement an embedded network subsystem, except TX/RX magnetics, 2 status LEDs, and a connector as provided on the L440GX+ baseboard.

The 82559 is a highly integrated PCI LAN controller for 10 or 100 Mbps Fast Ethernet networks. As a PCI bus master, the 82559 can burst data at up to 132 MB/s. This high-performance bus master interface can eliminate the intermediate copy step in RX/TX frame copies, resulting in faster frame processing. The network OS communicates with the 82559 using a memory-mapped I/O interface, PCI interrupt connected directly to the BUD, and two large receive and transmit FIFO's, which prevent data overruns or under runs while waiting for access to the PCI bus, as well as enabling back to back frame transmission within the minimum 960ns inter-frame spacing.

Supported Network Features

The 82559 contains an IEEE MII compliant interface to the components necessary to implement a IEEE 802.3 100BASE-TX network connection. L440GX+ supports the following features of the 82559 controller:

- Glue less 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with PCI Bus Specification, revision 2.1
- 82596-like chained memory structure, with improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- On-chip counters for network management
- Auto detect and auto switching for 10 or 100 Mbps network speeds

- Support for both 10 Mbps and 100 Mbps Networks, full or half duplex-capable, with back-to-back transmit at 100 Mbps
- Integrated physical interface to TX magnetics.

The magnetics component terminates the 100BASE-TX connector interface. A Flash device stores the network ID.

NIC Connector and Status LEDs

The 82559 drives the LED's on the network interface connector that indicate transmit/receive activity on the LAN, valid link to the LAN, and 10/100 Mbps operation. The location and function of each LED is shown in the following figure.

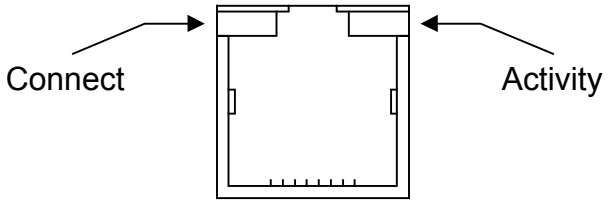


Figure 17. NIC Connector and Status LEDs

3.4. ISA I/O Subsystem

On the L440GX+, the PIIX4E provides a bridge to an ISA I/O subsystem that supports the following connectors and devices:

- Flash memory for BIOS ROM and extensions
- National Semiconductor PC87309VLJ Super I/O chip, which supports the following:
  - Two PC-compatible serial ports
  - Enhanced parallel port
  - Floppy controller
  - Keyboard/Mouse ports

The ISA I/O subsystem also connects with the Intel I/O APIC and BMC. The I/O APIC relays interrupts produced by ISA devices in dual processor operation (or in uni-processor operation) for increased performance with certain OS implementations. The BUD, a programmable logic device performs rerouting of PCI interrupts as ISA interrupts for MP OS implementations that are not fully MPS 1.4 compatible, and management interrupt (NMI_L and SMI_L) control. Refer to "Interrupts and I/O APIC" later in this chapter for more information on these devices and how they are used in the L440GX+ interrupt structure.

3.4.1. Compatibility I/O Controller Subsystem

The National Semiconductor* PC87309VLJ Super I/O device is a plug and play (PnP) compatible, standard I/O subsystem device. This device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. L440GX+ provides the connector interface for each. In addition, the Super I/O contains a real-time clock, which is unused on L440GX+.

Serial Ports

Two 9-pin D-Sub connectors in a side-by-side housing are provided for Serial ports A and B. Both ports are compatible with 16550A and 16450 UARTs, supporting relocatable I/O addresses. Each serial port can be set to 1 of 4 different COM ports, and can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. The pinout for the connectors is shown below:

Table 14: Serial Port Connector Pinout

Pin	Name	Description
1	DCD	Data Carrier Detected
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Return to Send
8	CTS	Clear to Send
9	RIA	Ring Indication Active

Parallel Port

The 25/15 pin high rise connector stacks the parallel port connector over serial connector ports A & B. The 87309 provides an IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS programming of the Super I/O registers enable the parallel port, and determine the port address and interrupt. When disabled, the interrupt is available to add-in cards. The Pin-out is shown below:

Table 15: Parallel Port Connector Pin-out

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

Floppy Disk Controller

The FDC on the Super I/O is functionally compatible with the PC8477, which contains a superset of the floppy disk controllers in the DP8473 and N82077. The baseboard provides the 24 MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the Super I/O, including analog data separator and 16-byte FIFO. The floppy disk connector located at J6H1 on the baseboard has the following pinout:

Table 16: Floppy Port Connector Pinout

Pin	Name	Pin	Name
1	GND	18	FD_DIR_L
2	FD_DENSEL	19	GND
3	GND	20	FD_STEP_L
4	Nc	21	GND
5	Key	22	FD_WDATA_L
6	FD_DRATE0	23	GND
7	GND	24	FD_WGATE_L
8	FD_INDEX_L	25	GND
9	GND	26	FD_TRK0_L
10	FD_MTR0_L	27	FD_MSEN0
11	GND	28	FD_WPROT_L
12	FD_DR1_L	29	GND
13	GND	30	FD_RDATA_L
14	FD_DR0_L	31	GND
15	GND	32	FD_HDSEL_L
16	FD_MTR1_L	33	GND
17	FD_MSEN1	34	FD_DSKCHG_L

Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single stacked housing. External to the board they appear as two connectors. The keyboard and mouse controller is software compatible with the 8042AH and PC87911. The keyboard and mouse connectors are PS/2 compatible and are interchangeable. The pinout definitions below are dependent on which device is plugged into which slot.

Table 17: Keyboard Connector Pinout

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	KEYCLK	Keyboard Clock
6	(NC)	

Table 18: Mouse Connector Pinout

Pin	Signal	Description
1	MSEDAT	Mouse Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	MSECLK	Mouse Clock
6	(NC)	

AT-style Front Panel Header

A 19-pin single inline header is provided for AT-style front panel connections, e.g., power, LED indicators, and reset. The connector has the following pinout:

Table 19: AT Front Panel Header Pinout

Pin	Signal
1	Pwr_Cntrl_Fp – 5V_STNDBY
2	Ground
3	No Pin
4	Hd_LED_Pwr – VCC
5	No Pin
6	Fp_HD_Act
7	Hd_LED_Pwr – VCC
8	Ground
9	No Pin
10	Spkr_Int
11	Spkr_Out
12	Ground
13	No Pin
14	Pwr_LED
15	No Pin
16	Ground
17	Rst_Fp
18	Fp_Sleep
19	Ground

3.4.2. Flash ROM BIOS

An 8Mbit flash memory (Intel 28F008S5) provides non-volatile storage space for BIOS and general purposes. The device is byte wide, of the Smart 5 FlashFile family and symmetrically blocked. The Flash device is directly addressed as 16 64-kbyte blocks of 8-bit ISA memory.

Secure Flash Programming Mechanism

On L440GX+, the BUD detects any write operation to Flash and asserts SMI_L. The SMI_L handler (part of BIOS) then looks for a signature from the Flash Memory Update utility (FMUP) before allowing any writes to Flash. This prevents accidental loading of non-compatible BIOS code into Flash.

3.5. System Reset Control

Reset circuitry on the L440GX+ baseboard monitors reset from the front panel, PIIX4, I/O controller, and processor subsystem to determine proper reset sequencing for all types of reset. The reset logic is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

3.6. Interrupts and I/O APIC

L440GX+ interrupt architecture accommodates both PC-compatible PIC mode, and dual-processor APIC mode interrupts. In addition, L440GX+ provides a PCI to ISA interrupt rerouting mechanism for compatibility with some multiprocessor operating systems that do not fully support the APIC.

3.6.1. PIIX4E Compatibility Interrupt Controller

For PC-compatible mode, the PIIX4E provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The PIIX4E and Super I/O contain configuration registers that define which interrupt source logically maps to I/O APIC INTx pins. In PIC mode, the PIIX4E provides a way to direct PCI interrupts onto one of the interrupt request levels 1-15. Note that this is only useful in compatibility mode since the redirected interrupts are not sourced on the outputs of the PIIX4.

3.6.2. Intel I/O APIC

For APIC mode, L440GX+ interrupt architecture incorporates the Intel I/O APIC device, to manage and broadcast interrupts to local APICs in each processor. The I/O APIC monitors interrupt requests from devices, and on occurrence of an interrupt sends a message corresponding to the interrupt via the APIC bus to each local APIC. The APIC bus minimizes interrupt latency time for compatibility interrupt sources, in both single and dual processor operation. The I/O APIC can also supply greater than 16 interrupt levels to the processor(s). The APIC bus consists of an APIC clock, and two bi-directional data lines.
L440GX+ APIC structure consists of a single I/O APIC device with 24 input interrupt requests. Compatibility interrupt levels 0 through 15 appear on inputs 0 through 15. The I/O APIC also manages 8 interrupt levels associated with PCI interrupts: PCI interrupts A through D are routed to APIC inputs 16 through 19. This supports more efficient interrupt processing. The PIIX4E also contains I/O APIC features that are not used in the L440GX+ platform.

3.6.3. Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on L440GX+. The actual interrupt map is defined using configuration registers in the PIIX4E and the I/O controller, and PCI to IRQ interrupt rerouter in the BUD. I/O Redirection Registers in the I/O APIC are provided for each interrupt signal, which define hardware interrupt signal characteristics for APIC messages sent to local APIC(s). Use the information provided in this table to determine how to program each interrupt.

Table 20: Interrupt Definitions

Interrupt	I/O APIC level	Description
INTR	INT0	Processor interrupt
NMI		NMI from BUD to processor
IRQ0	INT2	Timer interrupt from PIIX4
IRQ1	INT1	Keyboard interrupt
IRQ2		Interrupt signal from second 8259 internal to PIIX4
IRQ3	INT3	Serial port A or B interrupt from 87309VLJ device, user-configurable.
IRQ4	INT4	Serial port A or B interrupt from 87309VLJ device, user-configurable.
IRQ5	INT5	
IRQ6	INT6	Floppy disk
IRQ7	INT7	Parallel port
IRQ8_L	INT8	RTC interrupt
IRQ9	INT9	
IRQ10	INT10	
IRQ11	INT11	
IRQ12	INT12	Mouse interrupt
	INT13	
IRQ14	INT14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	INT15	Secondary IDE interrupt
INT_PCI1_L	INT16	PCI Interrupt signal A
INT_PCI2_L	INT17	PCI Interrupt signal A
INT_PCI3_L	INT18	PCI Interrupt signal A
INT_PCI4_L	INT19	PCI Interrupt signal A
INT_PCI5_L	INT 20	PCI Interrupt signal A – PCI Slot 5
INTB_L	INT 21	Shared PCI interrupt line B
INTC_L	INT 22	Shared PCI interrupt line C
INTD_L	INT 23_SMI_L	Shared PCI interrupt line D, System Management Interrupt

PCI Interrupt Rerouting

Some multiprocessor operating systems are unable to handle interrupts from PCI slots and devices as pure PCI interrupts, via inputs 16-23 (allocated to PCI) of the I/O APIC. Rather, they expect PCI interrupts to be delivered as ISA IRQs. Multiprocessor operating systems may also expect some interrupts from the PC-compatible PIC in the PIIX4, and others from the I/O APIC (Mixed Mode). Some device drivers check whether the device uses one of the traditional IRQs, and if not (when the PCI interrupt is connected directly to the I/O APIC), the driver fails to install or run properly. The PIIX4E performs internal PCI to IRQ interrupt steering so that PCI interrupts can be delivered to the PIC. However, the PCI interrupt steering feature is unidirectional, which means that it cannot redirect PCI interrupts to the I/O APIC.

For these reasons, L440GX+ incorporates an external PCI to IRQ rerouter circuit in the BUD, that can be programmed to pass PCI interrupts through to inputs 16-19 of the I/O APIC, or deliver a specific PCI interrupt to an ISA IRQ. Under software control, a PCI interrupt can be

individually rerouted to an ISA IRQ signal. This functionality is contained in the BUD and enabled in BIOS Setup under the “Advanced” Menu, “PCI IRQ to APIC Mapping-Enabled/Disabled”

Two 8-bit registers are provided in the rerouter circuit, with each nibble of a register controlling a specific PCI Interrupt line via PIO commands. The PIIX4E decodes the address of the PIO command and produces a chip select, which is controlled using the PIIX4E Programmable Chip Select Control register (78h - 79h). The rerouter uses only 2 bytes of the minimum 4 selectable, so aliases are provided.

3.6.4. System Management Interrupt Handling

The L440GX+ is designed to report these types of system errors: ISA bus, PCI bus, ECC memory, and System limit. Errors are reported by the BMC and PIIX4E using SMI_L. SMI is used for server management and advanced error processing. All errors can be intercepted by SMI for preprocessing (if SMI_L is enabled), or handled directly by NMI handlers. Some errors have to generate an NMI even if they are intercepted by the SMI, because the traditional way to handle errors in PC architecture is via the NMI. NMI/SMI handling logic in the BUD emulates non-ISA errors as ISA-compatible using NMI and SMI_L. Refer to “Server Management” later in this chapter for more information.

3.6.5. Basic Utility Device (BUD)

In addition to the PCI arbitration and interrupt rerouting functions described above, the BUD also gates and redirects SMI_L and NMI to generate SERR_L, and performs other miscellaneous logic functions (e.g., PCI arbitration expansion). The BUD contains an I/O mapped ISA interface for control of PCI-to-IRQ interrupt rerouting.

3.7. ACPI Power Management

The L440GX+ baseboard will be ACPI compliant as defined by the ACPI 1.0 and the PC97 specifications, ACPI covers more than just power management, but it is only the Power management aspect of the specification that affects the hardware implementation.

ACPI Global State Definitions

G0 - Working:
L440GX+ baseboard implications:
Full power to the system. The OS may halt one or both of the Processors by issuing a HALT instruction. BIOS should program the Processor to achieve the lowest possible power mode when in at a HALT instruction. The OS can also put embedded devices and plug-in controllers into a lower power mode if device driver allows this. OS idle policy could be set up to spin disk drives down to save additional power after long periods of idleness. This would increase the recovery latency if disk activity were required.

G1 - Sleeping:
L440GX+ baseboard implications
The baseboard will support both the S1 sleep state and the S4 sleep state. The baseboard will provide the means for the PIIX4 to send STPCLK to both processors, blank the console (already present as part of the security screen blank), and power down the system fans. Because the power supply will still be on and the processors will still be dissipating some power, the power supply and processor fans will be left on. The SCSI controller must supply a means for commanding the disk drives to power down, as they are a major consumer of power and a producer of noise. The hardware will provide a signal to the BMC so that the power LED can be blinked to indicate the system is in a sleeping state.

G2/S5 - Soft Off:
L440GX+ baseboard implications
System manually, or via Software, turned off without a save to disk

G3 - Mechanical Off:
L440GX+ baseboard implications
If the A/C cord is removed from the wall or power supply, 5V Standby will not be present on the baseboard. The only power remaining is that provided by the on board battery for the RTC function inside the PIIX4.

Table 21: Summary of Global Power States

Global System State	SOFTWARE RUNS	Latency	Power Consumption	OS restart required	Safe to disassemble computer	Exit state electronically
G0 – Working	Yes	0	Large	No	No	Yes
G1 – Sleeping	No	>0, varies with sleep state.	Smaller	No	No	Yes
G2/S5 – Soft Off	No	Long	Very near 0	Yes	No	Yes
G3 – Mechanical Off	No	Long	RTC battery	Yes	Yes	No

Note that the entries for G2/S5 and G3 in the Latency column of the above table are “Long.” This implies that a platform designed to give the user the appearance of “instant-on,” similar to a home appliance device, will use the G0 and G1 states almost exclusively (the G3 state may be used for moving the machine or repairing it).

ACPI Sleeping State Definitions

Sleep states (Sx states) are types of sleeping states within the global sleeping state, G1. The Sx states are briefly defined below.

S1 Sleeping State:
L440GX+ baseboard implications
Both processors are idle and the OS has placed one of the processors into a HALT state. The OS will then have the option of issuing an S1 or S4 sleeping state command. For entering an S1 sleeping state, the processor issues a command to the PIIX4 in order to cause STPCLK_L to be asserted (and optionally STP_L) to both processors thus placing the system into a G1/S1 state. The OS will have to mask off interrupts, in the PIIX4, so that the only way to wake the processor is via one of the predefined ACPI wake events. The OS should be able to blank the console with the exception of a visible LED, on the front panel, that blinks in order to indicate to the user that the system is sleeping. Prior to issuing the S1 command the OS should be able to spin down all disks, and stop all system fans so that, to the user, the system appears to be off. Stopping the fans should only be allowed if the system is not under thermal stress. Memory will only be refreshed. The criterion for an S1 sleeping state is that to the user, the system appears off.

S2 Sleeping State
L440GX+ baseboard implications

This state will NOT be supported on the L440GX+ baseboard.

S3 Sleeping State:
L440GX+ baseboard implications
This state will NOT be supported on the L440GX+ baseboard.

S4 - Non-Volatile Sleep:
L440GX+ baseboard implications
For entering the S4 sleeping state, much of the same activity will take place, except, the state of all the controllers and memory will be saved to disk before entering the S4 sleeping state. In the S4 sleeping state the power supply is turned off so only the 5V Standby voltage rail will be available to power the system board. All S4 sleeping state resume events have to be powered from 5V Standby. The OS could also be commanded to perform this operation via the front panel sleep button or from the user interface. The system can be manually woken up via the front panel power button, or, via one of the predefined ACPI wake events.

S5 Soft Off State:
L440GX+ baseboard implications
A system commanded off with no wakeup events enabled, has to be manually turned back on and the OS rebooted. Memory has not been saved to disk.

ACPI Processor Power State Definitions

Processor power states (Cx states) are processor power consumption and thermal management states within the global working state, G0. The Cx states are briefly defined below.

C0 Processor Power State:
While the processor is in this state, it executes instructions normally.

C1 Processor Power State
L440GX+ baseboard implications
Halt command executed.

C2 Processor Power State:
L440GX+ baseboard implications
This state will NOT be supported on the L440GX+ baseboard.

C3 Processor Power State:
L440GX+ baseboard implications
This state will NOT be supported on the L440GX+ baseboard.

3.7.1. Device Power State Definitions

Many devices do not have all of the four power states defined above. Devices may be capable of several different low power modes, but if there is no user-perceptible difference between the modes only the lowest power mode will be used. The *Device Class Power Management Specifications*, which are separate from this specification, describe which of these power states are defined for a given type (class) of device and define the specific details of each power state for that device class. For a list of the available *Device Class Power Management Specifications*, refer to the ACPI Specification.

D3 - Off:

L440GX+ baseboard implications

All embedded devices on the baseboard support this device power state, and it is required by ACPI as this is the state devices must be prepared to enter as part of the G1/S4 sleeping state.

D2:

L440GX+ baseboard implications

None of the embedded controllers on the baseboard support this device state.

D1:

L440GX+ baseboard implications

None of the embedded controllers on the baseboard support this device state.

D0 - Fully-On:

L440GX+ baseboard implications

All embedded PCI devices on the baseboard support this device state

Table 22: Summary of Device Power State

Device State	Power Consumption	Device Context Retained	Driver Restoration
D0 - Fully-On	As needed for operation.	All	None
D1	D0>D1>D2>D3	>D2	<D2
D2	D0>D1>D2>D3	<D1	>D1
D3 – Off	0	None	Full init and load

Note: Devices often have different power modes within a given state. Devices can use these modes as long as they can automatically switch between these modes transparently from the software, without violating the rules for the current D*x* state the device is in. Low power modes that affect performance, (i.e., low speed modes) or, that are not transparent to software, cannot be done automatically in hardware; the device driver must issue commands to use these modes

ACPI - PIIX4/BMC interaction

The BMC interacts with the PIIX4 to control the powering on and the powering off of the system. Essentially, all commands to power up and power down the system pass through the BMC and are then sent to the PIIX4. The BMC uses the PIIX4 power button input to accomplish this. Depending on how the PIIX4 has been programmed, the request to power down the system is handled by an ACPI OS, or, by the SMI handler for Non ACPI OS's. The net effect of a power down request is that the PIIX4 will assert the output SUSC_L. The BMC will look for this signal and shall control the power supply signal PS_ON appropriately. To power up the system, the BMC will assert the power button input to the PIIX4 and wait for the PIIX4 to de-assert the SUSC_L signal. When the signal is de-asserted the BMC will turn on the power supply by using the PS_ON signal. Note that the system can be turned on and off by events that are not under the control of the BMC, therefore, the BMC must only use the SUSC_L signal as the source of a power on/off request. Note that the BMC when in secure mode should block the generation of the power button signal to the PIIX4 but not block the SUSC_L signal.

Power on events

The following events should be able to cause the PIIX4 to issue a system wake up, even if the OS is a non-ACPI OS.

- Wake-On-LAN header (used by an add-in card).
- A COM 2 Ring indicator can be provided as a build option to replace Wake-On-LAN.
- PCI_PME (used by the embedded LAN controller).
- RTC - Note that if the PIIX4 observes a loss and restore of A/C power, any RTC wakeup command programmed into the PIIX4 will be lost.

The BMC can cause a system Wake up via:

- The SMM port.
- A command on the IMB bus.
- A command over the Emergency Management Port (or Ring Indicator if the EMP is disabled).
- A front panel power button.
- A restoration of A/C power if the system was ON prior to losing A/C power.

ACPI - PIIX4 Wake/Resume events

In order to comply with the ACPI wake/resume programming model, the PIIX4 contains two registers that control system wake up. The two registers are the Power Management Resume Enable Register (Base+02h) and the General Purpose Enable Register (base+0Eh). These two registers map to the ACPI defined registers PM1a_EVT_BLK and GPE0_EN. Note that any resume event must be able to cause a SCI.

The legal PIIX4 inputs for resume/wake events are RI, LID, GPI1, THRM and PWRBTN#. USB activity can only be used for a S1 resume, not a S4 wakeup. USB activity can only be detected if the system is already powered up and the system provides power to the USB peripherals and the USB logic is not on the PIIX4 resume Power well i.e. on 5V Standby. The RTC can only cause a S4 wake up and not a resume event as it does not cause a SCI. In the G1/S1 state the BMC will not assert PWRBTN as it is already asserted. Therefore, use of RI, RTC and USB for resume events will not work. The BMC will be connected to the LID input so that it can cause a S4 wake up and a S1 resume event.

G1/S1 resume Events

The number of events that can be used to resume to system from a G1/S1 to a G0/S0 state is very limited. Theoretically, all the S4 Wake-up events except USB activity can also be S1 resume events. In practice Wake-On-LAN has been defined as a S4 wake event and thus, normal LAN traffic will not cause a resume event unless the NIC controller can be programmed to cause a PCI_PME_L assertion. This also applies to the modem RI unless the modem board is a PCI modem and supports the assertion of PCI_PME_L on detection of a RI, then it cannot wake up the system.

ACPI - System Control Interrupt (SCI)

The SCI is used to replace SMI in all possible situations. As Microsoft* Windows* NT* Operating System has mandated. The SCI will have special abilities and can be generated by predefined activity detected within the PIIX4. The SCI comes out of the PIIX4 GPO29 pin (B3) and will be connected to the IRQ9 input of the IOAPIC and PIIX4. The IOAPIC will have to be programmed to look for an active low input. As the signal is active high, IRQ9 cannot be shared with any other ISA device and has to be dedicated to the SCI. In a uni-processor non-

APIC based system, the SCI is connected to the internal IRQ9 of the PIIX4. IRQ9 must be programmed for high level sensitive. This is done with the ELCR2 register.

When IRQ9 is being used for the SCI, the signal has to be removed from the ISA slots. This will be accomplished by logic on the baseboard controlled by a PIIX4 GPIO (General Purpose I/O) bit.

NIC Wake-On-LAN will be connected to RI so that it can wake the system up from a S4 state. The COM2 Ring indicator goes to the BMC so it will be able to wake from a S4 state on a Modem ring via the PWRBTN or wake from a S1 state via the BMC/LID connection.

3.8. Server Management

On L440GX+, three serial buses that follow IMB protocol provide independent pathways for server management functions. The PIIX4e system management bus mentioned above (PIIX4e SMB) connects with each DIMM, and controls SDRAM clocks and processor speed configuration. A single microcontroller referred to as the Baseboard Management Controller (BMC) manages the other two IMB segments:
Server Management Bus supporting 8K SEEPROM and processor/baseboard temperature sensors.
Intelligent Management Bus (IMB) supporting connectors to system-wide server management devices.
In addition, the BMC manages sensors directly using I/O and ADC lines, controls the Emergency Management Port (EMP), detects and reports system fan failures, and manages Fault Resilient Booting (FRB). The BMC provides the Host ISA and IMB interfaces to server management features on L440GX+. The following diagram illustrates server management architecture on the L440GX+ baseboard.

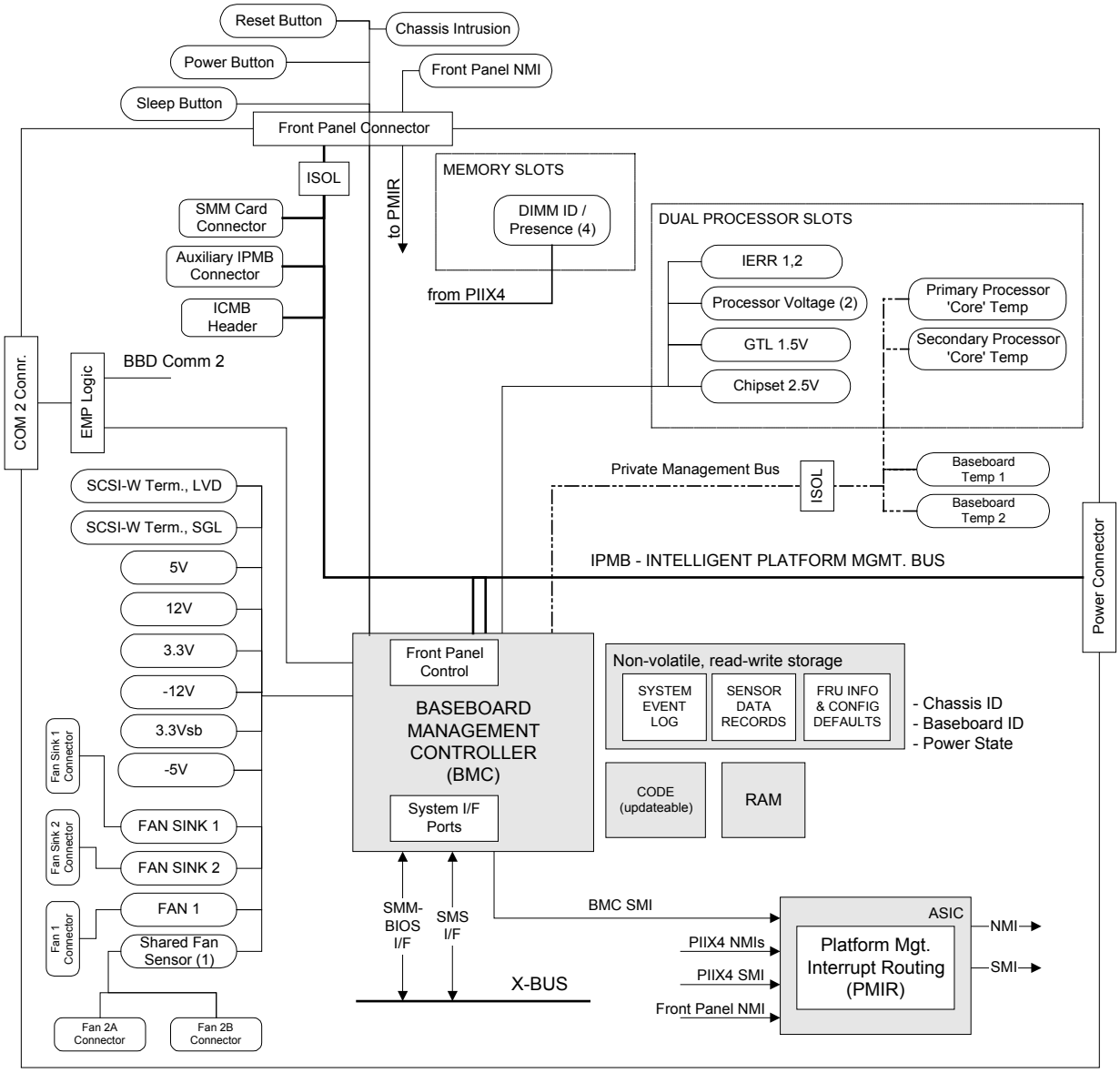


Figure 18. L440GX+ Server Management Block Diagram

3.8.1. Server Management Bus

The Server Management Bus (SMB) is a single master, open-drain, serial bus that is electrically and timing compatible with the 100 Kbps version of the IMB bus specification. The SMB extends throughout the baseboard providing an independent pathway for the BMC to communicate with 4 baseboard and two processor slot temperature sensors. In addition, the SMB supports an 8K SEEPROM device for non-volatile storage of the System Event Log (SEL), Sensor Data Record Repository (SDRR), FRU information, and configuration defaults. The BMC controls access to this device and manages the data structures within (refer to BMC description below). Buffers are provided to isolate the baseboard and processor temperature sensors from the rest of the SMB. These buffers, running on 5V_Standby, keep the bus alive to the BMC even though main power is switched off. This allows the BMC to communicate with its SEEPROM at all times.

3.8.2. Intelligent Management Bus

The Intelligent Management Bus (IMB) is a multi-master, open-drain, serial bus which is also electrically and timing compatible with the 100 Kbps version of the IMB bus specification. The IMB attaches to connectors on the baseboard creating a server management network that extends throughout the baseboard and system chassis, providing an independent pathway for communications between the BMC and system-level server management devices (e.g., Hot-swap SCSI controller). In addition, the IMB provides interchassis communications extensions for a complete server management network solution.
The protocol is designed to work with microcontrollers and other IMB masters, and slave devices such as IMB temperature sensors.
The IMB attaches to the following connector interfaces on the L440GX+ baseboard:

- Auxiliary IMB connector
- Server Monitor Module (SMM) card feature connector
- Front panel connector
- Auxiliary power connector (via isolation buffer)

Following are definitions of Aux. IMB, SMM card, Aux. Power and Main Front Panel connectors.

Auxiliary IMB Connector (Location J4J1)

The auxiliary IMB connector has the following pin-out.

Table 23: Auxiliary IMB Connector Pin-out

Pin	Signal
1	Local IMB SCL
2	GND
3	Local IMB SDA

Caution: A shorted IMB connection at the auxiliary IMB connector will disrupt proper operation of the IMB.

Front Panel Connector (Location J5J1)

A 16-pin header is provided that attaches to the system front panel, which contains reset, NMI, and power control switches, LED indicators, as well as the IMB connection. The connector has the following pinout:

Table 24: Front Panel Connector Pinout

Pin	Signal	Pin	Signal
1	GND	2	Hard disk activity LED
3	Front panel reset switch	4	Front panel power switch
5	+5V	6	nc (key)
7	Front panel NMI switch	8	+5V
9	Fan failure indicator LED	10	Chassis intrusion switch
11	Power fault LED	12	+5V standby
13	IMB Data line	14	GND
15	IMB Clock line	16	GND

3.8.3. Baseboard Management Controller (BMC)

On L440GX+, all server management functionality formerly distributed between 3 controllers is concentrated in the BMC. The BMC and associated circuitry are powered from 5V_Standby, which remains active when system power is switched off. The BMC is implemented using a Dallas Semiconductor* DS82CL10 (or equivalent) microcontroller. The primary function of the BMC is to autonomously monitor system platform management events, and log their occurrence in the non-volatile SEL (System Event Log). These include events such as over-temperature and over-voltage conditions, fan failure, or chassis intrusion. While monitoring, the BMC maintains the non-volatile SDRR, from which run-time information can be retrieved. The BMC provides an ISA host interface to SDRR information, so software running on the server can poll and retrieve the current status of the platform. A shared register interface is defined for this purpose. The SEL contents can be retrieved after system failure, for analysis by field service personnel using system management tools, such as Intel® Server Control. Since the BMC is powered by 5V_Standby, SEL (and SDRR) information is also available via the IMB. L440GX+ provides an Emergency Management Port (EMP), which allows remote access to the SEL and other features using the COM2 port. During its watch, the BMC performs the following functions:

- Baseboard temperature and voltage monitoring
- VID Bit reading
- Processor presence monitoring and FRB control
- Baseboard and Processor fan failure detection and indicator control
- SEL interface management
- SDR Repository interface management
- SDR/SEL timestamp clock
- Baseboard Field Replaceable Unit (FRU) information interface
- System management watchdog timer
- Periodic SMI timer
- Front panel NMI handling
- Event receiver
- ISA host and IMB interface management
- Secure mode control, video blank and floppy write protect monitoring and control, front panel lock/unlock initiation.
- Sensor event initialization agent
- Wake-on LAN (WOL) via Magic Packet support
- ACPI Support

A Server Management Card, such as the Intel LANDesk™ SMM card, can obtain the SEL and make it remotely accessible using a LAN or telephone line connection.

BMC Front Panel Control

The BMC performs all front panel controller functions on L440GX+. These include control of system power, hard-resets, and the power failure LED. The BMC drives system power-on/off or hard reset from the following sources:

- Front panel push-button
- SMM card feature connector signal (controlled by secure mode)
- Transition of PIIX real-time clock alarm/suspend signal
- Command from IMB via front panel connector, aux. IMB, or SMM card
- Magic Packet signal from NIC
- Command from EMP
- Command from ISA interface
- BMC watchdog timer

Secure Mode

The BMC monitors the SECURE_MODE signal from the baseboard keyboard controller. When the system is powered up, and SECURE_MODE asserted, the BMC prevents power off or reset via the front panel power and reset pushbuttons. A 'Secure Mode Violation Attempt' event is flagged by the BMC whenever a front panel pushbutton is pressed. The BMC also provides options for blanking the onboard video, and write-protecting the onboard floppy interface when Secure Mode is active.

Power Fault LED

The BMC controls the front panel Power Fault LED signal. The BMC asserts this signal whenever it attempts to power on the system without success, and when the BMC detects a power supply failure. The BMC can also be directed to assert this signal via an IMB 'Force Power Fault LED On' command.

3.8.4. Emergency Management Port (EMP)

The COM2 serial port on L440GX+ can be configured for use as an Emergency Management Port (EMP). EMP provides a level of system management via RS-232 during powered-down, pre-boot, and post-boot situations. This allows system management software (SMS) interactions via point-to-point RS-232 connections, or external modem. EMP provides access to these basic management features:

- System power up
- System power down (Not available in restricted mode).
- System Reset (Not available in restricted mode).
- NMI control (Not available in restricted mode).
- Access to the System Event Log, FRU, and Sensor Data Records.
- Access to BIOS Console Redirection.
- Password Protection

The COM2 port can be used on L440GX+ for three different purposes: EMP, console redirection, or normal COM usage. If the BMC is using the port for EMP purposes, it is unavailable to the BIOS or SMS during this mode. If the System BIOS is using the port for console redirection, it is unavailable to the BMC or SMS (since the machine is still doing POST). Under normal usage COM2 appears to the OS as a normal serial port; in this case the BMC and System BIOS cannot use the port.

L440GX+ EMP architecture supports several remote access modes, selectable using the F2 BIOS Setup Screen, as follows:

- **Pre-boot only mode** - The EMP is only available while the machine is powered off and during POST. Just prior to booting the OS, the System BIOS disables the EMP by sending a command to the BMC. COM2 is then available as a normal serial port.
- **SMS activated mode** - Essentially the same as Pre-boot only, except that SMS software may elect to take ownership or release control of COM2. This mode allows SMS to configure the system for remote access.
- **Always active mode** - EMP and Console Redirect are available under the same conditions as listed in #1 above. However, the System BIOS leaves the port enabled for run-time EMP and SMS usage. The BIOS configures the hardware such that the O/S can not "see" the port.
- **Always disabled mode** - EMP and Console Redirection are not available under any conditions.

- **Restricted mode -** This option can be selected in conjunction with either the 'Pre-boot Only' or 'Always Active' modes listed above, using the BIOS setup interface. When activated, Power Down control, Front Panel NMI, and Reset Control via the EMP are disabled. Power On control, System Event Log access, FRU Inventory, and Sensor Data Repository access remain enabled. Console redirection operation is unaffected by Restricted Mode.

EMP Password

The EMP is intended for use in a secure environment. A simple password can be configured to provide a rudimentary level of security on the interface. System configuration options can be used to disable this interface. The BMC implements a simple password mechanism for the EMP, activated by BIOS setup. If the password is active, a correct password must be received on the EMP before any other commands are accepted. The password must be entered every time COM2 is switched over to EMP operation. It must also be re-entered if the EMP has been inactive for more than 30 seconds. Only BIOS setup can set or clear the password, it cannot be changed remotely.

3.8.5. Fault Resilient Booting

The BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If two processors are installed and the processor designated as the BSP (Bootstrap Processor) fails to complete the boot process, FRB attempts to boot the system using the alternate processor.
FRB level 1 is for recovery from a BIST (Built-in Self-Test) failure detected during POST. This FRB recovery is fully handled by BIOS code.
FRB level 2 is for recovery from a Watchdog timeout during POST. The Watchdog timer for FRB level 2 detection is implemented in the BMC.
FRB level 3 is for recovery from a Watchdog timeout on Hard Reset / Power-up.
Hardware functionality for this level of FRB is provided by the BMC on the processor subsystem. FRB-3 is managed by the BMC, which controls the ability to boot using either processor in the event of a catastrophic processor failure. On power up, a timer starts that can only be stopped by a healthy processor using the GPIO bit, FRB_TMRHLT_L, on the PIIX4. If processor 0 fails to halt the FRB timer before timeout, the controller asserts STOP_FLUSH to the processor and asserts FRB_RST_L for 10ms. When the system comes out of reset, processor 0 is prevented from acting as the BSP, allowing the other processor to take over the boot process. Setting the "Processor Retest" option in BIOS setup clears FRB level 3 errors.

3.8.6. System Fan Interface

The L440GX+ provides five 3-pin, shrouded, and keyed fan connectors. Two of these connectors, located next to each processor card on the baseboard, are for processor fansinks. The remaining three connectors on the baseboard attach to chassis fans equipped with a sensor that indicates whether the fan is operating. The sensor pins for these fans are routed to the BMC for failure monitoring.

The ISP2150 utilizes two fans for cooling connected to headers J6G1 and J1J1. The connector has the following pinout:

Table 25: Fan Connector Pinout

Pin	Signal
1	GND
2	+12V
3	Fan Sensor

4.0 Configuration and Initialization

This chapter describes the initial programming environment including address maps for memory and I/O and hardware options configuration.

4.1. Memory Space

At the highest level, Pentium® II / Pentium® III processor address space is divided into 4 regions, as shown in the following figure. Each region contains subregions, as described in following sections. Attributes can be independently assigned to regions and subregions using 440GX registers.

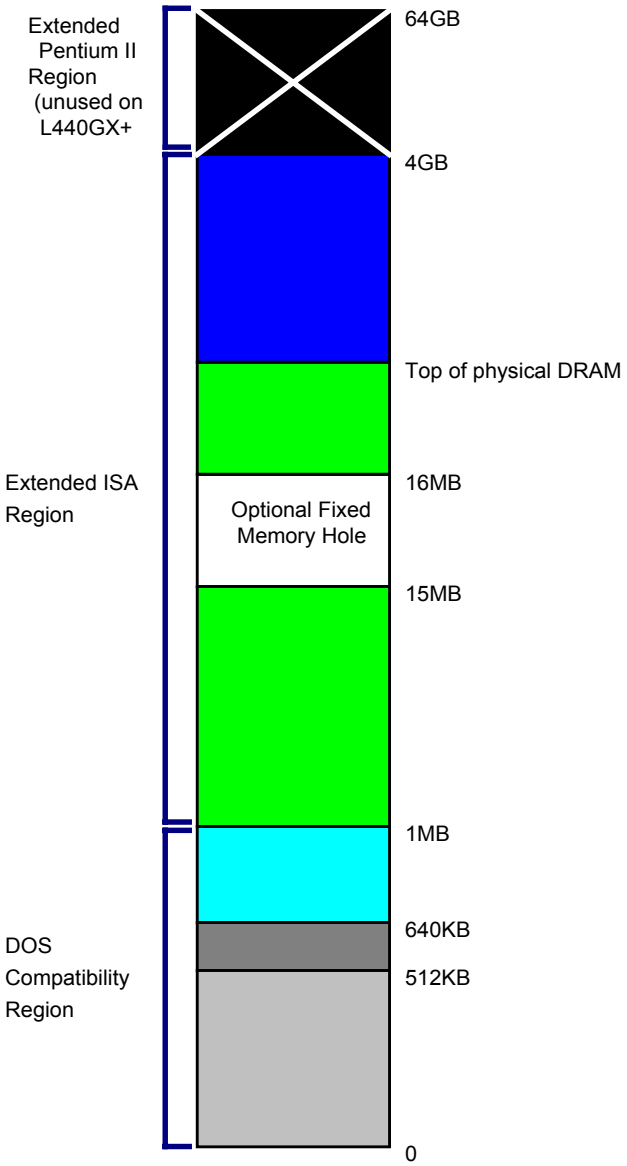


Figure 19. Pentium II /Pentium® III Processor Memory Address Space

4.1.1. DOS Compatibility Region

The first region of memory below 1 MB was defined for early PCs, and must be maintained for compatibility reasons. This region is divided into subregions as shown in the following figure.

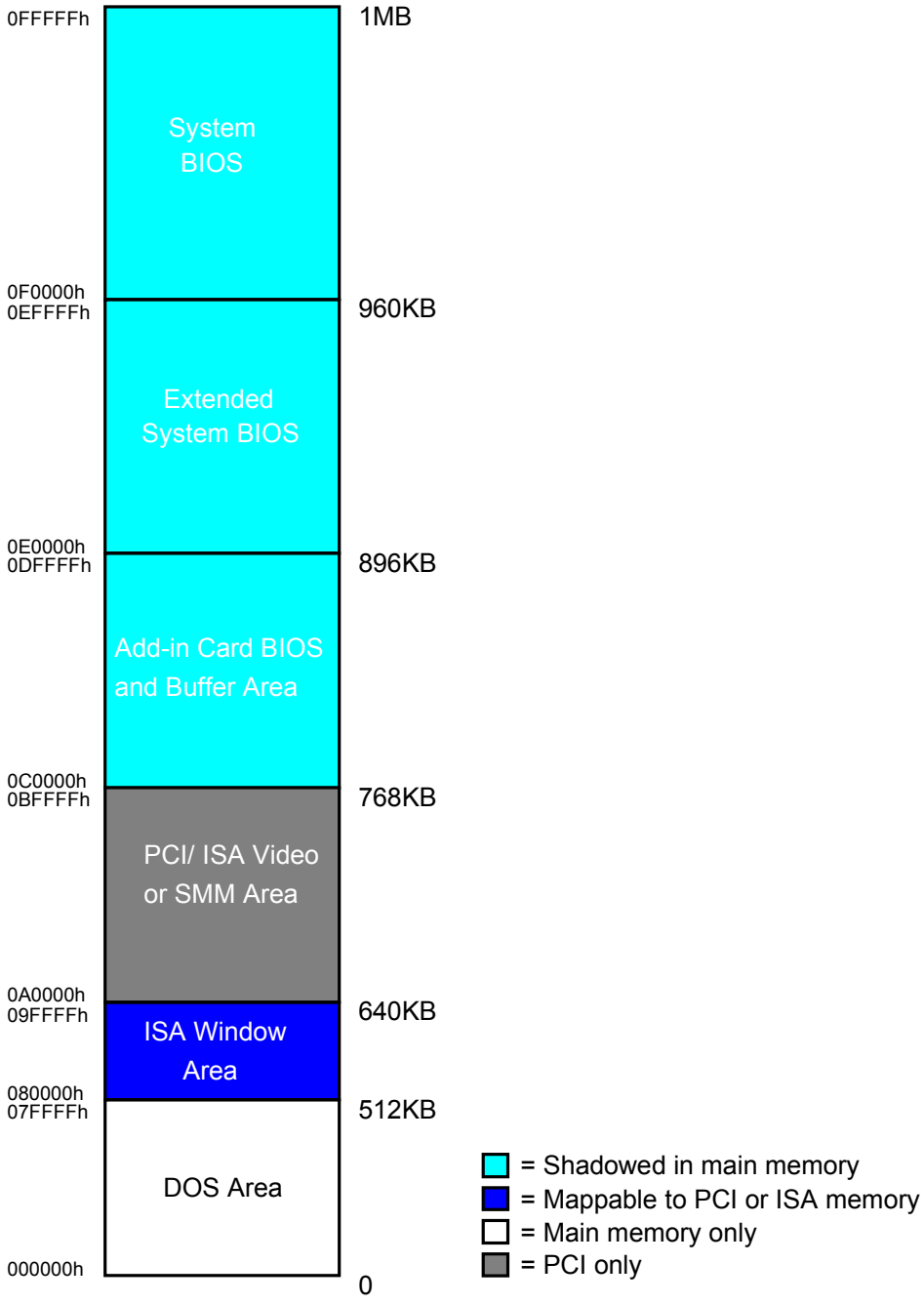


Figure 20. DOS Compatibility Region

DOS Area

The DOS region is 512 KB in the address range 0 to 07FFFFh. This region is fixed and all accesses go to main memory.

ISA Window Memory

The ISA Window Memory is 128 KB between the addresses of 080000h to 09FFFFh. This area can be mapped to the PCI bus or main memory.

Video or SMM Memory

The 128 KB Graphics Adapter Memory region at 0A0000h to 0BFFFFh is normally mapped to the VGA controller on the PCI bus. This region is also the default region for SMM space**.

Add-in Card BIOS and Buffer Area

The 128 KB region between addresses 0C0000h and 0DFFFFh is divided into eight segments of 16 KB segments mapped to ISA memory space, each with programmable attributes, for expansion card buffers. Historically, the 32 KB region from 0C0000h to 0C7FFFh has contained the video BIOS location on a video card. However, on L440GX+, the video BIOS is located in the Extended BIOS or System BIOS areas. This region can be used for extended SMM space**.

Extended System BIOS

This 64 KB region from 0E0000h to 0EFFFFh is divided into 4 blocks of 16 KB each, and may be mapped with programmable attributes to map to either main memory or to the PCI bus. Typically, this area is used for RAM or ROM. This region can also be used for extended SMM space**.

System BIOS

The 64 KB region from 0F0000h to 0FFFFFh is treated as a single block. By default this area is normally Read/Write disabled with accesses forwarded to the PCI bus. Through manipulation of R/W attributes, this region can be shadowed into main memory. This region can also be used for extended SMM space**.

** Refer to “System Management Mode Handling,” later in this chapter.

4.1.2. Extended Memory

Extended memory on L440GX+ is defined as all address space greater than 1 MB. The Extended Memory region covers 4 GB of address space from addresses 0100000h to FFFFFFFFh, as shown in the following figure.

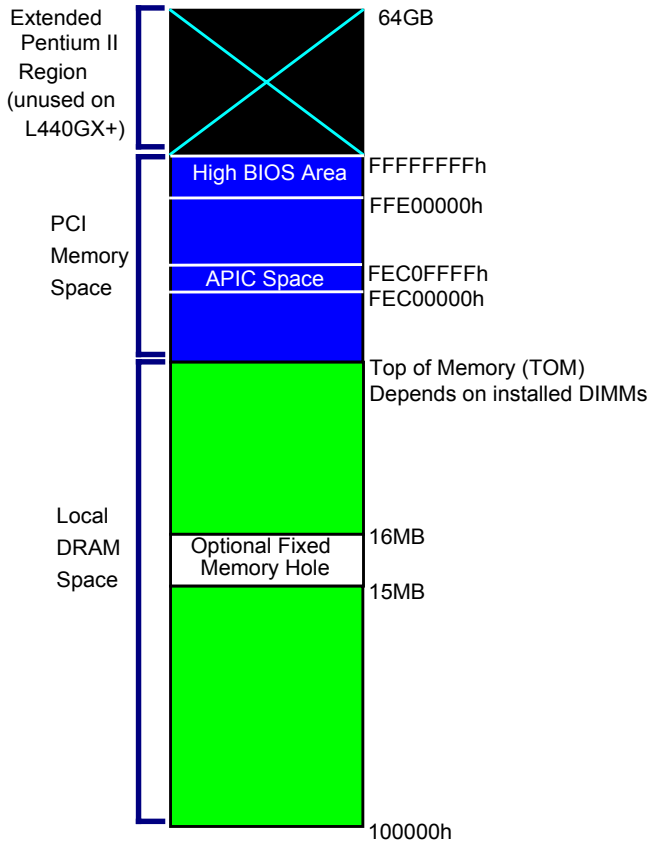


Figure 21. Extended Memory Map

Main Memory

All installed DRAM greater than 1 MB is mapped to local main memory, up to the top of physical memory which is located at 2 GB. Memory between 1 MB to 15 MB is considered to be standard ISA extended memory. 1 MB of memory starting at 15 MB can be optionally mapped to the PCI bus memory space.

The remainder of this space, up to 2 GB, is always mapped to main memory, unless Extended SMRAM is used, which limits the top of memory to 256MB. Refer to “System Management Mode Handling” below for more information.

PCI Memory Space

Memory addresses in the 2 GB to 4 GB range are mapped to the PCI bus. This region is divided into three sections: High BIOS, APIC Configuration Space, and General-purpose PCI Memory.

The General-purpose PCI Memory area is typically used for memory-mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers.

High BIOS

The top 2 MB of Extended Memory is reserved for the system BIOS, extended BIOS for PCI devices, and A20 aliasing by the system BIOS. The SECC PENTIUM II processor begins executing from the High BIOS region after reset. Only 256 KB of this area is actually required by the BIOS, but 2 MB is required by SECC PENTIUM II processor MTRR programming.

I/O APIC Configuration Space

A 64 KB block located 20 MB below 4 GB (0FEC00000h to 0FEC0FFFFh) is reserved for the I/O APIC configuration space.

Extended System Management RAM Space

The 440GX chip supports placement of System Management RAM (SMRAM) space in cacheable memory above 1MB. Extended SMRAM consists of up to 2MB of physical memory, located at the top of installed memory (up to 256MB boundary). This region is aliased to memory addresses below 1MB. Refer to “System Management Mode Handling”, later in this chapter.

Extended Pentium Pro Processor Region (above 4 GB)

A Pentium® II / Pentium® III processor-based system can have up to 64 GB of addressable memory. However, the 440GX only supports 32-bit addressing, with the BIOS operating in 4 GB of address space (the DIMMs provide up to 512 MB of main memory). All accesses to the region from 4 GB to 64 GB are claimed by the 440GX and terminated. Write data is dropped and zeroes are returned on reads.

4.1.3. Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into main memory. Typically, this is done to allow ROM code to execute more rapidly out of RAM. ROM is designated read-only during the copy process while RAM at the same address is designated write-only. After copying, the RAM is designated read-only and the ROM is designated write-only (shadowed). Processor bus transactions are routed accordingly. Transactions originated from the PCI bus or ISA masters and targeted at shadowed memory blocks will not appear on the processor's bus.

4.1.4. System Management Mode Handling

The 440GX supports System Management Mode (SMM) operation in standard (compatible) mode, and special extended modes. System Management RAM (SMRAM) provides code and data storage space for the SMI_L handler code, and is made visible to the processor only on entry to SMM, or other conditions which can be configured using 440GX PCI registers. The 440GX supports three flavors of SMRAM: Compatible SMRAM, located in main memory below the 1MB boundary at addresses 000A0000h through 000B0000h. This region is non-cacheable.
High SMRAM, which exists in physical memory above the 256MB boundary, and is write-back cacheable. The High SMRAM region is aliased to A0000h through FFFFF. Extended

SMRAM, providing up to 1MB at the top of main memory (TSEG) which is also cacheable. Use of extended SMRAM forces the upper limit of installed memory to 256MB.

The 440GX determines the nature and location of SMRAM space using the SMRAM Control (72h) and Extended SMRAM Control (73h) configuration space registers. Refer to Chapter 5 for more information.

4.2. Hardware Jumper Configuration

This section describes how to configure hardware jumper options on the baseboard for the following:

- System configuration
- Internal/external speaker selection
- Jumper locations and designations are marked on the baseboard, refer to the layout diagram in Chapter 1 for placement information.

4.2.1. System Configuration Jumpers

15-pin (J2J1 on the baseboard) and 11-pin (J3J1 on the baseboard) single inline headers provide seven 3-pin jumper blocks that control various configuration options, as shown in the figure below. The shaded areas show default jumper placement for each configurable option.

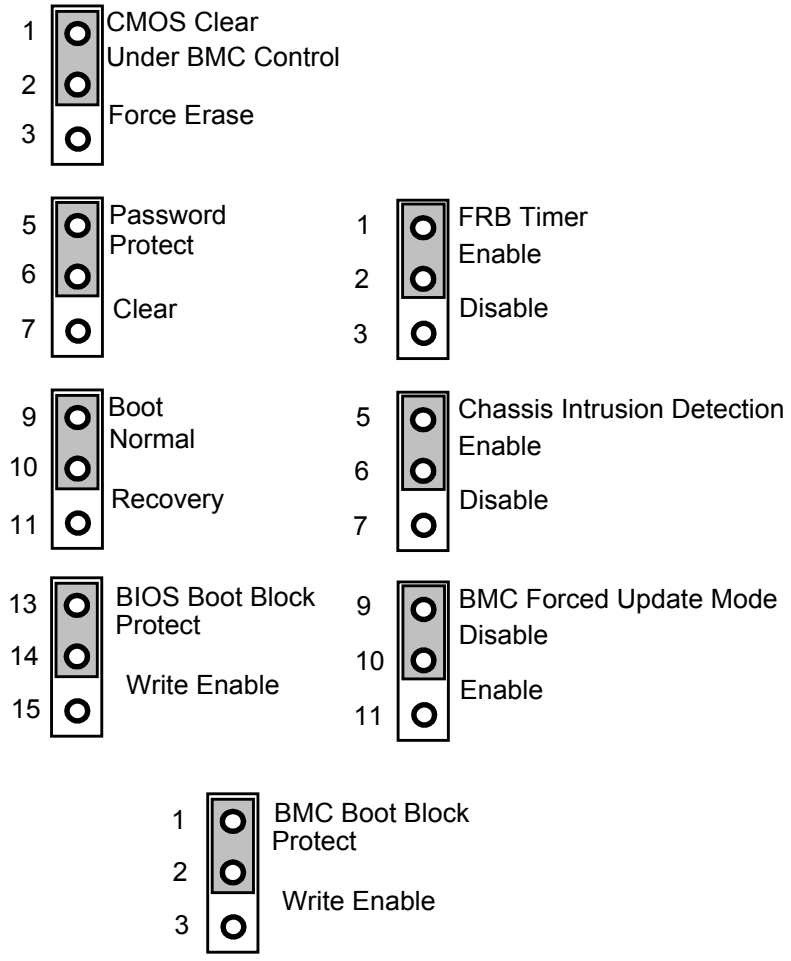


Figure 22. System Configuration Jumpers

The following table describes each system configuration jumper option.

Table 26: System Configuration Jumper Options

Option	Description
CMOS Clear	If pins 1 and 2 are jumpered (default), preservation of configuration CMOS through system reset is controlled by the BMC. If pins 2 and 3 are jumpered, CMOS contents are set to manufacturing default during system reset.
Password Clear	If pins 5 and 6 are jumpered (default), the current system password is maintained during system reset. If pins 6 and 7 are jumpered, the password is cleared on reset.
Recovery Boot	If pins 9 and 10 are jumpered (default) the system will attempt to boot using the BIOS programmed in the Flash memory. If pins 10 and 11 are jumpered, the BIOS will attempt a recovery boot, loading BIOS code from a floppy disk into the Flash device. This is typically used when the BIOS code has been corrupted.
BIOS Boot Block Write Protect	If pins 13 and 14 are jumpered (default), the BIOS boot block is write-protected. If pins 14 and 15 are jumpered, the boot block is erasable and programmable. ***WARNING: Incorrect programming of the boot block will render the system unbootable.***
FRB Timer Enable	If pins 1 and 2 are jumpered (default), FRB operation is enabled, which allows the system to boot from processor 1 if processor 0 fails. If pins 2 and 3 are jumpered, FRB is disabled.
Chassis Intrusion Detection	If pins 5 and 6 are jumpered (default), a switch installed on the chassis will indicate when the cover has been removed. If pins 6 and 7 are jumpered, the chassis intrusion switch is bypassed.
BMC Forced Update Mode	If pins 9 and 10 are jumpered (default), firmware status is maintained as is, and operational code will run. If pins 10 and 11 are jumpered, the system is placed into "Forced Update Mode." Only a minimal set of ISA and BMC functions are available. The system is forced to update firmware. ***WARNING: The system must have A/C power removed before moving any system jumpers.***
BMC Boot Block Write Protect	If pins 1 and 2 are jumpered (default), the BMC boot block is write-protected. If pins 2 and 3 are jumpered, the boot block is erasable and programmable. ***WARNING: Incorrect programming of the boot block will render the system unbootable.***

4.2.2. Speaker Circuit Jumper/Connector

A 4-pin block on the 19 pin single inline header labeled J6J1, provides a way to plug in an external speaker or, by jumper, enable the onboard speaker. The configuration is shown in the figure below.

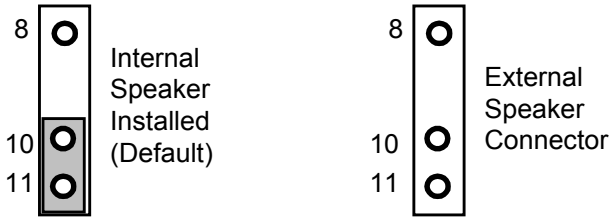


Figure 23. Speaker Circuit Jumper

4.2.3. Wake On LAN Jumper

The jumper at location J5A2 is used to enable/disable the Wake On LAN functionality of the on board network controller. By default the board is shipped with this option enabled. See Figure 3-6. If a power supply is used that does not provide 0.8A of +5 volt Stand-by, this option should be disabled.

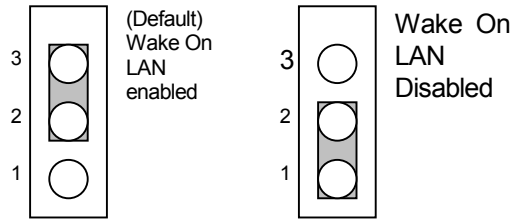


Figure 24. Wake On LAN Jumper (J5A2)

5.0 System BIOS

This chapter describes those features of the system BIOS that are unique to the L440GX+ server board.

Note: The ISP2150 platform does not provide legacy support USB. Legacy mode of USB keyboard emulating a PS/2 keyboard via SMM is not supported on L440GX+. While devices such as USB keyboards work with OS drivers, these keyboards do not respond during BIOS POST.

5.1. Security Features

The BIOS provides a number of security features. This section describes the security features and operating model.

5.1.1. Operating Model

The following table summarizes the operation of security features supported by the BIOS. CU in the following table refers to BIOS Configuration Utilities, which include BIOS Setup and System Setup Utility (SSU)-

Table 27: Security Features Operating Model

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Secure mode	Keyboard Inactivity Timer, Runtime activation of Key Board Controller Hotkey	User Password enabled in BIOS Setup	Screen goes blank (if enabled in CU). Floppy writes are disabled (if selected in CU). Power and Reset switches on the front panel are disabled (if enabled in Setup). No mouse or keyboard input is accepted.	User Password	Video is restored. Floppy writes are enabled. Power and Reset switches are enabled. Keyboard and mouse inputs are accepted.
Secure boot	Power On/Reset	User Password and Secure Boot Enabled in CU	Enter secure mode. Prompts for Password, if booting from drive A. Video is blanked (if enabled in Setup). Floppy writes are disabled (if programmed in CU). Power and Reset switches on the front panel are disabled(if programmed in CU). No mouse or keyboard input is accepted; however, the Mouse driver loads before a password is required. If booting from drive A, and the user enters correct password, the system boots normally.	User Password	Floppy writes are enabled. Power and Reset switches are enabled. Keyboard and mouse inputs are accepted. System attempts to boot from drive A. If the user enters correct password, and drive A is bootable, the system boots normally
Password on boot User Password boot (AT style)	Power On/Reset	User Password set and password on boot enabled and Secure Boot Disabled in CU	System halts for User Password before booting. The system is not in secure mode. Video is blanked (if enabled in CU). Floppy writes are disabled (if programmed so by CU). No mouse or keyboard input is accepted.	User Password	Keyboard and mouse inputs are accepted. The system boots normally. Boot sequence is determined by CU options.
Diskette Access	Power On/Reset	Set feature to Admin in CU	User is prevented from accessing the floppy drive. Administrator is always prevented from accessing the floppy drive.	Set feature to User in CU	User is allowed to access the floppy drive.

Password Protection

Through the use of passwords, the BIOS prevents unauthorized tampering with the system. Once secure mode is enacted, access to the system is allowed only after you have entered the correct password(s). Each of two passwords, for User and Administrator, can be created during system configuration using the CU (Configuration Utilities). An individual that may be doing maintenance to the server system uses the User password. An individual that may be changing the configurations to the server system in BIOS Setup uses the administrator password.

Once secure mode is enacted, access to the system is allowed only after you have entered the correct password. Each password, User and Administrator, can be created during system configuration using the CU. Once set, a password can be disabled by changing it to a null string. The User password can still modify the time and date, but other fields can only be modified if the Administrator password is entered. For example, system hardware configuration can be controlled by the User password, while Administrator control access to the machine's file system. If only an administrator password is set (no User password), this password is requested when entering Setup and must be entered before the majority of the fields can be modified. If only the User password is set (no administrator password), the User password must be entered to access Setup, but all fields can be modified once entered. Once set, a password can be disabled by changing it to a null string.

Inactivity timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified time-out period, the following occurs until the User password is entered:

- Keyboard and mouse input is disabled
- Video is blanked (if programmed in CU)
- Floppy drive is write protected (if enabled)
- Front panel reset and power switches are locked (if enabled)

Hot key activation

A Hotkey combination can activate secure mode immediately, rather than having to wait for the inactivity time-out to expire. The Hotkey combination is set using the CU. The following keys are valid hot keys: A-Z, 0-9.

Password clear switch

The BIOS determines if the password clear jumper is set. If set, all passwords are cleared from CMOS and password protection is disabled.

Floppy Write Protection

If enabled by the CU, floppy disk writes are blocked from anyone accessing it when the system is in secure mode. Floppy write protection is only in effect while the system is in secure mode. Otherwise, write protection is disabled and writes are then enabled.

Power Switch and Reset Button Lock

If enabled by the CU, the power switch and reset button are disabled when in secure mode.

Secure Boot (Unattended Start)

Secure Boot allows the system to boot and run the OS. However, until the User password is entered, mouse and keyboard input is not accepted and the front panel reset/power switches are disabled. The CU is used to place the system into secure boot mode. In secure boot mode, if the BIOS detects a floppy disk in the A drive at boot time, it prompts the User for a password. When the password is entered, the system can boot from the floppy and secure mode is disabled. Any one of the secure mode triggers cause the system to go back into secure mode. If there is no disk in drive A, the system boots from the next boot device and is placed in secure mode automatically. All of the enabled secure mode features go into effect at boot time.

5.1.2. Interaction with External Utilities

External utilities that need to perform password validation, such as SSU, can call the appropriate BIOS interface. The BIOS performs the password validation and returns the status. The interface is not described here for security reasons.

5.2. Auto-Configuration Features

The BIOS provides support for auto-configuration of the following:

- Plug and Play
- Processor speed
- SMP initialization
- Memory sizing
- Boot drive selection
- Mouse and keyboard swapping
- Pentium® III processor BIOS update

Plug and Play

The BIOS supports the following industry standards for full Plug and Play capabilities:

- Plug and Play (PnP) ISA specification
- Desktop Management Interface (DMI) BIOS specification
- Extended System Configuration Data Specification (EISA is not supported).
- PCI local Bus specification

Resource allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel servers. The BIOS scans for the following, in order:

1. Off board PCI devices: If found, the BIOS initializes and allocates resources to these devices.
2. On board Video, IDE, and SCSI devices: If equivalent functionality is not found off board, the BIOS allocates resources according to the parameters set up by the SSU.

PnP ISA auto-configuration

The BIOS:

- Fully supports the PnP ISA protocol
- Reads the PnP ISA configuration port
- Assigns the system I/O, memory, DMA channels, and IRQs from the resource pool
- The Super I/O chip is an example of a PnP ISA device.

PCI auto-configuration

The BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the PCI specification, Rev. 2.1. BIOS also supports the 16 and 32-bit protected mode interfaces as required by the PCI BIOS specification. System POST performs auto-detection and auto-configuration of ISA, ISA Plug-N-Play, and PCI devices. This process maps each device into memory and/or I/O space, and assigns IRQs and DMA channels as required, so that there are no conflicts prior to booting the system. BIOS scans the PCI devices on each PCI bus in low to high sequence. The PCI busses are also scanned in the same order. The BIOS programs the PCI-ISA interrupt routing logic in the Basic Utility Device (BUD) to steer PCI interrupts to compatible ISA IRQs.

Drivers and OS programs can determine the installed devices and their assigned resources using the BIOS interface functions. The BIOS does not support devices behind PCI-to-PCI bridges that require mapping to the first 1 MB of memory space due to architectural limitation. (Refer *to PCI-to-PCI Architecture Specifications*). The User can override the IRQ assigned to a PCI card by using SSU.

On board device auto-configuration

The BIOS detects all on board devices and assigns appropriate resources. The BIOS dispatches the option ROM code for the on board devices to DOS compatibility hole (C0000h to E7FFFh) and transfers control to the entry point. User may disable scanning of the on-board Adaptec SCSI ROM using the CU.

Automatic detection of video adapters

The BIOS looks for video adapters in the following order:

1. PCI
2. Baseboard

The on board (or off board) video BIOS is shadowed, starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to off board devices.

Multiprocessor specification support

The BIOS complies with all requirements of the Intel Multi-Processor Specification (MPS) version 1.4 for Symmetric Multi-Processor (SMP) support, as well as MPS version 1.1, for backward compatibility. The version number can be configured using the CU. The base MP Configuration Table contains the following entries:

- MP table header
- Processor entries
- PCI bus entries
- I/O APIC entries
- I/O interrupt entries
- Local interrupt entries

The extended MP table is constructed if MPS version 1.4 is selected. It contains these entries:

- System address space mapping entries
- Bus hierarchy descriptor
- Compatibility bus address space modifier entries

Note: The MP APIC table and ACPI table are the only places where the number of processors are dynamically reported from boot to boot.

Multiple Processor Support

On reset, the Primary Processor is selected by the BMC to become the Bootstrap Processor (BSP). The slot labeled Primary PROCESSOR is always examined first. If a serious error is detected during the Built-In Self-Tests (BIST), that processor does not participate in the initialization protocol and the Secondary processor then becomes the BSP and the Primary is halted and removed from the MP table. Whichever processor successfully passes BIST is automatically selected by the hardware as the BSP and starts executing from the reset vector (F000:FFF0h). A processor that does not perform the role of BSP is referred to as an Application Processor (AP). The BSP is responsible for executing POST and preparing the machine to boot the OS. BIOS performs several other tasks in addition to those required for MPS support, as described in *MP Specifications*, Rev. 1.4. These tasks are part of the fault resilient booting algorithm and are discussed in Section 2.4, Reliability Features . At the time of booting, the system is in virtual wire mode and the BSP alone is programmed to accept local interrupts (INTR driven by the PIC and NMI). As a part of the boot process, the BSP wakes up the AP. When woken up, the AP programs its memory type range registers (MTRRs) so that they are identical to those of the BSP. The AP executes a halt instruction with its local interrupts disabled.

Multiple Processor Speed Support

The BIOS supports different steppings of the Pentium® II/ Pentium® III processor as long as they are within 1 release of each other. Both processors must be of the same cache size. All installed processors must run at the same frequency (for example, the bus and core frequencies of all processors must be identical). Also, for best performance, all processors must be of the same PROCESSOR ID. The type and speed of all detected processors are also reported by the CU.

5.2.1. Memory Sizing

During POST the BIOS:

- Tests and sizes memory
- Configures the memory controller

L440GX+ supports various size and configurations of ECC and Non-ECC 100MHz SDRAM DIMMs. Memory sizing and configuration are only guaranteed for qualified DIMMs approved by Intel. The BIOS gathers all type, size, speed and memory attributes from the on-board EEPROM or SPD on the memory DIMM. It is required that the memory be stuffed from the lowest DIMM socket to the highest for the memory to function in all configurations over the full environmental range of the server.

A memory sizing algorithm determines the size of each row of DIMMs. The BIOS reads the DIMM speed information and programs the PAC accordingly. BIOS does not perform the extended memory test if instructed by the user via CU. Disabling the extended memory test reduces the boot time. In all cases, the BIOS will always initialize ECC memory. The BIOS is capable of detecting, sizing, and testing any amount of RAM, up to the physical maximum of 2 GB.

5.2.2. Boot Device Selection

The BIOS conforms to the Phoenix BIOS boot specification 1.01. The BIOS boot specification describes a method where the BIOS identifies all Initial Program Load (IPL) devices in the system, prioritizes them in the order the user selects, and then sequentially goes through each device and attempts to boot. It is possible to use the CU to change the boot order of devices

connected to the system. In the case where the order has been changed by a user, the system boots in the order chosen, with the exception of legacy devices. Legacy devices are those devices that tend to take control of the boot process altogether by hooking boot vector (interrupt 19h). Further, they provide no means for identifying themselves as an IPL device. Therefore, the BIOS cannot selectively boot from one of several Legacy IPL devices in a system. The user can choose whether the first boot device is a floppy, a CDROM, or ard drive through CU. The system BIOS tries to boot from devices in the order specified by the user. Further, the user can reorder the hard drives and choose the C: drive to be any IDE drive or any drive that is controlled by a Boot BIOS Specification compliant option ROM BIOS, such as the on-board Apdaptec BIOS. Hard drives that are controlled by all other controllers appear as 'Other bootable cards" in the setup menu, and the user cannot control the order on a drive by drive basis for such controllers. Some boot BIOS compliant option ROM BIOS's may present all the drives as a single device, and may not allow the user to manipulate the order on a drive by drive basis. The user is responsible for making sure that the C: drive has a bootable image, if booting from a hard drive.

5.2.3. Mouse and Keyboard Swapping

The BIOS allows users to swap the keyboard and PS/2 mouse connectors before the system is powered on. It detects the combination during POST and initializes the KBC accordingly. Hot plugging of the mouse and keyboard is **not** supported on L440GX+ and may have unpredictable results.

5.2.4. Boot Without Keyboard

The system can boot with or without a keyboard. There is no entry in the CU for keyboard enable/disable. The presence of the keyboard is detected automatically during POST, and the keyboard is tested if present. The BIOS does not detect or use Universal Serial Bus (USB) keyboards.

5.2.5. Front Panel CMOS Clear and Jumperless Processor Clock Ratio Settings

The BIOS has a front panel method of resetting system CMOS settings in addition to the standard jumper on the baseboard. During boot, if the CMOS jumper on the baseboard is set before power on, the BIOS scans a pin on the PIIX4 and resets the system to CMOS defaults. The following conditions also clear CMOS from the front panel:

1. system is off (5Vcc is off but 5v standby is present which means a AC power is applied)
2. user holds reset button down for at least 4 seconds.
3. while reset button is still depressed the user presses on/off button and system is off
4. release both on/off button and reset at same time.

This requires that the BMC supplies a command to the system BIOS indicating the user has completed the correct front panel button sequence. The BIOS clears CMOS as if the user had moved the CMOS clear jumper on the baseboard. Only in this one boot sequence should the CMOS be cleared. The BMC releases the CMOS clear line once the BIOS has acknowledged the CMOS clear and release it (back to 1). A reset or power down also removes the CMOS clear condition from the BMC (release is back to 1).

1. CMOS clear also reverts the system back to the lowest common clock speed for all available processors (200MHz and CACHE disable). The user needs to reboot the system once more without the CMOS clear jumper so that the actual processor speed for processors in the system is set to a clock speed default of (300MHz CACHE enable).
2. The CMOS clear setting also forces all SCSI option ROM's to their default state. See the SCSI configuration menu by pressing Ctrl-C during scan of the SCSI option ROM (Adaptec).

L440GX+ will also use a serial EEMUX to allow jumperless settings of the bus to clock ratio settings. The user will now be able to select the processor clock frequency from a BIOS setup menu.

5.3. Reliability Features

The BIOS supports several features to create a robust computing environment including the following:

- ECC memory and defective DIMM handling
- Fault resilient booting
- Logging of critical events
- IMB system management bus
- CMOS default override
- Emergency Management port

5.3.1. Defective DIMM Detection and Remapping

The ECC memory subsystem on L440GX+ is able to detect single-bit errors (SBE) and certain multi-bit errors (MBE) during reads from and writes to system DRAM. Single-bit errors can be detected and corrected. Certain patterns of MBEs can be detected but cannot be corrected, whereas other types of MBEs cannot be detected.

During POST memory testing, detection of single-bit and multi-bit errors in DRAM banks is enabled. An error is avoided by reducing the usable memory in that bank so that the byte containing the hard error is no longer accessible. The BIOS logs the errors in the nonvolatile system event log. The BIOS detects the speed of individual DIMMs. The BIOS disables a DIMM that is slower than what the hardware requires and displays a warning message.

Memory Configuration Algorithm

The algorithm for determining memory configuration is as follows:
If there is no DIMM population, or all the DIMMs are defective, or have the wrong speed, the BIOS sounds a beep code error (refer to Table 7-5) and POST is terminated. The BIOS requires at least 4 MB of good memory for POST to start up. The BIOS individually probes each bank for the size of installed DIMMs. The BIOS detects the speed and type of the DIMM SDRAM and programs the PCIset accordingly. If the bank does not match one of the allowable configurations, the BIOS reports the error with an error message. All configuration data for the memory DIMMs is gathered by the BIOS from the SPD or EEPROM on the DIMM. This is done via the SMBUS interface on the PIIX4.

In the event that the BIOS disables or resizes a bank, an error message displays with the DIMM number of the failing memory. Another message informs the user that the amount of usable memory in that bank is being reduced to eliminate the failing location. Eliminating hard errors in this way during POST is done as a precaution to prevent an SBE from becoming an MBE after the system has booted and to prevent SBEs from being detected and logged each time the failed location(s) are accessed. This is recorded in the SEL (System Event Log) at both post time as well as runtime with an SMI. See the Server management specification for the format of the memory errors in the SEL. This is implemented as an EEPROM that the BMC can access directly with the server on or off.

If the error is a SBE, the 440GX will automatically correct the data before it is returned to memory. The 440GX memory controller scrubs the memory location where the error occurred to correct the SBE and the BIOS will record the SBE via an SMI to the SEL. If the error is an

MBE, this condition is considered fatal, and after the error is logged, an NMI is generated, telling the OS to handle this fatal error.

> **Note:** EDO memory is not physically supported due to the memory socket used on the baseboard.

ECC Memory Initialization

The system BIOS handles ECC memory initialization. All memory locations, including System Management RAM and shadow memory region, are unconditionally initialized during POST (set to 0). Error detection is disabled while ECC memory is initialized to prevent false alarms caused by un-initialized memory bytes. If hard errors are detected during the memory test, the memory partition containing the error is resized to eliminate the failing locations.

ECC and SMI Support

During normal operation, any SBEs (single bit errors) are detected and are handled by the SMI support code. The SMI code logs the SBE, keeping up to 3 records of the last SBE logs in the system event log. The 440GX memory controller cannot locate the exact address of the error, but can only point to the row that contains the error location. The ECC memory feature may be disabled if significant performance increase is measured in the Platform. The BIOS setup will provide a switch to disable ECC memory. The default will be for ECC to be enabled. This switch will disappear in the shipping release if the performance is not deemed significant.

5.3.2. Fault Resilient Booting (FRB)

The BIOS and firmware provides a feature to guarantee that the system will boot even if one processor fails during POST or hangs while booting to the O/S. The BMC contains 2 watchdog timers that if they trip will reset the system. The first timer (FRB-3) starts counting down whenever the system comes out of hard reset and is usually about 5 seconds. If the BSP successfully resets and starts executing the BIOS will disable the FRB-3 timer in the BMC and system will continue on with POST. If the timer expires because of the BSP's failure to fetch or execute BIOS code, the BMC resets the system and disables the failed processor. The system will continue to reset, alternating BSP's between the primary and secondary processor socket, until the BIOS POST gets past disabling the FRB-3 timer in the BMC.

The second watchdog timer (FRB-2) in the BMC is set to 5-6 minutes and is designed to guarantee that the system will complete BIOS POST. Near the end of POST, before the options ROMs are initialized, the BIOS will disable the FRB-2 timer in the BMC. If the system hangs during POST, the BIOS will fail to disable the timer in the BMC which generates an ASR (Asynchronous System Reset).

In a dual processor system the BIOS will register the AP in the MP table. When started by the BSP, if an AP fails to complete initialization within a certain time, it is assumed to be non-functional. This AP is not listed in the MP table (refer to the *MP Specifications, Rev. 1.4*) and is invisible to the OS. If either processor fails the BIST it is marked bad and removed from the MP table. The BIOS will disable the processor and reset the system to make sure the failed processor will be electrically disabled on the next boot.

The BMC maintains a flag bit in non-volatile ROM for each processor. This bit is used to store a processor's track record. It is set whenever a processor fails and remains so until the user forces the system to "Retest Processor" in BIOS Setup and successfully makes it past both

FRB timers. The BIOS reminds the user of a previous processor failure during each boot cycle and keeps that processor disabled until the status flag is cleared by the user.

Processors that have failed in the past are not allowed to become the BSP[2], and are not listed in the MP table. It might happen that all the processors in the system are marked bad. An example is a uniprocessor system where the processor has failed in the past. If all the processors are bad, the BIOS does not alter the BSP and attempts to boot from the original BSP. It also informs the user that it is trying to boot from a failed processor if the POST gets executed. Error messages are displayed on the console and logged in the event log if a processor fails. The failed processor is identified by its number.

If the user replaces a processor marked bad by the BIOS, the system BIOS must be informed about this change by running BIOS setup and selecting that processor to be re-tested. If a bad processor is removed from the system, the BMC automatically detects this condition and clears the status flag for that processor.

Conditions under which BIOS will automatically force a retest on a processor:

1. if a processor was added to the system that was previously marked as not installed (replacing a terminator card with a processor).
2. CMOS was cleared.
3. FRB-3 or FRB-2 timer tripped and the system rebooted.
4. failed BIST on a processor

The BIOS will not automatically re-test a processor that was previously marked as failed. It cannot tell that a new processor has been added since it will not re-test the processor until the user has set the Processor Retest option to [YES] under the BIOS <F2> Setup. This option screen exists under Main→Processor Setting. The BIOS will report to the screen on POST that a processor has failed and will continue to do so until the user either marks it as failed or marks it as not installed and removes it.

Removing a processor and replacing it with a terminator module when it previously was marked as installed will cause the BIOS to indicate that it is no longer installed.

Any one of the failures (FRB-3, FRB-2 and BIST) are recorded to the BMC server event log. The processor (s) that failed are recorded as well.

If the FRB jumper on the baseboard is set to disable, the FRB-3 and FRB-2 timer shall never time-out. This effectively disables all FRB time-out features on the baseboard. **This is not a recommended setting, and should be used for debugging purposes only.**

5.3.3. Logging System Events

If enabled by the configuration utility or BIOS setup, the BIOS can log critical and informational events to nonvolatile memory. This area is managed by the Baseboard Management Controller (BMC) and can be accessed by sending commands to the BMC. A critical event is one that might result in the system being shut down to prevent catastrophic side effects from propagating to other parts of the system. Multi-bit and parity errors in the memory subsystem are considered critical errors, as are most errors that generate a Non-Maskable-Interrupt (NMI), which might subsequently generate a System Management Interrupt (SMI). These errors include I/O channel check, software generated NMI, and PCI SERR and PERR events.

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2 Since BSP selection is accomplished in hardware by Pentium II processors, it may be possible for a processor that has failed in the past, or one that has failed BIST to become the BSP. The BIOS can detect such conditions and transfer BSP ownership to another “good” processor, if available.

During POST, the BIOS initializes System Management RAM (SMRAM) with error handling and logging code. Each processor has a private area of SMRAM dedicated to it for SMI processing. The The DRAM controller and PIIX4 are programmed to generate an SMI for PCI SERR and PERR, software generated NMI, I/O channel check, and ISA watchdog time-out and NMIs. The PIIX4 can be programmed to generate an SMI on this interrupt. When these errors are detected, the SMI routines log the error or event in a manner that is transparent to the OS and then causes an NMI to be generated for certain events, so that the OS can respond appropriately. The BIOS also logs an event on another type of memory error called Single Bit Error (SBE). For this error, the BIOS will not generate a NMI to the OS.

If the OS device driver is using the watchdog timer to detect software or hardware failures and that timer expires, an Asynchronous Reset (ASR) is generated, which is equivalent to a hard reset. The POST portion of the BIOS can query the BMC for a watchdog reset event as the system reboots, and logs this event to the logging area. Failure of a processor during POST will also be logged in the Flash during POST.

5.3.4. IMB Diagnostic Bus (Intelligent Management Bus)

The IMB interface on the baseboard provides an independent interconnect between various devices in the system (for example, memory subsystem, processor subsystem, etc.), for diagnostic or other purposes normally unavailable to the system. The IMB bus acts as a system management bus and carries information about system events. The BIOS must go through the BUD interface of the BMC in order to send messages to IMB devices and receive messages. The BMC acts as a gateway to other IMB devices.

5.3.5. Emergency Management Port (EMP)

The L440GX+ provides a communication serial port with the BMC. A multiplexer controlled by the BMC determines if the COM2 external connector is attached to the BMC or the standard serial port in the Super I/O. The following features are available over this port:

- System power control (on/off remotely)
- Access to the event log, system serial no. and model no. and sensor data logs in the BMC
- System reset
- NMI control
- Allows BIOS console redirection through the BMC serial port
- Password security protection for EMP serial port
- Access to status of real time events in BMC
- Multiplexer configuration on COM2 connector
- The BIOS supports 4 different modes which the EMP can be configured for in F2 BIOS setup:

Disabled

COM2 is connected to the Super I/O and never is connected to the BMC. COM2 acts like a serial port on a normal system.

Pre-boot only

Only available when the machine is powered down and during post. If the BIOS is setup in this mode the multiplexer for COM2 is connected to the BMC during post and when the machine is off and on standby power. This requires that AC power be connected to the system. Just before boot to O/S (Int 18,19) the BIOS will switch the multiplexer via BMC command on its ISA interface over to the standard Super I/O COM2 port. The O/S or server management drivers may at anytime submit commands to the BMC to switch the multiplexer back.

Always Active

COM2 is dedicated to the serial port on the BMC. COM2 is removed from the system resources available to the O/S and BIOS. Baud rate is fixed by the BMC at 19200 baud. The BIOS does not send any commands to the BMC for this mode regarding EMP.
Restricted mode

Does not allow power control and reset functions via EMP

The EMP allows password security similar to the BIOS password security. In the F2 BIOS setup, the user may select a password, which will be downloaded to the BMC during setup. The BMC will wait until the password is submitted to the serial port. System power down, reset and NMI control are unavailable until this password is submitted. The EMP security only effects security to the BMC services and does not impact any other BIOS or O/S services in the system. BIOS will download all configuration information such as password and operation mode on saving of the BIOS setup screen (F10) to the BMC via the ISA interface.

BIOS console redirection

If the option in the BIOS for console redirection is turned on for COM2 there are some added functions allowed if the BMC EMP is setup for “Always active” or “Pre-boot” mode.

Escape characters for multiplexer control of COM2 port.

The BIOS console redirection will support an extra control escape sequence to force COM2 port over to the BMC. Once this command is sent, the COM2 port will be attached to the BMC EMP serial port and the Super I/O COM2 data will be ignored. This feature is available to the remote user to allow them to monitor the status of POST as the BIOS comes up over COM2 and then take control of the system reset or power from the BMC. If the system does not come up a watchdog time-out feature in the BMC will automatically switch the port over in case the system does not make it through POST.

The character sequence will be “ESC O 9”(also denoted as ^[O9) to switch the multiplexer to the BMC serial port. This key sequence is above the normal ANSI function keys and will never be used by an ANSI terminal.

A restriction of using COM2 for both EMP with BIOS console redirection is that the baud rate is fixed to 19200 baud and the port is setup for N,8,1 Xon/Xoff. See the section on Console Redirection for further details on how it works.

Modem support on EMP

BIOS setup will also provide a field for modem setup to the BMC. The BMC will be responsible for controlling the modem if it is attached to COM2 since the BMC will always have control of COM2 before system reset .

5.3.6. Platform Event Paging

With Platform Event Paging (PEP), the ISP2150 can be configured to automatically dial up a paging service and page you when a platform event occurs. Platform events include temperature out-of-range, voltage out-of-range, chassis intrusion, fan failure, etc.

If PEP is enabled and the BMC receives or detects a new event, it automatically sends a page. It can send a page if the processors are down or if the system software is unavailable. PEP needs an external modem connected to the server's EMP (Emergency Management Port) serial connection. This is the COM2 serial connector.

5.4. BIOS Setup Utility Operation

The ROM-resident Setup utility configures only on board devices. Configuration of added PCI or ISA cards requires the use of the diskette-loadable SSU.

The Setup utility screen is divided into four functional areas:

Table 28: Setup Utility Screens

Keyboard Command Bar	Located at the bottom of the screen. This bar displays the keyboard commands supported by the Setup utility.
Menu Selection Bar	Located at the top of the screen. Displays the various major menu selections available to the user. The Server Setup utility major menus are: Main Menu, Advanced Menu, Security Menu, Server Menu, Boot Menu, and the Exit Menu.
Options Menu	Each Options menu occupies the left and center sections of the screen. Each menu contains a set of features. Selecting certain features within a major Options menu drops you into sub-menus.
Item Specific Help Screen	Located at the right side of the screen is an item-specific Help screen.

5.4.1. Entering Setup Utility

During POST operation, the user is prompted to enter Setup using the F2 function key as follows:

Press <F2> to enter Setup

Note that a few seconds might pass before Setup is entered. This is the result of POST completing test and initialization functions that must be completed before Setup can be entered. When Setup is entered, the Main Menu options page is displayed.

5.4.2. Keyboard Command Bar

The bottom portion of the Setup screen provides a list of commands that are used for navigating the Setup Utility. These commands are displayed at all times, for every menu and sub-menu.

Each Setup menu page contains a number of features. Except those used for informative purposes, each feature is associated with a value field. This field contains user-selectable parameters. Depending on the security option chosen and in effect via password, a menu feature's value can be changeable or not. If a value is non-changeable due to insufficient security privilege (or other reasons), the feature's value field is inaccessible. The Keyboard Command Bar supports the following:

F1 Help

Pressing F1 on any menu invokes the general Help window. This window describes the Setup key legend. The up arrow, down arrow, Page Up, Page Down, Home, and End keys scrolls the text in this window.

Enter Execute Command

The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected feature has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.

ESC Exit

The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the ESC key is pressed in any sub-menu, the parent menu is re-entered. When the ESC key is pressed in any major menu, the Exit menu page displays.

↑ Select Item

The up arrow is used to select the previous value in a pick list, or the previous feature in a menu item's option list. The selected item must then be activated by pressing the Enter key.

↓ Select Item

The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the Enter key.

↔ Select Menu

The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.

- Change Value

The minus key is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.

+ Change Value

The plus key is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list.

F9 Setup Defaults

Pressing F9 causes the following to appear:

```
Setup Confirmation
Load default configuration now?
[Yes]        [No]
```

If “Yes” is selected and the Enter key is pressed, all Setup fields are set to their default values. If “No” is selected and the Enter key is pressed, or if the ESC key is pressed, then you are returned to where you were before F9 was pressed without affecting any existing field values.

F10 Save and Exit

Pressing F10 causes the following message to appear:

```
Setup Confirmation
Save Configuration changes and exit now?
[Yes]         [NO]
```

If “Yes” is selected and the Enter key is pressed, all changes are saved and Setup is exited. If “No” is selected and the Enter key is pressed, or the ESC key is pressed, you are returned to where you were before F10 was pressed without affecting any existing values.

5.4.3. Menu Selection Bar

The Menu Selection Bar is located at the top of the screen, and displays the various major menu selections.

- Main Menu
- Advanced Menu
- Security Menu
- Server Menu
- Boot Menu
- Exit Menu

These and associated sub-menus are described below.

Main Menu Selections

The following tables describe the available functions on the Main Menu, and associated sub-menus. Default values are highlighted.

Table 29: Main Menu Selections

Feature	Option	Description
System Time	HH:MM:SS	Set the System Time.
System Date	MM/DD/YYYY	Set the System Date.
Legacy Diskette A: Legacy Diskette B:	Disabled,360 KB, 720KB, 1.44 MB, 2.88 MB	Select the floppy diskette type.
Primary IDE Master	N/A	Selects sub-menu.
Primary IDE Slave	N/A	Selects sub-menu.
Secondary IDE Master	N/A	Selects sub-menu.
Secondary IDE Slave	N/A	Selects sub-menu.
Keyboard Features	N/A	Selects sub-menu.
Memory Cache	**Enabled**, Disabled	Enables Pentium® II / Pentium® III Processor Cache
PROCESSOR speed	200,250,**300, 3**50,400,450, 500	Selects the processor speed
Language	**English (US)**, Spanish, Italian, French, German	Selects which language BIOS displays.

Table 30: Primary IDE Master and Slave Adapters Sub-Menu Selections

Feature	Option	Description
Type	**Auto** None CDROM User	Auto allows the system to attempt auto-detection of the drive type. None informs the system to ignore this drive. CDROM allows the manual entry of fields described below. User allows the manual entry of all fields described below.
Cylinders	1 to 9999	Number of Cylinders on Drive. This field is only changeable for Type User. This field is informational only, for Type Auto.**
Heads	1 to 16	Number of read/write heads on Drive. This field is only available for Type User. This field is informational only, for Type Auto.**
Sectors	0 to 63	Number of Sectors per Track. This field only available for Type User. This field is informational only, for Type Auto.**
Maximum Capacity	see description	Computed size of Drive from Cylinders, Heads, and Sectors entered. This field is only available for Type User. This field is informational only, for Type Auto.**
LBA Format		information only
Total Sectors		information only
Maximum Capacity		information only
Multi-Sector Transfer	**Disabled** 2, 4, 8, or 16 Sectors	Determines the number of sectors per block for multiple sector transfers. This field is informational only, for Type Auto.
LBA Mode Control	**Disabled** Enabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors. This field is informational only, for Type Auto.
32 Bit I/O	**Disabled** Enabled	Enabling allows 32 bit IDE data transfers. This field is informational only, for Type Auto.
Transfer Mode	**Standard** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4	Select the method for moving data to/from the drive. This field is informational only, for Type Auto.
Ultra DMA	**Disabled** Enabled	For use with Ultra DMA drives. This field is informational only, for Type Auto.
** These fields appear only for Type Auto if a drive is detected.		

Table 31: Keyboard Sub-Menu Selections

Feature	Option	Description
Numlock	Auto On **Off**	Selects the power-on state of Numlock.
Key Click	**Disabled** Enabled	Enables key click.
Keyboard auto-repeat rate	**30/sec** 26.7/sec 21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	Selects key repeat rate.
Keyboard auto-repeat delay	¼ sec **½ sec** ¾ sec 1 sec	Selects delay before key repeat.

Advanced Menu Selections

The following tables describe the menu options and associated sub-menus available on the Advanced Menu.

Table 32: Advanced Menu Selections

Feature	Option	Description
Plug & Play OS	**No** Yes	Select 'Yes' if you are booting a Plug and Play capable OS (i.e. Win 95)
Reset Configuration Data	**No** Yes	Select 'Yes' if you want to clear the System Configuration Data during next boot. Automatically resets to 'No' in next boot.
PCI Configuration	N/A	Selects sub-menu.
Integrated Peripherals Configuration	N/A	Selects sub-menu.
Advanced Chipset Configuration	N/A	Selects sub-menu.
Use Multiprocessor Specification	**1.1** 1.4	Selects the version of MP spec to use. Some OS require version 1.1 for compatibility reasons.
Large Disk Access Mode	**DOS** Other	DOS - select 'DOS'. UNIX, Novell Netware, or other OS - select 'Other'.
Delay on option ROM	**Disabled** Enabled	If enabled, the BIOS pauses for 2 seconds after the option ROMs are scanned, and before option ROM screen is cleared.

Table 33: PCI Configuration Sub-Menu Selections

Feature	Option	Description
PCI Device, Embedded SCSI	N/A	Selects sub-menu
PCI Device, Slot #1	N/A	Selects sub-menu
PCI Device, Slot #2	N/A	Selects sub-menu
PCI Device, Slot #3	N/A	Selects sub-menu
PCI Device, Slot #4	N/A	Selects sub-menu

Table 34: PCI Device, Embedded SCSI Sub-Menu Selections

Feature	Option	Description
Option ROM Scan	**Enabled** Disabled	Enable option ROM scan of the selected device.
Wide SCSI Enable Master	**Enabled**	Enable selected device as a PCI bus master. Always enabled.
Latency Timer	Default 000h 020h **040h** 060h 080h 0A0h 0C0h 0E0h	Minimum guaranteed time, in units of PCI bus clocks, that a device may be master on a PCI bus.

Table 35: PCI Device, Slot #1 - Slot #4 Sub-Menu Selections

Feature	Option	Description
Enable Master	**Enabled** Disabled	Enable selected device as a PCI bus master.
Latency Timer	Default 000h 020h **040h** 060h 080h 0A0h 0C0h 0E0h	Minimum guaranteed time, in units of PCI bus clocks, that a device may be master on a PCI bus.

Table 36: Integrated Peripheral Configuration Sub-Menu Selections

Feature	Option	Description
COM 1	Disabled **Enabled** Auto PnP OS	If set to “Auto”, BIOS configures the port. If set to “PnP OS”, OS configures the port.
Base I/O Address	**3F8h** 2F8h 3E8h 2E8h	Selects the base I/O address for COM port A
Interrupt	**4** 3	Selects the IRQ for COM port A
COM 2	Disabled **Enabled** Auto PnP OS	If set to “Auto”, BIOS configures the port. If set to “PnP OS”, OS configures the port.
Base I/O Address	3F8h **2F8h** 3E8h 2E8h	Selects the base I/O address for COM port B
Interrupt	4 **3**	Selects the IRQ for COM port B
Parallel Port	Disabled **Enabled** Auto PnP OS	If set to “Auto”, BIOS configures the port. If set to “PnP OS”, OS configures the port.
Mode	Output only Bi-Directional EPP **ECP**	Selects Parallel Port Mode
Base I/O Address	**378h** 278h	Selects the base I/O address for LPT port.
Interrupt	5 **7**	Selects the IRQ for LPT port
DMA channel	**1** 3	Selects the DMA for LPT port
Floppy disk controller	Disabled **Enabled**	Enables on board floppy disk controller.

Security Menu Selections

The following options are available on the Security Menu.

Table 37: Security Menu Selections

Feature	Option	Description
User Password is	**Clear** Set	Status only; user cannot modify. Once set, it can be disabled by setting to a null string, or clearing via the clear password jumper on board.
Administrator Password is	**Clear** Set	Status only; user cannot modify. Once set, it can be disabled by setting to a null string, or clearing via the clear password jumper on board.
Set User Password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clearing via the clear password jumper on board
Set Administrator Password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clearing via the clear password jumper on board
Password on boot	**Disabled** Enabled	If enabled, and the USER password is set, the system will prompt the user for a password before system boots.
Diskette Access	User **Admin**	User is prevented from accessing the floppy drive if set to Admin. Administrator is always prevented from accessing the floppy drive.
Fixed disk boot sector	**Normal** Write protect	Will write protect the boot sector of the hard drive to prevent viruses from corrupting the drive under DOS if set to write protect.
Secure Mode Timer	**Disabled** 2 min, 5 min, 10 min, 20 min, 1 hr, 2 hr	Period of keyboard and PS/2 mouse inactivity specified for Secure Mode to activate. A USER password is required for Secure Mode to function. Cannot be enabled unless at least one password is enabled.
Secure Mode Hot Key (Ctrl-Alt-)	[ ] [A, B, ..., Z] [0-9]	Key assigned to invoke the secure mode feature. Cannot be enabled unless the USER password is enabled. Can be disabled by entering a new key followed by a backspace.
Secure Mode Boot	**Disabled** Enabled	System boots in Secure Mode. The USER must enter a password to unlock the system. Cannot be enabled unless at least one password is enabled.
Video Blanking	**Disabled** Enabled	Blank video when Secure mode is activated. A password is required to unlock the system. Cannot be enabled unless at least one password is enabled.
Floppy Write Protect	**Disabled** Enabled	When Secure mode is activated, the floppy drive is write protected. A password is required to re-enable floppy writes. Cannot be enabled unless at least one password is enabled.
Reset and Power Switch Lock	**Disabled** Enabled	When Secure Mode is activated, the Reset and Power switches are locked. A password is required to unlock the system. Cannot be enabled unless at least one password is enabled.
System backup reminder	**Disabled** Daily Weekly Monthly	Before booting the BIOS, the gives the user a reminder to perform system backup if set.
Virus check reminder	**Disabled** Daily Weekly Monthly	Before booting the BIOS, this gives the user a reminder to perform a virus check if set.

Server Menu selections

The following menu and sub-menu options are available on the Server Menu.

Table 38: Server Menu Selections

Feature	Option	Description
System Management	N/A	Selects sub-menu.
Console Redirection	N/A	Selects sub-menu.
PCI IRQs to IO-APIC mapping	**Disabled** Enabled	If Enabled, the BIOS describes direct PCI interrupt connections to the I/O APIC in the MP table. Do not enable if OS does not support this feature.
Processor Retest	Yes **No**	Select 'Yes', BIOS will clear historical processor status and retest all processors on next boot.

Table 39: System Management Sub-Menu Selections

Feature	Option	Description
System Management Mode	Disabled **Enabled**	If enabled, the Server Management Handler will be loaded.
System Event Logging	**Disabled** Enabled	When enabled, system events will be logged by BIOS and the BMC.
Clear Event Log	**No** Yes	If Yes, the System Event log will be cleared.
SMM Debug Mode	**Disabled** Enabled	If enabled the SMM will output to the video and Port 80
Server Management Info	N/A	Selects sub-menu
Set EMP Password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string. The valid characters are a-z, A-Z, 0-9 .
EMP Escape string	4 byte string	When EMP is used with a modem, BMC will use this string to inform the modem that the next bytes are to be interpreted as command. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default string is “+++”.
EMP Hang up string	8 byte string	When EMP is used with a modem, BMC will use this string to terminate a connection. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default is “ATH”.
EMP Modem Initialization String	16 byte string	When EMP is used with a modem, BMC will use this strings to configure the modem every time EMP initializes. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default is “AT&F0S0=1S14=0&D”.
EMP High modem Initialization String	4 byte string	When EMP is used with a modem, BMC will use this strings to configure the modem every time EMP initializes. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default is “0”.
EMP Access Mode	PreBoot Active **Disabled**	Pre-boot : EMP Enable during POWER DOWN or POST. Always Active : EMP always enabled. Disabled : EMP Disabled
EMP Restricted Mode Access	Enable **Disabled**	Restricted Mode : Power Down, Front Panel NMI , Reset Control via EMP are disabled. Can be selected with Pre-boot, or Always Active mode.
EMP Direct Connect/Modem Mode	**Direct Connect** / Modem Mode	Upon selection USER can connect DIRECTLY to port or using a MODEM.

Table 40: Server Management Info Sub-Menu Selections

Feature	Option	Description
Board Part Number	N/A	(DMI) Intel motherboard part no. (pba)
Board Serial Number	N/A	(DMI) Intel motherboard serial no.
System Part Number	N/A	(DMI) Integrated system part no.
System Serial Number	N/A	(DMI) Integrated system serial no.
Chassis Part Number	N/A	(DMI) Chassis part no.
Chassis Serial Number	N/A	(DMI) Chassis serial no.
BMC Revision	N/A	BMC revision ID. Revision of firmware for baseboard micro controller
HSBP Revision	N/A	HSBP revision ID. Revision of firmware on Hot Swap SCSI Backplane. Only shown if a Hot Swap BackPlane microcontroller exists in the system.

Table 41: Console Redirection Sub-Menu Selections

Feature	Option	Description
COM Port Address	**Disabled** 3F8 2F8 3E8	When enabled, Console Redirection uses the I/O port specified. Choosing “Disabled” completely disables Console Redirection.
IRQ #	3 or 4	When Console Redirection is enabled, this shows the IRQ assigned per the COM Port Address chosen above.
Baud Rate	9600 **19.2k** 38.4k 115.2k	When Console Redirection is enabled, it will use the baud rate specified.
Console Type	**ANSI** VT100	Enables the specified Console type.
Flow Control	None CTS/RTS XON/XOFF **CTS/RTS + CD**	None = No flow control CTS/RTS = Hardware based flow control XON/XOFF = Software flow control CTS/RTS +CD = Hardware based + Carrier Detect flow control

Boot menu selections

Boot Menu options allow the user to select the boot device. The following table is an example of a list of devices ordered in priority of the boot invocation. Items can be re-prioritized by using the up and down arrow keys to select the device. Once the device is selected, use the plus (+) key to move the device higher in the boot priority list. Use the minus (-) key to move the device lower in the boot priority list.

Table 42: Boot Menu Selections

Feature	Option	Description
Floppy Check	**Disabled** Enabled	If Enabled, the system verifies Floppy type on boot. Disable results in a faster boot.
Boot Device Priority	N/A	Selects sub-menu
Hard Drive	N/A	Selects sub-menu
Removable Devices	N/A	Selects sub-menu

Table 43: Boot Device Priority Selections

Boot Priority	Device	Description
1.	Removable Devices	Attempt to boot from a removable media device.
2.	Hard Drive	Attempt to boot from a hard drive device.
3.	ATAPI CD-ROM Drive	Attempt to boot from an ATAPI CD-ROM drive.
4.	LANDesk ® Service agent II	Attempt to boot from LANDesk ®.
4.	Diagnostic boot	Attempt to boot from diagnostic boot partition of the FlashF

Table 44: Hard Drive Selections

Option	Description
1. Drive #1 (or actual drive string) 2. Other bootable Cards Additional entries for each drive that has a PNP header.	To select the boot drive, use the up and down arrows to highlight a device, then press the plus key (+) to move it to the top of the list (or the minus key (-) to move it down). Other bootable cards cover all the boot devices that are not reported to the system BIOS through BIOS Boot specification mechanism. It may or may not be bootable, and may not correspond to any device. Press ESC to exit this menu.

Table 45: Removable Device Menu

Option	Description
1. Device #1 2. Other bootable devices such as Legacy Devices like floppy drives.	To select the device, use the up and down arrows to highlight a device, then press the plus key (+) to move it to the top of the list (or the minus key (-) to move it down). Press ESC to exit this menu. The operating system assigns drive letters to these devices in the order displayed.

Exit menu selections

The following menu options are available on the Server menu. Select an option using the up or down arrow key. Then press Enter to execute the option.

Table 46: Exit Menu Selections

Option	Description
Exit Saving Changes	Exit after writing all modified Setup item values to NVRAM
Exit Discarding Changes	Exit leaving NVRAM unmodified
Load Custom Defaults	Load values of all Setup items from previously saved Custom Defaults
Save Custom Defaults	Save present Setup values to Custom Defaults
Load Default Values	Load default values for all Setup items.
Discard Changes	Read previous values of all Setup items from NVRAM
Save Changes	Write all Setup item values to NVRAM

6.0 Flash Update Utility

The Flash Memory Update utility (IFLASH) loads a new copy of the BIOS into Flash ROM. The loaded code and data include the following:

- On board Video BIOS and SCSI BIOS
- BIOS Setup utility
- User-definable Flash area (User Binary Area)
- Diagnostic boot loader binary
- Language file

When running IFLASH in interactive mode, you may choose to update a particular Flash area. Updating a Flash area takes a file or series of files from a hard or floppy disk, and loads it in the specified area of Flash ROM. In interactive mode, IFLASH can display the header information of the selected files.

> **Note:** The utility iFLASH must be run without the presence of a Protected mode control program, such as Windows or EMM386 (Do not run in a DOS window under Windows NT*, Windows* 95 or Windows* 98. IFLASH uses the processor's flat addressing mode to update the Flash part.

Other platforms have shown interactions between system sensor event logging, and the IFLASH. With the L440GX+, Sensor event logging is not performed via SMI, thus there are no potential interactions to effect/corrupt FLASH.

6.1. Loading the System BIOS

A new BIOS is contained in .BIx files. The number of .BIx files is determined by the size of the BIOS area in the Flash part. They are named as follows:
xxxxxxxx.BIO
xxxxxxxx.BI1
xxxxxxxx.BI2
etc til xxxxxx.BI7
The first 8 letters of each filename on the release diskette can be any value, but cannot be renamed. Each file contains a link to the next file in the sequence. IFLASH does a link check before updating to ensure that the process is successful. However, the first file in the list can be renamed, but all subsequent filenames must remain unchanged. Once an update of the system BIOS is complete, you are prompted to reboot the system.

Language files are overwritten by updating the system BIOS. If a custom language file has been created, it must be Flashed in after the system BIOS has been updated. The user binary area and diagnostic loader binary image is also updated during a system BIOS update. User binary can be updated independent of the system BIOS.

6.2. User Binary Area

L440GX+ includes an 8KB area in Flash for implementation-specific customer add-ons. The User Binary area can be saved and updated exactly as described above in the *System BIOS* section. Only one file is needed. The valid extension for user files is USR.

6.3. Language Area

The system BIOS language area can be updated without having to update the entire BIOS. L440GX+ supports English, Spanish, French, German, and Italian (from Intel). These languages are selectable using the CU. When additional language files (*.LNG) are made available, they can be loaded into the system BIOS using IFLASH (in interactive mode, as described above), in the same manner as updating the system BIOS and the user binaries.

6.4. Recovery Mode

In the case of a corrupt .BIx image or an unsuccessful update of the system BIOS, L440GX+ can boot in recovery mode. To place L440GX+ into recovery mode, move the boot option jumper to recovery position. The jumper connects pins 1 and 2 (normal BIOS) by default.

Recovery mode requires at least 8 MB of RAM in the first DIMM socket, and drive A: must be set up to support a 3.5” 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not come up. In recovery mode operation, IFLASH (in non-interactive mode only) automatically updates only the main system BIOS. IFLASH senses that L440GX+ is in recovery mode and automatically attempts to update the system BIOS. It is recommended to disable FRB by setting the jumper to disable prior to attempting a recovery.

Before powering up L440GX+, obtain a bootable diskette that contains a copy of the BIOS release. Boot the system from the A: drive using this diskette, which executes a special AUTOEXEC.BAT file from the BIOS release. The batch file invokes IFLASH, which updates the Flash ROM with the BIOS found on the diskette.

Note: During recovery mode, video will not be initialized. One high-pitched beep tone announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beep tones. Failure is indicated by a long series of short beep tones.
If a failure occurs, it is most likely that one or more of the system BIOS IFLASH files is corrupt or missing. After a successful update, power down the system and move the recovery jumper back to pins 1 and 2. Power up the system and verify that the BIOS version number matches the version of the entire BIOS that you originally attempted to update. CMOS is not cleared when the system BIOS is updated. Configuration information like ESCD is not overwritten during BIOS flash update. Remember that any additional or different languages or User Binaries or diagnostic binaries that were present before updating need to be reloaded to Flash.

7.0 Error Handling

This chapter defines how errors are handled by the system BIOS on the L440GX+ platform. This chapter describes the role of BIOS in error handling and the interaction between the BIOS, platform hardware and server management firmware. In addition, error logging techniques are described, and beep codes for errors are defined.

7.1. Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors on L440GX+, which can be disabled and enabled individually or as a group, can be categorized as follows:

- ISA bus
- PCI bus
- Memory single and multi-bit errors
- Sensors
- processor internal error, thermal trip error, temperatures and voltages, GTL voltage levels

The BIOS cannot detect errors on the Pentium® II/Pentium® III processor bus because PAC does not monitor these.

ISA and PCI bus errors can be further classified as 'standard bus' errors, which have a standard register interface across all platforms. All other errors, such as Pentium II / Pentium® III processor and ECC errors, are referred to as 'product-specific' errors, which require special consideration depending upon the system configuration. Product-specific errors can be emulated as standard bus errors, if specific routing of certain hardware signals, as documented in this chapter, are followed. This emulation is important to both OS and BIOS NMI handlers, which have no knowledge of product-specific errors, but need to recover and shut down the system gracefully. In L440GX+, sensors are managed by the BMC. The BMC is capable of receiving event messages from individual sensors and log system events. The BIOS programs the BMC not to generate a SMI on sensor events such as fan failure.

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7.2. Error Handlers

The BIOS has an NMI handler that gets invoked when an NMI occurs in POST. Generally, the OS traps the NMI and does not pass it onto the BIOS NMI handler. Therefore, the BIOS NMI handler is rarely invoked in real operating environment. The SMI handler cannot be bypassed by the OS, and is used to handle and log system level events that are not visible to the server management firmware.

7.2.1. BIOS NMI handler

To maintain DOS compatibility, the BIOS NMI handler only processes enabled standard bus errors, such as ISA Parity check or IOCHK# errors. It displays an error message, issues a beep signal, and halts. It disables NMI using bit 7 of I/O port 70h (RTC Index Port) on the occurrence of an unknown or spurious NMI. This can cause unusual side effects because it allows a spurious NMI to block a subsequent valid NMI.

7.2.2. OS NMI handler

The OS NMI handler processes standard bus errors at the OS level. When SMI is disabled, hardware must ensure that these errors are routed to NMI. Most OS NMI handler implementations are not product specific and behave in a manner similar to a BIOS NMI handler. It is the responsibility of the BIOS SMI handler to present platform specific errors,

such as multi-bit ECC error, as one of the standard bus errors, like parity error, to the OS NMI handler. If the SMI handler is disabled via CU, the OS will not know about platform-specific critical errors.

7.2.3. SMI Handler

If the SMI handler control bit in Setup is disabled, no SMI signals are generated, and no SMI handler is required. If enabled, all system errors are preprocessed by the SMI handler, even those that are normally considered to generate an NMI. The SMI handler sends a command to the BMC to log the event and provides the data to be logged.

7.3. Handling and Logging System Errors

The BIOS is responsible for monitoring and logging certain system events. The BIOS sends an event request message to the BMC to log the event. Some errors, such as processor failure, are logged during early POST and not by the SMI handler. The following tables show the action taken by each error handler

Table 47: Error Handler Action on ISA Bus Error

Handler	Action
BIOS NMI	Displays an error message, and halts the system.
OS NMI	Logging of error and graceful system shutdown.
BIOS SMI	The SMI handler logs the event(s). There is only one OEM data byte that indicates the slot number. The slot number is set to 0ffh if it cannot be determined.

7.3.1. PCI Bus Error

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. The BIOS can be instructed to enable or disable reporting PERR# and SERR# through NMI. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported directly by SERR#. SERR# can be routed to NMI. In the L440GX+ platform, PAC is the device that reports errors on PCI #1 using SERR#. All the PCI-to-PCI bridges are configured so that it generates SERR# on the primary interface whenever there is SERR# on the secondary side, if SERR# is enabled through CU. The same is true for PERR#. Two OEM data bytes are present. The first OEM byte indicates the PCI bus number. The second OEM byte encodes the PCI device number and the PCI function number in a standard manner. The most significant 5 bits have the device number and the other 3 bits indicate the function number. The offset from the event trigger field determines whether it was a PERR or SERR. The following table show the action taken by each error handler.

Table 48: Error Handler Action on PCI Bus Error

Handler	Action
BIOS NMI	Halt the system, Disable NMI
OS NMI	Logging, shutdown
BIOS SMI	Logging PCI errors.

7.3.2. Pentium® II/ Pentium® III Processor Bus Error

Neither PAC nor the IMB controller reports Pentium® II / Pentium® III processor bus AERR# and BERR# error signals to the system. (AERR# indicates an address parity error and BERR# indicates an unrecoverable Pentium® II / Pentium® III processor bus error.) Therefore, the system SMM handler does not log and report these type of errors to the OS.

7.3.3. Memory Bus Error

PAC generates SERR# on single and double-bit errors. Generation of NMI on SBE is disabled when SMI is disabled. The following register bits control and log the errors. The following table show the action taken by each error handler.

Table 49: Error Handler Action on Memory Bus Error

Handler	Action
BIOS NMI	Emulation or Disable NMI
OS NMI	Logging, shutdown
BIOS SMI	Logging. **Note:** The SMI handler might emulate processor bus fatal errors (only), and pass control to the BIOS NMI handler.

7.3.4. System Limit Error

The L440GX+ IMB microcontroller monitors system operational limits. It manages the A/D converter, defining voltage and temperature limits, and fan senses and chassis intrusion. Any sensor values outside of specified limits are fully handled by BMC and there is no need to generate an SMI to the host processor.

7.3.5. Processor Failure

The BIOS detects BIST failure and watchdog timer reset events. The failed processor can be identified by the first OEM data byte field in the log. For example, if processor 0 fails, the first OEM data byte will be 0.

7.3.6. Configuration information

The BIOS logs the two types of BIOS configuration records. These records contain basic system configuration information and do not indicate any system error.

7.3.7. Boot event

The BIOS downloads the system date and time to the BMC during POST and logs a boot event.

7.4. Error Messages and Error Codes

The system BIOS displays error messages on the video screen. Prior to video initialization, beep codes inform you of errors. POST error codes are logged in the event log, as well as the EBDA.
The BIOS displays POST error codes on the video monitor. The error codes are defined by Intel and whenever possible are backward-compatible.
Following are definitions of POST error codes, POST beep codes, and system error messages.

7.4.1. POST Codes

The BIOS indicates the current testing phase during POST after the video adapter has been successfully initialized by writing a 2-digit hex code to I/O location 80h. If a Port-80h card (Post card) is installed, it displays this 2-digit code on a pair of hex display LEDs.

Table 50: Port-80h Code Definition

Code	Meaning
CP	Phoenix check point (port-80) code

The following table contains the port-80 codes displayed during the boot process. A beep code is a series of individual beeps on the PC speaker, each of equal length. The following table describes the error conditions associated with each beep code and the corresponding POST check point code as seen by a 'port 80h' card (for example, if an error occurs at check point 22h, a beep code of 1-3-1-1 is generated). The "-" means there is a pause between the sequence that delimits the sequence.

Table 51: Standard BIOS Port-80 Codes in Execution Sequence During POST

CP	Beeps	Reason
02		Verify Real Mode
12		Restore processor control word during warm boot (only occurs on warm reboot)
24		Set ES segment register to 4GB
04		Get processor type
06		Initialize system hardware
18		8254 timer initialization
08		Initialize PCIset registers with initial POST values
C4		Initialize system flags in CMOS
11		Load alternate registers with initial POST values
0E		Initialize I/O
0C		Initialize caches to initial POST values
16	1-2-2-3	BIOS ROM checksum
17		turn cache off
28		Autosize DRAM
2A		Clear 512K base RAM
2C	1-3-4-1	RAM failure on address line xxxx*
2E	1-3-4-3	RAM failure on data bits xxxx* of low byte of memory bus (1st 4 meg)
2F		Initialize L2 cache if enabled in CMOS
38		Shadow system BIOS ROM
20	1-3-1-1	Test DRAM refresh
29		Post Memory Manager Initialization (PMM)
33		Post Dispatch manager Initialization
34		Test CMOS
C1		Post error manager Intialization
09		Set in POST flag
0A		INITIALIZE PROCESSOR REGISTERS AND PROCESSOR MICROCODE
3A		Autosize cache
0B		Enable processor cache
0F		Initialize the local bus IDE (not used anymore but here for phx std)
10		Initialize Power Management (APM not used in L440GX+)
14		Initialize keyboard controller
1A		8237 DMA controller initialization
1C		Reset Programmable Interrupt Controller
22	1-3-1-3	Test 8742 Keyboard Controller
32		read processor bus-clock frequency and compute boot processor speed
67		Initialize and register other processor via SMM through apic bus
69		Initialize SMI handler for all processors
00		wait for secondary processor to execute init SMI handler
F4		exit SMI handler (secondary processor executed halt in SMI)
3C		Configure advanced PCIset registers and reset coprocessor
3D		Load alternate registers with CMOS values

42		Initialize interrupt vectors
46	2-1-2-3	Check ROM copyright notice
45		Initialize all pre-pnp devices

Table 52: Standard BIOS Port-80 Codes in Execution Sequence During POST (Continued)

CP	Beeps	Reason
49		Initialize PCI bus and devices (also read escd and allocate resources)
48		Check video configuration against CMOS (vga or mda)
4A		Initialize all video adapters in system
4C		Shadow video BIOS ROM
24		put PROCESSOR in big real mode (flat mode memory addressing - up to 4 Gb)
59		Post display manager initialization (video screen error codes now visible)
22		reset and test keyboard first try (only warm reset)
52		reset and test keyboard controller (both warm and cold reset)
54		Set key click if enabled
76		Enable keyboard
58	2-2-3-1	Test for unexpected interrupts
4B		Quietboot start (not used in *L440GX+*)
4E		Display copyright notice
50		Display PROCESSOR(s) type and speed
51		Eisa Init (Not used in L440GX+)
5A		Display prompt “Press F2 to enter SETUP”
5B		Disable PROCESSOR L1 cache for memory test
5C		Test RAM between 512 and 640k
60		Test extended memory (4Mb to top of memory)
62		Test extended memory address lines
64		Jump to UserPatch1
66		Configure advanced cache registers
68		Enable external and processor caches
6A		Display external cache size
6C		Display shadow message
6E		Display non-disposable segments
70		Display error messages to video
72		Check for configuration errors
74		Test real-time clock
7C		Set up hardware interrupt vectors
7E		Test coprocessor if present
80		not used
88		Initialize BIOS Data Area , timeouts for detecting parallel, serial and hdd controller clear CMOS shutdown flag
8A		Initialize Extended BIOS Data Area
81		late post core initialization of devices
87		configure mcd devices
85		Initialize and detect PC-compatible PnP ISA devices (serial, parallel etc)
82		not used
84		clear intrerrupts from com port detection
86		console redirection initialized
83		configure onboard hard disk controller
89		Enable NMI
8C		Initialize floppy controller
90		Initialize and detect hard disks

Table 53: Standard BIOS Port-80 Codes in Execution Sequence During POST (Continued)

CP	Beeps	Reason
8B		Detect and test for Mouse or Auxillary device on keyboard controller
95		Install CD-ROM for boot
92		Jump to UserPatch2
C5		Initialize GPNV areas of DMI
98	1-2	Search for option ROMs. One long, two short beeps on checksum failure of an option ROM
93		Scan for User flash ROMs MP table initialization (wake up secondary processor and halt it)
9C		Set up Power Management (not used)
9D		enable security
9E		Enable hardware interrupts
A0		Set time of day
A2		Check key lock
A4		Initialize typematic rate
C2		Initialize DMI tables
C3		Log post errors with Post error manager and to SEL in BMC also update VID bits and memory presence to BMC display and FRB errors (watchdog timeouts, bist or processor failures)
A8		Erase F2 prompt
AA		Scan for F2 key stroke
AC		Initialize EMP port if selected. Remove com2 from BDA if EMP is enabled. Enter SETUP
AE		Clear in-POST flag
B0		Turn on secure boot if enabled(secure front panel, blank video, floppy write protect) Check for errors
B2		POST done – prepare to boot Operating System
B4	1	One short beep before boot
B5		Display Quietboot (not used)
BE		Clear screen
B6		Check password (optional)
BC		Clear parity checkers
BA		not used
B7		ACPI configuration (table configuration in memory and BDA)
BD		Display multiboot menu if esc is hit
BF		Display system config summary(if enabled in CMOS)
8F		get total # of hard drives and put in BDA
91		Program IDE hard drives (timing, pio modes etc)
9F		save Total # of hard drives (scsi and ATA) in BDA
97		Fixup MP table (checksum)
99		check smart harddrive
C7		Prepare to boot to OS, clean up graphics and pmm areas.

Table 54: Standard BIOS Port-80 Codes in Execution Sequence During POST (Continued)

CP	Beeps	Reason
C0		Try to boot with INT 19 return to video mode 3 disable pmm return to real mode disable gate A20 clears system memory reset stack Invokes Int19
		Error handling Post codes (may occur at anytime during post)
DO		Interrupt handler error
D2		Unknown interrupt error
D4		Pending interrupt error
D6		Initialize option ROM error
D8		Shutdown error
DA		Extended Block Move
DC		Shutdown 10 error

7.4.2. POST Error Codes and Messages

The following table defines POST error codes and associated messages. The BIOS will prompt the user to press a key in case of serious errors. Some of the error messages are preceded by the string ‘Error” to highlight the fact that these indicate a possibly malfunctioning systems.

Table 55: POST Error Messages and Codes

Code	Error message	Pause on Error
0162	BIOS unable to apply BIOS update to processor 1	Yes
0163	BIOS unable to apply BIOS update to processor 2	Yes
0164	BIOS does not support current stepping for processor 1	Yes
0165	BIOS does not support current stepping for processor 2	Yes
0200	Failure Fixed Disk	No
0210	Stuck Key	No
0211	Keyboard error	No
0212	Keyboard Controller Failed	Yes
0213	Keyboard locked - Unlock key switch	Yes
0220	Monitor type does not match CMOS - Run SETUP	No
0230	System RAM Failed at offset:	No
0231	Shadow Ram Failed at offset:	No
0232	Extended RAM Failed at offset:	No
0250	System battery is dead - Replace and run SETUP	Yes
0251	System CMOS checksum bad - Default configuration used	Yes
0260	System timer error	No
0270	Real time clock error	No
0297	ECC Memory error in base (extended) memory test in Bank xx	Yes
02B2	Incorrect Drive A type - run SETUP	No
02B3	Incorrect Drive B type - run SETUP	No
02D0	System cache error - Cache disabled	No
02F5	DMA Test Failed	Yes
02F6	Software NMI Failed	No
0401	Invalid System Configuration Data - run configuration utility	No
None	System Configuration Data Read Error	No
0403	Resource Conflict	No
0404	Resource Conflict	No
0405	Expansion ROM not initialized	No
0406	Warning: IRQ not configured	No
0504	Resource Conflict	Error
0505	Expansion ROM not initialized	No
0506	Warning: IRQ not configured	No
0601	Device configuration changed	No
0602	Configuration error - device disabled	No
8100	processor 0 failed BIST	Yes
8101	processor 1 failed BIST	Yes
8104	processor 0 Internal Error (IERR) failure	Yes
8105	processor 1 Internal Error (IERR) failure	Yes
8106	processor 0 Thermal Trip failure	Yes
8107	processor 1 Thermal Trip failure	Yes
8108	Watchdog Timer failed on last boot, BSP switched.	Yes

Table 56: POST Error Messages and Codes (Continued)

Code	Error message	Pause on Error
810A	processor 1 failed initialization on last boot.	Yes
810B	processor 0 failed initialization on last boot.	Yes
810C	processor 0 disabled, system in Uni-processor mode	Yes
810D	processor 1 disabled, system in Uni-processor mode	Yes
810E	processor 0 failed FRB Level 3 timer	Yes
810F	processor 1 failed FRB Level 3 timer	Yes
8110	Server Management Interface failed to function	Yes
8120	IOP sub-system is not functional	Yes
8150	NVRAM Cleared by Jumper	Yes
8151	NVRAM Checksum Error, NVRAM cleared	Yes
8152	NVRAM Data Invalid, NVRAM cleared	Yes

8.0 Operating System Information

The following section contains information pertaining to operating systems that have been validated on the ISP2150 2U server platform. Please see the Late Breaking News, and any associated errata for current information on supported operating systems.

8.1. Red Hat Linux 6.1

Red Hat Linux 6.1 has been validated on the ISP2150.

8.2. Microsoft Windows NT 4.0 Service Pack 5

Microsoft Windows NT 4.0 with Service Pack 5 installed has been validated on the ISP2150.

8.3. Solaris 7

Solaris 7 has been validated on the ISP2150.

9.0 Server Management – Intel Server Control

The ISP2150 uses Intel Server Control (ISC) server management software. Intel ® Server Control (ISC) is a server-management tool targeted for a networked server environment. ISC uses the Desktop Management Interface (DMI) 2.0 framework to manage Windows NT* server hardware components. ISC provides real-time monitoring and alerting for server hardware sensors.

ISC has two main software components:

- *The managed server*: ISC Server Instrumentation is installed on the Windows NT, server that is going to be managed by the ISC Console software.
- *The managing console*: ISC Console software is installed on the user console that will manage the server.

This section contains information pertaining to the ISC software that supports the ISP2150. For further information or details on ISC software, please refer to the ISC Product Guide or http://support.intel.com/support/motherboards/server/isc/.

9.1. FRU/SDR Load Utility

The ISP2150 utilizes version 4.0 of the of the FRU/SDR utility. This utility is used for updating the server management subsystem product level Field Replacement Unit (FRU), Sensor Data Repository (SDR), and the System Management (SM BIOS) non-volatile storage components.

This utility is used to update the non-volatile storage device associated with the Baseboard Management Controller, which holds the SDR & FRU area, and also updates the SM BIOS (DMI) area located in the BIOS non-volatile storage device. The utility has the capability to generically handle FRU devices that may not be associated with the Baseboard Management Controller.

9.2. System Setup Utility (SSU)

The ISP2150 uses Release 4.0 RC 1 of the System Setup Utility (SSU).

9.3. ISC 1.8.1

9.3.1. ISC 1.8.1 Maintenance Release (MR) 2.1

If you are running Windows NT 4.0 on the ISP2150, you must use ISC 1.8.1 with MR 2.1. ISC version 1.8.1 has been validated on the ISP2150 when running Windows NT 4.0 with Service Pack 5.

9.4. ISC 1.10.1

If you are running Solaris 7 on the ISP2150, you must use ISC 1.10.1. ISC 1.10.1 has been validated in the ISP2150 when running Solaris 7.

9.5. Emergency Management Port (EMP) Console Utility

ISP2150 uses the EMP Console Utility version 1.8.0.3. The Emergency Management Port (EMP) Console provides an interface to the Emergency Management Port (EMP). This interface allows remote server management via a modem or direct (serial port to serial port) connection.

The server control operations available with EMP Console are:

- Connecting to remote servers
- Powering the server on or off
- Resetting the server

The EMP Console uses three management plug-ins to monitor the server:

- SEL Viewer
- SDR Viewer
- FRU Viewer

The EMP Console also has Phonebook plug-in that can be used to create and maintain a list of servers and their phone numbers.

NOTE

EMP and PEP (Platform Event Paging) share your modem. PEP has priority over all applications except EMP. If an alert occurs, PEP will reset your modem and page you.

9.6. Platform Event Paging (PEP)

With Platform Event Paging (PEP), your server can be configured to automatically dial up a paging service and page you when a platform event occurs. Platform events include temperature out-of-range, voltage out-of-range, chassis intrusion, fan failure, etc. If PEP is enabled and the BMC receives or detects a new event, it automatically sends a page. It can send a page if the processors are down or if the system software is unavailable. PEP needs an external modem connected to the server's EMP (Emergency Management Port) serial connection. This is typically the COM2 serial connector.

10.0 Electrical, Environmental, and Mechanical Specifications

This chapter specifies the operational parameters and physical characteristics for ISP2150 2U server system.

10.1. Absolute Maximum Ratings

Operation of ISP2150 at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 57: Absolute Maximum Ratings

Operating Temperature	0°C to +55°C **
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V ***
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

**Chassis design must provide proper airflow to avoid exceeding SECC Pentium® II / Pentium® III maximum case temperature.
*** V_{DD} means supply voltage for the device.

Further topics in this chapter specify normal operating conditions for ISP2150.

10.2. Electrical Specifications

DC specifications for ISP2150 power connectors and module power budgets are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications) can be obtained from other documents:

- PCI Connectors -- PCI Local Bus Specification Rev. 2.1

10.2.1. Power Connection to the Baseboard

The main power supply connection on the baseboard is obtained using the 24-pin style connector. The following table defines the pinouts and wire gauge/color for this connector.

Table 58: 24-pin Main Power Connector Pinout

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2	+3.3Vdc	Orange	14	-12Vdc	Blue
3	COM	Black	15	COM	Black
4	+5 Vdc	Red	16	PS-ON	Green
5	COM	Black	17	COM	Black
6	+5 Vdc	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray	20	-5V	White
9	5VSB	Purple	21	+5 Vdc	Red
10	+12Vdc	Yellow	22	+5 Vdc	Red
11	+12Vdc	Yellow	23	+5 Vdc	Red
12	+3.3Vdc	Orange	24	COM	Black

10.2.2. Power Consumption

The following table shows the power consumed on each supply line for a ISP2150 baseboard with 2 processors, 4 – 64 MB DIMMs, 1 Hot Swap Back Plane, 1 floppy drive, 1 slimline CD-ROM drive and 4 SCA hot swap SCSI drives while running a thermal stress test.

NOTE: The following numbers are provided as an example. Actual power consumption will vary depending on the exact ISP2150 configuration.

Description	# Items	3.3v	5v	12v	5v stby
Total Power (Amps)		7.4	18.8	7.5	0.8
Total Power (Watts)		24.4	94.0	90.1	3.8
				Total Watts	**212**

Table 59: ISP2150 Power Consumption

10.2.3. Power Supply Specifications

This section provides power supply design guidelines for a ISP2150-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

PARAMETER	MIN	NOM	MAX	UNITS	TOLERANCE
+3.3V	+3.17	+3.30	+3.43	V	± 4%
+5V	+4.80	+5.00	+5.20	V	± 4%
+12V	+11.4	+12.00	+12.6	V	± 5%
-12V	-10.80	-12.00	-13.20	V	± 10%
-5V	-4.50	-5.00	-5.50	V	± 10%
+5Vstdby	+4.75	+5.00	+5.25	V	± 5%

Table 60: ISP2150 Power Supply Voltage Specification

10.3. Mechanical Specifications

The following diagrams show the mechanical specifications of the L440GX+ baseboard. All dimensions are given in inches, and are dimensioned per ANSI Y15.4M. Maximum primary-side component height is .550" unless otherwise noted. Connectors are dimensioned to pin 1. Refer to "Connector Specifications" after the diagram for more information.

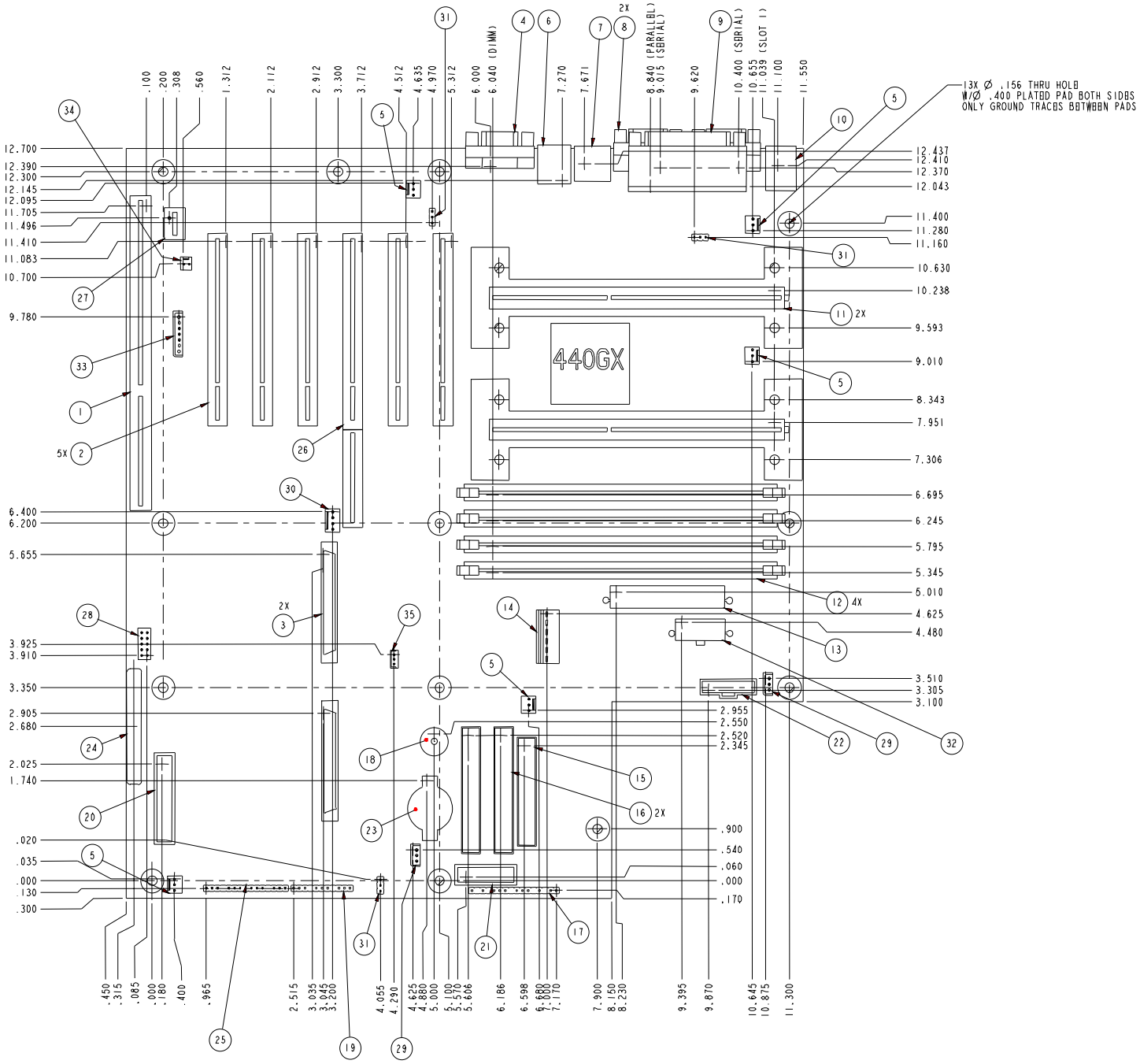

Figure 25. Baseboard Mechanical Diagram

Connector I/O Panel

The following diagram shows the I/O connector locations and mechanical dimensions for the ISP2150 I/O shield as viewed from the rear of the system.

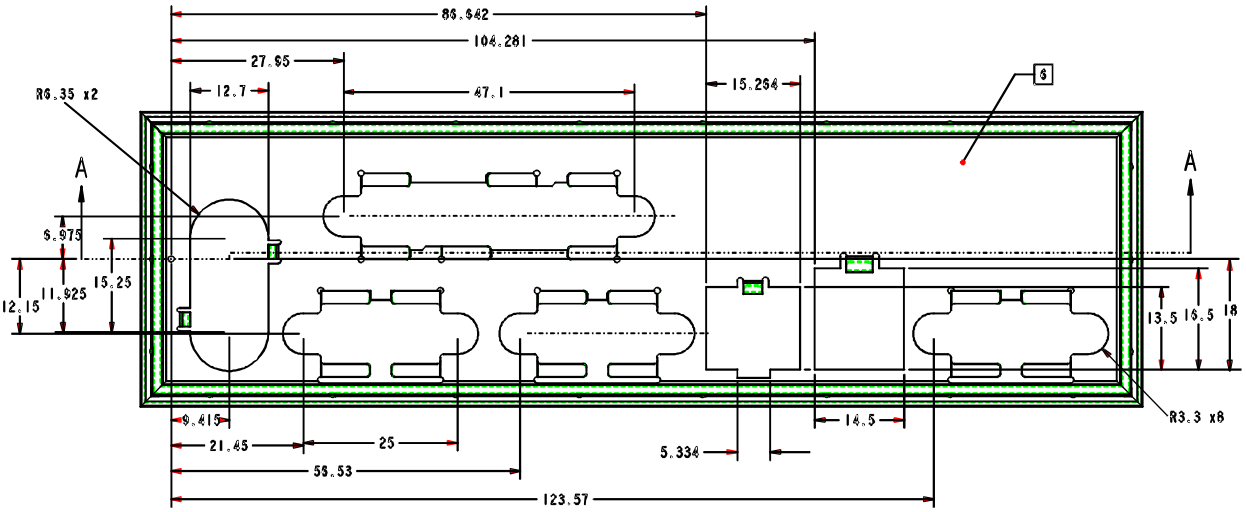

Figure 26. I/O Panel Connector Locations

[redacted]

11.0 Regulatory and Integration Information

11.1. Regulatory Compliance

This server systemcomplies with the following Safety and EMC regulations For updated product regulation information refer to Intel Server Builder web-site at: http://www.intel.com/business/ibp/servers/INDEX.HTM

Table 61: Safety Regulations

Regulation	Title
UL 1950/CSA950	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC60 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to IEC 60950. (Norway, Sweden, Denmark, and Finland)

Table 62: EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
ICES-003	Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374) (Canada)
CISPR 22 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
EN55022 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN55024	Generic Immunity Standard; (Europe)
AS/NZS 3548	Australian Communications Authority (via compliance to CISPR 22

11.2. Regulatory Compliance Markings

This product is provided with the following Product Certification Markings.

- UL & cUL Listing Mark
- CE Mark
- The CE marking on this product indicates that it is in compliance with the European community's EMC (89/336/EEC) and low voltage directives (73/23/EEC)
- NEMKO Mark
- ERG German GS Mark
- FCC, Class B Markings (Declaration of Conformity)
- ICES-003 (Canada EMC Compliance Marking)
- VCCI Mark
- C-Tick Mark