Enterprise Server Group

Intel® C440GX+ Server Board
Technical Product Specification

Version 1.0
May 1999

intel®

Revision History

Revision	Revision History	Date
Rev 0.9	Preliminary release of C440GX+ Server Board Technical Product spec.	1/99
Rev 1.0	Updated to reflect Pentium III Xeon support and other updates	5/99

The C440GX+ Server Board may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Preface

This document describes the architecture of the Intel® C440GX+ server board, an ultra high-performance server board optimized for 100MHz processor/memory operation.

Feature Summary

Major features of the C440GX+ server board:

- Support for dual Intel® Pentium®II Xeon™ and Pentium III Xeon processors. On the C440GX+, these processors operate with a 100MHz front side bus. Pentium II Xeon processors support core speeds of 400, 450 and 500 MHz while the Pentium III Xeon processor operate at core speeds starting at 500 MHz and higher as they become available.
- Using dual processors, the system is fully MPS 1.4 compliant (with appropriate *Pentium II or Pentium III* extensions). In addition, support is provided for MP operating systems that may not be fully MPS 1.4 compliant.
- Two 5 Volt or 12 Volt VRM 8.3-compliant voltage regulator slots
- System design based on Intel 440GX AGP set and I/O APIC devices.
- 100MHz main memory interface supporting up to 2GB of PC/100-compliant commodity SDRAM DIMMs.
- PCI I/O system, compliant with revision 2.1 of the PCI specification. The primary PCI bus is provided by the GX host bridge
- Four PCI 32 bit, 33 MHz expansion slots.
- Two PCI 32 bit, 66 MHz “Universal” 5V expansion slots.
- Dual-port PCI SCSI controller providing independent Ultra 2 and Ultra wide SCSI channels.
- PCI 10/100Mbit Ethernet controller with integrated physical layer.
- High performance 2D PCI video controller with 2MB of SGRAM video memory onboard.
- PCI IDE controller (in PIIX4E) providing dual independent Ultra DMA/33 IDE interfaces, each able to support 2 IDE drives.
- One ISA expansion slot. (Not Shared)
- Compatibility I/O device integrating floppy, dual serial and parallel ports.
- Two Universal Serial Bus (USB) ports.
- Integration of server management features, including thermal, voltage, fan, and chassis monitoring into one baseboard management controller (BMC).
- Emergency Management Port (EMP) feature.
- Platform Event Paging (PEP) feature.
- Flash BIOS support
- Designed to meet Microsoft* SDG 1.0 Compliance

Conventions and Terminology

This document uses the following terms and abbreviations:

Term	Definition
440GX+	Intel 82440GX basic AGP set joined with an Intel 21150 AGP to PCI-66 bridge
ACPI	Advanced Configuration and Power Interface. With respect to C440GX+, ACPI provides the programming standard for power management features.
AGP	Accelerated Graphics Port. This 440GX feature is not used on C440GX+.
AP	Application Processor. Processor not designated to boot the system in the multiprocessor configuration
APIC	Intel Advanced Programmable Interrupt Controller for Symmetric Multi-processor (SMP) systems.
ARO	A 0-channel Adaptec* ARO-1130U2 RAID Port III card capable of using the on-board SCSI interface
Asserted	Active-high (positive true) signals are asserted when in the high electrical state (near power potential). Active-low (negative true) signals are asserted when in the low electrical state (near ground potential).
Bridge	The circuitry that connects one computer bus to another, allowing an agent on one to access the other.
BSB	Back Side Bus. The Pentium II Xeon processor internal interface to its second level cache which operates at the same speed as the processor core.
BSP	Boot Strap Processor. Processor designated to boot the system in the multiprocessor configuration.
BUD	Basic Utility Device. On C440GX+, this refers to a custom ASIC for miscellaneous functions.
Byte	An 8-bit quantity.
Dword	Double word is a 32-bit quantity.
ECC	Error Checking and Correction. On C440GX+, error correction is provided for single-bit memory errors, and error detection for multiple-bit errors.
EDO	Extended Data Out memory device
FSB	Front Side Bus. Processor to system memory and chipset interface operating at 100MHz. Also referred to as the processor host bus.
GB	1024 MB
GTL	Gunning Transceiver Logic
Hard Reset	A reset event in the system that initializes all components and invalidates caches.
I^2C	Inter-Integrated Circuit - A bi-directional two-wire bus for direct connection to other I^2C compatible devices on a circuit board
I_2O	Intelligent I/O – An open architecture for the development of device drivers in network system environments
IMB	Intelligent Management Bus
Kb	1024 bits
KB	1024 bytes
LVD	Low Voltage Differential
Mb	1024 Kb
MB	1024 KB
MB/s	Mega**bytes** per second.
Mbps	Mega**bits** per second.
Nc	Signal is not connected
Negated	A signal is negated when inactive. Active-low signal names have "_L" at the end of the name. Active-high signal names have no "_L" suffix. To reduce confusion when referring to active-high and active-low signals, the terms one/zero, high/low, and true/false are not used when describing signal states.
NIC	Network Interface Controller. On C440GX+, the Intel 82559 device performs this function.

Term	Definition
p/d	Signal is grounded (pulled down)
p/u	Signal is pulled up or directly connected to VCC
PAC	PCI–AGP-Controller. Acronym used to describe the 440GX AGP set
PCI	Peripheral Component Interconnect. I/O bus for the C440GX+ server board.
Pentium II Xeon processor	Pentium II Xeon processor featuring a 100MHz FSB SC330 interface, starting at a 400 MHz core, 512KB cache, in an SECC2 cartridge. C440GX+ architecture is optimized to work with this particular flavor of Pentium II processor. This is also referred to as “CPU” or “processor” in this document.
Pentium III Xeon processor	Pentium III Xeon processor featuring a 100MHz FSB SC330 interface, starting at a 500 MHz core, 512KB cache, in an SECC2 cartridge. This is also referred to as “CPU” or “processor” in this document.
PIIX4E	PCI ISA bridge, IDE, USB, and power management controller, along with ISA interrupt, RTC, and DMA controllers.
POST	Power On Self Test
Processor card	SEC cartridge
Qword	Quad word is a 64-bit quantity.
RAID	Redundant Array of Independent Disks
SC330	330 pin contact slot connector formerly known as “Slot 2 connector”
SDRAM	Synchronous Dynamic RAM device
SE	Single Ended
SEC cartridge	Single Edge Contact cartridge packaging for Pentium II Xeon
SMP	Symmetric Multi-Processing
Soft Reset	A reset event in the system which forces processors to execute from the boot address, but does not change the state of any caches or peripheral devices.
Ultra 2 SCSI	SCSI interconnect operating at 40 MHz providing 80MB/s throughput
Ultra Wide SCSI	Small Computer Systems Interface (SCSI) interconnect operating at 20MHz, providing 40 MB/s throughput with 16-bit data width.

TABLE OF CONTENTS

Tables

Figures

1. Introduction

This chapter provides an overview of the C440GX+ showing functional blocks and their relationships, and proposed board layout diagram. The following diagram shows the functional blocks of the C440GX+ server board, and the plug-in modules that it supports.

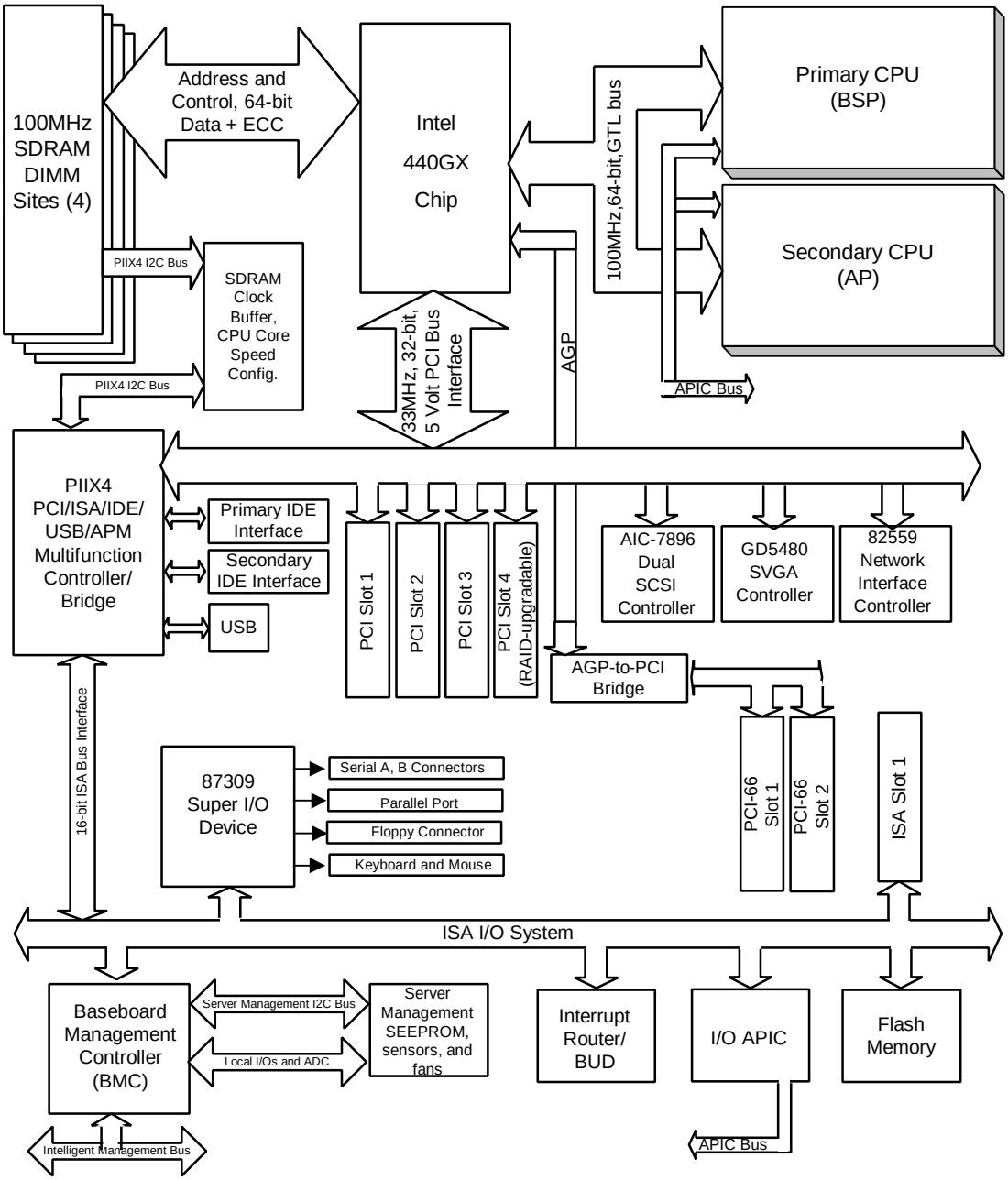


Figure 1-1. C440GX+ Block Diagram

1.1 Server board Architecture Overview

The C440GX+ server board architecture is based on a design supporting either dual Pentium II Xeon or Pentium III Xeon processors utilizing a 100 MHz FSB and the Intel 440GX AGP set. The C440GX+ provides a PCI-based I/O subsystem containing embedded devices for video, NIC, SCSI, and IDE, along with an ISA bridge to support compatibility devices. The server board also provides server management and monitoring hardware support, and interrupt control that supports dual processor and PC/AT compatible operation. This section provides an overview of these C440GX+ subsystems:

- Support for one to two identical Pentium II Xeon 100MHz FSB or Pentium III Xeon processors.
  - ⇒ Two "SC330" edge connectors operating at 100MHz
  - ⇒ One embedded 8.3-compliant voltage regulator (VRM) and two VRM 8.3-compliant voltage regulator slots supporting either 5 Volt or 12 Volt VRM cards.
- Intel 440GX AGP set providing processor host interface, PCI bridge, and memory controller with 100MHz pathway to memory.
- 4 DIMM sockets that support PC/100-compliant SDRAM devices.
- Intel 21150 AGP-PCI-66 Bridge
- 66 MHz PCI segment providing two PCI 32-bit, 5 Volt "Universal", 66 MHz Slots
- 33MHz PCI segment providing four 32-bit slots and four embedded devices.
  - ⇒ PCI/ISA/IDE Accelerator (PIIX4E) for PCI-to-ISA bridge, and PCI IDE interface, USB controller, and power management controller.
  - ⇒ PCI video controller - Cirrus Logic* GD5480.
  - ⇒ PCI dual channel SCSI controller – Adaptec* 7896, supporting independent Ultra2 and Ultra wide SCSI channels
  - ⇒ "RAID-upgradeable" PCI slot with special interrupt capabilities supporting the Adaptec* ARO-1130U2 RAID Port III card.
  - ⇒ PCI Network Interface Controller (NIC) with integrated physical layer - Intel 82559.
- ISA bus segment with one expansion connector and four embedded devices.
  - ⇒ National Semiconductor* 87309 Super I/O controller chip providing all PC-compatible I/O (floppy, parallel, serial, keyboard, mouse).
  - ⇒ I/O APIC
  - ⇒ Flash memory for system BIOS.
  - ⇒ Server management host interface.
  - ⇒ Interrupt Router and BUD (Basic Utility Device).
- Single server management Microcontroller providing monitoring, alerting, and logging of critical system information from embedded sensors on server board. C440GX+ includes the EMP (Emergency Management Port) interface for remote access to this information, along with reset and power control, via external modem.

1.1.1 Intel® Pentium® II Xeon™ and Pentium III Xeon Processor

The Intel Pentium II Xeon and Pentium III Xeon processor are specifically designed to meet the demands of the mid-range and higher server platform. To meet the demand, these processors combine several premium characteristics: the architectural compatibility of previous Intel microprocessor generations, the Dynamic Execution and Dual Independent Bus architecture of the P6 micro architecture found in the Pentium® II processor, and several new features designed to make these processors the right choice for advanced server management and business-critical applications.

Processor Highlights

- Power and performance for mid-range and higher server platforms
- Pentium II Xeon processors operate at frequencies of 400, 450 and 500 MHz and support the following L2 Cache sizes: **400 MHz**-512KB, 1MB; **450MHz-**512KB, 1MB, 2MB; **500MHz**-512KB, 1MB, 2MB.
- Pentium III Xeon processors operate at frequencies starting at 500 MHz with L2 cache sizes of 512 KB, 1 MB and 2 MB.
- 32KB (16KB data /16KB instruction) non-blocking, Level one (L1) cache provides fast access to heavily used data
- Dual Independent Bus (D.I.B.) architecture increases performance and provides more data to the processor core
- 100MHz system bus speeds data transfer between the processor and the system
- Level 2 cache bus operating at same speed as processor core provides new level of peak bandwidth to the processor
- Cacheable address space up to 64GB
- "Glueless" multiprocessing support
- Intel® Extended Server Memory Architecture--expanded 36-bit memory support which allows operating systems and applications to utilize memory greater than 4 Gbytes
- Cartridge packaging technology delivers state-of-the-art processing and bus technology to mid-range and higher servers and workstations

Advanced Management Features

- Thermal Sensor—To provide thermal protection, this device continuously monitors core temperatures via an on-core thermal diode and combines with platform manageability features to enable the system to actively manage thermal conditions.
- Error Checking and Correction—ECC helps protect mission-critical data. ECC is performed on the data signals for all L2 cache bus and system bus transactions, automatically correcting single-bit errors and alerting the system to any double-bit errors. All errors are logged, and the system can track error rates to identify failing system components. Functional Redundancy Checking—Full Functional Redundancy Checking (FRC) increases the integrity of critical applications by comparing the outputs of a processor pair and alerting the system if it detects any differences between them.
- System Management Bus—Inside the cartridge, two new components (in addition to the thermal sensor described above) use this interface to communicate with other system management hardware and software:
- Processor Information ROM (PIROM) contains information about the specific processor in which it resides. This information includes robust addressing headers to allow for flexible programming and forward compatibility, core and L2 cache electrical specifications, processor part and S-spec numbers, and a 64-bit processor number.

Other Significant Features

- Intel-developed Single Edge Contact (S.E.C.) cartridge packaging enables high-volume availability, improved handling protection and a common form factor for future Intel Pentium II Xeon and Pentium III Xeon processors.
- Dimensions:
  - Cartridge (without heatsink): 15.24 cm × 12.7 cm × 1.905 cm
  - Core CPU die: 130.9 mm2
  - Level 2 cache die: 222.21 mm2

1.1.2 Voltage Regulation Modules (VRMs)

The C440GX+ server board provides one embedded VRM 8.3-compliant voltage regulator (DC-to-DC converter) to provide VCC_P to the processor core of the primary processor. In addition, two VRM 8.3-compliant voltage regulator card sockets, capable of supporting either 5 Volt or 12 Volt VRMs, are mounted on the server board. Use of either 5 volt or 12 volt VRMs is dependent on power requirements for a particular system configuration. The primary VRM socket is used to provide VCC_p to the L2 cache of the primary and secondary processors. This VRM must be installed for either single or dual processor operation. The secondary VRM socket must be used to provide VCC_p to the processor core of the secondary processor in a dual processor configuration.

1.1.3 440GX Host Bridge / Memory Controller

The architecture used for the C440GX+ server board is designed around the Intel 440GX AGP set. This device provides 100MHz processor host bus interface support, DRAM controller, PCI bus interface, AGP interface (used on C440GX+ for an additional PCI-66 peer bus), and power management functions. The host bus/memory interface in the 440GX is optimized for 100MHz operation, using 100MHz SDRAM main memory. The PCI interface is PCI 2.1-compliant, providing a 33 MHz / 3.3V & 5V signaling environment for embedded controllers and slots in the single PCI segment on C440GX+. The 440GX memory controller supports up to 2 GB of memory, using PC/100 compliant Synchronous DRAM (SDRAM) devices on DIMM plug-in modules.

1.1.4 AGP to PCI-66 Bridge

The C440GX+ server board provides an additional PCI peer bus by using the AGP interface of the 440GX and coupling it with the Intel 21150 AGP to PCI-66 bridge chip. The 21150 PCI bridge is compliant with PCI *Local BUS Specification, Revision 2.1*. The 21150 provides full support for delayed transactions, enabling the buffering of memory read, I/O, and configuration transactions. It also supports buffering of simultaneous multiple posted write delayed transactions in both directions. The 21150 allows the two PCI buses to operate concurrently. This means that the master and target on the same PCI bus can communicate while the other PCI bus is busy. The 21150 bridge also allows for 33 MHz as well as 66 MHz clocking.

1.1.5 Memory

The C440GX+ server board only supports 100MHz, PC/100-compliant SDRAM DIMMs. Two types of SDRAM DIMMs are supported: registered and unbuffered.

The C440GX+ server board provides four DIMM sites capable of supporting either 72-bit registered or unbuffered ECC SDRAM DIMMs or 64-bit unbuffered Non-ECC SDRAM DIMMs.

The minimum supported memory size is 32 MB. The maximum memory size configurable is 2 GB. Memory can be installed in one, two, three or four sockets and populated in any order. However, unpopulated DIMM sockets between installed DIMMs is not supported. Memory sizes may vary between DIMMs. Mixing Registered and Unbuffered DIMMs is not supported.

Table 1-1 Supported DIMM Sizes

Unbuffered DIMM Sizes	*Registered DIMM Sizes*
32 MB	
64 MB	64 MB
128 MB	128 MB
256 MB	256 MB
	512 MB

The PIIX4E provides a local IMB interface to SDRAM DIMM information, SDRAM clock buffer control, and processor core speed configuration. BIOS code uses this interface during auto-configuration of the processor/memory subsystem, as part of the overall server management scheme.

1.1.6 PCI I/O Subsystem

The primary I/O bus for C440GX+ is PCI, compliant with revision 2.1 of the PCI specification. The primary PCI bus on C440GX+ supports embedded SCSI, network control, video, and a multi-function device that provides a PCI-to-ISA bridge, bus master IDE controller, Universal Serial Bus (USB) controller, and power management controller. The primary PCI bus also supports four slots for full-length PCI add-in cards.

PCI SCSI Subsystem

The embedded PCI SCSI controller on C440GX+ is the Adaptec* AIC-7896 dual function controller. This device provides both Ultra 2 wide and Ultra wide SCSI interfaces as two independent PCI functions[1]. PCI slot 4 is RAID-upgradeable, providing additional support for a 0-channel Adaptec ARO-1130U2 RAID port III card.

PCI Network Interface Subsystem

The network interface on C440GX+ is implemented using an Intel 82559. This device provides a 10/100Mbit Ethernet interface supporting 10baseT and 10baseTX, integrated with an RJ45 physical interface. The 82559 also provides Wake-On-LAN functionality if the power supply supports a minimum of 850mA of 5V standby current to the server board. Wake on LAN functionality can be enabled or disabled via a jumper on the server board (Jumper location J5A1).

PCI Video Subsystem

The embedded SVGA-compatible video controller on C440GX+ is a Cirrus Logic* GD5480 SGRAM GUI Accelerator. The SVGA subsystem also contains 2MB of SGRAM (synchronous graphics RAM).

PCI-to-ISA Bridge, IDE/USB/PM Controller

The PIIX4E is a multi-function PCI device, with four distinct PCI controllers onboard: PCI-to-ISA bridge, PCI bus master IDE interface, USB host controller, and enhanced power management. The PIIX4E also integrates a real-time clock (RTC), 82C54 Timer/Counter, two 82C59 interrupt controllers, and dual 82C37 DMA controllers on-chip that support “distributed DMA” transfers as well as compatibility operation. The PIIX4E also provides general purpose chip select decoding for BIOS, external RTC, keyboard controller and Intel I/O APIC. The integrated IDE controller supports up to four IDE devices in Bus Master mode at speeds up to 33MB/s (Ultra DMA/33 operation). The USB controller is Universal Host Controller Interface (UHCI) compatible.

1 The PIIX4E and AIC-7896 are “Multi-function” PCI devices that provide separate sets of configuration registers for each function, while sharing a single PCI hardware connection. Refer to the PCI specification.

1.1.7 ISA I/O Subsystem

The C440GX+ server board contains a full-featured ISA I/O subsystem with one full length ISA slot, and local ISA bus interface to embedded Super I/O, I/O APIC, Flash BIOS, Basic Utility Device2 (BUD2), and server management features.

National* 87309 Super I/O Device

Compatibility I/O on C440GX+ is implemented using a National* PC87309VLJ component. This device integrates a floppy disk controller, keyboard and mouse controller, two enhanced UARTs, full IEEE 1284 parallel port, and support for power management. The chip provides separate configuration register sets for each supported function. Connectors are provided for all compatibility I/O devices.

I/O APIC

The C440GX+ server board incorporates an Intel S82093AA Advanced Programmable Interrupt Controller to handle interrupts in accordance with Multiprocessor Specification 1.4.

Flash BIOS

The BIOS for the C440GX+ server board resides in an Intel 28F008S5 Flash File Memory Family, 8Mbit, symmetrically blocked (64KB) flash device.

1.1.8 Server Management Subsystem

C440GX+ incorporates a Dallas* 82CH10 micro-controller as the server board management controller (BMC). The BMC controls and monitors server management features on the server board, and provides the ISA interface to two independent IMB-based serial buses. The power supply on/off control, hard reset control, video blanking, watchdog timers, Fault Resilient Booting (FRB) functionality, and all temperature, voltage, fan and chassis intrusion monitoring are integrated into the BMC. The BMC can be polled for current status, or configured to automatically send an alert message when an error condition is detected either manually or by software.

In addition, the C440GX+ server board provides EMP (Emergency Management Port) functionality. This allows, when using an external modem, remote reset, power up/down control, and access to the event log, or run-time information. This port also supports console redirection, and, with additional software support, the EMP can also be used to download firmware and BIOS upgrades.

1.1.9 Basic Utility Device

C440GX+ provides the Basic Utility Device (BUD) for ISA and PCI interrupt routing, SMI/NMI routing, and PCI arbitration, S I/O and BMC chip selects. The physical device is an Altera* 7128 CPLD. Other features formerly handled by an external CPLD on previous servers, such as the host ISA interface to server management functions, now appear in the BMC.

1.2 Server board Placement Diagram

The following diagram shows the placement of major components and connector interfaces on the C440GX+ server board.

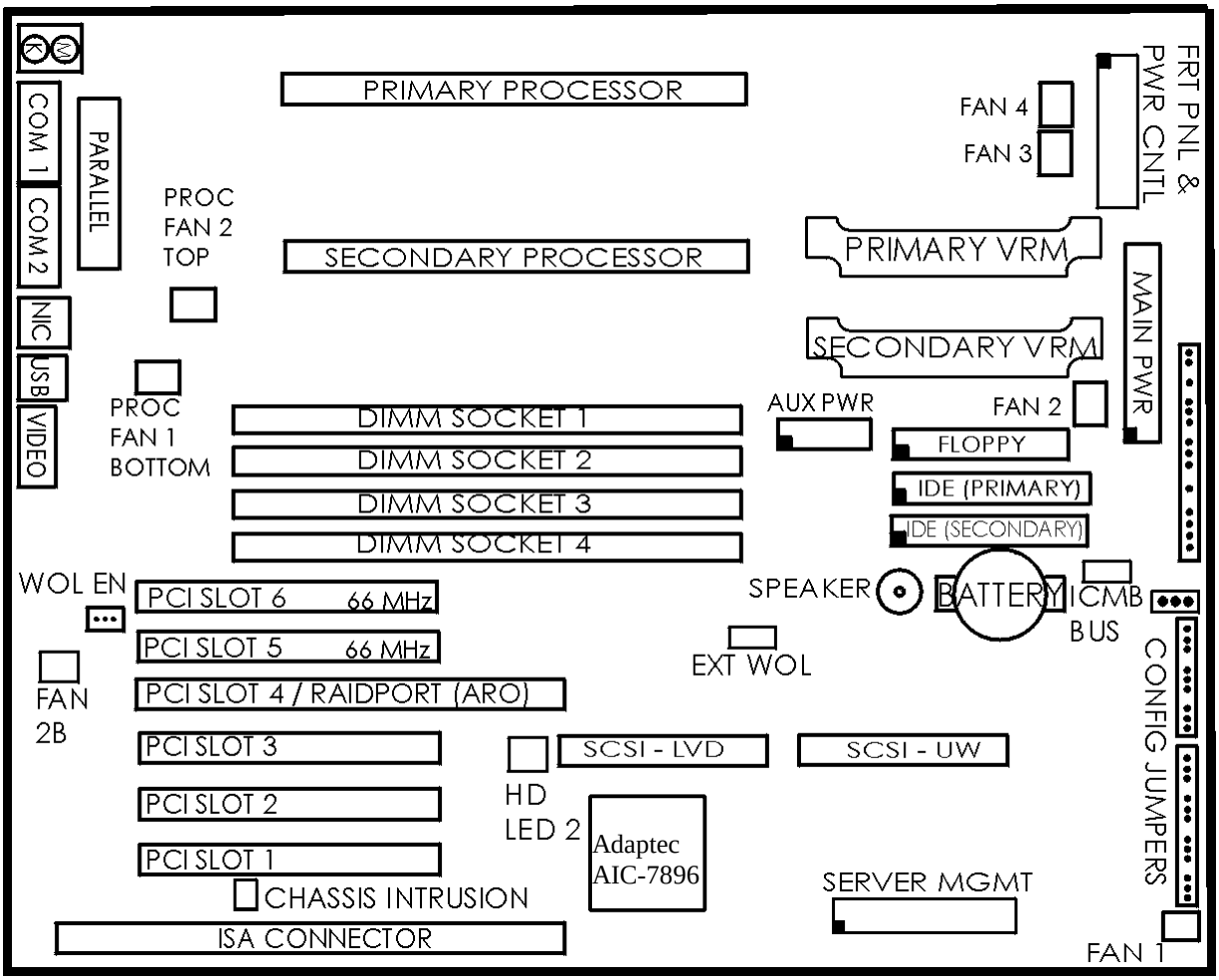


Figure 1-2. C440GX+ Server board Layout

2. Functional Architecture

This chapter describes the operation of each block and associated circuitry, and specifies the pinouts of related connectors. In addition, this chapter provides high level descriptions of functionality distributed between functional blocks (e.g., interrupt structure, clocks, resets, and server management). The following diagram illustrates the functional architecture of the C440GX+ server board.

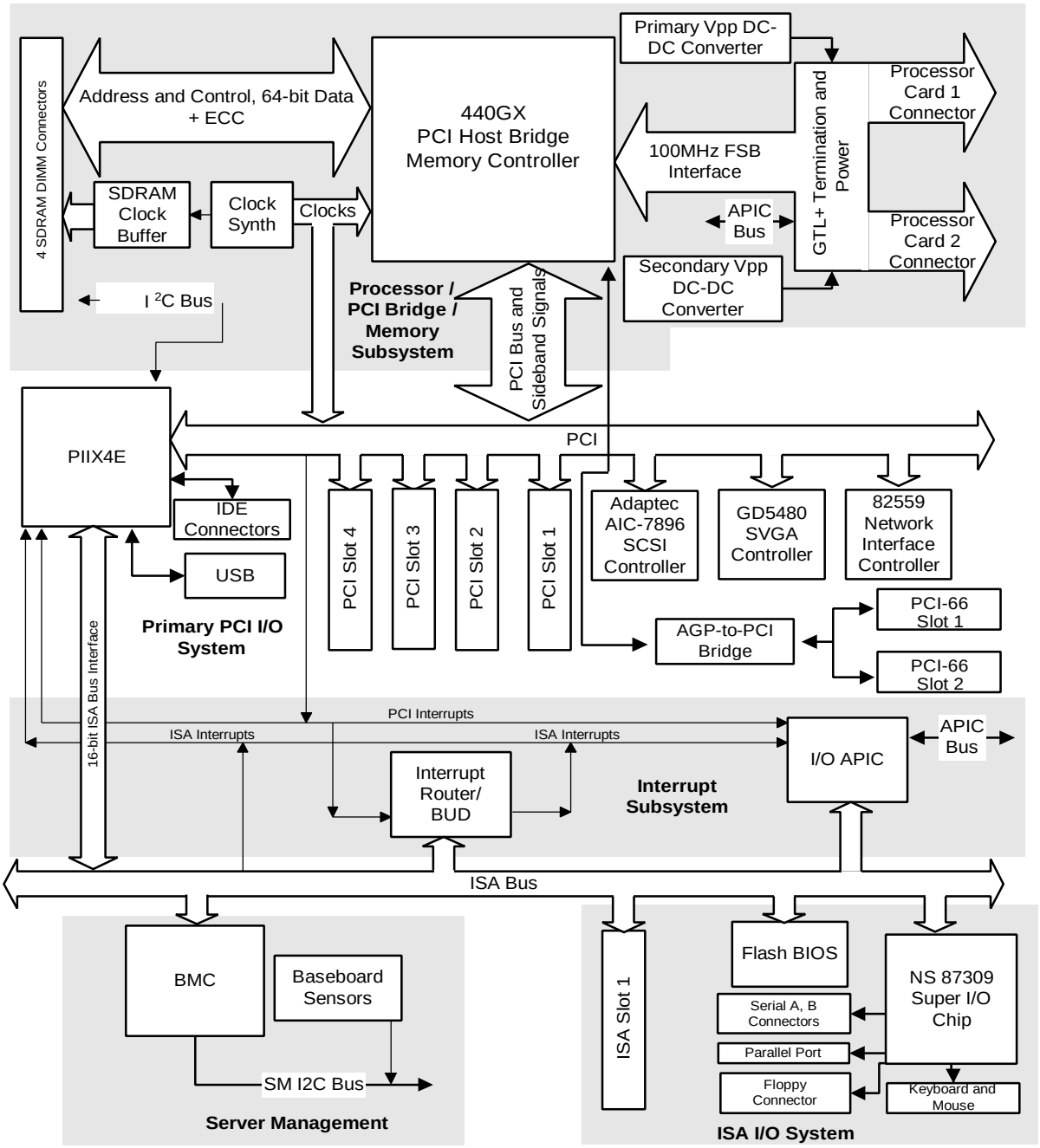


Figure 2-1. C440GX+ Server board Functional Blocks

2.1 Processor/PCI Host Bridge/Memory Subsystem

The processor/PCI bridge/memory subsystem consists of support for 1 to 2 identical Pentium II Xeon or Pentium III Xeon 100MHz FSB processors, and up to 4 SDRAM DIMMs. The support circuitry on the server board consists of the following:

- Intel 82440GX (440GX) PCI host bridge, memory, and power management[2] controller chip.
- Dual 100MHz FSB SC330 slots that accept identical Pentium II Xeon 100MHz FSB or Pentium III Xeon processors (if using 1 processor, a GTL+ terminator card goes in the empty slot).
- Four 168-pin DIMM sockets for interface to SDRAM memory.
- Processor host bus GTL+ support circuitry, including termination power supply.
- 1 Embedded DC-to-DC voltage converter providing VCC_P to the primary core processor.
- 2 voltage regulator slots providing 5 Volt or 12 Volt VRM capability to support:
  - VCCp for single and dual processor L2 caches
  - VCCp to the secondary processor core
- APIC bus.
- Miscellaneous logic for reset configuration, processor card presence detection, and ITP port.

2.1.1 440GX Host Bridge

The 440GX is a 492-pin BGA (Ball Grid Array) device with a 3.3V core and mixed 5V, 3.3V, and GTL+ signal interface pins. The PCI host bridge in the 440GX provides the sole pathway between processor and I/O systems, performing control signal translations and managing the data path in transactions with PCI resources onboard. This includes translation of 64-bit operations in the GTL+ signaling environment at 100MHz, to a 32-bit PCI Rev. 2.1 compliant, 5V signaling environment at 33MHz. The 440GX also handles arbitration for PCI bus master access. For more information on C440GX+ arbitration specifics, refer to "PCI Arbitration" later in this chapter. Although the 440GX is capable of being clocked to operate with multiple processor FSB frequencies, on C440GX+ the host bridge only supports a 100MHz FSB. The device also features 32-bit addressing (not 36-bit), 4 or 1 deep in-order and request queue (IOQ), dynamic deferred transaction support, and Desktop Optimized (DTO) GTL bus driver support (gated transceivers for reduced power operation). The PCI interface provides greater than 100 MB/s data streamlining for PCI to SDRAM accesses (120 MB/s for writes), while supporting concurrent processor host bus and PCI transactions to main memory. This is accomplished using extensive data buffering, with processor-to-SDRAM and PCI-to-SDRAM write data buffering and write-combining support for processor-to-PCI burst writes.

2.1.2 440GX AGP to PCI-66 Bridge

The Intel 21150 AGP-to-PCI-66 bridge chip is a 208-pin PQFP that supports both 5 Volt and 3.3 Volt signaling environments and supplies two 66MHz/32bit PCI Rev. 2.1 compliant slots from the 440GX AGP port. It implements delayed transactions for all PCI configurations, I/O, and memory read commands-up to three transactions simultaneously in each direction. The bridge allows for 88 bytes of buffering (data and address) for posted memory write commands in each direction with up to five write transactions simultaneously in each direction. It additionally allows for 72 bytes of read data buffering in each direction. Concurrent primary (AGP to Bridge) and secondary (Bridge to PCI-66 device) bus operation is done to isolate traffic. It provides 32-bit I/O address range, 32-bit memory-mapped I/O address range, and 64-bit prefetchable memory address range. The 21150 checks, forwards, and generates parity on both the primary and secondary interfaces. To maintain transparency, the 21150 always tries to forward the existing parity condition on one bus to the other along with the address and data.

2 Refer to "Power Management" later in this chapter, for information on how 440GX and PIIX4E power management features are used on C440GX+

2.1.3 440GX Memory Controller

The 440GX performs the function of memory controller for the C440GX+. Total memory of 32MB to 2GB is supported. Although the memory controller supports a variety of memory devices, the C440GX+ implementation only supports PC/100 compliant, 72-bit, unbuffered or registered ECC SDRAM DIMMs or 64-bit, unbuffered, Non-ECC SDRAM DIMMs.

The 440GX provides ECC that can detect and correct single-bit errors (SED/SEC), and detect all double-bit and some multiple-bit errors (DED). Parity checking and ECC can be configured under software control; higher performance is possible if ECC is disabled (1 clock savings). At initial power-up, ECC and parity checking are disabled.

SDRAM Memory DIMM Sites

C440GX+ provides 4 slots that accept 168-pin JEDEC, 3.3V, 72-bit unbuffered or registered ECC SDRAM DIMMs or 64-bit unbuffered Non-ECC SDRAM DIMMs. You cannot use EDO DIMMs, only SDRAM DIMMs are allowed. You can mix various sizes of DIMMs, but you cannot mix unbuffered and registered DIMMs. Best performance is obtained using unbuffered DIMMs. Registered DIMMs stack memory devices on each DIMM for greater memory capacity, but they require additional time (1 clock) for memory accesses. Each DIMM connector has the following pinout:

Table 2-1. Memory DIMM Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	Nc	86	DQ32	128	CKE0
3	DQ1	45	S2_L	87	DQ33	129	S3_L
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vcc	48	Nc	90	Vcc	132	A13
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	Nc	92	DQ37	134	nc
9	DQ6	51	Nc	93	DQ38	135	nc
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	Nc	103	DQ46	145	nc
20	DQ15	62	Nc	104	DQ47	146	nc
21	CB0	63	CKE1	105	CB4	147	REGE
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	Nc	66	DQ22	108	nc	150	DQ54
25	Nc	67	DQ23	109	nc	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0_L	69	DQ24	111	CAS_L	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0_L	72	DQ27	114	S1_L	156	DQ59
31	Nc	73	Vcc	115	RAS_L	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	Nc	122	BA0	164	nc

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
39	BA1	81	WP	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	CK1	167	SA2
42	CK0	84	Vcc	126	A12	168	Vcc

Note: NC = Not Connected

2.1.4 SC330 Connector Interface

The edge connector for both the Pentium II Xeon and Pentium III Xeon processor conforms to the SC330 specification, which can also accommodate future processor cards.

2.1.5 Processor Termination/Regulation/Power

The termination circuitry required by both the Pentium II Xeon and Pentium III Xeon processor bus (AGTL+) signaling environment, and the circuitry to set the AGTL+ reference voltage are implemented directly on the processor cards. The server board provides 1.5V AGTL+ termination power (VTT), and VRM 8.3-compliant DC-to-DC converters to provide processor power (VCCP) at each connector. One integrated VRM and Two VRM sockets are provided on the server board to power the processors, which derive power from either the 5 Volt or 12 Volt supply depending on the type of VRM used. Each processor has a separate VRM to power its core. The VRM integrated into the server board is used for the Primary Processor and the VRM Socket labeled “Secondary VRM” is used for the Secondary Processor. The VRM Socket labeled “Primary VRM” is used to power the L2 cache for both primary and secondary processors and must be populated for both single and dual processor configurations.

Termination Card

If only one processor card is installed in a system, a termination card *must* be installed in the vacant processor slot to start the system. The termination card contains AGTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector. The C440GX+ server board contains circuitry that will prevent the system from booting if a processor slot is left vacant.

2.1.6 APIC Bus

Interrupt notification and generation for dual processors is done using an independent path between local APICs in each processor and the Intel I/O APIC located on the server board. This simple bus consists of 2 data signals and one clock line. PC-compatible interrupt handling is done by the PIIX4E, with all interrupts delivered to the processor via the INTR line. However, reduced interrupt latency is possible when the APIC bus delivers interrupts in uni-processor operation (if supported by the OS). Refer to “Interrupts and I/O APIC” later in this chapter for more information.

2.1.7 Miscellaneous Processor/Memory Subsystem Circuitry

In addition to the circuitry described above, the processor subsystem contains the following:

- Processor core frequency configuration circuitry
- DIMM presence detection and auto-configuration logic
- Processor card presence detection circuitry
- ITP port for boundary scan support.

Processor Core Frequency and Memory Configuration Logic

The PIIX4E provides an independent I^2C segment, the PIIX4E System Management Bus (PIIX4E SMB), supporting an I^2C EEMUX device (PCF8550) for configuration of processor core speed. The PIIX4E I^2C segment also provides access to information stored in I^2C ROMs on installed DIMMs, and control of the SDRAM clock buffer that gates synchronous clocks to each DIMM. This feature allows a defective DIMM to be disabled, and total memory resized automatically. BIOS code controls these features using I^2C operations performed by the PIIX4E. Refer to the “Server Management” section below, for a description of the other two I^2C segments on

C440GX+, and information on how the PIIX4E SMB fits into the overall server management scheme.

Processor Card Presence Detection

Logic is provided on the server board to detect the presence and identity of installed processor or termination cards. A termination card *must* be installed in a vacant processor slot to ensure reliable system operation. If the logic senses an empty processor slot, the installed processor will not be allowed to leave the reset state, preventing operation of the system.

2.2 PCI I/O Subsystem

The primary PCI bus, running at 33 MHz including PCI and PC-compatible I/O, is directed through the PCI interface. On C440GX+, the primary PCI bus supports the following embedded devices and connectors:

- Four 120-pin, 32-bit, PCI expansion slots. Slot 4 is RAID-upgradeable and is designed to support the Adaptec ARO-1130U2 RAID port III card.
- PIIX4E PCI-to-ISA bridge / IDE / USB / Power Management (and PIIX4E SMB) controller
- PCI video controller, Cirrus Logic CL-GD5480
- PCI Ultra2/Ultra SCSI Controller, Adaptec AIC-7896
- PCI Network Interface Controller, Intel 82559

Each device under the PCI host bridge has its IDSEL signal connected to one bit out of the PCI Address/Data lines AD[31::11], which acts as a device select on the PCI bus. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the AD bit to which each IDSEL signal is attached, along with its corresponding device number.

Table 2-2. Primary PCI Configuration IDs

IDSEL Value	Device
20	PCI Slot 4
22	PCI Slot 3
23	SCSI
24	PCI Slot 2
25	NIC
27	PCI Slot 1
29	PIIX4E
31	Video

Table 2-3. Secondary PCI Configuration IDs

IDSEL Value	Device
20	PCI Slot 5
23	PCI Slot 6

2.2.1 PCI Arbitration

The primary PCI bus of the C440GX+ supports 8 PCI masters: NIC, PCI slots 1 through 4, SCSI, PIIX4E, and 440GX (video is always a slave). All PCI masters must arbitrate for PCI access, using resources supplied by both the 440GX and custom arbitration logic. The 440GX uses internal arbitration connections within its host interface, and the PCI interface on the 440GX provides 5 REQ_L/GNT_L pairs for external devices or bridges. Logic in the BUD, which is attached to the REQ4_L/GNT4_L signals, provides support for an additional master on “Round Robin” basis.

One of the arbitration extensions goes to the SCSI controller, which contains an internal arbiter for bus master access to each SCSI interface (LVDS and SE).

The PIIX4E operates with a private arbitration scheme using the 440GX P_PHOLD_L / P_PHOLDA_L signals, so that access time capability for ISA masters is guaranteed.

2.2.2 PCI Connectors

The following table defines the pinout for each 32-bit PCI expansion connector on the C440GX+ server board. Pins are numbered with respect to the module edge connector: B side signals appear on the front (component side) of the expansion board, A side on the back. Signals not connected are labeled with the signal mnemonic followed by "(NC)".

Table 2-4. 32-Bit Primary PCI Connector Signal Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST_L	B1	-12V	A32	AD16	B32	AD17
A2	+12V	B2	TCK	A33	+3.3V	B33	C/BE2_L
A3	TMS	B3	GND	A34	FRAME_L	B34	GND
A4	TDI	B4	TDO (nc)	A35	GND	B35	IRDY_L
A5	+5V	B5	+5V	A36	TRDY_L	B36	+3.3V
A6	INTA_L	B6	+5V	A37	GND	B37	DEVSEL_L
A7	INTC_L	B7	INTB_L	A38	STOP_L	B38	GND
A8	+5V	B8	INTD_L	A39	+3.3V	B39	LOCK_L
A9	Reserved	B9	PRSNT1_L	A40	SDONE	B40	PERR_L
A10	+5V	B10	Reserved	A41	SBO_L	B41	+3.3V
A11	Reserved	B11	PRSNT2_L	A42	GND	B42	SERR_L
A12	GND	B12	GND	A43	PAR	B43	+3.3V
A13	GND	B13	GND	A44	AD15	B44	C/BE1_L
A14	Reserved	B14	Reserved	A45	+3.3V	B45	AD14
A15	RST_L	B15	GND	A46	AD13	B46	GND
A16	+5V	B16	PCICLK	A47	AD11	B47	AD12
A17	GNT_L	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ_L	A49	AD9	B49 *	GND
A19	Reserved	B19	+5V	A50	Connector key	B50	Connector key
A20	AD30	B20	AD31	A51	Connector key	B51	Connector key
A21	+3.3V	B21	AD29	A52	C/BE0_L	B52	AD8
A22	AD28	B22	GND	A53	+3.3V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	+3.3V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	+3.3V	A56	GND	B56	AD3
A26	IDSEL	B26	C/BE3_L	A57	AD2	B57	GND
A27	+3.3V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	+5V	B59	+5V
A29	AD20	B29	AD21	A60	REQ64_L	B60	ACK64_L
A30	GND	B30	AD19	A61	+5V	B61	+5V
A31	AD18	B31	+3.3V	A62	+5V	B62	+5V

* For PCI-66 slot, this pin is M66EN.

2.2.3 RAID-upgradeable PCI Slot

The C440GX+ provides support on PCI slot 4 for a 0-channel SCSI RAID add-in card, the Adaptec ARO-1130U2 RAID port III. This PCI add-in card leverages the onboard SCSI controller chip along with its own built-in intelligence to provide a complete RAID controller subsystem onboard. If no

RAID card is installed, the interrupts pass through the PCI interrupt swizzle. Refer to "Interrupts and I/O APIC" later in this chapter for more information on C440GX+ interrupt structure.

2.2.4 PCI-66 Slots

PCI slots 5 and 6 are designed to support 5 Volt "Universal", 66 MHz, 32-bit, full-length PCI cards. These two slots are part of an isolated PCI peer bus and are interfaced through the 440GX AGP port via an Intel 21150 AGP-to-PCI bridge chip. This peer bus is compliant with version 2.1[3] of the PCI Specification. Standard 33 MHz PCI cards are capable of using slot 5, slot 6, or both. However using these slots for 33 MHz PCI cards will result with the entire peer bus operating at 33 MHz.

> **Note:** Although 33 MHz PCI cards are supported in slots 5 and 6, it is not a recommended configuration. PCI slots 5 and 6 are optimized to run with 66 MHz PCI cards. If 33 MHz PCI cards are used in these slots, they will experience some performance degradation. The amount of performance degradation is dependant on the type of card used and the load on the bus.

2.2.5 PCI Bus Termination

Certain PCI signals on C440GX+ have "functional" termination, i.e., either pull-up or pull-down resistors. In addition, certain PCI signals may require additional termination to meet signal quality requirements. These are driven through the board topology definition and simulation process, and are not specified in this document.

The C440GX+ implementation of TRST_L does not follow the PCI guideline, but instead implements a more robust solution by providing individual pull-down resistors for each slot. This is done to compensate for numerous PCI components that violate the PCI input low leakage current (I_{il}) specification. If an add-in card directly connects the TRST_L pin on one of these components to the PCI connector, the system would not work with that card installed if the TRST_L signals were bussed and the standard pull-down guideline were used.

SBO_L and SDONE are unused on C440GX+, but have separate pull-up resistors for each slot per the PCI specification. PRSNT1_L and PRSNT2_L are also not used, and are terminated on each connector with 0.1µF caps to ground on each slot. ACK64_L and REQ64_L have pull-up resistors since 64-bit PCI is not supported on C440GX+. REQ_L for each slot also has a separate pull-up resistor since these signals are not bussed. Note that REQ_L from onboard PCI components do not require pull-up resistors since they are always driven.

2.2.6 PIIX4E

The PIIX4E is a multi-function PCI device, providing four PCI functions in a single package: PCI-to-ISA bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the PIIX4E has its own set of configuration registers and once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

The PIIX4E is packaged as a 324-pin BGA device. Its primary role is to provide the gateway to all PC-compatible I/O devices and features. The C440GX+ uses the following PIIX4E features:

- PCI interface
- ISA bus interface
- Dual IDE interfaces
- USB interface
- Power management control
- System reset control
- ISA-compatible interrupt control
- PC-compatible timer/counters and DMA controllers

3 The C440GX+ PCI-66 implementation does not follow exactly the PCI specification 2.1 or later: A) AGP is lacking a PCI LOCK# signal; B) PCI slots 5 and 6 use "5V Universal" style PCI connectors to be compatible with both 33 MHz and 66 MHz PCI cards. All other required PCI 2.1 functions are supported.

- Server board plug-n-play support
- General purpose I/O
- Real-time Clock and CMOS configuration RAM.

The following are descriptions of each supported PIIX4E feature and related connector pinouts.

PIIX4E PCI Interface

The PIIX4E fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Rev. 2.1*. On C440GX+ the PCI interface operates at 33 MHz, using the 5 Volt signaling environment.

ISA Interface

Function 0 in the PIIX4E provides an ISA bus interface, operating at 8.33 MHz, that supports one ISA expansion connector, Flash memory, server management interface, and the Super I/O chip (PC87309VLJ). Refer to "ISA I/O Subsystem", later in this chapter, for more information.

PCI Bus Master IDE Interface

Function 1 in the PIIX4E provides a PCI bus master controller for dual IDE channels, each capable of programmed I/O (PIO) operation for transfer rates up to 14 MB/s, and Ultra DMA operation for transfer rates up to 33 MB/s. Each IDE channel supports two drives (0 and 1). Two IDE connectors, each featuring 40 pins (2 x 20), are provided on the server board, each with pinout as specified in the following table. Unused signals are labeled with the signal mnemonic followed by the C440GX+ implementation in parentheses: "p/u" = pull-up resistor, "nc" = no connection

Table 2-5. IDE Connector Pinout

Pin	Name	Pin	Name
1	RESET_L	21	IDEDRQ
2	GND	22	GND
3	DD7	23	DIOW_L
4	DD8	24	GND
5	DD6	25	DIOR_L
6	DD9	26	GND
7	DD5	27	IORDY
8	DD10	28	CSEL (1 KΩ p/d)
9	DD4	29	IDEDAK_L
10	DD11	30	GND
11	DD3	31	IDEIRQ
12	DD12	32	Reserved (nc)
13	DD2	33	IDESA1
14	DD13	34	PDIAG_L (tied to GND)
15	DD1	35	IDESA0
16	DD14	36	IDESA2
17	DD0	37	IDECS1_L
18	DD15	38	IDECS3_L
19	GND	39	IDEHDACT_L
20	Keyed	40	GND

Power Management Controller

One of the embedded functions in the PIIX4E is a power management controller. On C440GX+, power management features are obtained using ACPI-compatible software control. For a

complete discussion of power management architecture on C440GX+, refer to “Power Management” later in this chapter.

Compatibility Interrupt Control

The PIIX4E provides the functionality of two 82C59 PIC devices, for ISA-compatible interrupt handling. For a complete discussion of interrupt handling on C440GX+, refer to “Interrupts and I/O APIC” later in this chapter.

Real-time Clock

The PIIX4E contains an MC14681A compatible real-time clock with battery backup from an external battery. The device also contains 242 bytes of general purpose battery backed CMOS system configuration RAM. On C440GX+, these functions are duplicated in the Super I/O chip. However, the C440GX+ implementation uses the PIIX4E RTC and CMOS facilities.

2.2.7 SCSI Subsystem

The C440GX+ server board provides an embedded dual-channel, PCI SCSI host adapter: Adaptec AIC-7896. The AIC-7896 contains two independent SCSI controllers that share a single PCI bus master interface as a multi-function device, packaged in a 352-pin BGA. Internally, each controller is identical, capable of operations using either 16-bit SE (Ultra) or LVD (Ultra 2) SCSI providing 40 MB/s (Ultra) or 80 MB/s (Ultra2).

	Maximum Transfer Rate				
SCSI Port	**Asynchronous**	**Fast-5**	**Fast-10**	**Fast-20**	**Fast-40**
SE	yes	Yes	yes	yes	no
LVD	yes	Yes	yes	yes	yes

In the C440GX+ implementation, controller A attaches to a 68-pin 16-bit differential SCSI connector LVD interface, controller B attaches to a 68-pin 16-bit single ended (SE) SCSI connector interface. Each controller has its own set of PCI configuration registers (see Chapter 5) and SCSI I/O registers. As a PCI 2.1 bus master, the AIC-7896 supports burst data transfers on PCI up to the maximum rate of 133 MB/sec using on-chip buffers.

Adaptec AIC-7896 PCI Signals

The AIC-7896 supports all of the required 32-bit PCI signals including the PERR_L and SERR_L functions. Full PCI parity is maintained on the entire data path through the chip. The device also takes advantage of PCI interrupt signaling capability, using PCI_INTC_L on the C440GX+ server board. The figure below shows the PCI signals supported by the AIC-7896.

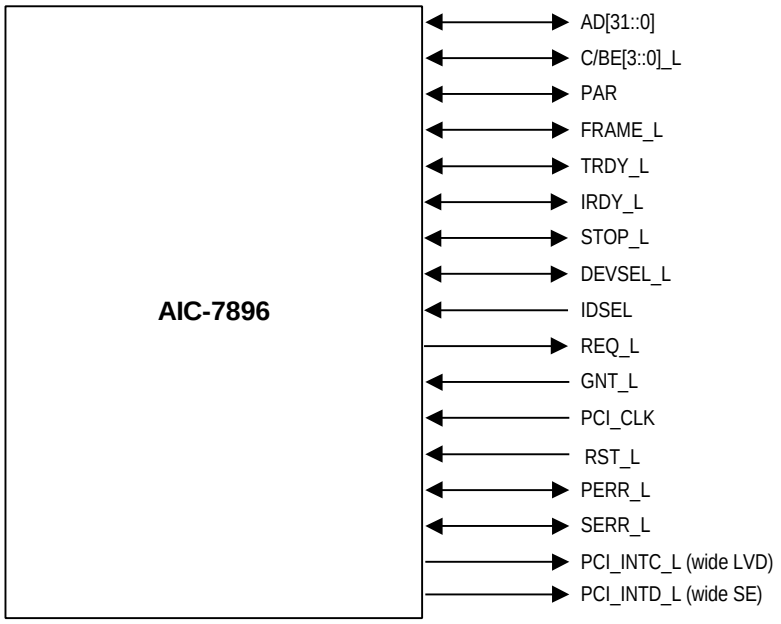


Figure 2-2. Embedded SCSI PCI Signals

AIC-7896 Supported PCI Commands

The AIC-7896 supports PCI commands as shown in the following table:

Table 2-6. Embedded SCSI Supported PCI Commands

C/BE [3::0] _L	Command	AIC-7896 Support	
		Target	Master
0000	Interrupt Acknowledge	No[1]	No
0001	Special Cycle	No[1]	No
0010	I/O Read	Yes[2]	No
0011	I/O Write	Yes[2]	No
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes[2,3]	Yes[4]
0111	Memory Write	Yes[2,3]	Yes[4]
1000	Reserved	No[1]	No
1001	Reserved	No[1]	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	Yes[5]	Yes
1101	Dual Address Cycle	Yes[6]	Yes
1110	Memory Read Line	Yes[5]	Yes
1111	Memory Write and Invalidate	Yes[7]	Yes

Notes:
1. Ignored after checking address parity.
2. Support for 8-bit transfers only for all registers in its device register space.
3. Support for 32-bit transfers only for the external ROM/ EEPROM.
4. Support for transfers from system memory.
5. Defaults to Memory Read.

6. Will respond to DAC if PCI Address matches the MBAR[63:12].
7. Defaults to Memory Write.

The extensions to memory commands (memory read multiple, memory read line, and memory write and invalidate) work with the cache line size register to give the cache controller advance knowledge of the minimum amount of data to expect. The decision to use either the memory read line or memory read multiple commands is determined by a bit in the configuration space command register for this device.

SCSI Interfaces

The AIC-7896 contains two independent SCSI controllers: Channel A for Wide Ultra2 SCSI, Channel B for Wide Ultra SCSI. Each controller supports 8-bit or 16-bit Fast-10 and Fast-20 SCSI operation at data transfer rates of 10, 20, or 40 MB/s. In addition, Channel A supports Fast-40 SCSI operation capable of transfer rates of 80 MB/s. Each maintains its own set of configuration and run-time registers.

Each SCSI interface on the C440GX+ offers active negation outputs, controls for external differential transceivers, a disk activity output, and a SCSI terminator power-down control. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48mA single-ended SCSI bus with no additional drivers (the SCSI segment can handle up to 15 devices). The on board SCSI termination for Channel A, LVD (low voltage differential), may be turned on or off through the SCSI BIOS setup <Cntrl-A> during POST. The on board SCSI termination for Channel B, SE (single ended), is permanently enabled (pull up resistors) and may not be disabled through the SCSI BIOS setup, <Cntrl-A>, during POST. To enter SCSI set up menus, input <CNTRL-A> during POST.

SCSI Bus

The SCSI data bus is 8- or 16-bits wide with odd parity generated per byte. SCSI control signals are the same for either bus width. To accommodate 8-bit devices on the 16-bit Wide SCSI connector, the AIC-7896 assigns the highest arbitration priority to the low byte of the 16-bit word. This way, 16-bit targets can be mixed with 8-bit if the 8-bit devices are placed on the low data byte. For 8-bit mode, the unused high data byte is self-terminated and need not be connected. During chip power-down, all inputs are disabled to reduce power consumption. The following table shows the pinout for the Single-Ended (SE) and LVD SCSI connectors.

Table 2-7. LVD SCSI Connector Pinout

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+DB(12)	18	TERMPWR	35	-DB(12)	52	TERMPWR
2	+DB(13)	19	RESERVED	36	-DB(13)	53	RESERVED
3	+DB(14)	20	GROUND	37	-DB(14)	54	GROUND
4	+DB(15)	21	+ATN	38	-DB(15)	55	-ATN
5	+DB(P1)	22	GROUND	39	-DB(P1)	56	GROUND
6	+DB(0)	23	+BSY	40	-DB(0)	57	-BSY
7	+DB(1)	24	+ACK	41	-DB(1)	58	-ACK
8	+DB(2)	25	+RST	42	-DB(2)	59	-RST
9	+DB(3)	26	+MSG	43	-DB(3)	60	-MSG
10	+DB(4)	27	+SEL	44	-DB(4)	61	-SEL
11	+DB(5)	28	+C/D	45	-DB(5)	62	-C/D
12	+DB(6)	29	+REQ	46	-DB(6)	63	-REQ
13	+DB(7)	30	+I/O	47	-DB(7)	64	-I/O
14	+DB(P)	31	+DB(8)	48	-DB(P)	65	-DB(8)

15	GROUND	32	+DB(9)	49	GROUND	66	-DB(9)
16	DIFFSENS	33	+DB(10)	50	GROUND	67	-DB(10)
17	TERMPWR	34	+DB(11)	51	TERMPWR	68	-DB(11)

Table 2-8. SE SCSI Connector Pinout

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+DB(12)	18	TERMPWR	35	GROUND	52	TERMPWR
2	+DB(13)	19	RESERVED	36	GROUND	53	RESERVED
3	+DB(14)	20	GROUND	37	GROUND	54	GROUND
4	+DB(15)	21	+ATN	38	GROUND	55	-ATN
5	+DB(P1)	22	GROUND	39	GROUND	56	GROUND
6	+DB(0)	23	+BSY	40	GROUND	57	-BSY
7	+DB(1)	24	+ACK	41	GROUND	58	-ACK
8	+DB(2)	25	+RST	42	GROUND	59	-RST
9	+DB(3)	26	+MSG	43	GROUND	60	-MSG
10	+DB(4)	27	+SEL	44	GROUND	61	-SEL
11	+DB(5)	28	+C/D	45	GROUND	62	-C/D
12	+DB(6)	29	+REQ	46	GROUND	63	-REQ
13	+DB(7)	30	+I/O	47	GROUND	64	-I/O
14	+DB(P)	31	+DB(8)	48	GROUND	65	GROUND
15	GROUND	32	+DB(9)	49	GROUND	66	GROUND
16	DIFFSENS	33	+DB(10)	50	GROUND	67	GROUND
17	TERMPWR	34	+DB(11)	51	TERMPWR	68	GROUND

2.2.8 PCI Video

The C440GX+ server board provides a Cirrus Logic CL-GD5480 video controller, along with 2 MB video SGRAM and support circuitry for an embedded SVGA video subsystem. The CL-GD5480 64-bit VGA Graphics Accelerator chip contains an SVGA video controller, clock generator, BitBLT engine, and RAMDAC in a 208-pin PQFP. 256K x 32 SGRAM chips provide 2 MB of 10ns video memory. The SVGA subsystem supports a variety of modes: up to 1600 x 1200 resolution, and up to 16.7 M colors. It also supports analog VGA monitors, single- and multi-frequency, interlaced and non-interlaced, up to 100 Hz vertical retrace frequency. The C440GX+ server board also provides a standard 15 pin VGA connector, and external video blanking logic for server management console redirection support.

Video Chip PCI Signals

The CL-GD5480 supports a minimal set of 32-bit PCI signals since it never acts as a PCI master. As a PCI slave, the device requires no arbitration or interrupt connections.

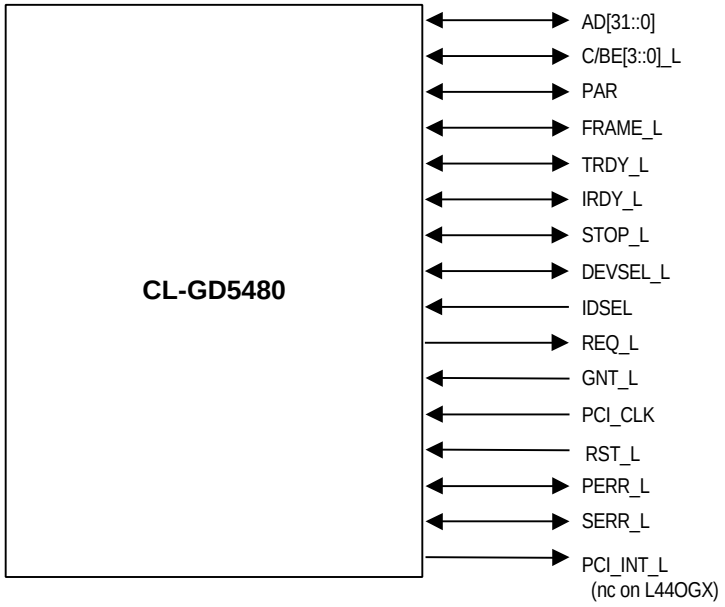


Figure 2-3. Video Controller PCI Signals

Video Controller PCI Commands

The CL-GD5480 supports the following PCI commands:

Table 2-9. Video Chip Supported PCI Commands

		CL-GD5480 Support	
C/BE[3::0]_L	Command Type	Target	Master
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	No
0111	Memory Write	Yes	No
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	No
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	No
1111	Memory Write and Invalidate	No	No

Video Modes

The CL-GD5480 supports all standard IBM VGA modes. Using 2 MB of SGRAM, C440GX+ supports special Cirrus Logic extended modes. The following tables show the standard and extended modes that this implementation supports, including the number of colors and palette size (e.g., 16 colors out of 256 K colors), resolution, pixel frequency, and scan frequencies.

Table 2-10. Standard VGA Modes

Mode(s) in Hex	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	16/256K	360 X 400	14	31.5	70
2, 3	16/256K	720 X 400	28	31.5	70
4, 5	4/256K	320 X 200	12.5	31.5	70
6	2/256K	640 X 200	25	31.5	70
7	Mono	720 X 400	28	31.5	70
D	16/256K	320 X 200	12.5	31.5	70
E	16/256K	640 X 200	25	31.5	70
F	Mono	640 X 350	25	31.5	70
10	16/256K	640 X 350	25	31.5	70
11	2/256K	640 X 480	25	31.5	60
12	16/256K	640 X 480	25	31.5	60
12+	16/256K	640 X 480	31.5	37.5	75
13	256/256K	320 X 200	12.5	31.5	70

Table 2-11. Extended VGA Modes

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Memory Option
58, 6A	16/256K	800 X 600	36	35.2	56	1MB
58, 6A	16/256K	800 X 600	40	37.8	60	1MB
58, 6A	16/256K	800 X 600	50	48.1	72	1MB
58, 6A	16/256K	800 X 600	49.5	46.9	75	1MB
5C	256/256K	800 X 600	36	35.2	56	1MB
5C	256/256K	800 X 600	40	37.9	60	1MB
5C	256/256K	800 X 600	50	48.1	72	1MB
5C	256/256K	800 X 600	49.5	46.9	75	1MB
5C	256/256K	800 X 600	56.25	53.7	85	1MB
5C	256/256K	800 X 600	68.2	63.6	100	1MB
5D	16/256K (interlaced)	1024 X 768	44.9	35.5	43	1MB
5D	16/256K	1024 X 768	65	48.3	60	1MB
5D	16/256K	1024 X 768	75	56	70	1MB
5D	16/256K	1024 X 768	78.7	60	75	1MB
5E	256/256K	640 X 400	25	31.5	70	1MB
5F	256/256K	640 X 480	25	31.5	60	1MB
5F	256/256K	640 X 480	31.5	37.9	72	1MB
5F	256/256K	640 X 480	31.5	37.5	75	1MB
5F	256/256K	640 X 480	36	43.3	85	1MB
5F	256/256K	640 X 480	43.2	50.9	100	1MB

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Memory Option
60	256/256K (interlaced)	1024 X 768	44.9	35.5	43	1MB
60	256/256K	1024 X 768	65	48.3	60	1MB
60	256/256K	1024 X 768	75	56	70	1MB
60	256/256K	1024 X 768	78.7	60	75	1MB
60	256/256K	1024 X 768	94.5	68.3	85	1MB
60	256/256K	1024 X 768	113.3	81.4	100	1MB
64	64K	640 X 480	25	31.5	60	1MB
64	64K	640 X 480	31.5	37.9	72	1MB
64	64K	640 X 480	31.5	37.5	75	1MB
64	64K	640 X 480	36	43.3	85	1MB
64	64K	640 X 480	43.2	50.9	100	1MB
65	64K	800 X 600	36	35.2	56	1MB
65	64K	800 X 600	40	37.8	60	1MB
65	64K	800 X 600	50	48.1	72	1MB
65	64K	800 X 600	49.5	46.9	75	1MB
65	64K	800 X 600	56.25	53.7	85	1MB
65	64K	800 X 600	68.2	63.6	100	1MB
66	32K	640 X 480	25	31.5	60	1MB
66	32K	640 X 480	31.5	37.9	72	1MB
66	32K	640 X 480	31.5	37.5	75	1MB
66	32K	640 X 480	36	43.3	85	1MB
66	32K	640 X 480	43.2	50.9	100	1MB
67	32K	800 X 600	36	35.2	56	1MB
67	32K	800 X 600	40	37.8	60	1MB
67	32K	800 X 600	50	48.1	72	1MB
67	32K	800 X 600	49.5	46.9	75	1MB
67	32K	800 X 600	56.25	53.7	85	1MB
67	32K	800 X 600	68.2	63.6	100	1MB
68	32K (interlaced)	1024 X 768	44.9	35.5	43	2MB
68	32K	1024 X 768	65	48.3	60	2MB
68	32K	1024 X 768	75	56	70	2MB
68	32K	1024 X 768	78.7	60	75	2MB
68	32K	1024 X 768	94.5	68.3	85	2MB
68	32K	1024 X 768	113.3	81.4	100	2MB
6C	16/256K (interlaced)	1280 X 1024	75	48	43	1MB
6D	256/256K (interlaced)	1280 X 1024	75	48	43	2MB
6D	256/256K	1280 X 1024	108	65	60	2MB
6D	256/256K	1280 X 1024	135	80	75	2MB
6D	256/256K	1280 X 1024	157.5	91	85	2MB
6E	32K	1152 X 864	94.5	63.9	70	2MB
6E	32K	1152 X 864	108	67.5	75	2MB
6E	32K	1152 X 864	121.5	76.7	85	2MB
6E	32K	1152 X 864	143.5	91.5	100	2MB
71	16M	640 X 480	25	31.5	60	1MB

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Memory Option
71	16M	640 X 480	31.5	37.9	72	1MB
71	16M	640 X 480	31.5	37.5	75	1MB
71	16M	640 X 480	36	43.3	85	1MB
71	16M	640 X 480	43.2	50.9	100	1MB
74	64K (interlaced)	1024 X 768	44.9	35.5	43	2MB
74	64K	1024 X 768	65	48.3	60	2MB
74	64K	1024 X 768	75	56	70	2MB
74	64K	1024 X 768	78.7	60	75	2MB
74	64K	1024 X 768	94.5	68.3	85	2MB
74	64K	1024 X 768	113.3	81.4	100	2MB
78	32K	800 X 600	36	35.2	56	1MB
78	16M	800 X 600	40	37.8	60	2MB
78	16M	800 X 600	50	48.1	72	2MB
78	16M	800 X 600	49.5	46.9	75	2MB
78	16M	800 X 600	56.25	53.7	85	2MB
78	16M	800 X 600	68.2	63.6	100	2MB
7B	256/256K (interlaced)	1600 X 1200	135	62.5	48	2MB
7B	256/256K	1600 X 1200	162	75	60	2MB
7C	256/256K	1152 X 864	94.5	63.9	70	1MB
7C	256/256K	1152 X 864	108	67.5	75	1MB
7C	256/256K	1152 X 864	121.5	76.7	85	1MB
7C	256/256K	1152 X 864	143.5	91.5	100	1MB
7D	64K	1152 X 864	94.5	63.9	70	2MB
7D	64K	1152 X 864	108	67.5	75	2MB
7D	64K	1152 X 864	121.5	76.7	85	2MB
7D	64K	1152 X 864	143.5	91.5	100	2MB

VGA connector

The following table shows the pinout of the VGA connector:

Table 2-12. Video Port Connector Pinout

Pin	Signal	Description
1	RED	Analog color signal R
2	GREEN	Analog color signal G
3	BLUE	Analog color signal B
4	Nc	No connect
5	GND	Video ground (shield)
6	GND	Video ground (shield)
7	GND	Video ground (shield)
8	GND	Video ground (shield)
9	Nc	No connect
10	GND	Video ground
11	Nc	No connect
12	DDCDAT	Monitor ID data
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync
15	DDCCLK	Monitor ID clock

2.2.9 Network Interface Controller (NIC)

The C440GX+ server board supports a 10BASE-T/100BASE-TX network subsystem based on the Intel 82559 Fast Ethernet PCI Bus Controller. This device is similar in architecture to its predecessor (Intel 82558, except with an integrated physical layer interface. No external devices are required to implement an embedded network subsystem, except TX/RX magnetics, 3 status LEDs, and a connector.

The 82559 is a highly integrated PCI LAN controller in a 208-pin SQFP for 10 or 100 Mbps Fast Ethernet networks. As a PCI bus master, the 82559 can burst data at up to 132 MB/s. This high-performance bus master interface can eliminate the intermediate copy step in RX/TX frame copies, resulting in faster frame processing. The network OS communicates with the 82559 using a memory-mapped I/O interface, PCI interrupt connected directly to the BUD2, and two large receive and transmit FIFOs, which prevent data over runs or under runs while waiting for access to the PCI bus, as well as enabling back to back frame transmission within the minimum 960ns inter-frame spacing. The figure below shows the PCI signals supported by the 82559:

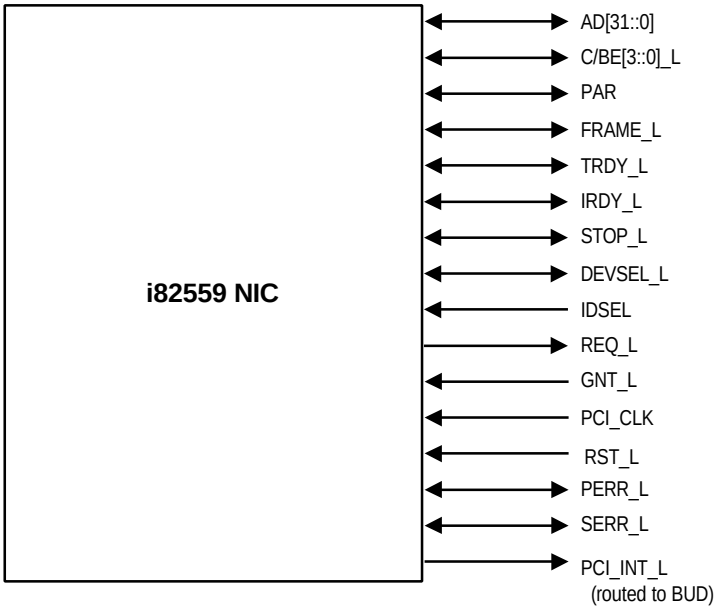


Figure 2-4. Embedded NIC PCI Signals

Supported Network Features

The 82559 contains an IEEE MII compliant interface to the components necessary to implement a IEEE 802.3 100BASE-TX network connection. C440GX+ supports the following features of the 82559 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with PCI Bus Specification, revision 2.1
- 82596-like chained memory structure, with improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- On-chip counters for network management

- Autodetect and auto switching for 10 or 100 Mbps network speeds
- Support for both 10 Mbps and 100 Mbps Networks, full or half duplex-capable, with back-to-back transmit at 100 Mbps
- Integrated physical interface to TX magnetics.
- The magnetics component terminates the 100BASE-TX connector interface. A Flash device stores the network ID.
- **NIC Connector and Status LEDs**

The 82559 drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, valid link to the LAN, and 10/100 Mbps operation. The location and function of each LED is shown in the following figure.

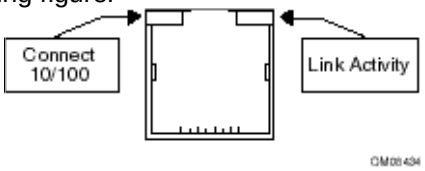


Figure 2-5. NIC Connector and Status LEDs

2.3 ISA I/O Subsystem

On C440GX+, the PIIX4E provides a bridge to an ISA I/O sub-system, that supports the following connectors and devices:

- One ISA slot
- Flash memory for BIOS ROM and extensions
- National Semiconductor PC87309VLJ Super I/O chip, which supports the following:
  - Two PC-compatible serial ports
  - Enhanced parallel port
  - Floppy controller
  - Keyboard/Mouse ports

The ISA I/O subsystem also connects with the Intel I/O APIC and BMC. The I/O APIC relays interrupts produced by ISA devices in dual processor operation (or in uni-processor operation for increased performance with certain OS implementations). The BUD, a programmable logic device, performs rerouting of PCI interrupts as ISA interrupts for MP OS implementations that are not fully MPS 1.4 compatible, and management interrupt (NMI_L and SMI_L) control. Refer to “Interrupts and I/O APIC” later in this chapter for more information on these devices and how they are used in the C440GX+ interrupt structure. The BMC controls server management features on C440GX+. Refer to “Server Management” later in this chapter for details.

2.3.1 ISA Connector

The following table defines the pinout for the expansion connector on C440GX+. Ax and Cx signals appear on the right (processor side of the server board), separated by the keying slot. Bx and Dx signals appear on the left (SCSI side of the server board), separated by the keying slot.

Table 2-13. ISA Connector Signal Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	IOCHK_L	B1	GND	A26	SA5	B26	DACK2_L
A2	SD7	B2	RESET	A27	SA4	B27	TC
A3	SD6	B3	+5V	A28	SA3	B28	BALE
A4	SD5	B4	IRQ9	A29	SA2	B29	+5V
A5	SD4	B5	-5V	A30	SA1	B30	OSC
A6	SD3	B6	DRQ2	A31	SA0	B31	GND
A7	SD2	B7	-12V	Connector key		Connector key	
A8	SD1	B8	SRDY_L	C1	SBHE_L	D1	MEMCS16_L
A9	SD0	B9	+12V	C2	LA23	D2	IOCS16_L
A10	IOCHRDY	B10	GND	C3	LA22	D3	IRQ10
A11	AEN	B11	SMEMW_L	C4	LA21	D4	IRQ11
A12	SA19	B12	SMEMR_L	C5	LA20	D5	IRQ12
A13	SA18	B13	IOW_L	C6	LA19	D6	IRQ15
A14	SA17	B14	IOR_L	C7	LA18	D7	IRQ14
A15	SA16	B15	DACK3_L	C8	LA17	D8	DACK0_L
A16	SA15	B16	DRQ3	C9	MEMR_L	D9	DRQ0
A17	SA14	B17	DACK1_L	C10	MEMW_L	D10	DACK5_L
A18	SA13	B18	DRQ1	C11	SD8	D11	DRQ5
A19	SA12	B19	REFRESH_L	C12	SD9	D12	DACK6_L
A20	SA11	B20	BCLK	C13	SD10	D13	DRQ6
A21	SA10	B21	IRQ7	C14	SD11	D14	DACK7_L
A22	SA9	B22	IRQ6	C15	SD12	D15	DRQ7
A23	SA8	B23	IRQ5	C16	SD13	D16	+5V
A24	SA7	B24	IRQ4	C17	SD14	D17	MASTER16_L
A25	SA6	B25	IRQ3	C18	SD15	D18	GND

2.3.2 ISA Bus Termination

The following table describes the ISA signals which have termination, i.e. either pull-up or pull-down resistors. In addition, certain ISA signals may have additional termination to meet signal quality requirements. Those additional requirements are driven through the board topology definition and simulation process. All signals listed in the table are bussed and contain a single pull-up or pull-down resistor.

Table 2-14. ISA Signal Termination

Signal	Pull-up/Pull-down	Signal	Pull-up/Pull-down	Signal	Pull-up/Pull-down
DRQx	pull-down - 5.6 K Ω	IRQx	Pull-up - 10 KΩ	REFRESH_L	pull-up - 4.7K Ω
IOCHK_L	pull-up - 4.7 KΩ	LA[23::17]	Pull-up - 10 KΩ	SA[19::0]	pull-up - 10 KΩ
IOCHRDY	pull-up - 1 KΩ	MASTER16_L	Pull-up - 1K Ω	SD[15::0]	pull-up - 10 KΩ
IOCS16_L	pull-up - 1K Ω	MEMCS16_L	Pull-up - 1 K Ω	SRDY_L	pull-up - 300 Ω
IOR_L	pull-up - 10 KΩ	MEMR_L	Pull-up - 10 KΩ	SMEMW_L	No Termination
IOW_L	pull-up - 10KΩ	MEMW_L	Pull-up - 10 KΩ	SMEMR_L	No Termination

2.3.3 Compatibility I/O Controller Subsystem

The National PC87309VLJ Super I/O device is a plug and play (PnP) compatible standard I/O subsystem chip, which appears in a 100-pin compact VLJ package. This device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. The C440GX+ server board provides the connector interface for each. In addition, the Super I/O contains a real-time clock, which is unused on C440GX+.

Note: Unlike its predecessor (87307), the PC87309VLJ provides no general purpose I/O bits or programmable chip selects. All GPIOs required by C440GX+ subsystems are supplied by the PIIX4E as specified above. In addition keyboard lock has been removed.

Serial Ports

Two 9-pin D-Sub connectors in a side-by-side housing are provided for Serial ports A and B. Both ports are compatible with 16550A and 16450 UARTs, supporting relocatable I/O addresses. Each serial port can be set to 1 of 4 different COM ports, and can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. The pinout for the connectors is shown below:

Table 2-15. Serial Port Connector Pinout

Pin	Name	Description
1	DCD	Data Carrier Detected
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Return to Send
8	CTS	Clear to Send
9	RIA	Ring Indication Active

Parallel Port

The 25/15 pin high rise connector stacks the parallel port connector over serial port connectors A and B. The 87309 provides an IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS programming of the Super I/O registers enable the parallel port, and determine the port address and interrupt. When disabled, the interrupt is available to add-in cards. Pinout is shown below:

Table 2-16. Parallel Port Connector Pinout

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND

Pin	Name	Pin	Name
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

Floppy Disk Controller

The FDC on the Super I/O is functionally compatible with the PC8477, which contains a superset of the floppy disk controllers in the DP8473 and N82077. The server board provides the 24 MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the Super I/O, including analog data separator and 16-byte FIFO. The floppy disk connector on the server board has the following pinout:

Table 2-17. Floppy Port Connector Pinout

Pin	Name	Pin	Name
1	GND	18	FD_DIR_L
2	FD_DENSEL	19	GND
3	GND	20	FD_STEP_L
4	Nc	21	GND
5	Key	22	FD_WDATA_L
6	FD_DRATE0	23	GND
7	GND	24	FD_WGATE_L
8	FD_INDEX_L	25	GND
9	GND	26	FD_TRK0_L
10	FD_MTR0_L	27	FD_MSEN0
11	GND	28	FD_WPROT_L
12	FD_DR1_L	29	GND
13	GND	30	FD_RDATA_L
14	FD_DR0_L	31	GND
15	GND	32	FD_HDSEL_L
16	FD_MTR1_L	33	GND
17	FD_MSEN1	34	FD_DSKCHG_L

Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single stacked housing. The mouse connector is stacked over the keyboard connector. External to the board they appear as two connectors. The keyboard and mouse controller is software compatible with the 8042AH and PC87911. The keyboard and mouse connectors are PS/2 compatible, with pinout shown below:

Table 2-18. Keyboard Connector Pinout

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	KEYCLK	Keyboard Clock
6	(NC)	

Table 2-19. Mouse Connector Pinout

Pin	Signal	Description
1	MSEDAT	Mouse Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	MSECLK	Mouse Clock
6	(NC)	

2.3.4 Flash ROM BIOS

An 8Mbit flash memory (Intel 28F008S5) provides non-volatile storage space for BIOS and general purposes, packaged as a 40-lead TSOP. The device is byte wide, of the Smart 5 Flash File family and symmetrically blocked. The Flash device is directly addressed as 16 64-kbyte blocks of 8-bit ISA memory.

Secure Flash Programming Mechanism

On C440GX+, the BUD detects any write operation to Flash and asserts SMI_L. The SMI_L handler (part of BIOS) then looks for a signature from the Flash Memory Update utility (FMUP) before allowing any writes to Flash. This prevents accidental loading of non-compatible BIOS code into Flash.

2.4 System Reset Control

Reset circuitry on the C440GX+ server board monitors resets from the front panel, PIIX4, I/O controller, and processor subsystem and determines proper reset sequencing for all types of resets. The system reset logic is designed to accommodate a variety of resets, which can be divided into the following categories:

Power-up reset

Hard reset

Soft (programmed) reset

2.4.1 Power-up Reset

Power-up reset occurs on the initial application of power to the system. The power supply asserts its "power good" signal within 400 to 2000ms of its output voltages being stable. The BMC monitors this signal, and asserts its power good output 30 to 40ms after detecting the power supply's power good signal asserted (the onboard VRMs are guaranteed to provide stable processor power 30 to 40ms after the main power is stable).

2.4.2 Hard Reset

Hard reset may be initiated by software, or by the user resetting the system through the front panel. For software initiated hard reset, the PIIX4E Reset Control register should be used. The front panel reset is routed to the PIIX4E through the reset and power micro-controller. Both sources of hard reset cause the PIIX4E to assert ISA bus reset (RST_RSTDRV) and PCI reset (RST_P_RST_LB). RST_RSTDRV resets the ISA subsystem, while RST_P_RST_L resets the PCI bus. The 440GX receives the PCI reset signal and propagates it to the processor subsystem

2.4.3 Soft Reset

Soft resets may be generated by the keyboard controller (RST_KB_L), or by the chipset in the processor subsection (RST_INIT_REQ_L). The two sources of soft reset are combined in the reset

logic, and routed to the processor subsection via the RST_INIT_CPU_L signal. Soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers.

A programmed reset may be initiated by software. Although reset control is provided by registers in the 440GX, the chip's documentation recommends that registers in the 440GX use the PIIX4E Reset Control register used instead for programmed resets.

The system BIOS will perform the same system reset functions for soft resets as it does for hard resets.

2.4.4 Reset Diagram

Reset flows throughout the C440GX+ server board as shown in the following figure.

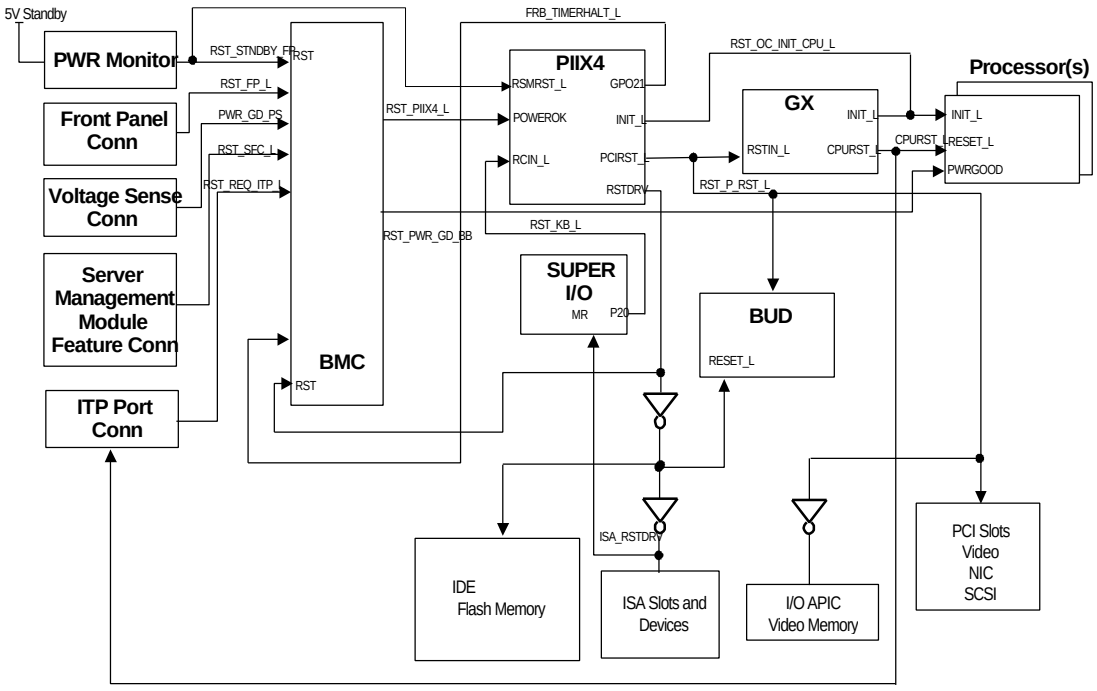


Figure 2-6. Reset Flow Diagram

2.5 Clock Generation and Distribution

All buses on C440GX+ operate using synchronous clocks. Clock synthesizer/driver circuitry on the server board generates clock frequencies and voltage levels as required, including the following:

100 MHz at 2.5V logic levels - Both SC330 connectors, the 440GX, the ITP port

100 MHz at 3.3V logic levels - SDRAM DIMMs

33.3 MHz at 3.3V logic levels - Reference clock for the PCI bus clock driver

16.6 MHz at 2.5V logic levels - Processor and I/O APIC bus clock

There are 4 main synchronous clock sources on the C440GX+ server board: 100MHz host clock generator for processors, clock buffer for SDRAM, 48 MHz clock for PIIX4E and Super I/O chips, 33.3 MHz PCI reference clock, and 16.6 MHz APIC and ISA clocks. In addition, C440GX+ provides asynchronous clock generators: 40 MHz clock for the embedded SCSI controller, 32 KHz clock for

the PIIX4E RTC, 22.1 MHz clock for the BMC, and a 25 MHz clock for the NIC. The following figure illustrates clock generation and distribution on the C440GX+ server board.

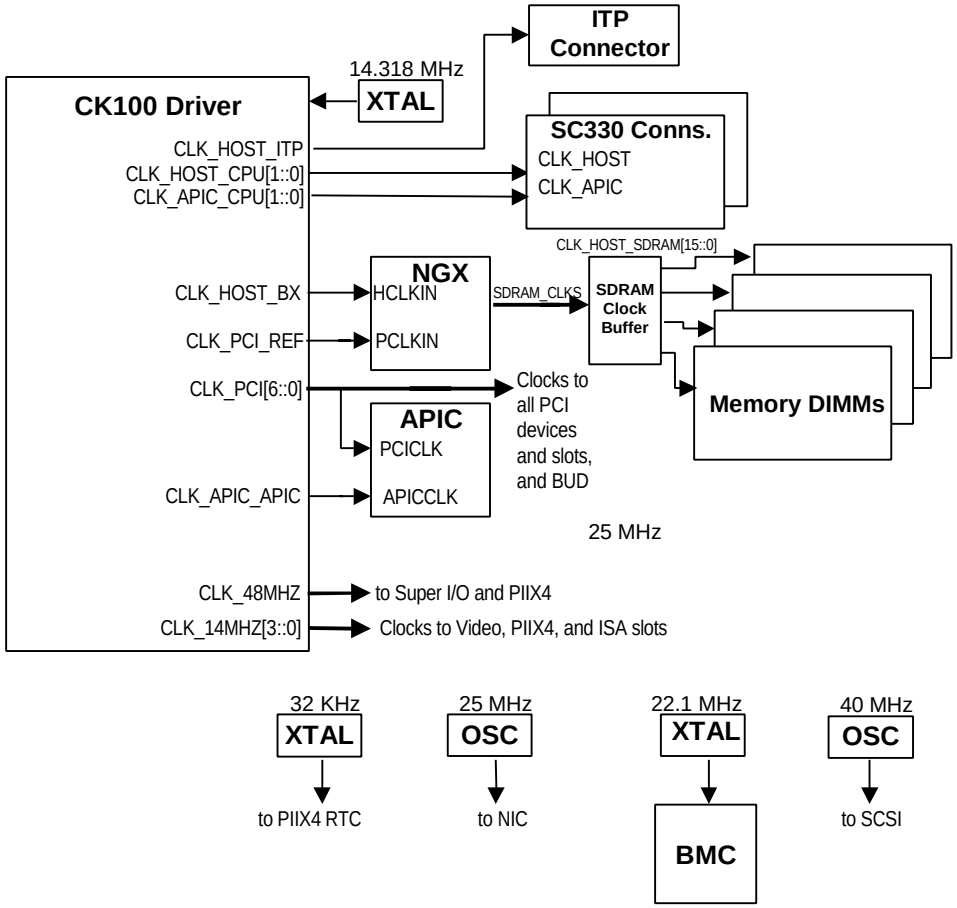


Figure 2-7. C440GX+ Server board Clock Generation and Distribution

2.6 Interrupts and I/O APIC

The C440GX+ interrupt architecture accommodates both PC-compatible PIC mode, and dual-processor APIC mode interrupts. In addition, the C440GX+ provides a PCI to ISA interrupt rerouting mechanism for compatibility with some multiprocessor operating systems that do not fully support the APIC.

2.6.1 PIIX4E Compatibility Interrupt Controller

For PC-compatible mode, the PIIX4E provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The PIIX4E and Super I/O contain configuration registers that define which interrupt source logically maps to I/O APIC INTx pins. In PIC mode, the PIIX4E provides a way to direct PCI interrupts onto one of the interrupt request levels 1-15. Note that this is only useful in compatibility mode since the redirected interrupts are not sourced on the outputs of the PIIX4.

2.6.2 Intel I/O APIC

For APIC mode, C440GX+ interrupt architecture incorporates the Intel I/O APIC device, to manage and broadcast interrupts to local APICs in each processor. The I/O APIC monitors interrupt requests from devices, and on occurrence of an interrupt sends a message corresponding to the interrupt via the APIC bus to each local APIC. The APIC bus minimizes interrupt latency time for compatibility interrupt sources, in both single and dual processor operation. The I/O APIC can also supply greater than 16 interrupt levels to the processor(s). The APIC bus consists of an APIC clock, and two bi-directional data lines.

C440GX+ APIC structure consists of a single I/O APIC device with 24 input interrupt requests. Compatibility interrupt levels 0 through 15 appear on inputs 0 through 15. The I/O APIC also manages 8 interrupt levels associated with PCI interrupts: PCI interrupts A through D are routed to APIC inputs 16 through 19. This supports more efficient interrupt processing. The PIIX4E also contains I/O APIC features that are not used in the C440GX+ platform.

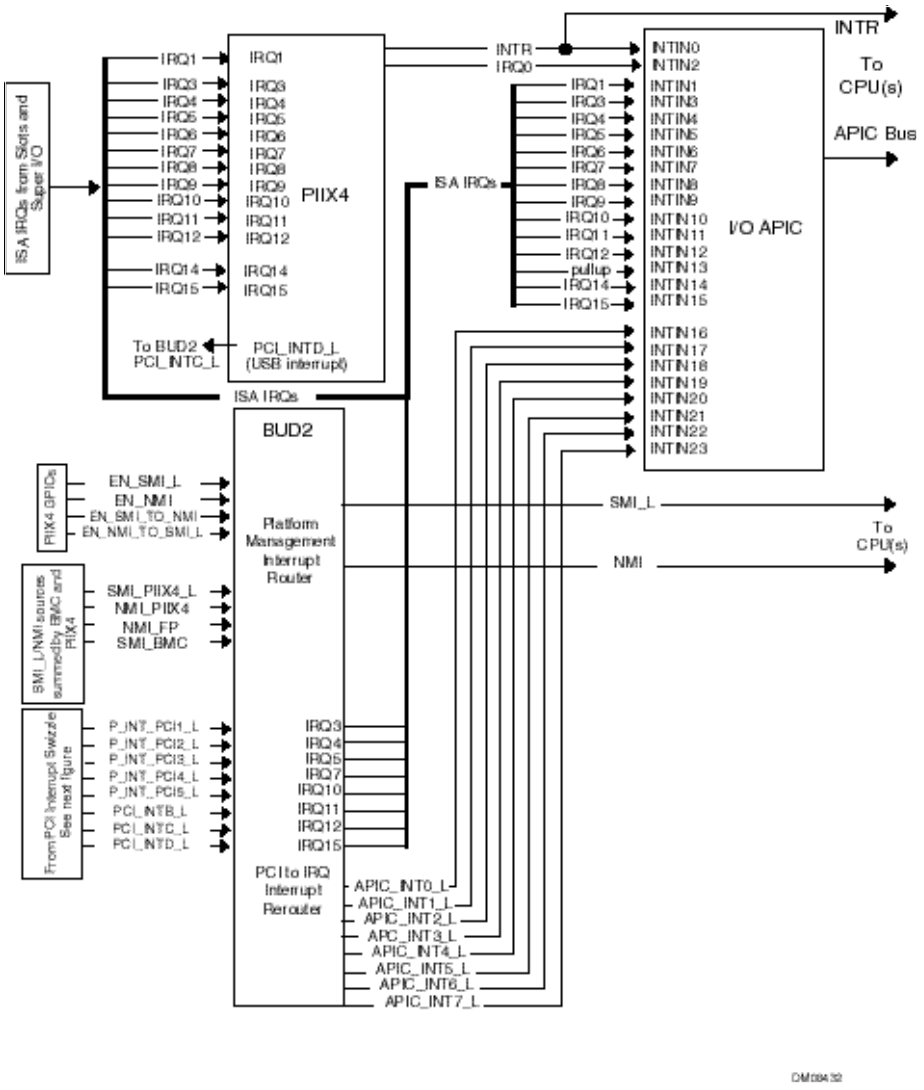


Figure 2-8. C440GX+ Interrupt Structure

2.6.3 Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on C440GX+. The actual interrupt map is defined using configuration registers in the PIIX4E and the I/O controller, and PCI to IRQ interrupt rerouter in the BUD. I/O Redirection Registers in the I/O APIC are provided for each interrupt signal, which define hardware interrupt signal characteristics for APIC messages sent to local APIC(s). Use the information provided in this table to determine how to program each interrupt.

Table 2-20. Interrupt Definitions

Interrupt	I/O APIC level	Description
INTR	INT0	Processor interrupt
NMI		NMI from BUD to processor
IRQ0	INT2	Timer interrupt from PIIX4
IRQ1	INT1	Keyboard interrupt
IRQ2		Interrupt signal from second 8259 internal to PIIX4
IRQ3	INT3	Serial port A or B interrupt from 87309VLJ device, user-configurable.
IRQ4	INT4	Serial port A or B interrupt from 87309VLJ device, user-configurable.
IRQ5	INT5	
IRQ6	INT6	Floppy disk
IRQ7	INT7	Parallel port
IRQ8_L	INT8	RTC interrupt
IRQ9	INT9	ACPI
IRQ10	INT10	
IRQ11	INT11	
IRQ12	INT12	Mouse interrupt
	INT13	
IRQ14	INT14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	INT15	Secondary IDE interrupt
PCI_INTA_L	INT16	PCI Interrupt signal A
PCI_INTB_L	INT17	PCI Interrupt signal B
PCI_INTC_L	INT18	PCI Interrupt signal C
PCI_INTD_L	INT19	PCI Interrupt signal D
SMI_L		System Management Interrupt. General-purpose error indicator from various sources. Controlled by BUD2.

2.6.4 PCI Add-in Card Slot Interrupt Sharing

The following figure shows how PCI interrupts, shared between slots and embedded controllers, are routed to the BUD. The BUD manages each PCI_INT_A from each slot, cascaded PCI_INTs B through C from each slot, and PCI interrupts from SCSI and NIC devices, to avoid conflicts (since most PCI cards use PCI_INTA_L as their interrupt pin). The arrows indicate the direction of interrupt flow from slot to slot, with final destination at the BUD interrupt inputs. The BUD then delivers each interrupt to the appropriate PIIX4E compatibility IRQ and I/O APIC INTIN pins.

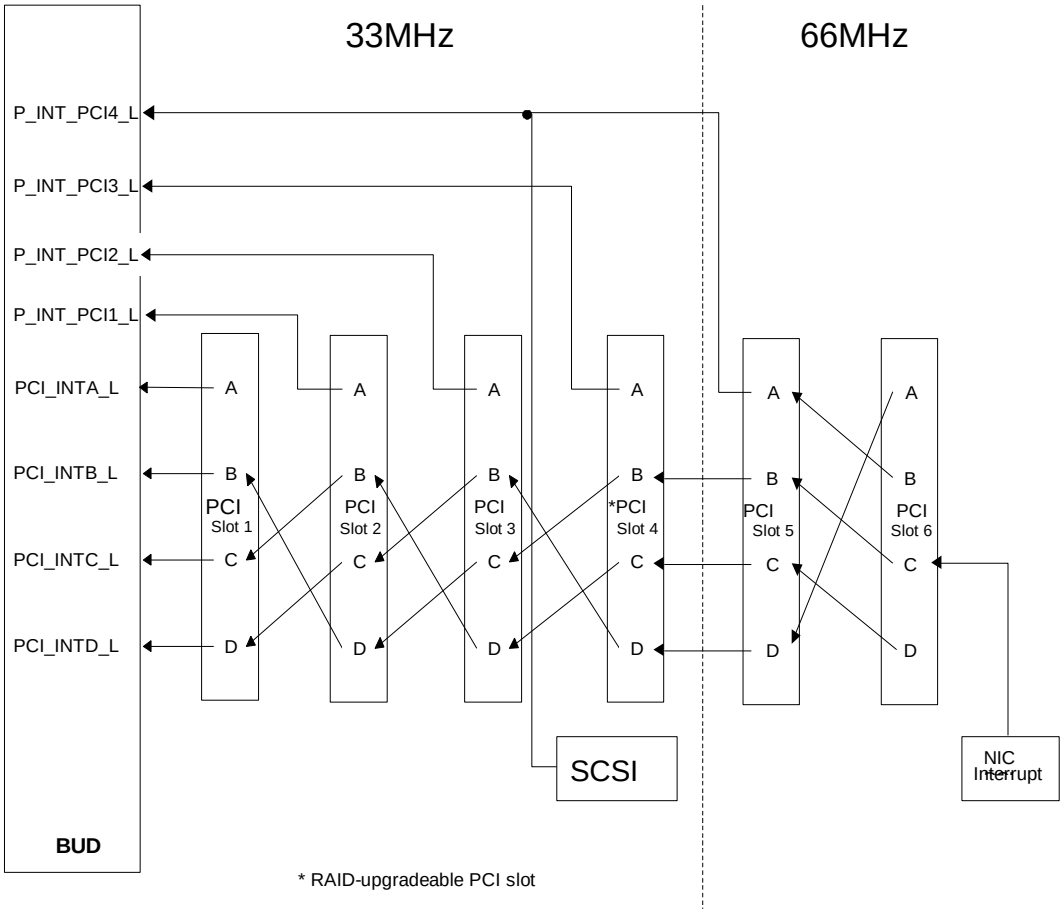


Figure 2-9. PCI Slot Interrupt Swizzle

2.6.5 PCI Interrupt Rerouting

Some multiprocessor operating systems are unable to handle interrupts from PCI slots and devices as pure PCI interrupts, via inputs 16-19 (allocated to PCI) of the I/O APIC. Rather, they expect PCI interrupts to be delivered as ISA IRQs. Multiprocessor operating systems may also expect some interrupts from the PC-compatible PIC in the PIIX4, and others from the I/O APIC (Mixed Mode). Some device drivers check whether the device uses one of the traditional IRQs, and if not (when the PCI interrupt is connected directly to the I/O APIC), the driver fails to install or run properly. The PIIX4E performs internal PCI to IRQ interrupt steering so that PCI interrupts can be delivered to the PIC. However, the PCI interrupt steering feature is unidirectional, which means that it cannot redirect PCI interrupts to the I/O APIC.

For these reasons, C440GX+ incorporates an external PCI to IRQ rerouter circuit in the BUD2, that can be programmed to pass PCI interrupts through to inputs 16-19 of the I/O APIC, or deliver a specific PCI interrupt to an ISA IRQ. Under software control, a PCI interrupt can be individually rerouted to an ISA IRQ signal. This functionality is contained in the BUD.

Two 8-bit registers are provided in the rerouter circuit, with each nibble of a register controlling a specific PCI Interrupt line via PIO commands. The PIIX4E decodes the address of the PIO command and produces a chip select, which is controlled using the PIIX4E Programmable Chip Select Control register (78h - 79h). The rerouter uses only 2 bytes of the minimum 4 selectable, so aliases are provided.

2.6.6 System Management Interrupt Handling

The C440GX+ is designed to report these types of system errors: ISA bus, PCI bus, ECC memory, and System limit. Errors are reported by the BMC and PIIX4E using SMI_L. SMI is used for server management and advanced error processing. All errors can be intercepted by SMI for preprocessing (if SMI_L is enabled), or handled directly by NMI handlers. Some errors have to generate a NMI even if they are intercepted by the SMI, because the traditional way to handle errors in PC architecture is via the NMI. NMI/SMI handling logic in the BUD emulates non-ISA errors as ISA-compatible using NMI and SMI_L. Refer to “Server Management” later in this chapter.

2.6.7 Basic Utility Device (BUD)

In addition to the PCI arbitration and interrupt rerouting functions described above, the BUD also gates and redirects SMI_L and NMI to generate SERR_L, and performs other miscellaneous logic functions (e.g., PCI arbitration expansion). The BUD contains an I/O mapped ISA interface for control of PCI-to-IRQ interrupt rerouting.

2.7 ACPI Power Management

The Advanced Configuration and Power Interface (ACPI) is the key element in implementing Operating System Power Management (OSPM). ACPI is intended for industry wide adoption in order to encourage hardware and software vendors to implement ACPI-compatible (and, thus, OSPM-compatible) systems**.** The C440GX+ server board will be ACPI compliant as defined by the ACPI 1.0 and the Server Design Guide (SDG) 1.0 "Basic Server" specifications. ACPI covers more than just power management, but it is only the Power management aspect of the specification that affects the hardware implementation. This section will describe how the C440GX+ server board implements each requirement of the specification.

2.7.1 ACPI states

Under ACPI, a system can be defined to be in one of several power states. Power states are used to define the level of power savings and the latency of waking up the system to a fully on condition.

ACPI Global State Definitions

G0 - Working:

A computer state, where the system dispatches user mode (application) threads and they execute. In this state, devices (peripherals) dynamically have their power state changed. The user will be able to select (through some user interface) various performance/power characteristics of the system to have the software optimize for performance or battery life. The system responds to external events in real time. It is not safe to disassemble the machine in this state.

On the C440GX+ server board, with full power is applied to the system, the OS may halt one or both of the Processors by issuing a HALT instruction. BIOS should program the Processor to achieve the lowest possible power mode when in at a HALT instruction. The OS can also put embedded devices and plug-in controllers into a lower power mode if their device driver so allows. OS idle policy could be set up to spin disk drives down to save additional power after long periods of idleness. This would increase the recovery latency if disk activity were required.

See the section below labeled "ACPI Processor Power State Definitions" for a description of how each G0 Power State is implemented on the C440GX+.

G1/S4 Non-Volatile Sleeping:

A state where the computer consumes a small amount of power, user mode threads are *not* being executed, and the system "appears" to be off (from an end user's perspective, the display is off, fans stop running etc.). The SDG 1.0 specification requires that a system implement specific sleep states depending on the level of the SDG 1.0 specification the board will adhere to.

The C440GX+ server board is designed to meet the SDG 1.0 "Basic Server" specification. Under this specification, the board must support an S4 Non-Volatile sleep state, that allows system context to be saved and restored (relatively slowly) when power is lost to the server board. To support this state, the server board will provide the means for the PIIX4 to send STPCLK to both processors, blank the console (already present as part of the security screen blank), and power down the system fans. The SCSI controller must supply a means for commanding the disk drives to power down, as they are a major consumer of power and a producer of noise. The hardware will provide a signal to the BMC so that the power LED can be blinked to indicate the system is in a sleeping state.

If the system has been commanded to enter the S4 sleeping state, the hardware and OS will write the system context to a non-volatile storage file and leave appropriate context markers. The machine will then enter the S4 sleeping state. When the system leaves the Soft Off or mechanical Off state, transitioning to the working (G0) state and restarting the OS, a restore from a NVS file can occur. This will only happen if a valid NVS data set is found, certain aspects of the configuration of the machine have not changed, and the user has not manually aborted the

restore. If all these conditions are met, as part of the OS restarting, it will reload the system context and activate it. The net effect for the user is what looks like a resume from a sleeping (G1) state (albeit slower). The aspects of the machine configuration that must not change, include but are not limited to disk layout and memory size. However, it may be possible for the user to swap a PC Card or a Drive Bay device. In the S4 sleeping state, the power supply is turned off so only the 5V Standby voltage rail will be available to power the system board. All S4 sleeping state resume events have to be powered from 5V Standby. The OS could also be commanded to perform this operation from the user interface. The system can be manually woken up via the front panel power button, or, via one of the predefined ACPI wake events.

The latency for returning to the Working state varies on the wakeup environment selected prior to entry of this state (for example, should the system answer phone calls, etc.). It is not safe to disassemble the machine in this state

Optional “Basic Server” S1, S2, and S3 sleep states are not supported.

G2/S5 - Soft Off:

The S5 sleeping state is similar to the S4 sleeping state except neither the hardware nor the OS will save any system context or enable any devices to wake the system. The system is in the “soft” off state and requires a complete boot when awakened. Software uses a different state value to distinguish between the S5 sleeping state and the S4 sleeping state in order to allow for initial boot operations within the BIOS to distinguish whether or not the boot is going to wake from a saved memory image. This state requires a large latency in order to return to the working state.

The C440GX+ server board will support a S5 Soft-off. The system can be manually, or via Software, be turned off without a save to disk. It is not safe to disassemble the machine in this state.

G3 - Mechanical Off:

A computer state that is entered through mechanical means (i.e.: switching off the power supply or removing power cord). Various government agencies and countries require this operating mode. It is implied by the entry of this off state through a mechanical means that no electrical current is running through the boards circuitry and it can be worked on without damaging the hardware or endangering the service personnel. The OS must be restarted to return to the working state. No hardware context is retained. Except for the real time clock, power consumption is zero.

On the C440GX+ server board, if the A/C cord is removed from the wall or power supply, There will be no 5 Volt Standby present on the server board. The only power remaining is that provided by the on board battery for the RTC function inside the PIIX4.

Table 2-21. Summary of Global Power States

Global System State	Software Runs	Latency	Power Consumption	OS restart required	Safe to disassemble computer	Exit state electronically
G0 – Working	Yes	0	Large	No	No	Yes
G1 – Sleeping	No	>0, varies with sleep state.	Smaller	No	No	Yes
G2/S5 – Soft Off	No	Long	Very near 0	Yes	No	Yes
G3 – Mechanical Off	No	Long	RTC battery	Yes	Yes	No

Note that the entries for G2/S5 and G3 in the Latency column of the above table are “Long.” This implies that a platform designed to give the user the appearance of “instant-on,” similar to a home appliance device, will use the G0 and G1 states almost exclusively (the G3 state may be used for moving the machine or repairing it).

ACPI Processor Power State Definitions

Processor power states (Cx states) are processor power consumption and thermal management states within the global working state, G0. The Cx states are briefly defined below.

C0 Processor Power State:

While the processor is in this state, it executes instructions normally.

C1 Processor Power State

This processor power state has the lowest latency, The hardware latency on this state is required to be low enough that the operating software does not consider the latency aspect of the state when deciding whether to use it. Aside from putting the processor in a non-executing power state, this state has no other software-visible effects. On the C440GX+, a “halt” command is executed when this power state is used.

C2 Processor Power State:

The C2 power state offers improved power savings over the C1 power state. The worst-case hardware latency for this state is declared in the FACP table which the operating software can use to determine when the C1 power state should be used instead of the C2 power state. Aside from putting the processor in a non-executing power state, this state has no other software-visible effects. On the C440GX+ server board, this state cannot be supported as part of the global system state G0 as it requires the PIIX4 to supply separate STPCLK signals and control registers for each processor. The C2 ‘Stop Clock’ state can only be supported as a by-product of entering a G1/S1 sleeping state.

C3 Processor Power State:

The C3 power state offers improved power savings over both the C1 and C2 power states. The worst-case hardware latency for this state is declared in the FACP table, which the operating software can use to determine when the C2 power state should be used instead. While in the C3 power state, the processor’s L1 and L2 caches maintain their state but ignore any snoops. The operating software is responsible for ensuring that the L1 and L2 caches maintain coherency. On the C440GX+ server board, this state cannot be supported as part of the global system state G0 as it requires the PIIX4 to supply separate STP_CPU signals and control registers for each processor.

Device Power State Definitions

Device power states are states specific to particular devices; as such, they are generally *not* visible to the user. For example, some devices may be in the Off state even though the system as a whole is in the Working state.

Device power states apply to any device on any bus. They are generally defined in terms of four principal criteria:

- Power consumption - how much power the device uses.
- Device context - how much of the context of the device is retained by the hardware. The OS is responsible for restoring any lost device context (this may be done by resetting the device).
- Device driver - what the device driver must do to restore the device to full on.
- Restore time - how long it takes to restore the device to full on.

The device power states are defined below. These states are defined very generically here. Many devices do not have all of the four power states defined above. Devices may be capable of several different low power modes, but if there is no user-perceptible difference between the modes only the lowest power mode will be used. The *Device Class Power Management Specifications*, which are separate from this specification, describe which of these power states are defined for a given type (class) of device and define the specific details of each power state for that device class.

D3 - Off:

Power has been fully removed from the device. The device context is lost when this state is entered so the OS will reinitialize the device when power is restored. Since device context and power are lost, devices in this state do not decode their address lines. Devices in this state have the longest restore times. This state is defined for all classes of devices. All embedded devices on the C440GX+ server board support this device power state in order to support the G1/S4 sleep state

D2:

Each class of device defines how the D2 device state is implemented. For some device classes it may not be defined at all. In general, the D2 device state is expected to save more power and preserve less device context than a D1 or D0 device state. Buses in the D2 device state may cause the device to loose some context (i.e., by reducing power on the bus, thus forcing the device to turn off some of its functions). The embedded controllers on the C440GX+ do not support this state.

D1:

Each class of device defines how the D1 device state is implemented. For some device classes it may not be defined at all. In general, the D1 device state is expected to save less power and preserve more device context than the D2 device state. On the C440GX+ server board, no special hardware support is provided. None of the embedded controllers on the server board support this device state.

D0 - Fully-On:

This state is assumed to be the highest level of power consumption. The device is completely active and responsive, and is expected to continuously remember its entire relevant context. On the C440GX+ server board all embedded PCI devices on the server board support this device state.

Table 2-22. Summary of Device Power State

Device State	Power Consumption	Device Context Retained	Driver Restoration
D0 - Fully-On	As needed for operation.	All	None
D1	D0>D1>D2>D3	>D2	<D2
D2	D0>D1>D2>D3	<D1	>D1
D3 – Off	0	None	Full init and load

Note: Devices often have different power modes within a given state. Devices can use these modes as long as they can automatically switch between these modes transparently from the software, without violating the rules for the current D*x* state the device is in. Low power modes that affect performance, (i.e., low speed modes) or, that are not transparent to software, cannot be done automatically in hardware; the device driver must issue commands to use these modes

Dual processor ACPI States and approximate power consumption

Table 2-23. Dual processor Power Consumption during ACPI Global States

	Processor-state		Memory		Saved to Disk	Disk Spin		Server board Power	System Power	ACPI Mode	Power
G0/S0	Run-C0	56W	Active	26W	N/A	Spin	65W	16W	ON		163
G0/S1	Halt-C1	5W	Refresh	20W	N/A	Spin	65W	12W	ON		102
G0/S1	Halt-C1	5W	Refresh	20W	N/A	Spin down	27W	12W	ON		64
G1/S1	Stopclk-C2	5W	Refresh	20W	NO	Spin	65W	6W	ON		96
G1/S1	Stopclk-C2	5W	Refresh	20W	NO	Spin down	27W	6W	ON		58
G1/S4	OFF	0W	OFF	0W	YES	OFF	0W	0W	5V Standby		0
G2/S5	OFF	0W	OFF	0W	NO	OFF	0W	0W	5V Standby		0
G3/S4	OFF	0W	OFF	0W	YES	OFF	0W	0W	NONE		0
G3/S5	OFF	0W	OFF	0W	NO	OFF	0W	0W	NONE		0

Table 2-24. C440GX+ server board ACPI State Transitions

G0/S0 >	G3/S5 Loss of A/C	> G0/S0 Restore A/C		
G0/S0 >	G2/S5 Power off	> G3/S5, Loss A/C	> G2/S5 Power off	>G0 restore system
G0/S0 >	G1/S4 NV-Sleep, save to disk	> G3/S4 Lose A/C > G0 Wake-On-LAN > G0 Wake on Ring > G0 RTC Wakeup > G0 P/S ON	> G1/S4 restore A/C	> G0 Wake-On-LAN > G0 Wake on Ring > G0 RTC Wakeup > G0 P/S ON
G0/S0 >	G1/S1 Sleeping	> G1/S4 > G0/S0 Interrupt	> G0 Wake-On-LAN > G0 Wake on Ring > G0 RTC Wakeup > G0 P/S ON > G0/S0 Interrupt	
G0/S0 >	G0/C1 (idle Processor)	> G0/C0 Interrupt > G0/C2 Both Idle > G0/C2/Disk Spindown (Optional)	 > G1/S1 Both Very Idle, Spindown (Optional) > G0/C0 Interrupt	 > G0/C0 Interrupt

2.7.2 ACPI - PIIX4/BMC interaction

The BMC interacts with the PIIX4 to control the powering on and the powering off of the system. Essentially, all commands to power up and power down the system pass through the BMC and are then sent to the PIIX4. The BMC uses the PIIX4 power button input to accomplish this. Depending on how the PIIX4 has been programmed, the request to power down the system is handled by an ACPI OS, or, by the SMI handler for Non ACPI OS's. The net effect of a power down request is that the PIIX4 will assert the output SUSC_L. The BMC will look for this signal and shall control the power supply signal PS_ON appropriately. To power up the system, the BMC will assert the power button input to the PIIX4 and wait for the PIIX4 to de-assert the SUSC_L signal. When the signal is de-asserted the BMC will turn on the power supply by using the PS_ON signal. Note that the system can be turned on and off by events that are not under the control of the BMC, therefore, the BMC must only use the SUSC_L signal as the source of a power on/off request. Note that when in secure mode, the BMC should block the generation of the power button signal to the PIIX4 but not block the SUSC_L signal.

Power on events

The following events should cause the PIIX4 to issue a system wake up, even if the OS is a non-ACPI OS.

- Wake-On-LAN header (used by a plug in card).
- A COM 2 Ring indicator can be provided as a build option to replace Wake-On-LAN.
- PCI_PME (used by the embedded LAN controller).
- RTC - Note that if the PIIX4 observes a loss and restore of A/C power, any RTC wakeup command programmed into the PIIX4 will be lost.

The BMC can cause a system Wake up via:

- The SMM port.
- A command on the IMB bus.
- A command over the External Management Port (or Ring Indicator if the EMP is disabled).
- A front panel power button.
- A restoration of A/C power if the system was ON prior to losing A/C power.

ACPI - PIIX4 Wake/Resume events

Under ACPI only a specific number of events can cause a legal wake event. Advanced Power Management has a much wider range of wake events but they are not supported by C440GX+.

In order to comply with the ACPI wake/resume programming model, the PIIX4 contains two registers that control system wake up: Power Management Resume Enable Register (Base+02h) and the General Purpose Enable Register (base+0Eh). These two registers map to the ACPI defined registers PM1a_EVT_BLK and GPE0_EN.

Note that any resume event must be able to cause a System Control Interrupt (SCI).

The legal PIIX4 inputs for resume/wake events are RI, LID, GPI1, THRM and PWRBTN#. USB activity can only be used for a S1 resume, not a S4 wakeup. USB activity can only be detected if the system is already powered up as the system provides power to the USB peripherals and the USB logic is not on the PIIX4 resume Power well i.e. on 5V Standby. The Real Time Clock (RTC) can only cause a S4 wake up and not a resume event as it does not cause a SCI. In the G1/S1 state the BMC will not assert PWRBTN as it is already asserted. Therefore, use of RI, RTC and USB for resume events will not work. The BMC will be connected to the LID input so that it can cause a S4 wake up and a S1 resume event.

G1/S1 resume Events

The number of events that can be used to resume to system from a G1/S1 to a G0/S0 state is very limited. Theoretically, all the S4 Wake-up events except USB activity can also be S1 resume events. In practice Wake-On-LAN has been defined as a S4 wake event and thus, normal LAN traffic will not cause a resume event unless the NIC controller can be programmed to cause a PCI_PME_L assertion. This also applies to the modem Ring Indicator (RI) unless the modem board is a PCI modem and supports the assertion of PCI_PME_L on detection of a RI, then it cannot wake up the system.

ACPI - System Control Interrupt (SCI)

The SCI is used to replace SMI in all possible situations. The Microsoft* Windows NT Operating System is mandating that it never looses control for more than an ever declining time period. The SCI will have special abilities and can be generated by predefined activity detected within the PIIX4. The SCI comes out of the PIIX4 GPO29 pin (B3) and will be connected to the IRQ9 input of the IOAPIC and PIIX4. The IOAPIC will have to be programmed to look for an active low input. As the signal is active high, IRQ9 cannot be shared with any other ISA device and has to be dedicated to the SCI. In a uni-processor non-APIC based system, the SCI is connected to the internal IRQ9 of the PIIX4. IRQ9 must be programmed for high level sensitive. This is done with the ELCR2 register.

When IRQ9 is being used for the SCI, the signal has to be removed from the ISA slots. This will be accomplished by logic on the server board controlled by a PIIX4 GPIO bit.

NIC Wake-On-LAN will be connected to RI so that it can wake the system up from a S4 state.

The COM2 Ring indicator goes to the BMC so it will be able to wake from a S4 state on a Modem ring via the PWRBTN or wake from a S1 state via the BMC/LID connection.

Thermal Throttle

The BMC will be hooked up to the PIIX4 THERM_L input and can cause a thermal event to be seen by the OS. This is referred to as a runtime event. Once a PIIX4 pin is defined for a run time event, it cannot be used for a wake/resume event. Because of multi-processor issues with Microsoft Windows NT, only a uni-processor ACPI system can implement thermal throttling. Although the system is wired to allow this, an ACPI compliant method has to be implemented by BIOS and Firmware to allow the OS to request the temperature of the processor. Other more robust operating systems, that are insensitive to runtime changes in processor speed, can implement thermal throttling either in the OS or in BIOS by enabling the H/W throttling mechanism in the PCNTRL register (base+10).

Thermal throttling is managed by cycling the STPCLK signal, from the PIIX4, on and off. The period of the cycle is set by the PIIX4 and is 244us. The on/off duty cycle can be in increments of 12.5% or approximately 30us. If enabled, hardware thermal throttling will occur, with a fixed duty cycle, if the THRM input is active for 2 seconds. OS throttling can implement variable duty cycles, but it would require assistance from the BMC in obtaining the system temperature.

For Microsoft Windows NT, the BMC will assert THERM whenever any sensor in the system reaches a thermal limit. Microsoft Windows NT will then cause the system to perform a shut down of the system to prevent data corruption. The system administrator should reduce the operating temperature to a safe level before attempting to restart the system.

2.8 Server Management

On C440GX+, three serial buses that follow IMB protocol provide independent pathways for server management functions. The PIIX4E system management bus mentioned above (PIIX4E SMB) connects with each DIMM, and controls SDRAM clocks and processor speed configuration. A single micro-controller referred to as the Server board Management Controller (BMC) manages the other two IMB segments:

Server Management Bus supporting 8K SEEPROM and processor/server board temperature sensors.

Intelligent Management Bus (IMB) supporting connectors to system-wide server management devices.

In addition, the BMC manages sensors directly using I/O and ADC lines, controls the Emergency Management Port (EMP), detects and reports system fan failures, and manages Fault Resilient Booting (FRB). The BMC provides the Host ISA and IMB interfaces to server management features on C440GX+. The following diagram illustrates server management architecture on the C440GX+ server board.

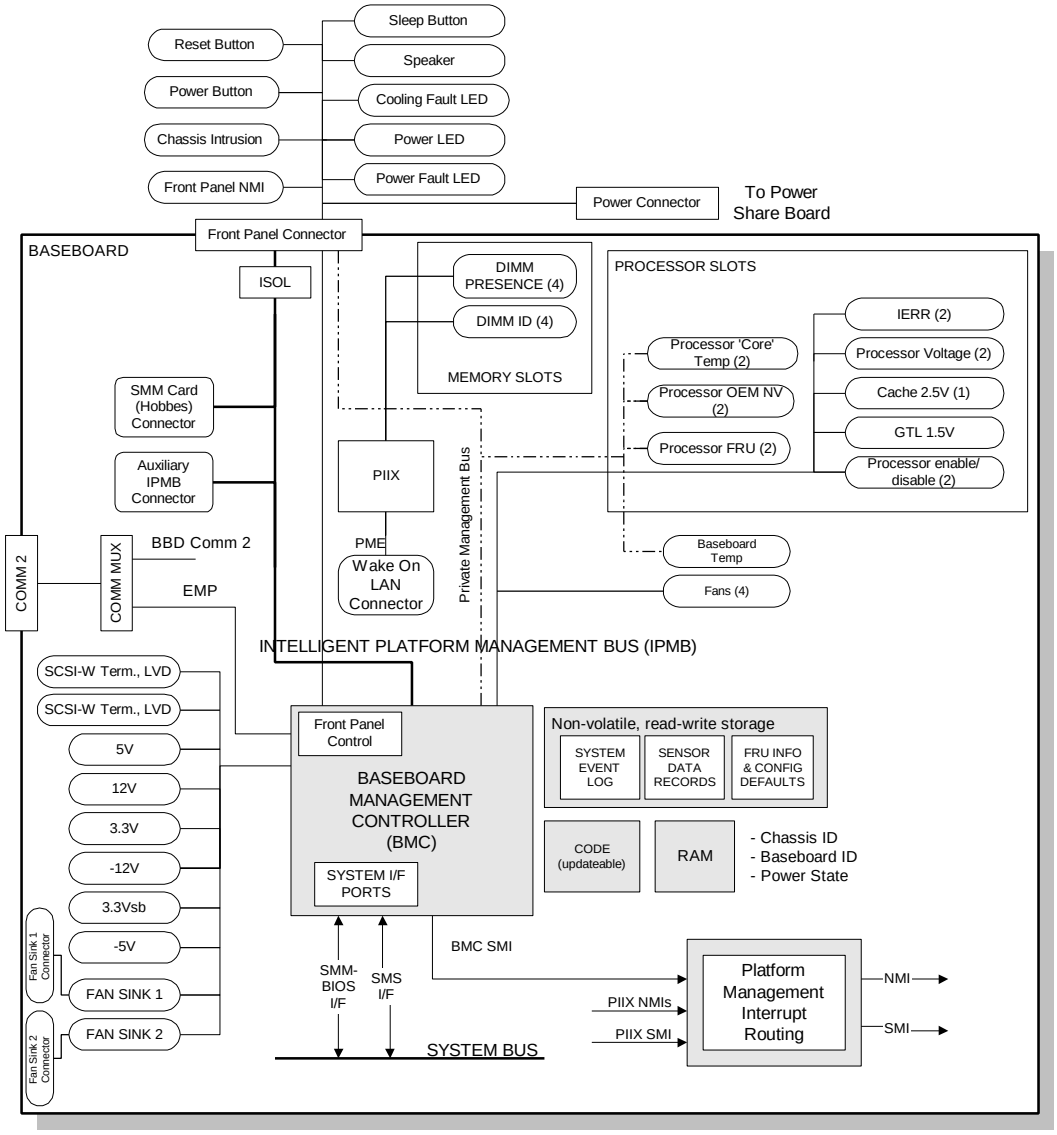


Figure 2-10. C440GX+ Server Management Block Diagram

2.8.1 Server board Management Controller (BMC)

On the C440GX+ server board, all server management functionality is provided by the BMC. The BMC and associated circuitry are powered from 5V_Standby, which remains active when system power is switched off. The BMC is implemented using a Dallas Semiconductor* DC80CH10 (or equivalent) Microcontroller.

The primary function of the BMC is to autonomously monitor system platform management events, and log their occurrence in the non-volatile System Event Log (SEL). These include events such as over-temperature and over-voltage conditions, fan failure, or chassis intrusion. While monitoring, the BMC maintains the non-volatile Sensor Data Record Recovery (SDRR), from which run-time information can be retrieved. The BMC provides an ISA host interface to SDRR information, so software running on the server can poll and retrieve the current status of the platform. A shared register interface is defined for this purpose. The SEL contents can be retrieved after system failure, for analysis by field service personnel using system management tools, such as Intel LANDesk™ Server Manager. Since the BMC is powered by 5V_Standby, SEL (and SDRR) information is also available via the IMB. An Emergency Management Card, such as the Intel LANDesk™ SMM card, can obtain the SEL and make it remotely accessible using a LAN or telephone line connection. C440GX+ provides an Emergency Management Port (EMP), which allows remote access to the SEL and other features using the COM2 port. During its watch, the BMC performs the following functions:

- System Power and Reset Control, including providing Sleep/Wake pushbutton interface for ACPI.
- Baseboard Temperature and Voltage Monitoring
- Platform Event Paging (PEP)
- Platform Event Filtering (PEF)
- VID Bit Reading (via BIOS. BIOS obtains the VID bit settings during POST and provides them to the BMC. The BMC then makes the information available via the SYSTEM interface and via the IPMB to provide a cross-platform mechanism for retrieving the nominal voltage for the processors.)
- On-board SCSI Terminator Voltage Monitoring
- Processor/Terminator Presence Monitoring
- Processor ‘Empty Slot’ Lockout
- Processor fan monitoring
- Speaker ‘Beep’ Capability (when system is powered up, used to indicate conditions such as ‘empty processor slot’)
- Baseboard Fan Failure Monitoring
- Fan Failure Light control
- System Event Log (SEL) interface
- Sensor Data Record (SDR) Repository interface
- SDR/SEL Timestamp Clock
- Baseboard FRU Information interface
- Fault Resilient Booting
- System Management Watchdog Timer
- Front Panel NMI Handling
- System interface to the IPMB (via SYSTEM Interface Ports)
- Secure Mode Control, including Video Blank and Floppy Write Protect option monitoring and control, and front panel lock/unlock initiation
- Sensor Event Initialization Agent
- Emergency Management Port (EMP) Interface
- ACPI Support
- Magic Packet and Wake on LAN support
- Chassis Power Fault Light control

This document provides detailed descriptions of the host ISA and IMB commands that provide external control of BMC operation.

BMC Front Panel Control

The BMC performs all front panel controller functions on Cypress. These include control of system power, hard-resets, and the power failure LED. The BMC is powered by 5V Standby Power. This allows the BMC to control power when the system is powered down and only 5V Standby power is available. The BMC drives system power-on/off or hard reset from the following sources:

- Front Panel Push-button (power-down blocked if Secure Mode active).
- SMM Card Feature Connector signal.
- IPMB Command.
- EMP Command. (Disabled if EMP set to 'disabled'. Power-down rejected if EMP set to 'restricted mode'. See Section 5.5.4 for information on EMP)
- Power-cycle command from system interface.
- Power-cycle from BMC Watchdog Timer.

Power Up Control

The BMC also drives system Power-up from the following sources. (Note that power up/wake can also be initiated by Wake-on-LAN (WOL) / Magic Packet signal from the attached Network Controller or PCI PME to the PIIX4:

- RTC Alarm Time (ACPI compatible): Time-of-day alarm triggered transition of PIIX4 Real Time Clock Alarm/SUSC_L (Suspend 'C') signal to the de-asserted (no suspend) state.
- A/C Power Restore. BMC can be configured to return system power to the state it was in when A/C power was lost.

Power Down Control

The BMC also drives system Power-down from the following sources:

- Power down from BMC Watchdog Timer.
- Power down command from system interface.

Hard Reset Control

The BMC drives system Hard-reset from the following sources:

- Front Panel Push-button (if Secure Mode deasserted).
- SMM Card Feature Connector signal.
- IPMB Command.
- BMC Watchdog Timer Reset.
- BMC Fault-resilient Booting (FRB-3) Time-out Reset.
- Command from Emergency Management Port.
- Command from system interface.

Front Panel Lockout

Locks out the system power and reset buttons when the Secure Mode is active. The BMC monitors the 'Secure Mode' signal from the baseboard keyboard controller. When the system is powered up, and the Secure Mode signal is asserted, the BMC locks out the ability to power down or reset the system using the front panel power and reset push-buttons. However, Secure mode does not lock out powering up the system, including powering up from an ACPI S4 (suspend to disk) state.

If the buttons are pressed while the Secure Mode state is active, the BMC will internally generate a 'Secure Mode Violation Attempt' Event Message. A 'Secure Mode Violation Attempt' event will not be logged.

The BMC also provides options for blanking the on-board video, and write-protecting the on-board floppy interface when Secure Mode is active.

Power LED Control

The BMC controls the front panel Power LED as indicated below.

Table 2-25. Power LED Control

State	Power Mode	Power LED
Power Off	Non-ACPI	Off
Power On	Non-ACPI	On
S5	ACPI	Off
S4	ACPI	Off
S3-S1[1]	ACPI	Blink, ~1/second 50/50 duty cycle
S0	ACPI	Steady On

[1] ACPI states S2-S3 are not supported on Cypress platforms.

Power Status (Fault) LED Signal

The BMC controls the front panel Power Status LED signal. The BMC asserts this signal whenever it detects a power control fault from the Power Share Controller (PSC). A power control fault is assessed when the BMC detects the system power state does not match the state being driven by the BMC. The BMC can also be directed to assert this signal via an IPMB 'Force Power Fault LED On' command. This command provides a mechanism for a chassis management controller to indicate that it has detected a redundant power supply failure. The command can also be used to check the power status signal as part of system integration testing.

The Power Status LED is used to report several power status conditions:

Table 2-26. Power Status (Fault) LED Signal

State	Power Status LED
Power Fault	Steady On
Power Control Fault	Fast FLASH (~3/second) 50/50 duty cycle
Power OK	LED Off
Force On command	LED On

Secure Mode

The BMC monitors the SECURE_MOD_KB signal from the baseboard keyboard controller. When the system is powered up, and SECURE_MOD_KB asserted, the BMC prevents power off or reset via the front panel power and reset pushbuttons. A 'Secure Mode Violation Attempt' event is flagged by the BMC whenever a front panel pushbutton is pressed. When secure mode has been established, the BMC:

- Locks out the front panel power and reset buttons
- Optionally blanks video
- Optionally places the floppy disk in write protect mode

As a BIOS setup option, the user may instruct the system to enter secure mode after a specified time interval with no activity on the keyboard or mouse.

2.8.2 Server Management Bus

The Server Management Bus (SMB) is a single master, open-drain, serial bus which is electrically and timing compatible with the 100 Kbps version of the IMB bus specification. The SMB extends throughout the server board providing an independent pathway for the BMC to communicate with the server board, two processor slot temperature sensors and to the 8550 EEMUX for processor speed detection. In addition, the SMB supports an 8K SEEPROM device for non-volatile storage of the

System Event Log (SEL), Sensor Data Record Repository (SDRR), FRU information, and configuration defaults. The BMC controls access to this device and manages the data structures within (refer to BMC description below).

Buffers are provided to isolate the server board and processor temperature sensors from the rest of the SMB. These buffers, running on 5V_Standby, keep the bus alive to the BMC even though main power is switched off. This allows the BMC to communicate with its SEEPROM at all times.

2.8.3 Intelligent Management Bus

The Intelligent Management Bus (IMB) is a multi-master, open-drain, serial bus which is also electrically and timing compatible with the 100 Kbps version of the IMB bus specification. The IMB attaches to connectors on the server board creating a server management network that extends throughout the server board and system chassis, providing an independent pathway for communications between the BMC and system-level server management devices (e.g., Hot-swap SCSI controller). In addition, the IMB provides inter-chassis communications extensions for a complete server management network solution.

The communication protocol for the IMB is defined in the *Intelligent Management Bus Communications Protocol Specification*. The protocol is designed to work with micro-controllers and other IMB masters, and slave devices such as IMB temperature sensors.

The IMB attaches to the following connector interfaces on the C440GX+ server board:

- Auxiliary IMB connector
- Server Monitor Module (SMM) card feature connector
- Front panel connector

The C440GX+ server board provides the main pullups on the clock (IMB_SCL) and data (IMB_SDA) lines of the IMB. This termination is sized to drive the full IMB, i.e., capacitive loading for not only the server board, but for the chassis, SMM Card IMB, and auxiliary IMB connections. Sufficient pull-up capability is provided on the isolated side of the IMB for the BMC, SMM Card, SMM Card IMB, Front Panel IMB, and aux. IMB connections. These pullups are driven by 5V Standby. Since a full set of pullups is provided on the server board, additional pullups are not necessary for external devices connecting to the IMB. Only the C440GX+ server board should provide pullups for these connections.

Auxiliary I^2C Connector

The auxiliary I^2C connector has the following pinout.

Table 2-27. Auxiliary I^2C Connector Pinout

Pin	Signal
1	Local I^2C SDA
2	GND
3	Local I^2C SCL

Caution:

A shorted IMB connection at the auxiliary I^2C connector will disrupt proper operation of the IMB.

SMM Card Feature Connector

The SMM card feature connector attaches to the IMB. In addition to IMB signals, the 26-pin connector provides the following signals as shown in the table below:

Table 2-28. SMM Card Feature Connector Pinout

Pin	Signal	Description
1	CPU_SMI_L	System Management Interrupt
2	LOCAL_IMB_SCL	IMB clock line
3	GND	Ground
4	Reserved	-
5	PWR_CNTRL_SFC_L	Host power supply on/off control
6	LOCAL_IMB_SDA	IMB serial data line
7	5VSTNDBY	+5V standby indication (power OK)
8	KEYLOCK_SFC_L	Keyboard lock signal
9	CPU_NMI	Non-maskable interrupt indication
10	VCC3	3.3V power supply status input
11	RST_SFC_L	Server board reset signal from Server Monitor Module
12	GND	Ground
13	GND	Ground
14	Reserved	-
15	SECURE_MODE_BMC	Secure mode indication
16	GND	Ground
17	SFC_CHASSIS_INSTRUSION_L	Chassis intrusion indication
18	Reserved	-
19	Reserved	-
20	GND	Ground
21	Reserved	-
22	Reserved	-
23	Reserved	Unused
24	Reserved	-
25	Key pin (nc)	Connector key
26	Reserved	-

Front Panel/Power Share Connector

A 30-pin header is provided that attaches to the system front panel and the power share board, which contains reset, NMI, and power control switches, LED indicators, as well as the IMB I^2C connection. The connector has the following pinout:

Table 2-29. Front Panel Connector Pinout

Pin	Signal	Pin	Signal
1	Speaker Data Out	2	GND
3	Chassis intrusion switch	4	Hard Disk Active
5	+5V	6	Sleep Active
7	Fan failure indicator LED	8	Power Indicator
9	Power fault LED	10	GND

Pin	Signal	Pin	Signal
11	I^2C Data line IMB	12	Front panel NMI switch
13	I^2C Clock line IMB	14	Reset Switch
15	+5V standby	16	Power Control Switch
17	GND	18	+5V Sense
19	+3.3V Sense	20	Fan Speed Control
21	Isol. I^2C Clock line SM	22	Isol. I^2C Data line SM
23	GND	24	Power Good Signal
25	Power On Signal	26	GND
27	-12V	28	No Connection
29	+12V Sense	30	GND

2.8.4 Fault Resilient Booting

The BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If two processors are installed and the processor designated as the BSP fails to complete the boot process, FRB attempts to boot the system using the alternate processor.

FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.

FRB level 2 is for recovery from a Watchdog timeout during POST. The Watchdog timer for FRB level 2 detection is implemented in the BMC.

FRB level 3 is for recovery from a Watchdog timeout on Hard Reset / Power-up. Hardware functionality for this level of FRB is provided by the BMC on the processor subsystem.

FRB-3 is managed by the BMC, which controls the ability to boot using either processor in the event of a catastrophic processor failure. On power up, a timer starts that can only be stopped by a healthy processor using the GPIO bit, FRB_TMRHLT_L, on the PIIX4. If processor 0 fails to halt the FRB timer before timeout, the controller asserts STOP_FLUSH to the processor and asserts FRB_RST_L for 10ms. When the system comes out of reset, processor 0 is prevented from acting as the BSP, allowing the other processor to take over the boot process.

FRB level 3 errors are cleared by setting the "Processor Retest" option in BIOS setup.

3. Configuration and Initialization

This chapter describes the initial programming environment including address maps for memory and I/O, techniques and considerations for programming ASIC registers, and hardware options configuration.

3.1 Memory Space

At the highest level, the Pentium II Xeon processor address space is divided into 4 regions, as shown in the following figure. Each region contains subregions, as described in following sections. Attributes can be independently assigned to regions and subregions using 440GX registers.

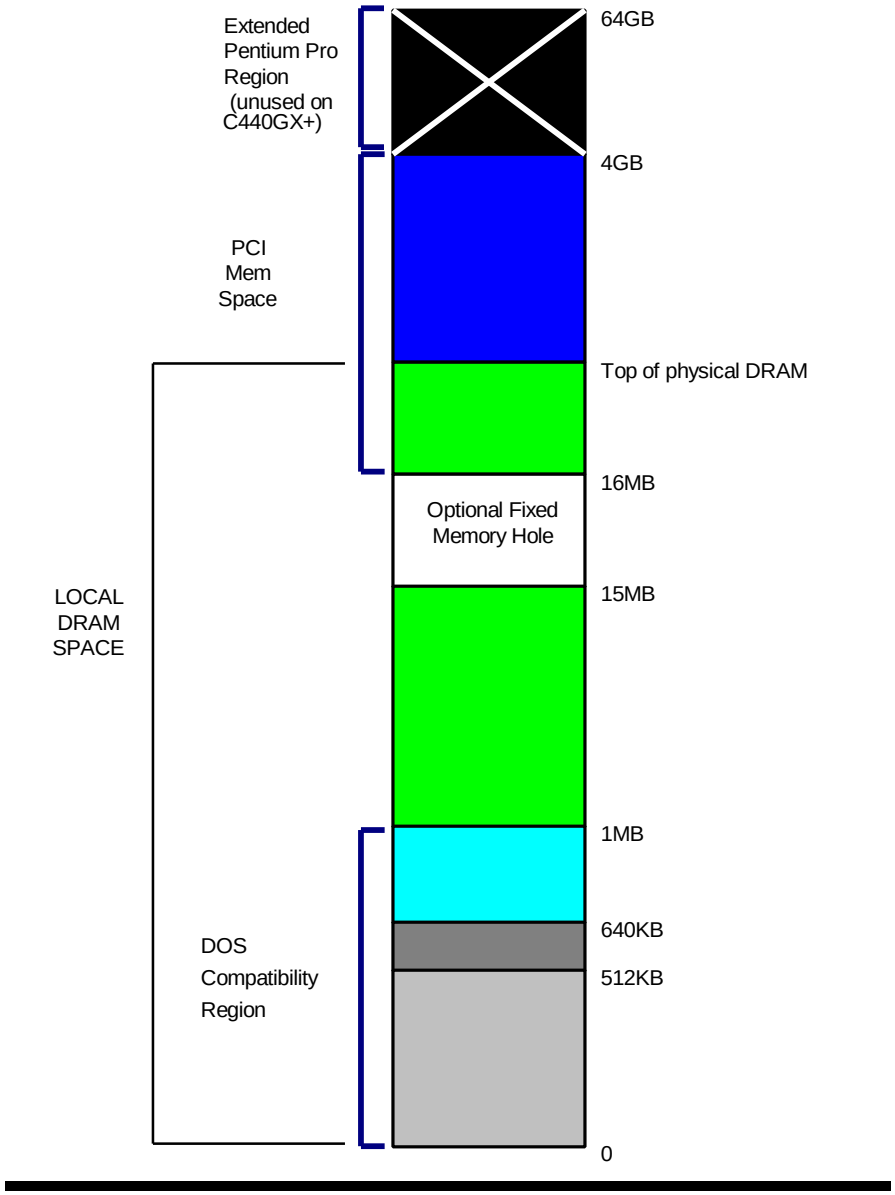


Figure 3-1. Pentium II Xeon and Pentium III Xeon Processor Memory Address Space

3.1.1 DOS Compatibility Region

The first region of memory below 1 MB was defined for early PCs, and must be maintained for compatibility reasons. This region is divided into subregions as shown in the following figure.

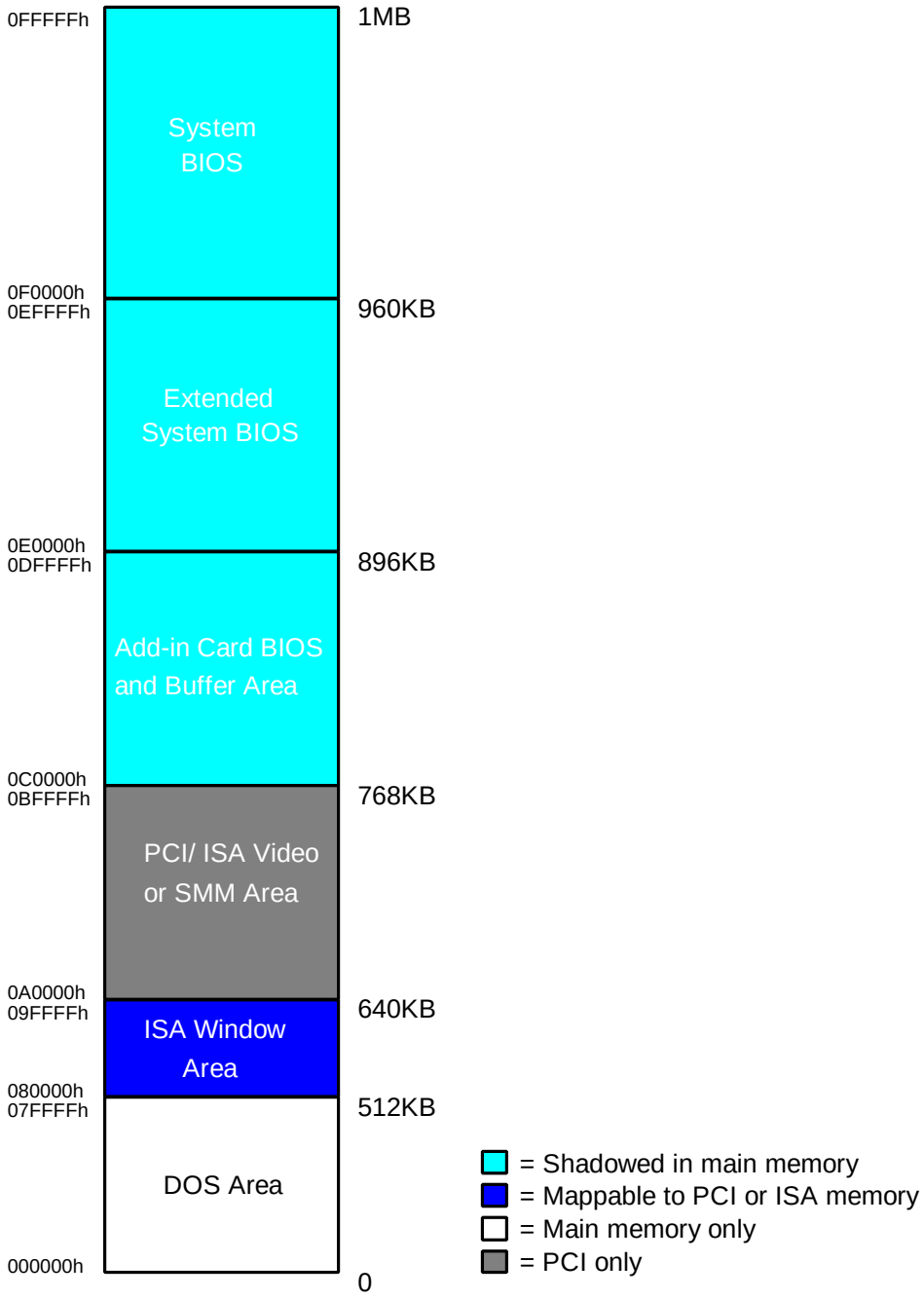


Figure 3-2. DOS Compatibility Region

DOS Area

The DOS region is 512 KB in the address range 0 to 07FFFFh. This region is fixed and all accesses go to main memory.

ISA Window Memory

The ISA Window Memory is 128 KB between the addresses of 080000h to 09FFFFh. This area can be mapped to the PCI bus or main memory.

Video or SMM Memory

The 128 KB Graphics Adapter Memory region at 0A0000h to 0BFFFFh is normally mapped to the VGA controller on the PCI bus. This region is also the default region for SMM space*.

Add-in Card BIOS and Buffer Area

The 128 KB region between addresses 0C0000h and 0DFFFFh is divided into eight segments of 16 KB segments mapped to ISA memory space, each with programmable attributes, for expansion card buffers. Historically, the 32 KB region from 0C0000h to 0C7FFFh has contained the video BIOS location on a video card. However, on C440GX+, the video BIOS is located in the Extended BIOS or System BIOS areas. This region can be used for extended SMM space*.

Extended System BIOS

This 64 KB region from 0E0000h to 0EFFFFh is divided into 4 blocks of 16 KB each, and may be mapped with programmable attributes to map to either main memory or to the PCI bus. Typically, this area is used for RAM or ROM. This region can also be used for extended SMM space*.

System BIOS

The 64 KB region from 0F0000h to 0FFFFFh is treated as a single block. By default this area is normally Read/Write disabled with accesses forwarded to the PCI bus. Through manipulation of R/W attributes, this region can be shadowed into main memory. This region can also be used for extended SMM space*.

* Refer to “System Management Mode Handling", later in this chapter.

3.1.2 Extended Memory

Extended memory on C440GX+ is defined as all address space greater than 1 MB. The Extended Memory region covers 4 GB of address space from addresses 0100000h to FFFFFFFFh, as shown in the following figure.

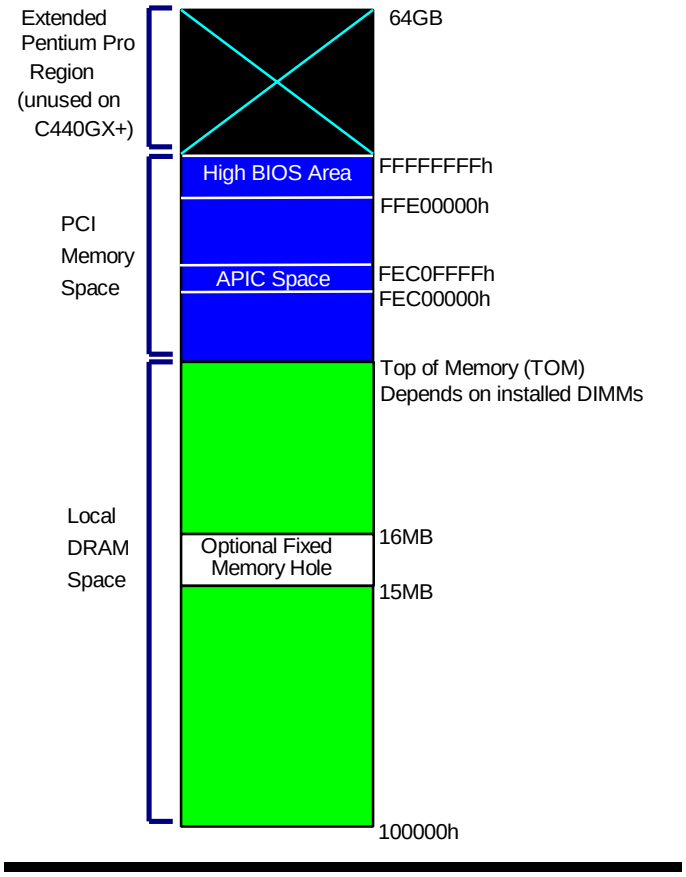


Figure 3-3. Extended Memory Map

Main Memory

All installed DRAM greater than 1 MB is mapped to local main memory, up to the top of physical memory which is located at 2 GB. Memory between 1 MB to 15 MB is considered to be standard ISA extended memory. 1 MB of memory starting at 15 MB can be optionally mapped to the PCI bus memory space.

The remainder of this space, up to 2 GB, is always mapped to main memory, unless Extended SMRAM is used, which limits the top of memory to 256MB. Refer to “System Management Mode Handling” below for more information.

PCI Memory Space

Memory addresses in the 2 GB to 4 GB range are mapped to the PCI bus. This region is divided into three sections: High BIOS, APIC Configuration Space, and General-purpose PCI Memory.

The General-purpose PCI Memory area is typically used for memory-mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers

High BIOS

The top 2 MB of Extended Memory is reserved for the system BIOS, extended BIOS for PCI devices, and A20 aliasing by the system BIOS. The CPU begins executing from the High BIOS region after reset.

I/O APIC Configuration Space

A 64 KB block located 20 MB below 4 GB (0FEC00000h to 0FEC0FFFFh) is reserved for the I/O APIC configuration space.

I/O APIC units are located beginning at a base address determined by subtracting 013FFFF0h from the reset vector. The first I/O APIC is located at FEC00000h. Each I/O APIC unit is located at FEC0x000h where x is the I/O APIC unit (0 through F).

Extended System Management RAM Space

The 440GX chip supports placement of System Management RAM (SMRAM) space in cacheable memory above 1MB. Extended SMRAM consists of up to 2MB of physical memory, located at the top of installed memory (up to 256MB boundary). This region is aliased to memory addresses below 1MB. Refer to “System Management Mode Handling”, later in this chapter.

Extended Pentium II Xeon Processor Region (above 4 GB)

A Pentium II Xeon or Pentium III Xeon processor-based system can have up to 64 GB of addressable memory. However, the 440GX only supports 32-bit addressing, with the BIOS operating in 4 GB of address space (the DIMMs provide up to 2GB of main memory). All accesses to the region from 4 GB to 64 GB are claimed by the 440GX and terminated. Write data is dropped and zeroes are returned on reads.

3.1.3 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into main memory. Typically, this is done to allow ROM code to execute more rapidly out of RAM. ROM is designated read-only during the copy process while RAM at the same address is designated write-only. After copying, the RAM is designated read-only and the ROM is designated write-only (shadowed). Processor bus transactions are routed accordingly. Transactions originated from the PCI bus or ISA masters and targeted at shadowed memory blocks will not appear on the processor's bus.

3.1.4 System Management Mode Handling

The 440GX supports System Management Mode (SMM) operation in standard (compatible) mode, and special extended modes. System Management RAM (SMRAM) provides code and data storage space for the SMI_L handler code, and is made visible to the processor only on entry to SMM, or other conditions which can be configured using 440GX PCI registers. The 440GX supports three flavors of SMRAM:

Compatible SMRAM, located in main memory below the 1MB boundary at addresses 000A0000h through 000B0000h. This region is non-cacheable.

High SMRAM, which exists in physical memory above the 256MB boundary, and is write-back cacheable. The High SMRAM region is aliased to A0000h through FFFFF.

Extended SMRAM, providing up to 1MB at the top of main memory (TSEG) which is also cacheable. Use of Extended SMRAM forces the upper limit of installed memory to 256MB.

NOTE: Proper operation in SMRAM above 1MB, including cacheability, requires enhancements to standard SMI_L handler code.

The 440GX determines the nature and location of SMRAM space using the SMRAM Control (72h) and Extended SMRAM Control (73h) configuration space registers.

3.2 I/O Map

The 440GX allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including PIIX4, have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On C440GX+, the PIIX4E provides the bridge to ISA functions.

The I/O map in the following table shows the location in C440GX+ I/O space of all directly I/O-accessible registers. PCI configuration space registers for each device control mapping in I/O and memory spaces, and other features that may affect the global I/O map. The Super I/O chip contains configuration registers that are accessed through an index and data port mechanism.

3.3 System Initialization Sequence

The C440GX+ system is initialized and configured in the following manner.

System power is applied. The power-supply provides resets using the RST_PWR_GD_BB signal. PCI reset (RST_P_RST_L) is driven to tri-state the PCI bus in order to prevent PCI output buffers from short circuiting when the PCI power rails are not within the specified tolerances. The 440GX asserts G_CPURST_L to reset the processor(s).

The 440GX is initialized, with its internal registers set to default values.

Before G_CPURST_L is deasserted, the 440GX asserts BREQ0_L. Processor(s) in the system determine which host bus agents they are, Agent 0 or Agent 1, according whether their BREQ0_L or BREQ1_L is asserted. This determines bus arbitration priority and order.

The processor(s) in the system determines which processor will be the BSP by issuing Bootstrap Inter Processor Interrupts (BIPI) on the APIC data bus. The non-BSP processor becomes an application processor and idles, waiting for a Startup Inter Processor Interrupt (SIPI).

The BSP begins by fetching the first instruction from the reset vector.

440GX registers are updated to reflect memory configuration. DRAM is sized and initialized.

All PCI and ISA I/O subsystems are initialized and prepared for booting.

3.4 Hardware Jumper Configuration

This section describes how to configure hardware jumper options on the server board for the following:

- System configuration
- Internal/external speaker selection

Jumper locations and designations are marked on the server board, refer to the layout diagram in Chapter 1 for placement information.

3.4.1 System Configuration Jumpers

15-pin and 11-pin single inline headers provide seven 3-pin jumper blocks that control various configuration options, as shown in the figure below. The shaded areas show default jumper placement for each configurable option.

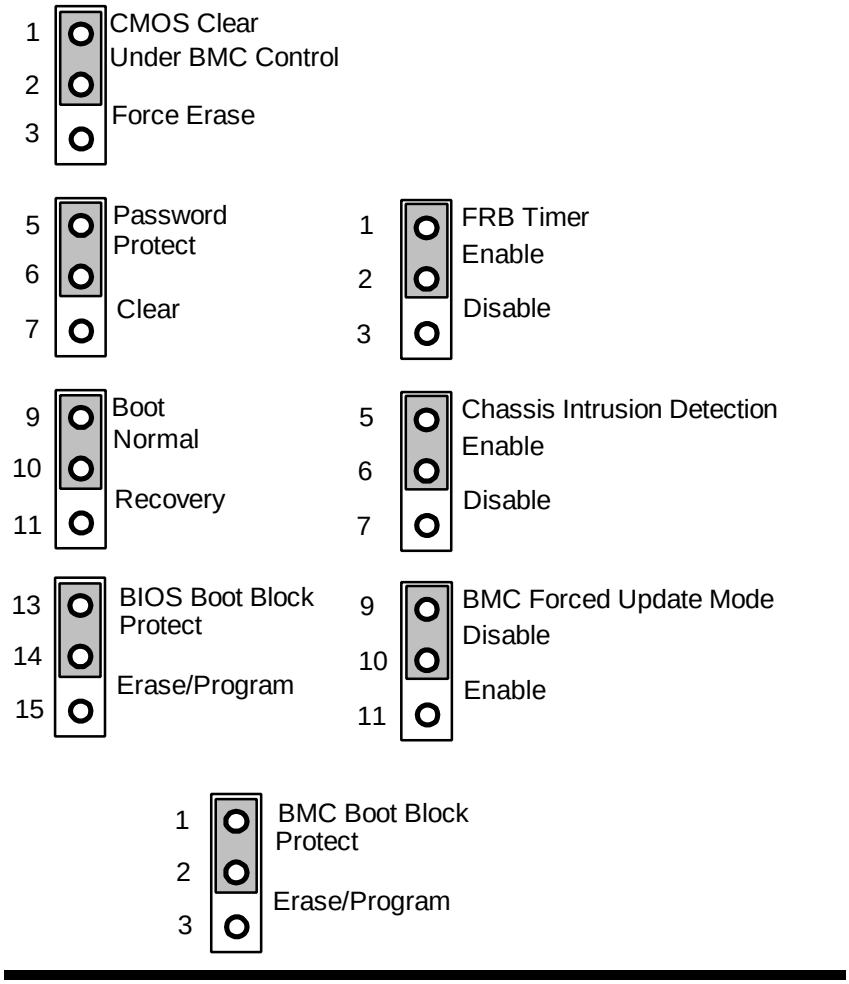


Figure 3-4. System Configuration Jumpers

The following table describes each jumperable option.

Table 3-1. System Configuration Jumper Options

Option	Description
CMOS Clear	If pins 1 and 2 are jumpered (default), preservation of configuration CMOS through system reset is controlled by the BMC. If pins 2 and 3 are jumpered, CMOS contents are set to manufacturing default during system reset.
Password Clear	If pins 5 and 6 are jumpered (default), the current system password is maintained during system reset. If pins 6 and 7 are jumpered, the password is cleared on reset.
Recovery Boot	If pins 9 and 10 are jumpered (default) the system will attempt to boot using the BIOS programmed in the Flash memory. If pins 10 and 11 are jumpered, the BIOS will attempt a recovery boot, loading BIOS code from a floppy disk into the Flash device. This is typically used when the BIOS code has been corrupted.
BIOS Boot Block Write Protect	If pins 13 and 14 are jumpered (default), the BIOS boot block is write-protected. If pins 14 and 15 are jumpered, the boot block is erasable and programmable. ***WARNING: Incorrect programming of the boot block will render the system unbootable.***

FRB Timer Enable	If pins 1 and 2 are jumpered (default), FRB operation is enabled, which allows the system to boot from processor 1 if processor 0 fails. If pins 2 and 3 are jumpered, FRB is disabled.
Chassis Intrusion Detection	If pins 5 and 6 are jumpered (default), a switch installed on the chassis will indicate when the cover has been removed. If pins 6 and 7 are jumpered, the chassis intrusion switch is bypassed.
BMC Forced Update Mode	If pins 9 and 10 are jumpered (default), firmware status is maintained as is, and operational code will run. If pins 10 and 11 are jumpered, the system is placed into "Forced Update Mode." Only a minimal set of ISA and BMC functions are available. The system is forced to update firmware. ***WARNING: The system must have A/C power removed before moving this jumper.***
BMC Boot Block Write Protect	If pins 1 and 2 are jumpered (default), the BMC boot block is write-protected. If pins 2 and 3 are jumpered, the boot block is erasable and programmable. ***WARNING: Incorrect programming of the boot block will render the system unbootable.***

3.4.2 AT-style Front Panel Header (J6H1)

A 19-pin labeled single inline header located at connector location J6H1 is provided for AT-style front panel connections, e.g., power, LED indicators, and reset. The connector has the following pinout:

Table 3-2. AT Front Panel Header Pinout

Pin	Signal
1	Pwr_Cntrl_Fp – 5V_STNDBY
2	Ground
3	No Pin
4	Hd_LED_Pwr – VCC
5	No Pin
6	Fp_HD_Act
7	Hd_LED_Pwr – VCC
8	Ground
9	No Pin
10	Spkr_Int
11	Spkr_Out
12	Ground
13	No Pin
14	Pwr_LED
15	No Pin
16	Ground
17	Rst_Fp
18	Fp_Sleep
19	Ground

Speaker Circuit Jumper/Connector

A 4-pin block on the AT Front Panel Header (labeled J6H1) provides a way to plug in an external speaker or, by jumper, enable the onboard speaker. The configuration is shown in the figure below.

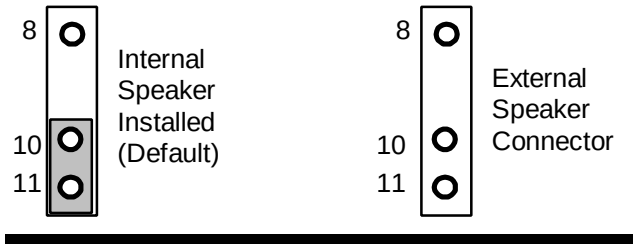


Figure 3-5. Speaker Circuit Jumper

3.4.3 Wake On LAN

The jumper at location J5A1 is used to enable/disable the Wake On LAN functionality of the on board network controller. By default the board is shipped with this option enabled. See Figure 4-9. If a power supply is used that does not provide 0.8A of +5 volt Stand-by, this option should be disabled.

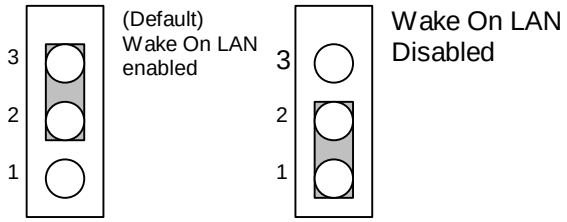


Figure 3-6. Wake On LAN Jumper (J5A1)

NOTE - Insure that the minimum required standby current is available from the power supply when enabling WOL

4. Environmental, Electrical, and Mechanical Specs

This chapter specifies the operational parameters and physical characteristics for C440GX+ server board. This is a board-level specification only. System specifications are beyond the scope of this document.

4.1 Absolute Maximum Ratings

Operation of C440GX+ at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 4-1. Absolute Maximum Ratings

Operating Temperature	5°C to +50°C *
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V **
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

* Chassis design must provide proper airflow to avoid exceeding Pentium® II Xeon™ 100MHZ FSB maximum case temperature.
** V_{DD} means supply voltage for the device.

Table 4-2 lists the maximum component case temperatures for base board components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.

CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5°C to 10 °C might cause components to exceed their maximum case temperature. When determining system compliance, considerations should be given for maximum rated ambient temperatures.

Table 4-2. Thermal Considerations for Components

Component	Maximum Temperature
Pentium II Xeon processor	75 °C (thermal plate)
Pentium III Xeon processor < 550MHz	75 °C (thermal plate)
Pentium III Xeon processor = 550MHz	68 °C (thermal plate)
Intel 82443GX PAC	105 °C (case)
Intel 82371EB PIIX4E	85 °C (case)
Lithium battery	70 °C (case)
PWB substrate	105 °C

Further topics in this chapter specify normal operating conditions for C440GX+.

4.1.1 System Cooling

The C440GX+ provides six 3-pin, shrouded, and keyed fan connectors. Two of these connectors, located next to each processor slot on the server board are for retention module fans. The remaining

four connectors on the server board attach to chassis fans equipped with a sensor that indicates whether the fan is operating. Note that fan connectors 2a and 2b cannot be used at the same time due to server management and possible power restrictions based on the type of fans that are used. The sensor pins for these fans are routed to the BMC for failure monitoring. The fan connectors have the following pinout:

Table 4-3. Fan Connector Pinout

Pin	Signal
1	GND
2	+12V
3	Fan Sensor

NOTE: It is highly recommended to always use the two fans attached to the processor retention module to ensure proper cooling of the processors.

4.2 Electrical Specifications

DC specifications for C440GX+ power connectors and module power budgets are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications), can be obtained from other documents:

PCI Connectors -- *PCI Local Bus Specification Rev. 2.1*

ISA slots -- *EISA Bus Specification*

4.2.1 Power Connection

The main power supply connection is obtained using the 24-pin ATX II-style connector. The following tables define the pinouts and wire gauge/color for each of these connectors. The main power connector can also accommodate a 20-pin style ATX power connector. Pins 1 – 10 and pins 13 – 22 are identical in form and fit to the ATX style connector. If using a standard ATX power supply to power the C440GX+ server board, simply insert the ATX connector from the power supply into the inner most pins on the main power connector on the server board. The outer most 4 pins will be unoccupied.

Table 4-4. 24-pin Main Power Connector Pinout

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2	+3.3Vdc	Orange	14	-12Vdc	Blue
3	COM	Black	15	COM	Black
4	+5 Vdc	Red	16	PS-ON	Green
5	COM	Black	17	COM	Black
6	+5 Vdc	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray	20	-5V	White
9	5VSB	Purple	21	+5 Vdc	Red
10	+12Vdc	Yellow	22	+5 Vdc	Red
11	+12Vdc	Yellow	23	+5 Vdc	Red
12	+3.3Vdc	Orange	24	COM	Black

To add additional power capabilities beyond those supplied by the Main 24-pin power connector, a straight 1x 6 AUX power connector has been added to the server board.

Table 4-5. 6-pin Auxiliary Power Connector Pinout

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	COM	Black	4	+3.3Vdc	Orange
2	COM	Black	5	+3.3Vdc	Orange
3	COM	Black	6	+5 Vdc	Red

4.2.2 Power Consumption

The following table shows the power consumed on each supply line for a C440GX+ server board with 2 Pentium II Xeon 450MHz processors, 4 (64MB) DIMMs, 1 Hot Swap Back plane, IDE Boot, and 1 SCA hot swap drive while running Kpower.

NOTE: The following numbers are provided as an **example**. Actual power consumption will vary depending on the exact C440GX+ configuration, temperature, voltage level, etc... Refer to the appropriate system chassis document for more information.

Table 4-6. C440GX+ Power Consumption using 12V VRMs

Device(s)	3.3V	+5V	-5V	+12V	-12V	5V Stndby	
Total Current (A)	7.04 A	5.1 A	0 A	9.96 A	.05 A	.75 A	Total
Total Power (W)	23.23 W	25.5 W	0 W	120 W	0.6 W	3.75 W	173.08 W

	3.3V	+5V	-5V	+12V	-12V	5V Stndby	
Cabrillo-C Pwrshr	**34.8A**	**22A**	**.05A**	**17A**	**.5A**	**1.5A**	**51.55A**
Cabrillo-C Pwrshr	115 W	110 W	.25 W	204 W	6 W	7.5 W	308.3W
Total Board Power	23.23 W	25.5 W	0 W	120 W	0.6 W	3.75 W	102.7W
Total Chassis Power Available	91.77 W	84.5 W	.25 W	84 W	5.4 W	3.75	205.6

Table 4-7. C440GX+ Power Consumption using 5V VRMs

Device(s)	3.3V	+5V	-5V	+12V	-12V	5V Stndby	
Total Current (A)	7.04A	16.2A	0A	4.77A	.05A	.75A	Total
Total Power (W)	23.23W	81W	0W	57.25W	0.6W	3.75W	102.7W

	3.3V	+5V	-5V	+12V	-12V	5V Stndby	
300W Delta DPS-300	**16A**	**25A**	**.05A**	**10A**	**.5A**	**.85A**	**51.55A**
300W Delta DPS-300	52.8 W	125 W	.25 W	120 W	6 W	4.25 W	308.3W
Total Board Power	15.05 W	42 W	.25 W	43.2 W	.6 W	1.6 W	102.7W
Total Chassis Power Available	37.75 W	73 W	0 W	76.8 W	5.4 W	2.65 W	195.6 W

#The total combined output power of the +3.3 and +5V channels shall not exceed 195W.

4.2.3 Power Supply Specifications

This section provides power supply design guidelines for a C440GX+-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

This section provides power supply design guidelines for a C440GX+ based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Note: The C440GX+ server board is able to support a standard 400W ATX compatible power supply. The 20 pin ATX connector from the power supply is inserted into pins 1-20 of the 24 pin Main power connector on the server board.

Table 4-8. C440GX+ DP Server Power Supply Voltage Specification

Item	Min	Nom	Max	Units	Tolerance
VOLTAGE TOLERANCE:					
3.3 Volts	3.20	3.30	3.46	V	-3/+5%
5 Volts	4.80	5.00	5.25	V	-4/+5%
+12 Volts	11.40	12.00	12.60	V	+/-5%
-12 Volts	-11.40	-12.00	-12.60	V	+10%
-5 Volts	-4.75	-5.00	-5.25	V	+10%
5 Volts Standby	+4.75	+5.00	+5.25	V	+/-5%

Table 4-9. Transient and Remote Sense/Sink Currents

Item	Min	Nom	Max	Units
TRANSIENT CURRENTS:				
Max dI/dt:				
5 Volts			0.5	A/µs
3.3 Volts			0.5	A/µs
+12 Volts			0.5	A/µs
-12 Volts			NA	A/µs
-5 Volts			NA	A/µs
5 Volts Standby			NA	A/µs
Amplitude:				
5 Volts			8.0	A
3.3 Volts			22	A
+12 Volts			.5	A
-12 Volts			Not Specified	
-5 Volts			Not Specified	
5 Volts Standby			Not Specified	
REMOTE SENSE:				
Fuse Rating:		N/A		A
Sense Trace Resistance:			0.05	Ω
SINK CURRENT (While Voltage Form Off):				
Off Voltage:				
5 Volts			0.113	V
3.3 Volts			0.007	V
+12 Volts			0.061	V
-12 Volts			NA	V
-5 Volts			NA	V

Table 4-10. Ramp Rate / Shape / Sequencing / Power Good & Power On Signals

Item	Min	Nom	Max	Units	Comments
Ramp Rate(On):					
5 Volts	5		70	Ms	From 10% to within regulation
3.3 Volts	5		70	Ms	From 10% to within regulation
+12 Volts	5		70	Ms	From 10% to within regulation
-12 Volts	5		70	Ms	From 10% to within regulation
-5 Volts	NA		NA	Ms	From 10% to within regulation
5 Volts Standby	5		70	Ms	From 10% to within regulation
Ramp "Shape"(On & Off):					Monotonic

Sequencing: **(with respect to 5 Volts)**					See Figure 6-1
3.3 Volts					**
+12 Volts					**
-12 Volts					
-5 Volts					
5 Volts Standby					
Power Good Signal					See Figure 6-2
Vil			0.6	V	
Vih	3.5			V	
Iil	-1.0		1.0	MA	
Iih			NA	MA	
Timing requirements				TBD	
Power On Signal (PS_ON_L)				TBD	
Vol			0.8	V	
Voh	3.5			V	
Iol	10			MA	
Ioh	1.5			MA	
Timing requirements				TBD	
Etc.					

** +3.3, +5, and +12V output voltages must come up within 100mS of each other.

4.2.4 Voltage Recovery Timing Specifications

The power supply must conform to the following specifications for voltage recovery timing under load changes:

1. Voltage shall remain within +/- 5% of the nominal set voltage on the +5V, +12V and 3.3V outputs, and +/- 5% of the nominal set voltage on the -5V and -12V outputs, during instantaneous changes in +5V and +12V load up to 8 Amps, and +3.3V load steps of 5 Amps.
2. Voltage regulation limits shall be maintained over the entire AC input range and any steady state temperature and operating conditions specified.
3. Voltages shall be stable as determined by bode plot and transient response. The combined error of peak overshoot, set point, regulation, and undershoot voltage shall be less than or equal to +/-5% of the output voltage setting. The transient response measurements shall be made with a load changing repetition rate of 50Hz to 5kHz. The load slew rate shall not be greater than 0.2A/µs.

4.2.5 Voltage Sequencing and Power Good Signal Characteristics

The following figures show the dynamic behavior of power signals when system power is switched on.

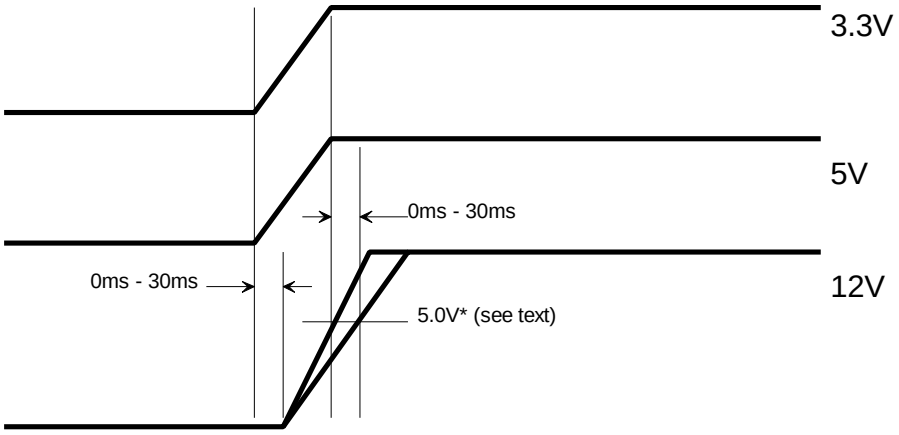
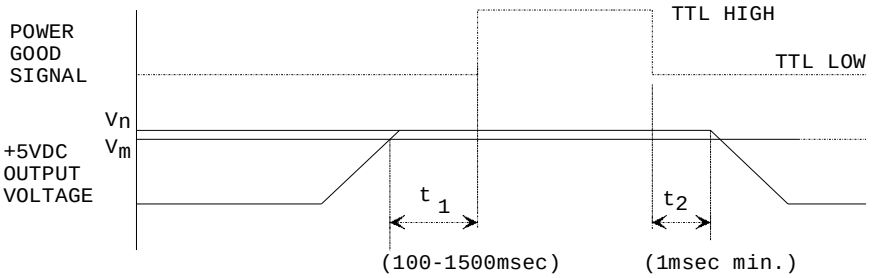


Figure 4-1. DC Voltage Sequencing

Note that the +3.3V and +5V supply voltages must begin their power-up ramp at the same time, and that +12V must start at the same time, or slightly after, the +5V supply. Additionally, the +12V must reach 5.0V at the same time, or slightly after, the +5V supply reaches 5.0V.

All supply voltages must have a monotonic ramp up.



Vn Nominal Output Voltage +5 VDC
Vm Minimum Output Voltage +4.75 VDC
t1 Delay Turn-on (100-1500msec)
t2 Delay Turn-off(1msec min)

Figure 4-2. Power Good Signal Characteristics

4.3 Mechanical Specifications

The following diagrams show the mechanical specifications of the C440GX+ server board. All dimensions are given in inches, and are dimensioned per ANSI Y15.4M. Maximum primary-side component height is .550” unless otherwise noted. Connectors are dimensioned to pin 1. Refer to “Connector Specifications” after the diagram for more information.

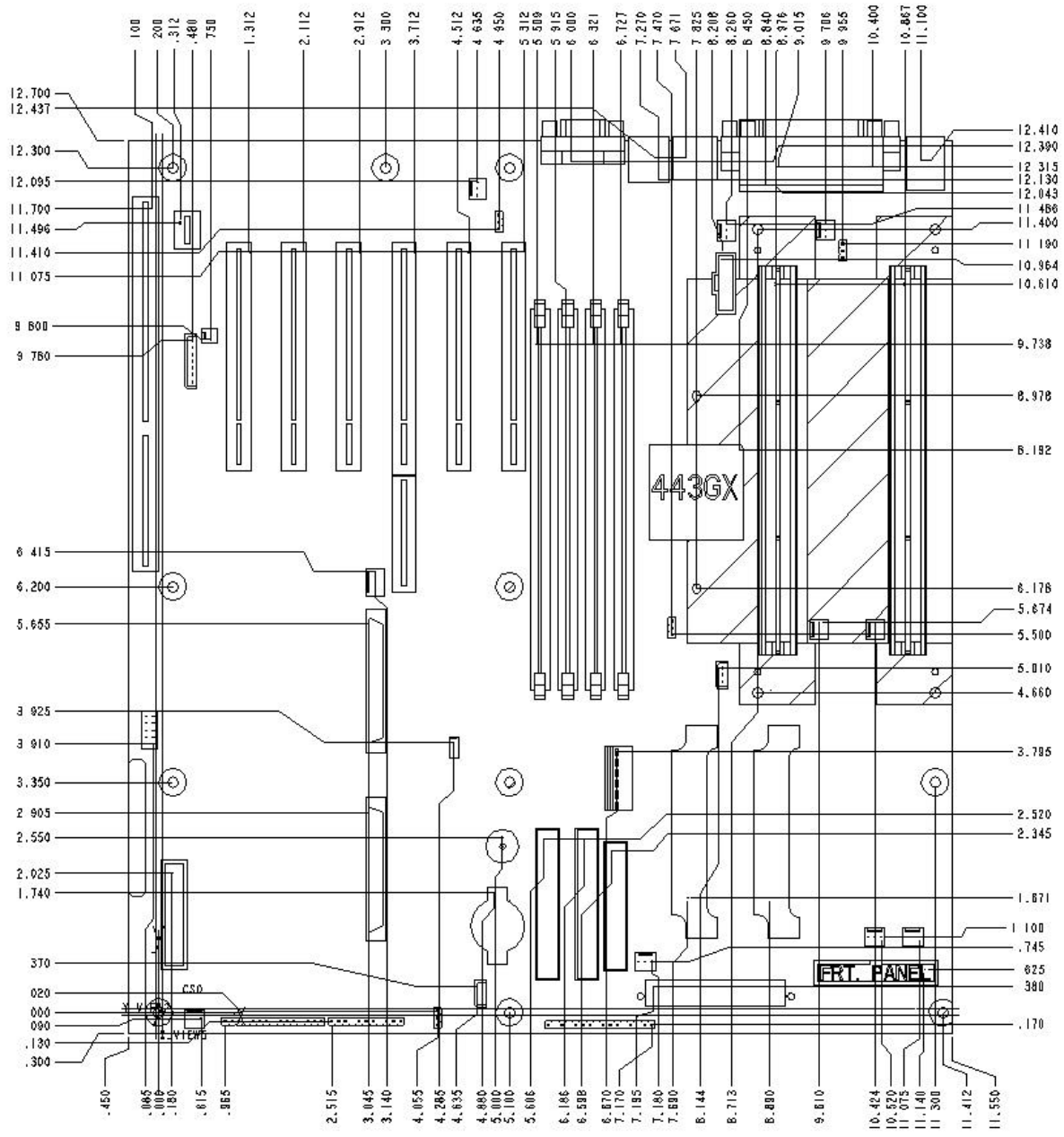


Figure 4-3. C440GX+ Mechanical Drawing

4.3.1 Connector I/O Panel

The following diagram shows the locations of serial, parallel, video, keyboard, and mouse connector interfaces on the system I/O panel, as viewed from the rear of the system.

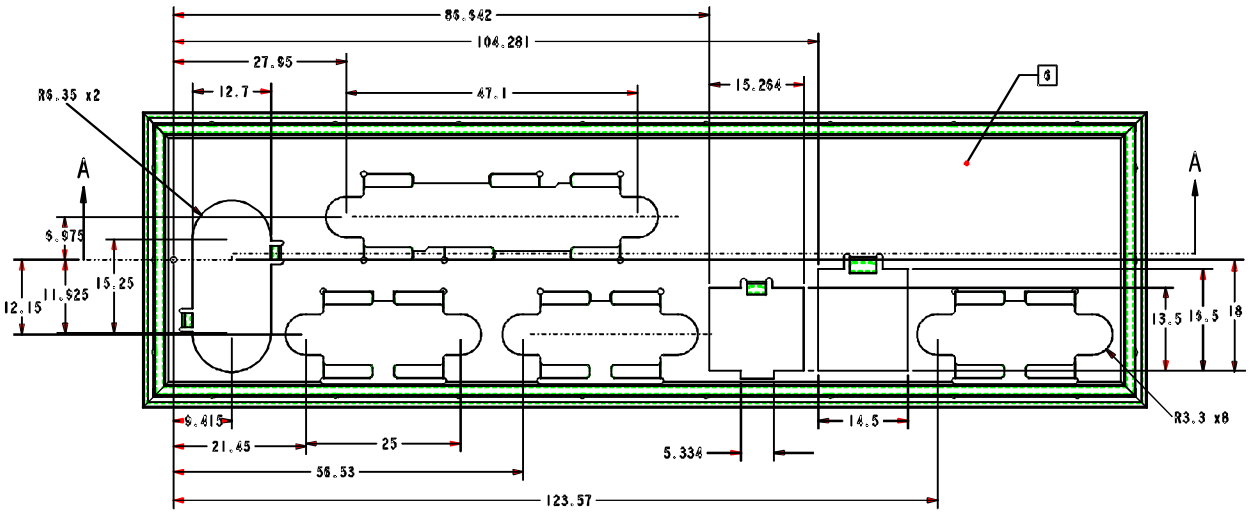


Figure 4-4. I/O Panel Connector Locations

5. System BIOS

This chapter describes those features of the system BIOS that are unique to the C440GX+ Server Board.

Note: The C440GX+ platform does not provide legacy support USB. Legacy mode of USB keyboard emulating a PS/2 keyboard via SMM is not supported on C440GX+. While devices such as USB keyboards work with OS drivers, these keyboards do not respond during BIOS POST.

5.1 BIOS Overview

The term “BIOS," as used in the context of this document, refers to the following:

- System BIOS, that controls basic system functionality using stored configuration values.
- Configuration Utilities (CU) consisting of a Flash ROM-resident Setup utility and Server Setup Utility (SSU), that provides user control of configuration values stored in NVRAM and battery-backed CMOS configuration RAM.
- Flash Memory Update utility (IFLASH), that loads predefined areas of Flash ROM with Setup, BIOS, and other code/data.

5.1.1 System BIOS

The system BIOS is the core of the Flash ROM-resident portion of the BIOS. The system BIOS provides standard PC-BIOS services and industry standards.

Industry Standards

- I_2O
- Plug and Play
- DMI

C440GX+ Specific Features:

- security features
- multiple-speed processor support
- SMP support
- fault resilient booting (FRB)
- logging of critical events
- server management features
- CMOS configuration RAM defaults
- multiple language support
- defective DIMM detection and remapping
- automatic detection of video adapters
- PCI BIOS interface including 66MHz
- option ROM shadowing
- system information reporting
- ECC support
- SMI support
- user-supplied BIOS support
- L2 cache support
- memory sizing
- boot drive sequencing
- resource allocation support

5.1.2 Configuration Utilities (CU)

The CU provides the means to configure on board hardware devices and add-in cards. The CU consists of the following:

- Standard PC-AT Setup utility (a.k.a. BIOS Setup), embedded in Flash ROM, for configuration of on board resources.
- SSU, for configuration of add-in cards as well as on board resources, which must be run from a boot diskette or CD-ROM shipped with the system.

CMOS configuration RAM summary

The PIIX4 chip on the baseboard contains battery-backed CMOS memory for system hardware setup parameters.

5.1.3 Flash Update and ROM Layout

The system BIOS and the setup utility is resident in partitioned Flash ROM. The device is in-circuit re-programmable, except for the recovery boot block, which is electrically protected from erasure. A jumper on the baseboard can enable writing to the boot block region. See section 3.4.1 for configuration jumper locations.

To reload Flash memory from a floppy disk (or from CD-ROM), use a Flash update utility (IFLASH). The file to be loaded contains a new copy of BIOS code. The utility must match the board ID with the one in the load file to protect against reprogramming the Flash with BIOS for another platform. Baseboard revisions may share a common CU but may require different BIOS code.

System Flash ROM Layout

The Flash ROM contains system initialization routines, a Setup utility, and runtime support routines. The exact layout is subject to change. All areas are 64KB in size (symmetric flash). 64KB is reserved for a diagnostic boot loader and an 8KB User block is available for user ROM code or custom logos. A 64KB area is used to store the string database. The complete ROM is visible, starting at physical address 4GB less 512KB. The Flash Memory Update Utility (IFLASH) loads BIOS components to blocks of specified length and location. None of the blocks are visible at the alias addresses below 1 MB due to shadowing. The BIOS alone needs to know the exact map. All blocks in this flash part are 64k (10000h) in length. The BIOS adjusts the size of each component to fit in a given block. Only the Recovery block, ESCD and DMI are fixed at a given location.

5.2 Security Features

The BIOS provides a number of security features. This section describes the security features and operating model.

5.2.1 Operating Model

Table 5-1 Security Features Operating Model, summarizes the operation of security features supported by the BIOS.

Table 5-1. Security Features Operating Model

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Secure mode	Keyboard Inactivity Timer, Runtime activation of KBC Hotkey	"User Password" enabled in CU	Screen goes blank (if enabled in CU). Floppy writes are disabled (if selected in CU). Power and Reset switches on the front panel are disabled(if enabled in Setup). No mouse or keyboard input is accepted.	"User Password"	Video is restored. Floppy writes are enabled. Power and Reset switches are enabled. Keyboard and mouse inputs are accepted.
Secure boot	Power On/Reset	"User Password" and Secure Boot Enabled in CU	Enter secure mode. Prompts for Password, if booting from drive A. Video is blanked (if enabled in Setup). Floppy writes are disabled (if programmed in CU). Power and Reset switches on the front panel are disabled(if programmed in CU). No mouse or keyboard input is accepted; however, the Mouse driver loads before a password is required. If booting from drive A, and the user enters correct password, the system boots normally.	"User Password"	Floppy writes are enabled. Power and Reset switches are enabled. Keyboard and mouse inputs are accepted. System attempts to boot from drive A. If the user enters correct password, and drive A is bootable, the system boots normally
Password on boot "User Password" boot (AT style)	Power On/Reset	"User Password" set and password on boot enabled and Secure Boot Disabled in CU	System halts for "User Password" before booting. The system is not in secure mode. Video is blanked (if enabled in CU). Floppy writes are disabled (if programmed so by CU). No mouse or keyboard input is accepted.	"User Password"	Keyboard and mouse inputs are accepted. The system boots normally. Boot sequence is determined by CU options.
Diskette Access	Power On/Reset	Set feature to Admin in CU	"User" is prevented from accessing the floppy drive. "Administrator" is always prevented from accessing the floppy drive.	Set feature to "User" in CU	"User" is allowed to access the floppy drive.

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Fixed disk boot sector	Power On/Reset	Set feature to Write Protect in CU	Write protects the boot sector of the hard drive to prevent viruses from corrupting the drive.	Set feature to Normal in CU	Hard drive behaves normally.

5.2.2 Password Protection

Through the use of passwords, the BIOS prevents unauthorized tampering with the system. Once secure mode is enacted, access to the system is allowed only after you have entered the correct password(s). Each of two passwords, for "User" and "Administrator", can be created during system configuration using the Configuration Utilities (CU). An individual that may be doing maintenance to the given server uses the "User" password. An individual that may be changing the configurations to the Network uses the "Administrator" password.

Once secure mode is enacted, access to the system is allowed only after you have entered the correct password. Each password, "User" and "Administrator", can be created during system configuration using the CU. Once set, a password can be disabled by changing it to a null string. The "User" password can still modify the time and date, but other fields can only be modified if the "Administrator" password is entered. For example, system hardware configuration can be controlled by the "User" password, while "Administrator" controls access to the machine's file system. If only an "Administrator" password is set (no "User" password), this password is requested when entering Setup and must be entered before the majority of the fields can be modified. If only the "User" password is set (no "Administrator" password), the "User" password must be entered to access Setup, but all fields can be modified once entered.

Once set, a password can be disabled by changing it to a null string.

Inactivity timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified time-out period, the following occurs until the "User" password is entered:

- Keyboard and mouse input is disabled
- Video is blanked (if programmed in CU)
- Floppy drive is write protected (if enabled)

Hot key activation

A Hotkey combination can activate secure mode immediately, rather than having to wait for the inactivity time-out to expire. The Hotkey combination is set using the CU. The following keys are valid hot keys: A-Z, 0-9.

Password clear switch

The BIOS determines if the password clear jumper is set. If set, all passwords are cleared from CMOS and password protection is disabled.

5.2.3 Floppy Write Protection

If enabled by the CU, floppy disk writes are blocked from anyone accessing it when the system is in secure mode. Floppy write protection is only in effect while the system is in secure mode. Otherwise, write protection is disabled and writes are then enabled.

5.2.4 Power Switch and Reset Button Lock

If enabled by the CU, the power switch and reset button are disabled when in secure mode.

5.2.5 Secure Boot (Unattended Start)

Secure Boot allows the system to boot and run the OS. However, until the "User" password is entered, mouse and keyboard input is not accepted and the front panel reset/power switches are disabled. The CU is used to place the system into secure boot mode. In secure boot mode, if the BIOS detects a floppy disk in the A drive at boot time, it prompts the "User" for a password. When the password is entered, the system can boot from the floppy and secure mode is disabled. Any one of the secure mode triggers cause the system to go back into secure mode. If there is no disk in drive A, the system boots from the next boot device and is placed in secure mode automatically. All of the enabled secure mode features go into effect at boot time.

5.2.6 Interaction with External Utilities

External utilities that need to perform password validation, such as SSU, can call the appropriate BIOS interface. The BIOS performs the password validation and returns the status. The interface is not described here for security reasons.

5.3 Auto-Configuration Features

The BIOS provides support for auto-configuration of the following:

- Plug and Play
- Processor speed
- SMP initialization
- Memory sizing
- Boot drive selection
- Mouse and keyboard swapping
- Pentium® II processor BIOS update
- LCD support

5.3.1 Plug and Play

The BIOS supports the following industry standards for full Plug and Play capabilities:

- Plug and Play (PnP) ISA specification
- Server Management (SM) BIOS specification 2.1
- Extended System Configuration Data Specification (EISA is not supported).
- PCI local Bus specification

Resource allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel servers. The BIOS scans for the following, in order:

1. ISA devices: If an ISA device is found, it is initialized and given resource priority over other devices of the same type plugged into the system.
2. Off board PCI devices: If found, the BIOS initializes and allocates resources to these devices.
3. On board Video, IDE, and SCSI devices: If equivalent functionality is not found off board, the BIOS allocates resources according to the parameters set up by the SSU.

PnP ISA auto-configuration

The BIOS:

- Fully supports the PnP ISA protocol
- Reads the PnP ISA configuration port
- Assigns the system I/O, memory, DMA channels, and IRQs from the resource pool
- The Super I/O chip is an example of a PnP ISA device.

PCI auto-configuration

The BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the PCI specification, Rev. 2.1. The System BIOS also supports the 16 and 32-bit protected mode interfaces as required by the PCI BIOS specification. System POST performs auto-detection and auto-configuration of ISA, ISA Plug-N-Play, and PCI devices. This process maps each device into memory and/or I/O space, and assigns IRQs and DMA channels as required, so that there are no conflicts prior to booting the system. The BIOS scans the PCI devices on each PCI bus in low to high sequence. The PCI busses are also scanned in the same order. The BIOS programs the PCI-ISA interrupt routing logic in the BUD to steer PCI interrupts to compatible ISA IRQs.

The BIOS detects the presence of I_2O compliant intelligent controllers, such as an i960 RD, and configures them as documented in the I_2O BIOS specification. The BIOS then queries each I_2O IOP to determine if it controls a PCI device. If a PCI device is controlled by an IOP, The BIOS does not enable the device and therefore does not allocate IRQ resources.

Drivers and OS programs can determine the installed devices and their assigned resources using the BIOS interface functions. The BIOS does not support devices behind PCI-to-PCI bridges that require mapping to the first 1 MB of memory space. The IRQ assigned to a PCI card can be overridden by using the System Setup Utility(SSU).

Legacy ISA configuration

Unlike Plug-N-Play cards, he BIOS cannot determine resource requirements for legacy ISA cards. Further, legacy ISA cards require fixed resources and cannot be software configured. The SSU can be used to reserve system resources required by Legacy ISA cards and save the information in NVRAM. The POST resource management does not allocate the resources that are reserved for legacy ISA cards to PnP devices.

On-board device auto-configuration

The BIOS detects all on board devices and assigns appropriate resources. The BIOS dispatches the option ROM code for the on board devices to a DOS compatibility location (C0000h to E7FFFh) and transfers control to the entry point. An option, configurable in the BIOS setup utility, can disable the BIOS from scanning the on-board Adaptec SCSI ROM.

Automatic detection of video adapters

The BIOS looks for video adapters in the following order:

1. ISA
2. PCI
3. Baseboard

The on-board (or add-in) video BIOS is shadowed, starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to add-in devices.

5.3.2 Multiple Processor Support

The BIOS supports single or dual Pentium II Xeon or Pentium III Xeon processor configurations. If only one processor is installed, the other slot must be populated with a terminator. In a single processor system the APIC tables are dynamically updated to reflect the actual status of good processors in the system.

Multiprocessor specification support

The BIOS complies with all requirements of the Intel Multi-Processor Specification (MPS) version 1.4 for Symmetric Multi-Processor (SMP) support, as well as MPS version 1.1, for backward compatibility. The version number can be configured using the CU. The base MP Configuration Table contains the following entries:

- MP table header
- Processor entries
- PCI bus entries
- I/O APIC entries
- I/O interrupt entries
- Local interrupt entries

The extended MP table is constructed if MPS version 1.4 is selected. It contains these entries:

- System address space mapping entries
- Bus hierarchy descriptor
- Compatibility bus address space modifier entries

Note: The MP APIC tables are the only places where the number of processors are dynamically reported from boot to boot.

Multiple Processor Support

On a system reset, whichever processor successfully passes BIST is automatically selected by the hardware as the BSP and starts executing from the reset vector (F000:FFF0h). A processor that does not perform the role of BSP is referred to as an Application Processor (AP).

The BSP is responsible for executing POST and preparing the machine to boot the OS. BIOS performs several other tasks in addition to those required for MPS support, as described in *MP Specifications*, Rev. 1.4. These tasks are part of the fault resilient boot algorithm. During POST the system is in virtual wire mode and the BSP alone is programmed to accept local interrupts (INTR driven by the PIC and NMI). As a part of the boot process, the BSP enables the AP. When enabled, the AP programs its memory type range registers (MTRRs) so that they are identical to those of the BSP. The AP executes a halt instruction with its local interrupts disabled.

Multiple Processor Speed Support

In dual processor configurations, the BIOS is capable of supporting processors with different stepping revisions. However, the stepping for each processor must be within 1 rev of each other. Both processors must have identical cache sizes, bus and core frequencies. Also, for best performance, all processors must be of the same CPU ID. The type and speed of detected processors are reported by the CU.

5.3.3 Memory Sizing http://support.intel.com/support/motherboards/server/C440GX/

During POST the BIOS:

- Tests and sizes memory
- Configures the memory controller

The C440GX+ supports various sizes and configurations of SDRAM DIMMS. Only memory listed on the Qualified Memory List, available at http://support.intel.com/support/motherboards/server/c440gx, are supported. The BIOS gathers type, size, speed and memory attributes from the on-board EEPROM or SPD located on the DIMM.

A memory sizing algorithm determines the size of each DIMMs. The BIOS reads the DIMM speed information and programs the PAC accordingly. BIOS will not perform the extended memory test if configured in the CU. Disabling the extended memory test reduces the boot time. The BIOS is capable of detecting, sizing, and testing any amount of RAM, up to the physical maximum of 2 GB.

The BIOS is capable of reporting up to 64 MB using INT 15h, AH = 88h, or INT 15h, function E801h, which can report up to 4,096 MB. INT 15h, function E820h supports reporting of the system memory regions.

5.3.4 Boot Device Selection

The BIOS conforms to the Phoenix* BIOS boot specification 1.01. The BIOS boot specification describes a method where the BIOS identifies all Initial Program Load (IPL) devices in the system, prioritizes them in the specified order, and sequentially goes through each device and attempts to boot. It is possible to use the CU to change the boot order of devices connected to the system. In cases where the boot order is changed, the system boots in the order chosen, with the exception of legacy devices. Legacy devices are those devices that tend to take control of the boot process altogether by hooking boot vector (interrupt 19h). Further, they provide no means for identifying themselves as an IPL device. Therefore, the BIOS cannot selectively boot from one of several Legacy IPL devices in a system. The CU gives the option of selecting the first boot device as either a floppy drive, a CDROM, a hard drive or an I_2O device. The system BIOS tries to boot from devices in the order specified. Further, the user can reorder the hard drives and choose the primary boot drive to be any IDE drive or any drive that is controlled by a Boot BIOS compliant option ROM BIOS. Hard drives that are controlled by all other controllers appear as 'Other bootable cards" in the setup menu. These controllers cannot have their drive order controlled. Some RAID card option ROM BIOS's may show all the drives as a single device, and may not allow the user to manipulate the order on a drive by drive basis.

5.3.5 Mouse and Keyboard Swapping

The keyboard and mouse connectors are not device dependent. The connectors are interchangeable. The BIOS detects the devices during POST and initializes the KBC accordingly. Hot plugging of the mouse and keyboard is not supported on C440GX+ and may have unpredictable results.

5.3.6 Boot Without Keyboard

The system can boot with or without a keyboard. There is no entry in the CU for keyboard enable/disable. The presence of the keyboard is detected automatically during POST, and the keyboard is tested if present. The BIOS does not detect or use Universal Serial Bus (USB) keyboards.

5.3.7 CMOS Clear and Jumperless Processor Clock Ratio Settings

The BIOS has a front panel method of resetting system CMOS settings in addition to the standard jumper on the baseboard. During boot if the CMOS jumper on the baseboard is set before power on, the BIOS scans the pin on the PIIX4 and resets the system to CMOS. The following conditions also clear CMOS from the front panel:

1. System is off (5Vcc is off but 5v standby is present)
2. Reset button is held for at least 4 seconds.
3. While the reset button is held, the on/off button is pressed and system is shutdown
4. Depress both on/off button and reset at same time.

This requires that the BMC supply a command to the system BIOS indicating the user has completed the correct front panel button sequence. The BIOS clears CMOS as if the user had moved the CMOS clear jumper on the baseboard. Only in this one boot sequence should the CMOS be cleared. The BMC releases the CMOS clear line once the BIOS has acknowledged the CMOS clear and release it (back to 1). A reset or power down also removes the CMOS clear condition from the BMC (release is back to 1).

1. CMOS clear also reverts the system back to the lowest common clock speed for all available processors (350MHz and CACHE disable). The user needs to reboot the system once more without the CMOS clear jumper so that the actual processor speed for processors in the system is set to a clock speed default of (300MHz CACHE enable).
2. The CMOS clear setting also forces all SCSI option ROMs to their default state.

The C440GX+ will also use a serial EEMUX to allow jumperless settings of the bus to clock ratio

settings. The user will now be able to select the processor clock frequency from a BIOS setup menu.

5.4 Performance Features

For enhanced performance, the BIOS configures the processor's L2 cache controller and performs option ROM shadowing.

5.4.1 L2 Cache Initialization

To boost system performance, BIOS programs L2 cache controllers of each processor in a manner that is consistent with the other processor and the AGP set.

The L2 cache is tested as a part of the processor BIST. If the L2 cache is bad, the processor indicates the error in the BIST and the BIOS disables the Processor. The BIOS detects the cache size and cache type (ECC or non-ECC), and programs the cache controller accordingly before performing any cache operations. The BIOS displays a warning message on the screen if the two processors have different cache sizes. Not all bus to core ratio settings support L2 cache enabled. Some bus to core ratios are not allowed by the processor and the BIOS will disable the cache accordingly with the registers in the processor.

Cache State on Boot

The BIOS looks at a bit in CMOS to determine if the system caches should be enabled or disabled. The user can modify the bit in the Boot Options of the Setup Main menu. If the cache is enabled, cache controllers in all processors are initialized in a consistent manner with each other and the 82440GX AGP Set.

5.4.2 Option ROM Shadowing

All on board adapter ROMs (stored in compressed form in the system Flash ROM), and PCI adapter ROMs are shadowed into RAM in the ISA-compatible ROM adapter memory space between C0000h to E7FFFh. The BIOS ROM found on ISA devices are shadowed (if capable) into adapter memory space in the same range after initialization. Shadowing for ISA devices can be disabled for various regions using the CU. PCI BIOS ROMs are always shadowed. Typically the onboard video BIOS is shadowed at C0000h.

5.4.3 Memory Speed Optimization

The BIOS detects the system memory speed and bus speed and optimizes the memory controller for the best performance.

The system bus speed can be detected by the processor internal speed and the bus ratio. The memory DIMM speed can be detected by its ID. Using this information the BIOS can set up the memory controller register for the best performance.

5.4.4 AGP set Performance Optimization

The BIOS detects the system configuration, such as board ID, AGP set stepping, processor stepping, and optimizes the AGP set for the best performance. Most of the AGP set registers are automatically set. The BIOS no longer supports a 1 Megabyte hole at the 15-16 Megabyte memory regions. The user may be allowed to control a limited number of performance features. For optimal system performance it is not recommended to change any of the default PCI timing settings.

5.5 Reliability Features

The BIOS supports several features to create a robust computing environment including the following:

- ECC memory and defective DIMM handling
- Fault resilient booting
- Logging of critical events
- CMOS default override
- Emergency Management port
- Platform Event Paging

5.5.1 Defective DIMM Detection and Remapping

The ECC memory subsystem on C440GX+ is able to detect single-bit errors (SBE) and certain multi-bit errors (MBE) during reads from and writes to system DRAM. Single-bit errors can be detected and corrected. Certain patterns of MBEs can be detected but cannot be corrected, whereas other types of MBEs cannot be detected.

During POST memory testing, detection of single-bit and multi-bit errors in DRAM banks is enabled. An error is avoided by reducing the usable memory in that bank so that the byte containing the hard error is no longer accessible. The BIOS logs the errors in the nonvolatile system event log. The BIOS detects the speed of individual DIMMs and disables a DIMM that is slower than what the hardware requires and displays a warning message.

Memory Configuration Algorithm

The algorithm for determining memory configuration is as follows:

If there is no DIMM population, or the DIMMs are all bad, or have the wrong speed, the BIOS sounds a beep code error and POST is terminated. The BIOS requires at least 4 MB of good memory for POST to start up. The BIOS individually probes each bank for the size, speed and type of each DIMM and programs the AGP set accordingly. If the bank does not match one of the allowable configurations, the BIOS reports the error with an error message. All configuration data for memory is gathered by the BIOS from the SPD or EEPROM on the DIMM. This is done via the SMBUS interface on the PIIX4.

In the event that the BIOS disables or resizes a bank, an error message displays with the DIMM number of the failing memory. Another message informs the user that the amount of usable memory in that bank is being reduced to eliminate the failing location. Eliminating hard errors in this way during POST is done as a precaution to prevent an SBE from becoming an MBE after the system has booted and to prevent SBEs from being detected and logged each time the failed location(s) are accessed. This is recorded in the SEL (System Event Log) at both post time as well as runtime with an SMI. This is implemented as an EEPROM that the BMC can access directly with the server on or off.

If the error is a SBE, the 440GX automatically corrects the data before it is returned to memory. The 440GX memory controller scrubs the memory location where the error occurred to correct the SBE and the BIOS will record the SBE via an SMI to the SEL. If the error is an MBE, this condition is considered fatal, and after the error is logged, an NMI is generated, telling the OS to handle this fatal error.

Note: EDO memory is not physically supported due to the memory socket used on the baseboard.

ECC Memory Initialization

The system BIOS handles ECC memory initialization. All memory locations, including System Management RAM and shadow memory region, are unconditionally initialized during POST (set to 0). Error detection is disabled while ECC memory is initialized to prevent false alarms caused

by uninitialized memory bytes. If hard errors are detected during the memory test, the memory partition containing the error is resized to eliminate the failing locations.

ECC and SMI Support

During normal operation, any SBEs (single bit errors) are detected and logged by the SMI support code. The SMI code keeps up to 3 records of the last SBE logs in the system event log. The 440GX memory controller cannot locate the exact address of the error, but can only point to the row that contains the error location. Memory scrubbing is performed by hardware and is always automatically enabled when ECC memory is detected. The row containing the failing location is scrubbed by reading the corrected data and writing back the correct data automatically by the memory controller. If MBEs are detected, the BIOS SMI handler will log an event into the SEL (System Event Log) and then generate an NMI to the OS. This functionality is part of the server management control, which the BMC provides with its non-volatile storage device (available out of band).

5.5.2 Fault Resilient Booting (FRB)

The BIOS and firmware provides a feature to guarantee that the system will boot even if one processor fails during POST or hangs while booting to the O/S. The BMC contains 2 watchdog timers that if they trip will reset the system. The first timer (FRB-3) starts counting down whenever the system comes out of hard reset and usually is about 5 seconds. If the BSP successfully resets and starts executing the BIOS will disable the FRB-3 timer in the BMC and system will continue on with POST. If the timer expires because of the BSP's failure to fetch or execute BIOS code, the BMC resets the system and disables the failed processor. The system will continue to reset alternating BSP's between the primary and secondary processor socket until the BIOS POST gets past disabling the FRB-3 timer in the BMC.

The second watchdog timer (FRB-2) in the BMC is set to 5-6 minutes and is designed to guarantee that the system will complete BIOS POST. Near the end of POST, before the options ROMs are initialized, the BIOS will disable the FRB-2 timer in the BMC. If the system hangs during POST, the BIOS will fail to disable the timer in the BMC which generates an ASR (Asynchronous System Reset). In a dual processor system the BIOS will register the AP in the MP table. When started by the BSP, if an AP fails to complete initialization within a certain time, it is assumed to be non-functional. This AP is not listed in the MP table and is invisible to the OS. If either processor fails the BIST it is marked bad and removed from the MP table. The BIOS will disable the processor and reset the system to make sure the failed processor will be electrically disabled on the next boot.

The BMC maintains a flag bit in non-volatile ROM for each processor. This bit is used to store a processor's track record. It is set whenever a processor fails and remains so until the user forces the system to retest the processor and it successfully makes it past both FRB timers. The BIOS reminds the user about a previous processor failure during each boot cycle and keeps that processor disabled until the status flag is cleared by the user. Processors that have failed in the past are not allowed to become the BSP, and are not listed in the MP table. It might happen that all the processors in the system are marked bad. An example is a uniprocessor system where the processor has failed in the past. If all the processors are bad, the BIOS does not alter the BSP and attempts to boot from the original BSP. It also informs the user that it is trying to boot from a failed processor if the POST gets executed. Error messages (defined in *Chapter 5: Error Handling*) are displayed on the console, errors are logged in the event log if a processor fails. The failed processor is identified by its number.

Any one of the failures (FRB-3, FRB-2 and BIST) are recorded to the BMC server event log. The processor (s) that failed are recorded as well.

If the FRB jumper on the baseboard is set to disable, the FRB-3 and FRB-2 timer shall never time-out. This effectively disables all FRB time-out features on the baseboard.

5.5.3 Logging System Events

If enabled by the configuration utility or BIOS setup, the BIOS can log critical and informational events to nonvolatile memory. This area is managed by BMC and can be accessed by sending commands to BMC. A critical event is one that might result in the system being shut down to prevent catastrophic side effects from propagating to other parts of the system. Multi-bit and parity errors in the memory subsystem are considered critical errors, as are most errors that generate a Non-Maskable Interrupt (NMI), which might subsequently generate a System Management Interrupt (SMI). These errors include I/O channel check, software generated NMI, and PCI SERR events. During POST, the BIOS initializes System Management RAM (SMRAM) with error handling and logging code. Each processor has a private area of SMRAM dedicated to it for SMI processing. The DRAM controller and PIIX4 are programmed to generate an SMI for PCI SERR, software generated NMI, I/O channel check, and ISA watchdog time-out and NMIs generated by the PAC. The PAC generates an SERR if parity/ECC errors are observed in the memory subsystem. The PAC generates an interrupt if a single-bit correctable error is observed in the memory subsystem. The PIIX4 can be programmed to generate an SMI on this interrupt. When these errors are detected, the SMI routines log the error or event in a manner that is transparent to the OS and then causes an NMI to be generated for certain events, so that the OS can respond appropriately. The BIOS also logs an event on another type of memory error called Single Bit Error (SBE). For this error, the BIOS will not generate an NMI to the OS. BMC may independently log events and is responsible for serializing accesses to the area.

If the OS device driver is using the watchdog timer to detect software or hardware failures and that timer expires, an Asynchronous Reset (ASR) is generated, which is equivalent to a hard reset. The POST portion of the BIOS can query BMC for watchdog reset event as the system reboots, and logs this event to the logging area. Failure of a processor during POST will also be logged in the Flash during POST.

5.5.4 Emergency Management Port (EMP)

The COM2 serial port on C440GX+ can be configured for use as an Emergency Management Port (EMP). EMP provides a level of system management via RS-232 during powered-down, pre-boot, and post-boot situations. This allows system management software (SMS) interactions via point-to-point RS-232 connections, or external modem. EMP provides access to these basic management features:

- System power control (on/off remotely)
- Access to the event log, system serial # and model #, and sensor data logs in the BMC
- System reset
- NMI control (Not available in restricted mode)
- Allows BIOS console redirection through the BMC serial port
- Password security protection for EMP serial port
- Access to status of real time events in BMC

The EMP is intended for use in a secure environment. A simple password can be configured to provide a rudimentary level of security on the interface. System configuration options can be used to disable this interface.

The COM2 port can be used on C440GX+ for three different purposes: EMP, console redirection, or normal COM usage. If the BMC is using the port for EMP purposes, it is unavailable to the BIOS or SMS during this mode. If the System BIOS is using the port for console redirection, it is unavailable to the BMC or SMS (since the machine is still doing POST). Under normal usage COM2 appears to the OS as a normal serial port; in this case the BMC and System BIOS cannot use the port.

The C440GX+ EMP architecture supports several remote access modes, selectable using the F1 BIOS Setup Screen, as follows:

Disabled - COM2 is connected to the Super I/O and never is connected to the BMC. COM2 acts like a serial port on a normal system.

Pre-boot only - The EMP is only available while the machine is powered off and during POST. Just prior to booting the OS, the System BIOS disables the EMP by sending a command to the BMC. COM2 is then available as a normal serial port.

> **NOTE –** In order to utilize the EMP port with the system powered down, AC power is still applied and the system's power supply must provide the minimum required standby current.

Always Active - EMP and Console Redirect are available under the same conditions as listed in Pre-Boot Mode. However, the System BIOS leaves the port enabled for run-time EMP and SMS usage. The BIOS configures the hardware such that the O/S can not "see" the port.

Restricted Mode - This option can be selected in conjunction with either the 'Pre-boot Only' or 'Always Active' modes listed above, using the BIOS setup interface. When activated, Power Down control, Front Panel NMI, and Reset Control via the EMP are disabled. Power On control, System Event Log access, FRU Inventory, and Sensor Data Repository access remain enabled. Console redirection operation is unaffected by Restricted Mode.

SMS Activated Mode - Essentially the same as Pre-boot only, except that SMS software may elect to take ownership or release control of COM2. This mode allows SMS to configure the system for remote access.

EMP Password

The BMC implements a simple password mechanism for the EMP, activated by BIOS setup. If the password is active, a correct password must be received on the EMP before any other commands are accepted. The password must be entered every time COM2 is switched over to EMP operation. It must also be re-entered if the EMP has been inactive for more than 30 seconds. Only BIOS setup can set or clear the password, it cannot be changed remotely.

Escape characters for multiplexer control of COM2 port

The BIOS console redirection will support an extra control escape sequence to force COM2 port over to the BMC. Once this command is sent, the COM2 port will be attached to the BMC EMP serial port and the Super I/O COM2 data will be ignored. This feature is available to the remote user to allow them to monitor the status of POST as the BIOS comes up over COM2 and then take control of the system reset or power from the BMC. If the system does not come up a watchdog time-out feature in the BMC will automatically switch the port over in case the system does not make it through POST.

The character sequence will be "ESC O 9"(also denoted as ^[O9) to switch the multiplexer to the BMC serial port. This key sequence is above the normal ANSI function keys and will never be used by an ANSI terminal.

A restriction of using COM2 for both EMP with BIOS console redirection is that the baud rate is fixed to 19200 baud and the port is setup for N,8,1 Xon/Xoff.

Modem support on EMP

The BMC is only in control of the modem if it is attached to COM2. The BMC always has control of COM2 before POST. The BIOS setup provides a field for modem setup.

5.5.5 Platform Event Paging (PEP)

Platform Event Paging provides the administrator with an out of band alerting mechanism which will dial a paging service and send a page if a problem has been detected on the server. PEP operates on top of the Server Board's BIOS, independent of the Operating System and is powered by the system's 5V Standby current. PEP relies on the Baseboard Management Controller (BMC) which is the server management microcontroller built on to Intel server boards. The BMC runs independently of the system processors, operating system and server management software. It autonomously

monitors the system health and collects platform events into a central System Event Log (SEL).

When PEP is enabled and the BMC receives or detects a new event, the BMC automatically performs the paging operation. Since the BMC is independent of the rest of the system, this allows pages to be sent even when the operating system is unresponsive or the system processors are down.

The following sensors are monitored and can generate a page if the BMC detects a failure from any of these:

- Temperature Sensor
- Voltage Sensor
- Fan Sensor
- Chassis Sensor
- Power Supply Sensor
- BIOS (SMI Handler)
- BIOS POST Error
- FRB Sensor
- Fatal NMI
- Watchdog Timer Reset
- System Restart

Note: The PEP has an 800mA +5V Standby power requirement. This means if the power supply used has the correct requirements for PEP the C440GX+ server board is powered whenever they are plugged in. To ensure the power supply selected fulfills this power requirement see the tested chassis and power supply summary at http://support.intel.com/support/motherboards/server/.

Though PEP uses a modem to dial the paging service, it cannot complete modem "handshakes" used by GSM (Global System for Mobile Communications) networks utilizing SMS (Short Message Service). This limitation makes functionality of PEP on any GSM network dependent on the carrier's ability to support touch tone inputs from a POTS. This mainly affects certain areas in Europe and Asia, however check with your paging service to ensure you can support PEP.

5.6 Console Redirection

The BIOS supports redirection of both video and keyboard via a serial link (COM 1 or COM 2). When console redirection is enabled, local (Host Server) keyboard input and video output is passed both to the local keyboard and video connections, and to the remote console via the serial link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs. Optionally, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console. Both Setup and the SSU can be accessed via console redirection. This feature is only designed to work with BIOS POST and DOS in standard text mode since most operating systems today no longer use real mode BIOS calls to communicate to the keyboard and video. This feature was intended to allow remote operation of the server for BIOS setup and the SSU. It is not tested or maintained under any other software.

5.6.1 Operation

When redirecting through a modem (as opposed to a Null modem cable), the modem needs to be configured as follows:

Auto-answer (for example, ATS0=2, to answer after 2 rings)

Modem reaction to DTR set to return to command state (for example, AT&D1)

Failure to provide #2 above causes the modem to either drop the link when the Server reboots (as in AT&D0), or make the modem unresponsive to Server baud rate changes (as in AT&D2).

The BIOS Setup/SSU option for handshaking must be set to CTS/RTS + CD. The CD refers to Carrier

Detect. In selecting this form of handshaking, the Server is prevented from sending video updates to a modem that is not connected to a remote modem. If this is not selected, video update data being sent to the modem disables many modems from answering an incoming call.

Once Console Redirection is selected via BIOS Setup or SSU, redirection is loaded into memory and activated during POST. While redirection cannot be “removed” without rebooting, it can be disabled and restarted. When disabled, the serial port is released by redirection and might be used by another application. Restarting reclaims the serial port and continues redirection. Disabling/restarting is accomplished through the following INT 16h mechanism. The standard INT 16h (Keyboard handler) function ah=05h places a keystroke in the key buffer, just as if an actual key had been pressed. Keystrokes so buffered are examined by redirection, and if a valid command string has been sent, it is executed. The following commands are supported in this fashion:

Esc-CDZ0 - Disable Console Redirection.

Esc-CDZ1 - Restart Console Redirection.

In order to disable redirection, the software must call INT 16h, function ah=05h five times to place the five keys in the key buffer. Keystrokes sent to the INT 16h buffers for purposes of invoking a command are buffered, and should be removed via the normal INT 16h calls to prevent these keystrokes from being passed on to another application. This feature was intended to allow downloading of files via Zmodem or Xmodem to the host server system from the remote target. BIOS iFlash update or the SSU could be downloaded to the host system in this manner and run remotely. This allows remote upgrade of the system software.

5.6.2 Keystroke Mappings

During console redirection, the **remote** terminal (which may be a dumb terminal or a system with a modem running a communication program, such as ProComm or Qmodem) sends keystrokes to the host server. The host server passes video back over this same link.

For keys that have an ASCII mapping, such as A and Ctrl-A, the remote simply sends the ASCII character. For keys that do not have an ASCII mapping, such as F1 and Alt-A, the remote must send a string of characters, as defined in the following tables. The strings are based on the ANSI terminal standards. Since the ANSI terminal standard does not define all the keys on the standard 101 key U.S. keyboard, mappings for these keys were created, such as F5 - F12, Page Up, and Page Down.

Alt key combinations are created by sending the combination **^[}** followed by the character to be ALT modified. Once this Alt key combination is sent (^[}), the next keystroke sent will be translated into its alt-key mapping (that is, if ^[} is mapped to Shift-F1, then pressing Shift-F1 followed by ‘a’ would send an Alt-a to the server).

The remote terminal can force a refresh of its video by sending **^[{**.

Presently, unusual combinations outside of the ANSI mapping and not in the table below, are not supported (for example, Ctrl-F1).

Table 5-2. Non-ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
ESC	^[	NS	NS	NS
F1	^[OP	NS	NS	NS
F2	^[OQ	NS	NS	NS
F3	^[OR	NS	NS	NS
F4	^[OS	NS	NS	NS
F5	^[OT	NS	NS	NS
F6	^[OU	NS	NS	NS
F7	^[OV	NS	NS	NS
F8	^[OW	NS	NS	NS
F9	^[OX	NS	NS	NS

F10	^[OY	NS	NS	NS
F11	^[OZ	NS	NS	NS
F12	^[O1	NS	NS	NS
EMP mux swch	^[O9	NS	NS	NS
Print Screen	NS	NS	NS	NS
Scroll Lock	NS	NS	NS	NS
Pause	NS	NS	NS	NS
Insert	^[[L	NS	NS	NS
Delete	(7Fh)	NS	NS	NS
Home	^[[H	NS	NS	NS
End	^[[K	NS	NS	NS
Pg Up	^[[M	NS	NS	NS
Pg Down	^[[2J	NS	NS	NS
Up Arrow	^[[A	NS	NS	NS
Down Arrow	^[[B	NS	NS	NS
Right Arrow	^[[C	NS	NS	NS
Left Arrow	^[[D	NS	NS	NS
Tab	(09h)	NS	NS	NS
NS = Not supported, (xxh) = ASCII character xx				

Note: ESC [O9 reserved for EMP port multiplexer switch control.

Table 5-3. ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
Backspace	(08h)	(08h)	(7Fh)	^[}(08h)
(accent) `	`	(tilda) ~	NS	^[}`
1	1	!	NS	^[}1
2	2	@	NS	^[}2
3	3	#	NS	^[}3
4	4	$	NS	^[}4
5	5	%	NS	^[}5
6	6	^	NS	^[}6
7	7	&	NS	^[}7
8	8	*	NS	^[}8
9	9	(	NS	^[}9
0	0	)	NS	^[}0
(dash) -	-	(under) _	(1Fh)	^[}-
=	=	+	NS	^[}=
a to z	a to z	A to Z	(01h) to (1Ah)	^[}a to ^[}z
[	[	{	(1Bh)	^[}[
]	]	}	(1Dh)	^[}]
\	\	|	(1Ch)	^[}\
(semi-colon) ;	;	(colon) :	NS	^[};
(apostrophe) '	‘	(quote) "	NS	^[}'
(comma) ,	,	<	NS	^[},
(period) .	.	>	NS	^[}.
/	/	?	NS	^[}/
(space)	(20h)	(20h)	(20h)	^[}(20h)

NS = not supported, (xxh) = ASCII character xx

5.6.3 Limitations

Console redirection is a Real Mode BIOS extension, and does not operate outside of Real Mode. Console redirection does not work once the OS or a driver like EMM386 takes the processor into protected mode. If an application takes the processor in and out of protected mode, it should disable redirection before entering protected mode and restart it once back into real mode. Video is redirected by scanning and sending changes in text video memory. Thus, console redirection is unable to redirect video in graphics mode. Keyboard redirection functions via the BIOS INT 16h handler. Software bypassing this handler does not receive redirected keystrokes.

5.7 Intelligent I/O (I_2O) Support

The BIOS is I_2O ready. It does not have an on-board I_2O bridge but will support I_2O cards in any PCI slot.

5.8 DMI Support

Desktop Management Interface (DMI) is a method of managing computers in an enterprise configuration. The main component of DMI is the Management Information Format Database, or MIF. This database contains all the information about the computing system and its components. Using DMI, a system administrator can obtain the types, capabilities, operational status, installation date, and other information about the system components. The Desktop Management BIOS Specification documents a standard embedded toolset to assist in the generation of a system MIF database.

The BIOS complies with DMI BIOS specification 2.0 and implements all the mandatory function calls. The DMI BIOS follows the System Device Node model used by Plug and Play, and uses Plug and Play BIOS functions to access DMI information. Plug and Play functions 50h-5Fh are assigned for the DMI BIOS interface. Each of the DMI BIOS Plug and Play functions are available both in real- mode and 16-bit protected mode. General Purpose Nonvolatile (GPNV) storage as defined in the DMI BIOS specification, Revision 2.0 will be provided. The total size of the GPNV storage area is at least 128 bytes. The exact size depends upon availability of non-volatile memory. A *Handle* parameter is passed into GPNV function calls to specify which GPNV area is to be accessed.

5.9 POST Memory Manager

The BIOS supports revision 1.0 of the PMM (POST Memory Manager) specifications. This specification allows external clients, such as option ROMs, to request a memory buffer during initialization and release it later. Without the PMM, the option ROMs may overwrite buffers used by the system BIOS or another client. Check with your plug-in card vendor to make sure that their PCI or ISA option ROM is PMM compliant. Being PMM compliant will ensure that the plug in cards will not cause system hangs or memory conflicts during post initialization of Option ROMs.

5.10 Wired for Management (WFM)

Wired for Management is an industry wide initiative to increase overall manageability and reduce total cost of ownership. WFM allows a server to be managed over network. The C440GX+ BIOS supports Wired For Management baseline specification 2.0 for Servers. The PXE is a selectable boot device in the BIOS setup boot menu. System BIOS contains hooks to support such a network card. System BIOS will support SM BIOS specification 2.0 to help higher level instrumentation software to meet the WFM requirements. The higher level software can use the information provided by SM BIOS to instrument DMI standard groups that are specified in WFM specification. The BIOS also sets up the SYSID table as described in NetPC specification. This table contains the globally unique ID (GUID) of the baseboard. The mechanism that sets the GUID in factory is defined in SYSID Interface Specification. The caller must provide the correct security key for this call to go through.

5.11 Power Switch

The C440GX+ supports up to 3 front panel buttons. The power button, the reset button and an NMI button. The NMI button is not accessible on all front panel designs.

The power button in the C440GX+ design is a request that is forwarded by the BMC to the power state machine in the PIIX4. It is monitored by the BMC and does not directly control power on the power supply. The BMC will convert all push buttons to SMI's on the PIIX4.

Off to On: The BMC monitors the power button and turns the system on. The BIOS is not running so it does not participate. The PIIX4 receives power good and reset to get into the ON state. PIIX4 may be setup for several different events to turn on the system: Wake on LAN and Real Time Clock Alarm. The Real Time Clock alarm can be setup in the standard CMOS locations 0 through 0Ch. Wake on LAN can be setup via the Wired for management interface to the 82558 on board NIC.

On to Off: BMC creates an SMI via the power button in the PIIX4. BIOS will service this SMI and set the state machine in the PIIX4 to the off state. The BMC monitors the state machine and will then turn off the power. As a safety mechanism the PIIX4 will automatically power the system off if BIOS fails to service the SMI from the BMC after 4-5 Sec. During power up of the system the SMI handler to service the power button is not loaded until SMI's are initialized. This occurs roughly around the time the video appears on the monitor or post code 52.

6. BIOS Setup Utility Operation

The ROM-resident Setup utility configures only on board devices. Configuration of added PCI or ISA cards requires the use of the diskette-loadable SSU.
The Setup utility screen is divided into four functional areas:

Keyboard Command Bar	Located at the bottom of the screen. This bar displays the keyboard commands supported by the Setup utility.
Menu Selection Bar	Located at the top of the screen. Displays the various major menu selections available to the user. The Server Setup utility major menus are: Main Menu, Advanced Menu, Security Menu, Server Menu, Boot Menu, and the Exit Menu.
Options Menu	Each Options menu occupies the left and center sections of the screen. Each menu contains a set of features. Selecting certain features within a major Options menu drops you into sub-menus.
Item Specific Help Screen	Located at the right side of the screen is an item-specific Help screen.

6.1 Entering Setup Utility

During POST operation, the user is prompted to enter Setup using the F2 function key as follows:

```
Press <F2> to enter Setup
```

Note that a few seconds might pass before Setup is entered. This is the result of POST completing test and initialization functions that must be completed before Setup can be entered. When Setup is entered, the Main Menu options page is displayed.

6.1.1 Keyboard Command Bar

The bottom portion of the Setup screen provides a list of commands that are used for navigating the Setup Utility. These commands are displayed at all times, for every menu and sub-menu.

Each Setup menu page contains a number of features. Except those used for informative purposes, each feature is associated with a value field. This field contains user-selectable parameters. Depending on the security option chosen and in effect via password, a menu feature's value can be changeable or not. If a value is non-changeable due to insufficient security privilege (or other reasons), the feature's value field is inaccessible. The Keyboard Command Bar supports the following:

F1 Help

Pressing F1 on any menu invokes the general Help window. This window describes the Setup key legend. The up arrow, down arrow, Page Up, Page Down, Home, and End keys scrolls the text in this window.

Enter Execute Command

The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected feature has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.

ESC Exit

The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a

menu, the parent menu is re-entered. When the ESC key is pressed in any sub-menu, the parent menu is re-entered. When the ESC key is pressed in any major menu, the Exit menu page displays.

- **Select Item**

The up arrow is used to select the previous value in a pick list, or the previous feature in a menu item's option list. The selected item must then be activated by pressing the Enter key.

¯ **Select Item**

The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the Enter key.

« **Select Menu**

The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.

- Change Value

The minus key is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.

+ Change Value

The plus key is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list.
F9 Setup Defaults

Pressing F9 causes the following to appear:

```
Setup Confirmation
Load default configuration now?
[Yes]        [No]
```

If "Yes" is selected and the Enter key is pressed, all Setup fields are set to their default values. If "No" is selected and the Enter key is pressed, or if the ESC key is pressed, then you are returned to where you were before F9 was pressed without affecting any existing field values.

F10 Save and Exit

Pressing F10 causes the following message to appear:

```
Setup Confirmation
Save Configuration changes and exit now?
[Yes]         [NO]
```

If "Yes" is selected and the Enter key is pressed, all changes are saved and Setup is exited. If "No" is selected and the Enter key is pressed, or the ESC key is pressed, you are returned to where you were before F10 was pressed without affecting any existing values.

6.1.2 Menu Selection Bar

The Menu Selection Bar is located at the top of the screen, and displays the various major menu selections.

- Main Menu
- Advanced Menu
- Security Menu
- Server Menu
- Boot Menu
- Exit Menu

These and associated sub-menus are described below.

Main Menu Selections

The following tables describe the available functions on the Main Menu, and associated sub-menus. Default values are highlighted.

Table 6-1. Main Menu Selections

Feature	Option	Description
System Time	HH:MM:SS	Set the System Time.
System Date	MM/DD/YYYY	Set the System Date.
Legacy Diskette A: Legacy Diskette B:	Disabled,360KB, 720KB, 1.44 MB, 2.88 MB	Select the floppy diskette type.
Primary IDE Master	N/A	Selects sub-menu.
Primary IDE Slave	N/A	Selects sub-menu.
Secondary IDE Master	N/A	Selects sub-menu.
Secondary IDE Slave	N/A	Selects sub-menu.
Keyboard Features	N/A	Selects sub-menu.
Memory Cache	**Enabled**, Disabled	Enables Pentium II Processor Cache
CPU speed	200,233,250,266 **300,**333,350,366 400,433,450,466 500	Selects processor speed when the processor speed jumper is in program position. Display only field, when the processor speed jumper is in protect position.
Language	**English (US)**, Spanish, Italian, French, German	Selects which language BIOS displays.

Table 6-2. Primary IDE Master and Slave Adapters Sub-Menu Selections

Feature	Option	Description
Type	**Auto** None CDROM User	Auto allows the system to attempt auto-detection of the drive type. None informs the system to ignore this drive. CDROM allows the manual entry of fields described below. User allows the manual entry of all fields described below.
Cylinders	1 to 9999	Number of Cylinders on Drive. This field is only changeable for Type User. This field is informational only, for Type Auto.*
Heads	1 to 16	Number of read/write heads on Drive. This field is only available for Type User. This field is informational only, for Type Auto.*
Sectors	0 to 63	Number of Sectors per Track. This field only available for Type User. This field is informational only, for Type Auto.*

Feature	Option	Description
Maximum Capacity	see description	Computed size of Drive from Cylinders, Heads, and Sectors entered. This field is only available for Type User. This field is informational only, for Type Auto.*
LBA Format		information only
Total Sectors		information only
Maximum Capacity		information only
Multi-Sector Transfer	**Disabled** 2, 4, 8, or 16 Sectors	Determines the number of sectors per block for multiple sector transfers. This field is informational only, for Type Auto.
LBA Mode Control	**Disabled** Enabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors. This field is informational only, for Type Auto.
32 Bit I/O	**Disabled** Enabled	Enabling allows 32 bit IDE data transfers. This field is informational only, for Type Auto.
Transfer Mode	**Standard** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4	Select the method for moving data to/from the drive. This field is informational only, for Type Auto.
Ultra DMA	**Disabled** Enabled	For use with Ultra DMA drives. This field is informational only, for Type Auto.
* These fields appear only for Type Auto if a drive is detected.		

Table 6-3. Keyboard Sub-Menu Selections

Feature	Option	Description
Numlock	Auto On **Off**	Selects the power-on state of Numlock.
Key Click	**Disabled** Enabled	Enables key click.
Keyboard auto-repeat rate	**30/sec** 26.7/sec 21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	Selects key repeat rate.
Keyboard auto-repeat delay	¼ sec **½ sec** ¾ sec 1 sec	Selects delay before key repeat.

Advanced Menu Selections

The following tables describe the menu options and associated sub-menus available on the Advanced Menu.

Table 6-4. Advanced Menu Selections

Feature	Option	Description
Plug & Play OS	**No** Yes	Select 'Yes' if you are booting a Plug and Play capable OS (i.e. Win 95)
Reset Configuration Data	**No** Yes	Select 'Yes' if you want to clear the System Configuration Data during next boot. Automatically resets to 'No' in next boot.
PCI Configuration	N/A	Selects sub-menu.
Integrated Peripherals Configuration	N/A	Selects sub-menu.
Advanced Chipset Configuration	N/A	Selects sub-menu.
Use Multiprocessor Specification	**1.1** 1.4	Selects the version of MP spec to use. Some OS require version 1.1 for compatibility reasons.
Large Disk Access Mode	**DOS** Other	DOS - select 'DOS'. UNIX, Novell Netware, or other OS - select 'Other'.
Delay on option ROM	**Disabled** Enabled	If enabled, the BIOS pauses for 2 seconds after the option ROMs are scanned, and before option ROM screen is cleared.

Table 6-5. PCI Configuration Sub-Menu Selections

Feature	Option	Description
PCI Device, Embedded SCSI	N/A	Selects sub-menu
PCI Device, Slot #1	N/A	Selects sub-menu
PCI Device, Slot #2	N/A	Selects sub-menu
PCI Device, Slot #3	N/A	Selects sub-menu
PCI Device, Slot #4	N/A	Selects sub-menu

Table 6-6. PCI Device, Embedded SCSI Sub-Menu Selections

Feature	Option	Description
Option ROM Scan	**Enabled** Disabled	Enable option ROM scan of the selected device.
Wide SCSI Enable Master	**Enabled**	Enable selected device as a PCI bus master. Always enabled.

Feature	Option	Description
Latency Timer	Default 000h 020h **040h** 060h 080h 0A0h 0C0h 0E0h	Minimum guaranteed time, in units of PCI bus clocks, that a device may be master on a PCI bus.

Table 6-7. PCI Device, Slot #1 - Slot #4 Sub-Menu Selections

Feature	Option	Description
Enable Master	**Enabled** Disabled	Enable selected device as a PCI bus master.
Latency Timer	Default 000h 020h **040h** 060h 080h 0A0h 0C0h 0E0h	Minimum guaranteed time, in units of PCI bus clocks, that a device may be master on a PCI bus.

Table 6-8. Integrated Peripheral Configuration Sub-Menu Selections

Feature	Option	Description
COM 1	Disabled **Enabled** Auto PnP OS	If set to “Auto”, BIOS configures the port. If set to “PnP OS”, OS configures the port.
Base I/O Address	**3F8h** 2F8h 3E8h 2E8h	Selects the base I/O address for COM port A
Interrupt	**4** 3	Selects the IRQ for COM port A
COM 2	Disabled **Enabled** Auto PnP OS	If set to “Auto”, BIOS configures the port. If set to “PnP OS”, OS configures the port.
Base I/O Address	3F8h **2F8h** 3E8h 2E8h	Selects the base I/O address for COM port B
Interrupt	4 **3**	Selects the IRQ for COM port B

Feature	Option	Description
Parallel Port	Disabled **Enabled** Auto PnP OS	If set to “Auto”, BIOS configures the port. If set to “PnP OS”, OS configures the port.
Mode	Output only Bi-Directional EPP **ECP**	Selects Parallel Port Mode
Base I/O Address	**378h** 278h	Selects the base I/O address for LPT port.
Interrupt	5 **7**	Selects the IRQ for LPT port
DMA channel	**1** 3	Selects the DMA for LPT port
Floppy disk controller	Disabled **Enabled**	Enables on board floppy disk controller.

Table 6-9. Advanced Chipset Configuration Sub-Menu Selections

Feature	Option	Description
640-768K Memory Region	640 768	If enabled ISA MASTER and DMA cycles are forwarded to PCI
Delayed Transaction	Enable **Disable**	Enable the delayed transaction mechanism when PIIX4 is target of a PCI transaction.
Passive Release	Enable **Disable**	Enable the Passive Release Mechanism PHOLD# signal when PIIX4 is a PCI Master.

Security Menu Selections

The following options are available on the Security Menu.

Table 6-10. Security Menu Selections

Feature	Option	Description
User Password is	**Clear** Set	Status only; user cannot modify. Once set, it can be disabled by setting to a null string, or clearing via the clear password jumper on board.
Administrator Password is	**Clear** Set	Status only; user cannot modify. Once set, it can be disabled by setting to a null string, or clearing via the clear password jumper on board.
Set User Password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clearing via the clear password jumper on board
Set Administrator Password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clearing via the clear password jumper on board
Password on boot	**Disabled** Enabled	If enabled, and the USER password is set, the system will prompt the user for a password before system boots.

Feature	Option	Description
Diskette Access	User **Admin**	User is prevented from accessing the floppy drive if set to Admin. Administrator is always prevented from accessing the floppy drive.
Fixed disk boot sector	**Normal** Write protect	Will write protect the boot sector of the hard drive to prevent viruses from corrupting the drive under DOS if set to write protect.
Secure Mode Timer	**Disabled** 2 min, 5 min, 10 min, 20 min, 1 hr, 2 hr	Period of keyboard and PS/2 mouse inactivity specified for Secure Mode to activate. A USER password is required for Secure Mode to function. Cannot be enabled unless at least one password is enabled.
Secure Mode Hot Key (Ctrl-Alt-)	[ ] [A, B, ..., Z] [0-9]	Key assigned to invoke the secure mode feature. Cannot be enabled unless the USER password is enabled. Can be disabled by entering a new key followed by a backspace.
Secure Mode Boot	**Disabled** Enabled	System boots in Secure Mode. The USER must enter a password to unlock the system. Cannot be enabled unless at least one password is enabled.
Video Blanking	**Disabled** Enabled	Blank video when Secure mode is activated. A password is required to unlock the system. Cannot be enabled unless at least one password is enabled.
Floppy Write Protect	**Disabled** Enabled	When Secure mode is activated, the floppy drive is write protected. A password is required to re-enable floppy writes. Cannot be enabled unless at least one password is enabled.
Reset and Power Switch Lock	**Disabled** Enabled	When Secure Mode is activated, the Reset and Power switches are locked. A password is required to unlock the system. Cannot be enabled unless at least one password is enabled.
System backup reminder	**Disabled** Daily Weekly Monthly	Before booting the BIOS, the gives the user a reminder to perform system backup if set.
Virus check reminder	**Disabled** Daily Weekly Monthly	Before booting the BIOS, this gives the user a reminder to perform a virus check if set.

Server Menu selections

The following menu and sub-menu options are available on the Server Menu.

Table 6-11. Server Menu Selections

Feature	Option	Description
System Management	N/A	Selects sub-menu.
Console Redirection	N/A	Selects sub-menu.
PCI IRQs to IO-APIC mapping	**Disabled** Enabled	If Enabled, the BIOS describes direct PCI interrupt connections to the I/O APIC in the MP table. Do not enable if OS does not support this feature.
Processor Retest	Yes **No**	Select 'Yes', BIOS will clear historical processor status and retest all processors on next boot.

Table 6-12. System Management Sub-Menu Selections

Feature	Option	Description
System Management Mode	Disabled **Enabled**	If enabled, the Server Management Handler will be loaded.
System Event Logging	**Disabled** Enabled	When enabled, system events will be logged by BIOS and the BMC.
Clear Event Log	**No** Yes	If Yes, the System Event log will be cleared.
SMM Debug Mode	**Disabled** Enabled	If enabled the SMM will output to the video and Port 80
Server Management Info	N/A	Selects sub-menu
Set EMP Password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string. The valid characters are a-z, A-Z, 0-9 .
EMP Escape string	4 byte string	When EMP is used with a modem, BMC will use this string to inform the modem that the next bytes are to be interpreted as command. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default string is "+++".
EMP Hang up string	8 byte string	When EMP is used with a modem, BMC will use this string to terminate a connection. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default is "ATH".
EMP Modem Initialization String	16 byte string	When EMP is used with a modem, BMC will use this strings to configure the modem every time EMP initializes. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default is "AT&F0S0=1S14=0&D".
EMP High modem Initialization String	4 byte string	When EMP is used with a modem, BMC will use this strings to configure the modem every time EMP initializes. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default is "0".
EMP Access Mode	PreBoot Active **Disabled**	Pre-boot : EMP Enable during POWER DOWN or POST. Always Active : EMP always enabled. Disabled : EMP Disabled

Feature	Option	Description
EMP Restricted Mode Access	Enable **Disabled**	Restricted Mode : Power Down, Front Panel NMI , Reset Control via EMP are disabled. Can be selected with Pre-boot, or Always Active mode.
EMP Direct Connect/Modem Mode	**Direct Connect** / Modem Mode	Upon selection USER can connect DIRECTLY to port or using a MODEM.

Table 6-13. Server Management Info Sub-Menu Selections

Feature	Option	Description
Board Part Number	N/A	(DMI) Intel motherboard part no. (pba)
Board Serial Number	N/A	(DMI) Intel motherboard serial no.
System Part Number	N/A	(DMI) Integrated system part no.
System Serial Number	N/A	(DMI) Integrated system serial no.
Chassis Part Number	N/A	(DMI) Chassis part no.
Chassis Serial Number	N/A	(DMI) Chassis serial no.
BMC Revision	N/A	BMC revision ID. Revision of firmware for baseboard micro controller
HSBP Revision	N/A	HSBP revision ID. Revision of firmware on Hot Swap SCSI Backplane. Only shown if a Hot Swap BackPlane microcontroller exists in the system.

Table 6-14. Console Redirection Sub-Menu Selections

Feature	Option	Description
COM Port Address	**Disabled** 3F8 2F8 3E8	When enabled, Console Redirection uses the I/O port specified. Choosing “Disabled” completely disables Console Redirection.
IRQ #	3 or 4	When Console Redirection is enabled, this shows the IRQ assigned per the COM Port Address chosen above.
Baud Rate	9600 **19.2k** 38.4k 115.2k	When Console Redirection is enabled, it will use the baud rate specified.
Console Type	**ANSI** VT100	Enables the specified Console type.
Flow Control	None CTS/RTS XON/XOFF **CTS/RTS + CD**	None = No flow control CTS/RTS = Hardware based flow control XON/XOFF = Software flow control CTS/RTS +CD = Hardware based + Carrier Detect flow control

Boot menu selections

Boot Menu options allow the user to select the boot device. The following table is an example of a list of devices ordered in priority of the boot invocation. Items can be re-prioritized by using the up and down arrow keys to select the device. Once the device is selected, use the plus (+) key to move the device higher in the boot priority list. Use the minus (-) key to move the device lower in the boot priority list.

Table 6-15. Boot Menu Selections

Feature	Option	Description
Floppy Check	**Disabled** Enabled	If Enabled, the system verifies Floppy type on boot. Disable results in a faster boot.
Boot Device Priority	N/A	Selects sub-menu
Hard Drive	N/A	Selects sub-menu
Removable Devices	N/A	Selects sub-menu

Table 6-16. Boot Device Priority Selections

Boot Priority	Device	Description
1.	Removable Devices	Attempt to boot from a removable media device.
2.	Hard Drive	Attempt to boot from a hard drive device.
3.	ATAPI CD-ROM Drive	Attempt to boot from an ATAPI CD-ROM drive.
4.	LANDesk ® Service agent II	Attempt to boot from LANDesk ®.
4.	Diagnostic boot	Attempt to boot from diagnostic boot partition

Table 6-17. Hard Drive Selections

Option	Description
1. Drive #1 (or actual drive string) 2. Other bootable Cards Additional entries for each drive that has a PNP header.	To select the boot drive, use the up and down arrows to highlight a device, then press the plus key (+) to move it to the top of the list (or the minus key (-) to move it down). Other bootable cards cover all the boot devices that are not reported to the system BIOS through BIOS Boot specification mechanism. It may or may not be bootable, and may not correspond to any device. Press ESC to exit this menu.

Table 6-18. Removable Device Menu

Option	Description
1. Device #1 2. Other bootable devices such as Legacy Devices like floppy drives.	To select the device, use the up and down arrows to highlight a device, then press the plus key (+) to move it to the top of the list (or the minus key (-) to move it down). Press ESC to exit this menu. The operating system assigns drive letters to these devices in the order displayed.

Exit menu selections

The following menu options are available on the Server menu. Select an option using the up or down arrow key. Then press Enter to execute the option.

Table 6-19. Exit Menu Selections

Option	Description
Exit Saving Changes	Exit after writing all modified Setup item values to NVRAM
Exit Discarding Changes	Exit leaving NVRAM unmodified
Load Custom Defaults	Load values of all Setup items from previously saved Custom Defaults
Save Custom Defaults	Save present Setup values to Custom Defaults
Load Default Values	Load default values for all Setup items.
Discard Changes	Read previous values of all Setup items from NVRAM
Save Changes	Write all Setup item values to NVRAM

7. Flash Update Utility

The Flash Memory Update utility (IFLASH) loads a fresh copy of the BIOS into Flash ROM. The loaded code and data include the following:

- On board Video BIOS and SCSI BIOS
- BIOS Setup utility
- User-definable Flash area (User Binary Area)
- Diagnostic boot loader binary
- Language file

When running IFLASH in interactive mode, you may choose to update a particular Flash area. Updating a Flash area takes a file or series of files from a hard or floppy disk, and loads it in the specified area of Flash ROM. In interactive mode, IFLASH can display the header information of the selected files.
Note: The utility iFLASH must be run without the presence of a Protected mode control program, such as Windows or EMM386 (Do not run in a DOS window under NT, Win 95 or Memphis. IFLASH uses the processor's flat addressing mode to update the Flash part.
Other platforms have shown interactions between system sensor event logging, and the IFLASH. With the C440GX+, Sensor event logging is not performed via SMI, thus there are no potential interactions to effect/corrupt FLASH.

7.1 Loading the System BIOS

A new BIOS is contained in .BIx files. The number of .BIx files is determined by the size of the BIOS area in the Flash part. For further information on logical area 1 - System BIOS, see Table 1.2. As of this writing, the system BIOS area is 8 files (512KB). They are named as follows:

xxxxxxxx.BIO
xxxxxxxx.BI1
xxxxxxxx.BI2
etc til xxxxxx.BI7

The first 8 letters of each filename on the release diskette can be any value, but cannot be renamed. Each file contains a link to the next file in the sequence. IFLASH does a link check before updating to ensure that the process is successful. However, the first file in the list can be renamed, but all subsequent filenames must remain unchanged. (See Section **Error! Reference source not found.**).

Once an update of the system BIOS is complete, you are prompted for a reboot. Language files are overwritten by updating the system BIOS. If a custom language file has been created, it must be

Flashed in after the system BIOS has been updated. The user binary area and diagnostic loader binary image is also updated during a system BIOS update. User binary can be updated independent of the system BIOS.

7.2 User Binary Area

C440GX+ includes an 16KB area in Flash for implementation-specific OEM add-ons. The User Binary area can be saved and updated exactly as described above in the *System BIOS* section. Only one file is needed. The valid extension for user files is USR.

7.3 Diagnostic Boot Loader Partition

C440GX+ supports 32KB of diagnostic boot loader, which can be saved and updated like the User Binary area, without having to update the rest of the BIOS. The valid extension for the diagnostic boot loader partition is .DBL.

7.4 Language Area

The system BIOS language area can be updated without having to update the entire BIOS. C440GX+ supports English, Spanish, French, German, and Italian (from Intel). These languages are selectable using the CU. When additional language files (*.LNG) are made available, they can be loaded into the system BIOS using IFLASH (in interactive mode, as described above), in the same manner as updating the system BIOS and the user binaries.

7.5 Recovery Mode

In the case of a corrupt .BIx image or an unsuccessful update of the system BIOS, C440GX+ can boot in recovery mode. To place C440GX+ into recovery mode, move the boot option jumper to recovery position. The jumper connects pins 1 and 2 (normal BIOS) by default.

Recovery mode requires at least 8 MB of RAM in the first DIMM socket, and drive A: must be set up to support a 3.5” 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not come up. In recovery mode operation, IFLASH (in non-interactive mode only) automatically updates only the main system BIOS. IFLASH senses that C440GX+ is in recovery mode and automatically attempts to update the system BIOS. It is recommended to turn off FRB by setting the jumper to disable while doing recovery.

Before powering up C440GX+ , obtain a bootable MS DOS diskette that contains a copy of the BIOS release. Boot the system from the A: drive using this diskette, which executes a special AUTOEXEC.BAT file from the BIOS release. The batch file invokes IFLASH, which updates the Flash ROM with the BIOS found on the diskette.

Note: During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. Failure is indicated by a long series of short beeps.

If a failure occurs, it is most likely that one or more of the system BIOS IFLASH files is corrupt or missing. After a successful update, power down the system and move the recovery jumper back to pins 1 and 2. Power up the system and verify that the BIOS version number matches the version of the entire BIOS that you originally attempted to update. CMOS is not cleared when the system BIOS is updated. Configuration information like ESCD is not overwritten during BIOS flash update. Remember that any additional or different languages or User Binaries or diagnostic binaries that were present before updating need to be reloaded to Flash.

8. Error Handling

This chapter defines how errors are handled by system BIOS on the C440GX+ platform. This chapter describes the role of BIOS in error handling and the interaction between the BIOS, platform hardware and server management firmware as far as error handling is concerned. In addition, error logging techniques are described, and beep codes for errors are defined.

8.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors on C440GX+, which can be disabled and enabled individually or as a group, can be categorized as follows:

- ISA bus
- PCI bus
- Memory single and multi-bit errors
- Sensors
- processor internal error, thermal trip error, temperatures and voltages, GTL voltage levels

The BIOS cannot detect errors on the Pentium II processor bus because PAC does not monitor these.

ISA and PCI bus errors can be further classified as 'standard bus' errors, which have a standard register interface across all platforms. All other errors, such as Pentium II processor and ECC errors, are referred to as 'product-specific' errors, which require special consideration depending upon the system configuration. Product-specific errors can be emulated as standard bus errors, if specific routing of certain hardware signals, as documented in this chapter, are followed. This emulation is important to both OS and BIOS NMI handlers, which have no knowledge of product-specific errors, but need to recover and shut down the system gracefully. In C440GX+, sensors are managed by the BMC. The BMC is capable of receiving event messages from individual sensors and log system events. The BIOS programs the BMC not to generate a SMI on sensor events such as fan failure.

8.2 Error Handlers

The BIOS has an NMI handler that gets invoked when an NMI occurs in POST. Generally, the OS traps the NMI and does not pass it onto the BIOS NMI handler. Therefore, the BIOS NMI handler is rarely invoked in real operating environment. The SMI handler cannot be bypassed by the OS, and is used to handle and log system level events that are not visible to the server management firmware.

8.2.1 BIOS NMI handler

To maintain DOS compatibility, the BIOS NMI handler only processes enabled standard bus errors, such as ISA Parity check or IOCHK# errors. It displays an error message, issues a beep signal, and halts. It disables NMI using bit 7 of I/O port 70h (RTC Index Port) on the occurrence of an unknown or spurious NMI. This can cause unusual side effects because it allows a spurious NMI to block a subsequent valid NMI.

8.2.2 OS NMI handler

The OS NMI handler processes standard bus errors at the OS level. When SMI is disabled, hardware must ensure that these errors are routed to NMI. Most OS NMI handler implementations are not product specific and behave in a manner similar to a BIOS NMI handler. It is the responsibility of the BIOS SMI handler to present platform specific errors, such as multi-bit ECC error, as one of the standard bus errors, like parity error, to the OS NMI handler. If the SMI handler is disabled via CU, the OS will not know about platform-specific critical errors.

8.2.3 SMI Handler

If the SMI handler control bit in Setup is disabled, no SMI signals are generated, and no SMI handler is required. If enabled, all system errors are preprocessed by the SMI handler, even those that are normally considered to generate an NMI. The SMI handler sends a command to the BMC to log the event and provides the data to be logged.

8.3 Error Messages and Error Codes

The system BIOS displays error messages on the video screen. Prior to video initialization, beep codes inform you of errors. POST error codes are logged in the event log, as well as the EBDA.

The BIOS displays POST error codes on the video monitor.

Following are definitions of POST error codes, POST beep codes, and system error messages.

8.3.1 POST Codes

The BIOS indicates the current testing phase during POST after the video adapter has been successfully initialized by writing a 2-digit hex code to I/O location 80h. If a Port-80h card (Post card) is installed, it displays this 2-digit code on a pair of hex display LEDs.

Table 8-1. Port-80h Code Definition

Code	Meaning
CP	Phoenix check point (port-80) code

The following table contains the port-80 codes displayed during the boot process. A beep code is a series of individual beeps on the PC speaker, each of equal length. The following table describes the error conditions associated with each beep code and the corresponding POST check point code as seen by a 'port 80h' card (for example, if an error occurs at check point 22h, a beep code of 1-3-1-1 is generated). The "-" means there is a pause between the sequence that delimits the sequence.

Table 8-2. Standard BIOS Port-80 Codes in Execution Sequence During POST

CP	Beeps	Reason
02		Verify Real Mode
12		Restore processor control word during warm boot (only occurs on warm reboot)
24		Set ES segment register to 4GB
04		Get processor type
06		Initialize system hardware
18		8254 timer initialization
08		Initialize PCI set registers with initial POST values
C4		Initialize system flags in CMOS
11		Load alternate registers with initial POST values
0E		Initialize I/O
0C		Initialize caches to initial POST values
16	1-2-2-3	BIOS ROM checksum
17		turn cache off
28		Autosize DRAM
2A		Clear 512K base RAM
2C	1-3-4-1	RAM failure on address line xxxx*
2E	1-3-4-3	RAM failure on data bits xxxx* of low byte of memory bus (1st 4 meg)

CP	Beeps	Reason
2F		Initialize L2 cache if enabled in CMOS
38		Shadow system BIOS ROM
20	1-3-1-1	Test DRAM refresh
29		Post Memory Manager Initialization (PMM)
33		Post Dispatch manager Initialization
34		Test CMOS
C1		Post error manager Intialization
09		Set in POST flag
0A		Initialize processor registers and CPU microcode
3A		Autosize cache
0B		Enable processor cache
0F		Initialize the local bus IDE (not used anymore but here for phx std)
10		Initialize Power Management (APM not used in C440GX+)
14		Initialize keyboard controller
1A		8237 DMA controller initialization
1C		Reset Programmable Interrupt Controller
22	1-3-1-3	Test 8742 Keyboard Controller
32		read processor bus-clock frequency and compute boot processor speed
67		Initialize and register other CPU via SMM through apic bus
69		Initialize SMI handler for all processors
00		wait for secondary processor to execute init SMI handler
F4		exit SMI handler (secondary processor executed halt in SMI)
3C		Configure advanced PCI set registers and reset coprocessor
3D		Load alternate registers with CMOS values
42		Initialize interrupt vectors
46	2-1-2-3	Check ROM copyright notice
45		Initialize all pre-pnp devices
49		Initialize PCI bus and devices (also read escd and allocate resources)
48		Check video configuration against CMOS (vga or mda)
4A		Initialize all video adapters in system
4C		Shadow video BIOS ROM
24		put CPU in big real mode (flat mode memory addressing - up to 4 Gb)
59		Post display manager initialization (video screen error codes now visible)
22		reset and test keyboard first try (only warm reset)
52		reset and test keyboard controller (both warm and cold reset)
54		Set key click if enabled
76		Enable keyboard
58	2-2-3-1	Test for unexpected interrupts
4B		Quietboot start (not used in *C440GX+*)
4E		Display copyright notice
50		Display CPU(s) type and speed
51		EISA Init (Not used in C440GX+)
5A		Display prompt “Press F2 to enter SETUP”
5B		Disable CPU L1 cache for memory test
5C		Test RAM between 512 and 640k
60		Test extended memory (4Mb to top of memory)
62		Test extended memory address lines
64		Jump to UserPatch1
66		Configure advanced cache registers
68		Enable external and processor caches
6A		Display external cache size

CP	Beeps	Reason
6C		Display shadow message
6E		Display non-disposable segments
70		Display error messages to video
72		Check for configuration errors
74		Test real-time clock
7C		Set up hardware interrupt vectors
7E		Test coprocessor if present
80		not used
88		Initialize BIOS Data Area , timeouts for detecting parallel, serial and hdd controller clear CMOS shutdown flag
8A		Initialize Extended BIOS Data Area
81		late post core initialization of devices
87		configure mcd devices
85		Initialize and detect PC-compatible PnP ISA devices (serial, parallel etc)
82		not used
84		clear interrupts from com port detection
86		console redirection initialized
83		configure onboard hard disk controller
89		Enable NMI
8C		Initialize floppy controller
90		Initialize and detect hard disks
8B		Detect and test for Mouse or Auxiliary device on keyboard controller
95		Install CD-ROM for boot
92		Jump to UserPatch2
C5		Initialize GPNV areas of DMI
98	1-2	Search for option ROMs. One long, two short beeps on checksum failure of an option ROM
93		Scan for User flash ROMs MP table initialization (wake up secondary processor and halt it)
9C		Set up Power Management (not used)
9D		enable security
9E		Enable hardware interrupts
A0		Set time of day
A2		Check key lock
A4		Initialize typematic rate
C2		Initialize DMI tables
C3		Log post errors with Post error manager and to SEL in BMC also update VID bits and memory presence to BMC display and FRB errors (watchdog timeouts, bist or CPU failures)
A8		Erase F2 prompt
AA		Scan for F2 key stroke
AC		Initialize EMP port if selected. Remove com2 from BDA if EMP is enabled. Enter SETUP
AE		Clear in-POST flag
B0		Turn on secure boot if enabled(secure front panel, blank video, floppy write protect) Check for errors
B2		POST done – prepare to boot Operating System
B4	1	One short beep before boot
B5		Display Quietboot (not used)
BE		Clear screen
B6		Check password (optional)
BC		Clear parity checkers

CP	Beeps	Reason
BA		not used
B7		ACPI configuration (table configuration in memory and BDA)
BD		Display multiboot menu if esc is hit
BF		Display system config summary(if enabled in CMOS)
8F		get total # of hard drives and put in BDA
91		Program IDE hard drives (timing, pio modes etc)
9F		save Total # of hard drives (scsi and ATA) in BDA
97		Fixup MP table (checksum)
99		check smart harddrive
C7		Prepare to boot to OS, clean up graphics and pmm areas.
C0		Try to boot with INT 19 return to video mode 3 disable pmm return to real mode disable gate A20 clears system memory reset stack Invokes Int19
		Error handling Post codes (may occur at anytime during post)
DO		Interrupt handler error
D2		Unknown interrupt error
D4		Pending interrupt error
D6		Initialize option ROM error
D8		Shutdown error
DA		Extended Block Move
DC		Shutdown 10 error

8.3.2 POST Error Codes and Messages

The following table defines POST error codes and associated messages. The BIOS will prompt the user to press a key in case of serious errors. Some of the error messages are preceded by the string ‘Error” to highlight the fact that these indicate a possibly malfunctioning systems.

Table 8-3. POST Error Messages and Codes

Code	Error message	Pause on Error
0162	BIOS unable to apply BIOS update to processor 1	Yes
0163	BIOS unable to apply BIOS update to processor 2	Yes
0164	BIOS does not support current stepping for processor 1	Yes
0165	BIOS does not support current stepping for processor 2	Yes
0200	Failure Fixed Disk	No
0210	Stuck Key	No
0211	Keyboard error	No
0212	Keyboard Controller Failed	Yes
0213	Keyboard locked - Unlock key switch	Yes
0220	Monitor type does not match CMOS - Run SETUP	No
0230	System RAM Failed at offset:	No
0231	Shadow Ram Failed at offset:	No
0232	Extended RAM Failed at offset:	No
0250	System battery is dead - Replace and run SETUP	Yes
0251	System CMOS checksum bad - Default configuration used	Yes
0260	System timer error	No

Code	Error message	Pause on Error
0270	Real time clock error	No
0297	ECC Memory error in base (extended) memory test in Bank xx	Yes
02B2	Incorrect Drive A type - run SETUP	No
02B3	Incorrect Drive B type - run SETUP	No
02D0	System cache error - Cache disabled	No
02F5	DMA Test Failed	Yes
02F6	Software NMI Failed	No
0401	Invalid System Configuration Data - run configuration utility	No
None	System Configuration Data Read Error	No
0403	Resource Conflict	No
0404	Resource Conflict	No
0405	Expansion ROM not initialized	No
0406	Warning: IRQ not configured	No
0504	Resource Conflict	Error
0505	Expansion ROM not initialized	No
0506	Warning: IRQ not configured	No
0601	Device configuration changed	No
0602	Configuration error - device disabled	No
8100	processor 0 failed BIST	Yes
8101	processor 1 failed BIST	Yes
8104	processor 0 Internal Error (IERR) failure	Yes
8105	processor 1 Internal Error (IERR) failure	Yes
8106	processor 0 Thermal Trip failure	Yes
8107	processor 1 Thermal Trip failure	Yes
8108	Watchdog Timer failed on last boot, BSP switched.	Yes
810A	processor 1 failed initialization on last boot.	Yes
810B	processor 0 failed initialization on last boot.	Yes
810C	processor 0 disabled, system in Uni-processor mode	Yes
810D	processor 1 disabled, system in Uni-processor mode	Yes
810E	processor 0 failed FRB Level 3 timer	Yes
810F	processor 1 failed FRB Level 3 timer	Yes
8110	Server Management Interface failed to function	Yes
8120	IOP sub-system is not functional	Yes
8150	NVRAM Cleared by Jumper	Yes
8151	NVRAM Checksum Error, NVRAM cleared	Yes
8152	NVRAM Data Invalid, NVRAM cleared	Yes