CN430TX Motherboard
Technical Product Specification

August, 1997

Order Number 677606-001

The CN430TX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the CN430TX Motherboard Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the CN430TX Technical Product Specification.	August, 1997

This product specification applies only to standard CN430TX motherboards with BIOS identifier 4C3NT0X0.86A.

Changes to this specification will be published in the CN430TX Motherboard Specification Update before being incorporated into a revision of this document.

Contents

5 Specifications and Customer Support

Figures

Tables

1 Motherboard Description

1.1 Overview

The CN430TX motherboard supports Pentium® processors, Pentium OverDrive® processors, and Pentium processors with MMX™ technology. Features of the motherboard include the following:

- NLX form factor
- Socket 7 Pentium processor socket

Main Memory

- Two 168-pin DIMM sockets
- Support for up to 256 MB DRAM

Second Level Cache Memory

- 256 KB or 512 KB Pipeline Burst SRAM (PBSRAM) soldered to the motherboard

Chipset and PCI/IDE Interface

- Intel 82430TX PCIset
- Integrated PCI bus mastering controller

I/O Features

- National Semiconductor PC87307 SuperI/O controller
- Integrates the following I/O functions: floppy drive interface, one multimode parallel port, two FIFO serial ports, real-time clock, keyboard and mouse controller
- Support for two Universal Serial Bus (USB) interfaces

Expansion Slots

- Riser connector supports up to three PCI slots and up to two ISA slots

Audio Subsystem

- Yamaha OPL3-SA3 audio codec

Graphics Subsystem

- S3† ViRGE/GX† graphics controller

Other Features

- Plug and Play compatible
- Support for Advanced Power Management (APM)
- Support for Advanced Configuration and Power Interface (ACPI)
- Hardware monitor ASIC

Software drivers and utilities are available from Intel.

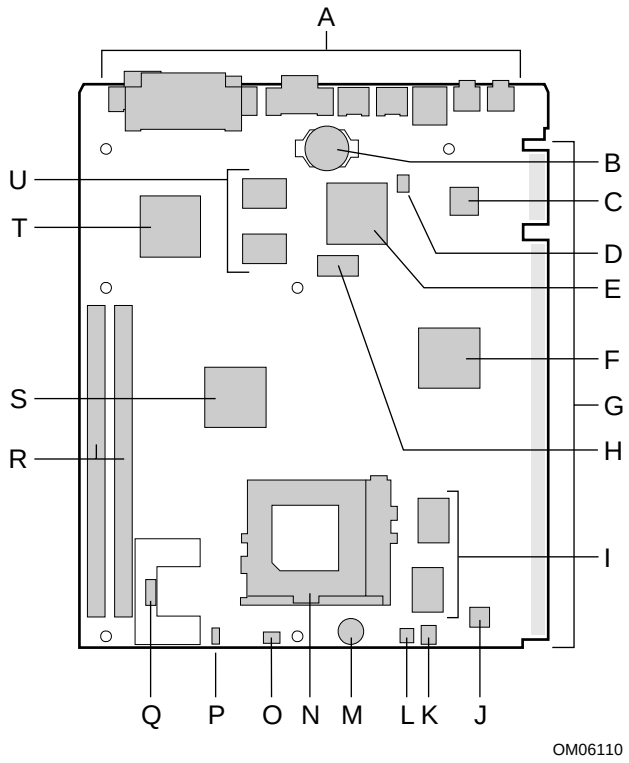


Figure 1. Motherboard Components

A	Back panel I/O connectors	L	Chassis security connector
B	Battery	M	Speaker
C	Yamaha OPL3-SA3 audio codec	N	Socket 7 Pentium processor socket
D	Bus frequency / BIOS recovery jumper	O	Clock multiplier jumper
E	National 87307 I/O controller	P	Voltage regulator jumper
F	430TX PCI ISA IDE Xcelerator (PIIX4)	Q	Voltage regulator
G	NLX Riser connector	R	DIMM connectors
H	2 Mbit Flash BIOS	S	430TX System Controller (MTXC)
I	256 or 512 KB L2 PBSRAM cache	T	S3 ViRGE/GX graphics controller
J	Hardware monitor ASIC	U	SGRAM video memory
K	Fan connector		

1.2 Motherboard Manufacturing Options

Motherboard manufacturing includes the following option - 256 or 512 KB PBSRAM second-level cache (L2) soldered onto the motherboard.

1.3 Form Factor

The motherboard is designed to fit into an NLX form factor chassis. Figure 2 illustrates the mechanical form factor for the motherboard. Location of the I/O connectors, riser slot, and mounting holes is in compliance with the NLX specification (see Section 5.2).

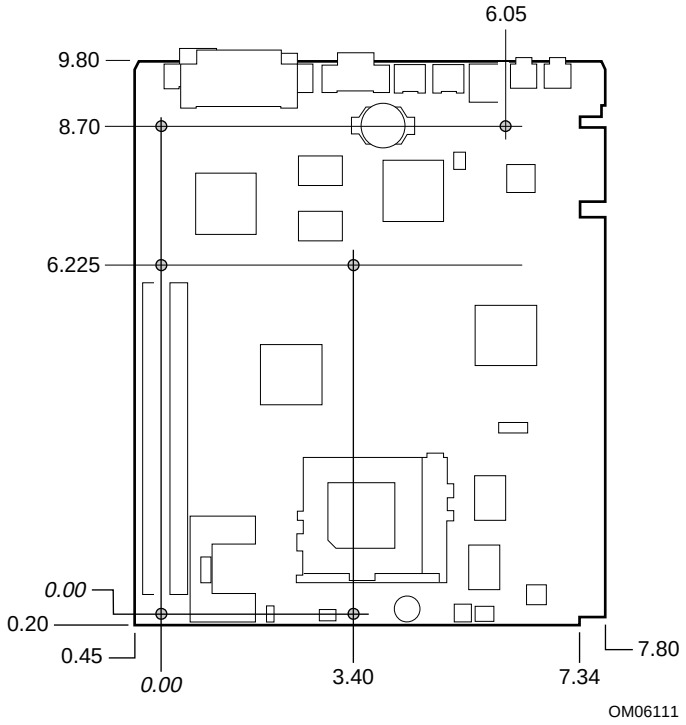


Figure 2. Motherboard Dimensions

Figure 3 specifies the dimensions of the heatsink keep out zone.

NOTE

Processor heatsinks used with this motherboard may interfere with add-in cards in the lower NLX riser card slot. This is a deviation from the NLX specification keepout zone C. The actual encroachment is 1.870 inches wide and 0.613 inches deep as shown in Figure 3. The total height of the processor socket, the microprocessor, and the heatsink must be no higher than 0.8 inches above the motherboard plane in order to avoid interference in this zone.

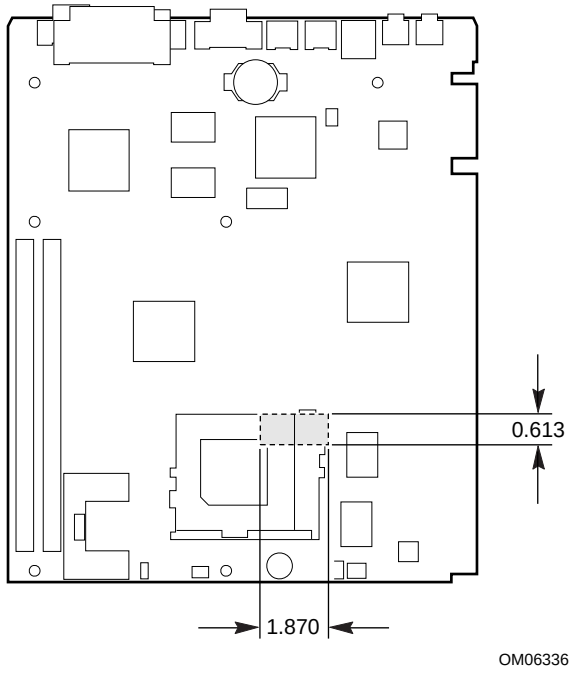


Figure 3. Heatsink Keep Out Zone Dimensions

1.4 I/O Shield

The back panel I/O shield for the motherboard must meet specific dimensional and material requirements. Computers built with this motherboard need the I/O shield to pass EMI certification testing. Figure 4 shows the critical dimensions for the I/O shield and indicates the position of each cutout. For more chassis design requirements, see the NLX specification.

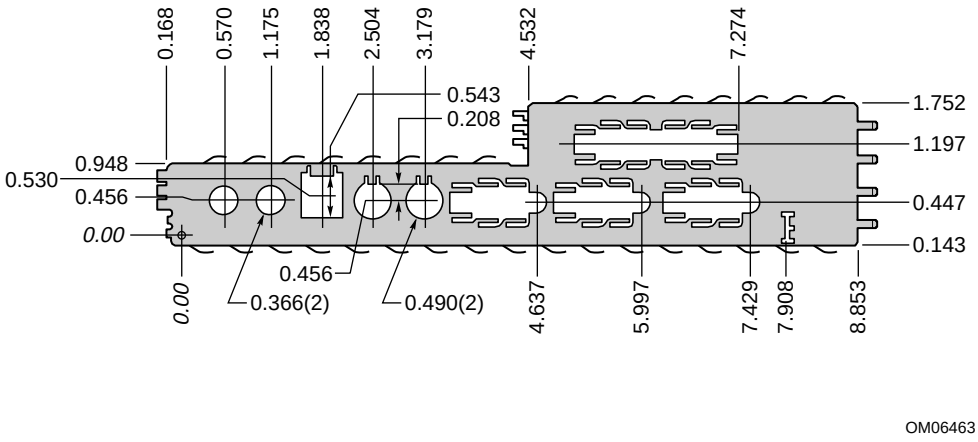


Figure 4. Back Panel I/O Shield Dimensions

1.5 Microprocessor

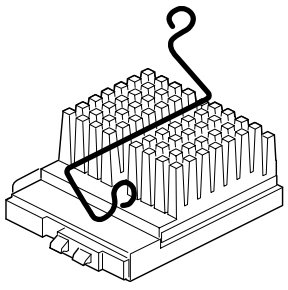
The motherboard supports the following:

- Pentium processors with MMX technology operating at 166, 200, and 233 MHz.
- Pentium processors operating at 90, 100, 120, 133, 150, 166, and 200 MHz.

An onboard voltage regulator derives the necessary voltage from the computer's power supply. For Pentium processors, a jumper enables the use of VR-, or VRE-specified processors. For Pentium processors with MMX technology, the required voltage is automatically detected by onboard circuitry. There are no separate or additional jumpering requirements for Pentium processors with MMX technology.

⚠ CAUTION

If you use clips to secure a heat sink to the processor, do not use bail-wire style heat sink clips. These clips have been known to damage the motherboard when installed or removed incorrectly. The figure to the right shows an example of the bail-wire style heat sink clip.



OM05554

1.5.1 Microprocessor Upgrade

The motherboard has a 321-pin Socket 7 zero insertion force (ZIF) microprocessor socket. Socket 7 supports upgrades to higher performance Pentium OverDrive processors.

1.6 Memory

1.6.1 Main Memory

The motherboard has two Dual Inline Memory Module (DIMM) sockets. Memory can be installed in one or two sockets. The minimum memory size is 8 MB, and the maximum is 256 MB. The BIOS automatically detects memory type, size, and speed so no jumper settings are required.

The motherboard supports the following:

- 168-pin 3.3 V DIMMs with gold-plated contacts
- 60 and 66 MHz bus speeds
- 60 ns 3.3 V unbuffered EDO memory
- 60 ns CAS Latency 2 unbuffered 4-clock 3.3 V SDRAM
- Caching for the first 64 MB of main memory
- 64-bit data path
- Single- or double-sided DIMMs in the following sizes:

DIMM Size	Type	Configuration	Technology
8 MB	60 ns EDO	1M x 64	16 Mbit
16 MB	60 ns EDO	2M x 64	16 Mbit
32 MB	60 ns EDO	4M x 64	16 Mbit
64 MB	60 ns EDO	8M x 64	16 Mbit
128 MB	60 ns EDO	16M x 64	64 Mbit
8 MB	CAS Latency 2 SDRAM	1M x 64	16 Mbit
16 MB	CAS Latency 2 SDRAM	2M x 64	16 Mbit
32 MB	CAS Latency 2 SDRAM	4M x 64	16 Mbit
64 MB	CAS Latency 2 SDRAM	8M x 64	64 Mbit
128 MB	CAS Latency 2 SDRAM	16M x 64	64 Mbit

Memory type, size, and speed can vary between sockets so EDO and SDRAM memory can be installed on the same motherboard. Parity (x 72) DIMMs are not recommended because the motherboard does not provide parity checking or ECC functionality.

1.6.1.1 EDO DRAM

EDO DRAM improves memory read performance by holding the memory data valid until the next CAS# falling edge. With EDO DRAM, the CAS# precharge overlaps the data-valid time, which allows CAS# to negate earlier while still satisfying the memory data-valid window. EDO DIMMs must meet the Intel EDO DRAM DIMM v1.2 Specification.

NOTE

Due to loading anomalies, using SDRAM DIMMs with a n x 4 DRAM base are not supported. For example, a DIMM that uses sixteen 16 Mbit x 4 devices should not be used.

1.6.1.2 SDRAM

Synchronous DRAM (SDRAM) improves memory performance. Unlike EDO memory, SDRAM is synchronous with the memory clock. This simplifies the timing design and increases memory speed because all timing is dependent on the number of memory clock cycles. To function correctly, SDRAM DIMMs must meet the Intel 4-clock 66 MHz 64-bit unbuffered SDRAM DIMM v1.0 Specification.

NOTE

Due to loading anomalies, using SDRAM DIMMs with a n x 4 DRAM base are not supported. For example, a DIMM that uses sixteen 16 Mbit x 4 devices should not be used.

NOTE

The board supports unbuffered, 4-clock 3.3 V SDRAM DIMMs only. Buffered, 5 V, or 2-clock SDRAM DIMMs cannot be used.

1.6.2 Second-level Cache

The 512 KB direct-mapped write-back L2 cache consists of two 64 Kbit x 32 global write enable (GWE) Pipeline PBSRAM devices soldered to the motherboard. A 32 Kbit x 8 external Tag SRAM provides caching support for up to 64 MB of main memory.

The 256KB L2 cache substitutes two 32 Kbit x 32 PBSRAMs and an 8 Kbit x 8 external Tag SRAM.

1.7 Chipset

The Intel 82430TX PCIset consists of the TX System Controller (MTXC) device and the PCI ISA IDE Xcelerator (PIIX4) device.

1.7.1 430TX System Controller (MTXC)

The MTXC integrates the cache and main memory DRAM control functions and provides bus control to handle transfers between the processor, cache, main memory, and the PCI bus. The MTXC allows PCI masters to achieve full PCI bandwidth by using the snoop ahead feature. For increased system performance the MTXC integrates posted write and read prefetch buffers. The MTXC features include:

- Microprocessor interface control
- Integrated L2 write-back cache controller
  - — Supports pipeline burst SRAM
  - — 64 MB maximum DRAM cacheability
  - — Direct mapped organization—write back only
  - — Cache hit read/write cycle timings at 3-1-1-1
  - — Back to back read/write cycles at 3-1-1-1-1-1-1-1
- Integrated DRAM controller
  - — 8 MB to 256 MB main memory
  - — 64-Mbit DRAM/SDRAM technology support
  - — 3.3 V EDO and unbuffered synchronous DRAM support
  - — Non-parity (x64) support only
- Fully synchronous minimum latency PCI bus interface
  - — PCI compliance (see Section 5.2 for compliance level)
  - — 30 and 33 MHz bus speeds
  - — PCI to DRAM data throughput or greater than 100 MB/sec
  - — Up to four PCI masters in addition to the PIIX4
- Power management control
  - — Provides PCI CLKRUN# signal to control memory clock on the PCI bus (on/off)
  - — Internal clock control (gated off if no host or PCI bus activity)

1.7.2 430TX PCI ISA IDE Xcelerator (PIIX4)

The Intel 430TX PCI ISA IDE Xcelerator (PIIX4) is a multifunction PCI device implementing a PCI to ISA bridge, PCI IDE functionality, a Universal Serial Bus (USB) host/hub function, and Enhanced Power Management. The PIIX4 features include:

- Multifunction PCI to ISA bridge
  - — Supports the PCI bus at 30 and 33 MHz
  - — PCI compliant (see Section 5.2 for compliance level)
  - — Full ISA or extended I/O (EIO) bus support

- USB controller
  - Two USB ports (see Section 5.2 for compliance level)
  - Supports legacy keyboard and mouse
  - Supports UHCI design guide revision 1.1 interface
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 14 MB/sec
  - Supports "Ultra DMA/33" synchronous DMA mode transfers up to 33 MB/sec
  - Integrated 8 x 32-bit buffer for bus master PCI IDE burst transfers
  - Bus master mode
- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Supports PCI DMA with three PC/PCI channels and distributed DMA protocols
  - Fast type-F DMA for reduced PCI bus usage
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
  - Supports thermal alarm
  - Support for Wake On Modem through Ring Indicate input
  - Support for Wake on LAN† through LID input
- Real-Time Clock
  - 256 byte battery-backed CMOS SRAM
  - Includes date alarm
- 16-bit counters/timers based on 82C54

1.7.3 Universal Serial Bus (USB) Support

The motherboard features two USB ports. The ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports. The motherboard fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible. Features of the USB include:

- Self-identifying, hot pluggable peripherals
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error handling and fault recovery mechanisms built into protocol

NOTE

Computers that have an unshielded cable attached to the USB port might not meet FCC Class B requirements, even if no device or a low speed USB device is attached to the cable. Use shielded cable that meets the requirements for full speed devices.

NOTE

Advanced Power Management will not function as expected when a USB keyboard or mouse is used. USB activity is not monitored by the APM event counter, therefore, activity from a USB keyboard or mouse will not keep the system awake or bring a system out of APM sleep mode. If a USB keyboard or mouse is being used, APM should be disabled.

1.7.4 IDE Support

The motherboard has two independent bus mastering PCI IDE interfaces that support PIO Mode 3, PIO Mode 4, ATA-33 (Ultra DMA-33), and ATAPI (e.g., CD-ROM) devices. The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. IDE device transfer rate and translation mode are automatically detected by the BIOS.

Normally, programmed I/O operations require a substantial amount of processor bandwidth; however, in multi-tasking operating systems like Windows† 95, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

1.7.4.1 LS-120 Support

LS-120 MB Diskette technology enables users to store 120 MB of data on a single, 3.5-inch removable diskette. LS-120 technology is backward (both read and write) compatible with 1.44 MB and 720 KB DOS-formatted diskettes and is supported by Windows 95 and Windows NT† operating systems.

The motherboard allows connection of an LS-120 compatible drive and a standard 3.5-inch diskette drive. The LS-120 drive can be configured as a boot device, if selected in the BIOS setup utility.

NOTE

If you connect an LS-120 drive to an IDE connector and configure it as the "A" drive and configure a standard 3.5-inch floppy as a "B" drive, the standard floppy must be connected to the floppy drive cable's "A" connector (the connector at the end of the cable).

1.8 Super I/O Controller

The PC87307VUL Super I/O Controller from National Semiconductor is an ISA Plug and Play compatible (see Section 5.2 for compliance level), multifunction I/O device that provides the following features:

- Serial ports:
  - — Two 16450/16550A-software compatible UARTs
  - — Send/receive 16-byte FIFO
  - — Four 8-bit DMA options for the UART with Slow Infrared Support (USI)
  - — Ring indicator support for both serial ports
- Multimode bi-directional parallel port
  - — Standard mode, IBM and Centronics compatible
  - — Enhanced Parallel Port (EPP) mode with BIOS and driver support
  - — High-speed Extended Capabilities Port (ECP) mode
- Floppy disk controller
  - — DP8473 and N82077 compatible
  - — 16 byte FIFO
  - — PS/2† diagnostic register support
  - — CMOS disk input and output logic
  - — High performance digital data separator (DDS)
  - — PC-AT† and PS/2 drive mode support
- Keyboard and mouse controller
  - — Industry standard 8042A compatible
  - — General purpose microcontroller
  - — 8 bit internal data bus
- Support for an IrDA† and Consumer IR-compliant infrared interface

By default, the I/O controller interfaces are automatically configured during boot up. The I/O controller can also be manually configured in the Setup program.

1.8.1 Serial Ports

The 16450/16550A compatible UART's support data transfers at speeds up to 115.2 Kbaud with BIOS serial port support. The ports are implemented with two 9-pin D-Sub serial port connectors located on the back panel.

1.8.2 Parallel Port

The motherboard supports one multimode bi-directional parallel port. The port is implemented with a one 25-pin D-Sub connector located on the back panel. In the Setup program, there are four options for parallel port operation:

- Compatible (standard mode)
- Bi-directional (PS/2 compatible)
- Bi-directional Enhanced Parallel Port (EPP)
- Bi-directional Extended Capabilities Port (ECP)

1.8.3 Floppy Controller

The I/O controller is software compatible with the DP8473 and N82077 floppy drive controllers and supports both PC-AT and PS/2 modes. The floppy interface can be configured for the following floppy drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

1.8.4 Keyboard and Mouse Interface

NOTE

The mouse and keyboard can be plugged into either of the PS/2 connectors.

The keyboard controller contains keyboard and mouse controller code from American Megatrends Incorporated (AMI). The code provides the traditional keyboard and mouse control functions, including Power On/Reset password protection. A password can be specified in the Setup program.

The keyboard controller also supports a three-key (<Ctrl><Alt><Del> software reset function. The key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power-on Self Test (POST).

1.9 Graphics Subsystem

The onboard graphics subsystem uses the S3 ViRGE/GX graphics controller, with the following features:

- 3-D graphics capability
- SGRAM-based chip optimized for synchronous operation
- 64-bit graphics engine with accelerator core
- 170 MHz 24-bit RAMDAC/clock synthesizer
- Dual programmable clock generators
- DCI-based linear addressing scheme
- S3 Streams Processor provides high video playback quality

1.9.1 Memory Type and Size

The controller is supported by 2 MB of SGRAM soldered to the motherboard.

1.9.2 Resolutions and Refresh Rates

Table 1. S3 ViRGE/GX Resolutions and Refresh Rates

	Refresh Rate (Hz) At:			
Resolution	**4-bit Color (16 Colors)**	**8-bit Color (256 Colors)**	**15/16-bit Color (32K/64K Colors)**	**24-bit Color (16M Colors)**
640 x 480	60	60, 70, 72, 75, 85	60, 72, 75, 85	60, 72, 75, 85
800 x 600	56, 60, 72, 75, 85	56, 60, 72, 75, 85	56, 60, 72, 75, 85	56, 60, 72, 75, 85
1024 x 768	43(IL), 60, 70, 75, 85	43(IL), 60 ,70, 75, 85	43(IL), 60, 70, 75, 85	not supported
1152 x 864	not supported	60	not supported	not supported
1280 x 1024	43(IL), 60, 75, 80	43(IL), 60, 75, 85	not supported	not supported
1600 x 1200	not supported	48.5(IL), 60	not supported	not supported

IL = Interlaced

1.9.3 Graphics Drivers and Utilities

Graphics drivers and common graphics utilities are available for Windows 3.x, Windows 95, and Windows NT. Drivers and utilities are available from Intel's World Wide Web site (see Section 5.1).

1.10 Audio Subsystem

The onboard audio subsystem features the Yamaha OPL3-SA3 audio codec. The chip integrates a 16-bit audio codec, OPL3 FM synthesis and its DAC, 3-D enhanced stereo controller, and an interface for MPU-401 and a joystick. The chip provides all the digital audio and analog mixing functions needed for recording and playing sound. Features of the chip include the following:

- Integrated 3-D enhanced stereo controller including all required analog components
- Stereo analog-to-digital and digital-to-analog converters
- Analog mixing, anti-aliasing, and reconstruction filters
- Support for 16-bit address decode
- ADPCM, A-law, or µlaw digital audio compression/decompression
- Full digital control of all mixer and volume control functions
- Plug and Play compatibility
- Sound Blaster† and Windows Sound System compatibility

The following table shows the IRQ, DMA channel, and base I/O address options for the audio subsystem. These options are automatically chosen by the Plug and Play interface, so there are no default settings.

Resource	IRQ (Options)	DMA Channel (Options)	I/O Address (Options)
Sound Blaster (DMA playback, DMA shared with Windows Sound System capture)	5 7 9 10 11	0 1 3	220h 240h 220-280h
Windows Sound System (DMA playback)	5 7 9 10 11	0 1 3	530h E80h 530-F48h
MPU-401 (IRQ shared with Sound Blaster)			330h 300h 300-334h
MIDI / Game Port			201h 201-211h
AdLib†			388h 388-3F8h

Note: The MIDI/Game Port feature is not implemented.

1.10.1 Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site (see Section 5.1).

1.10.2 Audio Connectors

The motherboard has Mic In and Line Out connectors on the back panel.

1.11 Hardware Monitor

The hardware monitor component (National Semiconductor LM78) provides low-cost instrumentation capabilities designed to reduce the total cost of owning a PC when used with LANDesk® Client Manager. The hardware implementation is a single-chip ASIC. Features include:

- An integrated ambient temperature sensor
- Fan speed sensors
- Power supply voltage monitoring to detect levels above or below acceptable values
- Registers for storing POST hardware test results and error codes
- Remote reset capabilities from a remote peer or server through LANDesk Client Manager, Version 3.0 and service layers (when available)

When suggested ratings for temperature, fan speed, or voltage are exceeded, an interrupt is activated. The hardware monitor component (LM78) connects to the ISA bus as an 8-bit I/O mapped device.

1.12 Motherboard Connectors

Figure 5 shows the connectors on the motherboard.

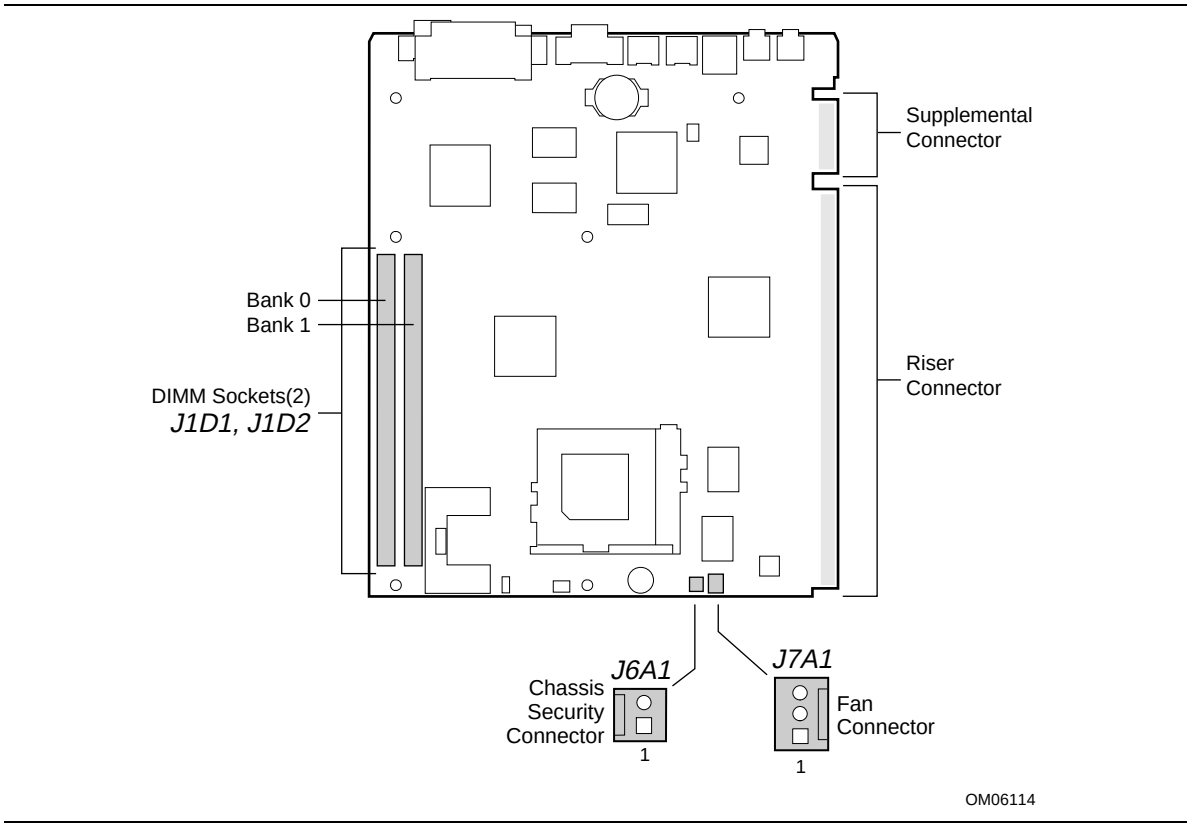


Figure 5. Motherboard Connectors

1.12.1 Chassis Security Connector

A 1 x 2-pin connector that supports an intrusion switch (or alarm) on the chassis.

Table 2. Chassis Security Connector (J6A1)

Pin	Signal Name
1	Ground
2	CHS_SEC

1.12.2 Fan Connector

A 1 x 3-pin fan connector can support a processor or chassis fan. Pin 3 on the connector can be used to implement a sensor that monitors fan operation.

Table 3. Processor Fan Connector (J7A1)

Pin	Signal Name
1	Ground
2	+12 V
3	Fan_sense (tachometer)

1.12.3 NLX Card Edge Connectors

The NLX motherboard connects to the riser with a 340 pin (2x170) pin, 1mm pitch, card edge connector. The pin-out for the riser interconnect is shown below. The "A" side is the bottom (secondary) side of the motherboard, and the "B" side is the top (primary) side of the motherboard. Pin 1 is toward the back of the motherboard (back panel I/O connectors). In addition, there is a 26 pin (2x13) supplemental gold finger contact. According to the NLX specification, the riser must provide signals for the following:

- PCI expansion slots
- ISA expansion slots
- IDE headers
- 1 floppy drive header
- Miscellaneous front panel signals

For power requirements, see Section 1.16.

Table 4, Table 5, and Table 6 specify the pinouts located on the primary connector; Table 7 specifies the pinouts located on the supplemental connector. All edge connector pin definitions are defined in the NLX specification, version 1.2.

Table 4. PCI Segment, Riser Interconnect Pin-out

Pin#	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A1	-12V	PWR	NA	NA	B1	PCSPKR_RT	AUDIO	O	NA
A2	REQ4#	PCI	I	RIS	B2	+12V	PWR	NA	NA
A3	+12V	PWR	NA	NA	B3	PCSPKR_LFT	AUDIO	O	NA
A4	GNT4#	PCI	O	RIS	B4	+12V	PWR	NA	NA
A5	3.3VDC	PWR	NA	NA	B5	PCICLK0	PCI	O	MB
A6	PCIINT3#	PCI	I	RIS	B6	GND	PWR	NA	NA
A7	3.3VDC	PWR	NA	NA	B7	PCICLK1	PCI	O	MB
A8	PCIINT0#	PCI	I	RIS	B8	SER_IRQ	MISC	I/O	MB
A9	PCIINT1#	PCI	I	RIS	B9	PCIINT2#	PCI	I	RIS
A10	PCICLK2	PCI	O	MB	B10	3.3VDC	PWR	NA	NA
A11	3.3VDC	PWR	NA	NA	B11	PCICLK3	PCI	O	MB
A12	PCI_RST#	PCI	O	MB	B12	GND	PWR	NA	NA
A13	GNT0#	PCI	O	RIS	B13	GNT3#	PCI	O	RIS
A14	PCICLK4	PCI	O	MB	B14	3.3VDC	PWR	NA	NA
A15	GND	PWR	NA	NA	B15	GNT2#	PCI	O	RIS
A16	GNT1#	PCI	O	RIS	B16	AD[31]	PCI	I/O	RIS
A17	3.3VDC	PWR	NA	NA	B17	REQ0#	PCI	I	RIS
A18	REQ2#	PCI	I	RIS	B18	GND	PWR	NA	NA
A19	REQ3#	PCI	I	RIS	B19	AD[29]	PCI	I/O	RIS
A20	AD[30]	PCI	I/O	RIS	B20	AD[28]	PCI	I/O	RIS
A21	GND	PWR	NA	NA	B21	AD[26]	PCI	I/O	RIS
A22	AD[25]	PCI	I/O	RIS	B22	3.3VDC	PWR	NA	NA
A23	REQ1#	PCI	I	RIS	B23	AD[24]	PCI	I/O	RIS
A24	AD[27]	PCI	I/O	RIS	B24	C/BE[3]#	PCI	I/O	RIS
A25	3.3VDC	PWR	NA	NA	B25	AD[22]	PCI	I/O	RIS
A26	AD[23]	PCI	I/O	RIS	B26	GND	PWR	NA	NA
A27	AD[20]	PCI	I/O	RIS	B27	AD[21]	PCI	I/O	RIS
A28	AD[18]	PCI	I/O	RIS	B28	AD[19]	PCI	I/O	RIS
A29	GND	PWR	NA	NA	B29	AD[16]	PCI	I/O	RIS
A30	AD[17]	PCI	I/O	RIS	B30	3.3VDC	PWR	NA	NA
A31	IRDY#	PCI	I/O	RIS	B31	C/BE[2]#	PCI	I/O	RIS
A32	DEVSEL#	PCI	I/O	RIS	B32	FRAME#	PCI	I/O	RIS
A33	3.3VDC	PWR	NA	NA	B33	TRDY#	PCI	I/O	RIS
A34	STOP#	PCI	I/O	RIS	B34	GND	PWR	NA	NA
A35	PERR#	PCI	I/O	RIS	B35	SDONE	PCI	I/O	RIS
A36	SERR#	PCI	I/O	RIS	B36	LOCK#	PCI	I/O	RIS
A37	GND	PWR	NA	NA	B37	SBO#	PCI	I/O	RIS

continued ☛

Table 4. PCI Segment, Riser Interconnect Pin-out (continued)

Pin#	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A38	C/BE[1]#	PCI	I/O	RIS	B38	3.3VDC	PWR	NA	NA
A39	AD[13]	PCI`	I/O	RIS	B39	AD[15]	PCI	I/O	RIS
A40	AD[10]	PCI	I/O	RIS	B40	PAR	PCI	I/O	RIS
A41	GND	PWR	NA	NA	B41	AD[14]	PCI	I/O	RIS
A42	C/BE[0]#	PCI	I/O	RIS	B42	GND	PWR	NA	NA
A43	AD[00]	PCI	I/O	RIS	B43	AD[11]	PCI	I/O	RIS
A44	AD[06]	PCI	I/O	RIS	B44	AD[12]	PCI	I/O	RIS
A45	3.3VDC	PWR	NA	NA	B45	AD[09]	PCI	I/O	RIS
A46	AD[05]	PCI	I/O	RIS	B46	3.3VDC	PWR	NA	NA
A47	AD[01]	PCI	I/O	RIS	B47	AD[08]	PCI	I/O	RIS
A48	AD[03]	PCI	I/O	RIS	B48	AD[07]	PCI	I/O	RIS
A49	GND	PWR	NA	NA	B49	AD[04]	PCI	I/O	RIS
A50	AD[02]	PCI	I/O	RIS	B50	GND	PWR	NA	NA
A51	5VDC	PWR	NA	NA	B51	PCI_PM#	PCI	I/O	MB

I/O Column Definitions Relative to Motherboard
O = Output from motherboard to riser
I = Input from riser to motherboard
Termination Column Definitions:
MB = Termination/Pullup/Pulldown/debounce is on Motherboard
RIS = Termination/Pullup/Pulldown is on Riser card
N/A = Not on Motherboard or Riser

Table 5. ISA Segment, Riser Interconnect Pin-out

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A52	RSTDRV	ISA	O	MB	B52	5VDC	PWR	NA	NA
A53	IOCHK#	ISA	I	MB	B53	IRQ9	ISA	O	MB
A54	SD[6]	ISA	I/O	MB	B54	DRQ2	ISA	I	MB
A55	SD[7]	ISA	I/O	MB	B55	SD[3]	ISA	I/O	MB
A56	SD[4]	ISA	I/O	MB	B56	0WS#	ISA	I	MB
A57	5VDC	PWR	NA	NA	B57	SD[1]	ISA	I/O	MB
A58	SD[2]	ISA	I/O	MB	B58	AEN	ISA	O	MB
A59	SD[5]	ISA	I/O	MB	B59	IOCHRDY	ISA	I	MB
A60	SD[0]	ISA	I/O	MB	B60	SA[18]	ISA	I/O	MB
A61	SMEMW#	ISA	O	MB	B61	SMEMR#	ISA	O	MB
A62	SA[19]	ISA	I/O	MB	B62	SA[16]	ISA	I/O	MB
A63	IOW#	ISA	I/O	MB	B63	IOR#	ISA	I/O	MB
A64	SA[17]	ISA	I/O	MB	B64	DRQ3	ISA	I	MB
A65	GND	PWR	NA	NA	B65	SA[15]	ISA	I/O	MB
A66	DACK#3	ISA	O	MB	B66	GND	PWR	NA	NA
A67	SA[14]	ISA	I/O	MB	B67	SA[13]	ISA	I/O	MB
A68	DACK1#	ISA	O	MB	B68	5VDC	PWR	NA	NA
A69	DRQ1	ISA	I	MB	B69	REFRESH#	ISA	I/O	MB
A70	SA[12]	ISA	I/O	MB	B70	SA[11]	ISA	I/O	MB
A71	SYSCLK	ISA	O	MB	B71	SA[10]	ISA	I/O	MB
A72	SA[9]	ISA	I/O	MB	B72	IRQ7	ISA	I	MB
A73	5VDC	PWR	NA	NA	B73	IRQ6	ISA	I	MB
A74	IRQ5	ISA	I	MB	B74	SA[8]	ISA	I/O	MB
A75	SA[7]	ISA	I/O	MB	B75	SA[6]	ISA	I/O	MB
A76	IRQ3	ISA	I	MB	B76	DACK2#	ISA	O	MB
A77	IRQ4	ISA	I	MB	B77	SA[4]	ISA	I/O	MB
A78	SA[5]	ISA	I/O	MB	B78	GND	PWR	NA	NA
A79	TC	ISA	O	MB	B79	SA[3]	ISA	I/O	MB
A80	BALE	ISA	O	MB	B80	SA[2]	ISA	I/O	MB
A81	GND	PWR	NA	NA	B81	SA[1]	ISA	I/O	MB
A82	OSC	ISA	O	MB	B82	SA[0]	ISA	I/O	MB
A83	IOCS16#	ISA	I	MB	B83	SBHE#	ISA	I/O	MB
A84	MEMCS16#	ISA	I	MB	B84	LA[23]	ISA	I/O	MB
A85	IRQ11	ISA	I	MB	B85	LA[22]	ISA	I/O	MB
A86	IRQ10	ISA	I	MB	B86	LA[21]	ISA	I/O	MB
A87	IRQ15	ISA	I	MB	B87	LA[20]	ISA	I/O	MB

continued ☛

Table 5. ISA Segment, Riser Interconnect Pin-out (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A88	IRQ12	ISA	I	MB	B88	LA[19]	ISA	I/O	MB
A89	GND	PWR	NA	NA	B89	LA[18]	ISA	I/O	MB
A90	IRQ14	ISA	I	MB	B90	LA[17]	ISA	I/O	MB
A91	DRQ0	ISA	I	MB	B91	DACK0#	ISA	O	MB
A92	MEMR#	ISA	I/O	MB	B92	DACK5#	ISA	O	MB
A93	MEMW#	ISA	I/O	MB	B93	SD[8]	ISA	I/O	MB
A94	SD[9]	ISA	I/O	MB	B94	DACK6#	ISA	O	MB
A95	DRQ5	ISA	I	MB	B95	SD[10]	ISA	I/O	MB
A96	DRQ6	ISA	I	MB	B96	5VDC	PWR	NA	NA
A97	5VDC	PWR	NA	NA	B97	SD[11]	ISA	I/O	MB
A98	SD[12]	ISA	I/O	MB	B98	DRQ7	ISA	I	MB
A99	DACK7#	ISA	O	MB	B99	SD[13]	ISA	I/O	MB
A100	SD[14]	ISA	I/O	MB	B100	SD[15]	ISA	I/O	MB
A101	MASTER#	ISA	I	MB	B101	GND	PWR	NA	NA

I/O Column Definitions Relative to Motherboard
O = Output from motherboard to riser
I = Input from riser to motherboard
Termination Column Definitions:
MB = Termination/Pullup/Pulldown/debounce is on Motherboard
RIS = Termination/Pullup/Pulldown is on Riser card
N/A = Not on Motherboard or Riser

Table 6. IDE, Floppy, and Front Panel Section, Riser Interconnect Pin-out

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A102	IDEA_DD8	IDE	I/O	MB	B102	GND	PWR	NA	NA
A103	IDEA_RESET#	IDE	O	MB	B103	IDEA_DD7	IDE	I/O	MB
A104	IDEA_DD9	IDE	I/O	MB	B104	IDEA_DD6	IDE	I/O	MB
A105	5VDC	PWR	NA	NA	B105	IDEA_DD5	IDE	I/O	MB
A106	IDEA_DD4	IDE	I/O	MB	B106	IDEA_DD11	IDE	I/O	MB
A107	IDEA_DD10	IDE	I/O	MB	B107	IDEA_DD12	IDE	I/O	MB
A108	IDEA_DD3	IDE	I/O	MB	B108	GND	PWR	NA	NA
A109	IDEA_DD13	IDE	I/O	MB	B109	IDEA_DD14	IDE	I/O	MB
A110	IDEA_DD1	IDE	I/O	MB	B110	IDEA_DD2	IDE	I/O	MB
A111	GND	PWR	NA	NA	B111	IDEA_DD0	IDE	I/O	MB
A112	IDEA_DIOW#	IDE	O	MB	B112	IDEA_DD15	IDE	I/O	MB
A113	IDEA_DMARQ	IDE	I	MB	B113	IDEA_DIOR#	IDE	O	MB
A114	IDEA_IORDY	IDE	I	MB	B114	IDEA_CSEL	IDE	O	MB
A115	IDEA_DMACK#	IDE	O	MB	B115	IDEA_INTRQ	IDE	I	MB
A116	RESERVED	RES	NA	NA	B116	5VDC	PWR	NA	NA
A117	IDEA_DA2	IDE	O	MB	B117	IDEA_DA1	IDE	O	MB
A118	IDEA_CS0#	IDE	O	MB	B118	IDEA_DA0	IDE	O	MB
A119	5VDC	PWR	NA	NA	B119	IDEA_CS1#	IDE	O	MB
A120	IDEA_DASP#	IDE	I	RIS	B120	IDEB_DD8	IDE	I/O	MB
A121	IDEB_RESET#	IDE	O	MB	B121	IDEB_DD7	IDE	I/O	MB
A122	IDEB_DD9	IDE	I/O	MB	B122	GND	PWR	NA	NA
A123	IDEB_DD6	IDE	I/O	MB	B123	IDEB_DD10	IDE	I/O	MB
A124	IDEB_DD5	IDE	I/O	MB	B124	5VDC	PWR	NA	NA
A125	IDEB_DD11	IDE	I/O	MB	B125	IDEB_DD4	IDE	I/O	MB
A126	IDEB_DD12	IDE	I/O	MB	B126	IDEB_DD3	IDE	I/O	MB
A127	GND	PWR	NA	NA	B127	IDEB_DD13	IDE	I/O	MB
A128	IDEB_DD2	IDE	I/O	MB	B128	IDEB_DD14	IDE	I/O	MB
A129	IDEB_DD15	IDE	I/O	MB	B129	IDEB_DD1	IDE	I/O	MB
A130	IDEB_DIOW#	IDE	I/O	MB	B130	IDEB_DD0	IDE	I/O	MB
A131	IDEB_DMARQ	IDE	I	MB	B131	IDEB_DIOR#	IDE	O	MB
A132	IDEB_IORDY	IDE	I	MB	B132	IDEB_CSEL	IDE	O	MB
A133	GND	PWR	NA	NA	B133	IDEB_INTRQ	IDE	I	MB
A134	IDEB_DMACK#	IDE	O	MB	B134	IDEB_DA1	IDE	O	MB
A135	RESERVED	RES	NA	NA	B135	IDEB_DA2	IDE	O	MB
A136	IDEB_DA0	IDE	O	MB	B136	IDEB_CS1#	IDE	O	MB
A137	IDEB_CS0#	IDE	O	MB	B137	IDEB_DASP#	IDE	I	RIS
A138	DRV2#	FLOPPY	GND	NA	B138	GND	PWR	NA	NA

continued ☛

Table 6. IDE, Floppy, and Front Panel Section, Riser Interconnect Pin-out (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A139	5VDC	PWR	NA	NA	B139	DRATE0	FLOPPY	O	NA
A140	RESERVED	RES	NA	NA	B140	FDS1#	FLOPPY	O	NA
A141	DENSEL	FLOPPY	O	NA	B141	FDS0#	FLOPPY	O	NA
A142	FDME0#	FLOPPY	O	NA	B142	DIR#	FLOPPY	O	NA
A143	INDX#	FLOPPY	I	RIS	B143	MSEN1	FLOPPY	I	NA
A144	FDME1#	FLOPPY	O	NA	B144	GND	PWR	NA	NA
A145	GND	PWR	NA	NA	B145	WRDATA#	FLOPPY	O	NA
A146	WE#	FLOPPY	O	NA	B146	TRK0#	FLOPPY	I	RIS
A147	STEP#	FLOPPY	O	NA	B147	MSEN0	FLOPPY	I	NA
A148	WP#	FLOPPY	I	RIS	B148	RDDATA#	FLOPPY	I	RIS
A149	HDSEL#	FLOPPY	O	NA	B149	DSKCHG#	FLOPPY	I	RIS
A150	SDA	MISC	I/O	MB	B150	GND	PWR	NA	NA
A151	SCL	MISC	O	MB	B151	IRSL0	MISC	I/O	NA
A152	FAN_TACH1	MISC	I	NA	B152	IRSL1	MISC	I/O	NA
A153	FAN_TACH2	MISC	I	NA	B153	IRSL2	MISC	I/O	NA
A154	FAN_TACH3	MISC	I	NA	B154	IRTX	MISC	I/O	NA
A155	FAN_CTL	MISC	I	NA	B155	IRRX	MISC	I/O	NA
A156	5VDC	PWR	NA	NA	B156	FP_SLEEP	MISC	I	MB
A157	USB1/3_N	MISC	I/O	RIS	B157	FP_RST#	MISC	I	MB
A158	USB1/3_P	MISC	I/O	RIS	B158	GND	PWR	NA	NA
A159	USB1/3_OC#	MISC	I	RIS	B159	PWRLED#	MISC	O	RIS
A160	USB2/4_N	MISC	I/O	RIS	B160	PWOK	PWR	I	NA
A161	USB2/4_P	MISC	I/O	RIS	B161	SOFT_ON/OFF#	PWR	I	MB
A162	USB2/4_OC#	MISC	I	RIS	B162	PS_ON#	PWR	O	NA
A163	GND	PWR	NA	NA	B163	LAN_WAKE	MISC	I	MB
A164	VBAT	MISC	O	RIS	B164	LAN_ACTVY_ LED#	MISC	O	NA
A165	TAMP_DET#	MISC	I	MB	B165	MDM_WAKE#	MISC	I	MB
A166	MSG_WAIT_ LED#	MISC	O	RIS	B166	1394_PWR	PWR	I	NA
A167	1394_GND	PWR	O	NA	B167	RESERVED	RES	NA	NA
A168	RESERVED	RES	NA	NA	B168	RESERVED	RES	NA	NA
A169	5VSB	PWR	I	NA	B169	RESERVED	RES	NA	NA
A170	3.3VSENSE	PWR	O	NA	B170	-5V	PWR	NA	NA

I/O Column Definitions Relative to Motherboard
O = Output from motherboard to riser
I = Input from riser to motherboard
Termination Column Definitions:
MB = Termination/Pullup/Pulldown/debounce is on Motherboard
RIS = Termination/Pullup/Pulldown is on Riser card
N/A = Not on Motherboard or Riser

Table 7. Signals, NLX Riser with Supplemental Connector

Pin	Signal Name	Type	I/O *	Description	Signal Type
X1	CD_IN_LT	AUDIO	I	CDROM line in left.	Analog 1V RMS
X2	AGND	PWR	NA	Low pass filtered ground for audio circuitry on the riser.	NA
X3	MIC_IN	AUDIO	I	Pre-amplified microphone input. Pre-amp circuitry to reside on riser or in microphone.	Analog 1V RMS
X4	LINE_OUT_LT	AUDIO	O	Analog line out left.	Analog 1V RMS
X5	FP_SPKR_EN **	AUDIO	I	This signal indicates if headphones have been plugged into the front panel LINE_OUT jack. The signal is connected to one of the wipers on the audio jack and is HIGH when the headphones are plugged into the front audio jack and LOW when they are not. The signal is pulled high through a pull up on the motherboard (Typically 100K).	TTL
X6	VOL_DN# **	AUDIO	I	Connects to Volume Down switch on front panel, appropriate pull-up resistor on motherboard. The motherboard provides debounce protection and a pull up resistor.	TTL
X7	GND	PWR	NA	Ground	NA
X8	SMI# **	SYS	I	System Management Interrupt that is an input to the motherboard.	open drain
X9	RESERVED	RES	NA	Reserved	NA
X10	RESERVED	RES	NA	Reserved	NA
X11	RESERVED	RES	NA	Reserved	NA
X12	AGND	PWR	NA	Low pass filtered ground for audio circuitry on the riser.	NA
X13	MODEM_MIC	AUDIO	O	Pre-amplified microphone mono output signal from motherboard to telephony device.	Analog 1V RMS
Y1	CD_IN_RT	AUDIO	I	CDROM line in right.	Analog 1V RMS
Y2	CD_IN_GND	PWR	I	Isolated CDROM Ground.	NA
Y3	AVCC	PWR	O	Clean power from the motherboard to audio circuitry on the NLX riser; could be an isolated power source; 1.5 Ampere max. limitation because of the connector / gold finger limitation.	5-9V DC
Y4	LINE_OUT_RT	AUDIO	O	Analog line out right.	Analog 1V RMS

continued ☛

Table 7. Signals, NLX Riser with Supplemental Connector (continued)

Pin	Signal Name	Type	I/O *	Description	Signal Type
Y5	FP_MIC_EN **	AUDIO	I	This signal indicates if a microphone has been plugged into the front panel MIC_IN jack. The signal is connected to a wiper on the MIC_IN jack and is LOW when the microphone is plugged in and HIGH when it is not. The signal is pulled LOW through a pull down on the motherboard (Typically 100K).	TTL
Y6	VOL_UP# **	AUDIO	I	Connects to Volume Up switch on front panel, appropriate pull-up resistor on motherboard. The motherboard provides debounce protection and a pull up resistor.	TTL
Y7	AC_RST# **	AC'97	O	AC'97 master H/W reset.	TTL
Y8	AC_SD_IN **	AC'97	I	Serial, time division, multiplexed, AC'97 input stream to the motherboard from the codec on the riser (output from the codec).	TTL
Y9	GROUND	PWR	NA	Digital (main motherboard) ground plane.	NA
Y10	AC_SD_OUT **	AC'97	O	Serial, time division, multiplexed, AC'97 output from the motherboard to the codec on the riser (input to the codec).	TTL
Y11	AC_SYNC **	AC'97	O	48KHz fixed rate sample sync signal from the motherboard to the codec on the riser.	TTL
Y12	AC_BIT_CLK **	AC'97	I	12.288 MHz serial data clock.	TTL
Y13	MODEM_SPKR	AUDIO	O	Analog mono output signal from telephony device to motherboard.	Analog 1V RMS

* I/O column: relative to motherboard, "O" = output, from motherboard to riser; "I" = input, from riser to motherboard.

** These signals are not supported.

1.12.4 Back Panel Connectors

Figure 6 shows the location of the back panel I/O connectors, which include:

- External audio jacks: Mic In, Line Out
- Two USB connectors
- PS/2-style keyboard and mouse connectors
- Two serial ports
- One parallel port
- VGA† video monitor connector

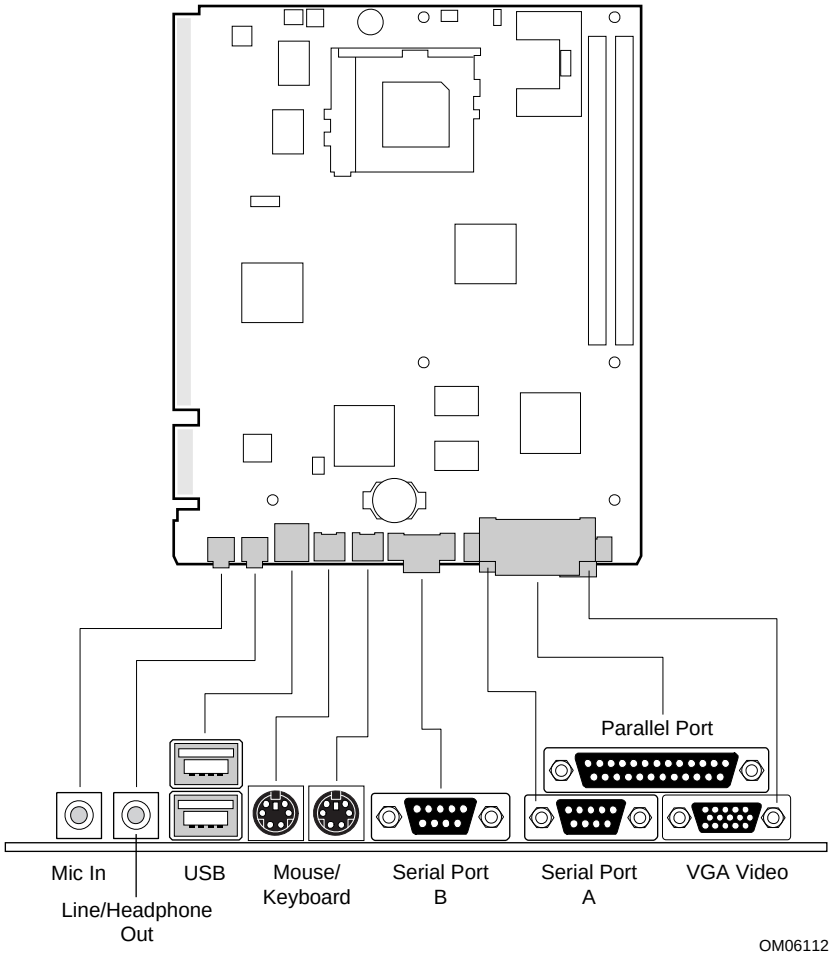


Figure 6. Back Panel I/O Connectors

Table 8. Serial Port Connectors

Pin	Signal Name
1	DCD
2	Serial In #
3	Serial Out #
4	DTR#
5	Ground
6	DSR#
7	RTS#
8	CTS#
9	Ground

Table 9. PS/2 Keyboard / Mouse Connectors

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

Table 10. Parallel Port Connector

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data bit 0	15	Fault#
3	Data bit 1	16	INIT#
4	Data bit 2	17	SLCT IN#
5	Data bit 3	18	Ground
6	Data bit 4	19	Ground
7	Data bit 5	20	Ground
8	Data bit 6	21	Ground
9	Data bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Error	25	Ground
13	Select		

Table 11. VGA Video Monitor Connector

Pin	Signal Name	Pin	Signal Name
1	Red	9	+5 V fused (for DDC2B monitors only)
2	Green	10	Ground
3	Blue	11	No connect
4	No connect	12	DDC Data
5	Ground	13	Horizontal Sync
6	Ground	14	Vertical Sync
7	Ground	15	DDC Clock
8	Ground		

Table 12. Stacked USB Connectors

Pin (Port 0)	Signal Name	Pin (Port 1)	Signal Name
1	Power	5	Power
2	USBP0#	6	USBP1#
3	USBP0	7	USBP1
4	Ground	8	Ground

Table 13. Audio Mic In Connector

Pin	Signal Name
Sleeve	Ground
Tip	Audio Mic In
Ring	Phantom Power

Table 14. Audio Line Out/Headphone Connector

Pin	Signal Name
Sleeve	Ground
Tip	Audio Left Out
Ring	Audio Right Out

1.13 Jumper Settings

Figure 7 shows the location of jumper blocks on the motherboard.

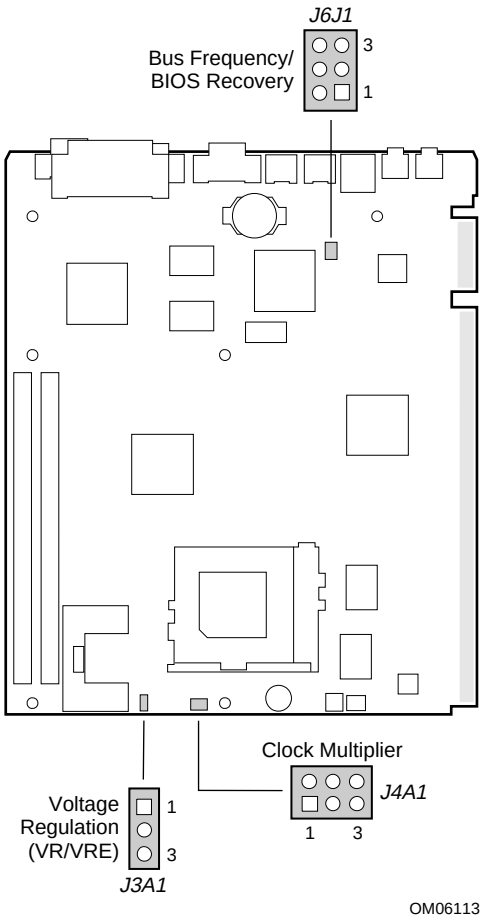


Figure 7. Jumper Block Locations

CAUTION

Do not move any of the jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumpers.

Table 15. Jumper Settings

Function	Jumper	Configuration
BIOS Configuration	J6J1	1-2 Normal operating mode (**Default**) 2-3 Configuration mode Off Recovery mode
Host Bus Frequency*	J6J1	4-5 60 MHz 5-6 66 MHz (**Default**)
Processor Voltage	J3A1	1-2 Standard voltage (**Default**) 2-3 VRE voltage
Clock Multiplier	J4A1	See Table 16

* This jumpers also sets the PCI and ISA bus frequencies

1.13.1 Normal Mode

This mode is for normal computer booting and operations. Connect pins 1 and 2 with a jumper on the configuration jumper block (J6J1) to enable the mode. The BIOS uses the current bus/processor frequency ratio, configuration information, and passwords to boot the computer. Access to the Setup program can be restricted using an administrative or user password.

In normal mode, the BIOS attempts an automatic recovery if the configuration information in flash memory is corrupted.

1.13.2 Configure Mode

This mode is for clearing passwords. Connect pins 2 and 3 with a jumper on the configuration jumper block (J6J1) to enable the mode. In this mode, Setup automatically executes after the POST runs, and no password is required. Setup provides the Maintenance menu with the option for clearing passwords. All other Setup screens are available. Configure mode uses the default BIOS settings for booting, not the current user or administrative settings. When the computer is rebooted, Setup uses the original user and administrative settings with the exception of the options that were changed. For the configuration changes to take effect after exiting the Setup program, power down the computer, set the configuration jumper to normal mode (see Section 1.13.1), and boot the computer.

1.13.3 Recovery Mode

This mode is for upgrading the BIOS or recovering BIOS data. Remove the jumper (no pins connected) from the configuration jumper block (J6J1), Pins 1-3 to enable this mode. After the computer is powered-on, the BIOS attempts to upgrade or recover the BIOS data from a diskette in the floppy drive. Beep codes indicate the recovery status: one beep indicates the start of the recovery, two beeps indicate a successful recovery, and multiple beeps indicate a failed recovery. If a diskette is not in the boot drive, the BIOS attempts to run the POST, does not boot the operating system, and displays a message that the jumper is not properly installed.

For the changes to take effect after a successful recovery, power down the computer, set the jumper to normal mode (see Section 1.13.1), and boot the computer.

NOTE

The LS-120 drive does not work as a legacy floppy drive when attempting to perform a BIOS recovery. A 1.44 MB disk must be used in place of an LS-120 disk in the LS-120 drive for BIOS recovery.

1.13.4 Processor Configuration (J4A1)

The motherboard must be configured for the frequency of the host bus and the frequency of the installed processor. Table 16 shows the jumper settings for each processor frequency and the corresponding host bus, PCI bus, and ISA bus frequencies.

Table 16. Jumper Settings for Processor Frequency

Processor Freq. (MHz)	Jumpers J4A1	Host Bus Freq. (MHz)	PCI Bus Freq. (MHz)	ISA Bus Freq. (MHz)	Clock Multiplier
233	1-2 and 4-5	66	33	8.33	3.5
200	1-2 and 5-6	66	33	8.33	3.0
166	2-3 and 5-6	66	33	8.33	2.5
150	2-3 and 5-6	60	30	7.5	2.5
133	2-3 and 4-5	66	33	8.33	2.0
120	2-3 and 4-5	60	30	7.5	2.0
100	1-2 and 4-5	66	33	8.33	1.5
90	1-2 and 4-5	60	30	7.5	1.5

NOTE:

There are no additional jumpering requirements for Pentium processors with MMX technology.

The 100 MHz Pentium processor and the 233 MHz Pentium processor with MMX technology have identical jumper settings. The motherboard automatically detects which processor type is installed.

1.14 Reliability

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC.

Motherboard MTBF: 153,898.24 hours calculated

1.15 Environmental

The motherboard was designed and manufactured to the following minimum environmental specifications.

Table 17. Motherboard Environmental Specifications

Parameter	Specification		
Temperature			
Nonoperating	-40 °C to +70 °C		
Operating	0 °C to +55 °C (0 °C to +45 °C if an OverDrive processor is installed)		
Shock			
Unpackaged	50 G trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight	**Free Fall (inches)**	**Velocity Change (inches/sec)**
	<20 lbs	36	167
	21-40 lbs	30	152
	41-80 lbs	24	136
	81-100 lbs	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz : 0.02g² Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015g² Hz (flat)		
	40 Hz to 500 Hz : 0.015g² Hz sloping down to 0.00015 g² Hz		

1.16 Power Consumption

Tables 18 and 19 list voltage and current specifications for a computer that contains the motherboard, a 233 MHz Pentium processor with MMX technology, 32 MB SDRAM, 256 KB cache, 3.5-inch floppy drive, 1.6 GB IDE hard drive, and 8X ATAPI CD-ROM. This information is provided only as a guide for calculating **approximate** power usage with additional resources added.

Values for the Windows 95 desktop mode are measured at 1024x768x256 colors and 70 Hz refresh rate. AC watts are measured with a typical 145 W supply, nominal input voltage and frequency, with true RMS wattmeter at the AC line input.

Table 18. DC Voltage

DC Voltage	Acceptable Tolerance
+3.3 V	± 5%
+5 V	± 5%
+5 V SB (standby)	± 5%
-5 V	± 5%
+12 V	± 5%
-12 V	± 5%

Table 19. Power Usage

Mode	AC (watts)	DC (amps) at:			
		+3.3 V	+5 V	+12 V	-12 V
DOS prompt, APM disabled	55.0 W	950 mA	4.68 A	890 mA	40 mA
Windows 95 desktop, APM disabled	55.3 W	890 mA	4.76 A	920 mA	40 mA
Windows 95 desktop, APM enabled, in System Management Mode (SIMM†)	24.2 W	570 mA	1.45 A	140 mA	40 mA

1.16.1 Power Supply Considerations

For typical configurations, the motherboard is designed to operate with at least a 145 W NLX power supply (see Section 5.2 for the NLX Power Supply Recommendations). A higher-wattage power supply should be used for heavily-loaded configurations. The power supply must comply with the following recommendations found in the indicated sections of that specification:

- The potential relation between +3.3V DC and +5V DC power rails (Section 4.5)
- The current capability of the +5V SB line (Section 4.1.2)
- All timing parameters (Section 4.5)
- All voltage tolerances (Section 4.5)

1.17 Regulatory Compliance

This printed circuit board assembly complies with the following safety and EMI regulations when correctly installed in a compatible host system.

Table 20. Safety Regulations

Regulation	Title
UL 1950 - CSA 950-95, 3rd edition, Dated 07-28-95	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA & Canada)
CSA C22.2 No. 950-95 3rd Edition	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (Canada)
EN 60 950, 2nd Edition, 1992 (with Amendments 1, 2 & 3)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2 & 3)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark & Finland)

Table 21. EMI Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 & 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
EN 55 022, 1995	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN 50 082-1 (1992)	Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
VCCI Class 2 (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
ICES-003, Issue 2	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

1.17.1 Product Certification Markings

This printed circuit board assembly has the following product certification markings:

- European CE Marking: Consists of a marking on the board and shipping container.
- UL Recognition Mark: Consists of the UL File No. E139761 on the component side of the board and the PB No. on the solder side of the board. Board material flammability is 94V-1 or -0.
- Canadian Compliance: Consists of small c followed by a stylized backward UR on component side of the board.

2 Motherboard Resources

NOTE

For more detailed information about the resources used for onboard audio, see the Audio Subsystem section in Chapter 1.

2.1 Memory Map

Table 22. Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 262144 K	100000 - 10000000	255 MB	Extended Memory
960 K - 1024 K	F0000 - FFFFF	64 K	System BIOS
944 K - 960 K	EC000 - EFFFF	16 K	Reserved for BIOS
936 K - 944 K	EA000 - EBFFF	8 K	ESCD (Plug and Play configuration and DMI)
932 K - 936 K	E9000 - E9FFF	4 K	Reserved for BIOS
928 K - 932 K	E8000 - E8FFF	4 K	OEM Logo or Scan User Flash
912 K - 928 K	E4000 - E7FFF	16 K	Reserved for BIOS (Available as UMB)
896 K - 912 K	E0000 - E3FFF	16 K	USB Buffer Area
800 K- 896 K	C8000 - DFFFF	96 K	Available High DOS memory (open to ISA and PCI bus)
640 K - 800 K	A0000 - C7FFF	160 K	Video memory and BIOS
638 K - 640 K	9F800 - 9FFFF	2 K	Extended BIOS data (movable by memory manager software)
512 K - 638 K	80000 - 9F7FF	126 K	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 K	Conventional memory

2.2 DMA Channels

Table 23. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio / Parallel Port
2	8- or 16-bits	Floppy Drive
3	8- or 16-bits	Parallel Port (for ECP or EPP) / Audio
4		Reserved - Cascade Channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.3 I/O Map

Table 24. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX4 - DMA 1
0020 - 0021	2 bytes	PIIX4 - Interrupt Controller 1
002E - 002F	2 bytes	Super I/O Controller Configuration Registers
0040 - 0043	4 bytes	PIIX4 - Counter/Timer 1
0048 - 004B	4 bytes	PIIX4 - Counter/Timer 2
0060	1 byte	Keyboard Controller Byte - Reset IRQ
0061	1 byte	PIIX4 - NMI, Speaker Control
0064	1 byte	Keyboard Controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX4 - Enable NMI
0070, bits 6:0	7 bits	PIIX4 - Real Time Clock, Address
0071	1 byte	PIIX4 - Real Time Clock, Data
0078 - 007F	8 bytes	Reserved - Board Configuration
0080 - 008F	16 bytes	PIIX4 - DMA Page Registers
00A0 - 00A1	2 bytes	PIIX4 - Interrupt Controller 2
00B2 - 00B3	2 bytes	APM Control
00C0 - 00DE	31 bytes	PIIX4 - DMA 2
00F0	1 byte	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
0201*	1 byte	Audio / Gameport
0220 - 022F	16 bytes	Audio (Sound Blaster compatible)
0240 - 024F	16 bytes	Audio (Sound Blaster compatible)
0278 - 027F	8 bytes	LPT2
02E8 - 02EF	8 bytes	COM4 / Video (8514A)
02F8 - 02FF	8 bytes	COM2
0290 - 0297	8 bytes	Hardware Monitor
0300 - 0301	2 bytes	MPU-401 (MIDI)
0330 - 0331	2 bytes	MPU-401 (MIDI)
0332 - 0333	2 bytes	MPU-401 (MIDI)
0334 - 0335	2 bytes	MPU-401 (MIDI)
0376	1 byte	Secondary IDE Channel Command Port
0377	1 byte	Floppy Channel 2 Command

continued ☛

Table 24. I/O Map (continued)

Address (hex)	Size	Description
0377, bit 7	1 bit	Floppy Disk Change, Channel 2
0378 - 037F	8 bytes	LPT1
0388 - 038D	6 bytes	AdLib (FM synthesizer)
03B4 - 03B5	2 bytes	Video (VGA)
03BA	1 byte	Video (VGA)
03BC - 03BF	4 bytes	LPT3
03C0 - 03CA	2 bytes	Video (VGA)
03CC	1 byte	Video (VGA)
03CE - 03CF	2 bytes	Video (VGA)
03D4 - 03D5	2 bytes	Video (VGA)
03DA	1 byte	Video (VGA)
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 byte	Primary IDE Channel Command Port
03F7 (Write)	1 byte	Floppy Channel 1 Command
03F7, bit 7	1 bit	Floppy Disk Change Channel 1
03F7, bits 6:0	7 bits	Primary IDE Channel Status Port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0530 - 0537	8 bytes	Windows Sound System
0604 - 060B	8 bytes	Windows Sound System
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + 400h
0CF8 - 0CFB**	4 bytes	PCI Configuration Address Register
0CF9***	1 byte	Turbo and Reset Control Register
0CFC - 0CFF	4 bytes	PCI Configuration Data Register
0E80 - 0E87	8 bytes	Windows Sound System
0F40- 0F47	8 bytes	Windows Sound System
0F86 - 0F87	2 bytes	Yamaha OPL3-SA Configuration
7000 - 700D	14 bytes	SMBus I/O space Registers
8000 - 8037	56 bytes	Power Management I/O space Registers
FF00 - FF07	8 bytes	IDE Bus Master Register
FFA0 - FFAF	16 bytes	Bus Master IDE Registers
Dynamically allocated in PCI I/O space	32 bytes	USB

* Gameport is not implemented on this motherboard

** DWORD access only

*** Byte access only

NOTE

See the Audio section(s) in Chapter 1 for specific I/O addresses that can be used by the audio components on your motherboard. This table does not list I/O addresses that may be used by add-in cards in the system.

2.4 PCI Configuration Space Map

Table 25. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 430TX (MTXC)
00	07	00	Intel 430TX (PIIX4) PCI/ISA bridge
00	07	01	Intel 430TX (PIIX4) IDE Bus Master
00	07	02	Intel 430TX (PIIX4) USB
00	07	03	Intel 430TX (PIIX4) Power Management
00	08	00	S3 ViRGE† Graphics

2.5 Interrupts

Table 26. Interrupts

IRQ	System Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard Buffer Full
2	Reserved, Cascade Interrupt From Slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option) / Audio / User available
6	Floppy Drive
7	LPT1*
8	Real Time Clock
9	User available
10	User available / USB
11	Windows Sound System* / User available
12	Onboard Mouse Port (if present, else user available)
13	Reserved, Math Coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

NOTE: PCI devices, including USB, will be assigned interrupts dynamically.

2.6 PCI Interrupt Routing Map

The PCI specification enables devices attached to the PCI bus to share interrupts. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. However, to achieve the maximum performance of a device, a dedicated IRQ can be specified in Setup to prevent interrupt sharing.

This section describes how the interrupt sharing mechanism works and how the interrupt signals are connected to the PCI expansion slots on an NLX riser card and installed PCI devices. This information can be used to specify the interrupt scheme for PCI add-in cards.

PCI devices are categorized by interrupt groupings as follows:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4 PCI-to-ISA bridge has four Programmable Interrupt Request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 27 lists the PIRQ signals and shows how the signals are connected to onboard PCI interrupt sources and how the signals could be connected to an NLX riser card

Table 27. PCI Interrupt Routing Map

PIIX4 PIRQ Signal	First PCI Expansion Slot	Second PCI Expansion Slot	Third PCI Expansion Slot	Onboard Video	USB
PIRQA	INTA	INTD	INTC		
PIRQB	INTB	INTA	INTD		
PIRQC	INTC	INTB	INTA		
PIRQD	INTD	INTC	INTB	X	X

In this example, the onboard video and USB PCI interrupt sources connect to PIRQD. An add-in card with one interrupt is installed in the first PCI slot. The interrupt source for this card is assigned to group INTA. An add-in card with two interrupts is installed in the second PCI slot. The first interrupt source for this card is assigned to group INTA, and the second to INTB. For the card in slot 1, the INTA interrupt source is connected to signal PIRQA. For the card in slot 2, the INTA interrupt source is connected to signal PIRQB, and the INTB interrupt source is connected to signal PIRQC. With no other cards installed, each interrupt source is connected to a different PIRQ signal. Typically, the cards will not share an interrupt.

NOTE

The PIIX4 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 11, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3 Overview of BIOS Features

3.1 Introduction

The motherboard uses a Phoenix BIOS, which is stored in Flash memory and can be upgraded using a floppy disk-based program. Flash memory also contains the Setup program, Power-on Self Tests (POST), Advanced Power Management (APM), the PCI auto-configuration utility, Windows 95-ready Plug and Play, and support for the S0, S1, and S5 states of the Advanced Configuration and Power Interface (ACPI). See Section 5.2 for the supported versions of these specifications.

This motherboard supports BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a revision code. The initial production BIOS on the motherboard is identified as 4C3NT0X0.86A.

3.1.1 BIOS Flash Memory Organization

The Intel 2-Mbit flash component is organized as 256 KB x 8 bits and is divided into areas as described in Table 28. The table shows the addresses in the ROM image in normal mode (the addresses change in BIOS Recovery Mode).

Table 28. Flash Memory Organization

Address (Hex)	Size	Description
FFFFC000 - FFFFFFFF	16 KB	Boot Block
FFFFA000 - FFFFBFFF	8 KB	Vital Product Data (VPD) Extended System Configuration Data (ESCD) (DMI configuration data / Plug and Play data)
FFFF9000 - FFFF9FFF	4 KB	Used by BIOS (e.g., for Event Logging)
FFFF8000 - FFFF8FFF	4 KB	OEM logo or Scan Flash Area
FFFC0000 - FFFF7FFF	224 KB	Main BIOS Block

3.1.2 BIOS Upgrades

The BIOS can be upgraded from a diskette using the IFLASH.EXE utility that is available from Intel. This utility does BIOS upgrades as follows:

- Updates the flash BIOS from a file on a disk
- Updates the language section of the BIOS
- Makes sure that the upgrade BIOS matches the target system to prevent accidentally installing a BIOS for a different type of system.

BIOS upgrades and the IFLASH.EXE utility are available from Intel through the Intel World Wide Web site. See Section 5.1 for information about this site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

3.1.3 Plug and Play: PCI Auto-configuration

The BIOS automatically configures PCI devices and Plug and Play devices. PCI devices may be onboard or add-in cards. Plug and Play devices are ISA add-in cards built to meet the Plug and Play specification. Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system. When a user turns on the system after adding a PCI or Plug and Play card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in the extended system configuration data (ESCD) format.

For information about the versions of PCI and Plug and Play supported by this BIOS, see Section 5.2. Copies of the specifications can be obtained from the Intel World Wide Web site (see Section 5.1).

3.1.4 PCI IDE Support

If you select “Auto” in Setup, the BIOS automatically sets up the two local bus IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives and tape drives (see Section 5.2 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in Setup. The ATAPI Specification recommends that ATAPI devices be configured as shown in Table 29.

Table 29. Recommendations for Configuring an ATAPI Device

	Primary Cable		Secondary Cable	
	Drive 0	Drive 1	Drive 0	Drive 1
Normal, no ATAPI	ATA			
Disk and CD-ROM for enhanced IDE systems	ATA		ATAPI	
Legacy IDE system with only one cable	ATA	ATAPI		
Enhanced IDE with CD-ROM and a tape or two CD-ROMs	ATA		ATAPI	ATAPI

3.1.5 ISA Plug and Play

If the board is configured to boot with a PnP OS (see Section 5.2), the BIOS automatically configures only those ISA Plug and Play cards and motherboard configurable devices that are required for booting (initial program load devices). If the board isn't configured to boot with a PnP OS, the BIOS automatically configures all Plug and Play ISA cards and motherboard configurable devices.

3.1.6 ISA Legacy Devices

The BIOS can't automatically configure resources for ISA legacy cards, but the resources for these cards can be configured in Setup or with an ISA configuration utility (see Section 5.1 for a Web site address).

The ISA card configuration information is stored in ESCD format. The ESCD data can be cleared using the Reset Configuration Data option in the Advanced Menu. See Section 3.2.4 for more information.

3.1.7 Desktop Management Interface

The Desktop Management Interface (DMI) is designed to make information about the motherboard more easily and readily available to the service personnel who are installing and maintaining computers in an organization.

The main component of DMI is the Management Information Format (MIF) database, which stores information about the computer and its components. With DMI, a system administrator can determine the system's type, capabilities, operational status, installation date, and information about other computer components. This information is located in a series of data structures that can be accessed by the DMI service layer and made available to application programs like LANDesk Client Manager. Component instrumentation gives the service layer access to information stored in the general-purpose area of nonvolatile RAM. The MIF database defines the data and provides access to the information.

The BIOS stores and can report the following types of DMI information:

- BIOS data, such as the BIOS revision level
- Fixed information about the computer, such as motherboard data, peripherals, serial numbers and asset tags
- Information that is displayed at bootup, such as memory size, cache size, and processor speed
- Dynamic information, such as event detection and error logging

A utility can be used to program DMI information into flash memory, so the BIOS also can report the DMI information. Once this information is programmed, it is read-only.

Intel can provide a utility for making DMI calls to the BIOS. The latest DMI specification is available from Intel (see Section 5.1) and other sites.

DMI does not work directly under operating systems that are not Plug and Play (e.g., Windows NT). However, the BIOS supports a DMI table interface that enables a DMI service-level application to access the DMI BIOS information.

3.1.8 Advanced Power Management

The BIOS supports Advanced Power Management (APM); see Section 5.2 for the version supported. You can initiate the energy saving Standby mode in these ways:

- Optional front panel Sleep/Resume button
- Prolonged inactivity; the timeout period is adjustable in the Setup program

When in Standby mode, the motherboard reduces power consumption by using the processor's System Management Mode (SMM) capabilities and by spinning down hard drives and reducing power to or turning off VESA DPMS-compliant monitors. In Setup you can select the DPMS mode to use for the monitor: Standby, Suspend, Sleep, or Disabled.

While in Standby mode, the computer retains the ability to respond to external interrupts; it can service requests such as incoming faxes or network messages while unattended. Any keyboard or mouse activity brings the computer out of Standby mode and immediately restores power to the monitor.

APM is enabled in the BIOS by default; however, the computer must be configured with an OS-dependent APM driver for the power-saving features to take effect. For example, Windows 95 enables APM automatically upon detecting the presence of the APM BIOS.

NOTE

Advanced Power Management will not function as expected when a USB keyboard or mouse is used. USB activity is not monitored by the APM event counter, therefore, activity from a USB keyboard or mouse will not keep the system awake or bring a system out of APM sleep mode. If a USB keyboard or mouse is being used, APM should be disabled.

3.1.9 Advanced Configuration and Power Interface (ACPI)

The BIOS supports ACPI; see Section 5.2 for the version supported. ACPI is an interface for configuring the motherboard and managing the power subsystem from the computer's operating system. ACPI requires an operating system that supports the ACPI features and interface. The ACPI features include:

- Sleep mode provides below 30 W power
- ACPI front-panel power button for sleep mode and power
  - — Pressing the button for one or two seconds puts the computer in sleep mode
  - — Pressing the button for four seconds turns the computer off
- Soft-off feature allows computer to be powered off by the operating system
- Green-enabled ATAPI devices can be automatically powered down

- Devices that support power-down modes can be put in suspension mode
- At least 10 mA standby current maintained for the CMOS RAM and real-time clock
- Fan control for computer cooling and quiet operation
- Wake-up events supported including: USB events, real-time clock alarm, Wake on LAN, and wake-on-ring
- Last power state is saved if AC power is lost while the computer is powered up

3.1.9.1 ACPI 1.0 System States and Power States

The following table is a description of supported ACPI 1.0 power states:

Table 30. Supported ACPI-1.0 Power States

Global states	Sleep states	CPU states	Device states	Targeted system power
G0/S0 - working state	N/A	C0 - working	D0 - working state	Full power > 60 W
G1 - sleeping state	S1 - CPU stopped	C1-stop grant	D1, D2, D3- device specification specific	5 W< power <30W
G2/S5	S5 - soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic	5 W < power *
G3 - mechanical off. The power supply cord is unplugged from the system.	No power to the system	No power	D3 - no power. No power for wake up logic, except when provided by battery or ext. source.	No power to the system so that service can be performed.

* - assumes limited number of wake up devices.

3.1.9.2 ACPI 1.0 Wake up Events

The ability for the system to wake up is described in the following table. Please note that sleeping states S4 and S5 are the same (no power to CPU) for the wake up events.

Table 31. ACPI 1.0 Wake up Events

Wake up Event	From State
Power button	S1, S4, S5
RTC alarm	S1, S4, S5
LAN	S1, S4
Modem	S1*, S4
Thermal event	S1, S4
USB	S1
Keyboard	S1
Mouse	S1

NOTE: The S4 state shown here may be implemented by an operating system, but is not a BIOS feature.

* If Caller ID support is required, wake up on modem is only applicable from the S1 state.

3.1.10 Language Support

The BIOS Setup program and help messages can be supported in 32 languages. Two languages are available at this time: American English and German. The BIOS includes extensions that support the Kanji character set and other character sets that are not ASCII based. Translations of other languages may become available at a later date.

The default language is American English, which is always present unless another language is programmed into the BIOS using the IFlash Memory Utility Program. See Section 5.1 for information about downloading the IFlash Memory Utility Program and other utilities.

3.1.11 Boot Options

Booting from CD-ROM is supported in adherence to the "El Torito" bootable CD-ROM format specification developed by Phoenix Technologies and IBM. Under the Boot Screen field in Setup, CD-ROM is one of four possible boot devices, which are defined in priority order. If you select CD-ROM as the boot device, it must be the first device.

The default settings are:

- First boot device - Removable devices (floppy drive)
- Second boot device - Hard drive
- Third boot device - CD-ROM
- Fourth boot device - Network
- Fifth boot device - LANDesk Service Agent (LSA)

NOTE

Intel's LSA code is included in the BIOS flash memory area. If an Intel EtherExpress™ Pro/100b Ethernet† add-in card is installed in a PCI slot (on a compatible NLX riser card), the motherboard will boot to an Intel LANDesk Configuration Manager server without a separate boot ROM.

NOTE

A copy of the "El Torito" specification is available on the Phoenix Technologies Web site http://www.ptltd.com/techs/specs.html.

3.1.12 OEM Logo or Scan Area

The motherboard supports a 4 KB programmable flash memory user area. You can use this area to display a custom OEM logo during POST, or can insert a binary image that executes at certain times during the POST. A utility is available from Intel's world wide web site to assist with installing a logo into flash memory for display during POST. See Section 5.1.

3.1.13 USB Support

The USB connectors on the motherboard allow you to attach any of several USB devices as they become available. Typically, the device driver for USB devices will be managed by the OS. However, because keyboard and mouse support may be needed in the Setup program before the OS boots, the BIOS supports USB keyboards and mice. You can disable this support in the BIOS if necessary.

NOTE

USB keyboards and mice will work even if the operating system does not support USB devices.

3.1.14 Security Screen

This section describes the options that can be set to restrict access to the Setup program and to restrict who can boot the computer.

A supervisor password and a user password can be set for the Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the Setup program. This is supervisor mode.
- The user password gives restricted access to view and change Setup options in the Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 32 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 32. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options *	Can change all options *	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

* If no password is set, any user can change all Setup options.

3.1.15 Recovering BIOS Data

Some types of failure can destroy the BIOS data. For example, the data could be lost if a power outage occurs while your are updating the BIOS in flash memory. You can recover the BIOS data from a diskette by changing the setting of the BIOS Recovery jumper at location J6J1.

To create a BIOS recovery diskette, you must make a bootable DOS diskette and place the recovery files on it. The recovery files are available from Intel's world wide web site. See Section 5.1.

To recover the BIOS, turn off the computer and remove the BIOS configuration jumper. Insert the bootable BIOS recovery diskette in drive A:. Boot the computer to recover the BIOS. Two beeps and the end of floppy access to drive A: indicate a successful BIOS recovery. After a successful recovery, turn off the computer by holding down the power button for at least four seconds. Then return the jumper to the original pins to restore normal operation. A series of continuous beeps indicates that the recovery operation failed.

NOTE

No video is displayed during the recovery process.

NOTE

The LS-120 drive does not work as a legacy floppy drive when attempting to perform a BIOS recovery. A 1.44 MB disk must be used in place of an LS-120 disk in the LS-120 drive for BIOS recovery.

3.2 BIOS Setup Program

The Setup program is for viewing and changing the BIOS settings for a computer. Setup is accessed by pressing the <F2> key after the Power-On Self Test (POST) memory test begins and before the operating system boot begins.

Table 33 shows the menus available from the menu bar at the top of the Setup screen.

Table 33. Setup Menu Bar

Setup Menu Screen	Description
Maintenance	Clears the Setup passwords. This is only available in configure mode. Refer to Section 1.13.2 for information about configure mode.
Main	Allocates resources for hardware components.
Advanced	Specifies advanced features available through the chipset.
Security	Specifies passwords and security features.
Power	Specifies power management features.
Boot	Specifies boot options and power supply controls.
Exit	Saves or discards changes to the Setup program options.

Table 34 shows the function keys available for menu screens.

Table 34. Setup Function Keys

Setup Key	Description
<F1> or <Alt-H>	Brings up a help screen for the current item.
<Esc>	Exits the menu.
<←> or <→>	Selects a different menu screen.
<↑> or <↓>	Moves cursor up or down.
<Home> or <End>	Moves cursor to top or bottom of the window.
<PgUp> or <PgDn>	Moves cursor to top or bottom of the window.
<F5> or <->	Selects the previous value for a field.
<F6> or <+> or <Space>	Selects the next value for a field.
<F9>	Load the default configuration values for the current menu.
<F10>	Save the current values and exit Setup.
<Enter>	Executes command or selects the submenu.

3.2.1 Maintenance Menu

This menu is for setting the processor speed and clearing the Setup passwords. Setup only displays this menu in configure mode. See Section 1.13.2 for information about setting configure mode.

Table 35. Maintenance Menu

Feature	Options	Description
Clear All Passwords	No options	Clears the user and supervisor passwords.

The Setup program lets you modify the configuration for most basic changes without opening the computer. Setup is accessible only during the Power-on Self Test (POST). To enter Setup, press the <F2> key after the POST memory test has begun and before boot begins.

3.2.2 Overview of the Setup Menu Screens

Table 36 lists the screens displayed by the Setup program. Setup initially displays the Main menu screen. In each screen there are options for modifying the computer's configuration. Select a menu screen by pressing the left <←> or right <→> arrow keys. Use the up <↑> or down <↓> arrow keys to select items in a screen. Use the <Enter> key to select a sub-menu. After you have selected an item, use the <+> and <–> keys to modify the setting.

Table 36. Overview of the Setup Menu Screens

Setup Menu	**Use this menu to...**
Maintenance	Clear the Setup passwords.
Main	Configure basic features of the computer, such as time, date, diskette drives, and hard drives.
Advanced	Configure advanced features of the computer, such as peripheral configuration and advanced chipset configuration.
Security	Set passwords.
Power	Configure Power Management options.
Boot	Configure how the computer boots up.
Exit	Save or discard changes.
Setup Submenu	**Use this submenu to...**
Floppy Options	Configure the diskette drive interfaces.
Primary IDE Master	Configure the primary master IDE drive.
Primary IDE Slave	Configure the primary slave IDE drive.
Secondary IDE Master	Configure the secondary master IDE drive.
Secondary IDE Slave	Configure the secondary slave IDE drive.
Resource Configuration	Reserve memory blocks and specific IRQs.
Peripheral Configuration	Configure peripherals.
Keyboard Configuration	Configure keyboard functions.
Video Configuration	Configure onboard video resources.
DMI Event Logging	View and modify desktop management interface (DMI) event logs.
Hard Drive	Select hard disk drives.
Removable Devices	Select removable devices.

3.2.3 Main Menu

The following table lists the program items in the Main menu.

Program Item	This program item...
Processor Type	Displays the processor type
Processor Speed	Displays the processor speed
Cache RAM	Displays the size of L2 cache
Total Memory	Displays the total amount of RAM on the motherboard
BIOS Version	Displays the version of the BIOS
Language	Displays the specified language **English** (**US**) (**default**) / Deutsch
System Time	Sets the time
System Date	Sets the date
Floppy Options	Displays the floppy options submenu
Primary IDE Master	Reports the size of the connected IDE device; displays the device configuration submenu for the Primary IDE master interface
Primary IDE Slave	Reports the size of a connected IDE device displays; displays the device configuration submenu for the Primary IDE slave interface
Secondary IDE Master	Reports size of a connected IDE device; displays the device configuration submenu for the Secondary IDE master interface
Secondary IDE Slave	Reports the size of the connected IDE device; displays the device configuration submenu for the Secondary IDE slave interface

3.2.3.1 Floppy Options Submenu

The following table lists the program items and configuration options in the Floppy Options submenu.

Program Item	Configuration Options
Diskette A:	• Disabled • 360 KB, 5.25 inch • 1.2 MB, 5.25 inch • 720 KB, 3.5 inch • **1.44/1.25 MB, 3.5 inch (default)** • 2.88 MB, 3.5 inch
Diskette B:	• **Disabled (default)** • 360 KB, 5.25 inch • 1.2 MB, 5.25 inch • 720 KB, 3.5 inch • 1.44/1.25 MB, 3.5 inch • 2.88 MB, 3.5 inch
Floppy Write Protect	**Disabled (default)** / Enabled

3.2.3.2 Primary/Secondary IDE Master/Slave Configuration Submenus

The following table lists the program items and configuration options in the Primary/Secondary IDE Master/Slave Configuration submenus.

Program Item	Configuration Options
Type	• None • ATAPI Removable • IDE Removable (for example an LS-120 drive) • CD-ROM • User • **Auto (default)**
Program Item	**Configuration Options, Auto or User enabled**
Cylinders	Reports the number of cylinders for the hard disk drive (Auto enabled) or enables the user to the specify the number of cylinders for the hard disk (User enabled)
Heads	Reports the number of cylinders for the hard disk drive (Auto enabled) or enables the user to the specify the number of cylinders for the hard disk (User enabled)
Sectors	Reports the number of cylinders for the hard disk drive (Auto enabled) or enables the user to the specify the number of cylinders for the hard disk (User enabled)
Maximum Capacity	Reports the maximum capacity of the hard disk (calculated from the number of cylinders, heads, and sectors)
Program Item	**Configuration Options**
Multi-Sector Transfers	For the setting that provides optimum performance, see the specifications for the hard disk drive. • Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**
LBA Mode Control	Specifies the IDE translation mode. LBA, or logical block addressing, replaces cylinders, heads, and sectors. Disabled / **Enabled (default)**

continued ☛

Primary/Secondary Master/Slave Configuration Submenu (continued)

Program Item	Configuration Options
Transfer Mode	Sets the transfer mode for the IDE interface • Standard • Fast PIO 1 • Fast PIO 2 • Fast PIO 3 • **Fast PIO 4 (default)** ⚠ **CAUTION!** Do not change the IDE translation mode after formatting the hard disk drive. Changing the mode after formatting can corrupt data.
Ultra DMA	Sets the Ultra DMA mode for the hard disk drive. • **Disabled (default)** • Mode 0 • Mode 1 • Mode 2

3.2.4 Advanced Menu

The following table lists the program items and configuration options in the Advanced menu.

Program Item	Configuration Options
Plug & Play O/S	No / **Yes (default)**
Reset Configuration Data	**No (default)** / Yes
Memory Cache	Disabled / **Enabled (default)**
Memory Bank 0	None. Reports the size and type of the memory module in bank 0
Memory Bank 1	None. Reports the size and type of the memory module in bank 1
Resource Configuration Submenu	None. Displays the resource configuration submenu
Peripheral Configuration Submenu	None. Displays the peripheral configuration submenu
Keyboard Configuration Submenu	None. Displays the keyboard features submenu
Video Configuration Submenu	None. Displays the video configuration submenu
DMI Event Logging Submenu	None. Displays the DMI event logging menu

3.2.4.1 Resource Configuration Submenu

The following table lists the program items and configuration options in the Resource Configuration submenu.

Program Item	Configuration Options
Memory Reservation	Reserves specific upper memory blocks for use by legacy ISA devices.
	C800 - CBFF **Available (default)** | Reserved
	CC00- CFFF **Available (default)** | Reserved
	D000 - D3FF **Available (default)** | Reserved
	D400 - D7FF **Available (default)** | Reserved
	D800 - DBFF **Available (default)** | Reserved
	DC00 - DFFF **Available (default)** | Reserved
	Memory hole **Disabled (default)** | Conventional | Extended
IRQ Reservation	Reserves specific IRQs for use by legacy ISA devices
	IRQ3 Available | Reserved
	IRQ4 Available | Reserved
	IRQ5 Available | Reserved
	IRQ7 Available | Reserved
	IRQ10 Available | Reserved
	IRQ11 Available | Reserved
	An asterisk (*) indicates an IRQ conflict

3.2.4.2 Peripheral Configuration Submenu

The following table lists the program items and the configuration options in the Peripheral Configuration submenu.

Program Item	Configuration Options
Serial Port A	Disabled / Enabled / **Auto (default)**
	Setup assigns the first free COM port, normally COM1, 3F8h, IRQ4
	An asterisk (*) indicates a conflict with another device
Serial Port B	Disabled / Enabled / **Auto (default)**
	Setup assigns the first free COM port, normally COM2, 2F8h, IRQ3
	An asterisk (*) indicates a conflict with another device
Serial Port B Mode	**Normal (default)** / IrDA / ASK-IR
Parallel Port	Disabled / Enabled / **Auto (default)**
	Setup assigns LPT1, 378h, IRQ7
	An asterisk (*) indicates a conflict with another device

continued ☛

Peripheral Configuration Submenu (continued)

Parallel Port Mode	• Output only (operates in AT†-compatible mode) • **Bi-directional (default)** (operates in bi-directional PS/2-compatible mode)) • EPP (Extended Parallel Port, a high-speed bi-directional mode) • ECP (Enhanced Capabilities Port, a high-speed bi-directional mode)
Floppy Disk Controller	Disabled / **Enabled (default)**
IDE Controller	Disabled / Primary / Secondary / **Both (default)**
Audio	Disabled / **Enabled (default)**
Legacy USB Support	Disabled / **Enabled (default)**
Hardware Monitor	Disabled / **Enabled (default)**

NOTE

If you specifically set either serial port address, that address will not appear in the list of options for the other serial port. If an ATI mach32† *or an* ATI mach64† *video controller is active (as an add-in card), the COM4, 2E8h address will not appear in the list of options for either serial port.*

3.2.4.3 Keyboard Features Submenu

The following table lists the program items and configuration options in the Keyboard features submenu.

Program Item	**Configuration Options**
Numlock	**Auto (default)** / On / Off
Key Click	**Disabled (default**) / Enabled
Keyboard Auto-repeat Rate	• **30/sec (default)** • 26.7/sec • 21.8/sec • 18.5/sec • 13.3/sec • 10/sec • 6/sec • 2/sec
Keyboard Auto-repeat Delay	• ¼ sec • **½ sec (default)** • ¾ sec • 1 sec

3.2.4.4 Video Configuration Submenu

The following table lists the program items and configuration options in the Video Configuration submenu.

Program Item	Configuration Options
Palette Snooping	Enables a primary PCI graphics controller to share a common palette with an ISA add-in video card. **Disabled (default)** / Enabled

3.2.4.5 DMI Event Logging Submenu

The following table lists the program items and configuration options in the DMI Event Logging submenu.

Program Item	Configuration Options
Event Log Capacity	None. Reports if there is space available in the event log.
Event Log Validity	None. Reports if the contents of the event log is valid.
View DMI event log	None. Enables viewing of DMI event log. Press <Enter> to view the event log.
Clear all DMI event logs	Clears the DMI Event Log after reboot. **No (default)** / Yes
Event Logging	Enables or disables even logging. Disable / **Enabled (Default)**
Mark DMI Events as read	Mark all DMI events as read. Press <Enter> to access the confirmation dialog box.

3.2.5 Security Menu

The following table lists the program items and configuration options in the Security menu.

Program Item	Configuration Options
User Password Is	None. Reports the User password if set.
Supervisor Password Is	None. Reports the Supervisor password if set.
Set User Password	The user can enter a password up to seven alphanumeric characters.
Set Supervisor Password	The user can enter a password up to seven alphanumeric characters.
Unattended Start	Locks the keyboard at boot; requires the user to enter the User password. **Disabled (default)** / Enabled

3.2.6 Power Menu

The following table lists the program items and configuration options in the Power menu.

Program Item	Configuration Options
Power Management	Disabled / **Enabled (default)**
Inactivity Timer	Sets the time before the computer enters standby mode • **Off (default**) • 1 Minute • 2 Minutes • 4 Minutes • 6 Minutes • 8 Minutes • 12 Minutes • 16 Minutes
Hard Drive	Enables the hard drive to be power-managed during Standby and Suspend. Disabled / **Enabled (default)**
VESA Video Power Down	Enables video to be power-managed during Standby and Suspend. Disabled / **Standby (default)** / Suspend / Sleep

3.2.7 Boot Menu

The following table lists the program items and configuration options in the Boot menu.

Program Item	Configuration Options	
Scan User Flash Area	Enables the BIOS to scan the flash memory for user binaries. **Disabled (default)** / Enabled	
Restore on AC Power Loss	Stay off / **Last State (default)** / Power On	
On Modem Ring	Stay Off / **Power On (default)**	
On LAN	Stay Off / **Power On (default)**	
On PME	Stays Off / **Power On (default)**	
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device Fifth Boot Device*	• Removable devices • Hard Drive • ATAPI CD-ROM Drive • Network boot • LANDesk Service Agent	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering.
Hard Drive, submenu	No options	Lists available hard drives. When selected, displays the Hard Drive submenu.
Removable Devices, submenu	No options	Lists available removable devices. When selected, displays the Removable Devices submenu.

* This option is only available if an Intel EtherExpress Pro/100b Ethernet add-in card is installed in the system.

3.2.7.1 Hard Drive Submenu

This submenu is for configuring the boot sequence for hard drives.

Options	Description
• Installed hard drive • Bootable ISA Cards	Specifies the boot sequence for the hard drives attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

3.2.7.2 Removable Devices Submenu

This submenu is for configuring the boot sequence for removable devices.

Options	Description
• Legacy Floppy Drives	Specifies the boot sequence for the removable hard drives attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

3.2.8 Exit Menu

The following table lists the program items and options in the Exit menu.

Program Item	Select this program item to...
Exit Saving Changes	Exit Setup and save any changes. To exit Setup and save changes from anywhere in Setup, press <F10>.
Exit Discarding Changes	Exit Setup and discard any changes. Pressing the <Esc> key in any of the four main screens will also exit and discard changes.
Load Setup Defaults	Return all program items to the factory defaults. To return all program items to their defaults from anywhere in Setup, press <F9>.
Load Custom Defaults	Return all program items to the custom defaults.
Save Custom Defaults	Normally, the BIOS reads the setup settings from battery backed CMOS RAM. If the CMOS RAM fails, the BIOS uses the custom defaults. If no custom defaults are set, the BIOS uses the factory defaults.
Discard Changes	Discard changes without exiting Setup. This selection loads the CMOS RAM values that were present when the computer was turned on.

4 Error Messages

4.1 BIOS Error Messages

Table 37. BIOS Error Messages

Error Message	Explanation
Diskette drive A error or Diskette drive B error	Drive A: or B: is present but fails the BIOS POST diskette tests. Check to see that the floppy drive controller is enabled and the drive is defined with the proper diskette type in Setup and that the diskette drive is attached correctly.
Extended RAM Failed at offset: nnnn	Extended memory not working or not configured properly at offset nnnn.
Failing Bits: nnnn	The hex number nnnn is a map of the bits at the RAM address (in System, Extended, or Shadow memory) which failed the memory test. Each 1 (one) in the map indicates a failed bit.
Fixed Disk 0 Failure or Fixed Disk 1 Failure or Fixed Disk Controller Failure	Fixed disk is not working or not configured properly. Check to see if fixed disk is attached properly. Run Setup be sure the fixed-disk type is correctly identified and enabled.
Incorrect Drive A type - run SETUP	Type of floppy drive A: not correctly identified in Setup.
Incorrect Drive B type - run SETUP	Type of floppy drive B: not correctly identified in Setup.
Invalid NVRAM media type	Problem with NVRAM (CMOS) access.
Keyboard controller error	The keyboard controller failed test. Try replacing the keyboard.
Keyboard error	Keyboard not working.
Keyboard error nn	BIOS discovered a stuck key and displays the scan code nn for the stuck key.
Keyboard locked - Unlock key switch	Unlock the system to proceed.
Monitor type does not match CMOS - Run SETUP	Monitor type not correctly identified in Setup.
Operating system not found	Operating system cannot be located on either drive A: or drive C:. Enter Setup and see if fixed disk and drive A: are properly identified.
Parity Check 1	Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Parity Check 2	Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Press <F1> to resume, <F2> to Setup	Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change any settings.

continued ☛

Table 37. BIOS Error Messages (continued)

Error Message	Explanation
Previous boot incomplete - Default configuration used	Previous POST did not complete successfully. POST loads default values and offers to run Setup. If the failure was caused by incorrect values and they are not corrected, the next boot will likely fail. On systems with control of wait states, improper Setup settings can also terminate POST and cause this error on the next boot. Run Setup and verify that the wait-state configuration is correct. This error is cleared the next time the system is booted.
Real-time clock error	Real-time clock fails BIOS test. May require board repair.
Shadow Ram Failed at offset: nnnn	Shadow RAM failed at offset nnnn of the 64k block at which the error was detected.
System battery is dead - Replace and run SETUP	The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.
System cache error - Cache disabled	RAM cache failed the BIOS test. BIOS disabled the cache.
System CMOS checksum bad - run SETUP	System CMOS has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Run Setup and reconfigure the system either by getting the Default Values and/or making your own selections.
System RAM Failed at offset: nnnn	System RAM failed at offset nnnn of in the 64k block at which the error was detected.
System timer error	The timer test failed. Requires repair of system board.

4.2 Port 80h POST Codes

During POST (power-on self test), the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires the use of an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The following table provides the POST codes that can be generated by the motherboard's BIOS. Some codes are repeated in the table because that code applies to more than one operation.

Table 38. Port 80h Codes

Code	Description of POST Operation Currently In Progress
02h	Verify Real Mode
03h	Disable Non-Maskable Interrupt (NMI)
04h	Get CPU type
06h	Initialize system hardware
08h	Initialize chipset with initial POST values
09h	Set IN POST flag
0Ah	Initialize CPU registers
0Bh	Enable CPU cache
0Ch	Initialize caches to initial POST values
0Eh	Initialize I/O component
0Fh	Initialize the local bus IDE
10h	Initialize Power Management
11h	Load alternate registers with initial POST values
12h	Restore CPU control word during warm boot
13h	Initialize PCI Bus Mastering devices
14h	Initialize keyboard controller
16h	BIOS ROM checksum
17h	Initialize cache before memory autosize
18h	8254 timer initialization
1Ah	8237 DMA controller initialization
1Ch	Reset Programmable Interrupt Controller
20h	Test DRAM refresh
22h	Test 8742 Keyboard Controller
24h	Set ES segment register to 4 GB
26h	Enable A20 line
28h	Autosize DRAM
29h	Initialize POST Memory Manager
2Ah	Clear 512 KB base RAM
2Ch	RAM failure on address line ***xxxx****
2Eh	RAM failure on data bits ***xxxx**** of low byte of memory bus
2Fh	Enable cache before system BIOS shadow
30h	RAM failure on data bits ***xxxx**** of high byte of memory bus
32h	Test CPU bus-clock frequency
33h	Initialize POST Dispatch Manager
34h	Test CMOS RAM
35h	Initialize alternate chipset registers
36h	Warm start shut down
37h	Reinitialize the chipset (MB only)

continued ☛

Table 38. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
38h	Shadow system BIOS ROM
39h	Reinitialize the cache (MB only)
3Ah	Autosize cache
3Ch	Configure advanced chipset registers
3Dh	Load alternate registers with CMOS values
40h	Set Initial CPU speed new
42h	Initialize interrupt vectors
44h	Initialize BIOS interrupts
45h	POST device initialization
46h	Check ROM copyright notice
47h	Initialize manager for PCI Option ROMs
(Rel. 5.1 and earlier)	
48h	Check video configuration against CMOS
49h	Initialize PCI bus and devices
4Ah	Initialize all video adapters in system
4Bh	Display QuietBoot screen
4Ch	Shadow video BIOS ROM
4Eh	Display BIOS copyright notice
50h	Display CPU type and speed
51h	Initialize EISA board
52h	Test keyboard
54h	Set key click if enabled
56h	Enable keyboard
58h	Test for unexpected interrupts
59h	Initialize POST display service
5Ah	Display prompt "Press F2 to enter SETUP"
5Bh	Disable CPU cache
5Ch	Test RAM between 512 and 640 KB
60h	Test extended memory
62h	Test extended memory address lines
64h	Jump to UserPatch1
66h	Configure advanced cache registers
67h	Initialize Multi Processor APIC
68h	Enable external and CPU caches
69h	Setup System Management Mode (SMM) area
6Ah	Display external L2 cache size
6Ch	Display shadow-area message
6Eh	Display possible high address for UMB recovery

continued ☛

Table 38. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
70h	Display error messages
72h	Check for configuration errors
74h	Test real-time clock
76h	Check for keyboard errors
7Ah	Test for key lock on
7Ch	Set up hardware interrupt vectors
7Eh	Initialize coprocessor if present
80h	Disable onboard Super I/O ports and IRQs
81h	Late POST device initialization
82h	Detect and install external RS232 ports
83h	Configure non-MCD IDE controllers
84h	Detect and install external parallel ports
85h	Initialize PC-compatible PnP ISA devices
86h	Re-initialize onboard I/O ports
87h	Configure Motherboard Configurable Devices
88h	Initialize BIOS Data Area
89h	Enable Non-Maskable Interrupts (NMIs)
8Ah	Initialize Extended BIOS Data Area
8Bh	Test and initialize PS/2 mouse
8Ch	Initialize floppy controller
8Fh	Determine number of ATA drives
90h	Initialize hard-disk controllers
91h	Initialize local-bus hard-disk controllers
92h	Jump to UserPatch2
93h	Build MPTABLE for multi-processor boards
94h	Disable A20 address line (Rel. 5.1 and earlier)
95h	Install CD-ROM for boot
96h	Clear huge ES segment register
97h	Fixup Multi Processor table
98h	Search for option ROMs. One long, two short beeps on checksum failure
99h	Check for SMART Drive
9Ah	Shadow option ROMs
9Ch	Set up Power Management
9Eh	Enable hardware interrupts
9Fh	Determine number of ATA and SCSI drives
A0h	Set time of day
A2h	Check key lock
A4h	Initialize typematic rate

continued ☛

Table 38. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
A8h	Erase F2 prompt
Aah	Scan for F2 key stroke
Ach	Enter SETUP
Aeh	Clear IN POST flag
B0h	Check for errors
B2h	POST done - prepare to boot operating system
B4h	One short beep before boot
B5h	Terminate QuietBoot
B6h	Check password (optional)
B8h	Clear global descriptor table
B9h	Clean up all graphics
Bah	Initialize DMI parameters
BBh	Initialize PnP Option ROMs
BCh	Clear parity checkers
BDh	Display MultiBoot menu
Beh	Clear screen (optional)
BFh	Check virus and backup reminders
C0h	Try to boot with INT 19
C1h	Initialize POST Error Manager (PEM)
C2h	Initialize error logging
C3h	Initialize error display function
C4h	Initialize system error handler
	The following are for boot block in Flash ROM
E0h	Initialize the chipset
E1h	Initialize the bridge
E2h	Initialize the CPU
E3h	Initialize system timer
E4h	Initialize system I/O
E5h	Check force recovery boot
E6h	Checksum BIOS ROM
E7h	Go to BIOS
E8h	Set Huge Segment
E9h	Initialize Multi Processor
Eah	Initialize OEM special code
Ebh	Initialize PIC and DMA
Ech	Initialize Memory type
Edh	Initialize Memory size

continued ☛

Table 38. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
Eeh	Shadow Boot Block
Efh	System memory test
F0h	Initialize interrupt vectors
F1h	Initialize Run Time Clock
F2h	Initialize video
F3h	Initialize beeper
F4h	Initialize boot
F5h	Clear Huge segment
F6h	Boot to Mini DOS
F7h	Boot to Full DOS

5 Specifications and Customer Support

5.1 Online Support

Find information about Intel motherboards under “Product Info” or “Customer Support” at this World Wide Web site:

`http://www.intel.com/`

or at this FTP site:

`ftp://ftp.intel.com/pub/bios/`

5.2 Specifications

The motherboard complies with the following specifications:

Table 39. Compliance with Specifications

Specification	Description	Revision Level
ACPI	Advanced Configuration and Power Interface specification	Version 1.0, Date December 22, 1996 Intel Corp., Microsoft Corporation, Toshiba Corporation
APM	Advanced Power Management BIOS interface specification	Revision 1.2, Date February, 1996 Intel, Microsoft
ATA-33	Synchronous DMA Transfer Protocol specification (to be proposed as Ultra DMA/33 standard)	Revision 0.7, May 21, 1996 Quantum document no. 70-108412-1
DDC2	Display Data Channel standard	Version 2, Revision 0, April 9, 1996 Video Electronics Standards Association
DMI	Desktop Management Interface BIOS specification	Version 2.0, October 16, 1995 American Megatrends Inc., Award Software International Inc., Dell Computer Corporation, Intel, Phoenix Technologies Ltd, SystemSoft Corporation
DPMS	Display Power Management Signaling	Revision 1.0 Video Electronics Standards Association

continued ☛

Table 39. Compliance with Specifications (continued)

Specification	Description	Revision Level
"El Torito"	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies, IBM Corporation
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2]
Feature Connector	Standard VGA Pass-Through Connector (VSPC)	Version 1.0, March, 1994 Video Electronics Standards Association
NLX	NLX Form Factor Specification	Version 1.2
NLX Power Supply	NLX Power Supply recommendations	Version 1.1
PCI	PCI Local Bus specification	Revision 2.1, June 1, 1995 PCI Special Interest Group
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994 Compaq Computer Corp, Phoenix Technologies, Intel
UHCI	Universal Host Controller Interface	Revision 1.1
USB	Universal Serial Bus specification	Revision 1.0, January 15, 1996 Compaq, Digital Equipment Corporation, IBM PC Company, Intel, Microsoft, NEC, Northern Telecom