P A C I F I C E L E C T R O D A T A , I N C

PACIFIC ELECTRO DATA
PED-4001
DATA ACQUISITION AND EMULATION MODULE
USER'S MANUAL

Board design information

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INFORMATION TO USER

If this equipment does cause interference to radio or television reception which can be determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one or more of the following measures:

- reorient the receiving antenna
- relocate the computer with respect to the receiver
- move the computer away from the receiver
- plug the computer into a different outlet so that the computer and receiver are on different circuits.

If necessary, the user should consult the dealer or experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to Identify and Resolve Radio and Television Interference Problems"

This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock Number 004-000-0345-4.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SECTION 1. GENERAL OVERVIEW

1.1 BRIEF DESCRIPTION

The PED-4001 Small Computer System Interface (SCSI) State and Emulation module is a high-performance 'third party' state analyzer and SCSI controller developed specifically to support the Small Computer System Interface. The module occupies a single, full-length expansion slot of a PC or compatible and attaches to the SCSI bus via a 50 pin connector.

The module is a passive observer of bus activity during state analysis. Captured state vectors are stored in a high-speed, 2048-word acquisition memory. Each state vector includes the binary state of the 18 SCSI signals, 5 external signals and elapsed time from previous state vector capture. State vectors are written to memory only at specific state changes as defined by 16 edge qualifiers. The capture process is controlled by high-speed, user-programmable sequence control logic, 16-state masks and four 16-bit counters.

Emulation of a SCSI initiator or target device is done using an LSI SCSI protocol controller, and the host PC memory and DMA controller.

1.2 PURPOSE and SCOPE

This document describes the hardware design and operating characteristics of the PED-4001 module. It is intended for hardware and software designers, programmers, engineers and interested persons who need to understand the hardware and operation of the module. Readers should understand the concepts of logic design and controller programming. Familiarity with the IBM PC and the Small Computer System Interface is desirable.

This document contains the latest information available at the time of publication. Every effort has been made to ensure its accuracy. However, PED cannot be responsible for inadvertent errors and reserves the right to modify the contents at any time.

1.3 DOCUMENTATION

The following documents contain information the reader might find helpful in understanding the module.

Intel Component Data Catalog, Intel Corporation, Santa Clara, CA.

IBM Personal Computer Hardware Technical Reference Manual, IBM Corporation, Boca Raton, FL.

The TTL Data Book, Vol. 1, 2 and 3, Texas Instruments, Dallas, TX.

Programmable Logic Handbook, Monolithic Memories, Santa Clara, CA.

NCR 5380 SCSI Interface Chip Design Manual, NCR Corporation,

BSR X3.131-1986 Small Computer System Interface, American National Standards Institute

1.4 NOTATION

The following symbols, abbreviations, and notations are used throughout this manual.

Parentheses ( ) indicate an acronym or technical equivalent for the term preceding it. For example, "ACK (port 2, bit 1)" means that the signal ACK is assigned to bit 1 of port 2.

Square Brackets [ ] indicate that the preceding signal or part has a number of lines or signals comprising it. For instance, "DB[7-0]" means that the data bus DB is comprised of eight different signals ranging from DB7 through DB0.

Forward Slash / preceding an acronym indicates this is a signal that is at a low voltage when in its active, asserted state. An exception to this are the signals "C/D" and "I/O" where the initial signal prefix / has usually been excluded to avoid confusion.

SECTION 2. PRINCIPALS OF PASSIVE STATE ANALYSIS

The module acts as a passive 'third-party' observer during analysis operations. Captured data is stored in the 2048 word acquisition memory during state analysis. A captured state vector is made up of the 18 SCSI signals, 5 external signals and a 8- or 32-bit time tag.

The on-board timer is incremented every 100 nsec by the 10 MHz clock. Transition time state recording writes a state vector into acquisition memory, including a record of elapsed time from the previous write during specific state changes. This technique greatly conserves acquisition memory space while maintaining a constant time resolution of 100 nsec.

Saved state times are determined by 16 edge qualifiers. Either or both edges of the 18 SCSI signals can be selected in combination in each edge qualifier. The capture sequence is controlled by the acquisition program, the 16 state masks and four 16-bit counters in response to events occurring on the SCSI and external inputs.

This section describes in detail operating features of the PED-4001 module used to maximize its effectiveness in passive state analysis.

2.1 TRANSITION TIME STATE RECORDING

Most high-speed timing analyzers store samples of data at a selectable but fixed clock rate, with each sample using one word of the analyzer's total depth of the acquisition memory. At the high sampling frequencies necessary for good time resolution, several consecutive memory locations are often filled with the same information. Transition Time State Recording stores a new data sample only when there is a change. Along with the new data sample, a time tag is stored providing a measure of the time elapsed from the previous sample.

In operation, state data is sampled every 100 nanoseconds. Each sample is compared with the previous sample. If they are identical, the 32-bit timer is incremented. If they are different, the counter's value and the latest state data is stored into memory and the counter is reset to zero.

This method allows recording short bursts of activity separated by long intervals of inactivity, which parallels the operation of many electro-mechanical peripherals using the SCSI protocol.

2.2 STATE CHANGE QUALIFICATION

Even with efficient transition time state recording, capturing each state change of the 18 SCSI bus signals can rapidly fill the memory with superfluous data. It is desirable, therefore, to save only states involving the change of key "clock" (time significant) signals.

The SCSI has no single clock signal. While in an asynchronous information phase, information bytes are transferred across the SCSI bus using the two handshake semaphore signals request (REQ) and acknowledge (ACK). While in a synchronous data transfer phase, data bytes are transferred with a single "clock": REQ during a DATA IN phase and ACK during a DATA OUT phase. During the non-information phases, BUS-FREE, ARBITRATION, and (RE)SELECTION, or during the RESET condition, individual bus control signals have both state and timing significance. Examples of such signals are reset (RST), busy (BSY), and select (SEL). Even the individual data bits, D7 through D0, have time significance as the SCSI device ID during the ARBITRATION process.

To cope with the variety of situations outlined above, the analyzer has the ability to specify the edge of the SCSI signal to be used as a "clock" in capturing state data. The analyzer can use the rising edge, the falling edge or both edges of the eighteen SCSI bus signals in any combination as qualifying edges.

2.3 TIME TAG

The time tag is attached to each new state vector in the acquisition memory. The time tag contains the count in 100 nanosecond increments occurring between that state and the previous state vector. The time tag can be attached to the state data either horizontally, by extending the width of memory, or vertically, by extending the depth and bandwidth of the memory. Both methods are inefficient but at opposite ends of the frequency range. With horizontal attachment, considerable width must be added to handle the case of widely separated events. With vertical attachment, the memory bandwidth must be at least twice the maximum data capture rate. To overcome this inefficiency, the PED-4001 uses a combination of horizontal and vertical packing.

2.3.1 Data Word

Appended to the state data fields of each acquisition memory word is an eight-bit time field. This horizontal attachment of time information is sufficient to save up to 256 counts, or 25.6 microseconds of time, between consecutive events.

The format of this 32-bit DATA WORD is illustrated below with a definition of each bit of the 32-bit word.

Table 1. 32-Bit Data Word Format.

DATA WORD bits 31 through 00												
3 1	32222222 09876543	2 2	2 1	21111 09876	1 5	1 4	1 3	1 2	1 1	1 0	0 9	0 8	00000000 76543210
0	TTTTTTTT 65432107 TIME	R S T	D P	EEEEE 43210 EXTRN	B S Y	S E L	A T N	M S G	C / D	I / O	R E Q	A C K	DDDDDDDD 76543210 DATA

where the bit assignment is as follows:

- 0: Always '0' to identify the memory word as a DATA word.
- TIME: Least significant byte of time with a bias of minus 1. (Zero value implies +1 count). Note that the most significant bit of the time byte (T7) is assigned as DATA word bit 23.
- RST: SCSI control signal RST.
- DP: Parity bit of the SCSI data byte signals (ninth data bit).
- EXTRN: Five external input bits EX4 through EX0.
- BSY: SCSI control signal Busy
- SEL: SCSI control signal Select
- ATN: SCSI control signal Attention
- MSG: SCSI phase control bit Message
- C/D: SCSI phase control bit Command/Data
- I/O: SCSI phase control bit Input/Output
- REQ: SCSI data Request strobe
- ACK: SCSI data Acknowledge strobe
- DATA: 8 bit SCSI data byte, excluding parity bit (bits D7 through D0).

2.3.2 Time Word

The eight-bit time field of the DATA word overflows after 256 counts. If two consecutive events are separated by more than the 25.6 microseconds, a second word of the acquisition memory is used to store the upper 24 bits of a 32-bit time word. This second word is formatted as illustrated below.

Table 2. Time Word.

TIME WORD bits 31 through 00	
33222222 10987654	22221111111111000000000 32109876543210987654321
11111111 TIME FLAG	TTTTTTTTTTTTTTTTTTTTTTT 33222222222111111111100 10987654321098765432109 UPPER TIME

Where the bits are assigned as follows:

TIME FLAG: an eight bit field of all '1's identifying the memory word as a TIME word

UPPER TIME: most significant three bytes (24 bits) of time (T31 through T08). Upper time byte field is biased by a minus 256. A value of zero represents 256 counts or 25.6 microseconds.

2.4 INDEX OPERATION

The Index operation allows the user to save time and state data around some key Index event. The operation is analogous to the pre-/post-trigger counter and trigger mask operation of the universal logic analyzer. As in a logic analyzer, the capture operation is halted after a specified number of writes to the acquisition memory following the Index, thereby protecting saved data on either side of the Index.

When the analyzer is capturing data, time and state information is written into the Acquisition Memory, starting at address 000. At each write, the memory address register is incremented by 1. The total Acquisition Memory is 2048 words in length.

After data is written into word 2047, the address returns to the beginning of the memory space and the next data is written into address 000, writing over what was previously stored in memory. This overwriting process continues with the 2048 words most recently written to residing in memory.

The Index operation controls the capture process using the following procedure. The Index command loads the Index counter with the Index count value, from 1 to 2047 and forces a state vector write to the acquisition memory. In addition, the Index command causes the Index counter to increment after every write to the Acquisition Memory. When the counter reaches the maximum count of 2048, the capture operation is automatically stopped. The analyzer can be re-indexed any number of times before automatically stopping. Re-indexing causes the analyzer to reset the Index counter to its initial value.

2.5 SEQUENCE CONTROL PROGRAM

The state capture process is controlled by the sequence control program in the 32-byte acquisition program memory. The program consists of one- or two-byte commands. All one-byte commands execute in one system clock period (100 nsec) while all two-byte commands execute in two system clock periods (200 nsec). The commands can be broadly categorized into two groups: operation commands and flow-control commands. The majority of the commands fall into the latter group.

The operation commands are: Save, Skip, Sync, Index and NoOp. The Save command puts the analyzer in a state capture mode, saving all new states entered as the result of a state change qualified by the selected edge qualifier. The Skip command suspends the state capture mode until it is invoked again by another Save command. The Sync command causes a 100 nsec. pulse at the SYNC signal output. The Index operation was described in detail in section 2.4. The Index command initiates the Index process. The NoOp command is a "do-nothing" command.

The flow-control commands are made up of several conditional jump commands plus Load Counter commands. The Load Counter command is used to initialize one of the three general purpose 16-bit event counters. The Index command is a special case of the Load Counter command involving the Index counter, C0, which is dedicated to the Index operation.

Two conditional jump commands are of the "increment counter and test for end-count" type, allowing jumps conditioned on whether or not one of three counters has reached its end-count. Two other conditional jump commands allow testing the present state input against one of sixteen state masks and make the jump whether or not there is a match between the two. If the condition for the jump is met, the next command is accessed from the jump-to address of the program contained in the command. If the condition is not met, the next command is accessed from the next consecutive address. There is also an unconditional jump command which always accesses the next command from the jump-to address.

SECTION 3. FUNCTIONAL DESCRIPTION

A functional block diagram of the PED-4001 module is shown in Figure 1. The logic design and operation of each functional block is described in the following paragraphs. The circuitry making up each block is identified by component reference designation and schematic sheet number (refer to Appendix D).

3.1 SCSI BUS and EXTERNAL INPUTS DATA LATCHES

Schematic sheet 14 is of the sampled data latch for the SCSI bus signals and of the external inputs buffer. The "wire-OR" for each of the 18 SCSI signals from the J2 and J3 connectors are sampled every 100 nsec and saved in three 74LS174 Hex D-type Flip Flops, U91 through U93. Each IC is clocked by the buffered system clock SCLK1B. The external inputs from the J1 connector are buffered by the 74LS365 Hex Three-state Buffer, U90. The buffered outputs are enabled to the PA[4-0] bus with the signal /EXTEN. The SYNC output to J1-2 is also from U90.

3.2 ACQUISITION MEMORY AND DATA MULTIPLEXER

Sheet 13 of the schematic shows the acquisition memory and data multiplexer logic. The 2048-word-by-32-bit acquisition memory is implemented with four TMM2018D 2048x8 static RAM NMOS ICs, U20 through U23, each connected as 8 bits of the 32-bit wide acquisition data bus. A common output enable, /AMOE, write enable, /AMWE, and chip select, /AMCS, drive the four RAM devices.

Three TTL 74LS161 4-bit synchronous counters, U1, U10, U19, are cascaded to form the 11-bit acquisition memory address register. The register is cleared to zero with /AMACLR. The register is incremented each time a data word or a time word is written to memory by AMACKEN and SCLKB1. The counter rolls over from address 2047 to 0000. The twelfth bit is used to set a RS latch AMFULL, U88B and U24A, to signify that all addresses of the memory have been written to at least once.

Four 74LS244 octal buffers, U2 through U5, are used to multiplex the 32-bit acquisition memory bus (AM[31-00]) down to the 8-bit PA[]B bus, readable by the host PC. The buffer outputs are individually enabled by /AMI0, /AMI8, /AMI16 and /AMI24.

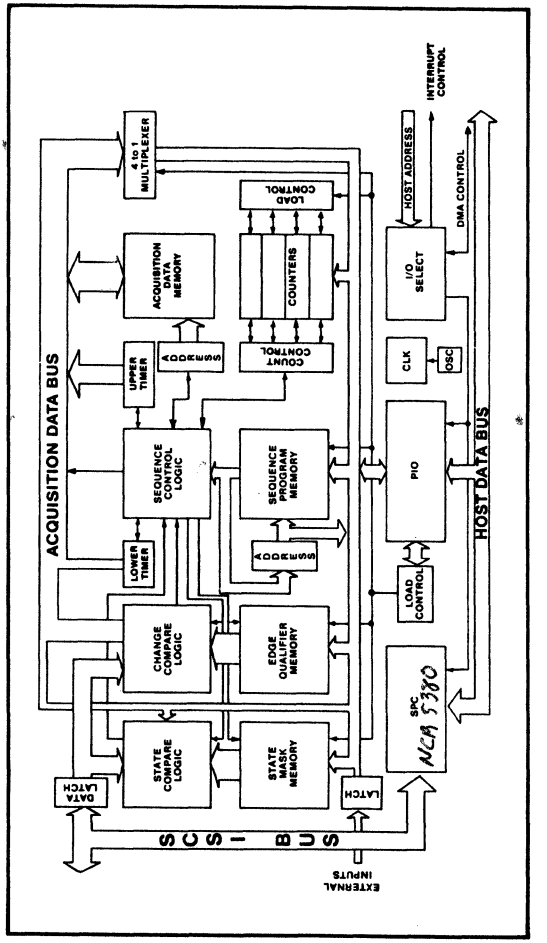


Figure 1. Data Analysis Module Functional Block Diagram.

3.3 CHANGE COMPARE LOGIC AND QUALIFIER MEMORY

The sixteen-word-by-36-bit edge qualifier memory is diagrammed on schematic sheet 7. The edge qualifier memory is implemented with nine 74LS189 16x4 static RAM ICs, U41 through U44 and U49 through U53. A 74LS376 transparent latch contains the address of the edge qualifier selected by /SAVEN. The latch is driven by the sequence controller data bits 3 through 0 (SCD3-SCD0). Two bits of the edge qualifier memory (/Q1Dn and /Q0Dn) are used to identify either the rising, falling, both or neither edges of each of the eighteen SCSI bus signals resulting in a qualified state change.

The change compare logic is on sheet 8 of the schematic. Six PAL16R4 ICs, U32 through U37, and a 74S30 NAND gate implement the change compare logic. The truth table of the compare logic for a single SCSI bus signal is provided below. In the table "n" takes all consecutive values from 0 to 15 plus 21 and 22. Q1Dn and Q0Dn are two bits from the edge qualifier memory corresponding to signal "n". DDn represents the present sampled state of the input signal "n". The name of the input signal assigned each value of "n" is listed in Table 3. AMn is the previous state sampled for the same input. If the change compare logic output CHNG is "1" for one or more of the eighteen SCSI signals and save-enable (SAVEN) is TRUE, the present sampled state will be written to the acquisition memory after being latched into the AM register, U31 through U37.

Table 3. Change Compare Logic Truth Table

Q1Dn	Q0Dn	AMn	DDn	CHNG
0	0	X	X	0
0	1	0	X	0
0	1	1	1	0
0	1	1	0	1
1	0	1	X	0
1	0	0	0	0
1	0	0	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

for n from 0 to 15, 21 and 22.
where X signifies "don't care."

Table 4. SCSI Bus Input DDn.

DDn	Input	DDn	Input	DDn	Input
0	DB0L	6	DB6L	12	MSGL
1	DB1L	7	DB7L	13	ANTL
2	DB2L	8	ACKL	14	SELL
3	DB3L	9	REQL	15	BSYL
4	DB4L	10	I/OL	21	DBPL
5	DB5L	11	C/DL	22	RSTL

3.4 STATE MASK MEMORY AND COMPARE LOGIC

Sixteen state mask words are stored in the state mask memory implemented with 12 74LS189A 16x4 RAM ICs, U58 through U63 and U74 through U79, as illustrated on sheet 5 of the schematic. The 74LS173 Quad Latch, U64, is loaded from SCD[3-0] with the 4-bit address of the selected state mask stored in the 74LS189 RAMs. Each state mask is 48 bits long, with two bits (/M0Dn and /M1Dn) assigned to each of the 18 SCSI signal, 5 buffered PA bus lines (PA[4-0]B) and a data parity odd/even signal (PEVEN).

The state compare logic, given on sheet 6 of the schematic, is implemented using five PAL16C1 ICs, U65 through U70, a 74S280 9-input comparator and a 74S30 8-input NAND gate. A truth table for a single bit 'n' of the state mask logic is shown in Table 5. Table 6 pairs each of the 24 input signals, DD0 through DD23, with the specific analyzer signal. For a state mask compare operation to be TRUE all 24 MTCH outputs must be '1'.

Table 5. State Mask Logic Truth Table for Bit n.

M1Dn	M0Dn	DDn	MTCH
0	0	X	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	X	1

for n from 0 to 23 and where X signifies "don't care."

Table 6. SCSI and EXTERN Input, DDn.

DDn	Input	DDn	Input	DDn	Input
0	DB0L	8	ACKL	16	PA0B
1	DB1L	9	REQL	17	PA1B
2	DB2L	10	I/OL	18	PA2B
3	DB3L	11	C/DL	19	PA3B
4	DB4L	12	MSGL	20	PA4B
5	DB5L	13	ATNL	21	DBPL
6	DB6L	14	SELL	22	RSTL
7	DB7L	15	BSYL	23	PEVEN

External signals

3.5 COUNTER LOGIC

The logic for the four 16-bit counters is shown on sheet 11 of the schematic. Each counter is implemented with two 74LS592 8-bit binary counters and one quarter of a 74S32 quad 2-input AND gate. The 74LS592 consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. All storage registers are driven by the PA[7-0]B bus. Each of the eight 74LS592 storage register clocks are driven by an output of an 74LS138 1-of-8 demultiplexer which in turn is driven by PB[2-0] and /LCSTB. All storage registers and counters are cleared with /RESET. All counter clock inputs are driven by SCLKB2.

The counter load control of counter C0, the Index counter, consisting of U9, U18 and U25D, is driven by the signal /SINDEX. The counter increment enable is driven by /INDXINC. The signal /INDXEND becomes active low when the count reaches FF00H.

The load control of counter C1, consisting of U8, U17 and U25C, is driven by the signal /C1CLD. Similarly, the load control of counters C2 and C3, consisting respectively of U7, U16, U6, U15, and sections A and B of U25, are driven by /C2CLD and /C3CLD respectively. The counter increment enables for C1 and C2 are driven by /C1CKEN and /C2CKEN. The counter increment enable for C3, the edge counter, is driven by /CHANGE. The signals /C1ZERO, /C2ZERO, and /C3ZERO go active low when the count of each associated counter, C1 through C3, reaches FF00h.

3.6 TIMER LOGIC

The 32-bit timer is shown on sheet 12 of the schematic. It is implemented with four cascaded 74LS590 8-bit binary counters, U11 through U14. Each of these devices contain an 8-bit counter that feeds an 8-bit output register. A counter clear signal, /TZERO, common to all counter stages, is active each time a data word is written to the acquisition memory. TZERO is output from the latch-gate combination of U48A and U39C, sections of a 74LS74 D-type Flip Flop, and a 74LS00 NAND gate driven by the signal /SAVE.

At every occurrence of the buffered 10MHz system clock /SCLKB3, the contents of the lower stage counter, U14, are transferred to the output register and the counter itself is incremented by one. An occurrence of the overflow signal from the lowest stage, /TLOV, transfers the contents of the upper stage counters to the output registers and, 100 nsec later, the upper stage counter is incremented. At that same time, the contents of the upper stage output registers, U11-U13, are placed on the AM[23-00] bus with output enable signal /TUEN and written to acquisition memory.

If the upper stage were to reach the maximum count, the lower counter is inhibited, freezing the count at this maximum value. This is done by the signal TUOV.

3.7 SEQUENCE CONTROL MEMORY and LOGIC

This section provides a description of all sequence control memory and logic operations performed by the PED-4001 module.

3.7.1 Sequence Control Memory

The logic diagram for the sequence control memory is on sheet 9 of the schematic. The memory is made up of four 74S189 16x4, inverted output RAMs, U46, U47, U55, and U56, organized as a 32-byte memory. Of the 32 bytes, only 29 are usable without restriction. The use of the first two bytes is restricted because of the possibility that the first operating clock period may be short. The last byte of RAM is not usable for reasons discussed in 3.7.2. The data inputs of each RAM is driven by a nibble of the PA[7-0]B bus. The write enable (/SCRW) signal is common to the four RAMs. The active low data outputs form the Sequence Controller Data bus, SCD[7-0].

A 74AS161 4-bit synchronous binary counter, U57, and a section of a 74AS74 D-type FF, U40B, are used for the 5-bit sequence controller address register. The D-type Flip Flop forms the least significant address bit with its Q output (SCA0) driving the chip selects of U46 and U55 and the increment enable input of U57 while the /Q output drives the chip selects of U47 and U56. The outputs of U57, SCA[4-1] drive the address inputs of the four RAMs. The address register is driven by the sequence controller memory outputs /SCD[4-0].

The state of the signal /SCALD controls the next address of the sequence controller; either the present address is incremented by one or the next address is specified by the inputs /SCD[4-0]. The output SCREND becomes active high when the address reaches 1Fh. SCREND immediately stops the system clock. This last memory location is not usable for program code.

3.7.2 Sequence Control Logic

Sheet 10 of the schematic contains the sequence control logic. The core of the sequence control logic is implemented with two 20R4B PALs, U28 and U29. U28 is programmed to control the writing to the acquisition memory. It functions independently from the sequence controller "next address" and counter control logic which is implemented using U29 and a 74LS139 dual 1-of-4 demultiplexer, U26. Both U28 and U29 share as common inputs SCD[7-5,1,0], FCR, and buffered system clock /SCLKB2.

3.7.2.1 Acquisition Memory Control

In addition to the inputs listed above, the signals /SCD4, /AMWE, and CHANGE are inputs to the acquisition memory controller, U28. The output signal /AMCS is the chip select for the acquisition memory. When this signal is active low, the memory is written to or read from memory depending on the states of /AMWE and /AMOE. If /AMWE is active low, /AMCS is active at each occurrence of /SAVE (see the discussion below) or at the overflow of the lower stage of the timer (/TLOV).

Output AM31 is the acquisition memory flag bit, identifying a data word if '0' or a time word if '1'. Active low outputs /TLEN and /TUEN serve to enable either the data word or the time word, respectively, to the acquisition memory bus, AM[30-0].

The save enable output signal, /SAVEN, is set active by the sequencer Save command and reset low by the Skip command. The /SAVEN signal is used internally by U28 as well as for clocking the edge qualifier address latch U46. The /SAVE signal is active each time a new data word is to be written

to the acquisition memory, because CHANGE occurs while SAVEN is active, an unconditional save is specified by an active /SCD4 /SCD4, or by the Index command. /SAVE is used by the timer logic.

The output signal /AMACKEN enables the incrementing of the acquisition memory address register.

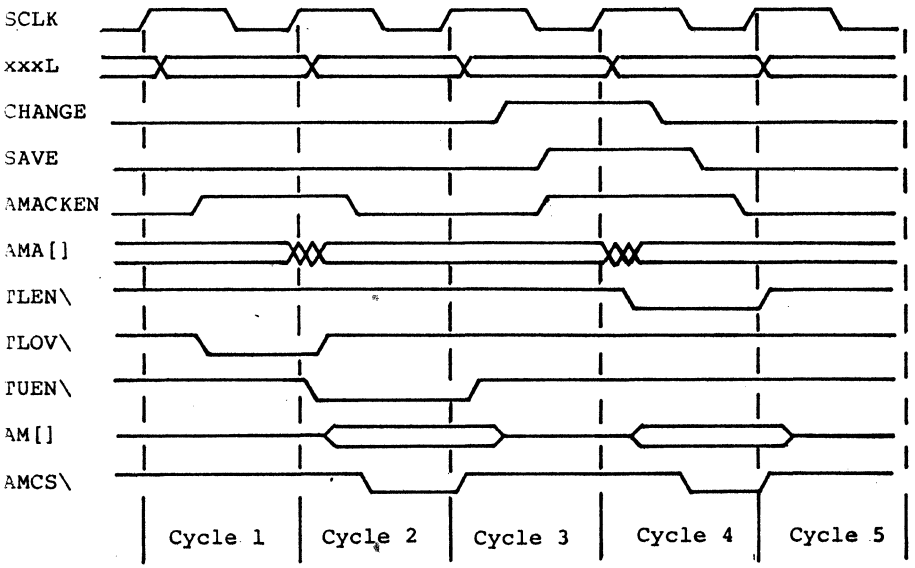


Figure 2. Acquisition Memory Data/Timer Write Timing.

Acquisition memory data and time word write timing is given in Figure 2. Five cycles of the 10 MHz system clock are shown with /AMWE and SAVEN assumed active. Cycle 1 occurs 256 SCLKs after a data write to acquisition memory, resulting in the assertion of /TLOV. Because this is the first lower-timer overflow (/TLOV) since a data word write, AMACKEN becomes active causing the AMA[] register to be incremented. /AMCS causes the write to acquisition memory in Cycle 2 with /TUEN enabling the time word to the AM[] bus. During Cycle 3 a qualified data CHANGE is detected which sets SAVE and AMACKEN followed in Cycle 4 with /TLEN and /AMCS. These signals enable the data word to the AM[] bus which is written to acquisition memory. No activity occurs during Cycle 5. Note that if Cycle 1 were not the first

overflow of the lower timer, AMACKEN would not be asserted and the AMA[] register would not be incremented. The new time word would be written over the old value during Cycle 2.

The only input to U28 not yet mentioned is the next address fetch signal, NAFTCH. This signal is only active when the "next address" is on the /SCD[] bus. U28 ignores the /SCD[] lines during NAFTCH.

3.7.2.2 Next-Address and Counter Control

The "next address" and counter logic of U29 and U26 have five inputs in addition to those common with U28. They will be identified in the following discussion of each U29 and U26 output.

NAFTCH was introduced in the discussion of U28. This output is active during the sequence control "next address" fetch cycle. Any sequencer command byte with a one as its MSB will be followed by a "next address" byte.

The signal /CNCLD, along with /SCD[1-0], drive U26B to generate counter load strobes /C1CLD, /C2CLD, and /C3CLD. These strobes cause the contents of the input register of C1 through C3 to be transferred to their respective counter. The fourth output of U26B (which occurs if the Index counter, C0, is selected) is OR'ed with the manual index signal (/MINDEX) to form /SINDEX. /SINDEX sets the INDEXED latch [U88A] and causes the contents of the input register of the Index counter to be transferred to the counter proper. The /CNCLD signal is generated whenever the Load Counter command (001ixxcc) is decoded by U29.

The signal /CNINC, along with /SCD[1-0], drives U26A to generate the counter increment enables /C1INC and /C2INC. These enables cause their respective counters to be incremented by one count. The /CNINC signal is generated by U29 whenever either the Jump Zero (100ixxcc) or Jump Not Zero (101ixxcc) commands are decoded. If INDEXED is TRUE, the signal /AMACKEN causes /INDXINC which increments the Index counter, C0.

The SYNC output of U29 is generated whenever the Sync command (000i0000) is decoded.

The last two outputs of U29 control the sequence control address register, SCA[]. The signals are /DSCA0 and /SCALD. /DSCA0 is the input to the D-type Flip Flop U40B whose outputs are SCA0 and /SCA0. /SCALD controls the load/increment operation of the SCA[4-1] counter.

Table 7 provides a summary of the logic operation. In the table, (t) and (t+1) refer to the signal state at clock time "t" and the clock time immediately following. Note that the upper four bits of the "next address" byte, /SCD[4-1], are logically inverted. Therefore, bits 4 through 1 of the "next address" must be complemented prior to being written to the acquisition memory during program load.

Table 7. "Next Address" Control Signal Logic.

COMMAND	CONDITION	SCA0(t+1)	SCALD	SCA[4-1](t+1)
Jump Zero	CnZERO=1	/SCA0(t)	FALSE	SCA[4-1](t)+SCA0(t)
Jump Zero	CnZERO=0	SCD0	TRUE	/SCD[4-1]
Jump Not Zero	CnZERO=1	SCD0	TRUE	/SCD[4-1]
Jump Not Zero	CnZERO=0	/SCA0(t)	FALSE	SCA[4-1](t)+SCA0(t)
Jump On Match	MATCH=1	SCD0	TRUE	/SCD[4-1]
Jump No Match	MATCH=0	/SCA0(t)	FALSE	SCA[4-1](t)+SCA0(t)

Figure 3 is a signal timing diagram of the "next address" control logic.

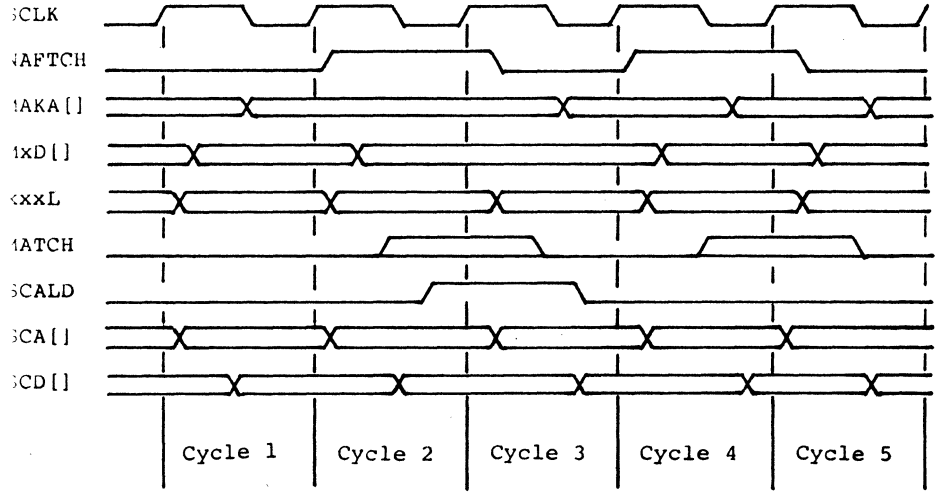


Figure 3. Sequence Controller "Next Address" Logic Timing.

Cycle 1 of the timing diagram depicts a jump command operation code access cycle. During this cycle, bits /SCD[3-0] are transferred to the MAKA[] register on the falling edge of SCLK. Cycle 2 is a "next address" access cycle, as identified by NAFTCH. During this cycle, the contents of the sampled input data latch (xxxL) is compared with the state mask memory output (MxD[]). This comparison logic generates the MATCH signal. MATCH is tested per the operation code of the previous cycle and SCALD becomes active, causing SCD[4-0] to be transferred to the SCA[] register at the next SCLK (the beginning of Cycle 3). Cycle 3 represents conditional jump operation code access cycle in which the jump was not taken since no SCALD was generated.

3.8 SCSI PROTOCOL CONTROL (SPO) LOGIC

Sheet 3 of the schematics shows the NCR 5380 SCSI interface device, U94. This is a 40-pin NMOS device designed to accommodate the SCSI. The device operates in both initiator and target roles. It supports arbitration, including reselection. Special high-current open collector output devices, capable of sinking 48 mA at 0.5 V, allow for direct connection to the single-ended SCSI bus.

The NCR 5380 SCSI device appears as a set of eight registers to the host PC. By reading and writing the appropriate registers, the PC can initiate any SCSI bus activity or sample and assert any signal on the SCSI bus. This allows the user to implement all or parts of the SCSI protocol in software. Table 8 shows the 5380 possible registers, their addresses, and names.

Table 8. 5380 Registers.

Address				
A2	A1	A0	Type	Name
0	0	0	R	Current SCSI Data
0	0	0	W	Output Data
0	0	1	R/W	Initiator Command
0	1	0	R/W	Mode
0	1	1	R/W	Target Command
1	0	0	R	Current SCSI Bus Status
1	0	0	W	Select Enable
1	0	1	R	Bus and Status
1	0	1	W	Start DMA Send
1	1	0	R	Input Data
1	1	0	W	Start DMA Target Receive
1	1	1	R	Reset Parity/Interrupts
1	1	1	W	Start DMA Initiator Receive

3.8.1 Data Registers

Three data registers are used to transfer SCSI commands, data, status, and message bytes between the host PC data bus and the SCSI bus. The current SCSI data register is a read-only register allowing the PC to read the active SCSI data bus. If parity checking is enabled, the SCSI bus parity is checked at the beginning of the read cycle. This register is used during a programmed I/O data read or during arbitration to check for higher priority arbitrating devices. Parity is not guaranteed during arbitration.

The Output Data Register is a write-only register used to send data to the SCSI bus, either using a normal I/O write, or under DMA control. This register is also used to assert the proper ID bits or the SCSI bus during the arbitration and selection phases.

The Input Data Register is a read-only register used to read latched data from the SCSI bus. Data is latched either during a DMA Target receive operation when /ACK goes active, or during a DMA Initiator receive when /REQ goes active. The DMA Mode bit (port 2, bit 1) must be set before data can be latched in the Input Data Register. This register may be read under DMA control. Parity is optionally checked when the Input Data Register is loaded.

3.8.2 Initiator Command Register

The Initiator Command Register is a read/write register used to assert certain SCSI bus signals, to monitor those signals, and to monitor the progress of bus arbitration. Many of these bits are significant only when being used as an Initiator; however, most can be used during Target operation.

The following discussion explains all bits used in the Initiator Command Register.

Bit 7 **ASSERT /RST**

Whenever a one is written to bit 7 of the Initiator Command Register, the /RST signal (pin 16) is asserted on the SCSI bus. The /RST signal will remain asserted until this bit is reset or until an external /RESET (pin 28) occurs. After this bit is set to one, IRQ (pin 23) goes active and all internal logic and control registers are reset (except for the interrupt latch and the ASSERT /RST bit). Writing a zero to bit 7 de-asserts the /RST signal. Reading this register simply reflects the status of the bit.

BIT 6 AIP (Arbitration in Progress - read bit)

This bit is used to determine if arbitration is in progress. For this bit to be active, the ARBITRATE bit (port 2, bit 0) must have been set previously. It indicates that a bus free condition has been detected, the chip has asserted BSY (pin 13), and the contents of the Output Data Register (port 0) are on the SCSI bus. AIP remains active until the ARBITRATE bit is reset.

BIT 6 TEST MODE (write bit)

This bit may be written during a test to disable all output drivers, effectively removing the 5380 from the circuit. Resetting this bit returns the part to normal operation.

BIT 5 LA (Lost Arbitration - read bit)

When active this bit indicates the 5380 has detected a bus free condition, has arbitrated for use of the bus by asserting /BSY (pin 13), placed its ID on the data bus, and lost arbitration due to assertion of /SEL (pin 12) by another bus device. For this bit to be active, the ARBITRATE bit (port 2, bit 0) must be active.

BIT 4 ASSERT /ACK

This bit is used by the bus initiator to assert /ACK (pin 14) on the SCSI bus. In order to assert /ACK, the TARGETMODE bit (port 2, bit 6) must be false. Writing a zero to this bit resets /ACK on the SCSI bus. Reading this register simply reflects the status of the bit.

BIT 3 ASSERT /BSY

Writing a one into this bit position asserts /BSY (pin 13) onto the SCSI bus. Conversely, a zero resets the /BSY signal. Asserting /BSY indicates a successful select or reselection has taken place and resetting this bit creates a bus disconnect condition. Reading this register simply reflects the status of this bit.

BIT 2 ASSERT /SEL

Writing a one into this bit position asserts /SEL (pin 12) onto the SCSI bus. /SEL is normally asserted after arbitration is completed. /SEL may be de-asserted by resetting this bit to zero. A read of this register simply reflects the status of the bit.

BIT 1 **ASSERT /ATN**

/ATN (pin 15) may be asserted on the SCSI bus by setting this bit to a one if the TARGETMODE bit (port 2, bit 6) is false. /ATN is normally asserted by the initiator to request a Message Out bus phase. Since ASSERT /SEL and ASSERT /ATN are located in the same register, a select with /ATN can be implemented with one MPU write. /ATN can be de-asserted by resetting this bit to zero. A read of this register simply reflects the status of the bit.

BIT 0 **ASSERT DATA BUS**

When set, the ASSERT DATA BUS bit enables the contents of the Output Data Register as chip outputs on the signals DB[0-7]. Parity is also generated and asserted on DBP.

When connected as an Initiator, the outputs are only enabled if the TARGETMODE bit (port 2, bit 6) is false, the received signal I/O (pin 17) is false, and the phase signals (C/D, I/O, and MSG) match the contents of the ASSERT C/D, ASSERT I/O, and ASSERT MSG in the Target Command Register.

This bit should also be set during DMA send operations.

3.8.3 Mode Register

The Mode Register is used to control the operation of the 5380. This register determines whether the chip operates as an initiator or target, whether DMA transfers are being used, whether parity is checked, and whether interrupts are generated on various external conditions. This register may be read to check the value of these internal control bits.

The following discussion explains the operation of these control bits.

BIT 7 **BLOCK MODE DMA**

The BLOCK MODE DMA bit controls the characteristics of the DMA DRQ/DACK handshake. This bit must be reset (0) when the DMA MODE bit is active (1). The DMA handshake uses the normal interlocked handshake and the rising edge of /DACK (pin 26) indicating the end of each byte being transferred.

BIT 6 TARGETMODE

The TARGETMODE bit allows the 5380 to operate as either an SCSI bus initiator, when the bit is reset (0), or as an SCSI bus target device, when the bit is set (1). In order for the signals /ATN (pin 15) and /ACK (pin 14) to be asserted on the SCSI bus, the TARGETMODE bit must be reset (0). In order for the signals C/D, I/O, /MSG, and /REQ to be asserted on the bus, the TARGETMODE bit must be set (1).

BIT 5 ENABLE PARITY CHECKING

The ENABLE PARITY CHECKING bit determines whether parity errors are ignored or saved in the parity error latch. If this bit is reset (0), parity is ignored. If this bit is set (1), parity errors are saved.

BIT 4 ENABLE PARITY INTERRUPT

The ENABLE PARITY INTERRUPT bit, when set (1), causes an interrupt (IRQ) to occur if a parity error is detected. A parity interrupt is only generated if the ENABLE PARITY CHECKING bit (bit 5) is also enabled (1).

BIT 3 ENABLE EOP INTERRUPT

When set (1), the ENABLE EOP INTERRUPT causes an interrupt to occur when DMA controller logic issues an /EOP (End of Process) signal (pin 27).

BIT 2 MONITOR BUSY

When true (1), the MONITOR BUSY bit causes an interrupt to be generated for any unexpected loss of BSY (pin 13). When the interrupt is generated because of the loss of BSY, the lower 6 bits of the Initiator Command Register are reset (0) and all signals are removed from the SCSI bus.

BIT 1 DMA MODE

The DMA MODE bit is normally used to enable a DMA transfer and must be set (1) before writing ports 5 through 7. Ports 5 through 7 are used to start DMA transfers. The TARGETMODE bit (port 2, bit 6) must be consistent with writes to port 6 and 7 (i.e. set for a write to port 6 and reset for a write to port 7). The control bit ASSERT DATA BUS (port 1, bit 0) must be true (1) for all DMA send operations. In the DMA mode, /REQ (pin 20) and /ACK (pin 14) are automatically controlled.

The DMA MODE bit is not reset on the receipt of an /EOP signal. Any DMA transfer may be stopped by writing a zero into this bit location; however, care must be taken not to cause /CS or /DACK to become active simultaneously.

BIT 0 **ARBITRATE**

The ARBITRATE bit is set (1) to start the arbitration process. Before setting this bit, the Output Data Register should contain the proper SCSI device ID value. Only one data bit should be active for SCSI bus arbitration. The 5380 waits for a bus free condition before entering the arbitration phase. The results of the arbitration phase can be determined by reading the status bits LA and AIP (port 1, bits 5 & 6, respectively).

3.8.4 Target Command Register

When connected as a target device, the Target Command Register enables the PC to control the SCSI bus information transfer phase and/or to assert /REQ (pin 20) simply by writing this register. The TARGETMODE bit (port 2, bit 6) must be true (1) for bus assertion to occur. The SCSI bus phases are described in Table 9.

Table 9. SCSI Information Transfer Phases.

Bus Phase	bit 0 assert I/O	bit 1 assert C/D	bit 2 assert MSG
Data Out	0	0	0
Unspecified	0	0	1
Command	0	1	0
Message Out	0	1	1
Data In	1	0	0
Unspecified	1	0	1
Status	1	1	0
Message In	1	1	1

When connected as an Initiator with DMA Mode true, and if the phase lines (I/O, C/D, and MSG) do not match the phase bits in the Target Command Register, a phase mismatch interrupt is generated when /REQ (pin 20) goes active. In order to send data as an Initiator, the ASSERT /I/O, ASSERT /C/D, and ASSERT /MSG bits must match the corresponding bits in the current SCSI Bus Status Register (port 4). The ASSERT /REQ bit (bit 3) has no meaning when operating as an Initiator.

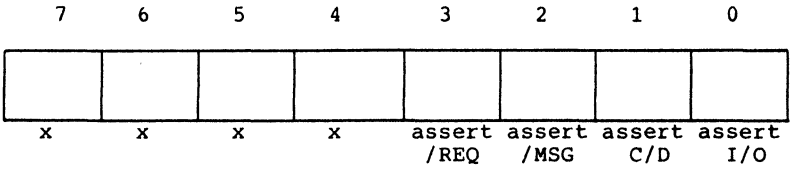


Figure 4. Target Command Register.

3.8.5 Current SCSI Bus Status

The Current SCSI Bus Status register is a read-only register used to monitor seven SCSI bus control signals plus the data bus parity bit. For example, an Initiator device can use this register to determine the current bus phase and poll /REQ for pending data transfers. This register can also be used to determine why a particular interrupt occurred.

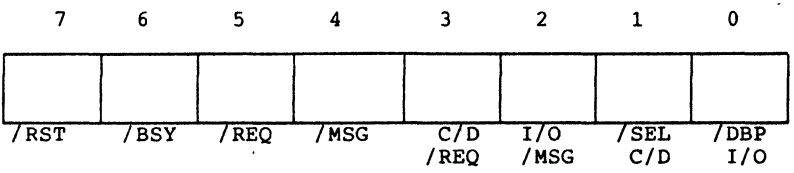


Figure 5. Current Bus Status Register.

3.8.6 Select Enable Register

The Select Enable Register is a write-only register used as a mask to monitor a single ID during a selection attempt. The simultaneous occurrence of the correct ID bit, /BSY false, and /SEL true causes an interrupt. This interrupt can be disabled by resetting all bits in this register. If the ENABLE PARITY CHECKING bit (port 2, bit 5) is active (1), parity is checked during selection.

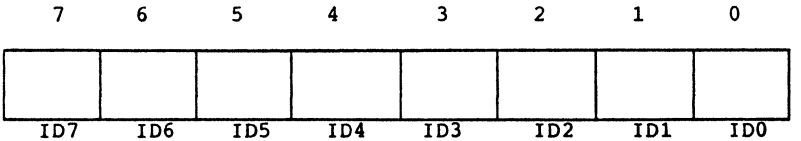


Figure 6. Set Enable Register.

3.8.7 Bus and Status Register

The Bus and Status Register is a read-only register used to monitor the remaining SCSI control signals not found in the Current SCSI Bus Status Register (/ATN & /ACK) as well as six other status bits. The following discussion explains each bit of the Bus and Status Register individually.

BIT 7 END OF DMA TRANSFER

The END OF DMA TRANSFER bit is set if /EOP (pin 27), /DACK (pin 26), and either /IOR (pin 24) or /IOW (pin 29) are simultaneously active for at least 100 nsec. Since the /EOP signal can occur during the last byte sent to the Output Data Register (port 0), the /REQ and /ACK signals should be monitored to insure the last byte has been transferred. This bit is reset when the DMA MODE bit is reset (0) in the Mode Register (port 2).

BIT 6 DMA REQUEST

The DMA REQUEST bit enables the MPU to sample the output pin /DRQ (pin 22). DRQ can be cleared by asserting /DACK (pin 26) or by resetting the DMA MODE bit (bit 1) in the Mode Register (port 2). The DRQ signal does not reset when a phase mismatch interrupt occurs.

BIT 5 PARITY ERROR

This bit is set if a parity error occurs during a data receive or a device selection. The PARITY ERROR bit can only be set (1) if the ENABLE PARITY CHECK bit (port 2, bit 5) is active (1). This bit may be cleared by reading the Reset Parity/Interrupt Register (port 7).

BIT 4 INTERRUPT REQUEST ACTIVE

This bit is set if an enabled interrupt condition occurs. It reflects the current state of the IRQ (pin 23) output and can be cleared by reading the Reset Parity/Interrupt Register (port 7).

BIT 3 PHASE MATCH

The SCSI signals /MSG, /C/D, and /I/O (pins 19, 18, and 17 respectively) represent the current information transfer phase. The PHASE MATCH bit indicates whether the current SCSI bus phase matches the lower three bits of the Target Command Register. PHASE MATCH is continuously updated and is only significant when operating as a bus initiator. A Phase Match must be active for data transfers to occur on the SCSI bus.

BIT 2 BUSY ERROR

The BUSY ERROR bit is active if an unexpected loss of the /BSY signal (pin 13) has occurred. This latch is set whenever the MONITOR BUSY bit (port 2, bit 2) is true and /BSY is false. An unexpected loss of /BSY disables any SCSI outputs and resets the DMA MODE bit (port 2, bit 1).

BIT 1 ATN

This bit reflects the condition of the SCSI bus control signal /ATN (pin 15). This signal is normally monitored by the target device.

BIT 0 ACK

This bit reflects the condition of the SCSI bus control signal /ACK (pin 14). This signal is normally monitored by the target device.

3.8.8 DMA Registers

Three write-only registers are used to initiate all DMA activity. They are Start DMA Send (port 5), Start DMA Target Receive (port 6), and Start DMA Initiator Receive (port 7). Simply by writing to these registers starts the DMA transfer. Data presented to the 5380 on signals D[0-7] during the register write is meaningless and has no effect on the operation. Prior to writing these registers, the BLOCK MODE DMA bit (bit 7), the DMA MODE bit (bit 1), and the TARGETMODE bit (bit 6) in the Mode Register (port 2) must be appropriately set. The individual registers are briefly discussed below.

The Start DMA Send register is written to initiate a DMA send from the DMA to the SCSI bus, for either initiator or target operations. The DMA MODE bit (port 2, bit 1) must be set before writing to this register.

:e Start DMA Target Receive register is written to initiate a
'A receive from the SCSI bus to the DMA for target operations
ıly. The DMA MODE bit (bit 1) and the TARGETMODE bit (bit 6) in
.e Mode Register (port 2) must both be set (1) before writing to
ıis register.

:e Start DMA Initiator Receive register is written to initiate a
1A receive from the SCSI bus to the DMA for initiator operations
ıly. The DMA MODE bit (bit 1) must be true (1) and the
ARGETMODE bit (bit 6) must be false (0) in the Mode Register
ort 2) before writing to this register.

.8.9 Interrupts

ne 5380 provides an interrupt output (IRQ) to indicate a task
ompletion or an abnormal bus occurrence. Choose from four
ossible IRQ assignments on the host PC: IRQ7, IRQ4, IRQ3, or
RQ2, corresponding to jumpers E3 through E6 respectively (see
able 10). Refer to Figure 7 for the location of the jumper
ins.

Table 10. Interrupt Select Jumpers

Jumpers	Interrupt
E3	IRQ7
E4	IRQ4
E5	IRQ3
E6	IRQ2

Jse of interrupts is optional and can be disabled by resetting
:he appropriate bits in the Mode Register (port 2) or the Select
Enable Register (port 4).

Vhen an interrupt occurs, the Bus and Status Register and the
Current SCSI Bus Status Register must be read to determine which
condition created the interrupt. IRQ (pin 23) can be reset
simply by reading the Reset Parity/Interrupt Register (port 7) or
by an external chip reset (/RESET active for 200 nsec).

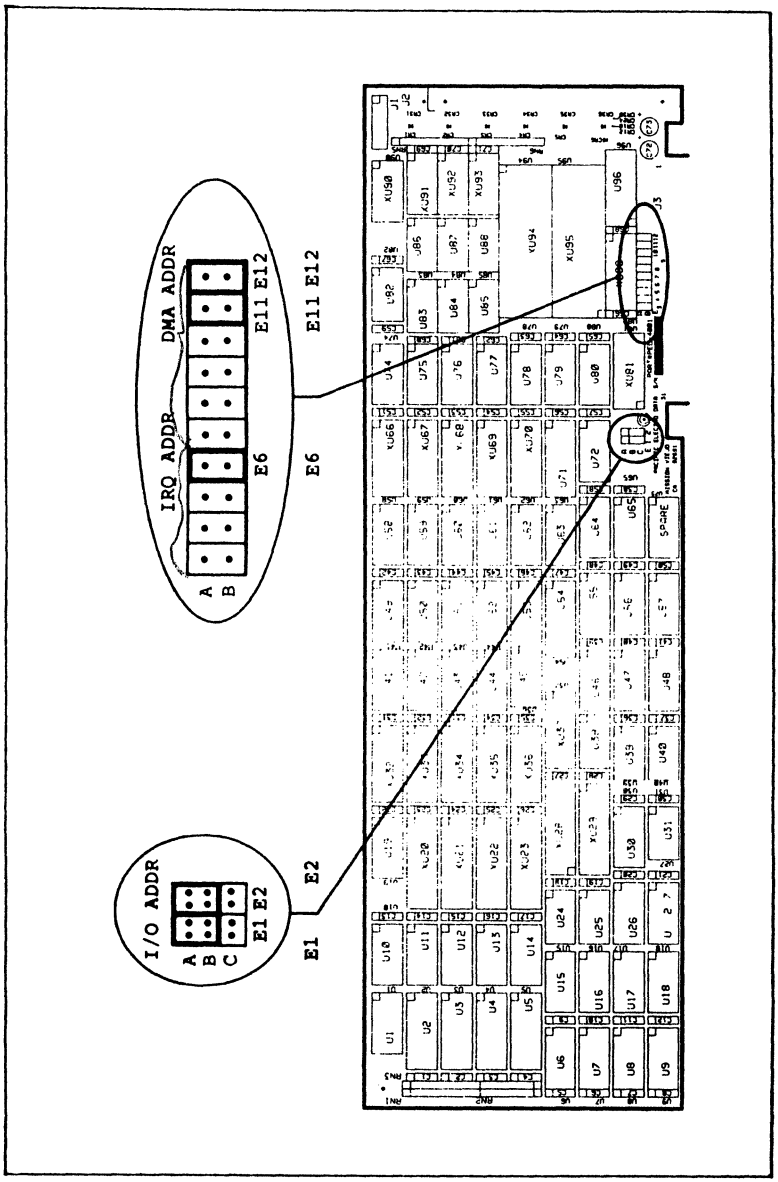


Figure 7. Jumper Block Locations on the Module.

An interrupt can be generated if any of these six conditions exists.

1. The chip is selected or reselected.
2. An /EOP signal occurs during a DMA transfer.
3. An SCSI bus reset occurs.
4. A parity error occurs during a data transfer.
5. A bus phase mismatch occurs.
6. An SCSI bus disconnection occurs.

The 5380 can generate a Selection/Reselection interrupt if /SEL (pin 12) is true (1), its device ID is true (1), and /BSY (pin 13) is false (0) for at least a bus settle delay (400 ns). If /I/O (pin 17) is active, this should be considered a reselect interrupt. The correct ID bit is determined by a match in the Select Enable Register (port 4). Only a single bit match is required to generate an interrupt. This interrupt may be disabled by writing zeros into all bits of the Select Enable Register.

An End of Process signal (/EOP at pin 27) is derived from the host PC bus terminal count signal (T/C). This signal sets the END OF DMA status bit (port 5, bit 7) and optionally generates an interrupt if the ENABLE EOP INTERRUPT bit (port 2, bit 3) is true. The /EOP pulse is not recognized (END OF DMA bit set) unless /EOP, /DACK, and either /IOR or /IOW are concurrently active for at least 100 nsec. DMA transfers can still occur if /EOP is not asserted at the correct time. This interrupt can be disabled by resetting the ENABLE EOP INTERRUPT bit.

The 5380 generates an interrupt when the /RST signal (pin 16) changes to true. The device releases all bus signals within 800 nsec of this change. This interrupt also occurs after setting the ASSERT /RST bit (port 1, bit 7). This interrupt cannot be disabled. The /RST signal is not latched in bit 7 of the Current SCSI Bus Status Register and may not be active when this port is read. Given this situation, the Bus Reset interrupt is determined by default.

An interrupt is generated for a received parity error if the ENABLE PARITY CHECK (bit 5) and the ENABLE PARITY INTERRUPT (bit 4) bits are set (1) in the Mode Register (port 2). Parity is checked during a read of the Current SCSI Data Register (port 0) and during a DMA receive operation. A parity error can be detected without generating an interrupt by disabling the ENABLE PARITY INTERRUPT bit and checking the PARITY ERROR flag (port 5, bit 5).

The SCSI phase lines are comprised of the signals I/O, C/D, and MSG. These signals are compared with the corresponding bits in the Target Command Register: ASSERT I/O (bit 0), ASSERT C/D (bit 1), and ASSERT MSG (bit 2). Comparisons are made continuously and are reflected in the PHASE MATCH bit (bit 3) of the Bus and Status Register (port 5). If the DMA MODE bit (port 2, bit 1) is active and a phase mismatch occurs when /REQ (pin 20) changes from false to true, an interrupt (IRQ) is generated.

A phase mismatch prevents the recognition of /REQ and removes the chip from the bus during an initiator send operation. /DB[0-7] and /DBP cannot be driven even though the ASSERT DATA BUS port (port 1, bit 0) is active. This interrupt is only significant when connected as an Initiator and can be disabled by resetting the DMA MODE bit. This interrupt can occur when connected as a Target if another device is driving the phase lines to a different state.

If the MONITOR BUSY bit (bit 2) in the Mode Register (port 2) is active, an interrupt will be generated if the /BSY signal (pin 13) goes false for at least 400 nsec. This interrupt may be disabled by resetting the MONITOR BUSY bit.

3.8.10 Data Transfers

Data can be transferred between SCSI bus and the host PC in one of two ways: Programmed I/O and Normal DMA. The following discussion describes these modes in detail.

Programmed I/O is the most primitive form of data transfer. The /REQ (pin 20) and /ACK (pin 14) handshake signals are individually monitored and asserted by reading and writing the appropriate register bits.

An Initiator Send operation would begin by setting the C/D, I/O, and /MSG bits in the Target Command Register to the correct state so that a phase match exists. In addition to the phase match condition, it is necessary for the ASSERT DATA BUS bit (port 1, bit 0) to be true and the received I/O signal to be false for the 5380 to send data.

For each byte transferred, the data is loaded into the Output Data Register (port 0) during an output operation, or the data is read from the Input Data Register (port 6) during an input operation.

Direct memory access (DMA) transfer is accomplished by way of the host PC DMA channel 1, 2, or 3 as selected by jumpers E7 through E12. Jumpers settings are defined in Table 11. Refer to Figure 7 for the location of the jumper pins.

Table 11. 5380 DMA Select Jumpers

Jumpers	DMA Channel
E7, E8	3
E9, E10	2
E11,E12	1

The SCSI chip outputs a DMA request (DRQ from pin 22) whenever it is ready for a byte transfer. The host DMA controller uses this DRQ signal to generate /DACK and an /IOR or an /IOW pulse to the 5380. DRQ goes inactive when /DACK is asserted and /DACK goes inactive sometime after the minimum read or write pulse width. This process is repeated for every byte transferred.

For all data transfer operations, /DACK and /CS should never be active simultaneously.

3.9 HOST INTERFACE, LOAD and CLOCK CONTROL LOGIC

The host computer communicates with the PED-4001 module through a 8255 Programmable Peripheral Interface device, U95, and the 5380 SCSI Protocol Controller device, U94. The two devices are mapped in the I/O space of the host. The host I/O address bus, A[9-2], and address enable, AEN, is decoded by U81, a PAL14L4. Jumpers E1 and E2 feed U81 to allow for the selection of different module address paragraph assignments.

The three paragraph segments are listed in Table 12 along with their value and jumper settings. Read the jumper setting "A-to-B" to mean the jumper should be placed across terminals A and B of the E pins. Refer to Figure 7 for the location of the jumper pins.

Table 12. Module I/O Address Define Constants.

Paragraph	0 x 30	0 x 33	0 x 38
E2 Jumper	C-to-B	A-to-B	A-to-B
E1 Jumper	A-to-B	C-to-B	A-to-B
Register	**Address**	**Address**	**Address**
5380 Current/Output Data	0 x 300	0 x 330	0 x 380
5380 Initiator Command	0 x 301	0 x 331	0 x 381
5380 Mode	0 x 302	0 x 332	0 x 382
5380 Target Command	0 x 303	0 x 333	0 x 383
5380 Current Status/ Select Enable	0 x 304	0 x 334	0 x 384
5380 Status/DMA Send	0 x 305	0 x 335	0 x 385
5380 Input Data/ DMA Receive	0 x 306	0 x 336	0 x 386
5380 Interrupts/ Initiator DMA	0 x 307	0 x 337	0 x 387
8255 Port A	0 x 308	0 x 338	0 x 388
8255 Port B	0 x 309	0 x 339	0 x 389
8255 Port C	0 x 30A	0 x 33A	0 x 38A
8255 Control	0 x 30B	0 x 33B	0 x 38B
8255 Port A	0 x 30C	0 x 33C	0 x 38C
8255 Port B	0 x 30D	0 x 33D	0 x 38D
8255 Port C	0 x 30E	0 x 33E	0 x 38E
8255 Control	0 x 30F	0 x 33F	0 x 38F

Lower host address lines go directly to both devices to select one of four addressable registers of the 8255 or one of eight addressable registers of the 5380. The host data bus is buffered by a 74LS245 (U96). A 74S08 NOR gate, U83C, creates the module /RESET signal by OR'ing the host I/O bus RESET and Port B bit 7 of the 8255 (PB7).

The three ports of the 8255 are partitioned as follows. The upper half of Port C, PC[7-4], is configured as an input port to monitor four module status signals /AMFULL, FCR, INDEXED and /INDXEND. The lower half of Port C, PC[3-0], is configured as an output port and is used for module clock and strobe control. Port B is configured as an output port. Output PB[7] enables the host PC to reset the module under software control. Output PB[6] is used to select the PED-4010 differential interface adapter when it is installed at the J2 SCSI interface connector. The lower 6 bits of port B, PB[5-0], select the several registers and memory devices on the module. Port A, configured as a bi-directional port, drives U71, a 74LS245 which connects to the 8-bit internal data bus of the module, PA[7-0]B. PA[7-0]B serves as the data pathway over the entire module.

The PB[5-3] bits drive the binary select inputs of U65, a 74LS138 1-of-8 decoder. PC2 drives the enable input of the same IC. The outputs of U65 serve as timed strobes in selecting registers and memory on the module. They are listed individually in Table 13.

Four outputs drive the enable input of other decoders. /LCSTB drives U27, a 74LS138 on sheet 11 of the schematic, which selects the counter input registers (/CnCLD). /MSKSTB drives the enable input of U72, another 74LS138, which uses PB[2-0] to select one of the module RAM write enable strobes or /AMACLR as shown in Table 14. /AMISTB drives the enable input of U38B, one half of a 74LS139 dual 1-of-4 decoder, which uses PB1-0] to select the AM[] bus byte enable strobes as shown in Table 15. /QALSTB drives the enable input of the other half of the 74LS139, U38A, which with PB[1-0], generate the write enable strobes for the Edge Qualifier Memory as shown in Table 16. U80, a 74LS175 latch, is the module mode register loaded and cleared by /MODSTB and /MODCLR, respectively. The inputs to the 4-bit latch are driven by the PA[3-0]B bus.

Table 13. Register/RAM Timed Strobes

PB 543	Output	Function
000	/LCSTB	Load Counter Strobe
001	/SCRW	Sequence Control Memory Write Enable
010	/MSKSTB	State Mask Memory Write Timing Strobe
011	/AMISTB	Acquisition Memory Multiplexer Timing Strobe
100	/QALSTB	Edge Qualifier Memory Write Timing Strobe
101	/MINDEX	Manual Index Command
110	/MODSTB	Module Mode Latch Load Strobe
111	/MODCLR	Module Mode Latch Clear

Table 14. /MSKSTB Outputs.

Port B Bits 2->0

PB 210	Output	PB 210	Output
000	/M0WE	100	/M12WE
001	/M4WE	101	/M16WE
010	/M8WE	110	/M20WE
011	/QUWE	111	/AMACLR

/AMACLR — Clear Memory Address

Table 15. /AMISTB Outputs.

Port B Bit 1&0

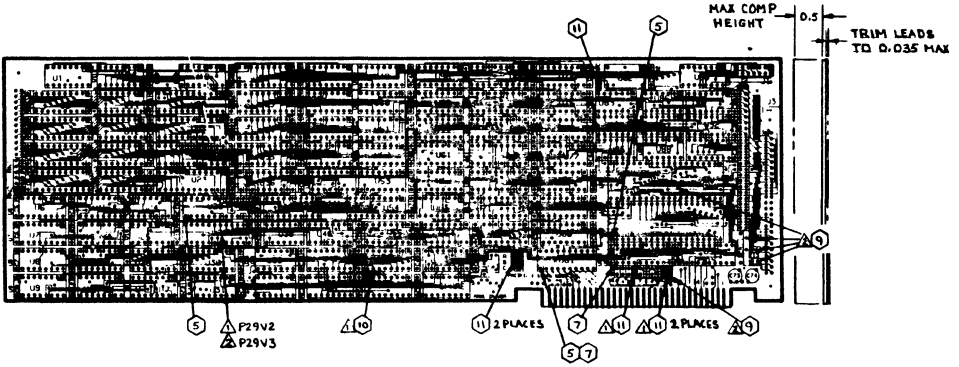
PB 10	Output
00	/AMI0
01	/AMI8
10	/AMI16
11	/AMI24

Table 16. /QALSTB Outputs.

PB 10	Output
00	/Q0WE
01	/Q4WE
10	/Q8WE
11	/QCWE

The module clock control logic is shown on sheet 1 of the schematic. U82, a 10.000MHz hybrid clock oscillator, is the source of the internal "run" clock for the module. Whenever the signal FCR is high, C10MC is gated to /SCLK via the AND/OR gates U83A, U83B and U87B. The buffered clocks SCLK1B, SCLK2B and SCLK3B are derived from /SCLK. If FCR is low, PC0 becomes the clock source for the module. The host generates SCLKs by toggling 8255 output PC0. FCR is the output from the D-type Flip Flop U84A. The FF is cleared by /RESET, selecting PC0 as SCLK. C10MC is selected by PC1. If the signals /INDXEND or SCREND become active, FCR is set LOW on the next SCLK.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
⚠ D	ADD C76 TO PED-4001-110 ADD DASH NUM & REV LET. COMPLETE REDRAW	3/13/87	

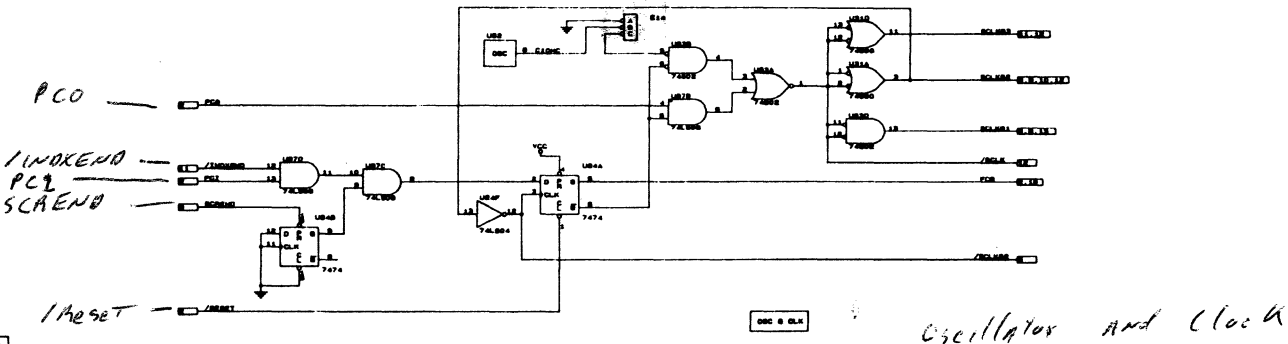


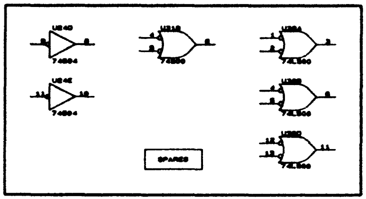
NOTE:

1. ASSEMBLE PER WSM04000
2. COMPONENT SIDE SHOWN
3. COMPONENTS IDENTIFIED BY REFERENCE DESIGNATOR IN MATERIAL LIST ML400100
4. OBSERVE ORIENTATION ON ALL ICS AND SOCKETS. PIN 1 IDENTIFIED BY SQUARE PAD
5. COMPONENT PIN 1 ORIENTATED AT LOWER LEFT
6. OBSERVE POLARITY ON CAPACITORS C73 THRU C75 AND DIODE CR1
7. SOCKETTED COMPONENT
8. IC COMPONENTS ARE ELECTROSTATIC SENSITIVE. ALL HANDLING, ASSEMBLY, TEST OPERATIONS TO BE DONE AT PROTECTED WORK STATION
9. ⚠ COMPONENTS C72, C75, CR1, E3-E12, E13 AND U94 OMITTED. COMPONENT HOLES TO BE CLEAR OF SOLDER.
10. ⚠ C76 LOCATED ON COMPONENT SIDE BETWEEN U57 PIN 7 AND U57 PIN 8, TWO LEADS PER HOLE
11. CONNECTOR SHUNT (ITEM 63) INSTALLED
12. PART DASH NUM, REV LETTER AND SERIAL NUMBER IN BLACK INK, CLEARLY LEGIBLE
13. ASSEMBLY SHALL BE TESTED PER TS400125
14. REFERENCE SCHEMATIC SD400100

⚠ PED-4001-110 ONLY
⚠ PED-4001-120 ONLY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: FRACTIONS ±1/64, ANGLES ±1°		PACIFIC ELECTRO DATA, INC.
APPROVALS	DATE	MODULE ASSEMBLY, DATA ACQUISITION AND EMULATION
DRAWN: T. KELLEY	3/13/87	
CHECKED:		SIZE C — DRAWING NO AD400100
		DO NOT SCALE DRAWING — SHEET 1 OF 1





SHEET	REV	DESCRIPTION	DATE	APPROVED
ALL	0	PRODUCTION RLSE	3/8/87	

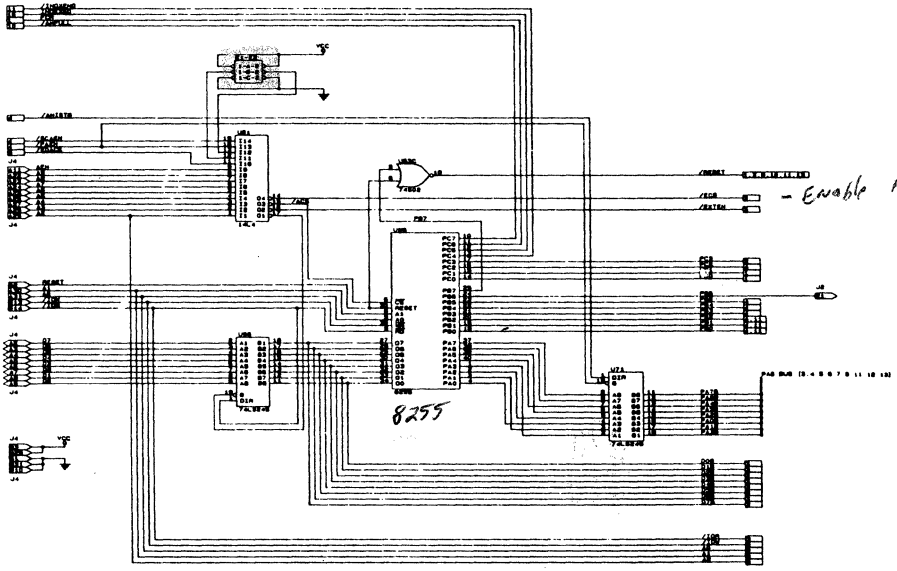
PACIFIC ELECTRO DATA
14 HUGHES ST.
SUITE B000
IRVINE, CAL. 92718

TITLE
DATA ACQUISITION AND EMULATION MODULE

SIZE	DOCUMENT NUMBER	REV
C	50400100	0

VOLTAGE & GROUND PINS

VCC	GND	COMPONENT
16	8	U1, U3–U18, U25, U27, U29, U41–U53, U55–U66, U73–U86, U90–U93
20	10	U2–U8, U28–U37, U54, U58–U71, U21, U88, U89
24	12	U30–U32, U38, U39
14	7	U24, U26, U31, U38–U40, U82–U89
+	-	C1 thru C78

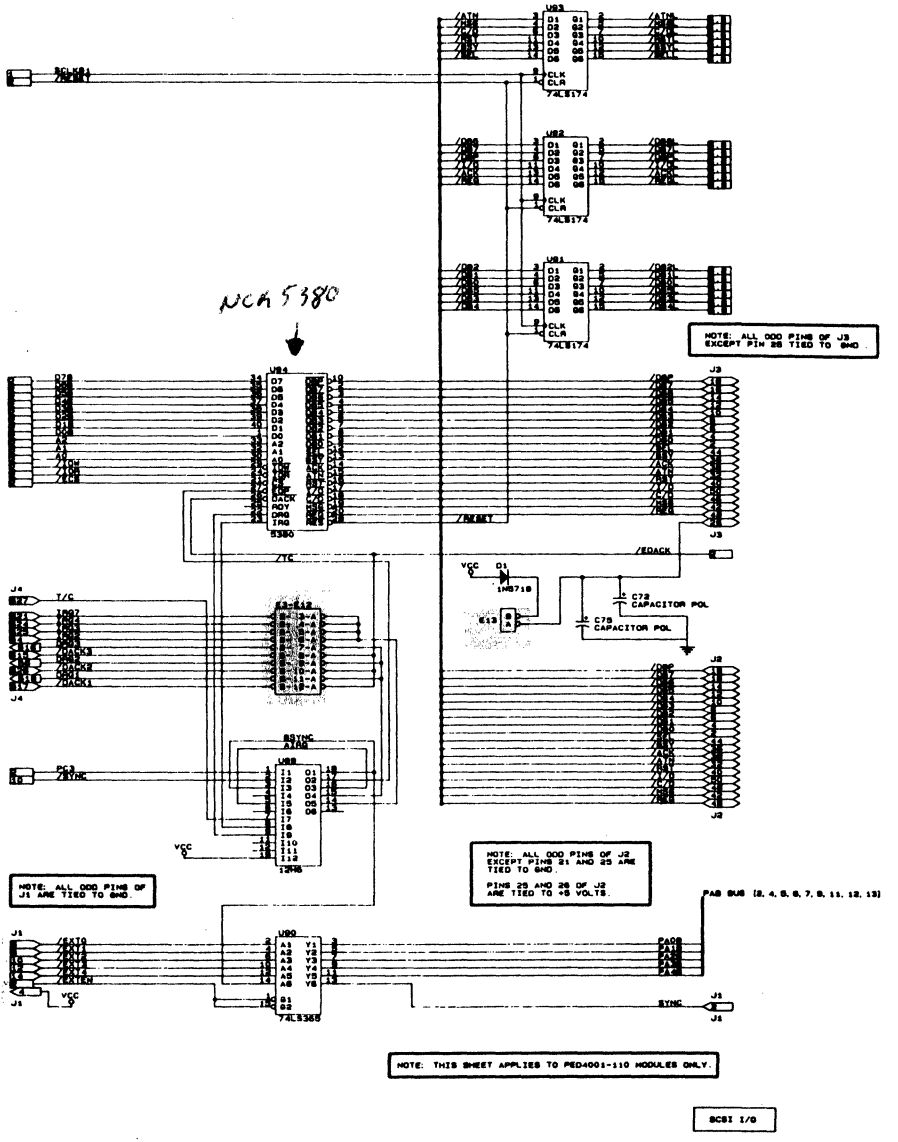


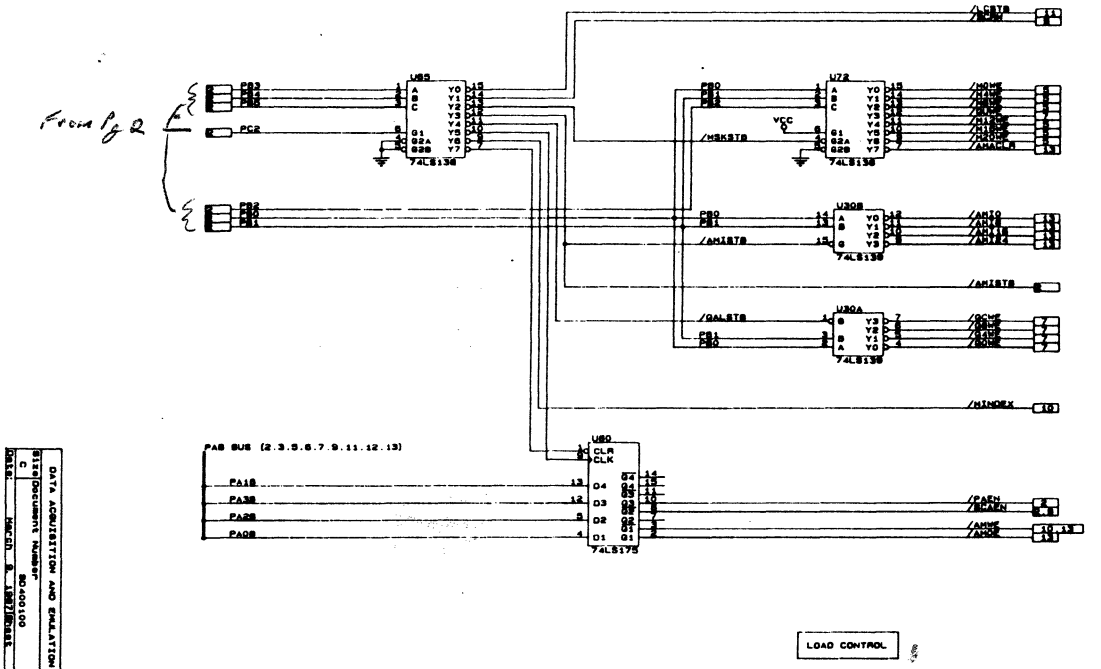
- Enable for NCR 538

HOST I/O

Host I/O

DATA ACQUISITION AND EMULATION MODULE

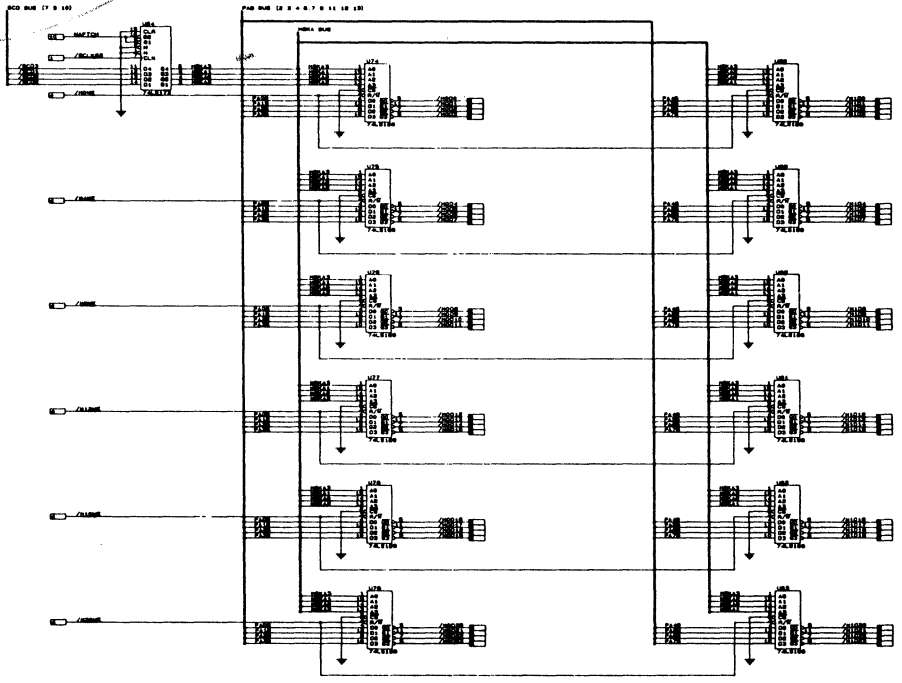

NCR 5380
NOTE: ALL ODD PINS OF J3 EXCEPT PIN 26 TIED TO GND.
NOTE: ALL ODD PINS OF J2 EXCEPT PINS 21 AND 25 ARE TIED TO GND.
PINS 25 AND 26 OF J2 ARE TIED TO +5 VOLTS.
NOTE: ALL ODD PINS OF J1 ARE TIED TO GND.
NOTE: THIS SHEET APPLIES TO PED4001-110 MODULES ONLY.
SCSI I/O
DATA ACQUISITION AND EMULATION MODULE
Size C
Document Number 90400100
REV D
Date: March 6, 1987 Sheet 3 of 10



DATA ACQUISITION AND EVALUATION MODULE

Size C | Document Number 8040100 | Rev D

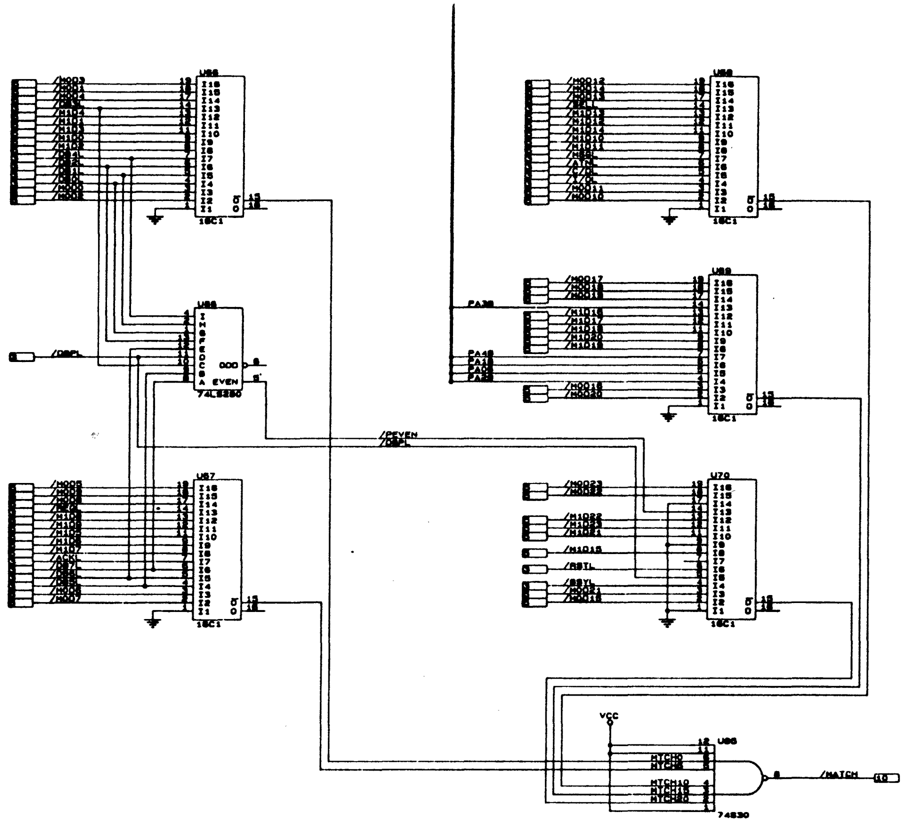
Date: MARCH 8, 1983 | Sheet 4 of 16



STATE MASK memory

STATE MASK MEMORY

DATA ACQUISITION AND EMULATION MODULE		
Size	Document Number	REV
C	80480150	D
Date: MARCH 6, 1987 Sheet 5 of 14		

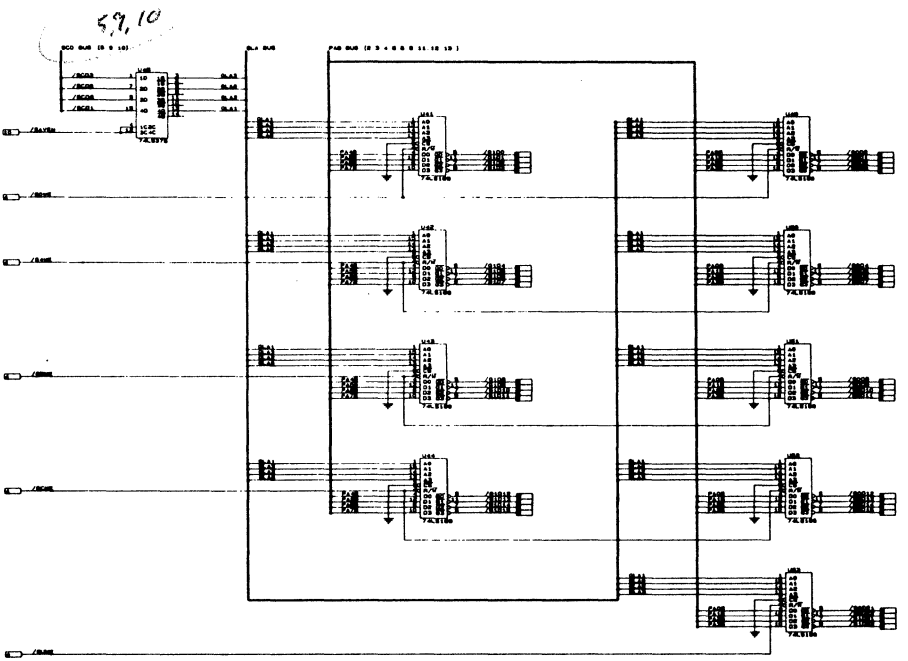


DATA ACQUISITION AND EMULATION MODULE

Size C | Document Number 8D400100 | REV D

Date: March 8, 1987 | Sheet 8 of 14

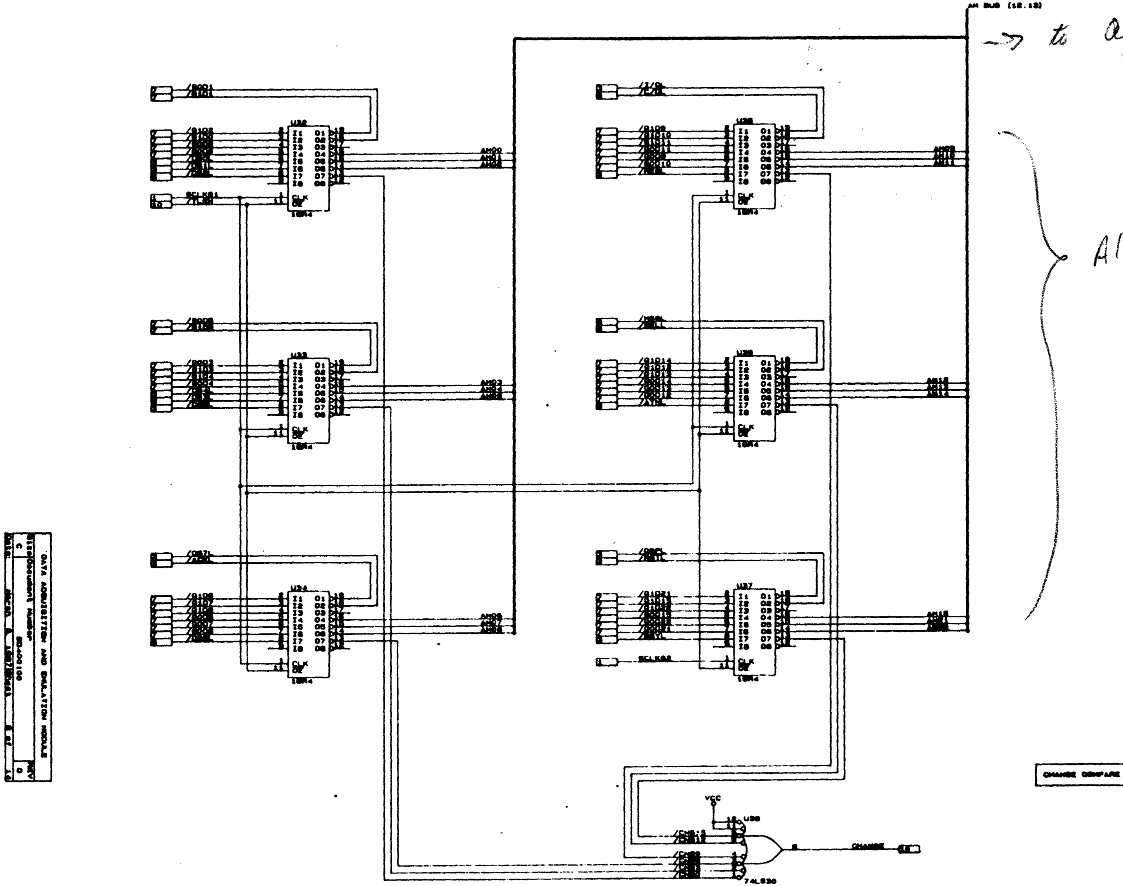
STATE COMPARE



EDGE QUALIFIER MEMORY

DATA ACQUISITION AND EMULATION MODULE

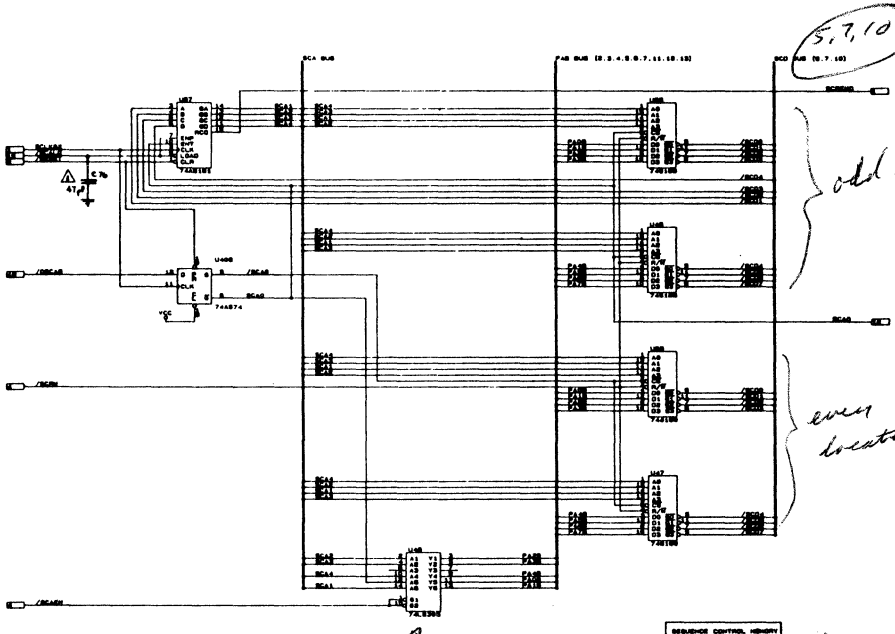
Edge qualifier Memory



→ to Aquistion mem

All PAL

change c



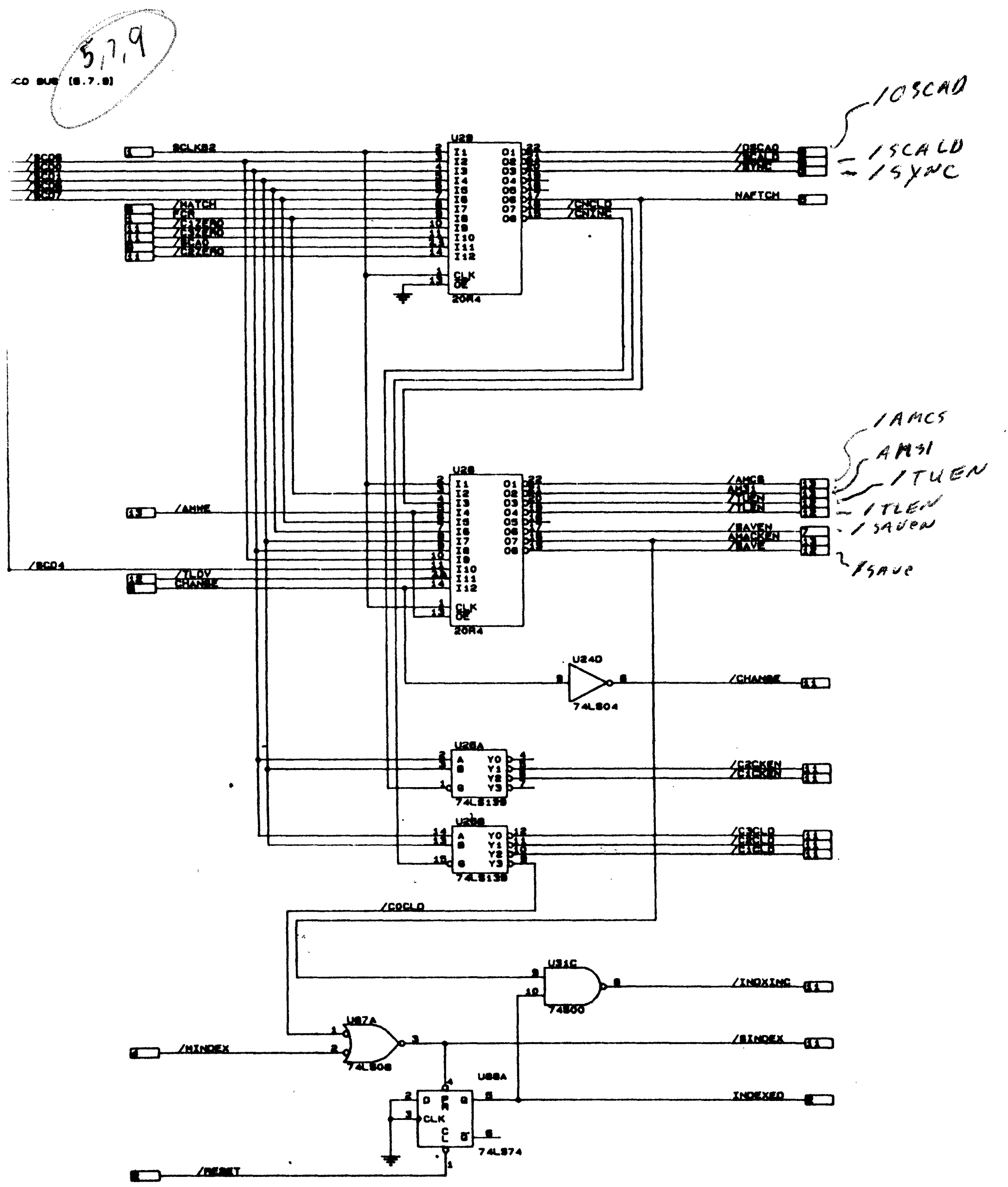
For Trace option to store the program address in the EXT. bits of the aquisition memory

Sequence Control Memory

⚠ PED4001-110 ONLY

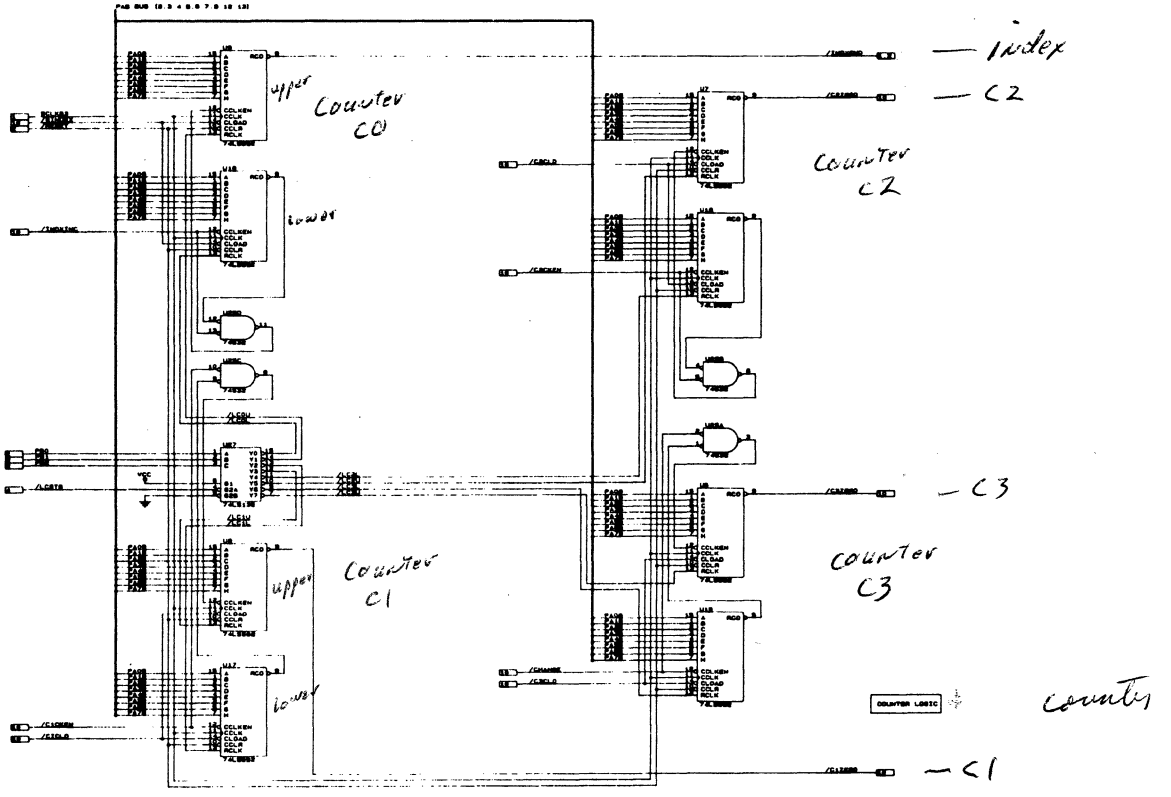
DATA ACQUISITION AND EMULATION MODULE

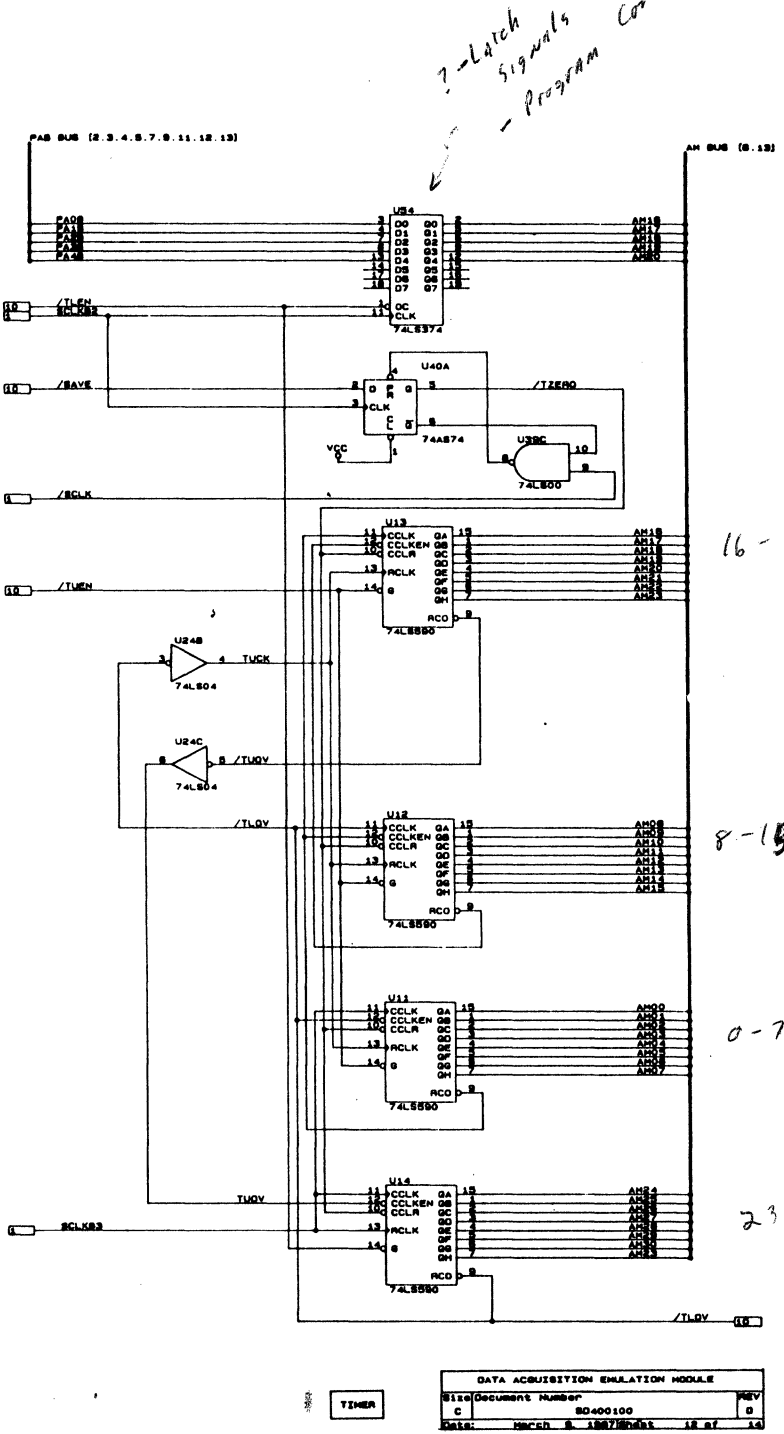
Size	Document Number	REV
C	62-400100	D

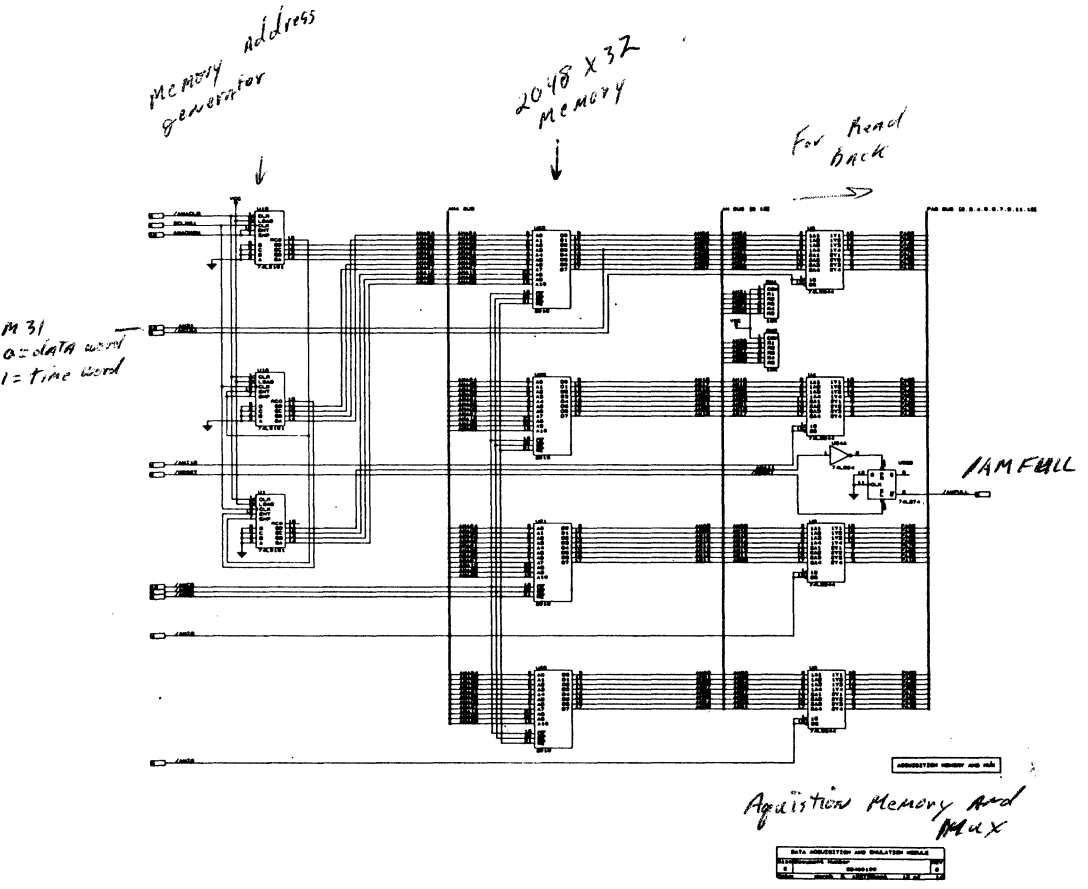


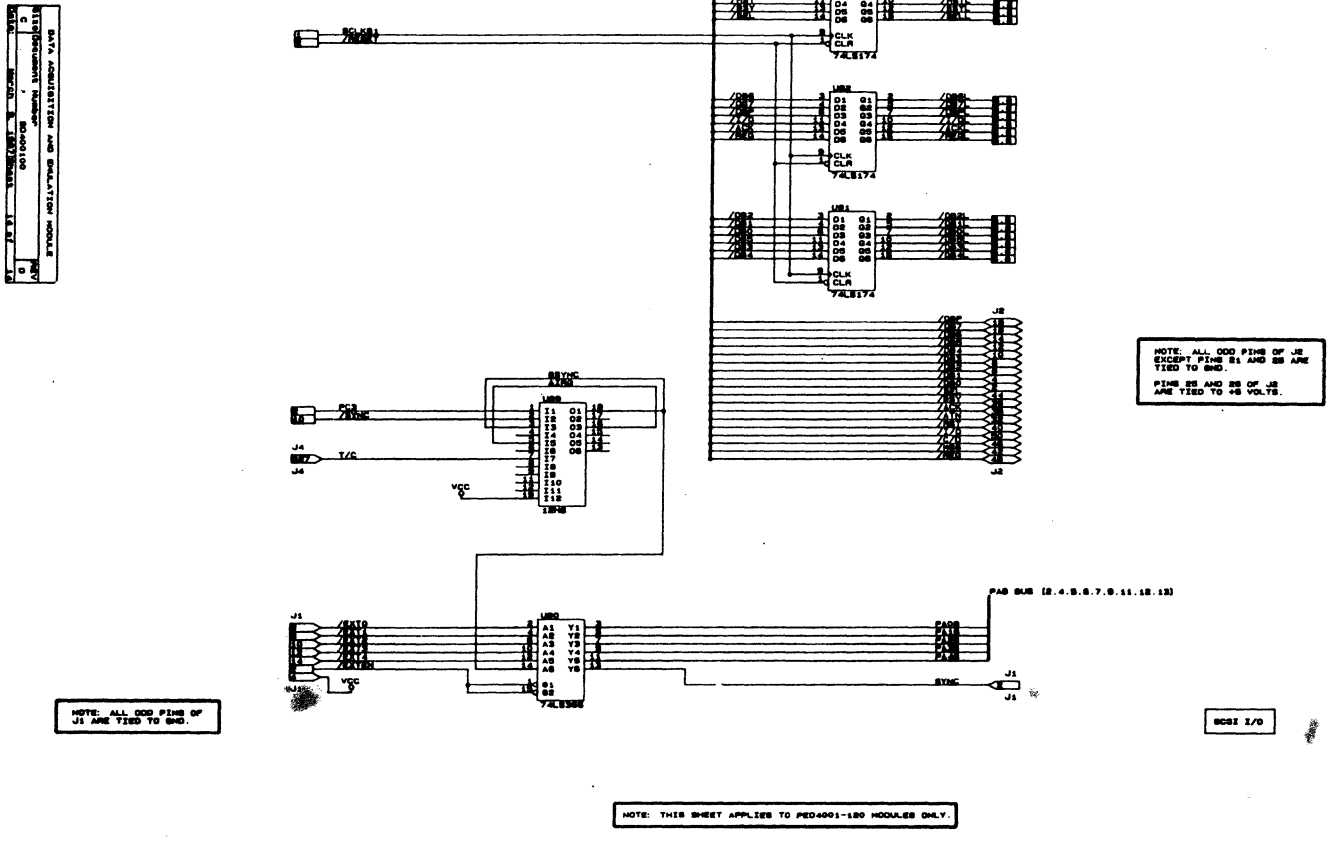
SEQUENCE CONTROL LOGIC

DATA ACQUISITION AND EMULATION MODULE		
Size	Document Number	REV
C	SD400100	D
Date: March 9, 1987	Sheet 10 of 14	


upper
Counter
C0
lower
upper
Counter
C1
lower
Counter
C2
Counter
C3
index
C2
C3
C1
COUNTER LOGIC
counter


PAB BUS (2.3.4.5.7.9.11.12.13)
AM BUS (0.13)
U64
74LS374
/TLEN
/SAVE
U40A
74AS74
/TZERO
U39C
74LS00
/SCLK
U13
74LS550
/TWEN
U24B
74LS04
TUCK
U24C
/TUOV
/TLOV
U12
U11
U14
TUOV
SCLK83
/TLOV
16 - 23
8 - 15
0 - 7
23 - 30
100NS
TIMER
DATA ACQUISITION EMULATION MODULE
Size C
Document Number 80400100
REV B
Date: March 8, 1987
Sheet 12 of 14


Memory Address generator
2048 X 32 Memory
For Read Back
M 31
0 = data word
1 = time word
IAM FULL
Aquisition Memory And Mux


DATA ACQUISITION AND EMULATION MODULE
SCSI I/O
NOTE: ALL ODD PINS OF J2 EXCEPT PINS 21 AND 25 ARE TIED TO GND.
PINS 25 AND 25 OF J2 ARE TIED TO +5 VOLTS.
NOTE: ALL ODD PINS OF J1 ARE TIED TO GND.
NOTE: THIS SHEET APPLIES TO PED4001-120 MODULES ONLY.

APPENDIX B. MODULE PARTS LIST.

Table B-1 includes all components and parts making up the PED-4001 Dat Analyzer Module. Parts are listed by item type, item description, manufacturer, schematic reference number, and quantity.

Table B-1. Parts List.

ITEM	DESCRIPTION	MFG	NOTE	REFERENCE	QUAN
1	IC, 74S00	TI		U31	1
2	IC, 74LS00	TI		U39	1
3	IC, 74S02	TI		U83	1
4	IC, 74LS04	TI		U24	1
5	IC, 74LS08	TI		U87	1
6	IC, 74S30	TI		U85, U38	2
7	IC, 74S32	TI		U25	1
8	IC, 7474	TI		U84	1
9	IC, 74AS74	TI		U40	1
10	IC, 74LS74A	TI		U88	2
11	IC, 74LS138	TI		U27, U65, U72	3
12	IC, 74LS139	TI		U26, U30	2
13	IC, 74AS161	TI		U57	1
14	IC, 74LS161A	TI		U1, U10, U19	3
15	IC, 74LS173A	TI		U64	1
16	IC, 74LS174	TI		U91-U93	3
17	IC, 74LS175	TI		U80	1
18	IC, 74LS189A	TI		U41-U44,U49-U53 U58-U63,U74-U79	21
19	IC, 74S189B	TI		U46,U47,U55,U56	4
20	IC, 74LS244	TI		U2-U5	4
21	IC, 74LS245	TI		U71, U96	2
22	IC, 74S280	TI		U86	1
23	IC, 74LS365	TI		U90, U48	2
24	IC, 74LS374	TI		U54	1
25	IC, 74LS375	TI		U45	1
26	IC, 74LS590	TI		U11-U14	4
27	IC, 74LS592	TI		U6-U9, U15-U18	8
28	IC, 18255A-5	INT	UPD8255AC5	U95	1
29	IC, P28V0	PED	M/F PAL20R4BS	U28	1
30	IC, P29V2	PED	M/F PAL20R4BS	U29	1
31	IC, P32V0	PED	M/F PAL16R4A-2	U32	1
32	IC, P33V0	PED	M/F PAL16R4A-2	U33	1
33	IC, P34V0	PED	M/F PAL16R4A-2	U34	1

Table B-1. Parts List (Continued).

ITEM	DESCRIPTION	MFG	NOTE	REFERENCE	QUAN
34	IC, P35V0	PED	M/F PAL16R4A-2	U35	1
35	IC, P36V0	PED	M/F PAL16R4A-2	U36	1
36	IC, P37V0	PED	M/F PAL16R4A-2	U37	1
37	IC, P66V0	PED	M/F PAL16C1	U66	1
38	IC, P67V0	PED	M/F PAL16C1	U67	1
39	IC, P68V0	PED	M/F PAL16C1	U68	1
40	IC, P69V0	PED	M/F PAL16C1	U69	1
41	IC, P70V0	PED	M/F PAL16C1	U70	1
42	IC, P81V1	PED	M/F PAL14L4-2	U81	1
43	IC, P89V1E	PED	M/F PAL12H6-2	U89	1
44	IC, TMM2018D-45	THB		U20-U23	4
45	IC, NCR5380	NCR		U94	1
46	Osc, TTL, 10Mhz, 100ppm		OSC10.000	U82	1
47	Diode	MOT		CR1	1
48	Cap, mono, 0.1uF 50V, .3 mil	AVX	SR275E104ZAA	C1-C72	72
49	Cap, mono, 47pF 50V, .1 mil	AVX	SA151A470KAA	C76	1
50	Cap, tantalum 150uF, 10V	SPG	196D157X9010TE4	C73, C74	2
51	Cap, tantalum 33uF, 10V	ITT	TAPS33K10	C75	1
52	Network 5 resistor, 10K	CTS	770-61-R10K	RN1, RN2	2
53	Socket, High Rel 20 pin			X81, X89	1
54	Header, 3 x 2 gold pin	CA	CA-D06-23B-43	E1-E2	1
55	Header, 7 x 2 gold pin	CA	CA-D14-23B-43	J1	1
56	Header, 10 x 2 gold pin	CA	CA-D20-23B-43	E3-E12	10
57	Header, 2 x 1 gold pin	CA	CA-S02-23B-43	E13	1

Table B-1. Parts List (Continued).

ITEM	DESCRIPTION	MFG	NOTE	REFERENCE	QUAN
58	Header, 4 x 1 gold pin	CA	CA-S04-23B-43X	E14	1
59	Header, 25 x 2 gold pin	CA	CA-D50-23B-43	J2	1
60	Connector, RT 50 pin	CA	CA50HR-1BSR	J3	1
61	Jumper, Shorting Header	CA	CA02SJ-OPEN-B		7
62	PCB, PED4001-100	PED			1

Manufacturers Codes:

AGT	Augat Inc.	MOT	Motorola Semiconductor
AVX	AVX	NCR	NCR Microelectronics
BRN	Bourns	PED	Pacific Electro Data
CA	Circuit Assemblies	SPG	Sprague Electronics
CTS	CTS Inc.	THB	Toshiba Electronics
INT	Intel Semiconductor	TI	Texas Instruments
ITT	ITT Electronics		

APPENDIX C. GLOSSARY OF KEY STATE ANALYZER SIGNALS

Table C-1 provides a list of key signals used in the PED-4001 module. Sources and descriptions of each signal are given.

Table C-1. Glossary of Key Signals.

NAME	SOURCE	DESCRIPTION
/ACKL	U92p12	Sampled /ACK
/ACK	J2p38	SCSI Data Acknowledge
AEN	J3pA11	Host Address Enable
AMACKEN	U28p16	Increments AMA register
/AMACLR	U72p7	Clears AMA register to 0000h
AMA[11-0]	U1,U10,U19	Acquisition Memory Address Register Output
/AMCS	U28p22	Acquisition Memory (AM) Chip Select
/AMFULL	U88p8	All locations of AM have been written once
/AMI0	U30p12	Puts AM[7-0] on PAB bus
/AMI16	U30p10	Puts AM[23-16] on PAB bus
/AMI24	U30p9	Puts AM[31-24] on PAB bus
/AMI8	U30p11	Puts AM[15-8] on PAB bus
/AMISTB	U65p12	AM[] to PA[]B strobe
/AMOE	U80p2	Acquisition Memory Output Enable - to AM bus
/AMWE	U80p3	Acquisition Memory Write Enable
AM[31-00]	bus	Acquisition Memory Data Bus
/ATNL	U93p2	Sampled /ATN

Table C-1. Glossary of Key Signals (continued).

NAME	SOURCE	DESCRIPTION
/ATN	J2p32	SCSI Attention Control
A[9-0]	J3pA[22-31]	Host Address Bus (10 bits)
/BSYL	U93p12	Sampled /BSY
/BSY	J2p36	SCSI Busy Control
/COCLD	U26p9	Load counter C0 from latch
/C1CKEN	U26p6	Enable clock of counter C1
/C1CLD	U26p10	Load counter C1 from latch
/C1ZERO	U8p9	Counter C1 at maximum count FF00h
/C2CKEN	U26p5	Enable clock of counter C2
/C2CLD	U26p11	Load counter C2 from latch
/C2ZERO	U7p9	Counter C2 at maximum count FF00h
/C3CLD	U26p12	Load counter C3 from latch
/C3ZERO	U6p9	Counter C3 at maximum count FF00h
/CHANGE	U38p8	Qualified Edge detected
/CNCLD	U29p16	Load selected counter 'n' from its input latch
/CNG0	U32p13	Qualified Edge detected, bits 0-2
/CNG12	U36p13	Qualified Edge detected, bits 12-14
/CNG15	U37p13	Qualified Edge detected, bits 15,21,22
/CNG3	U33p13	Qualified Edge detected, bits 3-5
/CNG5	U34p13	Qualified Edge detected, bits 6-8
/CNG9	U35p13	Qualified Edge detected, bits 9-11
/CNINC	U29p15	Increment selected counter 'n'

Table C-1. Glossary of Key Signals (continued).

NAME	SOURCE	DESCRIPTION
/C/DL	U93p7	Sampled /Command/Data
/C/D	J92p7	SCSI Command/Data Control
DBPL	U92p7	Sampled SCSI Data Parity bit
/DBP	J2p18	SCSI Data Parity bit
/DB[7-0]L	U91, U92	Sampled SCSI Data bus (8 bits)
/DB[7-0]	J2p[16-2]	SCSI Data bus (8 bits) even pins ONLY
/DSCAO	U29p22	Next state of SCA bit 0
D[7-0]	J3pA[2-9]	Host Data Bus (8 bits)
D[7-0]B	Bus	Internal Host Data Bus (8 bits)
/EXT[4-0]	J1p[12-4]	External TTL inputs (5 bits) even pins ONLY
FCR	U84p5	Fast Clock Running - 10 Mhz SCLK when FCR is HIGH
/FUEN	U28p18	Enable AMA increment at upper stage timer save
/INDEXED	U88p5	Module has been indexed
/INDXEND	U9p9	Counter C0 (index counter) at maximum count FF00
/INDXINC	U31pB14	Index counter (C0) clock enable
/IOR	J3pB14	Host I/O Read
/IOW	J3pB13	Host I/O Write
/I/OL	U92p10	Sampled /I/O
/I/O	J2p50	SCSI Input/Output Control
/LCSTB	U65p15	Counter Input latch strobe
/MOD[23-0]	U79-U74	State Mask '0' Memory (24 bits)

Table C-1. Glossary of Key Signals (continued).

NAME	SOURCE	DESCRIPTION
/MOWE	U72p15	MxD[3-0] Memory Write Enable (x: 0,1)
/MO	U29p18	
/M12WE	U72p11	MxD[15-12] Memory Write Enable (x: 0,1)
/M16WE	U72p10	MxD[19-16] Memory Write Enable (x: 0,1)
/M1D[23-0]	U63-U58	State Mask '1' Memory (24 bits)
/M1	U29p19	
/M20WE	U72p9	MxD[23-20] Memory Write Enable (x: 0,1)
/M4WE	U72p14	MxD[7-4] Memory Write Enable (x: 0,1)
/M8WE	U72p13	MxD[11-8] Memory Write Enable (x: 0,1)
MATCH	U85p8	Data and State Mask Match, all bits
/MINDEX	U65p9	Manual Index
/MODCLR	U65p7	Mode Latch Clear
/MSGL	U93p5	Sampled /MSG
/MSG	J2p42	SCSI Message Control
MSKA[3-0]	U64	State Mask Memory Address (4 bits)
/MSKSTB	U65p13	State Mask Memory write enable strobe
/MTCH0	U66p15	Data and State Mask Match, bits 0-4
/MTCH10	U68p15	Data and State Mask Match, bits 10-14
/MTCH15	U69p15	Data and State Mask Match, bits 16-20
/MTCH20	U70p15	Data and State Mask Match, bits 15, 21, 22

Table C-1. Glossary of Key Signals (continued).

NAME	SOURCE	DESCRIPTION
/MTCH5	U67p15	Data and State Mask Match, bits 6-9
NAFTCH	U29p17	Next Address Fetch cycle
/PAEN	U80p10	PA[7-0] to PA[7-0]B Enable
PA[7-0]B	bus	Module internal 8-bit data bus
PB6	U95p24	Differential SCSI select
PB7	U95p25	Module software reset
PB[5-0]	U95[23-18]	Module Register Address/Select
PC0	U95p14	System Clock external source
PC1	U95p15	System Clock Select - 10 Mhz if HIGH, else PC0
PC2	U95p16	Module Register Strobe
PC3	U95p17	
/PEVEN	U86p5	Even parity on sampled SCSI data bus
/QOD[15-0]	U52-U49	Edge Qualifier "negative edge" Memory (16 bits)
/QOD[21,22]	U53	Edge Qualifier "negative edge" Memory (2 bits)
/QOWE	U30p4	QxD[3-0] Memory write enable (x: 0,1) \018
/Q1D[15-0]	U44-U41	Edge Qualifier "positive edge" Memory (16 bits)
/Q1D[21,22]	U53	Edge Qualifier "positive edge" Memory (2 bits)
/Q4WE	U30p5	QxD[7-4] Memory write enable (x: 0,1)
/Q8WE	U30p6	QxD[11-8] Memory write enable (x: 0,1)

Table C-1. Glossary of Key Signals (continued).

NAME	SOURCE	DESCRIPTION
/QALSTB	U65p11	Edge Qualifier Memory write enable strobe
/QCWE	U30p7	QxD[15-12] Memory write enable (x: 0,1)
/QLA[3-0]	U45	Edge Qualifier Memory Address (4 bits)
/QUWE	U92p12	QxD[22,21] Memory write enable (x: 0,1)
/REQL	U92p15	Sampled /REQ
/REQ	J2p48	SCSI Data Request
RESET	J3pB2	Host RESET
/RESET	U83p10	NOR of RESET and PB7
/RSTL	U93p10	Sampled /RST
/RST	J2p40	SCSI Reset Control
/SAVEN	U28p17	Save state in AM on all CHANGEs
/SAVE	U28p15	Save state data and lower timer in AM
SCA0	U40p9	SCA bit 0 - Selects even bytes of SC memory
/SCA0	U40p8	/SCA[0] - Selects odd bytes of SC memory
/SCAEN	U80p6	SCA[4-0] to PA[4-0]B Enable
/SCALD	U29p21	Load SCA register from SCD[4-0] (i.e. use jump)
SCA[4-1]	U57	Sequence Controller Memory Address, bits 1-4
/SCD[3-0]	U55, U56	Sequence Controller Memory, lower nibble (4 bits)

Table C-1. Glossary of Key Signals (continued).

NAME	SOURCE	DESCRIPTION
/SCD[7-4]	U46, U47	Sequence Controller Memory, upper nibble (4 bits)
SCLK2	U31p3	System Clock from Buffer 2
SCLKB1	U83p13	System Clock from Buffer 1
/SCLKB2	U24p12	Inverted System Clock from Buffer 2
SCLKB3	U31p11	System Clock from Buffer 3
/SCLK	U83p1	Inverted System Clock
/SCREND	U57p15	Sequence Controller Memory at Maximum Address, 1
/SCRW	U65p14	Sequence Controller Memory Write Enable Strobe
/SELL	U93p15	Sampled /SEL
/SEL	J2p44	SCSI Select Control
/SINDEX	U87p3	Set Index counter - transfer input register to count
/SYNC	U29p20	Synchronization Pulse Output
/TLEN	U28p19	Enable state data and lower timer to AM[30-0]
/TLV	U14p9	Lower timer stage at maximum count, FFh
TUCK	U24p4	Upper Timer Clock
/TUEN	U28p20	Enable upper stage of timer to AM[23-0]
/TUOV	U24p6	Upper Timer at maximum count, FFFFFF00h
/TZERO	U40p5	Clear Timer to zero