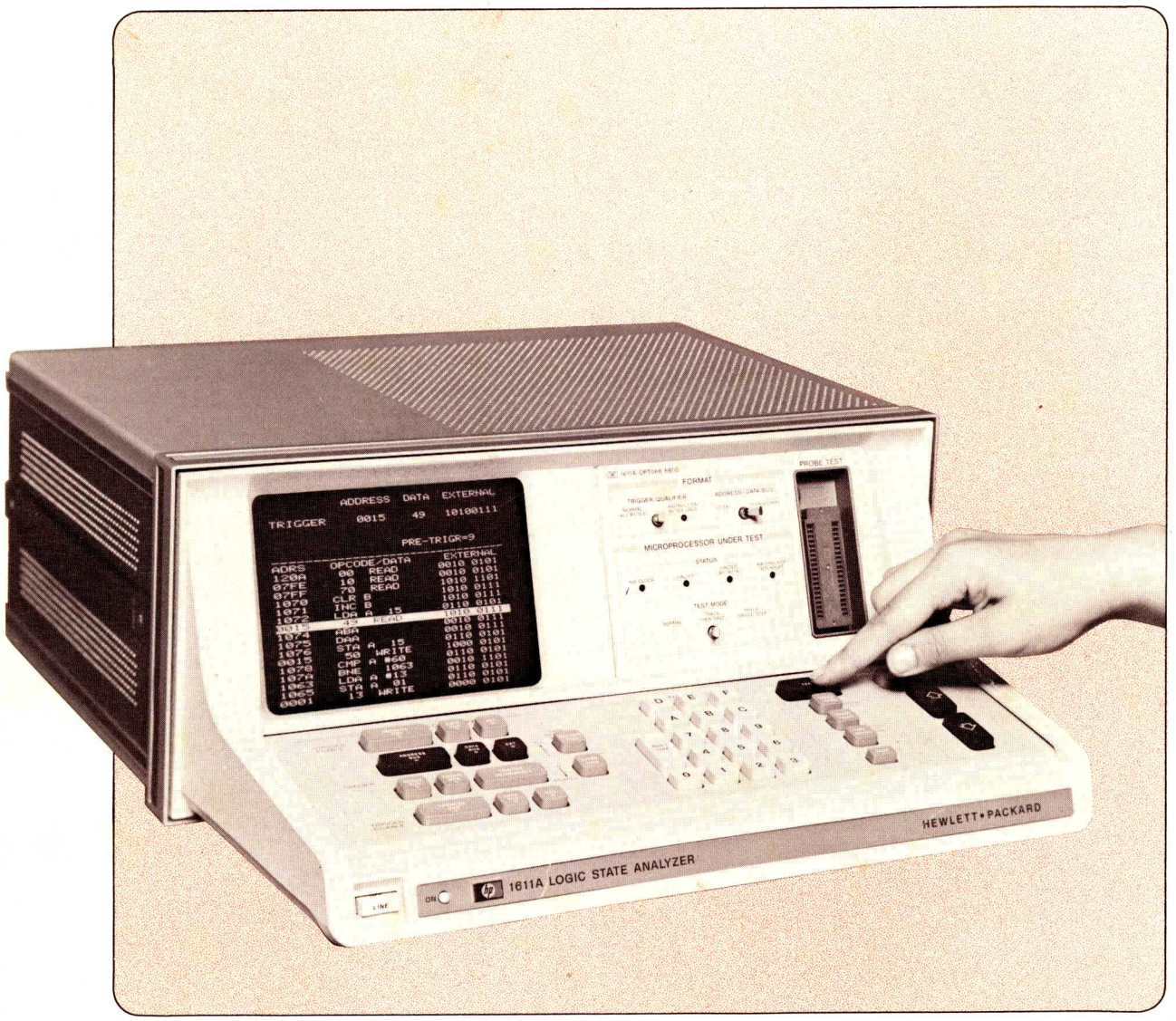
1611A LOGIC STATE ANALYZER



FIELD TRAINING MANUAL

HEWLETT hp PACKARD

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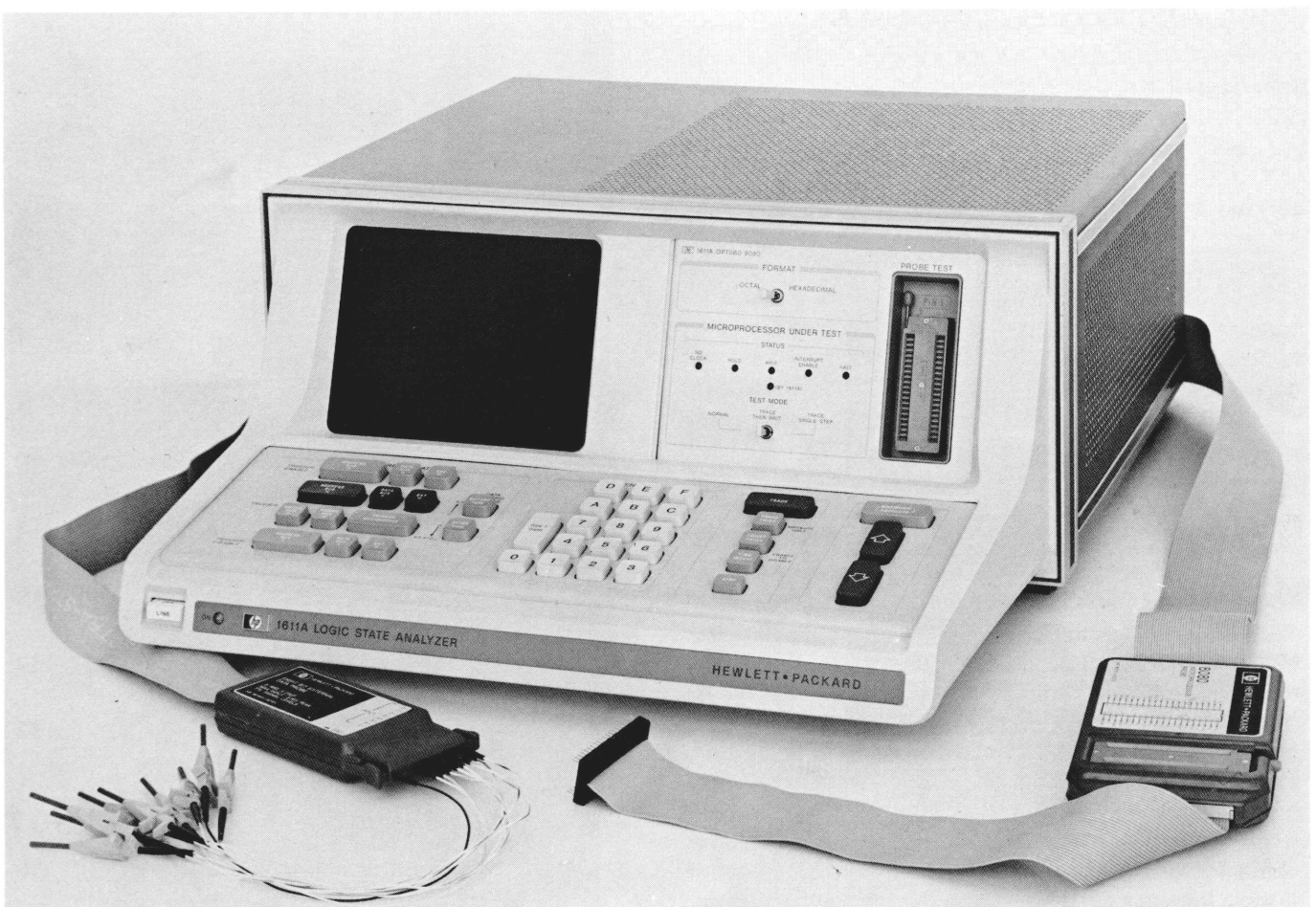
What the HP 1611A can do for your customer:

- **Provide more triggering capability than ever before possible**
- **Increase efficiency in solving microprocessor problems and systems debug**
- **Measure time intervals from point to point in his program**
- **Provide a display of program flow as he wrote it in mnemonic code**
- **Automatically code Address and Data in hexadecimal or octal**



INTRODUCTION

The 1611A is the first of a new generation of digital measurement instruments. It has an on board microprocessor which provides intelligence to simplify the controls and reduce setup and measurement errors. Instead of a bewildering array of knobs, pushbuttons and switches, most of the controls are located neatly on a keyboard and grouped together according to function. The instrument has self testing capabilities which make checks on its internal hardware and software.

It is a special purpose synchronous state analyzer designed specifically for use with microprocessors. At present there are two interchangeable options available: Option 080 for use with the Intel 8080A and 8080 plus second source versions and Option 068 for the Motorola 6800 and second source versions. Additional option modules can be added to the line in the future if the potential volume justifies the development cost.

Among the many measurement contributions offered by the 1611A, the most significant is the greatly expanded triggering capability. Other contributions include new measurement features such as trigger counting, time interval measurement, mnemonic display, and error messages to warn of improper operation or setup.

DISPLAY MODES

The 1611A has several different display modes which can be selected depending on the type of information required from the measurement.

TRACE

The most commonly used mode is Trace which is a line by line listing of the memory transactions or program flow and an information field which provides further descriptive information about the memory transaction. After a completed trace run the memory contains 64 bytes of data, 32 bits in length. The memory is viewed through a 16 line movable window (figure 1).

Trace display is interchangeable between either of two modes. The absolute mode displays the program address and the machine language op code or data (figure 2). In the mnemonic mode, the program address

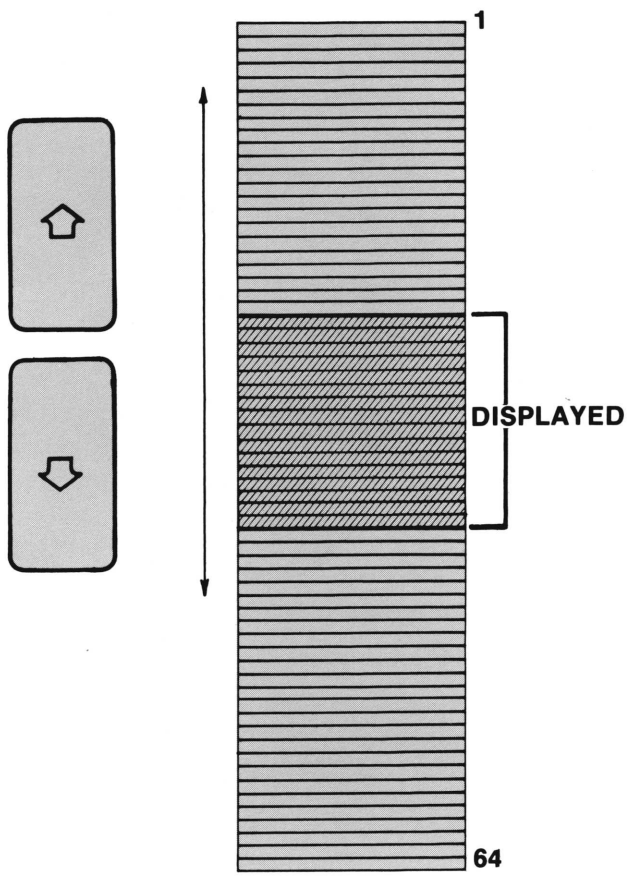


Figure 1. The 64-byte memory is viewed through a 16-byte window which is positioned with the "ROLL" keys.

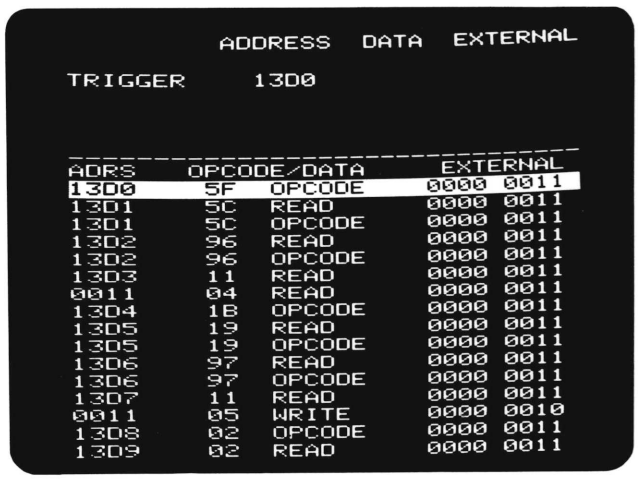


Figure 2. Absolute mode displays data or op codes in numeric format.

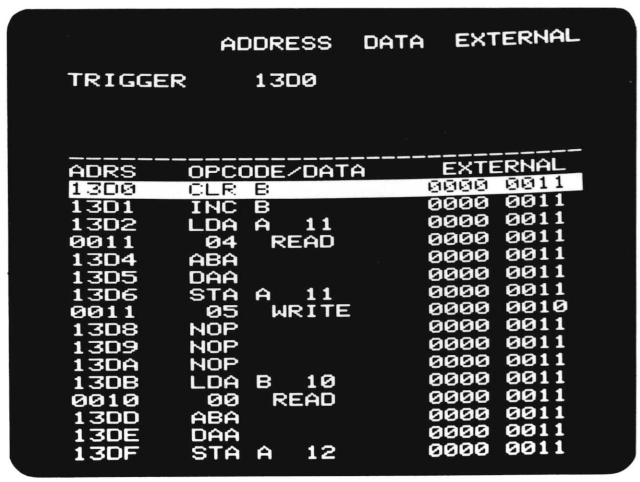


Figure 3. Display format may be switched to mnemonic for referencing the written program.

is displayed along with the assembly language mnemonic and 8 or 16 bit operand (figure 3). Either display mode is selectable and interchangeable in hexadecimal or octal format.

TRACE TRIGS

Trace Trigs display is a listing in the absolute mode of only those words that match the preselected trigger conditions (figure 4).

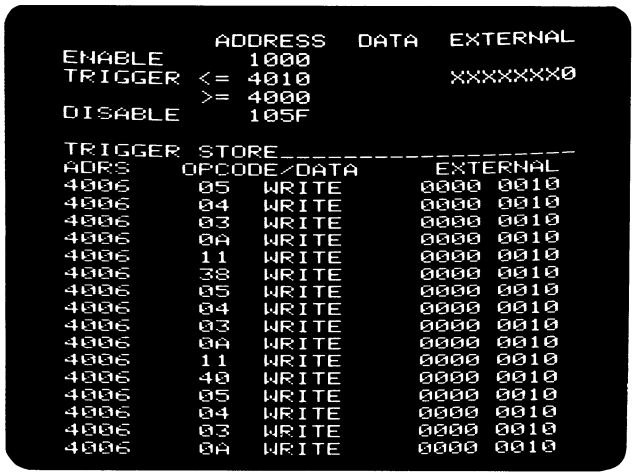


Figure 4. Trace Triggers mode provides a display of data that satisfies only the trigger conditions. In this photo, the External trigger of LSB 0 defined that only writes to a display would be captured.

COUNT TRIGS

Display is a decimal number equal to the number of trigger matches which occur between two selected points in the program. The count can be updated in real time (figure 5).

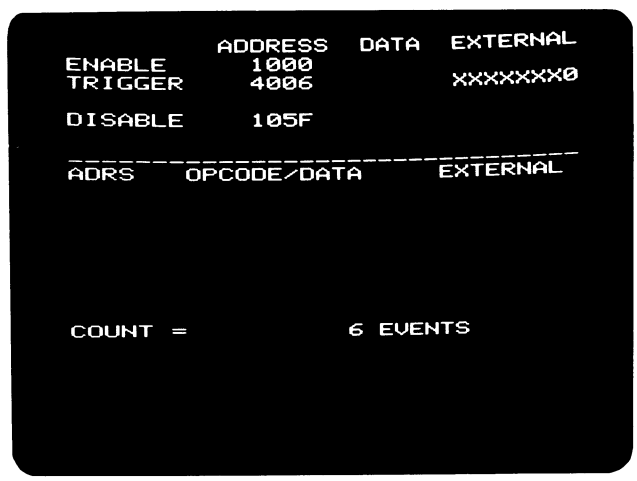


Figure 5. Count Triggers mode provides a measurement of the number of trigger events occurring between two program points. This photo shows that six trigger events (4006) occurred between the Enable and Disable points.

TIME INTERVAL

Time interval display is a single decimal number equal to the elapsed time between two selected points in the program (figure 6).

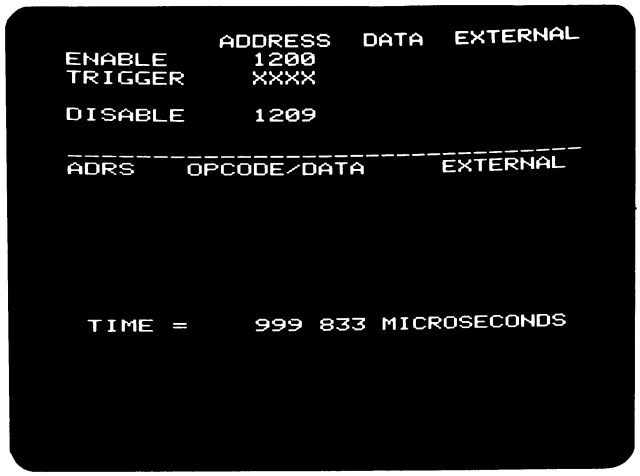


Figure 6. Time Interval mode counts the time between the trigger Enable and Disable points and directly displays the time in microseconds.

TRIGGERING

The 1611A makes its greatest contribution in the area of triggering capability which has been extended far beyond that of other instrumentation. With the 1611A it's possible to enter a trigger word of up to 24 bits in hex or octal plus an additional 8 bits in binary. The trigger word can then be qualified in a number of ways using additional trigger controls. For example, the trigger word may be enabled or disabled by another word or it may be recognized on the nth occurrence, $1 \leq n \leq 256$.

Another set of trigger controls (Address Bus$\geq$, Address Bus $\leq$) are used to allow trigger recognition on any occurrence $\geq$ or $\leq$ the preselected address. These two modes may be used together to define a band over which any address bus activity will be recognized.

WHY IS THE 1611A NEEDED?

The 1611A is a very powerful yet very specialized instrument. It is designed to serve a market consisting of those people engaged in design and development, debug, production test, or maintenance of systems using the 8080A or the 6800 microprocessors. Although the market may be quite narrow, it has considerable depth. The 8080A and the 6800 are the two most widely used microprocessors in the industry today. This is a market which is still in its infancy and is growing rapidly.

There are an abundance of microprocessor analyzers, emulators, and simulators now on the market. All of these systems can solve microprocessor problems in various ways but none contain as much measurement power in one instrument as the 1611A. The powerful triggering capability, mnemonic display, and time interval features can save hours of time over other measurement techniques.

TABLE I
FEATURES AND ADVANTAGES

1. On Board Microprocessor	Simplifies controls. Provides diagnostic and error messages, increases measurement power.
2. Trace Trigs	Very powerful display qualifier scheme which allows selective trace on data of interest while ignoring all else. For example all "write" instruction occurring in a range of memory can be captured and displayed.
3. 64 Byte Memory	Deeper memory provides larger window and allows looking back further in time before trig event.
4. Mnemonic Display	Allows operator to view code as written, saves time translating from machine language.
5. Hex/Octal	Operator can choose number system with which he is most comfortable or that used by his assembler.
6. Time Interval	Allows measurement of true time elapsed in subroutine or between any two states of interest.
7. Trigger Count	Operator can quickly obtain an accurate count of the occurrence of a word or words without resorting to calculation or hand counting from a code sheet. Allows optimization of code by determining where the processor spends most of its time.
8. Trigger Enable/Disable	Errors may occur only in one branch of program; Trigger search can be limited to area of interest.
9. Trigger Occurrence Counter	Now the user can select which transaction to observe in a multiple pass operation.
10. Address $\geq$ Address $\leq$	Often it is of interest to know if a program has gone into a forbidden area of memory and if so how it got there. These trigger functions substitute for the 1600A map in this respect.
11. Trig Out	Provides a method of obtaining a real time look at area of interest.
12. Trace Point Out	Provides a gate pulse which can be used by peripheral equipment to enable or inhibit activity during Trace. Can be used to generate an interrupt signal to the processor for a register dump.
13. Trace Single Step	Provides interaction with processor. Processor can be stepped through area of interest one operation at a time.
14. Self Test	No external equipment is needed to determine if the instrument is working properly.

PRINCIPLES OF OPERATION

The 1611A is a state analyzer which is synchronous with the ϕ_2 clock pulse of the microprocessor under test. The clock is internally qualified such that the instrument can look at an entire instruction cycle and clock in only the desired information (figure 7). The 32 bits are entered as 16 bits of address from the address bus followed by 16 bits from the data bus and uncommitted external lines. Data is clocked in until the memory is full and the trigger and delay conditions have been met or the capture is halted. The capture memory then becomes the display memory until a new Execute function is initiated and the memory is cleared.

The Trace may be made to start before the trigger (Before Trig) or following the trigger (After Trig). When Before Trig is selected, the 1611A counts 63 minus the Before Trig number of bytes after the trigger is recognized and then displays the contents of memory. If After Trig is selected, 63 plus the After Trig number of bytes are clocked in before the contents of the memory are displayed. If no selection is made the display starts with the inverse video trigger word and continues through the following 63 bytes (figure 8).

PARTIAL DISPLAYS

When Trace or Trace Trigs is initiated, all previous data is lost except the 16 lines in the display buffer and if Count Trigs or Time Interval is selected, all data is lost. If the data capture is halted before 64 bytes have been entered, only the new data is displayed.

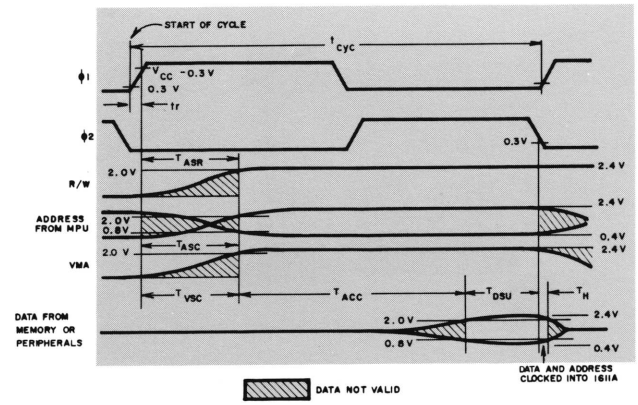


Figure 7A. 6800 memory read cycle shows when data is clocked into the 1611A.

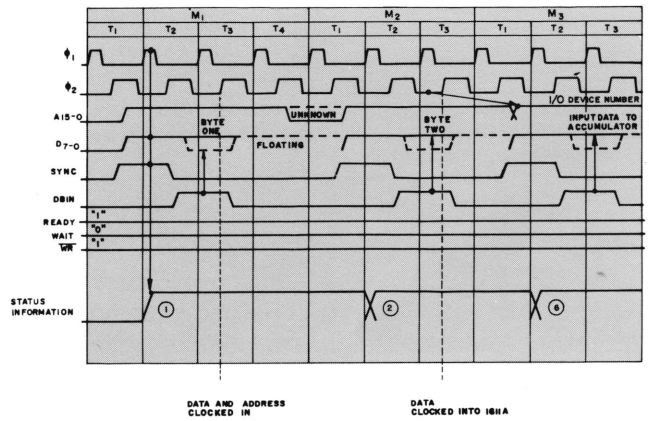


Figure 7B. 8080 instruction cycle shows when data is clocked into the 1611A.

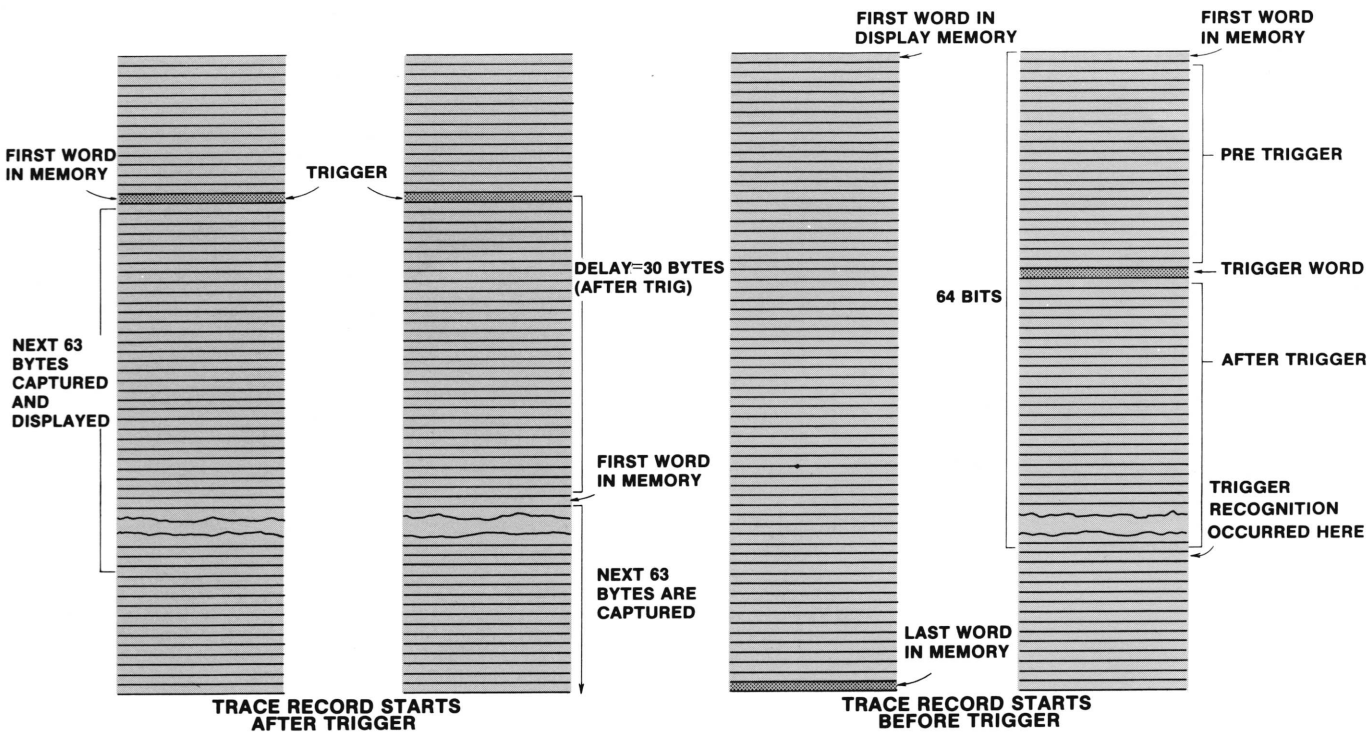


Figure 8. Memory diagrams show relationships of delay and pretrigger conditions.

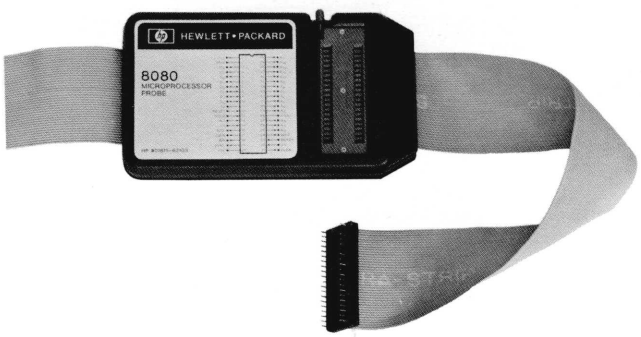


Figure 9. Dedicated probe offers fast connection to the system microprocessor socket with its 40-pin connector. The system microprocessor is relocated to the probe body.

PROBES

The 1611A uses two probes to acquire data from the system under test. The primary probe is dedicated to the microprocessor and is not interchangeable with other 1611A options. It is a pod that gathers the signals from the microprocessor data and address buses along with the Φ_2 clock and control signals and transmits them to the 1611A (figure 9). The pod contains a 40-pin connector socket in which the microprocessor is placed. Connection is made from the pod to the microprocessor socket in the system under test through a ribbon cable and 40-pin connector plug. If the microprocessor cannot be removed from the system, the connector cable and plug can be replaced with a ribbon cable terminated with a 40-pin dual in-line package connector (figure 10) which provides a direct connection from the pod to the processor.

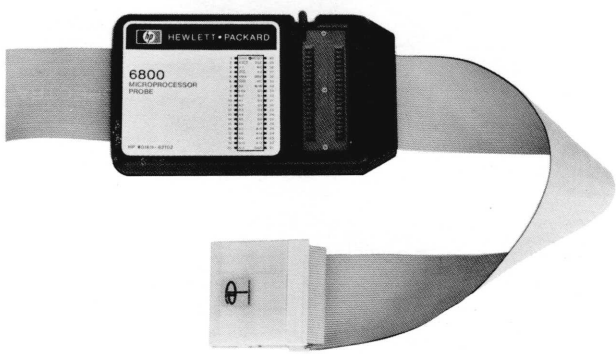


Figure 10. Where the microprocessor is easily accessible or not easily removed a 40-pin clip can be used for connection to the system.

The External probe is secondary, with no clock input, and is not required for instrument operation (figure 11). It does have 8 uncommitted input lines to accept data coincident with data bus inputs on the primary probe. The input impedance is specified at approx 1 MΩ shunted by ≤25 pF at the probe tip.

CONTROLS

The on board microprocessor in the 1611A allows keyboard entry for most of the controls which offers several advantages. The controls can be neatly arranged in related groups. Front panel clutter is reduced and fewer controls are required because the internal intelligence makes each one more powerful. Another advantage is that all of the information concerning the status of the controls is presented on the display rather than depending on the operator to read the status of various switches, knobs, and pushbuttons.

Figure 11. An external probe permits connection to other points of interest in the system for additional data gathering capability.

The keyboard controls are arranged in four groups (figure 12). The various controls are discussed in some detail in the following paragraphs. For more detailed descriptions, refer to the 1611A Operator's Manual.

Trace Specification: This group contains all of the controls associated with setting up the trigger conditions. Selection of one of these keys opens a field as indicated by the inverse video on the display.

Entry Keys: Numerical data is entered into the open Trace Specification field using keys in the Entry Group.

Execute: Selection of these keys determines the type measurement which the 1611A is to perform and therefore the type of display obtained.

Display: The display group controls are used to manipulate the CRT display but have no effect on the memory content.

TRACE SPECIFICATION

The Trace Specification group contains three subgroups—Trigger, Trigger Enable, and Trigger Disable.

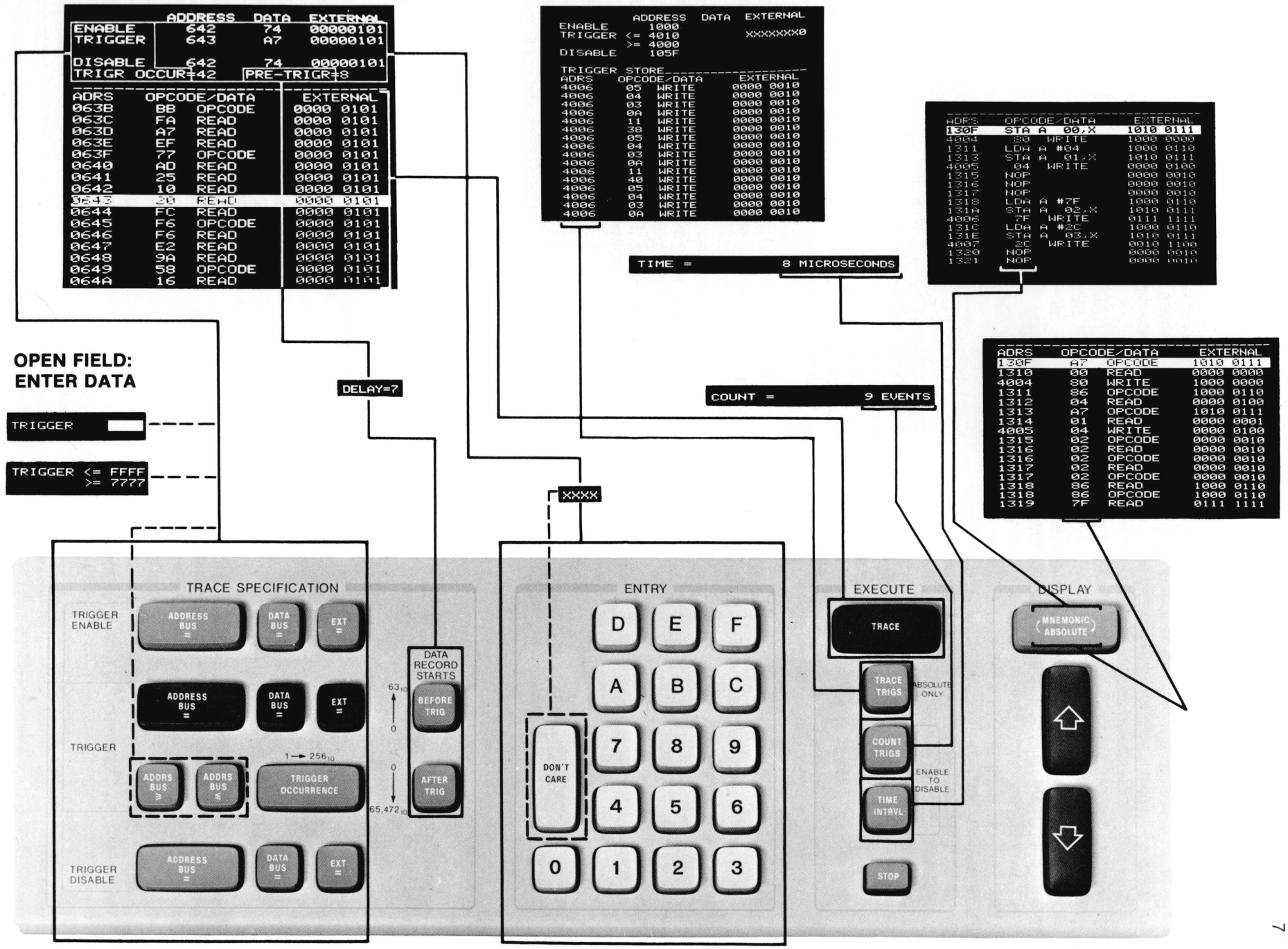


Figure 12. Keyboard with related traces generated by various keyed entries.

Trigger: The selected trigger word may be as short as one bit or as long as thirty-two bits in length. Any unspecified fields are automatically read as don't cares. Trigger entry is separated into three parts. As the key is selected for each part, the corresponding field is opened on the display.

Address Bus =: Controls the field for entry of the desired program or memory address trigger word. Entry is made with 4 hex or 6 octal characters and is automatically right justified with leading zeroes assumed.

Data Bus =: Controls the selection of an 8 bit trigger word on the data bus. Entries may be made as 2 hex or 3 octal characters and are automatically right justified with leading zeroes.

The Address Bus and Data Bus controls allow the operator to enter trigger conditions exactly as they appear on his code sheets. The arrangement is also much less confusing than working with individual bits from 24 uncommitted inputs which can lead to time-consuming errors in setup.

Ext =: Controls trigger recognition on 8 external lines. Entry is made in binary and is automatically right justified with leading don't cares assumed. These eight lines can be used to monitor the activity external to the processor such as control lines and can also be used as trigger and display qualifiers. For example, the Trace Trigs display could be qualified with a signal such as the R/W line on the 6800 to produce a display containing only "write" instructions. The Ext inputs are active only when the Data Bus inputs are active.

The trigger word recognized by the 1611A is the AND combination of the 32 bits controlled by the Address Bus, Data Bus, and Ext keys. Further qualification can be obtained using additional Trigger group keys.

Trigger Occurrence: This control is used to determine the number of trigger word occurrences before recognition. Selection of the key opens a field for the entry of a decimal number $1 \leq n \leq 256$. An obvious application for this control is triggering on the nth occurrence of a subroutine to look for an error. This feature could also be used to trigger on the nth occurrence of an external bit or combination of bits such as the output of a shift register.

Address Bus ≥, (Address Bus ≤): Additional triggering power is achieved with the use of these keys which limit triggering to activity ≥ (≤) the selected address. An alternate approach is to consider any address ≥ (≤) the selected address as a don't care. These controls can be used to look for trigger occurrences in forbidden areas of ROM or RAM using pretrigger to determine how the program arrived there. In this respect, they perform one of the functions of the map mode of the 1600A. The Address Bus ≥ (≤) controls could also be used along with the occurrence counter to page through a section of ROM or RAM where an error is suspected in a stored table which is a common problem encountered when debugging a system. For example:

ADDRS	ADDRS		
BUS 8000	BUS	9000	n = 1, 2, 3, . . . 256
≥	≤		

Trigger Enable and Trigger Disable: Functions are entered in the same manner as the Trigger word. They can be considered as a trigger arm and disarm circuit. When used in conjunction with the Trigger word, a sequence of trigger events is described. The 1611A will look for a trigger word after the occurrence of the Enable word and before the occurrence of the Disable word. These features, for example, allow the search for a trigger word only as it occurs in a subroutine bounded by the Enable and Disable Addresses or perhaps by an external control signal going high and then returning low.

Trigger Enable and Trigger Disable functions are also used in conjunction with the Count Trigs and Time Interval modes to determine the limits of activity.

Unless otherwise specified, the display begins with the trigger word (displayed in inverse video) and continues through the following 63 words. **Delay** can be added by selecting Trace Starts After Trig and entering a decimal number $n \leq 65\,472$.

"Negative Time" or pretrigger is displayed by selecting Trace Starts Before Trig and entering a decimal number $n \leq 63$. Note that Delay refers to qualified clocks or memory transactions and not to the number of ϕ_2 clocks.

EXECUTE CONTROLS

The execute group is used to instruct the 1611A to perform a specific task or measurement. Any Execute function except Stop immediately clears the main memory of old data. Upon execution of a Trace or Trace Trig, the 16 bytes of data in the display buffer will remain on display until the new acquisition is complete and a display cycle is initiated.

Trace: The Trace is the most general mode of data acquisition because it provides the capture of 64 consecutive memory transactions in order to provide a display of microprocessor program execution. When Trace is selected, the trigger circuit is activated and data acquisition begins. After the main memory is filled and the delay and trigger conditions have been satisfied, data acquisition is halted and a display cycle is initiated. The display cycle consists of a transfer of data from the main memory to the display and requires approximately 200 ms (figure 13).

Trace Triggers: In the Trace Trigger mode, the 1611A captures and displays only those bytes that contain a match with the preselected trigger conditions. This mode can be considered as a qualified display. For example, the operator may want to look at only the

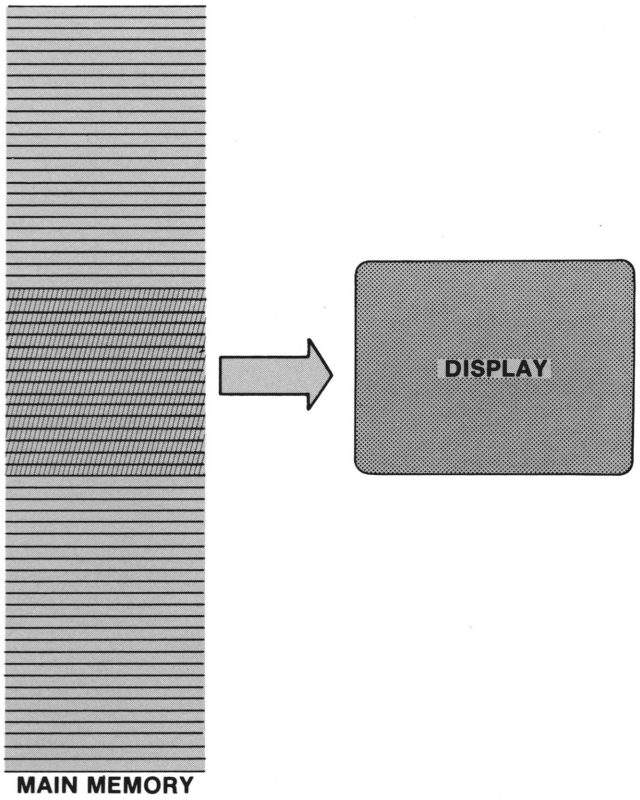


Figure 13. 16-bytes of data out of the 64 bytes in memory are written directly to the display.

"Read" instruction from a block of memory in order to verify that the proper data was entered there or he may want to acquire data only when a specified peripheral device is addressed.

Count Trigs: In the Count Trigs mode, 1611A counts the trigger occurrences between the Trig Enable and Trig Disable words. The display contains no data other than the decimal number equal to the number of trigger words recognized. One of the primary uses of this mode is in determing the number of times a subroutine is called in a branch of the program. Some times a programmer might miscalculate the number of times a program iterates through an increment, decrement or delay loop. This new feature allows rapid verification of the number of iterations that occur.

Time Interval: The Time Interval mode produces a readout of the elapsed time between the occurrence of two states defined by the Trigger Enable and the Trigger Disable. The timing measurement is made using an internal 1 MHz clock and the accuracy of the measurement is within 0.1% ±1 μs.

Verifying the accuracy of wait loops is an obvious application of the time interval features but it is also useful to know the time required for execution of a subroutine when a critical timing interface is involved with the system hardware or an external device.

Stop: Selection of the Stop key halts any execute function in progress. A display of the activity leading to the Stop command will result.

DISPLAY GROUP

Display group controls are used to determine the format in which data is displayed—they have no bearing on the actual data stored in memory.

Mnemonic/Absolute: This control determines whether the data is displayed as captured (absolute) or if the data is to be inverse assembled into mnemonic statements with operands (mnemonic). In Absolute mode, each line of display represents one memory transaction which includes an address, data word, description of operation (i.e. op code, read, write), and 8 external bits. The mnemonic mode data is inverse assembled into a display which often contains more than one memory transaction per line. Each line contains an address, a mnemonic symbol, and possibly an 8 or 16 bit operand in addition to the operation description field and 8 bits of external probe data. It's usual for the mnemonic display to contain less than 64 lines although the data content is the same as the 64 line absolute display.

Roll ↑ ↓ : These key controls are used to roll the 16 line display window through the 64 byte memory.

TRIGGER OUT

Three output connectors are provided on the rear panel of the 1611A for supplying trigger pulses to peripheral device.

Trigger Output: *Provides ~ 75 ns, RZ, TTL output on each and every occurrence of the selected trigger word. This output can be especially useful for triggering an oscilloscope.

Trace Point Out (⌐‾) (¬_): *These outputs are levels which change state when a trace is initiated and return to previous state when a trigger word is recognized or the trace point is reached after delay.** This provides a transition for triggering and pulse for gating. A useful application is to connect one of these outputs to the interrupt line of the microprocessor under test. The arrival at the trace point is under control of the operator who can initiate an interrupt at any time, which enables him to call up special debug software of his own during development.

*The Trigger Output and Trace Point Out transitions occur within 350 ns (opt 080) or 550 ns (opt 068) of trigger recognition.

**If delay has been added, the output transition will occur one memory transaction before the first word in the display (figure 14).

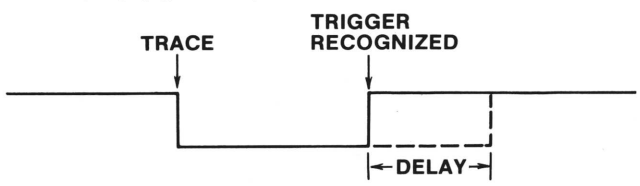
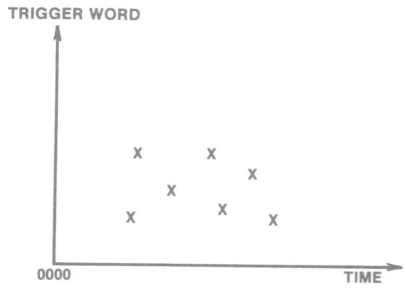


Figure 14. Trace Point timing diagram. When Trace is pressed the signal changes state and upon trigger recognition returns to its original level. If delay is added the return transition occurs one memory transaction prior to the first displayed word.

TABLE II
THE 1611A TRIGGERING STORY

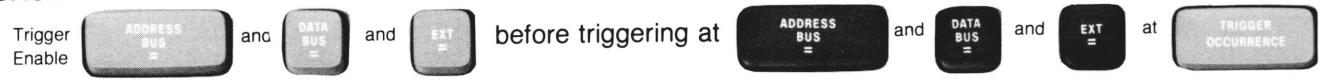
1. Simple triggering is accomplished with the logical AND combinations of 32 possible bits with don't cares allowed.



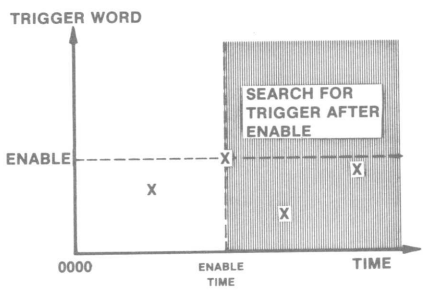
2. Triggering power can be increased by specifying which occurrence of the trigger word is to be recognized. If not specified, the first occurrence is recognized.

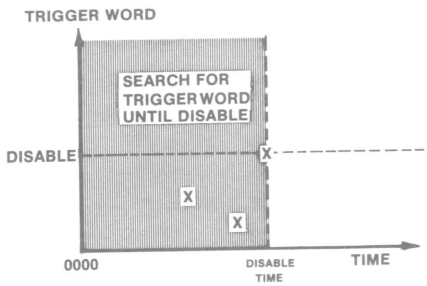
3. The trigger word can be further qualified using the Trigger Enable and Trigger Disable features.

CASE I

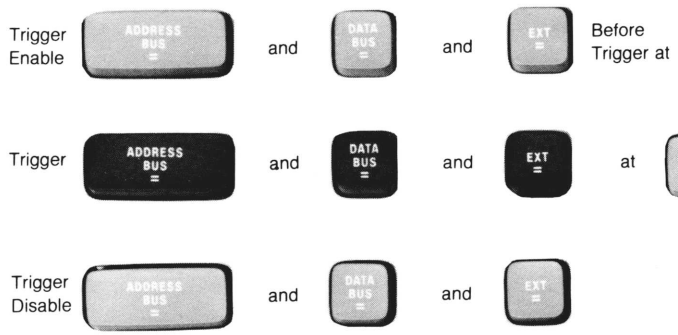


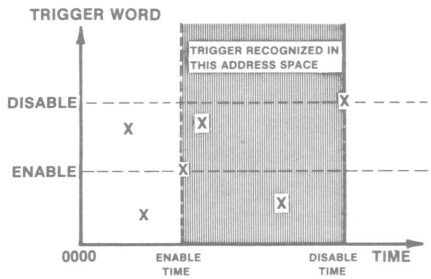
CASE II





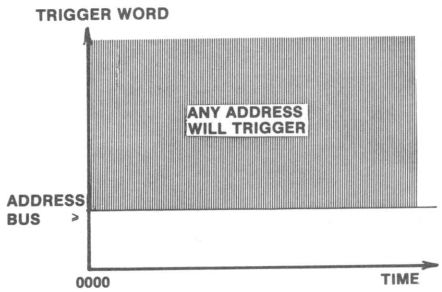
4. Used together triggering can be limited to area of interest such as a subroutine.





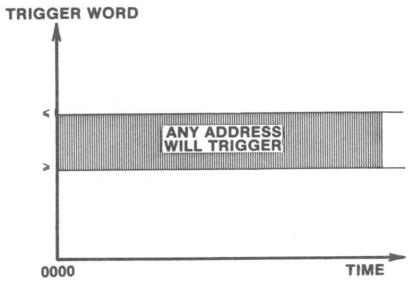
5. Trigger circuit can be made to recognize any address ≥ or ≤ its selected address. In effect, any address ≥ (≤) the selected address is a don't care.

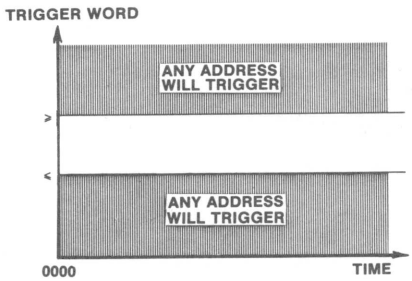
Trigger on any Address ≥ [ADDRS BUS ≥] at [TRIGGER OCCURRENCE]



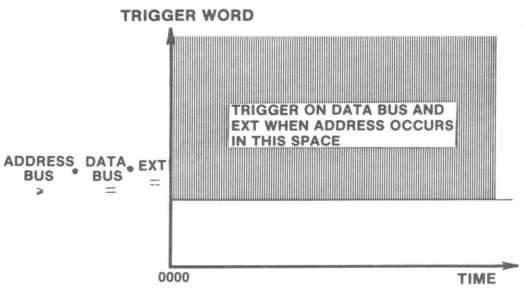
6. The [ADDRS BUS ≥] and [ADDRS BUS ≤] can be used together

to define a band of interest.





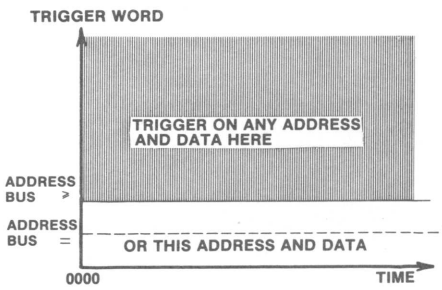
7. The [ADDRS BUS ≥] and [ADDRS BUS ≤] are logically ANDed with [DATA BUS =] and [EXT =] at [TRIGGER OCCURRENCE]



8. The [ADDRS BUS ≥] can be logically ORed with

[ADDRESS BUS =] and [DATA BUS =] and [EXT =]

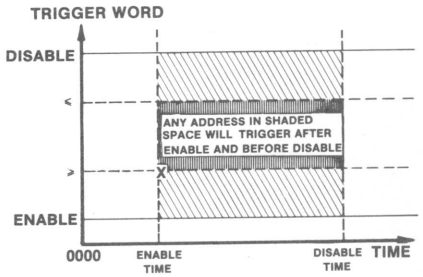
[ADDRS BUS ≥] and [DATA BUS =] and [EXT =] or [ADDRESS BUS =] and [DATA BUS =] and [EXT =] at [TRIGGER OCCURRENCE]



9. The functions can be nested to produce:

Trigger Enable [ADDRESS BUS =] and [DATA BUS =] and [EXT =] Before Triggering on any Address between [ADDRS BUS ≥] and [ADDRS BUS ≤] before

Trigger Disable [ADDRESS BUS =] and [DATA BUS =] and [EXT =]



Option 068

1 Allows operator to prevent 1611A from triggering on 6800 "look ahead." Also excludes triggering on data bytes.

2 No Clock light is on when no ϕ_2 clock is present.

3 Halted indicated when microprocessor has been halted externally.

4 Halted by 1611A indicates the microprocessor has been halted after Trace has completed or Trace Single Step has been executed.

5 Waiting For Interrupt indicates that microprocessor has executed a Wait for Interrupt instruction (WAI).

6 Selects Octal or Hex format for data display and heading decimal numbers are unchanged (figure 15).

Option 080

7 No Clock light is on when no ϕ_2 clock is present.

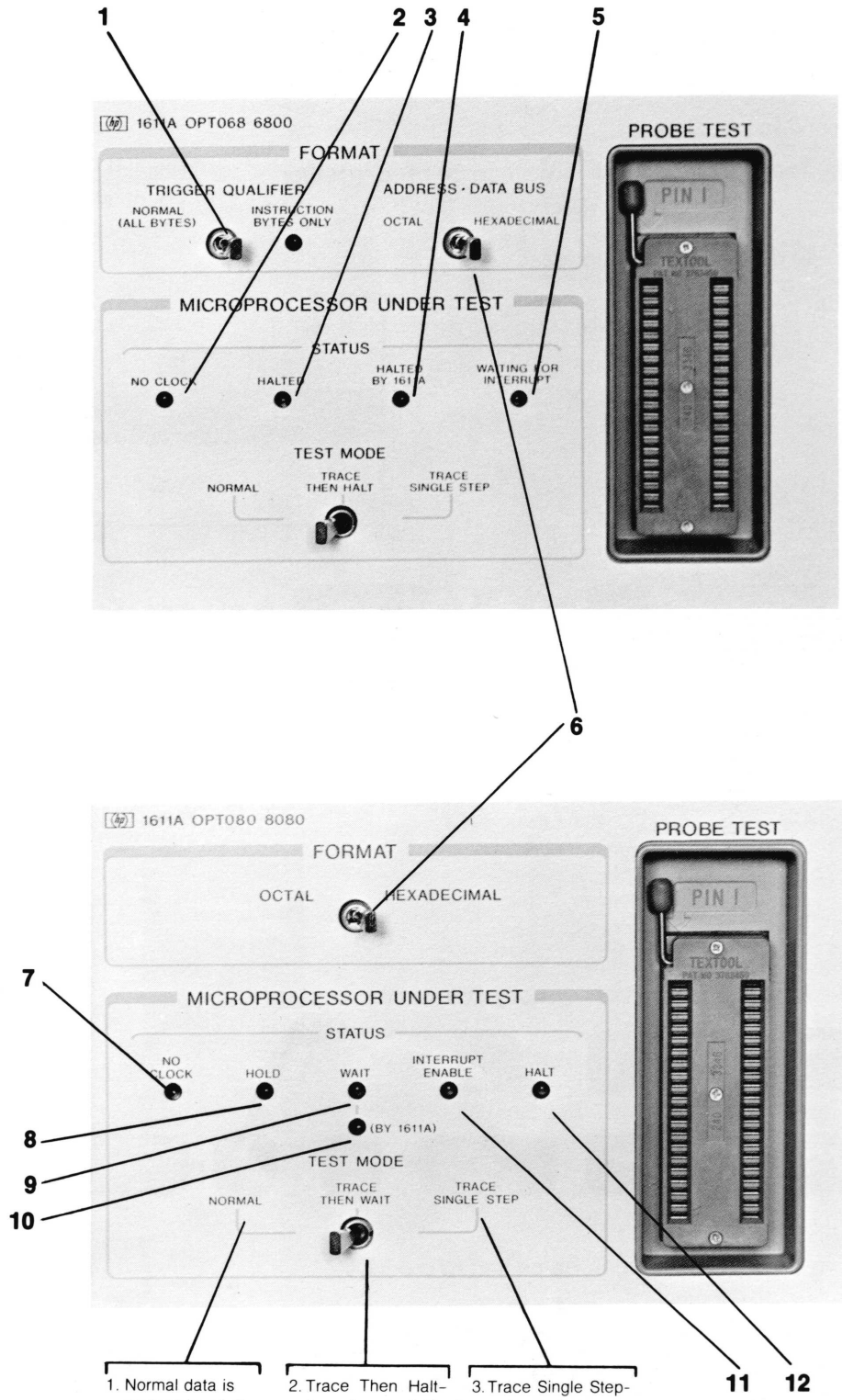
8 Hold indicates Hold line low and 8080 is holding.

9 Wait indicates 8080 is in Wait mode and is waiting for inputs from memory or peripheral device.

10 By 1611A indicates when Wait state is generated by 1611A in TH or TSS mode.

11 Interrupt enable indicates status of internal enable bit which will allow interrupt to be processed.

12 Halt indicates that a Halt instruction has been executed by 8080A.
Switch selects test move.



```
                ADDRESS   DATA   EXTERNAL

TRIGGER          13D0

ADRS    OPCODE/DATA          EXTERNAL
13D0    CLR B                0000 0011
13D1    INC B                0000 0011
13D2    LDA A   11           0000 0011
0011     04   READ           0000 0011
13D4    ABA                  0000 0011
13D5    DAA                  0000 0011
13D6    STA A   11           0000 0011
0011     05   WRITE          0000 0010
13D8    NOP                  0000 0011
13D9    NOP                  0000 0011
13DA    NOP                  0000 0011
13DB    LDA B   10           0000 0011
0010     00   READ           0000 0011
13DD    ABA                  0000 0011
13DE    DAA                  0000 0011
13DF    STA A   12           0000 0011
```

```
                ADDRESS   DATA   EXTERNAL

TRIGGER          011720

ADRS    OPCODE/DATA          EXTERNAL
011720  CLR B                00 000 011
011721  INC B                00 000 011
011722  LDA A   021          00 000 011
000021   004 READ            00 000 011
011724  ABA                  00 000 011
011725  DAA                  00 000 011
011726  STA A   021          00 000 011
000021   005 WRITE           00 000 010
011730  NOP                  00 000 011
011731  NOP                  00 000 011
011732  NOP                  00 000 011
011733  LDA B   020          00 000 011
000020   000 READ            00 000 011
011735  ABA                  00 000 011
011736  DAA                  00 000 011
011737  STA A   022          00 000 011
```

Figure 15. Traces at the same trigger point showing capability of switching from hexadecimal format (upper photo) to octal format (lower photo).

SELF TEST

During power up, the internal microprocessor makes some internal tests on the 1611A. A check sum on the ROM is performed which tests the ROM for dropped bits. Next a test pattern is written to the RAM and then read back and checked for accuracy. Upon satisfactory completion of these tests, the message "SELF TEST COMPLETED" is written on screen by the microprocessor which gives a visual indication that the display circuitry and microprocessor are working properly.

```
                ADDRESS   DATA   EXTERNAL

TRIGGER          XXXX     AA

                          PRE-TRIGR=7

ADRS    OPCODE/DATA          EXTERNAL
3333     33   WRITE          0000 0000
4444     44   WRITE          0000 0000
5555     55   WRITE          0000 0000
6666     66   WRITE          0000 0000
7777     77   WRITE          0000 0000
8888     88   WRITE          0000 0000
9999     99   WRITE          0000 0000
AAAA     AA   WRITE          0000 0000
BBBB     BB   WRITE          0000 0000
CCCC     CC   WRITE          0000 0000
DDDD     DD   WRITE          0000 0000
EEEE     EE   WRITE          0000 0000
FFFF     FF   WRITE          0000 0000
0000     00   WRITE          0000 0000
1111     11   WRITE          0000 0000
2222     22   WRITE          0000 0000
```

Figure 16. Internally generated test display in the probe test mode.

PROBE TEST: Functional tests may be made on the 1611A without any external circuits. These tests are made by connecting the microprocessor probe plug into the front panel socket. Executing a trace generates the display shown in figure 16. All of the system's functions and controls may then be exercised on this pattern.

QUESTIONS ABOUT THE 1611A

Q Are there any additional microprocessor options planned for the near future?

A Additional options are being considered and can be introduced as required when the market picture clarifies and settles on various processors. Field Engineers should make their inputs known to the Colorado Springs Division.

Q What is involved in converting from one option to another?

A The conversion process involves removing the top cover, exchanging two boards, and replacing the front panel unit and microprocessor probe with the new option. It takes about 15 minutes to make a changeover.

Q Can the 1611A be used as a general purpose state analyzer?

A No. The personality modules require special qualification of the Φ_2 clock in order to capture data in the proper order.

Q Will Hewlett-Packard design and build option kits for a customer's "in house" microprocessor?

A Probably not, the development would be expensive and the customer would probably be required to commit to purchase a substantial number of units.

Q Can the 1611A option 080 be used with 8080A's produced by manufacturers other than Intel?

A Yes, the 1611A is compatible with all the second source versions of the 8080A.

Q Why was a map mode not included?

A The map was omitted for a number of reasons, one being that it is not compatible with the CRT used in the 1611A. However, one of the key features of the map is available with the 1611A Trace Specification keys. For example, if the program is running off to the "bushes" use the $\geq(\leq)$ keys and enter the allowable address bounds along with several bits of pretrig. The 1611A will then trigger and display on any memory transaction which occurs at an address outside that specified.

SILICON GATE MOS 8080A

INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
$MOV_{r1,r2}$	Move register to register	0	1	D	D	D	S	S	S	5
MOV M, r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r, M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

NOTES: 1. DDD or SSS – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.
2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

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M6800 INSTRUCTION SET SUMMARY

ACCUMULATOR AND MEMORY OPERATIONS	MNEMONIC	IMMED OP	IMMED ~	IMMED #	DIRECT OP	DIRECT ~	DIRECT #	INDEX OP	INDEX ~	INDEX #	EXTND OP	EXTND ~	EXTND #	INHER OP	INHER ~	INHER #	BOOLEAN/ARITHMETIC OPERATION (All register labels refer to contents)	5 H	4 I	3 N	2 Z	1 V	0 C
Add	ADDA	8B	2	2	9B	3	2	AB	5	2	BB	4	3				A + M → A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	5	2	FB	4	3				B + M → B	↕	•	↕	↕	↕	↕
Add Acmltrs	ABA													1B	2	1	A + B → A	↕	•	↕	↕	↕	↕
Add with Carry	ADCA	89	2	2	99	3	2	A9	5	2	B9	4	3				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	5	2	F9	4	3				B + M + C → B	↕	•	↕	↕	↕	↕
And	ANDA	84	2	2	94	3	2	A4	5	2	B4	4	3				A • M → A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	5	2	F4	4	3				B • M → B	•	•	↕	↕	R	•
Bit Test	BITA	85	2	2	95	3	2	A5	5	2	B5	4	3				A • M	•	•	↕	↕	R	•
	BITB	C5	2	2	D5	3	2	E5	5	2	F5	4	3				B • M	•	•	↕	↕	R	•
Clear	CLR							6F	7	2	7F	6	3				00 → M	•	•	R	S	R	R
	CLRA													4F	2	1	00 → A	•	•	R	S	R	R
	CLRB													5F	2	1	00 → B	•	•	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	5	2	B1	4	3				A − M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	5	2	F1	4	3				B − M	•	•	↕	↕	↕	↕
Compare Acmltrs	CBA													11	2	1	A − B	•	•	↕	↕	↕	↕
Complement, 1's	COM							63	7	2	73	6	3				$\overline{M} \rightarrow M$	•	•	↕	↕	R	S
	COMA													43	2	1	$\overline{A} \rightarrow A$	•	•	↕	↕	R	S
	COMB													53	2	1	$\overline{B} \rightarrow B$	•	•	↕	↕	R	S
Complement, 2's (Negate)	NEG							60	7	2	70	6	3				00 − M → M	•	•	↕	↕	①	②
	NEGA													40	2	1	00 − A → A	•	•	↕	↕	①	②
	NEGB													50	2	1	00 − B → B	•	•	↕	↕	①	②
Decimal Adjust, A	DAA													19	2	1	Converts Binary Add. of BCD Characters into BCD Format	•	•	↕	↕	↕	③
Decrement	DEC							6A	7	2	7A	6	3				M − 1 → M	•	•	↕	↕	④	•
	DECA													4A	2	1	A − 1 → A	•	•	↕	↕	④	•
	DECB													5A	2	1	B − 1 → B	•	•	↕	↕	④	•
Exclusive OR	EORA	88	2	2	98	3	2	A8	5	2	B8	4	3				A ⊕ M → A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	5	2	F8	4	3				B ⊕ M → B	•	•	↕	↕	R	•
Increment	INC							6C	7	2	7C	6	3				M + 1 → M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1 → A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1 → B	•	•	↕	↕	⑤	•
Load Acmltr	LDAA	86	2	2	96	3	2	A6	5	2	B6	4	3				M → A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	5	2	F6	4	3				M → B	•	•	↕	↕	R	•
Or, Inclusive	ORAA	8A	2	2	9A	3	2	AA	5	2	BA	4	3				A + M → A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	5	2	FA	4	3				B + M → B	•	•	↕	↕	R	•
Push Data	PSHA													36	4	1	A → M_{SP}, SP − 1 → SP	•	•	•	•	•	•
	PSHB													37	4	1	B → M_{SP}, SP − 1 → SP	•	•	•	•	•	•
Pull Data	PULA													32	4	1	SP + 1 → SP, M_{SP} → A	•	•	•	•	•	•
	PULB													33	4	1	SP + 1 → SP, M_{SP} → B	•	•	•	•	•	•
Rotate Left	ROL							69	7	2	79	6	3				M	•	•	↕	↕	⑥	↕
	ROLA													49	2	1	A	•	•	↕	↕	⑥	↕
	ROLB													59	2	1	B	•	•	↕	↕	⑥	↕
Rotate Right	ROR							66	7	2	76	6	3				M	•	•	↕	↕	⑥	↕
	RORA													46	2	1	A	•	•	↕	↕	⑥	↕
	RORB													56	2	1	B	•	•	↕	↕	⑥	↕
Shift Left, Arithmetic	ASL							68	7	2	78	6	3				M	•	•	↕	↕	⑥	↕
	ASLA													48	2	1	A	•	•	↕	↕	⑥	↕
	ASLB													58	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Arithmetic	ASR							67	7	2	77	6	3				M	•	•	↕	↕	⑥	↕
	ASRA													47	2	1	A	•	•	↕	↕	⑥	↕
	ASRB													57	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Logic.	LSR							64	7	2	74	6	3				M	•	•	R	↕	⑥	↕
	LSRA													44	2	1	A	•	•	R	↕	⑥	↕
	LSRB													54	2	1	B	•	•	R	↕	⑥	↕
Store Acmltr.	STAA				97	4	2	A7	6	2	B7	5	3				A → M	•	•	↕	↕	R	•
	STAB				D7	4	2	E7	6	2	F7	5	3				B → M	•	•	↕	↕	R	•
Subtract	SUBA	80	2	2	90	3	2	A0	5	2	B0	4	3				A − M → A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	5	2	F0	4	3				B − M → B	•	•	↕	↕	↕	↕
Subract Acmltrs.	SBA													10	2	1	A − B → A	•	•	↕	↕	↕	↕
Subtr. with Carry	SBCA	82	2	2	92	3	2	A2	5	2	B2	4	3				A − M − C → A	•	•	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	E2	5	2	F2	4	3				B − M − C → B	•	•	↕	↕	↕	↕
Transfer Acmltrs	TAB													16	2	1	A → B	•	•	↕	↕	R	•
	TBA													17	2	1	B → A	•	•	↕	↕	R	•
Test, Zero or Minus	TST							6D	7	2	7D	6	3				M − 00	•	•	↕	↕	R	R
	TSTA													4D	2	1	A − 00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B − 00	•	•	↕	↕	R	R

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M6800 INSTRUCTION SET SUMMARY (Con't)

INDEX REGISTER AND STACK		IMMED			DIRECT			INDEX			EXTND			INHER				5	4	3	2	1	0
POINTER OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BOOLEAN/ARITHMETIC OPERATION	H	I	N	Z	V	C
Compare Index Reg	CPX	8C	3	3	9C	4	2	AC	6	2	BC	5	3				$(X_H/X_L) - (M/M+1)$	•	•	⑦	↕	⑧	•
Decrement Index Reg	DEX													09	4	1	$X - 1 \rightarrow X$	•	•	•	↕	•	•
Decrement Stack Pntr	DES													34	4	1	$SP - 1 \rightarrow SP$	•	•	•	•	•	•
Increment Index Reg	INX													08	4	1	$X + 1 \rightarrow X$	•	•	•	↕	•	•
Increment Stack Pntr	INS													31	4	1	$SP + 1 \rightarrow SP$	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	6	2	FE	5	3				$M \rightarrow X_H, (M+1) \rightarrow X_L$	•	•	⑨	↕	R	•
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	6	2	BE	5	3				$M \rightarrow SP_H, (M+1) \rightarrow SP_L$	•	•	⑨	↕	R	•
Store Index Reg	STX				DF	5	2	EF	7	2	FF	6	3				$X_H \rightarrow M, X_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Store Stack Pntr	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H \rightarrow M, SP_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Indx Reg → Stack Pntr	TXS													35	4	1	$X - 1 \rightarrow SP$	•	•	•	•	•	•
Stack Pntr → Indx Reg	TSX													30	4	1	$SP + 1 \rightarrow X$	•	•	•	•	•	•

JUMP AND BRANCH		RELATIVE			INDEX			EXTND			INHER				5	4	3	2	1	0
OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BRANCH TEST	H	I	N	Z	V	C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = Zero	BEQ	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										$N \oplus V = 0$	•	•	•	•	•	•
Branch If > Zero	BGT	2E	4	2										$Z + (N \oplus V) = 0$	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										$C + Z = 0$	•	•	•	•	•	•
Branch If ≤ Zero	BLE	2F	4	2										$Z + (N \oplus V) = 1$	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										$C + Z = 1$	•	•	•	•	•	•
Branch If < Zero	BLT	2D	4	2										$N \oplus V = 1$	•	•	•	•	•	•
Branch If Minus	BMI	2B	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	26	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	BD	9	3					•	•	•	•	•	•
No Operation	NOP										01	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		———		⑩			———
Return From Subroutine	RTS										39	5	1	See special Operations	•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1		•	S	•	•	•	•
Wait for Interrupt	WAI										3E	9	1		•	⑪	•	•	•	•

CONDITIONS CODE REGISTER		INHER			BOOLEAN	5	4	3	2	1	0
OPERATIONS	MNEMONIC	OP	~	=	OPERATION	H	I	N	Z	V	C
Clear Carry	CLC	0C	2	1	$0 \rightarrow C$	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	$0 \rightarrow I$	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	$0 \rightarrow V$	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	$1 \rightarrow C$	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	$1 \rightarrow I$	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	$1 \rightarrow V$	•	•	•	•	S	•
Acmltr A → CCR	TAP	06	2	1	$A \rightarrow CCR$	———			⑫		———
CCR → Acmltr A	TPA	07	2	1	$CCR \rightarrow A$	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES:

(Bit set if test is true and cleared otherwise)

① (Bit V) Test: Result = 10000000?
② (Bit C) Test: Result = 00000000?
③ (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
④ (Bit V) Test: Operand = 10000000 prior to execution?
⑤ (Bit V) Test: Operand = 01111111 prior to execution?
⑥ (Bit V) Test: Set equal to result of N ⊕ C after shift has occurred.
⑦ (Bit N) Test: Sign bit of most significant (MS) byte of result = 1?
⑧ (Bit V) Test: 2's complement overflow from subtraction of LS bytes?
⑨ (Bit N) Test: Result less than zero? (Bit 15 = 1)
⑩ (All) Load Condition Code Register from Stack. (See Special Operations)
⑪ (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt is required to exit the wait state.
⑫ (ALL) Set according to the contents of Accumulator A.

LEGEND:

OP	Operation Code (Hexadecimal);	00	Byte = Zero;
~	Number of MPU Cycles;	H	Half-carry from bit 3;
#	Number of Program Bytes;	I	Interrupt mask
+	Arithmetic Plus;	N	Negative (sign bit)
–	Arithmetic Minus;	Z	Zero (byte)
•	Boolean AND;	V	Overflow, 2's complement
M_{SP}	Contents of memory location pointed to be Stack Pointer;	C	Carry from bit 7
		R	Reset Always
		S	Set Always
+	Boolean Inclusive OR;	↕	Test and set if true, cleared otherwise
⊕	Boolean Exclusive OR;	•	Not Affected
$\overline{M}$	Complement of M;	CCR	Condition Code Register
→	Transfer Into;	LS	Least Significant
0	Bit = Zero;	MS	Most Significant

SPECIFICATIONS, 1611A

PERSONALITY MODULES

OPTION 080 (8080 MICROPROCESSORS)

CLOCK (Φ_2 only)

Repetition Rate: 300 kHz to 4 MHz.

Width: 75 ns minimum for either high or low state.

Threshold: 9 to 13 V, logic 1 (high); —1 to 0.8 V, logic 0 (low).

Input Resistance: approx 12 kΩ.

Input Capacitance: approx 25 pF, includes capacitance of 30.5 cm (12 in.) cable, approx 15 pF with 7.6 cm (3 in.) cable.

DATA, ADDRESS, WAIT, READY, HLDA, INTE, SYNC

Threshold: 3 V to 6 V, logic 1 (high); —1 to 0.8 V, logic 0 (low).

Input Resistance: approx 1 MΩ.

Input Capacitance: approx 25 pF, includes capacitance of 30.5 cm (12 in.) cable, approx 15 pF with 7.6 cm (3 in.) cable.

SETUP AND HOLD TIMES: timing measured at 8 V level for leading edge of Φ_2 and 1 V level for trailing edge.

Address and μP status on Data lines relative to leading edge of Φ_2 at T_2. **Setup:** 100 ns min. **Hold:** 25 ns min.
Data relative to leading edge of Φ_2 at T_3. **Setup:** 100 ns min. **Hold:** 25 ns min.
Sync relative to trailing edge of Φ_2 at T_1. **Setup:** 100 ns min. **Hold:** 25 ns min.
Ready relative to trailing edge of Φ_2 at T_2. **Setup:** 80 ns min. **Hold:** 0 ns min.

READY OUTPUT: TTL open-collector compatible output capable of sinking at least 8 mA when active.

OUTPUTS: all timing relative to leading edge of Φ_2 in T_3 cycle.

Low: < 0.4 V into 50Ω.

High: > 2.0 V into 50Ω (nominally 3.9 V into an open circuit).

Trigger: duration, approx 75 ns (RZ format); delay, approx 350 ns after the Φ_2 clock pulse which defines a valid trigger.

Trace Point (⌐‾): provides a positive edge approx 350 ns after the Φ_2 clock that defines the specific valid trigger to be displayed on the 1611A. If the 1611A Delay is set such that the trigger is not displayed, the Trace Point Output occurs approx 350 ns after the Φ_2 clock that defines the valid trigger word immediately preceding the first word displayed on the 1611A.

Trace Point (‾⌐): complement of Trace Point (⌐‾).

COMPATIBILITY

Intel: 8080, 8080A, 8080A-2, 8080A-1.

AMD: 9080A, 9080A-1, 9080A-2, 9080A-4.

NEC: μPD8080, μPD8080A-E.

TI: TMS8080, TMS8080A.

National: INS8080A.

Note: The 1611A Option 080 is designed to be compatible with any microprocessor that meets the specifications of the Intel 8080A.

OPTION 068 (6800 MICROPROCESSORS)

CLOCK AND DATA INPUTS

Clock Rate: 70 kHz to 1.4 MHz.

Input Resistance: approx 1 MΩ for all inputs.

Input Capacitance: approx 30 pF for D_0-D_7 inputs; approx 40 pF for all other inputs including the capacitance of the 30.5 cm (12 in.) connecting cable, approx 10 pF less with 7.6 cm (3 in.) connecting cable.

Threshold: 2.4 V to 5.5 V, logic 1 (high); —0.8 V to 0.8 V, logic 0 (low).

Setup Time: D_0-D_7 must be present prior to the falling edge of the Φ_2 clock for at least 110 ns. $\overline{\text{HALT}}$ must be present prior to the leading edge of the Φ_2 clock for at least 250 ns. All other inputs must be present prior to the falling edge of the Φ_2 clock for at least 250 ns.

Hold Time: $\overline{\text{HALT}}$ must be present after the leading edge of the Φ_2 clock for at least 10 ns. All other inputs must be present after the falling edge of the Φ_2 clock for at least 10 ns.

HALT OUTPUT: TTL open-collector compatible output capable of sinking at least 8 mA when active.

OUTPUTS

Low: < 0.4 V into 50Ω.

High: > 2.0 V into 50Ω (nominally 3.9 V into an open circuit).

Trigger Output: duration, approx 75 ns in RZ format; delay, approx 550 ns after the active edge of the Φ_2 clock pulse that defines a valid trigger.

Trace Point (⌐‾): provides a positive edge approx 550 ns after the Φ_2 clock pulse that defines the specific valid trigger to be displayed on the 1611A. If the 1611A Delay is set such that the trigger word is not displayed, the Trace Point output occurs approx 500 ns after the active edge of the Φ_2 clock that defines the valid word immediately preceding the first displayed word.

Trace Point (‾⌐): complement of Trace Point (⌐‾).

COMPATIBILITY

Motorola: 6800.

AMI: 6800.

Note: The 1611A Option 068 is designed to be compatible with any microprocessor that meets the specifications of the Motorola 6800.

EXTERNAL PROBE INPUTS

RESISTANCE: approx 1 MΩ.

CAPACITANCE: approx 25 pF measured at probe tip.

THRESHOLD: 2.4 V to 5.5 V, logic 1 (high); —0.8 V to 0.8 V, logic 0 (low).

SETUP TIME: input must be present for at least 250 ns prior to falling edge at Φ_2 clock.

HOLD TIME: input must be present for at least zero ns after falling edge of Φ_2 clock.

GENERAL

CONNECTION BETWEEN μP and 1611A INPUT BUFFERS: one 40 pin dual in-line package connector with 30.5 cm (12 in.) cable, one 40 pin male socket with 30.5 cm (12 in.) cable, or one 40 pin male socket with 7.6 cm (3 in.) cable.

MEMORY DEPTH: 64 data transactions; 16 transactions are displayed at one time, roll keys permit viewing all 64 transactions.

TIME INTERVAL: accuracy, 0.1% ±1 μs. Maximum time, 2^{24}—1 μs (16.7 seconds).

EVENTS COUNT: 2^{24}—1 events (16.7 million) max.

LOGIC PROBE OUTPUT POWER: 5 V dc at 0.1 A max.

POWER: 100, 120, 220, 240 V ac; —10% +5%; 48 to 440 Hz; 120 VA max.

DIMENSIONS: see outline drawings.

OPERATING ENVIRONMENT

Temperature: 0°C to 55°C.

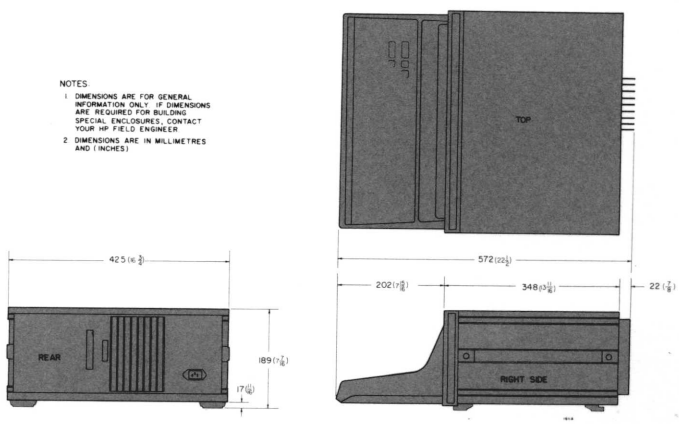
Humidity: up to 95% relative humidity at 40°C.

Altitude: to 4600 m (15 000 ft).

Vibration: vibrated in three planes for 15 min. each with 0.38 mm (0.015 in.) excursions, 10 to 55 Hz.

WEIGHT: net, 15 kg (33 lb); shipping, 19.5 kg (43 lb).

ACCESSORIES SUPPLIED: one microprocessor probe (for 6800 with Opt 068, for 8080 with Opt 080), external 8-bit probe; one 40 pin clip with 30.5 cm (12 in.) cable, one 40 pin male socket with 30.5 cm (12 in.) cable; one 40 pin male socket with 7.6 cm (3 in.) cable; one 2.3 m (7.5 ft) power cord; and one Operating and Service Manual.



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