UniSite 40
UNIVERSAL PROGRAMMER
Maintenance Manual

972-0014 January 1987

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ORDERING INFORMATION

This manual applies to engineering part number 991-0014-001 thru -099.

SAFETY SUMMARY

General safety information is contained in this summary. In addition, specific WARNING and CAUTION notes appear throughout this manual where they apply which are not included in this summary.

DEFINITIONS

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

CAUTION statements identify conditions or practices that could result in damage to equipment or other property.

SYMBOLS

⚠ : This symbol appears on the equipment to indicate the operator should consult the appropriate manual for details.

V~ : This symbol stands for Vac (e.g., 120 V ~ = 120 Vac)

QUALIFIED SERVICE PERSONNEL

This Manual contains instructions to be performed by qualified service personnel. To avoid personal injury do not perform any servicing instructions unless you are qualified to do so.

POWER SOURCE

Check the voltage selection marking (located on the top panel) to verify that the product is configured for the appropriate line voltage.

POWER CORD

Verify that the power cord used is the one specified for your equipment.

FUSE REPLACEMENT

For continued protection against the possibility of fire, replace the fuse only with a fuse of the specified voltage, current and type ratings.

GROUNDING

This product is grounded through the grounding conductor of the power cord. To avoid electric shock, verify that the power cord is plugged (or wired) into a properly wired receptacle only. Grounding this equipment is essential for its safe operation.

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Section 1
Introduction

1.1 OVERVIEW

This manual contains the maintenance information for UniSite, and is divided into the following sections:

INTRODUCTION	An overview of the product. Includes a complete list of product options, service information and the product warranty.
INSTALLATION/ DISASSEMBLY	Explains how to disassemble UniSite for troubleshooting or maintenance work.
CIRCUIT DESCRIPTION	Describes UniSite's theory of operation. Includes general and detailed block diagrams and circuit descriptions.
MAINTENANCE/ TROUBLESHOOTING	Explains routine maintenance for UniSite, including information on cleaning and reducing electrostatic discharge, and fault isolation information.
APPENDICES	Include a list of mnemonics for signal/bus lines used on the Controller board schematic, a list of UniSite's error messages, read/write diagrams, a set of UniSite schematics and a complete index.

WARNING

The procedures described in this manual should only be performed by trained electronics service personnel. Do not attempt these procedures if you are not qualified to do so.

1.2 OPTIONS

Standard features of the UniSite are included in a system package called the **UniSite 40**. The UniSite 40 includes 640K x 8 DRAM (512K system, 128K user), a 40-pin DIP socket module, one 3-1/2" disk drive and two serial (RS-232C) ports. UniSite also is compatible with 41 I/O translation formats. With UniSite's Expansion RAM board, memory capabilities can be increased to 512K x 8 bytes. A second 3-1/2" disk drive and optional module for PLCC/SOIC package support are also available. Options are included in the UniSite **System 40** package, and include:

- A second 3-1/2" disk drive
- Plastic leadless chip carrier (PLCC)/SOIC socket module
- ASCII terminal

Other UniSite options, available from your nearest sales office:

- Box of blank 3-1/2" diskettes
- Expansion RAM board

If you wish to purchase any UniSite options, contact your nearest Data I/O sales office. A list of all the sales offices may be found at the back of this manual. Orders placed with Data I/O must include the following:

- Description of the present equipment's configuration
- Desired options and accessories
- Purchase order number
- Desired method of shipment
- Quantity of each item ordered
- Shipping and billing address of your company, including ZIP code
- Name of the person ordering the equipment
- Signed software license agreement

1.3 SERVICE INFORMATION AND WARRANTY

When calling Data I/O for service help, you should have ready the information shown in table 1-1. For future reference, you may write in the numbers in the spaces provided.

Table 1-1. Service Information

Product name: UniSite

Serial number: _____

Model number: 991-0014- _____

Part number: 901-0058- _____

Diskette software version: _____

EPROM version level: _____

TELEPHONE NUMBER/ NAME OF NEAREST SERVICE OFFICE: _____
(from address list at back of manual)

NOTE

The serial number, model number and the part number are printed on a back panel plate, just above the terminal and remote port connectors. The diskette and EPROM version are displayed on the UniSite power-up screen.

1.3.1 Service Information and Hardware Warranty

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period for UniSite's hardware is one year, unless specified otherwise, and begins when you receive the equipment. The warranty for the program diskette is 90 days and applies only to the diskette itself. See the licensing agreement shipped with your System diskette for more details about the software warranty. The warranty card inside the back cover of the Operator's manual contains specific information on the length and conditions of the hardware warranty. For warranty service, contact your nearest Data I/O Service Center.

Data I/O maintains Service Centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. This includes not only repairs but also calibration of all Data I/O products. A list of all the Data I/O Service Centers is located in the address list at the back of this manual.

1.3.2 Software Warranty Information

You should carefully read the terms and conditions of the software licensing agreement, which was included with your Operator's Manual. Possession of this software product indicates the user's acceptance of these terms and conditions. If you do not agree with them, promptly return the product and the purchase price will be refunded to the original purchaser of this product.

Section 2
Installation/Disassembly

2.1 OVERVIEW

This section describes how to disassemble UniSite for troubleshooting or maintenance work.

WARNING

These procedures MUST ONLY be performed by Data I/O personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

To disassemble UniSite, you will need the following equipment:

- 3/16" thin-walled nut driver or 3/64" allen wrench
- Medium flat-head screwdriver
- Long philips-head screwdriver; minimum 5-inch blade
- Grounded wrist-strap and/or antistatic workstation

2.2 DISASSEMBLY

Table 2-1 lists circuit boards and OEM items, and what needs to be removed in order to gain access to each:

Table 2-1. UniSite Disassembly

ITEM	DISASSEMBLY REQUIRED
PIN DRIVER BOARDS	Top cover; follow subsections 2.2.1 and 2.2.2.
CONTROLLER BOARD	Top cover and Pin Driver boards; follow subsections 2.2.1, 2.2.2. and 2.2.3.
EXPANSION RAM BOARD	Top cover, Pin Driver boards and Controller board; follow subsections 2.2.1 through 2.2.4.
WAVEFORM BOARD	Top cover, Pin Driver boards, Controller board and rear panel; follow subsections 2.2.1 through 2.2.6.
POWER SUPPLY	Top cover, Pin Driver boards, Controller board and rear panel; see subsections 2.2.1 through 2.2.7.
FAN ASSEMBLY	Top cover, Pin Driver boards, Controller board and rear panel; see subsections 2.2.1 through 2.2.7.
DISK DRIVES	See subsection 2.2.7.

2.2.1 TOP COVER REMOVAL

WARNING

To avoid electrical shock, disconnect the power cord before removing the top cover. Do not reconnect the power cord until the top cover has been reinstalled.

1. Place UniSite onto an anti-static workstation.
2. Turn off UniSite's power switch.
3. Remove any front panel modules that may be installed (such as the Site 40 or Chip Site). If you have a blank FSM panel installed, it need not be removed.
4. Remove the power cord from UniSite's rear panel.
5. Using the philips-head screwdriver, remove the two retaining screws, shown in figure 2-1.
6. Remove the top cover by first sliding it toward the front (about 1/4"), then lifting the cover straight up.

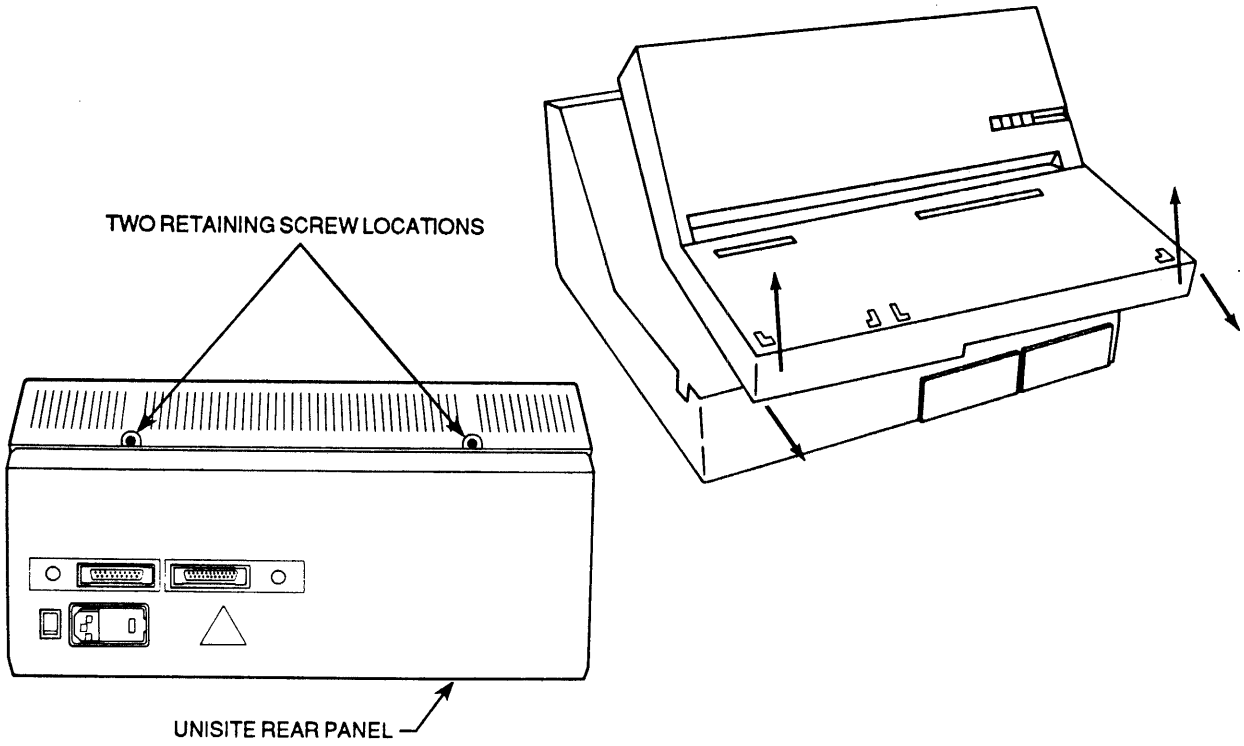


Figure 2-1. Removing UniSite's Top Cover

2.2.2 Pin Driver Board Removal

CAUTION

Many of UniSite's components are static sensitive. Observe standard handling precautions AT ALL TIMES: perform the procedures at an anti-static workstation and wear a grounded wrist-strap; otherwise, damage to the unit may result.

1. Attach your grounded wrist-strap.

2. Remove all of the Pin Driver boards, laying them carefully to the side at the anti-static workstation (see figure 2-2). Special care must be taken not to bend the Controller board's connector pins.

2.2.3 Controller Board Removal

1. Remove the power supply connector cable, located at J22 of the Controller board (see figure 2-2). Squeeze the two locking tabs on either side of the connector to release it from J22.

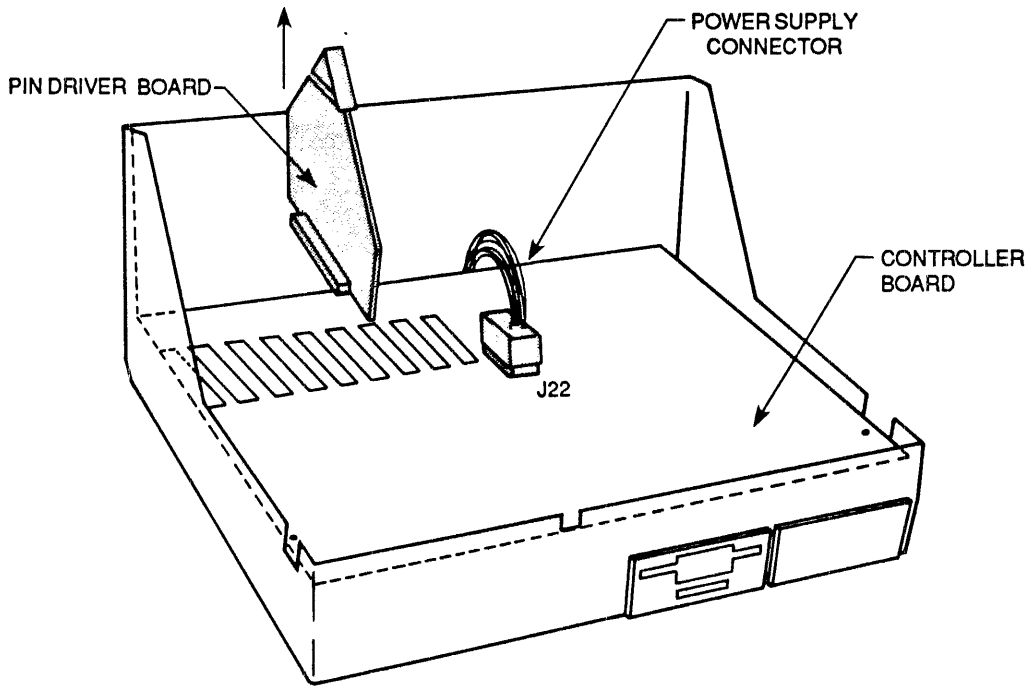


Figure 2-2. Removing the Pin Driver Boards

2. Using the screwdriver, remove the five screws (see figure 2-3). Use the nut driver or allen wrench to remove the four guide pins located at the socket module connectors. If you are using the allen wrench for removal, insert it into the small holes in the sides of the guide pins.

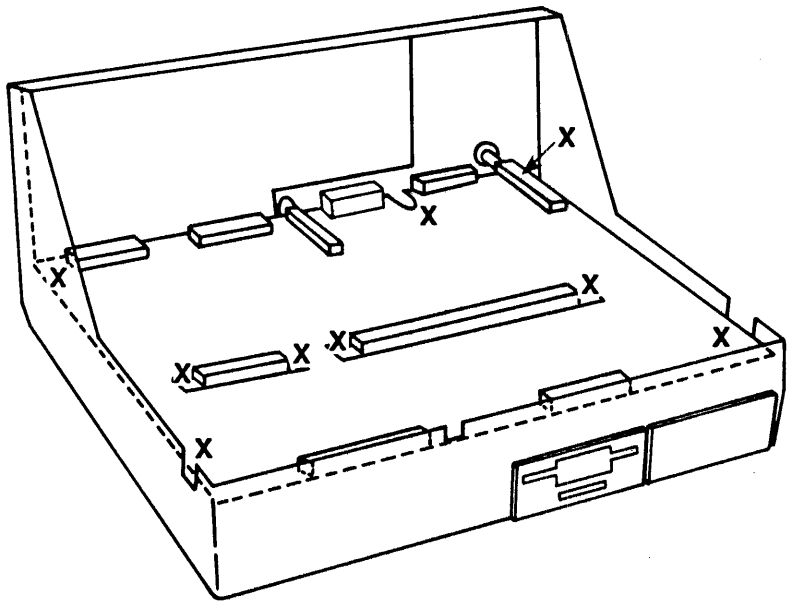


Figure 2-3. Controller Board Retaining Screw Locations

3. Lift up the front edge of the Controller board and disconnect the disk drive cable connector, located at J26 (see figure 2-4). If installed, also remove the Expansion RAM board interconnect cable, J25. Take special care not to lift the board vertically more than about one inch, to avoid damage to the Waveform board's connecter pins.

4. Remove the Controller board from the chassis, carefully pulling it away from the two Waveform board connecters, J1 and J2.

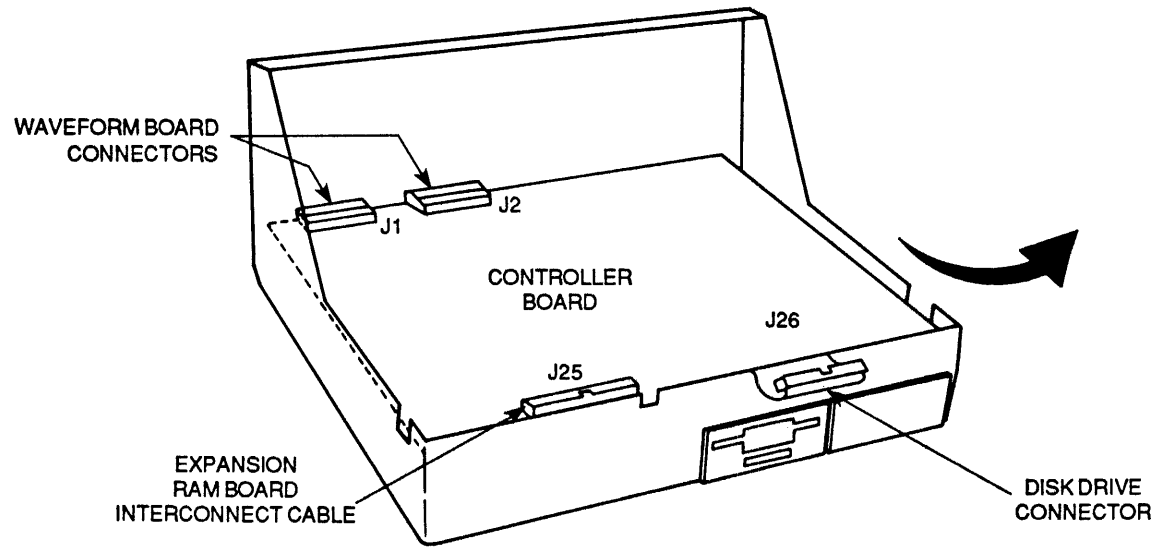


Figure 2-4. Removing the Controller Board

2.2.4 Expansion RAM Board Removal

1. Remove the top cover, Pin Driver boards and Controller board as described in the previous subsections.

2. Remove the four retaining screws shown in figure 2-5.

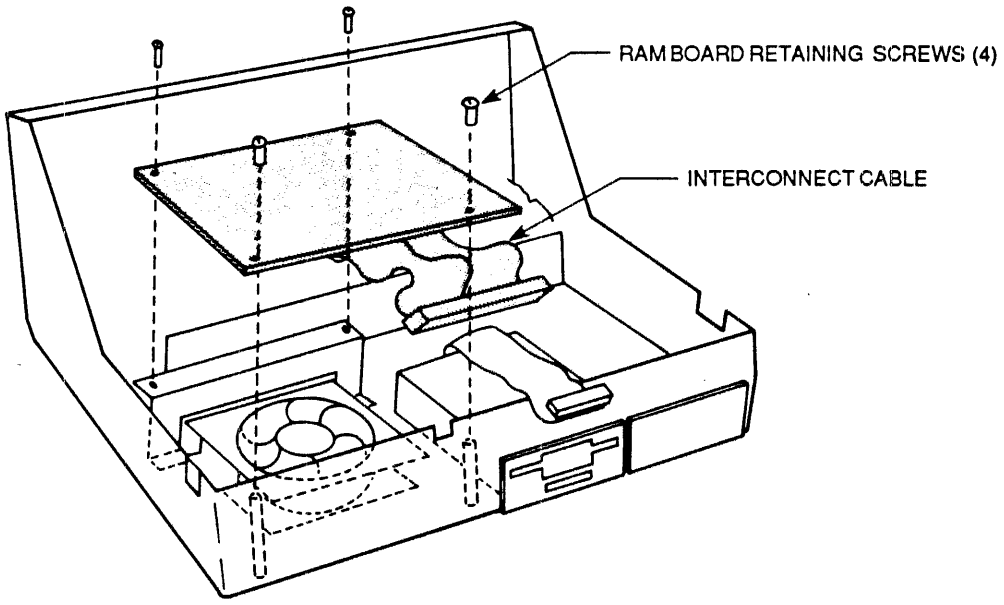


Figure 2-5. Removing the Expansion RAM Board

2.2.5 Rear Panel Removal

1. Remove the top cover, Pin Driver boards and Controller board as described in the previous subsections.

2. Remove the two rear panel retaining screws shown in figure 2-6.

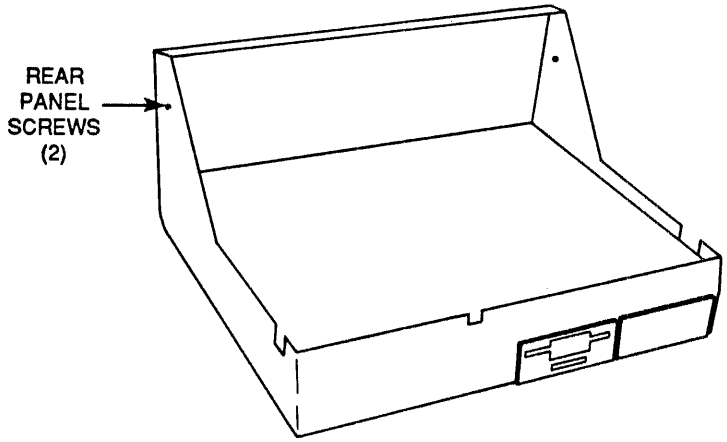


Figure 2-6. Removing the Rear Panel

2.2.6 Waveform Board Removal

1. Remove the top cover, Pin Driver boards, Controller board and rear panel, as described in the previous subsections.

2. The Waveform board need not be removed from the rear panel assembly for troubleshooting or maintenance work.

2.2.7 Other Disassembly

NOTE

The following items are replaced as a whole unit, if faulty. If you have a problem with the disk drives, power supply or fan assembly, simply remove them, contact Data I/O Service and send the item in for servicing. For further information, see section 1 of this manual.

DISK DRIVE(S) REMOVAL

1. Remove the four phillips head screws securing the disk drive to UniSite's chassis.

2. Pull the disk drive out from its receptacle.

3. Disconnect the cables to the power supply and Controller board.

POWER SUPPLY REMOVAL

1. Remove the top cover, Pin Driver boards, Controller board and rear panel, as described in the previous subsections.

2. Remove the interconnect cable to the fan.

3. Remove the four retaining screws located on UniSite's bottom panel.

FAN REMOVAL

1. Remove the top cover, Pin Driver boards, Controller board and rear panel, as described in the previous subsections.

2. If your UniSite has an Expansion RAM board, remove it also at this time: see subsection 2.2.4.

3. a. If your UniSite fan assembly has plastic rivets, remove them as follows: using a slender (#1) screwdriver, push out the four rivets holding the fan assembly to the chassis (see figure 2-7). Push down with the screwdriver at the center of the rivet; when you have pushed it down about 1/8", it can be pulled through the chassis bottom.

   b. If your UniSite fan is held by screws, tip UniSite so that its bottom panel is facing you, and remove the four fan retaining screws.

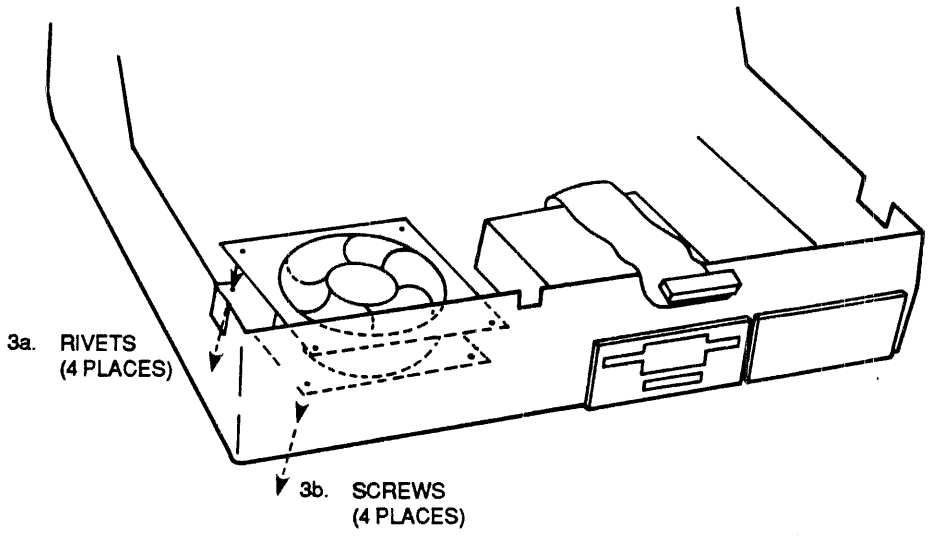


Figure 2-7. Removing the Fan Assembly

2.3 REASSEMBLY

In general, boards may be installed in the reverse order they were removed. Following are some special hints or notes regarding reassembly.

2.3.1 Reinstalling the Expansion RAM Board

Install the Expansion RAM board as follows:

1. Attach the Controller board's interconnect cable to the RAM board.

2. Lay the Expansion board down onto the bracket and standoffs, **component side down** and with the Interconnect cable toward the front. Attach the board to the bracket and standoffs using four screws.

3. Thread the Expansion board and disk drive interconnect cables up and rest them on the front panel.

2.3.2 Controller Board Reassembly

1. Insert the Controller board into the Waveform board connecters. **Again, care must be taken to not bend the Waveform board's interconnect pins.**

2. Insert the RAM board interconnect and disk drive cables into the Controller board. Gently lower the Controller board down into the chassis. Push the extra RAM cable length under the Expansion board, NOT between the Controller and RAM boards.

3. Install the five screws and four guide pins in the order shown in figure 2-8.

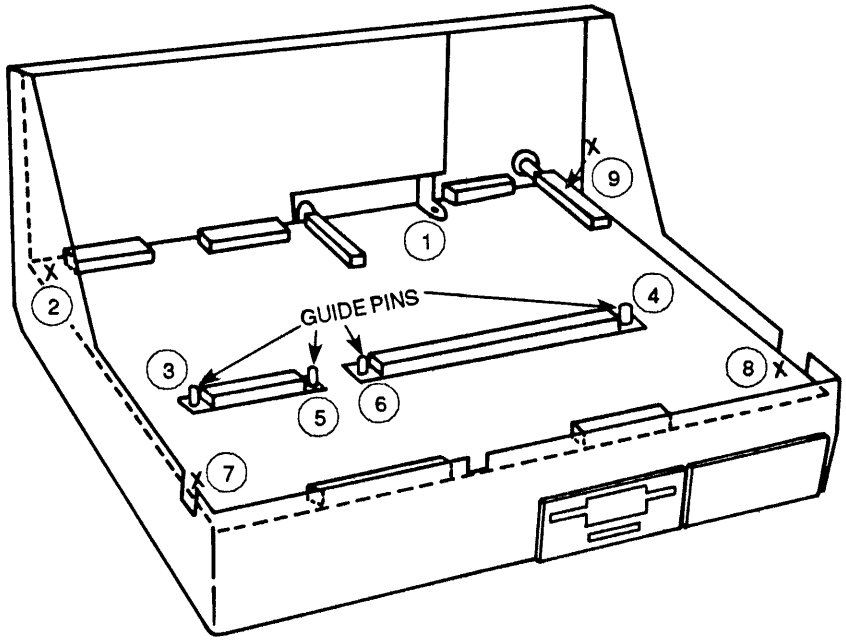


Figure 2-8. Reinstalling the Controller Board

2.3.3 Reinstalling the Pin Driver Boards

CAUTION

Many of UniSite's components are static sensitive. Observe standard handling precautions AT ALL TIMES: perform the procedures at an anti-static workstation and wear a grounded wrist-strap; otherwise, damage to the unit may result.

1. Install the Pin Driver boards with the 68-pin, pin-logic chip facing to the left (see figure 2-9).

2. Take special care and make certain that the Pin Driver board connector is perfectly aligned with the Controller board's connector pins before you push the board down. Use the white stripe on the Controller board as an alignment guide.

   USE EXTREME CAUTION WHEN REINSTALLING THE PIN DRIVER BOARDS: THEY ARE LIKELY TO BE DAMAGED IF INSERTED INCORRECTLY!

3. Insert the Pin Driver boards starting with the J5 connector, and work toward the right. After all the boards have been installed, visually check them, making sure that they are correctly inserted: no pins should be visible at the board's base, and the boards should appear evenly aligned with each other. POWERING UP A UNISITE WITH PIN DRIVER BOARDS INSTALLED INCORRECTLY CAN DESTROY THOSE BOARDS!

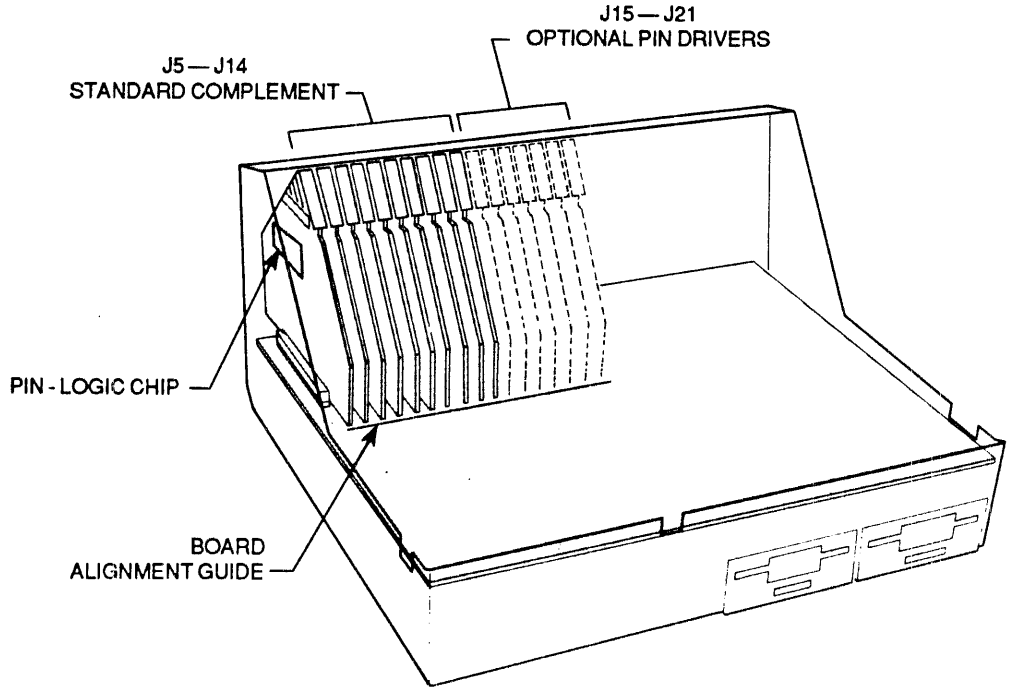


Figure 2-9. Installing the Pin Driver Boards

Section 3
Circuit Description

3.1 OVERVIEW

This section contains the theory of operation for the Data I/O UniSite Programmer. The theory of operation is presented in two descriptive levels, starting with an overall description and block diagram. This is followed by a circuit description and detailed block diagram description of the individual printed circuit boards. Here is a listing of the circuitry discussed in this section:

subsection #	topic
3.2	Description of the overall UniSite system, including a system block diagram.
3.3	Explanation of the Controller board's circuitry. Includes an overall block diagram. Separate discussion and diagram for the pin control unit (PCU) and floppy disk controller.
3.4	Discussion of the Waveform board. Includes both an overall block diagram and drawings for each main circuit.
3.5	Discussion of the Function-Specific Module (FSM) board's circuitry.
3.6	Discussion of the Program-Specific Module (PSM) board's circuitry.
3.7	Explanation of the optional Expansion RAM board's circuitry. Includes a block diagram.

NOTE

Because both the disk drive(s) and the power supply are OEM, their circuitry information is not available for this manual. The Pin Driver boards'circuitry is proprietary and therefore also not described here. The Pin Driver boards are also interchangeable: a faulty one can simply be removed and sent in for servicing. If you should need servicing of either a Pin Driver board or an OEM item, contact your nearest Data I/O Service Center (see list at the back of the manual).

3.2 SYSTEM DESCRIPTION

3.2.1 Overview

The UniSite circuitry consists of the following main components, shown in the system block diagram, figure 3-1.

- CPU
- Pin Control Unit (PCU)
- Pin Drivers
- Dynamic RAM
- 40-pin socket module (Site 40)
- Waveform board
- EPROM
- Power Supply/Fan
- Serial Ports
- Floppy Disk Controller
- PLCC/SOIC socket module (Chip Site)

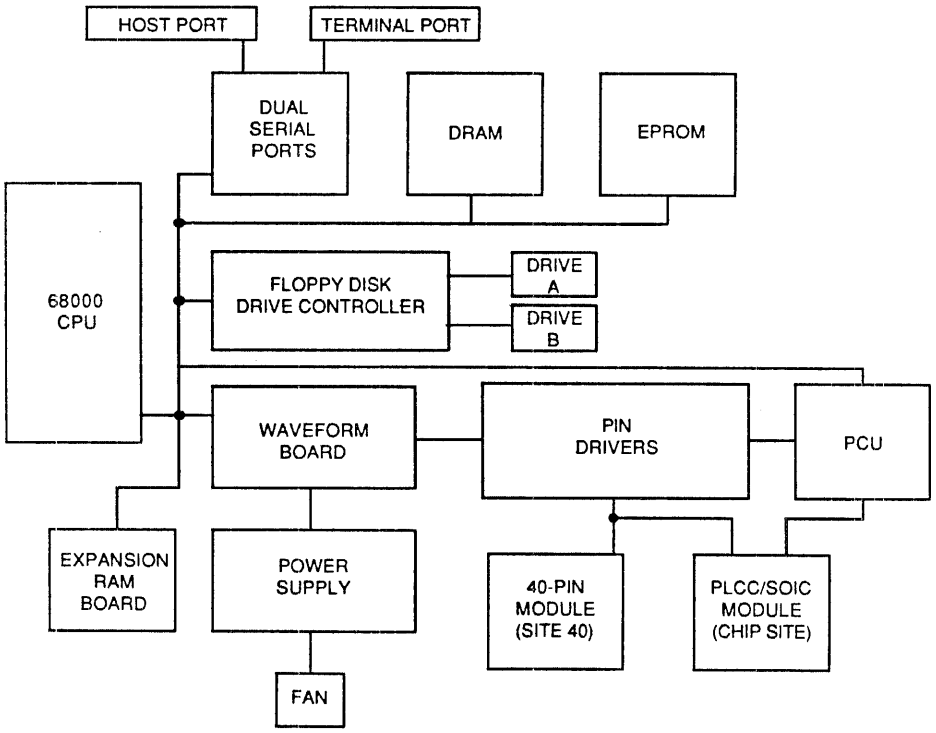


Figure 3-1. UniSite System Block Diagram

3.2.2 General System Description

The central processing unit (CPU) centers around the 10 MHz, 16-bit 68000 microprocessor, which controls all user operations for UniSite. The CPU also has 64K of program memory (EPROM) and 640K bytes (standard) of Read/Write memory (DRAM). System RAM extends from address 080000 to 0FFFFF. User RAM occupies address locations 100000 to 11FFFF. A complete address map is shown in **table 3-1.**

NOTE

Additional information may be found in this manual to supplement this circuit description. Appendix B contains a set of control signal diagrams. Appendix C lists all of the mnemonics (signal line abbreviations) used in the Controller board's schematic, and their meanings.

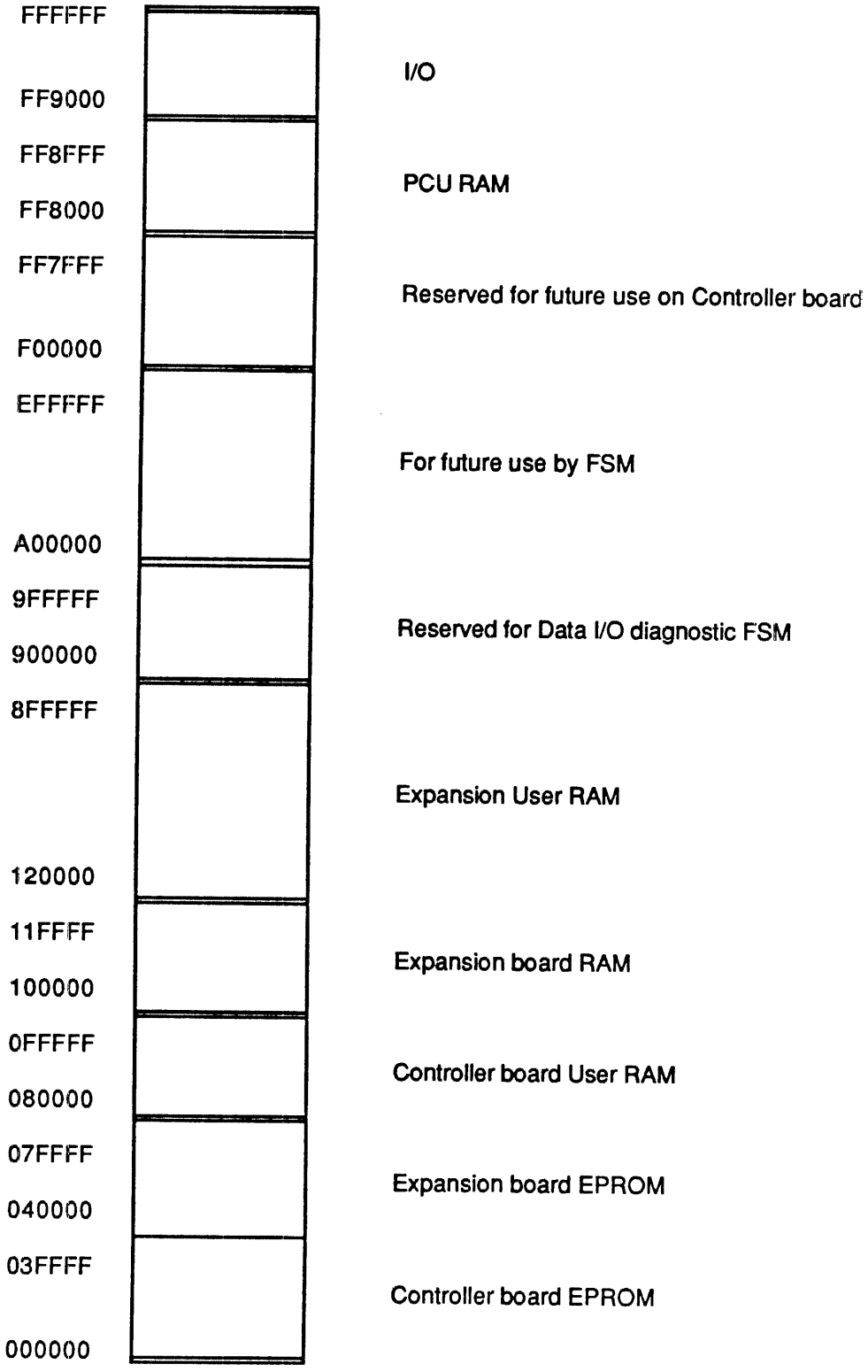
The Controller board contains special digital circuitry which is collectively termed the Pin Control Unit (PCU). The PCU provides an interface between the 68000 and the pin logic IC's on the Pin Driver boards, controlling all the Read/Write operations to the pin drivers.

UniSite's programming hardware is contained in the Waveform board and Pin Driver boards. The Waveform board supplies the necessary voltage and current levels for the pin drivers. The Waveform board is controlled from the CPU. An interconnect diagram is shown in figure 3-2. The Pin Driver boards interface to the PCU and to the Waveform board. Each Pin Driver board has one pin-logic IC and two pin-driver IC's, supporting four device socket pins.

UniSite includes a custom parallel-programming processor, which consists of the PCU and the pin logic IC's on the Pin Driver boards. Each pin logic chip acts as a 32-bit slice of the programming processor. Therefore, a UniSite with 10 Pin Driver boards installed has an effective word-width of 320 bits.

An optional Expansion RAM board is available for UniSite, which expands memory capabilities to over 1 Megabyte. This RAM board may only be installed by authorized Data I/O Customer Support personnel.

Table 3-1. System Memory Map



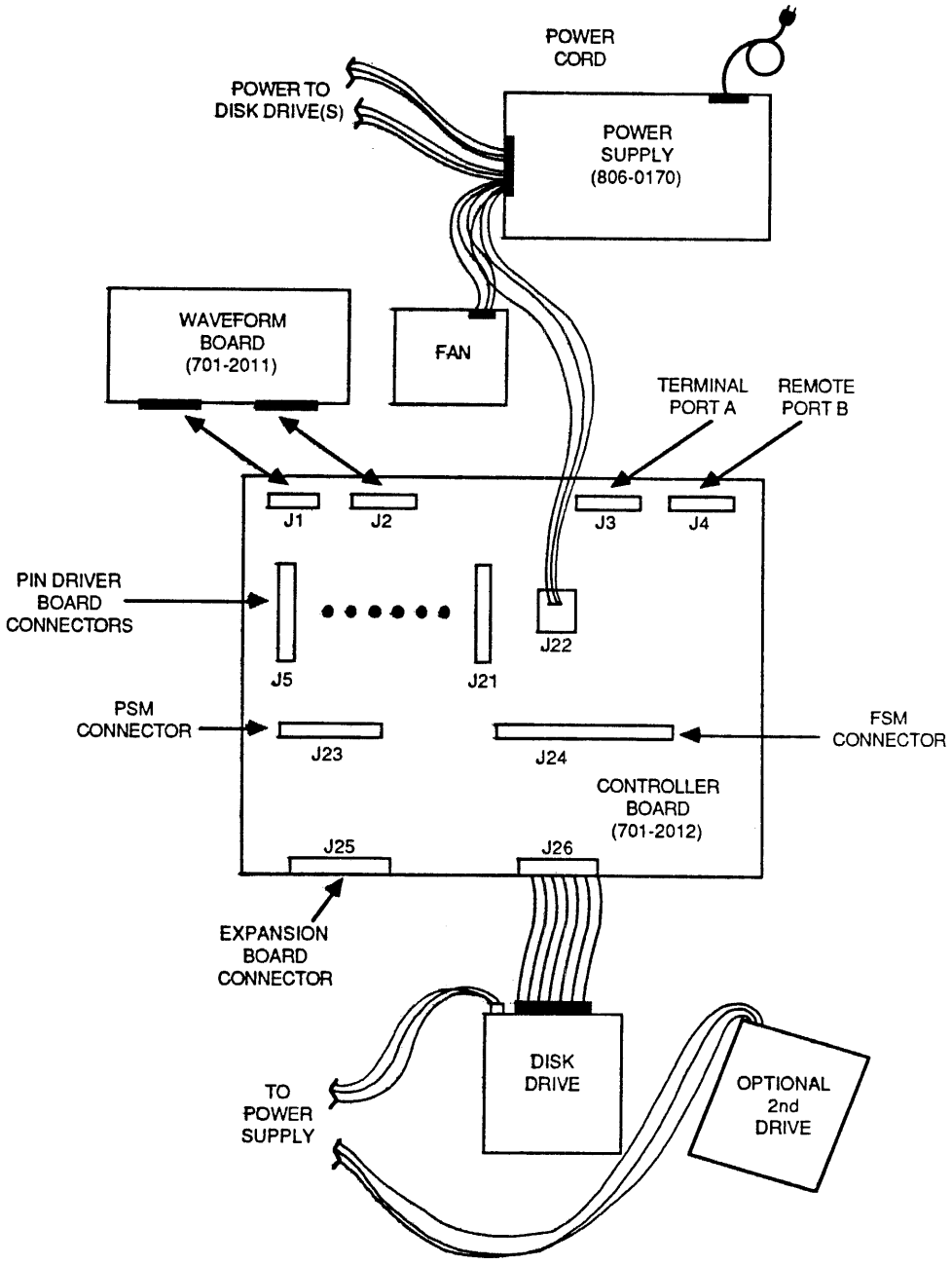


Figure 3-2. System Interconnect Diagram

3.3 CONTROLLER BOARD

UniSite's Controller board (701-2012) circuitry includes the CPU, disk controller, PCU, EPROM and DRAM. A block diagram of the Controller board, figure 3-3, is shown below. A table showing mnemonics for the Controller board (useful when reading the schematic) may be found in appendix C of this manual.

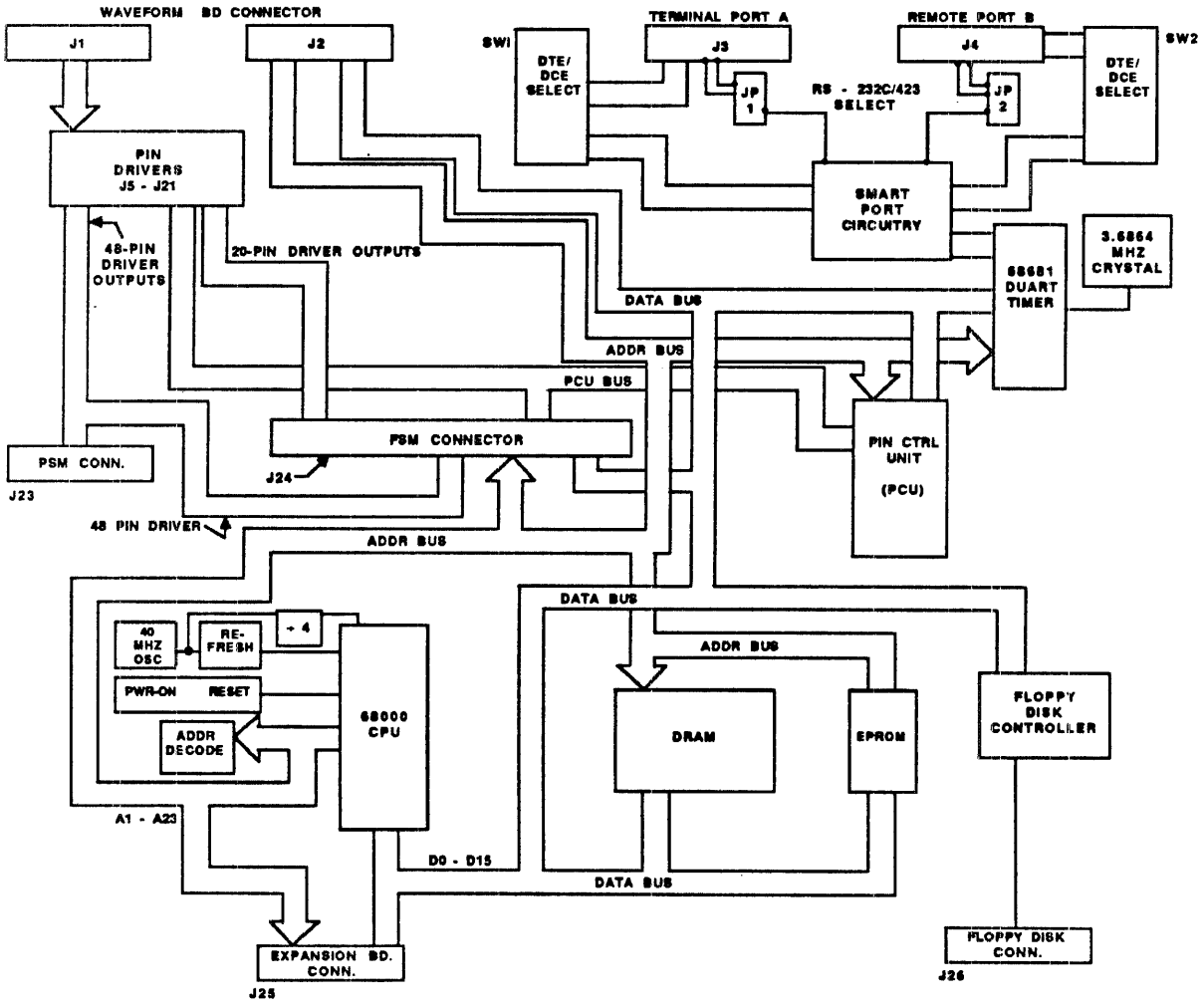


Figure 3-3. Controller Board Block Diagram

3.3.1 Oscillators

The main frequency generator for the controller board is the 40 MHz oscillator, U67. U41 and U66 combine to make the divide-by-5 and divide-by-4 circuitry. The divide-by-5 becomes 8 MHz that drives both the PCU and disk controller; the divide-by-4 becomes the 10 MHz used by the 68000. The 8 MHz generated from the divide-by-5 is further divided by U44, into 4, 2, 1 and 0.5 MHz clocks. These frequencies are for clock signals used when programming microcontroller devices.

The 68681 DUART obtains its clock signal from crystal Y1. The 68681 oscillator's output is also divided by two, then by 256 twice. The resultant frequency is 28.125Hz, which is used as a real time clock interrupt.

3.3.2 Decoding

U91 arbitrates between refresh and normal memory cycles, and provides five RAS decodes. U91 also controls the data bus buffer and the DTACK signal for DRAM and EPROM. U110 provides detection of emulator cycles, ensuring that no glitches occur in RAS/CAS timing when the Controller board is used with an Applied Microsystems 68000 emulator. PAL U92 provides CAS decoding to DRAM, EPROM, the FSM and I/O decodes. U95, U96, U111 and U112 together provide the rest of the system decoding.

NOTE

The emulator's continuous address strobe parameter has to be enabled in order for the emulator to work correctly.

U39 is a shift register used as a delay, which provides timing signals. These signals are used to generate the DTACK signal at the appropriate times, for all devices decoded by U95 and U96. U90 and U93 are address multiplexers for DRAM. U37 and U78 cause the processor to use auto-vectoring during interrupts. (The processor obtains the interrupt vectors from predetermined EPROM locations.) U63 and U64 buffer the data bus onto the controller board from the kernel (68000, DRAM and EPROM).

U94 has a special test shunt, normally installed. When this shunt is removed, it forces the 68000 to execute Move Quick (Read) instructions from all memory address locations. This feature is useful for diagnostic testing of address lines and decoding. While in this condition, the processor executes consecutive Reads throughout the entire memory range.

3.3.3 Dynamic RAM Refresh Circuitry

Dynamic RAM (DRAM) refresh for UniSite occurs every 12 us. Read/Write timing diagrams for dynamic RAM may be found in the Appendix of this manual. U100 takes the 8 MHz from the oscillator circuitry and divides it by 6, yielding 1.33 MHz. U43 works as a delay element to get the 12 us. U43's pin 9 is the refresh request line, and connects to U99. U99 is used to synchronize the refresh cycle with the end of a 68000 bus cycle. U98 establishes refresh timing and is a shift register, with 100ns delay between RAS and CAS refresh. The DRAM uses the CAS-before-RAS refresh mode, and supplies its refresh address internally.

3.3.4. Serial Port Interfacing

Resistors and capacitors on the port connectors prevent damage to buffers when the SmartPort switch is in the wrong position, and also help protect against electrostatic discharge (ESD).

Two zener diodes on each of the drivers (CR1 and CR2, for example) prevent opposing drivers from harming UniSite and provide ESD protection. The 3.3K resistors going into the receivers also protect against ESD. R47 sets the slew rate for the terminal port; R36 performs the same function for the remote port.

68681 DUART

Serial port interface to the controller board is via the 68681 DUART, U14. The DUART contains two independent serial ports, a baud rate generator, 8 parallel output lines and 6 parallel input lines. Crystal Y1 provides a 3.6864 MHz signal, used by the 68681's baud rate generator.

RS-232C AND RS-423 CONFIGURATIONS

Jumpers JP1 and JP2 configurexthe interface for RS-232C and RS-423 operation. In RS-423 configuration, ground lines for each of the drivers are separated from those of the receivers, providing better noise immunity. Pin 9 of the serial connectors is used as the separate receiver ground in RS-423 configuration.

3.3.5 Floppy Disk Control Circuitry

The WD1772 floppy disk controller, U102, provides the interface from the controller board to the disk drives. A block diagram of the disk control circuitry is shown in figure 3-4.

Data and control signals from the 68000 are routed to the 1772 and to an 8-bit latch, U103. From there, signals are either fed through buffer U115 or through NAND gates to J26, the disk drive connector. Buffer U104 feeds back disk drive information to the 1772.

Four of the disk controller circuitry's signals are logically AND'ed with the Power-loss Write Protect signal, ensuring that no disk Write operations occur during power up and power down. The four NAND'ed inputs are WG and WD (Write Gate and Write Data) from the 1772 and DRIVE0 and DRIVE1 from latch U103.

Buffer U115 takes Step and Direction signals from the 1772, and Side and Motor-on signals from latch U103. Output from U103 are signals MOTON-, DIRIN-, STEP- and SIDE1-. These signals tell the disk drive to turn on, tell the drive head which direction to go and tell it which side to read.

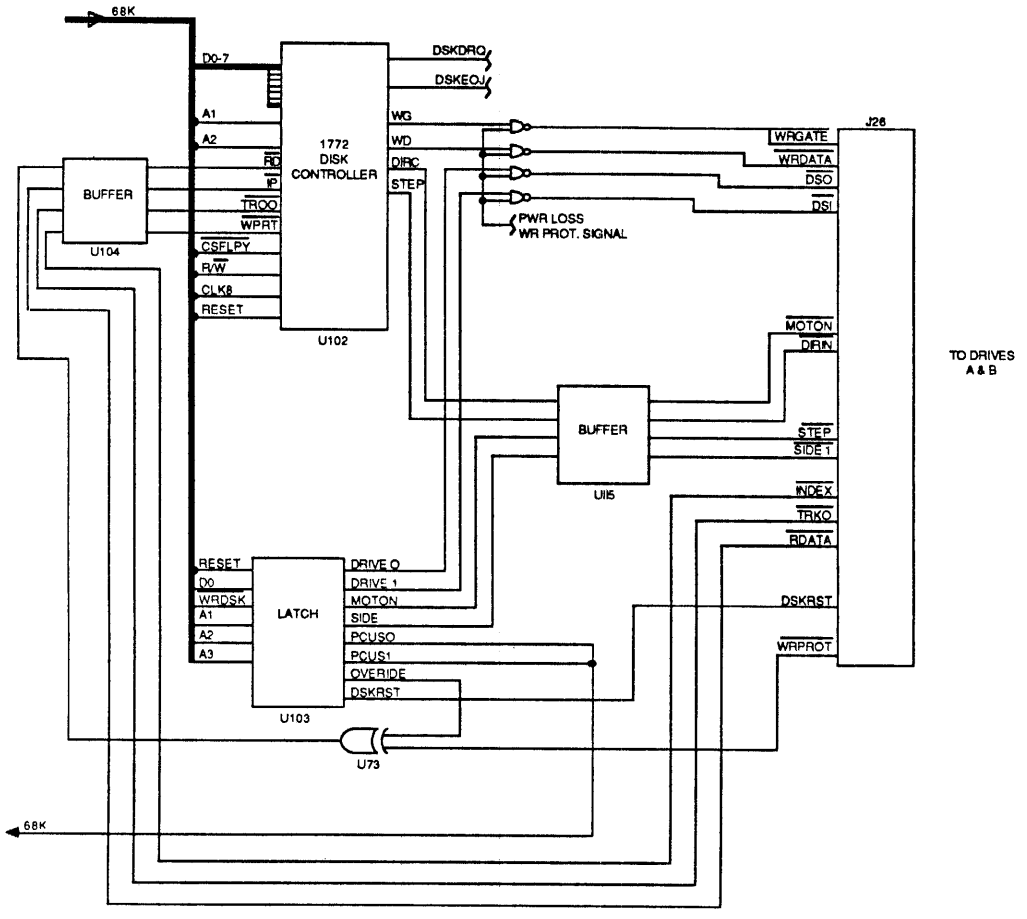


Figure 3-4. Floppy Disk Control Circuitry

3.3.6 Pin Control Unit (PCU)

The Controller board's PCU performs all the Write operations to the pin logic IC's on the Pin Driver boards. The pin logic IC's, in turn, control the pin drivers. The block diagram, figure 3-5, shows the major components of the PCU. Both the PCU's hardware and software will be discussed in this subsection. The hardware discussion includes address decoding and signal routing to the Pin Driver boards. The software description explains some of the PCU's internal functions; how commands are interpreted by the PCU via the 32-bit instruction word. Because of the proprietary nature of the pin logic IC interface, a detailed software description is not available.

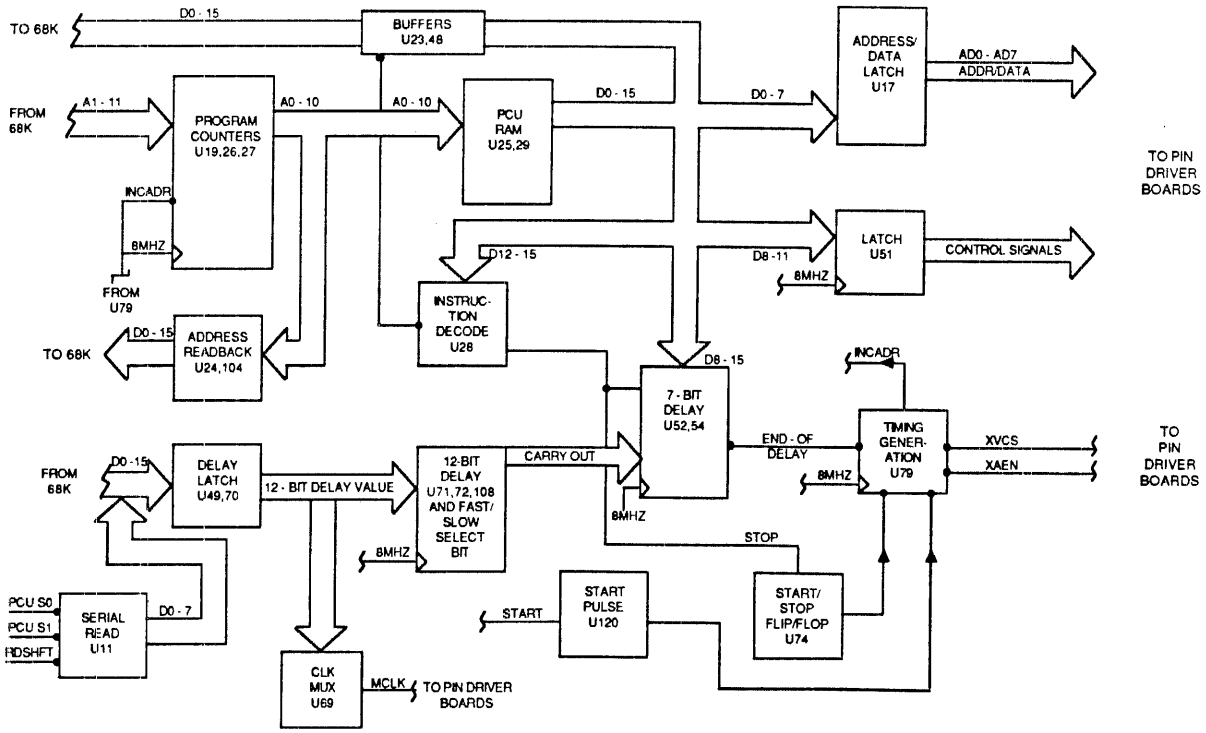


Figure 3-5. PCU block diagram

PCU RAM

The PCU's memory consists of two 2K x 8 static RAMs, U25 and U29. PCU RAM resides at addresses FF8000-FF8FFF in the microprocessor's memory map (see table 3-1).

Commands are sent to the pin logic IC's via a 32-bit instruction word, stored in U25. 16 bits of information are sent out at a time onto the PCU bus. **Figure 3-6** shows a sample timing diagram for the PCU driver bus. When the XAEN line is low (logic "0"), 16 bits of address instruction information are sent out on the pin driver bus. When the XVCS line is low, the other 16 bits are sent out. Read/Write timing for the PCU RAM is available in Appendix B of this manual.

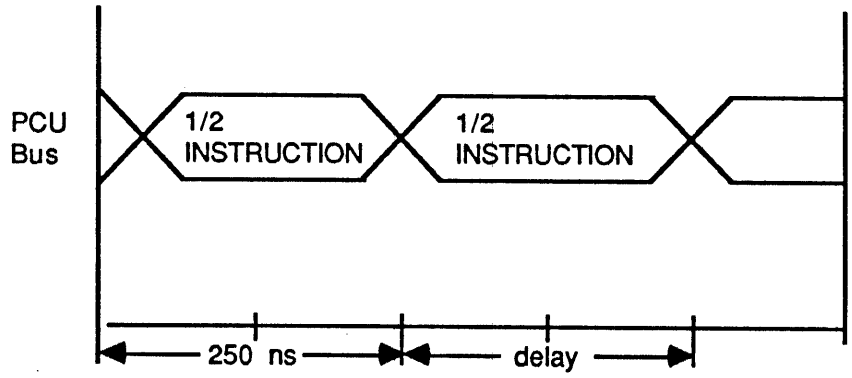


Figure 3-6. PCU Timing Diagram

ADDRESS AND DATA WORD INSTRUCTIONS

Latch U17 multiplexes instructions from PCU RAM, U25. The resulting AD0-AD7 are then buffered by U9 and U15 and passed through impedance-matching resistors. These resistors--R4, 60, 62, 66 and 72--help match impedance between the transmission line and the two buffers, to minimize over- or undershoot. Buffer U9 outputs are routed to the internal pin driver bus (IPD); U15's outputs go to the FSM's pin driver bus (FPD). U21 reads back AD0-AD7 to the 68000. U4 and U5 are wire-OR'ed, making the IPD and FPD busses appear to the system as just one bus.

DELAY WORD

The 8-bit delay portion consists of one timing bit, FS, and a 7-bit delay value. The PCU uses either a 7-bit or a 19-bit delay circuit, depending on the programming time of the socketed device. If the FS bit is a logic "1", then the fast (7-bit) delay is selected; "0" selects the slow delay (the 7-bit PLUS the 12-bit delays).

The 4-bit counters used in the delay circuit are synchronously clocked from the 8 MHz PCUCLK signal. A shift register, U11, is used to read serial information via the pin driver boards, and works with serial-oriented devices. The pin driver boards' CMP line is fed into U11 through its two serial-input lines, SL and SR. The I/O decoder, U112, enables the data from the shift register, U11. This data is then put onto the 68000 bus via the RDSHFT line. Two inputs from the processor, PCUS0 and PCUS1, direct U11 to shift either left or right.

When the 68000's PCUDLY line goes high, delay and clock select information is loaded into U49 and U70. The delay consists of an 8-bit output from U49 coupled with 4 bits from U70. This 12-bit delay is then sent to U71, U72 and U108. The remaining 4-bits from U70 are used to select one of the available clock sources. U69's output, XPCLK, is used as a clock signal. This signal is used by UniSite either when programming microcontrollers or when using test vectors.

Logic circuitry takes the output from the 7- and 12-bit delays and functions as a slow or fast counter, depending on the delay required. When the delay period has cycled through, the EVOKE line is pulled low. This tells U79 to start the next instruction. U79 is a shift register, functioning as a timing generator. U79 synchronizes address/data to the pin drivers.

3.4 WAVEFORM BOARD

The primary function of the Waveform board is to produce several individually controlled voltages for use by the pin drivers. These voltages provide the pin drivers with power to operate, they serve as reference levels to control the pin drivers, and provide voltages which are either re-regulated and applied to the part being programmed or switched there directly.

3.4.1 Address / Decode

Each output on the Waveform board has a specific address location, shown in table 3.2. Decoding is done in the following manner.

The Controller board's CSWFB- line, J2 pin 6, is the main Waveform board enable signal. It becomes active when valid addresses whose most-significant four hexadecimal digits equal FFB8 are issued by the controller. The two least-significant digits of the six-digit hex address are decoded by the decode PAL, U24.

The decode PAL uses R/W-, CSWFB-, and A2-A8 as inputs to generate 10 decode signals which form the Decode bus. These signals provide enables to all memory-mapped devices on the board.

TABLE 3.2 Waveform Board Read/Write Addresses

WRITE ONLY addresses:

FFB800	Cmpref
FFB804	DUTVCC
FFB808	Ref 1
FFB80C	Ref 2
FFB810	Ref 3
FFB820	V+
FFB822	V-
FFB824	VLH
FFB826	VLL
FFB828	FCHR
FFB82A	FCLR
FFB82C	FCLC
FFB82E	FCHC
FFB830	CC (Coarse Current)
FFB832T	Vslew
FFB834	Future use (always set to 0)
FFB836	Clamp
FFB83C	Output Latch (U14)

READ ONLY address:

FFB8F8	Comparator Latch (U3, U4)

3.4.2 Data Bus

The 16-bit data bus (D0 through D15) is used to carry binary data from the controller to each of the eight DAC IC inputs and the output latch, U14. It also carries information from the comparator latches (U3 and U4) to the controller.

The data Buffers (U11 & U12) isolate the Controller board's data bus from the Waveform board's data bus. They are enabled by a low level on the CSWFB- signal. The direction of these buffers is controlled by the inverted R/W- signal. A low on the direction input defines the "B" side of the buffers as inputs and the "A" side as outputs; a high reverses this direction.

3.4.3 Power Supply System

The Waveform board receives its power from four of the five system power supply's outputs. These are used directly and re-regulated to lower levels for use on the Waveform and Pin Driver boards.

RAW VOLTAGES

The system power supply outputs go directly to the Controller board. From there, the +5, +21, -15, and +48V outputs are routed to the Waveform board connectors.

RE-REGULATED VOLTAGES

The +21V supply is re-regulated to +15V, +18.5V, and the 21PR voltage. This re-regulating is done in the following fashion.

+15 and +18.5 Voltages: These voltages are produced by single three-terminal, series regulators, VR2 and Q5.

21PR Voltage: This voltage has two levels, depending on the state of the Output Latch (U14) pin 16. When this output is in the TTL Low state, Q6 is turned off. This allows R119 to pull the base of Q39 to approximately +22 V. This, in turn, produces a voltage of approximately +20V on the 21PR output.

By setting pin 16 of the output latch to a TTL high, Q6 is turned on. When this occurs, the anode of the zener diode (CR1) is pulled to ground, which sets the base of Q39 to approximately 13V. Since Q39 is a darlington transistor, the emitter will then be held at about two volts less than its base; about +11V.

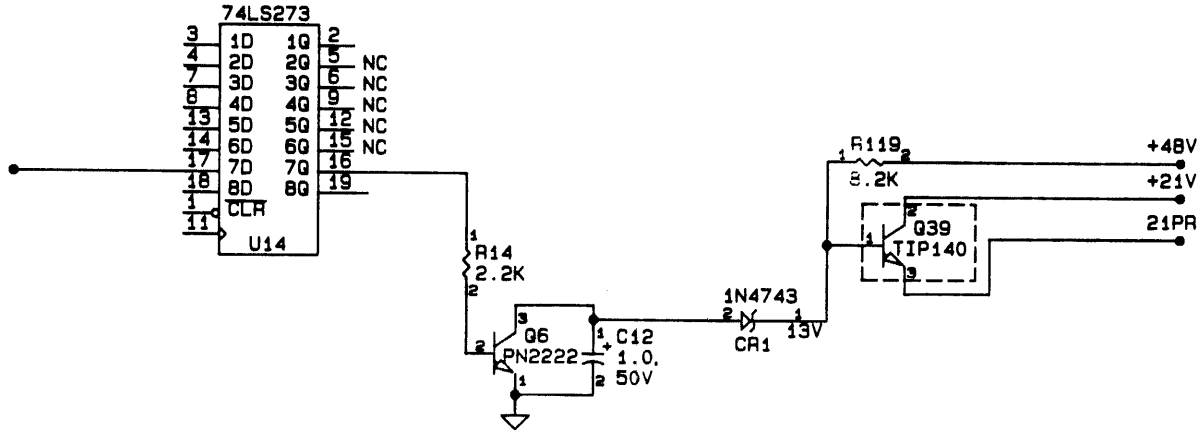


Figure 3-7. 21PR Supply

The +48V supply is re-regulated down to +40V using a discrete regulator circuit:

+40 Volts: This is a precision voltage source (+_1.5%). The collector of the darlington power transistor (Q48) is held at +40V in the following manner. The collector voltage of Q48 (+40V output) is divided by four, using the voltage divider network formed by R165 and R166. When the +40V from the output is present at this divider, the resulting +10V level is produced and applied to the positive input of op amp (U30 pin 3).

The negative input of this op amp (pin 2) is held at +10V by the precision reference. The op amp output (pin 1) voltage adjusts the anode of the 43V zener diode (CR35) within the +1V to -3V region. The cathode of CR35, in turn, adjusts the base of Q48 to a voltage which holds the collector of Q48 to the desired +40V level.

An overcurrenttrip circuit is incorporated at the emitter of Q48, which includes R88, R183, R169, and Q53. The action of this circuitry is typical of the overcurrent circuitry described at the end of this section.

R184 is used to provide current to CR35. CR40, CR43, and CR44 ensure that the op amp is supplied with enough operating voltage in the event that +21V is not present. This condition may occur upon system power up or power down. CR31 ensures that the +40V supply goes no lower than about +4V when an overcurrent condition turns the +40V supply off. This is done to prevent damage to the semi-custom linear IC on the Pin Driver boards.

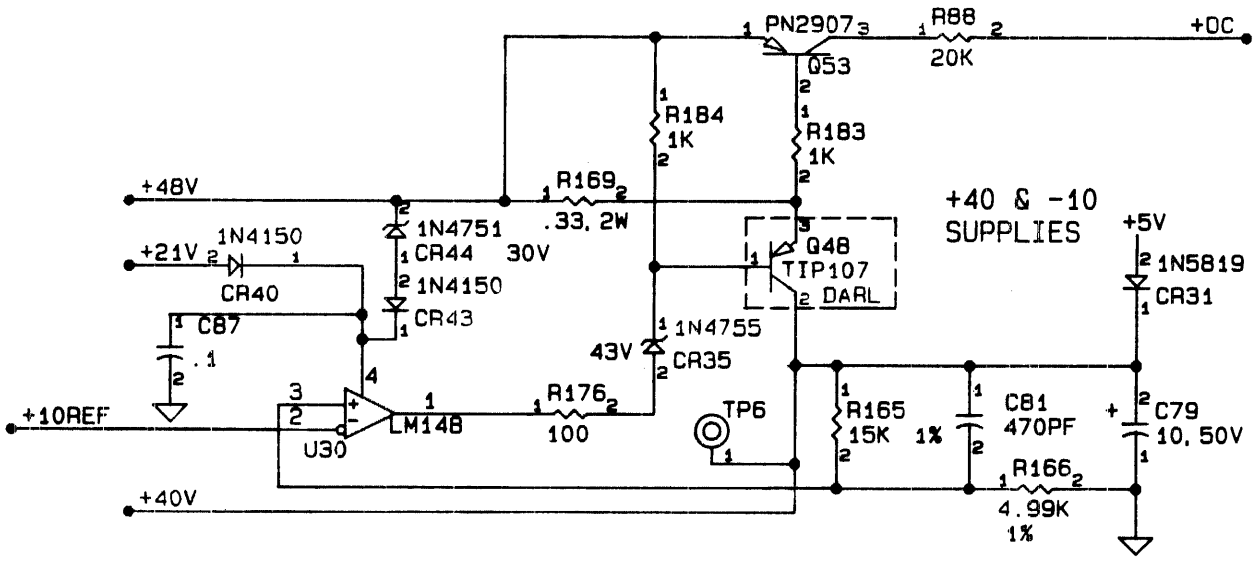


Figure 3-8. +40V Supply

The -15V supply is re-regulated down to -5 and -10V:

-5 Volts: This voltage is produced by a single three-terminal series regulator IC, VR3.

-10 Volts: This voltage (+_2%) is developed at the collector of the darlington power transistor (Q49) in the following manner.

The collector voltage of Q49 (-10V output) is applied to a voltage-divider network, composed of 10KΩ resistors (R178, 177). The other end is connected to the precision +10V reference. The resulting voltage of this divider is a halfway point between the end points; nominally 0V. This level is then applied to the positive input of the op amp (U30 pin 12). The negative input of the op amp (pin 13) is tied to analog ground, which is a sense of the actual programming site's ground. The cathode of CR34 is driven by the output of the op amp (pin 14). The anode of CR34 then adjusts the voltage at the base of Q49 such that a regulated -10V is developed at the collector.

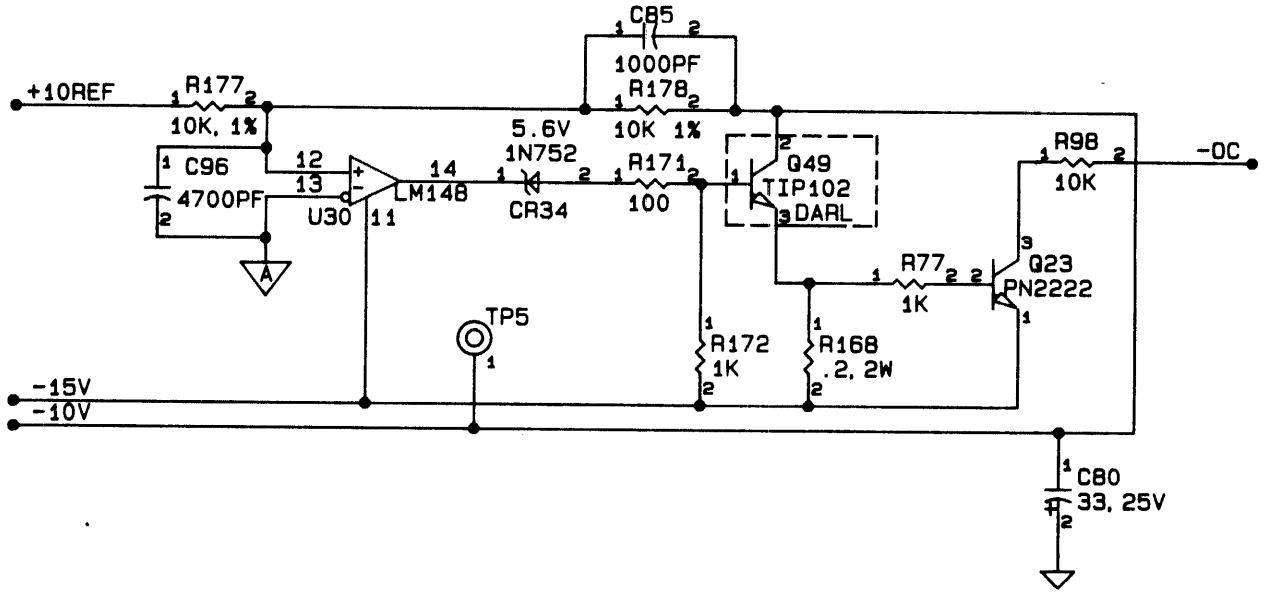


Figure 3-9. -10V supply

GROUNDING SYSTEM

It is important to note the difference between the two ground nodes used on the Waveform board: "PGND" and "AGND". PGND is the "power ground", serving as the return current path for all of the analog circuitry on the Waveform board as well as the rest of the system. AGND is a sense line. In normal operation, this line is connected to PGND by the Programming Module, installed on the front of UniSite. In the event that this connection is not made, which may be the case when servicing the system, a 100Ω resistor, R49, will make this connection. This resistor is not small enough to allow the system to calibrate without either an FSM or a PSM installed.

WAVEFORM BOARD OUTPUTS

This subsection describes in detail the purpose, the output range and the circuit operation of each individual Waveform board voltage source.

Reference 1, 2, and 3.

Purpose:
These voltages are used as input to the pin driver's voltage source circuit.

Output range:
The voltage level of all three of these outputs swings between +5 and -10V.

Circuit operation:
Because these three supplies vary so little from each other, a description of the Reference 1 supply will be given and will apply to the operation of all three.

The output of DAC IC U7 (figure 3-10) is converted to a voltage by the LM148 op amp, U20. This voltage is applied to R56. Since the "+" input of U20 (pin 5) is connected to ground, the op amp will adjust its output to hold the "-" input (pin 6) at the same ground potential. This is done in the following manner.

The "-" input (pin 6) of the op amp is connected by R56, R57, and R58 to three different voltage levels. R57 always pulls the input to the +10V level, while R56 compensates by always pulling to the negative level set by the DAC output. It is these two resistors that allow (by varying the DAC voltage) the "-" input voltage to be set at either a positive or negative level. R58 supplies the feedback current from the op amp output required to hold the op amp inputs at the same potential. When the DAC voltage rises, the "-" input also rises. As a result, the op amp output lowers its voltage, allowing R58 to pull the input back down to ground potential. C58, which is placed across R58, stabilizes the op amp, eliminating oscillation.

Two voltage comparators of U17 are connected to the op amp output. They are used to indicate when the output crosses either the +10V level or the -5V level.

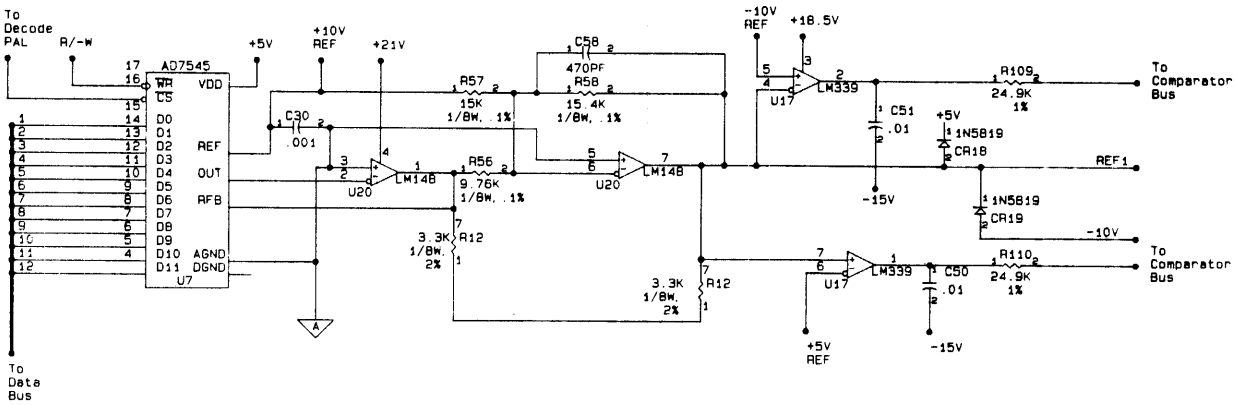


Figure 3-10. Ref 1,2, and 3

Comparator Reference

Purpose:
The output of this circuit is used exclusively by the Waveform board's comparator inputs.

Output Range:
-10V to +15V.

Circuit Operation:
The output of DAC U5 (see figure 3-11) is converted to a voltage by the LM148 op amp, U19 at pin 1. This voltage is applied to R46. Since the "+" input of U19, pin 3, is connected to ground, the op amp will adjust its output to hold the "-" input,pin 2, at the same (ground) potential. This is done in the following manner:

The "-" input (pin 6) of the op amp is connected by R46, R47, and R48 to three different voltage levels. R47 always pulls the input to the positive 10V level while R46 compensates by always pulling to the negative level, set by the DAC output. By varying the DAC voltage, these two resistors allow the "-" input voltage to be set at either a positive or negative level. R48 supplies the feedback current, from the op amp output, required to hold the op amp inputs at the same potential.

When the DAC voltage rises, the "-" input also tries to rise. As a result, the op amp output lowers its voltage, allowing R48 to pull the input back down to ground potential. C54, which is placed across R48, stabilizes the op amp to eliminate oscillation.

Two voltage comparators of U18, are connected to the op amp output. They are used to indicate when the output crosses either the +10V level or the -10V level.

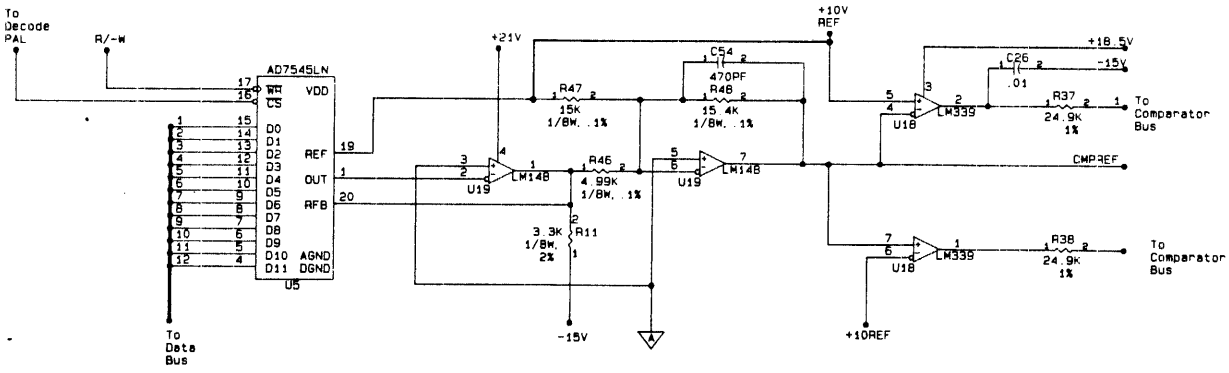


Figure 3-11. Comparator Reference

VCC

Purpose:
This circuit supplies voltage directly to the Vcc pin of the programmable device, when the appropriate Vcc relay is closed on the programming module.

Output range:
No load: -10V to +20V.
Full load: (2.5 amps) -6V to +15V.

Circuit operation:
The output of DAC U6 (see figure 3-12) is converted to a voltage by the LM148 op amp, U19, at pin 14. This voltage is applied to R148. The output voltage is developed by adjusting the voltage drop across the D44H11 and D45H11 output transistors, Q43 and Q44. The op amp (U29) output voltage applied to R154, establishes the op amp output current from either the positive or negative supply. It is this current, when directed through R152 or R151, that controls the Vcc voltage level.

Since the op amp's "+ supply" current must flow through the 160Ω resistor R152, (assuming Q32 is off) the resistor will develop the voltage required to turn Q35 on. This causes the collector of D44H11 to pull up to a positive voltage.

The reverse in operation occurs when the op amp's output voltage is a negative value. The op amp output current flows through R151 (assuming Q29 is off), which develops the voltage required to drive Q34. This causes the collector of Q43 to pull to a negative voltage.

The change of Vcc output voltage is sensed by the VCCSEN signal. The VCCSEN signal is normally connected to the Vcc output at the programming site on the programming module, but if the module is not installed, the VCCSEN signal is connected to the Vcc output via the 100Ω resistor R145.

When the DAC voltage tries to change the op amp's "-" input, the resultant change in Vcc and VCCSEN counteracts this change by applying an opposing voltage to the "-" input through R149. This satisfies the op amp's requirement to keep both "+" and "-" inputs at the same voltage level, while changing the output voltage to its new level.

Operation of the Vcc supply depends both Q32 and Q29 being off. This is not the case when the over-current circuit has tripped. When this happens, the LM339 inputs, U18 pin 8 and U26 pin 9 go low. Since the other inputs on these comparator are connected to a 2.5V level, divided between +5V and ground by R131 and 132, the output of U26 lowers and the output of U18 rises from the -15V rail to ground. This turns on both Q32 and Q29, shorting out R151 and R152, which shuts off the entire Vcc supply.

Reference 0

Purpose:
The pin driver's circuitry requires that one of the Reference outputs (0 through 3), tracks the voltage level on the Vcc supply output. Like the Reference 1, 2, and 3 sources, Reference 0 is another input to the Pin Driver board's voltage source circuit. The difference is that this reference voltage tracks the Vcc supply output, and is not independently adjustable.

Output range:
-3.75 V to +1.5 V.

Circuit operation:
The Vcc supply output voltage (see figure 3-12) is divided down to 1/3 of its value by R115 and R116. This voltage is applied to the inverting, unity-gain amplifier circuit, R120, R103, and pin 6 of U16. This supplies the pin driver with a reference which is 1/3 the voltage of Vcc, and opposite in polarity. CR15 and CR17 are clamp diodes.

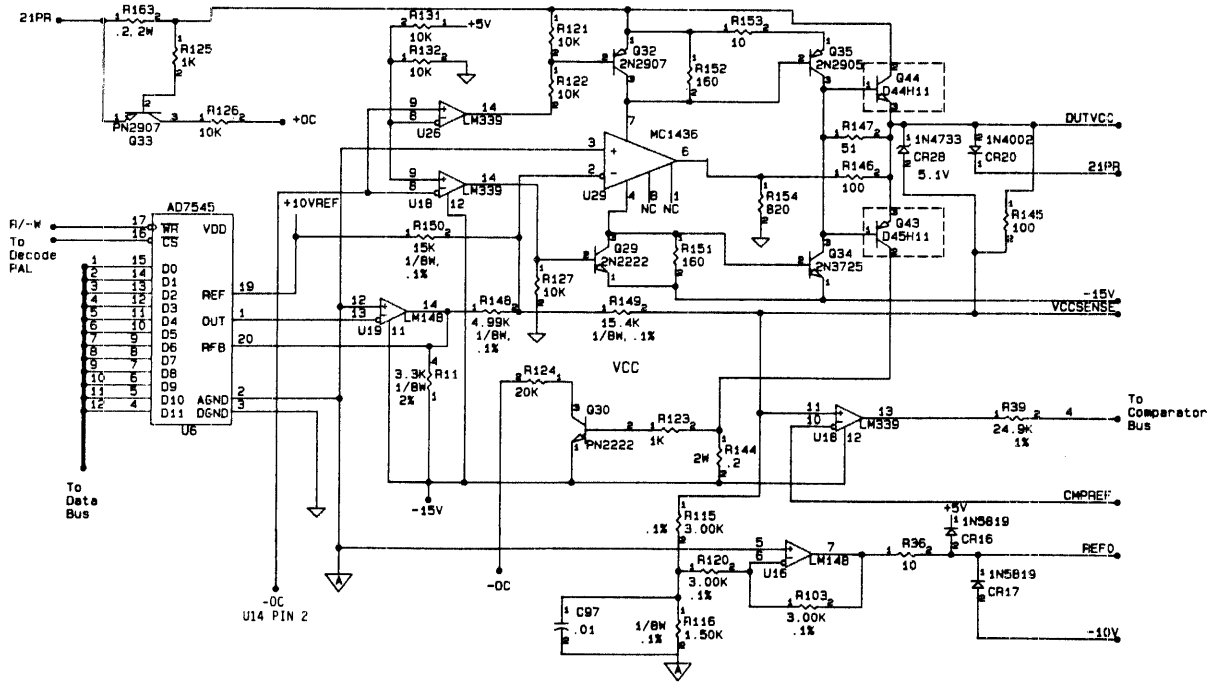


Figure 3-12. Vcc and Ref 0 Supplies

V+

Purpose:
This output is the positive power supply to the pin drivers' voltage source, located on the Pin Driver board.

Output range:
Full load: 0V to +37V
No load: 0V to +40V

Circuit operation:
DAC U23 pin 2 outputs its voltage level to the "-" input of op amp U30, pin 9 (see figure 3-13). The voltage at the "+" input, pin 10, is set to 1/4 of the V+ output voltage by the resistor divider network, R180 and R185.

To turn the output transistor on, its base voltage need only drop to 0.6V below the +48 supply voltage. Since CR38 is a 47V zener diode, the output transistor will turn on when the op amp output voltage is at, or below, about 0V.

As the DAC voltage rises, the op amp output voltage will drop, which raises the V+ output voltage (collector of Q45). The V+ voltage is fed back to the "+" input of the op amp, to balance its input voltages.

The +OC signal goes high when too much V+ output current is sensed by R162 and the overcurrent transistor, Q28, turns on. The output voltage of this supply is sensed by the "+" input of U28 pin 5. It is compared against the COMPREF signal. The output connects to the comparator bus.

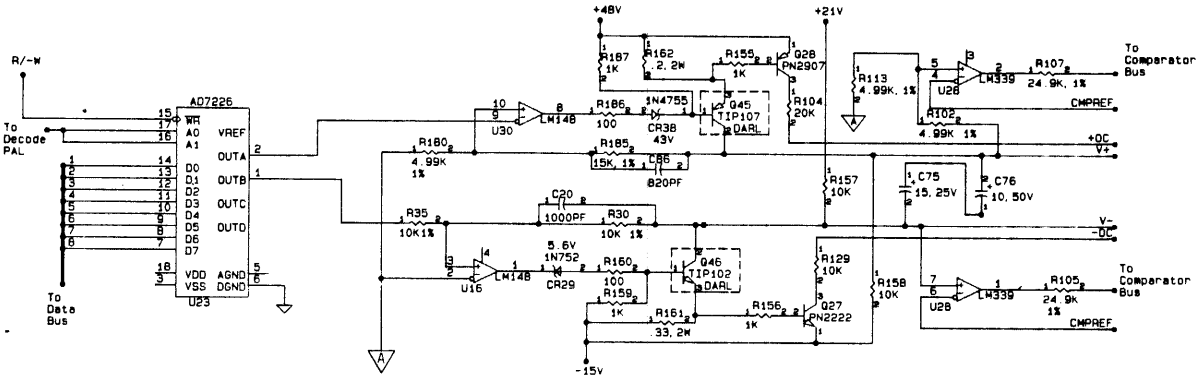


Figure 3-13. V+ and V- Supplies

V-

Purpose:
This output is the negative power supply to the pin driver voltage source, located on the Pin Driver board.

Output range:
-10V to 0V

Circuit operation:
The "-" input of the op amp, U16 pin 2, is connected to ground (see figure 3-13). As the DAC voltage changes, the V+ output voltage will change to a level that is equal and of opposite polarity, to maintain the "+" input (pin 3) at 0V.

To turn the output transistor on, its base voltage need only rise to 0.6V above the -15 supply voltage. Since CR29 is a 5.6V zener diode, the output transistor will turn on when the op amp output voltage is at, or above, about -9V.

As the DAC voltage rises, the op amp output voltage will rise. This causes the V- output voltage (collector of Q46) to drop. The V- voltage is fed back to the "+" input of the op amp to balance its input voltages.

The -OC signal goes low when too much V- output current is sensed by R161 and the overcurrent transistor, Q27, turns on. The output voltage of this supply is sensed by the "+" input of U28 pin 7. It is compared against the COMREF signal. The output connects to the comparator bus. A 15 µF capacitor is connected to the output for stability and filtering.

Over-voltage Crowbar:

Purpose:
In the event of a hardware failure, the over-voltage crowbar circuit will ensure that the maximum difference between +V and -V never exceeds 42V. If this voltage were to exceed 42V, all of the pin drivers installed in the system could potentially be damaged.

Circuit operation:

R95 and R96 set the TL431, Q24, making it act as a 36V zener diode. The +V and -V outputs are applied across R118, CR10, and Q24. When the voltage exceeds the sum of the two zener voltages of CR10 and Q24, current will flow through R118. This voltage triggers the TRIAC, and it clamps the two supplies together. This results in either an overcurrent condition or a complete shut down of the system, depending on the source of the problem.

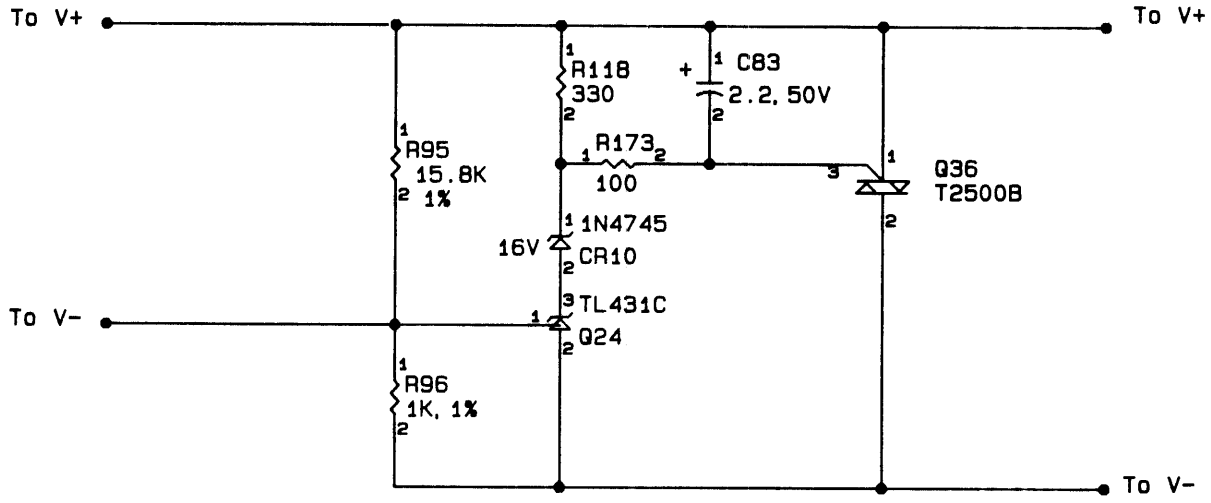


Figure 3-14. Over-voltage Crowbar Circuit

VLH:

Purpose:
This supply provides power to the logic driver circuit on the Pin Driver boards.

Output range:
Full load: 0 to +20V
No load : 0 to +17.5V

Circuit operation:
The DAC output (see figure 3-15) is connected to the "-"input of the LM148 op amp, U16 pin 9. When this voltage is increased, the op amp output decreases. This raises the VLH output (collector of Q40) to a higher voltage. This voltage is sensed by the "+" input of the op amp through R33, to balance the op amp input voltages. The +OC signal goes high when too much VLH output current is sensed by R142 and the overcurrent transistor, Q26 turns on.

The output voltage of this supply is sensed by the "+" input of the LM339, U28 pin 9. It is then compared against the COMREF signal. The output connects to the comparator bus. A 15 µF capacitor is connected to the output for stability and filtering.

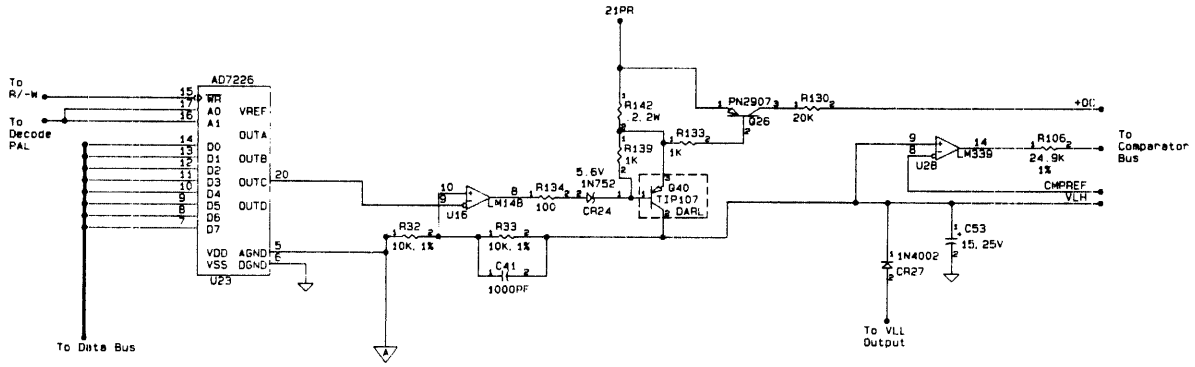


Figure 3-15. VLH Output

VLL

Purpose:

The Vll supply provides the negative voltage required by the logic driver on the Pin Driver boards.

Range:
No load: 0 to -10V
Full load: 0 to -8V

Circuit operation:
The DAC's output is connected to the 60.4KΩ resistor, R31. The output of the VLL supply is connected to the 60.4KΩ resistor, R34. R34 and R31 are connected together at the "-" input of op amp U16, pin 13. When the DAC's output rises, the op amp output voltage lowers to a level that is two base-emitter voltage drops--that of the Q41 darlington transistor-- away from the final output voltage.

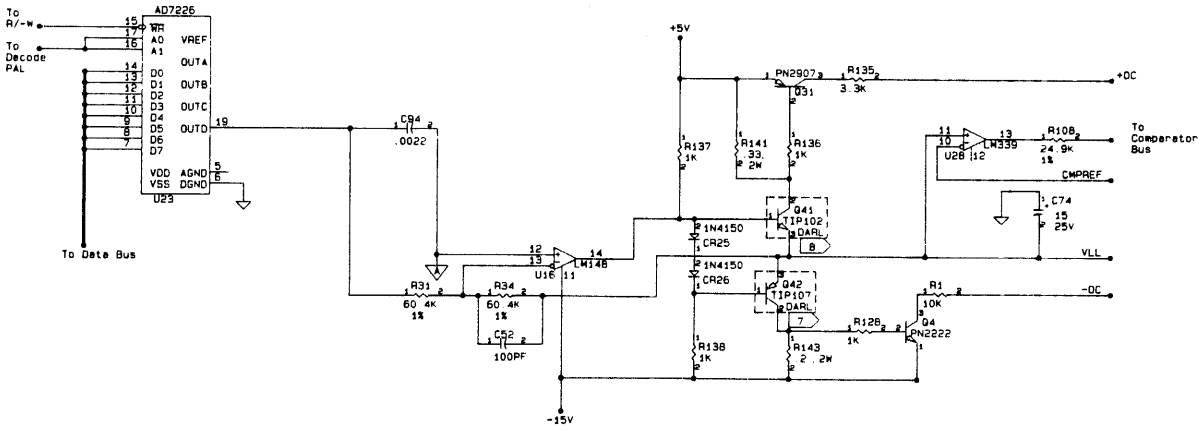


Figure 3-16. VLL Output

While Q41 is supplied by +5V, the VLL output never goes above 0V. The reason for its presence in the circuit is to allow the VLL supply to source as well as sink current at a negative voltage, a condition required by the Pin Driver boards.

The reason for the two series diodes is to compensate for one of the two base-emitter voltage drops in each of the darlington transistors, Q41 and Q42. This way, the op amp output does not have to swing as far to turn on either of the two output transistors.

The -OC signal goes negative when too much VLL output current is sensed by R143 and the overcurrent transistor, Q4, turns on. The +OC signal goes positive when too much VLL output current is sensed by R141 and the overcurrent transistor, Q31, turns on. R137 and R138 provide current for the two series diodes to operate.

The output of the VLL supply is compared to the COMPREF signal by pins 11 and 10 of U28. The output of this comparator goes to the comparator bus. C74 is used for stabilization and filtering of the VLL output voltage.

FCHR

Purpose:
This circuit provides the fine current source on the Pin Driver board with a reference voltage. This reference voltage sets the current level of the fine current source.

Range:
+14.3 to +19.3V

Circuit operation:
This circuit (see figure 3-17) runs a desired current through a 200Ω resistor (R24 and R91 in this case), measures the resultant voltage drop across that resistor and delivers that voltage to the Pin Driver board. The circuitry functions as follows:

Q19 is always on, so its effects can be ignored. The DAC's output voltage is applied to the 200KΩ resistor, R72 while the FCHR output is connected to the 100KΩ resistor, R71. R72 and R71 are connected together at pin 2 of the LM148 op amp. The other input of the LM148 is connected to a voltage divider set up by R70 and R69 between +21V and ground. This holds the inputs of the op amp at about +14V.

When the DAC voltage rises, Q18's emitter voltage drops. The emitter voltage of Q20 is then one base-emitter voltage drop below the FCLR voltage. The emitter voltage is also applied to the 200Ω resistor, R24.

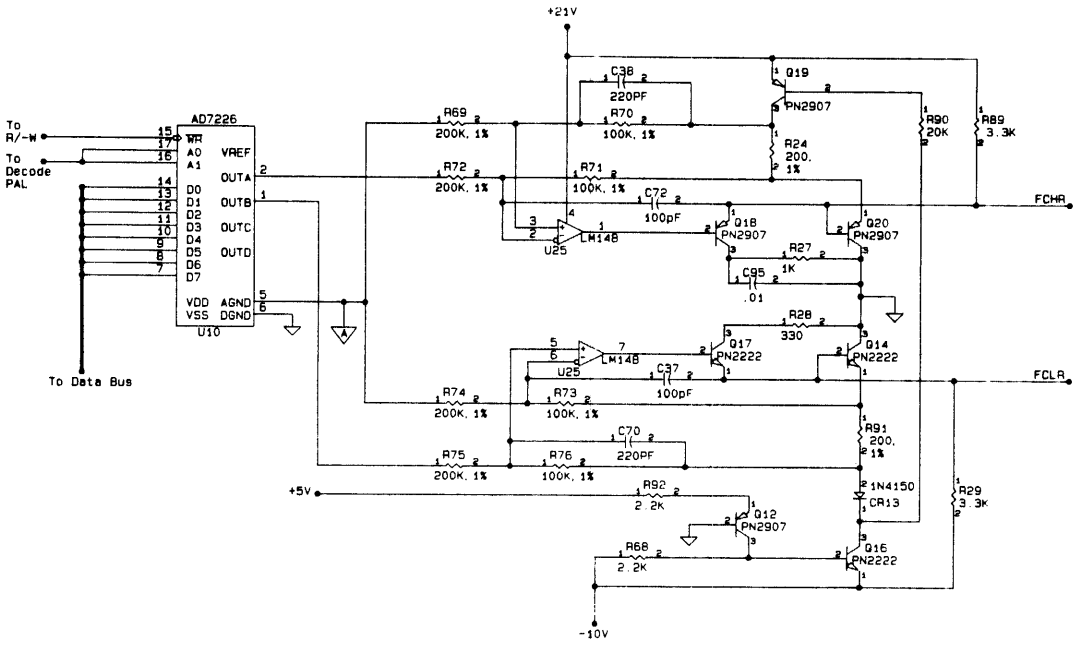


Figure 3-17. FCHR and FCLR Supplies

FCLR

Purpose:
To provide the fine current source on the Pin Driver board with a reference voltage. This reference voltage sets the current level of the fine current source.

Range:
-3.6V to -8.6V

Circuit operation:
The DAC's output (see figure 3-17) is applied to the "+" input of op amp U25 through R75. The output voltage is sensed on the "-" input of the op amp through R73.

When the DAC's output voltage decreases, the op amp's output also decreases. This voltage appears on the emitter of Q17 (minus a base-emitter voltage drop) and is the FCLR output. This decreases the voltage across the 200Ω resistor R91 through the base-emitter of Q14. The lower output voltage is fed back the "-" input of the op amp through R73, balancing both inputs of the op amp. Q12 and Q16 remain on all the time.

FCLC

Purpose:
To set a clamp voltage on the pin driver's output when the pin driver's fine current source is sinking current.

Range:
No load: -10 to +10V
Full load: -8.8 to +10V

Circuit operation:
The "-" input of the op amp, U25 pin 9 (see figure 3-18), is set to a voltage that is halfway between the output voltage and the +10V ref signal. The "+" input is set by the DAC's output. The output of the op amp drives the gate of Q51. The output voltage is fed back to the "-" input of the op amp through R62 to balance the op amp inputs. When overcurrent is sensed on R189, Q21 is turned on, pulling over-current.

FCHC

Purpose:
To set a clamp voltage on the pin driver's output when the pin driver's fine current source is sourcing current.

Range:
No load: -7.3V to +16.3V
Full load: -5V to +20V

Circuit operation:
The "-" input voltage of the op amp (see figure 3-18) is set between the output of the FCHC supply and the +5V ref signal. The "+" input voltage is set by the DAC's output. The op amp output drives the base of Q47 such that its emitter becomes the output. The output voltage is fed back to the "-" input of the op amp through R63 to balance the op amp inputs. When overcurrent is sensed on R167, Q3 is turned on, pulling over-current.

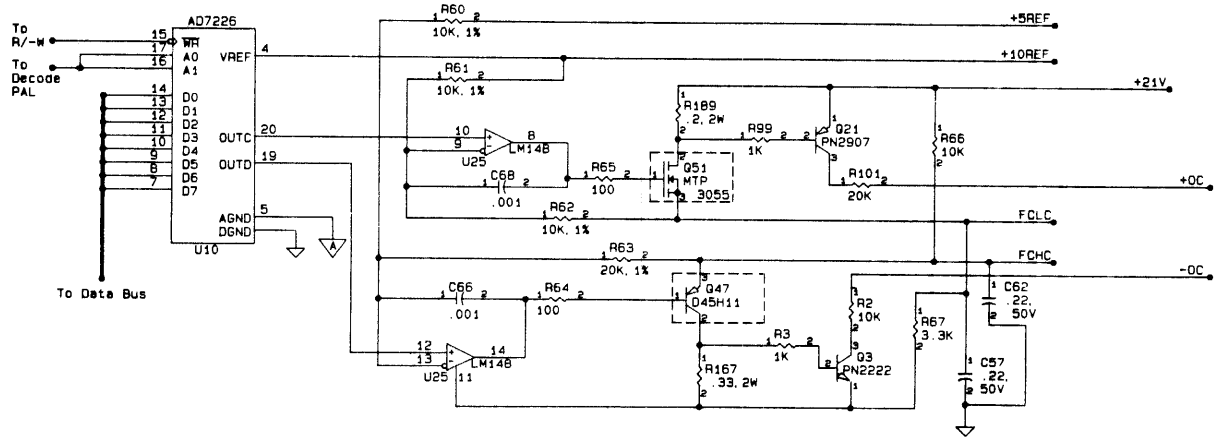


Figure 3-18. Fine Current Clamps

Overcurrent Integrator:

Purpose:
To accept overcurrent signals from the Waveform board circuits and the Pin Driver board's OCTRIP signal.

Circuit operation:
When the "-" input of the comparator, U27 pin 4, lowers to less than its "+" input voltage (see figure 3-19), the comparator output goes high and C19 begins to charge to a positive voltage through R80 and CR12. When the voltage across C19 exceeds 2.5V, the output of the next comparator, U27 pin 1, goes low. This output pulls the CLEAR input of the auxiliary latch, U14, low and sets all its outputs to a low. When the output of U27 (pin 2) goes low, the charge across C19 is drained off through R86. In this way, the overcurrent integrator will not respond to transient overcurrent inputs--those caused by slewing of supply output voltages--but will respond to any long-duration overcurrent inputs (those that are less than one millisecond).

The "-" input of U27, pin 4, can be pulled low in either one of three ways: the OCTRIP (active high) signal can be raised, Q15 can be turned on, or Q13 can be turned on.

The OCTRIP signal comes from the Pin Driver boards when their overcurrent circuit activates. Q13 is turned on when any of the -OC signals goes low. Q15 is turned on when any of the +OC signals goes high.

R81 and R82 form a voltage divider to produce a 2.5V reference that U27's comparators use. R83 is a pull-down resistor for the input of U27, pin 10. CR3 and CR11 clamp the OCTRIP input to ground and +5V. The 100KΩ and 1KΩ resistors on pin 7 of U27 provide the output of U27, pin 1, with 25mV of hysteresis for stabilization.

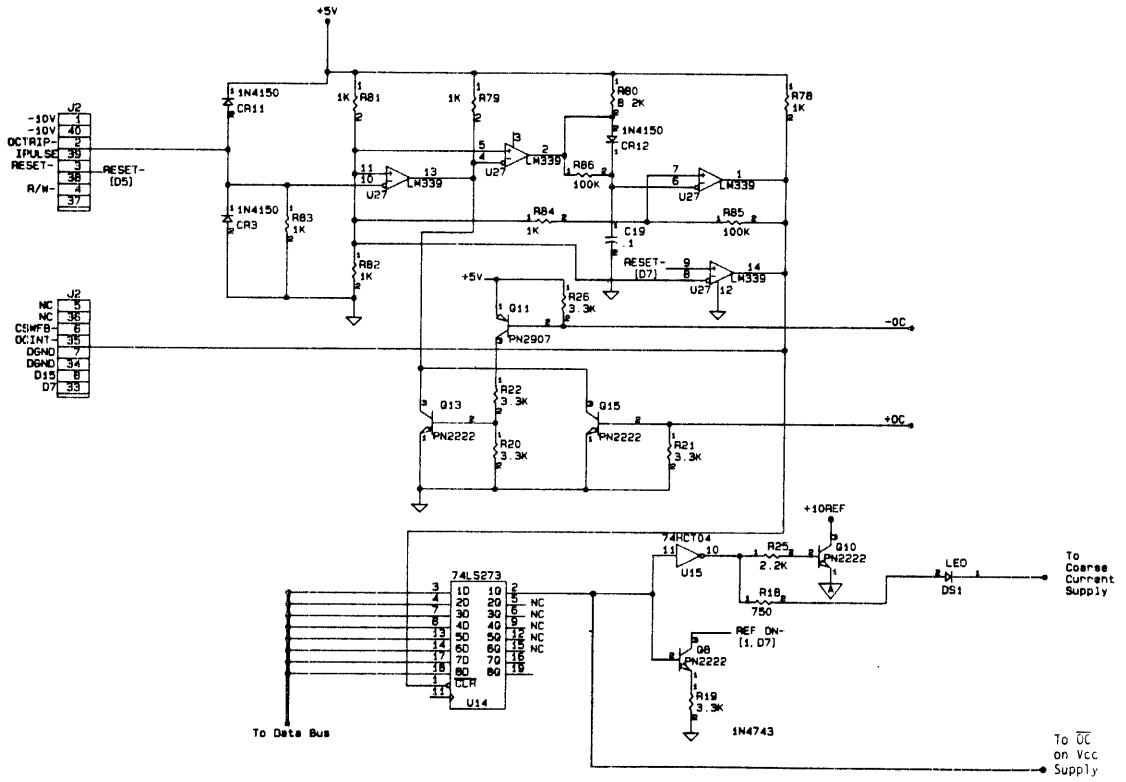


Figure 3-19. Overcurrent Integrator

Coarse current (CC)

Purpose:
This supply provides the pin driver output with a constant current which is adjustable down to the 1mA level. This supply will only source current.

Range:
Voltage: 0 to 33V
Current: 0 to 250 mAs

Circuit operation:
The goal of this circuit is to set up a regulated voltage across the 10Ω resistor, R193. In doing so, a constant current will be established. The DAC's output voltage is applied to the "+" input of U30, pin 5. The op amp of U30 pins 5, 6, and 7 is set up in a unity gain configuration (its input voltage equals its output voltage). The output of this op amp is tied directly to the base of Q37. The emitter voltage of Q37 is applied to a 1KΩ resistor, R190.

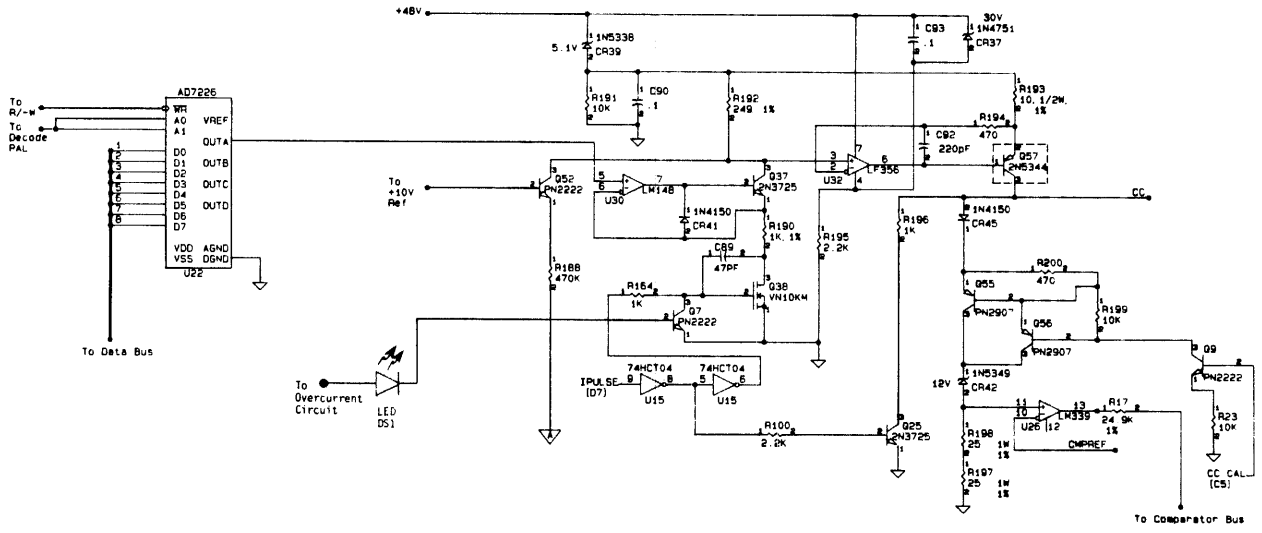


Figure 3-20. Coarse Current Supply

When the FET, Q38 is turned on, a constant current is established through it. This current comes from the +48V supply, through R192. Since the op amp of U32 pins 2, 3, and 6 is also set up as unity gain, the voltage developed across R192 will appear across R193 and thus establish the final output current.

For this to happen, two conditions must be satisfied: the overcurrent condition must be cleared, and the IPULSE signal must be in a high state. Clearing the overcurrent condition causes Q7 to turn off, allowing the FET, Q38, to turn on. Pulling overcurrent will also lower the +10ref signal to 0V. This action turns off Q52, which shuts off the coarse current completely. Having the IPULSE signal in the high state turns on Q38, which enables the entire circuit.

CR 39 and R191 work together to drop the +48V supply level to limits which are acceptable to the output transistor, Q57. CR37 and R195 work together to drop the +48V supply level to limits which are acceptable to the op amp, U32. The output of the coarse current supply is connected to the coarse current calibration circuit. When the CC CAL signal is taken high, Q9, Q56 and Q55 all turn on. This directs current from the coarse current supply through CR45, CR42 and a fixed load of 50Ωs. The 50Ω load is made up of R198 and R197. The voltage developed across these resistors is input to the comparator, U26 pin 11. The other input to this comparator is connected to the CMPREF signal. By varying the CMPREF level, a current measurement can be made. The output of the comparator is connected to the comparator bus.

Slew Rate reference (Vslew)

Purpose:
This supply provides the custom linear IC, mounted on the Pin Driver boards, with a reference voltage which it uses to determine the slew rate of the pin driver voltage source.

Range:
+3.4 to +38.4V

Circuit operation:
The voltage level of the "+" input of the op amp, U19 pin 10, is set at a point between the DAC's output voltage and the Vslew supply output voltage by R43 and R114. The voltage of the "-" input on the op amp is set at a point between the voltage at the cathode of CR21 and ground.

Since the "-" input is held at a constant voltage, the output of the op amp adjusts the collector of Q50 to a voltage which feeds back and keeps both inputs equal. There are two DAC outputs associated with this supply. One is applied to the op amp input through a 10KΩ resistor and the other is applied the 470KΩ resistor R42. The DAC output associated with the 10KΩ resistor makes large adjustments to the output voltage, while changes on the DAC's output associated with the 10KΩ resistor make fine adjustments.

The three diodes CR21, CR22, and CR23, have no function on the Waveform board itself, but are required by the Pin Driver board's linear IC. R140 provides a current source for the output transistor. CR14 and CR15 in conjunction with R94, R97 and Q22 form a 2 mA current source which can pull the output voltage up in addition to the current supplied by R140. The output current is monitored by R170. When the voltage developed across this resistor is high enough, Q54 turns on and pulls over-current.

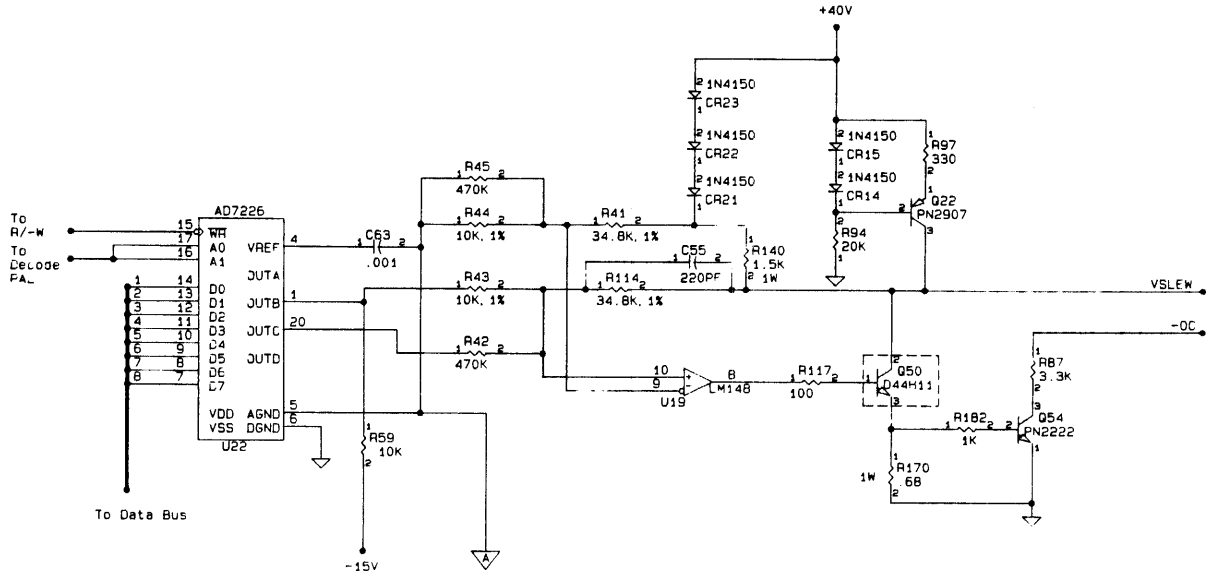


Figure 3-21. Slew Rate Reference

Clamp

Purpose:
The output of this supply provides a capacitor, charged to a predetermined voltage level, to the device socket pins. The device socket pins are connected to this capacitor through a diode. If the voltage on Clamp is 10V and the voltage on the pin tries to momentarily rise to a higher voltage than 10V, it will be clamped by the diode on the device socket pin. This eliminates overshoot that may occur in any operation done on a device in the socket.

Range:
0 to +40V

Circuit operation:
The "+" input of the op amp, U31 pin 3, is set to a voltage by the DAC's output while the "-" input, pin 2, is set to a level between the output voltage and ground. The output of the op amp adjusts to a voltage which will keep both inputs at the same level.

The 10KΩ resistor to ground provides a current path for current that comes out of the op amp and doesn't go to charge C82. The op amp current is limited by R179, the 100Ω resistor.

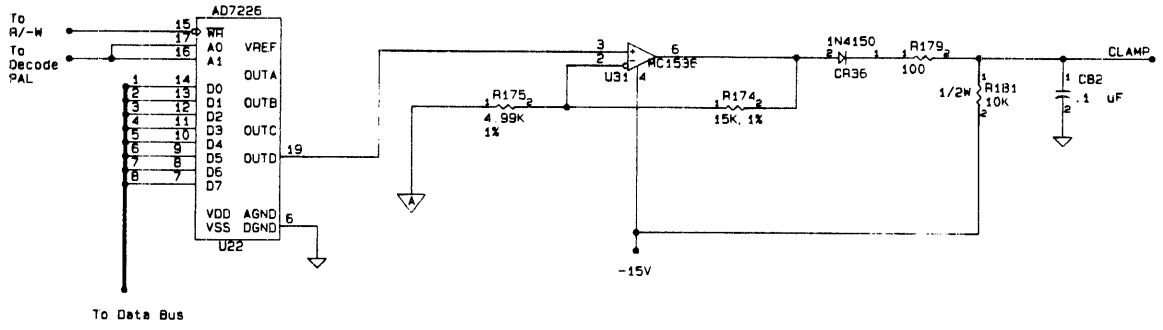


Figure 3-22. Clamp

3.4.4 Basic Operation of the Waveform Board's Outputs

NOTE

This section is a basic explanation of Waveform board voltage outputs, and is not intended for personnel already experienced in working with analog circuitry.

Following are the three basic elements of a typical Waveform board's voltage source. These three elements are found in several (but not all) of the individual Waveform board outputs.

1. The DAC IC (Digital to Analog Convertor).
2. The power amplifier.
3. The output comparator.

The DAC IC converts a binary value, placed at its inputs, to an analog voltage associated with that binary value. This action is initiated when the chip select (CS) or address lines (A0, A1) are active, and the Write (WR) signal makes the proper transition.

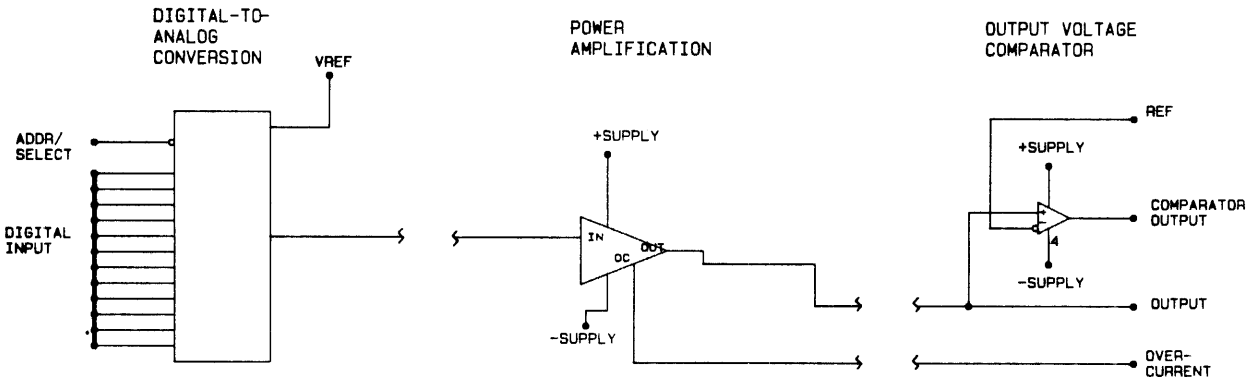


Figure 3-23. Basic Elements of a Waveform Board Output

The Waveform board uses two types of DAC IC's: the 7545 and the 7226. The 7545 uses twelve binary digits as its digital input, and contains only one voltage output. The other DAC used, the 7226, uses eight binary digits as input, and outputs four separate analog voltages. The 7545 is selected by a chip select (CS) signal, and is written to with a positive transition on the write (WR) signal. Since the 7226 contains four DAC's, each DAC is selected by an appropriate address on the A0 and A1 inputs. The 7226 is written to with a negative transition on the write input.

When troubleshooting the DAC IC's, it is important to understand that the 7545 DAC outputs an analog current, which is difficult to measure. This current is converted to an analog voltage by the op amp connected to its output. Verifying the operation of the DAC is best done by measuring the output of the output op amp. With the 7226 DAC, this is not the case. The 7226 DAC contains its own op amps, so that the DAC output is on an analog voltage and is easier to measure.

The power amplifier is composed of either an op amp driving a power transistor or, where less current is required, an op amp alone. The function of the op amp is to maintain regulation of each waveform board output.

All the op amps on UniSite's Waveform board are configured to operate as shown in either of the two figures below.

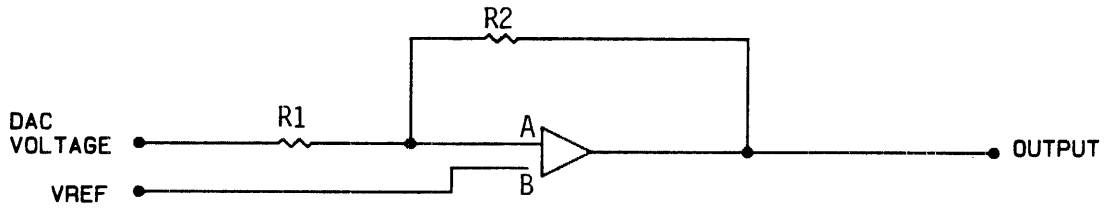


Figure 3-24a. An op amp Power Amplifier

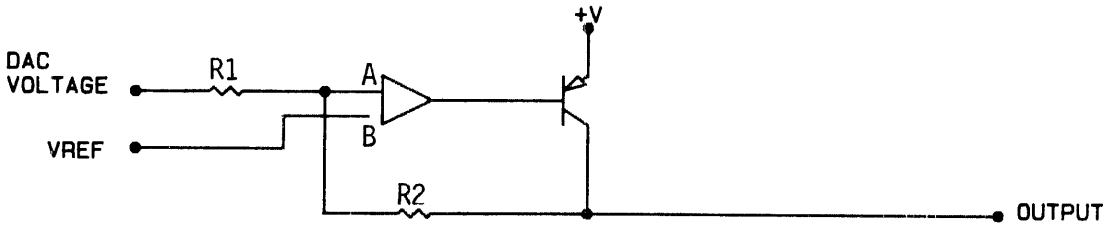


Figure 3-24b. A Power Amplifier That Uses an Output Transistor

When describing the op amp power amplifier, it is helpful to remember that the op amp functions in the following way: When the "+ input" voltage is greater than the"- input" voltage, the output voltage will approach the "+ supply" voltage. Conversely, when the "+ input" voltage is less than the "- input" voltage, the output voltage approaches the "- supply" voltage. Keeping this in mind, we will look at the operation of the circuit shown in figure 3-24a.

R1 and R2 form a resistor divider network, with the DAC output voltage applied to one end, and the op amp output voltage to the other. The center of the divider network is connected to input A of the op amp. Op amp input B is connected to a fixed reference voltage. It is the function of the op amp to adjust its output voltage, such that the resistor divider holds input A at the same voltage as the reference voltage on input B. When the DAC voltage changes, the op amp output voltage changes correspondingly to maintain the same voltage on both op amp inputs.

If at any time the two op amp inputs are not at the same voltage level, a problem is indicated. The circuit shown in figure 3-24a works the same way as that of figure 3-24b; the only difference being the output transistor, which is placed between the op amp output and the feedback resistor R2. The transistor provides far more current to the output than the op amp could supply on its own.

As shown in figure 3-24a, when the DAC voltage of figure 3-24b changes, current through R1 tries to change the voltage on input A of the op amp. The op amp responds by using its output to adjust the collector voltage of the output transistor. When the collector voltage changes, current through R2 is fed back to the A input of the op amp. This readjusts the voltage at the A input such that it equals the voltage of the B input again. In this fashion, the output voltage will always adjust to a level which offsets the DAC voltage level placed at R1, the input of the power amplifier circuit. This output voltage is used by the rest of the programming electronics.

The output comparator is either an LM339 or an LM148 IC. One of its inputs is connected to a reference voltage and the other to the output of the power amplifier. The output is connected via the Comparator Bus to the input of the Comparator Latch, U3 and U4. The reference voltage is either fixed, as in the case of the +5REF, +10REF, and the -10REF, or is variable, as in the case of the COMPREF signal.

The comparator provides a way for the system controller (located on the Controller board) to monitor the output voltage level of each voltage source. By varying COMPREF until the comparator output toggles, the voltage source output level can be accurately determined. In the case of +5REF, +10REF, and -10REF, the output of the voltage source is varied until the comparator output toggles. This is important when performing system diagnostics such as self test and auto-calibrate.

In the low state, the comparator outputs will pull down to the -15V supply rail. Since this is an unacceptable level for the 74HC373 comparator latch, it is connected to one end of a 24.9KΩ resistor. The other end is connected to the 74HC373 input and a 10KΩ resistor to form a voltage divider network. This provides acceptable input voltages to the comparator latches. There is a 0.01 mF capacitor on the output of each comparator, whose function is to stabilize the output when both inputs are at equal levels.

3.5 FSM BOARD

The Chip Site FSM board (701-2042) provides an interface between the controller board and the LCC/SOIC device sockets.

Clamp diodes CR1-15 coupled with 0.01 uF capacitors prevent voltage spikes to socketed devices. Relays K1-K40 are used to cleanly produce Vpp and ground signals to the sockets. Individual socket and "ACTIVE "LED's connected to the relay circuitry indicate whether a device is being programmed. 12 O.1uF capacitors on all +5V lines reduce noise.

3.6 PSM BOARD

The Site 40 board (701-2021) provides an interface between the controller board and the 40-pin device socket.

Relays K1-K40 are used to cleanly produce Vpp and ground signals to the sockets. "READY" and "ACTIVE" LED's attached to these relays indicate whether a device is being programmed. Clamping diodes CR1-6 prevent voltage spikes to socketed devices.

3.7 EXPANSION RAM BOARD

Signals between the Expansion RAM board and the Controller board are routed through connector J1; see figure 3-25 on the next page. The RAM board's DRAM consists of eight 9-bit-wide SIMMs and 12 64K x 4 DIPs, split between the high- and low-order data bytes. DRAM uses the CAS-before-RAS refresh mode.

Address lines A1-A20 are multiplexed through U38,U39 and U40. The resulting addresses, low- and high- A0-A9, are then routed to DRAM. A17-23 are the address lines for the two decode PLDs.

Data lines are buffered by either U18 or U37, and then routed to either the high- or low-order DRAM. D0-D7 are routed through buffer U37 to the low-order DRAM; D8-D15, to buffer U18 and the high-order DRAM. Parity checking for the by-9 SIMMs is performed by parity checkers U9 and U19. If a parity error occurs during a memory cycle, U9 or U19 send a logic low onto the PERR- line to PLD U26. U26 then stops sending a DTACK (data acknowledge) signal to the 68000. The 68000 waits for the DTACK signal for 3µs; then signals a bus error. A parity error will then appear on UniSite's screen.

Refresh for DRAM occurs through the refresh circuitry, U15, U17 and U24. Data strobe lines UDS and LDS are fed through J1 to the RAM board's PLD U26. A refresh request is routed from U17 to the refresh alternator, U24, via a logic high on the REFREQ line. The column- and row-refresh signals, RCS and RRS, are routed to the two PLDs. PLD U10 then sends out RAS- to DRAM; PLD U26 sends the CAS- signals.

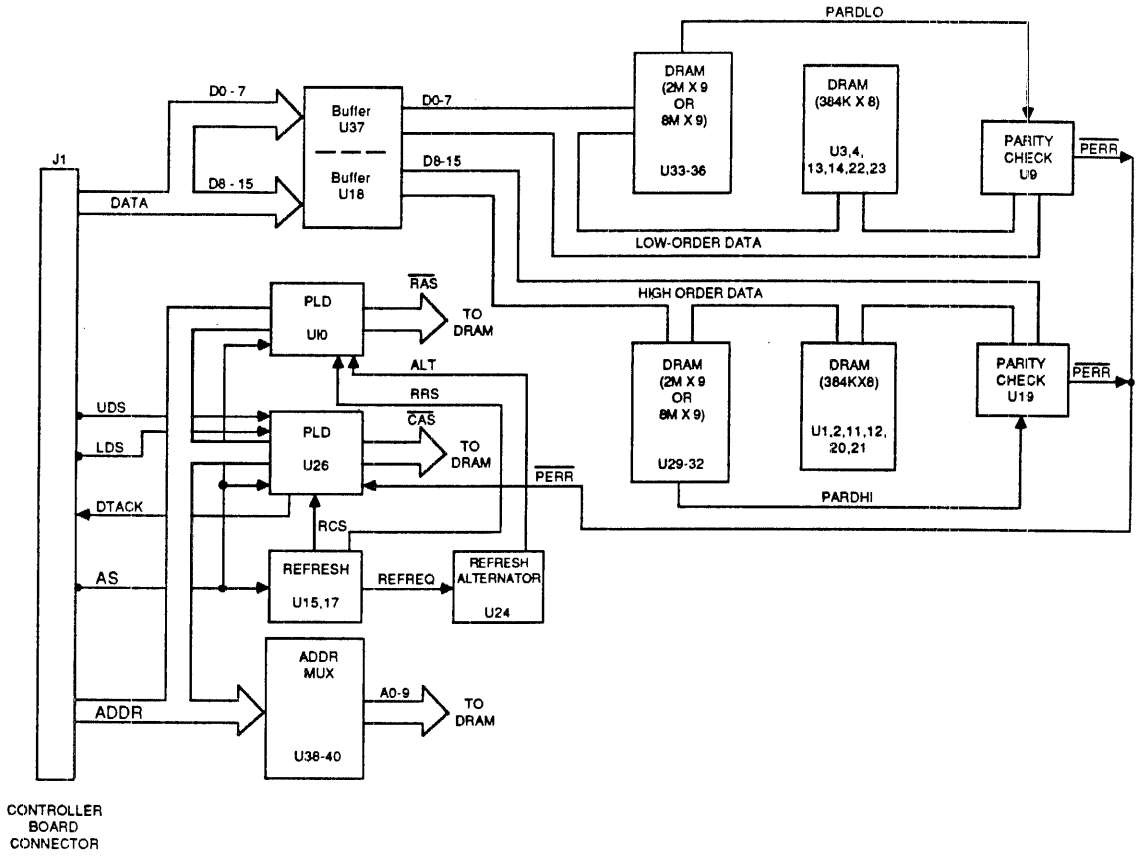


Figure 3-25. Expansion RAM Board

Section 4
Maintenance/Troubleshooting

4.1 OVERVIEW

4.1.1 Introduction

This section of the manual describes UniSite maintenance and troubleshooting. Also included in this section is some information on preventing static damage to UniSite's circuitry.

WARNING

This manual is intended for use only by service personnel. Do not attempt any of these procedures unless you are qualified to do so.

4.1.2 Reducing Electrostatic Discharge

Some devices installed in or programmed by UniSite are susceptible to electrostatic discharge (ESD), which may cause subsequent failure or unsatisfactory operation of the part or its related circuitry. The effects of ESD are reduced through the use of special equipment and procedures This subsection describes the methods you can use to lessen the likelihood of ESD.

ESD PRECAUTIONS

The easiest way to prevent ESD damage is to make sure a common static potential (ground) exists between the static-sensitive device, its environment and you. This can be accomplished by grounding the operator to the work station via an antistatic strap and covering the surface of the work area with an antistatic material. Devices to be programmed may also be protected by either placing them on a non-conductive foam pad or enclosing them in an antistatic material. The most common antistatic material is a special, conductive plastic, commonly referred to as "pink poly."

The following list contains some precautions that may be used at a prepared workstation to reduce ESD in the work environment.

⇒ Do not install or remove static-sensitive (or any other) devices from a circuit that has power or signals applied to it.

⇒ Install antistatic tops and wrist strap grounding studs on work benches and tables. (UniSite has a factory installed grounding stud.)

⇒ Provide antistatic trays, carriers or toteboxes for transporting assemblies.

⇒ Maintain the relative humidity above 40%.

⇒ Connect UniSite's chassis to Ground using the banana plug receptacle on the left-hand side of the programmer.

STATIC SENSITIVE DEVICES

The following is a partial list of devices that are particularly static sensitive and that may be encountered while programming with or servicing UniSite.

⇒ MOS and CMOS devices

⇒ Schottky and low-power Schottky TTL logic circuits

⇒ Small-signal diodes

⇒ TTL logic circuits

⇒ Junction FETs

⇒ Small-signal transistors

⇒ Metal-oxide resistors

4.2 MAINTENANCE

Periodic maintenance of UniSite consists of cleaning the unit and checking the sockets. UniSite requires no calibration, although the Waveform board's VREF supply and the power supply's voltages may be checked (see the next subsection).

4.2.1 Cleaning

UniSite's exterior may be cleaned with a clean cloth, dampened with water and a mild detergent. Never use caustic cleaning agents that could damage the unit's surface. To prevent any damage, always disconnect the power cord before cleaning.

4.2.2 Socket Maintenance

Check the socket module periodically for accumulation of dirt and debris. Dust may be removed with dry, compressed air. The socket itself should only be cleaned with methyl alcohol, Freon TE ™ or detergent and water. When checking the socket, also check for signs of socket wear; the average lifetime of a socket is 25,000 to 50,000 insertions.
If the socket is not opening and closing smoothly, it may need replacing.

4.2.3 Calibration

UniSite never needs to be calibrated by a user. All calibration is performed by software, and is compared to a laser-trimmed voltage reference on the Waveform board. You may check the voltage, VREF, by using a digital multimeter. See table 4-1 for allowable values. Figure 4-1 shows test point locations.

Table 4-1. Waveform Board Supply Voltages

TESTPOINT	TOLERANCE
TP1 (+10V)	+9.090V to +10.010V
TP2 (GND)	GND
TP3 (+5V)	+4.9V to +5.1V
TP4 (-10V)	-9.8V to -10.2V
TP5 (-10V)	-9.8V to -10.2V
TP6 (+40V)	+39.20V to +40.80V

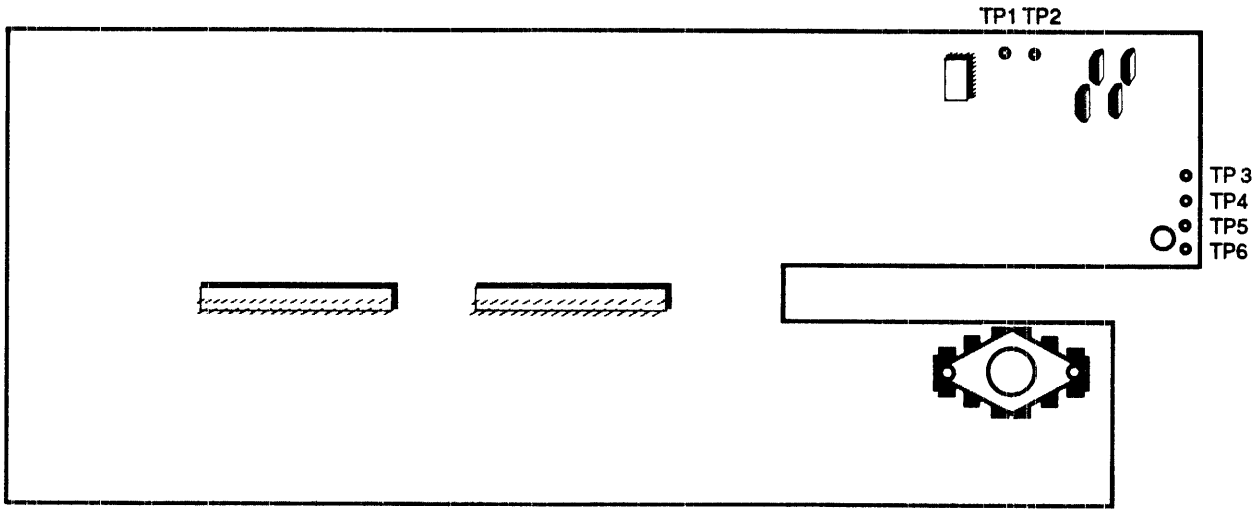


Figure 4-1. Waveform Board Test Point Locations

4.3 TROUBLESHOOTING

4.3.1 Using the Front Panel LEDs to Isolate Faults

UniSite always performs a self-test upon power-up. The four front panel LEDs illuminate in different patterns, depending on the results of the self-test. This subsection explains what to do if the LEDs signal an error condition. Table 4-2 shows all possible LED combinations and what each means.

In general, if one or more front panel indicators is blinking after the self-test, there may be a faulty circuit board in UniSite. Contact your nearest Data I/O Service office and arrange to send the unit in for servicing. This section is intended for use in isolating the problem board.

Table 4-2. Front Panel Indicators

INDICATOR				DESCRIPTION
Power	**Terminal**	**Remote**	**Self-test**	
on	off	off	on	Self-test in progress. No error condition.
on	on	off	off	Terminal port OK; self-test finished. No error condition.
on	off	on	off	Remote port OK; self-test finished. No error condition.
on	on	on	off	Remote & terminal ports OK; self-test finished. No error condition.
on	off	off	off	Terminal port not properly connected; check connection.
off	n/a	n/a	n/a	Power supply off, or no 5V supply; see subsection 4.3.2.
on	blinking	on	on	Bad CPU, EPROM, U50 or power-fail detect.
on	on	blinking	on	Bad system RAM (locations 80000-FFFFF).
on	blinking	blinking	on	Bad serial port DUART (68681).

WHEN THE TERMINAL INDICATOR BLINKS--ALL OTHER INDICATORS ILLUMINATED CONTINUOUSLY

If the terminal indicator on the front panel blinks after power-up while the other three indicators are illuminated continuously, the problem is either a bad CPU, EPROM, bad U50 device or a power-fail detect error.

If the CPU is faulty, the Controller board may need replacement. If the problem is in EPROM, verify the checksum of each EPROM on the Controller board using another UniSite--the EPROM may need to be changed out. If the problem is a power-fail detect error, the power supply may be bad. In all cases, UniSite needs servicing.

Check to see if U50 is properly inserted. The circuitry is designed to not allow operation if U50 is missing.

WHEN THE REMOTE INDICATOR BLINKS--ALL OTHER INDICATORS ILLUMINATED CONTINUOUSLY

If the remote indicator on the front panel blinks after power-up while the other three indicators are illuminated continuously, the problem is bad system RAM, at locations 80000-FFFFF. If this is the case, one or more of the system RAM chips may need replacing.

WHEN THE REMOTE AND TERMINAL INDICATORS BLINK--ALL OTHER INDICATORS ILLUMINATED CONTINUOUSLY

If the terminal AND the remote indicators on the front panel blink after power-up while the other two indicators are illuminated continuously, the problem is with the serial port. Check the 68681 serial port device, U14. See the circuit description in section 3 for more details on operation.

WHEN THE POWER INDICATOR BLINKS OR DOES NOT ILLUMINATE

When the power LED indicator on the front panel either blinks or does not light up, the problem may be with either the Waveform board's power transistors or the Power Supply. Check the power supply connector's test points, as explained in the following two procedures:

1. a. Remove the top cover, as described in section 2.

   b. With the power supply connector plugged in (J22), measure all five of the power supply's outputs, located next to J22 on the Controller board (see figure 4-2). Table 4-3 shows the allowable values for each supply. If the measured values are not within those measured in the table below, you may have a bad power supply: contact your nearest Data I/O Service office.

Table 4-3. Power Supply Outputs

TESTPOINT	RANGE
-15V	-14.29 to -15.3V
+5V	+4.75 to +5.25V
+12V	+11.4 to +12.6V
+21V	+19.9 to +22.8V
+48V	43.0 to 55.0V

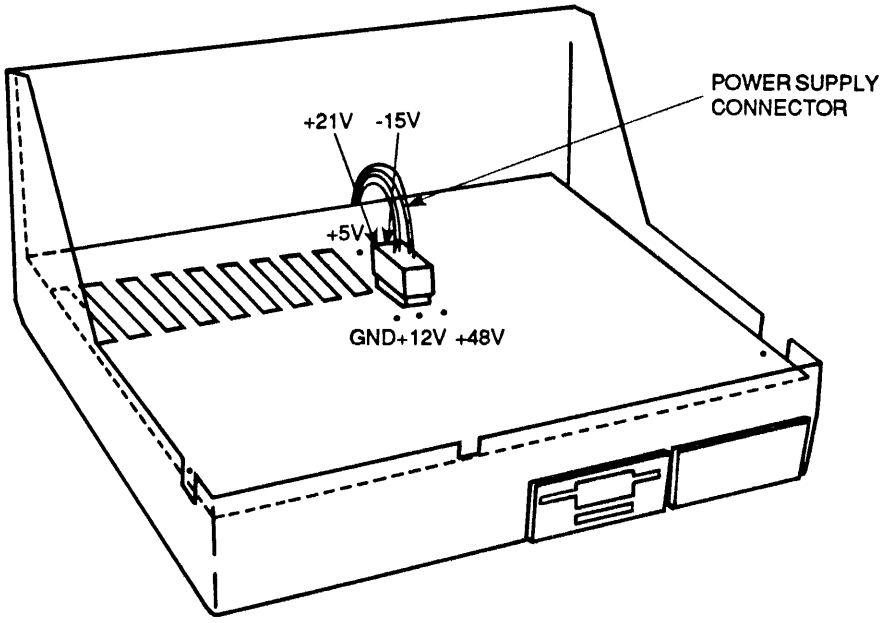


Figure 4-2. Power Supply Outputs

2. Disconnect the power supply connecter, J22. Using a digital multimeter, measure the resistance between the GND test point and each of the other five test points next to J22. Table 4-4 shows the allowable resistance values. If the measured resistances do not fall within those specified here, there may be a short on one of the circuit boards. To isolate the problem board, disconnect each board in turn, and check the values listed in table 4-4. contact your nearest Data I/O Service office.

Table 4-4. Resistance Values

OUTPUT	TYPICAL RESISTANCE FROM GND
-15V	greater than 5Ω
+5V	greater than 0.5Ω
+12V	greater than 14Ω
+21V	greater than 8Ω
+48V	greater than 50Ω
supply-to-supply	greater than 200Ω

4.3.2 Using Power-up Error Messages to Isolate Faults

On power-up, UniSite checks all major systems. If there is a malfunction, an error message will be displayed at the top of the screen: "POWER UP SELFTEST FAILED". This message is accompanied by a list of problems detected by the self-test. Following is a list of those possible messages, and what to check. See the circuit description in section 3 for more details on operation.

FSM/PSM socket not empty.
If you get this error during the power-up self-test, check to make sure there are no devices in the programming sockets. If this error appears some time AFTER self-test, it could mean there is a bad Pin Driver board; see the next subsection.

No FSM or PSM installed.
If you get this error, install the FSM or PSM and cycle the power (turn UniSite off and then on again). If the FSM or PSM are installed and you get this message, check U107 (74LS251) and U73 (74LS86) on the Controller board. These two are FSM/PSM detect devices. If either one of these is bad, replace both devices--electrostatic discharge (ESD) may have damaged them. See subsection 4.1 for information on reducing ESD.

No pin drivers installed.
UniSite must have a Pin Driver board installed in connector J5, the left-most connector, in order to pass the self-test. Make sure that the Pin Driver boards are properly installed.

PCU error.
If this error appears, cycle the power; if the message returns, then either the PCU is bad, there is a bad Pin Driver board in the left-most position, or the Waveform board is faulty.

Pin Driver error.
If this message appears, go to the self-test screen and check to see which Pin Driver board is faulty. Remove the top cover and the faulty Pin Driver board according to the procedure in section 2; then call your nearest Data I/O Service office and arrange replacement of the board.

Waveform board error.
If you get a Waveform board error, do the following: Remove the top cover according to the procedure in section 2. Next, switch the left-most Pin Driver board (the board installed at J5) with any other Pin Driver board. The reason for board swapping is that the Waveform board's self-test requires a functioning Pin Driver board in the left-most position. If the test passes after you swap board positions, you know the problem is with the Pin Driver, rather than the Waveform board.

NOTE

To fully calibrate the Site 40's PSM module, the first TEN Pin Driver board sockets (J5-J14) must contain a board. This is necessary so that the self-test may check all the FSM's relays.

4.3.3 Isolating Errors That Occur After Self-test

DISK DRIVE ERRORS
If you get a disk drive failure error, try using a different diskette. If that does not alleviate the problem, remove the problem drive (according to the procedure in section 2) and arrange to have it serviced at your nearest Data I/O Service office.

NOTE

Make certain that the Controller board's mounting screw located between the two RS-232C connectors is inserted completely. This screw makes the chassis ground connection to the Controller board and is necessary for reliable disk drive operation.

SOCKET NOT EMPTY ERROR
If you get this error some time after the self-test has completed, then the problem may be with either the Pin Drivers or one of the socket modules. Execute the Self-test command and see if the PSM/FSM tests pass and if the Pin Driver boards pass. See the previous subsection's Waveform board error hints.

FSM or PSM ERRORS
If any problems seem to be related to the FSM or PSM, check the following components on the Controller board: U73, U77, U107 and U117. These chips provide interfacing between the Controller board and the FSM or PSM. Also check to see that sufficient Pin Driver boards are installed: to fully calibrate the Site 40's PSM module, each of the first ten Pin Driver board sockets (J5-J14) must contain a board. This is necessary so that the self-test may check all the PSM's relays.

4.3.4 Using the Kernel Jumper Checks to Isolate Problems

If UniSite will not power-up, you can use a kernel jumper test to diagnose the problem. For more information on the Controller board's circuitry, see subsection 3.3 of this manual. If UniSite does not power-up, you should check JP1-JP4. You should also remove the Controller board's DIP jumper and then read signal outputs. Follow the procedures of the next paragraphs.

CHECKING JP1-JP4

Remove the top cover according to the procedure given in section 2 of this manual. Check the Controller board's four jumpers to make sure they are properly positioned. JP1 and JP2 select the serial port configuration, JP3 specifies EPROM as the type of program memory and JP4 selects EPROM size. See figure 4-3 for proper jumper positioning.

NOTE

Check to see what type of EPROM is installed: if 27256's are installed, JP4 is optional and therefore need not be installed.

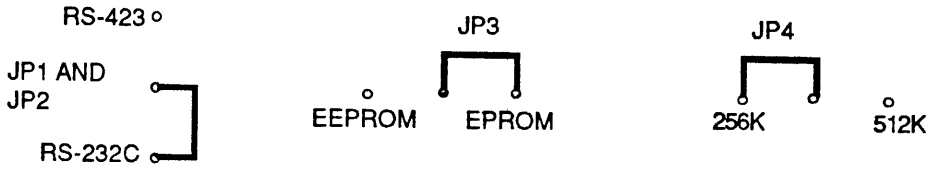


Figure 4-3. Controller Board Jumper Positioning

CHECKING THE 68000'S SIGNALS

Remove the DIP jumper, U49, on the Controller board. Removing this jumper causes the 68000 processor to execute continuous read operations of UniSite's entire memory range. Then, by checking various control signals, you can pinpoint the problem. Appendix B of this manual contains diagrams of various Controller board signal waveforms, during normal operation. With the jumper removed, check the following signals:

1. Check the following 68000 control signals:

   a. The CLK, AS-, LDS-, and UDS- signals; these should all be toggling.

   b. The following 68000 signals should be at a logic high level: RESET-, HALT-, BERR-, IPL0-, IPL1-, and IPL2-.

2. Check the 68000's address and data lines:

   a. All of the address lines (A1-A23) should all be toggling.

   b. The data lines should toggle when the processor cycles through the EPROM memory range: this will appear as an infrequent burst of data.

3. Check the decode signals. All decodes that are related to read operations should toggle (although the period may be quite brief).

4. Check the dynamic RAM refresh signals, REFRAS- and REFCAS-. These signals should be low for 300ns and occur every 12µs.

5. Check the real-time clock signal. This signal should have about a 35ms period.

6. Check the 8-MHz clock signal at the 1772 disk-control chip, U14.

7. Reinstall the U94 jumper.

4.4 POWER-UP RETESTING

To test UniSite after reassembly, do the following:

1. Plug in UniSite's power cord.

2. Insert the UniSite system disk into drive A.

3. Plug in the ASCII terminal's power cord and power up the terminal.

4. Turn on UniSite. The Power and Self-test indicators on UniSite's front panel will illuminate. Drive A's active indicator will also be illuminated. If the drive indicator does not illuminate, check to see that the disk is properly inserted.

5. When the drive A indicator goes off, make sure all self-tests have been completed. The Self-test indicator will extinguish when the self-test is completed. The Terminal indicator on UniSite's front panel will now illuminate. If this indicator does not light up, press the terminal port's DCE/DTE switch on UniSite's back panel.

6. When the Terminal indicator lights up, the serial port connection has been properly established.

   NOTE

   If the terminal indicator still does not light up after you have pressed the DCE/DTE switch, your RS-232C cable or terminal may be defective.

   If the terminal now displays random or incorrect characters, press **BREAK A**. This automatically sets UniSite's baud rate to that of the terminal. The terminal should now display the UniSite system configuration information.

7. Verify that the terminal type is correct.

8. Verify that the RAM size configuration information appearing on the screen matches the actual UniSite RAM size.

9. Respond to the question concerning terminal type: press the carriage return key if you do not want to select a new terminal type; press **y** if you do.

10. Get to the Self-test screen, by pressing **m** and then **s**. The Self-test screen will then appear.

    NOTE

    To perform the Self-test, the System disk should be installed into drive A. If you have a 2nd disk drive, install the utility disk there. You must also have a PSM installed in order to perform the Self-test.

11. Move the cursor to "Perform all Tests" and press the carriage return key.

12. Testing will begin immediately. The cursor will flash beside the area being tested. "TESTING" will appear on the large reverse video block at the top of the screen.

13. If the RAM board was installed correctly, "PASS" will be displayed on the screen next to the various UniSite systems. If a "FAIL" message appears, recheck your reassembly procedure, making sure all cables are installed correctly.

    If you check the reassembly and the problem still persists, try to isolate the area of concern by disconnecting the RAM board and running a complete system self-test. If available, you may use a UniSite Diagnostic board to check out the system. If the problem still cannot be isolated, call the Data I/O Redmond Service office.

Appendix A
Messages

A.1 INTRODUCTION

This appendix lists and describes all of the messages that appear on UniSite screens. Some messages require some action from the operator; instructions for those actions are included in the message's description. All of the messages are listed in alphabetical order. At the end of this section is a list of error codes that appear only when UniSite is being operated in remote control mode; these messages are listed in numerical order according to the error code that appears on the host computer's screen.

NOTE

The use of "PSM" and "FSM" in this section refers to the modules that are installed on UniSite's front panel. The PSM is the small socket module located on the left side of the top panel; the FSM is the optional, large module on the right.

A.2 TERMINAL MESSAGES

Addr err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

Address error

This message appears during data transfer and indicates that the address received from the remote system caused the translator to attempt to put the data at some address outside of the user RAM area. This could be caused by inappropriate use of the I/O offset variable.

Address out of range

The address you tried to select is beyond the selected device's range. Select an address that is within the limits of the device or select a different device. This message appears while you are in the memory editor, fuse editor, or using the under/overblow feature.

Beginning of file

This message appears when you are using the memory editor, vector editor, fuse editor, or using the under/overblow feature, and you press CTRL P (previous page) when the first block is already being displayed.

Begin address too large

The beginning address you selected in the memory editor was too large and is beyond the limits of the selected device. Change the begin address to one within the device's range.

Bus err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

Bytes copied = nnnnnn

This message appears while the COPY FILE operation is in progress; "nnnnnn" refers to the number of bytes copied.

Calculating sumcheck

This message appears when you in the Device Check's Sumcheck screen, informing you that the RAM sumcheck is being calculated.

Cannot access system file. Insert system disk.

This message indicates that UniSite was not able to read a system file from the system disk. Make sure that the installed disk is in fact the system disk. Reinsert the disk and press RETURN to re-execute the command. If the error message reappears, try to reboot with a back-up system disk. If the message continues to be displayed, contact the nearest Data I/O Service Center for assistance.

Cannot allocate file space

The disk is full; file the data on another disk or delete some current disk files that are no longer used.

Cannot begin job file recording from this screen.

This message appears when you attempt to create a new job file from an illegal screen: one that cannot be part of a job file. Use a different screen to start the job file.

Cannot execute job file while recording job file.

A job file cannot be executed while another is being recorded. You may "chain" job files together by ending the recording of a job file in the job file execution screen.

Cannot purge file.

This message means that, for some reason OTHER than the disk's being write-protected, the file cannot be removed from the disk. If the disk IS write-protected, a different message will be generated.

Cannot update yield tally.

This message will appear after a programming session or during device selection if the system disk is write-protected or contains data errors. The yield tally information is stored on the system disk. Remove the system disk and check to see if the write-protect slide is blocking the hole in the disk. If the hole is blocked, the disk is not write-protected and was not the cause of the problem. If the disk is not write-protected the cause of the problem is probably a data error on the system disk: use another copy of the system disk and try the same operation. If the problem persists, contact your nearest Data I/O Service Center for assistance.

Check sum error

The data that you downloaded was not sent in the data translation format that was selected on-screen. Change the data file to conform to the select data format, or change the selected data translation format.

Checksum error, Transmission Checksum = ssss

The checksum of the data received (as the result of a JEDEC logic file download) did not match the checksum downloaded from the host computer. The host computer sends a transmission checksum and a fuse map checksum as a part of the data record. UniSite compares those checksums with the checksums it created on that same data. If the two checksums do not match, this message will appear, indicating that some of the data transmitted by the host was not received by UniSite. Try the operation again, and if the problem continues, verify that the checksums generated from the host are correct. If the checksums are correct, consult your UniSite Service Manual or contact your nearest Data I/O Service Center.

[Computer Remote Control: enter Control-Z to exit].

This message informs you that Unisite is now in remote control mode and all programmer commands are now read from the remote port. Typing CTRL Z returns control to terminal mode.

Copying sectors ssss - ssss Reading source disk

This message appears while the Disk Copy command is proceeding. The information presented in this message displays the number of sectors copied in each pass. There are 1440 sectors on each disk. This message is accompanied by the message "Copying sectors ssss - ssss Writing destination disk" which appears while UniSite is writing data onto the destination disk.

Copying sectors ssss - ssss+120 Writing destination disk

This message appears during the Disk Copy routine,indicating that the data is being copied.

Could not initialize default system parameters from disk

When UniSite was booting up, the default and programming system parameters could not be loaded. Reboot UniSite with a different system disk, or call your nearest Data I/O Service Center for assistance.

Data conversion error.

This data transfer error indicates that the selected I/O translator could not handle the data properly (a mismatch between selected translator and data).

DATA ERROR: Data size exceeded user memory!

This message appears when you try to load a data file that is too large for user RAM. Specify the size of the data file before reattempting the operation.

Data load error.

If an error in reading the device data occurs in a load operation, this message will be generated. Try the operation again; if the message appears again, contact the nearest Data I/O Service Center for assistance.

Data operation complete

This message after a data transfer with an external source was successfully completed.

Data record error

The data that you attempted to transfer did not conform with the data translation format selected; put the data into the correct format and attempt the operation again.

Data operation complete Transmission Checksum = ssss

After a JEDEC datafile is downloaded to user RAM, this message appears. The number at the end of the message--represented here as "ssss"--is the transmission checksum of the transferred data.

Data transfer operation complete: data saved on disk

After a datafile is downloaded to disk, this message appears.

Data transfer error

Data could not be successfully transferred to or from the disk; try the operation again.

Data verify error

Data in RAM (or disk) was not the same as the data that was transferred from the remote system, or not the same as device data in a Verify operation.

Destination file already exists.

The filename you selected for the file is the same as an existing one. Create a different filename.

Destination file already exists. Hit return to continue, ^Z to abort.

The filename that you have designated as the destination for the data already exists, so existing data will be written over if you execute the operation. This is a precautionary message which occurs on any file operation which could over-write an existing file.

Device algorithm not found:

This message will occur if device selection is attempted using family/pinout codes, and the codes selected correspond to an algorithm which is not supported by UniSite.

Device erased with no illegal bits remaining.

This message is generated in the Device Check's Illegal Bit screen, but only for EEPROMS which have a byte-by-byte erase capability. For this device, the illegal-bit test is designed to see if each bit within the user selected region of the part can be reset (erased) to the "un-programmed" state. If this test fails, the device is not programmable and should be discarded.

Device must be previously selected:

Before you may enter the Load, Program, Verify or Device Checks screens, you must first select a device. This message appears if you have not yet selected a part.

Disk boot err

UniSite has experienced an error that it cannot recover from. Turn UniSite off and reboot the system.

Disk data error

UniSite could not read from or write to the disk due to a defective disk. Reformat the disk or use a new one.

Disk data error

The read or write operation that was attempted could not be completed because there is a problem with the disk; try the operation again with a different disk.

Disk error, terminal type not saved!

If you try to save the terminal type as one of the power-up parameters and there is a write problem with the disk (the disk is either full or is defective), this message will appear.

Disk is write-protected.

The disk cannot be written to because it is write-protected. Move the write-protect slide so that the hole through the disk is blocked, or use another disk.

Disk Boot Error

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the message persists with the same system disk, then use another system disk.

Disk write-protected, terminal type not saved!

If you try to save the terminal type as one of the power-up parameters and the disk is write-protected, this message will appear. Move the write-protect slide so that the hole through the disk is blocked.

0 div err

UniSite has experienced a divide-by-zero error that it cannot recover from; turn UniSite off and reboot the system.

Done.

The operation is completed. Proceed to the next operation you want to perform.

Done. Bytes copied = nnnnnn

This message appears after the Copy File operation is complete. It displays the size of the file that was copied in hexadecimal bytes. Proceed to the next operation you want to perform.

Done: Certain tests not performed due to Socket not empty.

If a device was present in the socket when the message "TEST HALTED: Socket not empty, hit return to continue, ^Z to abort." and you pressed the carriage return key, this message will appear. Any test requiring the device socket to be empty will not be performed. Remove the socketed device and try the operation again.

Edit begin address must be greater than or equal to offset.

This message indicates that the begin address is greater than system user memory. The memory data editor's offset is used as a reference for user memory addresses. The offset represents the beginning address of user data. Reset the parameters.

Electronic bulk erase not supported by device

You tried to electronically erase a device that was not electronically erasable. Erase the device with ultraviolet light, or select a device that can be electrically erased.

Electronic signature not supported by device.

This message appears after UniSite tried to read the electronic signature of a device that does not have a signature. Check to make sure you selected the correct device.

End of data. Hit return to continue

This message appears after a download operation, signalling that the operation is complete.

End of file

When you are using the memory editor, vector editor, fuse editor, or the over/under blow feature, this message will appear if you press CTRL N (next page) when the last block of data is already being displayed.

ERROR: Device not supported on this system disk.

The device you selected is not supported by this system disk. Try selecting the device using a family/pinout code instead. If there is another device on the system disk that uses the same family/pinout code, your device can be used.

ERROR: Illegal file name

The filename you assigned contained characters that are not part of UniSite's character set for filenames. Type in a filename that contains only alphabetics and numerals.

Extension '.SYS' is reserved for system use.

This message appears when you attempt to use ".SYS" as an extension for one of your filenames. Give your file another extension, such as ".DAT or ".DOC".

Factory default save file is protected:

This message appears when you try to save parameter file 0. Parameter file number zero is the file containing the set of configuration or system parameters. This file is set by the factory and cannot be changed.

Fatal system err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

File does not exist.

The file you tried to use is not on this disk; try another disk or another filename.

FILE ERROR: Cannot access yield data.

This message appears if yield data could not be updated for one of the following reasons: the system disk not installed, the system disk is write-protected or yield file has been corrupted. Correct the problem and try the operation again.

FILE ERROR: Can't reach track 0.

If this message appears, a fatal disk error has occurred. The disk drive may be faulty.

FILE ERROR: Data transfer error.

This message appears if Unisite could not successfully read or write user or system data to the disk. If trying the operation again still makes the error message appear, a new disk (and a new copy of whatever software or data the unit needs) must be used.

FILE ERROR: Routine cannot be loaded from disk, insert system disk.

This message appears when you attempt an operation that requires the use of a utility on the system disk, when the system disk is not in the disk drive. Remove the data disk from the disk drive and insert the system disk.

FILE ERROR: source file does not exist

This message appears during the Copy File operation, if the file that you want to copy is not on the disk that is in the disk drive. Insert the disk that has the source file into the disk drive and attempt the operation again.

FILE ERROR: Track not found.

This message appears if UniSite cannot find the disk track associated with the system file, or user data needed to support whatever action was requested by the user. If you try the operation again and the error message reappears, a new disk (or a new copy of whatever software or data the unit needs) must be used.

File not initialized! Enter 'C' to initialize, any other key to quit

This message appears with the fuse editor, vector editor and when the under/overblow feature is selected. The file that you have selected is not in a format that is compatible with the feature that you want to use. If you want to use the fuse editor, and the data file you have is not formatted for the device you have selected, pressing C will reformat the data file to be compatible with the device.

FSM/PSM for the device selected is not installed.

The device you selected cannot be programmed in the PSM or FSM that is presently installed. If you select a device that is not supported by an installed PSM or FSM, the Load, Program, Verify, and Device Check screens cannot be entered. Install the correct module and try the operation again.

Formatting and initializing user disk.

This message appears while a disk is being formatted.

Hit return to continue, ^Z to abort.

This message appears after a Verify operation has failed. If you want to ignore the warning (not check out the errors) and proceed with the operation, press RETURN. If you want to investigate the errors, press CTRL Z and the Verify screen will reappear.

IOX init err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

Illegal instr err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

ILLEGAL KEY INPUT: Type control-Z to abort parameter entry.

This message appears when you press an inappropriate key while specifying a parameter: for example, if you try to use a hex character to specify the data word-width for a Load operation. Press CTRL Z to exit the parameter entry mode or use the correct characters to specify the parameter.

Illegal parameter value

This message will appear if you use an inappropriate number to specify a parameter. Type in a legal value.

Illegal parameter value. Electronic signature option not supported by device.

The electronic signature verify option is not supported by the selected device, so this option cannot be set.

Illegal parameter value. Electronic erase option not supported by device.

The electronic bulk erase programming option is not supported by the device selected, so this option cannot be set. Make you selected the correct device, or disable the option, and try the operation again.

Illegal parameter value. Security fuse option not supported by device.

The security fuse programming option is not supported by the device selected, so this option cannot be set. Make you selected the correct device, or disable the option, and try the operation again.

Illegal options for this command

This message appears when you attempt an operation that needs an option that is not enabled. For example, the Verify function requires that the "number of verify passes" be set to either "1" or "2". When this message appears, go to the Programming Parameters screen or to the Options screen and enable the appropriate option. Try the operation again.

Illegal terminal type!

The terminal-type number you entered was not one of the choices presented on the Terminal Select screen. Type in a valid terminal-type number.

Incompatible baud rates between remote & terminal ports: no changes entered.

If you selected incompatible baud rates for an operation and then pressed the carriage return key, this message will appear. Select a compatible baud rate. Refer to the Configure System command description in the Commands section of the Operator's manual for a listing of incompatible baud rates.

Insert blank device. Hit return.

This message appears during the Quick Copy mode operation. Remove the newly programmed device or the master device from the device socket, place a blank device in the socket and press the carriage return key. UniSite will then begin programming the blank device with RAM data loaded from the master device.

Insert destination disk in drive A. Hit return to continue.

This message appears during the Duplicate Disk or a Copy File operation, when a UniSite with one disk drive is being used. When this message appears, remove the source disk, insert the destination disk and press the carriage return key. Make sure to use a formatted disk: if you insert an unformatted disk, UniSite will abort the operation and display "Sector not found".

Insert master device. Hit return to continue

This message appears during the Quick Copy operation. Place the master device into the device socket, lock it into place, and press the carriage return key. UniSite will then start to load RAM with data from the master device.

Insufficient block size.

This message occurs when a Program or Verify operation is attempted with a memory block size of zero (which means there is no user data present). If you have selected the disk as the data source and specified a file length of zero, then the memory block size will also get set to zero. Change the block size to a usable value.

Insufficient pin driver boards installed for the device selected.

The device you are trying to load, program, verify or check requires more Pin Driver boards than are installed in your UniSite. Each Pin Driver board drives 4 pins. For example, a 16R8 in a PLCC package (28 pins with 8 "no connects") requires 28 pin-drivers; therefore, seven Pin Driver boards.

Insert source disk in drive A. Hit return to continue.

This message is a prompt that appears during the Duplicate Disk operation, if you are using a UniSite with a single disk drive. When this message appears, remove the destination disk from the disk drive, insert the source disk and press the carriage return key.

I/O timeout error

During a download transfer operation of a non-JEDEC data file, too much time passed before UniSite received any data. Increase the I/O timeout parameter in the Configure System Parameters screen, if necessary.

I/O timeout error Transmission checksum = ssss

Too much time passed before UniSite started to receive a JEDEC data file. The I/O timeout period may be changed via the Configure System's Communications Parameters screen.

I/O translation format error

There is a compatibility problem with the data translation format you are using. Check the format of your data. The Computer Remote Control section of the Operator's manual contains a description of all the data translation formats supported by UniSite.

I/O translation format error Transmission Checksum = ssss

The format of the downloaded JEDEC data file is incorrect. Correct the format problem and try the operation again. Consult the Computer Remote Control section of the Operator's manual for an explanation of the JEDEC format.

Invalid file name

The filename you typed in either contained characters that are not part of UniSite's character set or do not conform to the DOS file conventions. Type in a valid filename.

Job file save aborted. Keystrokes not recorded.

This message appears in the following situation: If you attempt to end job file recording, and either the system disk is not in the drive or Unisite has difficulty reading the disk, an error message will appear. If you type CTRL Z after seeing that message, the above message will appear.

Job file playback ended.

This message informs you that a job file's playback has ended and you may continue with operation where the job file left off.

Key error: Hit space bar to toggle parameter or hit character desired.

This message appears if you tried to type in a parameter using an inappropriate character, such as a letter instead of a number. Type in a valid parameter.

Keystroke recording ended. Select job file for saving.

This message appears after you have pressed ESC CTRL R a second time, to end recording keystrokes for a job file. Specify a job file number, by typing a number between 0 and 9. Then type in a job file description, such as "27128.dat".

Keystroke recording for job file has begun.

After you press ESC CTRL R once, this message will appear. You are now in the job file record mode: every keystroke that you make will be recorded. Type ESC CTRL R a second time to end the session.

Loading data from file.

This message appears while data is being loaded into user RAM from a disk's data file.

Loading device algorithm

When you restore a set of system parameters that includes a specific device, this message will appear while the programming algorithm is being loaded.

Loading from disk.

This message appears when UniSite is reading system information or routines from the disk.

Loading programming parameters

When you restore a set of system parameters from the Configuration file directory, this message will appear while the programming parameters are being loaded.

Logic device must be previously selected.

This message appears if you try to use the under/over-blow feature but have not selected a logic device. Use the Verify command (if you are checking a memory device) or select the a logic device and load the data to be verified.

Loop count = Hit CTRL Z to abort this test

This message appears while a self-test is running in the continuous mode. The loop count is the number of times the selected test has been repeated.

Memory parity error at:XXXXXX

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the problem persists, record the location at which the error is occurring (represented above by "XXXXXX"), and call your nearest Data I/O Service office.

Missing description.

You did not type in a description for the recorded job file. Type in a description or press the PF1 or PF2 keys to escape from the job file screen.

MODULE ERROR: FSM ID not recognized. Reinsert module.

This message appears if there is a problem with the FSM module. Remove the module and inspect the interconnection pins to see if they are all intact. If the pins are OK, reinsert the module and watch for this message to appear. If the message reappears, you are using an obsolete version of software.

MODULE ERROR: FSM mis-socketed. Reinsert module.

This message appears if the FSM is inserted incorrectly. Remove the module and inspect the interconnection pins to see if they are all intact. If all the pins are straight and free of debris, reinstall the module, making sure the two retaining hooks are inserted into their slots. When the FSM is reinstalled, see if the message reappears. If the message continues to reappear, the FSM may be defective; call your nearest Data I/O Service Center for assistance.

MODULE ERROR: PSM ID not recognized. Reinsert module.

This message appears if there is a problem with the PSM module. Remove the module and inspect the interconnection pins to see if they are all intact. If the pins are OK, reinsert the module and watch for the message to reappear. If the message does not appear, you may resume normal operation. If the message does reappear, you are using an obsolete version of software.

MODULE ERROR: PSM mis-socketed. Reinsert module.

This message appears if the PSM is inserted incorrectly. Remove the module and inspect the interconnection pins to see if they are all intact. If all the pins are straight and free of debris, reinstall the module, making sure the two retaining hooks are inserted into their slots. When the PSM is reinstalled, see if the message reappears. If the message continues to reappear, the PSM may be defective; call your nearest Data I/O Service Center for assistance.

No disk in drive A.

There is no disk in the disk drive. Insert the system disk into disk drive A and try the operation again.

No FSM or PSM installed.

This message appears when you have selected a device-dependent operation and a FSM or PSM is not installed. The Load, Program, Verify, Device Select and Device Check operations all require the presence of a FSM or PSM. Install the correct module and try the operation again.

Non-blank device. Hit return to continue, ^Z to abort.

This message appears after UniSite has performed a blank check on a device and has detected bits that are not in their erased or blank state, and are not illegal bits. If you press the carriage return key, UniSite will proceed with the Programming operation and program over the existing data. If you press CTRL Z, the Program screen will reappear and you can try the operation again with another device. The Blank Check option in the Programming Parameters screen must be enabled before this test can be performed.

OPERATION ABORTED BY USER

If you press CTRL Z to abort an operation, this message will appear. After you have aborted an operation it must re-executed; UniSite will not allow you to resume the same operation.

OPERATION ABORTED: I/O translator format not selected.

The data translation format must be selected before an external data transfer may be performed. Select a data translation format from the Format Select screen and atternpt the operation again.

OPERATION ABORTED: JEDEC translator must be selected for logic device.

This message appears if you try a download or upload data without using the JEDEC I/O translation format, when a logic device has been selected.

OPERATION ABORTED: Logic device must be selected for JEDEC translation.

You attempted to upload or download data with the JEDEC I/O translation format when a memory device was selected. Select a compatible I/O translation format, or select a logic device.

OPERATION ABORTED: Software security violation.

You tried to perform a software operation that violates Data I/O's software security policy. Return to the Main menu screen and resume operation.

OPERATION COMPLETE.

The operation you selected has been completed; you may now proceed with other operations.

Operation complete: data saved on disk

This message indicates that the data transfer operation is completed and was saved onto the disk.

OPERATION COMPLETE. Sumcheck = ssssssss

This message appears after the completion of a Program, Load or Verify operation. The "s's" represent the sumcheck of the data that was programmed into the device.

OPERATION COMPLETE. Sumcheck = ssssssss Set Sumcheck = ssssssss

This message appears after the completion of a Set Program, Load, or Verify operation. "Sumcheck = ssssssss" is the sumcheck of data that was just programmed into the last set member. "Set Sumcheck = ssssssss" is the sumcheck of all the set members that have been programmed.

OPERATION FAILED: Cannot erase device data

This message appears after UniSite was not able to erase an EEPROM. The device may be defective: try another device.

OPERATION FAILED: Device insertion error

When this message appears, the problem may be one of the following: either the device socket is not in the locked position, the device is inserted backwards or is not bottom-justified in the socket, or the device pins are not making good contact. Check the device's continuity in the socket and then try to program the part again. If the same message appears, try a different device.

OPERATION FAILED: Data load error

Data could not be read from the device during a load operation. Try the operation; if the message reappears, the device may be faulty.

OPERATION FAILED: Device over-current fault

This message appears when you attempt to program a socketed device that requires more programming current than the device you selected on-screen. The device may be faulty; insert another device into the socket and try the operation again.

OPERATION FAILED: Device programming error

This message appears when UniSite detected a defective memory cell in a device during the programming operation. If this message appears, try another device.

OPERATION FAILED: Device verify error (VCC nominal)

This message appears after UniSite has performed a device Verify operation and has found a memory cell that was programmed incorrectly. This message appears only if "1" was selected as the number of Verify passes (Vcc at the device's normal operating voltage). The number of Verify passes may be selected from both the Edit Programming Parameters screen and the Program Device screen. When this message appears, try another part.

OPERATION FAILED: Electronic signature verify error.

The device you tried to program did not have the correct electronic signature. Insert the correct device in the socket, or select a different device from the Select Device menu.

OPERATION FAILED: Illegal bit error.

This message appears when UniSite has detected a device that has a bit programmed to the incorrect state. When this message appears, try erasing the part (if possible) and then attempt to program the part again. If this message continues to appear, it may be because the device is defective. Discard the part and try another device. The illegal-bit check is selected from both the Programming Parameters screen and the Program Device screen.

OPERATION FAILED: Incompatible user data for the device selected.

This message appears when you attempt to load an inappropriate fuse map for the selected device. This message will appear only if a format-sensitive device, such as a logic device, was selected. If this message appears, select an appropriate device for the fuse map you intend to program.

OPERATION FAILED: Insufficient block size.

If the memory block size is set too small for the data file to be loaded into it, this message will appear. Increase the memory block size so that the entire file will fit into the device.

OPERATION FAILED: Security fuse programming error

This message appears when UniSite cannot program the security fuse. If this message appears, the device you are trying to program may be defective; try programming another device.

OPERATION FAILED: Security Fuse Violation.

If you tried to load, program, or verify data from a device that has its security fuse programmed, this message may appear. If this message appears, use a master device that does not have its security fuse programmed.

OPERATION FAILED: Structured test error (VCC high)

This message appears when UniSite has performed a functional test of a logic device and detected a failure. If you selected "2" for the number of Verification passes, one pass is performed while the lowest specified operating voltage is applied to the device, and the second pass is performed while the highest specified operating voltage is applied to the device. The above message is the result of a failed Verify at the high operating voltage applied. When this message appears, try another device.

OPERATION FAILED: Structured test error (VCC low)

This message appears when UniSite has performed a functional test on a logic device at the low operating voltage and has detected a failure. If you selected "2" for the number of Verification passes, one pass is performed while the lowest specified operating voltage is applied to the device, and the second pass is performed while the highest specified operating voltage is applied to the device. When this message appears, try another device.

OPERATION FAILED: Structured test error (VCC nominal)

This message appears when UniSite has performed a functional test on a logic part and discovered a bit that was not programmed. If you selected "1" as the number of Verify Passes, UniSite will verify the logic device at its normal operating voltage. When this message appears, try another device.

OPERATION FAILED: Verify data error (VCC high)

This message appears when UniSite has performed a Verify and has found a memory cell that was not programmed correctly. The device was verified while being operated with its highest operating voltage applied. When this message appears, try another device.

OPERATION FAILED: Verify data error (VCC low)

This message appears when UniSite has performed a Verify and has found a memory cell that was programmed incorrectly. The device was verified while being operated with its lowest operating voltage applied. When this message appears, attempt to program the device again. If this message reappears, try a different device.

OPERATION FAILED: Verify data error (Vcc nominal)

This message appears when UniSite has performed a Verify at the device's nominal voltage and has found a memory cell that was programmed incorrectly.

Options installed. Hit Return after changing your terminal settings.

This message appears in the Serial Port Configuration screen after the terminal serial port parameters have been changed and the carriage return key has been pressed. After this message appears, all output to the screen is suspended until a Return key is entered so that the user will have the opportunity to first configure his terminal to match the entered changes. Place the terminal in the setup mode (see your terminal's Instruction manual for setup procedure) and select the correct setting for the parameters that you changed in the Serial I/O screen.

Parameter Entered:

This message acknowledges that the parameter you entered was accepted.

Parameter field full. Hit return or arrows to enter.

This message appears when you have tried to enter too many characters into a parameter field. Press the carriage return key, the PF1 or PF2 keys, or use the arrow keys to enter the parameter.

Power down

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

POWER UP SELFTEST FAILED:

On power-up, UniSite checks all major systems. If there is a malfunction, an error message will be displayed at the top of the screen: "POWER UP SELFTEST FAILED". This message is accompanied by a list of problems detected by the self-test. Following is a list of those possible messages, and what to check. See the circuit description in section 3 for more details on operation.

FSM/PSM socket not empty.

If you get this error during the power-up self-test, check to make sure there are no devices in the programming sockets. If this error appears some time AFTER self-test, it could mean there is a bad Pin Driver board; see subsection 4.3 of this manual.

No FSM or PSM installed.

If you get this error, install the FSM or PSM and cycle the power (turn UniSite off and then on again). If the FSM or PSM are installed and you get this message, check U107 (74LS251) and U73 (74LS86) on the Controller board. These two are FSM/PSM detect devices. If either one of these is bad, replace both devices--electrostatic discharge (ESD) may have damaged them. See subsection 4.1 for information on reducing ESD.

No pin drivers installed.

UniSite must have a Pin Driver board installed in connector J5, the left-most connector, in order to pass the self-test. Make sure that the Pin Driver boards are properly installed.

PCU error.

If this error appears, cycle the power; if the message returns, then either the PCU is bad, there is a bad Pin Driver board in the left-most position, or the Waveform board is faulty.

Pin Driver error.

If this message appears, go to the self-test screen and check to see which Pin Driver board is faulty. Remove the top cover and the faulty Pin Driver board according to the procedure in section 2; then call your nearest Data I/O Service office and arrange replacement of the board.

User RAM failed.

This power-up message is displayed if the power-on version of the user RAM test fails.

Waveform board error.

If you get a Waveform board error, do the following: Remove the top cover according to the procedure in section 2. Next, switch the left-most Pin Driver board (the board installed at J5) with any other Pin Driver board. The reason for board swapping is that the Waveform board's self-test requires a functioning Pin Driver board in the left-most position. If the test passes after you swap board positions, you know the problem is with the Pin Driver, rather than the Waveform board.

NOTE

To fully calibrate the Site 40's PSM module, the first TEN Pin Driver board sockets (J5-J14) must contain a board. This is necessary so that the self-test may check all the FSM's relays.

Pre-format check.

This message appears when you have selected the Format Disk operation, and means that UniSite is checking to see if the disk you want to format is a system disk.

Preload is not supported by device.

This message appears when a preload vector in your data cannot be applied to the logic device.

Premature End-of-file detected.

If file delimiters are used for data transfer, this message will indicate that the file delimiter was detected during an unexpected condition (for example, within a data field). End-of-file delimiters are non-printable ASCII characters which are used only with printable ASCII-type translator formats.

Programmer set size limit (99) exceeded.

This error message occurs during a device serial set load operation, when the set member counter has been exceeded, yet the available memory has not. The programmer limit is 99 devices.

Programming hardware hasn't passed self-test. See Self-test screen.

This message appears if you attempt to select a Load, Program, Verify, Device Check or a Device Select screen when a self-test has failed. These screens cannot be entered until sufficient hardware has passed self-test. At power-up, this condition may occur if a device was left in a socket: if so, remove the socketed part and cycle the power.

Reading user data file size

This message appears while UniSite is reading the data file size from disk.

Recording system state parameters.

This message appears after you select a file number for the set of system parameters that you want to save. This message remains until Unisite is finished recording the parameters.

Remote port is not properly connected.

This message appears when UniSite is in the transparent mode or is performing a data transfer operation, and the remote port is not properly connected. The front panel LEDs indicate when the remote port is properly connected.

Restore operation aborted: save area empty

This message appears when you try to restore a set of configuration or system parameters that are not on the system disk you are using. Select a configure file filename.

Restoring system state variables.

This message appears while UniSite is reading the recorded system variables from the selected file.

RTE Init err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

RTC err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

Saving data to file.
This message appears while data is being written to a file on disk.

Saving parameters
This message appears when UniSite is saving the selected variables onto the disk.

Saving job file.
This message appears when UniSite is saving a job file.

Search pattern not found
If you specified a data pattern for a file that does not contain that pattern, this message will appear. This message appears while UniSite is in the memory editor or in the under/overblow display.

Selection process aborted due to disk change.
This message appears if you change diskettes while using the Device Select screen. Because the device manufacturer and part number screens rely on the presence of the system disk, UniSite aborts the operation. Insert the system disk and try the operation again.

Selection process aborted due to disk change.
You removed the disk before UniSite had finished reading the device's algorithm data. Insert the system disk and press the carriage return key.

Socket is empty.
The FSM or PSM sockets are empty when a device-related operation is being attempted. This error condition will not abort the device operation.

System parameters restored:
This message appears when you have restored a configure file from the Restore Programming Parameters screen.

System parameters saved:
This message appears when you save a set of system parameters.

Task cr err
UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

TEST ABORTED: Both waveform board & PCU must pass before Pin driver test.
If you selected self-tests for the Pin Driver boards, and either the Waveform board or the Pin Control Unit did not pass the self-test, this message will appear. Perform separate self-tests on both the Waveform board and the Pin Control Unit, to determine which is failing. See the Troubleshooting section of this manual.

TEST ABORTED: Diskette not installed.
If you selected either Drive A or Drive B from the self-test screen, but a formatted disk is not in that drive, this message will appear. Insert a formatted disk into the drive and try the test again.

TEST ABORTED: Drive B not installed.

If you selected drive B from the self-test screen, but drive B is not installed, this message will appear. Install the disk drive, or select Drive A.

TEST ABORTED: FSM and PSM not installed.

If you selected a self-test for either the Waveform board, Pin Control Unit, or Pin Driver board, and the PSM and FSM are not installed, this message will appear. Install one or both of the modules.

TEST ABORTED: FSM not installed.

If you selected the FSM test from the self-test screen and an FSM is not installed, this message will appear. Install the module and try the self-test again.

TEST ABORTED: PSM not installed.

If you selected the PSM test from the self-test screen and a PSM is not installed, this message will appear. Install the module and try the self-test again.

TEST ABORTED: Selected pin driver board is not installed.

The Pin Driver board you attempted to self-test is not installed. Install the board or select a different board to test.

TEST ABORTED: Waveform board test must pass before PCU can be tested.

This message appears when you have attempted to perform a self-test on the Pin Control Unit (PCU) when the Waveform board has failed its self-test. Correct the problem with the Waveform board and try the operation again. See the Troubleshooting section of the manual.

Testing

This message appears when a self-test is in progress.

TEST HALTED: Socket not empty, hit return to continue, ^Z to abort.

The self-test that you are attempting requires that the device socket does not contain any devices. Remove the socketed part and try the operation again, or type CTRL Z to abort the operation. Note: If you press the carriage return key, UniSite will run the test and the socketed device could be damaged.

The operation was not enabled

If you aborted the disk format or disk duplication operation by not changing "N" to a "Y" on the "Are You Sure?" prompt, this message will appear. Return to the Main menu or reattempt the operation.

Transferring data.

This message appears while a data transfer operation is being performed.

[transparent mode]

This message appears on the screen when UniSite enters the transparent mode.

Trc init err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

User RAM full.

This message appears when user RAM becomes completely full during a device loading operation. Change the memory block parameters and try the operation again.

User RAM sumcheck = ssssssss

This message contains the sumcheck for all of user RAM and is generated in the Sumcheck device check screen. This calculation is done regardless of whether or not user data is in RAM or on disk.

Vector out of range

The vector you tried to select does not exist for the device you have selected. Select an vector that is within the limits of the device or select a different device. This message may appear while you are using the vector editor.

Waiting for self-test completion.

This power-up message shows up only if you are changing the terminal selection before the power-up self-test has been completed.

WARNING! End of device exceeded

There is not enough room in the device to hold all the data you have specified. You may have the device beginning address set too high, the block size set too high, or you may need a larger device. Although the operation may still be performed, only part of the device will be programmed.

WARNING! End of file exceeded

This message appears when the memory block size and memory begin address parameters you specified in the Programming screen are too large enough for the data file you intend to use for programming. When this message appears, change the memory block size and memory begin address file size parameters so they are small enough to accommodate the data file. You can perform the operation without changing anything, but only part of the device will be programmed.

WARNING! End of user RAM exceeded

There is not enough user RAM for the amount of data you want to Load into it or program from it. You may have the device block size set too large, or the beginning RAM address too high. The operation may still be performed, but only part of the device will be programmed.

WARNING: Selection not compatible with other channel!

This message appears if you are scrolling through the list of baud rates for one port, and encounter a baud rate that is incompatible with the selected baud rate of the other port.

WARNING: Set size may be greater than programmer limit (99).

This message appears when the device set's determining variables (memory block size, data word-width, and device block size) indicated a set larger than 99. Adjust the variable sizes so the set number is smaller than 99.

WARNING: system disk in drive. Hit return to continue, ^Z to abort.

This message appears during any file operation that displaces disk data. Any information currently on the disk will be erased and is not retrievable. Press the carriage return key if you want to go ahead with the operation; CTRL Z, if you do not.

A.3 CRC ERROR MESSAGES

Following is a list of messages that appear while UniSite is being operated in the computer remote control mode. The list is in numerical order, according to the error code (left column).

ERROR CODE **MESSAGE and DESCRIPTION**

0x1f Cannot erase device error
This message appears after UniSite was not able to erase an EEPROM. The device may be defective: try another device.

0x20 Non-blank device
This message appears after UniSite has performed a blank check on a device and has detected bits that are not in their erased or blank state, and are not illegal bits. If you press the carriage return key, UniSite will proceed with the Programming operation and program over the existing data. If you press CTRL Z, the Program screen will reappear and you can try the operation again with another device. The Blank Check option in the Programming Parameters screen must be enabled before this test can be performed.

0x21 Illegal bit error
This message appears when UniSite has detected a device that has a bit programmed to the incorrect state. When this message appears, try erasing the part (if possible) and then attempt to program the part again. If this message continues to appear, it may be because the device is defective. Discard the part and try another device. The illegal-bit check is selected from both the Programming Parameters screen and the Program Device screen.

0x22 Device programming error
This message appears when UniSite detected a defective memory cell in a device during the programming operation. If this message appears, try another device.

NOTE

The two following messages have the same error code. In order for this message to appear, you must have selected command x23 (SELECT VERIFY OPTION). If "1" was specified as the variable, use the first description. If "2" was specified, use the second description.

0x23 Verify data error (Vcc Nominal)
This message appears when UniSite has performed a Verify and has found a memory cell that was not programmed correctly. The device was verified while being operated with its highest operating voltage applied. When this message appears, try another device.

0x23 Verify data error (Vcc low)
This message appears when UniSite has performed a Verify and has found a memory cell that was programmed incorrectly. The device was verified while being operated with its lowest operating voltage applied. When this message appears, attempt to program the device again. If this message reappears, try a different device.

0x24 Verify data error (Vcc high)

This message appears when UniSite has performed a Verify and has found a memory cell that was programmed incorrectly. The device was verified while being operated with its high operating voltage applied. When this message appears, attempt to program the device again. If this message reappears, try a different device.

0x27 End of user ram exceeded

There is not enough user RAM for the amount of data you want to Load into it or program from it. You may have the device block size set too large, or the beginning RAM address too high. The operation may still be performed, but only part of the device will be programmed.

0x30 Device algorithm not found

This message will occur if device selection is attempted using family/pinout codes, and the codes selected correspond to an algorithm which is not supported by UniSite.

0x2a Device insertion error

When this message appears, the problem may be one of the following: either the device socket is not in the locked position, the device is inserted backwards or is not bottom-justified in the socket, or the device pins are not making good contact. Check the device's continuity in the socket and then try to program the part again. If the same message appears, try a different device.

NOTE

The two following messages have the same error code. In order for this message to appear, you must have selected command x23 (SELECT VERIFY OPTION). If "1" was specified as the variable, use the first description. If "2" was specified, use the second description.

0x2b Structured test error (Vcc Nominal)

This message appears when UniSite has performed a functional test on a logic part and discovered a bit that was not programmed. If you selected "1" as the number of Verify Passes, UniSite will verify the logic device at its normal operating voltage. When this message appears, try another device.

0x2b Structured test error (Vcc low)

This message appears when UniSite has performed a functional test on a logic device at the low operating voltage and has detected a failure. If you selected "2" for the number of Verification passes, one pass is performed while the lowest specified operating voltage is applied to the device, and the second pass is performed while the highest specified operating voltage is applied to the device. When this message appears, try another device.

0x2c Structured test error (Vcc high)

This message appears when UniSite has performed a functional test of a logic device and detected a failure. If you selected "2" for the number of Verification passes, one pass is performed while the lowest specified operating voltage is applied to the device, and the second pass is performed while the highest specified operating voltage is applied to the device. The above message is the result of a failed Verify at the high operating voltage applied. When this message appears, try another device.

0x2d FSM/PSM for device not installed

The device you selected cannot be programmed in the PSM or FSM that is presently installed. If you select a device that is not supported by an installed PSM or FSM, then the Load, Program, Verify and Device Check screens cannot be entered. Install the correct module and try the operation again.

0x2e Programming Hardware hasn't passed self-test

This message appears after UniSite has performed a device Verify operation and has found a memory cell that was programmed incorrectly. This message appears only if "1" was selected as the number of Verify passes (Vcc at the device's normal operating voltage). The number of Verify passes may be selected from both the Edit Programming Parameters screen and the Program Device screen. When this message appears, try another part.

0x2f Insufficient pin driver boards installed for the device selected.

The device you are trying to load, program, verify or check requires more Pin Driver boards than are installed in your UniSite. Each Pin Driver board drives 4 pins. For example, a 16R8 in a PLCC package (28 pins with 8 "no connects") requires 28 pin-drivers; therefore, seven Pin Driver boards.

0x31 Device over-current fault

This message appears when you attempt to program a socketed device whose programming current is higher than the device you selected on-screen. The device may be faulty; insert another device into the socket and try the operation again.

0x40 I/O initialization error

An attempt to initialize the remote port with parameters has failed. Check connections and attempt the operation again.

0x41 Serial-framing error

The remote serial interface detected a start bit, but the stop bit was incorrectly positioned. Check the baud rate and stop bit setting for the remote port, or use hardware handshaking.

0x42 Serial-overrun error

The remote serial interface received characters that UniSite was unable to service. Check the baud rate and stop bit settings for the remote port, or use hardware handshaking.

0x43 Serial framing/overrun error

This is a combination of serial-framing error 0x41 and overrun error 0x42. Check the baud rate and stop bit settings for the remote port, or use hardware handshake.

0x46 I/O timeout

Too much time passed before UniSite received a JEDEC data file. The I/O timeout period may be changed via the Configure System's Communications Parameters screen.

0x52 Data verify error

The data from the remote port did not match the data in RAM. Check the data and try the operation again.

0x75 Security Fuse Violation

If you tried to load, program or verify data from a device that has its security fuse programmed, this message may appear. If this message appears, use a master device whose security fuse is still intact.

0x77 Security fuse programming error

This message will appear if UniSite cannot program the security fuse. If this message appears, the device you are trying to program may be defective; try programming another device.

0x79 Preload not supported by this device

This message appears when a preload vector in the programming data cannot be applied to the logic device.

0x81 Serial-parity error

The remote serial interface detected incoming data that had incorrect parity. Check the parity setting for the remote port.

0x82 Sumcheck error

The checksum of the data received (as the result of a JEDEC logic file download) did not match the checksum downloaded from the host computer. The host computer sends a transmission checksum and a fuse map checksum as a part of the data record. UniSite compares those checksums with the checksums it created on that same data. If the two checksums do not match, this message will appear, indicating that some of the data transmitted by the host was not received by UniSite. Try the operation again, and if the problem continues, verify that the checksums generated from the host are correct. If the checksums are correct, consult your UniSite Service Manual or contact your nearest Data I/O Service Center.

0x84 I/O format error

There is a compatibility problem with the data translation format you are using. Check the format of the data. The Computer Remote Control section of the UniSite Operator's manual contains a description of all the data translation formats supported by UniSite.

0x88 Invalid number of parameters

This error will be generated when a CRC command is preceded by an invalid number of parameters. Try entering the command again.

0x89 Illegal parameter value

This message will appear if an illegal parameter precedes a CRC command. Verify that the parameter is within the range specified for the command.

0x8A Insufficient block size

This message occurs when a Program or Verify operation is attempted with a memory block size of zero (which means there is no user data present). If you have selected the disk as the data source and specified a file length of zero, then the memory block size will also get set to zero. Change the block size to a usable value.

0x8B Error restoring/saving system parameters or restoring factory defaults.

An error has occurred while attempting to restore or save system parameters (commands FD or FE) or restoring factory defaults (command FC). Check to make sure the disk is not write-protected and that the valid system disk is in drive A.

0x8E File error

A disk file error has occurred during a command that accesses disk file, such as Upload yield tally (command 43]). The disk is probably write-protected. Remove the write-protection and try the operation again.

0x8F NON-JEDEC data present in RAM or a NON-logic device was selected with a JEDEC I/O translation

Check the JEDEC RAM data, or select a different I/O format or logic device.

0x90 Illegal I/O format

You tried to select an I/O format that is not supported by UniSite. Select a valid format.

0x94 Data record error

The data that you attempted to transfer did not conform with the selected translation format; edit the data file so that it matches one of UniSite's supported translator formats. See the UniSite Operator's manual for output samples of each translator.

0x97 Block move error

A block move within RAM has violated the RAM boundaries. Check the memory begin address and memory block size and try the operation again.

0x98 End of device exceeded

There is not enough room in the device to hold all the data you have specified. You may have the device beginning address set too high, the block size set too high, or you may need a larger device. Although the operation may still be performed, only part of the device will be programmed.

0x99 End of file exceeded

This message appears when the memory block size and memory begin address parameters you specified in the Programming screen are too large enough for the data file you intend to use for programming. When this message appears, change the memory block size and memory begin address file size parameters so they are small enough to accommodate the data file. You can perform the operation without changing anything, but only part of the device will be programmed.

0xa2 Electronic signature verify error

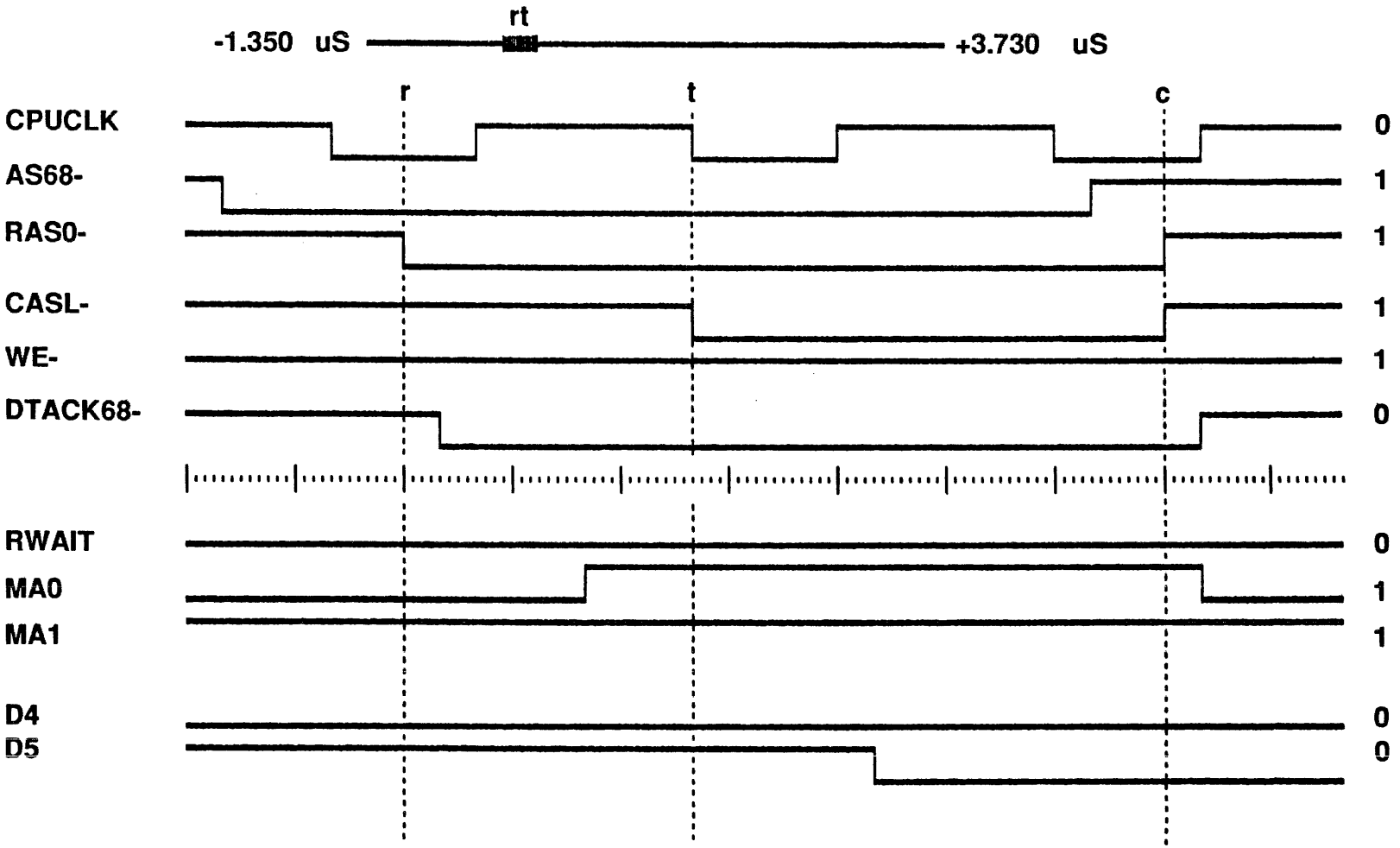
The device you tried to program did not have the correct electronic signature. Insert the correct device in the socket, or select a different device from the Select Device menu.

Appendix B
Waveforms

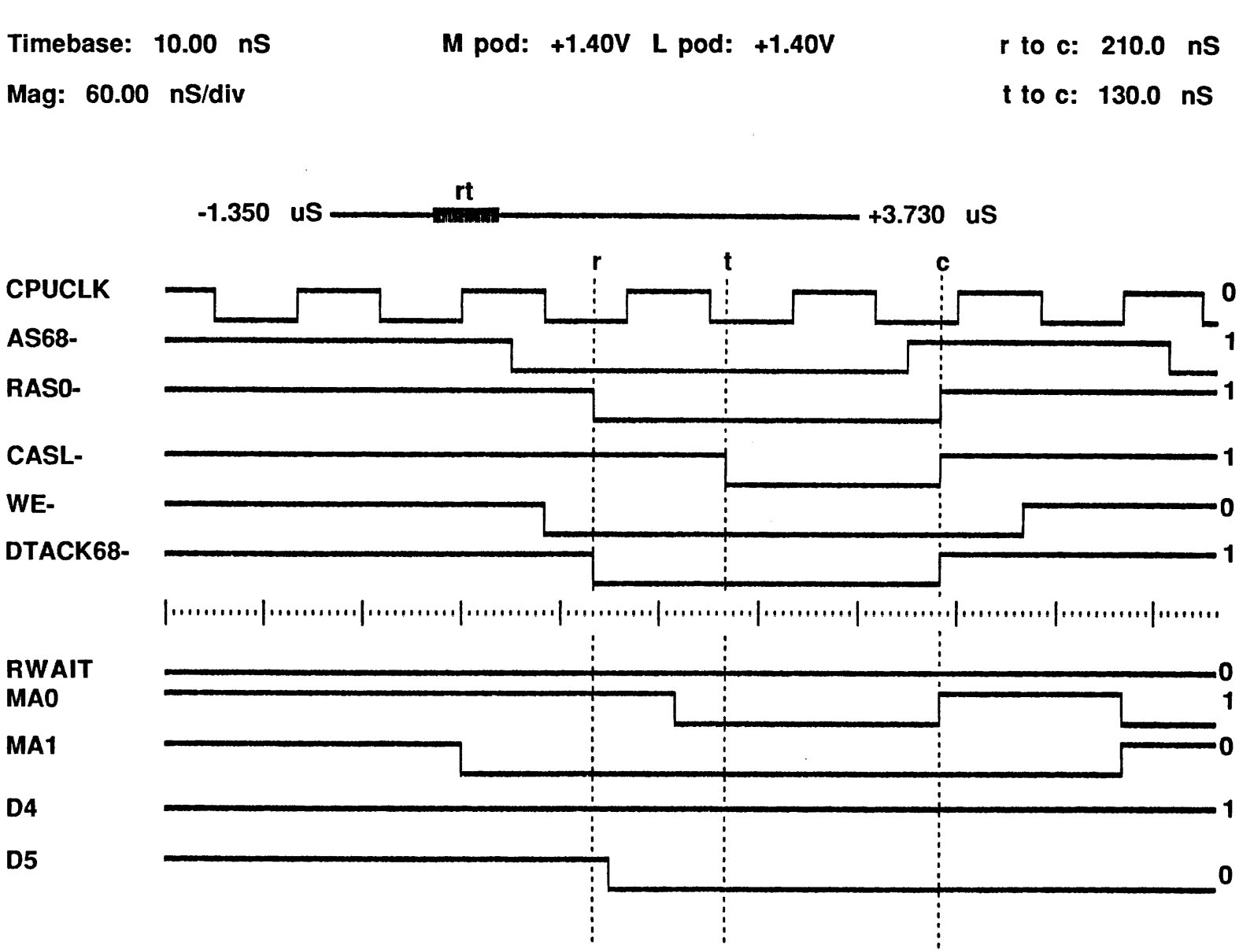
This appendix consists of a set of waveform diagrams, taken with a logic analyzer. You do not necessarily need an analyzer to compare waveforms, but using one will yield more information. An oscilloscope may also be used to compare portions of the waveforms. These waveforms are helpful in isolating UniSite memory problems.

Timebase: 10.00 nS M pod: +1.40V L pod: +1.40V r to c: 210.0 nS

Mag: 30.00 nS/div t to c: 130.0 nS



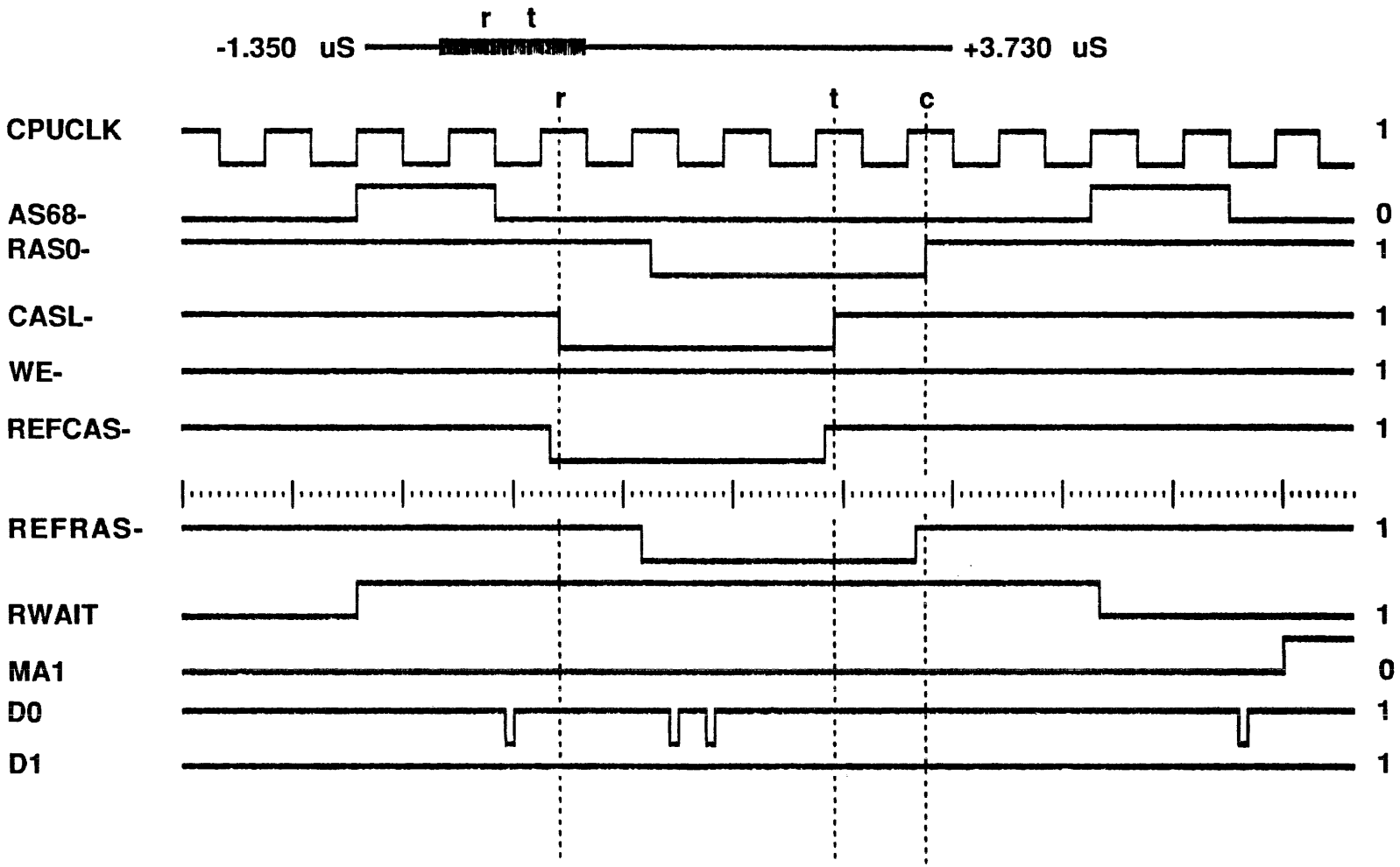
DRAM READ



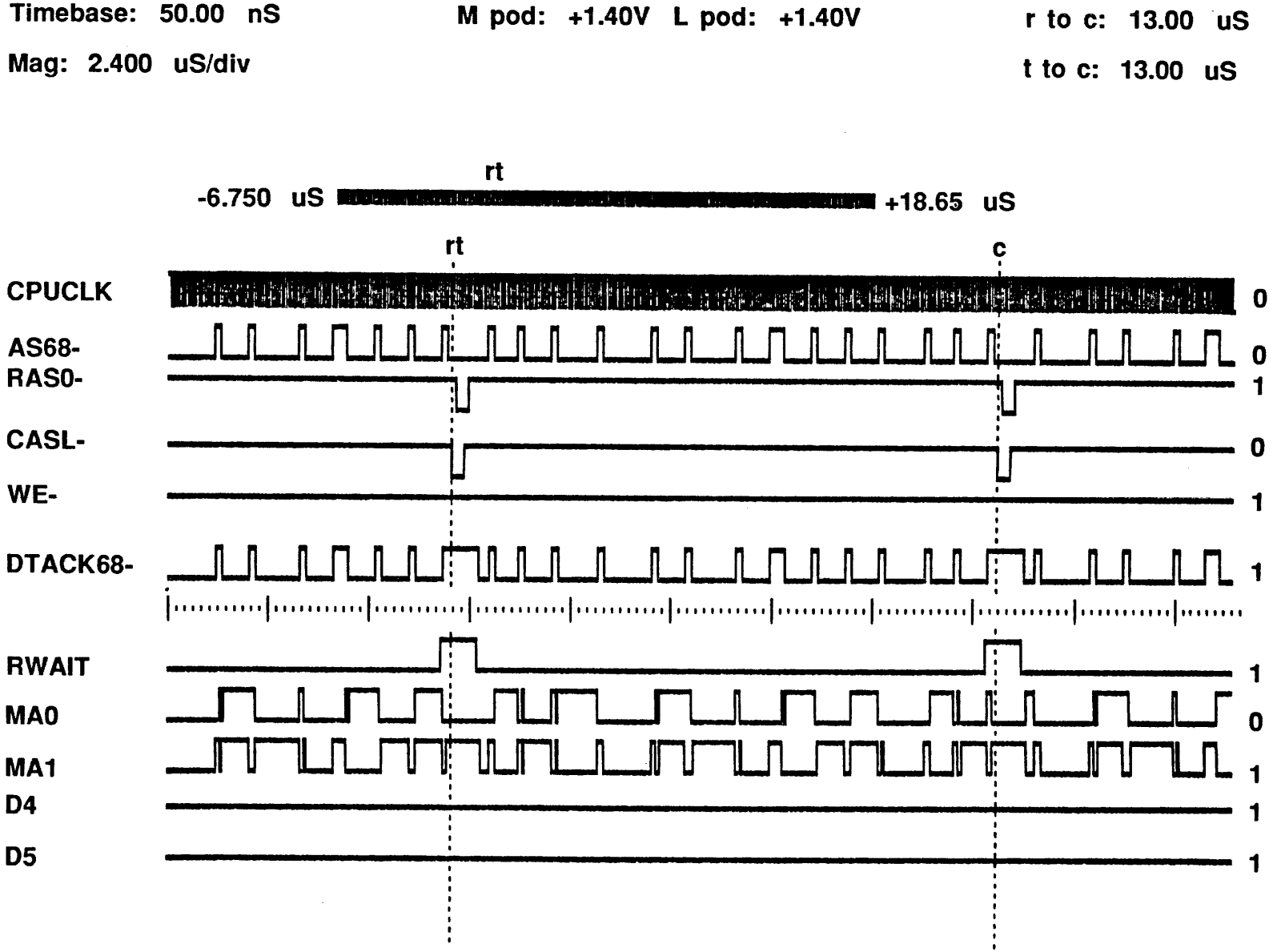
DRAM WRITE CYCLE

Timebase: 10.00 nS M pod: +1.40V L pod: +1.40V r to c: 400.0 nS

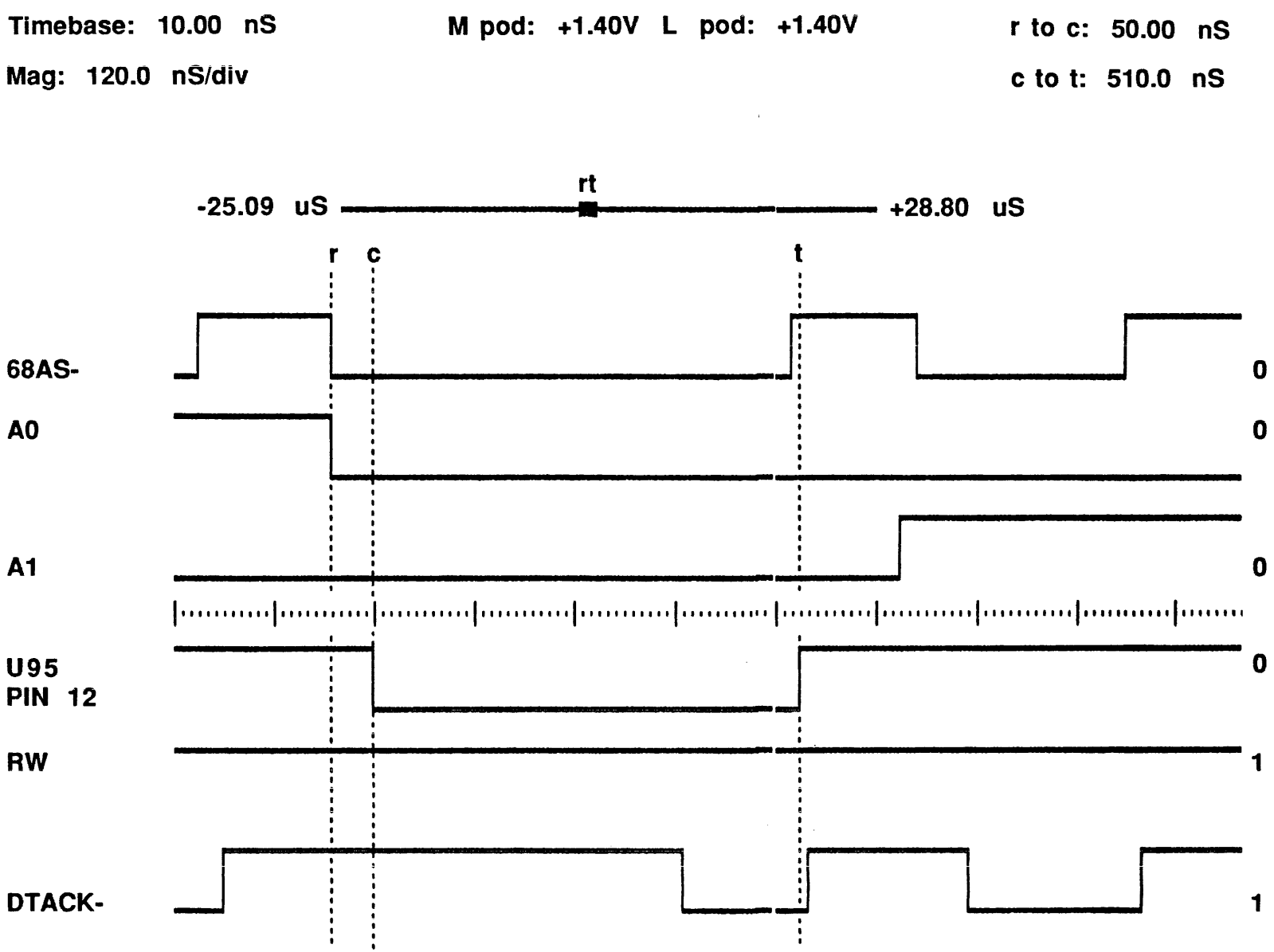
Mag: 120.0 nS/div t to c: 100.0 nS



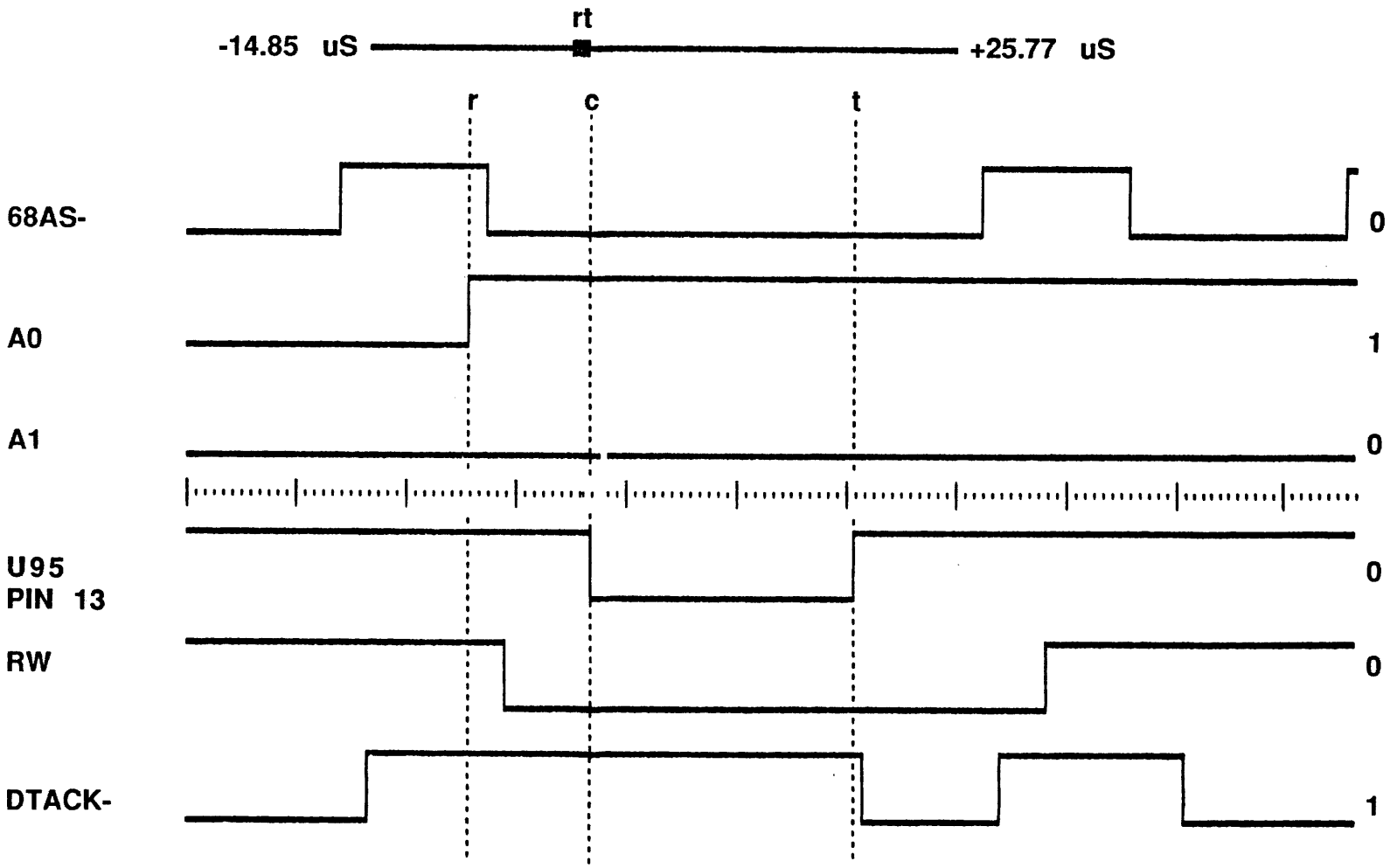
DRAM REFRESH CYCLE



DRAM REFRESH, TWO CYCLES



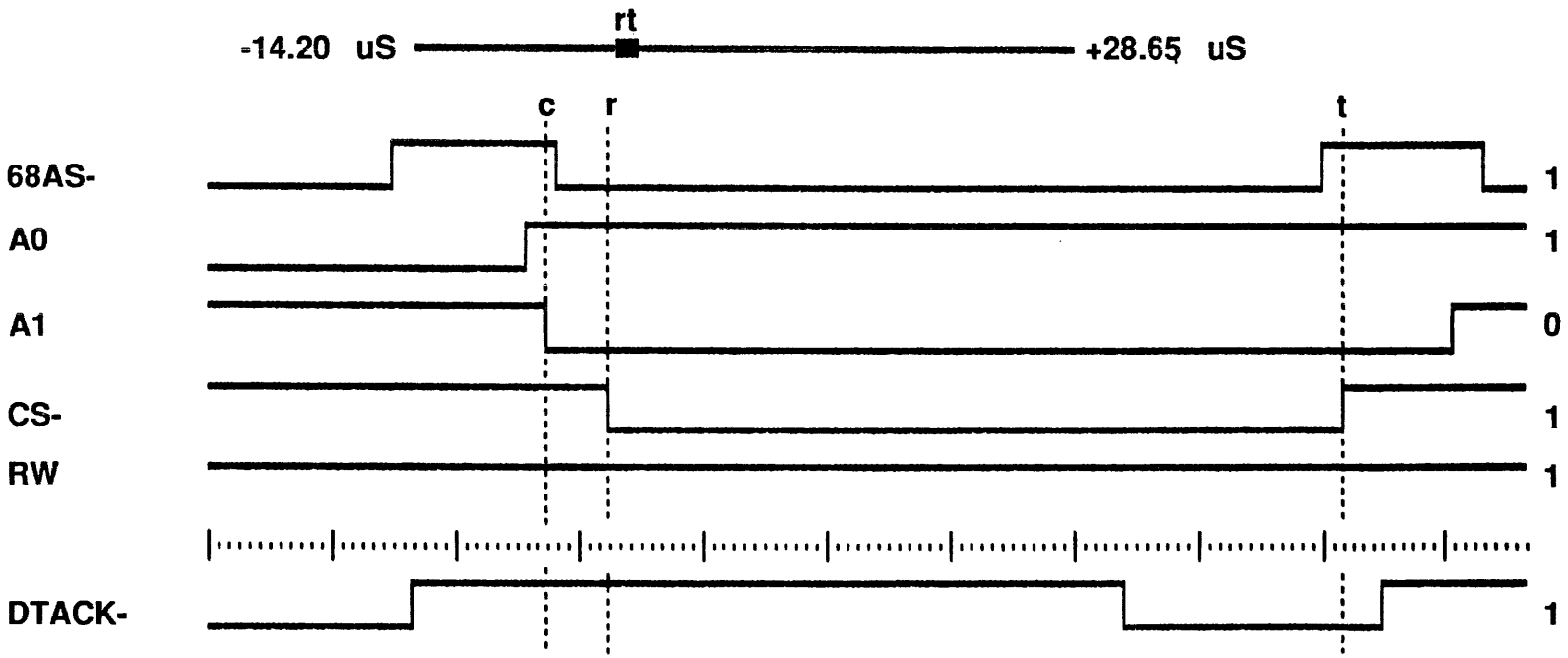
GENERAL I/O READS



GENERAL I/O WRITE OPERATION

Timebase: 10.00 nS M pod: +1.40V L pod: +1.40V c to r: 60.00 nS

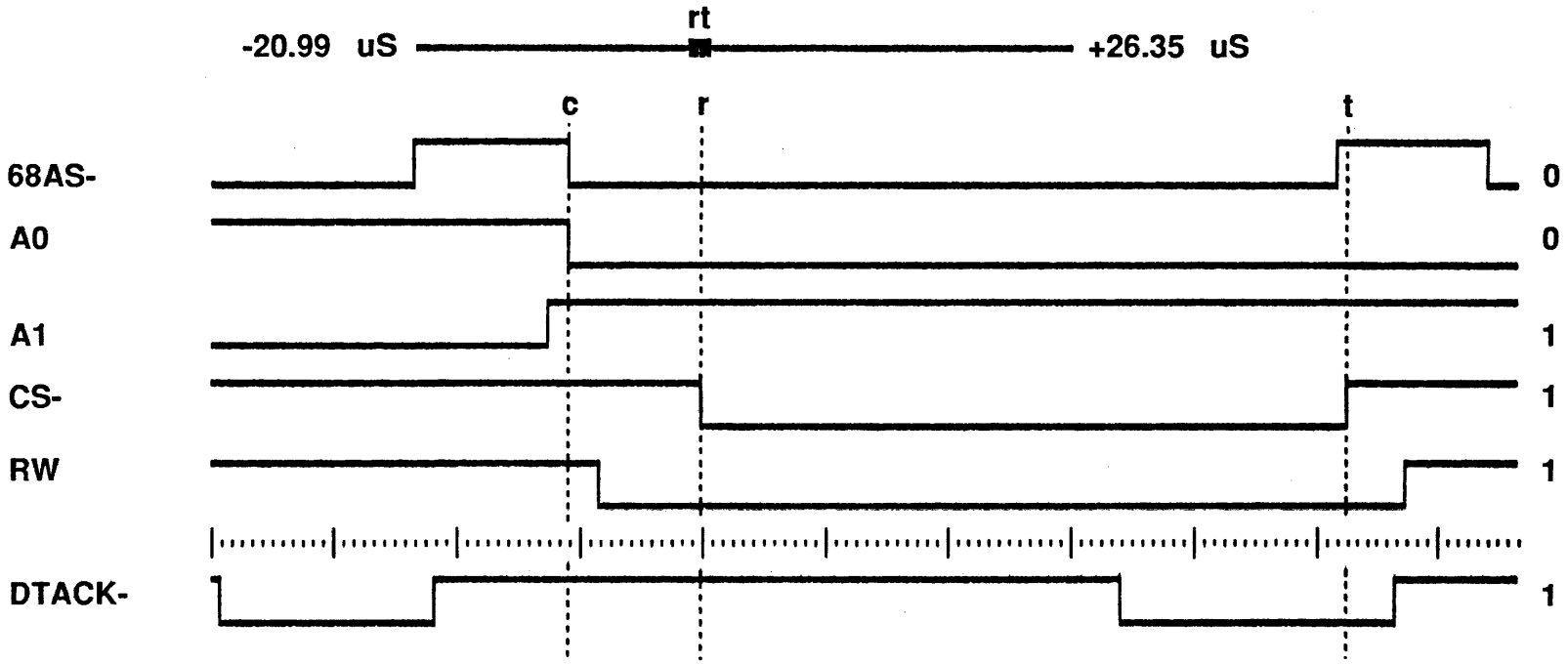
Mag: 120.0 nS/div c to t: 770.0 nS



68681 READ

Timebase: 10.00 nS M pod: +1.40V L pod: +1.40V c to r: 130.0 nS

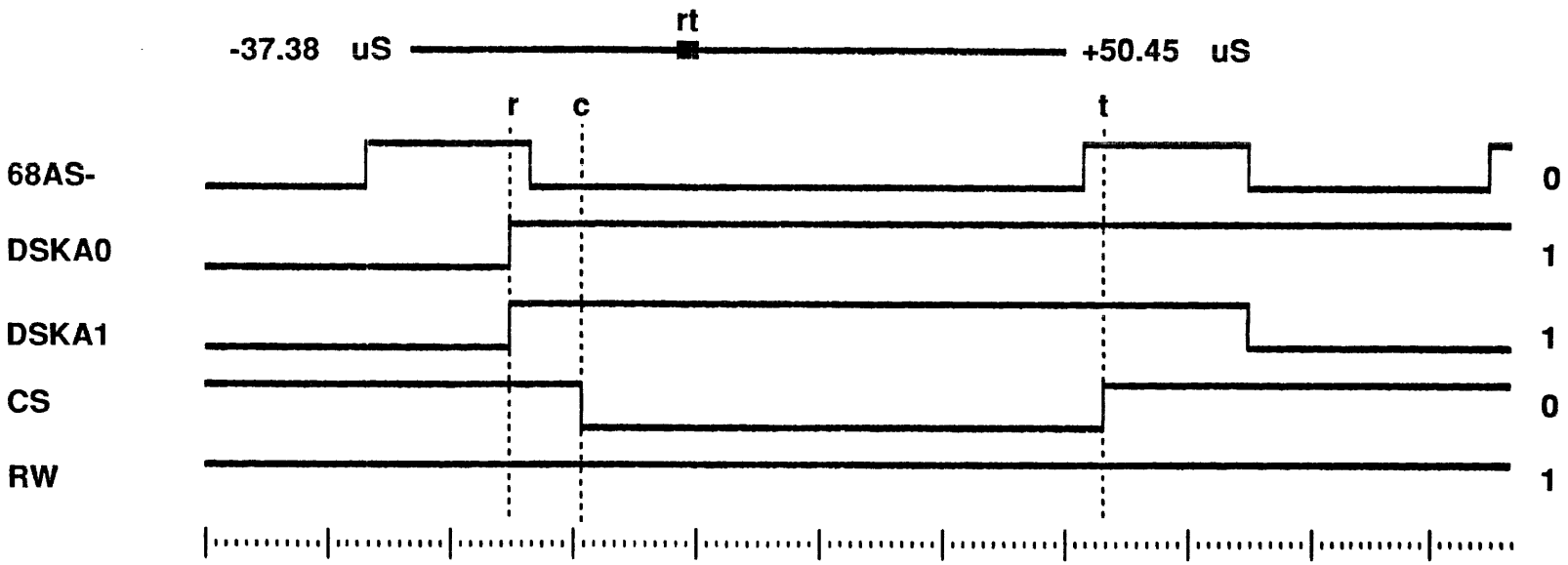
Mag: 120.0 nS/div c to t: 760.0 nS



68681 WRITE

Timebase: 10.00 nS M pod: +1.40V L pod: +1.40V r to c: 70.00 nS

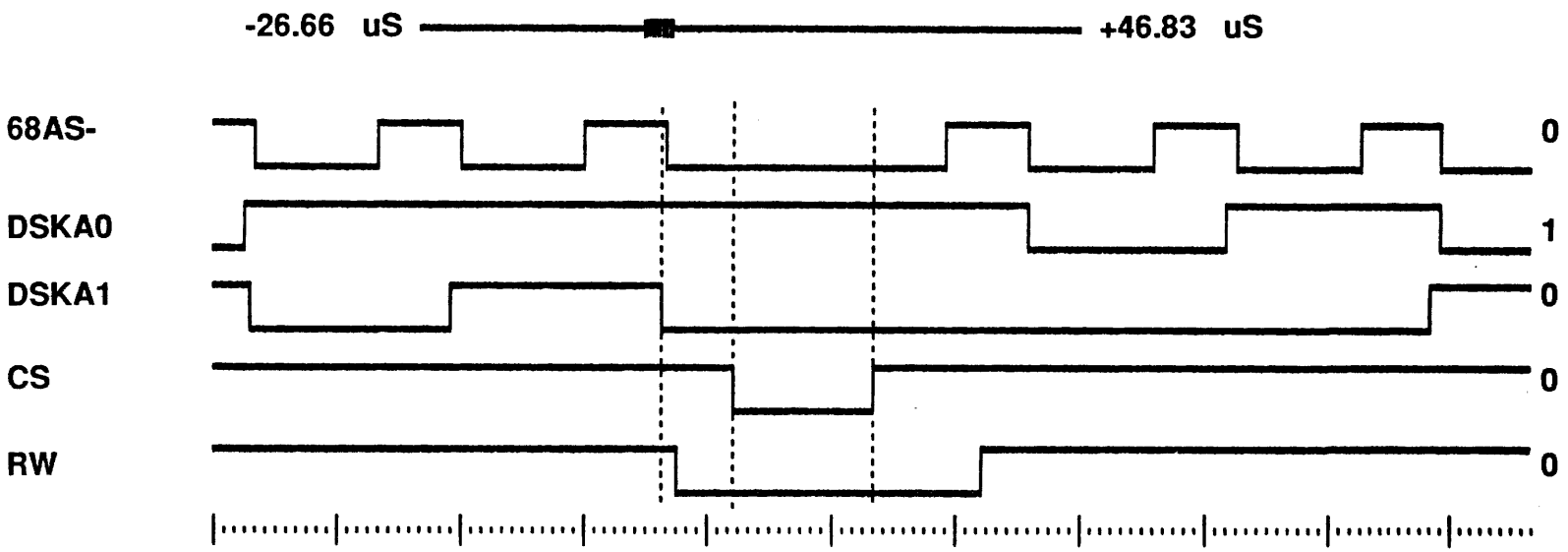
Mag: 120.0 nS/div c to t: 510.0 nS



1772 READ

Timebase: 10.00 nS M pod: +1.40V L pod: +1.40V r to c: 140.0 n

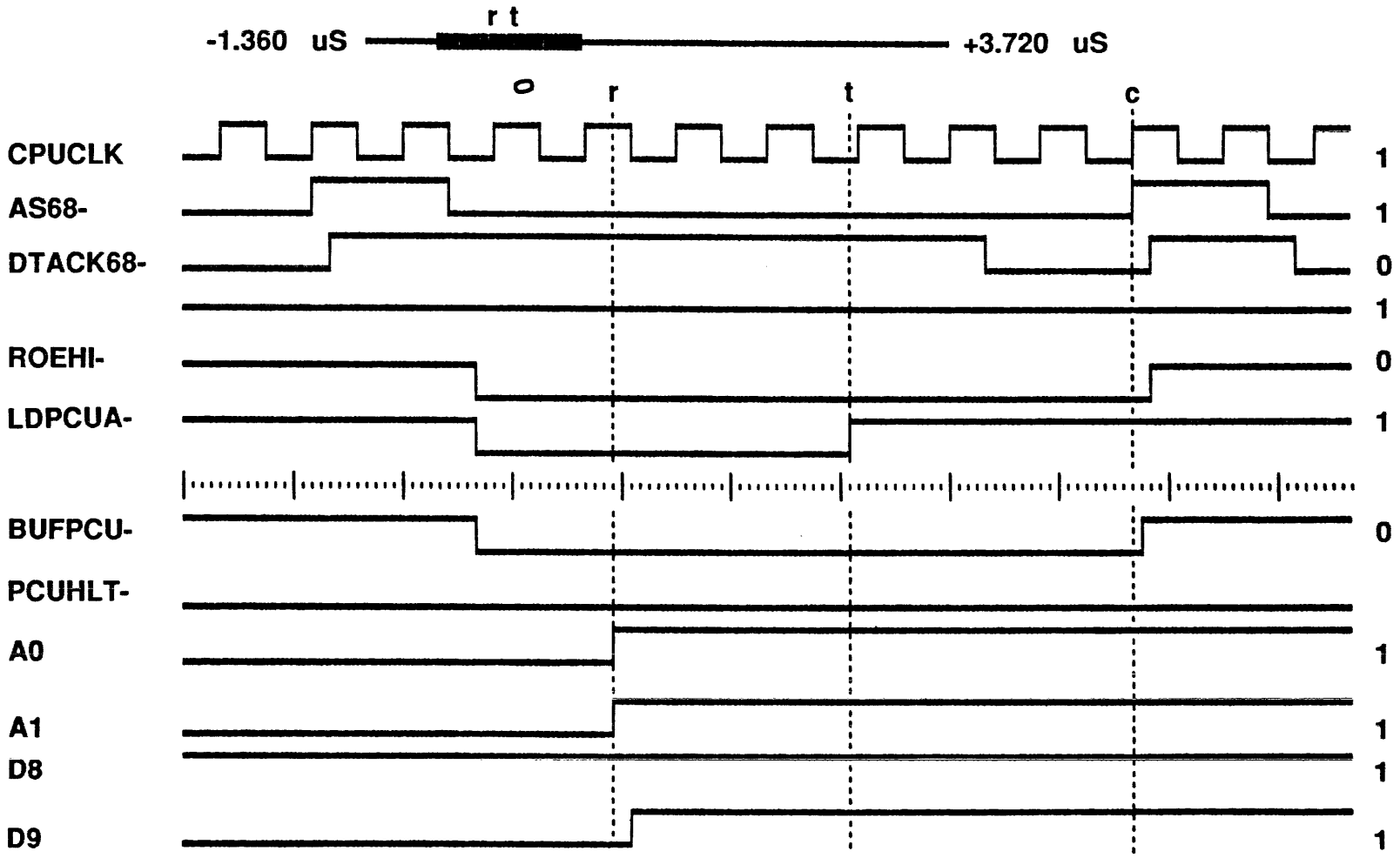
Mag: 240.0 nS/div c to t: 270.0 nS



1772 WRITES

Timebase: 10.00 nS M pod: +1.40V L pod: +1.40V r to c: 570.0 nS

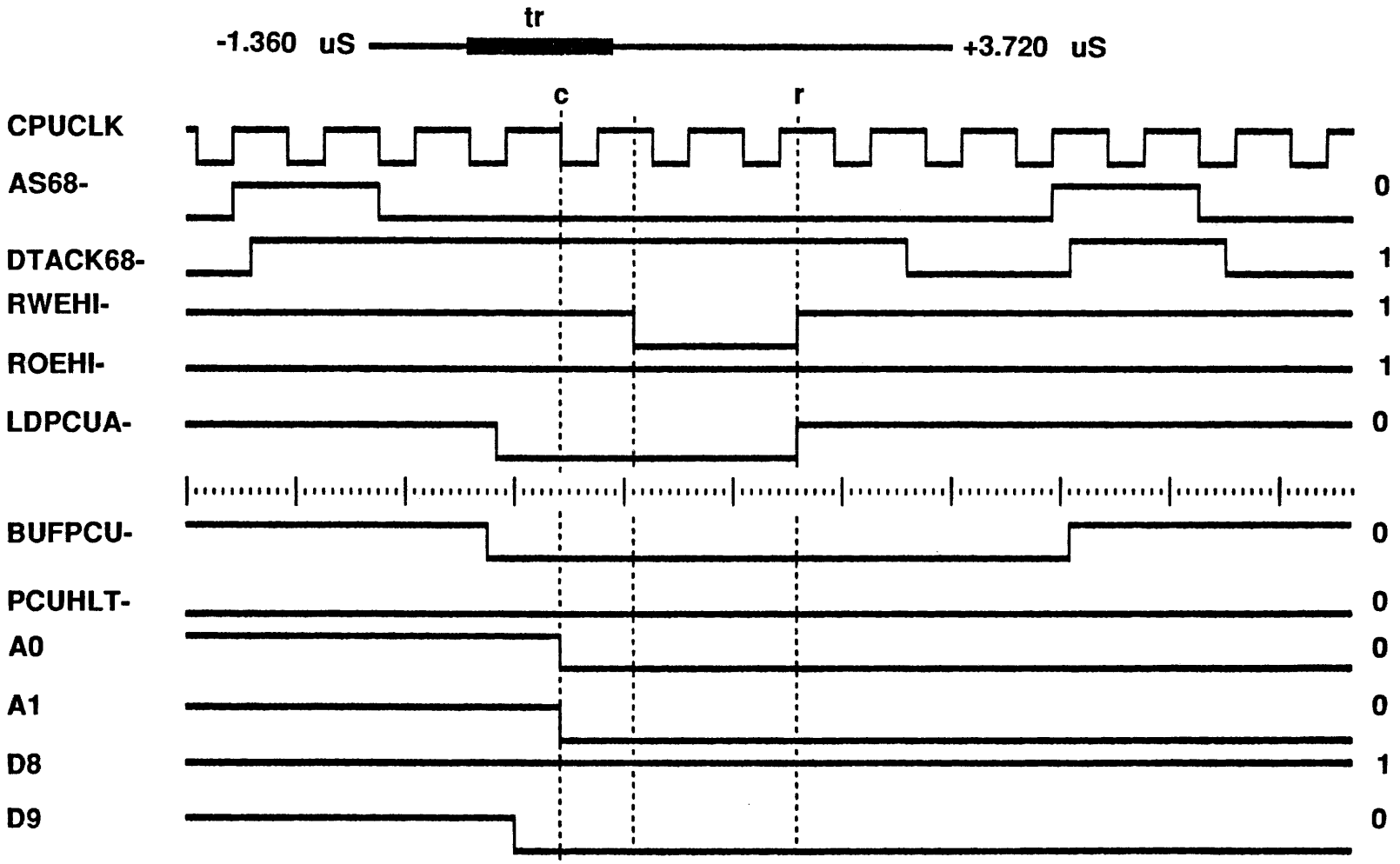
Mag: 120.0 nS/div t to c: 310.0 nS



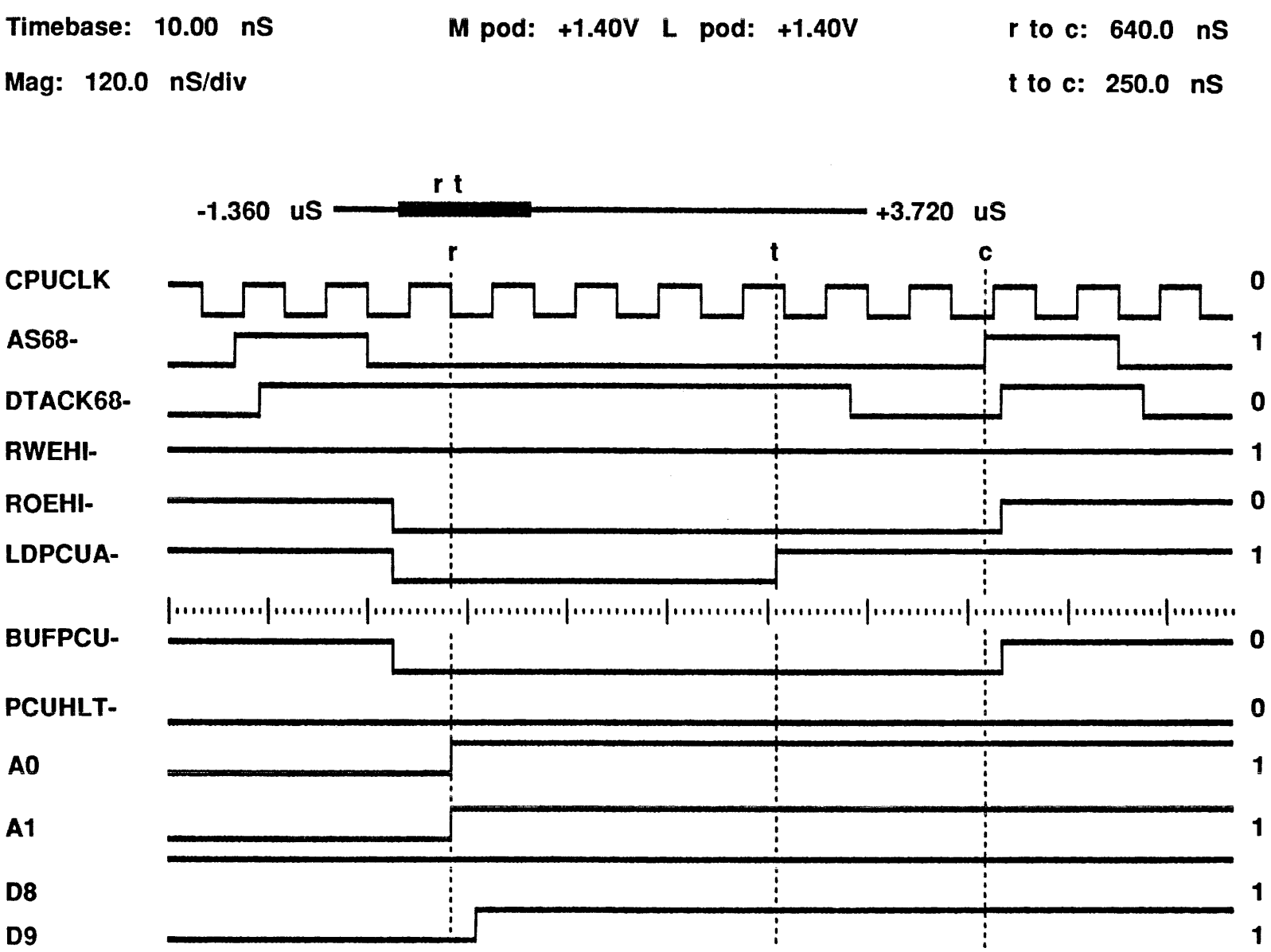
PCU RAM READ

Timebase: 10.00 nS M pod: +1.40V L pod: +1.40V c to r: 260.0 nS

Mag: 120.0 nS/div c to t: 80.00 nS



PCU RAM WRITE


Timebase: 10.00 nS
M pod: +1.40V L pod: +1.40V
r to c: 640.0 nS
Mag: 120.0 nS/div
t to c: 250.0 nS
r t
-1.360 uS
+3.720 uS
r
t
c
CPUCLK
AS68-
DTACK68-
RWEHI-
ROEHI-
LDPCUA-
BUFPCU-
PCUHLT-
A0
A1
D8
D9
0
1
0
1
0
1
0
0
1
1
1
1

PCU RAM READ

Appendix C
Mnemonics

This table lists the main signal and bus line mnemonics used on the Controller Board schematic, and gives a description of each. Use this table as a helpful reference when reading the circuit description or when troubleshooting UniSite.

BUS/LINE MNEMONIC	DESCRIPTION
68K	68000 CPU control bus
ADR/CNT	Strobe used to latch control and address information in PCU.
AEN	Address enable; signal latching address to pin logic chips.
AGND	Sense line for ground at PSM/FSM
AS	Buffered address strobe from 68K
AS68	Address strobe directly from 68K
BERR	Bus error signal to 68K
BGACK	Bus grant acknowledge from DMA peripheral
BUFENA	Buffer enable for 68K data bus
BUFPCU	PCU RAM buffer
CMPF	Compare line from FSM bus
CSFLPY	Floppy controller (1772) select
CSSER	68681 DUART select
CSWFBD	Chip-select line for Waveform Board
DAT/DLY	Strobe signal used to latch data and delay information in PCU.
DCHG	Disk change signal from floppy disk
DIRIN	Floppy disk step direction
DRDY	Floppy disk ready
DSKRST	Floppy disk reset
DSKEOJ	Disk end-of-job interrupt
DSKDRQ	Disk data request interrupt
DTACK	Data acknowledge to the 68K
DUTVCC	Device-under-test (DUT) Vcc

BUS/LINE MNEMONIC	DESCRIPTION
EEWR	EEPROM write strobe
EHELLO	Expansion board insertion/removal interrupt
EVOKE	Instruction cycle execution signal in PCU
EXPINT	Expansion board interrupt
FAST	Fast/slow delay select in PCU
FCHC	Fine-current high clamp
FCLC	Fine-current low clamp
FCHR	Fine-current high rail (used by pin driver)
FCLR	Fine-current low rail (used by pin driver)
FHELLO	FSM insert/removal interrupt
FPD	FSM pin driver bus
FSMAS	FSM addr strobe from 68K
FSMDTK	FSM data acknowledge to 68K
FSMINT	FSM interrupt to 68K
HLOENA	Insert/removal interrupt disable/enable
HLT68	68000 halt
INCADR	PCU instruction address increment
INDEX	Index pulse from floppy disk drive
IPD	Internal pin driver bus
IRQ681	Interrupt request from 68681 DUART
LATCHP	Latch output signal to PSM, used to transfer serial data to LEDs and relays
LDS	Buffered lower data strobe from 68K; indicates D0-D7 are being used.
LDS68	Lower data strobe direct from 68K.
LDPCUA	Load PCU address
LSIF	Serial output data to FSM, used to initialize virtual address to pin logic chips

BUS/LINE MNEMONIC	DESCRIPTION
LSII	Serial output data to IPD bus, used to initialize virtual address to pin logic chips
LSOI	Serial input data from IPD bus (pin logic chips)
MA0-MA7	Memory address bits 0-7 to DRAM
MOTON, MOTORON	Motor-on signal to floppy disk drive
OCINT	Overcurrent interrupt from Waveform board to 68K
OCTRIP	Overcurrent trip-line from Pin Driver boards to the Waveform board (2.5V threshold point)
OVCENA	Overcurrent interrupt enable
OVERCUR	Overcurrent interrupt output
OVERIDE	Override diskette write-protection
PCUDLY	Write strobe from 68K, used to load the 12-bit slow-delay counter in the PCU
PCUENA	PCU interrupt enable
PCUHOLD	Hold signal from PCU instruction decoder to counters.
PCUINT	PCU interrupt
PCURST	PCU reset
PCUS0,PCUS1	PCU serial data shift register's direction select lines
PD	Pin driver bus
PGND	Programming ground; the high-current ground for programming supplies
PHELLO	PSM insert/removal interrupt
PUP1	Pullup resistor 1
PUPALY	Pullup resistor to sense-line relay control flip/flop
RAM	RAM data
RDATA	Read data from floppy disk
RDDUT	Read device-under-test's (DUT's) data
RDINT	Read interrupt status

BUS/LINE MNEMONIC	DESCRIPTION
RDMISC	Read LSO, SODAT, PCU and disk status
RDPCUA	PCU address readback
RDSER	Read serial status
RDSHFT	Read shift register
REFACK	Refresh acknowledge
REFCAS	Refresh column-address strobe
REFRAS	Refresh row-address strobe
ROEHI	Output enable (high-order) to PCU RAM
ROELO	Output enable (low-order) to PCU RAM
RST68	68000 reset
RTCINT	Real-time clock interrupt enable
RWEHI	Write enable (high-order) to PCU RAM
RWELO	Write enable (low-order) to PCU RAM
RXRDY	Receiver-ready interrupt from 68681 to the 68000
SCLKF	Serial clock to FSM: used for LEDs, relay, ID, shift data clock
SCLKP	Serial clock to PSM: used for LEDs, relay, ID, shift data clock
SIDATP	Serial data sent to PSM, LEDs and relays
SIDATF	Serial data sent to FSM, LEDs and relays
SIDE, SIDE1	Side-select signals to disk drives
SODATF	Serial data from FSM: identifier code
SODATP	Serial data from PSM: identifier code
STEP	Floppy disk's step-to-next-cylinder signal
STRT, STRTPCU	Start PCU signals
TRK0	Track zero indicator from floppy disk
TSTCLR	GenRad test input, used to clear PCU counters.
UDS	Buffered upper data strobe from 68K

BUS/LINE MNEMONIC	DESCRIPTION
UDS68	Upper data strobe direct from 68K
VCS	Virtual chip select from PCU to pin driver bus
VPA68	Valid peripheral address, also used for auto-vector interrupt acknowledge
WRDATA	Write data to floppy disk
WRDSK	Write strobe for disk-control signals
WRGATE	Floppy disk write enable
WRLED	Write strobe for LEDs and interrupt enable latches
WRMISC	Write strobe for setup clocks, data and control
WRPROT	Write-protect status from floppy disk
WRRELAY	Write strobe for FSM/PSM sense relay
XAEN	Address enable signal to FSM and internal pin driver bus
XPCLK	Clock signal used for generating device-under-test (DUT) processor clock or structured test clocks
XRCLK	Receive DUT data latch signal
XVCS	Virtual chip select signal to FSM and internal pin driver bus

Appendix D
Schematics

Table D-1. List of Schematics

Part Number	Description
30-701-2011	Waveform board
30-701-2012	Controller board
30-701-2114	Expansion RAM board
30-701-2021	PSM board
30-701-2042	FSM board

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE				
B	INCORP ADCN'S A1,A2,A3 PER ECP 0262				
C	INC. ADCN B1,B2 ECP 0262	MP			1-87
D	INC. ADCN C1,C2. ECP 0369,0376	BV			5-10-87

+10, +5, -10V REFERENCES

COMPARATOR REFERENCE

REFERENCE 0

REFERENCE 1

REFERENCE 2

REFERENCE 3

VCC

VCCSENSE

DUTVCC

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATORS USED: CS9; CR45, J2, D57, R201, TP6, U34, VR3
4. POWER AND GROUND OF DEVICES:

REF. DES.	+5V	GND
U3, 4, 11, 12, 13, 14	20	10
U15	14	7
U24	24	12

5. UNUSED GATES: +5V, 74HCT04 (U15), LM148 (U21)
6. GROUND SYMBOLS: = ANALOG GROUND; = PROGRAM GROUND; = DIGITAL GROUND
7. PNP DARLINGTON FOR Q40, 42, 45, 48:
8. NPN DARLINGTON FOR Q41, 46, 49:
9. COMPONENTS OMITTED: C54

ANALOG BUS
COMPARATOR BUS
POWER BUS
DECODE BUS
ADDRESS BUS
DATA BUS
OVERCURRENT BUS

701-2011-005

DRAWN TLOTH	DATE 7/2/86	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED B. Valdivia	7/3/86	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM WAVEFORM BOARD
ELEC ENG P.L.S.	7/29/86	DO NOT SCALE DRAWING	SIZE D; FSCM NO. 54193; DRAWING NO. 30-701-2011
MECH ENG D.N.	7/29/86		SCALE NONE; D.A.D.; SHEET 1 OF 3
MFG ENG C.R.J.	7/29/86		
QUAL ASSUR E.B.	7/29/86		
APPD P.L.S.	7/29/86		

C.G.

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
D	SEE SHEET 1	TLL 7-18-86	BJ 7-7-86	[illegible]	9-1-86

OVERVOLTAGE CROWBAR 42V 1.5V TRIP POINT

V+ & V- SUPPLIES

FINE CURRENT REFERENCES

FINE CURRENT CLAMPS

LOGIC HIGH & LOGIC LOW SUPPLIES

COMPARATOR LATCHES

DECODE PAL

POWER BUS
DECODE BUS
ADDRESS BUS
DATA BUS
ANALOG BUS
COMPARATOR BUS
OVERCURRENT BUS

DRAWN TLOTH	DATE 7/1/86	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM WAVEFORM BOARD
ELEC ENG		DO NOT SCALE DRAWING	SIZE D · FSCM NO. 54193 · DRAWING NO. 30-701-2011
MECH ENG			SCALE NONE · SHEET 2 OF 3
MFG ENG			
QUAL ASSUR			
APPD			

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
D	SEE SHEET 1	[illegible]	BV 7-8-85	[illegible]	8-1-86

OVERCURRENT INTEGRATOR

COARSE CURRENT SUPPLY

40 PIN CONNECTOR

40 PIN CONNECTOR

BUFFERS

OUTPUT LATCH

+40 & -10 SUPPLIES

SLEW RATE REFERENCE

PIN CLAMP REFERENCE

POWER BUS

ANALOG BUS

COMPARATOR BUS
POWER BUS
DECODE BUS
ADDRESS BUS
DATA BUS
ANALOG BUS
OVERCURRENT BUS

DRAWN TLOTH	DATE 7/16/86	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM WAVEFORM BOARD
ELEC ENG			
MECH ENG		DO NOT SCALE DRAWING	SIZE D · FSCM NO. 54193 · DRAWING NO. 30-701-2011
MFG ENG			SCALE NONE · SHEET 3 OF 3
QUAL ASSUR			
APPD			

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
4	RELEASE	JK		K.C.	4-1-6
B	INCORP ADCN A1, A2, A3 PER ECP # 262	JK	BY 1-12-87	K.C.	1-9-87

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTERS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE 50V.
3. ALL DIODES ARE 1N4148.
4. LAST REFERENCE DESIGNATOR USED: U121, J26, C171, Y1, R212, CR14, DS4, JP4, SW2, TP13, K1, G1
5. POWER AND GROUND:

REF.DES.	GND	+5V
U37-40, 42, 46 67, 68, 78, 99, 110	7	14
U41, 43, 44, 90, 93, 97, 98, 100, 111, 112	8	16
U50, 83-85, 91 92, 95, 96, 113	10	20
U60, 61	14	28
U62	16, 53	14, 49

6. UNUSED REFERENCE DESIGNATORS R106 - R199
7. ⏚ = DIGITAL GROUND

Note: The following configurations are valid for the PROM jumpers:
A - 27128, JP3 (open), JP4 (open)
B - 27256, JP3 (1 to 2), JP4 (open)
C - 27512, JP3 (1 to 2), JP4 (1 to 2)
D - X2864A, JP3 (2 to 3), JP4 (open)

Note: The POWER ON initialization routine must provide a delay of 130 usec prior to using the dynamic memory. This delay insures that the memory's receive at least 8 CAS before RAS cycles before they are used.

Note: The Kernel test plug will not work with most emulators. The input buffers in most emulators increase the loading such that the resistors cannot force the Moveq instruction on the bus properly.

Note: Any 68000 emulator which is used with this board must support continuous Address Strobe, otherwise the DRAM will NOT be refreshed.

	DRAWN	DATE
	CHECKED	4/1/86
	ELEC. ENG	4/1/86
	MECH. ENG	4/1/86
	MFG. ENG	4/1/86
	QUAL ASSUR	4/1/86
	APPR'D	4-1-6

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

TITLE: SCHEMATIC DRAWING, UNISITE CONTROLLER BD.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-2012

SCALE NONE SHEET 1 OF 8

701-2012-004

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	SEE SHEET ONE	JK	BZ 3-27-86	J.C.	4-1-6

FLOPPY DISK CONTROLLER

WD1772

74HCT244

74LS86

74LS04

74LS38

74LS240

HCT00

74LS259

FLOPPY DISK CONNECTOR

J26

DSKRST

DCHG-

INDEX-

DS0-

DS1-

MOTON-

DIRIN-

STEP-

WRDATA-

WRGATE-

TRK0-

WRPROT-

RDATA-

SIDE1-

DRDY-

DGND

68K 1.82

WGATE

RESET-

WRDSK-

PCUS0 (SEE PAGE 3)

PCUS1 (SEE PAGE 3)

POWER-LOSS WRITE PROTECT

PCUDLY (SEE PAGE 3)

PCUDLY- (SEE PAGE 2)

PCURST-

WRLED-

SELFTEST

REMOTE

TERMINAL

PCUENA

OVCENA

RTCENA

HLOENA

R68 180 3950 DS1 POWER ON

R70 180 3850 DS2 SELF-TEST

R69 180 3850 DS4 REMOTE

R71 180 3850 DS3 TERMINAL

R96 3.3KSIP

74LS112

74LS74

74LS08

74LS02

74LS174

74LS148

74LS251

PCUINT-

OVERCUR-

RTCINT-

EXPINT-

FSMINT-

FHELLO-

PHELLO-

IRQ68I-

RXRDY-

INT1- INT2- INT3- INT4- INT5- INT6- INT7-

DSKEOJ

DSKDRQ

FSM INT ENABLE

PSM/FSM CHANGE DETECTOR

INTERRUPT CONTROLLER

D7

RCINT-

A3 A2 A1

POWERFAIL-

IPL0- IPL1- IPL2-

CPUCLK

POWERFAIL-

PUP1

POWER ON RESET

THIS CIRCUIT ALSO INSURES THE DISK DRIVE IS WRITE PROTECTED DURING POWER ON AND POWER OFF.

NOTE: THE 1N4623 WAS CHOOSEN FOR LOW LEAKAGE CURRENT AND SHOULD NOT BE SUBSTITUTED.

1N4623 4.3V CR13

LM339

R80 330K

C78 1.0uF 10TAN

R81 6.8K 1.2V HYSTERESIS

R78 750

R76 68

R77 6.8K

R79 3.3KSIP

RST68-

HLT68-

EEWR-

REF2.5

R-/W

POWER AND GROUND:

REF.DES.	GND	+5V
U30	12	3
U36, 68, 73, 40, 119, 116, 114	7	14
U106, 75, 76, 105, 107, 117, 103	8	16
U104, 115	10	20
U102	14	15

UNUSED GATES:

		DATE
DRAWN	Hilda Crisfulli	3/24/86
CHECKED	Barry V.	3/27/86
ELEC ENG	Hilda Crisfulli	3/26/86
MECH ENG		
MFG ENG		
QUAL ASSUR		
APPD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± XXX ± ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

TITLE: SCHEMATIC DRAWING, UNISITE CONTROLLER BD.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-2012

SCALE NONE SHEET 2 OF 8

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	SEE SHEET ONE	JK	BV 3-27-86	J.C.	4-1-86

PD 7.B7

IPULSE

PCUINT-

68K 1.C2

PIN CONTROL UNIT

PROGRAM COUNTER

CONTROL STORE RAM

74LS161A

2015-90

74F08

74HCT244

74HCT373

74LS299

74LS151

74LS74

74F374

74F174

74F10

74F00

16R8A

PCU 4.C7

INSTRUCTION DECODER

FAST COUNTER

LOOK-AHEAD RIPPLE CARRY

SLOW COUNTER

START/STOP TIMING GENERATOR

VCS/AEN TIMING GENERATOR

START PULSER

PCU ADDRESS READBACK

SERIAL READ REGISTER

CLOCK SELECTOR

TEST POINTS

RCLK PCLK VCS PHLT TEST

(PROGRAMMABLE CLK FROM 68681)

CLK0.5 0.5MHz

CPUCLK 10MHz

PCUCLK 8MHz

CLK4 4MHz

CLK2 2MHz

CLK1 1MHz

CLOCK CONTROLLED BY PCU

(BUFFERED PCLK)

POWER AND GROUND:		
REF.DES.	GND	+5V
U53, 78, 110, 109, 120, 74	7	14
U19, 26, 52, 71, 27, 54, 72, 105	8	15
U11, 24, 17, 28, 49, 70, 104	10	20
U25, 29	12	24
U51, 79, 69	8	16

Note: The following test points shall be designated on the silkscreen with same names: TEST, VCS, PCLK, RCLK, PHLT

DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED	3/21/86		
ELEC ENG	3/21/86	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE: SCHEMATIC DRAWING, UNISITE CONTROLLER BD.
MECH ENG		DO NOT SCALE DRAWING	
MFG ENG			SIZE D · FSCM NO. 54193 · DRAWING NO. 30-701-2012
QUAL ASSUR			SCALE NONE · SHEET 3 OF 8
APPD			

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	SEE SHEET ONE	JK	BV 4-1-86	P.C.	4-1-6

PORT A (TERMINAL)

PORT B (REMOTE)

Note: The zener's, caps, and series resistors shown in the serial circuit provide ESD protection and reduce the EMI.

POWER AND GROUND:

REF.DES.	GND	+5V	+12V	-12V
U1, 2, 3	4		8	5
U8, 12, 13, 120	7	14		
U6, 7, 18	8	16		
U14	20	40		

DRAWN	Vince Warhol	DATE	3/28/86
CHECKED	Barry V.		4/1/86
ELEC ENG	Keller Campbell		3/28/86
MECH ENG			
MFG ENG			
QUAL ASSUR			
APPD			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

TITLE: SCHEMATIC DRAWING, UNISITE CONTROLLER BD.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-2012

SCALE NONE SHEET 4 OF 8

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	SEE SHEET ONE	JK	BV 3-27-86	P.P.	4-1-6

PCU 3.D2

68K 1.D2

INTERNAL PIN DRIVER BUS IPD 8.B8

FSM PIN DRIVER BUS FPD 7.A8

PPD 7.C3

TO PSM

PIN LOGIC READBACK BUFFER

OR READ DATA FROM FSM AND INTERNAL BUS

BUS TERMINATION

Note: R1, R2 shown above are located at the far end of the IPD bus

POWER AND GROUND:		
REF.DES.	GND	+5V
U4, 5, 40, 116	7	14
U77, 118	8	16
U9, 10, 15, 16, 21, 23, 48, 113	10	20

DRAWN	Kelley Cronquist	3/21/86
CHECKED	Barry V.	3/27/86
ELEC ENG	Kelley Cronquist	3/21/86
MECH ENG		
MFG ENG		
QUAL ASSUR		
APPD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR

DO NOT SCALE DRAWING

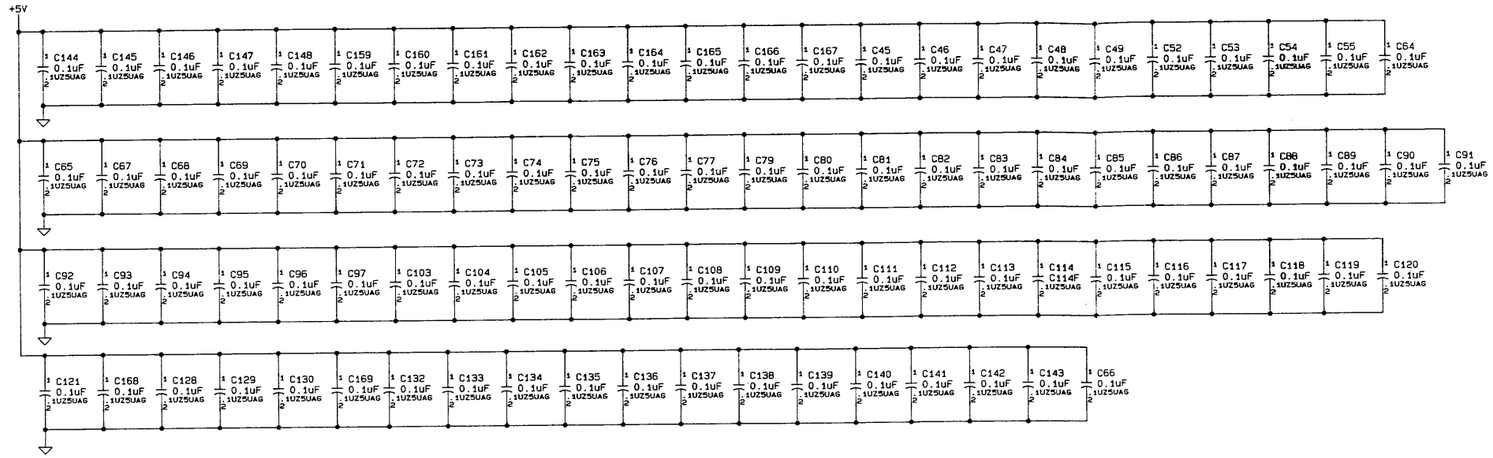
DATA I/O REDMOND, WASH.

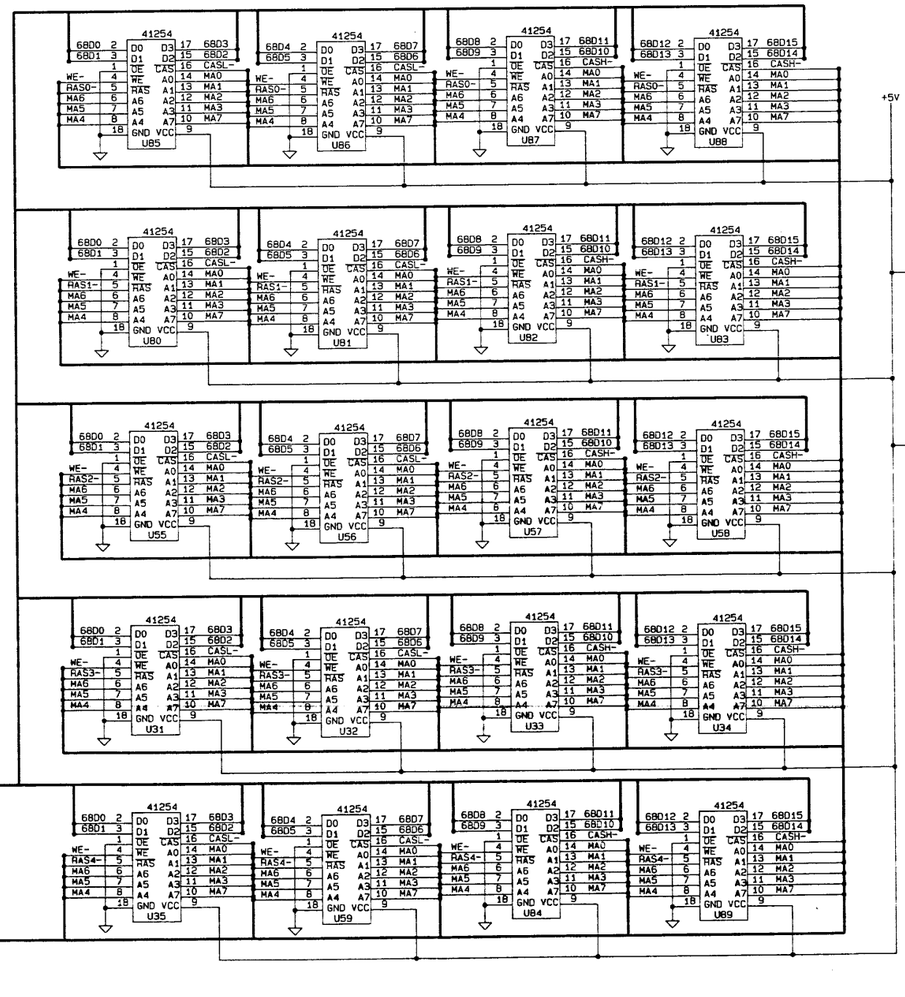
TITLE: SCHEMATIC DRAWING, UNISITE CONTROLLER BD.

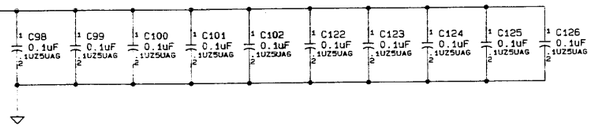
SIZE D | FSCM NO. 54193 | DRAWING NO. 30-701-2012

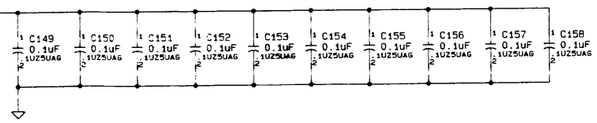
SCALE NONE | SHEET 5 OF 8

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	SEE SHEET ONE	JK	BV 3-27-86	R.P.	4-1-6









POWER AND GROUND:

REF.DES.	GND	+5V
U31-35, U80-U89, U55-U59	18	9

DRAWN	Lisa Wachel	DATE 3/24/86
CHECKED	Barry V.	3/27/86
ELEC ENG	Kelly Griffith	3/24/86
MECH ENG		
MFG ENG		
QUAL ASSUR		
APPD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

TITLE: SCHEMATIC DRAWING, UNISITE CONTROLLER BD.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-2012

SCALE NONE SHEET 6 OF 8

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	SEE SHEET ONE	JK	BV 3-27-86	KC.	4-1-86

TEST POINTS

Note: The test points shown below are located immediately next to the power connector, along front edge.

POWER SUPPLY CONNECTOR

Note: The ground test point shown below is located directly below the 68000.

THIS RESISTOR MAINTAINS CURRENT THROUGH THE CONNECTOR TO KEEP THE CONTACT CLEAN. THE POWER SUPPLY SHALL SOURCE 1.0 MA AT 2.7 VOLTS WHILE POWER IS VALID.

68K 1.82

PCU 3.82

WAVEFORM BOARD CONNECTOR

J1

REF0	1	40	REF1
REF2	2	39	REF3
VSLEW	3	38	CMPREF
FCHR	4	37	FCLR
AGND	5	36	VCCSENSE
FCHC	6	35	FCLC
CC	7	34	CLAMP
PGND	8	33	PGND
VLH	9	32	VLH
VLL	10	31	VLL
PGND	11	30	PGND
V+	12	29	V+
V-	13	28	V-
PGND	14	27	PGND
+48V	15	26	+48V
DUTVCC	16	25	DUTVCC
+21V	17	24	+21V
-15V	18	23	-15V
PGND	19	22	-15V
+40V	20	21	+40V

J2

-10V	1	40	-10V
OCTRIP-	2	39	IPULSE
RESET-	3	38	
R/W-	4	37	
	5	36	
CSMFB-	6	35	OCINT-
DGND	7	34	DGND
D15	8	33	D7
D14	9	32	D6
D13	10	31	D5
D12	11	30	D4
D11	12	29	D3
D10	13	28	D2
D9	14	27	D1
D8	15	26	D0
DGND	16	25	+5V
A8	17	24	A4
A7	18	23	A3
A6	19	22	A2
A5	20	21	A1

POWERFAIL-
FHELLO-
FHELLO-
DTACK5-

74LS244 U46: RESET-, UDS-, LDS-, R/W-, CPUCLK, TEST-

74LS245 U20: D0–D7, R/W-, FSM-

74LS245 U101: DB–D15, R/W-, D1, WRRELAY-

74LS373 U22: A1–A8, AS

74LS373 U47: A9–A16, AS

74LS373 U45: A17–A23, AS, FSMINT-

OCINT-

FSMDTK-

74LS02 U68

74LS86 U73

R97 3.3K

SENSE LINE SELECTOR

R213 750

R214 750

74F74 U99

Q1 2N2907

D1 1N4002 CR14

VCCSENSE
AGND
PAGND
FAGND
PVCSENSE
FVCSENSE

(FSM / BENCH TEST) CONNECTOR

J24A

	1		
CMPREF	2	39	REF3
REF3	3	38	CMPREF
FCHC	4	37	FCLR
V+	5	36	VCCSENSE
CC	6	35	FCLC
PD50	7	34	CLAMP
PD53	8	33	PGND
PD57	9	32	VLH
PD60	10	31	VLL
PD64	11	30	PGND
PD67	12	29	V+
PD44	13	28	V-
PD41	14	27	PGND
PD37	15	26	+48V
PD34	16	25	DUTVCC
PD30	17	24	+21V
PD27	18	23	-15V
PD23	19	22	-15V
PD20	20	21	+40V

J24B

FAGND	1	40	REF1
REF0	2	39	REF3
PGND	3	38	CMPREF
VLL	4	37	FCLR
FVCSENSE	5	36	VCCSENSE
VSLEW	6	35	FCLC
PGND	7	34	CLAMP
PD50	8	33	PGND
PD53	9	32	VLH
PD57	10	31	VLL
PD61	11	30	PGND
PGND	12	29	V+
PD47	13	28	V-
PD43	14	27	PGND
PD40	15	26	+48V
PGND	16	25	DUTVCC
PD33	17	24	+21V
PD29	18	23	-15V
PGND	19	22	-15V
PD23	20	21	+40V

J24C

1	FCLR	2	REF1
3	CLAMP	4	VLH
5	PGND	6	PD48
7	PD51	8	PD52
9	PGND	10	PD62
11	PD65	12	PD45
13	PGND	14	PD39
15	PD36	16	PD32
17	PGND	18	PD25
19	PD22	20	PD18
21	PGND	22	PD11
23	PD8	24	PD4
25	PD0	26	+21V
27	+48V	28	FPCUR/W-
29	C2	30	AD2
31	DGND	32	CMPF
33	LSTF	34	RESET-
35	DGND	36	UDS-
37	D2	38	D6
39	DGND	40	D13
41	FSMDTK-	42	A4
43	DGND	44	A11
45	A14	46	A18
47	DGND	48	STOATF

J24D

FCHR	1	2	REF2
FCLC	3	4	V-
DUTVCC	5	6	PD49
PD52	7	8	PD56
PD59	9	10	PD63
PD66	11	12	PD45
PD42	13	14	PD38
PD35	15	16	PD31
PD28	17	18	PD21
PD17	19	20	PD14
PD10	21	22	PD7
PD3	23	24	-15V
PGND	25	26	PGND
DGND	27	28	C0
C3	29	30	A03
A06	31	32	CLK
VCC-	33	34	FSMINT-
R/W-	35	36	D0
D3	37	38	D7
D10	39	40	D14
A1	41	42	A5
A8	43	44	A12
A15	45	46	A19
A22	47	48	SODATP

PD 8.88

PGND

NOTE: THIS CAPACITOR IS USED TO DECREASE THE CURRENT SPIKE GENERATED BY PLUGGING IN THE PSM.

C170 1.0uF

PSM CONNECTOR

J23A

1	SODATP	2	
3	DGND	4	
5	PD0	6	
7	PD4	8	
9	PD7	10	
11	PD11	12	
13	PD14	14	
15	PD18	16	
17	PD21	18	
19	PD25	20	
21	PD28	22	
23	PD32	24	
25	PD35	26	
27	PD39	28	
29	PD42	30	
31	PD46	32	
33	PGND	34	

J23B

1	SIDATP	2	+5V
3	PD1	4	PGND
5	PD8	6	PD12
7	PD15	8	PGND
9	PD22	10	PD26
11	PD29	12	PGND
13	PD36	14	PD40
15	PD43	16	PGND
17	PVCSENSE	18	

J23C

1	SCLKP	2	
3	DGND	4	
5	PD2	6	
7	PD5	8	
9	PD9	10	
11	PD23	12	
13	PGND	14	
15	PD37	16	
17	PGND	18	
19	PD44	20	
21	PD47	22	
23	PAGND	24	

J23D

1	LATCHP	2	
3	CLAMP	4	
5	PD3	6	
7	PD6	8	
9	PD10	10	
11	PD13	12	
13	PD17	14	
15	PD20	16	
17	PD24	18	
19	PD27	20	
21	PD31	22	
23	PD34	24	
25	PD39	26	
27	PD41	28	
29	PD45	30	
31	DUTVCC	32	
33	PHELLO-	34	

Notes:

1) DGND (digital ground) is tied to PGND (programming ground) and at the power connector.

2) AGND is a sense line of the DUT ground used on the waveform board

POWER AND GROUND:

REF.DES.	GND	+5V
U68, 73, 99	7	14
U20, 22, 45-47, 101	10	20

3) = PROGRAMMING GROUND

= DIGITAL GROUND

Note: All connectors shown on this page shall have silkscreen designations on the pcb which indicates both row and column of each end of the connector.

FPD 5.D3
PPD 5.A2

DRAWN	Vince Warhol	DATE	3/26/86
CHECKED	Barry V.		3/27/86
ELEC ENG	Peter Campbell		3/26/86
MECH ENG			
MFG ENG			
QUAL ASSUR			
APPD			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED
.XX ±
.XXX ±
ANGULAR

DO NOT SCALE DRAWING

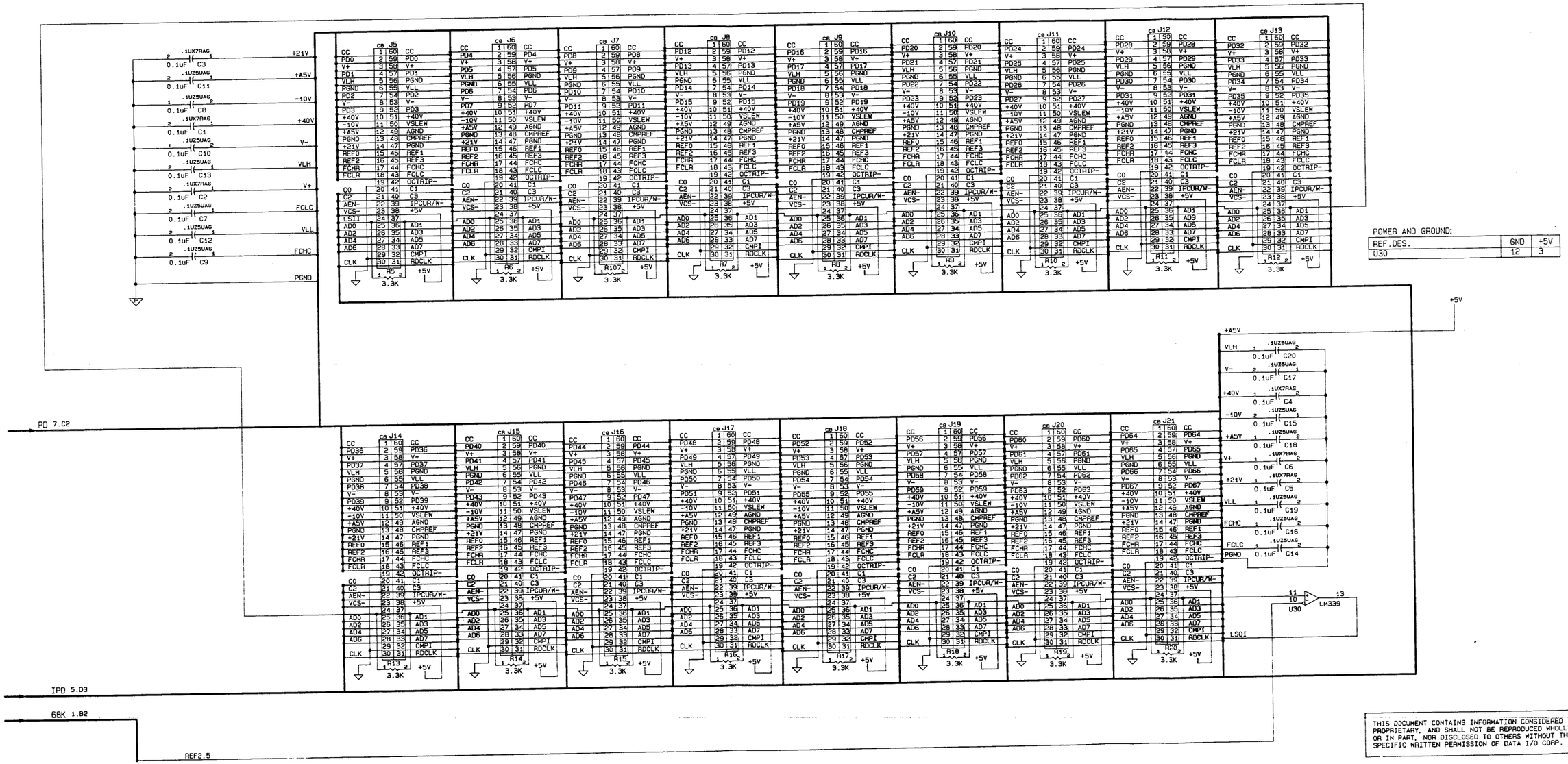
DATA I/O REDMOND, WASH.

TITLE
SCHEMATIC DRAWING,
UNISITE
CONTROLLER BD.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-2012

SCALE NONE SHEET 7 OF 8

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	SEE SHEET ONE	JK	BW 32786	RC.	4-1-6



POWER AND GROUND:

REF.DES.	GND	+5V
U30	12	3

DRAWN	Vince Workel	DATE 3/24/86
CHECKED	Barry V.	3/27/86
ELEC. ENG.	Kathy Crawford	3/24/86
MECH ENG		
MFG ENG		
QUAL ASSUR		
APPD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED:
.XX ±
.XXX ±
ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

TITLE: SCHEMATIC DRAWING, UNISITE CONTROLLER BD.

SIZE	FSCM NO	DRAWING NO.
D	54193	30-701-2012

SCALE NONE SHEET 8 OF 8

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	WL	BZ 8-3-86	RE 4-17-86	9/1/86

NOTE: These resistor pull-ups shall force all ones if a location is read that does not have a ram board installed. These pull-ups also insure no parity error will occur if no ram board is installed. (assume [6(20pf)+50pf] x 1.8K => 310ns to 3.1V)

NOTICE: The drams must have IOL > 4.2 ma
(5/1764) + LS245 (200ua) + LS74 (200ua) + F280 (600ua)
IOL > 2.85 ma + 1.00ma => 3.85 mA

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTERS ARE IN OHMS, 1/8 W, 2%
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. LAST REFERENCE DESIGNATOR USED: U40, J1, C45, R19, TP1
4. REFERENCE DESIGNATOR NOT USED: C33, U5, R12, R13
5. POWER AND GROUND:

REF.DES.	GND	+5V
U6, 7, 8, 9, 15, 19	7	14
U24, 28		
U16, 17, 25, 27, 38	8	16
U39, 40		
U18, 37	10	20

6. UNUSED GATES:

Note: Servicing Rev A PWB's 410-2114-001A
This schematic shows several unused gates above, these gates are also not used on the the Rev A PWB. The connections of unused gates is slightly different on the Rev A PWB.

Note: Parity enable/disable
At reset, the parity detect is disabled
Write a 1 to location $60001 to enable
Write a 0 to location $60001 to disable

Note: To establish the amount of ram in the system, a simple test write followed by a read for the following two words of data should be used: $5A5A, $A5A5

Note: At power on, all locations with parity must be written to with any data pattern to initialize the parity bits. The best method would be to write a random number followed by a read for a simple fast test.

Note: To test the parity bit a regular ram test shall be used which writes and reads both an even and odd number of ones to both the upper and lower bytes of memory.
If a parity error occurs, no Dtack is sent for that location, and the controller will provide a bus error in 3 usec. The bus error handler routine can determine if a parity error occured by looking at the error address and comparing to valid memory

Note: Any 68000 emulator which is used with this board must support continuous Address Strobe, otherwise the DRAM will NOT be refreshed.

REFRESH ALTERNATOR
1 => REFRESH RAS0, RAS1, RAS3, RAS4
0 => REFRESH RAS2, RAS5, RAS6

THE REFRESH ALTERNATOR CUTS MAXIMUM REFRESH CURRENT IN HALF

REFRESH EVERY 6.4 USEC

2 TO 3 WAIT STATES => 600 OR 700NS RAM CYC

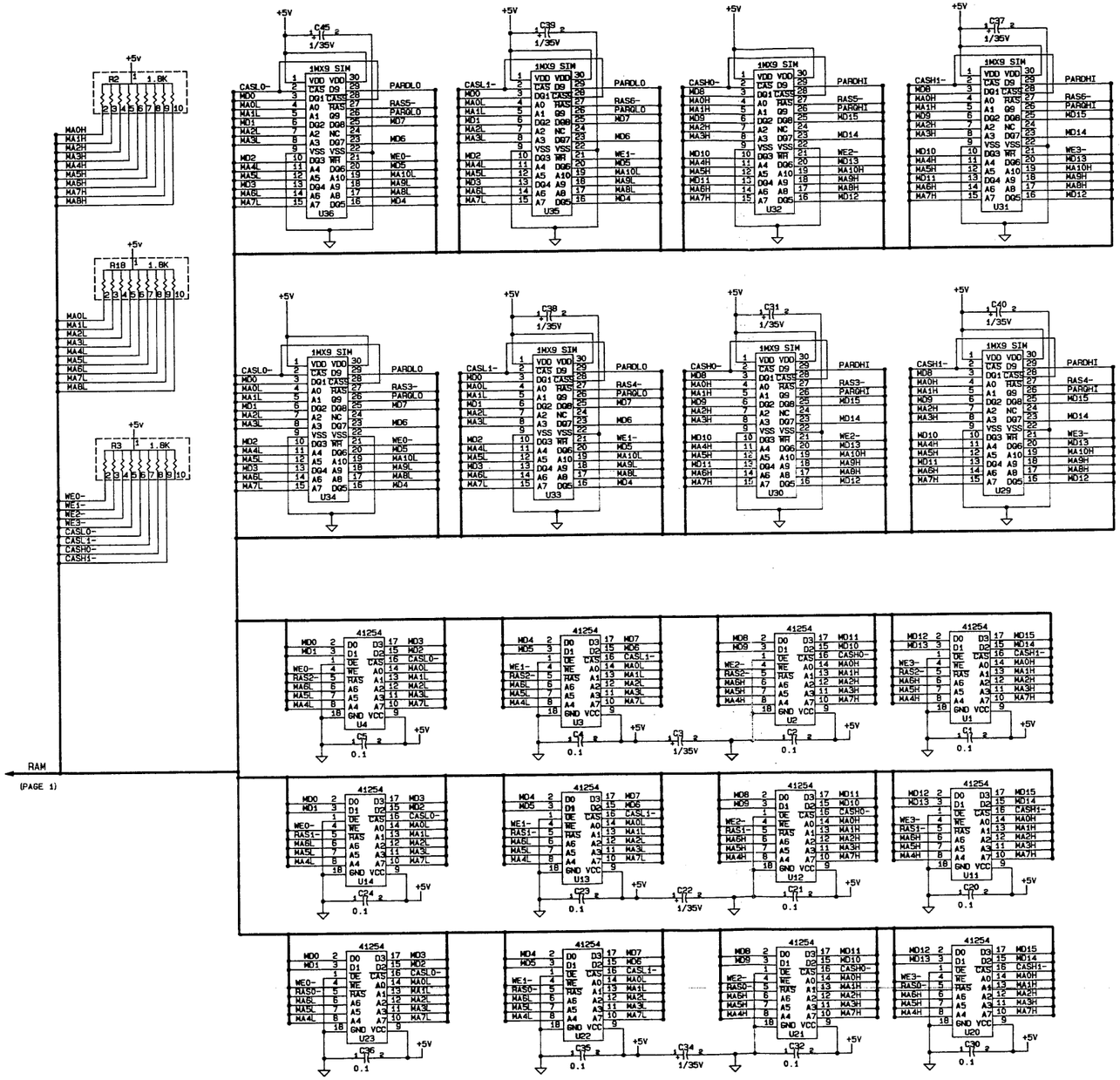
ADDRESS MULTIPLEXER

For App Micro Sys 68000 emulator

P/N 701-2114-001

DRAWN	DATE 7/31/86	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED Nancy Overman		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, UNISITE EXPANSION RAM BD.
ELEC ENG	9-17-86	DO NOT SCALE DRAWING	SIZE D · FSCM NO. 54193 · DRAWING NO. 30-701-2114
MECH ENG	9/9/86		SCALE — · D.A.D. · SHEET 1 OF 2
MFG ENG CR Jensen	9/17/86		
QUAL ASSUR	9/17/86		
	9-17-86		

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	SEE SHEET ONE	MJL	BS/RB	[illegible] 4-17-86	8/19/86



DRAWN K. Hall	DATE 8/19/86	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED B. Valduria	8/19/86	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, UNISITE EXPANSION RAM BD.
ELEC ENG			
MECH ENG		DO NOT SCALE DRAWING	
MFG ENG			SIZE D · FSCM NO. 54193 · DRAWING NO. 30-701-2114
QUAL ASSUR			SCALE — · D.A.D. · SHEET 2 OF 2
APPD			

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP	BV 5-20-86	[illegible]	3/86
B	INC ADCN A1 ECP 0262	MP	BV 5-20-86	[illegible]	8-86
C	INC ADCN B1 ECP 0006	MP	BV 1-87	[illegible]	1-87

PINDRIVER BUS

RELAY BUS

"ACTIVE" DS1 R1 330 "READY" DS2 R2 330

RELAY ENABLE DELAY CIRCUIT

CASE GND

XU1

NOTES: UNLESS OTHERWISE SPECIFIED:

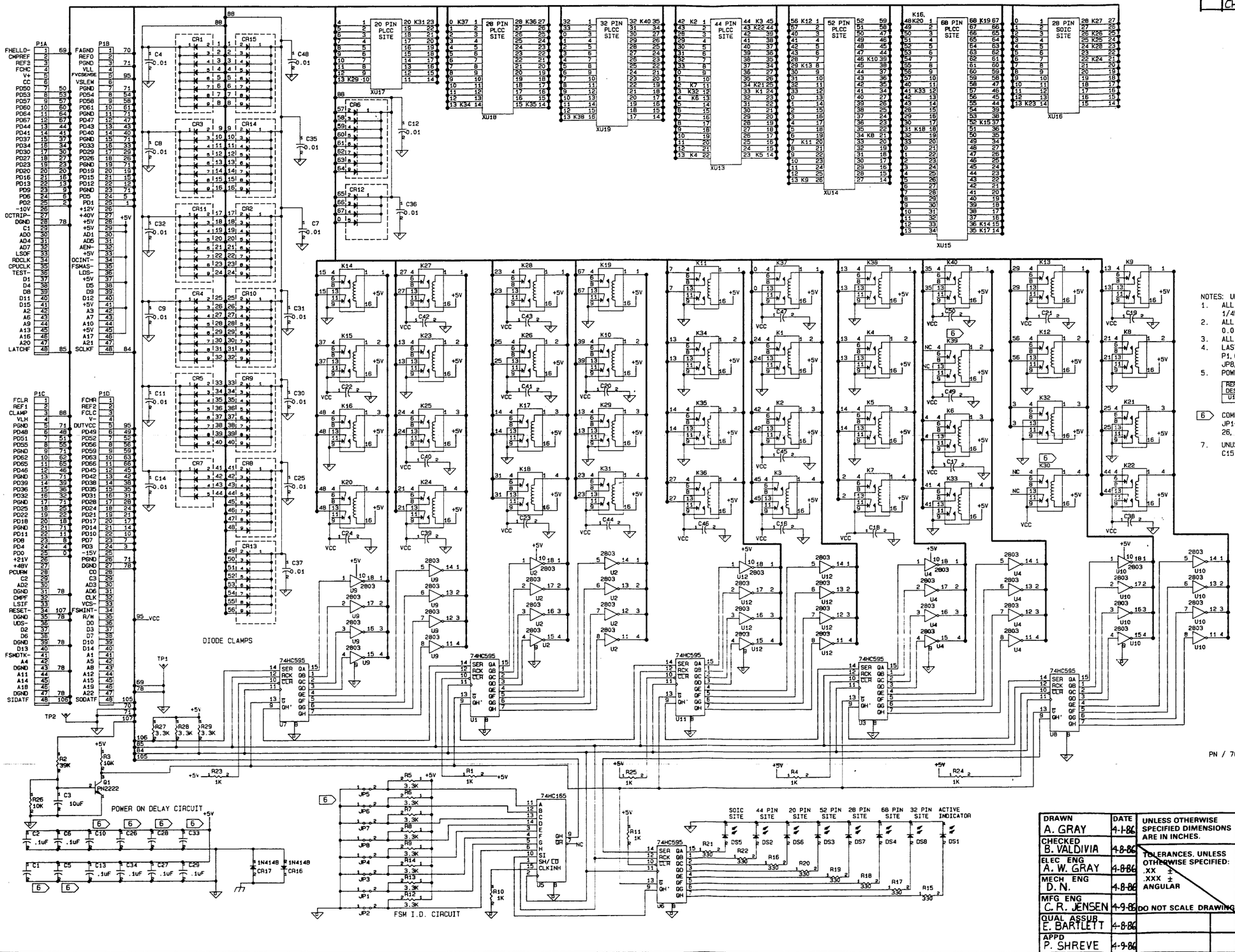
1. ALL DIODES ARE 1N4148.
2. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
3. ALL CAPACITORS ARE IN MICROFARADS, 50V.
4. LAST REFERENCE DESIGNATORS USED: J1, CR8, C19, U10, R7, K30, JP5, DS2, B40.
5. POWER AND GROUND:

REFERENCE DESIGNATOR	+5V	DGND
U2, U4, U7, U8, U10	16	8
U3, U5, U6, U6	10	9

701-2021-002

DRAWN MARK PATTEE	DATE 3/86	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED B. Valdivia	3/20/86	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM SITE 28/40/48
ELEC ENG [illegible]	3/[illegible]	DO NOT SCALE DRAWING	SIZE D; FSCM NO. 54193; DRAWING NO. 30-701-2021
MECH ENG [illegible]	3/20/86		SCALE NONE; D.A.D; SHEET 1 OF 1
MFG. ENG [illegible]	3/[illegible]		
QUAL ASSUR [illegible]	5/21/86		
APPD [illegible]	5/21/86		

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	REDRAWN WITHOUT CHANGE INC. ADCN A1,A2,A3,A4 PER ECP 0262 PG 30,106,114,130 CHANGED -001 TO -002	DJL	BV 11-20-86		11/20/86



NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 0.01/50V.
3. ALL DIODES ARE 1N4148.
4. LAST REFERENCE DESIGNATOR USED: P1, CR17, XU19, K40, C50, DS8, R29, Q1, JP8, TP2
5. POWER AND GROUND:

REFERENCE DESIGNATOR	+5V	GROUND
U1, 3, 5-8, 11	16	8

6. COMPONENTS OMITTED : JP1-4, JP6-8, K30, 39, C1, 5, 10, 26, 28, 33.
7. UNUSED REFERENCE DESIGNATOR: C15

PN / 701-2042-002

DRAWN A. GRAY	DATE 4-1-86	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED B. VALDIVIA	4-8-86	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, CHIPSITE FSM
ELEC ENG A. W. GRAY	4-8-86	DO NOT SCALE DRAWING	SIZE D; FSCM NO. 54193; DRAWING NO. 30-701-2042
MECH ENG D. N.	4-8-86		SCALE NONE; D. A. D.; SHEET 1 OF 1
MFG ENG C. R. JENSEN	4-9-86		
QUAL ASSUR E. BARTLETT	4-8-86		
APPD P. SHREVE	4-9-86		

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