PROM PROGRAMMER
Program Card Set
909/919-1174-1

025-1174-1 REV U SEPT 81

FOREWORD

The 909-1174-1 Program Card Set cannot be used with the Data I/O Programmer Satellite.

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SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

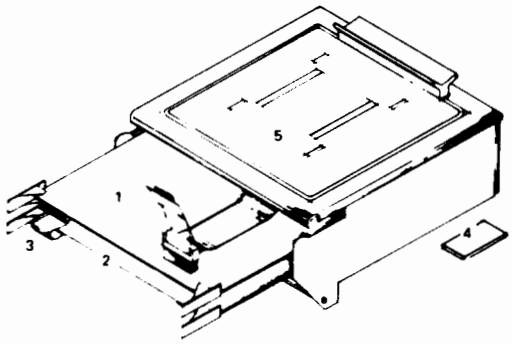
Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

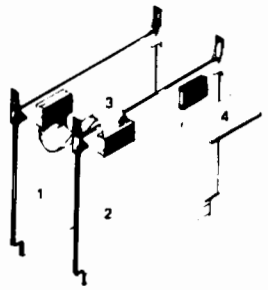
Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
ADVANCED MICRO DEVICES				
1024x8 MOS	2708	VOL TS	24 PIN	1033-4
ELECTRONIC ARRAYS				
1024x8 MOS	2708	VOL TS	24 PIN	1033-4
FAIRCHILD				
1024x8 MOS	2708	VOL TS	24 PIN	1033-4
FUJITSU				
1024x8 MOS	8518 (2708)	VOL TS	24 PIN	1033-4
INTEL				
512x8 MOS	2704/8704	VOL TS	24 PIN	1033-2
1024x8 MOS	2708/8708	VOL TS	24 PIN	1033-4
INTERSIL				
1024x8 MOS	2708	VOL TS	24 PIN	1033-4
MITSUBISHI				
1024x8 MOS	58732S(2708)	VOL TS	24 PIN	1033-4
1024x8 MOS	2708	VOL TS	24 PIN	1033-4
MOTOROLA				
1024x8 MOS	68708/2708	VOL TS	24 PIN	1033-4
1024x8 MOS	2708P	VOL TS	24 PIN	1033-4
2048x8 MOS	2716	VOL TS	24 PIN	1398
NATIONAL SEMICONDUCTOR				
1024x8 MOS	2708	VOL TS	24 PIN	1033-4
SIGNETICS				
1024x8 MOS	2708	VOL TS	24 PIN	1033-4
TEXAS INSTRUMENTS				
1024x8 MOS	2708/27L08	VOL TS	24 PIN	1033-4
2048x8 MOS	2716	VOL TS	24 PIN	1398
TOSHIBA				
512x8 MOS	321	VOL TS	24 PIN	1033-2
1024x8 MOS	322	VOL TS	24 PIN	1033-4

The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences and shapes of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909-part number. See Figure 1-1 b).



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1-9 Programmers

1. DIGITAL CARD	701-1196
2. ANALOG CARD	701-1174-1
3. INTERCONNECT CABLE	709-1608
4. CALIB. PROGRAM ADAPTER	910-1174-1
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

1.2 CALIBRATOR PROGRAM ADAPTER

The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.

1.3 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable-jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

Table 2-1. Customer-Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP2	Word Limit	2048	Selection defaults to socket adapter

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 and 2 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

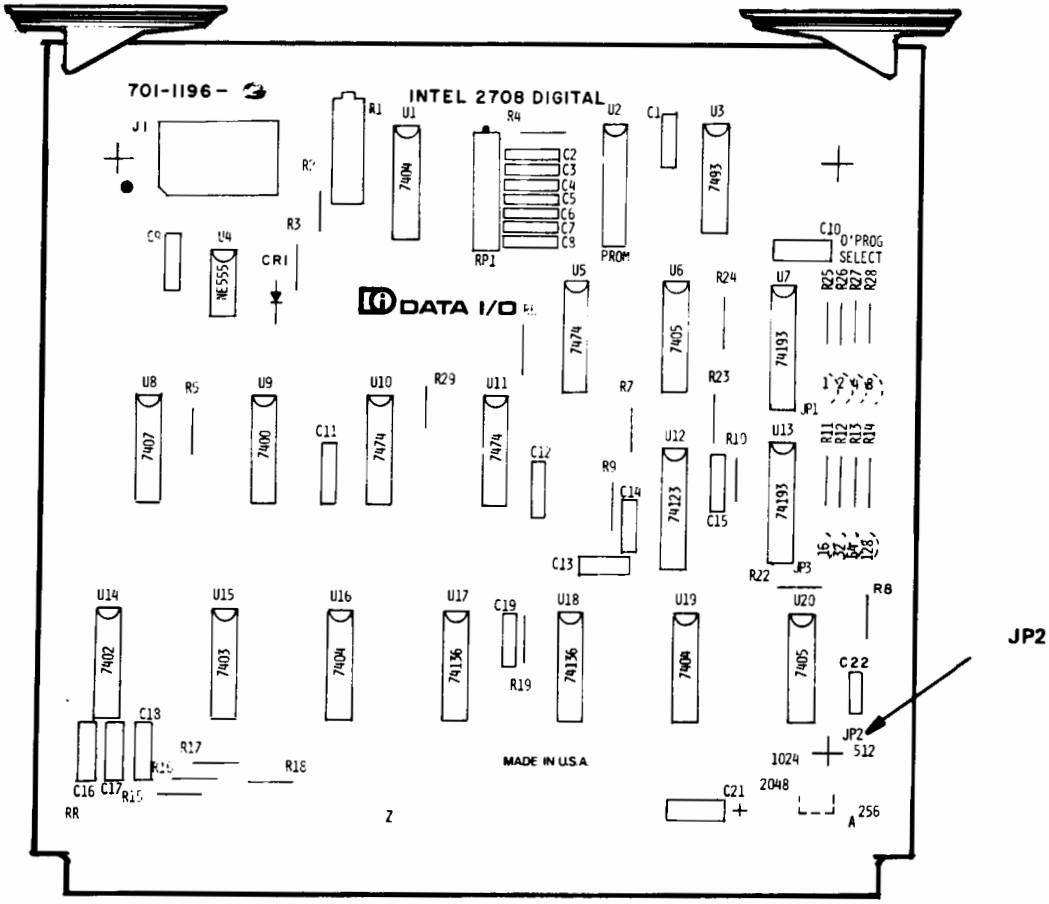


Figure 2-1. Digital Card Jumper Locations

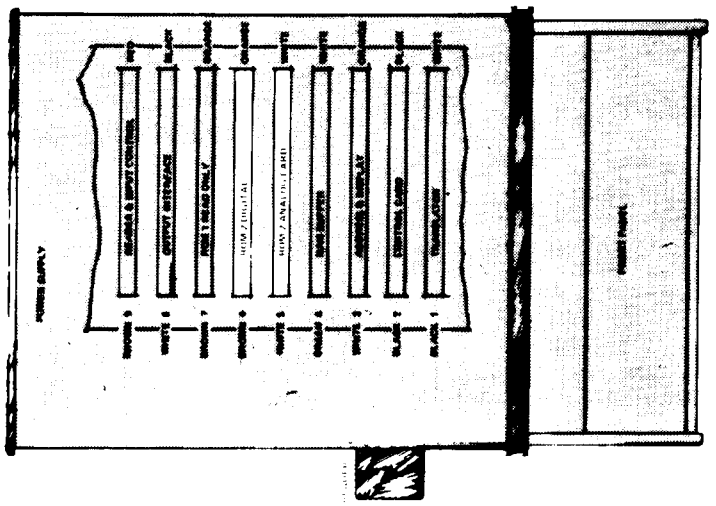


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

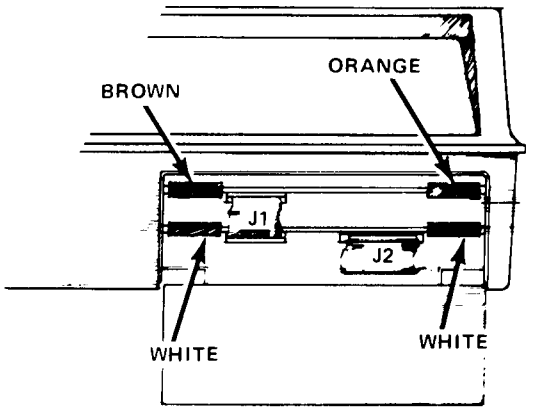


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

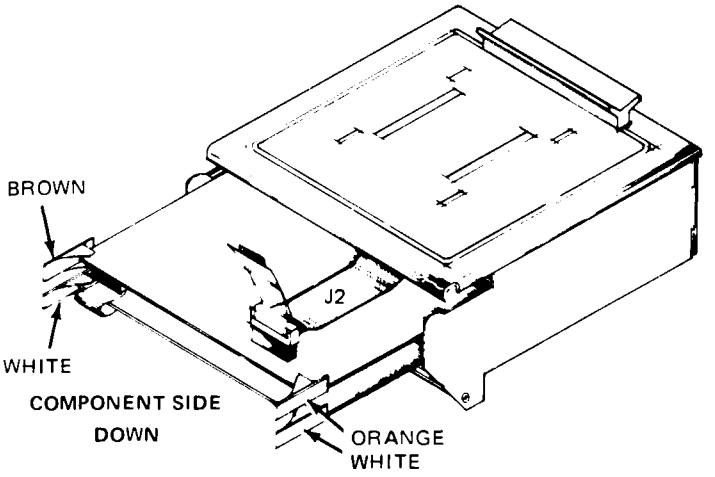


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

3.1 INTRODUCTION

The 1174-1 cardset can only be operated in an *automatic* program sequence, because of special recycle requirements of the 3-voltage MOS parts. A special operating procedure is required when programming with Models 1, 2, 3, and 5. NO SPECIAL PROCEDURE IS REQUIRED FOR MODELS 7 and 9 or Systems 17 and 19. Refer to the programmer instruction manual for complete operation information.

3.2 MODELS 1-5

Programmer Models 1, 2, 3, and 5 are operated in the usual fashion, except when actually programming the device. Programming in the MANUAL mode is not allowed. To program the device AUTO must be selected. The input source, when programming the device, is RAM. (ROM 1 is a valid input if a READ ONLY card is present in the ROM 1 position.)

NOTE

The 909-1174-1 Program Card Set cannot be used in the Data I/O Programmer Satellite.

3.2.1 MODELS 3 AND 5

In a Model 3 or 5, when RAM-ROM 2, PROGRAM, and AUTO are selected and RESET is depressed, followed by START, the following sequence of events takes place:

1. Machine will perform a blank check from word Ø to Word Limit and back to Ø.
2. The PROG light will illuminate and the A and B lights will be extinguished. The Word Count will increment from Ø to Word Limit, jump back to Ø and increment to Word Limit, until the device is programmed. Programming requires approximately 100 zero to Word Limit cycles—up to 10 minutes.
3. When programming is complete, the A and B lights will illuminate and the PROG light will be illuminated for 1 cycle. The PROG light will then be extinguished as the machine cycles from Ø to Word Limit back to zero performing its usual Verify cycle. The machine will stop with STOP illuminated.
4. If the device does not program within the required number of cycles, the device will be rejected. This is evidenced by the machine halting with the A and B lights extinguished and the PROG and START lights illuminated.

3.2.2 MODELS 1 AND 2

In a Model 1 or 2 when RAM to ROM 2, PROGRAM and AUTO are selected and RESET is depressed, followed by START, the following sequence of events takes place:

1. The PROG light will illuminate and the A and B lights will be extinguished. The word count will increment from Ø to Word Limit, jump back to Ø and increment to Word Limit until the device is programmed. Programming requires approximately 100 zero to Word Limit cycles—up to 10 minutes.
2. When programming is complete, the A and B lights will illuminate for 1 cycle. The machine will then stop at Word Limit with STOP illuminated. A Verify should then be performed by the operator.
3. If the device does not program within the required number of cycles, the device will be rejected. This is evidenced by the machine halting with the A and B lights extinguished and the PROG and START lights illuminated.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

a. Data I/O Universal Calibrator, P/N 910-1071

b. Calibration Extender:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1521

c. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.

d. A potentiometer adjustment tool

e. Dual-trace oscilloscope — Tektronix 465 or equivalent

f. A jumper wire approximately 12 inches in length

g. Data I/O interconnection cables:

Models 1-5	P/N 709-1613
Model 9	P/N 709-2608, 709-1613
System 19	P/N 709-2612, 709-1613

h. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1-5

Refer to Figure 4-1.

a. Make sure the programmer power is OFF.

b. Remove the cover from the programmer and remove the Program Card Set from the card cage.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

d. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power **ON**. Prepare the programmer for calibration using the following key sequence:

RESET
ROM2 — ROM2
MANUAL
PROGRAM
START

Figure 4-1. Set-up of Models 1-5 for DC Calibration.

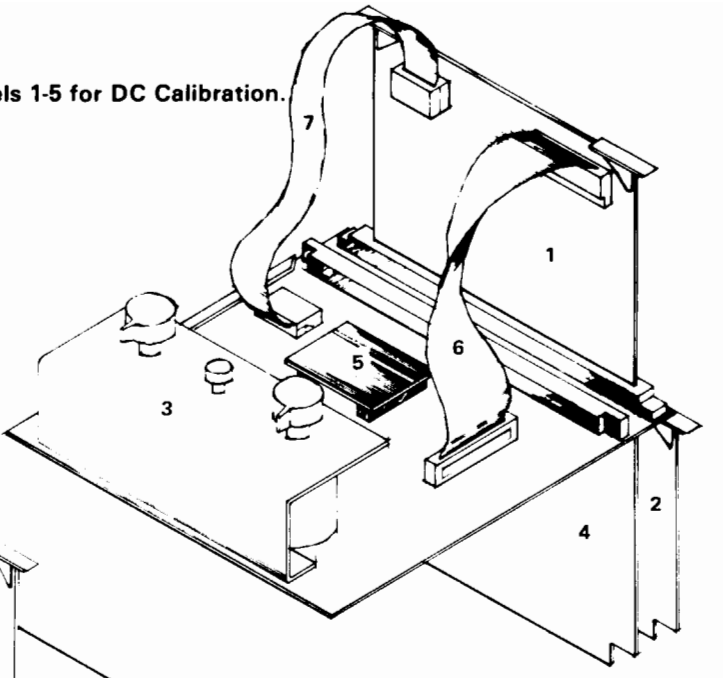
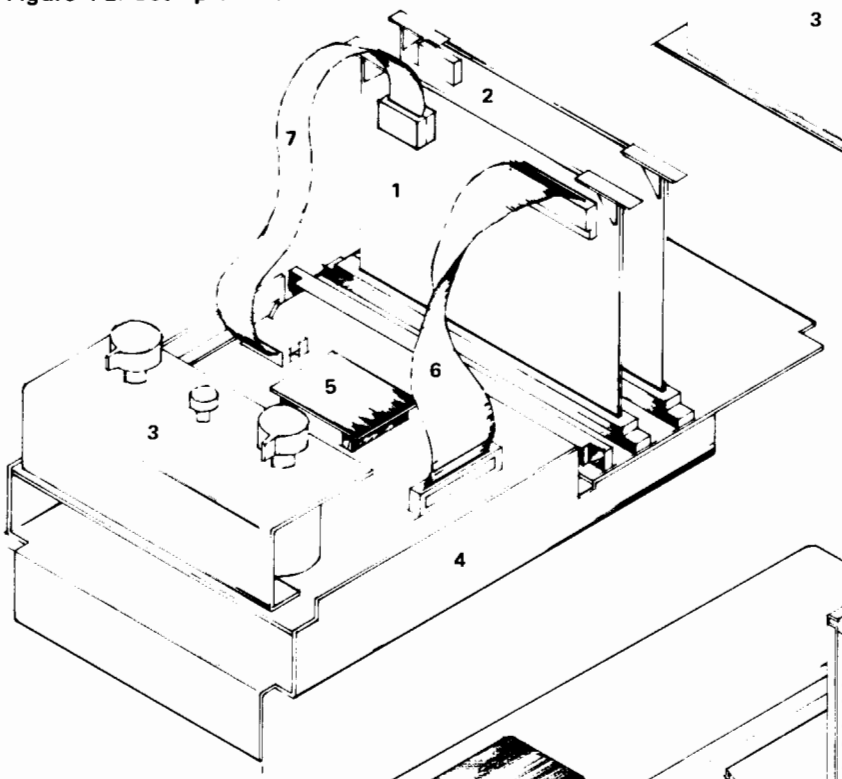
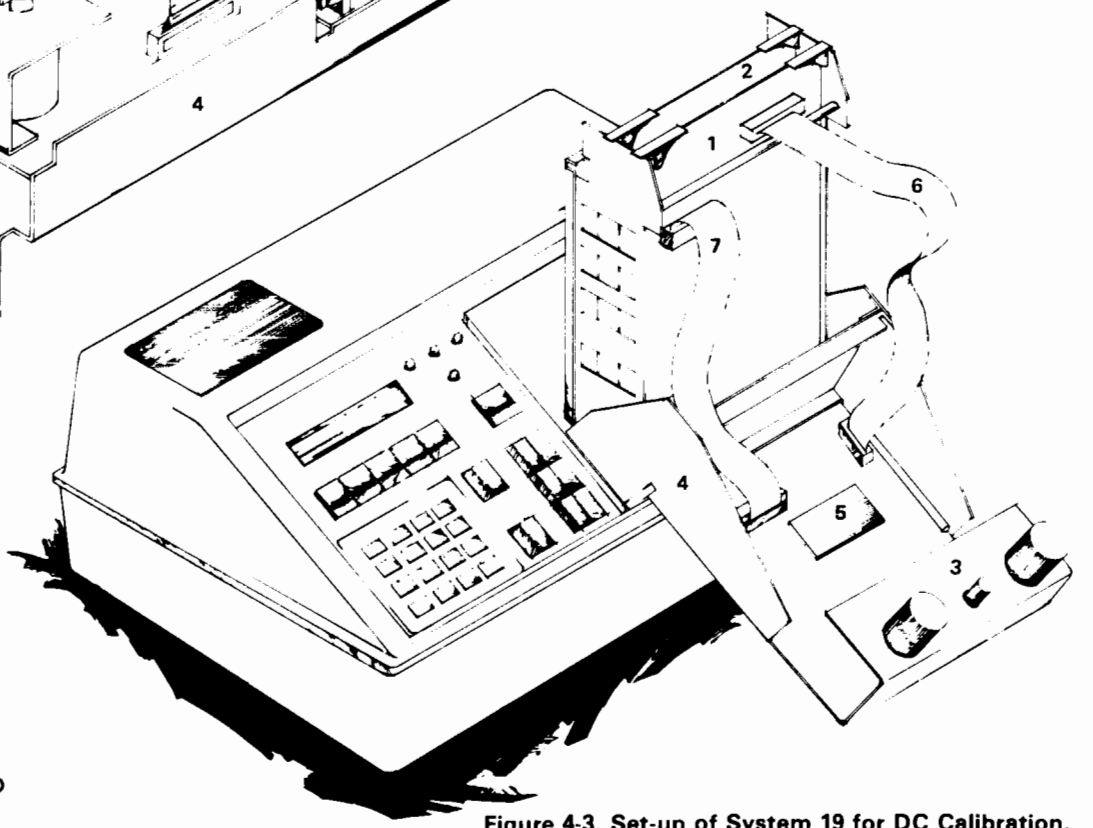


Figure 4-2. Set-up of Model 9 for DC Calibration.





1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATION EXTENDER
5. CALIBRATOR PROGRAM ADAPTER
6. 26-CONDUCTOR CABLE
7. 16-CONDUCTOR CABLE

Figure 4-3. Set-up of System 19 for DC Calibration.

4.2.2 MODEL 9

Refer to Figure 4-2.

a. Make sure the programmer power is OFF.

b. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

d. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's digital card position (brown/orange). Be sure that the edge of the Extender Card is securely seated. Install the Digital and Analog cards into the 1074 calibration extender according to Figure 4-2.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

KEYBOARD
EXECUTE
NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

a. Make sure the programmer power is OFF.

b. Remove the Programming Pak from the programmer.

c. Insert the Calibration Extender, P/N 910-1521, in the same way as the Programming Pak, being sure to seat it properly in the programmer's mating connector.

d. With the handle of the Programming Pak down, connect the 64-pin connectors of the Programming Pak and Calibration Extender. Be sure the connectors mate securely.

e. Slide the Universal Calibrator securely into the card slots at the front of the Calibration Extender.

f. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe with the connector dot.

g. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe with the connector dot.

h. Plug the Calibrator Program Adapter into the Program Adapter slot on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number of the Calibrator Program Adapter corresponds to the 919-XXXX part number of the Programming Pak.

i. Connect the DVM ground lead to GND test point on the Universal Calibrator.

j. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

SELECT
C1 (calibrate ON)
START

k. Press:

KEYBD
ENTER

The TEST light comes ON and remains ON throughout calibration.

NOTE
To exit calibration, press:
SELECT
C0 (calibrate OFF)
START
(Test light goes OFF.)

l. Press START.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

- The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

- The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

- The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

- The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the Calibration Chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

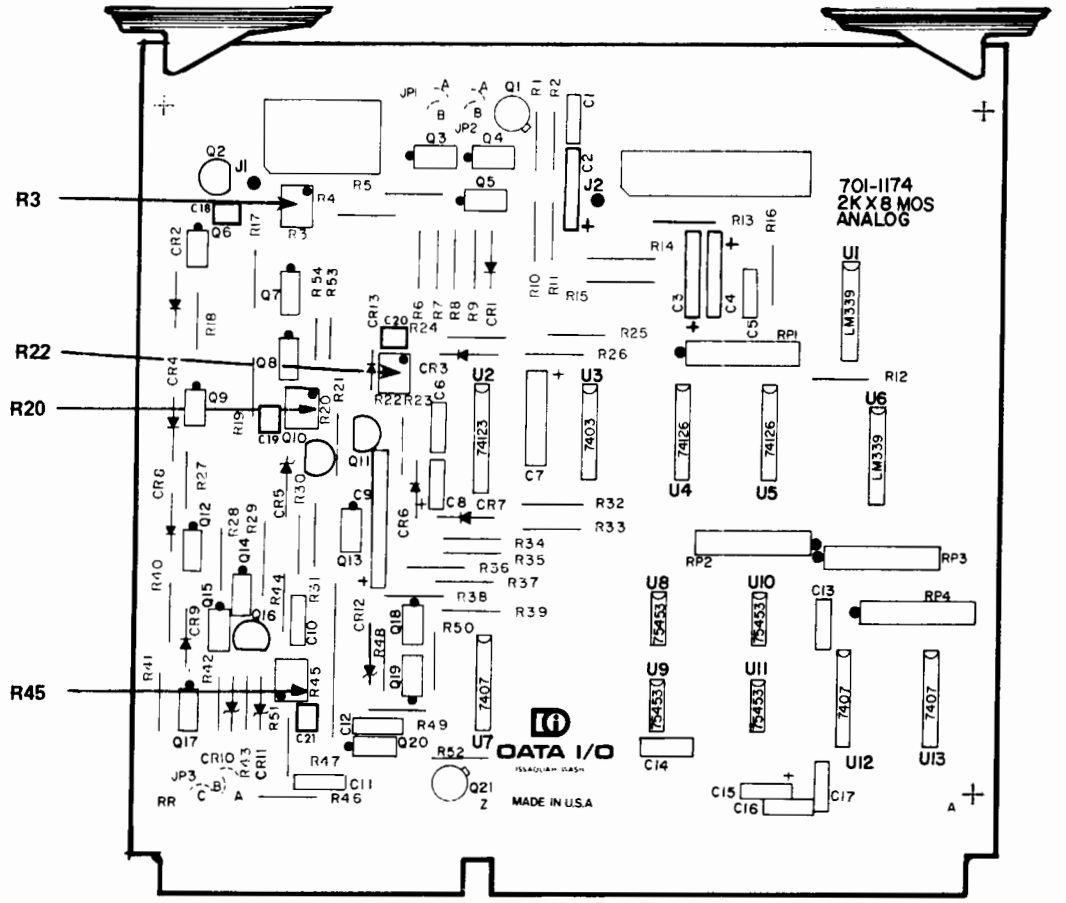


Figure 4-4. Analog Card Adjustment Locations

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1174-1 | PROGRAM CARD 909-1174-1
FIXTURE 702-1071 | MANUFACTURER
PAGE 1 OF 3 | PROGRAM ADAPTER 910-1174-1 | PROM 2716/8716, 2708/8708, 2704/8704

10/81 U ECN #4223 | 6-80 U ECN #3708 EF

DATE	REV	REVISION RECORD	DR	CK
10-20-78	T	CN #1905	GJ	GJ
11-78	-	CN #2565	FS	
12-1-78	U	CN #2613	KL	
4-79		ECN #2565	FS	
3-5-80	U	ECN #3475	EF	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
44	02	+24	1-1	000	00	000			-24		23.5	24.0	24.5
44	02	POWER +48	1-2	000	00	000			-48	R24	49.4	49.7	49.8
44	02	SUPPLIES +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15
44	02	-9	1-4	000	00	000			-9	R40	-9.2	-9.0	-8.8
44	00	PROGRAMMABLE SUPPLY	1-5	001	01	001			PROG V		14.0		18.0
44	00	VCC PROGRAM V SET	2-1	001	01	001	5	1	P3	R3	4.75	5.0	5.25
44	00	VCC KILL/ICC RESET	2-2	001	01	001	6	1	P3		0.0		0.4
44	00	VDD PROGRAM V SET	2-3	001	01	001	5	6	P3	R20	11.4	12.0	12.6
44	00	VDD KILL/IDD RESET	2-4	001	01	001	6	6	P3		0.0		0.4
44	00	VBB PROGRAM	2-5	001	01	001	5	4	P3	R22	-5.25	-5.0	-4.75
44	00	VBB KILL, IBB RESET	2-6	001	01	001	6	4	P3		-0.4		0.0
44	00	PROGRAM LINE, PROG (VPP) (3)	3-1	002	02	002	7	7	P3	R45	26.6	26.8	27.0
44	00	PROG LINE LOAD TEST	3-2	002	02	002	3	7	P3		25.6		26.2
44	00	PROG LINE KILL, IBB RESET	3-3	002	02	002	5	7	P3				
44	02	PROG LINE, VERIFY	3-4	003	03	003	7	7	P3		0.0		0.4
44	04	CE PROGRAM (1)	3-5	004	04	004	7	5	P3		11.4		12.6
44	01	CE VERIFY	3-6	005	05	005	7	5	P3		0.0		0.4
44	01	REFERENCE LEVEL	4-1	005	05	005	7	5	U P8		1.6		2.0
C4	05	BIT 8 PROGRAM	5-1	006	06	006	7	8	P3		0.0		0.4
C4	05	BIT 7 NO PROGRAM	5-2	006	06	006	7	9	P3		4.75		5.25
C4	05	BIT 6 PROGRAM	5-3	006	06	006	7	10	P3		0.0		0.4
C4	05	BIT 5 NO PROGRAM	5-4	006	06	006	7	11	P3		4.75		5.25
C4	05	BIT 4 PROGRAM	5-5	006	06	006	7	12	P3		0.0		0.4
C4	05	BIT 3 NO PROGRAM	5-6	006	06	006	7	23	P3		4.75		5.25
C4	05	BIT 2 PROGRAM	5-7	006	06	006	7	22	P3		0.0		0.4
C4	05	BIT 1 NO PROGRAM	5-8	006	06	006	7	21	P3		4.75		5.25
C4	05	BIT 8 NO PROGRAM	5-9	006	06	006	7	8	P3		4.75		5.25
C4	05	BIT 7 PROGRAM	5-10	006	06	006	7	9	P3		0.0		0.4
C4	05	BIT 6 NO PROGRAM	5-11	006	06	006	7	10	P3		4.75		5.25

COMMENTS

NOTES are on pages 2 and 3.
Switch S1 must be depressed for accurate readings.
CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

Use paragraphs 4.3.1 - 4.3.5 for key sequences for COMMENTS below.
Adjustments are located on the power supply board.
See programmer manual.

Adjustment Step.
Confirm programmer in STOP.
Adjustment Step. Set programmer in START.
Confirm programmer in STOP.
Adjustment Step. Set programmer in START.
Confirm programmer in STOP. See NOTE 1.
Adjustment Step. Set programmer in START.

Confirm programmer in STOP. See Note 3.
Set programmer in START.

	MODEL 5	9	19	
Test point located on analog card.				
LOAD	BITS 2,4,6,8,ON	AA	55	DI BUS
Confirm	BITS 2,4,6,8,ON	55	55	DO BUS
LOAD	BITS 1,3,5,7,ON	55	AA	DI BUS
CONFIRM	BITS 1,3,5,7,ON	AA	AA	DO BUS

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
C4	05	BIT 5 PROGRAM	5-12	006	06	006	7	11	TP3		0.0		0.4
C4	05	BIT 4 NO PROGRAM	5-13	006	06	006	7	12	TP3		4.75		5.25
C4	05	BIT 3 PROGRAM	5-14	006	06	006	7	23	TP3		0.0		0.4
C4	05	BIT 2 NO PROGRAM	5-15	006	06	006	7	22	TP3		4.75		5.25
C4	05	BIT 1 PROGRAM (2)	5-16	006	06	006	7	21	TP3		0.0		0.4
C4	00	DATA DISABLE	6-1	007	07	007	7	8	TP3		4.75		5.25
C4	00		Model 9 users see NOTE 4 to perform step 6-1.										
C4	00	BACKWARDS DEVICE TEST	6-2	007	07	007	6	21					
44	00	ADDRESS TEST VIL (4)	7-1	682	2AA	1252	7	20	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-2	682	2AA	1252	7	19	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-3	682	2AA	1252	7	18	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-4	682	2AA	1252	7	17	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-5	682	2AA	1252	7	16	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-6	682	2AA	1252	7	15	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-7	682	2AA	1252	7	14	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-8	682	2AA	1252	7	13	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-9	682	2AA	1252	7	2	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-10	682	2AA	1252	7	3	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-11	682	2AA	1252			U7 P10		0.0		0.4
44	00	ADDRESS TEST VIH	7-12	1365	555	2525	7	20	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-13	1365	555	2525	7	19	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-14	1365	555	2525	7	18	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-15	1365	555	2525	7	17	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-16	1365	555	2525	7	16	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-17	1365	555	2525	7	15	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-18	1365	555	2525	7	14	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-19	1365	555	2525	7	13	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-20	1365	555	2525	7	2	TP3		4.75		5.25
44	00	ADDRESS TEST VIL	7-21	1365	555	2525	7	3	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-22	1365	555	2525			U7 P10		4.75		5.25
44	00	VSS TEST	8-1	1365	555	2525	8	24	TP3		0.0		0.08
04	00	← DATA PATTERN FOR WORDS NOT SHOWN											

CALIBRATION CHART 017-1174-1

	MODEL 5	9	19	
LOAD	BITS 1,3,5,7,ON	55	AA	DI BUS
Confirm	BITS 1,3,5,7,ON	AA	AA	DO BUS
LOAD	ALL BITS ON	00	00	DI BUS
Confirm	ALL BITS OFF	FF	FF	DO BUS

See NOTE 2.

Set programmer in START.

Test point located on analog card. See NOTE 3.

Perform these tests with word limit jumper JP2 on digital card set to 2K.

Test point located on analog card. See NOTE 3.

NOTES:

1. For 909-1174-1 REV. "H" or earlier card sets, the programmer will not STOP. To obtain measurement set the programmer in STOP.
2. Set programmer in STOP. Press S1 on calibrator and hold to simulate backwards device while attempting to set programmer in START. Programmer must remain in STOP.
3. Omit this Step for 909-1174-1 REV. "H" or earlier card sets.

(continued Next Page)

NOTES:

4. For Model 9 users with Revision A Software;
   (see paragraph 4.3 to determine the correct revision letter):
   To perform this test, set the NORMAL/INVERT switch in NORMAL
   a. Press: LOAD, EXECUTE, KEYBOARD.
   b. Key in hex data in parentheses on the calibration chart.
   c. Press: PROGRAM, EXECUTE. The programmer will reamain in Program for up to 18 minutes. When the "P" indicator flashes, continue to step d.
   d. Press: STOP, KEYBOARD, EXECUTE.
   e. Advance to the word count specified on the calibration chart. Press the PROM key to observe the DO-bus data called out on the chart.

- The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

- The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

- The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4.3.1 – 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 – 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5:	Observe the START and STOP indicators.
Model 9:	Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.
System 19:	Observe the START light. If the START light is on, the programmer is in START.

4.3.2 SET THE STATE OF THE START/STOP LINE

Models 1, 2, 3 and 5:	Press the START/STOP key.
Model 9:	a. Press KEYBOARD to stop.
	b. Press EXECUTE to start.
System 19:	a. To set the programmer in START, press KEYBD, ENTER and START.
	b. To set programmer in STOP, press KEYBD.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5:	Press the FWD key or the REV key.
Model 9:	See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.
Revision "A" Software:	Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify:
	a. Ground J1-16 on the analog card.
	b. Press LOAD.
	c. Press EXECUTE.
	d. Press KEYBOARD.
	e. Key in data – Ø hex – at address ØØ1.
	f. Press VERIFY.
	g. Press EXECUTE. The programmer will mis-verify

at the address containing data and will STOP in FWD.

h. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD. Press ENTER and then REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the Calibration Chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: (See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.)

Revision "A" Software: Halt the programmer in the automatic program mode with data on the DI bus.

a. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.

b. Press the KEYBOARD key, and key in the Model 9 hex data called out on the Calibration Chart.

c. Press the PROGRAM key.

d. Ground J1-16 on the analog card.

e. Press EXECUTE and wait for the programmer to abort.

f. Press STOP, KEYBOARD and EXECUTE.

g. Disconnect J1-16 from ground.

h. SET the address specified on the Calibration Chart in order to make the measurement.

Revision "B" or later Software: With the KEYBOARD indicator illuminated and all the others OFF, use the hex keypad to key in the Model 9 hex data called out on the Calibration Chart.

System 19:

a. Press KEYBD, key in the address and press ENTER.

b. Key the System 19 hex data into RAM at the specified address.

c. Press ENTER and then REVIEW.

4.3.5 CONFIRM DATA ON THE DO BUS

Models 1, 2, 3 and 5: Compare the bit callout on the Calibration Chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF.

Model 9: With the EXECUTE light ON, press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the Calibration Chart.

System 19: With KEYBD selected, press the DEVICE DATA key. Hold it down while reading the hex data. The programmer must be in START.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the Timing Diagram, have the same reference on the Calibration Chart. Waveforms are selected using Universal Calibrator switches S2 and S3 as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

a. Make sure that the programmer power is OFF.

b. Remove the digital card from the card slot.

c. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

d. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.

e. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the Timing Diagram. Connect an input probe to TP3 on the calibrator.

f. Reinstall the digital card in the slot from which it was removed.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1—5, press:	RESET RAM-RAM PROGRAM MANUAL START
Model 9:	Set the NORMAL/INVERT switch in NORMAL if the Program Card Set is calibrated VOH or in the INVERT position if VOL. The NOTES column on the Timing Diagram specifies the correct polarity. Press: KEYBOARD.
System 19 press:	KEYBD Ø ENTER

3. Key in data for bit 1 at several addresses:

Models 1—5:	Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.
Model 9:	Enter hex data "Ø1" at several addresses.
System 19:	Enter hex data "Ø1" at several addresses. Check the NOTES column on the Timing Diagram to determine the correct data polarity. If the Timing Diagram indicates VOL, enter a hex "E" for 4-bit card sets; "FE" for 8-bit card sets. Return to address ØØØ.

4. Select the PROGRAM mode:

Models 1 — 5, press:	RESET PROGRAM AUTO RAM-ROM2
Model 9, press:	PROGRAM
System 19, press:	PROG

5. Initiate waveforms:

Models 1 — 5, press:	START
Model 9, press:	EXECUTE
System 19, press:	START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the Timing Diagram and Calibration Chart by the circled digits (1 , 2 , 3 , ...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

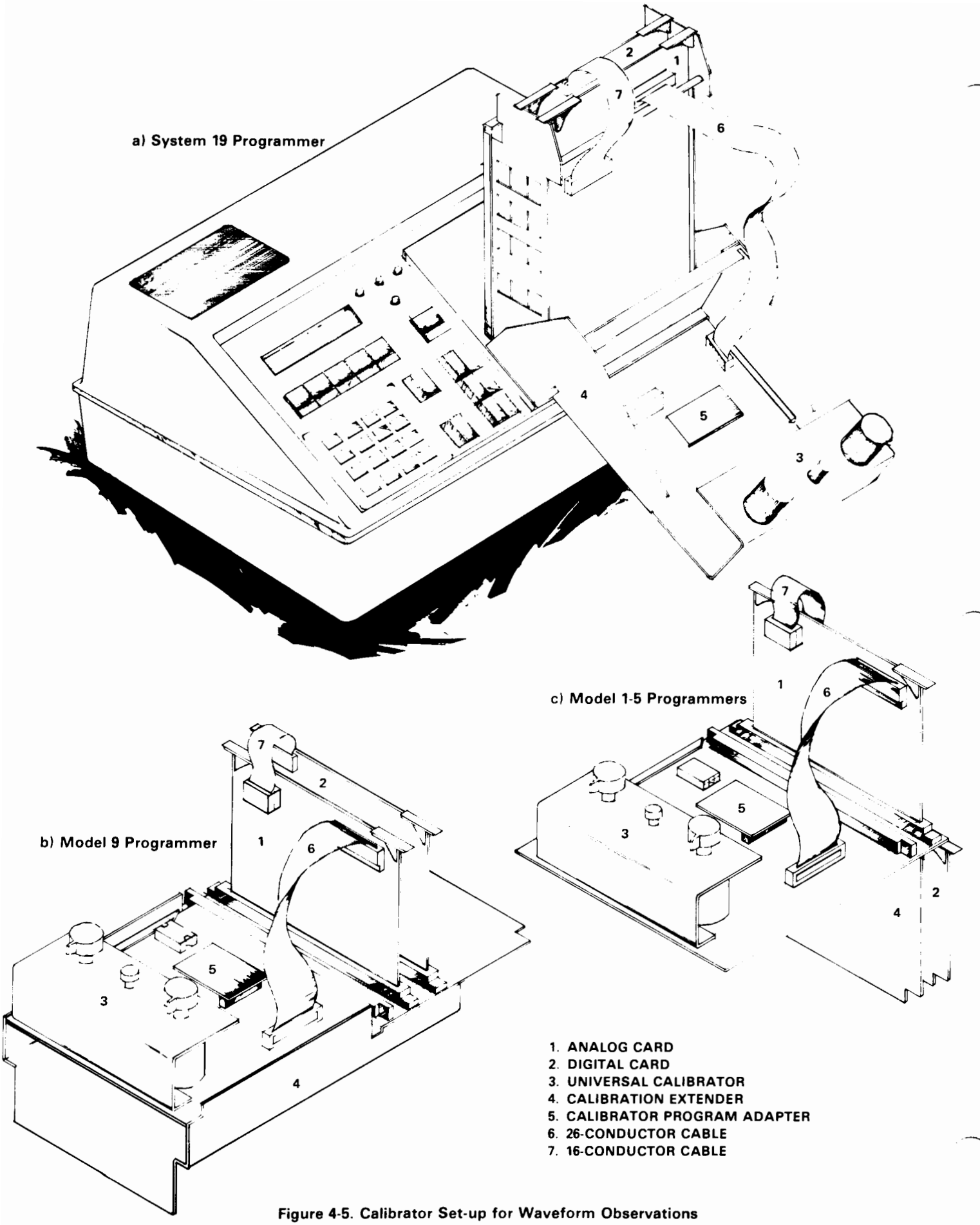
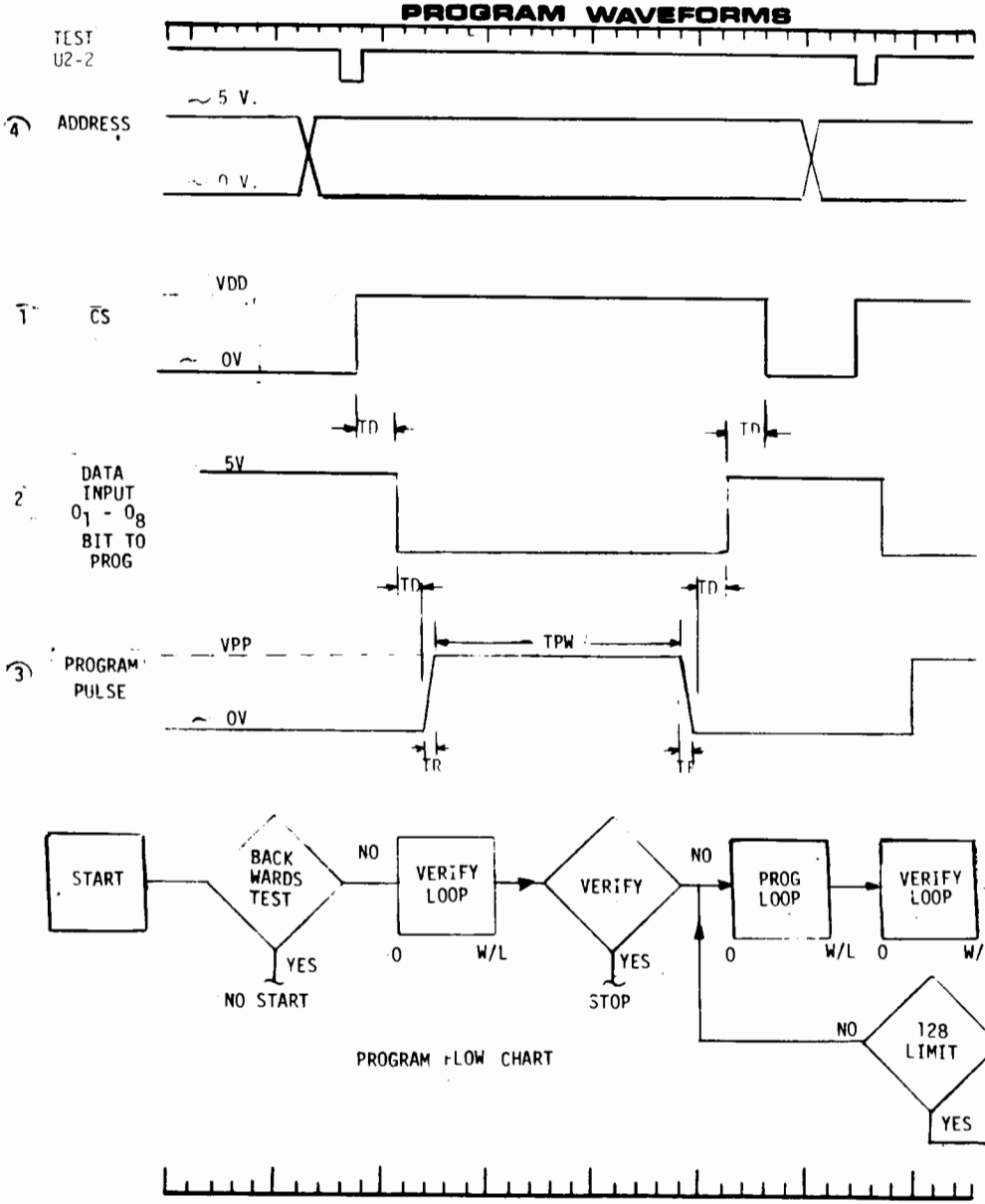


Figure 4-5. Calibrator Set-up for Waveform Observations

1/80	R	ECN #3430	EF				
3/80	R	ECN #3475	EF				

DATE	SYM	REVISION RECORD	DR.	CK
	D	ECN #1393		
6-24-77	R	ECN #1461	PW	GJ
11-78	-	ECN #2594	FS	

PROGRAM WAVEFORMS



NOTES

TIMING PROM

For Rev. "B" Analog Card Sets, or later. For Rev. "A" cards use same program except Bit 8 is inverted at all words shown.

1106 DIGITAL CARD JPRS

JP1,2,4,8 = Short
JP3,32,128 = Short & 16, 64 = Open
JP2 W/L = 2048
JPR Configuration gives 80 over program loops and 128 loops before reject.

Waveform Variables
VCC = 5.0 + 0.25V
VDD = 12.0 + 0.60V
VBB = 5.0 + 0.25V
VPP = 26.8 + 0.2V
TD > 10 us
TPW = 1 ms + 0
- 0.1 ms
TR - TF = 0.5 to 2.0 us

For calibration, the card set polarity defaults to VOL.

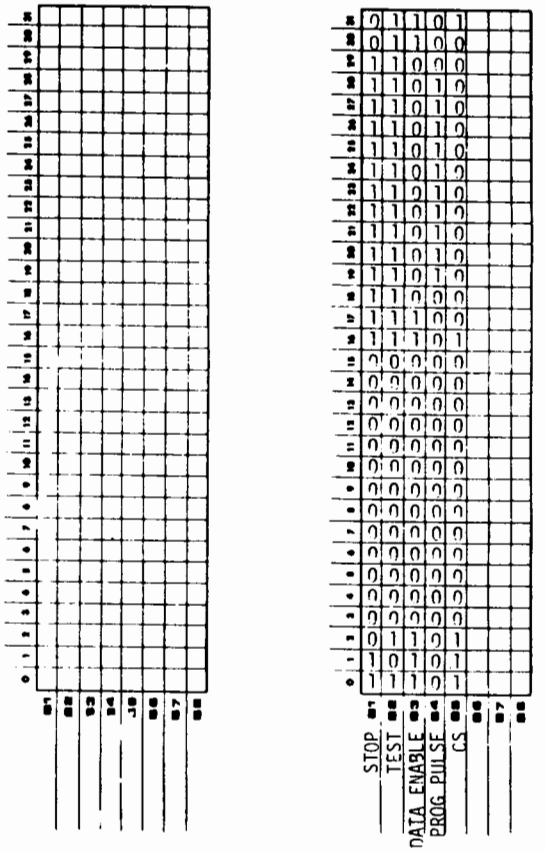
For 2716 Timing, refer to 031-1398 Socket Adapter Data.

PROGRAM FLOW CHART

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(0)

TIMING PROM



DATA I/O ISSAQUAH, WASH.

DRAWN BY PW & LC
APPROVED BY GJ

TITLE: 2708 TIMING DIAGRAM

DATE: 6-24-77

DRAWING NUMBER: 007-1174-1

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the Calibration Chart is of no importance during waveform observation.

CAUTION

When S1 is depressed, high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1 – 5 and 9, press: STOP

System 19, press KEYBD

NOTE

The digital card has one or more potentiometers for calibrating various timing functions of the card set. In normal usage, the card set will rarely need to have these functions re-calibrated.

However, in the event that the card set waveforms do not conform to the specifications of the Timing Diagram contact your nearest Data I/O Service Representative for calibration information.

SECTION 5
CIRCUIT DESCRIPTION

5.1 INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 5-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

5.1.1 DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signalled or until the bit is programmed.

5.1.2 ANALOG CARD

The analog card receives the DI Bus, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturers' specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow, timing and reject conditions. Detailed circuit schematics are found at the rear of this manual — refer to these for pin-out and interconnection information.

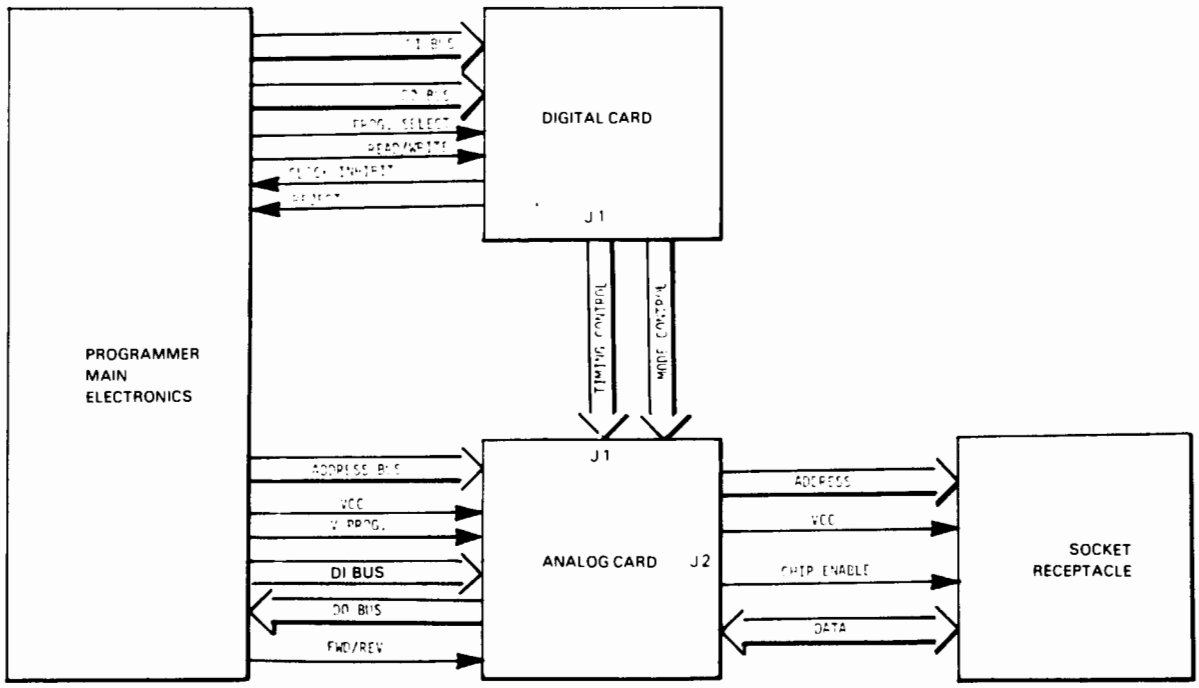


Figure 5-1. Simplified Block Diagram of Program Card Set

5.2 DIGITAL CARD

Figure 5-2 gives a generalized block diagram of the digital card. This diagram shows signal flow and functional relationships between the blocks but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) for details of circuit connection and operation. The following paragraphs discuss the functions performed by the digital card.

5.2.1 SELECT GATING

The select gates monitor the programmer status lines in order to enable operation of the digital card. Outputs supply data to the Program Memory, control Verify A and B for 4/8 bit operation and Abort condition, and are routed to the analog card to control the data bus drivers.

5.2.2 PROGRAM MEMORY

When the digital card is selected for operation, the Program Memory will set when it receives a Write command. This causes the digital card to begin operation and halts the programmer clock. Initialization of the Program Pulse Counter, Bit Counter and Sequence Counter and clearing of the Overprogram Counter occur before the Program Memory is set.

5.2.3 MASTER CLOCK

The Master Clock is stopped prior to setting of the Program Memory. When the Program Memory sets, the Master Clock is enabled. This clock drives the sequence generator, thereby providing the timing reference for all waveforms presented to the PROM.

5.2.4 SEQUENCE GENERATOR

The sequence generator consists of a 4-bit Sequence Counter and a 32x8 Timing ROM. The combination generates timing signals for analog card control, along with bit test and Master Clock control.

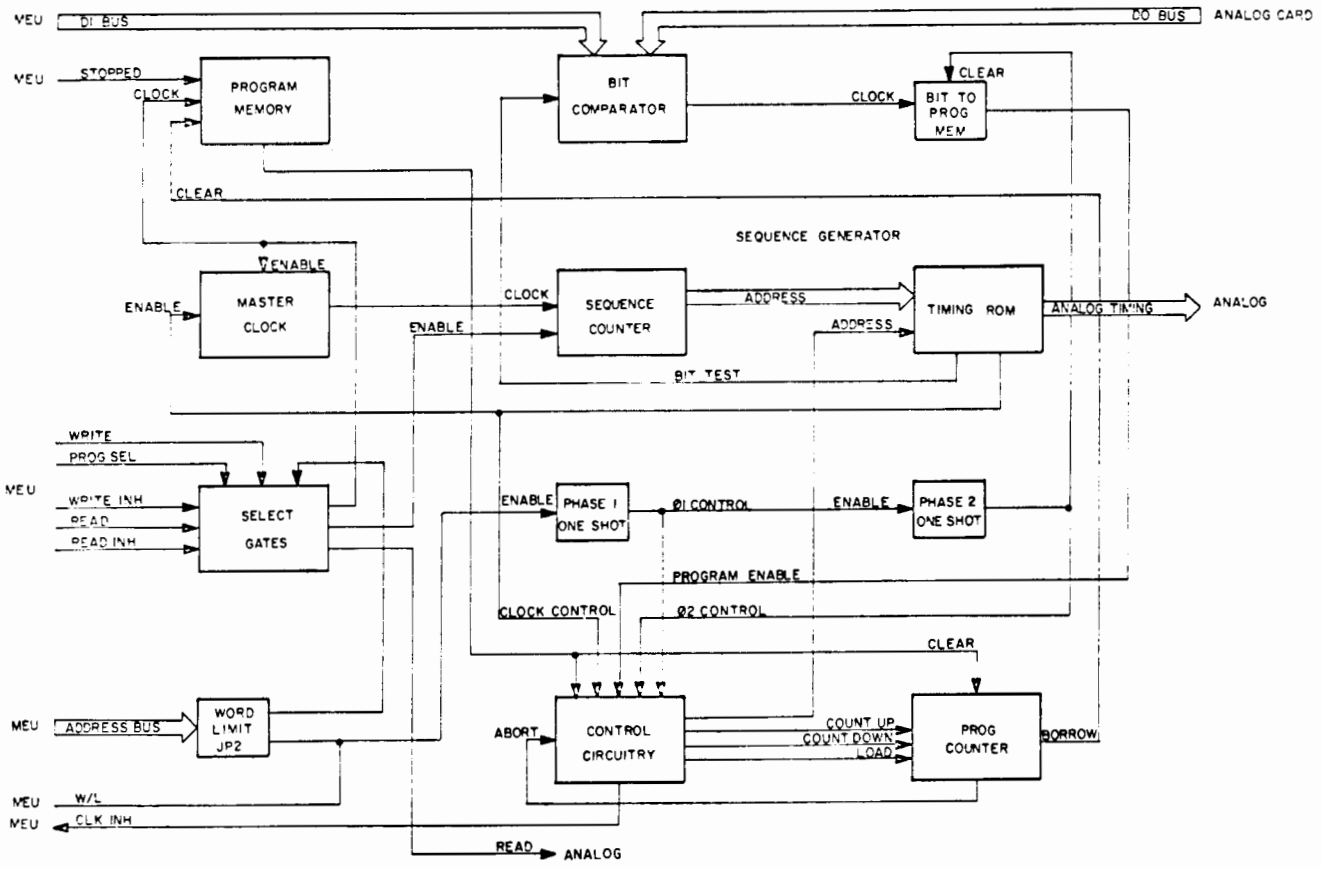


Figure 5-2. Block Diagram 1196 Digital Card

5.2.5 READ OPERATION

The Timing ROM issues a pulse to the Bit Test gate on the second clock pulse. The clock is stopped on the next clock pulse defeating CLK INH (busy signal). The programmer then increments the word count and issues another write command.

The entire cycle repeats itself for every address up to word limit. If the PROM verifies at each address, the Comparators will not enable the Bit Test gate. The Bit to Program Memory will remain reset, applying a low to the "D" input of the overprogram memory.

When word limit is reached, the programmer jumps to address Ø, rather than counting back down to Ø. This is determined by the low level on card pin 26.

Word limit also triggers the Phase-1 One-shot, which will clock the Overprogram Memory, resetting it. The count-down input of the Program Loop Counter will then be able to receive the Q pulse from the Phase-1 One-shot. As the counter is initially cleared, a count-down pulse will cause the counter to issue a borrow pulse. This pulse resets the Program Release latch, resetting the Program Memory.

The card set will repeat the verify on the second Ø-to-word-limit loop. At word limit, the programmer will not jump to Ø but will change direction and count downword. The direction change occurs because pin 26 is now high as a result of the program memory's resetting when the last word limit occurred. Control is then returned to the programmer.

5.2.6 PROGRAM OPERATION

If any bit to program is found at any address the Bit-to-Program Memory will set and remain so until cleared by the Phase-2 One-shot at the next word limit. Setting this flip-flop enables the Loop Count gate and applies a high to the "D" input of the Overprogram Memory. This inhibits the count-down input of the counter. At word limit, the address will jump to Ø, and the Phase-1 One-shot will increment the Program Loop Counter and also clock the H/O Memory.

As the Timing ROM continues to receive count pulses, bits 3, 4 and 5 send voltage commands to the analog card. At the end of this program loop, word limit triggers the One-shot, resetting the H/O memory and again incrementing the counter. Another verify loop is then performed. Program and Verify loops alternate until the bits are programmed, up to a maximum of 128 pairs of program-verify loops. At 128, the programmer is stopped, indicating an abort.

5.2.7 OVERPROGRAM OPERATION

When a verify loop yields no bits to program, the Bit-to-Program Memory will remain reset. At word limit the Overprogram Memory will reset and enable the Overprogram Load gate. This loads the counter with its preset input (80). The counter then counts down through 80 loops. H/O memory will remain preset so that program pulses will be applied to the PROM during all 80 loops, rather than on alternate loops only. When the counter reaches word Ø, a borrow pulse from the counter resets the Program Release flip-flop. This resets the Program Memory, which, in turn, causes pin 26 to to high. The high on pin 26 disables the jump to Ø at the end of the next loop, and the programmer then resumes the normal sequence of counting back down to Ø, performing the final verify sequence, and then stopping.

5.2.8 WORD LIMIT GATING

Word Limit gates provide the capabilities for a jumperable Word Limit. The gate output pulls Word Limit low when the jumper-selected address line goes high.

5.3 ANALOG CARD

Figure 5-3 is a generalized block diagram of the analog card. This diagram shows signal flow and functional relationships between the blocks. Refer to the schematics and Timing Diagram (with truth tables) for details of circuit connection and operation.

5.3.1 POWER UP DELAY

This delay is used to inhibit the Program or Verify cycle from beginning after START is depressed. This is done to allow time for the device to recover from power-up of V_{CC}, V_{DD} and V_{BB}. This delay is accomplished by holding CLK INH (Y) low during the time-out of one-shot U2.

5.3.2 BACKWARDS DEVICE TEST

When a device is inserted in the socket backwards, the bit 1 line is held low. Before power is applied to the device a test is made to see if the bit 1 line is low. This is accomplished using the one-shot Q output, pin 13 of U2, to enable the backwards device test gate. The one-shot is triggered by START going high. If the bit 1 line is held low by a device inserted backwards, U6 pin 13 will be low, causing the backwards device test gate to pull the RESET line low. No power is applied to the device since the output of U2 holds the V_{CC}, V_{DD}, V_{PP}, and V_{BB} supplies cut off for the duration of the test.

5.3.3 V_{CC} SUPPLY

The V_{CC} supply is an emitter-follower pass transistor (Q6) with its output voltage controlled by the adjustable shunt regulator (Q2) and adjusted by R3. Transistor Q7 and resistors R10, R14, and R17 provide current limiting. Foldback current-limiting is accomplished as follows: When the supply current-limits and transistor Q1 turns ON, pulling RESET, transistor Q15 also turns ON, pulling the shunt regulator output OFF via diode CR2. While RESET, the programmer START line is low. Thus diode CR6, and gate U3 keep transistor Q15 turned ON, holding the supply output OFF.

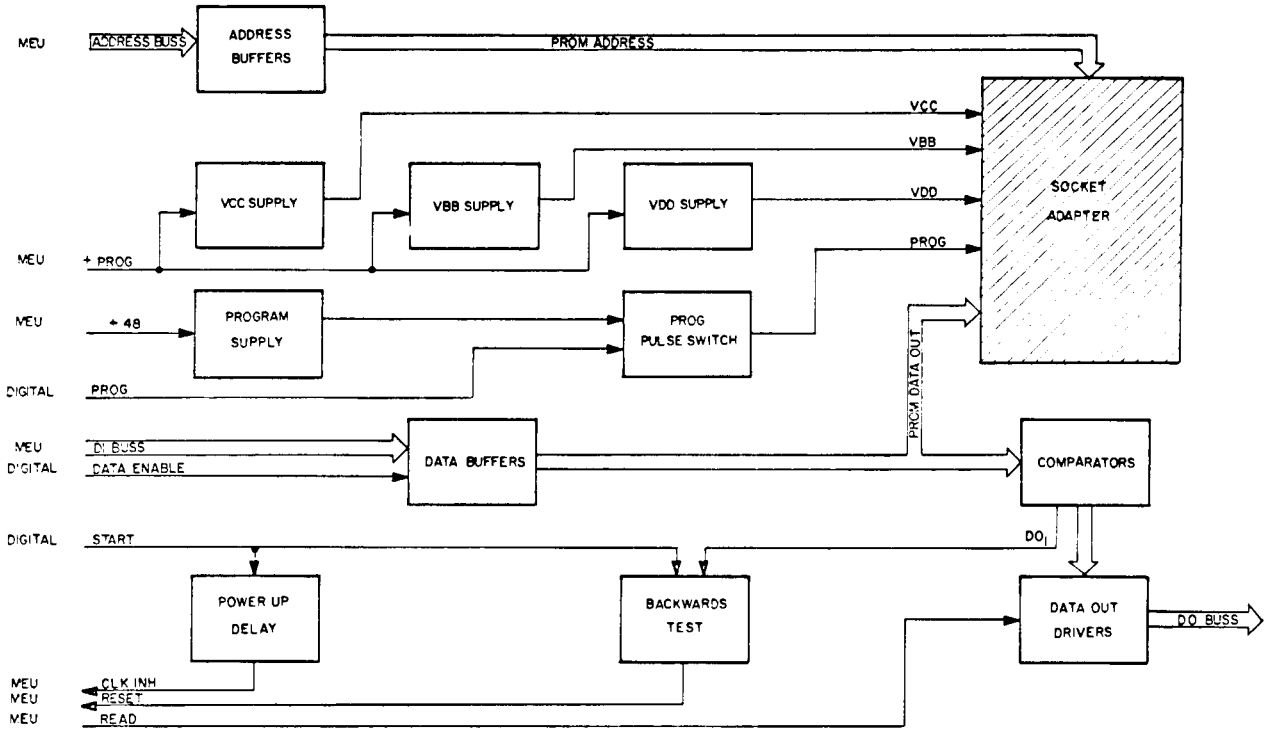


Figure 5-3. Analog Card Block Diagram

5.3.4 V_{DD} SUPPLY

The V_{DD} supply is identical to the V_{CC} supply except for its output voltage setting. Like the V_{CC} supply, it has foldback current limiting (Q8) with its output held OFF, through CR4, during STOP.

5.3.5 V_{BB} SUPPLY

The V_{BB} supply consists of emitter-follower pass transistor Q12, adjustable shunt regulator Q11 and current-limit transistors Q13 and Q14. Zener diode CR5 and resistor R44 shift the positive regulator Q11 to a negative value. This shift enables the supply to output a negative voltage.

5.3.6 PROGRAM SUPPLY AND PROGRAM PULSE SWITCH

The Program Supply (V_{PP}) consists of emitter-follower pass transistor Q17, adjustable shunt regulator Q16 and current-limit transistor Q20. Current limiting is accomplished when the zener voltage of CR12 plus the base-emitter voltage of Q20 is developed across resistor R47. Foldback current limiting is accomplished by transistor Q15 and diode CR9 by the same action previously described for the V_{CC} supply.

The program pulse switch routes the program supply output or the V_{CE} saturation voltage of Q19 to the PROM upon command from the digital card via J1 pin 2.

5.3.7 DATA BUFFERS

Information on the DI Bus is gated to the PROM through the Data Buffers. During Program, these gates are enabled by J1 pin 1 (Data). During Read, this line is disabled.

5.3.8 DATA OUT DRIVERS AND COMPARATORS

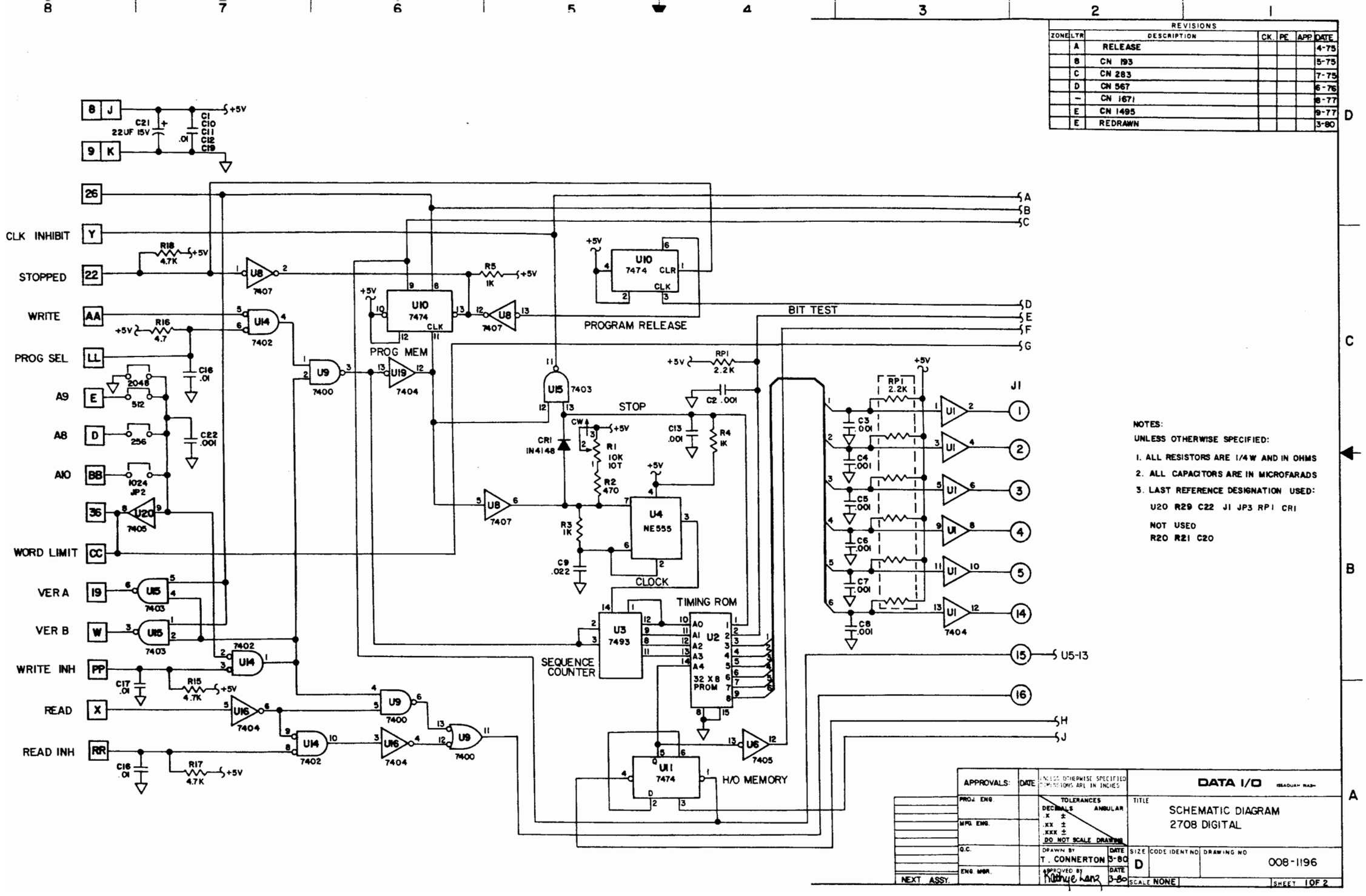
The Comparator compares PROM bit data against the reference level. The reference for the Comparator is determined by voltage divider action of R12 and R16. Comparator outputs are transferred to the DO bus during Read by the data out drivers. This transfer allows the digital card to make a digital comparison between the transferred PROM output (DO Bus) and the programmer input (DI Bus).

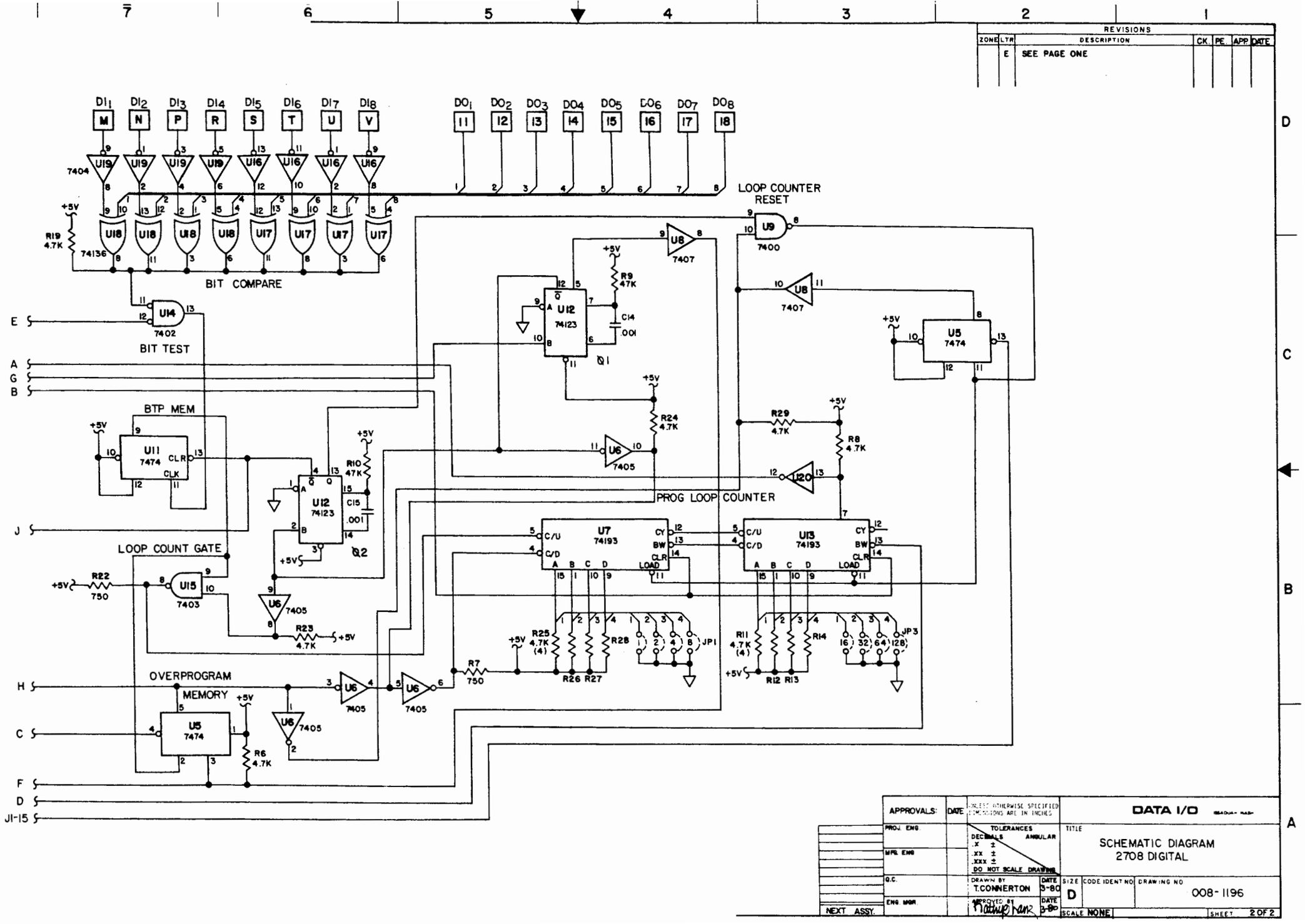
5.3.9 ADDRESS BUFFERS

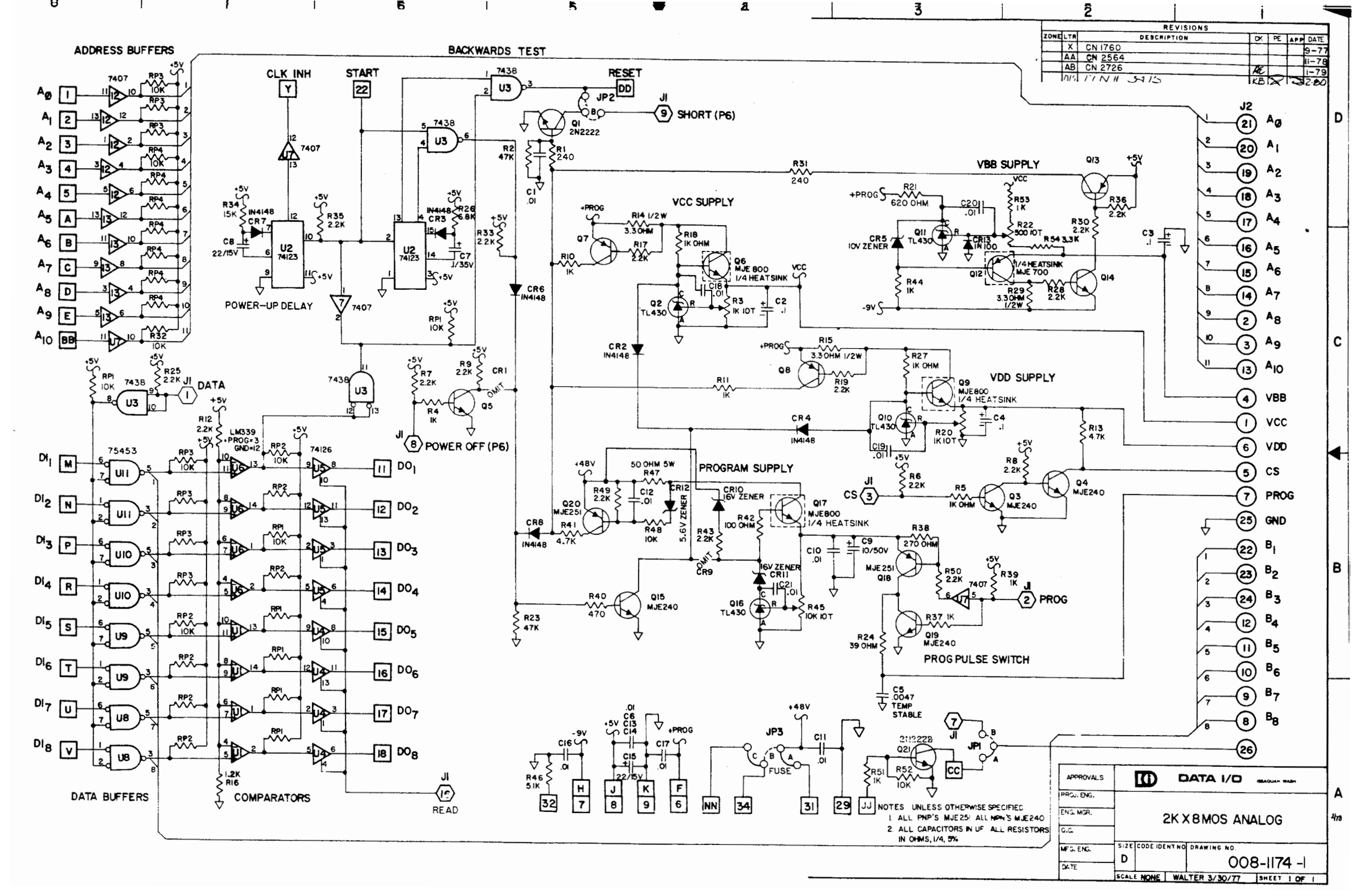
The address buffers accommodate the ten incoming address lines emanating from the programmer MEU. Outputs from these lines address the PROM.

SECTION 6
SCHEMATICS

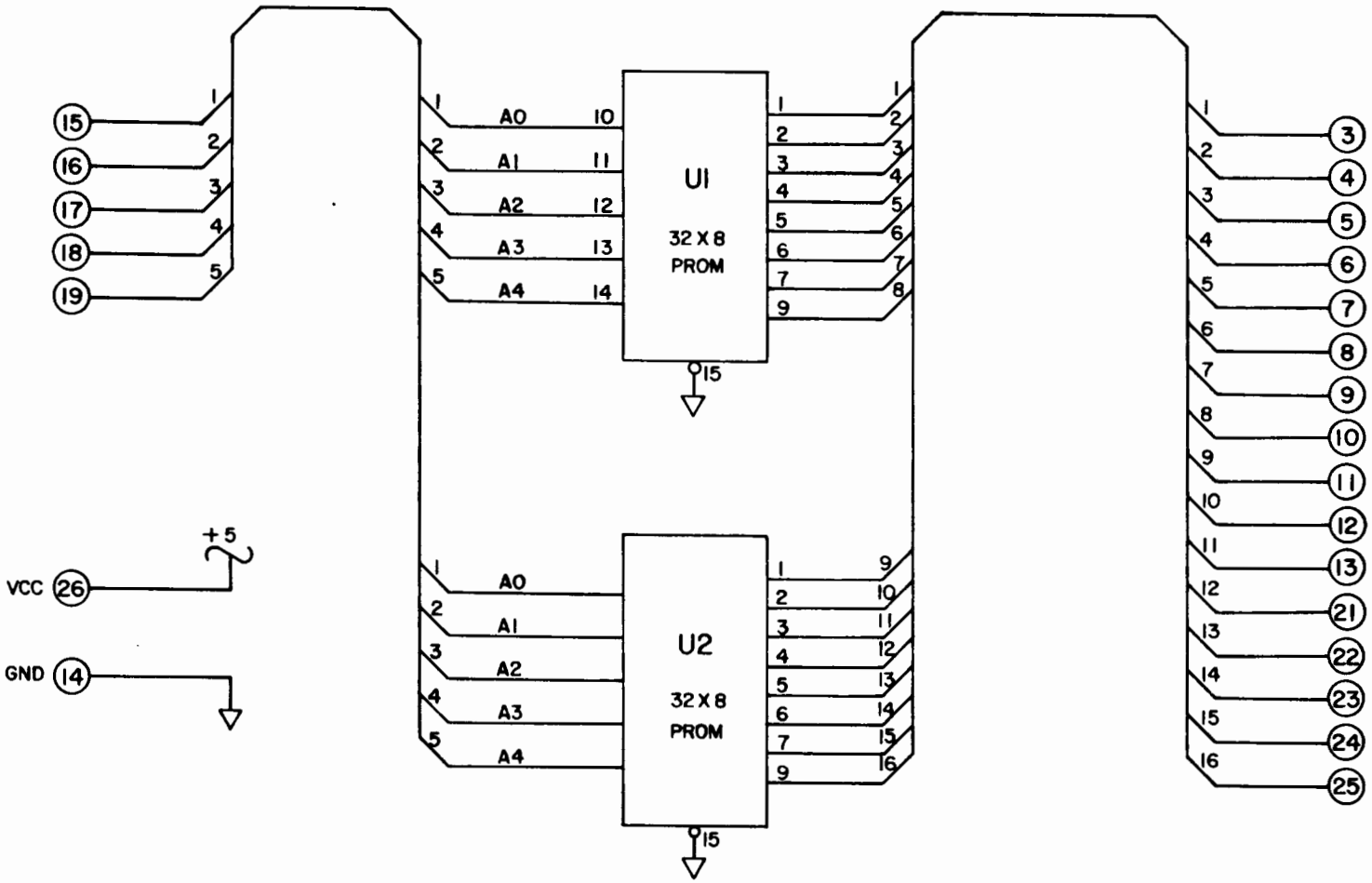
008-1196	Digital
008-1174-1	3-Voltage MOS
008-1072	Calibration Adapter


REVISIONS
ZONE LTR DESCRIPTION CK. PE. APP. DATE
A RELEASE 4-75
B CN 193 5-75
C CN 283 7-75
D CN 567 6-76
– CN 1671 8-77
E CN 1495 9-77
E REDRAWN 3-80
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE 1/4 W AND IN OHMS
2. ALL CAPACITORS ARE IN MICROFARADS
3. LAST REFERENCE DESIGNATION USED:
U20 R29 C22 J1 JP3 RP1 CR1
NOT USED
R20 R21 C20
CLK INHIBIT
STOPPED
WRITE
PROG SEL
A9
A8
A10
WORD LIMIT
VER A
VER B
WRITE INH
READ
READ INH
PROGRAM RELEASE
BIT TEST
PROG MEM
STOP
CLOCK
TIMING ROM
SEQUENCE COUNTER
H/O MEMORY
APPROVALS:
DATE
PROJ. ENG.
MFG. ENG.
Q.C.
ENG. MGR.
NEXT ASSY.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS ANGULAR
.X ±
.XX ±
.XXX ±
DO NOT SCALE DRAWING
DRAWN BY T. CONNERTON DATE 3-80
APPROVED BY DATE 3-80
DATA I/O
TITLE
SCHEMATIC DIAGRAM
2708 DIGITAL
SIZE D
CODE IDENT NO
DRAWING NO 008-1196
SCALE NONE
SHEET 1 OF 2


REVISIONS
ZONE LTR DESCRIPTION CK PE APP DATE
E SEE PAGE ONE
DI1 DI2 DI3 DI4 DI5 DI6 DI7 DI8
M N P R S T U V
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8
11 12 13 14 15 16 17 18
7404
74136
R19 4.7K
BIT COMPARE
LOOP COUNTER RESET
7400
7407
74123
R9 47K
C14 .001
Q1
R24 4.7K
7405
R29 4.7K
R8 4.7K
7474
BTP MEM
CLR CLK
R10 47K
C15 .001
Q2
PROG LOOP COUNTER
74193
C/U C/D CY BW CLR LOAD A B C D
LOOP COUNT GATE
7403
R22 750
R23 4.7K
OVERPROGRAM MEMORY
R6 4.7K
R7 750
R25 4.7K (4)
R26 R27 R28
JP1
R11 4.7K (4)
R12 R13 R14
JP3
E
BIT TEST
A
G
B
J
H
C
F
D
JI-15
APPROVALS: DATE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS ANGULAR
.X ±
.XX ±
.XXX ±
DO NOT SCALE DRAWING
PROJ. ENG.
MFR. ENG.
Q.C.
ENG. MGR.
NEXT ASSY.
DRAWN BY T.CONNERTON DATE 5-80
APPROVED BY DATE 5-80
DATA I/O
TITLE
SCHEMATIC DIAGRAM
2708 DIGITAL
SIZE D
CODE IDENT NO
DRAWING NO 008-1196
SCALE NONE
SHEET 2 OF 2


ADDRESS BUFFERS
BACKWARDS TEST
CLK INH
START
RESET
SHORT (P6)
POWER-UP DELAY
DATA
POWER OFF (P6)
VCC SUPPLY
VBB SUPPLY
VDD SUPPLY
PROGRAM SUPPLY
PROG PULSE SWITCH
DATA BUFFERS
COMPARATORS
READ
PROG
CS
VBB
VCC
VDD
GND
FUSE
NOTES UNLESS OTHERWISE SPECIFIED
1. ALL PNP'S MJE251 ALL NPN'S MJE240
2. ALL CAPACITORS IN UF ALL RESISTORS IN OHMS, 1/4, 5%
REVISIONS
ZONE LTR DESCRIPTION DK PE APP DATE
X CN 1760 9-77
AA CN 2564 11-78
AB CN 2726 1-79
2-80
DATA I/O
2K X 8 MOS ANALOG
008-1174-1
SCALE NONE
WALTER 3/30/77
SHEET 1 OF 1

DATE	SYM	REVISION RECORD	DR	CK.
11-15-75	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL .-		SCALE	DRAWN BY G. ROPPE
FRACTIONAL .-	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		APPROVED BY
ANGULAR .-	DATE 10-15-75	DRAWING NUMBER 008-1072	