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K105-D LOGIC ANALYZER

USERS MANUAL ADDENDUM

68000 DISASSEMBLER

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INTRODUCTION

This addendum provides the user with specific information on the 68000 target microprocessor Disassembler. Included in the addendum are a microprocessor pinout diagram, microprocessor-to-logic analyzer connection data, screen displays of the preprogrammed menus, a screen display of captured data in the disassembled format and special notes on the disassembler/logic analyzer.

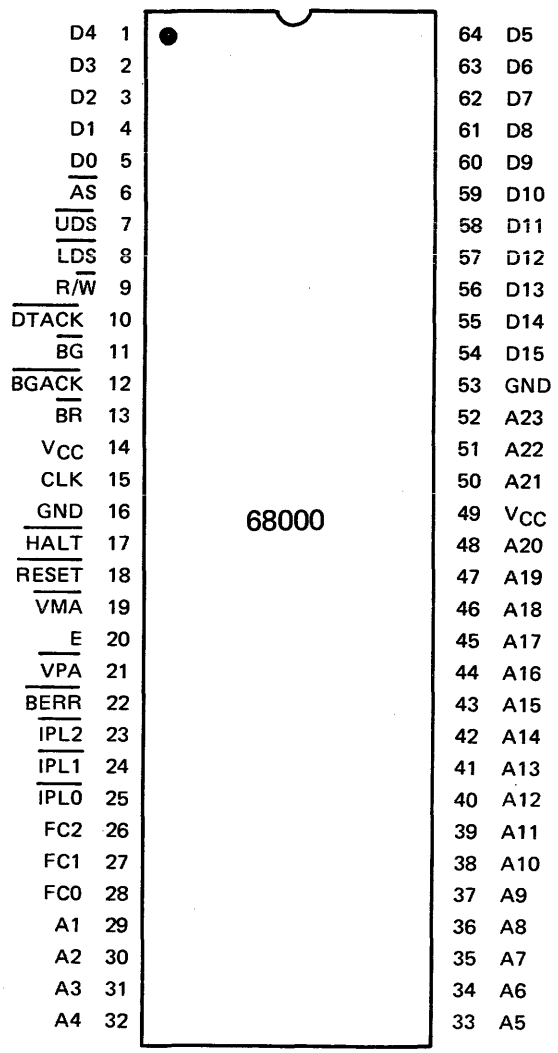

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Figure 1-1. 68000 Microprocessor Pinout Diagram

Table 1-1. Microprocessor-To-Logic Analyzer Connection Data

68000 SIGNAL	68000 PIN	K105-D PIN ASSIGNMENT
D4	1	A4
D3	2	A3
D2	3	A2
D1	4	A1
D0	5	A0
$\overline{AS}$	6	BJ
$\overline{UDS}$	7	BO
$\overline{LDS}$	8	CF
R/$\overline{W}$	9	CE
$\overline{DTACK}$	10	
$\overline{BG}$	11	
$\overline{BGACK}$	12	
$\overline{BR}$	13	
VCC	14	
CLK	15	$\overline{BK}$
GND	16	GND-A-B-C-D SECTIONS
$\overline{HALT}$	17	
$\overline{RESET}$	18	
$\overline{VMA}$	19	
$\overline{E}$	20	
$\overline{VPA}$	21	
$\overline{BERR}$	22	
$\overline{IPL2}$	23	CD
$\overline{IPL1}$	24	CC
$\overline{IPL0}$	25	CB
FC2	26	CA
FC1	27	C9
FC0	28	C8
A1	29	B1
A2	30	B2
A3	31	B3
A4	32	B4

Table 1-1. Microprocessor-To-Logic Analyzer Connection Data (Cont'd)

68000 SIGNAL	68000 PIN	K105-D PIN ASSIGNMENT
D5	64	A5
D6	63	A6
D7	62	A7
D8	61	A8
D9	60	A9
D10	59	AA
D11	58	AB
D12	57	AC
D13	56	AD
D14	55	AE
D15	54	AF
GND	53	GND-A-B-C-D SECTIONS
A23	52	C7
A22	51	C6
A21	50	C5
VCC	49	
A20	48	C4
A19	47	C3
A18	46	C2
A17	45	C1
A16	44	C0
A15	43	BF
A14	42	BE
A13	41	BD
A12	40	BC
A11	39	BB
A10	38	BA
A9	37	B9
A8	36	B8
A7	35	B7
A6	34	B6
A5	33	B5

ATTACHMENT TO A TARGET SYSTEM

Figure 1-2 illustrates a typical RTE to target system connection.

```
* * * * * * * * * * * * * * * * * * * * * * * *
*                  CAUTION                      *
*                                               *
* In the event the microprocessor on your target*
* system is hard-wired to the board, there is   *
* the possibility of inducing reflective noise  *
* into the test signals.  To eliminate this     *
* problem, we recommend varying the threshold   *
* voltage levels                                *
* * * * * * * * * * * * * * * * * * * * * * * *
```

NOTE: Figure 1-2 shows one of several possible connections of the RTE to a target system. As the configuration of the microprocessor pinouts change, the RTE to target system interface may also change.

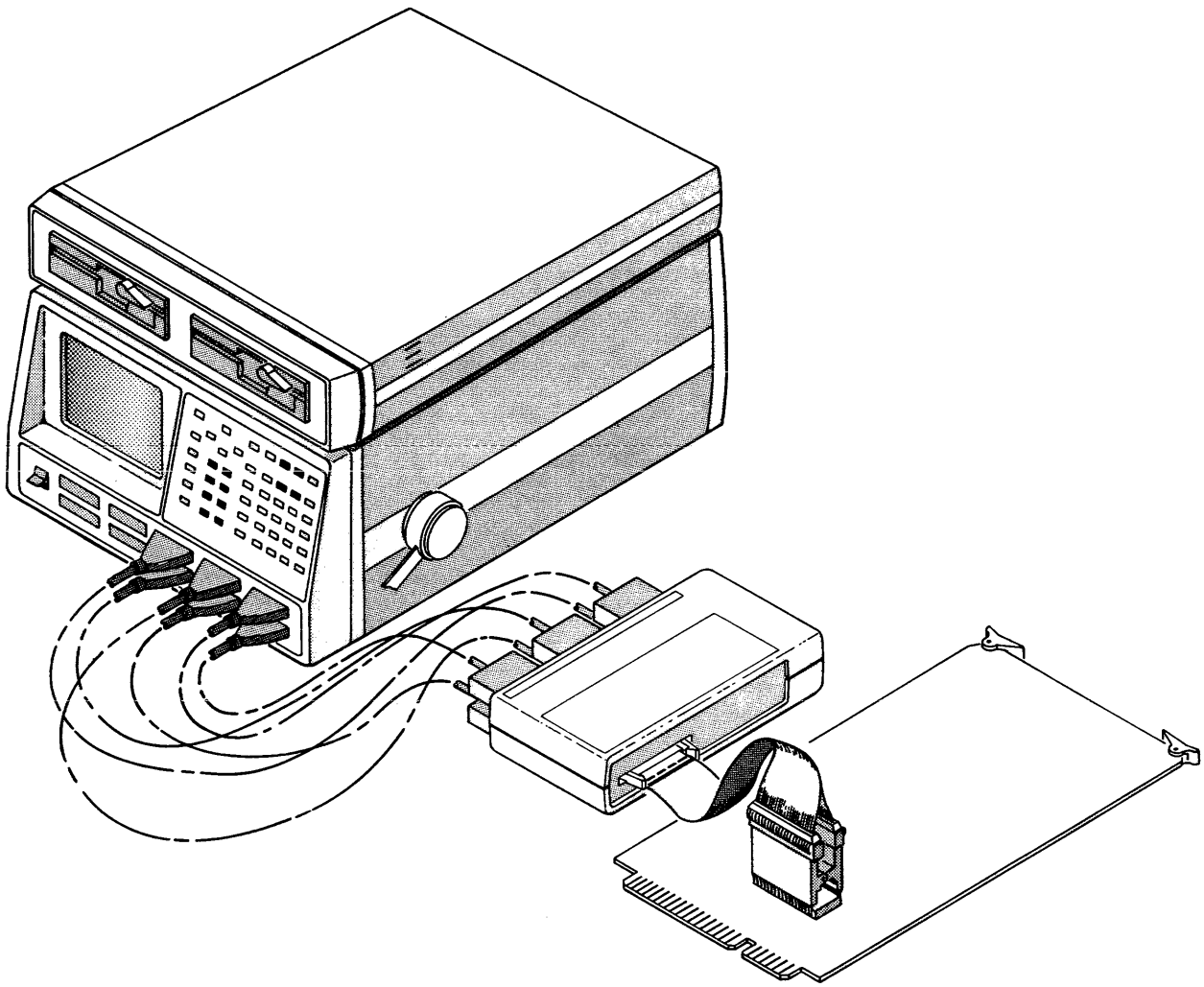

Figure 1-2. Typical RTE to Target System Connection

The RTE probe connectors are labeled to identify the input probe that must be plugged into a specific connector. The user shall remove the probe tips and install the probes, label up, into the RTE connectors. When connecting the microprocessor dip-clip cable into the RTE, special attention should be given to the keyed position of the connectors. The user should also ensure that pin 1 of the dip-clip is aligned with pin 1 of the microprocessor when connecting to the target microprocessor.

LOADING THE DISASSEMBLER

The following procedure provides step-by-step instructions for loading the Disassembler:

a. Enter the Disk Operating System screen.

b. Gently insert the disk into Drive B, with the disk slot toward the rear of the unit and the label up. Next, lock the disk in place with the drive latch handle.

c. Depress function key F3 to display the B directory.

d. Depress 1 to select the Recall function.

e. Use the right arrow cursor to enter the filename field and then use either the up or down cursor to select the Disassembler.

f. Depress function key F4 to load the Disassembler.

g. Depress the Format key to enter the Format screen.

h. Depress 6 and then Data to enter Disassembler mode.

```
* * * * * * * * * * * * * * * * * *
*                                   *
*              CAUTION              *
*                                   *
*  It is suggested that the user    *
*  make a backup copy of the        *
*  master disk prior to attempting  *
*  use of the disassembler.         *
*                                   *
* * * * * * * * * * * * * * * * * *
```

SPECIFICATIONS

PHYSICAL DIMENSIONS AND WEIGHT

Height - 2.25 inches (5.7 cm)
Width - 9.5 inches (24.1 cm)
Depth - 5.5 inches (14 cm)

Weight - 1 lb. 14 oz. (.84 kg) with flat cable and device clip

ELECTRICAL CHARACTERISTICS

Loading (Signal Inputs)

Input Resistance - 1 megohm ±2% to threshold (-1.4 volts)

Input Impedance - 150 ohms (approximate)

Typical Rise/Fall Distortion - heavily dependent on reserve drive of microprocessor and its support devices. The 68000 microprocessor typically slows 1.5 nanoseconds on edge rates.

Loading (Ground/Reference Input)

Input Resistance - Less than 1 ohm referenced to target system ground.

Ground Difference Immunity - ± 0.25 volts between logic analyzer ground and target system ground.

Reflected Noise Into Target System

Probed with Dip Clip or Circuit Board Socket - heavily dependent on target system ground. Typically, the system noise is reduced due to slower edge rates caused by probe load. This condition occasionally masks the problem being pursued.

SCREEN DISPLAYS OF PREPROGRAMMED SET UP MENUS

Figures 3-1 through 3-3 illustrate the preprogrammed setup menus downloaded from disk to the K105-D. Figures 3-4 and 3-5 illustrate the Disassembled Data and an Extended Instruction, respectively. When in the Disassembled Data display, sequential depression of the SHIFT and V keys causes the software version number for the disassembler to be displayed.

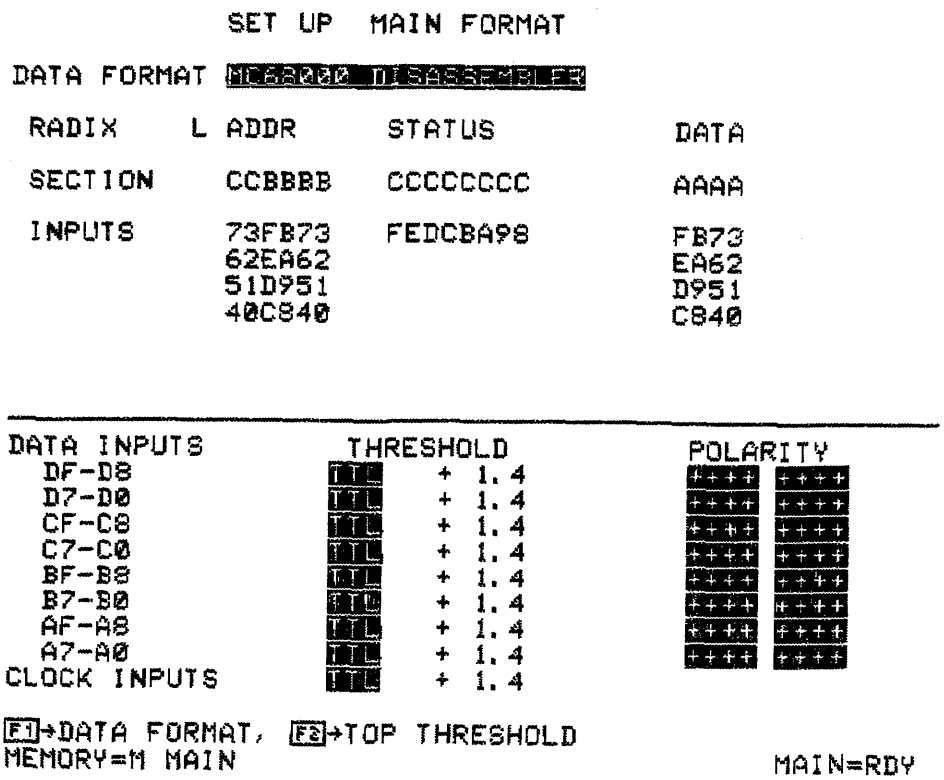

Figure 3-1. Disassembler Data Format Set Up Menu

SCREEN DISPLAYS OF PREPROGRAMMED SET UP MENUS (cont'd)

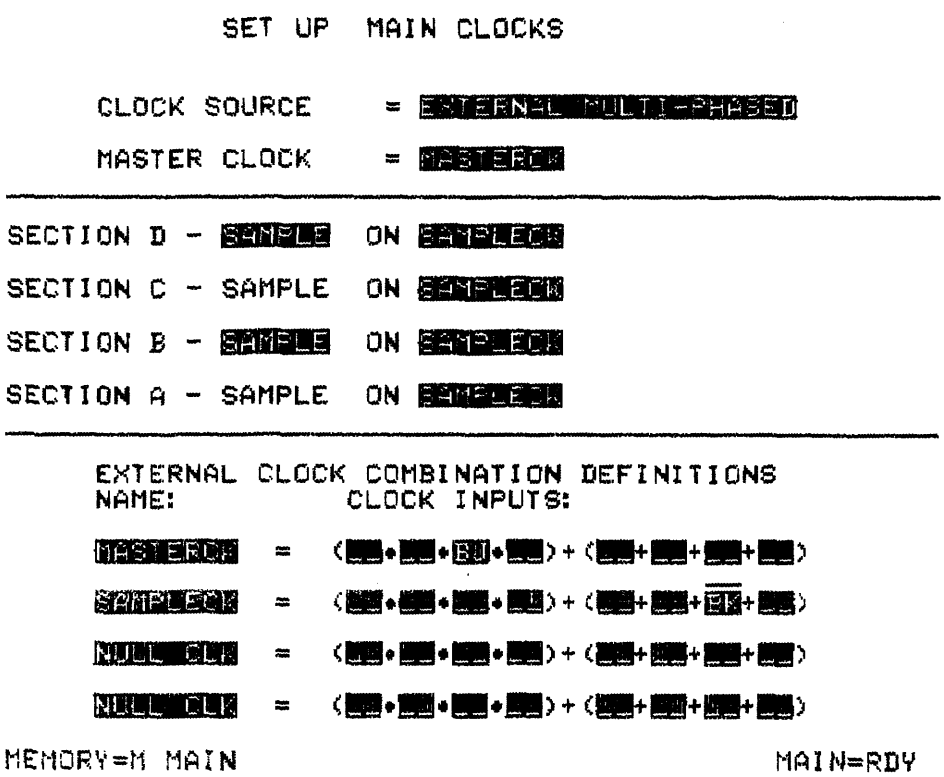

Figure 3-2. Clock Set Up Menu

SCREEN DISPLAYS OF PREPROGRAMMED SET UP MENUS (cont'd)

```
                SET UP  MAIN TRACE

LVL     COMMAND SEQUENCE:
0:TRACE  UNTIL    SAMPLE = ENABLE
1:TRACE  UNTIL    SAMPLE = TRIGGER
2:LINK ON ENTRY TO LEVEL
  TRACE  FOR    00500 CLOCKS
  -----

        PATTERN DEFINITIONS:
 NAME:          ADDR      STATUS          DATA
00 ENABLE   =XXXXXX    XXXXXXXX          XXXX
01 TRIGGER  =XXXXXX    XXXXXXXX          XXXX
02 _        =XXXXXX    XXXXXXXX          XXXX


F1→TOP CMD, F2→TOP PTRN
MEMORY=M MAIN                                   MAIN=RDY
```

Figure 3-3. Trace Control Set Up Menu

NOTE: In disassembler mode, the trace control patterns are formatted into address, status and data. When the Status field is selected as the active field, the possible choices are the status conditions of the processor as follows:

(0) S-PROG-R	(8) ACK
(1) U-PROG-R	(9) INT1
(2) U-DATA-R	(A) INT2
(3) U-DATA-W	(B) INT3
(4) U-PROG-W	(C) INT4
(5) S-DATA-R	(D) INT5
(6) S-DATA-W	(E) INT6
(7) S-PROG-W	(F) INT7

In Edit mode, status bits can be edited on a bit-by-bit basis. "X" selects all don't-cares.

SCREEN DISPLAYS OF PREPROGRAMMED SET UP MENUS (cont'd)

```
                    MC68000 DISASSEMBLER      CLK=EXT.MLT.

     S=XXXXXX XXXX                                          X
FRAME ADDR   OBJECT CODE  MNEMONIC                          L
   25 000754 S-DATA-W                2704                   2
   26 000756 S-DATA-W                0000                   2
   27 00007C S-DATA-R                0000                   2
   28 00007E S-DATA-R                991E                   2
   29 00991E 46FC2700      MOVE      #$2700,SR              2
   31 009922 S-PROG-R                21CF                   2
   32 009922 21CF0444      MOVE.L    A7,$444                2
   34 009926 4FFA000A      LEA       $A(PC),A7              2
   35 000444 S-DATA-W                0000                   2
   36 000446 S-DATA-W                0754                   2
   38 00992A 21CF04D6      MOVE.L    A7,$4D6                2
   40 00992E 6000F35C      BRA.L     $F35C(PC)              2
   41 0004D6 S-DATA-W                0000                   2
   42 0004D8 S-DATA-W                9932                   2
   44 008C8C 4FF80444      LEA       $444,A7                2
C  46 008C90>48E7FFFE      MOVEM.L   D0/D1/D2/D3/D4/D       2
   48 008C94 4FF8078A      LEA       $78A,A7                2
   49 000442 S-DATA-W                0540                   2
   50 000440 S-DATA-W                0000                   2
   51 00043E S-DATA-W                0540                   2
   52 00043C S-DATA-W                0000                   2

CONTROL=0046      REF=1023        R-C=+ 977
F1→PG UP F2→PG DOWN F3→DSPLY OBJ F4→DSPLY MNEMONICS
MEMORY=A MAIN                                    MAIN=RDY
```

Figure 3-4. Captured Data in Disassembled Format

NOTES:

1. After the disassembler data format, and clock select menus of the logic analyzer are pre-programmed, the trace control selections must be made by the user before making a recording. The trace control selections determines exactly which portions of the data stream are recorded or ignored.

2. The object code or operand of an instruction may be too long in some cases to be displayed on the K105-D screen. In these cases, a greater than symbol (>) is used to mark the code that has been truncated. The user can move the cursor to the indicated frame, depress the SHIFT key and then the E key to obtain an instruction expansion on the screen (see Figure 3-5).

3. When monitoring the 68000 pinout, words with "Program Read" status are being fetched to be put into the queue. Not all instruction words fetched are executed. Instruction words not executed are displayed with the "Program Read" status. Refer to the MC68000 Users Manual.

4. The SEARCH and COMPARE keys are not active in the Data Display Screen. The Edit mode can be used to change the search word. After leaving Edit mode, the NEXT and PREVIOUS keys locate target data in memory. If the search word is not active, the NEXT and PREVIOUS keys update the display to the next or previous trace level transition.

5. Depression of the F3 function key changes the display of recorded information. Code is not disassembled, but recorded information is displayed from the control cursor (C) position to the end of memory as frame number, address, status and data.

   If recorded data is displayed in object format, depressing the F4 function key invokes the disassembly process for data from the control cursor to the end of memory.

6. Illegal instructions are displayed as ???.

7. A Move to SR or CCR causes an extra clock cycle and duplication of the address and data. See Figure 3-4, frames 31 and 32.

8. The disassembler is first downloaded from disk to the K105-D and the disassembler format is selected. Then the trace patterns are configured as desired. It is suggested that the user make a backup copy of the master disk prior to attempting use of the disassembler.

```
                MC68000 DISASSEMBLER      CLK=EXT.MLT.

                INSTRUCTION EXPANSION

FRAME:              46
ADDRESS:          008C90
OBJECT CODE:      48E7 FFFE
MNEMONIC CODE:    MOVEM.L
OPERAND CODE:     D0/D1/D2/D3/D4/D5/D6/D7/A0/A1/
                  [illegible]

CONTROL=0046      REF=1023        R-C=+ 977
PRESS ANY HEX KEY TO LEAVE EXPANDED DISPLAY
MEMORY=A MAIN                                  MAIN=RDY
```

Figure 3-5. Expanded Instruction

68000 INSTRUCTION SET

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	(Destination)$_{10}$ + (Source)$_{10}$ → Destination	*	U	*	U	*
ADD	Add Binary	(Destination) + (Source) → Destination	*	*	*	*	*
ADDA	Add Address	(Destination) + (Source) → Destination	–	–	–	–	–
ADDI	Add Immediate	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDX	Add Extended	(Destination) + (Source) + X → Destination	*	*	*	*	*
AND	AND Logical	(Destination) Λ (Source) → Destination	–	*	*	0	0
ANDI	AND Immediate	(Destination) Λ Immediate Data → Destination	–	*	*	0	0
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count> → Destination	*	*	*	*	*
B$_{CC}$	Branch Conditionally	If $_{CC}$ then PC + d → PC	–	–	–	–	–
BCHG	Test a Bit and Change	~(<bit number>) OF Destination → Z ~(<bit number>) OF Destination → <bit number> OF Destination	–	–	*	–	–
BCLR	Test a Bit and Clear	~(<bit number>) OF Destination → Z 0 → <bit number> → OF Destination	–	–	*	–	–
BRA	Branch Always	PC + d → PC	–	–	–	–	–
BSET	Test a Bit and Set	~(<bit number>) OF Destination → Z 1 → <bit number> OF Destination	–	–	*	–	–
BSR	Branch to Subroutine	PC → SP@ – ; PC + d → PC	–	–	–	–	–
BTST	Test a Bit	~(<bit number>) OF Destination → Z	–	–	*	–	–
CHK	Check Register against Bounds	If Dn <0 or Dn> (<ea>) then TRAP	–	*	U	U	U
CLR	Clear an Operand	0 → Destination	–	0	1	0	0
CMP	Compare	(Destination) – (Source)	–	*	*	*	*
CMPA	Compare Address	(Destination) – (Source)	–	*	*	*	*
CMPI	Compare Immediate	(Destination) – Immediate Data	–	*	*	*	*
CMPM	Compare Memory	(Destination) – (Source)	–	*	*	*	*
DB$_{CC}$	Test Condition, Decrement and Branch	If ~ $_{CC}$ then Dn – 1 → Dn; if Dn ≠ – 1 then PC + d → PC	–	–	–	–	–
DIVS	Signed Divide	(Destination)/(Source) → Destination	–	*	*	*	0
DIVU	Unsigned Divide	(Destination)/(Source) → Destination	–	*	*	*	0
EOR	Exclusive OR Logical	(Destination) ⊕ (Source) → Destination	–	*	*	0	0
EORI	Exclusive OR Immediate	(Destination) ⊕ Immediate Data → Destination	–	*	*	0	0
EXG	Exchange Register	Rx ↔ Ry	–	–	–	–	–
EXT	Sign Extend	(Destination) Sign-extended → Destination	–	*	*	0	0
JMP	Jump	Destination → PC	–	–	–	–	–
JSR	Jump to Subroutine	PC → SP@ – ; Destination → PC	–	–	–	–	–
LEA	Load Effective Address	Destination → An	–	–	–	–	–
LINK	Link and Allocate	An → SP@ – ; SP → An; SP + d → SP	–	–	–	–	–
LSL, LSR	Logical Shift	(Destination) Shifted by <count> → Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source) → Destination	–	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source) → CCR	*	*	*	*	*
MOVE to SR	Move to the Status Register	(Source) → SR	*	*	*	*	*

* affected 0 cleared U defined
– unaffected 1 set

68000 INSTRUCTION SET (cont'd)

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
MOVE from SR	Move from the Status Register	SR → Destination	–	–	–	–	–
MOVE USP	Move User Stack Pointer	USP → An; An → USP	–	–	–	–	–
MOVEA	Move Address	(Source) → Destination	–	–	–	–	–
MOVEM	Move Multiple Registers	Registers → Destination (Source) → Registers	–	–	–	–	–
MOVEP	Move Peripheral Data	(Source) → Destination	–	–	–	–	–
MOVEQ	Move Quick	Immediate Data → Destination	–	*	*	0	0
MULS	Signed Multiply	(Destination)*(Source) → Destination	–	*	*	0	0
MULU	Unsigned Multiply	(Destination)*(Source) → Destination	–	*	*	0	0
NBCD	Negate Decimal with Extend	$0-(\text{Destination})_{10}-X \rightarrow$ Destination	*	U	*	U	*
NEG	Negate	0 – (Destination) → Destination	*	*	*	*	*
NEGX	Negate with Extend	0 – (Destination) – X → Destination	*	*	*	*	*
NOP	No Operation	–	–	–	–	–	–
NOT	Logical Complement	~(Destination) → Destination	–	*	*	0	0
OR	Inclusive OR Logical	(Destination) v (Source) → Destination	–	*	*	0	0
ORI	Inclusive OR Immediate	(Destination) v Immediate Data → Destination	–	*	*	0	0
PEA	Push Effective Address	Destination → SP@ –	–	–	–	–	–
RESET	Reset External Devices	–	–	–	–	–	–
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count> → Destination	–	*	*	0	*
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count> → Destination	*	*	*	0	*
RTE	Return from Exception	SP@ + → SR; SP@ + → PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	SP@ + → CC; SP@ + → PC	*	*	*	*	*
RTS	Return from Subroutine	SP@ + → PC	–	–	–	–	–
SBCD	Subtract Decimal with Extend	$(\text{Destination})_{10}-(\text{Source})_{10}-X \rightarrow$ Destination	*	U	*	U	*
S_{CC}	Set According to Condition	If CC then 1's → Destination else 0's → Destination	–	–	–	–	–
STOP	Load Status Register and Stop	Immediate Data → SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination) – (Source) → Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination) – (Source) → Destination	–	–	–	–	–
SUBI	Subtract Immediate	(Destination) – Immediate Data → Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination) – Immediate Data → Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination) – (Source) – X → Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16] ↔ Register [15:0]	–	*	*	0	0
TAS	Test and Set an Operand	(Destination) Tested → CC; 1 → [7] OF Destination	–	*	*	0	0
TRAP	Trap	PC → SSP@ –; SR → SSP@ –; (Vector) → PC	–	–	–	–	–
TRAPV	Trap on Overflow	If V then TRAP	–	–	–	–	–
TST	Test an Operand	(Destination) Tested → CC	–	*	*	0	0
UNLK	Unlink	An → SP; SP@ + → An	–	–	–	–	–

[ ] = bit number

* affected 0 cleared U defined
– unaffected 1 set