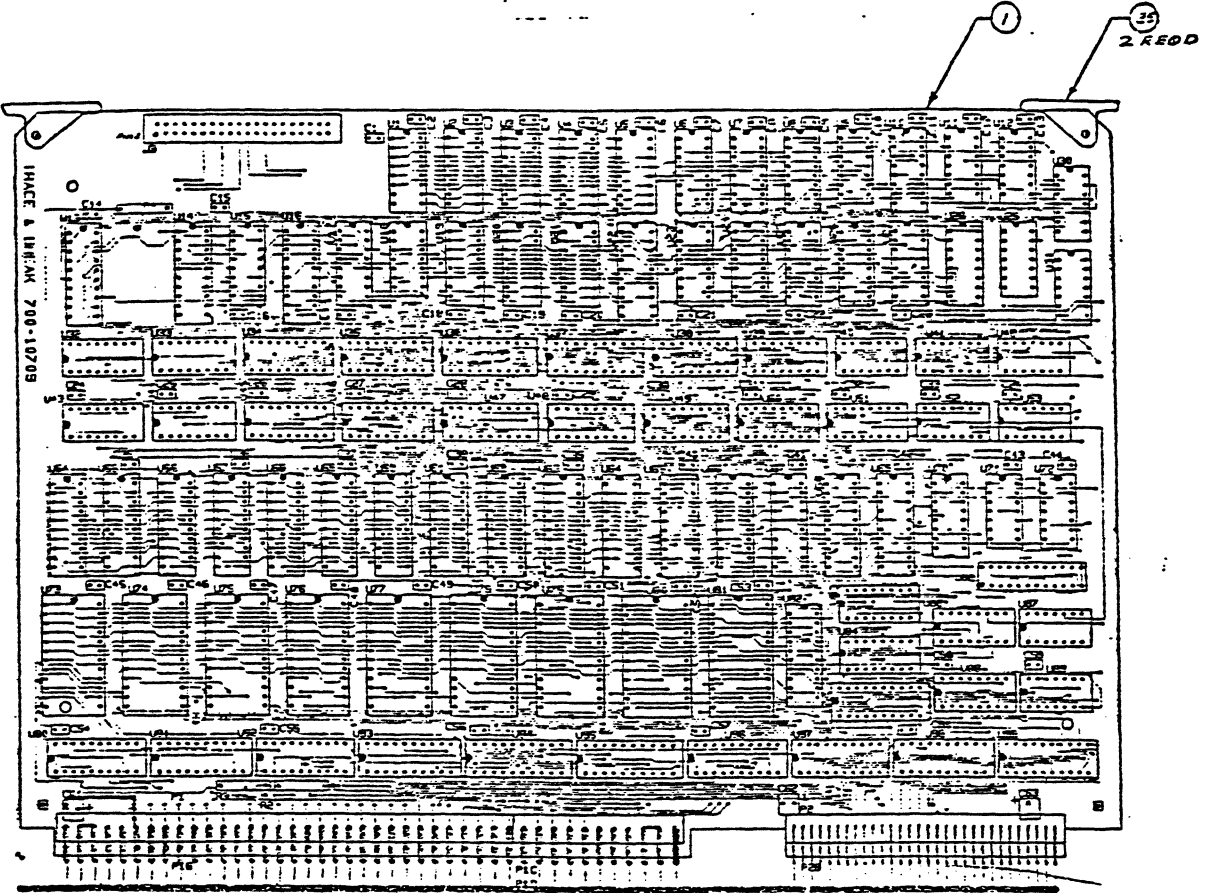


G INC ECN 508	DATE 1/1	REV 1	DESCRIPTION
F ECN 606	DATE 2/1	REV 1	DESCRIPTION
K INC ECN 254	DATE 1/1	REV 1	DESCRIPTION
L ECN 334	DATE 1/1	REV 1	DESCRIPTION
M ECN 333	DATE 1/1	REV 1	DESCRIPTION
N ECN 467	DATE 1/1	REV 1	DESCRIPTION
DRAWING CLARIFICATION 453 LK 2:25 F INC ECN 256			DESCRIPTION



QTY/DASH NO.	ITEM NO.	PART NUMBER	DESCRIPTION	REF DES/PAO	
	1	42	335-10470-01	IC RAM-2149H-2	1637
		41	DELETED		
	1	40	470-10500	RES-22 OHM, 1/4 W, 5%	24
	3	39	470-10283	RES-75 OHM, 1/4 W, 5%	21-3
		38	DELETED		
	9	37	210-10075	SOCKET-24 PIN DIP	44-73-81
	1	36	210-10297	CONN-40 PIN HEADER 27 A66	13
	2	35	220-10687	EXTRACTOR CARD	
	3	34	120-10091	CAP-.33 MFD 10V 50V	61-23
	40	33	150-10003	CAP-.1 MFD, 50V CER	61-60
	7	32	314-10677	IC-74LS273, OCT D-LATCH TS	U90-96
	1	31	314-10705	IC-74LS260, POSI NOR GATE	U89
	1	30	314-10328	IC-74LS04, HIGH SPEED INV	U87
	1	29	314-10619	IC-74LS158, MAGNITUDE COMP	U85
	2	28	314-10895	IC-25452538	U82, 88
	9	27	335-10694-01	SRAM-4096 2K X8 NVDS CMOS	U73-81
	1	24	320-10704	IC-74LS10-100	U71
	3	25	314-10702	IC-74LS669, UP/DWN 5-MC CTR	U70, 82, 84
	1	26	314-10123	IC-74LS379, OCT D F-F	U69
	1	23	314-10284	IC-74LS379	U68
	14	22	314-10070	IC-74LS245, BUS DIR. 16 BIT	U65, 66, 67, 68
	1	21	314-10703	IC-74LS79, POS EDGE TRIGG FE	U63
	1	20	314-11058	IC-74LS32, QUAD 2-INPUT NOR	U62
	1	19	314-10063	IC-74LS10, TRIP 3-CART NAND	U61
	1	18	314-10052	IC-74LS02, QUAD 2-INPUT NOR	U60
	2	17	335-11407-00	RAM-2147	U55, 56
	4	16	335-10671	RAM-2116AL-3, 150 NS	U59, 65-67
	1	15	314-10255	IC-74LS27, TRIP 3-IMP NOR	U51
	2	14	314-10053	IC-74LS04, HEX INVERTER	U50,
	1	13	314-10655	IC-74LS74, DUAL D F-F	U49
	4	12	314-10669	IC-74LS244, OCT BUF, NON INV	U47, 48, 49
	2	11	314-10699	IC-74LS00, POSITIVE NANC GATE	U45, 46
	2	10	314-10234	IC-74LS373, OCT D-LATCH TS	U44, 46
	2	9	314-10062	IC-74LS00, QUAD NAND	U42, 44
	1	8	314-10117	IC-74LS20, DUAL 4-INPUT NAND	U41
	5	7	314-10173	IC-74LS138, DECODER 3-B LINE W/ 8 C. LINES	U40
	1	4	314-10614-00	IC-74LS86, QUAD EXCL-OR	U3
	4	5	314-10121	IC-74LS161A, 4 BIT BIN CTR	U6, 24, 28
	5	4	314-10704	IC-74LS670, 4X4 REGIST FILE	U6, 7, 23, 25, 27
	18	3	335-10698	RAM-2125H-4, 1K X1 INTEL	U5, 13, 17, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47
		2	DELETED		
	1	1	170-10663-05	PVNB-ES/EX TRACE & BREAK	
			-03 (SUPERCEDES-00, N/A) PCB-ES TRACE & BREAK		

1. FOR 170-10663-03 & 04 REWORK PER ECN S 254 & 334 & 333 606
 NOTES: UNLESS OTHERWISE SPECIFIED

JUN 16 1986
 SEP 20 1985

APPLIED
 MICROSYSTEMS

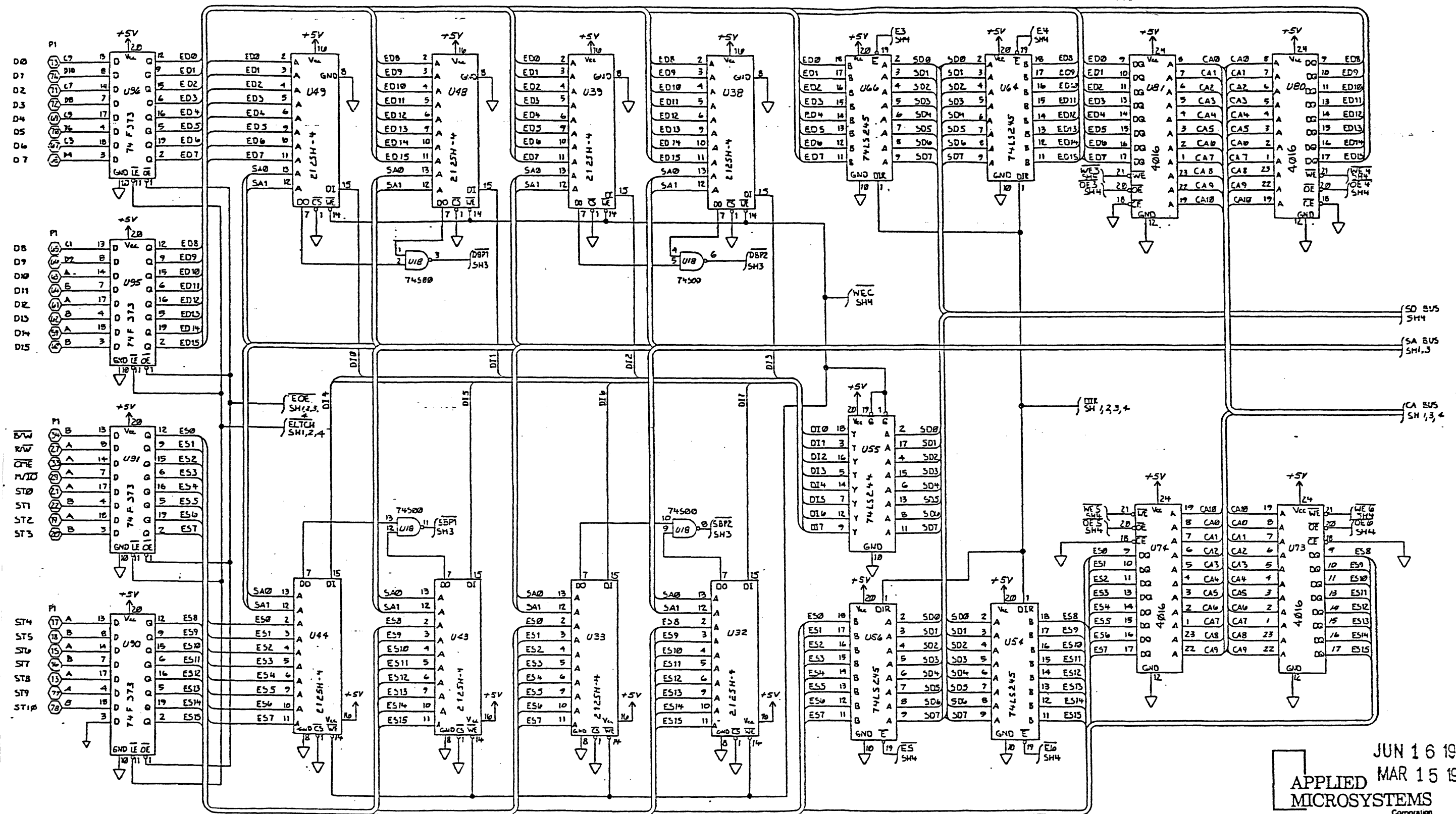
PCB ASSY-
 TRACE & BREAK ES

DRAMA	M	2-3-82	700-10709-PL
CHECK	J. Q.	4-1-82	
DATE	WR	1-11-82	

NEXT USED ON: 900-10930-01

PRODUCTION

1	SEE SHT 1
2	1Mk ED TEST (MS) - MATCHES - DB ADDRESS
3	ALSO - S70 & S11 - DB, U7 WAS LUNA-1
	SEE SHT 2



JUN 16 1986
 APPLIED MAR 15 1985
 MICROSYSTEMS
 Corporation

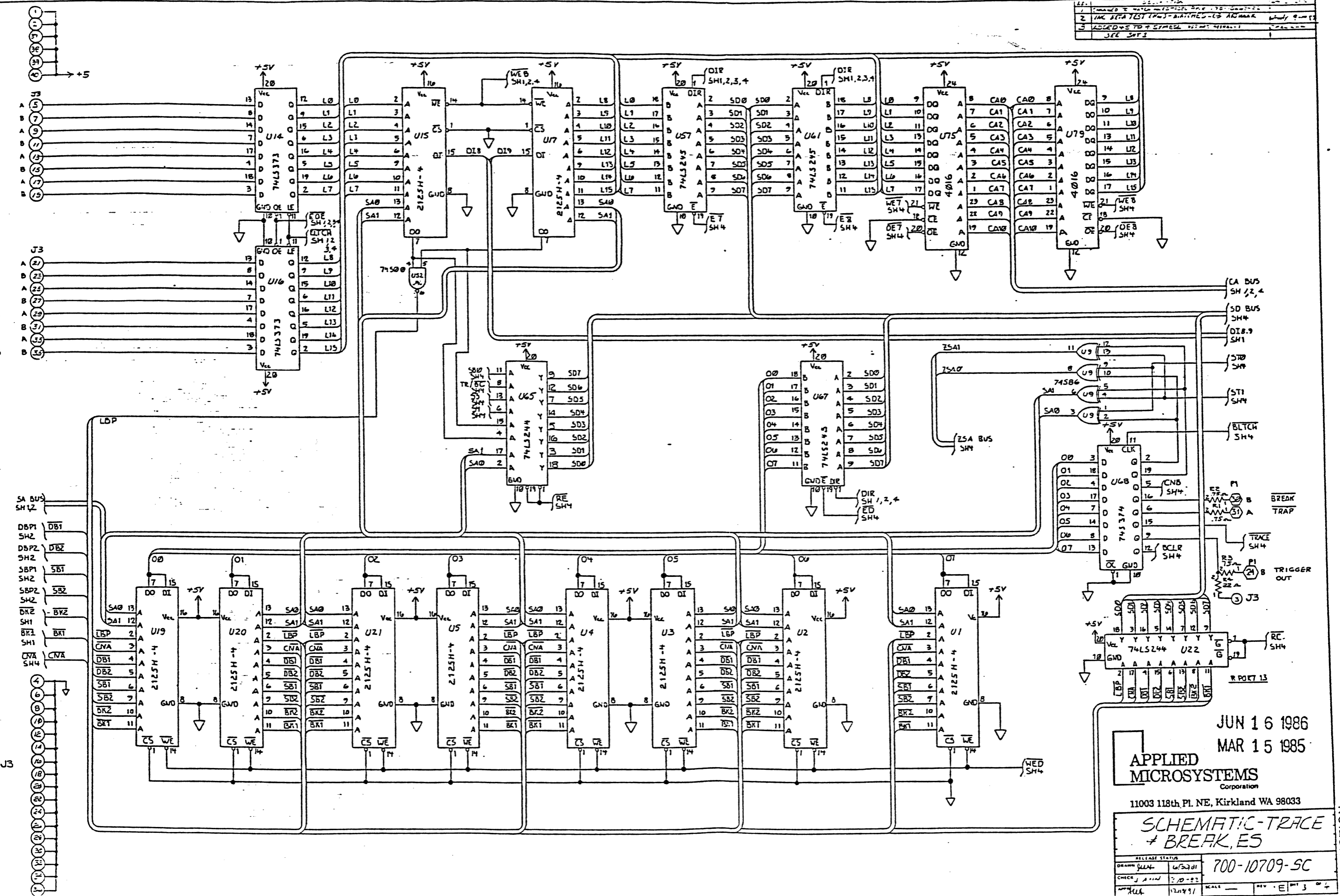
11003 118th Pl. NE, Kirkland WA 98033

**SCHEMATIC - TRFCE
 & BREAK, ES**

DATE	6/30/81	700-10709-SC
CHG		
APP		
SCALE		

11003 118th Pl. NE, Kirkland WA 98033

1	ADDED TO 7 SYMBOLS	12/18/85
2	ADDED TO 7 SYMBOLS	12/18/85
3	ADDED TO 7 SYMBOLS	12/18/85
SEE SH3		

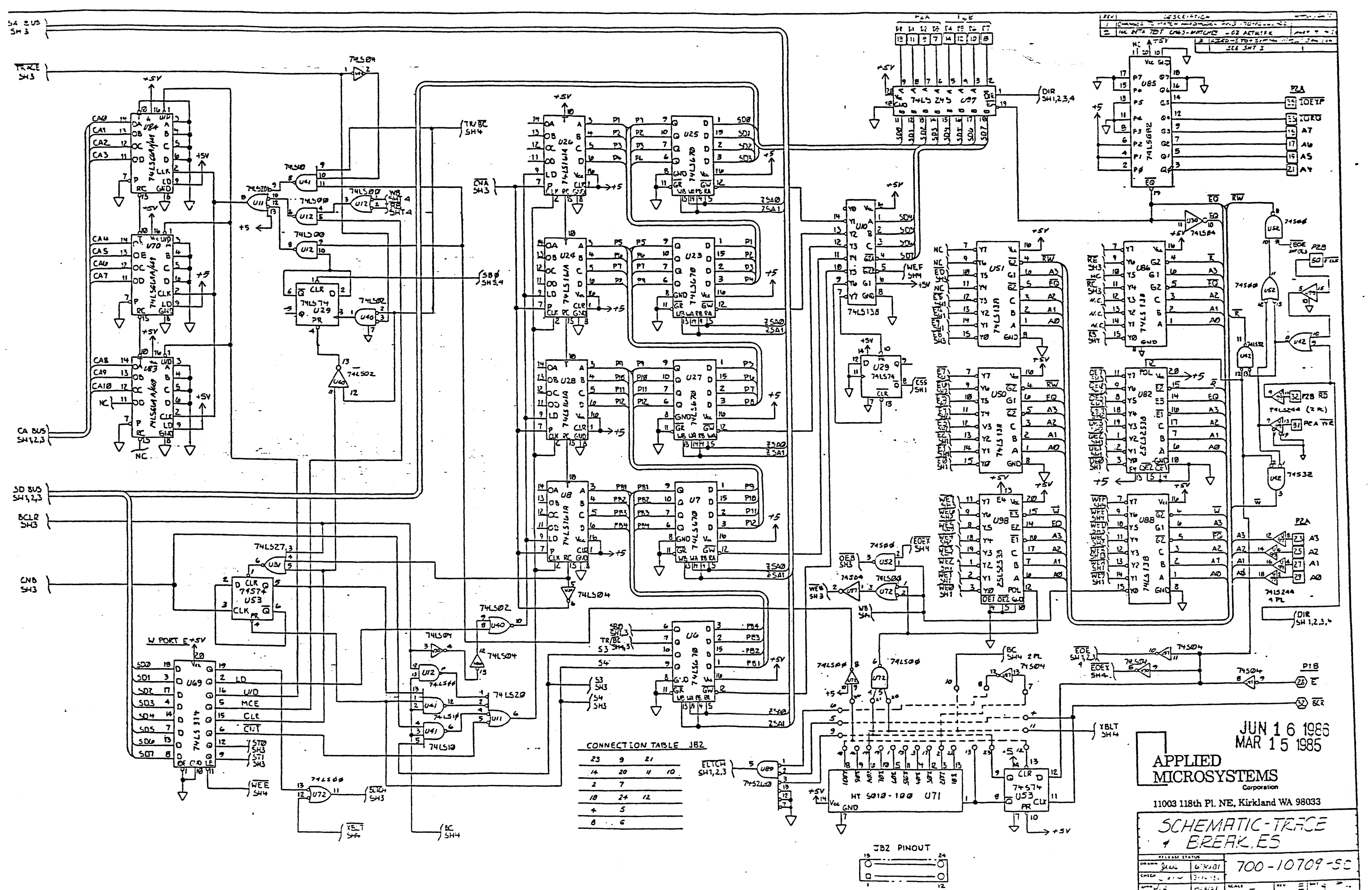


JUN 16 1986
 MAR 15 1985
 APPLIED
 MICROSYSTEMS
 Corporation

11003 118th Pl. NE, Kirkland WA 98033

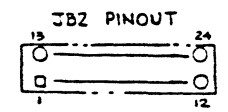
SCHMATIC TRACE
 # BREAK, ES

RELEASE STATUS	700-10709-SC
DRAWN BY	6/5/81
CHECKED BY	7/10/82
DATE	12/18/85
SCALE	1:1
PRODUCTION	3



CONNECTION TABLE J82

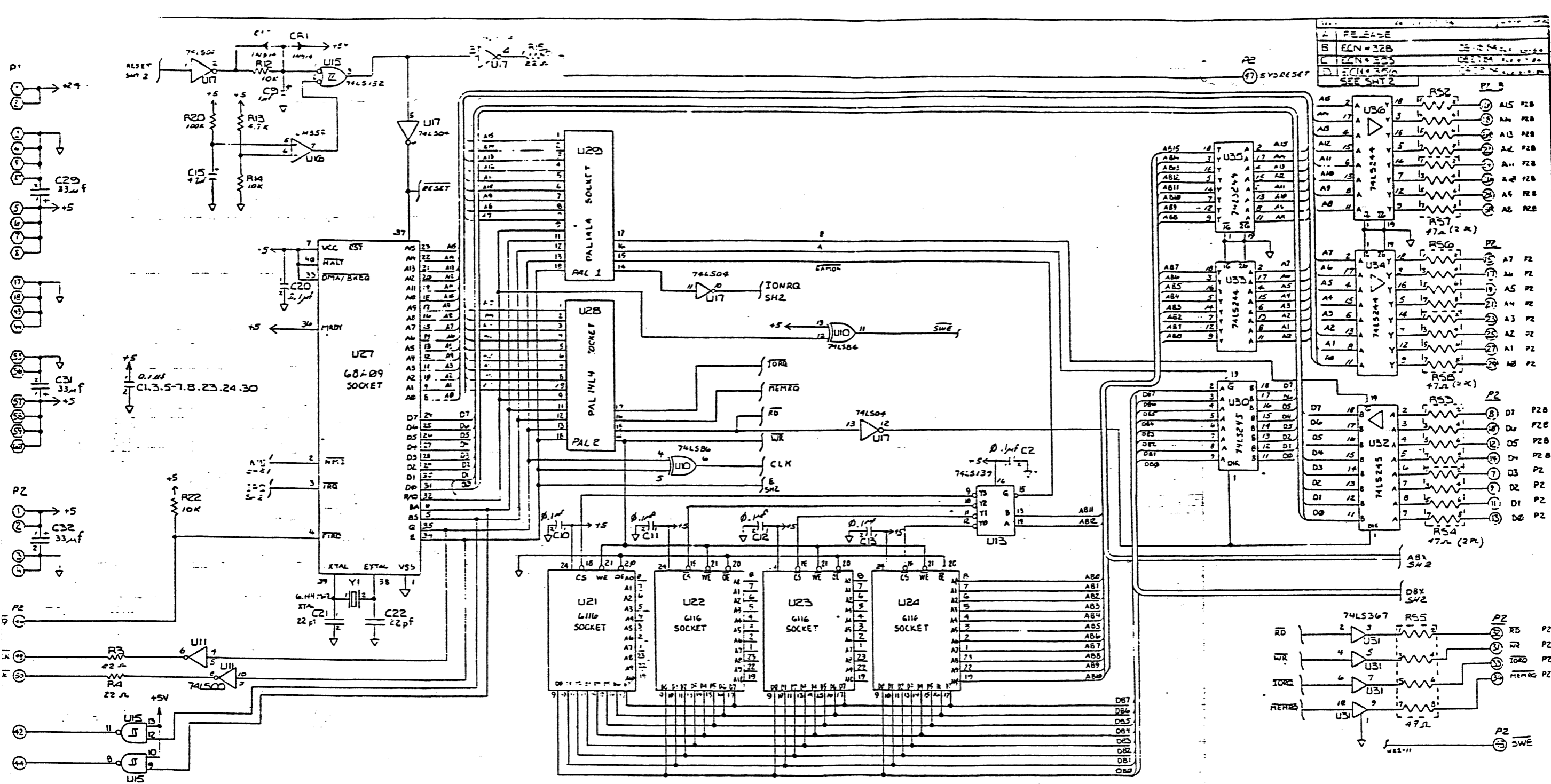
23	9	21
14	20	11
2	7	
18	24	12
+	5	
8	6	



JUN 16 1986
MAR 15 1985
APPLIED MICROSYSTEMS Corporation
11003 118th Pl. NE, Kirkland WA 98033

SCHMATIC-TRACE & BREAK-ES

DESIGN	DATE	6/20/81	700-10709-50
CHECK	DATE	3-11-85	
APPROV	DATE	7/1/81	



RELEASE
B ECN # 32B
C ECN # 333
D ECN # 334
SEE SHT 2

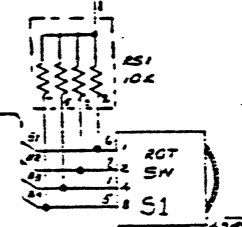
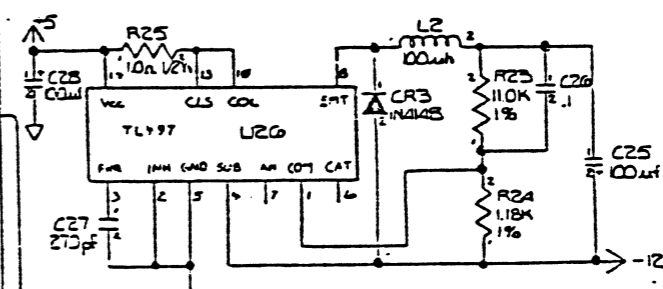
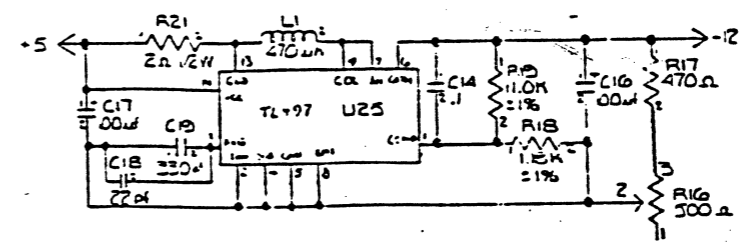
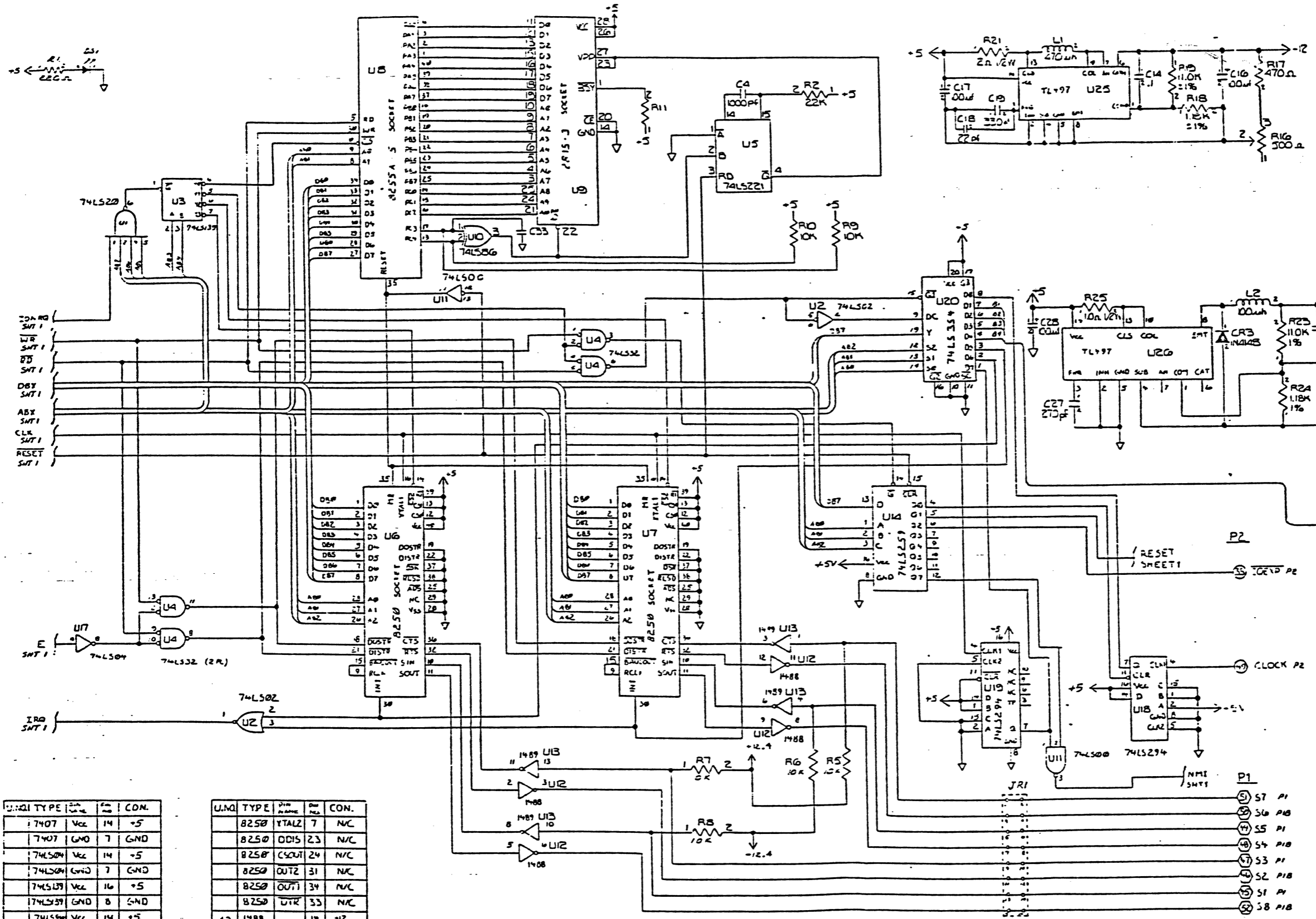
JUN 16 1986
MAR 15 1985

APPLIED MICROSYSTEMS
Corporation

11003 118th Pl. NE, Kirkland WA 98033

SCHEMATIC - UNIVERSAL CONTROLLER

700-10853-02



U.NO.	TYPE	Pin No.	CON.
1	7407	Vcc	14 +5
2	7407	GND	7 GND
3	74LS04	Vcc	14 +5
4	74LS04	GND	7 GND
5	74LS139	Vcc	16 +5
6	74LS139	GND	8 GND
7	74LS139	Vcc	14 +5
8	74LS139	GND	7 GND
9	74LS20	Vcc	14 +5
10	74LS20	GND	7 GND
11	1489	14	+5
12	1489	7	GND

U.NO.	TYPE	Pin No.	CON.
1	8250	ITALZ	7 N/C
2	8250	ODIS	23 N/C
3	8250	CSOUT	24 N/C
4	8250	OUT2	31 N/C
5	8250	OUT1	34 N/C
6	8250	UTR	33 N/C
7	1488	14	+5
8	1488	1	-12
9	1488	13	N/C
10	1488	10	N/C
11	1488	7	N/C
12	1489	12	N/C
13	1489	9	N/C
14	1489	5	N/C
15	1489	2	N/C

JUN 16 1986
 MAR 15 1985

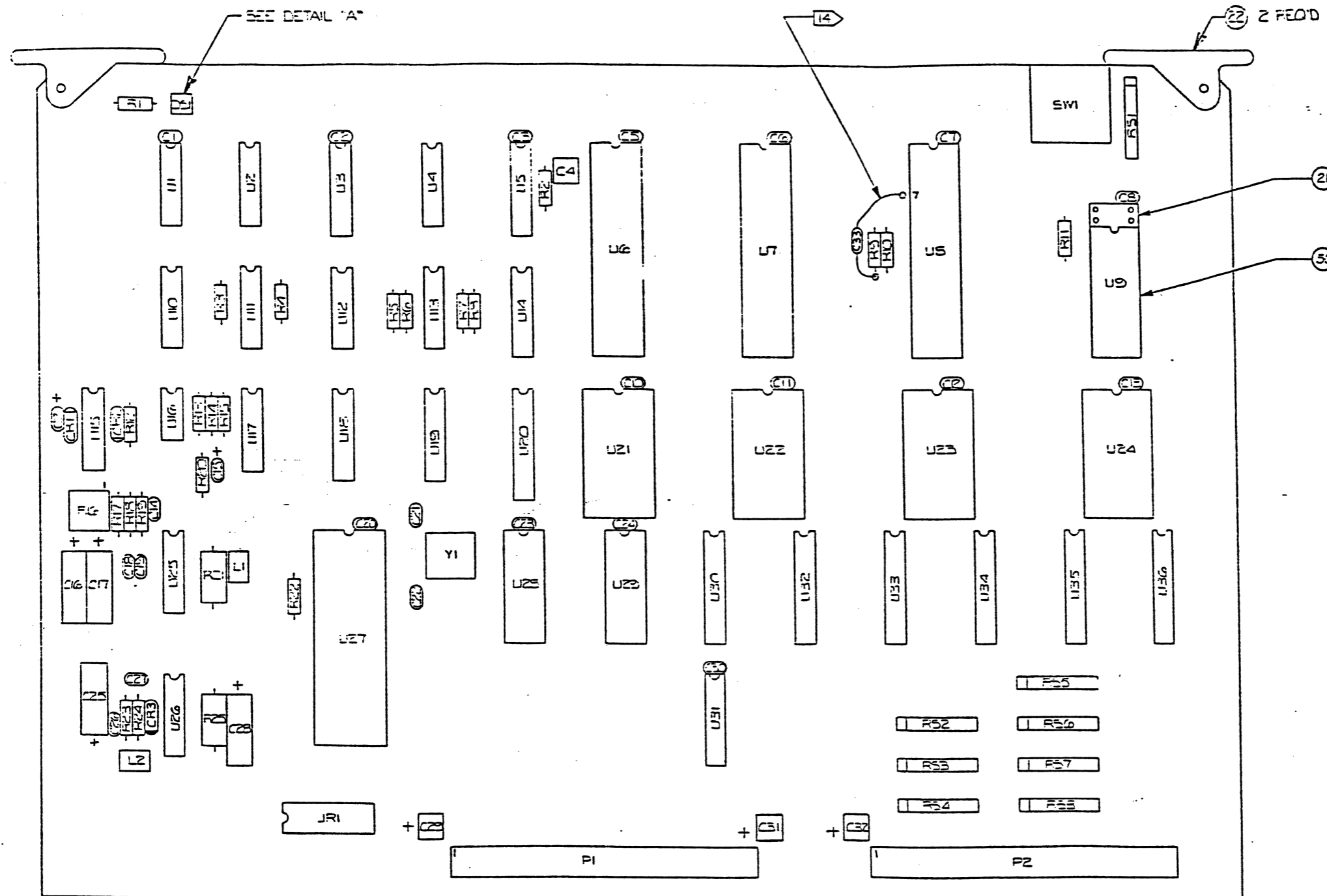
APPLIED MICROSYSTEMS
 Corporation

11003 118th PL. NE, Kirkland WA 98033

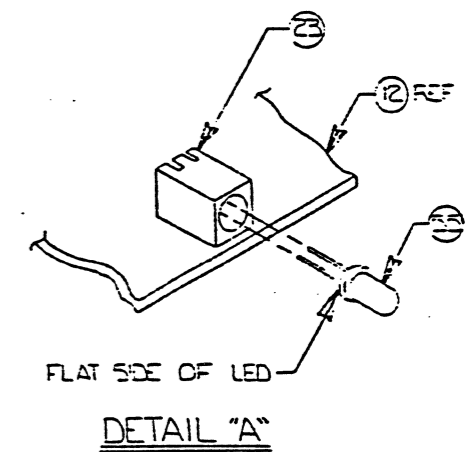
SCHEMATIC - UNIVERSAL CONTROLLER

DATE	BY	SCALE	SHEET	TOTAL
TCL	2/2/84		2	2
700-10853-02				

REVISIONS			
ZONE	LTR	DESCRIPTION	DR / CHN / APPD / DATE
	G	ECN # 856 FOR REV F SEE HISTORY FILE	ME / JB / 12/85
	H	CHANGE CONNECTIONS	ME / JB / 12/85
	H	ECN # 855	ME / JB / 12/85
	J	ECN # 784	ME / JB / 12/85
	K	ECN # 856	ME / JB / 12/85



21 (28 PIN) (SOCKET REF.)
 59 (LOCATE ON LOWER PORTION OF SOCKET) (24 PIN IC REF.)



JUN 16 1985

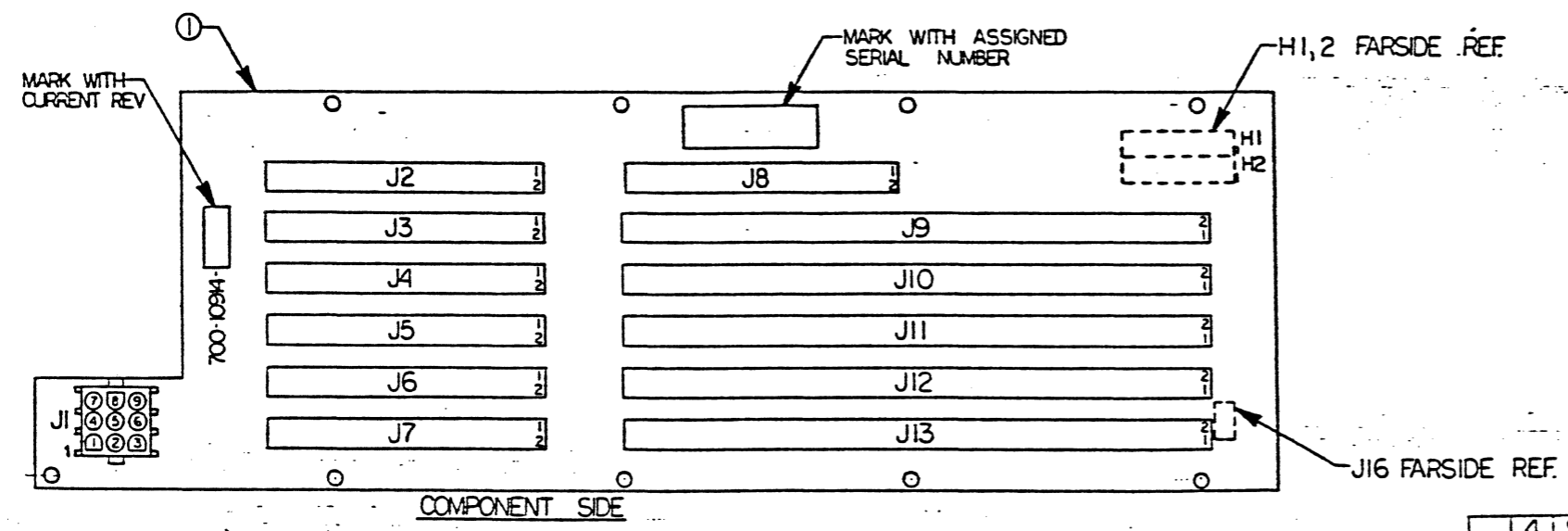
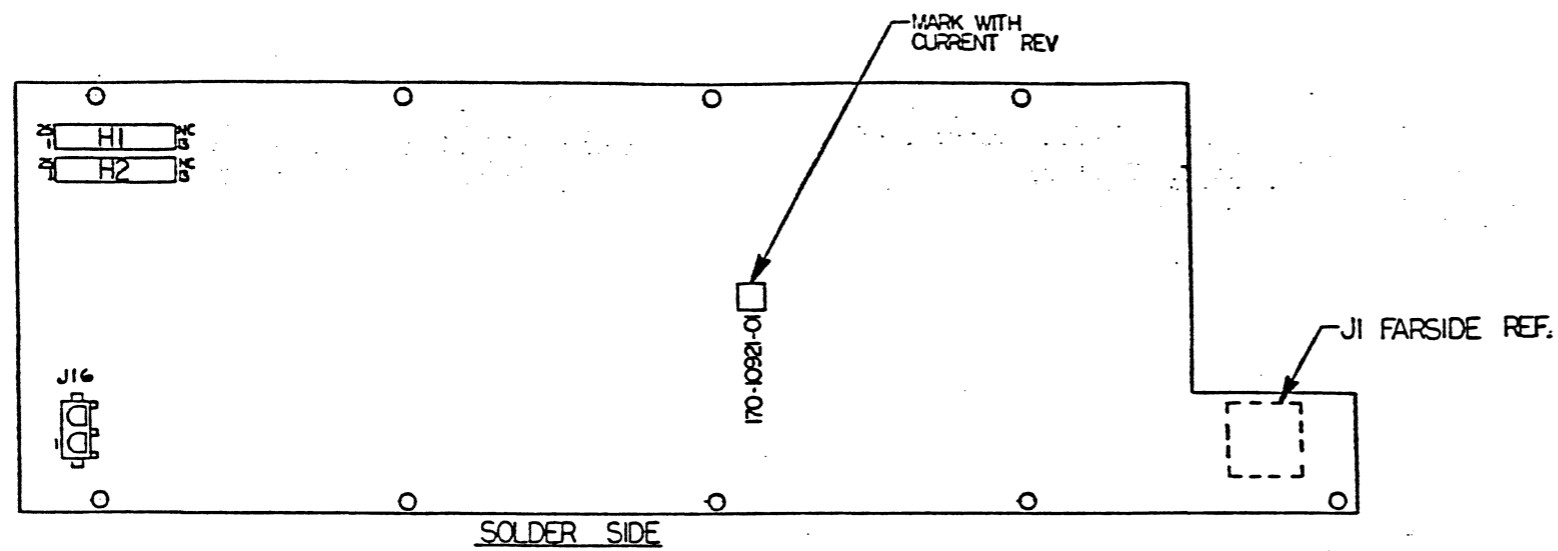
SEE M.I.S FOR PARTS LIST

7. U15 PIN 12 TO U27 PIN 5
 6. U15 PIN 9 TO U27 PIN 6
 5. U15 PINS 10 AND 13 TO U15 PIN 14
 WIRE THE FOLLOWING WITH 30 AWG KYNAR WIRE:
 4. CUT TRACE TO P2 PIN 60 ON SOLDER SIDE
 3. CUT TRACE TO P2 PIN 58 ON SOLDER SIDE
 2. CUT TRACE TO P2 PIN 59 ON COMPONENT SIDE
 1. CUT TRACE TO P2 PIN 57 ON COMPONENT SIDE
- NOTES:

16. LARGE TRACE TO R5 (-12V) MUST BE CUT LOOSE. THIS END OF R5 MUST BE WIRED TO THE LARGE TRACE RUNNING TO R6. (+12V) WITH 22 AWG BUS WIRE.
 15. ADD WIRE FROM (-) SIDE OF C25 TO P2 PINS 55 & 56.
 14. ADD 33PF CAP (C33) FROM R9 (SIDE CLOSEST TO U8 PIN 15) TO U8 PIN 7.
 13. U12 PIN 7 TO U3 PIN 8
 12. U10 PIN 11 TO P2 PIN 43
 11. U10 PIN 12 TO U27 PIN 32
 10. U10 PIN 13 TO U10 PIN 14
 9. U15 PIN 11 TO P2 PIN 42
 8. U15 PIN 8 TO P2 PIN 44

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: LIN .X-± .XXX+± IN .XX-± .ANG+± ALL DIM. AFTER PLATING BREAK ALL SHARP EDGES REMOVE ALL BURRS	APPROVED	DATE	APPLIED MICROSYSTEMS CORPORATION
	DWN	12/85	
	CHK	12/85	
	PROJECT ENG		
	ME		
QC			DESCRIPTION ASSY - UNIVERSAL CONTROLLER
ENG MGR			SIZE DWG NO. D 700-0533-02
DO NOT SCALE DRAWING			SCALE 1:1

REVISIONS					
ZONE	LTR	DESCRIPTION	DR	CHK	APPR DATE
	F	ECN # 803	MEJ	SEN	6/15/86



JUN 16 1986

SPECIFICATION CONTROL DRAWING

ITEM	PART NUMBER	DESCRIPTION	REF DES.
4	913-1000-02-05-099	CONTACT STRIP, CUT TO SIZE	H1,2
5	8101-1562-10-01-025	INSULATOR, OEO	J9-13
5	7101-1562-10-01-018	INSULATOR, OEO	J9-13
10	643-1562-02-07-077	CONTACT STRIP	J9-13
7	501-1001-12-02-030	INSULATOR	J2-8
14	430-1002-02-07-077	CONTACT STRIP	J2-8
1	3350432-1	CONN - POWER, 9-PIN	J1
1	2350428-1	CONN - POWER, 2-PIN	J16
1	170-10921-01	PWB-ES MOTHER BOARD	

-00	CONNECTOR TECH INC (CTI) ANAHEIM, CA. 92806	700-10914-00	ES MOTHER BOARD
DASH NO	SUPPLIER CODE IDENT NO.	SUPPLIER PART IDENT NO.	APPLICATION
SUGGESTED SOURCE(S) OF SUPPLY			

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
LIN .X± .XXX±
 XX± ANG±
ALL DIM. AFTER PLATING
BREAK ALL SHARP EDGES
REMOVE ALL BURRS

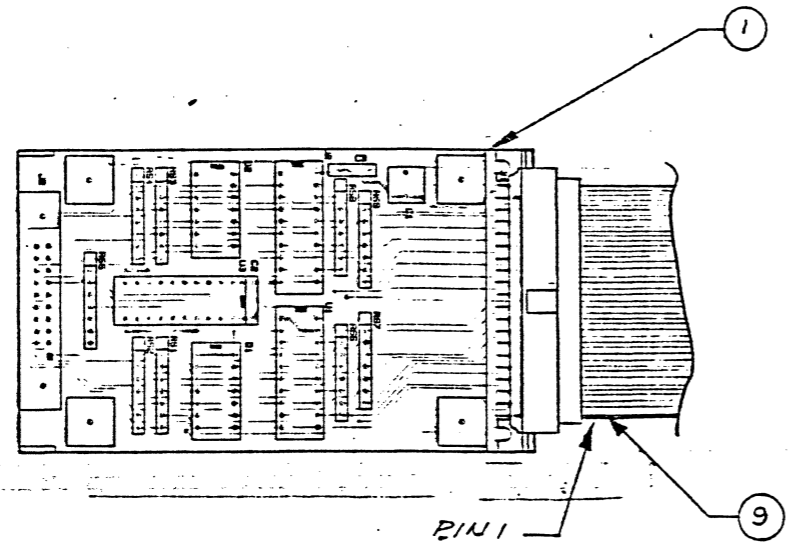
APPROVED: DWG ILEANA 6/25/86
CHK: MEJ 7/14/86
PROJECT ENG: ME P. BATES 7/15/86
OC: [Signature] 7/15/86
ENG MGR: [Signature]

APPLIED MICROSYSTEMS
DESCRIPTION: PCB ASSEMBLY ES MOTHER BOARD
SIZE: D DWG NO: 700-10914-00 REV: F
SCALE: NONE SHEET: 1 OF 1

DO NOT SCALE DRAWING

NOTES: UNLESS OTHERWISE SPECIFIED.

REV	DESCRIPTION	DATE
1	PROTOTYPE	
2	NO. HEADERS PL C03E	
3	PROD. REL.	7/25/82
4	ADDITIONAL CABLE	5/83



QTY	DASH NO.	ITEM NO.	PART NUMBER	DESCRIPTION	REF DES/VENDOR
				PCB- LOGIC STATE PROBE	
1	9		600-10192	CABLE ASSY 40 CONN. 41"	
1	8		210-11116	CONN-HEADER, 20 PIN MALE	J2
1	7		210-10297	CONN-HEADER, 40 PIN MALE	J1
2	6		430-10708	DIPDE- FSA 2501	D1,2
2	5		150-10372	CAP-.1 MFD 50V DIP	C2,3
1	4		150-10091	CAP-55MFD 50V TANT	C1
3	3		314-10069	IC-74LS244,	U1-3
9	2		470-10351	RES SIP- 22 OHM	R51-9
1	1		170-11098-01	PWB- LOGIC STATE PROBE	
				PCB- LOGIC STATE PROBE	
QTY/DASH NO.	ITEM NO.	PART NUMBER	DESCRIPTION	REF DES/VENDOR	

JUN 16 1982

APPLIED MICROSYSTEMS
 Corporation
 11003 118th Pl. NE, Kirkland WA 98033

PCB ASSY-
 LOGIC STATE PROBE

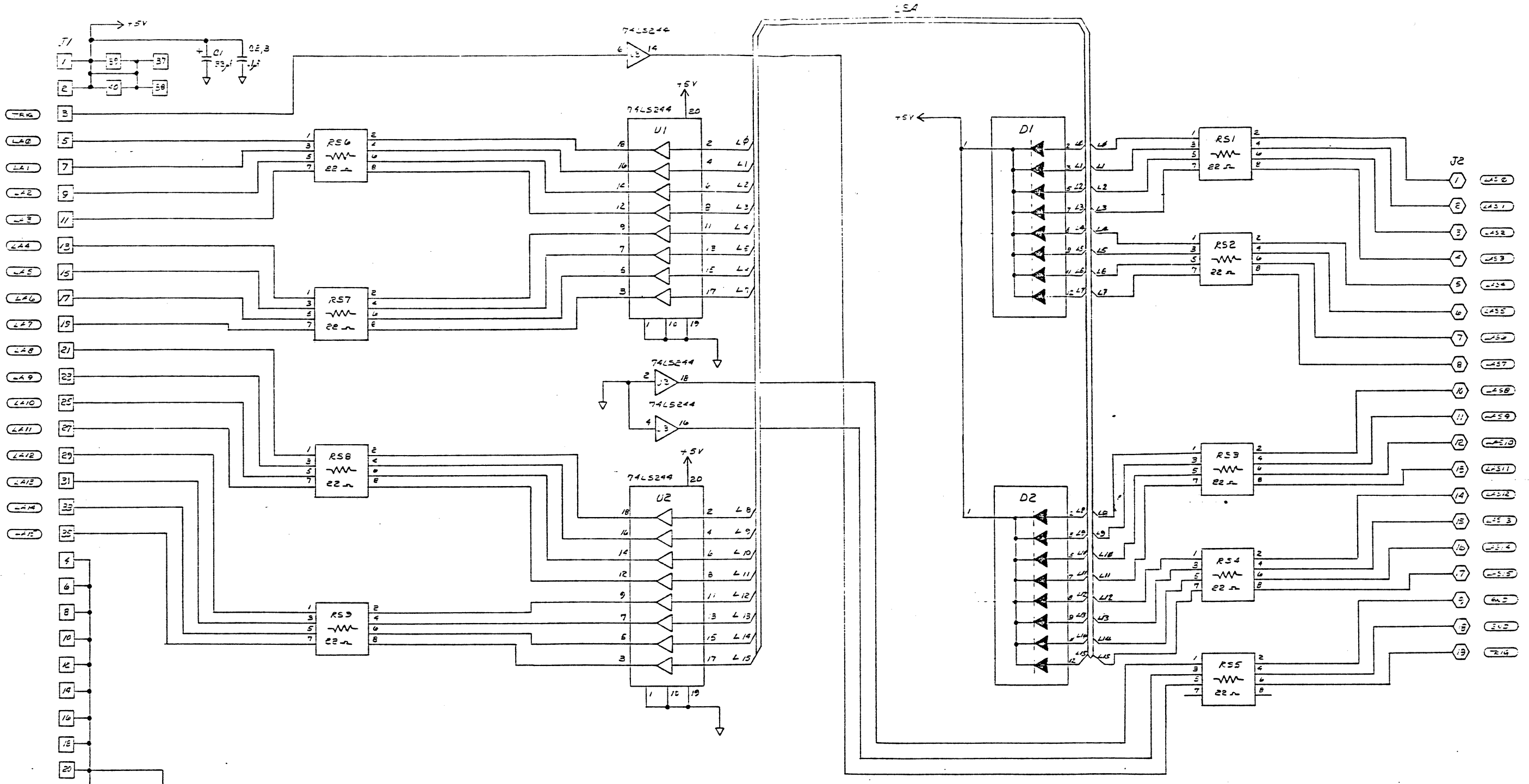
RELEASE STATUS		700-11099-PL
DRAWN MW	7/6/82	
CHECK JMS	9-2-82	
APPR. WR	4-10-82	
SCALE 1/1	REV A	SMT. 1 OF 1

NEXT USED ON: 900-10841

WR 3-18-82
 SC 3-18-83

PRODUCTION

REV.	DESCRIPTION
1	PROTOTYPE
2	ADDED SYMBOLS
3	REVISED



NOTES:
UNUSED GATES OF U3-8, 11, 13, 15, 17 ARE TIED TO GND.

JUN 16 1986

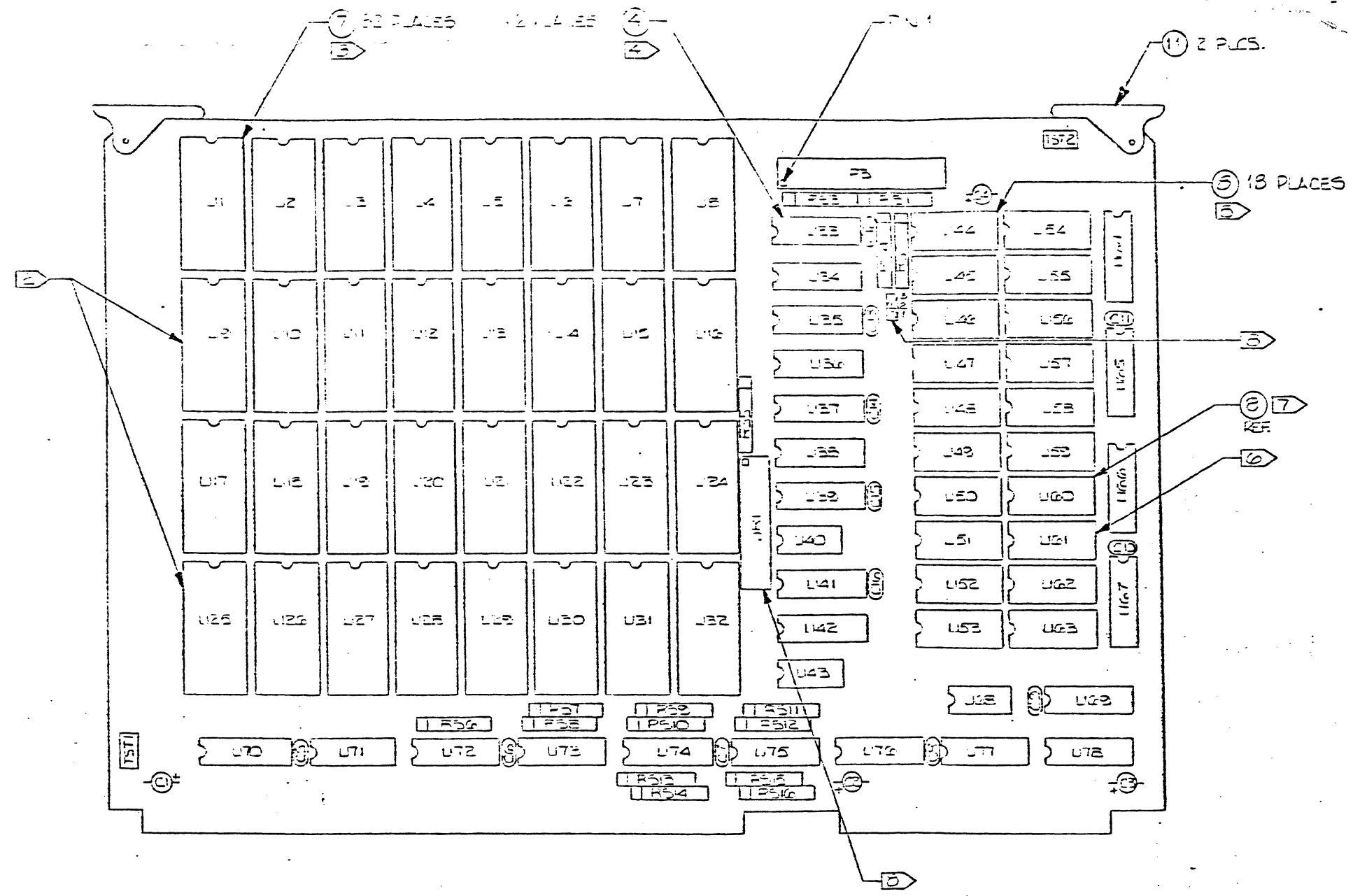
APPLIED MICROSYSTEMS
Corporation
11003 118th Pl. NE, Kirkland WA 98033

SCHEMATIC- LOGIC STATE PROBES	
RELEASE STATUS	700-039-SC
DRAWN: WR	DATE: 6/10/82
CHECKED: WR	DATE: 6/10/82
APPROVED: WR	DATE: 6/10/82

NEXT USED ON: 900-10241

PRODUCTION

REV	DATE	BY	CHK



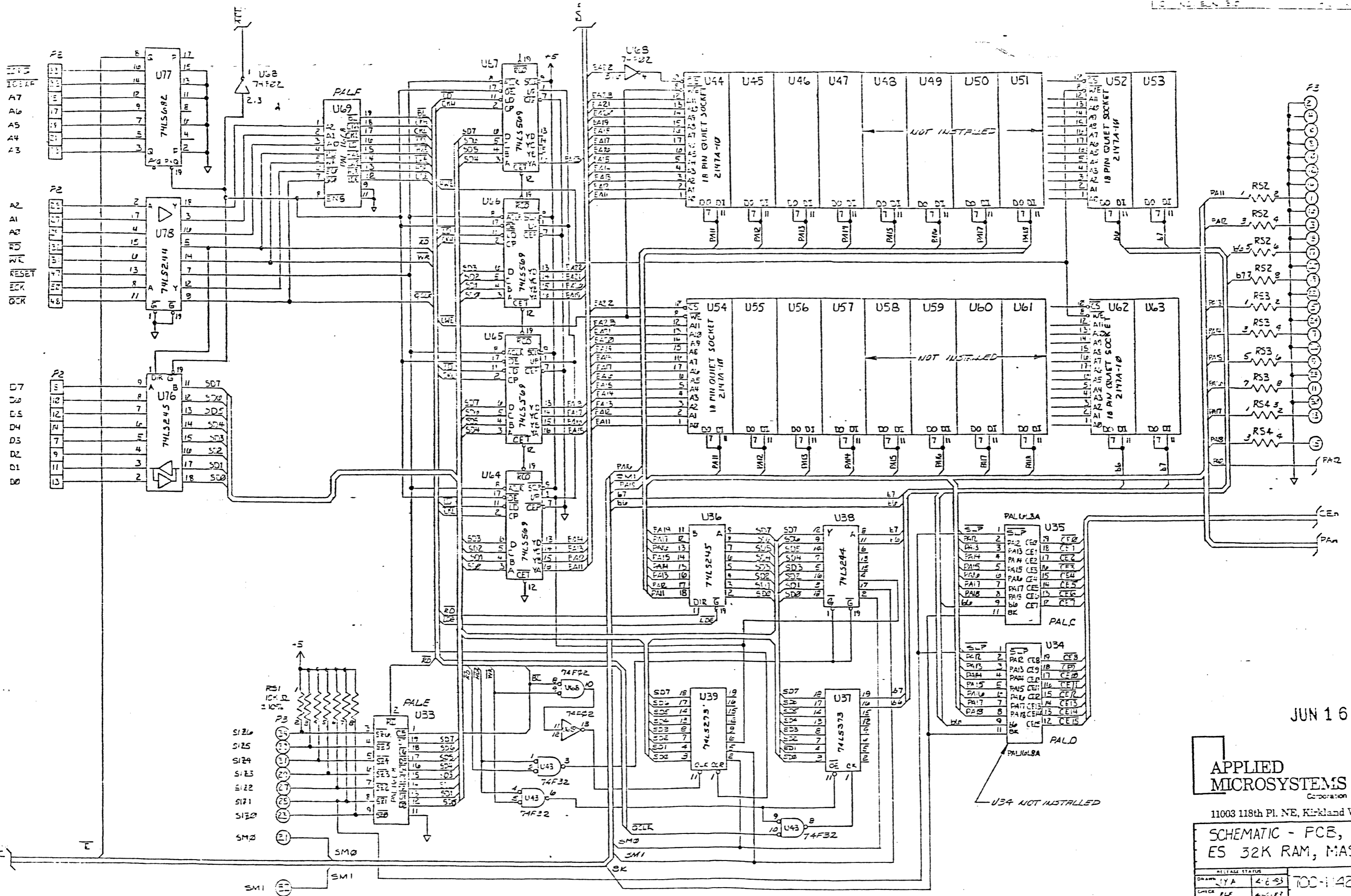
- 5 INSTALL SHUNTS, ITEM 6 :
 U21, PINS: 8-6
 U22, PINS: 1-2
 9-10
 13-14
 17-18
 19-20
 23-24
- 7 INSTALL SOCKETS ONLY IN LOCATION U30 & U60.
- 6 U51 AND U51 NOT INSTALLED.
- 5 INSTALL ITEM 5, 18 PIN SOCKET: U44-U50, U52-U60, U62, U63.
- 4 INSTALL ITEM 4, 20 PIN SOCKET: U33-U35, U41, U42, U49.
- 3 INSTALL ITEM 7, 28 PIN SOCKET: U1-U32.
- 2 SOCKETS INSTALL ONLY: U1-U16, U25-U32.

1. SEE M.I.S FOR PART LIST.

NOTES:

JUN 16 1986

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE LIN .XXX ± .005 .XX ± .002 ALL DIM AFTER PLATING BREAK ALL SHARP EDGES REMOVE ALL BURRS	APPROVED	DATE	APPLIED MICROSYSTEMS DESCRIPTION ASSY-ES SERIES 23K RAM OVERLAY SIZE DWS NO D 700-11275-00
	DWN	2/11/84	
	CHK	BGM 1/2/85	
	PROJECT ENG		
	ME		
	QC		
	ENG MGR		



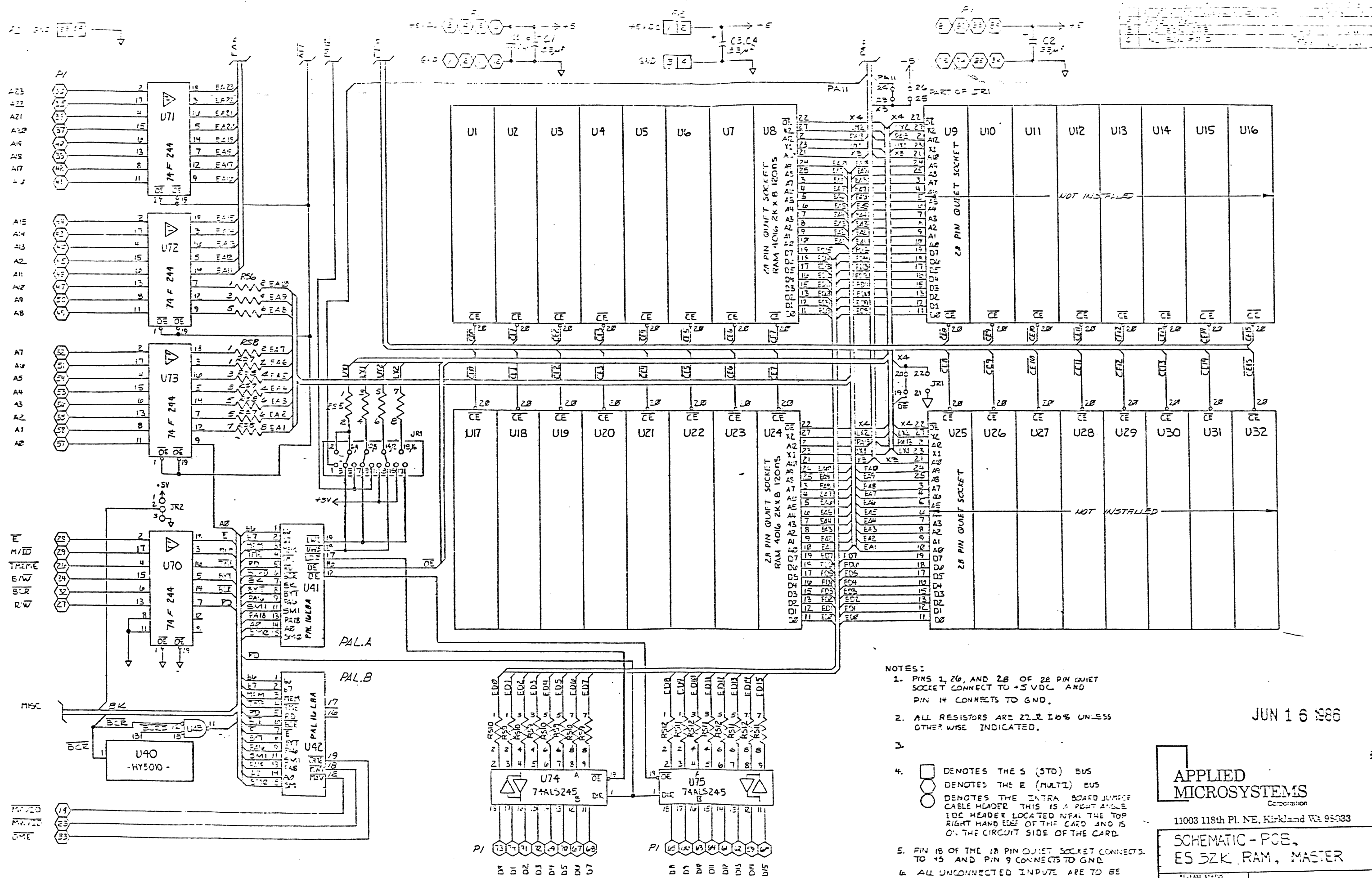
JUN 16 '86

APPLIED MICROSYSTEMS
Corporation

11003 118th Pl. NE, Kirkland WA 98033

SCHEMATIC - PCB,
ES 32K RAM, MASTER

RELEASE STATUS	
DATE	1986-06-16
BY	100-11427-00 SC
CHKD	100-11427-00 SC
APP'D	100-11427-00 SC



- NOTES:
1. PINS 1, 26, AND 28 OF 28 PIN QUIET SOCKET CONNECT TO +5 VDC AND PIN 14 CONNECTS TO GND.
 2. ALL RESISTORS ARE 22Ω 10% UNLESS OTHERWISE INDICATED.
 - 3.
 4. □ DENOTES THE S (STD) BUS
○ DENOTES THE E (MULTI) BUS
○ DENOTES THE INTRA BOARD JUMPER CABLE HEADER THIS IS A RIGHT ANGLE IDC HEADER LOCATED NEAR THE TOP RIGHT HAND EDGE OF THE CARD AND IS 0'. THE CIRCUIT SIDE OF THE CARD.
 5. PIN 18 OF THE 18 PIN QUIET SOCKET CONNECTS TO 15 AND PIN 9 CONNECTS TO GND.
 6. ALL UNCONNECTED INPUTS ARE TO BE GROUNDING.

JUN 16 1986

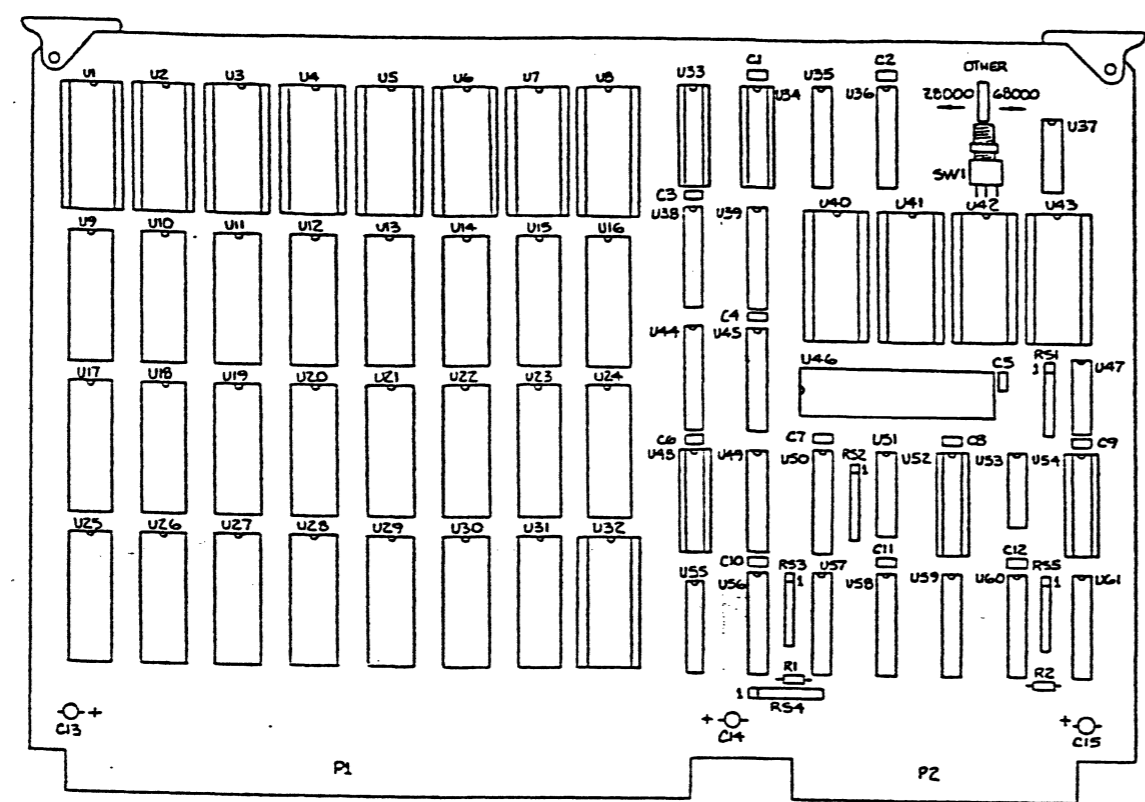
APPLIED MICROSYSTEMS Corporation
 11003 118th Pl. NE, Kirkland WA 98033

SCHEMATIC - PCB,
 ES 32K RAM, MASTER

RELEASE STATUS	
DATE	11/13/86
BY	JL
CHECKED	JL
APP'D	JL

700-1427-00 50

REVISIONS						
ZONE	LTR	DESCRIPTION	DR	CHK	APPR	DATE
A		RELEASE	2-2-84	TCC		
B		ECN # 375	10-3-84	DB		
C		ECN # 387	3-28-84	DB		
D		ECN # 427	6-2-84	TCC		
E		ECN # 495	11-9-84	DB		
-		ECN # 561	3-12-85	MEJ		

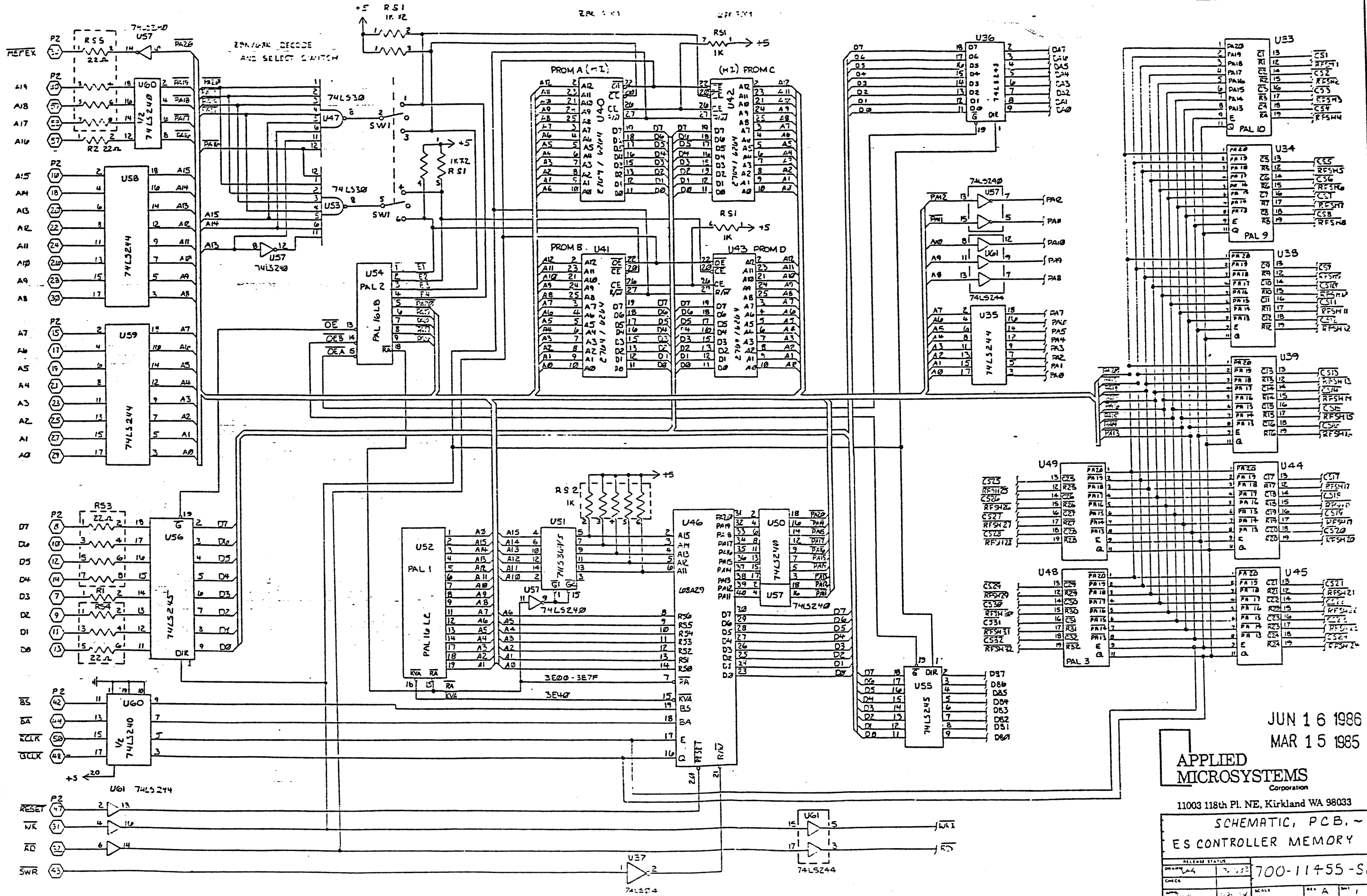


-04 SHOWN

- NOTES:
1. -00, -02, -04 VERSION IS WITH SYMBOLIC DEBUG
 2. -01, -03, -05 VERSION IS WITHOUT SYMBOLIC DEBUG
 3. REFER TO COMPUTER PARTS LISTS 700-11455-00 THRU -05 FOR BILL OF MATERIALS
 5. CUT TRACE FROM P2-37 TO U38-1.
 6. ADD JUMPER FROM U38-1 TO P2-43. } REWORK FOR -01 ONLY

JUN 16 1986
MAR 19 1985

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: LIN .X± .XXX± .XX± .ANG± ALL DIM. AFTER PLATING BREAK ALL SHARP EDGES REMOVE ALL BURRS	APPROVED	DATE	APPLIED MICROSYSTEMS Corporation
	DWN T.CONNERTON	9-23-83	
	CHK		
	PROJECT ENG	11/2/84	
NOTICE: APPLIED MICROSYSTEMS CLAIMS PROPRIETARY RIGHTS IN THE INFORMATION DISCLOSED ON THIS DRAWING. IT IS ISSUED IN CONFIDENCE FOR ENGINEERING INFORMATION ONLY AND MAY NOT IN WHOLE OR IN PART BE USED TO MANUFACTURE ANYTHING WHETHER OR NOT SHOWN HEREON REPRODUCED OR DISCLOSED TO ANYONE WITHOUT DIRECT WRITTEN PERMISSION FROM APPLIED MICROSYSTEMS CORP.	ME	1/2/85	DESCRIPTION ASSEMBLY - CONTROLLER MEMORY BOARD, E.S.
	OC	4/22/84	
	ENG MGR		
DO NOT SCALE DRAWING		SCALE 1/1	SIZE DWG NO. D 700-11455-PL
			REV E



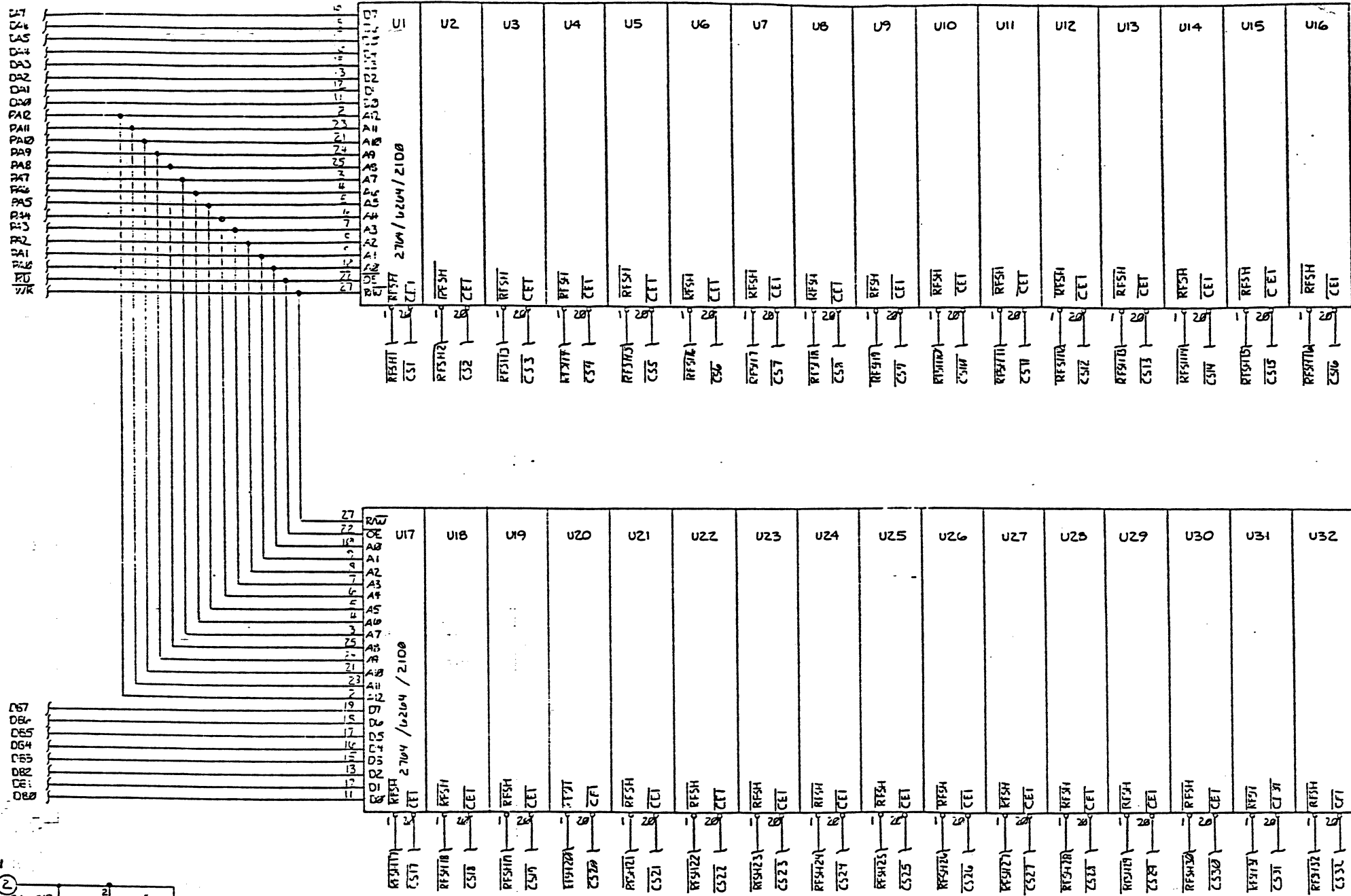
JUN 16 1986
 MAR 15 1985

APPLIED MICROSYSTEMS
 Corporation

11003 118th Pl. NE, Kirkland WA 98033

SCHMATIC, PCB. -
 ES CONTROLLER MEMORY

700-11455-SC

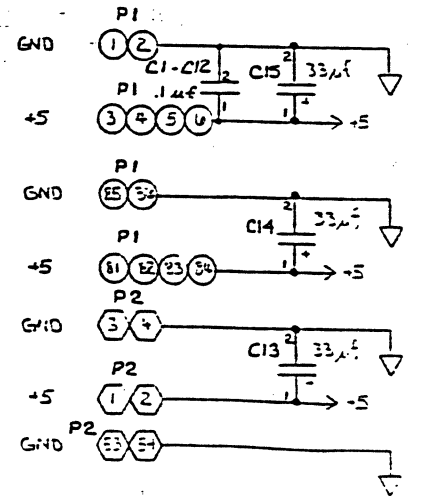
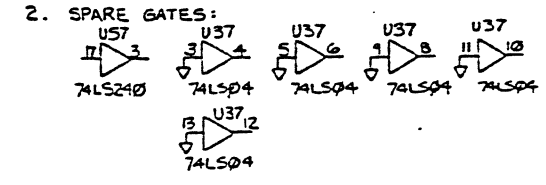


POWER AND GROUNDING INFORMATION

CHIPS	CONNECT TO +5	CONNECT TO GND
U35, 50, 50-61	20	1, 10, 11
U33, 34, 36, 38, 39, 44, 45, 46, 49, 52, 55, 56	20	10
U47, 53	14	7
U54	20	10
U51	10	8
U46	22	1
U57	20	1, 10, 15, 17
U40-43	28, 1, 26	14
U1-32	25, 20	14
U37	14	7, 3, 5, 9, 11, 13

NOTES:

- STANDS FOR THE S BUS. (P2)
 STANDS FOR THE E BUS. (P1)



JUN 16 1986
MAR 15 1985

APPLIED
MICROSYSTEMS
Corporation

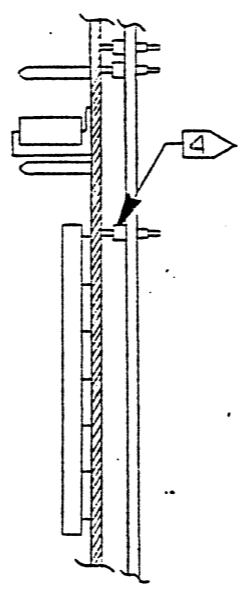
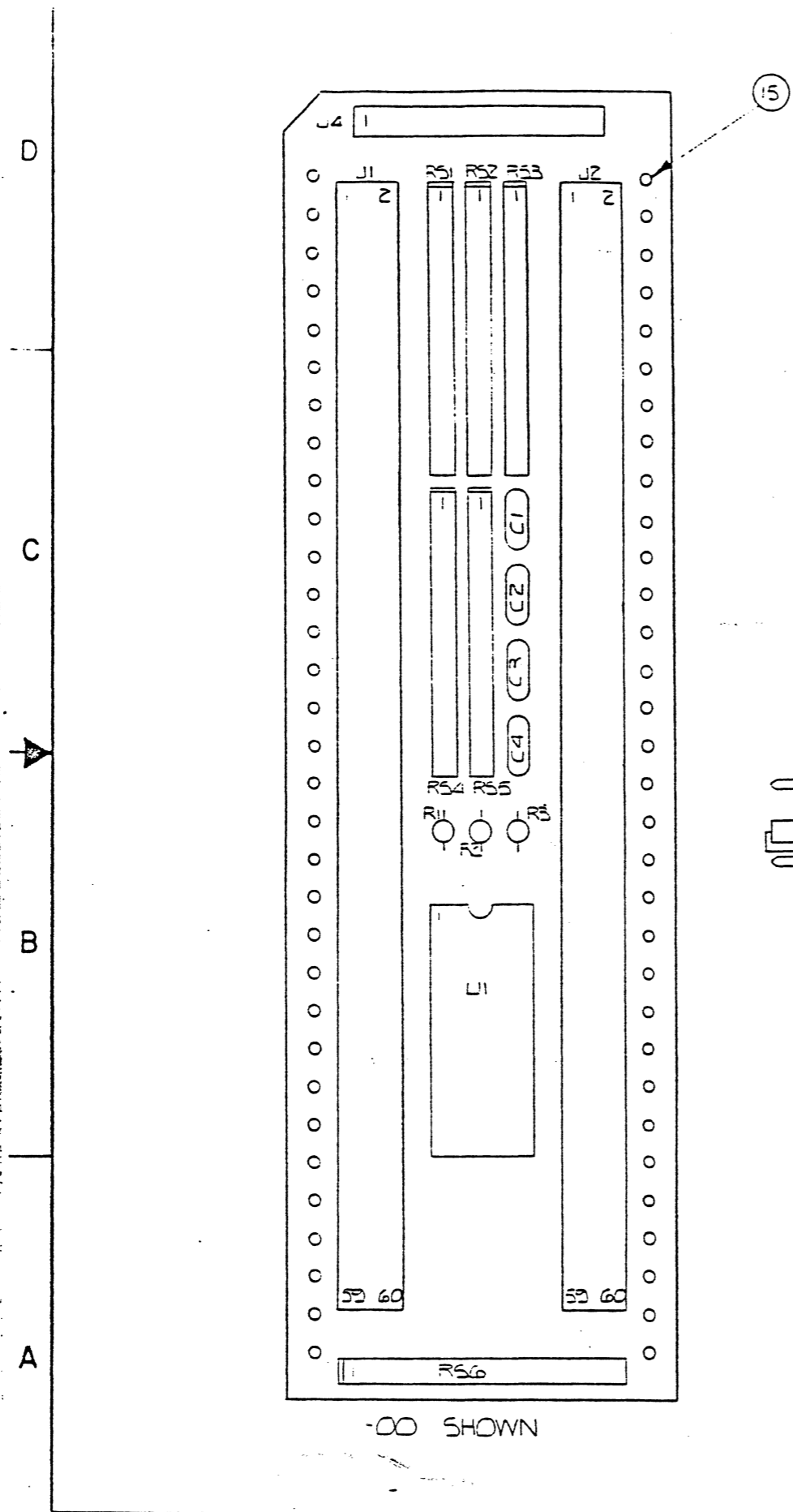
11003 118th Pl. NE, Kirkland WA 98033

SCHMATIC, PCB, -
ES CONTROLLER MEMORY

RELEASE STATUS		700-11455-SC	
DRAWN	DATE	SCALE	REV
CHECK			

Handwritten signature and date

PRODUCTION RELEASE	IDE
B INC ECN #324	DB
DRAWING CLARIFICATION # 445	LR
ECN # 595	IDE



NOTES:

- 1 FOR 170-11468-01 BOARDS REWORK PER ECN # 324
- 2 -0. SUPERSEDES -00 PER ECN # 324
- 3 INSTALL HOLTITES FROM SOLDER SIDE
- 4 INSTALL THICK BASE OF 210-11412-00 TO PCB BOARD

JUN 19 1985

QTY/DASH	ITEM	PART NO.	DESCRIPTION	REF. DES.
		.17		
2	2	16	210-11110 CONN HEADER 60 PIN MALE	J1,2
71	71	15	210-10264 TERMINAL-HOLTITE, SMALL	
1	1	14	20-11412 ADAPTOR-IC, 64 PIN, .018/.018	
		13		
1	1	12	34-10637-00 IC 74F32	U1
		11		
4	4	10	150-10003 CAP. 0.1 MF 50V	C1-4
		9		
1	1	8	470-10688 RES. 330 OHM, 1/4W, 5%	R3
1	1	7	470-10229 RES. 75 OHM, 1/4W, 5%	R2
1	1	6	470-10472 RES. 47 OHM, 1/4W, 5%	R1
2	2	5	470-10279 RES. SIP, 75 OHM, 8 PIN	R54,6
4	4	4	470-10351 RES. SIP, 22 OHM, 8 PIN	R51,2,3,5
1	-	3	170-11468-02 PWB-PROBE TIP 68000/68010	
-	1	2	170-11468-01 PWB-PROBE TIP 68000/68010	
-	-	1	700-11468-01 PCB ASSY-PROBE TIP E.S. 68000/68010	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE LIN X ± XXX ± XX ± ANG ± ALL DIM AFTER PLATING BREAK ALL SHARP EDGES REMOVE ALL BURRS		APPROVED DWN T. CONNERTON CHK RLF	DATE 6-20-85 6-23-85	APPLIED JUN 16 1986 MICROSYSTEMS Corporation
NOTICE APPLIED MICROSYSTEMS CLAIMS PROPRIETARY RIGHTS IN THE INFORMATION DISCLOSED ON THIS DRAWING. IT IS ISSUED IN CONFIDENCE FOR ENGINEERING INFORMATION ONLY AND MAY NOT IN WHOLE OR IN PART BE USED TO MANUFACTURE ANYTHING WHETHER OR NOT SHOWN HEREON. REPRODUCED OR DISCLOSED TO ANYONE WITHOUT DIRECT WRITTEN PERMISSION FROM APPLIED MICROSYSTEMS CORP.		PROJECT ENG Jim E. Nelson ME OC ENG MGR	DATE 2-10-84 2-17-84 3-7-84 2-6-84	DESCRIPTION PCB ASSY - PROBE TIP E.S. 68000/68010
DO NOT SCALE DRAWING		SIZE C	DWG NO. 700-11468-PL	REV C

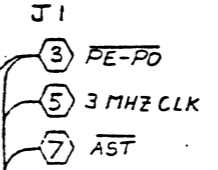
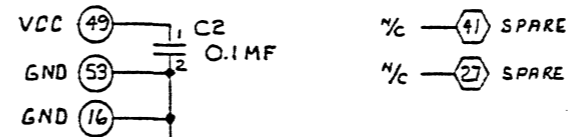
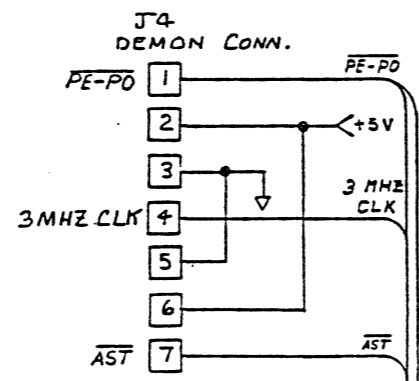
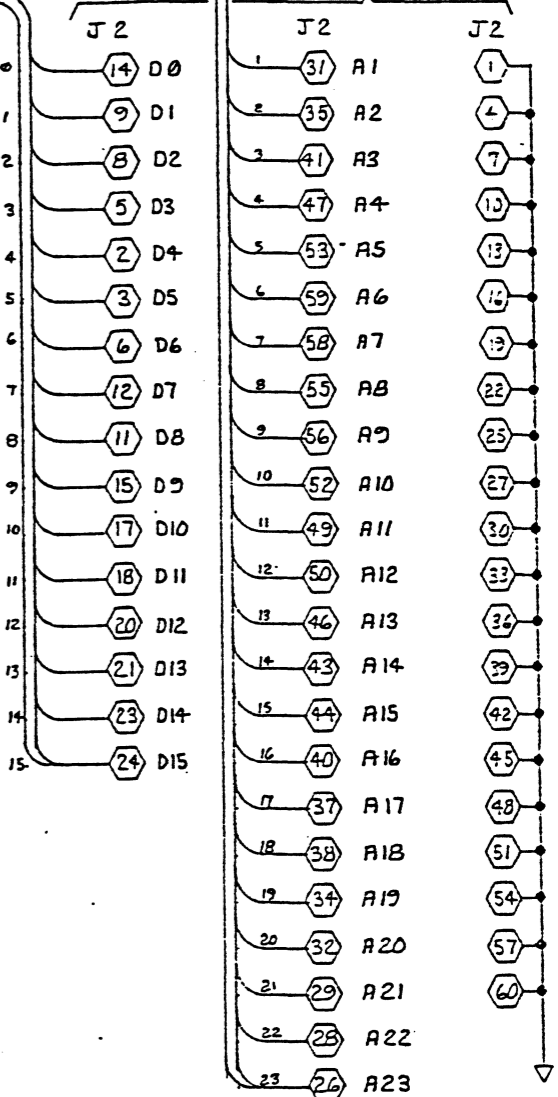
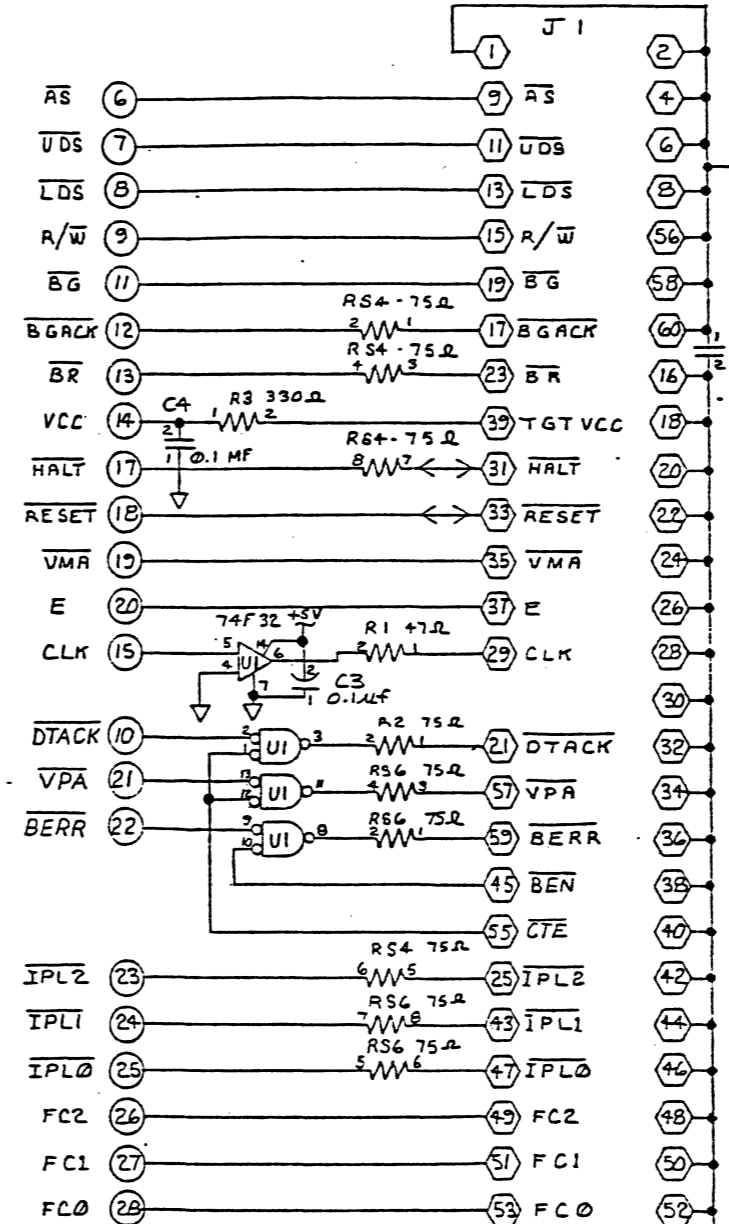
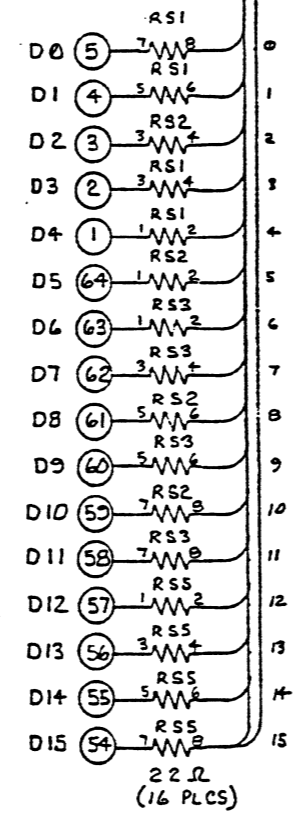
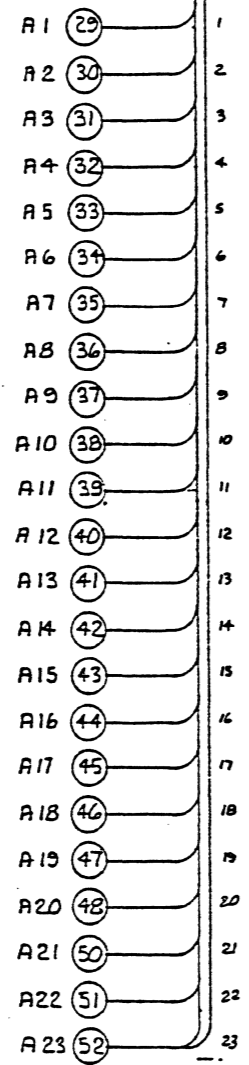


64 PIN SOCKET CONNECTIONS

J1-TO PDD (60 PIN)

REV	DESCRIPTION	APP/DATE
A	PRODUCTION RELEASE	2/1/84

J2-TO PDD (60 PIN)



JUN 16 1986
MAR 15 1985

APPLIED MICROSYSTEMS
Corporation

11003 118th Pl. NE, Kirkland WA 98033

SCHEMATIC- PROBE TIP
E.S. 68000/68010 EMUL.

RELEASE STATUS		700-11468-SC
DRAWN	RLF 4-7-87	
CHECK	JYA 4-8-83	
APPD	Jim F. Khan 2-10-84	SCALE
REV	A	SMT
QF		

H.E. & G. 2-17-84
P.D. H. B. 2-21-84

8

7

6

5

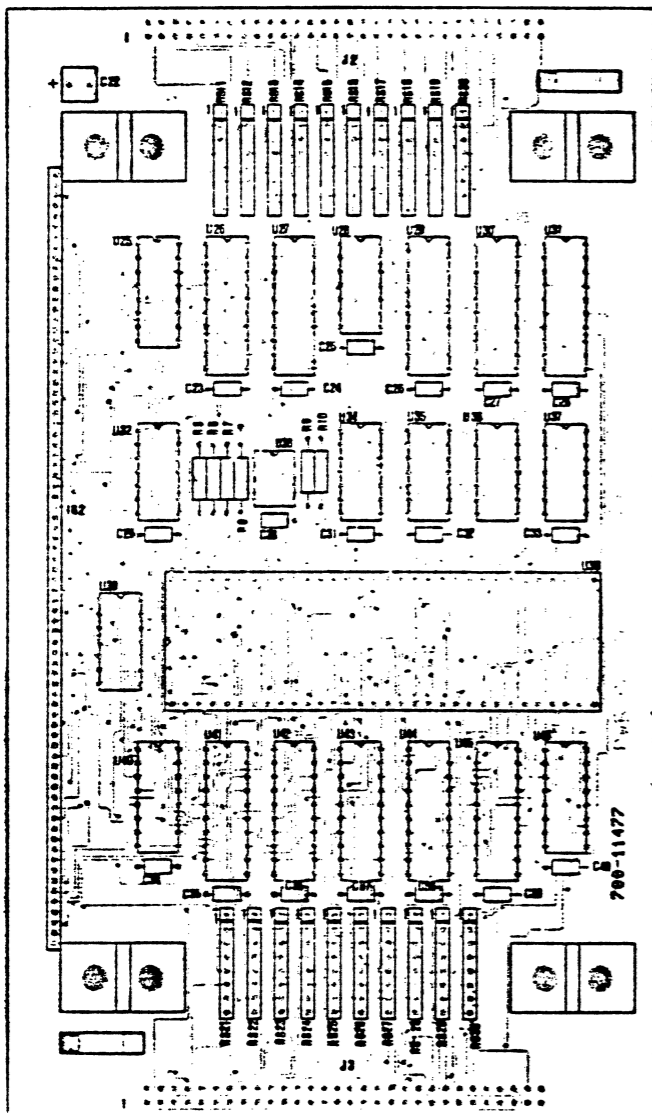
4

3

2

1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	BY
	A	PRODUCTION RELEASE		
	B	ECN # 344	10/31	
	C	ECN # 347	11/1	
	D	ECN # 439	12/1	
	E	ECN # 585	10/1	
	F	ECN # 651	12/1	



- 3. FOR PARTS LIST SEE MIS SYSTEM.
- 2. FOR 170-11477-00 B05 REWORK PER ECN #344, 347
- 1. USE -02 ASSY FOR G63010 EMULATORS.
- USE -03 ASSY FOR G63000 EMULATORS.

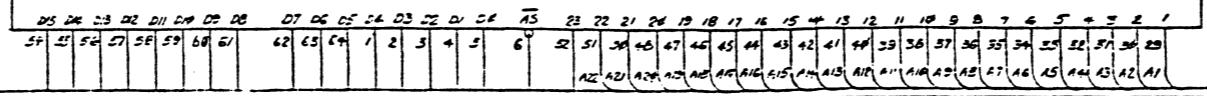
NOTES : UNLESS OTHERWISE SPECIFIED

JUN 16 1986

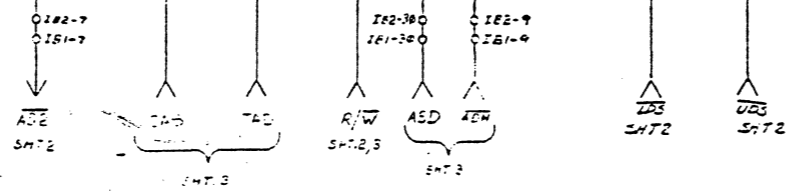
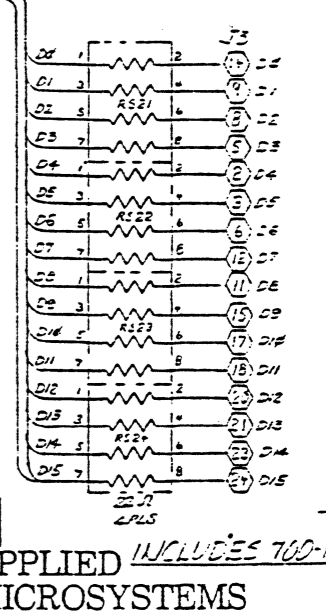
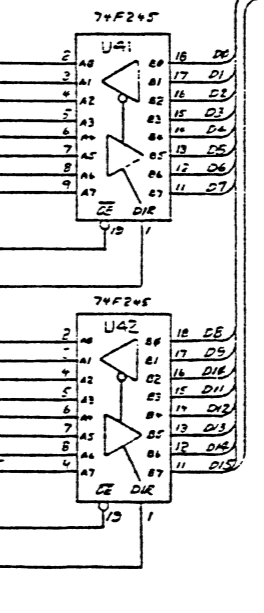
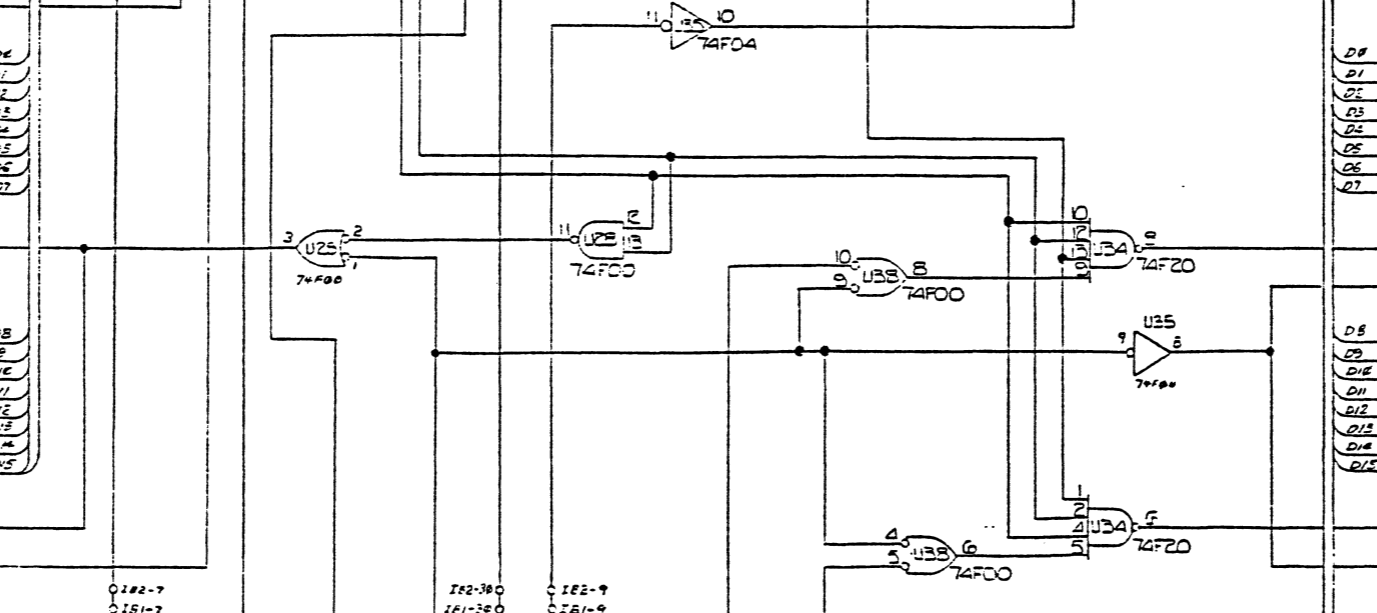
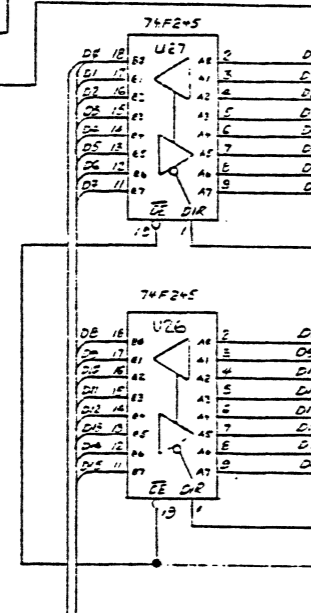
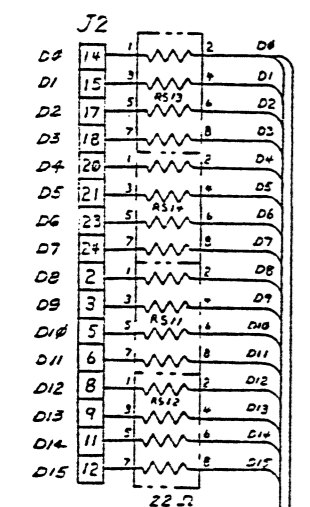
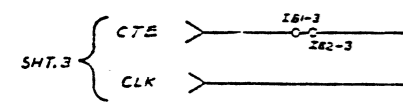
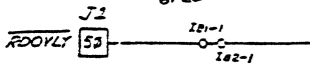
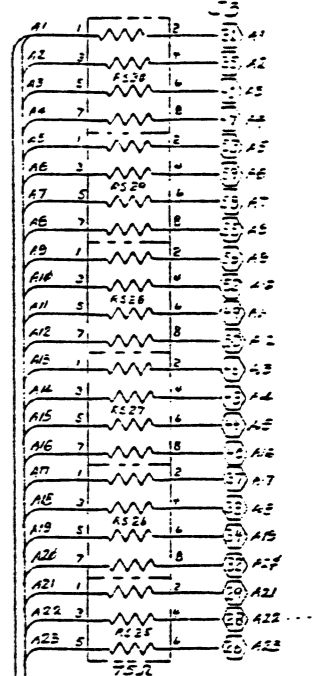
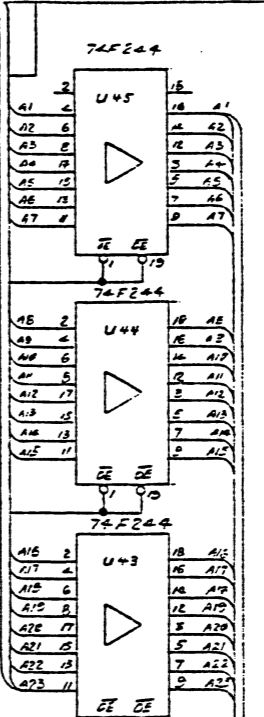
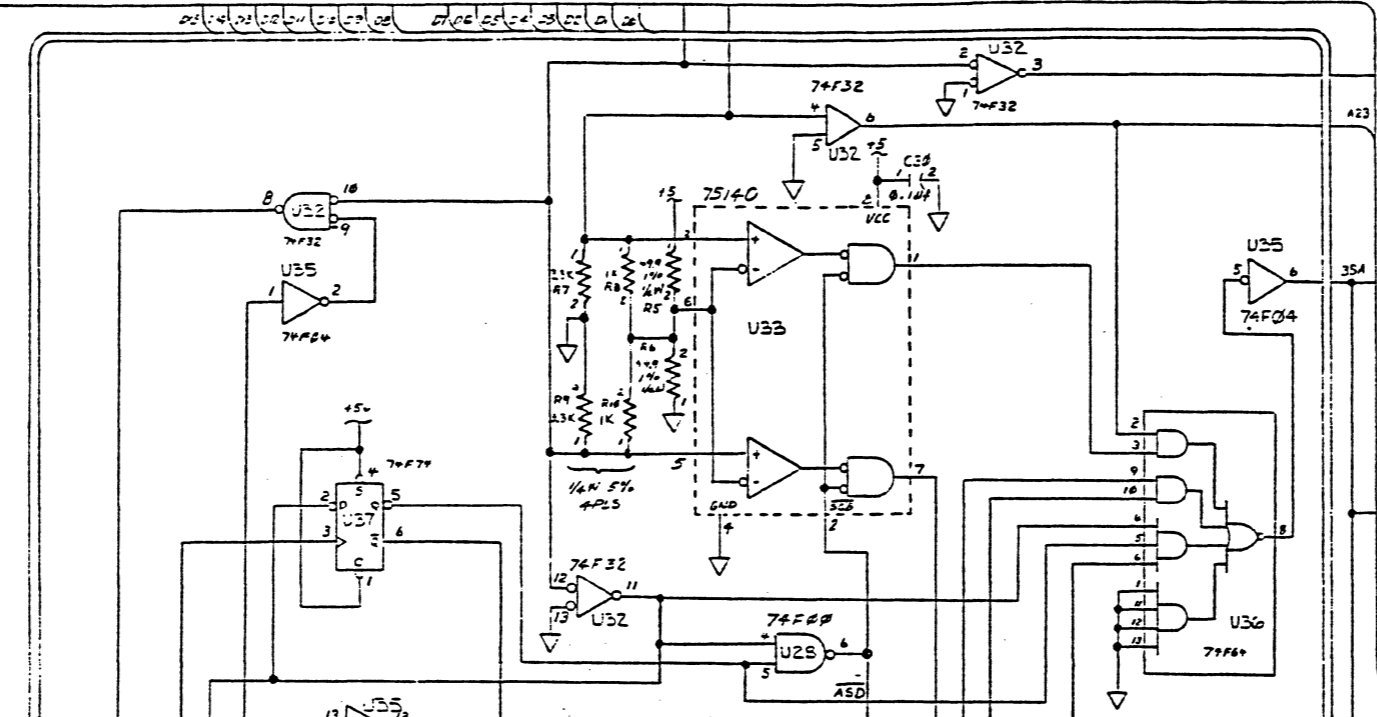
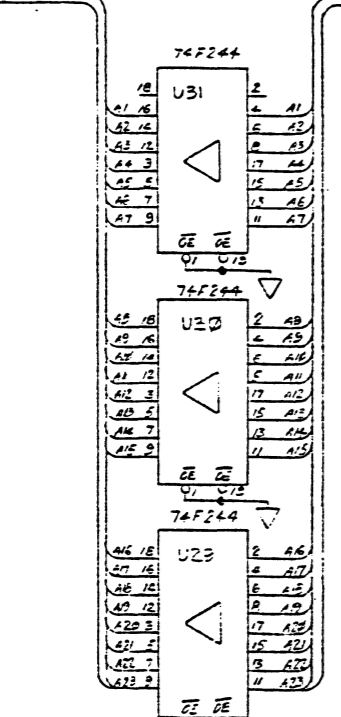
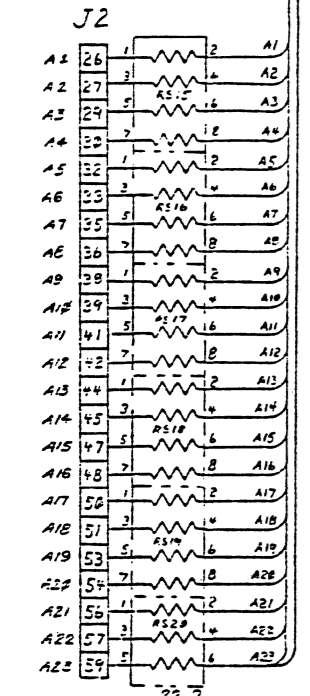
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: LW .X ± .XXX ± .XX ± .ANG ± ALL DIM AFTER PLATING BREAK ALL SHARP EDGES REMOVE ALL BURRS	APPROVED	DATE	APPLIED MICROSYSTEMS <small>Corporation</small>
	DWN ILEANA DEL BARCO	12/28/83	
	CHK		DESCRIPTION
	PROJECT ENG Jim Nelson	3-7-84	ASSEMBLY - POD G63000/10 BD # 1
ME	3-17-84	SIZE	DWG NO.
QC	2-2-84	D	700-11477-02/03
ENG MGR	3-6-84	SCALE	REV
DO NOT SCALE DRAWING			F
			SHT 1 OF 1

ECN # 734	REV	DESCRIPTION	DATE
	A	PRODUCTION RELEASE	
	B	ECN # 499	
	C	ECN # 506	

MC 68010 L12 U39



TO ENULATOR CARD



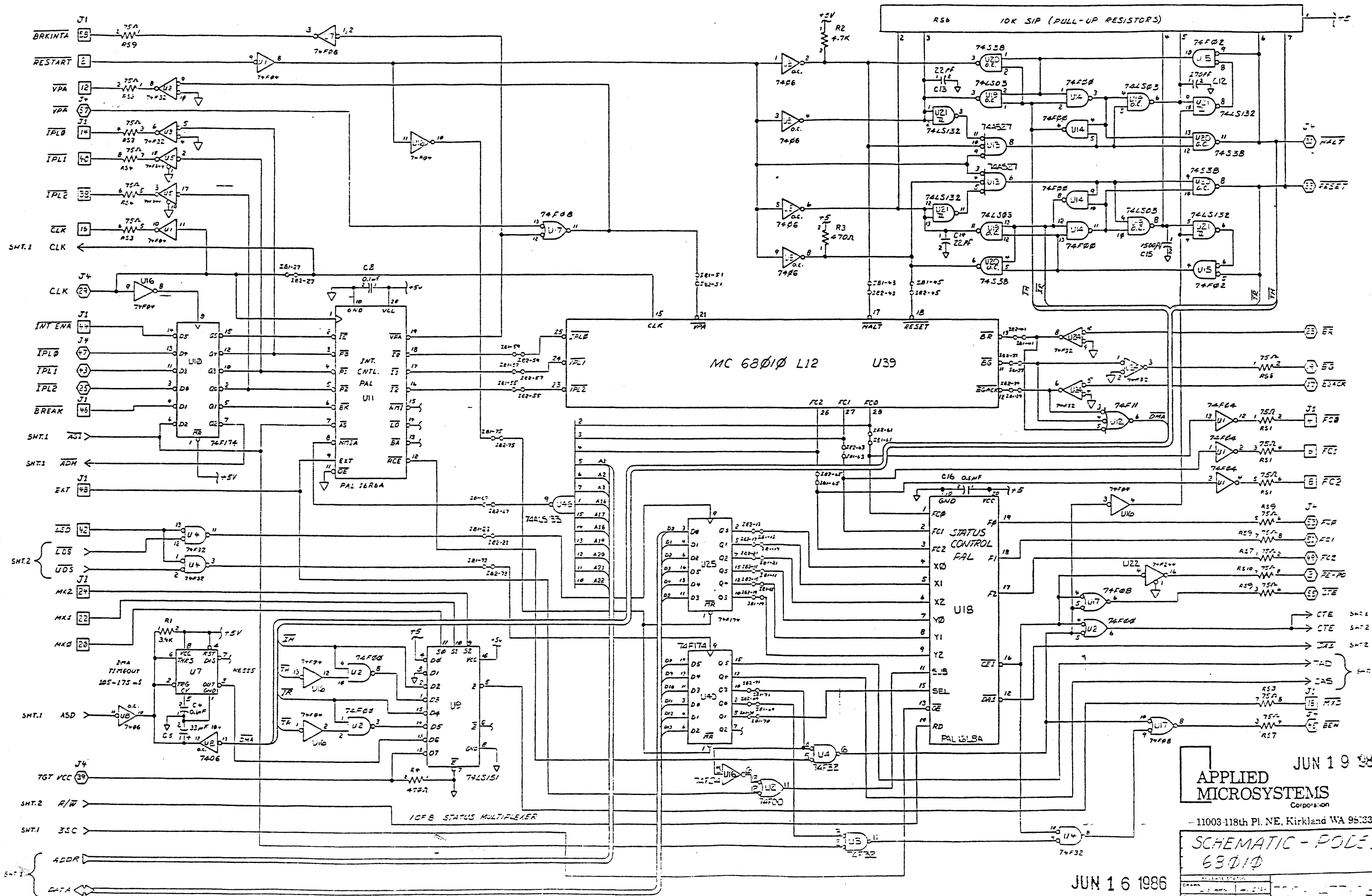
APPLIED MICROSYSTEMS Corporation

-11003 118th Pl. NE, Kirkland WA 98033

JUN 16 1986
JUN 19 1985

SCHEMATIC - PODS 1-2
68010

DATE	BY	DESCRIPTION



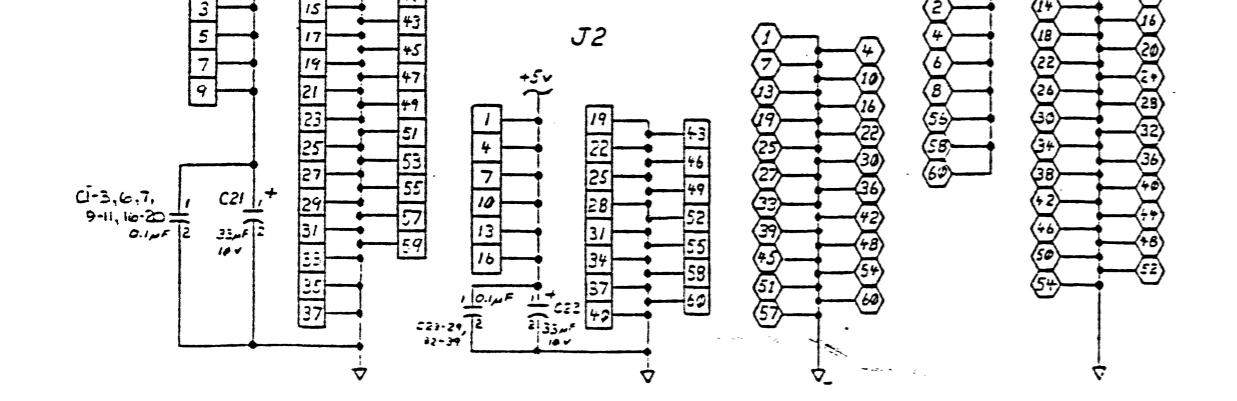
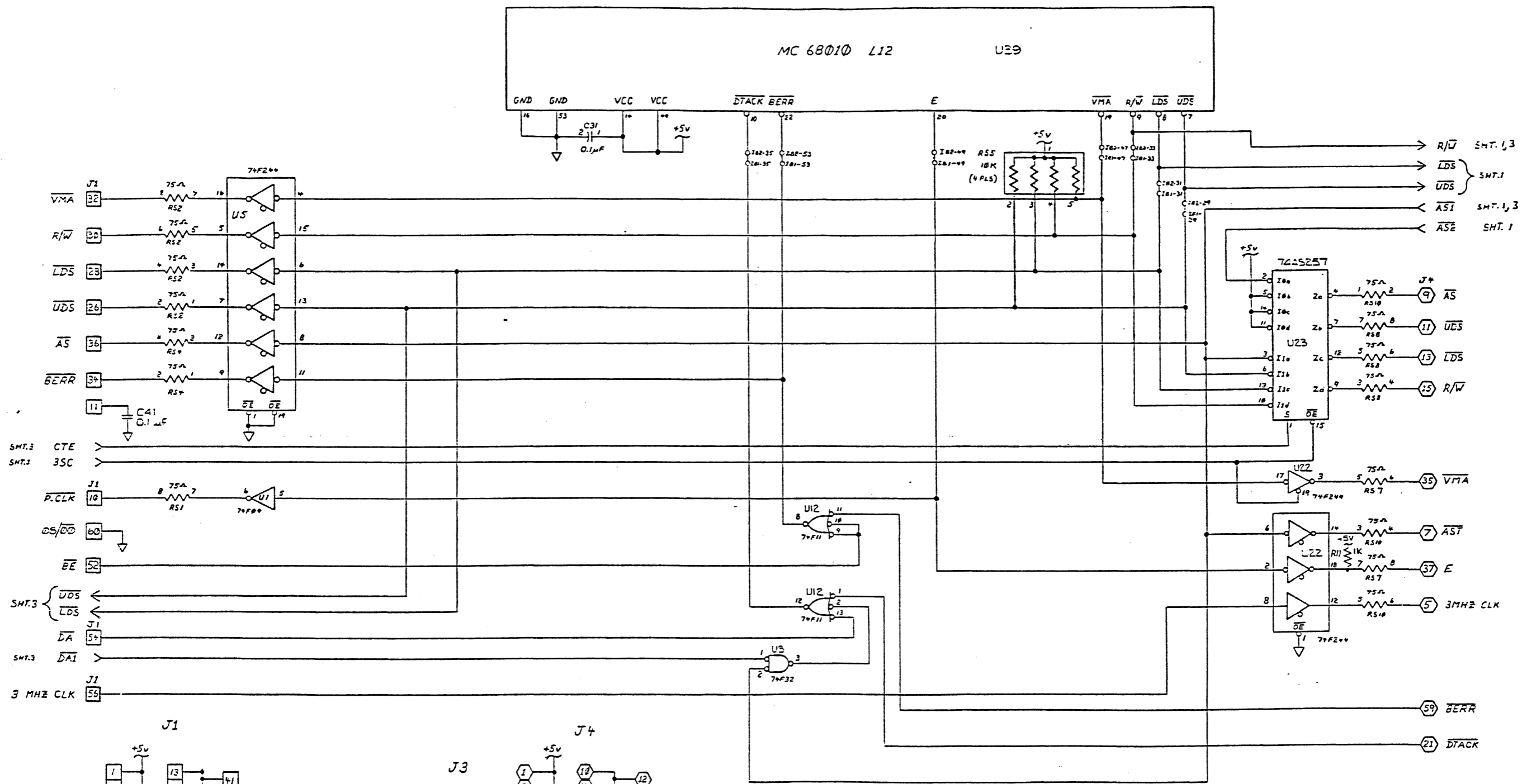
JUN 19 1985
APPLIED MICROSYSTEMS
 Corporation

- 11003-118th Pl. NE, Kirkland WA 98033

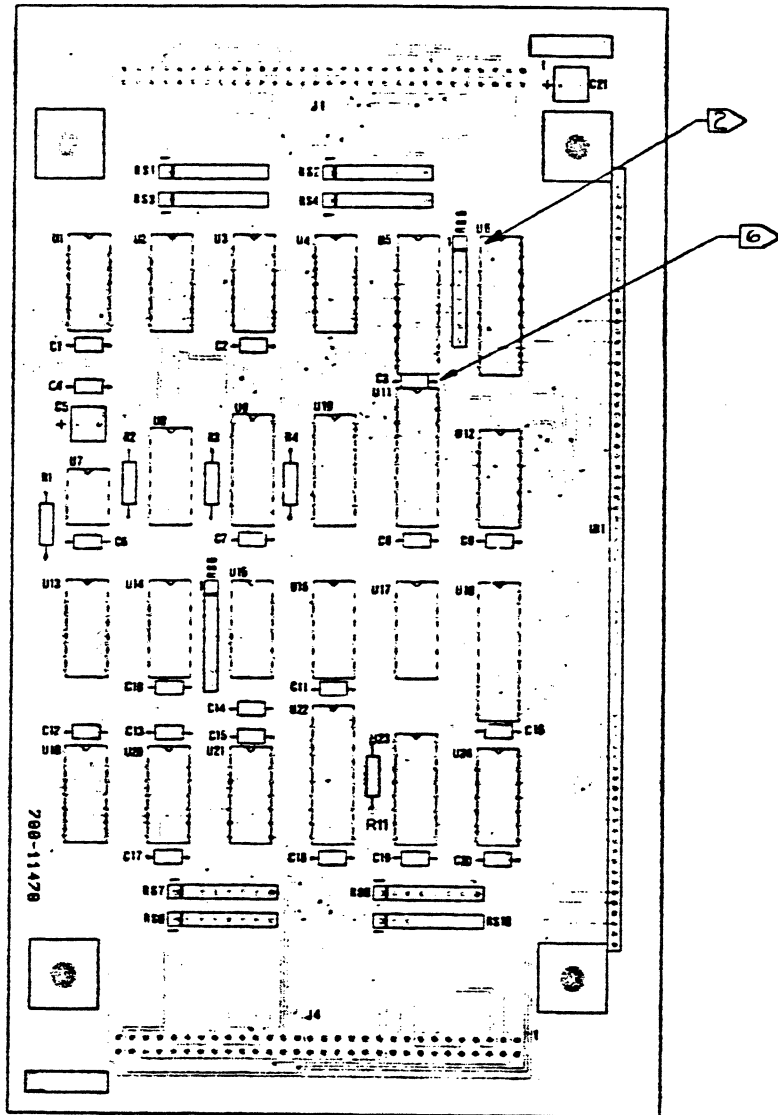
SCHEMATIC - POLES: 2
68010

JUN 16 1986

DATE	DESIGNED BY	CHECKED BY
APP'D		



APPLIED JUN 19 1985
 MICROSYSTEMS Corporation
 11003 118th Pl. NE, Kirkland WA 98033
 SCHEMATIC - PODS 1-2
 68010
 JUN 16 1986
 100-11477-05



REVISIONS			
REV	DESCRIPTION	DATE	BY
A	PRODUCTION RELEASE		
B	ECN # 344		
C	ECN # 347		
	DRAWING CLARIF #347		
	CLARIFIED J6 INSTALLATION		
D	ECN # 449		
E	ECN # 499		
F	ECN # 506		
G	ECN # 537	3-8-85	ME/591
	DWG CLARIF #632		
H	ECN # 651		
J	ECN # 734		
K	ECN # 690	11-5-85	ME/591
L	ECN # 856	2-5-86	JB/391

QTY	REF	DESCRIPTION	PART NO.	REF DES.
1	1	IC 74F257	34-11409	U23
1	1	RES 1K OHM 1/4W 5%	39-470-0177	R11
2	2	RES 51P, OK, 8 PIN	38-470-10823	R55,6
2	2	470 OHM, 1/4W, CARBON	37-470-10525	R34
1	1	3.9K, 1/4W, CARBON	36-470-10422	R1
1	1	4.7K, 1/4W, CARBON	35-470-10412	R2
8	8	RES, 51P, 75 OHM, 8 PIN	34-470-10279	R51-4,7-9
1	1	PLA-68010, POD, PAL "B"	34-00018	U11
1	1	PLA-68010, POD, PAL "A"	34-00017-01	U8
1	1	PLA-68000/08, POD, "STC"	34-00034-00	U15
1	1	IC 555 TIMER	315-10635	U7
1	1	74538, 2 INPUT, NAND, BUFFER	34-11435	U20
1	1	74F174, HEX, D, FLIP-FLOP	34-11433	U10
1	1	74AS27, TRIPLE, 3 INPUT, NOR	34-11432	U13
1	1	74AS257, 2 INPUT, MULTIPLEXER	34-11410	U23
1	1	74F11, 3 INPUT, AND, GATE	34-11143	U12
1	1	74LS03, 2 INPUT, NAND, OPEN	34-11021	U19
1	1	74F02	34-10877	U15
3	3	74F32, QUAD, 2 INPUT, OR, GATE	34-10637	U3,4,24
1	2	74F08, QUAD, 2 INPUT, AND	34-10636	U6,17
2	2	74F04, HEX, INVERTER	34-10610	U1,16
2	2	74F00, QUAD, 2 INPUT, NAND	34-10609	U2,14
2	2	74F244, OCTAL, BUFF/IN, DRV	34-10605	U5,22
1	1	74LS151, 8 INPUT, MULTIPLEXER	34-10503	U9
1	1	74LS132, 2 INPUT, SCHMITT, TRG	34-10170	U21
1	1	IC 7406, HEX, INV, BUFFER/DRIVER	34-10061	U8
2	2	CONN. HEADER, 60 PIN, MALE	20-11110	J1, J4
2	2	SOCKET, DIP, SOLDER, 20 PIN	20-10763-01	USE W/ U11, U18
1	1	CAP 1500 PF, 50V, D.I.P.	150-11145	C15
14	15	.1 MFD, 50V, D.I.P.	150-10572	C1, 2, 4, 6-11, 16-20
2	2	22 PF, 50V, RADIAL, CERAMIC	150-10633	C13, 14
1	1	270 PF, 1KV, RADIAL, CERAMIC	150-10524	C12
2	2	CAP 33 MFD, 10V, RADIAL, TANT	150-10091	C5, 21
2	1	CAP 0.1 MFD 50V, CERAMIC RADIAL	150-10003	C3, C41
1	1	PWB 68010 POD BD #2	170-11478-00	
1	1	PWB 68000 POD BD #2	170-11478-01	

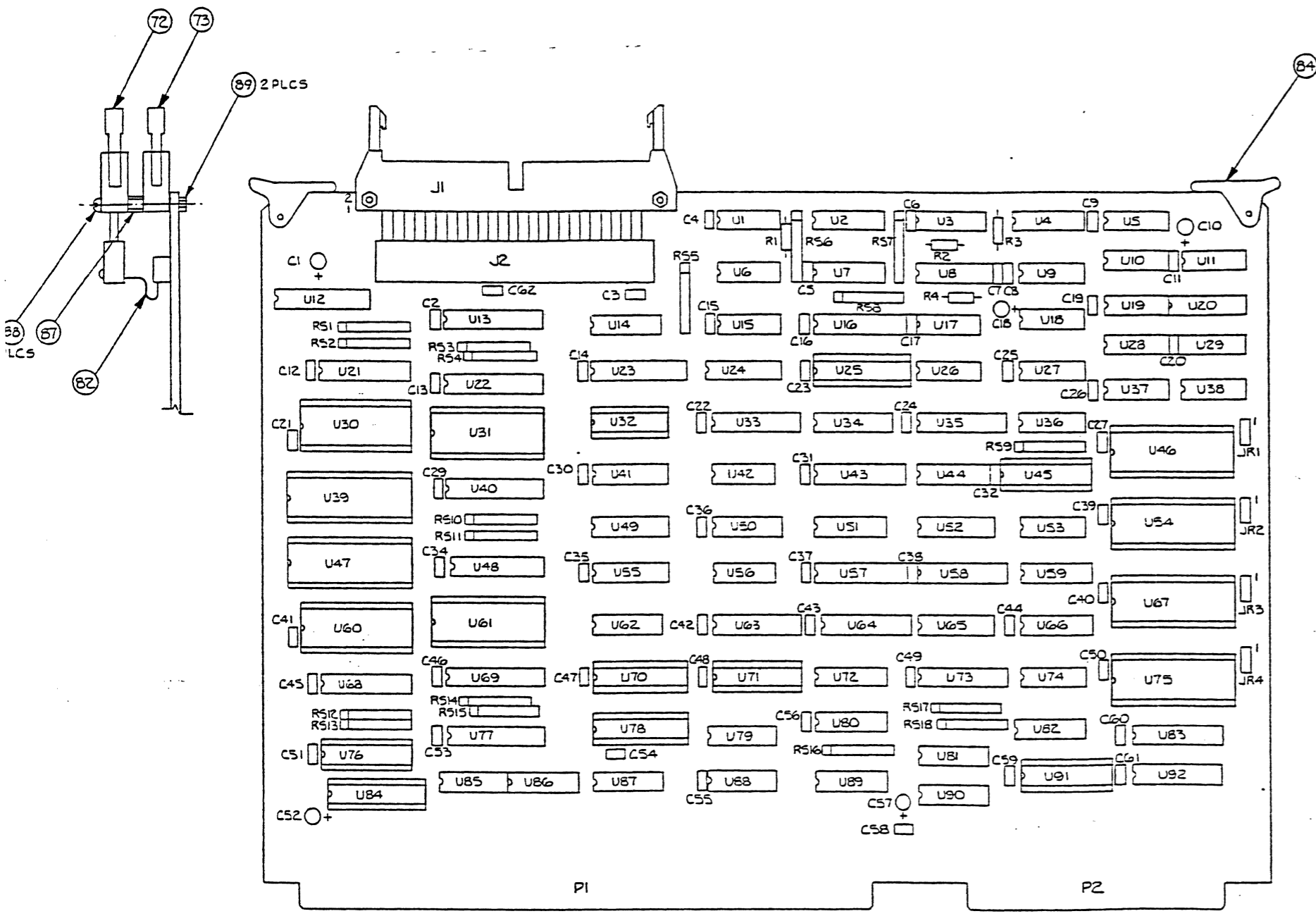
- 6 C3 LEADS MUST BE SPECIALLY PREPPED TO MATCH BOARD HOLE PATTERN.
- 5 U6 NOT INSTALLED IN -03 CONFIGURATION
- 4 REWORK -01 BOARDS PER ECN # 506
- FOR 170-11478-00 BDS REWORK PER ECN # 344, 347
- INSTALLING A 16 PIN IC TO A 20 PIN HOLE CALL OUT ALREADY ON BOARD (U6) INSTALL PIN 1 ON TOP LEFT HAND SIDE 4 UNUSED PINS SHOULD BE AT BOTTOM OF IC.
- 1 USE -02 ASSY FOR 68010 EMULATORS
USE -03 ASSY FOR 68000 EMULATORS

NOTES: UNLESS OTHERWISE SPECIFIED

JUN 16 1986

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE LIN .X ± .XXX ± .XX ± .ANG ± ALL DIM AFTER PLATING BREAK ALL SHARP EDGES REMOVE ALL BURRS	APPROVED DWN LEANA DEL BARRIO 10/23/85	DATE 10/23/85	APPLIED MICROSYSTEMS DESCRIPTION ASSEMBLY POD-68000/10 BD.#2 SIZE DWG NO D 700-11478-02/03 REV L
	PROJECT ENG J. T. HAN	DATE 3-7-84	
NOTICE: APPLIED MICROSYSTEMS CLAIMS PROPRIETARY RIGHTS IN THE INFORMATION DISCLOSED ON THIS DRAWING. IT IS ISSUED IN CONFIDENCE FOR ENGINEERING INFORMATION ONLY AND MAY NOT IN WHOLE OR IN PART BE USED TO MANUFACTURE ANYTHING WITHOUT THE WRITTEN PERMISSION OF APPLIED MICROSYSTEMS CORP.	ENG MGR J. T. HAN	DATE 2-17-84	
DO NOT SCALE DRAWING		SCALE NONE	SHT 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DR	CHK/APP'D/DATE
E		ECN # 464 FOR D REV. SEE HISTORY FILE	TC	1/15/85
F		ECN # 530	TC	1/15/85
-		DRAWING CLARIFICATION PER ECN # 573		1/15/85
G		ECN # 574	VEJ	1/15/85
H		ECN # 603	VEJ	1/15/85
J		ECN # 668	VEJ	1/15/85
K		ECN # 593	VEJ	1/15/85
L		ECN # 731	VEJ	1/15/85
M		ECN # 848	VEJ	1/15/85



USE -04 ASSY FOR 68000/68008 EMULATORS
 USE -05 ASSY FOR 68010 EMULATORS

1. SEE M15 SYSTEM FOR PARTS LIST.
 NOTES:

JUN 16 1986

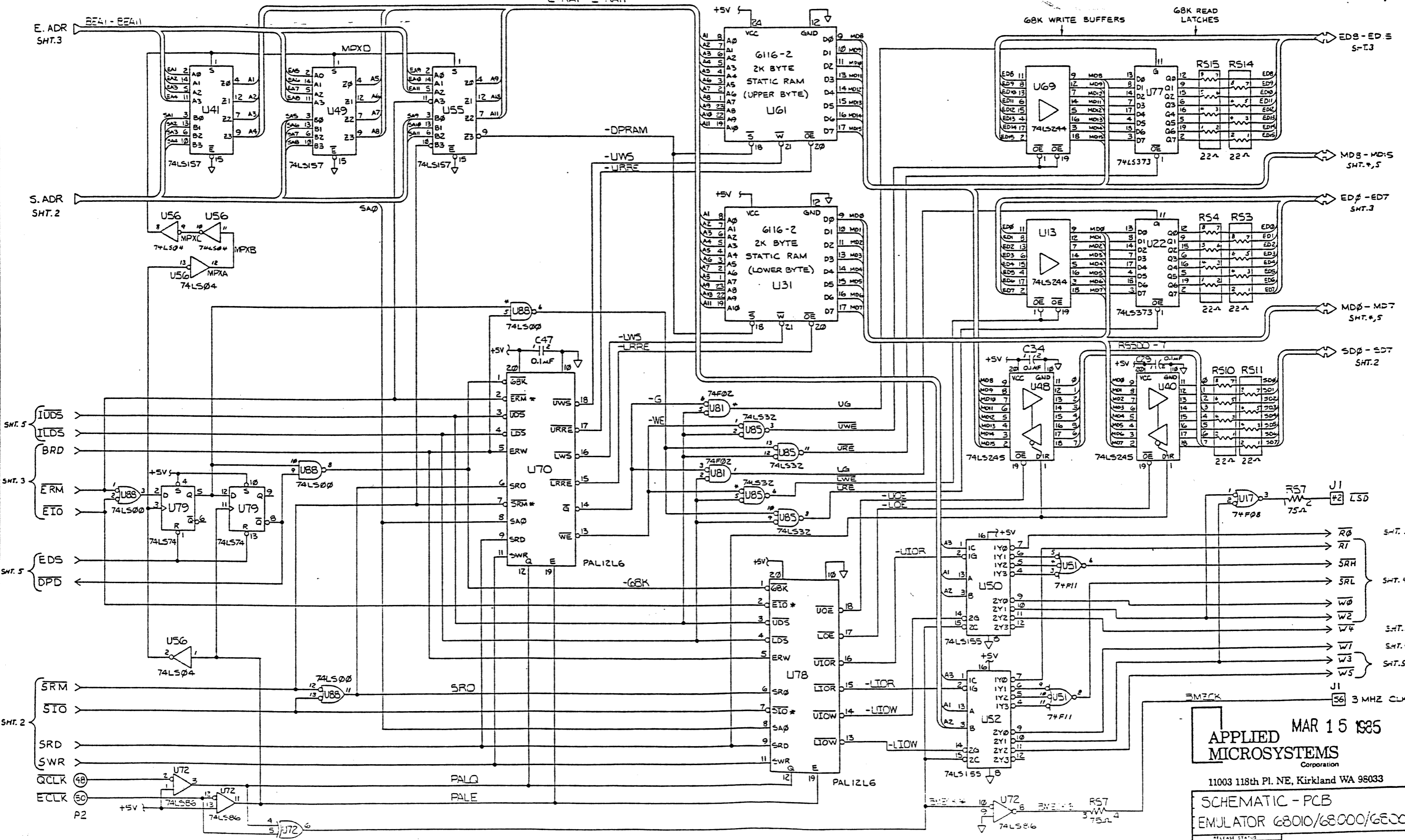
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: LIN .X± .XXX± .XX± ANG± ALL DIM. AFTER PLATING BREAK ALL SHARP EDGES REMOVE ALL BURRS	APPROVED	DATE	APPLIED MICROSYSTEMS CORPORATION DESCRIPTION ASSEMBLY - EMULATOR BOARD 68000/C3/10 SIZE DWG NO. D 700-11485-C4-05
	DWN	12/10/84	
	CHK	1/14/85	
	PROJECT ENG	1/14/85	
	ME	1/14/85	
	QC		
	ENG MGR		

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68010/CONTROLLER ADDRESS MULTIPLEXER

CTRA1 - CTRAI1

C	ECN # 464	TCC #	1/11/85	ZONE	LTR	DESCRIPTION	DR	CHK	APPROV	DATE
D	ECN # 530	TCC #	1/16/85	A		RELEASE				
				B		ECN # 459				

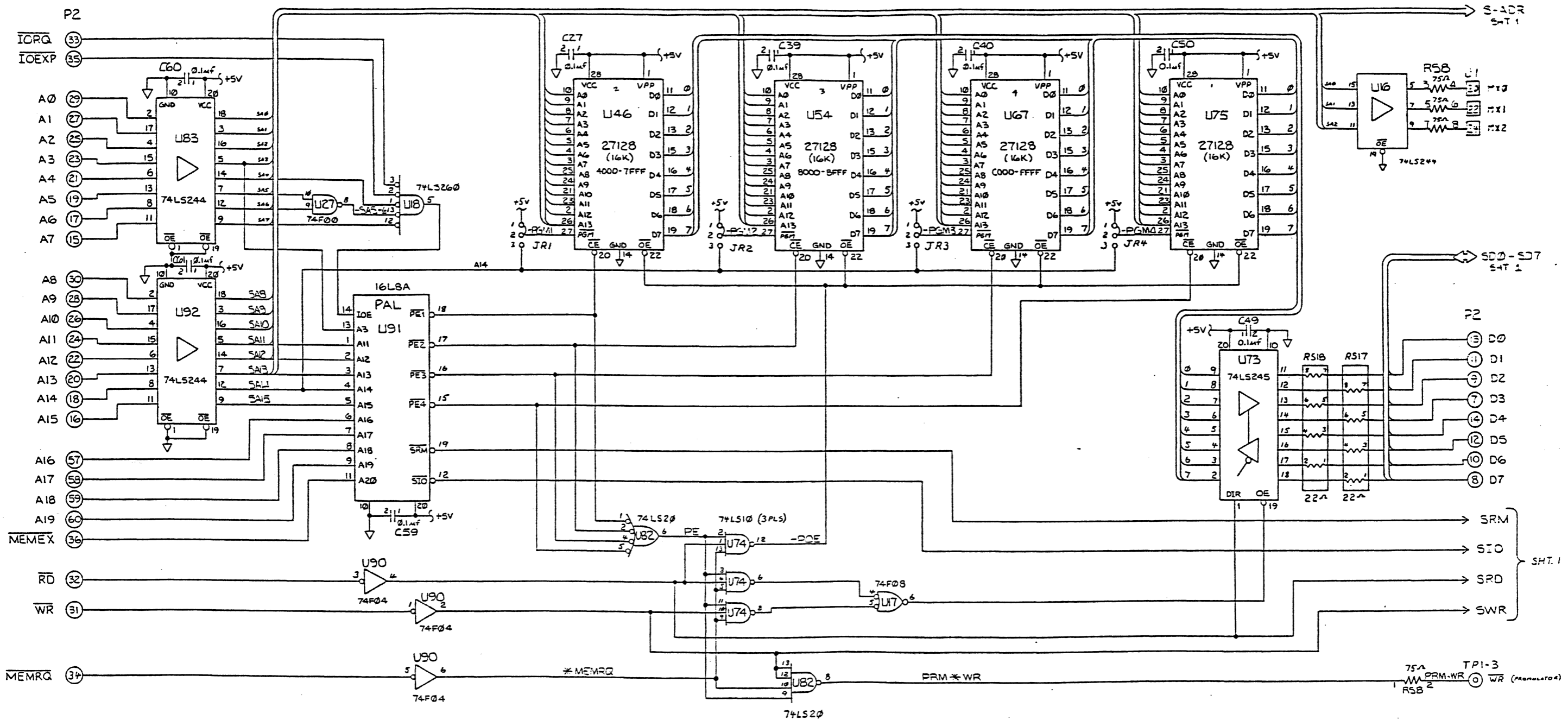


APPLIED MICROSYSTEMS Corporation
 11003 118th Pl. NE, Kirkland WA 98033

SCHEMATIC - PCB
 EMULATOR 68010/68000/68008

JUN 16 1986

RELEASE STATUS	700-11485-SC
CHECKED	SCALE
DATE	REV D



MAR 15 1985
APPLIED MICROSYSTEMS
 Corporation

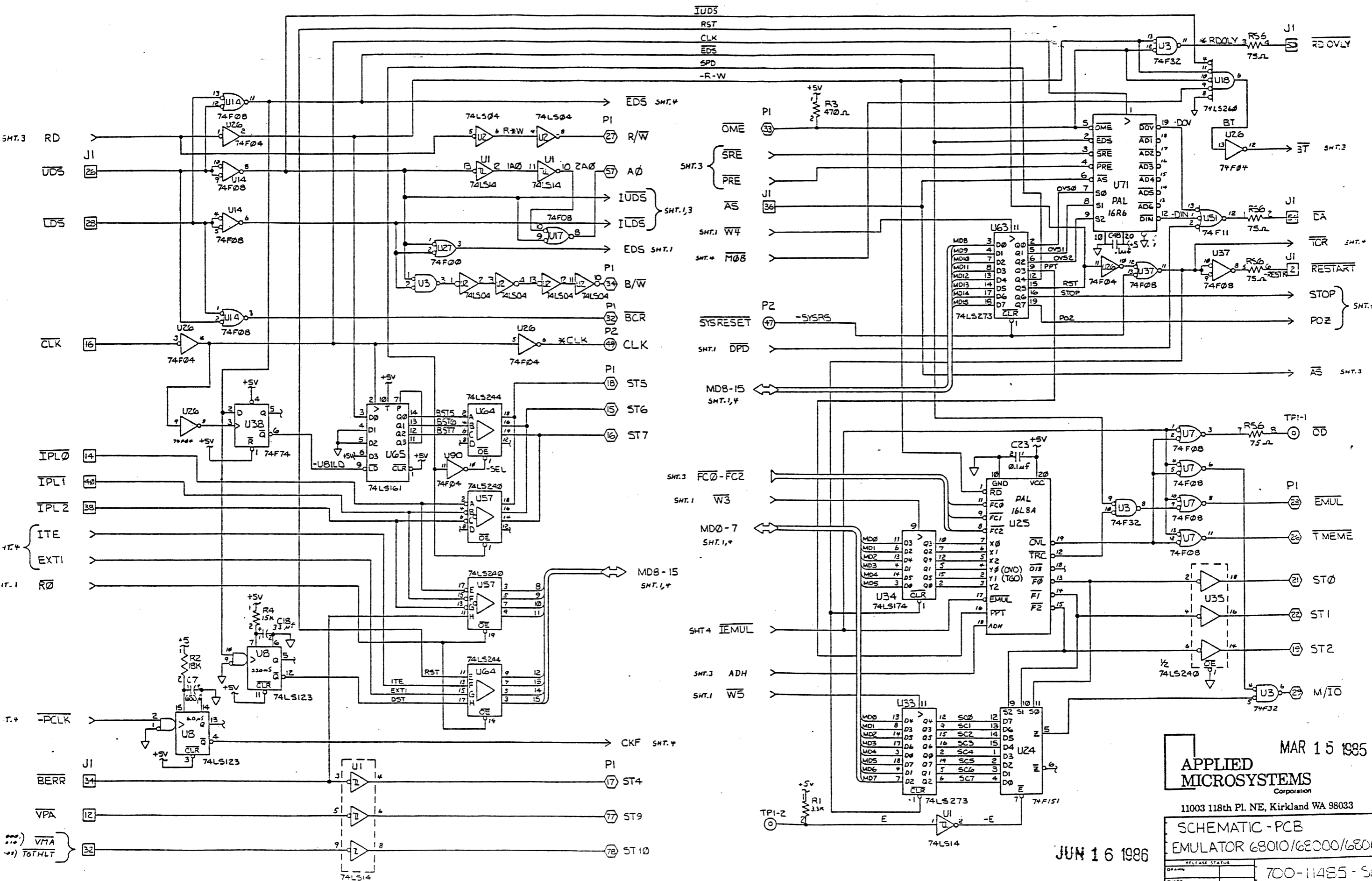
11003 118th Pl. NE, Kirkland WA 98033

SCHEMATIC - PCB
 EMULATOR 68010/68000/68008

JUN 16 1985

RELEASE STATUS	700-1455 - 50
DRAWN	
CHECK	
DATE	3-10-84
SCALE	
REV	
BY	

APPLIED MICROSYSTEMS CORPORATION



MAR 15 1985
APPLIED MICROSYSTEMS
 Corporation

11003 118th Pl. NE, Kirkland WA 98033

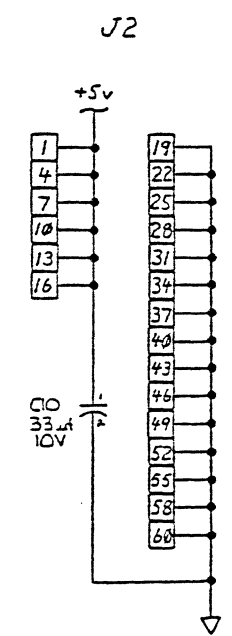
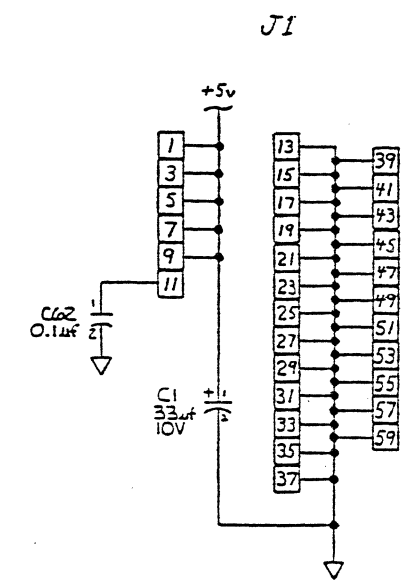
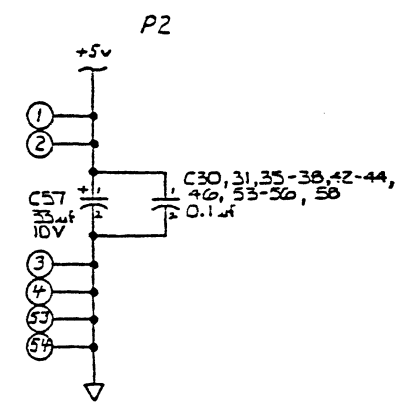
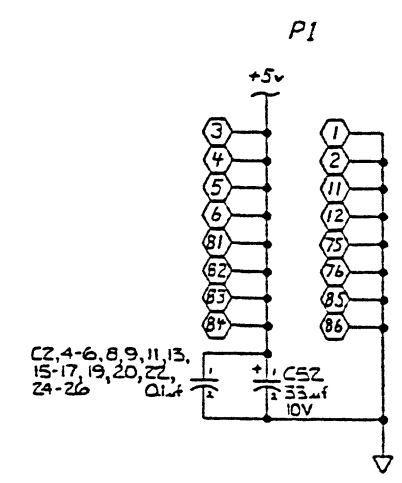
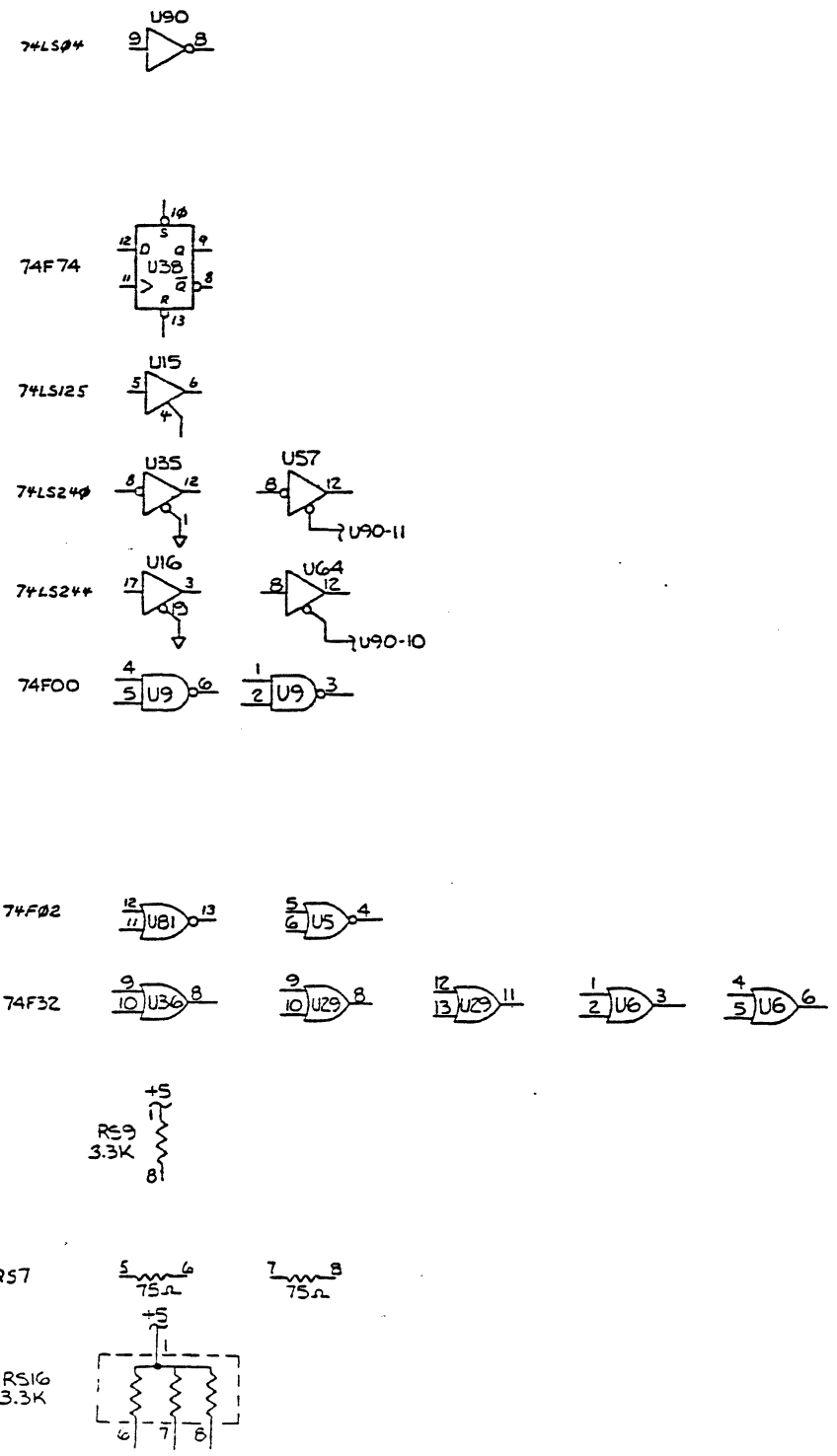
SCHMATIC - PCB
 EMULATOR 68010/68000/68008

JUN 16 1986

RELEASE STATUS	700-11485-SC
CHECK	
DATE	2-10-84
SCALE	1:1
SHEET	5 of 6

REVISIONS						
ZONE	LTR	DESCRIPTION	OR	CHK	APPR'D	DATE

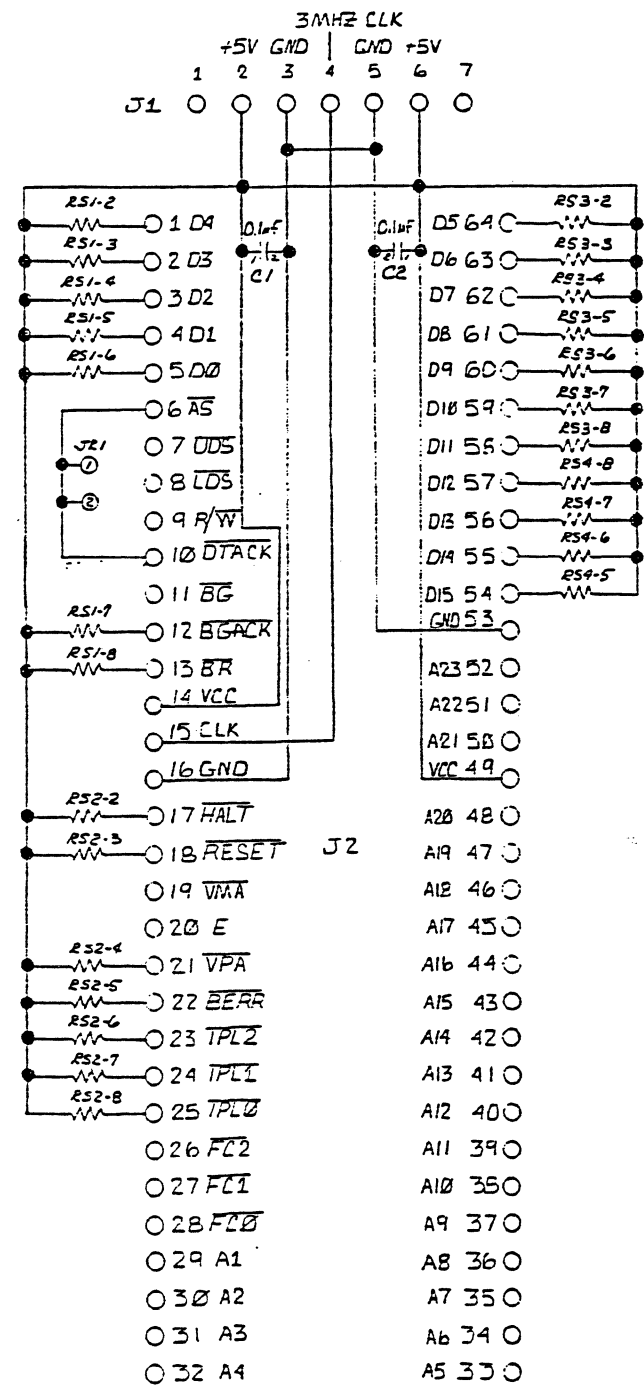
SPARES:



JUN 16 1986
MAR 15 1985

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: LIN .X± .XXX± .XX± ANG± ALL DIM. AFTER PLATING BREAK ALL SHARP EDGES REMOVE ALL BURRS	APPROVED	DATE	APPLIED MICROSYSTEMS Corporation	
	DWN <i>[Signature]</i>	7-30-85		
NOTICE: APPLIED MICROSYSTEMS CLAIMS PROPRIETARY RIGHTS IN THE INFORMATION DISCLOSED ON THIS DRAWING. IT IS ISSUED IN CONFIDENCE FOR ENGINEERING INFORMATION ONLY AND MAY NOT IN WHOLE OR IN PART BE USED TO MANUFACTURE ANYTHING WHETHER OR NOT SHOWN HEREON. REPRODUCED OR DISCLOSED TO ANYONE WITHOUT DIRECT WRITTEN PERMISSION FROM APPLIED MICROSYSTEMS CORP.	CHK <i>[Signature]</i>	2-16-84	DESCRIPTION SCHEMATIC - PCB EMULATOR 68010/68000/68008	
	PROJECT ENG <i>[Signature]</i>	2-10-84		
	ME <i>[Signature]</i>	2-17-84		
	QC <i>[Signature]</i>	2-17-84		
DO NOT SCALE DRAWING	ENG MGR <i>[Signature]</i>	2-11-84	SIZE DWG NO. D 700-11485 - SC	REV D
			SCALE —	SHT 6 OF 6

DR.	DESCRIPTION	APP / DATE
1	HARDMODEL	
A	PROD. REL	



RS1-4 PIN 1 IS TIED TO +5
* ALL RESISTORS ARE 3.3KΩ
PULL-UPS

JUN 16 1986
MAR 15 1985

APPLIED
MICROSYSTEMS
Corporation

11003 118th Pl. NE, Kirkland WA 98033

SCHEMATIC -
NULL TARGET, 65000

RELEASE STATUS		900-11268-50
DESIGNED BY	REVISION	
CHECKED BY	DATE	
APPROVED BY	DATE	
SCALE		1" = 4"