ZDS-1/40

Hardware Reference Manual

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SECTION 1

GENERAL INFORMATION

1.1 Introduction

This manual describes the Z-80 Development System from the hardware point of view. It is intended to be used as a tool for the engineer/programmer to design systems based on Z-80 hardware and software. In particular, the user is guided in the debug of his prototype hardware and software.

Although reference is frequently made to Development System Software, the main descriptions and operating instructions are contained in the following documents:

- RIO OS User Manual
- RIO Relocating Assembler and Linker User Manual
- RIO Text Editor User Manual
- ZDS-1/40, ZDS-1/25 PROM User Manual
- Zilog Analyzer Program (ZAP) Software Manual

This manual describes the basic operation and basic components of the ZDS-1/40 Development System.

1.2 Z-80 Development System Description

The Z-80 Development System is a computer system designed to support all activities associated with the creation of microprocessor hardware and software. The system includes two floppy disks with a sophisticated file maintenance system. With this capability, the user can quickly retrieve, manipulate, and store large files of data to minimize software development time. The system also includes an advanced real time debug module that connects directly to the user's system, thus, providing a simultaneous hardware and software debug capability. A block diagram of the ZDS-1/40 is shown in Figure 1-1.

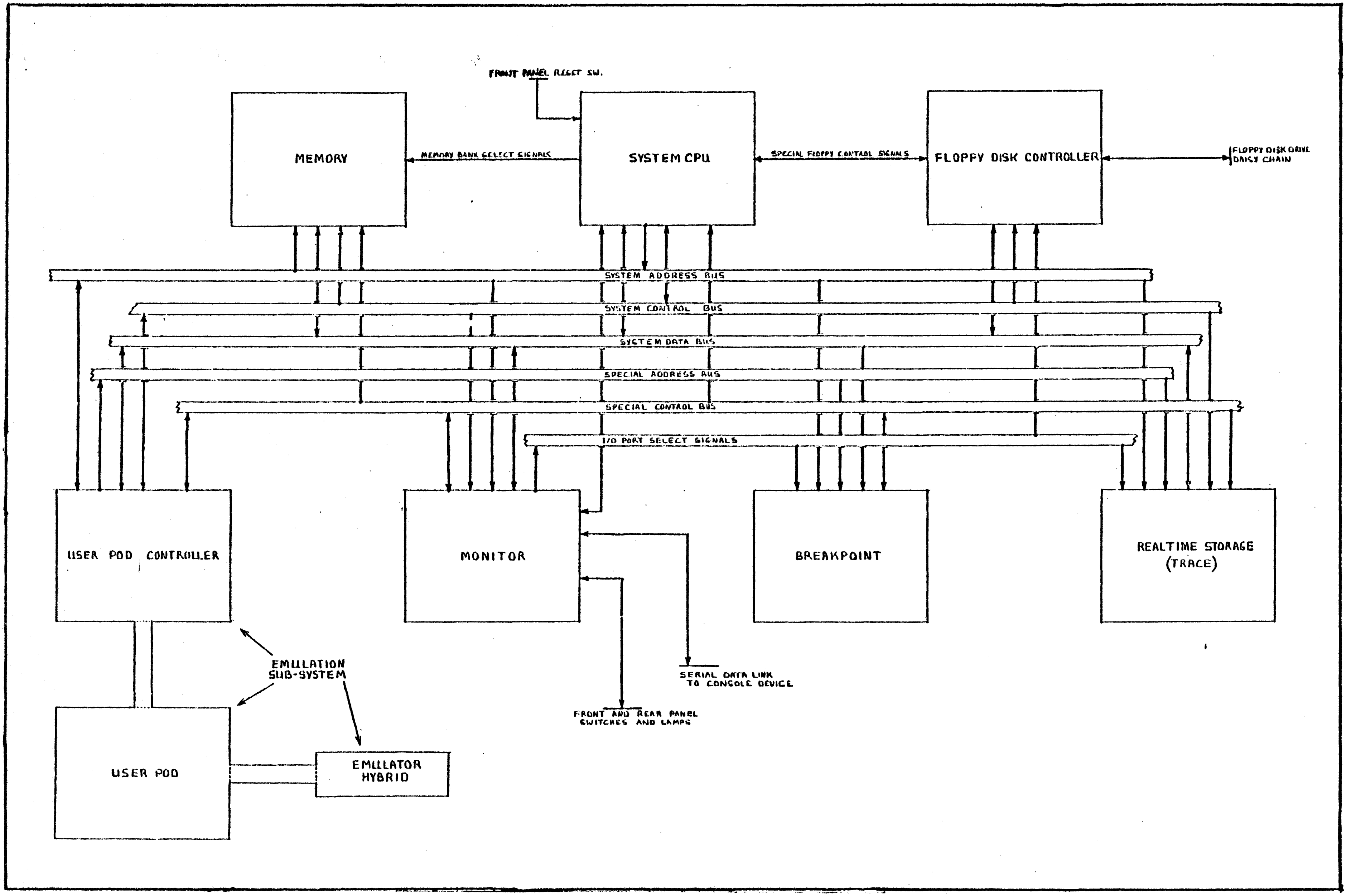


Figure 1-1. ZDS-1/40 Block Diagram

The specific features of the Development System include:

- Z-80 CPU with 4K bytes dedicated RAM/ROM
- RS-232 or current-loop serial interface
- 60K bytes of general-purpose read/write memory
- Programmable hardware breakpoint module
- Programmable real time event storage module
- In-circuit emulation module to connect system to user's equipment
- 2 floppy disk drives and controller
- Full software including:
    - ROM-based I/O handler and command interpreter
    - Disk-based debug package
    - RIO operating system
    - Editor
    - Assembler and Linker

The ZDS-1/40 uses a Z-80 2.5 MHz CPU to accommodate the system's operation in the monitor mode and a special Z-80A 4 MHz CPU in the emulator to accommodate in-circuit emulation in the user's system.

In the Program Development mode, the system performs as a stand-alone program development tool, allowing software programs to be entered into RAM, edited, assembled, filed on disk for future use, and loaded for execution. This entire process is performed through simple commands from the user's terminal.

In the Hardware/Software Debug mode(ZAP), the system memory and peripheral elements are available to the user's own system. The system peripherals use I/O port number E0H through FFH. These port numbers are reserved for the system in monitor mode. In user mode, a RAM resident user's program is executed in real time and all I/O ports may be in the User System. The use of Ram for the program eliminates costly and time-consuming PROM programming in the early phases of software development.

A major feature of the ZDS-1/40 Development System is its powerful debug module. This module allows ZDS-1/40 emulation system bus transactions that are designated pertinent by the user to be stored in real time into an independent memory. The user can also specify that any type of system transaction can suspend user operation and cause the system to re-enter the monitor mode. The complete record of all transactions preceding this suspension that was recorded in the independent memory can then be conveniently displayed on the system terminal. This ability to freeze real time event sequences and then to review selected events in detail, permits the user to accomplish product design and hardware/software debugging in the shortest possible time. Without this feature, it is extremely difficult to find errors in programs or hardware where the user cannot single step through a program due to real time I/O restrictions.

1.3 Note To The Design Engineer

Although the ZDS-1/40 represents the state-of-the-art in development systems, there are certain characteristics and restrictions associated with its use that must be considered by design engineers. These considerations are summarized in this section of the manual so that they might serve as a convenient reference when planning design procedures.

First, the Z-80 CPU Emulator possesses the characteristics of the Z-80 CPU Chip, with the following exceptions:

1) maximum high-level preload is 10 microamps.

2) maximum low-level preload is 200 microamps.

3) maximum cable preload capacitance is 30 picofarads.

4) maximum low output voltage is 0.51 volts.

Second, because of the MOS interface and the emulator hybrid concept used in the ZDS-1/40, certain lines to the emulator must be controlled:

1)	BUSRQ	-	Bus request
2)	NMI	-	Non-maskable Interrupt Request
3)	INT	-	Maskable Interrupt Request
4)	MQR	-	Memory Request
5)	WR	-	Write
6)	CLK	-	Clock Input Signal

This approach allows the development system to communicate with the emulator without disturbing the user's system. This approach is also required to provide memory mapping features.

The WAIT line from the emulator is not controlled, but is OR'd with the WAIT line from the development system.

In addition, there is a control switch associated with the +5 Vdc supply.

The BUSRQ, NMI, and INT lines are controlled by the system so that the development system software, the Zilog Analyzer Program (ZAP), may communicate with the emulator without disruption. These lines are enabled or disabled simultaneously when the software communicates with the emulator. They are disabled by ZAP on initialization, and must be enabled by a command from the system console. These lines may be disabled by the ZAP command when the prototype device is being debugged.

The MQR and WR lines are controlled for memory mapping. The reason is to allow the development system to always see the MQR and WR signals from the emulator, but only to allow the user's system to see them when the map defines memory to exist in the user system at a specified address. These lines are also controlled to prevent spurious access to user memory during Monitor Mode operation, while still allowing refresh of user RAM.

The WAIT line is a special line to the emulator, in that it may be activated from two different sources. Again, this approach is due to the memory mapping features of the system. This line may be activated from the user's system, or by the logic of the development system, when accessing memory that has been defined to exist in the development system. The development system presently pulls the WAIT line for one T-state for each access to development system memory at frequencies above 2.5 MHz. When accessing user memory, the access will occur without wait states unless the user's prototype device generates wait states. The WAIT line is also pulled by the development system during transitions between User and Monitor Modes.

Because the user and system WAIT lines to the emulator are OR'd through a simple transistor gate rather than a TTL gate in the Z-80 CPU emulator, it is extremely important that the WAIT line is terminated properly by the user's system. This line should be pulled up with a resistance value greater than 4.7K ohms, and driven by a logic device with an open-collector output.

The clock (PHI) line to the Z-80 CPU, as well as any other microprocessor, is one of the most critical signals. This signal should be generated using the logic circuitry described in the Zilog Application Note for the Z-80 Clock Driver, or with an equivalent circuit. The clock stablility and frequency should be examined under load, with the Z-80 CPU installed, before connecting the emulator and the prototype device.

The Emulator PC board contains a switch that is used to select either an internal or external clock source for the emulator. When running on internal clock, the frequency will be 2.5 MHz. If the clock selected is internal, and the prototype device is also providing clock, the two will be tied directly together, making the emulator inoperative.

In order for the emulator to operate when it is not supplied with +5 vdc from the user system, the development system power supply can be connected to the emulator CPU by means of a switch located next to the internal/external clock switch on the emulator PC board. If this switch is left in the internal, or development system, position when the user's prototype is also providing VCC, the two power supplies will be connected directly together, causing difficulties and possible damage to the equipment.

When the emulator executes a HALT instruction, it behaves exactly like a Z-80 CPU. However, some users may use a HALT instruction as a wait loop to await an interrupt. If the user executes a HALT instruction and presses the MON button on the front panel, the development system will reset the emulator to exit the HALT state. This will have the following effects:

a) The reset will clear the PC, I, and R registers and disable interrupts.
b) The development system can recover the PC, but the I and R register contents will be lost.

The most important design consideration in using the emulator is the fact that only the MRQ and WR lines are controlled by the development system. The RD line is not controlled because it cannot be controlled without controlling M1. This is because a Z-80 PIO chip will reset itself when it sees an M1 without a RD or IORQ signal also present.

Because RD is not controlled by the development system, the user must not use the RD signal alone to control bi-directional data bus drivers in the prototype device. The control logic for the drivers must use MRQ as one of the enabling terms. If it is not used, bus conflicts (contention) will occur, rendering the emulator inoperative. A recommended circuit for control of the user's data bus is shown in Figure 1-2.

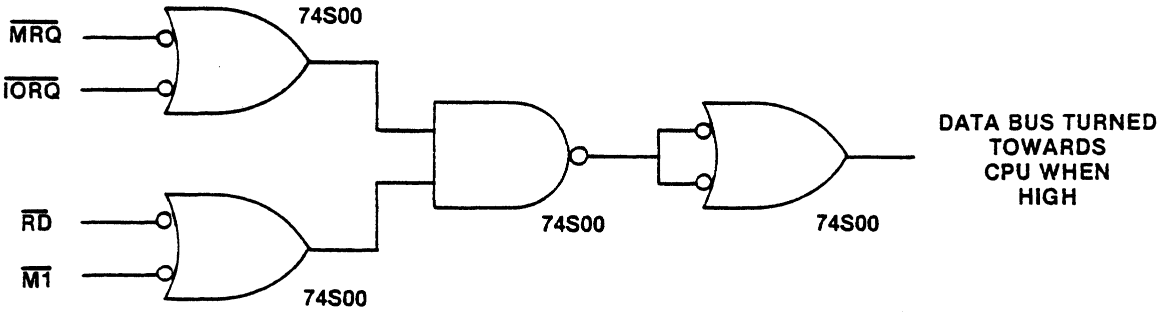


Figure 1-2 Bus Driver Control Circuit

This circuit allows the emulator to control the bus drivers using MRQ. It also allows the bus to function properly for input instructions and for interrupt acknowledge cycles. Using this scheme, the user's data bus is turned away from the emulator Z-80 CPU unless a MRQ+RD (memory read), IORQ+RD (port read), or IORQ+M1 (interrupt acknowledge) occurs.

The MRQ line is controlled to facilitate transitions between Idle Mode when the emulator is not running a program and Run Mode when the emulator is running a program.

When the system is in Idle Mode, user dynamic RAM refresh is maintained by causing the emulator to continuously execute a jump relative minus 2 instruction. This step keeps the emulator Z-80 CPU in a tight loop with constant fetch cycles (known as idling). During the refresh interval of each fetch cycle, MRQ is enabled and refresh occurs in a normal manner. In Run Mode, the emulator runs in the usual manner.

When a transition is made from Idle to Run, the first fetch from user memory occurs in a cycle in which MRQ is delayed until after the rising edge of T2 by the state machine in the user pod, which controls the operating mode. Two wait states are then forced by the state machine to ensure that the user memory access has sufficient time to occur. The prototype device may create additional wait states in the usual way.

When a transition is made from Run to Idle, a final fetch from the prototype device memory will be attempted, but the MRQ line will be disconnected from the user bus after the leading edge of T3, and the cycle will be prolonged by three wait states. This allows the emulator Z-80 CPU to actually read the jump relative instruction minus 2 instruction referred to above. The user WAIT line can cause additional wait states to be added to this cycle.

SECTION 2

INSTALLATION

2.1 Initial Unpacking and Inspection

Inspect the product for shipping damage as soon as it is unpacked. Check for any physical damage that may be attributed to abuse and handling during shipment. If the product is damaged in any way, notify the carrier and Zilog immediately.

2.2 Power and Signal Connections

Inspect the power connector area on the rear panel of the two chassis units. Next to the power connector is a small switch imprinted with either "120" or "230" to indicate the AC line voltage for which the unit is configured. In the unlikely event that this figure disagrees with the user site voltage, the power supply can be reconfigured by simply moving the switch element until the proper voltage figure is visible. Verify that the main AC power-on switch is in the OFF position. The power switch for the ZDS-1/40 system is located on the rear panel. Now connect the AC power cords to the source and rear panel jacks.

The terminal for user communication with the Development System must now be connected. Such a terminal can be purchased as an option from Zilog, however, any standard teletype with a 20mA interface or CRT terminal with an RS-232 interface may be used. Connect the terminal's interconnect cable, supplied with the terminal, to connector J106 on the rear of the microcomputer chassis.

*** NOTE ***

The J106 connector on the rear of the microcomputer chassis, used for terminal interface, is shipped with pins 5, 6, and 8 permanently wired high. According to standard RS-232 specifications, these pins are designated:

Pin 5 - Clear to Send
Pin 6 - Data Set Ready
Pin 8 - Carrier Detect

It is true, however, that some RS-232 interface terminals are not fully compatible with these specifications, i.e., the terminal interface might use pins 5, 6, or 8 for a function other than listed, and when connected to the system, the terminal may not function properly.

If the user determines that the terminal interface does indeed have pin requirements other than those listed above for Pins 5, 6, and 8, the user must modify the cable to interconnect to the microcomputer by cutting the wires in the cable associated with these three pins. If such a change is necessary, the microcomputer's J106 pin assignments are listed below to make the change easier.

Pin No.	Signal Name
2	RS-232 Data In
3	RS-232 Data Out
7	RS-232 Return
10	TTY Data In
5,24,6,8	TTY In Return (200 ohms to +12)
16	TTY Data Out
17	TTY Out Return (200 ohms to ground)
23,25	GND 01
20,21,22	GND 02
18,19	GND 03
14,15	GND 04

SECTION 3

PRINCIPLES OF OPERATION

3.1 Processor Module

The processor module is a single card containing all elements necessary to function as a stand-alone computer. The card contains 3K bytes of PROM and 1K bytes of RAM in which reside the operating system, peripheral drivers and bootstrap loader. The peripheral driver routines can be accessed by the user.

3.2 Real Time Debug Module

The Z-80 Development System real time debugging capability enables the user to easily locate and correct any hardware or software design errors. With this disk-based module, the user monitors the operation of his software in real time and sets hardware breakpoints to stop the program on any data, address, or control bit pattern. Once stopped, the system returns to the monitor mode where the debug software allows the user to display the contents of any internal CPU register, or memory location, or to change any register or memory location prior to continuing the program from that point.

The real time debug module consists of a real time storage board, breakpoint board, pod controller board, pod and emulator. The real time storage board contains a 256 by 32 storage array. This array stores up to 256 events. The 32 stored bits include:

- 16-bit address bus
- 8-bit data bus
- 7-bit control bus

The last bit is used as a marker to identify the first transaction that is stored when the user's program begins execution. The debug software package allows the user to specify the types of transactions that are to be stored in the memory. Any combination of the following transactions can be stored:

- Memory Reads
- Memory Writes
- I/O Port Reads
- I/O Port Writes

After the system returns to the monitor, the contents of the storage array can be printed on the user's terminal in a concise form to readily show how the program arrived at the current point.

The breakpoint card monitors the system bus and halts emulation if a user-specified transaction occurs. The user may specify that a break should occur on any combination of the following transactions:

- Ml Fetch
- Memory Read
- Memory Write
- I/O Port Read
- I/O Port Write

In addition, he may specify that the selected transaction have a specified 16-bit memory address or an 8-bit I/O port address and/or any specific bit pattern on the data bus. Thus, the user can specify complex events such as writing a "1" on bit 6 of I/O port number F6H.

3.3 System Memory Module

The system uses standard 16K elements configured in 16K byte increments, with 64K bytes on a single system memory board. System memory is shared between the monitor mode and the user mode.

In Program Development mode, programs are entered, edited, assembled and loaded directly into RAM for immediate execution without the additional cost and time delays associated with programming PROMs.

In the Hardware/Software Debug mode, Development System Memory contains the RIO Operating System, the ZAP Operating System, and the PROM Operating System. The remaining RAM is available for mapping into the User System. Any combination of external ROM, RAM or PROM can be used in place of, or in combination with, the standard system RAM through the in-circuit emulation bus.

3.4 Floppy Disk Controller Module

This single circuit board interfaces two floppy disk drives for support of the Z-80 disk-based operating software and for user program storage. The utility for the control of the disk drives is embodied in system firmware located in PROM on the processor module.

3.5 User Pod Controller

This card contains all elements necessary to interface the system bus to the special Emulator bus. In addition, a User Pod and hybrid emulator are provided to complete the systems interface. The User Pod contains all time critical emulator control logic and buffers. The hybrid emulator is a modified Z-80A. This interface includes:

- 16-bit address bus
- 8-bit data bus
- All CPU control signals
- System clock

All lines provide TTL-compatible MOS signal levels for connection to any external User System. The switch on the emulator hybrid allows for the use of an external clock.

SECTION 4

USER OPERATION

4.1 Introduction

The user is directed to the manuals listed in Section 1.1 for a detailed description of the operation of the system software.

4.2 Front Panel Indicators and Switches

There are four lighted button-type switches/indicators on the front panel of the microcomputer chassis. Each switch has a specific function related to a specified system operating mode.

- WAIT

Pressing the WAIT Button resets the entire system to the debug level by providing a power-on clear. At this time, a character "S" or a carriage return must be entered from the terminal in order to resume operation. Depressing the WAIT button removes the refresh signals to the internal dyanamic RAM so that any programs stored there may be destroyed. The lamp under this switch serves as an indicator that the computer is in a WAIT state. During normal system operation, the CPU enters the WAIT state during disk operations. The only other time that the CPU should enter the WAIT state is during hardware/software debug mode when the user's hardware forces a WAIT state.

- USER

The indicator light is on any time the systems is in the user mode; that is, when it is running a real-time user's program and it is not in the operating system, edit, assemble, or debug software environments. The USER button has been disabled so that the only way to start an emulation is through the debug software.

- MON

This indicator is lit any time the system is in Monitor mode; that is, whenever it is in the operating system, edit, assemble, or debug software environments. The button switch can be pressed to take the system from the ZAP emulation to the ZAP monitor mode. The MON switch is disabled in all other environments. However, the ESC key on the console will stop operation and return to the operating system from any operation.

4.3 Rear Panel Switches

The microcomputer chassis has three toggle switches and one BNC connector on the back panel.

One switch is the main power-on switch for the microcomputer chassis.

Two sense switches are provided but are not used by any standard software.

The back panel on the microcomputer chassis has a standard 3-pronged AC power cable connector, and a BNC connector which allows the synchronization of an oscilloscope to a user selected system event. Refer to the pulse command described in the Z-80A CPU Emulator Software Manual for a description of oscilloscope synchronization.

4.4 External Cables

A flat ribbon cable is provided to interface the dual floppy disk unit to the CPU unit. This cable is connected to J107 of the CPU unit.

4.5 Monitor Mode

In Monitor mode, the operator can call for four operating system environments: Edit, Assemble, and Zap. Each of these environments has its own special command structure derived from the tasks it performs. Together, they comprise a very powerful and complete software and hardware development system that allows programs to be entered into memory, edited, assembled or compiled, filed on disk for future use, and loaded into memory for execution and emulation. The ZAP environment allows user programs to be loaded, executed, and quickly debugged.

4.6 Zilog Analyser Program (ZAP)

A major feature of the Z-80 Development System is its powerful debug capability. This capability allows selected emulator transactions to be stored into a special memory in real-time as the program is being executed by the emulator. The user can also specify that any type of system transaction, such as setting Bit 6 of Port 8BH, or reading from address 1C8H, can suspend execution of the user program and cause the system to re-enter the monitor mode. Then, a complete record of the last 256 bus transactions (which were recorded in a separate Real-Time Storage Module memory stack just prior to the suspension) can be conveniently displayed on the system terminal. This ability to store real-time event sequences and then to review selected events in detail permits the user to accomplish product design and hardware/software debugging in the shortest possible time.

4.7 Memory Mapping

A memory mapping function is provided that allows the user to define the specific nature of his memory address space. The 64K bytes of the user memory space is divided into 64 1K-byte blocks. Each block may be defined to exist in either the User System, the Development System, or to be non-existent. If a block is defined to be non-existent, then any access to that block causes a break in emulation. If a block is defined to exist in the Development System, then an address transformation may be specified. This address transformation allows a block of System memory to respond to an address other than the physical address assigned to that block.

Environment	Dynamic Memory Usage
Debug	Store user program
Edit	Edit software and file work space
Assemble	Assembler software and work space
ZAP	User program to be executed, RIO Operating System, and ZAP Operating System
OS	Executive Commands

4.8 I/O Ports

The Z-80 CPU can address up to 256 I/O ports. The following list shows how these ports are utilized in the basic ZDS-1/40. During an emulation, the mapping of I/O ports depends on the emulation clock that is selected. When user clock is selected, all ports exist only in the User System. When system clock is selected, all ports are in the development system.

ADDRESS	READ FUNCTION	WRITE FUNCTION
0FFH	BAUD RATE DETECTION	NOT USED
0FEH	STATUS PORT	NOT USED
0FDH	SOFTWARE SYSTEM RESET	SET USER MODE
0FCH	RTSM CONTROL PORT	RTSM CONTROL PORT
0FBH	BRKPT CONTROL PORT	BRKPT CONTROL PORT
0FAH	DISK CONTROL PORT A	DISK CONTROL PORT A
0F9H	DISK CONTROL PORT B	DISK CONTROL PORT B
0F8H	DISK DATA PORT	DISK DATA PORT
0F7H	SET MONITOR MODE	SET MONITOR MODE
0F6H	NOT USED	NOT USED
0F5H	USART CONTROL PORT	USART CONTROL PORT
0F4H	USART DATA PORT	USART DATA PORT
0F3H	SYSTEM CTC C3	SYSTEM CTC C3
0F2H	SYSTEM CTC C2 - BAUD RATE	SYSTEM CTC C2 - BAUD RATE
0F1H	SYSTEM CTC C1 - SER. CLK.	SYSTEM CTC C1 - SER. CLK.
0F0H	SYSTEM CTC C0 - DISK SECTOR	SYSTEM CTC C0 - DISK
0EFH	USER MEMORY MAP PORT	USER MEMORY MAP PORT
0EEH	USER INTERFACE CONTROL PORT	USER INTERFACE CONTROL PORT
0EDH	NOT USED	NOT USED
0ECH	NOT USED	NOT USED
0EBH	USER INTF. BREAK GEN.	USER INTF. BREAK GEN.
0EAH	USER INTF. WRITE PROT. ERR.	USER INTF. WRITE PROT. ERR.
0E9H	USER INTF. NO MEM. ERR.	USER INTF. NO MEM. ERR.
0E8H	USER INTF. BAD CLOCK ERR.	USER INTF. BAD CLOCK ERR.
0E7H	USER INTF. CASCADED CTC C3	USER INTF. CASCADED CTC C3
036H	USER INTF. CASCADED CTC C2	USER INTF. CASCADED CTC C2
0E5H	USER INTF. CASCADED CTC C1	USER INTF. CASCADED CTC C1
0E4H	USER INTF. CASCADED CTC C0	USER INTF. CASCADED CTC C0
0E3H	NOT USED	NOT USED
0E2H	NOT USED	NOT USED
0E1H	NOT USED	NOT USED
0E0H	NOT USED	NOT USED

SECTION 5

OPTIONS

5.1 The Peripheral Interface Board

The Zilog peripheral interface board (PIB) is a general purpose I/O board for interface to devices that accept data in a parallel format. The PIB contains two Z-80 PIO's with supporting logic to provide 32 bi-directional I/O bits. The card also contains plated through holes for insertion of a Z-80 CTC to provide four counter/timers channels.

The uncommitted PIO's and/or the user supplied CTC can be interfaced with the system daisy-chain priority interrupt structure. Unused space is provided with 16-pin dip locations (Vcc on pin 16, GND on pin 8) to allow additional logic at the user's discretion.

The four-bit dip switch determines the ports' address locations while additional control logic directs port transactions with the CPU system data bus.

The PIB can be configured for specific peripherals. The detailed logic description for each of the following configurations is provided separately.

- Printer Interface
- Paper tape reader/punch

5.2 The Auxiliary Serial/Parallel I/O Board

The Z-80 auxiliary serial/parallel I/O (ZDS/ASPIO) board provides the development system with one additional programmable serial communications interface and one additional programmable parallel interface. The serial interface is implemented with an 8251 universal synchronous/asynchronous receiver/transmitter (USART) to provide a RS232-compatible output. The parallel interface consists of the Z-80 PIO, which has been configured as a printer interface.

The USART is programmed by means of a control byte loaded by the Z-80 CPU. Controllable parameters include stop bits per character (1.0, 1.5, 2.0), bits per character (5-8), parity insertion/checking (odd, even, or none), and clocking of transmitted and received data at frequencies of 1, 16, or 64 times the data rates. The USART accepts data characters from the Z-80 in a parallel format and converts them into a continuous serial data stream for transmission. The USART can simultaneously receive serial data streams and convert them into parallel data characters for the Z-80.

The Z-80 PIO provides a software programmable, two port parallel I/O device for standard hardware interface between peripheral devices and the Z-80A CPU. The PIO contains two independent 8-bit ports with full handshake control that can be configured by the CPU to operate in any of four major modes. In the output mode (Mode 0), data is written to the ports from the Z-80 and onto the port data bus. In the input mode (Mode 1), the peripheral device supplies data to the port. The bidirectional mode (Mode 2) allows one port (Port A) to be bidirectional using the handshake signals from both ports. The control mode (Mode 3) allows for direct bit set and reset capability. This mode also allows any bit in either port to be individually programmed to be either an input bit or an output bit. Vectored interrupt communication with the CPU is included to facilitate data transfer. A unique feature of the PIO is that it can be programmed to interrupt the Z-80 CPU on the occurrence of specified status conditions in the peripheral device. One port has the ability to source a minimum of 1.5mA of current at 1.5 volts allowing Darlington transistors to be directly driven (for printer and high voltage displays, for example).

The CTC provides a data rate clock for the USART with all the common communication baud rates between 50 and 9600 baud. Unused area on the card is filled with plated-through holes on .10 inch centers for insertion of wire-wrap sockets.

SECTION 6

TECHNICAL DESCRIPTION

6.1 Introduction

The following sections describe the standard boards in the ZDS-1/40 system.

6.2A Processor Module Introduction (Schematics, page E-43) (09-0099-03 only)

The processor card contains a Z-80 CPU, Z-80 CTC and USART for console interface, plus 3K of PROM and 2K of static RAM for controlling the system environment. System PHI derives from a 19.6608 MHz quartz oscillator divided by eight. An additional 16.589 MHz oscillator is provided to the floppy disk controller for synchronous data separation. The CPU bus is fully buffered to support stand-alone system operation with full memory and I/O compliments. The relationship of these elements is represented in Figure 6.2-1, below.

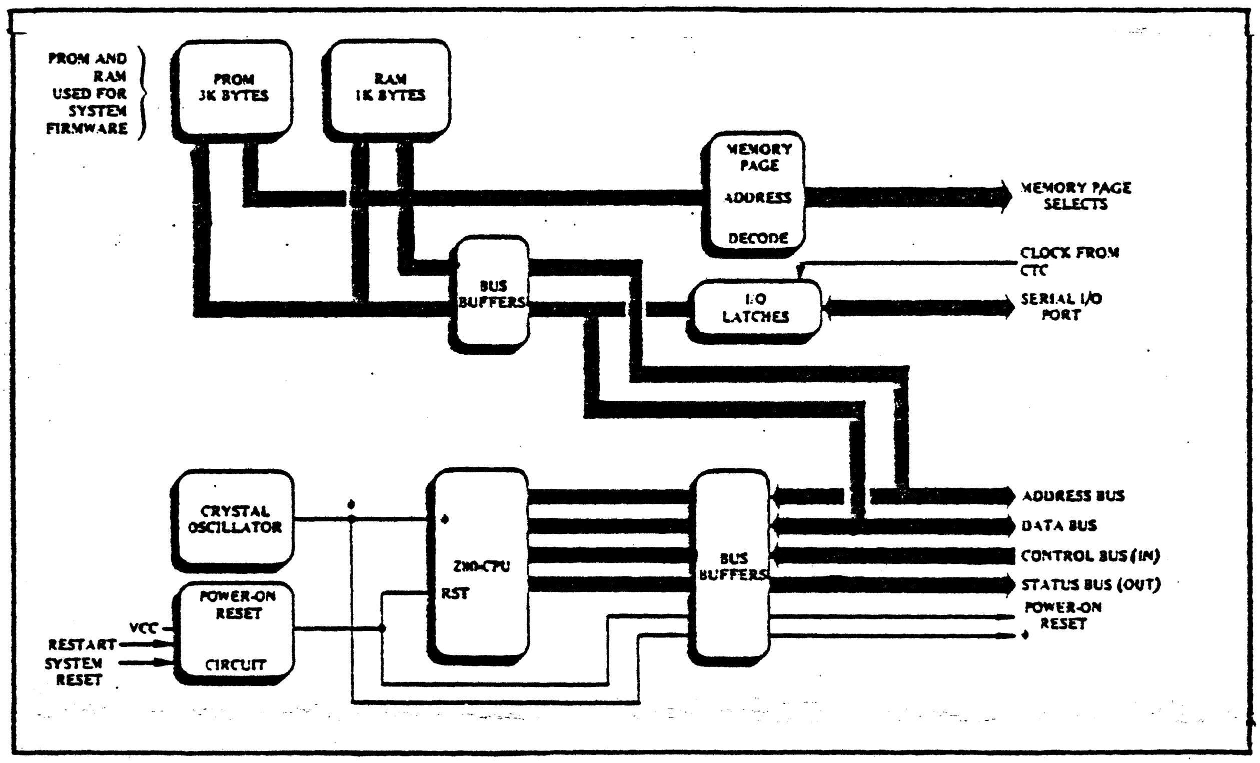


Figure 6.2-1. Processor Module Block Diagram

The Z-80 CPU bus buffers are shown on Sheet One of the schematics. System PHI is generated by hybrid oscillator A15. Counter A19 produces the 2.46 MHz system clock as well as half PHI for baud rate timing. The discrete circuit oscillator is controlled by a 16.589 MHz crystal and is used by the floppy controller's synchronous data separator.

Data bus buffers A35 and A36 interface the CPU to the system bus (backplane) and drive toward the CPU during M1 or Read cycles. Buffers A23 and A24 drive the system address bus. A30 drives outbound control signals such as M1, IORQ, RD, etc., while A32 receives inputs, e.g., INT, NMI, RESET, etc.

Zilog clock driver A21 provides a MOS-compatible clock source for the LSI devices.

Sheet Two depicts the address decoding assignments for the following:

Prom Firmware	F000H - FFFFH
Dynamic Memory	0H - EFFFH
System Ports	F0H - FFH

Adder A16 always translates addresses from 00H to F000H so that ROM is always in low memory (0000H - 0BFFH). Gate A17 generates the Page 15 address enable that allows access to PROM when user memory is mapped to system memory 0000H and when a system access is made to 0000H - 0BFFH. System I/O ports are decoded by the logic of A2 and A3.

Sheet Three of the schematics details the PROM/RAM implementation and the bus control logic for A33, A34, A35 and A36 buffers.

Chip selects for A9-A11, A1 and A2 occur when prom addresses are decoded by Sheet Two logic. These decoded addresses, along with I/O and interrupt requests from peripherals A20 and A8 (Sheet Four) cause bus drivers A35 and A36 to drive the system data bus toward the CPU. Automatic baud rate timing is acquired through tristate A18 and data bit D0.

Sheet Four contains the peripherals found on the CPU-3 card. The console interface is implemented by way of USART A8 and CTC A20. Highest priority in the daisy chain, the CTC provides interrupt capability for the floppy disk interface and the USART status lines. Jumpers E1 and E2 allow receiver interrupts from the USART. Flip-flop A4 provides a square wave baud rate clock source to the USART.

6.2B Processor Module Introduction (Schematics, pages E-31 through 42) (09-0099-02 and -01 only)

The processor card contains a Z-80 CPU, Z-80 CTC and USART for console interface, plus 3K of PROM and 2K of static RAM for controlling the system environment. System PHI is derived from a 19.6608 MHz quartz oscillator divided by eight. An additional 16.589 MHz oscillator is provided to the floppy disk controller for synchronous data separation. The CPU bus is fully buffer to support stand alone system operation with full memory and I/O compliments. The relationship of these elements is represented in Figure 6.2-1, above.

The Z-80 CPU bus buffers are shown on Sheet One of the schematics. System PHI is generated by hybrid oscillator A29. Counter A22 produces the 2.46 MHz system clock as well as half PHI for baud rate timing. The discrete circuit oscillator is controlled by a 16.589 MHz crystal and is used by the floppy controller's synchronous data separator.

Data bus buffer A31 interfaces the CPU to the system bus (backplane) and drives toward the CPU during M1 or read cycles. Buffers A26 and A23 drive the system address bus. A32 drives outbound control signals such as M1, IORQ, RD, etc., while A27 receives user provided inputs (e.g., INT, NMI, RESET, etc.).

Zilog clock driver A25 provides a MOS compatible clock source for the LSI devices.

Sheet Two of the schematics detail the PROM/RAM implementation and the bus control logic for both A31 and A16 buffers.

Chip selects for A17-A19, A13 and A14 occur when prom addresses are decoded by Sheet Three logic. These decoded addresses, along with I/O and interrupt requests from peripherals A20 and A21 (Sheet Four) cause bus driver A16 to drive the system data bus toward the CPU. Automatic baud rate timing is acquired through tristate A28 and data bit D0.

Sheet Three depicts the address decoding assignments for the following:

Prom Firmware	F000H - FFFFH
Dynamic Memory	0H - EFFFH
System Ports	F0H - FFH

Adder A34 always translates addresses from 00H to F000H so that ROM is always in low memory (0000H - 0BFFH). Gates A7 and A11 generate the page 15 address enable which allows access to PROM when user memory is mapped to system memory 0000H and when a system access is made to 0000H - 0BFFH. System I/O ports are decoded by the logic of A2 and A3.

Sheet Four contains the peripherals found on the CPU-2 card. The console interface is implemented by way of USART A21 and CTC A20. Highest priority in the daisy chain, the CTC provides interrupt capability for the floppy disk interface and the USART status lines. Jumpers E1 and E2 allow receiver interrupts from the USART. Flip-flop A8 provides a square wave baud rate clock source to the USART.

6.2.1 Reset Logic

A power-on clear sequence, or depressing the WAIT button on the front panel will reset the entire system to the Debug level, at which time an "S" character or a carriage return must be entered from the terminal to re-establish "handshake" with the system.

6.3 Hardware Breakpoint Module (Schematics, page E-59)

A block diagram of this module is shown in Figure 6.3-1. The type of transaction selected for the breakpoint, the specific address, and data mask are programmed through the ZAP software as the user issues terminal commands. The breakpoint module is addressed at CPU I/O Port FBH. The logic is designed so that successive writes to Port FBH will load all these program arguments via the system data bus into an internal data bus and then into various registers on this module according to the following sequence:

1st write: Load type of transaction (mode).
2nd write: Load data argument register.
3rd write: Load lower 8 bits of address argument.
4th write: (If memory transaction) Load upper eight bits of address argument.
5th write: Load data bus mask argument, if specified.

On Sheet 4 of the schematics, devices A7 and A14 make up the cycle counter that controls this loading sequence. A7 is a module 8 binary counter which increments on each cycle of its clock input. The clock input is, according to the logic on Sheet 3, merely an I/O port write request to Port FBH. As A7 increments, the five outputs of A14 go true successively to load the sequence of registers indicated above. All data loaded into these registers is buffered by A29 and A30 on Sheet 1. Then, in sequence:

1. One of five possible Control Bus Transactions is clocked into A21 on Sheet 3.
2. An 8-bit data word is clocked into A22 and A23 on Sheet 1.
3. The lower 8 address bits are clocked into A19 and A20 on Sheet 2.
4. The upper 8 address bits are clocked into A17 and A18 on Sheet 2.
5. The data mask register contents are clocked into A1 and A2 on Sheet 5.

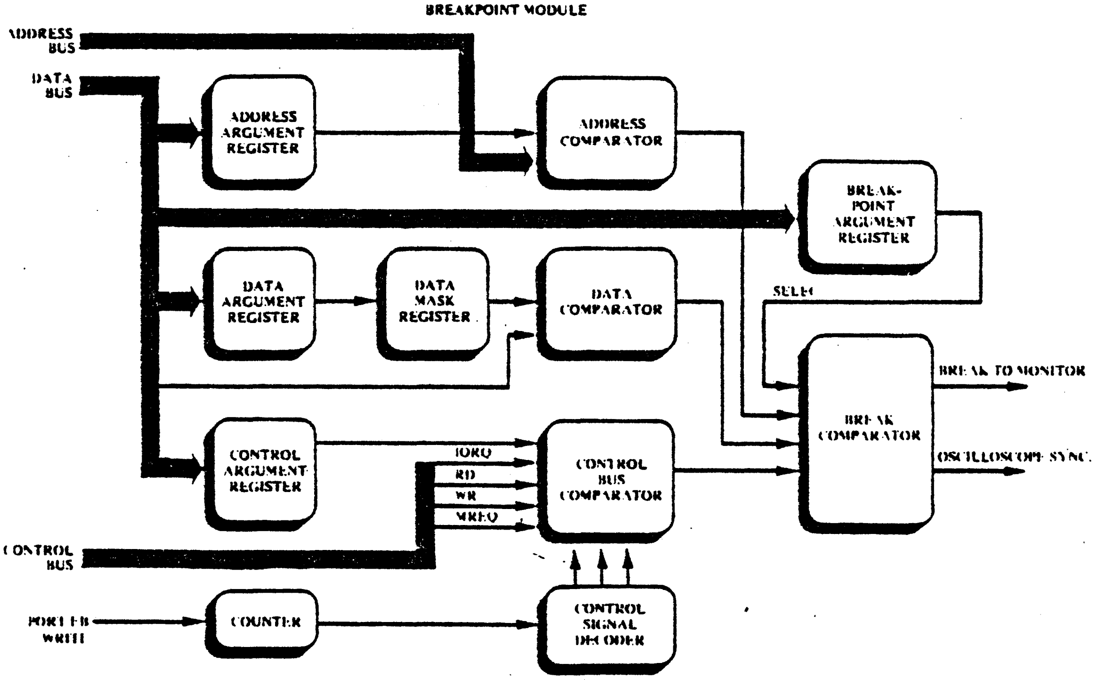


Figure 6.3-1. Hardware Breakpoint Module

Thus, when program execution begins under emulation, the contents of these registers are compared with the current states of the system address, data and status/control busses, and true compares will generate breakpoint and scope sync output signals on Sheet 4.

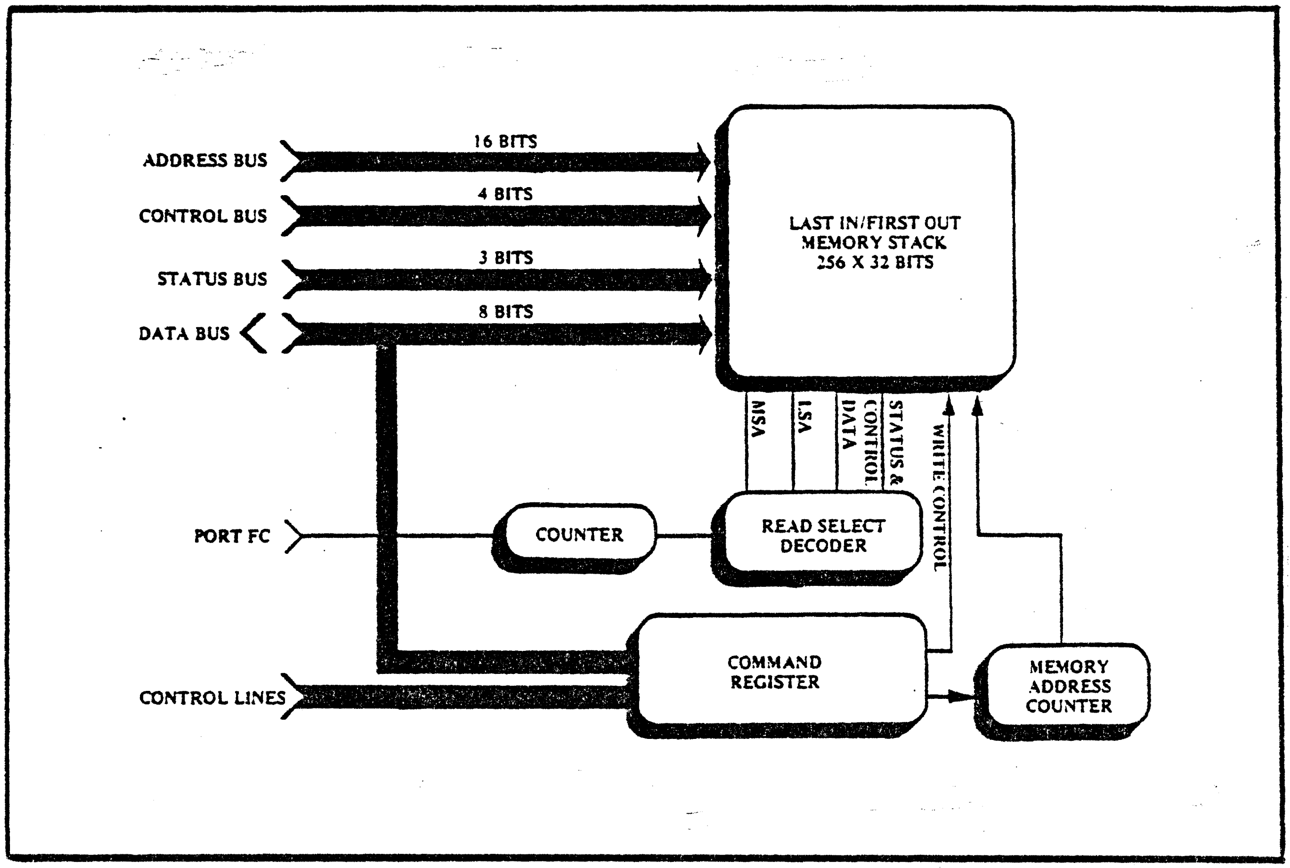


Figure 6.3-2. Real-Time Storage Module

6.4 Real-Time Storage Module (RTSM2) (Schematics, page E-67)

The general layout of this card is shown in Figure 6.3-2. Sheet 2 of the schematics contains 2101-1 RAMs for the push-down stack. The 16 address bits are stored after they are clocked through latches A30, A31 and A32. A19 and A17 on Sheet 2 store the 8 data bits via latches A27 and A25, while A18 and A20 on the same sheet store the control and status bits, respectively.

Register A9 on Sheet 1 will be loaded with selected bits to indicate which type(s) of transactions will be stored, and the AND gate A3 will pass a WRITE DATA signal to the RAMs any time such a transaction is detected on the system control bus.

Sheet 1 contains the counter that generates the addresses for the 256-word stack. After the breakpoint is reached and the system returns to the debug environment, the contents of the stack can be read out for printing via buffers A28 and A29 on Sheet 1.

6.5 Monitor Module (Schematics, page E-19)

This board performs several independent functions which will be detailed.

Sheet 2 of the monitor schematics contains the circuitry to interface both TTY or RS232 terminals to the serial TTL I/O data streams generated and received by the CPU module. (Schematics, page 152)

On Sheet 2 of the monitor schematics, A30, A31, and A32 comprise I/O port decoders, which turn an address on the lower 8 bits of the address bus into enables for various I/O device control or data functions.

Sheet 1 contains the lamp drivers for the four front panel lamps. Also, a buffer (A25) is enabled whenever an I/O read is performed to Port FEH. This will drive the following "System Status" information onto the system data bus: the state of the MON and USER front panel switches (via debounce latches), the state of the two rear panel sense switches, and the BREAK STATUS signal from the breakpoint module. At the bottom of Sheet 1 is logic to turn breakpoint signals from any sort of change of mode into proper timing signals for the POD CONTROLLER.

6.6 64K Memory Module (Schematics, page E-25)

The Z-80 Development System contains one memory module consisting of 64K bytes.

6.6.1 System Memory Organization

The memory is partitioned into sixteen 4K byte pages. Page 0 begins at address 0000H, page 1 at 1000H, etc. (See Figure 6.6.1-1.) Page 0 consists of the 4K bytes of system firmware.

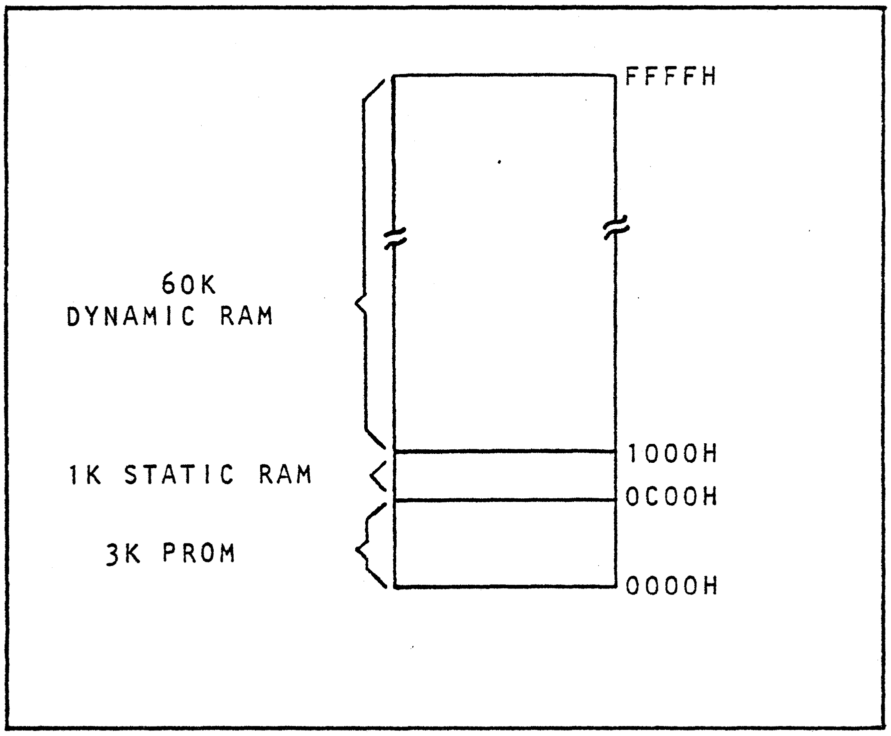


Figure 6.6.1-1. System Memory Organization

6.6.2 Interpretation of Schematic (64K MEMORY)

Sheet 2 contains bi-directional data buffers, with each bit divided into a Data In and a Data Out line on the storage array side of the buffer, to effect the required division of these two signals on the memory chip itself. The other side of the buffers connects to the system data bus.

Sheet 2 also depicts multiplexers used to split the 14 address bits into two 7-bit segments, in accordance with the requirements of the 16-pin 16K memory chips.

Sheet 1 contains the 60K strapping options. The discussion to follow will assume that the board is wired for 60K capacity. This sheet contains the logic for generating the RAS (Row Address Strobe) and CAS (Column Address Strobe) signals. At the memory chip, the RAS signal latches in the seven least significant address bits from the multiplexer on Sheet 2; then, after sufficient delay to change the select on this multiplexer, the seven most significant address bits are latched into the memory chip by CAS.

There are four different RAS signals to select a different group of memory chips for each of the four PS (Page Select) signals. These PS signals are generated on the processor module from card select (CD) signals, and only one of the four will be true for any particular memory request. The PS signal is buffered by multiplexer All, and will be passed through Al and A2 when MRQ (Memory Request) timing signal is true. The resulting signal is one of four possible RAS signals. In a Memory Refresh operation, all four RAS signals will be enabled.

The buffer A5 on the lower right causes a delay that allows the RAS to latch the first seven address bits; later, a control signal changes the select on the address multiplexer. After further delay, CAS is generated to latch the most significant address bits.

Sheet 3 contains the memory array, organized 4 x 8, to correspond to the four different RAS (page select) signals and to the eight bits per data word.

6.7 Floppy Disk Controller (Schematics, page E-49)

The Z-80 Development System utilizes a dual Shugart 801 floppy disk drive for bulk storage of data and operating programs. The controller is designed to use 32 sectors (records) per track and 77 tracks per disk. It provides all control functions for two disk drives. The controller's operations are facilitated by the fast interrupt response of the CPU, the programmable timing features of the CTC module, and the Z-80 I/O block transfer capability.

6.7.1 Data Format

All formatting of the data on the disk is accomplished under the control of the CPU. Figure 6.7.1-1 represents the formatting structure: 16 bytes of all zeros for the preamble; one byte for sector address with the first bit being a start bit; one byte for the track address; then 128 bytes of data; 4 bytes of linkage (forward/backward) for file maintenance; 2 bytes of CRC; and then a postamble of all zeros.

6.7.2 Sector Recording Format

In this format, the user may record up to 32 sectors (records) per track. Each track is started by a physical index pulse, and each sector is started by a physical sector pulse. This type of recording is called hard sectoring.

6.7.3 Tracks

The Shugart drive is capable of recording up to 77 tracks of data. The tracks are numbered 0-76. Each track is made available to the read/write head by accessing the head with a stepper motor and carriage assembly.

Basic Track Characteristics	Unformatted	Formatted
Number bits/track	41,300 bits	32,768
Index pulse width	1.7+/-.5 ms	
Index/sector pulse width	.4+/-.2 ms	

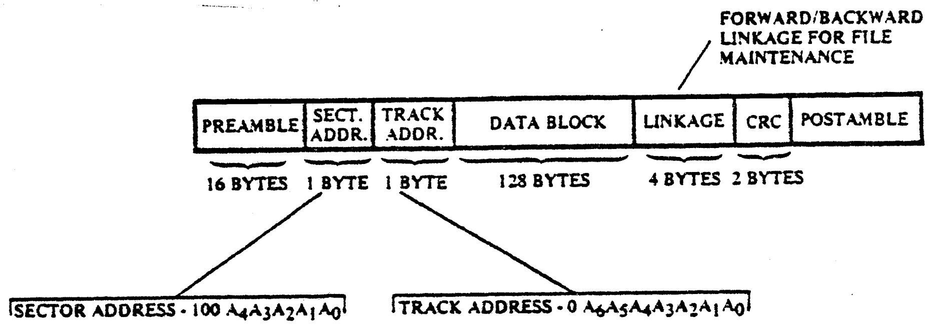

FORWARD/BACKWARD LINKAGE FOR FILE MAINTENANCE
PREAMBLE
SECT. ADDR.
TRACK ADDR.
DATA BLOCK
LINKAGE
CRC
POSTAMBLE
16 BYTES
1 BYTE
1 BYTE
128 BYTES
4 BYTES
2 BYTES
SECTOR ADDRESS - 100 $A_4A_3A_2A_1A_0$
TRACK ADDRESS - 0 $A_6A_5A_4A_3A_2A_1A_0$

Figure 6.7.1-1 DISK FORMAT

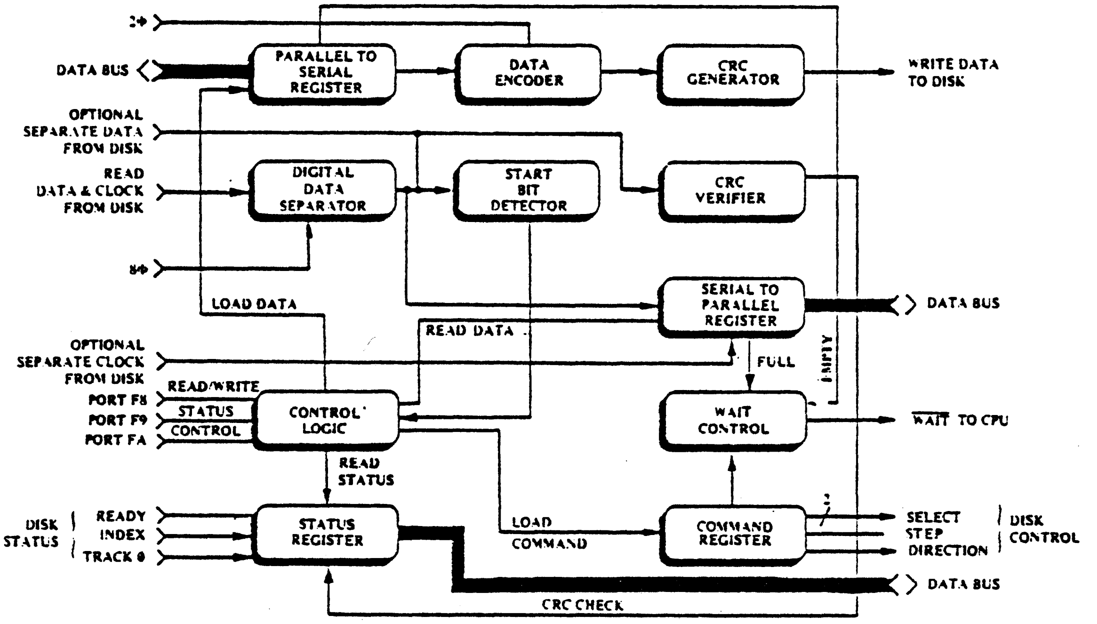


Figure 6.7.4-1. Floppy Disk Controller

6.7.4 Controller Functional Description

Zilog's simple controller, which interfaces the disk drives, is diagrammed in Figure 6.7.4-1. The controller enables the user to store or retrieve information from any one of the disk drives under its control. Under Z-80 CPU control, it positions the head carriage assembly at the desired track; locates the field of interest; and either writes or reads. Read/Write transfer of data takes place through the Z-80 CPU I/O channel. The controller's basic functions are read data separation, write data assembly, and parallel/serial data conversion.

1. ERROR CONTROL: The controller includes a CRC generator and checker to insure that all data has been properly recorded and retrieved from the disk. During a write data assembly, a 16-bit CRC is appended by the controller as the last two bytes of data. During Read operations a hardware check on the 16-bit CRC code is performed and the result is

monitored by the CPU. Every sector of disk data contains its own sector and track address. The CPU checks this address after every Read operation to insure that it was correct.

2. CONTROL AND STATUS: The status register permits the controller to advise the CPU of the condition of the disk via Port F9H by monitoring Ready, Index, Track 0, and CRC check.

   Port F8H is used to control the desired disk through the select, step, and direction lines.

3. WRITE DATA: Write Data is latched from the CPU into the parallel-to-serial shift register and shifted out to the CRC generator and on to the data encoder where it is gated with the 2-phase clock signal, at the rate of one clock time per bit cell.

4. READ DATA: The combined Read Data and Read Clock are gated into the data separator with the 8-phase clock. The data is separated from the clock and fed into the start bit detector to sense the end of all zero preamble. Upon detection of the first bit in the sector address byte, the data is fed into the serial-to-parallel register and out to the CPU data bus.

5. WAIT: In order to match the disk transfer rate and the CPU software transfer rate, it is necessary to slow down the instruction execution time of the processor through the use of the WAIT line. The WAIT control logic performs this function.

6.7.5 Recording Format

The format of the data recorded on the diskette is totally a function of the system resident firmware. Data is recorded on the diskette using frequency modulation as the recording mode; i.e., each data bit recorded on the diskette has an associated clock bit recorded with it. This is referred to as FM. Data written on and read back from the diskette takes the form shown in Figure 6.7.5-1. The binary data pattern shown represents a 101.

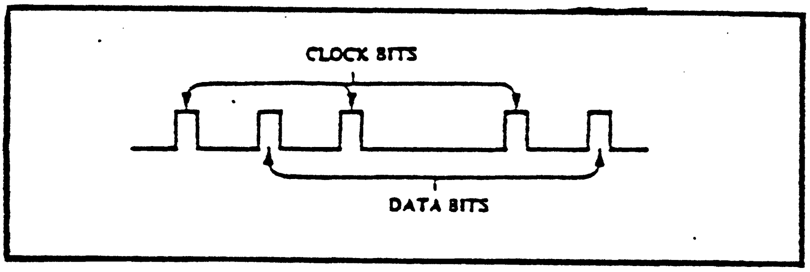


Figure 6.7.5-1. Data Pattern

a. BIT CELL - As shown in Figure 6.7.5-1, the clock bits and data bits (if present) are interleaved. By definition, a bit cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit.

b. BYTE - A byte, when referring to serial data (being written onto or read from the disk drive) is defined as 8 consecutive bit cells. The most significant bit cell is defined as bit cell 0, and the least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During a write operation, bit cell 0 of each byte, is transferred to the disk drive first with bit cell 7 being transferred last. Correspondingly, the most significant byte of data is transferred to the disk first, and the least significant byte is transferred last.

When data is read back from the drive, bit cell 0 of each byte will be transferred first with bit cell 7 last. As with writing, the most significant byte will be transferred first from the drive to the user.

Figure 6.7.5-2 illustrates the relationship of the bits within a byte, and Figure 6.7.5-3 illustrates the relationship of the bytes for read and write data.

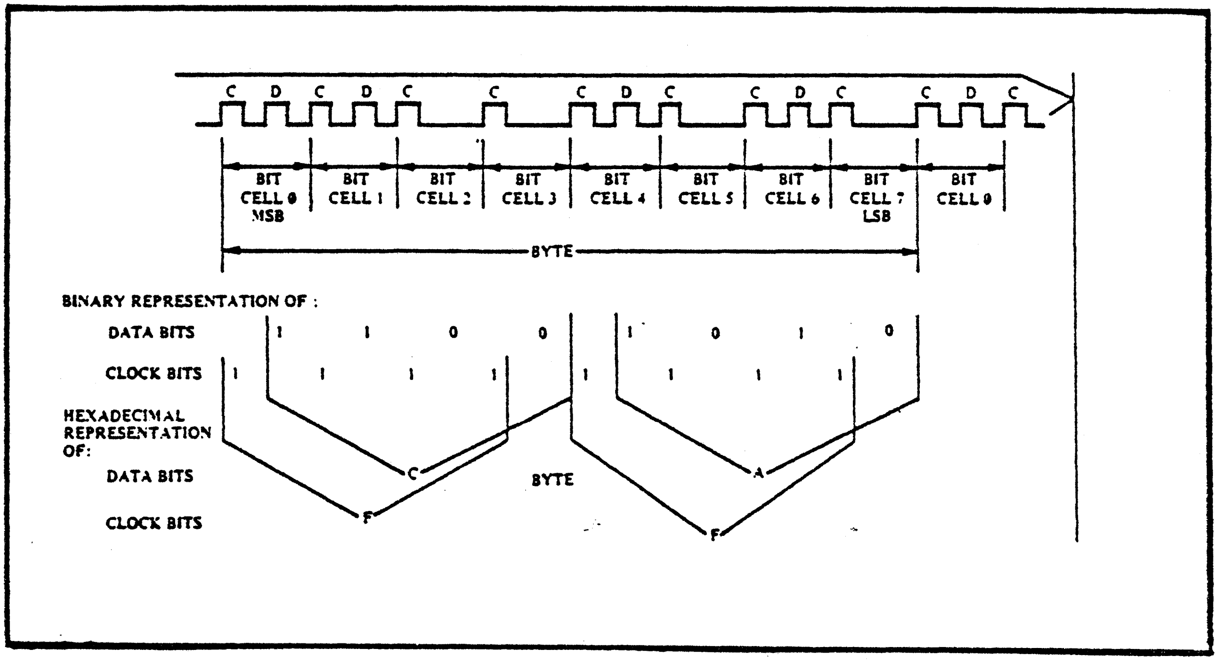


Figure 6.7.5-2. Bits Within a Byte

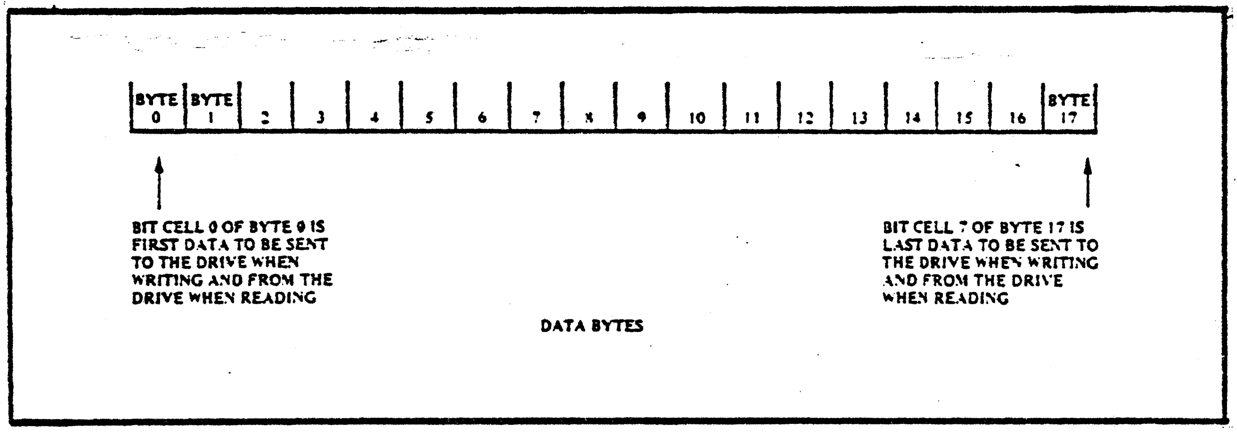

BYTE 0
BYTE 1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
BYTE 17
BIT CELL 0 OF BYTE 0 IS FIRST DATA TO BE SENT TO THE DRIVE WHEN WRITING AND FROM THE DRIVE WHEN READING
BIT CELL 7 OF BYTE 17 IS LAST DATA TO BE SENT TO THE DRIVE WHEN WRITING AND FROM THE DRIVE WHEN READING
DATA BYTES

Figure 6.7.5-3. Data Byte Relationships

6.8 Z-80A CPU Emulator Sub-System (Schematics, pages E-1, E-7, E-15, E-17)

The purpose of the Development System Z-80A CPU Emulator is to permit real-time analysis and debugging of hardware and software systems. This tool presents the user with a minimum number of restrictions while providing him with a maximum number of capabilities.

6.8.1 Introduction

The Z-80A CPU emulator module for the Development System consists of three sub-assemblies: the User Pod Controller, the User Pod, and the Emulator. The User Pod Controller is housed in the Development System and provides an interface between the User Pod/Emulator and the Development System. The User Pod is an integral part of the six-foot user cable and contains all time critical Emulator control logic and buffers to interface the Emulator to the user cable. The Emulator is a special version of the Z-80A CPU that replaces the Z-80 CPU or Z-80A CPU in the User System. It should be noted that only CPU activity, which is performed by the Emulator, is tested for break conditions and is stored in the real time storage module. The entire system is shown in Figure 6.8.1-1 while block diagrams of the User Pod and User Pod Controller are shown in Figures 6.8.1-2 and 6.8.1-3. The major features of the system are:

1) The system is capable of real-time debug of systems with a CPU clock rate up to 4MHz.

2) The only deviations from an actual CPU are an additional 200 microampere, 30 picofarad load and a maximum low level output voltage of 0.51 volts.

3) Disk-based debug software that allows the user complete visibility into the operation of the hardware/software system.

4) Uses real time storage module to record the data bus, address bus, and control bus status during the most recent 256 bus transactions.

5) Uses breakpoint module to monitor and test for user specified condition on the data bus, address bus, and control bus.

6) Memory mapping and protection in blocks of 1024 bytes.

7) Hardware check of user clock integrity.

8) User system dynamic RAM refresh is maintained while emulation is halted.

6.8.2 Capabilities

The Z-80A Emulator module is designed to allow the user to set and display any memory location in user memory space, set and display any I/O port in the user I/O space, or set and dsplay the current status of the Emulator.

A memory mapping function is provided that allows the user to define the specific nature of his memory address space. The 64K bytes of the user memory space are divided into 64 1K-byte blocks. Each block may be defined to exist in either the User System, the Development System, or to be non-existent. If a block is defined to be non-existent, any access to that block causes a break in emulation. If a block is defined to exist in the Development System, then an address transformation may be specified. This address transformation allows a block of Development System memory to respond to an address other than the physical address assigned to that block. As an example, assume that the memory block in the user space defined by the range FCOOH to FFFFH is mapped into the Development System memory block 1000H to 13FFH. When the User System accesses memory at address FC20H, the Development System memory at 1020H will respond. This memory mapping function also allows any 1K block to be write-protected. When a block is write-protected, all writes to that block are inhibited. In addition, the user may specify that a break be generated when a write is attempted on a protected block. A map specified for an emulation applies to all memory accesses made during that emulation regardless of what generates the memory access request. This means that the map is used by all devices in the User System that access user memory; DMAs, other CPUs, and the emulator, provide that the user system design responds properly and buffers are bi-directional.

The user may select to run on either the internal (system) clock (2.5MHz) or an external (user) clock. The clock signal is monitored and a break is generated if the clock fails to meet minimum frequency specifications (250KHz). The addressing of the user I/O space is determined by the clock and the system mode that has been selected as described in Figure 6.8.2-1. The purpose of allowing the emulator module to operate with the Development System clock is to insure that software programs can be debugged using the real time storage module and breakpoint module.

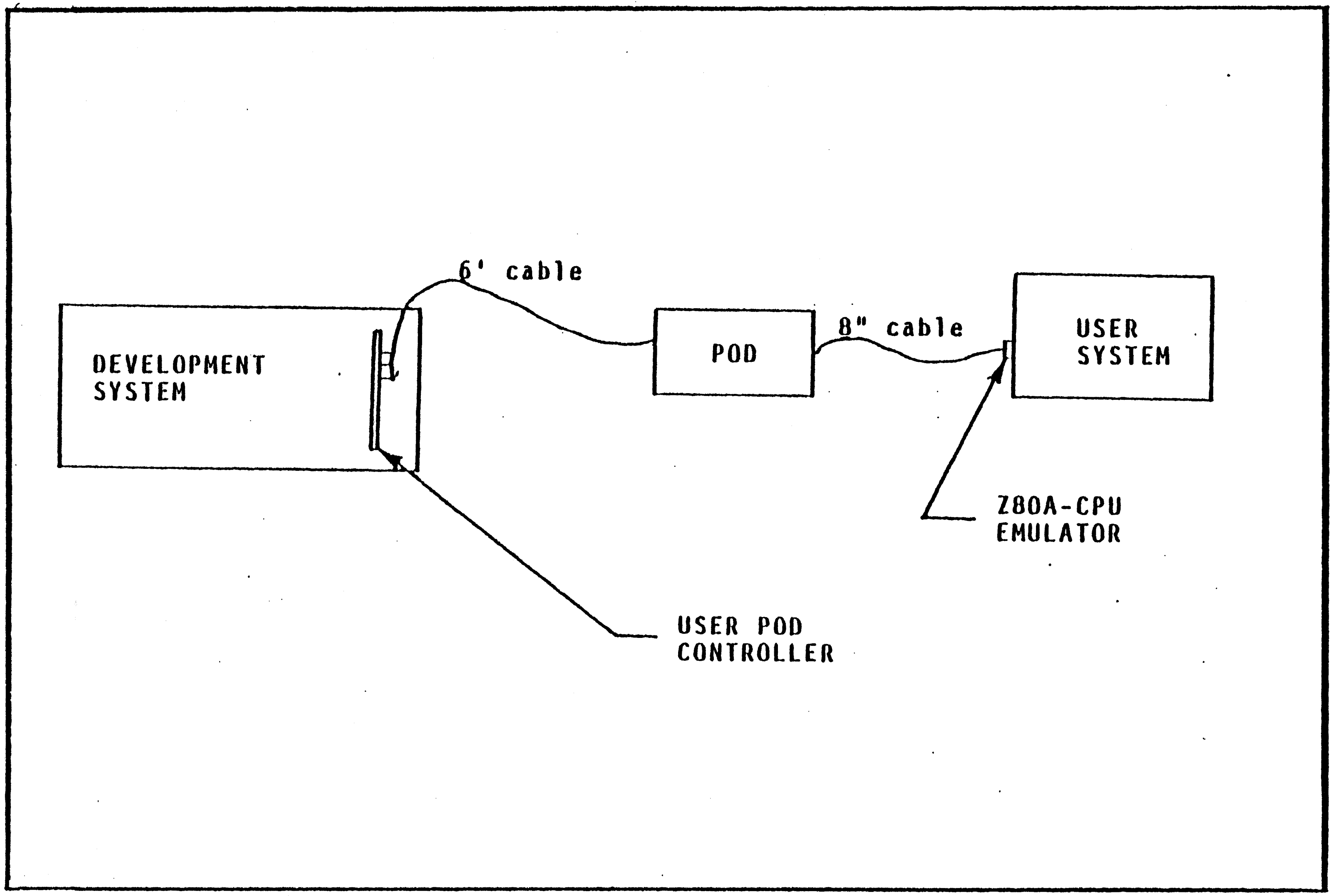


FIGURE 6.8.1-1

Z80A CPU EMULATOR MODULE DIAGRAM

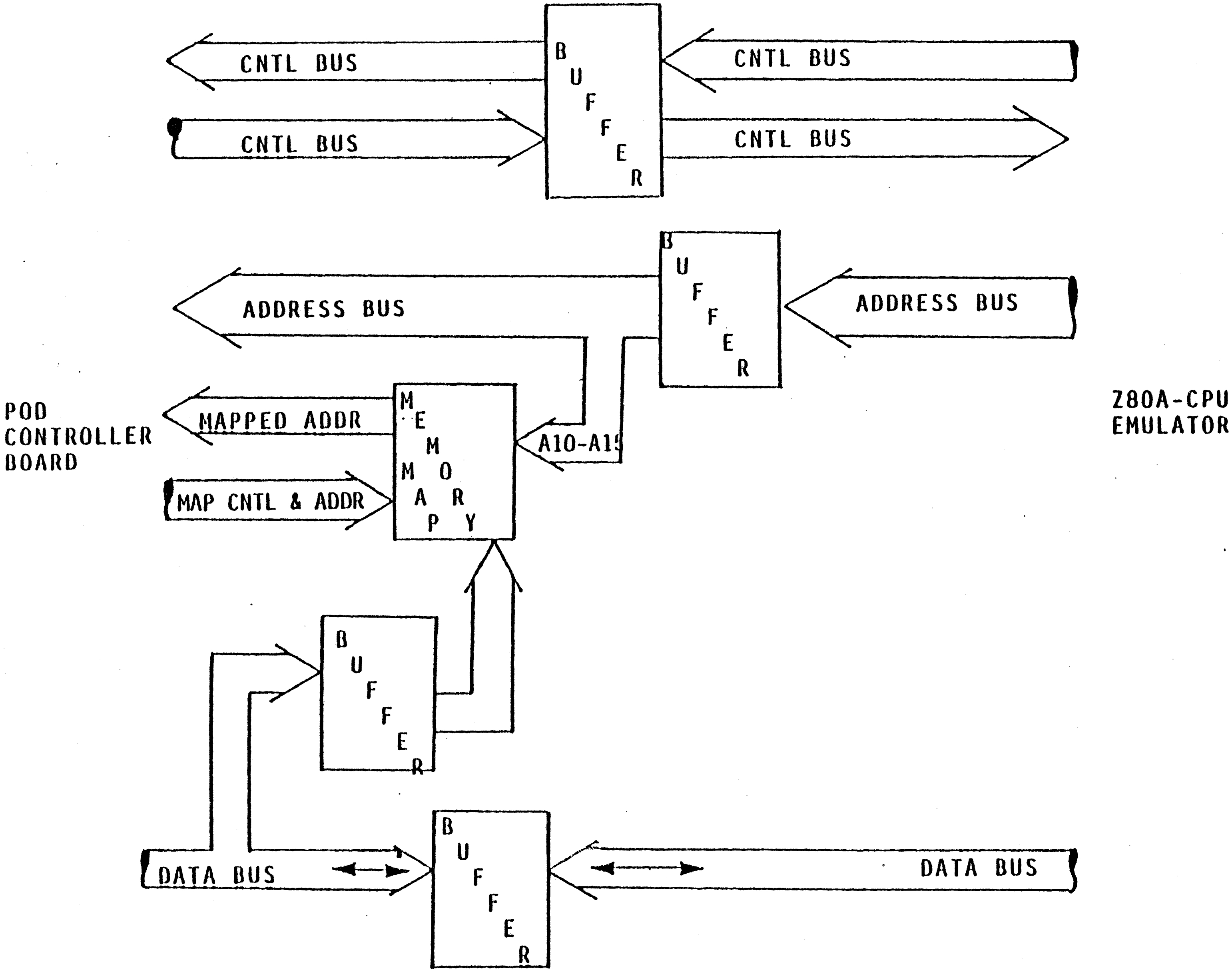


FIGURE 6.8.1-2

POD BLOCK DIAGRAM

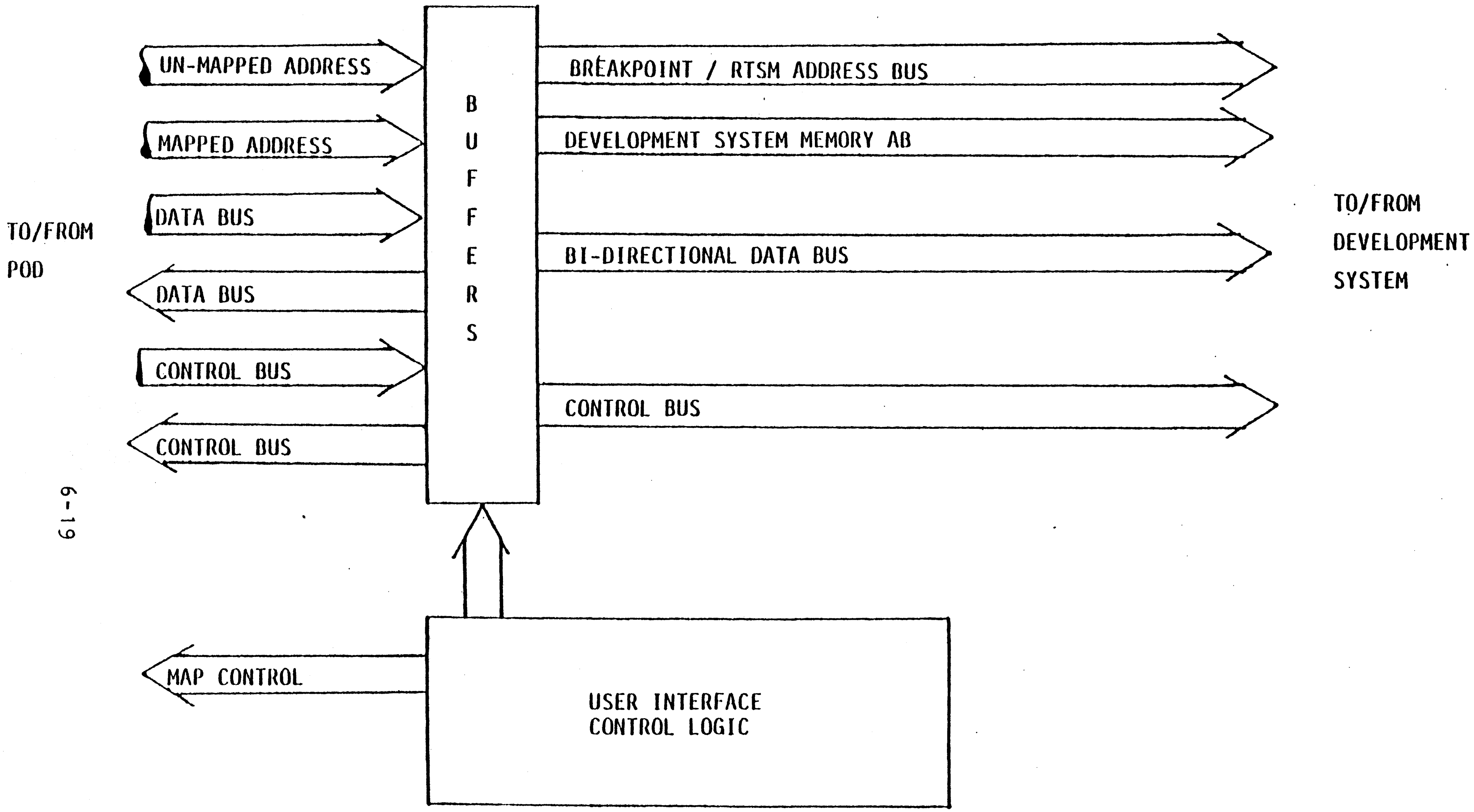


FIGURE 6.8.1-3

USER POD CONTROLLER BLOCK DIAGRAM

MONITOR MODE	USER MODE	
All I/O in DS E0-FF used	All I/O in DS E0-FF used	SYSTEM CLOCK
All I/O in User System except EE & EF	All I/O in User System	USER CLOCK

Figure 6.8.2-1.

6.8.3 Architecture

The Z-80A CPU Emulator module described in this document is designed to replace Zilog's original user interface, in those applications requiring 4MHz emulation. This new Emulator module contains an emulator to emulate either a Z-80A CPU or a Z-80 CPU in the User System. The Emulator appears to the User System as a Z-80A CPU with a 200 microampere load, 30 picofarads additional input capacitance and an increased maximum oputput low voltage. (Maximum Vol = 0.51 volts. Maximum high level load = 20 microampere. Maximum low level load = 200 microampere.) The only CPU allowed to access the user memory or I/O space is the emulator. While few changes were required on the breakpoint module and the real time storage module, the modules have been removed from the Development System bus and placed on a special bus driven by the User Pod Controller. Because the pinout of the User Pod Controller is completely different from the user interface, the entire J1 connecter has been re-wired. In addition, the monitor module has been modified so that the MON button generates a manual break for the debug software. The User button has been disabled so that the only way to start an emulation is through the debug software.

6.8.4 Restrictions

The User System must not prevent the Development System memory from being refreshed. As an example, the User System may not perform an extended DMA operation that does not generate memory request and refresh. This restriction can be eliminated by replacing the standard Development System dynamic RAM with an optional static RAM memory module.

When a portion of the user memory space is mapped into the Development System, some WAIT states may be inserted to insure that data reaches the emulator. This means that emulation may not be in real-time if memory is mapped into the Development System. Since the duration of the WAIT state is determined only by the emulator module delay and the Development System memory access speed, no WAIT state is required by user hardware operating with low frequency CPU clocks while several WAIT states are required by user hardware operating with high frequency CPU clocks. The number of wait states will be minimized with the use of the optional high speed static RAM board.

The emulator module is designed not to restrict the maximum frequency of the user's CPU clock, but the real time storage module (RTSM) and the breakpoint module will only operate up to 4MHz.

The Emulator module makes one restriction on the User System design. When memory is to be mapped into the Development System, then the User System memory and data bus buffers must remain inactive when Memory Request is inactive. The Emulator will not issue a MRQ- to the user system when Development System memory is accessed. In addition a special signal, called System Memory Access, is provided to the user to disable his memory and data bus buffers. It should be noted that system level emulations are performed to display, and set memory, or, to display and set registers. When these emulations are run, a portion of Development System memory is automatically mapped into the User Memory space; therefore, ZAP will not run properly if this design restriction is violated.

6.9 Hardware Overview

The Z-80A Emulator Module for the Z-80 Development System consists of three sub-assemblies: the User Pod Controller, the User Pod, and the Emulator. The User Pod Controller contains the control and interface electronics necessary to interface the Z-80 Development System to the User Pod. The User Pod contains the cable buffer-drivers and time critical electronics required to interface to the emulator. The emulator is a special Z-80A CPU which replaces the Z-80 CPU or Z-80A CPU in the system under development. The Z-80A Emulator Module is shown in Figure 6.9-1. This configuration allows in-circuit emulation of the microprocessor in all systems developed around the Z-80 and Z-80A families of microprocessor and support devices.

The following signal naming convention has been used through out this document. All signal names are written in upper case letters and match the names used on the logic diagrams. Negative true (active low) signals are indicated by appending a minus sign to the end of the name. For example, CPU AB 0 is a positive true (active high) signal derived from address bus bit 0 of a CPU. A logic 1 is represented by a voltage greater than 2.4 volts. Similarly, CPU RD- is a negative true (active low) signal derived from the read line of a CPU. A logic 1 is represented by a voltage less than 0.8 volts.

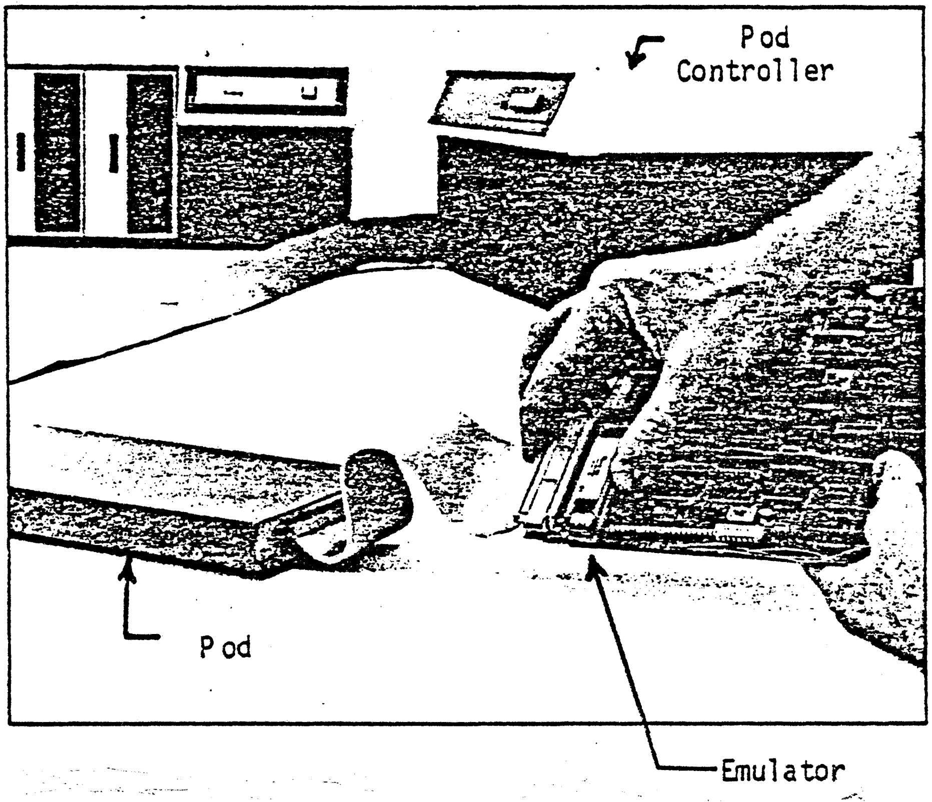


Figure 6.9-1. User Pod, Pod Controller and Emulator Relationships

SECTION 7

THE EMULATOR

7.1 EMULATOR (Schematics, page E-15)

The emulator supplied with the Z-80A CPU Emulation Module may be configured to operator in three modes: Software System, Hardware System-User Clock, and Hardware System-System Clock. The Software System emulator obtains power and clock from the Development System and is not intended to be inserted into a User System. The Hardware System-User Clock emulator obtains power and clock from the User System and is intended to replace the Z-80 CPU or Z-80A CPU in the User System. The Hardware System-System Clock emulator obtains power from the User System and clock from the Development System and is also intended to replace the CPU in the User System. While Hardware System-System Clock emulator makes the selected clock available to the User System on the clock pin of the emulator (Pin 6), it is provided only for the early phases of system debug when clock loading is light. It must be remembered that the clock that is selected by the emulator determines what I/O ports are available to the system being developed. When System Clock is selected, all I/O ports exist in the Development System and ports E0 hex through FF hex are used by the Development System. When user clock is selected all ports are located in the User System.

MONITOR MODE	USER MODE	
All I/O in DS E0-FF used	All I/O in DS E0-FF used	System CLOCK
All I/O in User System except EE & EF	All I/O in User System	USER CLOCK

The emulator consists of a Z-80A CPU emulator and a shielded interface cable. The Z-80A CPU emulator is a special version of a Z-80A CPU with the following characteristics:

1) Program execution can be stopped at any time.

2) Dynamic RAM is always refreshed.

3) The CPU can execute from either "User Memory" or "System Memory".

4) When stopped, the status of all registers can be determined.

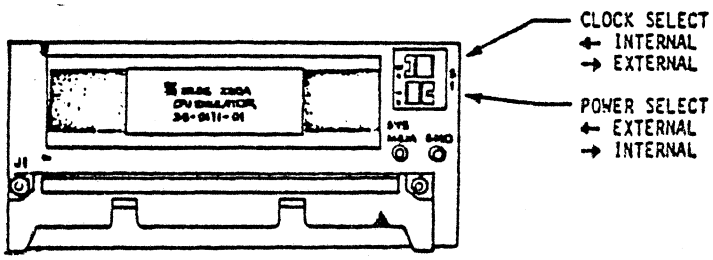
5) Timing characteristics identical to a Z-80A CPU.

6) AC/DC characteristics identical to a Z-80A CPU with the following maximum variations on all pins:

   20 microampere high-level preload
   200 microampere low level preload
   30 picofarad capacitive preload
   0.51 volts output low voltage

7.2 Z-80A CPU EMULATOR (Schematic, Page E-17)

This schematic shows the logic contained in the hybrid Z-80A CPU emulator. This hybrid is a Z-80A CPU with externally controlled MOS-FET switches to permit the control of BUSRQ-, INT-, NMI-, MRQ-, and WR-. Since it is necessary to shut off MRQ- and WR- when they are active, an active pull-up has been added. The three transistors in the WAIT- path form an OR gate that combines the USER WAIT- and the SWITCH WAIT- generated by the system.



SECTION 8

THE USER POD

8.1 USER POD (Schematics, page E-7)

The primary purpose of the User Pod is to provide buffers that isolate the six-foot user cable from the Emulator. In addition, the User Pod contains the logic that maps memory and the logic that stops the Emulator. Hysteresis buffers (74LS240-74LS244) have been used for both drivers and receivers to maximize noise immunity and minimize loading and power dissipation. All cable drivers use series terminations to further reduce power dissipation. These drivers and receivers are shown on Sheets 1 through 5 of the User Pod logic diagram. Three state buffers (74LS125 - shown on Sheet 3) permit the Development System or User Pod Controller to generate WAIT-, BUSRQ-, RESET-, and NMI for the User System. The clock driver (A25) used to supply the Emulator with system clock is also shown on Sheet 3.

The Emulator is stopped by forcing it to execute a jump relative instruction with an offset of -2 (18 hex, FE hex). This instruction keeps the program counter of the Emulator from being advanced while keeping the dynamic memory of the User System refreshed. This instruction sequence is generated by the read-only memory (7603) at location A1, shown on Sheet 1, when the Emulator module is idle. During this time, the control logic at the top of Sheet 5 and on Sheet 6 drives WR ENA and MRQ ENA to the inactive state (low). These two control signals cause the Emulator to stop issuing MRQ- and WR- to the User System, thus disabling all read and write operations on the User Memory. In the event that the memory of the User System would respond without these signals, a SYS MEM ACCESS signal is made active (high) and available on the Emulator so that the User Memory may be disabled when the Emulator is idle or accessing memory mapped into the Development System. The Emulator always issues MRQ- during the refresh portion of the M1 cycles.

The exact nature of the User Memory space is stored in a static random access memory located at A7 (shown on Sheet 4). When this memory map is read or written, it is accessed through port 0EFH. The 64 bytes of storage in the RAM are treated as 64 registers within the single I/O port. The address lines for this RAM are multiplexed between the Emulator trace address lines and the map address lines supplied by the User Pod Controller. The state of this multiplexer is controlled by the MAP SEL bit of the control port (bit 1, port 0EEH) located on the User Pod Controller.

For proper operation of the mapping logic, the MAP SEL bit must be reset (0) when the Emulator is running an emulation.

During an emulation, the six high order address bits are used to access the map RAM, thus permitting each 1024-byte block of user memory to be given one of the attributes listed below.

1) Nonexistent: no access is permitted; a break is generated if access is attempted.

NOTE: The instruction involving the access is completed before the break is generated; therefore, an invalid instruction may be executed.

2) User: read/write access is permitted.

3) User/write protected: read access is permitted; write access is not permitted and will generate a break if the WP INT ENA bit of the User POD Controller control port is set (Bit 3, Port 0EEH).

4) System <n>: Development System memory block <n> is accessed instead of this User Memory block; read/write access is permitted; some wait states may be inserted to adjust for cable delays.

5) System block <n>/write protected: Development System memory block <n> is accessed instead of this user memory block; read-only access is permitted while write access is not permitted and will generate a break if the WP INT ENA bit of the User POD Controller control port is set (Bit 3, Port 0EEH).

NOTE: In the case of a write access to a write protected block of memory the WR- signal does not go active. As a result, the memory sees a memory access cycle with only MRQ- active (neither RD- or WR- are active), and no entry will be entered in the history.

NOTE: All operations using the User System Address Bus are affected by the memory map RAM, since the User Address Bus is used to address the RAM. This means that DMA (direct memory access) operations may bus request the Emulator and use the same memory space of their operation, but if the User System design uses uni-directional buffers on the Z-80 CPU address bus of the Z-80 CPU, then addresses generated by DMA or other processors cannot reach the map RAM, and no mapping will be performed.

SECTION 9

THE USER POD CONTROLLER

9.1 USER POD CONTROLLER (Schematics, page E-1)

The User Pod Controller provides all the control logic for the User Pod as well as the receiver-drivers used to interface the User Pod to the Development System. Here again, hysteresis buffers were used (74LS240-74LS244) to minimize power and maximize noise immunity. Control functions performed by the User Pod Controller include detecting invalid memory access (nonexistent memory or write protect violations), starting and stopping an emulation, verifying the integrity of the clock, adding wait states to adjust for cable delays, and generating break request interrupt vectors.

The table below summarizes the port assignments in the User Pod Controller. Each of these ports is discribed in greater detail in the sections that follow.

Table 9-1. User Pod Controller Port Assignments

Ports E4-E7 (Hex)	Four cascaded CTC channels for emulation time-out breaks and instruction-counting breaks (cascaded 0-1-2-3).
Port E8 (Hex)	CTC Channel Zero; bad clock interrupt generator.
Port E9 (Hex)	CTC Channel One; non-existent memory interrupt generator.
Port EA (Hex)	CTC Channel Two; write-protect violation interrupt generator.
Port EB (Hex)	CTC Channel Three; break interrupt generator.
Port EE (Hex)	User Interface control port
Port EF (Hex)	User Memory Map.

9.2 Memory Map Software Interface

All access to the memory map are made by instructions of the class IN (C),<r> or OUT (C), <r>. These instructions place the contents of the C register on the low order address lines, the contents of the B register on the high order address lines, and the contents of the <r> register on the data bus. Therefore, the C register contains the map port address (0EFH), the <r> register contains the memory map definition, and the B register contains the right justified high order six bits of the block address. For example:

```
        LD      A, 081H ;SYSTEM MEMORY 8000H, WRITE ENABLE
        LD      B, 005H ;USER ADDRESS 1400H --> BLOCK 5H
        LD      C, 0EFH ;MAP PORT ADDRESS
        OUT     (C), A  ;SET MAP DEFINITION
```

This routine programs the memory map RAM to transform the address 1400H generated by the emulator into an access to Development System memory location 8000H with write operations allowed. The data bus bits have the following meaning for both read and write to port 0EFH.

BIT	MEANING
0	0=write protected No write access is allowed. A break is generated if bit 3 of the control port (EEH) is also set.
1	1=User memory User memory will be accessed. 0=System memory Development System memory will be accessed, wait states will be inserted as required.

The following bits will be used to address Development System memory if bit 1 is 0.

BIT	MEANING
2	System memory address bus bit 10 This bit is used to indicate non-existent memory, when bit 1 is 1.
3	System memory address bus bit 11
4	System memory address bus bit 12
5	System memory address bus bit 13
6	System memory address bus bit 14
7	System memory address bus bit 15

NOTE: Setting bits 1 and 2 to a logical 1 (high) defines that block as nonexistent.

9.3 User Pod Control Port

The User Pod Controller control port 0EEH may be accessed with any input or output instructions. The bits of this port have the following meanings:

BIT	ON WRITE	ON READ
0	RUN EMULATION	RUN EMULATION
1	MAP SELECT	MAP SELECT
2	not used	EMULATOR HALT STATUS
3	WRITE PROTECT INTERRUPT ENABLE	WRITE PROTECT INTERRUPT ENABLE
4	RESET EMULATION MODULE	RESET EMULATION MODULE
5	EMULATION INTERRUPT ENABLE	EMULATION INTERRUPT ENABLE
6	not used	BAD CLOCK STATUS
7	not used	System CLOCK SELECTED

RUN EMULATION (Bit 0): When set to 1, the Development System CPU is bus requested and the Emulator is enabled when BUSAK- becomes true. This bit is reset to idle by POWER-ON CLEAR-, RESET USER INTERFACE-, or the generation of a break request interrupt.

MAP SELECT (Bit 1): Must be reset to 0 to allow the map logic to function properly during an emulation. When set to 1, the map logic takes the address information from the Development System address bus through the User Pod Controller instead of from the Emulator. This bit is reset by POWER-ON CLEAR- or RESET USER INTERFACE-.

EMULATOR HALT STATUS (Bit 2): A read-only status bit indicating that the Emulator is halted as a result of executing a HALT instruction. The bit is high as long as the Emulator remains halted.

WRITE PROTECT INTERRUPT ENABLE (Bit 3): When set to 1, any attempt to write protected memory will generate a break interrupt. This bit is reset by POWER-ON CLEAR- or RESET USER INTERFACE-.

RESET EMULATION module (Bit 4): While this bit is set (to 1), all User POD Controller logic is held reset (no emulations may be run). In addition, the RESET- line to the Emulator/User System is held active (low). This bit is reset by POWER-ON CLEAR- and generates the signal RESET USER INTERFACE-.

EMULATION INTERRUPT ENABLE (Bit 5): When this bit is set to 1, both non-maskable interrupts and maskable interrupts will be accepted by the Emulator while running an emulation. When this bit is reset to 0, all interrupts are ignored by the Emulator while running an emulation. The Emulator ignores all interrupts when it is idle. This bit is reset by POWER-ON CLEAR- or USER INTERFACE RESET-.

BAD CLOCK STATUS (Bit 6): A read-only status bit indicating that a valid clock is present at the Emulator if the bit is set.

SYSTEM CLOCK SELECTED (Bit 7): A read-only status bit indicating that an Emulator that expects system clock is attched to the USER POD. A high indicates that System clock is used. A low indicates that the User clock is used.

The sequences listed below are used to control the Emulator.

NORMAL RUN SEQUENCE

A) Run is set (performed by software)
B) Request Development System bus (Performed by hardware)
C) Receive bus acknowledge from Development System (performed by hardware)
D) Start running emulation on next M1 cycle (performed by hardware)

NORMAL IDLE SEQUENCE

A) Run is reset (performed by software under emulation)
B) Complete I/O instruction (resetting run)
C) Execute one additional single opcode instruction
D) Begin idle on next M1 cycle (two-M1 cycles after resetting run)
E) Drop bus request (performed by hardware)

NOTE: Software that resets the run latch during emulation must keep track of the value of the PC, because the real time storage module will not contain the first idle instruction.

BREAK HALT

A) When interrupt is generated by bad clock, write protected, non-existent memory, break, or time-out of software timer
B) Reset run (performed by hardware)
C) Complete current instruction
D) Begin idle on next M1 cycle (first M1 cycle after interrupt)
E) Drop bus request (when the Development System comes back on the bus, the interrupt line is active).

NOTE: The value of the PC may be determined by examining the address stored in the last entry in the real time storage module. This entry should show an instruction fetch of data 18H (the first machine cycle of a jump relative minus two).

9.4 User Pod Controller (Sheet 1)

The buffers at A11 and A15 receive the Emulator address bus and allow these address bits onto the Development System address bus when an emulation is running. The high order six address bits (SAB 10, SAB 11, SAB 12, SAB 13, SAB 14, and SAB 15) of this bus are sent only to the breakpoint Module and the real time storage module so that unmapped address information is used for break and history activity. Buffer A10 buffers the low order address bits of the Development System to the port decoder logic and Z-80 CTCs shown on Sheets 2 and 5. The logic below A11 supplies the real time storage module with the correct I/O request signal. When an emulation is running, IORQ- must come from the Emulator, and when the Emulator is idle, the IORQ- must come form the Development System.

This sheet contains most of the memory map interface logic. The buffer at A8 receives the output from the memory map RAM and allows it onto the data bus of the Development System to permit the reading of the map. Buffer A7 receives the output from the memory map RAM to provide an interface to the Development System address bus, the NO-MEMORY detector, and the write protect violation detector. The mapped address lines (MAPPED AB 10, MAPPED AB 11, MAPPED AB 12, MAPPED AB 13, MAPPED AB 14, and MAPPED AB 15) are placed on the Development System memory address bus so that mapped address information is used to access the memory. The buffer A1 drives the six least significant address bits of the Development System high order address bus out to the memory map RAM along with the map control lines.

9.5 User Pod Controller (Sheet 2)

The buffers at A13 and A14 receive the control bus of the Emulator and pass M1-, RD-, WR-, IORQ-, RFSH-, HALT-, MRQ-, and SBUSAK- on to the Development System control bus and real time storage module. The Emulator clock (TRC PHI) is also buffered and sent to the monitor module. The logic at the middle of Sheet 2 provides the write protection for the Development System memory when activated write protection violation break requests are also generated in the logic at the middle of Sheet 2.

Sheet 2 shows the two Z-80 CTC devices used to generate break interrupt vectors. The upper CTC uses channel zero for the bad clock vector, channel one for the non-existent memory vector, channel three for the break vector. The second CTC is wired as a very large programmable timer. This timer can be programmed to break emulation after a period of time, if no other breaks have occured. The timer is triggered by the first M1- after the run latch is set and counts the 2.5MHz clock of the Development System until the channel programmed to interrupt reaches zero then an interrupt is generated that stops the emulation. This CTC can also be programmed as a counter, then it counts M1S- which occurs once per instruction thereby counting instructions and again interrupting when the appropri- ately programmed channel reaches zero. The remainder of the logic at the bottom of Sheet 2 generates the control signal that determines the direction of the data bus drivers of the User Pod Controller.

9.6 User Pod Controller (Sheet 3)

The buffer at A2 drives general control signals to the User Pod. The remainder of the logic on Sheet 4 interfaces the Development System data bus to the User Pod/Emulator data bus and to the User Pod Controller internal data bus.

9.7 User Pod Controller (Sheet 4)

The logic at the top of Sheet 4 is used for starting and stopping emulations. The Development System CPU sets the run bit (bit 0, port 0EEH) which makes RUN REQ active and generates a BUSRQ- to the Development System CPU. When the Development System responds with BUSAK-, the run latch (A20) is clocked set by the leading edge (high to low transition) of the M1- from the Emulator. Once the run latch is set, STOP becomes false (0) and allows the Emulator to run. If the Emulator resets the run bit of the control port, then the second M1- clocks the run latch reset and halts the emulation by idling the Emulator. This action of the run latch permits the Emulator to reset the run latch and execute one additional single opcode instruction to position the program counter or load a register. However, if a break request is generated, then the monitor module drives FORCE NOP true (high) which causes the run latch to be reset. This procedure also assures that the emulation will stop at the end of any instruction that generates a break. The Real Time Storage Module and Breakpoint Module in the Development System are now enabled by RUN instead of MONITOR. This allows both modules to operate in both monitor mode and user mode. When an emulation is stopped by a break condition, then the last entry in the Real Time Storage Module contains the PC in the address field. On the other hand, if the emulation was stopped by resetting the run bit (bit 0, port OEEH), then the Real Time Storage Module may not contain a value that accruately reflects the PC. However, since the control program caused the run bit to reset, it also knows the actual value of the PC. For example, if the following program were executed by the Emulator,

```
        ORG     8000H
        LD      A,0             ;DATA TO RESET RUN
        OUT     (0EEH),A        ;RESET RUN
        JP      0000            ;USE EXTRA INSTRUCTION TO
                                ; POSITION PC
```

the Real Time Storage Module would show a last event of memory read from address 8006H, data of 00H, while the PC would be 0000H.

The remainder of the logic on Sheet 4 is used to buffer the Development System clock and the Development System control bus into the internal clock and control bus used on the User POD Controller. The same buffer is also used to drive the enable interrupts control signal out to the POD.

9.8 User Pod Controller (Sheet 5)

The logic at the top of Sheet 5 is the I/O port decoder logic for the User POD Controller. Ports 0E4H through 0E7H are decoded for selecting the second Z-80 CTC on Sheet 2, while ports 0E8H through 0EBH are decoded to select the first Z-80 CTC on Sheet 2. Port 0EEH is decoded for the control port which is the logic at the bottom of Sheet 5, and port 0EFH is decoded to be the memory map port. All ports of the Development System are accessible to both the Development System and the Emulator in accordance with the following table.

MONITOR MODE	USER MODE	
All I/O in DS E0-FF used	All I/O in DS E0-FF used	System CLOCK
All I/O in User System except EE & EF	All I/O in User System	USER CLOCK

The one-shot at the bottom of Sheet 5 verifies that the Emulator clock has a period greater than 4 microseconds which is the minimum clock for a Z-80 CPU. The state of this one-shot can be read through the control port (bit 6, port 0EEH) to verify that the Emulator is being driven by a clock. The second one-shot generates wait states for for the Emulator when it accesses the Development System memory or I/O ports. The third one-shot generates wait states for the Development System when it accesses the memory map RAM. The eight input or-gate at A17 collects the various break requests and generates the BREAK EMULATION signal for the monitor module (shown as BREAK on the monitor module logic diagram). The monitor module then guarantees that the current instruction is completed before issuing the FORCE NOP signal that stops emulation. At the bottom of Sheet 5 is the buffer that brings the control port data bits onto the Development System data bus when the control port is read.

APPENDIX A

PORT ASSIGNMENTS FOR THE ZDS-1/40

PORT ASSIGNMENTS FOR THE ZDS-1/40

ADDRESS	READ FUNCTION	WRITE FUNCTION
0FFH	BAUD RATE DETECTION	NOT USED
0FEH	STATUS PORT	NOT USED
0FDH	S0FTWARE SYSTEM RESET	SET USER MODE
0FCH	RTSM CONTROL PORT	RTSM CONTROL PORT
0FBH	BRKPT CONTROL PORT	BRKPT CONTROL PORT
0FAH	DISK CONTROL PORT A	DISK CONTROL PORT A
0F9H	DISK CONTROL PORT B	DISK CONTROL PORT B
0F8H	DISK DATA PORT	DISK DATA PORT
0F7H	SET MONITOR MODE	SET MONITOR MODE
0F6H	NOT USED	NOT USED
0F5H	USART CONTROL PORT	USART CONTROL PORT
0F4H	USART DATA PORT	USART DATA PORT
0F3H	SYSTEM CTC C3	SYSTEM CTC C3
0F2H	SYSTEM CTC C2 - BAUD RATE	SYSTEM CTC C2 - BAUD RATE
0F1H	SYSTEM CTC C1 - SER. CLK.	SYSTEM CTC C1 - SER. CLK.
0F0H	SYSTEM CTC C0 - DISK SECTOR	SYSTEM CTC C0 - DISK
0EFH	USER MEMORY MAP PORT	USER MEMORY MAP PORT
0EEH	USER INTERFACE CONTROL PORT	USER INTERFACE CONTROL PORT
0EDH	NOT USED	NOT USED
0ECH	NOT USED	NOT USED
0EBH	USER INTF. BREAK GEN.	USER INTF. BREAK GEN.
0EAH	USER INTF. WRITE PROT. ERR.	USER INTF. WRITE PROT. ERR.
0E9H	USER INTF. NO MEM. ERR.	USER INTF. NO MEM. ERR.
0E8H	USER INTF. BAD CLOCK ERR.	USER INTF. BAD CLOCK ERR.
0E7H	USER INTF. CASCADED CTC C3	USER INTF.CASCADED CTC C3
0E6H	USER INTF. CASCADED CTC C2	USER INTF.CASCADED CTC C2
0E5H	USER INTF. CASCADED CTC C1	USER INTF.CASCADED CTC C1
0E4H	USER INTF. CASCADED CTC C0	USER INTF.CASCADED CTC C0
0E3H	NOT USED	NOT USED
0E2H	NOT USED	NOT USED
0E1H	NOT USED	NOT USED
0E0H	NOT USED	NOT USED

APPENDIX B

ZDS-1/40 CONFIGURATION

PCB LOCATION FOR ZDS-1/40

CONNECTOR	PRINTED CIRCUIT BOARDS
J01	POD CONTROLLER - Z-80A CPU EMULATOR
J02	MONITOR
J03	ZDS/ASPIO, PROM PROGRAMMER
J04	PROM PROGRAMMER
J05	PROM PROGRAMMER, CIB, PIB
J06	PROM PROGRAMMER
J07	PROM PROGRAMMER, USER-DEFINABLE I/O
J08	32K, 48K, 60K DYNAMIC RAM
J09	CPU
J10	FLOPPY CONTROLLER
J11	BREAKPOINT
J12	REAL TIME STORAGE MODULE

I/O CONNECTORS

J13	LINE PRINTER CABLE (CIB/PIB)
J14	USER DEFINABLE (SPARE)
J15	USER DEFINABLE (SPARE)
J16	FLOPPY DRIVE CABLE
J17	TERMINAL CABLE
J18	AUXILIARY SERIAL CABLE
J19	LINE PRINTER CABLE (ASPIO)
J20	PROLOG PROM PROGRAMMER CABLE
J21	SPARE
J22	SPARE
J23	FRONT PANEL CABLE
J24	POWER CABLE

REAR PANEL CONNECTORS

J101	SPARE
J102	SPARE
J103	PROLOG PROM PROGRAMMER
J104	LINE PRINTER (ASPIO)
J105	AUXILIARY SERIAL PORT
J106	TERMINAL
J107	FLOPPY DISK DRIVES
J108	SPARE
J109	SPARE
J110	SECOND LINE PRINTER (CIB/PIB)

INTERRUPT DAISY CHAIN

PRIORITY		CARD
1	J09	CPU
2	J01	POD CONTROLLER
3	J03	ZDS/ASPIO
4	J05	CIB/PIB

APPENDIX C

BACKPLANE DEFINITION FOR ZDS-1/40

BACKPLANE DEFINITION FOR ZDS-1/40

```
                NAME=ZDS-1/40
SYSTEM=ZDS-1/40
REVISION=13-1079-02/REV.A
GEOMETRY=ZDS.1.40.GEO
NETS=

+05V.1
                    J01-059
                    J23-009

+05V.2
                    J01-060
                    J23-008

+05V.3
                    J01-061
                    J23-007

+05V.4
                    J02-061
                    J23-010

+12V.1
                    J08-090
                    J08-091
                    J08-092
                    J24-007

+12V.2
                    J08-093
                    J08-094
                    J08-095
                    J24-008

+12V.3
                    J01-105
                    J02-095
                    J03-090
                    J09-090
                    J24-009

-05V.1
                    J08-068
                    J08-069
                    J16-013
                    J24-001
```

-05V.2	J08-083
	J08-084
	J08-085
	J24-002
-05V.3	J09-099
	J24-003
-12V.1	J03-107
	J24-004
-12V.2	J02-098
	J24-005
8.PHI	J09-023
	J10-023
A00	J01-100
	J02-016
	J03-016
	J04-016
	J05-016
	J06-016
	J07-016
	J08-016
	J09-016
	J11-016
	J12-016
A01	J01-098
	J02-017
	J03-017
	J04-017
	J05-017
	J06-017
	J07-017
	J08-017
	J09-017
	J11-017
	J12-017

ZDS-1/40 BACKPLANE DEFINITION (cont.)

A02

J01-097
J02-018
J03-018
J04-018
J05-018
J06-018
J07-018
J08-018
J09-018
J11-018
J12-018

A03

J01-108
J02-019
J03-019
J04-019
J05-019
J06-019
J07-019
J08-019
J09-019
J11-019
J12-019

A04

J01-109
J02-020
J03-020
J04-020
J05-020
J06-020
J07-020
J08-020
J09-020
J11-020

A05	
	J01-096
	J02-021
	J03-021
	J04-021
	J05-021
	J06-021
	J07-021
	J08-021
	J09-021
	J11-021
	J12-021
A06	
	J01-104
	J02-009
	J03-009
	J04-009
	J05-009
	J06-009
	J07-009
	J08-009
	J09-009
	J11-009
	J12-009
A07	
	J01-101
	J02-010
	J03-010
	J04-010
	J05-010
	J06-010
	J07-010
	J08-010
	J09-010
	J11-010
	J12-010
A08	
	J01-086
	J05-011
	J06-011
	J07-011
	J08-011
	J09-011
	J11-011
	J12-011

A09	J01-085
	J05-014
	J06-014
	J07-014
	J08-014
	J09-014
	J11-014
	J12-014
A10	J01-116
	J05-013
	J06-013
	J07-013
	J08-013
	J09-013
A11	J01-119
	J05-012
	J06-012
	J07-012
	J08-012
	J09-012
A12	J01-115
	J09-042
A12+	J08-042
	J09-068
A13	J01-117
	J09-040
A13+	J08-040
	J09-066
A14	J01-118
	J09-041
A15	J01-114
	J09-043

ACK-.LP	J03-082
	J19-011
ACK-.LP2	J05-082
	J13-011
ADDRESS.PROLOG	J05-117
	J20-015
BKPT.SEL-	J02-070
	J11-015
BREAK-	J01-066
	J11-100
BREAK.EMULATION-	J01-077
	J02-102
BREAK.PENDING	J01-004
	J02-103
BREAK.STATUS	J02-116
	J11-085
BREAK.SYNC	J11-101
	J23-003
BUSAK-	J01-112
	J09-022
BUSRQ-	J01-110
	J09-107
BUSY.LP	J03-076
	J19-023

```
BUSY.LP2
                    J05-076
                    J13-023

CARRIER.DETECT
                    J03-038
                    J18-008

CD.0-
                    J08-038
                    J09-038

CD.1-
                    J07-038
                    J08-037
                    J09-037

CD.2-
                    J06-038
                    J08-036
                    J09-036

CD.3-
                    J05-038
                    J08-035
                    J09-035

D0
                    J01-074
                    J02-054
                    J03-054
                    J04-054
                    J05-054
                    J06-054
                    J07-054
                    J08-054
                    J09-054
                    J10-054
                    J11-054
                    J12-054
```

ZDS-1/40 BACKPLANE DEFINITION (cont.)

D1

J01-068
J02-055
J03-055
J04-055
J05-055
J06-055
J07-055
J08-055
J09-055
J10-055
J11-055
J12-055

D2

J01-075
J02-057
J03-057
J04-057
J05-057
J06-057
J07-057
J08-057
J09-057
J10-057
J11-057
J12-057

D3

J01-072
J02-056
J03-056
J04-056
J05-056
J06-056
J07-056
J08-056
J09-056
J10-056
J11-056
J12-056

D4	J01-070
	J02-047
	J03-047
	J04-047
	J05-047
	J06-047
	J07-047
	J08-047
	J09-047
	J10-047
	J11-047
	J12-047
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	J03-048
	J04-048
	J05-048
	J06-048
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	J11-048
	J12-048
D6	J01-073
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	J03-051
	J04-051
	J05-051
	J06-051
	J07-051
	J08-051
	J09-051
	J10-051
	J11-051
	J12-051

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	J01-069
	J02-052
	J03-052
	J04-052
	J05-052
	J06-052
	J07-052
	J08-052
	J09-052
	J10-052
	J11-052
	J12-052
DATA.1	
	J06-065
	J22-001
DATA.1.LP	
	J03-065
	J19-001
DATA.1.LP2	
	J05-065
	J13-001
DATA.2	
	J06-066
	J22-002
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	J03-066
	J19-002
DATA.2.LP2	
	J05-066
	J13-002
DATA.3	
	J06-067
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	J03-067
	J19-003

DATA.3.LP2	J05-067 J13-003
DATA.4	J06-068 J22-004
DATA.4.LP	J03-068 J19-004
DATA.4.LP2	J05-068 J13-004
DATA.5	J06-069 J22-005
DATA.5.LP	J03-069 J19-005
DATA.5.LP2	J05-069 J13-005
DATA.6	J06-070 J22-006
DATA.6.LP	J03-070 J19-006
DATA.6.LP2	J05-070 J13-006
DATA.7	J06-071 J22-007
DATA.7.LP	J03-071 J19-007

DATA.7.LP2	J05-071 J13-007
DATA.8	J06-072 J22-008
DATA.8.LP	J03-072 J19-008
DATA.8.LP2	J05-072 J13-008
DATA.RDY	J06-117 J21-009
DATA.STB	J02-101 J11-114 J12-114
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DATA.STB-.LP2	J05-073 J13-009
DI.0	J06-104 J21-001
DI.1	J06-105 J21-002
DI.2	J06-106 J21-003
DI.3	J06-110 J21-004

DI.4	J06-111 J21-005
DI.5	J06-113 J21-006
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DI.7	J06-115 J21-008
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DI2.PROLOG	J05-106 J20-017
DI3.PROLOG	J05-110 J20-018
DI4.PROLOG	J05-111 J20-023
DI5.PROLOG	J05-113 J20-024
DI6.PROLOG	J05-114 J20-021
DI7.PROLOG	J05-115 J20-022

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DISK.CONTROL.B.PORT-	J02-068 J10-118
DISK.DATA.PORT-	J02-067 J10-116
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DO1.PROLOG	J05-094 J20-012
DO2.PROLOG	J05-095 J20-007
DO3.PROLOG	J05-096 J20-009
DO4.PROLOG	J05-097 J20-010
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DO6.PROLOG	J05-099 J20-006

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	J20-008
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	J21-017
DRIVE.RT	J06-103
	J21-016
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	J20-014
EXT.INH	J06-102
	J21-015
EXT.PHI	J09-058
	J09-115
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	J19-012
FAULT-.LP2	J05-078
	J13-012
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	J02-106
	J09-106
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	J12-037
GND.01	J03-062
	J13-018
	J13-019
	J13-020

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	J03-063
	J16-014
	J16-015
	J16-016
GND.03	
	J03-064
	J16-017
	J16-018
	J16-019
GND.04	
	J01-062
	J16-020
	J16-021
	J16-022
GND.05	
	J01-063
	J16-023
	J16-024
	J16-025
	J16-026
GND.06	
	J01-064
	J18-007
	J19-018
	J19-019
	J19-020
GND.07	
	J02-120
	J20-025
	J21-011
	J21-012
GND.08	
	J02-121
	J21-013
	J21-024
	J21-025
GND.09	
	J02-122
	J22-016
	J22-017
	J22-018

GND.10	J02-062
	J22-023
	J22-025
GND.11	J02-063
	J23-001
GND.12	J02-064
	J23-002
GND.13	J01-120
	J23-006
GND.14	J01-121
	J23-013
GND.15	J01-122
	J23-024
HALT-	J01-089
	J02-027
	J09-027
	J12-027
HALT.LAMP-	J02-005
	J23-020
HIS.IORQ-	J01-095
	J11-030
	J12-030
INDX	J09-078
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INDX.0-	J10-015 J16-012
INPUT.MODE.SEL	J06-074 J22-014
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INPUT.PRIME-.LP2	J05-081 J13-010
INT-	J01-107 J03-109 J05-109 J09-109
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INT.DAISY.CHAIN.2	J01-087 J03-088
INT.DAISY.CHAIN.3	J03-112 J05-088
INTERLOCK.PROLOG	J05-103 J20-005
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	J18-010
M1-	
	J01-083
	J02-028
	J03-028
	J04-028
	J05-028
	J06-028
	J07-028
	J09-028
	J12-028
M1RQ	
	J02-090
	J11-090
M1S-	
	J01-065
	J02-089
MODE.PROLOG	
	J05-102
	J20-003
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	J01-106
	J02-110
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	J02-006
	J23-022
MONTR.NC	
	J02-082
	J23-026
MONTR.NO	
	J02-083
	J23-025
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	J02-076
	J05-046
	J06-046
	J07-046
	J08-046

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	J05-029
	J06-029
	J07-029
	J08-029
	J09-029
	J11-029
	J12-029
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	J18-009
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	J22-015
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	J19-013
PAPER.EMPTY.LP2	J05-077
	J13-013
PG.15-	J05-039
	J06-039
	J07-039
	J08-039
	J09-039
PHI	J01-067
	J03-024
	J04-024
	J05-024
	J06-024
	J07-024
	J09-024
POWER.ON.CLR-	J01-076
	J02-026
	J09-026
	J11-026

PS.0-	
	J05-034
	J06-034
	J07-034
	J08-034
	J09-034
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	J05-033
	J06-033
	J07-033
	J08-033
	J09-033
PS.2-	
	J05-032
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	J08-032
	J09-032
PS.3-	
	J05-031
	J06-031
	J07-031
	J08-031
	J09-031
PUNCH.COM	
	J06-073
	J22-011
PUNCH.RDY	
	J06-076
	J22-012
R.I	
	J03-089
	J18-022

RD-	
	J01-092 J02-045 J03-045 J04-045 J05-045 J06-045 J07-045 J09-045 J10-045 J11-045 J12-045
RD.CLK-	
	J10-081 J16-001
RDR.OUT.MODE	
	J06-119 J21-010
RDR.RDY	
	J06-118 J21-014
RDY-	
	J10-016 J16-011
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	J10-009 J16-002
REFRESH-	
	J01-090 J08-025 J09-025
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	J09-049 J23-019
RESPONSE.PROLOG	
	J05-116 J20-016
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	J02-011 J12-050

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	J02-093 J17-002
RS232.DATA.OUT	
	J02-086 J17-003
RS232.RETURN	
	J02-091 J17-007
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	J01-113 J02-036 J11-111 J12-111
SA10	
	J01-079 J11-013 J12-013
SA11	
	J01-078 J11-012 J12-012
SA12	
	J01-084 J11-042 J12-042
SA13	
	J01-080 J11-040 J12-040
SA14	
	J01-081 J11-041 J12-041
SA15	
	J01-082 J11-043 J12-043

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	J01-088
	J12-022
SEL.0-	
	J10-018
	J16-010
SEL.1-	
	J10-084
	J16-009
SELECT.LP	
	J03-075
	J19-024
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	J05-075
	J13-024
SENSE.SW.1-	
	J02-117
	J23-015
SENSE.SW.2-	
	J02-118
	J23-014
SERIAL.IN	
	J02-087
	J09-008
SERIAL.OUT	
	J02-085
	J09-015
STEP-	
	J10-028
	J16-007
STOR.SEL-	
	J02-066
	J12-066
SYNC	
	J03-049
	J18-024

SYS.RESET-	J02-046
	J03-026
	J05-053
	J09-053
	J10-053
SYSMEM	J01-006
	J09-067
SYSTEM.RDY	J06-075
	J22-013
TAPE.ERR	J06-078
	J22-020
TAPE.LOW	J06-077
	J22-021
TCTS	J03-007
	J18-005
TDSR	J03-008
	J18-006
TDTR	J03-050
	J18-020
TERM.BUSY	J03-025
	J18-025
TRANSFER.PROLOG	J05-119
	J20-002
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	J02-024
TRK.00-	J10-011
	J16-004

TRTS	J03-006 J18-004
TRXD	J03-005 J18-003
TTXD	J03-004 J18-002
TTY.DATA.IN	J02-092 J17-010
TTY.DATA.OUT	J02-084 J17-016
TTY.IN.RETURN	J02-097 J17-005 J17-006 J17-008 J17-024
TTY.OUT.RETURN	J02-099 J17-017
TY.HI	J02-012 J09-046
USER.LAMP-	J02-008 J23-021
USER.NC	J02-077 J23-012
USER.NO	J02-078 J23-011

WAIT-	
	J01-111
	J02-108
	J09-108
	J10-108
WAIT.LAMP-	
	J02-007
	J23-023
WR-	
	J01-094
	J02-044
	J03-044
	J05-044
	J06-044
	J07-044
	J08-044
	J09-044
	J10-044
	J11-044
	J12-044
WR.DATA-	
	J10-006
	J16-006
WR.PROT.0-	
	J10-013
	J16-003
WRITE.GATE-	
	J10-025
	J16-005

APPENDIX D

PINOUT CHARTS

CONTENTS

PINOUT FOR POD CONTROLLER BOARD - 09-0055-01

J01

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	BREAK.PENDING
005	(SYS.DB.DISABLE-)
006	SYSMEM.(SYSTEM.MEMORY)
007	.
008	.
009	.
010	.
011	.
012	.
013	.
014	.
015	.
016	.
017	.
018	.
019	.
020	.
021	.
022	.
023	.
024	.
025	.
026	.
027	.
028	.
029	.
030	.
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.
044	.
045	.
046	.

PINOUT FOR POD CONTROLLER BOARD - 09-0055-01 (cont.)

J01

PIN #	SIGNAL NAME
047	.
048	.
049	.
050	.
051	.
052	.
053	.
054	.
055	.
056	.
057	.
058	.
059	+05V.1.(PRINTED.DISTRIBUTION)
060	+05V.2.(PRINTED.DISTRIBUTION)
061	+05V.3.(PRINTED.DISTRIBUTION)
062	GND.04.(PRINTED.DISTRIBUTION)
063	GND.05.(PRINTED.DISTRIBUTION)
064	GND.06.(PRINTED.DISTRIBUTION)
065	M1S-
066	BREAK-
067	PHI.(SYSTEM.CLOCK)
068	D1
069	D7
070	D4
071	D5
072	D3
073	D6
074	D0
075	D2
076	POWER.ON.CLR-
077	BREAK.EMULATION-
078	SA11
079	SA10
080	SA13
081	SA14
082	SA15
083	M1-
084	SA12
085	A09
086	A08
087	INT.DAISY.CHAIN.[#IEO].(IEO.OUT)
088	SBUSAK-
089	HALT-
090	REFRESH-
091	IORQ-
092	RD-

PINOUT FOR POD CONTROLLER BOARD - 09-0055-01 (cont.)

J01

PIN #	SIGNAL NAME
093	MRQ-
094	WR-
095	HIS.IORQ-
096	A05
097	A02
098	A01
099	TRC.PHI.(EMULATOR.CLOCK)
100	A00
101	A07
102	INT.DAISY.CHAIN.[#IEI].(IEI.IN)
103	FORCE.NOP
104	A06
105	+12V.3
106	MONITOR
107	INT-
108	A03
109	A04
110	BUSRQ-
111	WAIT-
112	BUSAK-
113	RUN
114	A15
115	A12
116	A10
117	A13
118	A14
119	A11
120	GND.13.(PRINTED.DISTRIBUTION)
121	GND.14.(PRINTED.DISTRIBUTION)
122	GND.15.(PRINTED.DISTRIBUTION)

PINOUT FOR MONITOR BOARD - 09-0093-01

J02

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	HALT.LAMP-
006	MONITOR.LAMP-
007	WAIT.LAMP-
008	USER.LAMP-
009	A06
010	A07
011	RESTART.D-
012	TY.HI
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	TRC.PHI.(CLOCK.FROM.EMULATOR)
025	(GND)
026	POWER.ON.CLR-
027	HALT-
028	M1-
029	MRQ-
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	RUN
037	FORCE.NOP.DELAYED
038	.
039	.
040	.
041	.
042	.
043	.
044	WR-
045	RD-
046	SYS.RESET-

PINOUT FOR MONITOR BOARD - 09-0093-01 (cont.)

J02

PIN #	SIGNAL NAME
047	D4
048	D5
049	.
050	(RESTART-)
051	D6
052	D7
053	(USER.MEM.ENABLE-)
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	+05V.4.(PRINTED.DISTRIBUTION)
062	GND.10.(PRINTED.DISTRIBUTION)
063	GND.11.(PRINTED.DISTRIBUTION)
064	GND.12.(PRINTED.DISTRIBUTION)
065	.
066	STOR.SEL-
067	DISK.DATA.PORT-
068	DISK.CONTROL.B.PORT-
069	DISK.CONTROL.A.PORT-
070	BKPT.SEL-
071	.
072	.
073	.
074	.
075	(UB.CONT-)
076	MRD-
077	USER.NC
078	USER.NO
079	(SPARE.SEL-)
080	(CTC.CARD.SEL-)
081	.
082	MONTR.NC
083	MONTR.NO
084	TTY.DATA.OUT
085	SERIAL.OUT
086	RS232.DATA.OUT
087	SERIAL.IN
088	.
089	M1S-
090	M1RQ
091	RS232.RETURN
092	TTY.DATA.IN

PINOUT FOR MONITOR BOARD - 09-0093-01 (cont.)

J02

PIN #	SIGNAL NAME
093	RS232.DATA.IN
094	.
095	+12V.3
096	(IE*)
097	TTY.IN.RETURN
098	-12V.2
099	TTY.OUT.RETURN
100	(RFI)
101	DATA.STB
102	BREAK.EMULATION-
103	BREAK.PENDING
104	.
105	.
106	FORCE.NOP
107	.
108	WAIT-
109	.
110	MONITOR
111	(MONITOR-)
112	.
113	.
114	.
115	(PHI.B.[CLOCK.BUFFERED])
116	BREAK.STATUS
117	SENSE.SW.1-
118	SENSE.SW.2-
119	.
120	GND.07.(PRINTED.DISTRIBUTION)
121	GND.08.(PRINTED.DISTRIBUTION)
122	GND.09.(PRINTED.DISTRIBUTION)

PINOUT FOR ZDS/ASPIO BOARD - 09-0034-01

J03

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	TTXD
005	TRXD
006	TRTS
007	TCTS
008	TDSR
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	TERM.BUSY
026	SYS.RESET-
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	CARRIER.DETECT
039	.
040	.
041	.
042	.
043	.
044	WR-
045	RD-
046	.

PINOUT FOR ZDS/ASPIO BOARD - 09-0034-01 (cont.)

J03

PIN #	SIGNAL NAME
047	D4
048	D5
049	SYNC
050	TDTR
051	D6
052	D7
053	.
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	GND.01.(PRINTED.DISTRIBUTION)
063	GND.02.(PRINTED.DISTRIBUTION)
064	GND.03.(PRINTED.DISTRIBUTION)
065	DATA.1.LP
066	DATA.2.LP
067	DATA.3.LP
068	DATA.4.LP
069	DATA.5.LP
070	DATA.6.LP
071	DATA.7.LP
072	DATA.8.LP
073	DATA.STB-.LP
074	.
075	SELECT.LP
076	BUSY.LP
077	PAPER.EMPTY.LP
078	FAULT-.LP
079	.
080	.
081	INPUT.PRIME-.LP
082	ACK-.LP
083	.
084	.
085	.
086	.
087	.
088	INT.DAISY.CHAIN.[#IEI].(IEI)
089	R.I
090	+12V.3
091	ORIGINATE.MODE
092	LOCAL.MODE

PINOUT FOR ZDS/ASPIO BOARD - 09-0034-01 (cont.)

J03

PIN #	SIGNAL NAME
093	.
094	.
095	.
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	-12V.1
108	.
109	INT-
110	.
111	.
112	INT.DAISY.CHAIN.[#IEO].(IEO)
113	.
114	.
115	.
116	.
117	.
118	.
119	.
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR PROM PROGRAMMER BOARD - 09-0031-02
J03, J05, J06, J07

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	.
026	.
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.
044	.
045	RD-
046	.

PINOUT FOR PROM PROGRAMMER BOARD - 09-0031-02 (cont.)
J03, J05, J06, J07

PIN #	SIGNAL NAME
047	D4
048	D5
049	.
050	.
051	D6
052	D7
053	.
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.PRINTED.DISTRIBUTION)
063	(GND.PRINTED.DISTRIBUTION)
064	(GND.PRINTED.DISTRIBUTION)
065	.
066	.
067	.
068	.
069	.
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	.
078	.
079	.
080	.
081	.
082	.
083	.
084	.
085	.
086	.
087	.
088	(IEI)
089	.
090	.
091	.
092	.

PINOUT FOR PROM PROGRAMMER BOARD - 09-0031-02 (cont.)
J03, J05, J06, J07

PIN #	SIGNAL NAME
093	.
094	.
095	.
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	.
108	.
109	(INT-)
110	.
111	.
112	(IEO)
113	.
114	.
115	.
116	.
117	.
118	.
119	.
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR CIB BOARD - 09-0020-01

J05

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	.
026	.
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.
044	.
045	RD-
046	.

PINOUT FOR CIB BOARD - 09-0020-01 (cont.)

J05

PIN #	SIGNAL NAME
047	D4
048	D5
049	.
050	.
051	D6
052	D7
053	SYS.RESET-
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.PRINTED.DISTRIBUTION)
063	(GND.PRINTED.DISTRIBUTION)
064	(GND.PRINTED.DISTRIBUTION)
065	DATA.1.LP2
066	DATA.2.LP2
067	DATA.3.LP2
068	DATA.4.LP2
069	DATA.5.LP2
070	DATA.6.LP2
071	DATA.7.LP2
072	DATA.8.LP2
073	DATA.STB-.LP2
074	.
075	SELECT.LP2
076	BUSY.LP2
077	PAPER.EMPTY.LP2
078	FAULT-.LP2
079	.
080	.
081	INPUT.PRIME-.LP2
082	ACK-.LP2
083	.
084	.
085	.
086	.
087	.
088	INT.DAISY.CHAIN.[#IEI].(IEI)
089	.
090	.
091	.
092	.

PINOUT FOR CIB BOARD - 09-0020-01 (cont.)

J05

PIN #	SIGNAL NAME
093	DO0.PROLOG
094	DO1.PROLOG
095	DO2.PROLOG
096	DO3.PROLOG
097	DO4.PROLOG
098	DO5.PROLOG
099	DO6.PROLOG
100	.
101	DO7.PROLOG
102	MODE.PROLOG
103	INTERLOCK.PROLOG
104	DI0.PROLOG
105	DI1.PROLOG
106	DI2.PROLOG
107	.
108	.
109	INT-
110	DI3.PROLOG
111	DI4.PROLOG
112	(IEO)
113	DI5.PROLOG
114	DI6.PROLOG
115	DI7.PROLOG
116	RESPONSE.PROLOG
117	ADDRESS.PROLOG
118	ERROR.PROLOG
119	TRANSFER.PROLOG
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR PIB BOARD - 09-0020-02

J05

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	.
026	.
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.
044	.
045	RD-
046	.

PINOUT FOR PIB BOARD - 09-0020-02 (cont.)

J05

PIN #	SIGNAL NAME
047	D4
048	D5
049	.
050	.
051	D6
052	D7
053	SYS.RESET-
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.PRINTED.DISTRIBUTION)
063	(GND.PRINTED.DISTRIBUTION)
064	(GND.PRINTED.DISTRIBUTION)
065	DATA.1.LP2
066	DATA.2.LP2
067	DATA.3.LP2
068	DATA.4.LP2
069	DATA.5.LP2
070	DATA.6.LP2
071	DATA.7.LP2
072	DATA.8.LP2
073	DATA.STB-.LP2
074	.
075	SELECT.LP2
076	BUSY.LP2
077	PAPER.EMPTY.LP2
078	FAULT-.LP2
079	.
080	.
081	INPUT.PRIME-.LP2
082	ACK-.LP2
083	.
084	.
085	.
086	.
087	.
088	INT.DAISY.CHAIN.[#IEI].(IEI)
089	.
090	.
091	.
092	.

PINOUT FOR PIB BOARD - 09-0020-02 (cont.)

J05

PIN #	SIGNAL NAME
093	DO0.PROLOG
094	DO1.PROLOG
095	DO2.PROLOG
096	DO3.PROLOG
097	DO4.PROLOG
098	DO5.PROLOG
099	DO6.PROLOG
100	.
101	DO7.PROLOG
102	MODE.PROLOG
103	INTERLOCK.PROLOG
104	DI0.PROLOG
105	DI1.PROLOG
106	DI2.PROLOG
107	.
108	.
109	INT-
110	DI3.PROLOG
111	DI4.PROLOG
112	(IEO)
113	DI5.PROLOG
114	DI6.PROLOG
115	DI7.PROLOG
116	RESPONSE.PROLOG
117	ADDRESS.PROLOG
118	ERROR.PROLOG
119	TRANSFER.PROLOG
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR 60K MEMORY BOARD - 09-0101-04

J08

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	.
025	REFRESH-
026	.
027	.
028	.
029	MRQ-
030	.
031	PS.3-
032	PS.2-
033	PS.1-
034	PS.0-
035	CD.3-
036	CD.2-
037	CD.1-
038	CD.0-
039	PG.15-
040	A13+
041	.
042	A12+
043	.
044	WR-
045	.
046	MRD-

PINOUT FOR 60K MEMORY BOARD - 09-0101-04 (cont.)

J08

PIN #	SIGNAL NAME
047	D4
048	D5
049	.
050	.
051	D6
052	D7
053	.
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.PRINTED.DISTRIBUTION)
063	(GND.PRINTED.DISTRIBUTION)
064	(GND.PRINTED.DISTRIBUTION)
065	.
066	.
067	.
068	-05V.1
069	-05V.1
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	.
078	.
079	.
080	.
081	.
082	.
083	-05V.2
084	-05V.2
085	-05V.2
086	.
087	.
088	.
089	.
090	+12V.1
091	+12V.1
092	+12V.1

PINOUT FOR 60K MEMORY BOARD - 09-0101-04 (cont.)

J08

PIN #	SIGNAL NAME
093	+12V.2
094	+12V.2
095	+12V.2
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	.
108	.
109	.
110	.
111	.
112	.
113	.
114	.
115	.
116	.
117	.
118	.
119	.
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR CPU BOARD - 09-0099-03

J09

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	RCVR.OUT-
005	(SERIAL.OUT)
006	RCV.CLK
007	RCV.CLK.(XMIT.CLK)
008	SERIAL.IN
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	SERIAL.OUT
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	BUSAK-
023	8.PHI.(8X.SYSTEM.CLOCK)
024	PHI.(SYSTEM.CLOCK)
025	REFRESH-
026	POWER.ON.CLR-
027	HALT-
028	M1-
029	MRQ-
030	IORQ-
031	PS.3-
032	PS.2-
033	PS.1-
034	PS.0-
035	CD.3-
036	CD.2-
037	CD.1-
038	CD.0-
039	PG.15-.(MDIS-)
040	A13
041	A14
042	A12
043	A15
044	WR-
045	RD-
046	TY.HI.(MONITOR)

PINOUT FOR CPU BOARD - 09-0099-03 (cont.)

J09

PIN #	SIGNAL NAME
047	D4
048	D5
049	RESET.SW-
050	(RESTART-)
051	D6
052	D7
053	SYS.RESET-
054	D0
055	D1
056	D3
057	D2
058	EXT.PHI.(EXTERNAL.SYSTEM.CLOCK)
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.PRINTED.DISTRIBUTION)
063	(GND.PRINTED.DISTRIBUTION)
064	(GND.PRINTED.DISTRIBUTION)
065	.
066	A13+
067	SYSMEM.(SYSTEM.MEMORY)
068	A12+
069	.
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	RCVR.OUT-
078	INDX.(EN-CLK0)
079	INT.DAISY.CHAIN.[#IEO].(IE*)
079	.
080	.
081	.
082	.
083	(GND)
084	(GND)
085	(GND)
086	(GND)
087	(GND)
088	.
089	.
090	+12V.3
091	.

PINOUT FOR CPU BOARD - 09-0099-03 (cont.)

J09

PIN #	SIGNAL NAME
092	.
093	.
094	.
095	.
096	.
097	.
098	.
099	-5V.3
100	.
101	.
102	.
103	.
104	.
105	.
106	FORCE.NOP
107	BUSRQ-
108	WAIT-
109	INT-
110	(NMI-)
111	.
112	.
113	.
114	.
115	EXT.PHI.(S2.46MHZ)
116	.
117	.
118	.
119	.
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR FLOPPY CONTROLLER BOARD - 09-0004-01

J10

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	WR.DATA-
007	INDX
008	(WR.PROT.1-)
009	READ.DATA-
010	(TRK.01-)
011	TRK.00-
012	(DOOR.OPEN-)
013	WR.PROT.0-
014	(INDX.1-)
015	INDX.0-
016	RDY-
017	(CURRENT-)
018	SEL.0-
019	(LOAD.HEAD.1-)
020	(STEP.OUT.1-)
021	(WRITE.1-)
022	(STEP.IN.1-)
023	8.PHI.(8X.SYSTEM.CLOCK)
024	.
025	WRITE.GATE-
026	.
027	DIRECTION
028	STEP-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.
044	WR-
045	RD-
046	.

PINOUT FOR FLOPPY CONTROLLER BOARD - 09-0004-01
J10 (continued)

PIN #	SIGNAL NAME
047	D4
048	D5
049	.
050	.
051	D6
052	D7
053	SYS.RESET-
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.PRINTED.DISTRIBUTION)
063	(GND.PRINTED.DISTRIBUTION)
064	(GND.PRINTED.DISTRIBUTION)
065	.
066	.
067	.
068	.
069	.
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	.
078	.
079	.
080	.
081	RD.CLK-
082	(GND)
083	(GND)
084	SEL.1-
085	(GND)
086	.
087	(LOAD.HEAD.0-)
088	.
089	.
090	.
091	.
092	.

PINOUT FOR FLOPPY CONTROLLER BOARD - 09-0004-01

J10 (continued)

PIN #	SIGNAL NAME
093	.
094	.
095	.
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	.
108	WAIT-
109	.
110	.
111	.
112	.
113	.
114	.
115	.
116	DISK.DATA.PORT-
117	DISK.CONTROL.A.PORT-
118	DISK.CONTROL.B.PORT-
119	.
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR BREAKPOINT BOARD - 09-0003-02

J11

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	A08
012	SA11
013	SA10
014	A09
015	BKPT.SEL-
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	.
025	.
026	POWER.ON.CLR-
027	.
028	.
029	MRQ-
030	HIS.IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	SA13
041	SA14
042	SA12
043	SA15
044	WR-
045	RD-
046	.

PINOUT FOR BREAKPOINT BOARD - 09-0003-02 (cont.)

J11

PIN #	SIGNAL NAME
047	D4
048	D5
049	.
050	.
051	D6
052	D7
053	.
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.PRINTED.DISTRIBUTION)
063	(GND.PRINTED.DISTRIBUTION)
064	(GND.PRINTED.DISTRIBUTION)
065	.
066	.
067	.
068	.
069	.
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	.
078	.
079	.
080	.
081	.
082	.
083	.
084	.
085	BREAK.STATUS
086	.
087	.
088	.
089	.
090	M1RQ
091	.
092	.

PINOUT FOR BREAKPOINT BOARD - 09-0003-02 (cont.)

J11

PIN #	SIGNAL NAME
093	.
094	.
095	.
096	.
097	.
098	.
099	.
100	BREAK-
101	BREAK.SYNC
102	.
103	.
104	.
105	.
106	.
107	.
108	.
109	.
110	.
111	RUN
112	.
113	.
114	DATA.STB
115	.
116	.
117	.
118	.
119	.
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR RTSM2 BOARD - 09-0109-01

J12

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	A08
012	SA11
013	SA10
014	A09
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	SBUSAK-
023	.
024	.
025	.
026	.
027	HALT-
028	M1-
029	MRQ-
030	HIS.IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	FORCE.NOP.DELAYED
038	.
039	.
040	SA13
041	SA14
042	SA12
043	SA15
044	WR-
045	RD-
046	.

PINOUT FOR RTSM2 BOARD - 09-0109-01 (cont.)

J12

PIN #	SIGNAL NAME
047	D4
048	D5
049	.
050	RESTART.D-
051	D6
052	D7
053	.
054	D0
055	Dl
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.PRINTED.DISTRIBUTION)
063	(GND.PRINTED.DISTRIBUTION)
064	(GND.PRINTED.DISTRIBUTION)
065	.
066	STOR.SEL-
067	.
068	.
069	.
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	.
078	.
079	.
080	.
081	.
082	.
083	.
084	.
085	.
086	.
087	.
088	.
089	.
090	.
091	.
092	.

PINOUT FOR RTSM2 BOARD - 09-0109-01 (cont.)

J12

PIN #	SIGNAL NAME
093	.
094	.
095	.
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	.
108	.
109	.
110	.
111	RUN
112	.
113	.
114	DATA.STB
115	.
116	.
117	.
118	.
119	.
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR I/O CONNECTOR: LINE PRINTER (CIB/PIB) CABLE
J13

PIN #	SIGNAL NAME
001	DATA.1.LP2
002	DATA.2.LP2
003	DATA.3.LP2
004	DATA.4.LP2
005	DATA.5.LP2
006	DATA.6.LP2
007	DATA.7.LP2
008	DATA.8.LP2
009	DATA.STB-.LP2
010	INPUT.PRIME-.LP2
011	ACK-.LP2
012	FAULT-.LP2
013	PAPER.EMPTY.LP2
014	.
015	.
016	.
017	.
018	GND.01
019	GND.01
020	GND.01
021	.
022	.
023	BUSY.LP2
024	SELECT.LP2
025	.

PINOUT FOR I/O CONNECTOR: FLOPPY DRIVE CABLE
J16

PIN #	SIGNAL NAME
001	RD.CLK-
002	READ.DATA-
003	WR.PROT.0-
004	TRK.00-
005	WRITE.GATE-
006	WR.DATA-
007	STEP-
008	DIRECTION
009	SEL.1-
010	SEL.0-
011	RDY-
012	INDX.0-
013	-05V.1
014	GND.02
015	GND.02
016	GND.02
017	GND.03
018	GND.03
019	GND.03
020	GND.04
021	GND.04
022	GND.04
023	GND.05
024	GND.05
025	GND.05
026	GND.05

PINOUT FOR I/O CONNECTOR: TERMINAL CABLE
J17

PIN #	SIGNAL NAME
001	.
002	RS232.DATA.IN
003	RS232.DATA.OUT
004	.
005	TTY.IN.RETURN
006	TTY.IN.RETURN
007	RS232.RETURN
008	TTY.IN.RETURN
009	.
010	TTY.DATA.IN
011	.
012	.
013	.
014	.
015	.
016	TTY.DATA.OUT
017	TTY.OUT.RETURN
018	.
019	.
020	.
021	.
022	.
023	.
024	TTY.IN.RETURN
025	.

PINOUT FOR I/O CONNECTOR: AUXILIARY SERIAL CABLE J18

PIN #	SIGNAL NAME
001	.
002	TTXD
003	TRXD
004	TRTS
005	TCTS
006	TDSR
007	GND.06
008	CARRIER.DETECT
009	ORIGINATE.MODE
010	LOCAL.MODE
011	.
012	.
013	.
014	.
015	.
016	.
017	.
018	.
019	.
020	TDTR
021	.
022	R.I
023	.
024	SYNC
025	TERM.BUSY

PINOUT FOR I/O CONNECTOR: LINE PRINTER (ZDS/ASPIO) CABLE
J19

PIN #	SIGNAL NAME
001	DATA.1.LP
002	DATA.2.LP
003	DATA.3.LP
004	DATA.4.LP
005	DATA.5.LP
006	DATA.6.LP
007	DATA.7.LP
008	DATA.8.LP
009	DATA.STB-.LP
010	INPUT.PRIME-.LP
011	ACK-.LP
012	FAULT-.LP
013	PAPER.EMPTY.LP
014	.
015	.
016	.
017	.
018	GND.06
019	GND.06
020	GND.06
021	.
022	.
023	BUSY.LP
024	SELECT.LP
025	.

PINOUT FOR I/O CONNECTOR: PROLOG PROM PROGRAMMER CABLE
J20

PIN #	SIGNAL NAME
001	.
002	TRANSFER.PROLOG
003	MODE.PROLOG
004	.
005	INTERLOCK.PROLOG
006	DO6.PROLOG
007	DO2.PROLOG
008	DO7.PROLOG
009	DO3.PROLOG
010	DO4.PROLOG
011	DO0.PROLOG
012	DO1.PROLOG
013	DO5.PROLOG
014	ERROR.PROLOG
015	ADDRESS.PROLOG
016	RESPONSE.PROLOG
017	DI2.PROLOG
018	DI3.PROLOG
019	DI0.PROLOG
020	DI1.PROLOG
021	DI6.PROLOG
022	DI7.PROLOG
023	DI4.PROLOG
024	DI5.PROLOG
025	GND.07

PINOUT FOR I/O CONNECTOR: FRONT PANEL CABLE
J23

PIN #	SIGNAL NAME
001	GND.11
002	GND.12
003	BREAK.SYNC
004	.
005	.
006	GND.13
007	+05V.3
008	+05V.2
009	+05V.1
010	+05V.4
011	USER.NO
012	USER.NC
013	GND.14
014	SENSE.SW.2-
015	SENSE.SW.1-
016	.
017	.
018	.
019	RESET.SW-
020	HALT.LAMP-
021	USER.LAMP-
022	MONITOR.LAMP-
023	WAIT.LAMP-
024	GND.15
025	MONTR.NO
026	MONTR.NC

PINOUT FOR I/O CONNECTOR: POWER CABLE
J24

PIN #	SIGNAL NAME
001	-05V.1
002	-05V.2
003	(-05V.3)
004	-12V.1
005	-12V.2
006	(-12V.3)
007	+12V.1
008	+12V.2
009	+12V.3
010	(+05V.PRINTED.DISTRIBUTION)
011	(GND.PRINTED.DISTRIBUTION)

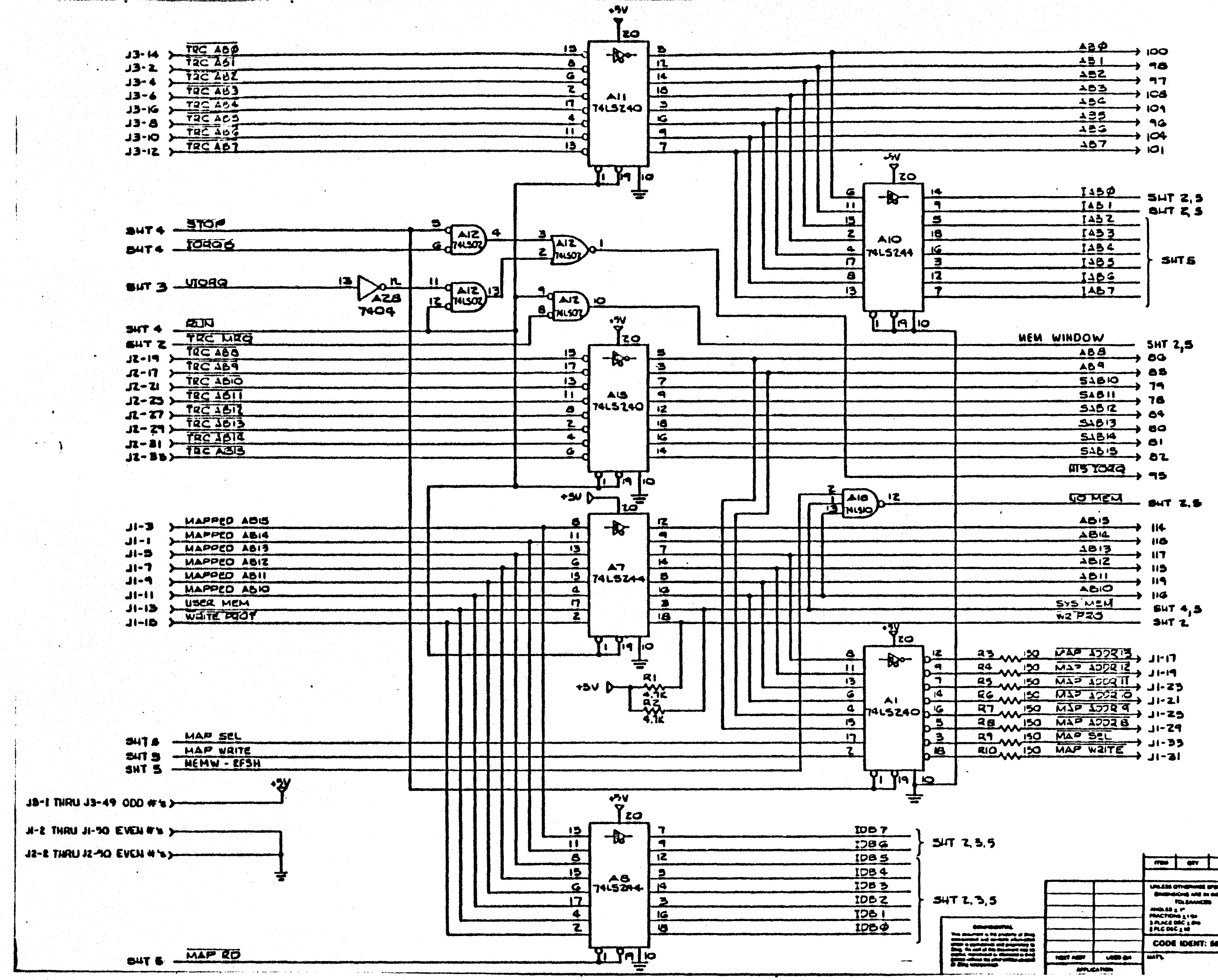
APPENDIX E

LOGIC DIAGRAMS

CONTENTS

LOGIC DIAGRAMS, USER POD CONTROLLER

A RELEASE PER ECN 01026



NOTES:
UNLESS OTHERWISE SPECIFIED.
1. RESISTORS ARE IN OHMS, ¼W, 5%.
2. CAPACITORS ARE IN MICROFARADS.

LAST REF DES USED				
A42	C21	CR1	R46	
REF DES NOT USED				
			R29	

IC'S	
TYPE	SPARE
74LS244	A16-F
9602	A26-B
74LS175	A41-D

PARTS LIST

CODE IDENT: 56700

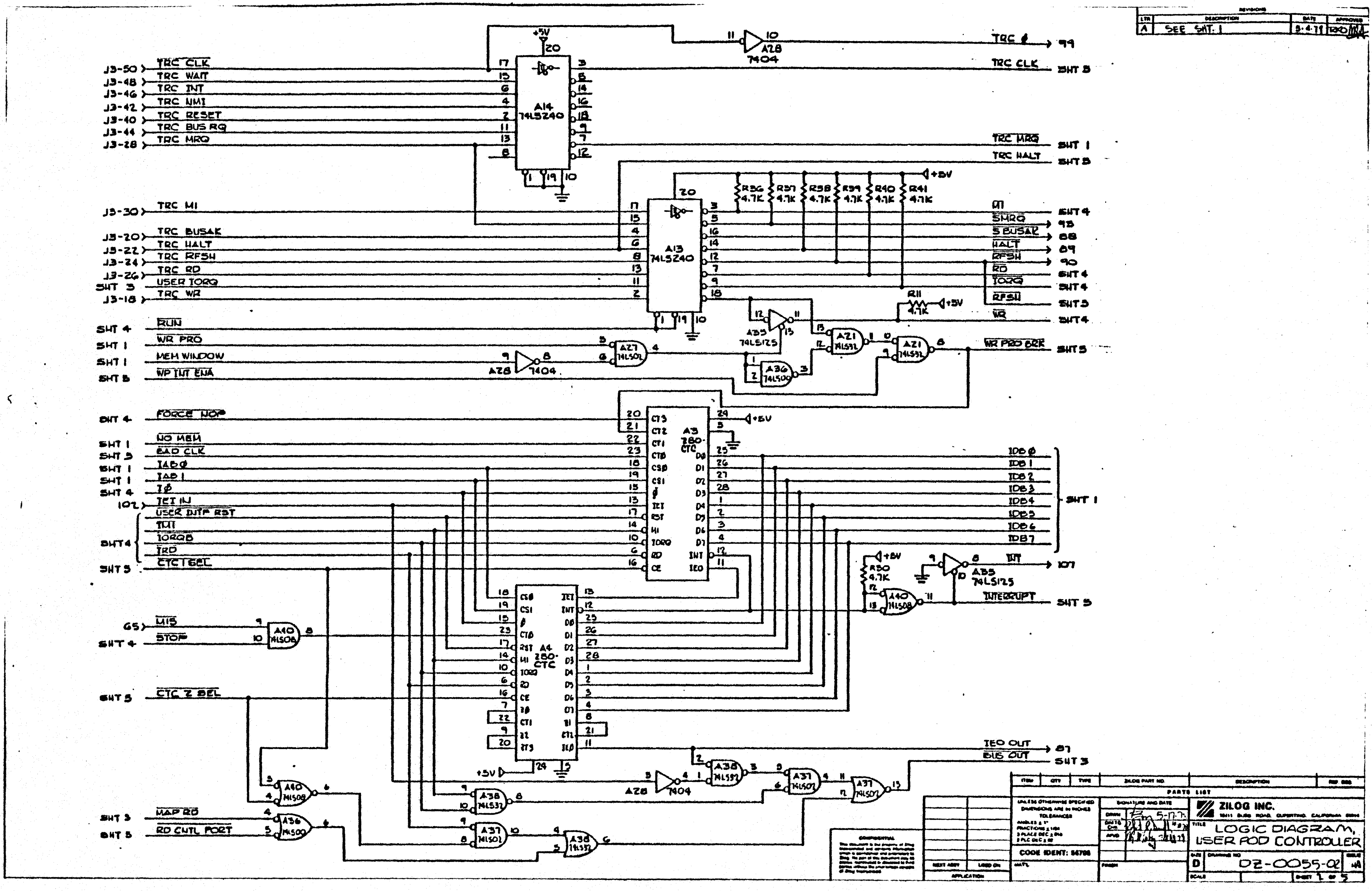
DRAWN 5-16-78

ZILOG INC.

TITLE LOGIC DIAGRAM, USER POD CONTROLLER

SIZE D DRAWING NO DZ-0055-02 ISSUE A

SHEET OF 5



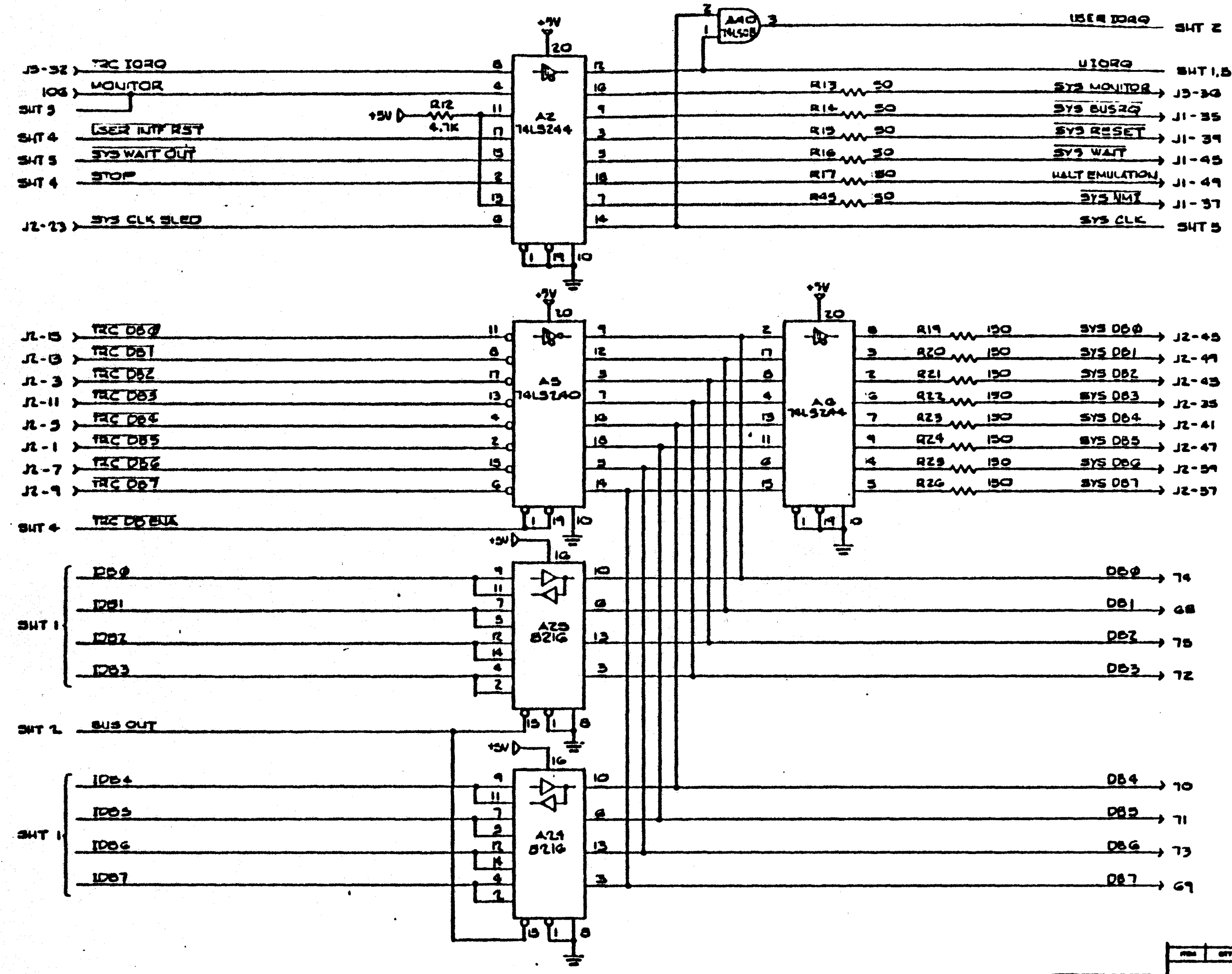
ZILOG INC.

LOGIC DIAGRAM, USER POD CONTROLLER

SIZE D DRAWING NO DZ-0055-02 ISSUE A

SHEET 2 OF 5

LTR	DESCRIPTION	DATE	APPROVED
A	SEE SHT. 1	5-4-79	[illegible]



ITEM	QTY.	TYPE	ZILOG PART NO.	DESCRIPTION	REF DES.

PARTS LIST

CONFIDENTIAL

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES

CODE IDENT: [illegible]

SIGNATURE AND DATE

DRWN 9-17-78

ZILOG INC.

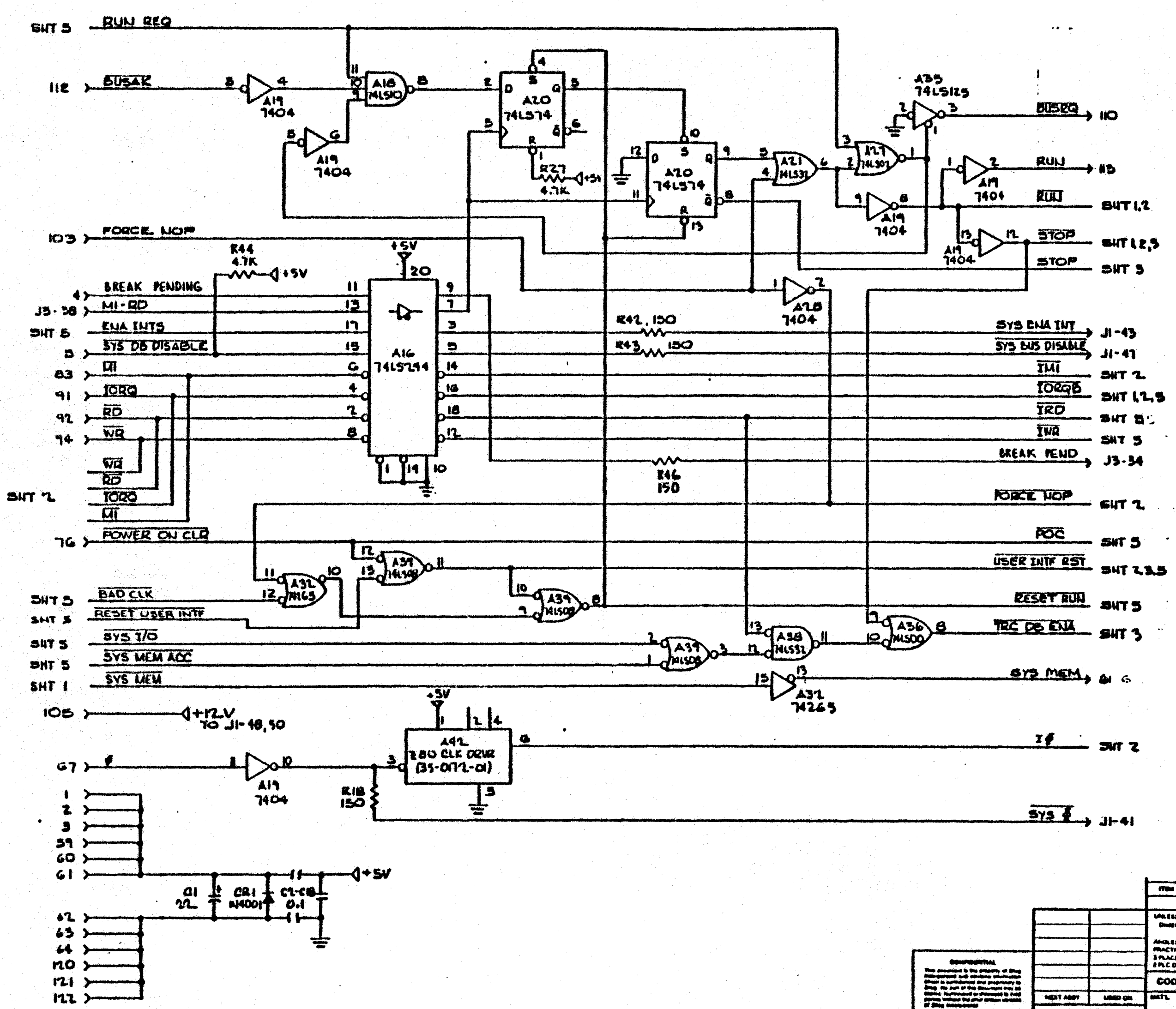
TITLE LOGIC DIAGRAM, USER POD CONTROLLER

SIZE D DRAWING NO D2-0055-02 ISSUE A

SCALE SHEET 3 OF 5

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	SEE SHT. 1	6-4-79	TRO



ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF. DES.

PARTS LIST

CONFIDENTIAL

[illegible]

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .03

CODE IDENT: 56708

MAT'L

SIGNATURE AND DATE
DRWN 5-79
DRFTG CHK
APVD

FINISH

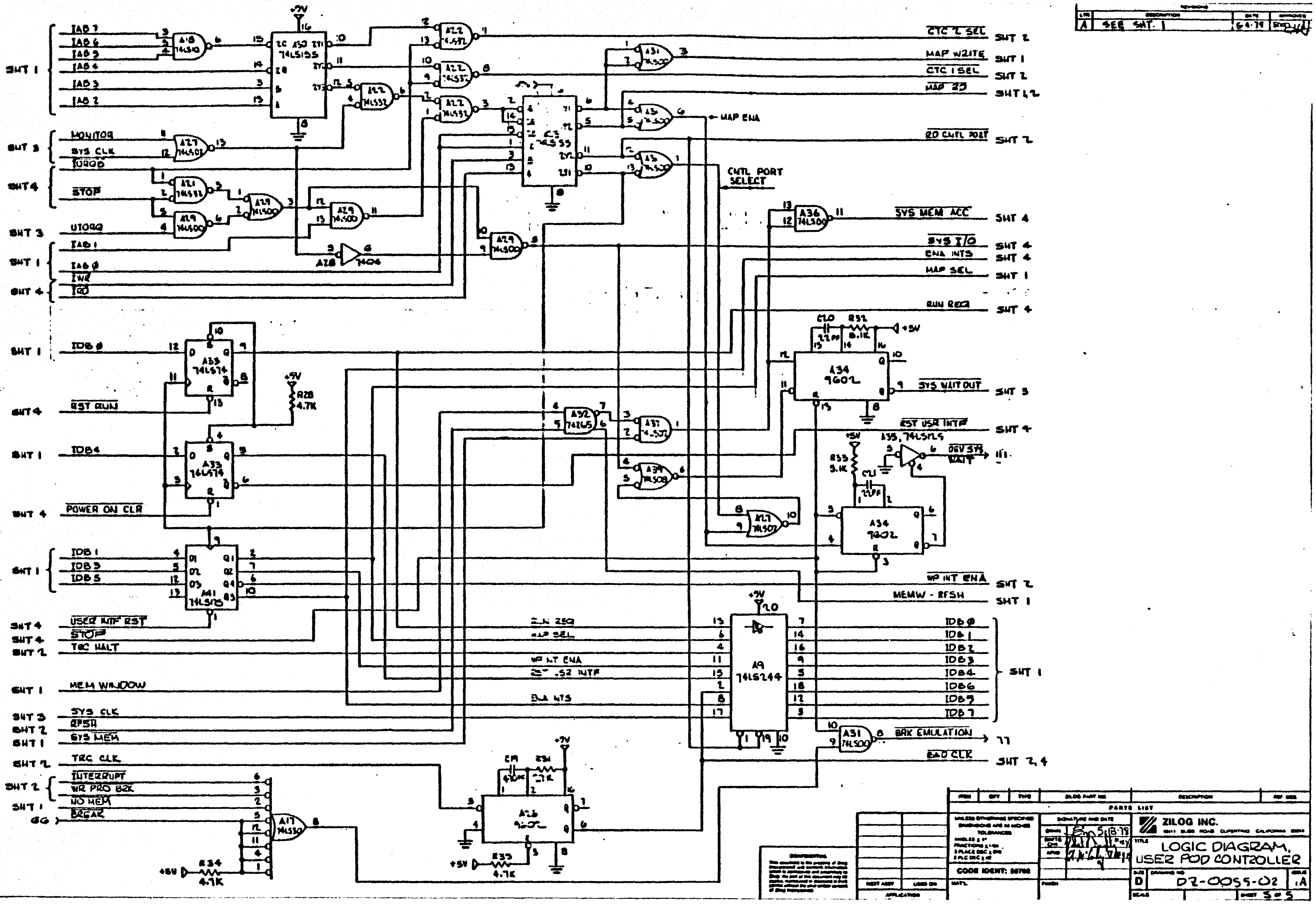
ZILOG INC.
10411 BUBB ROAD, CUPERTINO, CALIFORNIA 95014

TITLE LOGIC DIAGRAM, USER POD CONTROLLER

SIZE D
DRAWING NO D2-0055-02
ISSUE A

SCALE

SHEET 4 OF 9



LTR	DESCRIPTION	DATE	APPROVED
A	SEE SHT. 1	6-4-79	

PARTS LIST

CODE IDENT: 56708

Drawn: 5-18-79

ZILOG INC.

TITLE: LOGIC DIAGRAM, USER POD CONTROLLER

SIZE: D

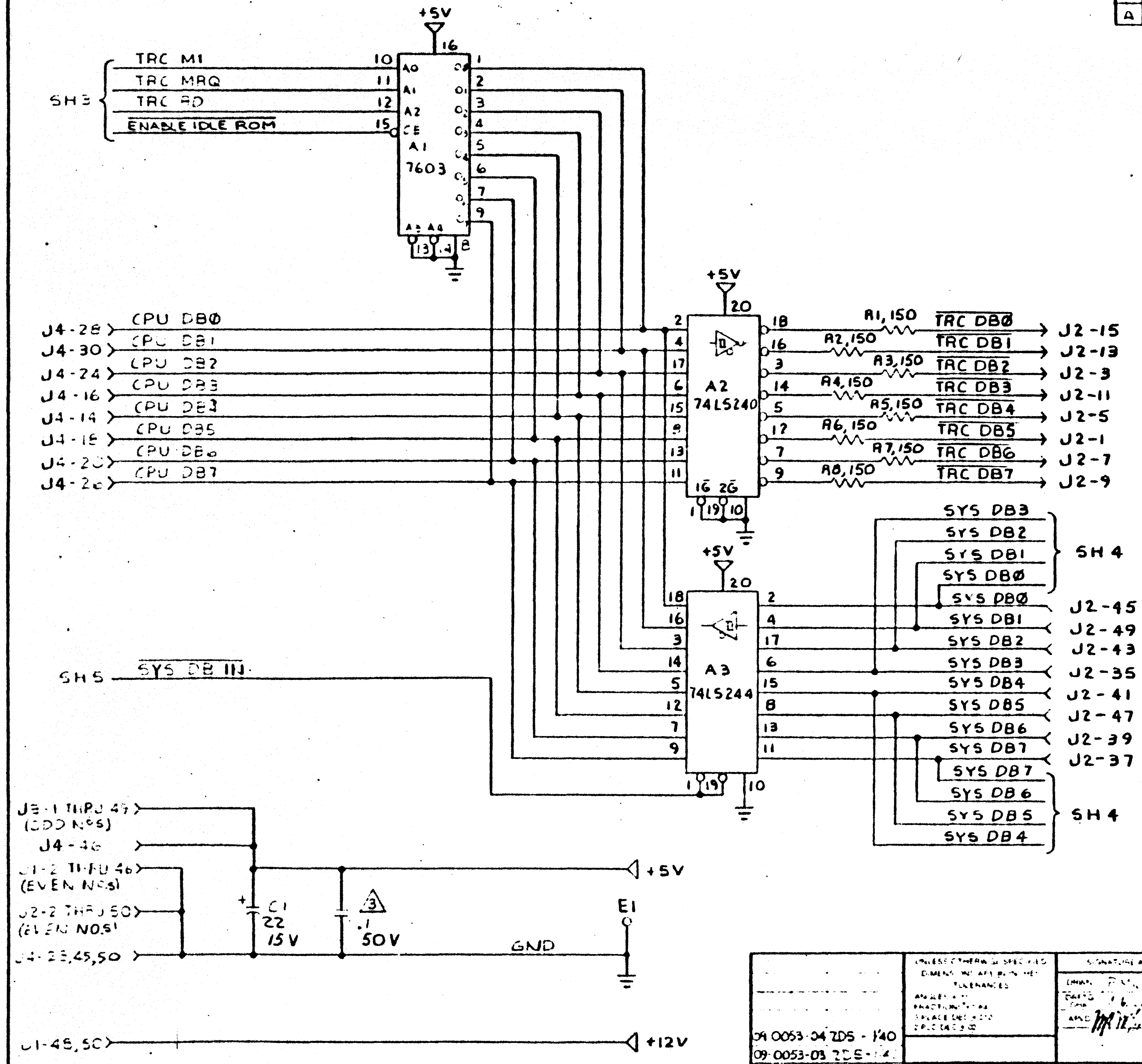
DRAWING NO: D2-0055-02

ISSUE: A

SHEET 5 OF 5

LOGIC DIAGRAMS, USER POD

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
1	EAR 410,480,508,509,573,623,637, 648	1-25-79	RKG
A	RELEASE PER ECN 01010	4 23 79	RED



NOTES-UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTANCE VALUES ARE IN OHMS, 1/4 W, 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. -02 USES C2-C6 ; -05 USES C2-C17.

REF DESG	
LAST USED	UNUSED
A28	
R74	R40 44,62,65,69
3	
TP1	

INTEGRATED CIRCUITS	
TYPE	SPARES
74LS08	2
7406	1
74LS32	2
74LS02	3

09-0053-04 ZDS-1/40 09-0053-03 ZDS-1/40	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES FRACTIONS 2 PLACE DEC 3 PLACE DEC	SIGNATURE AND DATE DRWN CHKD APVD	ZILOG INC. CUPERTINO CALIFORNIA
NEXT ASSY / USED ON			TITLE LOGIC DIAGRAM USER POD
APPLICATION	MAT'L	FINISH	SIZE C / DRAWING NO. DZ-0053-C5 / REV A
			SCALE NONE / SHEET 1 OF 6

CONFIDENTIAL

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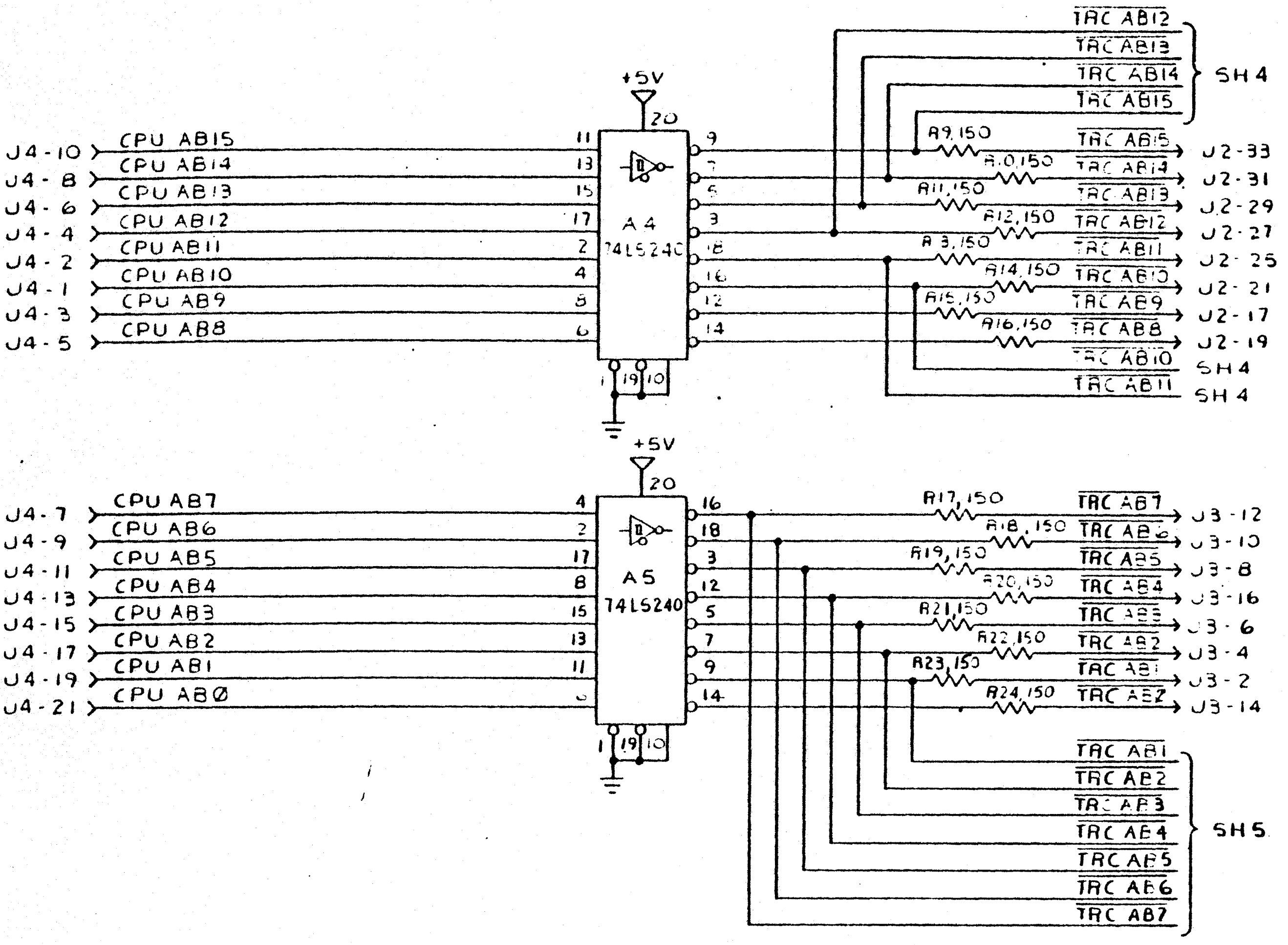
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	SEE SH. 1	4 [illegible] 79	RRD



+5V
20
A4
74LS240
J4-10 CPU AB15 11 9 R9,150 TRC AB15 J2-33
J4-8 CPU AB14 13 7 R10,150 TRC AB14 J2-31
J4-6 CPU AB13 15 5 R11,150 TRC AB13 J2-29
J4-4 CPU AB12 17 3 R12,150 TRC AB12 J2-27
J4-2 CPU AB11 2 18 R13,150 TRC AB11 J2-25
J4-1 CPU AB10 4 16 R14,150 TRC AB10 J2-21
J4-3 CPU AB9 8 12 R15,150 TRC AB9 J2-17
J4-5 CPU AB8 6 14 R16,150 TRC AB8 J2-19
1 19 10
TRC AB12
TRC AB13
TRC AB14
TRC AB15
SH 4
TRC AB10 SH 4
TRC AB11 SH 4
+5V
20
A5
74LS240
J4-7 CPU AB7 4 16 R17,150 TRC AB7 J3-12
J4-9 CPU AB6 2 18 R18,150 TRC AB6 J3-10
J4-11 CPU AB5 17 3 R19,150 TRC AB5 J3-8
J4-13 CPU AB4 8 12 R20,150 TRC AB4 J3-16
J4-15 CPU AB3 15 5 R21,150 TRC AB3 J3-6
J4-17 CPU AB2 13 7 R22,150 TRC AB2 J3-4
J4-19 CPU AB1 11 9 R23,150 TRC AB1 J3-2
J4-21 CPU AB0 6 14 R24,150 TRC AB2 J3-14
1 19 10
TRC AB1
TRC AB2
TRC AB3
TRC AB4
TRC AB5
TRC AB6
TRC AB7
SH 5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ±
FRACTIONS ± 1/64
1 PLACE DEC ± .1
2 PLACE DEC ± .02

SIGNATURE AND DATE
DRWN R MILES
CHKD [illegible]
APVD M.V. [illegible]

SEE SH. 1
NEXT ASSY USED ON
APPLICATION

MAT'L

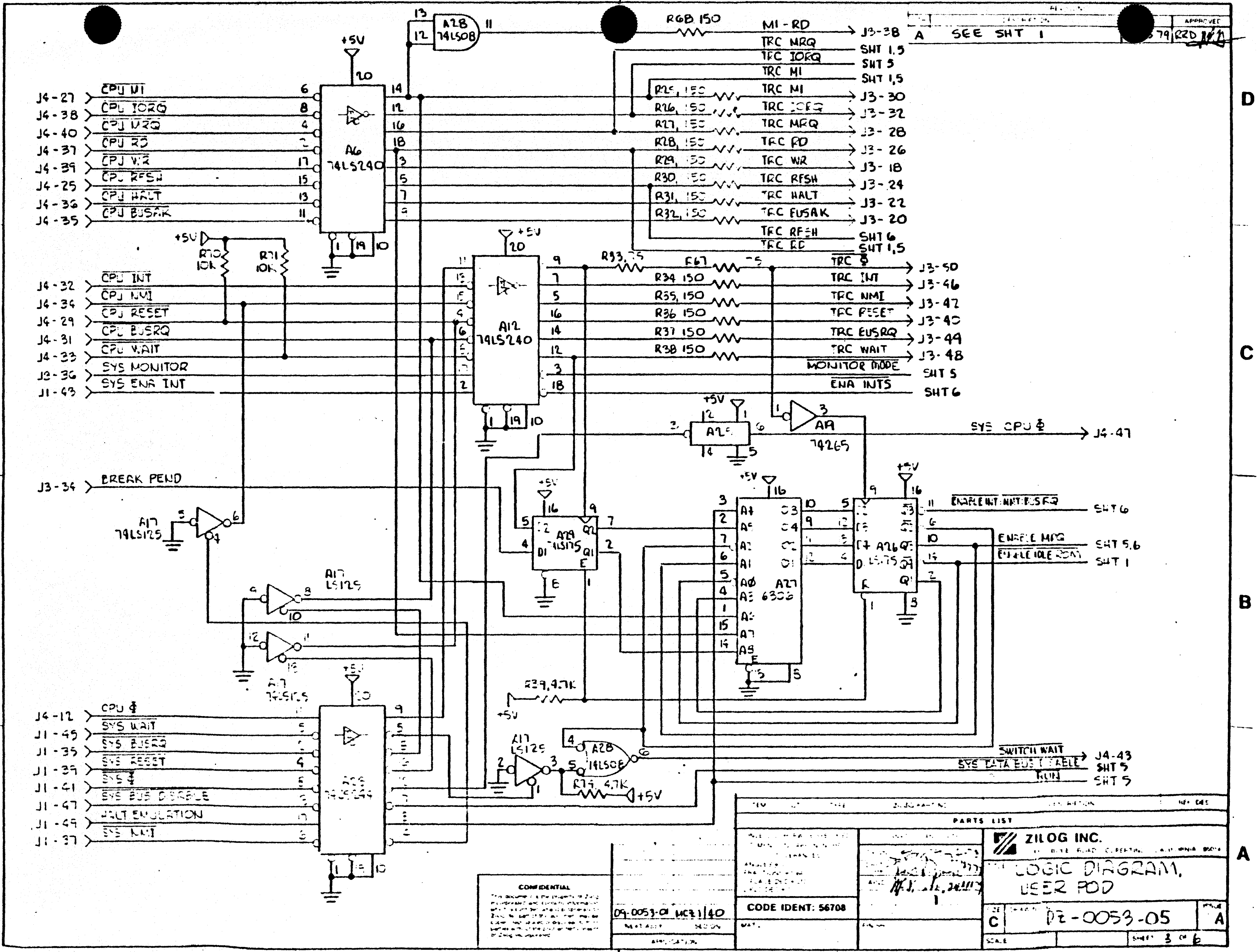
FINISH

ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE LOGIC DIAGRAM USER POD

SIZE C DRAWING NO. 02-0053-05 ISSUE A

SCALE — SHEET 2 OF 6



PARTS LIST

CONFIDENTIAL

09-0053-01 MCZ 1/40

CODE IDENT: 56708

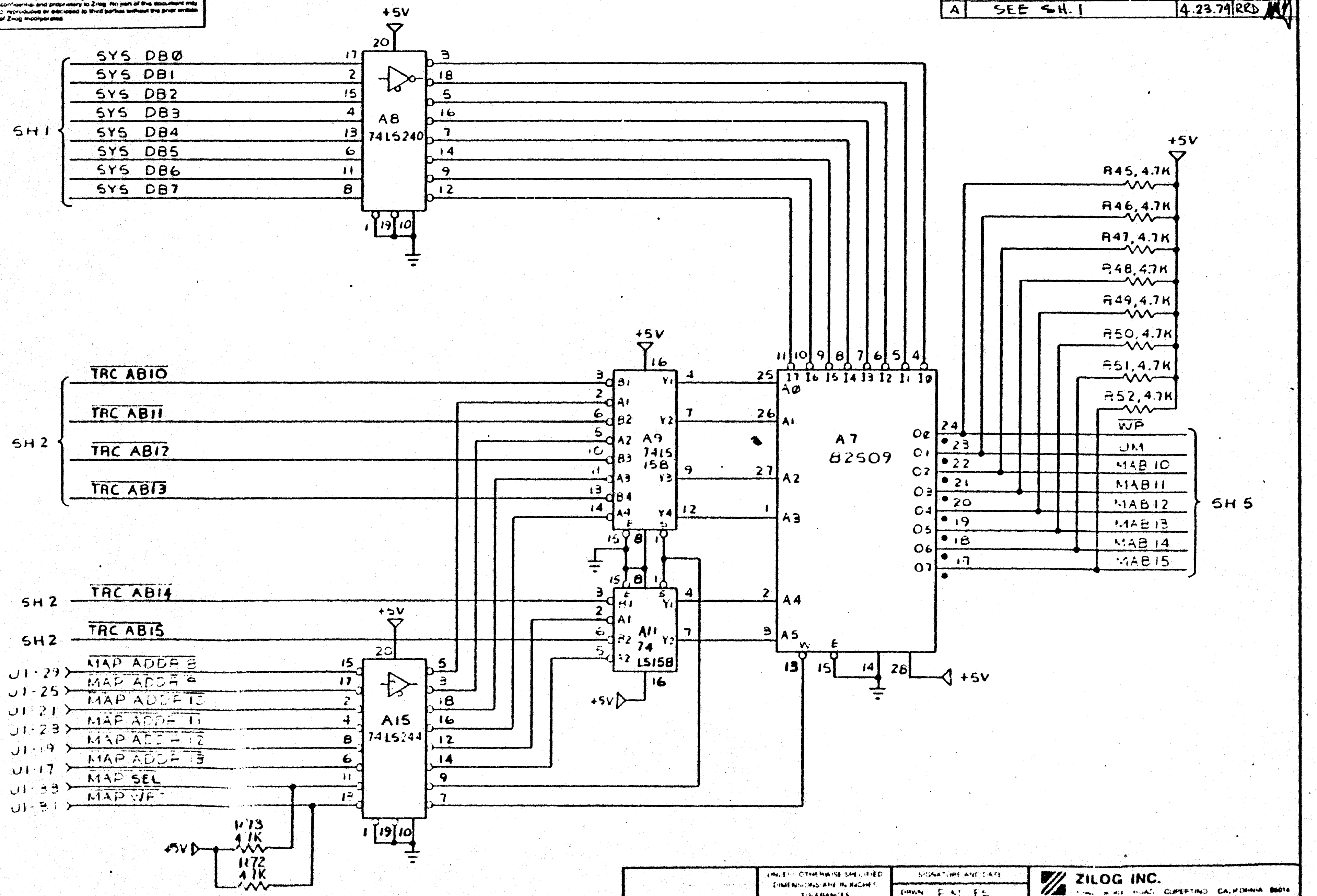
ZILOG INC.

LOGIC DIAGRAM, USER POD

C DZ-0053-05 A

SHEET 3 OF 6

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	SEE SH. I	4.23.79	RRD



SEE SH.I

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLACE DEC ± .02

MAT'L

FINISH

SIGNATURE AND DATE
DRWN F. AYLES
DRFTG CHK
APVD 24 MR 79

ZILOG INC.
ROAD CUPERTINO CALIFORNIA 95014

TITLE
LOGIC DIAGRAM
R POD

SIZE C
DRAWING NO. DZ-0053-05
ISSUE A
SCALE —
SHEET 4 OF 6

CO[illegible]AL

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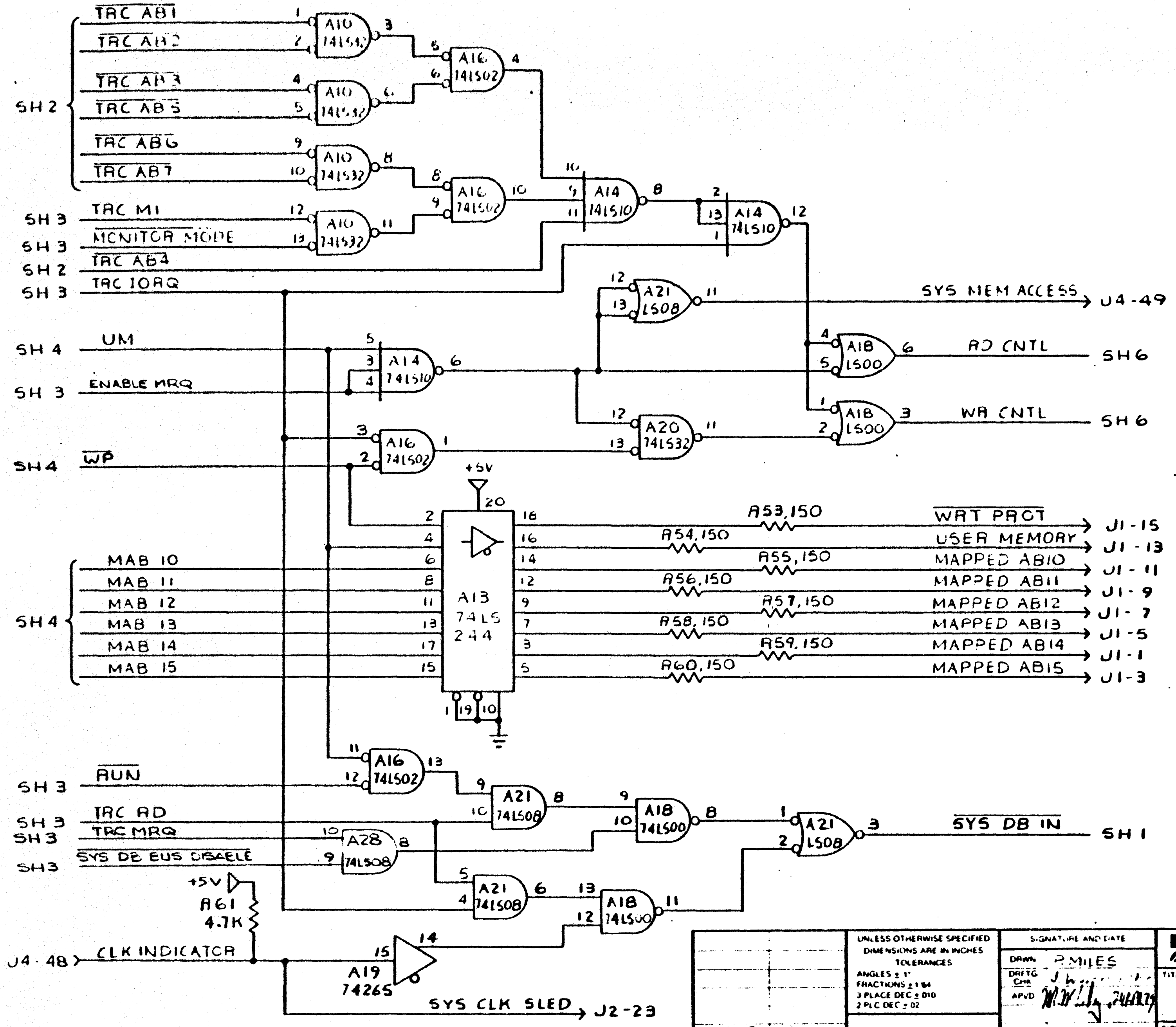
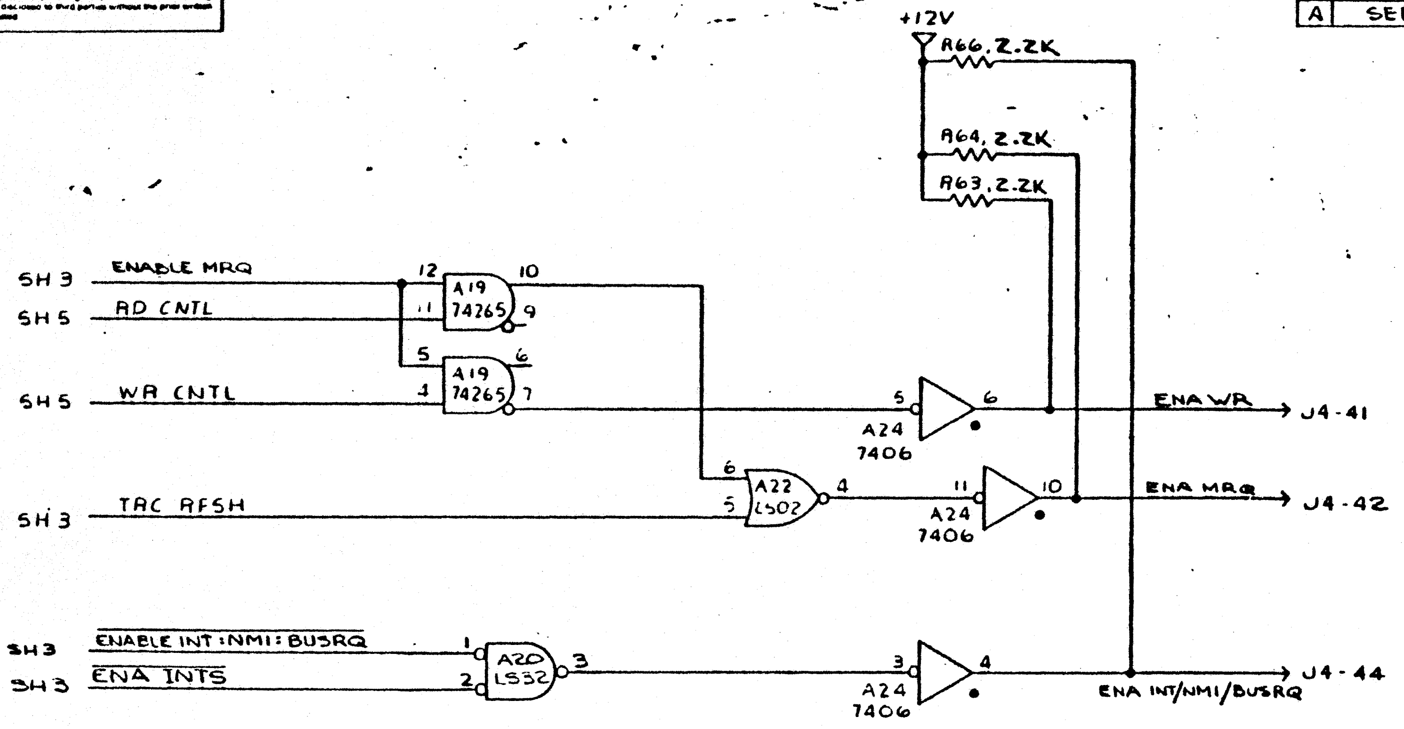
REVISIONS			
LTR	DESCRIPTION		APPROVED
A	SEE SH.1	4.23.79	RRD



SEE SH.1 NEXT ASSY USED ON APPLICATION	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02 MAT'L	SIGNATURE AND DATE DRWN R. MILES DRFTG CHK J. [illegible] APVD [illegible] 7/4/79 FINISH	ZILOG INC. 10460 BUBB ROAD CUPERTINO CALIFORNIA 95014 TITLE LOGIC DIAGRAM USER POD SIZE C DRAWING NO DZ-0053-05 ISSUE A SCALE —— SHEET 5 OF 6

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	SEE SH. I	4.23.79	RRD



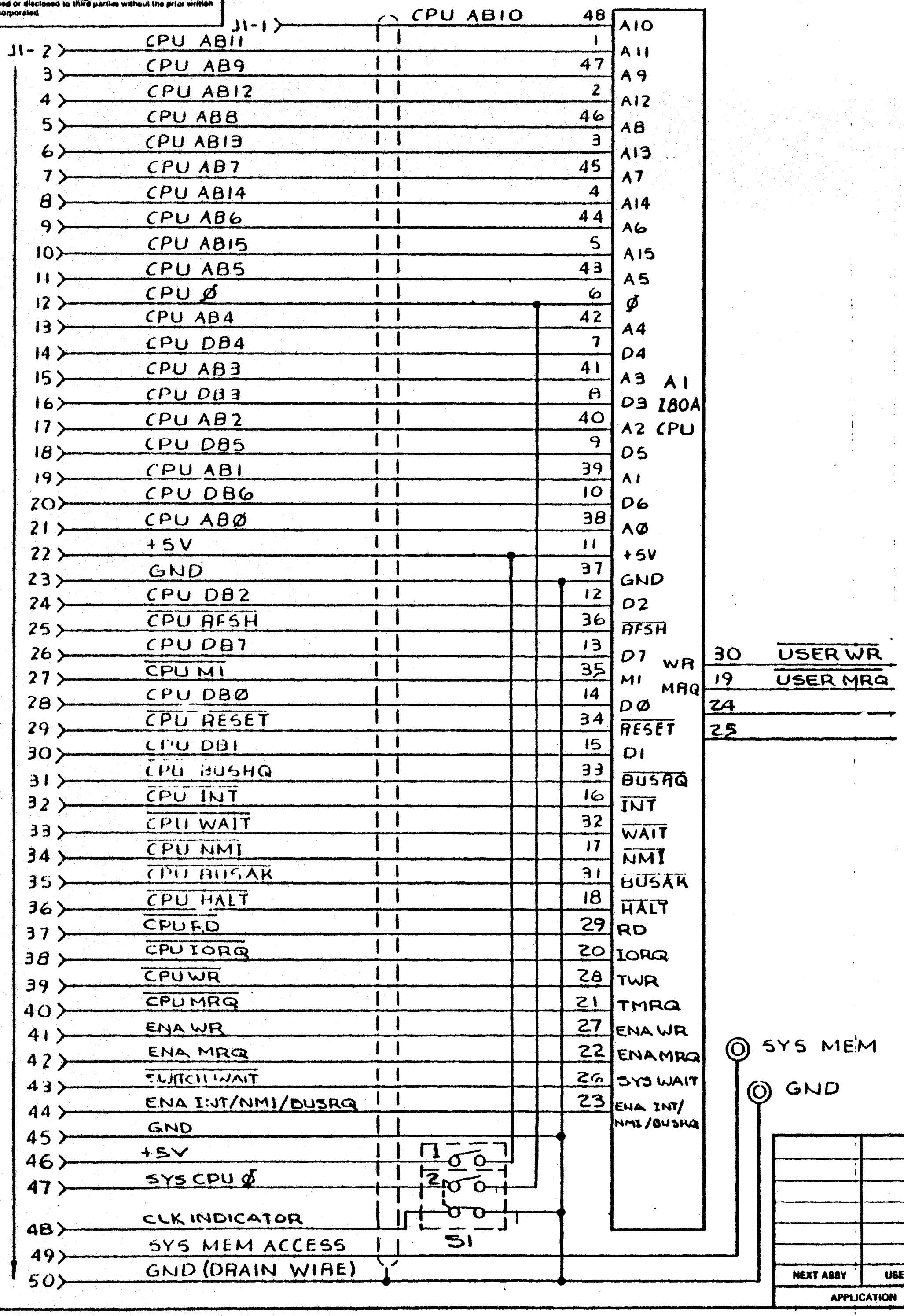
SEE SH. I NEXT ASSY USED ON APPLICATION	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02 MAT'L	SIGNATURE AND DATE DRWN P MILES DRFTG CHK APVD FINISH	ZILOG INC. 10460 BUBB ROAD CUPERTINO CALIFORNIA 95014 TITLE LOGIC DIAGRAM USER POD SIZE C DRAWING NO DZ-0053-05 . ISSUE A SCALE —— SHEET 6 OF 6

LOGIC DIAGRAMS, EMULATOR

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE ECN 00385	9-13-78	LLF
B	ECN 00537	10-27-78	RKO
C	ECN 00634	11-20-78	
D	ECN 00786	1-3-79	RKO

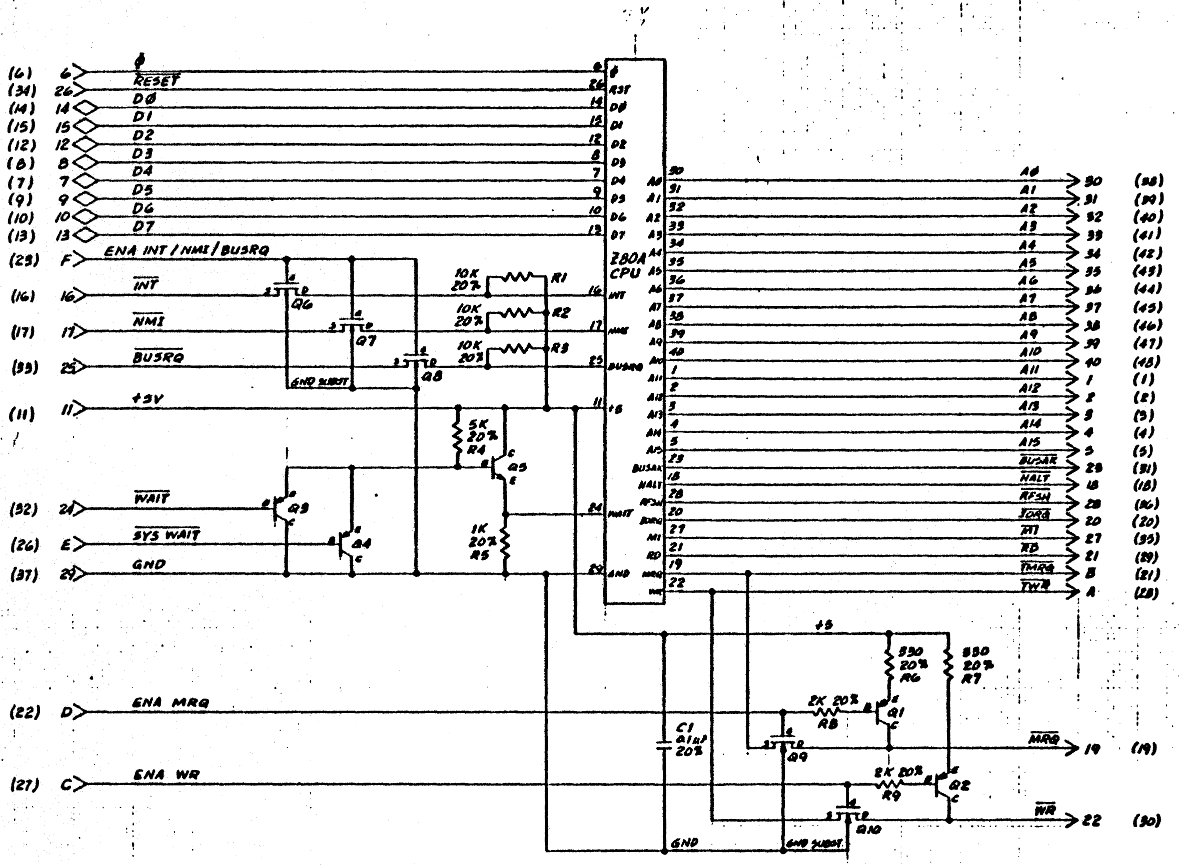
M
M
M



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± 010 2 PLC DEC ± 02	SIGNATURE AND DATE	
			DRWN P. MILES 10-14-77	ZILOG INC. 10460 BUBB ROAD, CUPERTINO, CALIFORNIA 95014
			DRFTG CHK	TITLE LOGIC DIAGRAM EMULATOR
			APVD 780606	
NEXT ASSY	USED ON	MAT'L:	FINISH	SIZE C · DRAWING NO. DZ-0056-02 · ISSUE D
APPLICATION				SCALE NONE · SHEET 1 OF 1

LOGIC DIAGRAMS, Z-80A CPU EMULATOR (HYBRID)

LTR	DESCRIPTION	DATE	APPROVED
D	ECN 00515	12-7-78	



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL PINS PREASSIGNED TO STANDARD 48 PIN DIP AS INDICATED. PACKAGE PIN # IN ( ).
PIN SPACING: 0.100 X 0.600 IN. NOM.
PIN LENGTH: 0.330 IN NOM.

2. MARK:

ZILOG Z80A
CPU EMULATOR
33-0171-01

MARK WITH LOT NUMBER

REV. A	NO LOT, LOT 01 AND LOT 02
REV. B	NONE MADE
REV. C	NONE BUILT
REV. D	LOT 3 AND UP

3.	Q1 AND Q2	2N3546
	Q3 AND Q4	2N2907, 2N2907A, 2N2944, 2N2944A, 2N2945, 2N2945A, 2N2946, 2N2946A
	Q5	2N2222, 2N2222A
	Q6 THRU Q10	SIGNETICS SD5200B MOS FET SWITCH ARRAY

4. PINS H AND G NOT USED (24) AND (25)

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

CONFIDENTIAL

[illegible]

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .005
2 PLC DEC ± .01

CODE IDENT: [illegible]

MAT'L —
FINISH —

SIGNATURE AND DATE	
DRAWN	V Nopman 9 14 78
CHECKED	[illegible] 12/5/78
APVD	[illegible]

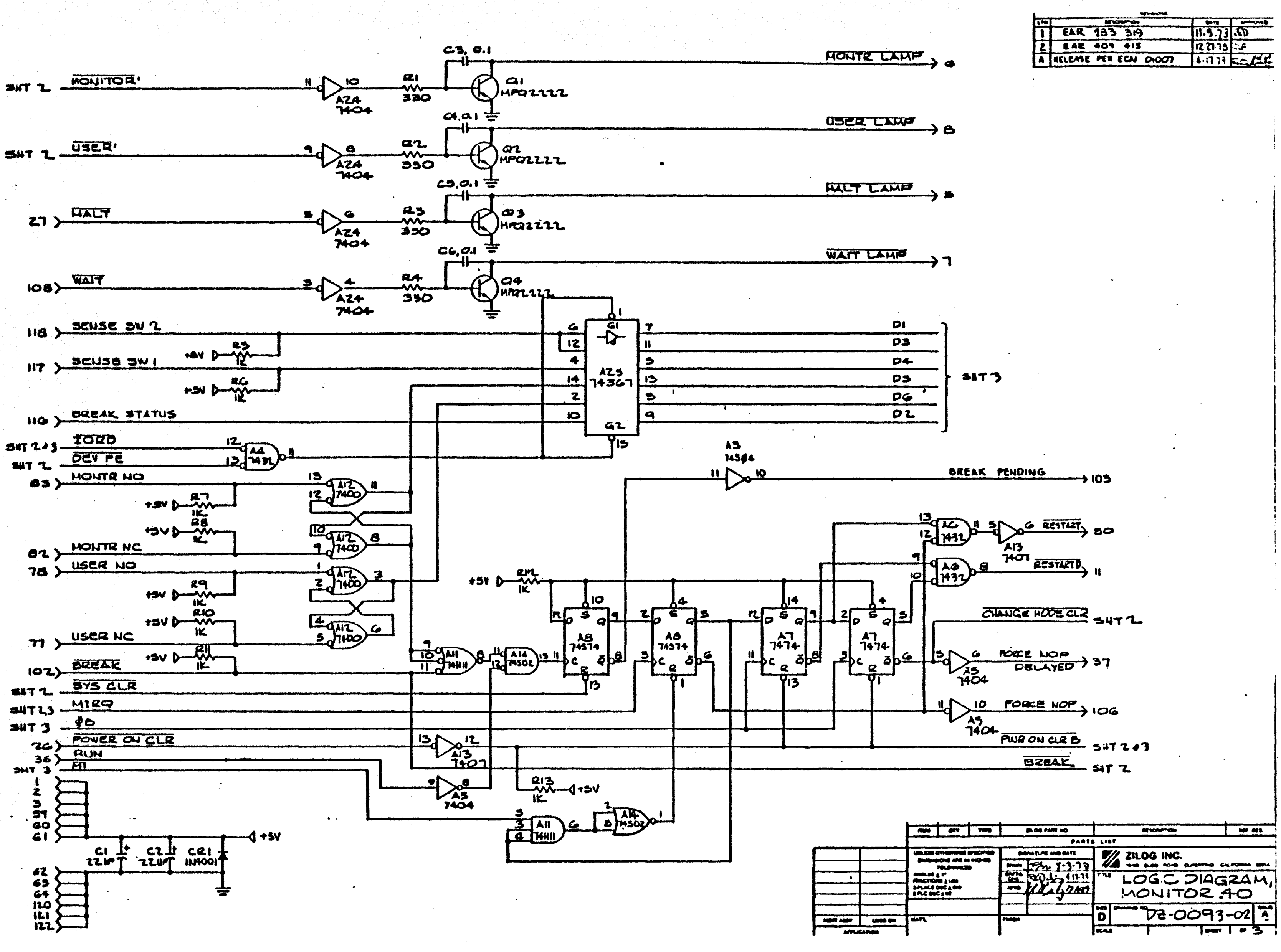
ZILOG INC.
[illegible] CUPERTINO, CALIFORNIA [illegible]

TITLE
Z80A CPU EMULATOR

SIZE	DRAWING NO	ISSUE
D	33-0171-01	D

SCALE NONE SHEET 1 OF 1

LOGIC DIAGRAMS, MONITOR.40



LTR	DESCRIPTION	DATE	APPROVED
1	EAR 183 319	11.9.73	ED
2	EAR 409 415	12.21.73	JF
A	RELEASE PER ECN 01007	6.17.73	

PARTS LIST

ZILOG INC.

DRAWN 5-3-73

CHECKED 6-11-73

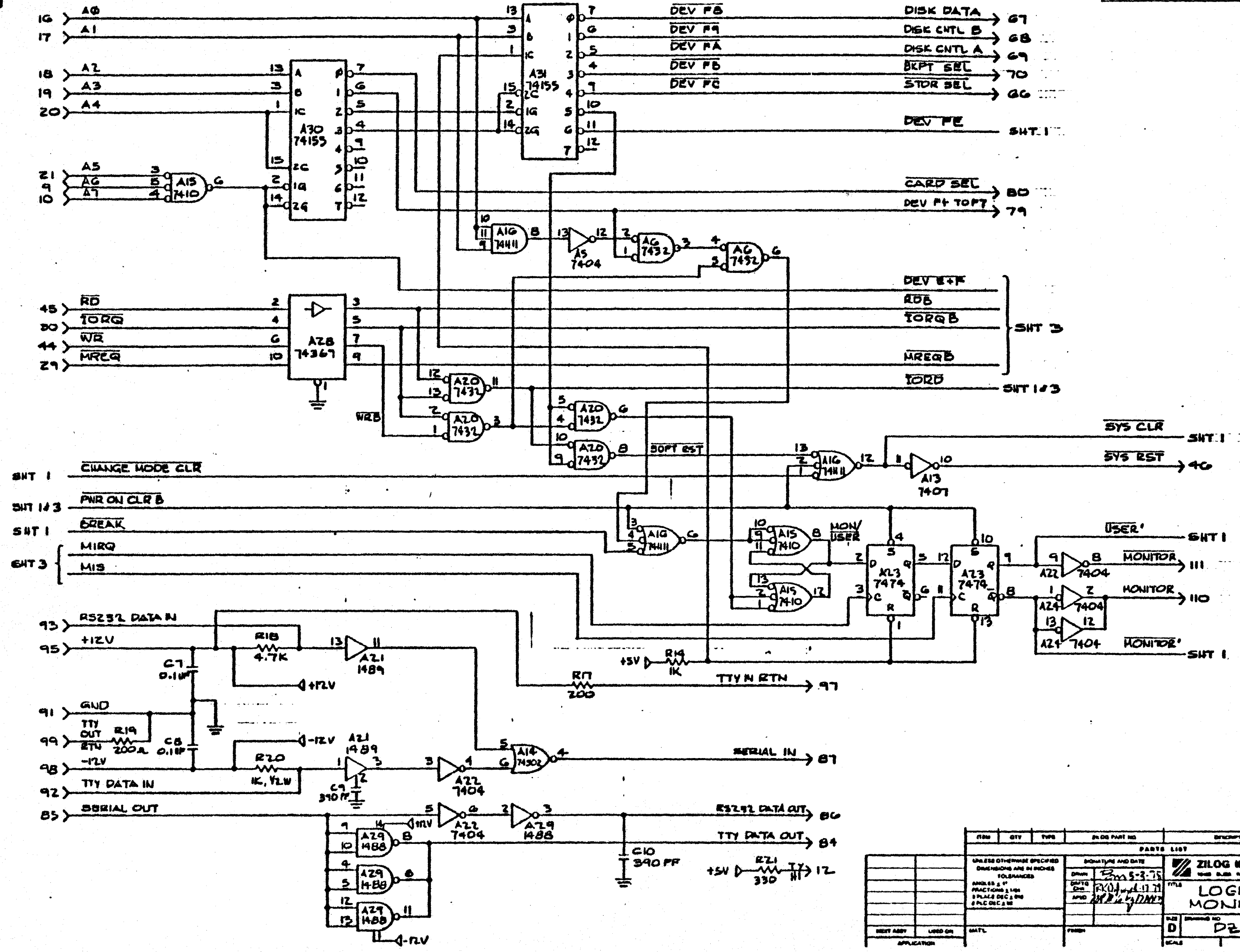
TITLE LOGIC DIAGRAM, MONITOR 40

SIZE D DRAWING NO. D2-0093-02 REV A

SHEET 1 OF 3

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	SEE SHT 1	4-17-79	[illegible]



ZILOG INC.

TITLE LOGIC DIAGRAM, MONITOR 40

DRAWN [illegible] 5-3-75

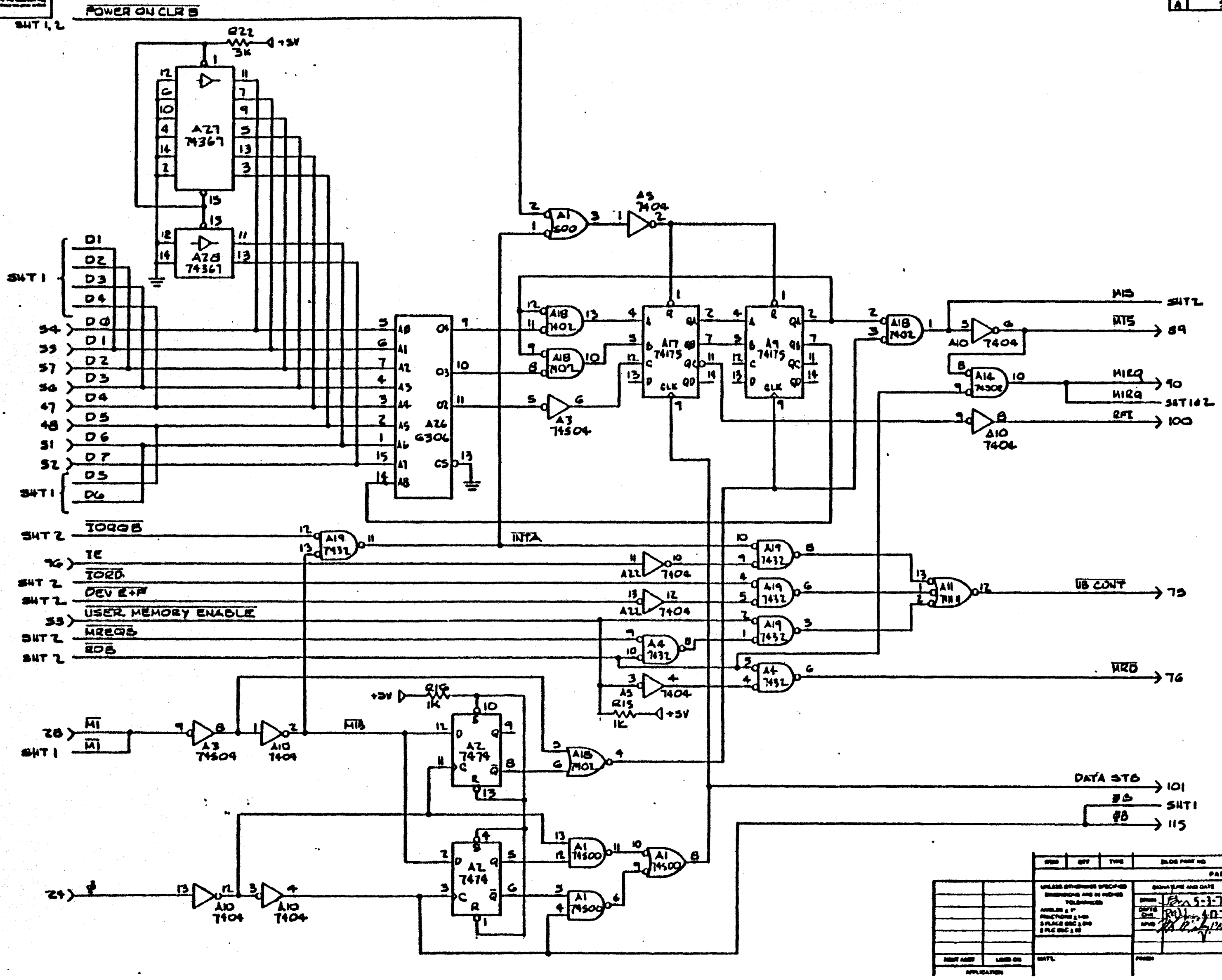
DFTG CHK [illegible] 4-17-79

APVD [illegible]

SIZE D DRAWING NO DZ-0093-02 REV A

SHEET 2 OF 4

LTR	DESCRIPTION	DATE
A	SEE SHT 1	4-12-79



ZILOG INC.

TITLE LOGIC DIAGRAM, MONITOR 40

DRAWN 5-3-76

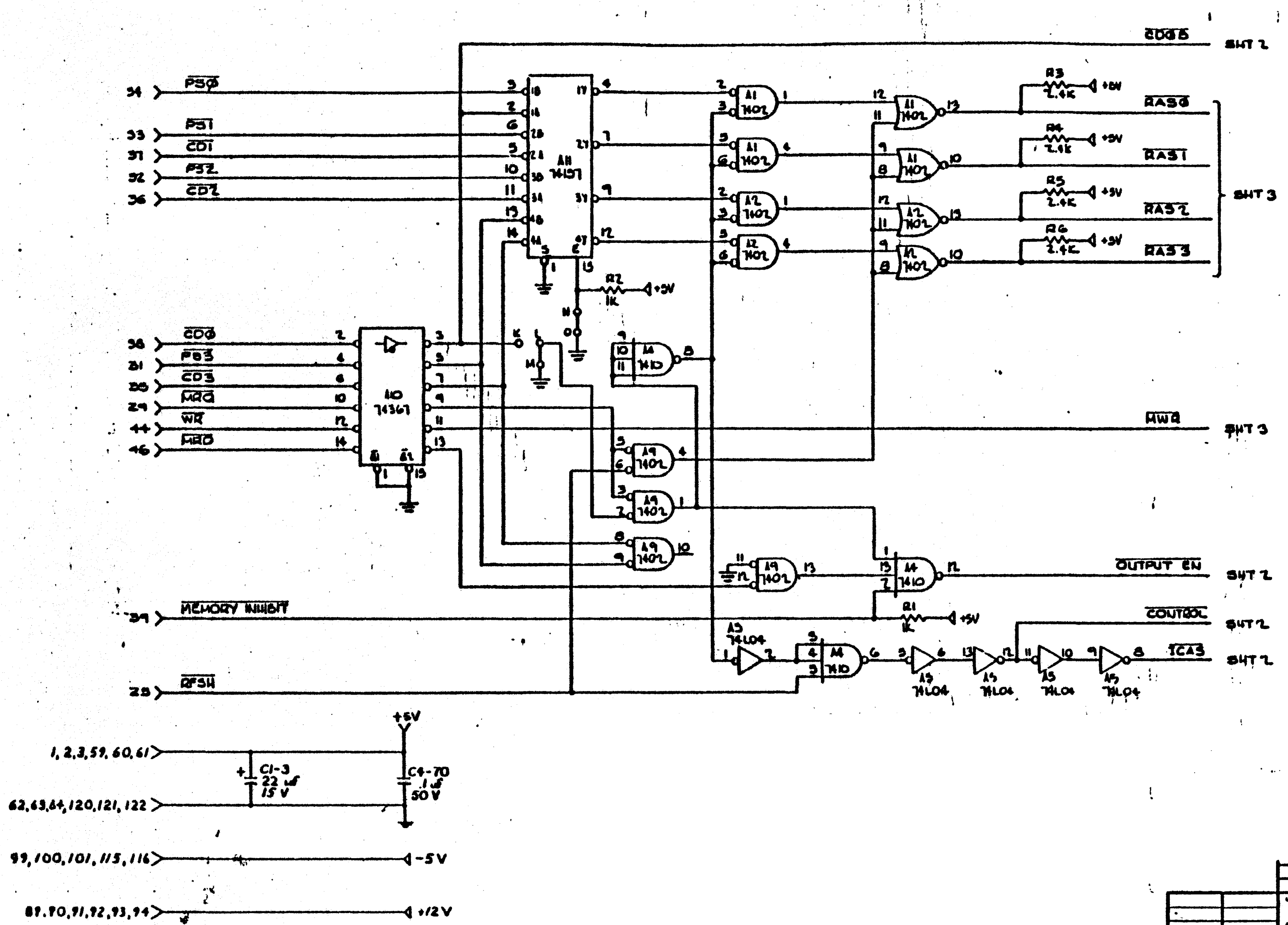
CHK 4-12-79

SIZE D DRAWING NO DZ-0093-02 REV A

SHEET 3 OF 3

LOGIC DIAGRAMS, MEMORY 25

A	ECN 00320	9-1-78	
B	ECN 00482	4.16.79	



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS. 1/4 W, 5%
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.

REF. DESIG.	
LAST USED	UNUSED
A43	
C70	
R7	

PARTS LIST

ZILOG INC.

LOGIC DIAGRAM,
MEMORY 25

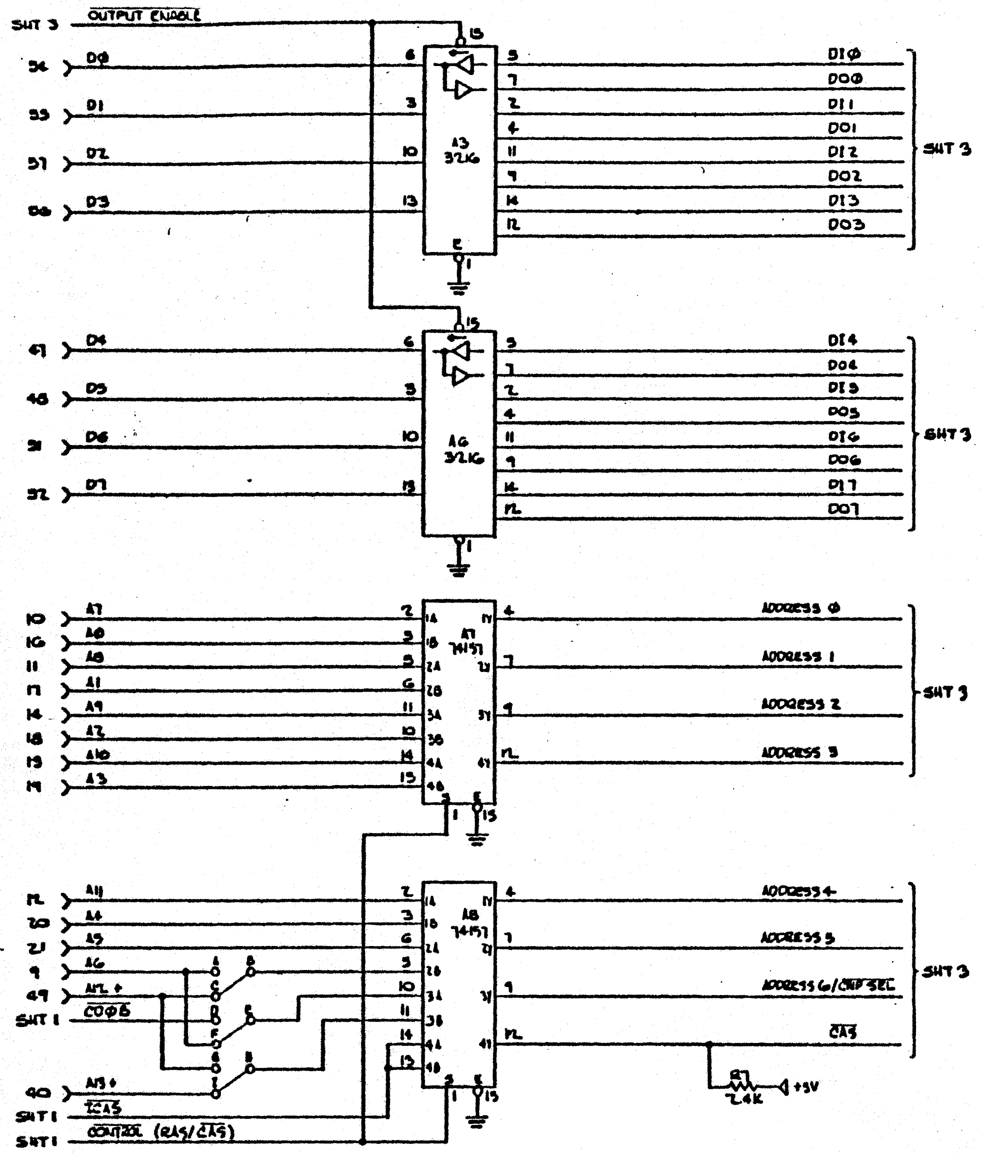
	ZDS-1/40
02-0101-0	ZDS-1/25

6-23-76

D 02-0101-01 B

SHEET 1 OF 3

LTR	DESCRIPTION	DATE	APPROVED
B	SEE SHT. 1	4 4 79	[illegible]



ITEM	QTY.	TYPE	ZILOG PART NO.	DESCRIPTION	REF DES.

PARTS LIST

ZILOG INC.

	ZDS-1/40
09-0101-01	ZDS-1/25
NEXT ASSY	USED ON

APPLICATION

SIGNATURE AND DATE

DRAWN Bm 4-28-75

DRFTG CHK NF 4 16 78

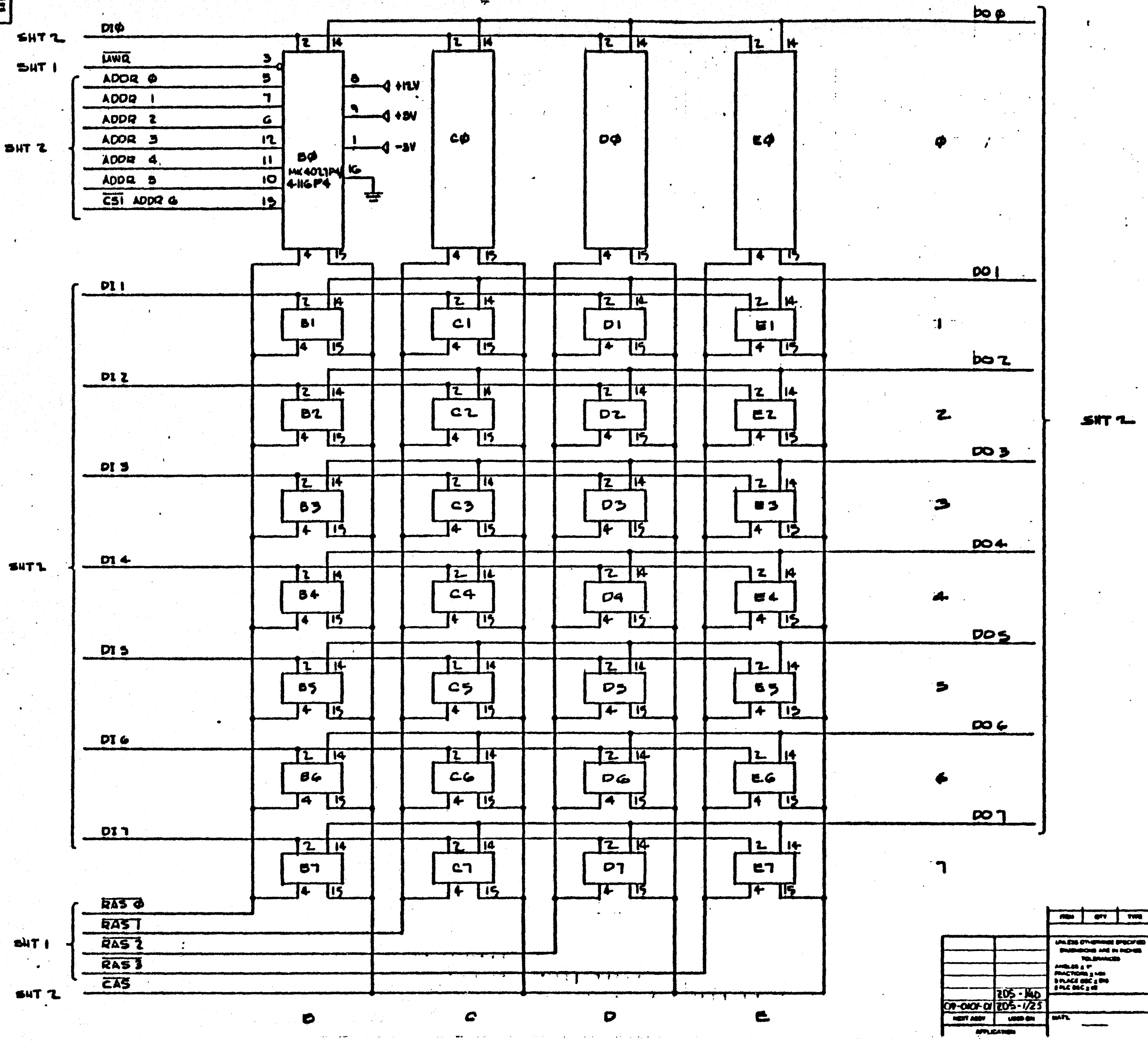
APVD K Hennig 3 8 75

TITLE LOGIC DIAGRAM,
MEMORY 25

SIZE D DRAWING NO. 02-0101-01. ISSUE B

SCALE SHEET 2 OF 3

B	SEE SHT 1	4-16-79	



ALL DEVICES ARE WIRE AS
SHOWN ON DEVICE NO BΦ
FOR 16K x8 USE MK4027P-4
FOR 60K x8 USE MK4116P-4

PARTS LIST

	205-140
09-0101-01	205-1/25

ZILOG INC.

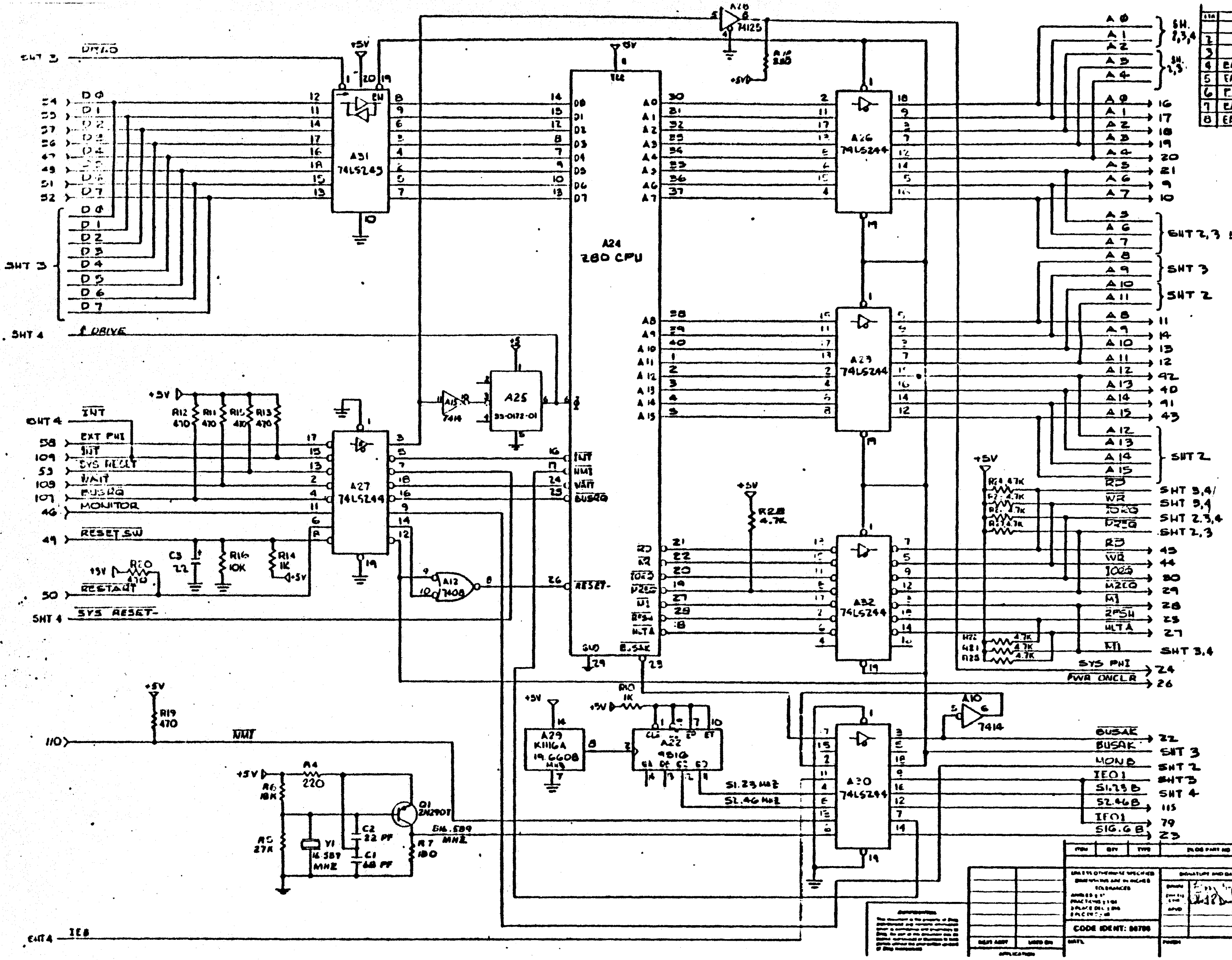
LOGIC DIAGRAM,
MEMORY 25

D | DZ-0101-01 | B

SHEET 3 OF 3

LOGIC DIAGRAMS, CPU

(09-0099-01)



NOTES:- UNLESS OTHERWISE SPECIFIED
1 ALL RESISTANCE VALUES IN OHMS 1/4 W. 5 %
2 ALL CAPACITANCE VALUES IN UF.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
2			
3			
4	EAR 002, 035, 139, 041		
5	EAR 186	10.17.78	RD
6	EAR 262, 277	11.3.78	RD
7	EAR 301, 306, 316	11.3.78	RD
8	EAR 511, 564	2.2.79	RW

DEVICE TABLE	
TYPE	REFERENCE DES.
7400	A1 A6
7432	A2 A5. A7. A11
9321	A3. A33
7420	A4
7474	A8
7414	A10. A15
7408	A12
9118	A13. A14
74LS245	A16 A31
2708	A17 A18 A19
Z80-CTC	A20
9551	A21
9316	A22
74LS244	A23 A26 A27 .A30.A32
Z80-CPU	A24
CLK DRVR	A25
74125	A28
K-1116	A29
74LS283	A34

REFERENCE DESIGNATION		
COMP	LAST USED	NOT USED
IC	A34	A9
CAP	C36	
DIODE	CR1	
RESISTOR	Q1	
RESISTOR	R28	
CRYSTAL	Y1	

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

CODE IDENT: 00786

ZILOG INC.

LOGIC DIAGRAM, CPU 2

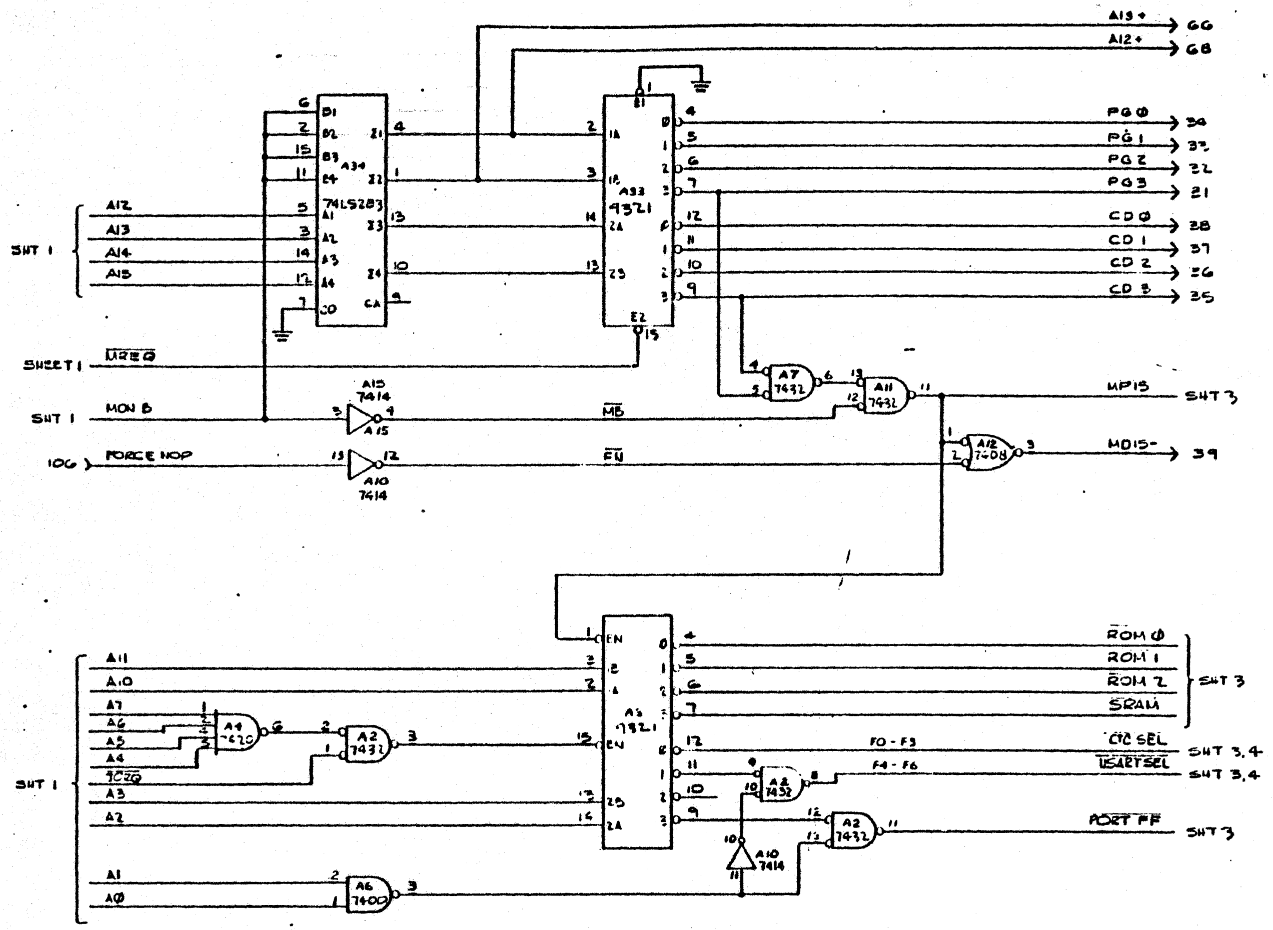
D

DZ-0099-01

SHEET 1 OF 6

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
7	SEE SHT. 1	11.8.78	RRD



CONFIDENTIAL

PARTS LIST

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

NEXT ASSY | USED ON

APPLICATION

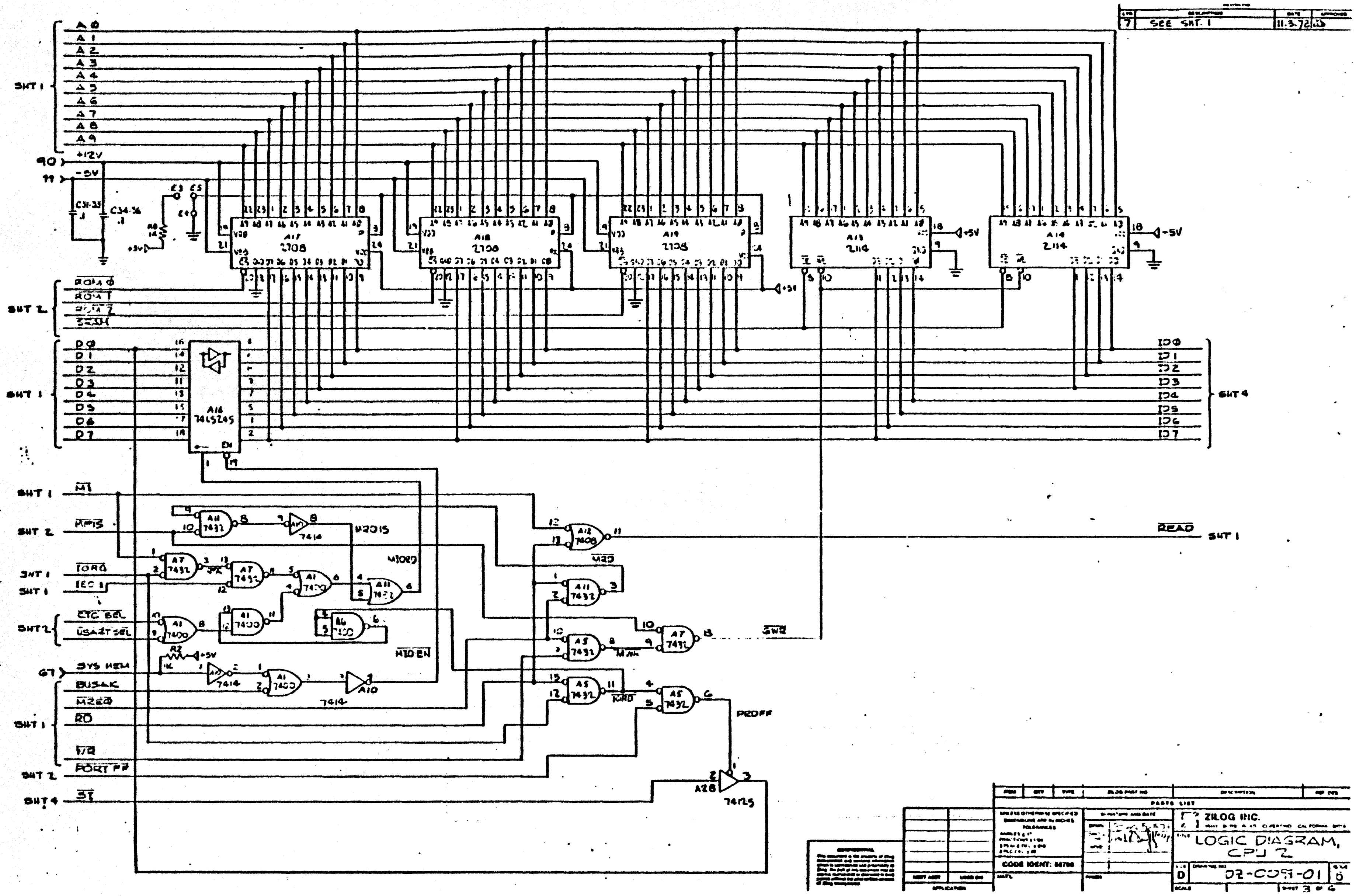
CODE IDENT: 34700

ZILOG INC.

TITLE LOGIC DIAGRAM, CPU 2

SIZE D DRAWING NO. D2-0099-01

SCALE SHEET 2 OF 4



LTR	DESCRIPTION	DATE	APPROVED
7	SEE SHT. 1	11.3.72	JJ

PARTS LIST

ZILOG INC.

LOGIC DIAGRAM,
CPU 2

CODE IDENT: 56790

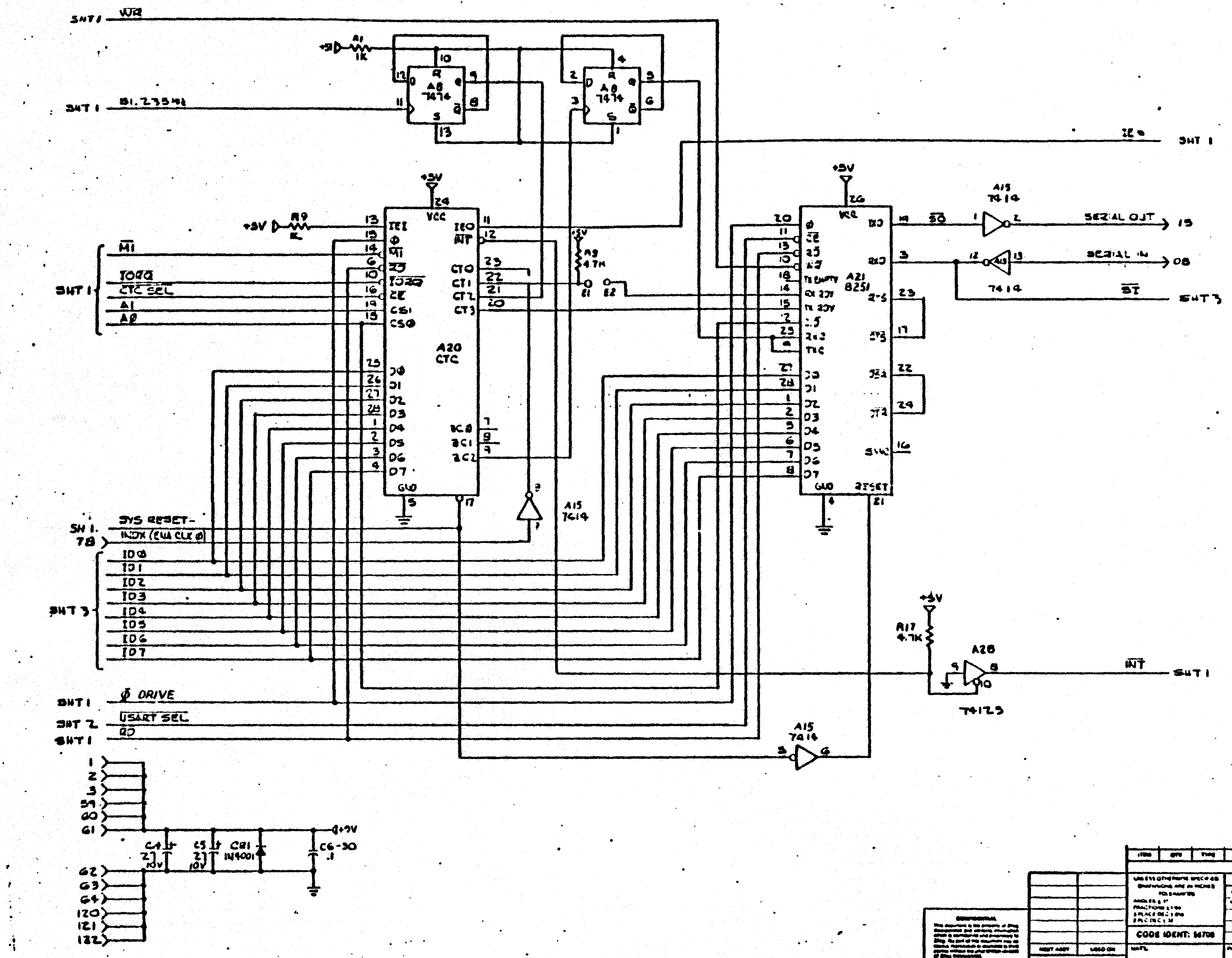
D

02-C09-01

0

SHEET 3 OF 6

7	SEE SHT 1	11 3 7



CONFIDENTIAL

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
2 PLACE DEC ± .010
3 PLACE DEC ± .005

CODE IDENT: 56708

MAT'L

SIGNATURE AND DATE
DRWN
CHK
APVD

FINISH

ZILOG INC.

TITLE LOGIC DIAGRAM, CPU 2

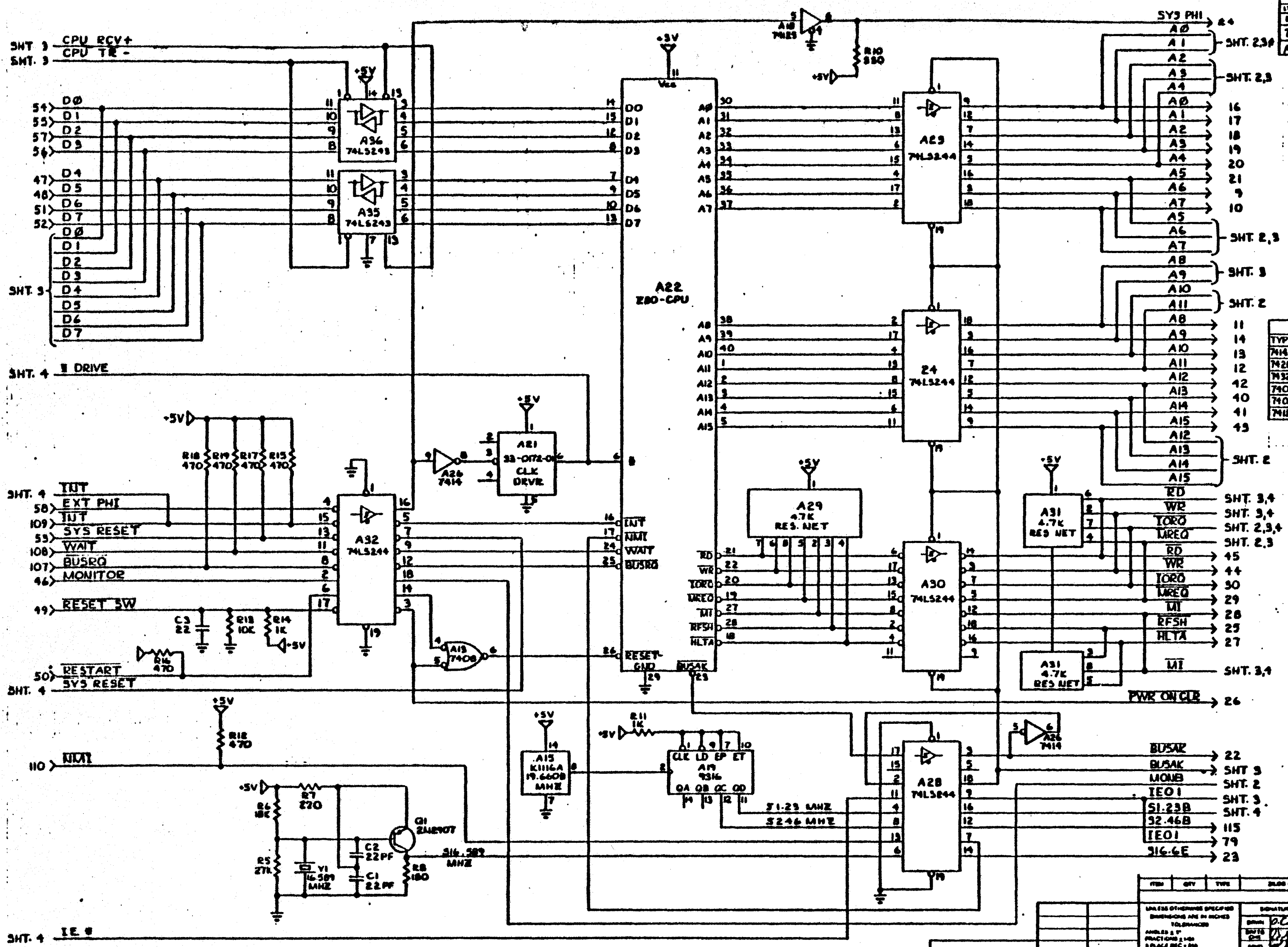
SIZE D DRAWING NO D2-0099-01 ISSUE 8

SCALE SHEET 6 OF 6

LOGIC DIAGRAMS, CPU-3

(09-0099-03)

LTR	DESCRIPTION	DATE	APPROVED
1	EAR # 298	12.11.78	RED
2	EAR # 459,564	1.29.79	RED
A	RELEASE PER ECN 01017	4.17.79	RED



DEVICE TABLE				
TYPE	GND	Vcc	REF. DES.	USED OUTPUT PINS
7414	7	14	A3 A26	A3-8,12 A26-9
7420	7	14	A5	A5-8
7432	7	14	A6	A6-3,6,11
7400	7	14	A7	A7-8,11
7408	7	14	A13	A13-3,11
74125	7	14	A18	A18-3

REF. DES.	
HIGHEST USED	NOT USED
A36	
R19	
C36	
Y1	
Q1	

NOTES-UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTANCE VALUES IN OHMS, 1/4W, 5%
2. ALL CAPACITANCE VALUES ARE IN µF.

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

CONFIDENTIAL

10-0099-03 | 2D6-1140
NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .03

CODE IDENT: 56700

MATL | FINISH

SIGNATURE AND DATE
DRWN 11-9-78
CHKD
APPD

ZILOG INC.

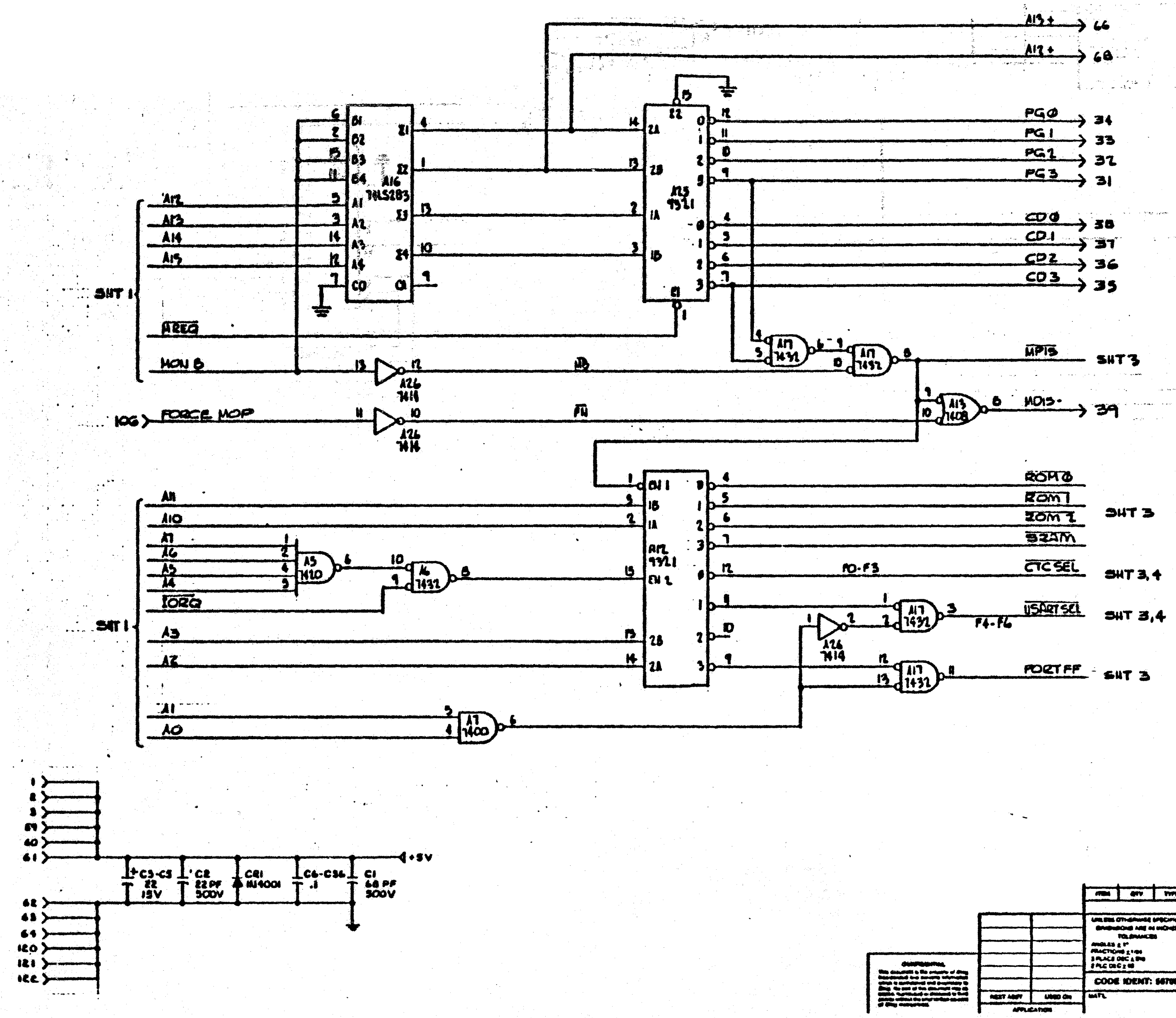
TITLE LOGIC DIAGRAM CPU 3

SIZE D DRAWING NO DZ-0099-03 ISSUE A

SCALE NONE SHEET 1 OF 4

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	SEE SHEET 1	4.17.79	RV



ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

CONFIDENTIAL

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .005
2 PLC DEC ± .01

CODE IDENT: 56700

MAT'L

SIGNATURE AND DATE
DRAWN 11-2-78
DSGN CHK
APPD

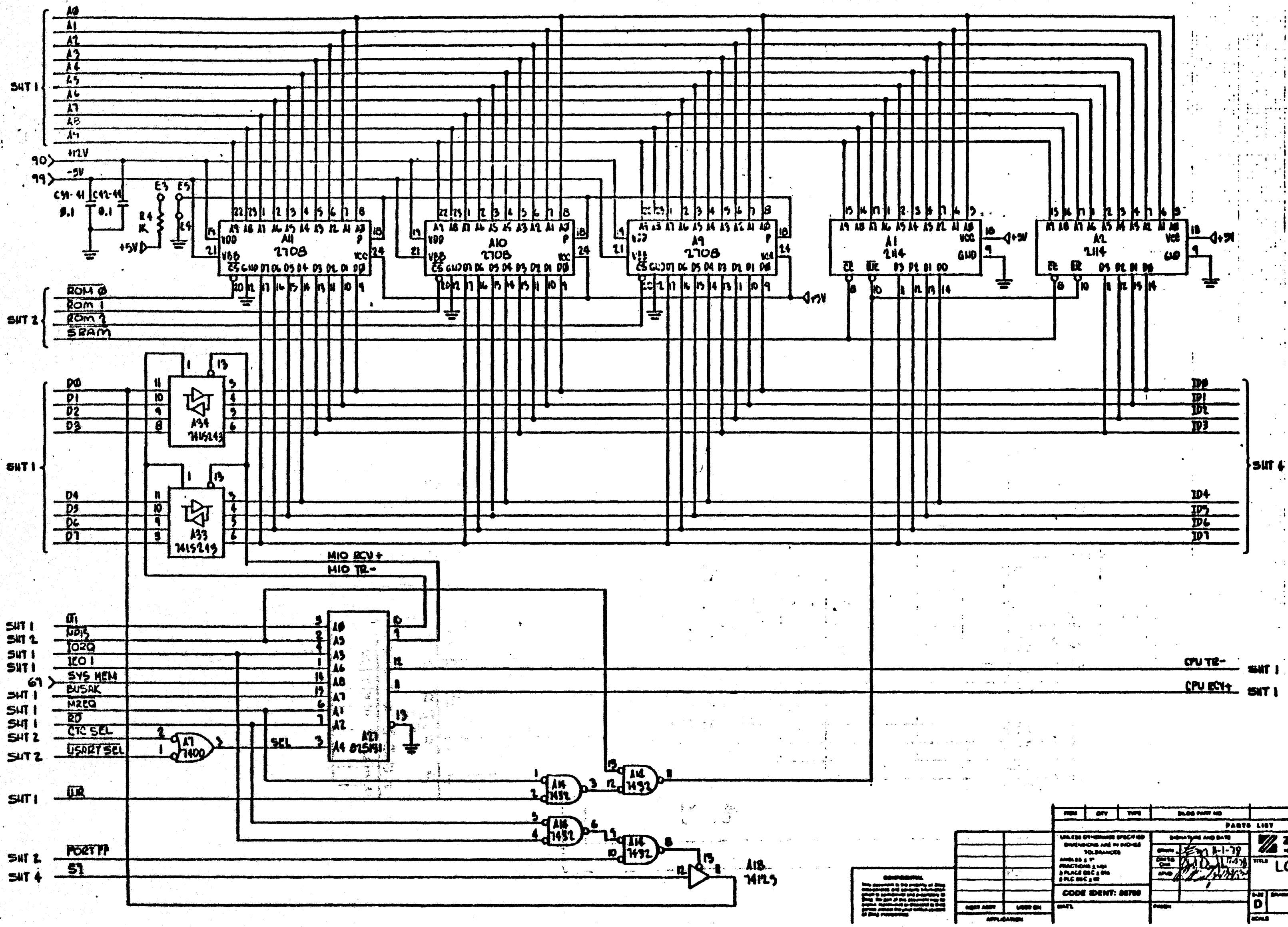
FINISH

ZILOG INC.
10411 BUBB ROAD, CUPERTINO, CALIFORNIA 95014

TITLE LOGIC DIAGRAM, CPU 3

SIZE D
DRAWING NO DZ-0099-03
REV A
SCALE
SHEET 2 OF 4

LTR	DESCRIPTION	DATE	APPROVED
A	SEE SHEET 1	4-17-79	



PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .005
2 PLC DEC ± .01

CODE IDENT: [illegible]

SIGNATURE AND DATE
DRAWN 1-1-79

ZILOG INC.
10411 BUBB ROAD, CUPERTINO, CALIFORNIA 95014

TITLE LOGIC DIAGRAM, CPU 3

SIZE D DRAWING NO. DZ-0099-03 REV A

SHEET 3 OF 4

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
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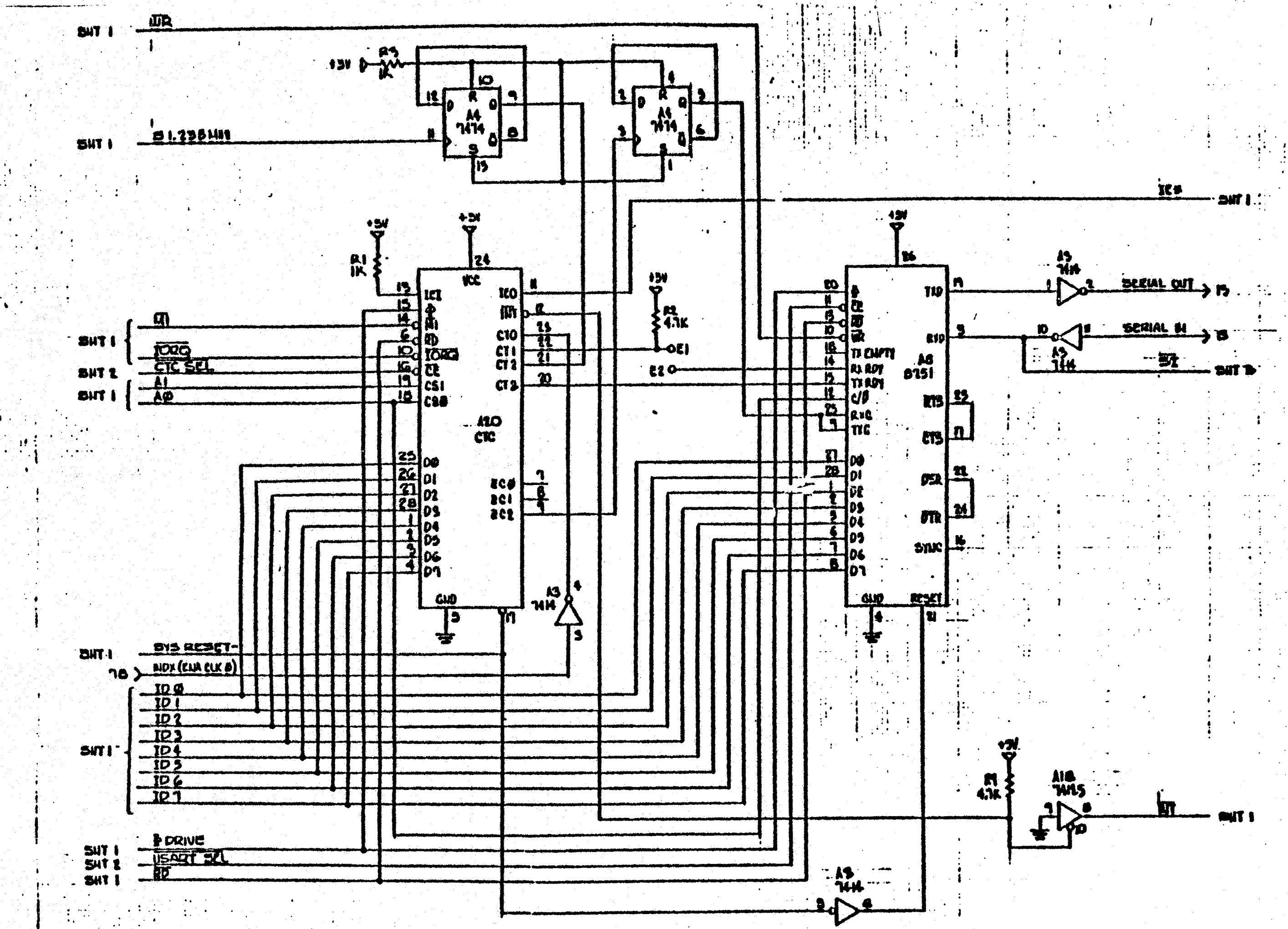


PARTS LIST

ZILOG INC.

TITLE LOGIC DIAGRAM, CPU 3

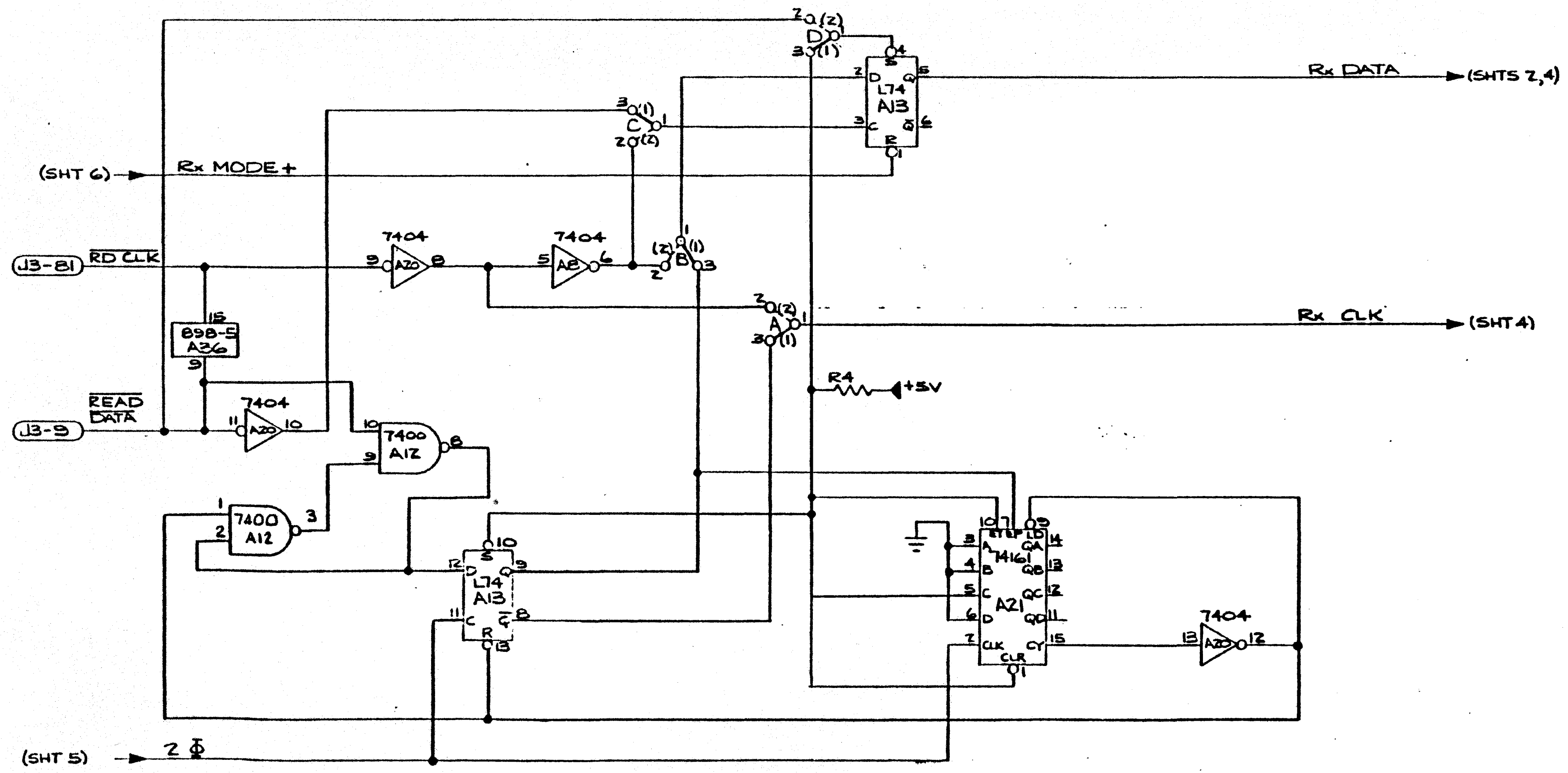
D 02-0099-03 A.

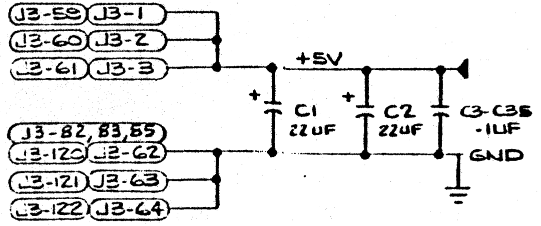
SHEET 4 OF 4

LOGIC DIAGRAMS, FLOPPY CONTROLLER

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
C	ECN 00202	1-26-8	A~
D	ECN 00610	11-8-78	A~

M



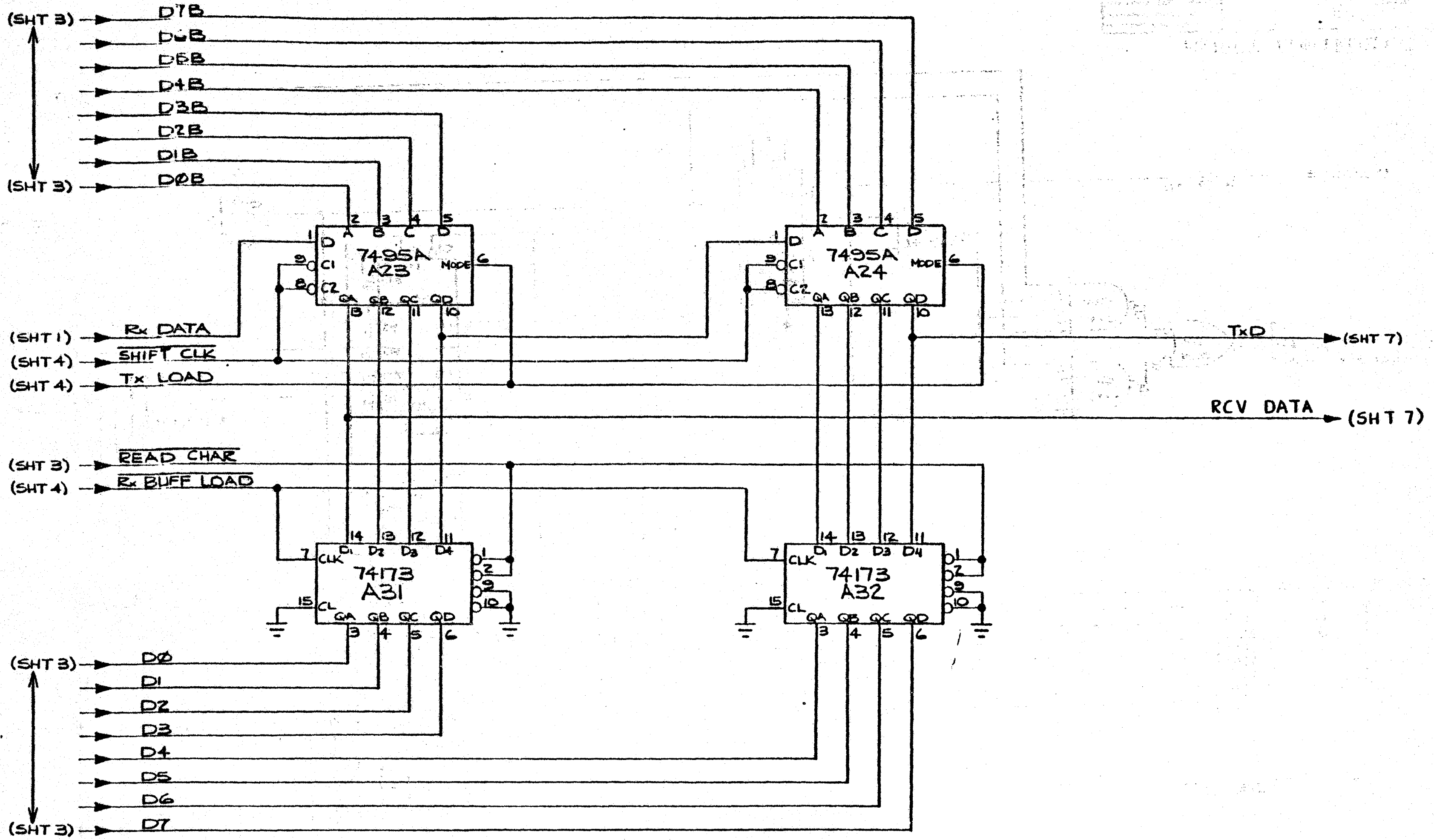


J-3

FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	Zilog
APPROVALS / DATE DRAWN M. Lic 4-13-76 CHECKED	CONFIDENTIAL This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced or disclosed to third parties without the prior written consent of Zilog Incorporated.
	SCALE NONE / SIZE C / DRAWING NO DZ-0004-01
	DO NOT SCALE DRAWING / SHEET 1 OF 7

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	



FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

APPROVALS	DATE
DRAWN Malie	4-13-76
CHECKED	

Zilog

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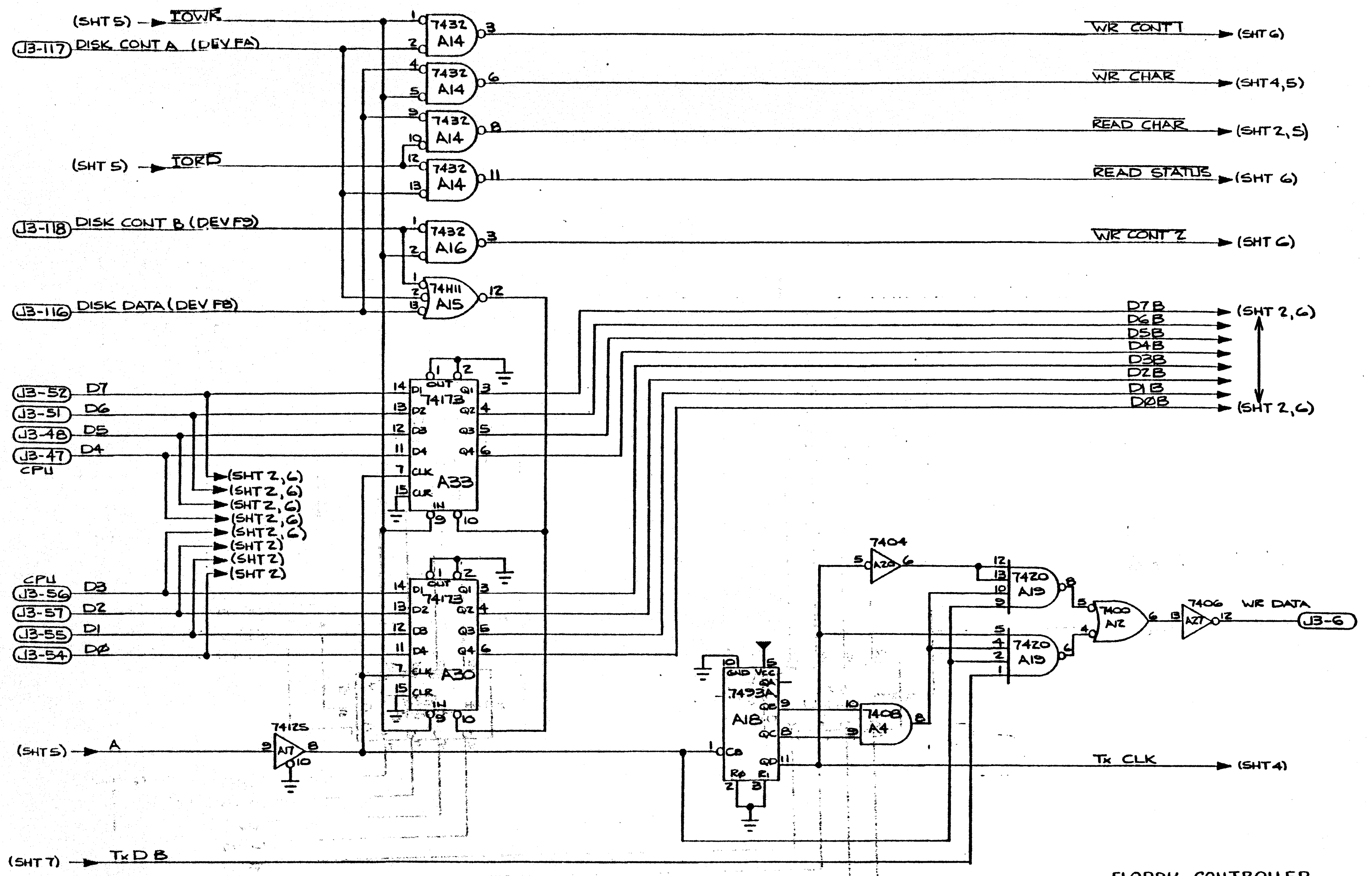
SCALE NONE | SIZE C | DRAWING NO. DZ-0004-01

DO NOT SCALE DRAW | SHEET 2 OF 7

BISHOP GRAPHICS / ACC
REORDER NO. A-6719

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	



FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED

FRACTIONS ± DEC ± ANGLES ±

APPROVALS	DATE
DRAWN	4-12-76
CHECKED	

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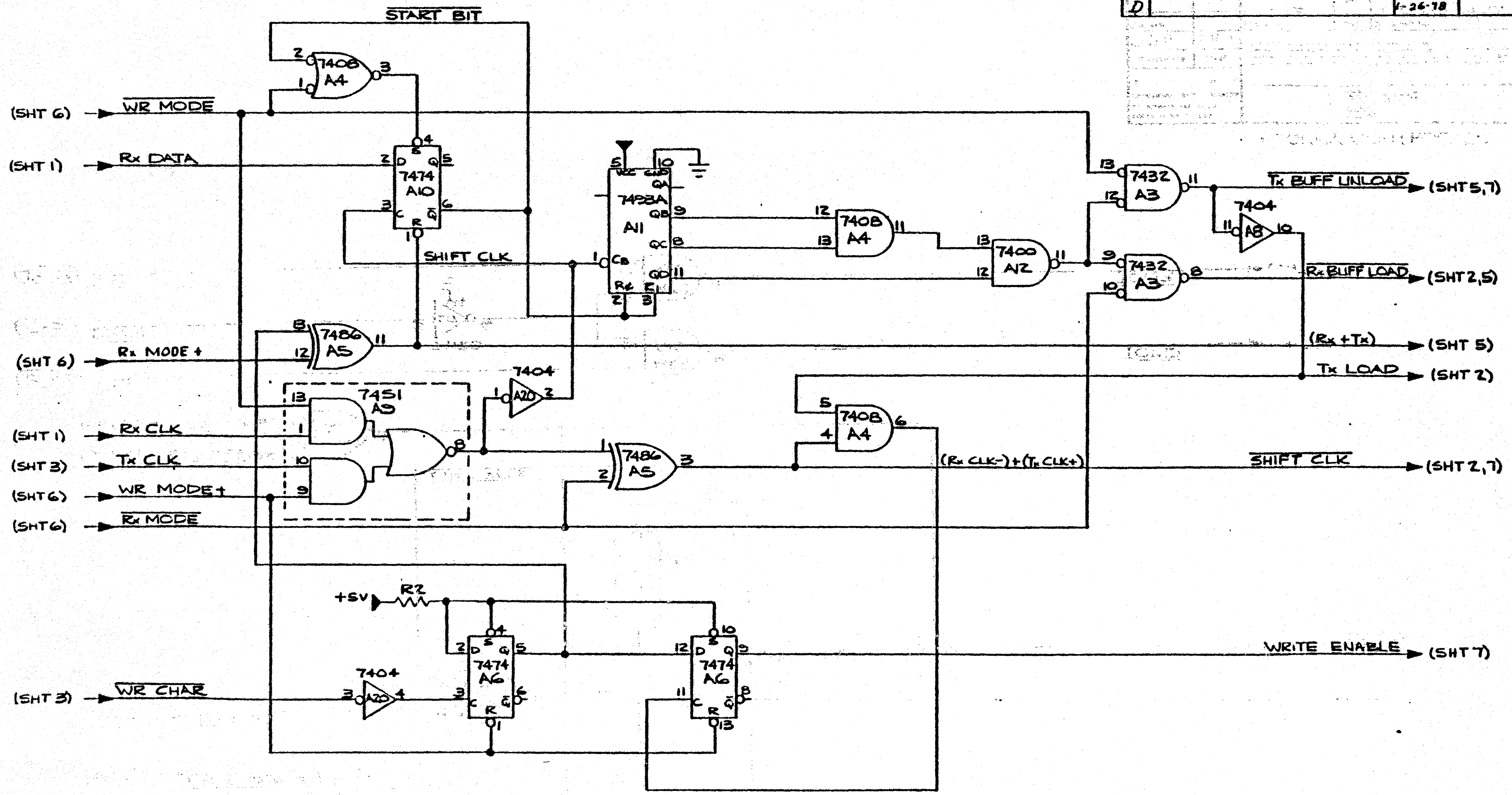
SCALE NONE | SIZE C | DRAWING NO. DZ-0004-01

DO NOT SCALE DRAWING | SHEET 3 OF 7

BISHOP GRAPHICS / ACCUPRESS REORDER NO. A-6719

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	



FLOPPY CONTROLLER

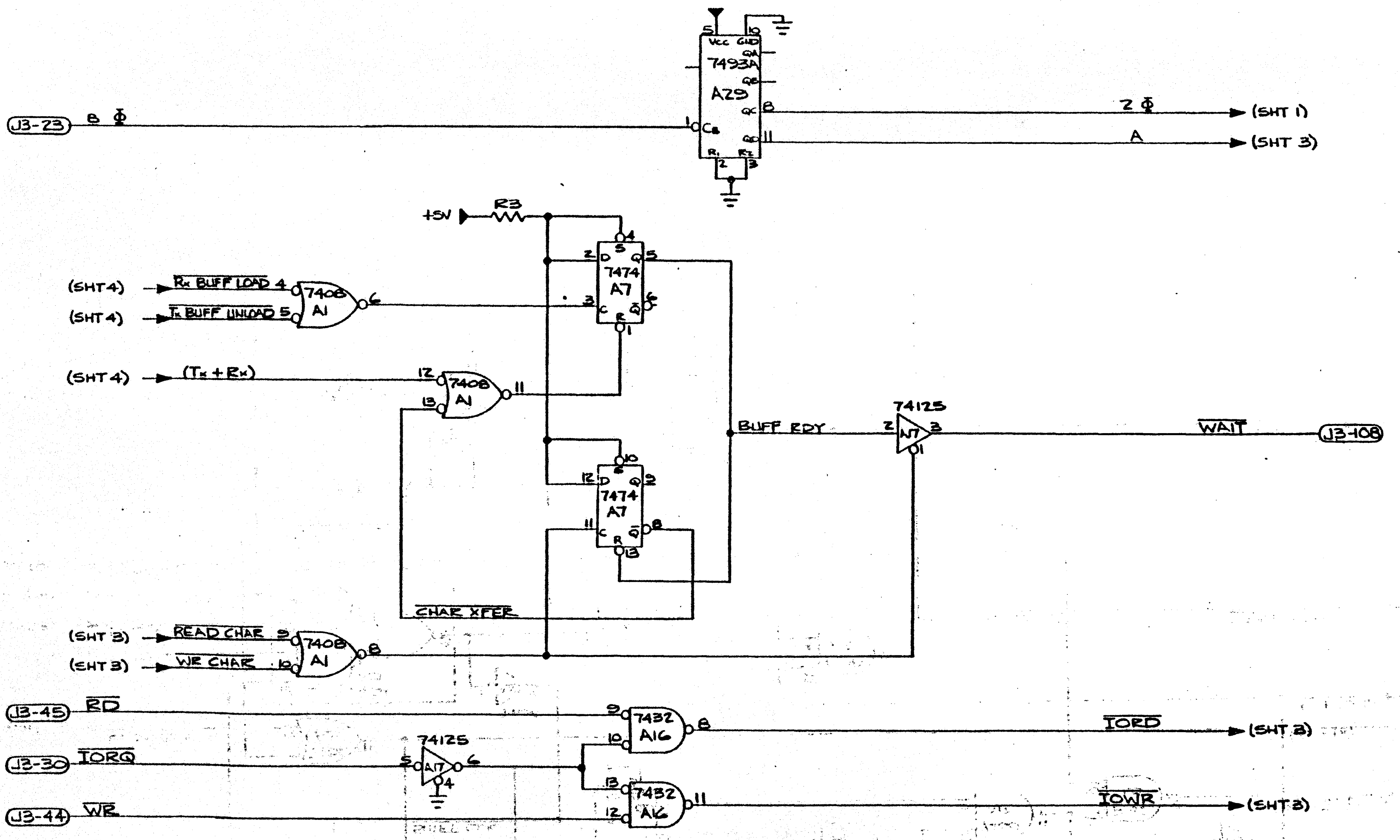
TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	Zilog
	CONFIDENTIAL This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced or disclosed to third parties without the prior written consent of Zilog, Incorporated

APPROVALS	DATE
DRAWN	4-15-76
CHECKED	

SCALE NONE | SIZE C | DRAWING NO DZ-000401

DO NOT SCALE DR | SHEET 4 OF 7

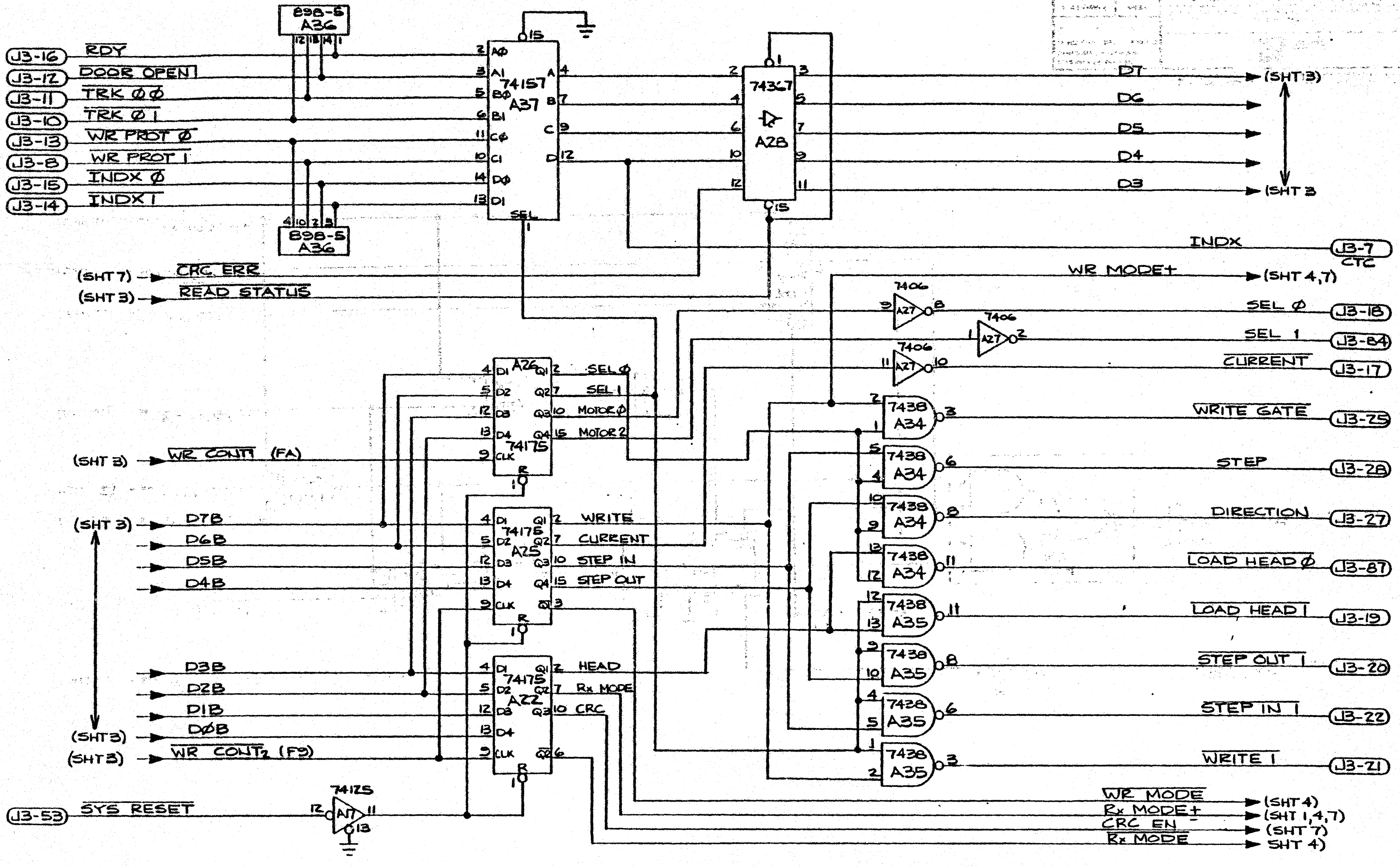
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	



FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED			Zilog		
FRACTIONS	DEC	ANGLES	CONFIDENTIAL This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced or disclosed to third parties without the prior written consent of Zilog Incorporated		
±	±	±			
APPROVALS	DATE				
DRAWN Nilie	4-15-7_		SCALE 1/1 E	SIZE C	DRAWING NO DZ-0004-01
CHECKED					
			DO NOT SCALE DRAWING		SHEET 5 OF 7

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	



FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN Ilalic	4-15-76
CHECKED	

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SCALE	SIZE	DRAWING NO.
NONE	C	DZ-0004-01

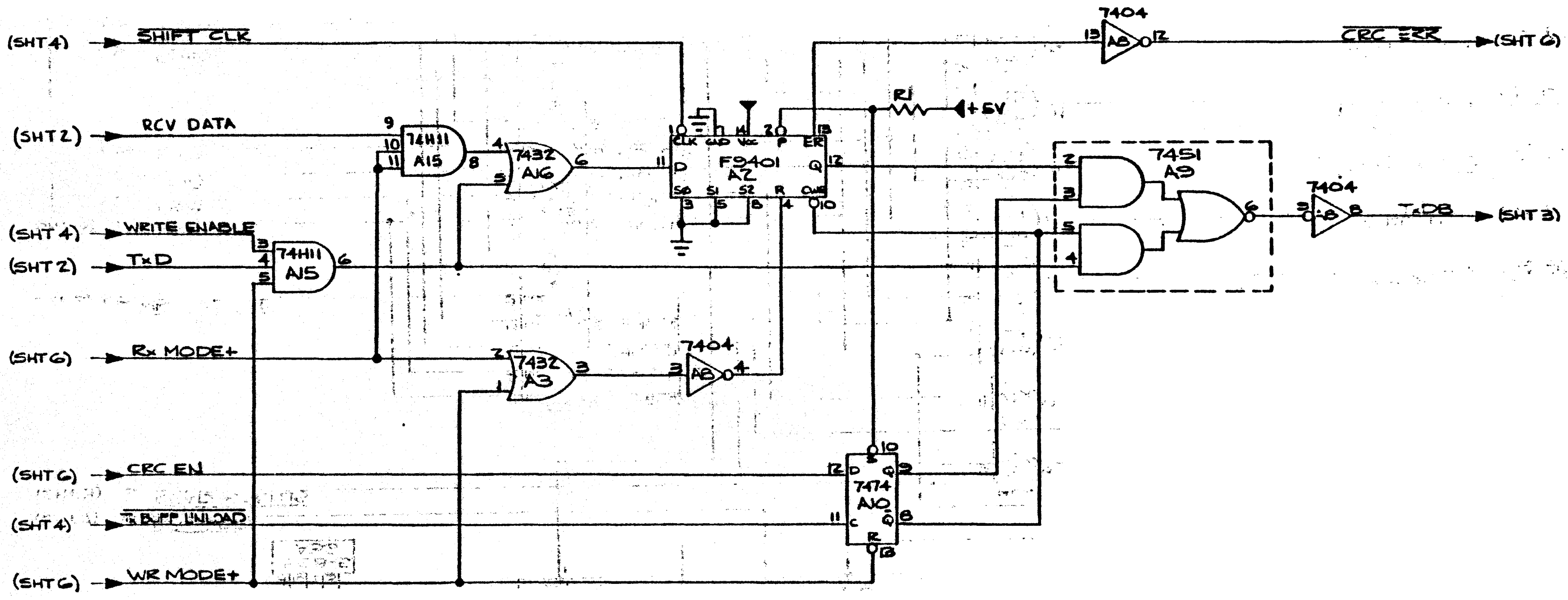
DO NOT SCALE DRAW

SHEET 6 OF 7

BISHOP GRAPHICS/ACC
REORDER NO. A6719

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	

M



FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	Zilog
APPROVALS | DATE DRAWN Mclu 4-15-76 CHECKED	CONFIDENTIAL This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced or disclosed to third parties without the prior written consent of Zilog Incorporated
	SCALE NONE | SIZE C | DRAWING NO. 02-0004-01
	DO NOT SCALE DRAWING | SHEET 7 OF 7

LOGIC DIAGRAMS, BREAKPOINT

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
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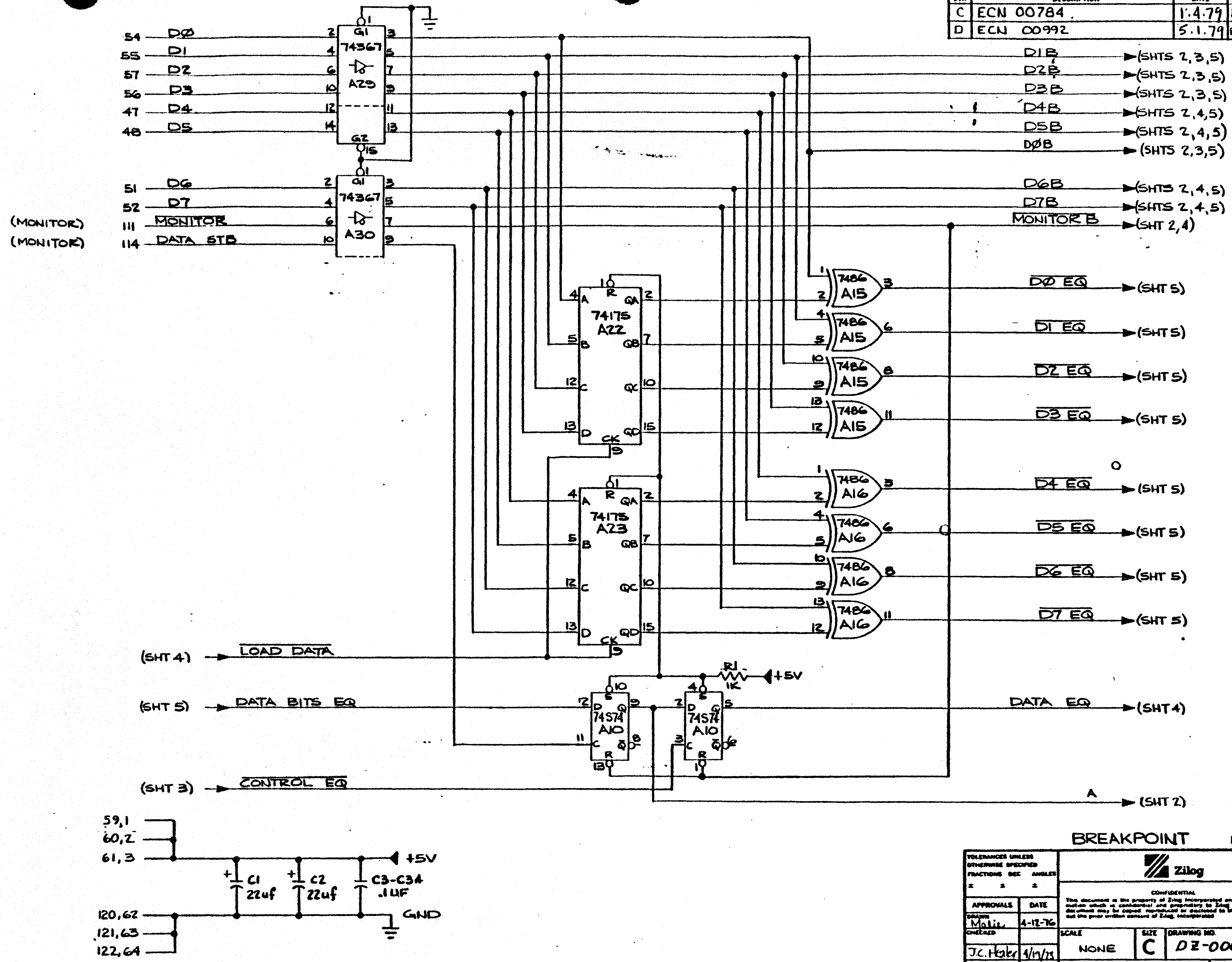
D	ECN 00992	5.1.79	RRD



BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

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APPROVALS	DATE
DRAWN Malic	4-12-76
CHECKED	
J.C. Haler	4/19/75
JCH	7/21/77

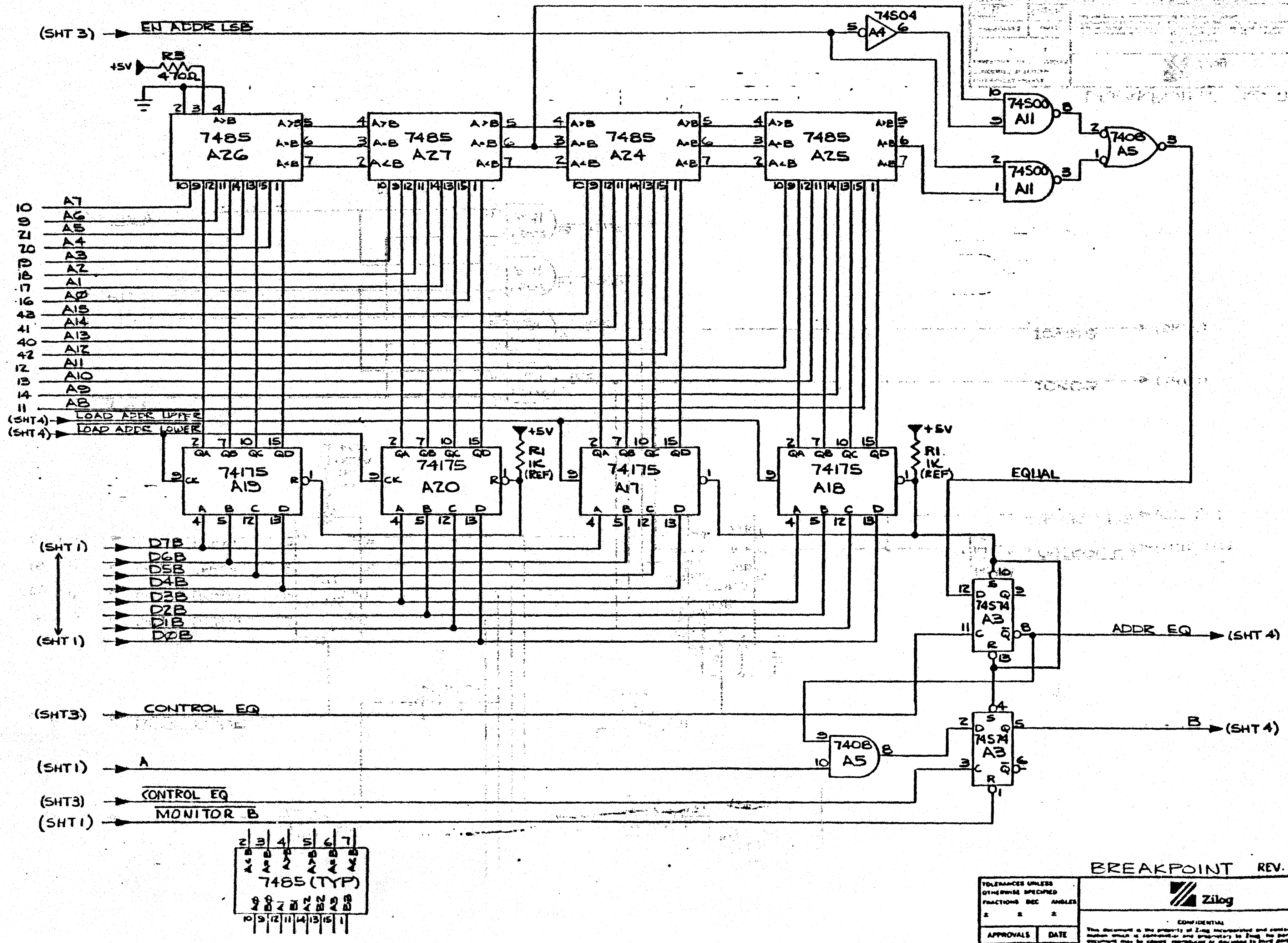
SCALE	SIZE	DRAWING NO.
NONE	C	DZ-0003-02

DO NOT SCALE DRAWING

SHEET 1 OF 5

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-6710

LTR	DESCRIPTION	DATE	APPROVED
D	SEE SHT. 1	5-1-79	KRD



BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

APPROVALS	DATE
DRAWN	4-12-76
CHECKED	
π Hata	4/13/78

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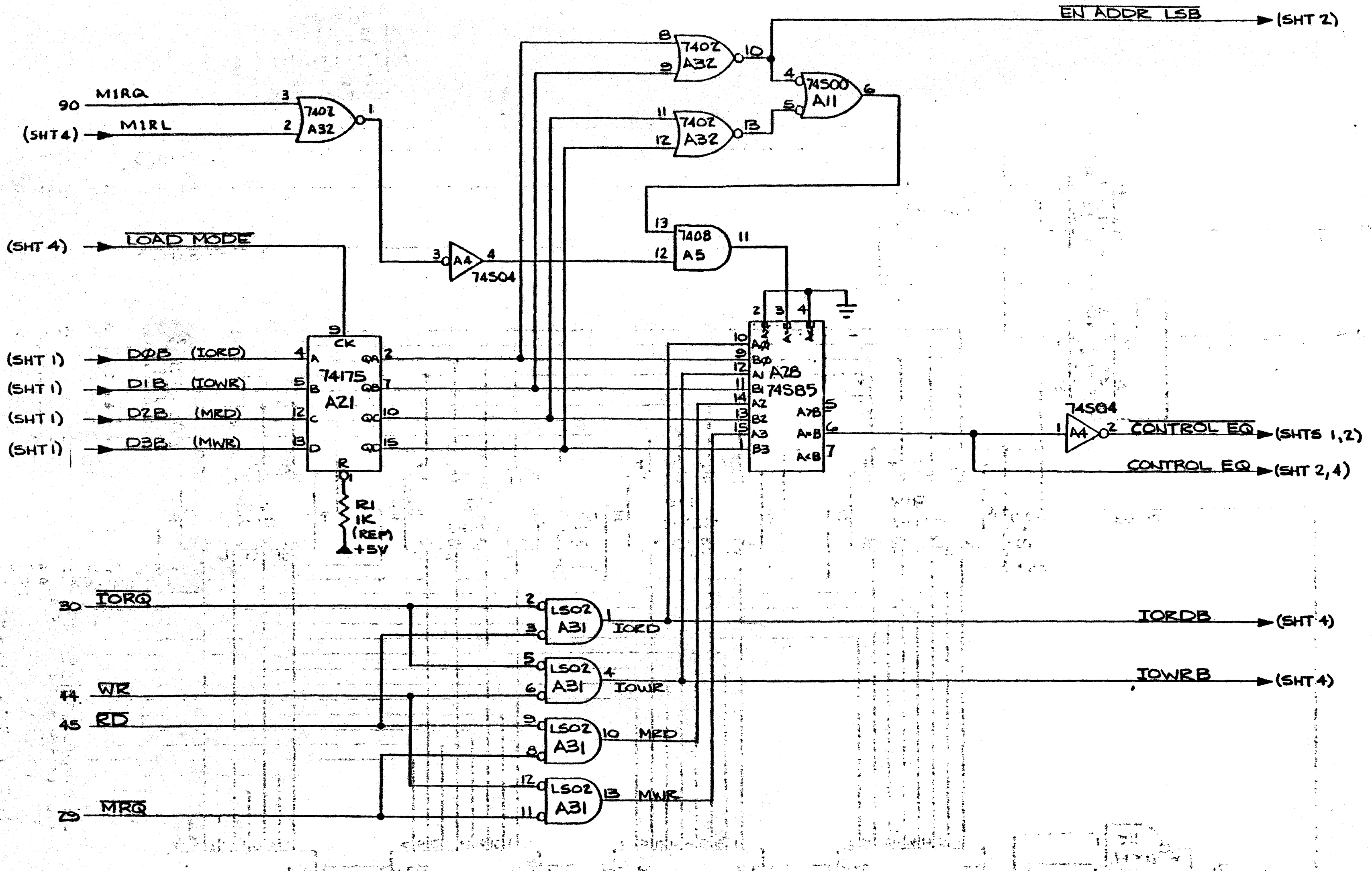
SCALE NONE SIZE C DRAWING NO DZ-0003-C2

DO NOT SCALE D

SHEET 2 OF 5

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	SEE SHT. 1	5.1.79	RRD



BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

Zilog

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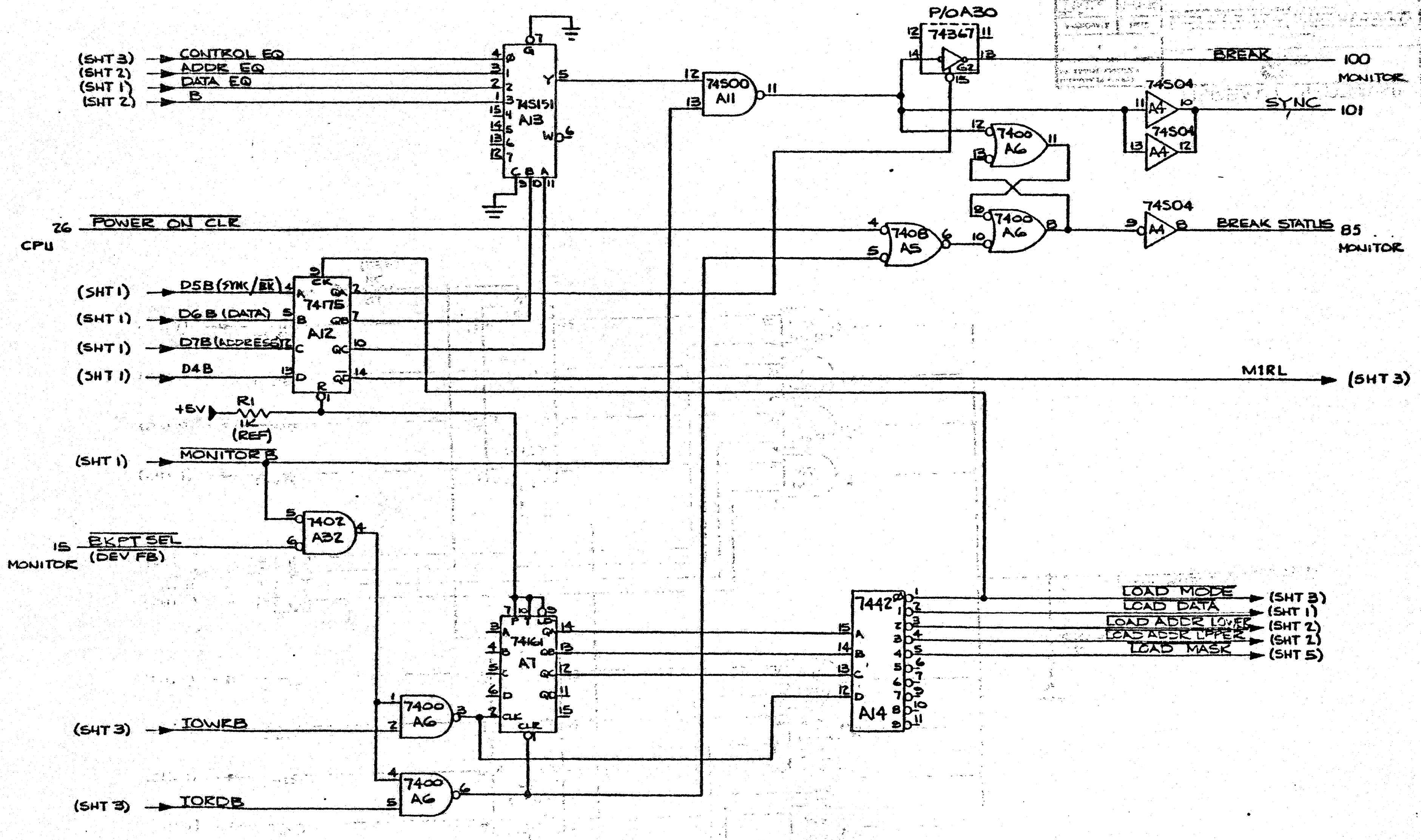
APPROVALS	DATE
DRAWN Malis	4-12-76
CHECKED	
JC Haber	1/19/78
JCH	7/31/77

SCALE	SIZE	DRAWING NO.
NONE	C	DZ-0003-02

DO NOT SCALE DRAWING

SHEET 3 OF 5

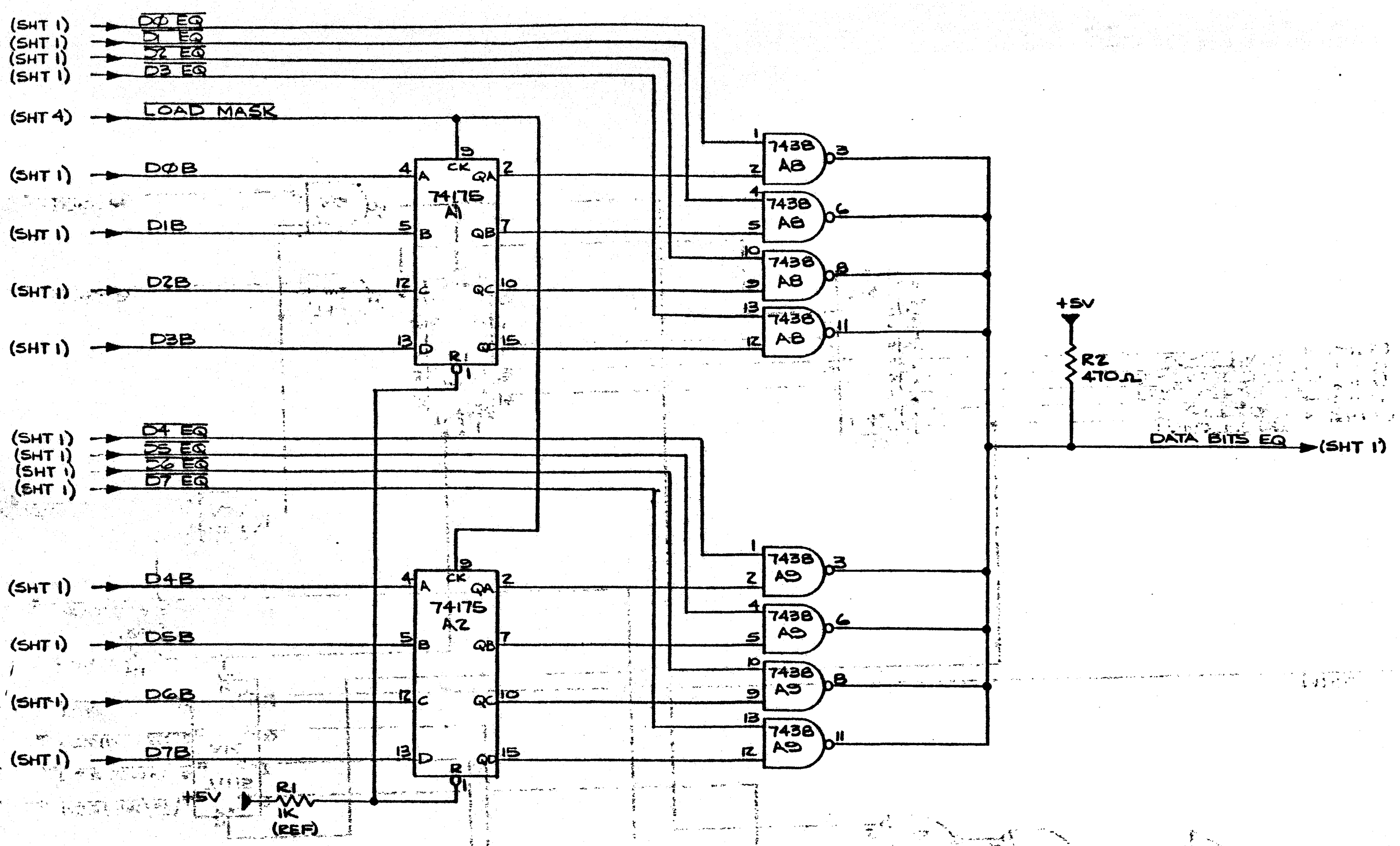
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	SEE SHT. 1	5.1.79	RRD



BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		Zilog		
APPROVALS	DATE	CONFIDENTIAL		
DRAWN	n-12-76			
CHECKED		SCALE NONE	SIZE C	DRAWING NO DZ-0003-02
TC Healer	4/13/[illegible]			
Z[illegible]	[illegible]	DO NOT SCALE DRA[illegible]		SHEET 4 OF 5

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	SEE SHT. 1	5.1.79	RRD

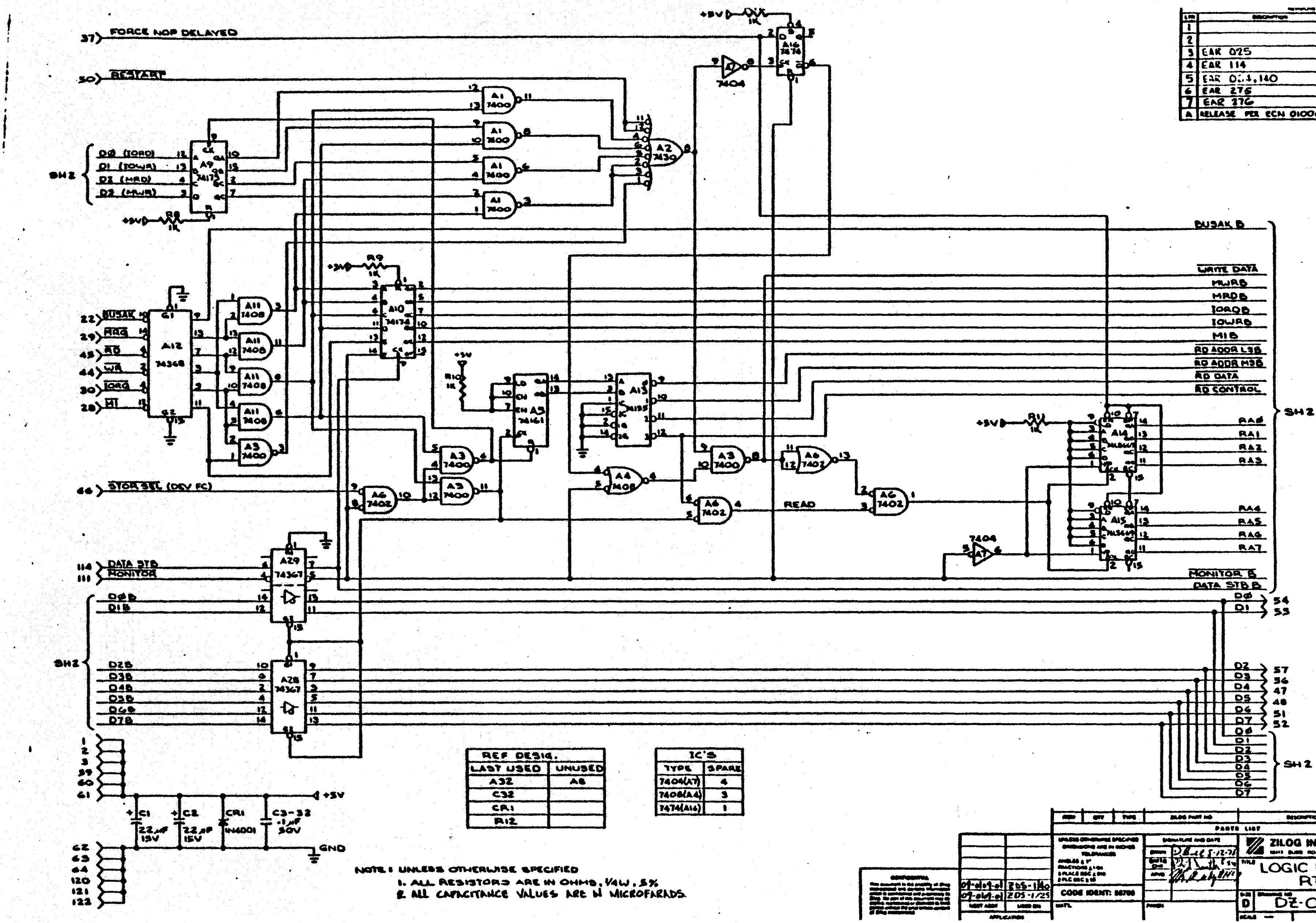


BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	Zilog
	CONFIDENTIAL This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced or disclosed to third parties without the prior written consent of Zilog Incorporated.

APPROVALS	DATE	SCALE	SIZE	DRAWING NO.
DRAWN Malin	4-13-76			
CHECKED		NONE	C	DZ-0003-02
JC Healer	4/19/78			
JZH	7/5/77	DO NOT SCALE DRAWING		SHEET 5 OF 5

LOGIC DIAGRAMS, RTSM2



LTR	DESCRIPTION	DATE	APPROVED
1			
2			
3	EAR 025	9.1.78	
4	EAR 114	9.1.78	
5	EAR 0:4,140	9.1.78	
6	EAR 275	10.9.78	
7	EAR 276	10.16.78	
A	RELEASE PER ECN 01006	4.17.79	

REF DESIG.	
LAST USED	UNUSED
A32	A8
C32	
CR1	
R12	

IC'S	
TYPE	SPARE
7404(A7)	4
7408(A4)	3
7474(A16)	1

NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

PARTS LIST

NEXT ASSY	USED ON
09-0109-01	ZDS-1/40
09-0109-01	ZDS-1/25

APPLICATION

CODE IDENT: [illegible]

DRAWN DB 5-12-78

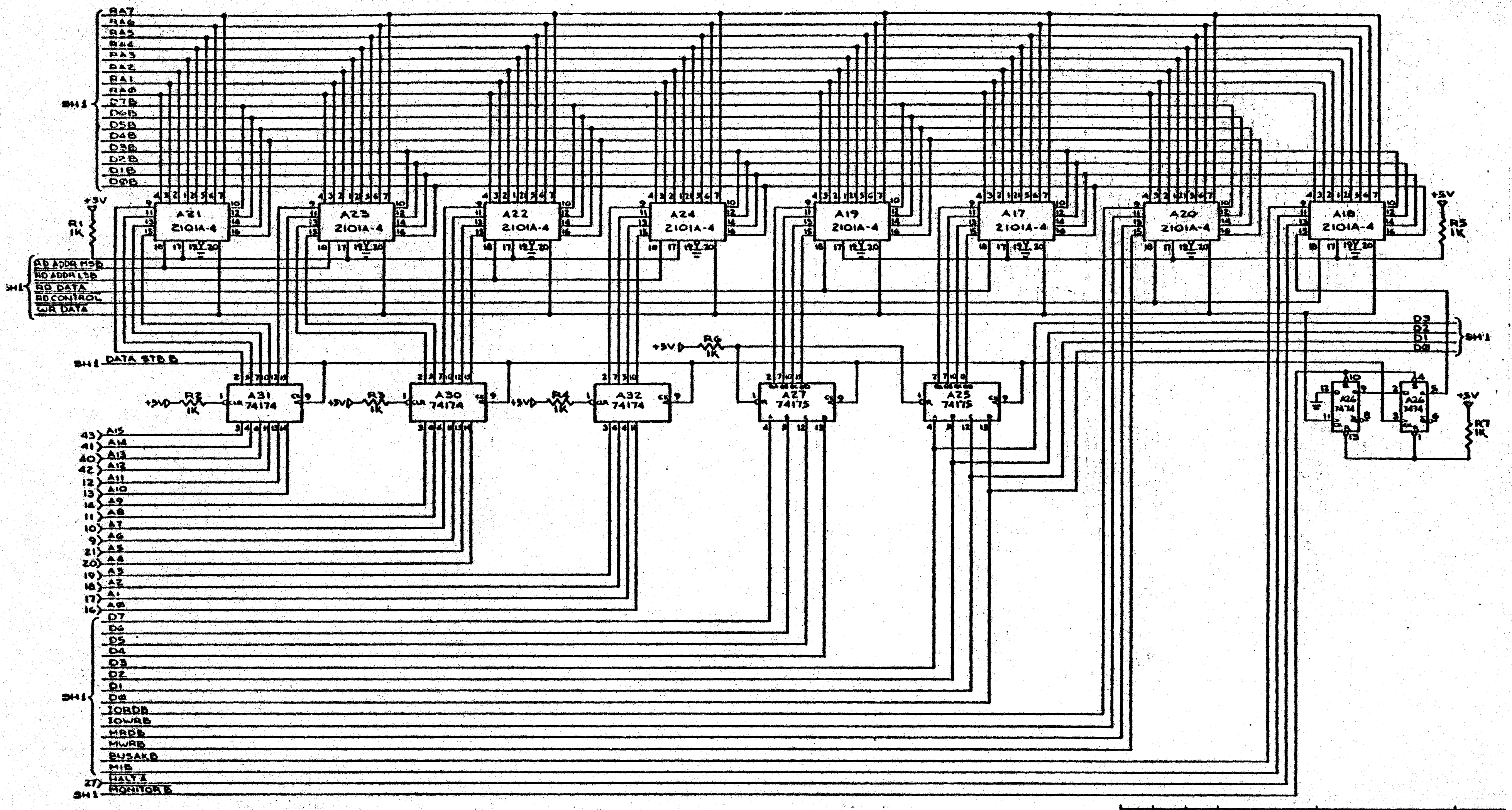
ZILOG INC.

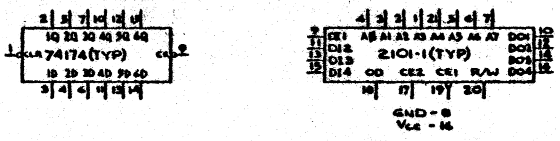
TITLE LOGIC DIAGRAM RTSM2

SIZE D DRAWING NO DZ-0109-01 REV A

SCALE — SHEET 1 OF 2

LTR	DESCRIPTION	DATE	APPROVED
A	SEE SH. 1	4·17·79	MO





ZDS-1/40	
ZDS-1/25	
NEXT ASSY	USED ON
APPLICATION	

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .03

CODE IDENT: 56708

MATL

SIGNATURE AND DATE
DRAWN
DRFTG CHK
APVD

FINISH

ZILOG INC.
10411 BUBB ROAD CUPERTINO, CALIFORNIA 95014

TITLE
LOGIC DIAGRAM RTSM2

SIZE D
DRAWING NO DZ-0109-01
REV A
SCALE —
SHEET 2 OF 2

Zilog

DOCUMENT CHANGE NOTICE

DATE: 12-07-79

DCN NUMBER: E3-3018-03, Rev. A

PUBLICATION NUMBER: 03-3018-03

TITLE: ZDS-1/40 HARDWARE REFERENCE MANUAL

PREVIOUS DCN's BY NUMBER: None

EFFECTIVE DATE: 12-07-79

This Document Change Notice provides change pages for the publication specified above. These change pages contain changes to the technical contents of the manual specified above, and will remain in effect unless specifically amended or superseded by another DCN, or merged into the manual by a publication revision. The following pages are to be treated as described.

Replace page D-22 in manual with change page attached.

Replace CONTENTS page of APPENDIX E with change page attached.

Replace page E-33 in manual with change page attached.

Replace Logic Diagram Set DZ-0099-03, Rev. A with DZ-0099-04, Rev. A

Changes to text are indicated by a vertical line in the right margin, opposite the changed text portion.

NOTE: Please file this DCN at the back of the manual to provide a record of changes.

PINOUT FOR 60K MEMORY BOARD - 09-0101-04 (cont.)

J08

PIN #	SIGNAL NAME
093	+12V.2
094	+12V.2
095	+12V.2
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	.
108	.
109	.
110	.
111	.
112	.
113	.
114	.
115	.
116	.
117	.
118	.
119	.
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR CPU BOARD - 09-0099-01 or 09-0099-04

J09

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	RCVR.OUT-
005	(SERIAL.OUT)
006	RCV.CLK
007	RCV.CLK.(XMIT.CLK)
008	SERIAL.IN
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	SERIAL.OUT
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	BUSAK-
023	8.PHI.(8X.SYSTEM.CLOCK)
024	PHI.(SYSTEM.CLOCK)
025	REFRESH-
026	POWER.ON.CLR-
027	HALT-
028	M1-
029	MRQ-
030	IORQ-
031	PS.3-
032	PS.2-
033	PS.1-
034	PS.0-
035	CD.3-
036	CD.2-
037	CD.1-
038	CD.0-
039	PG.15-.(MDIS-)
040	A13
041	A14
042	A12
043	A15
044	WR-
045	RD-
046	TY.HI.(MONITOR)

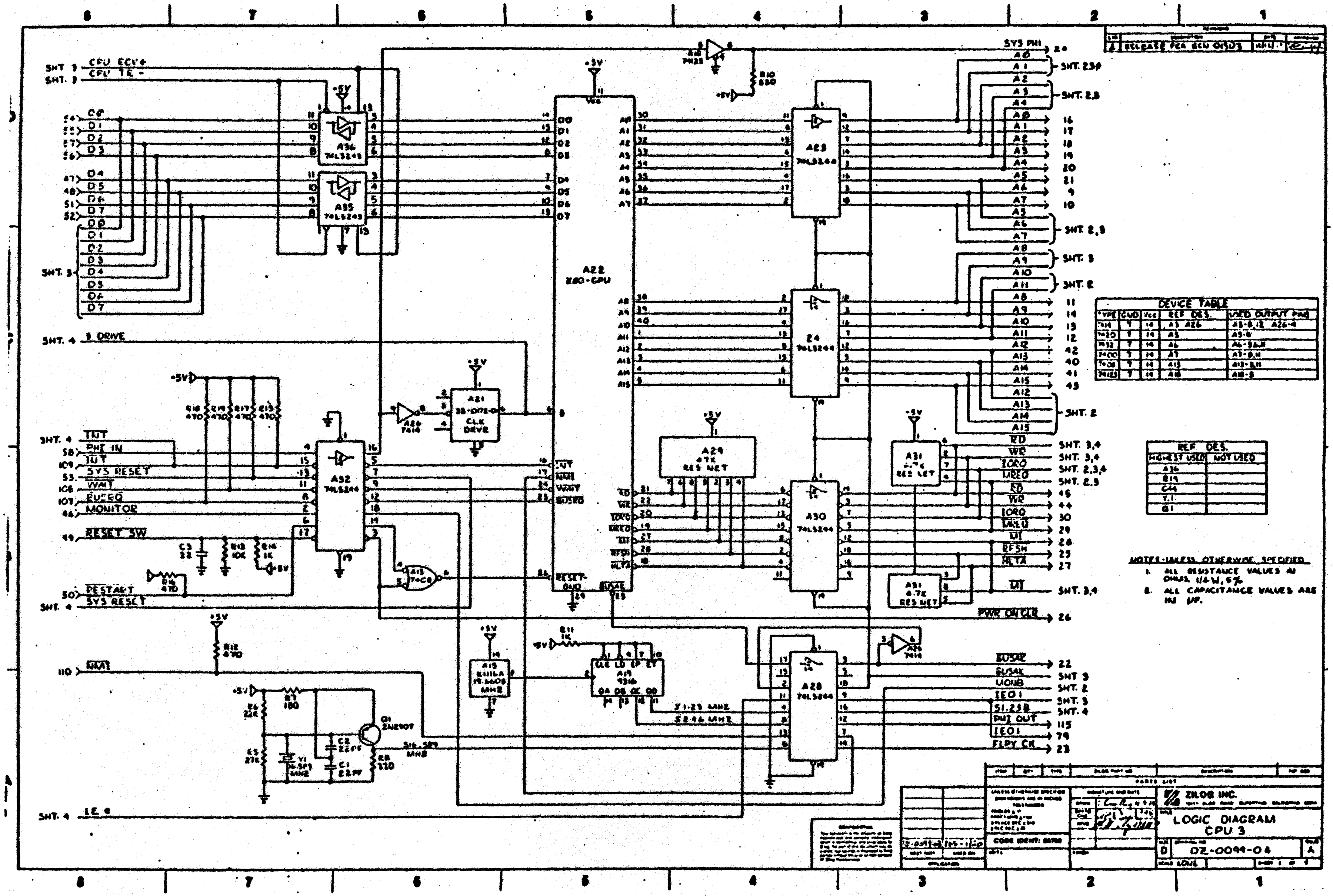
APPENDIX E

LOGIC DIAGRAMS

CONTENTS

LOGIC DIAGRAMS, CPU-3

(09-0099-04)



DEVICE TABLE				
TYPE	GND	Vcc	REF DES.	USED OUTPUT PINS
7414	7	14	A3 A26	A3-8,12 A26-4
7420	7	14	A5	A5-8
7432	7	14	A6	A6-3,6,11
7400	7	14	A7	A7-8,11
7400	7	14	A13	A13-3,11
74125	7	14	A18	A18-3

REF DES.	
HIGHEST USED	NOT USED
A36	
R19	
C44	
Y.1.	
Q1	

NOTES-UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES IN OHMS, 1/4W, 5%
2. ALL CAPACITANCE VALUES ARE IN µF.

PARTS LIST

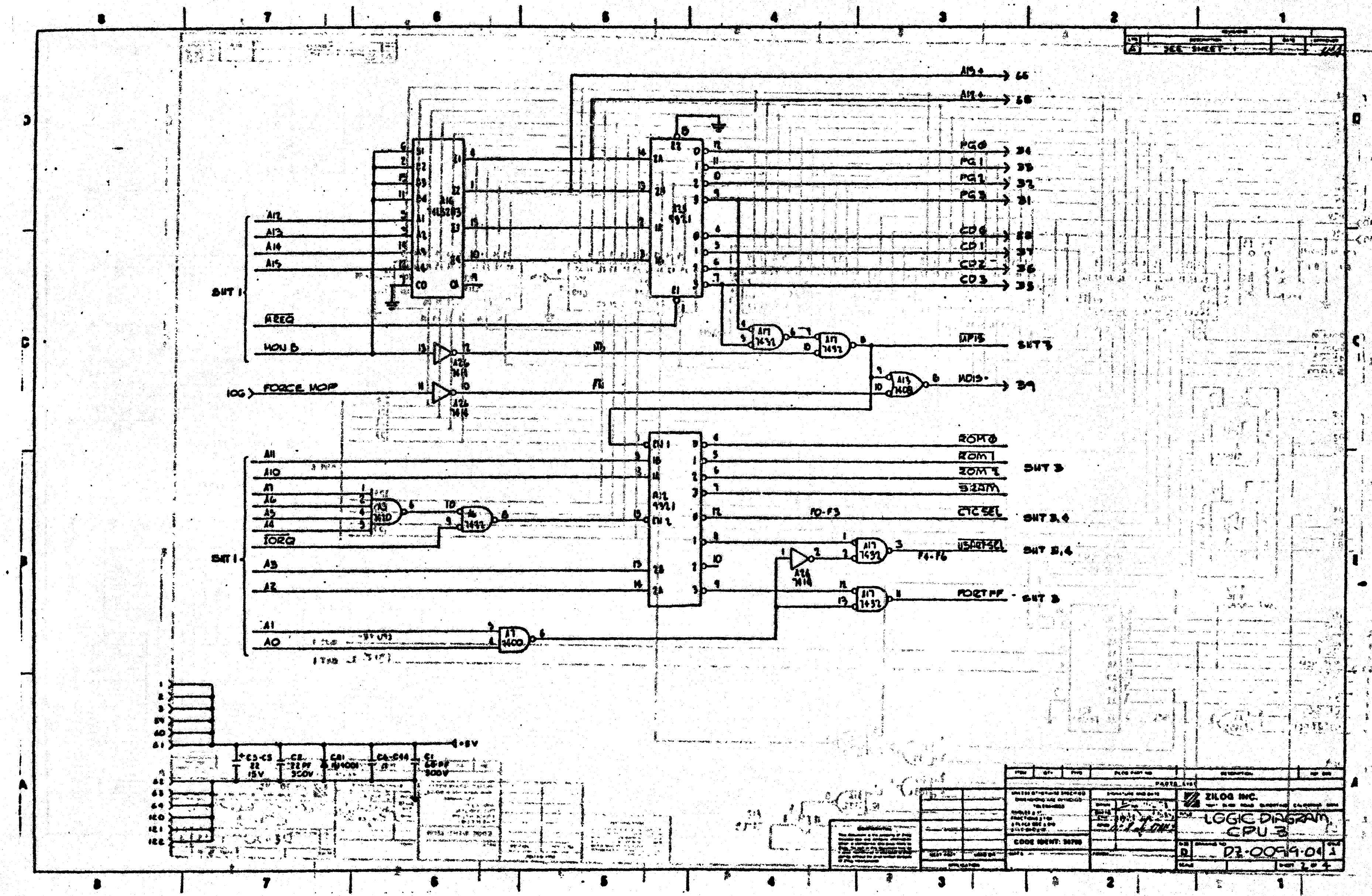
CODE IDENT: 56708

ZILOG INC.

LOGIC DIAGRAM
CPU 3

D DZ-0099-04 A

SCALE NONE



PARTS LIST

ZILOG INC.

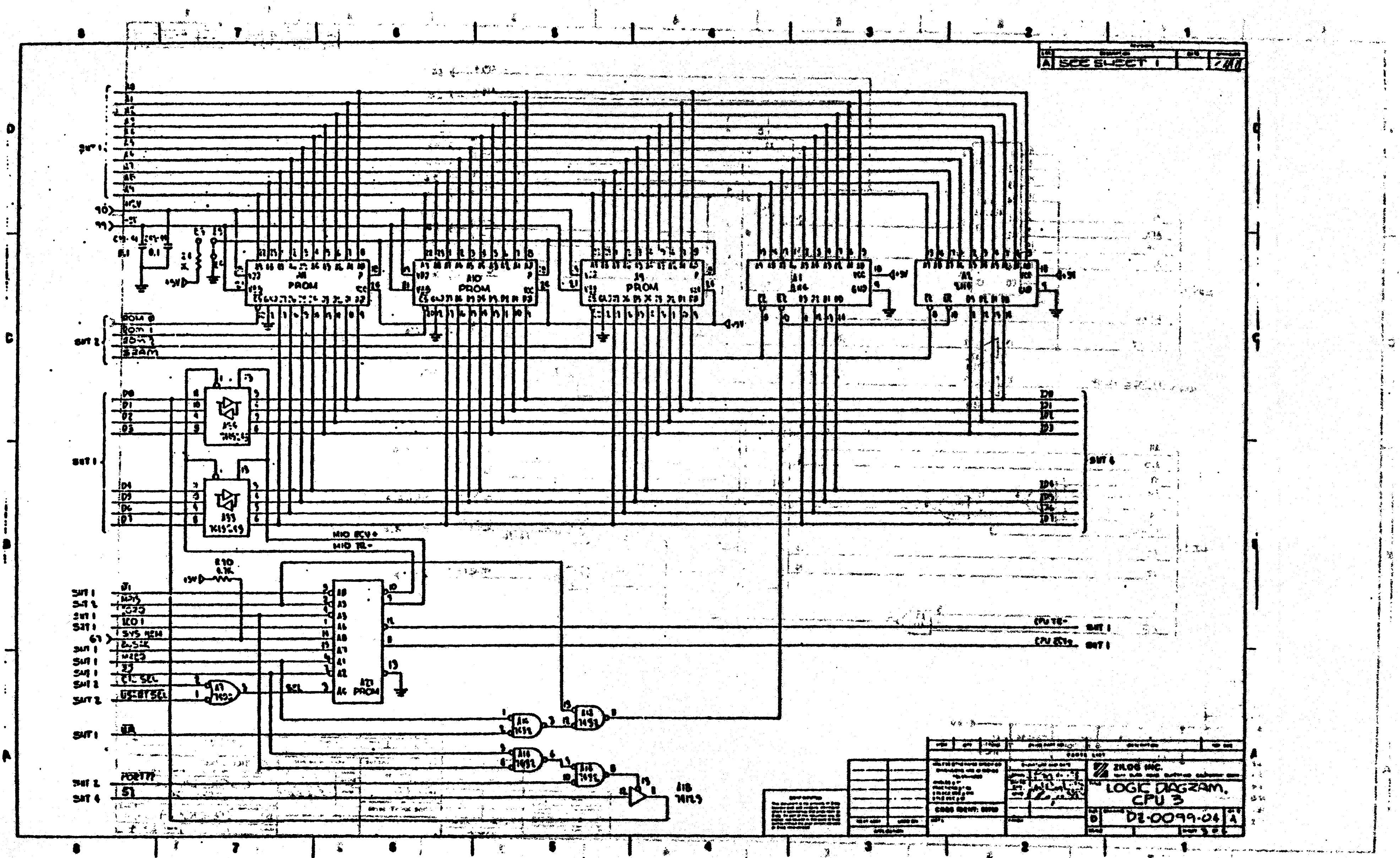
CODE IDENT: 30700

LOGIC DIAGRAM, CPU 3

D

D3-0099-01

SHEET 2 OF 4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A0
A1
A2
A3
A4
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A7
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A9
+12V
-5V
90
99
SHT 1
A8
PROM
A10
PROM
A9
PROM
+5V
SHT 2
ROM 0
ROM 1
ROM 2
SRAM
D0
D1
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A36
74LS245
A35
74LS245
SHT 1
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D6
D7
SHT 4
MIO RCV+
MIO TR-
R10
4.7K
+5V
SHT 1
ST1
SHT 2
MPTS
SHT 1
CPZ3
SHT 1
IEO 1
SYS MEM
67
BUS RQ
SHT 1
MREQ
SHT 1
ST3
SHT 1
CTL SEL
SHT 2
USART SEL
SHT 2
A7
74S32
SEL
A21
PROM
CPU TR-
SHT 1
CPU RCV+
SHT 1
A16
74S32
A16
74S32
A16
74S32
A16
74S32
SHT 1
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PORT??
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ST
SHT 4
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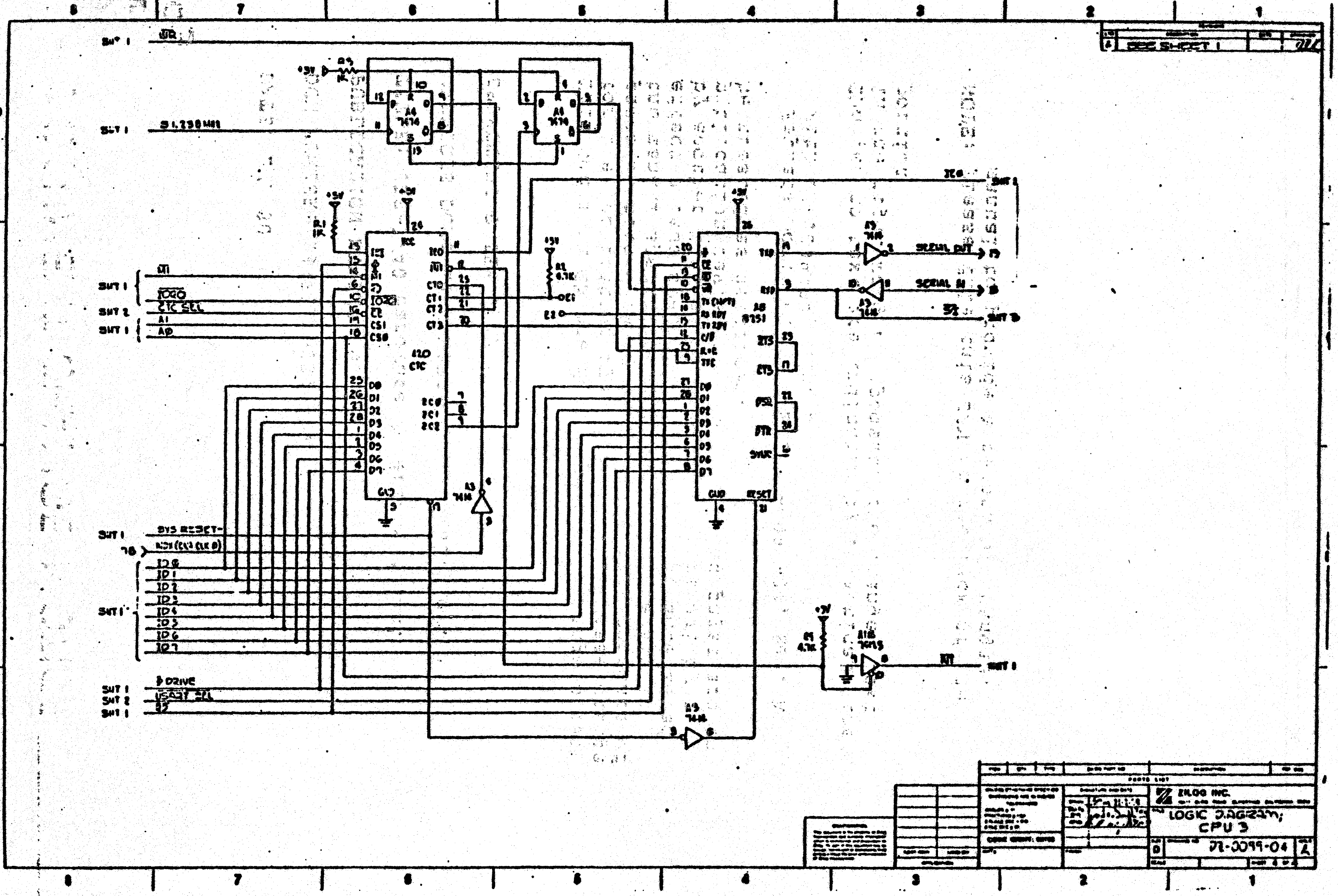
CAGE IDENT: 50150
ZILOG INC.
LOGIC DIAGRAM,
CPU 3
D
DZ-0099-04
A



PARTS LIST

ZILOG INC.

LOGIC DIAGRAM;
CPU 3

D

71-0099-04

A

Zilog

DOCUMENT CHANGE NOTICE

DATE: 2/1/80

DCN NUMBER: E3-3018-03, Rev. B

PUBLICATION NUMBER: 03-3018-03

TITLE: ZDS-1/40 Hardware Reference Manual

PREVIOUS DCNs BY NUMBER: E3-3018-03, Rev. A

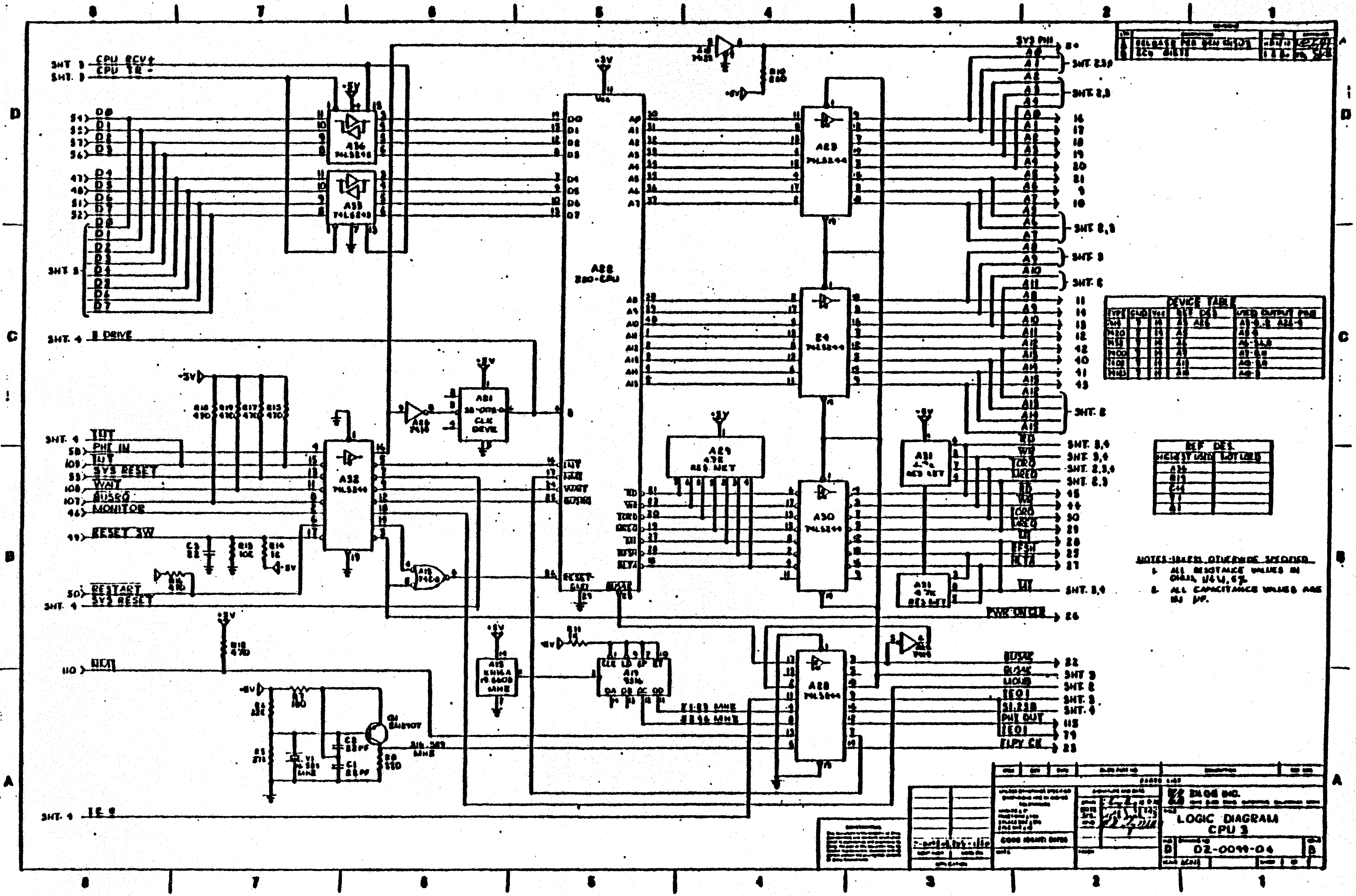
EFFECTIVE DATE: 2/1/80

This Document Change Notice provides change pages for the publication specified above. These change pages contain changes to the technical contents of the manual specified above, and will remain in effect unless specifically amended or superseded by another DCN, or merged into the manual by a publication revision. The following pages are to be treated as described.

Replace Logic Diagram Set DZ-0099-04, Rev. A with DZ-0099-04, Rev. B

Changes to text are indicated by a vertical line in the right margin, opposite the changed text portion.

NOTE: Please file this DCN at the back of the manual to provide a record of changes.



DEVICE TABLE				
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[illegible]	7	14	A13 A26	[illegible]
[illegible]	7	14	A2	[illegible]
[illegible]	7	14	A6	[illegible]
[illegible]	7	14	A7	[illegible]
[illegible]	7	14	A11	[illegible]
[illegible]	7	14	A8	[illegible]

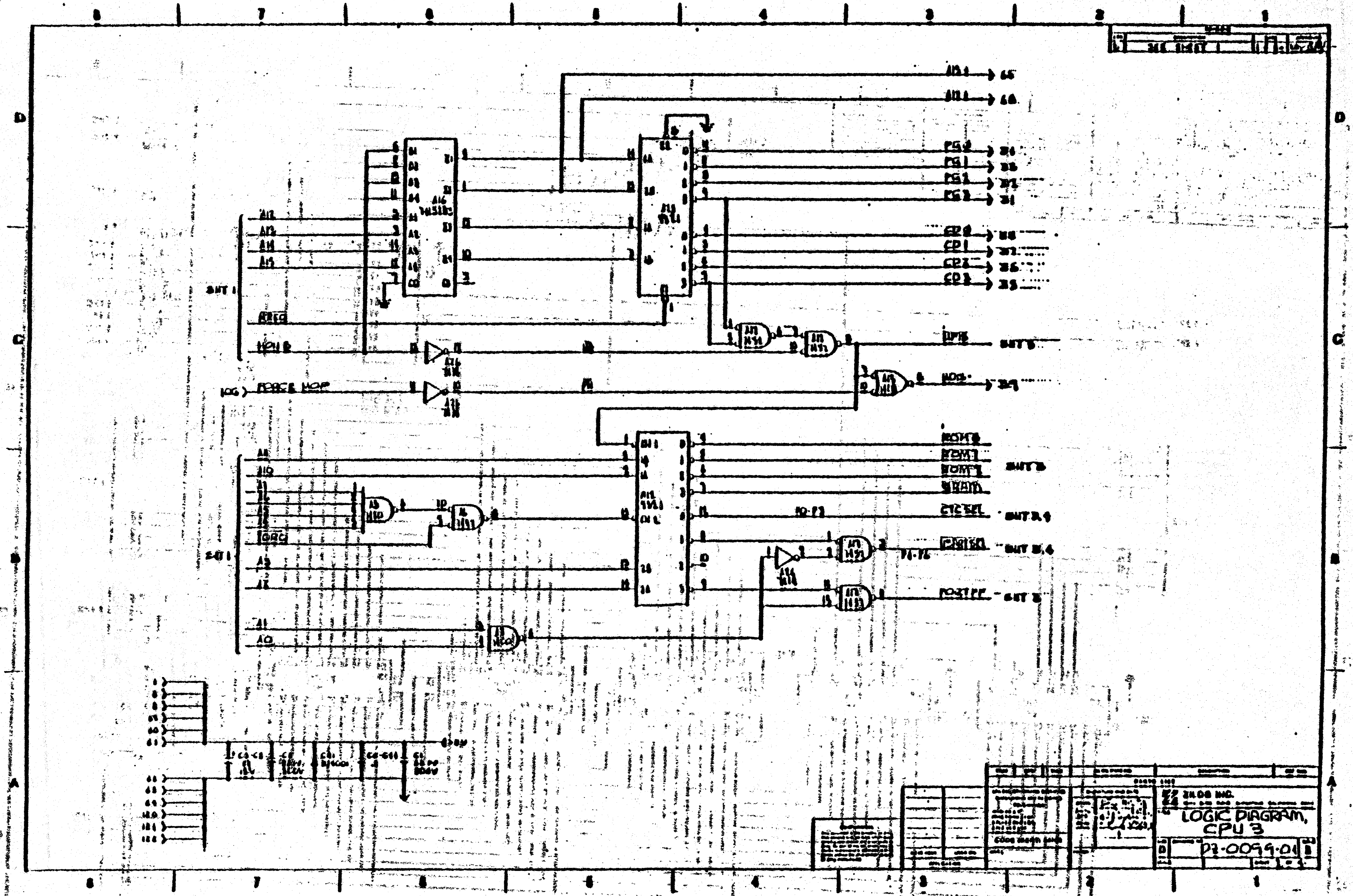
REF DES.	
HIGHEST USED	NOT USED
A36	
R13	
C4	
Y1	
Q1	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES IN OHMS, 1/4 W, 5%.
2. ALL CAPACITANCE VALUES ARE IN µF.

ZILOG INC.

LOGIC DIAGRAM
CPU 3

D
D2-0099-04
D

8
7
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D
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A13
A14
A15
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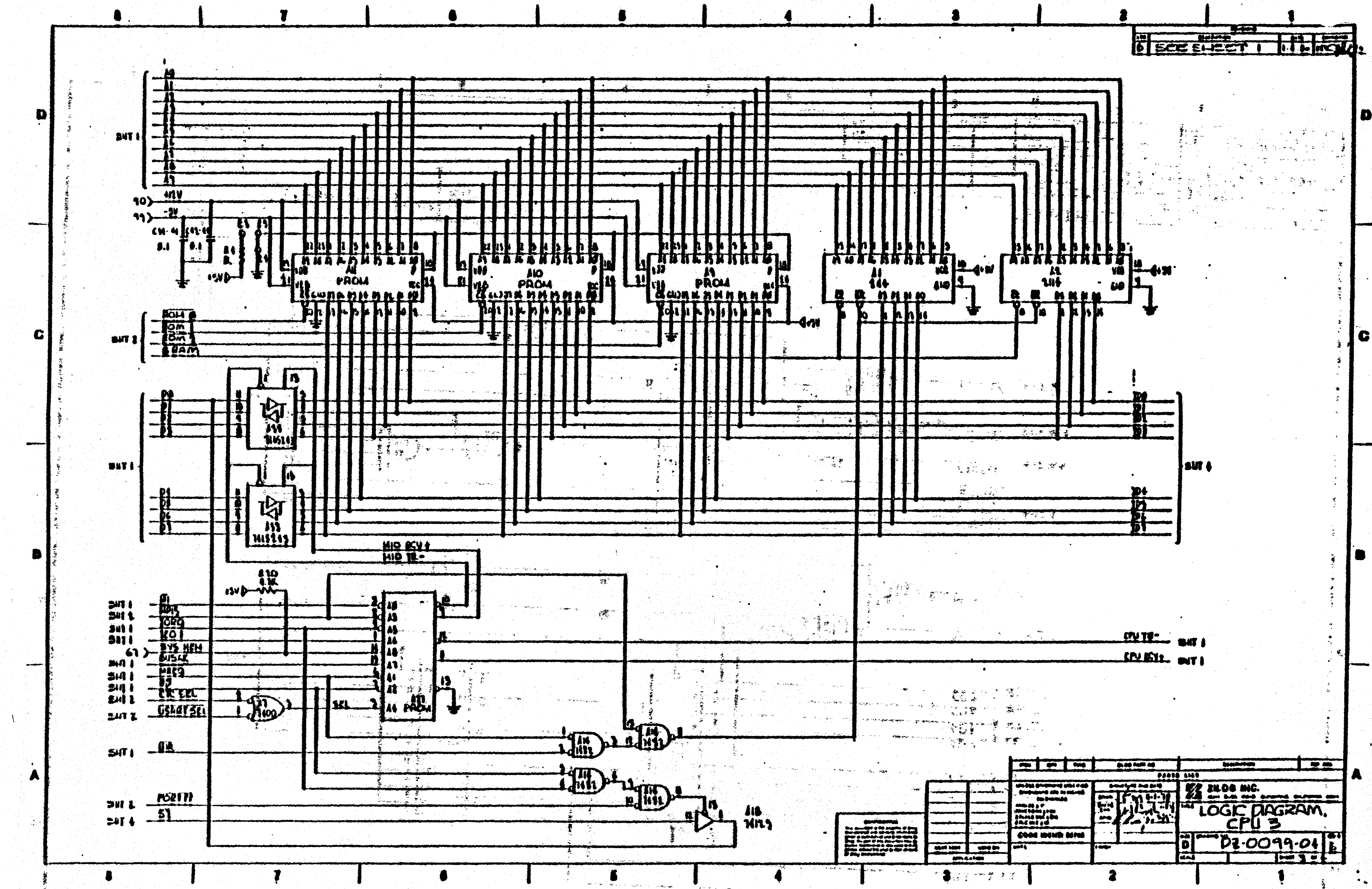
74LS138
PG0
PG1
PG2
PG3
CP0
CP1
CP2
CP3
FORCE HOP
LOG
SHT 5
SHT 3
A8
A9
A10
A5
A4
A3
A2
A1
A0
ROM0
ROM1
ROM2
SRAM
CTC SEL
SHT 3,4
SHT 3,4
POSTPF
SHT 3
ZILOG INC.
LOGIC DIAGRAM,
CPU 3
03-0099-01

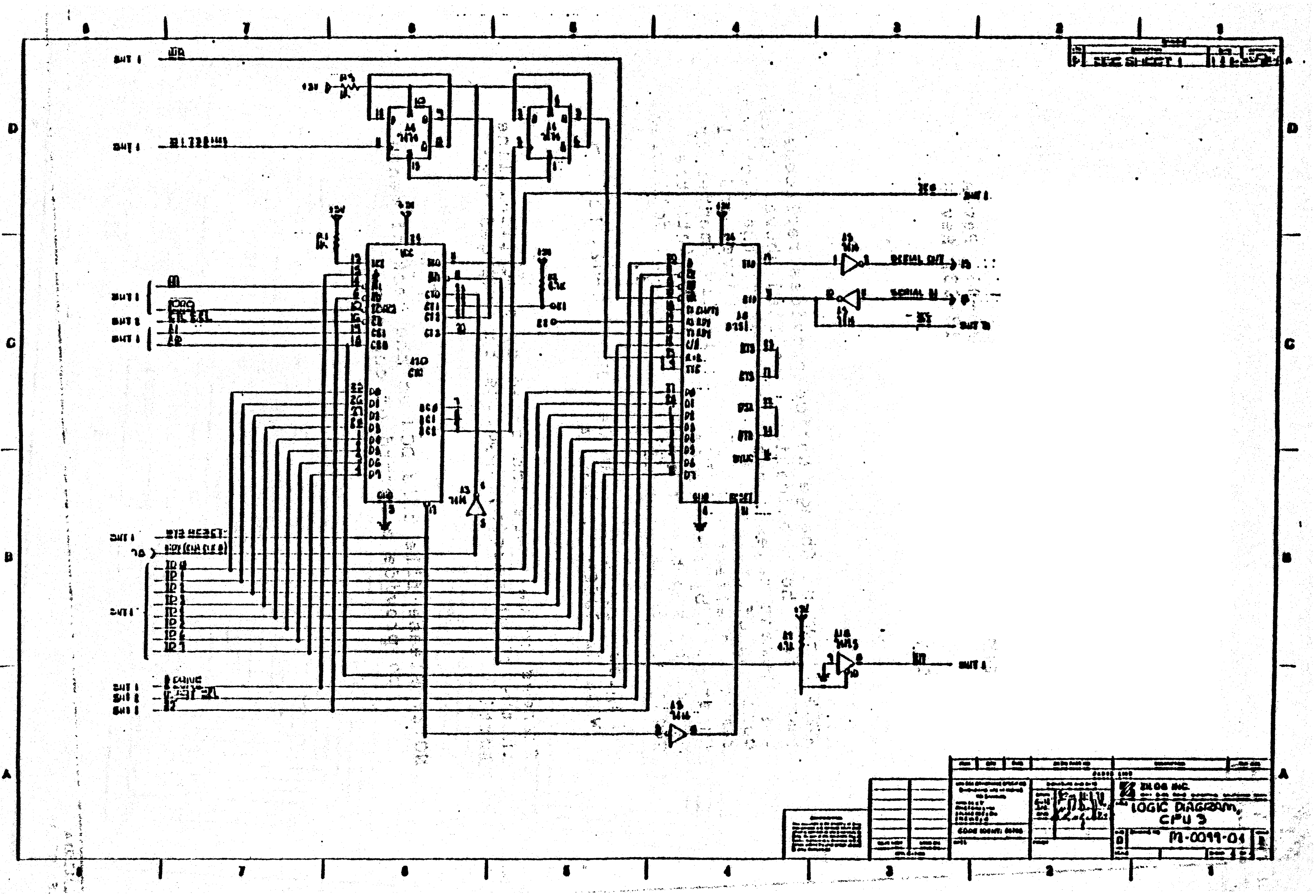


D | SEE SHEET 1

ZILOG INC.

LOGIC DIAGRAM, CPU 3

D | DZ-0099-04

SEE SHEET 1
SHT 1
SERIAL OUT
SERIAL IN
VCC
D0
D1
D2
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D4
D5
D6
D7
GND
RESET
ZILOG INC.
LOGIC DIAGRAM,
CPU 3
D
M-0099-04
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B
C
D
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1

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DOCUMENT CHANGE NOTICE

DATE: 04-03-80

DCN NUMBER: E3-3018-03, Rev. C

PUBLICATION NUMBER: 03-3018-03

TITLE: ZDS-1/40 Hardware Reference Manual

PREVIOUS DCNs BY NUMBER: E3-3018-03, Rev.A
E3-3018-03, Rev.B

EFFECTIVE DATE: 04-03-80

This Document Change Notice provides replacement pages for the publication specified above. These replacement pages contain changes to the technical contents of the manual specified above, and will remain in effect unless specifically amended or superseded by another DCN, or merged into the manual by a publication revision. The following pages are to be treated as described.

Replace Logic Diagram Set DZ-0056-02, Rev. D with DZ-0056-03, Rev. A.

Changes to text are indicated by a vertical line in the right margin, opposite the changed text portion.

NOTE: Please file this DCN at the back of manual to provide a record of changes.

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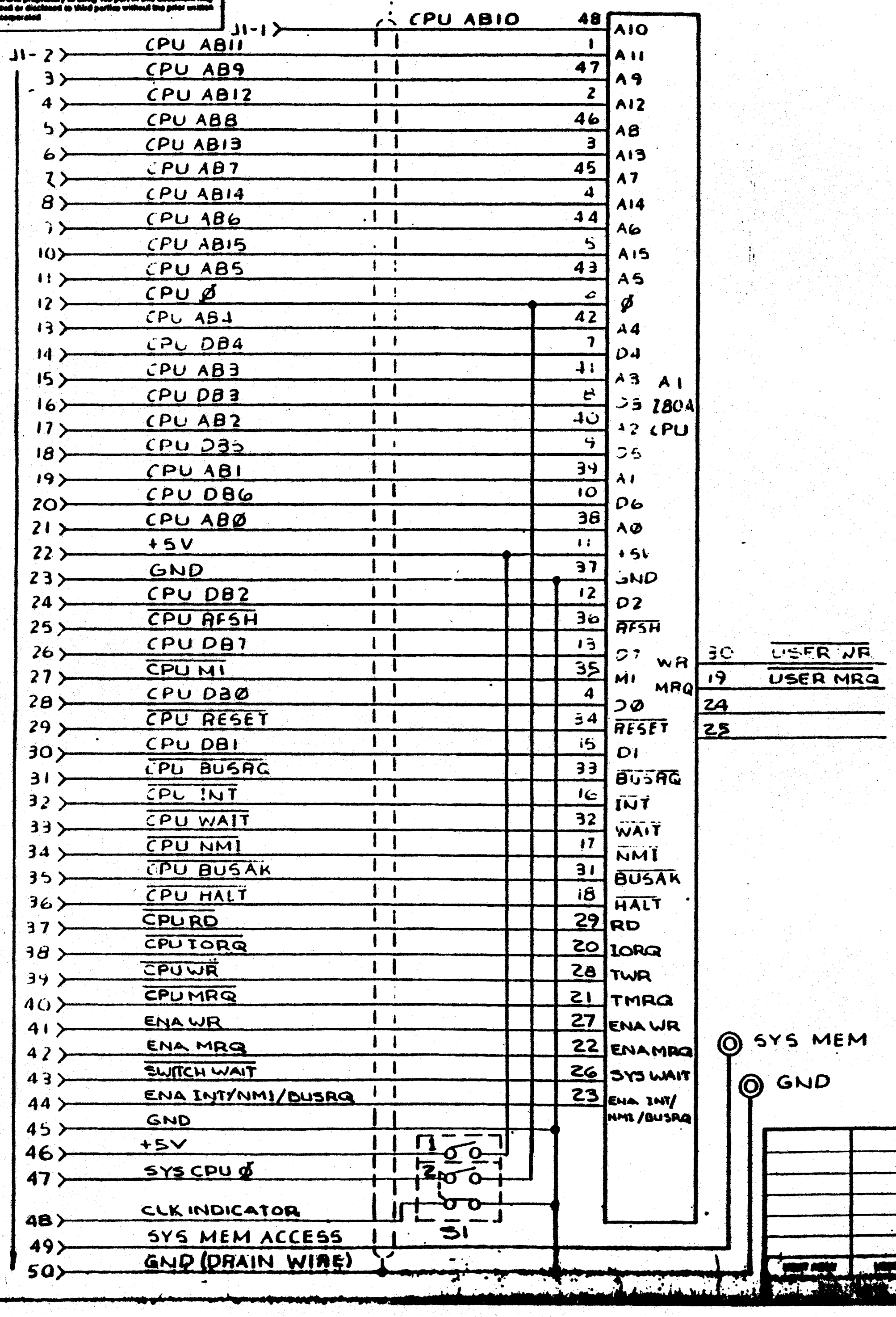
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECN 01575	2-14-80	[illegible]



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02	SIGNATURE AND DATE	
			DRAWN	P. MILES 10-14-77
			DRFTG CHK	2-14-80
			APVD	780606
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ZILOG INC.
10460 BUBB ROAD. CUPERTINO, CALIFORNIA 95014

TITLE LOGIC DIAGRAM
EMULATOR

SIZE	DRAWING NO	ISSUE
C	DZ-0056-03	A

SCALE NONE SHEET 1 OF 1

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