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Lyman et al.

[11] **4,047,248**

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[54] **LINKED LIST DATA ENCODING METHOD AND CONTROL APPARATUS FOR A VISUAL DISPLAY**

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[73] Assignee: **Hewlett-Packard Company**, Palo Alto, Calif.

[*] Notice: The portion of the term of this patent subsequent to July 27, 1993, has been disclaimed.

[21] Appl. No.: **665,829**

[22] Filed: **Mar. 11, 1976**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 508,600, Sept. 23, 1974, Pat. No. 3,972,026.

[51] **Int. Cl.**[2] **G06F 3/14**

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** 340/172.5

[56] **References Cited**

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Primary Examiner—Raulfe B. Zache

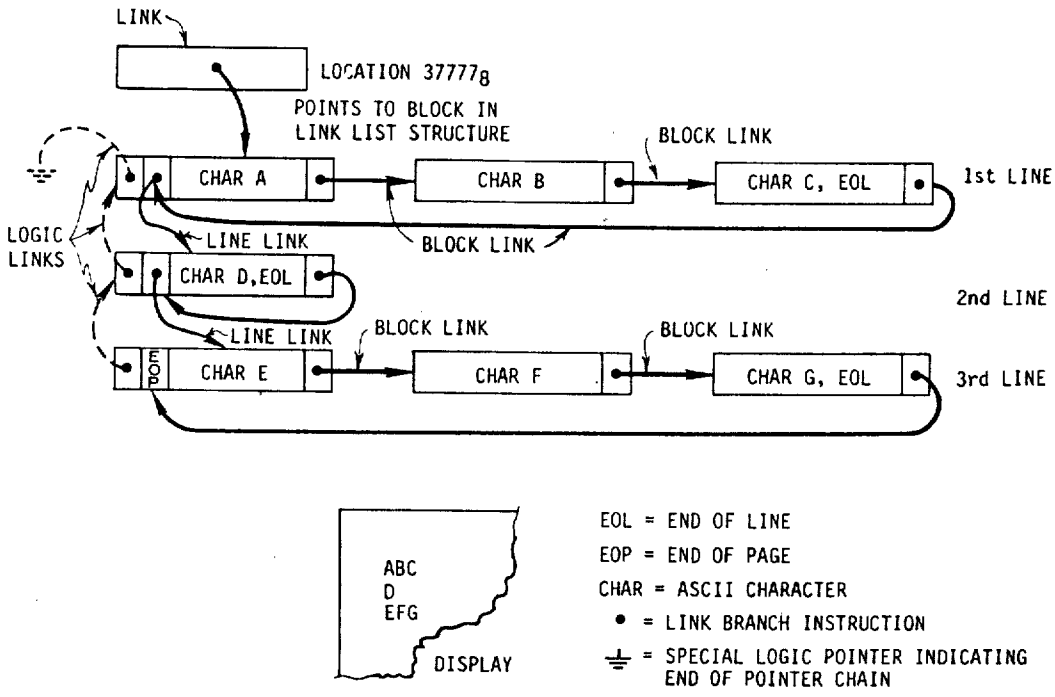
Attorney, Agent, or Firm—Theodore Scott Park

[57] **ABSTRACT**

Data is configured in 8-bit control characters and 8-bit data characters and stored in a random access memory as a linked list structure. Control apparatus accesses the data stored in the memory in 16-character blocks and identifies the accessed information as representing figures to be displayed, video enhancement features, or program execution path changes. Each 2-character link provides an address pointer to the next 16-character block of data and control information. The first character block of a line of displayable figures has links to the previous displayable line and the next line of characters to be displayed.

The control apparatus combines internal hardware functions and the linked list encoding structure as implemented by program logic to provide display and control character identification, data access address modification, video display enhancement and selection of alternate character sets.

54 Claims, 12 Drawing Figures



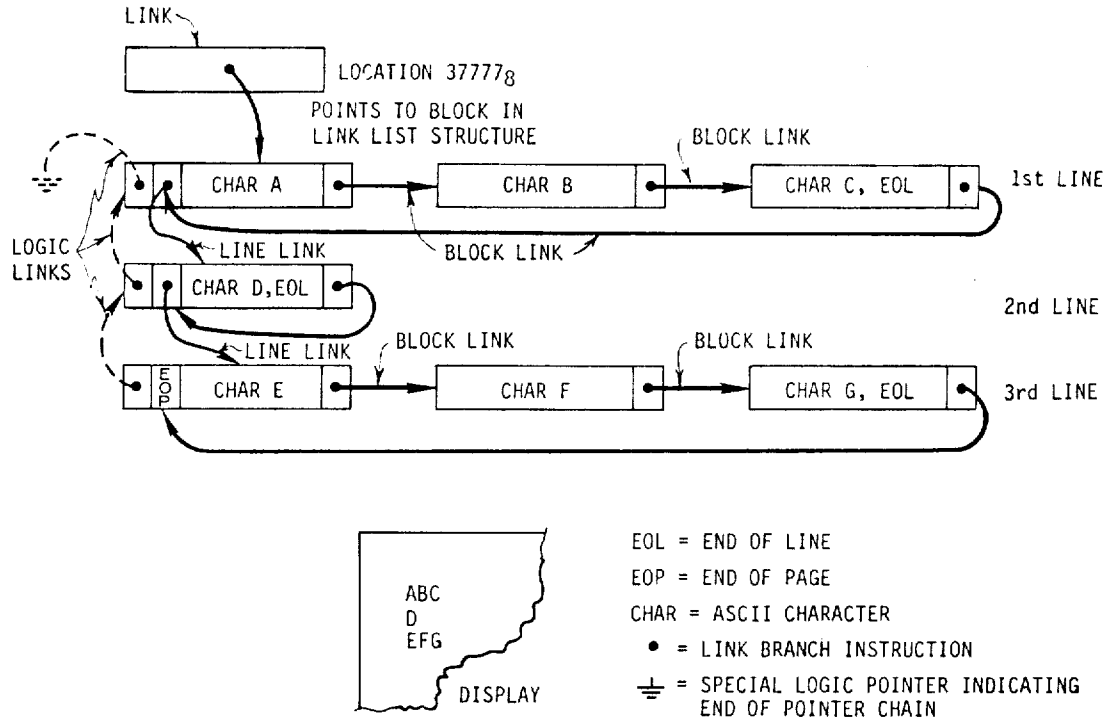


FIGURE 5

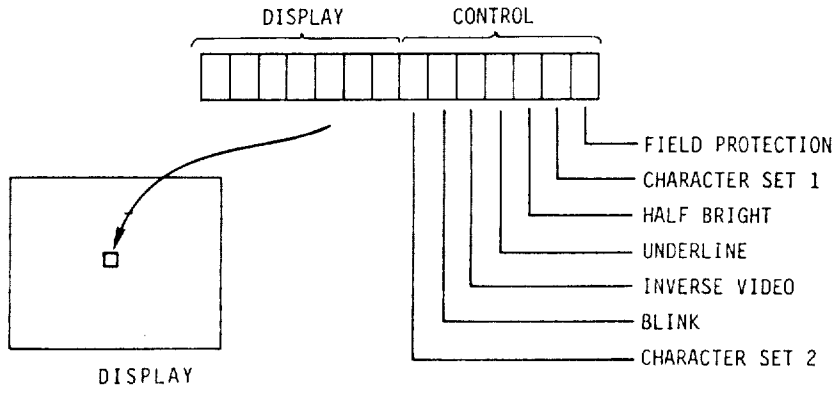


FIGURE 1

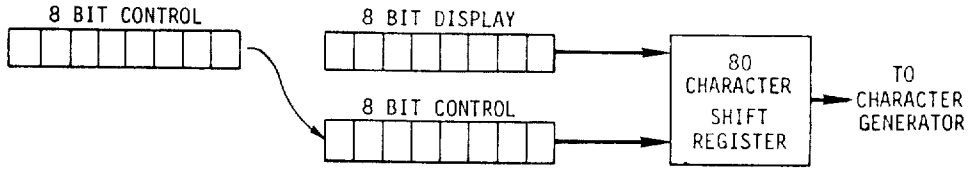


FIGURE 2A

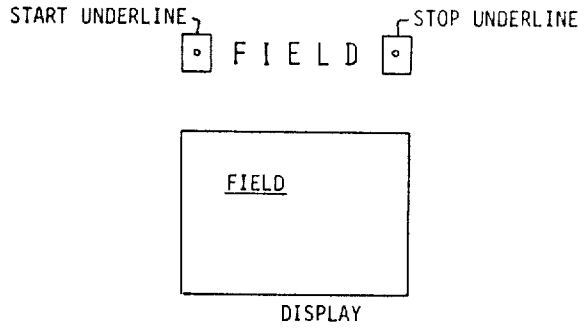


FIGURE 2B

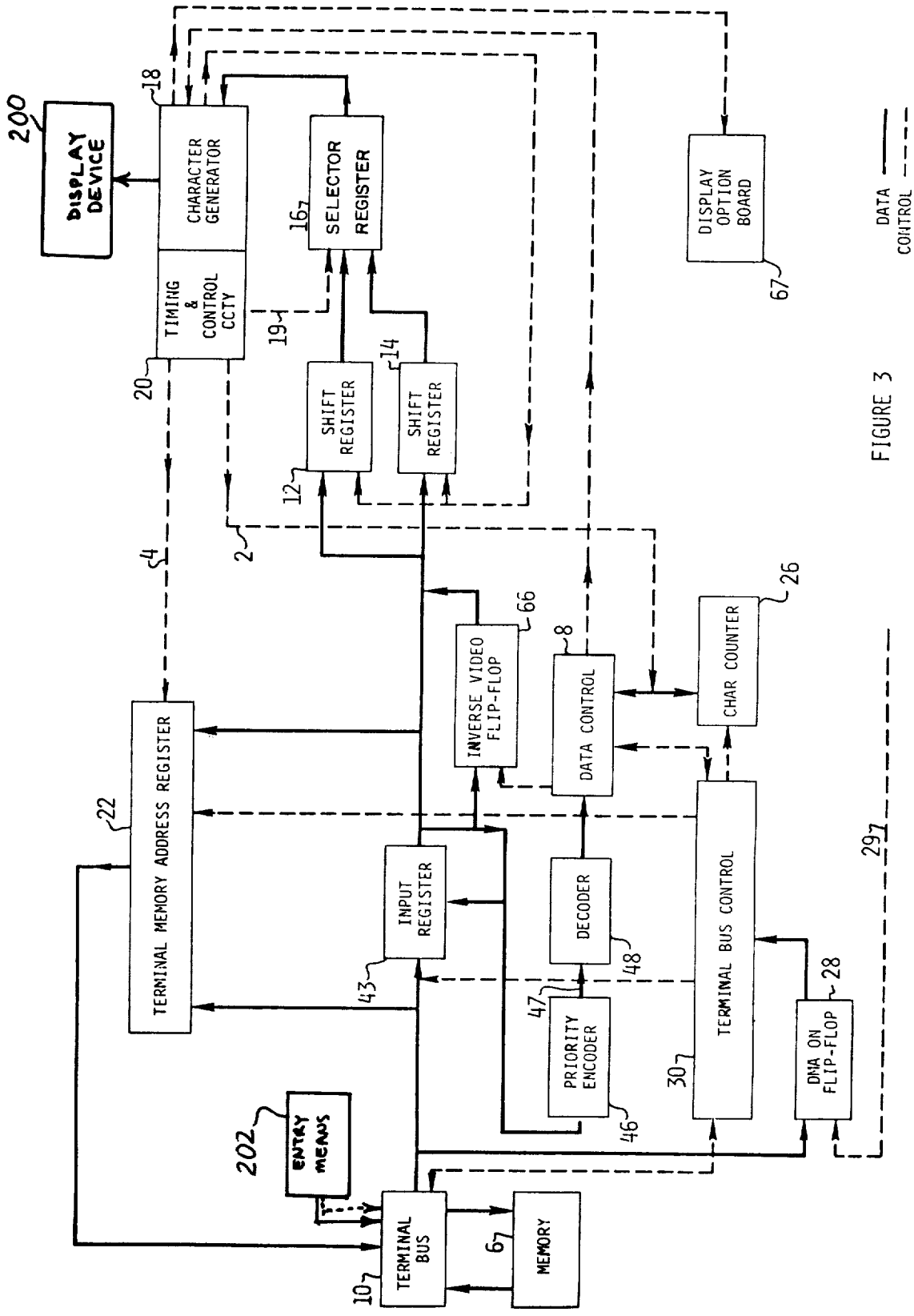

200
DISPLAY DEVICE
18
CHARACTER GENERATOR
TIMING & CONTROL CCTY
19
20
16
SELECTOR REGISTER
14
SHIFT REGISTER
SHIFT REGISTER
12
2
4
DISPLAY OPTION BOARD
67
DATA
CONTROL
66
INVERSE VIDEO FLIP-FLOP
8
DATA CONTROL
26
CHAR COUNTER
22
TERMINAL MEMORY ADDRESS REGISTER
INPUT REGISTER
43
DECODER
48
47
PRIORITY ENCODER
46
TERMINAL BUS CONTROL
30
29
28
DMA ON FLIP-FLOP
202
ENTRY MEANS
TERMINAL BUS
10
67
MEMORY

FIGURE 3

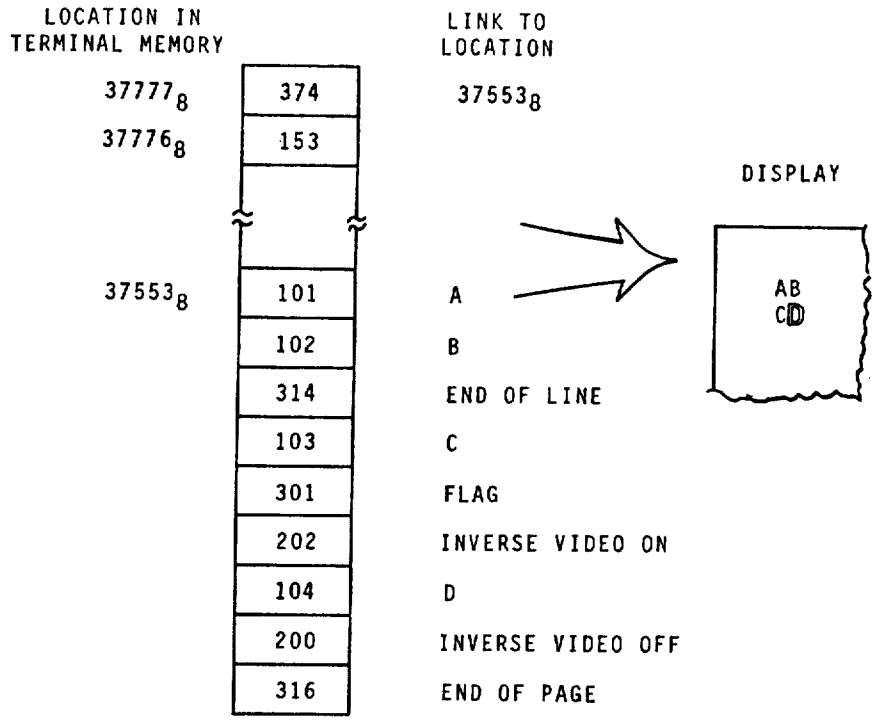


FIGURE 4

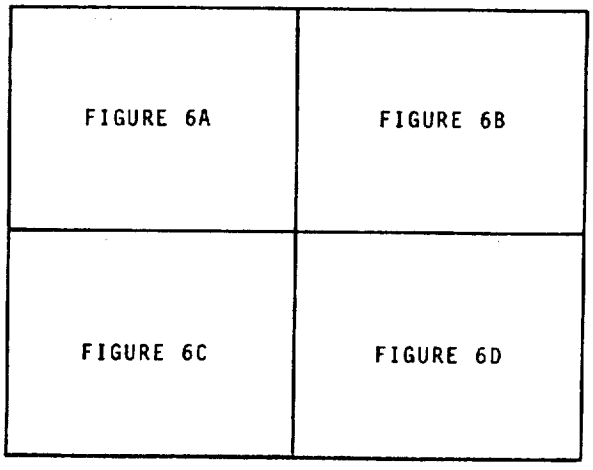


FIGURE 6

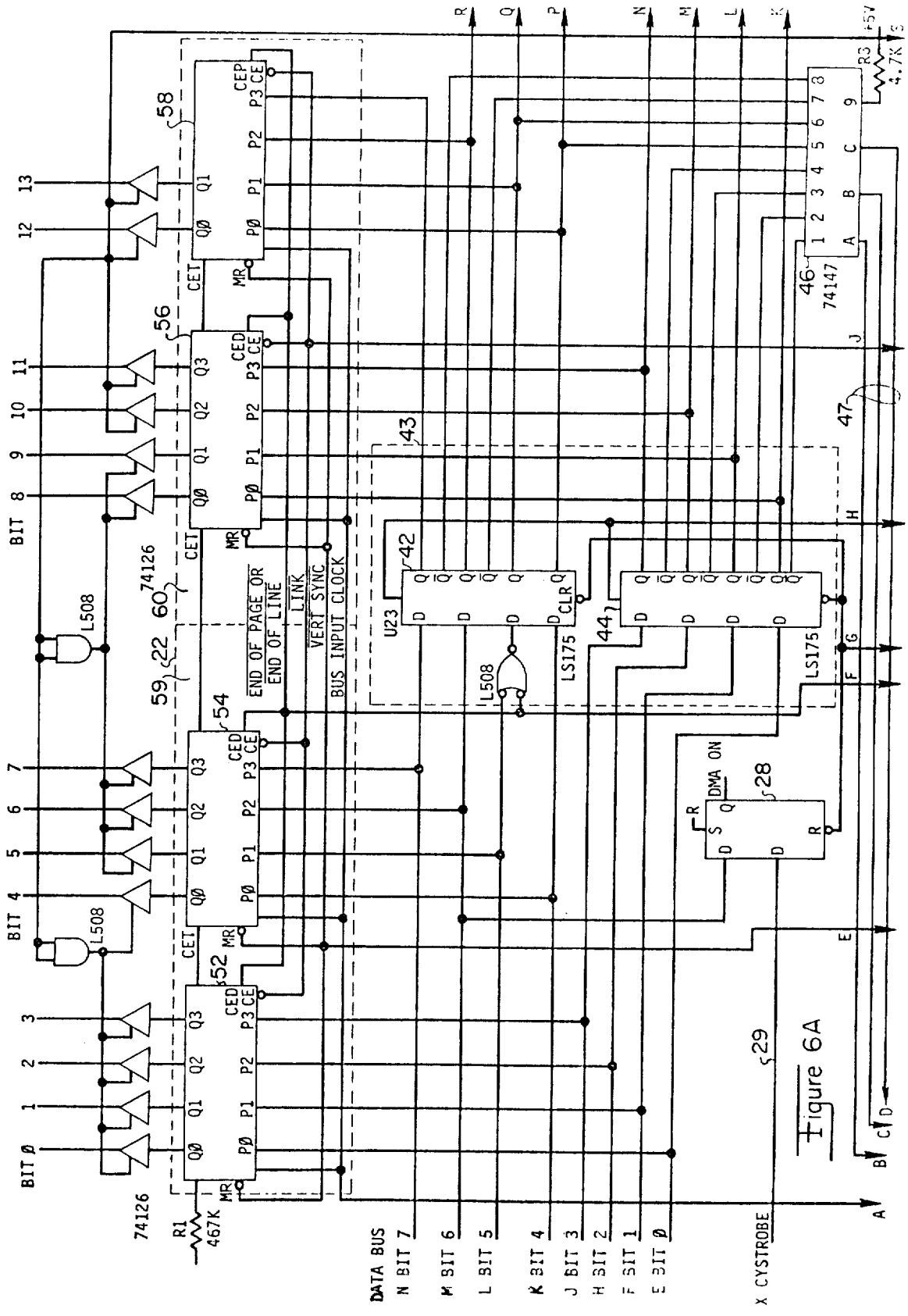

BIT 0
BIT 4
BIT 8
74126
R1
467K
L508
END OF PAGE OR
END OF LINE
LINK
VERT SYNC
BUS INPUT CLOCK
U23
LS175
DMA ON
74147
R3
4.7K
+5V
DATA BUS
N BIT 7
M BIT 6
L BIT 5
K BIT 4
J BIT 3
H BIT 2
F BIT 1
E BIT 0
X CYSTROBE

Figure 6A

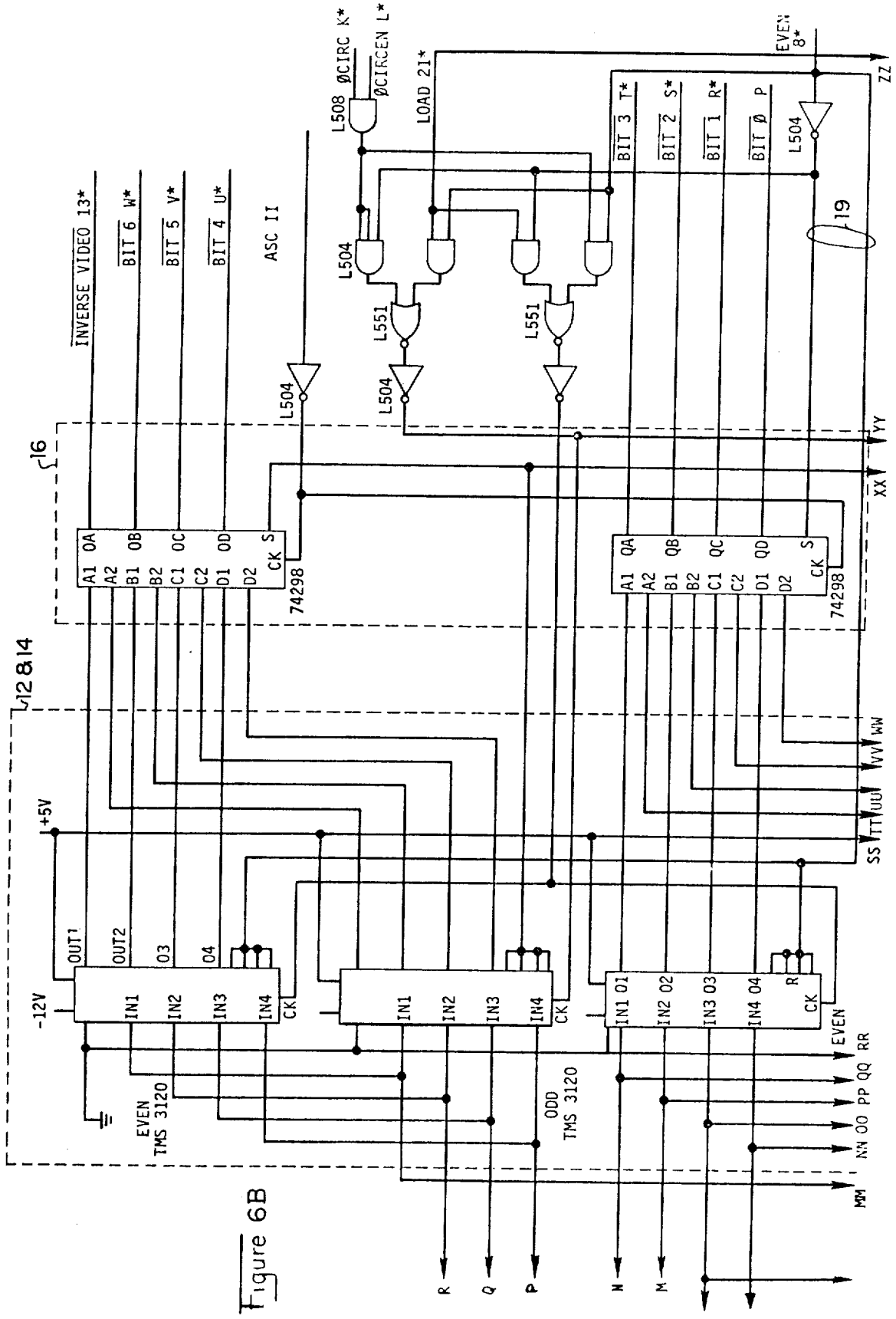

INVERSE VIDEO 13*
BIT 6 W*
BIT 5 V*
BIT 4 U*
ASC II
L508 ØCIRC K*
ØCIRCEN L*
LOAD 21*
BIT 3 T*
BIT 2 S*
BIT 1 R*
BIT Ø P
EVEN 8*
ZZ
L504
L551
19
16
74298
YY
XX
12 & 14
WW
VV
UU
TT
SS
+5V
-12V
OUT1
OUT2
O3
O4
IN1
IN2
IN3
IN4
CK
EVEN TMS 3120
ODD TMS 3120
EVEN
RR
QQ
PP
OO
NN
MM
R
Q
P
N
M

Figure 6B

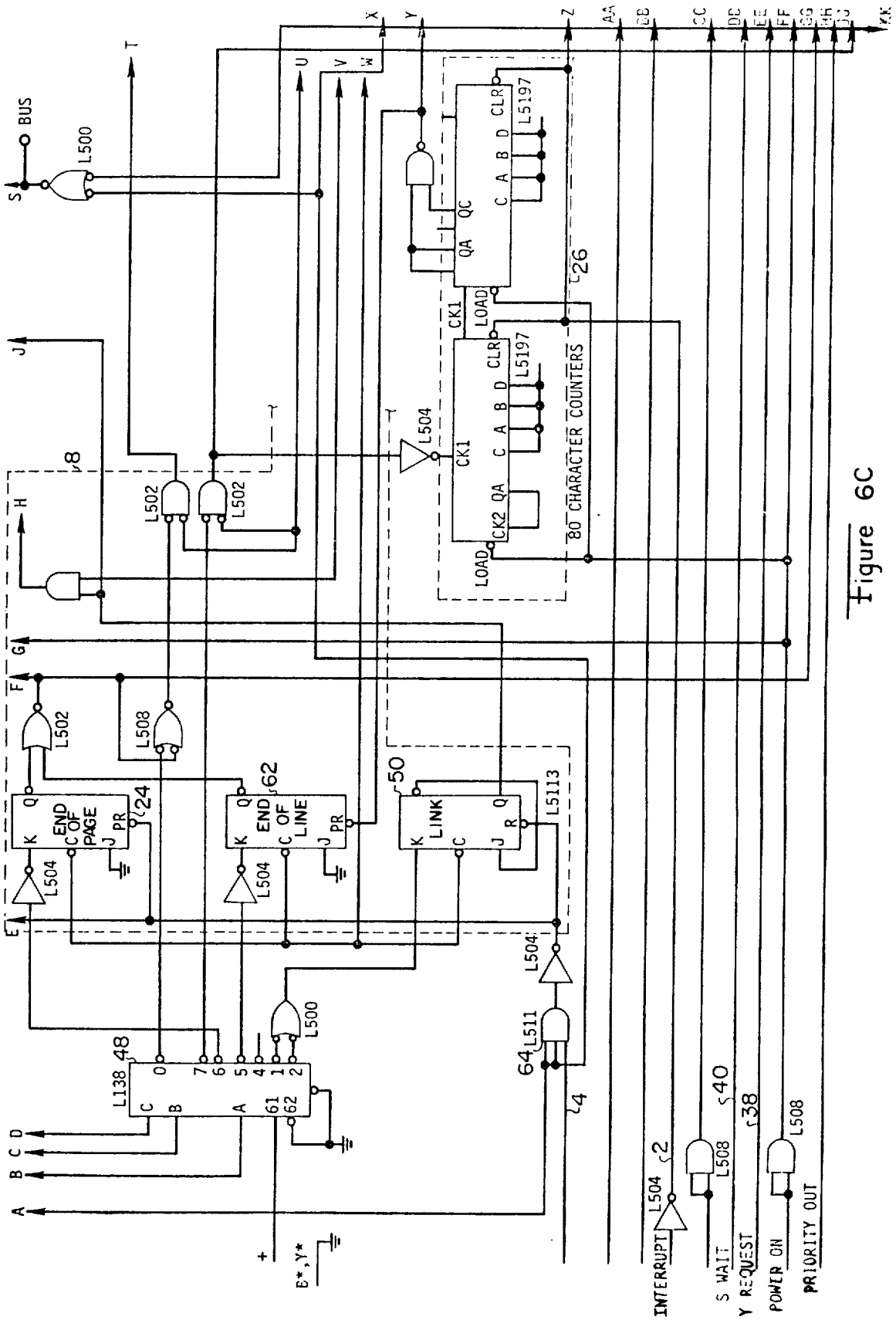
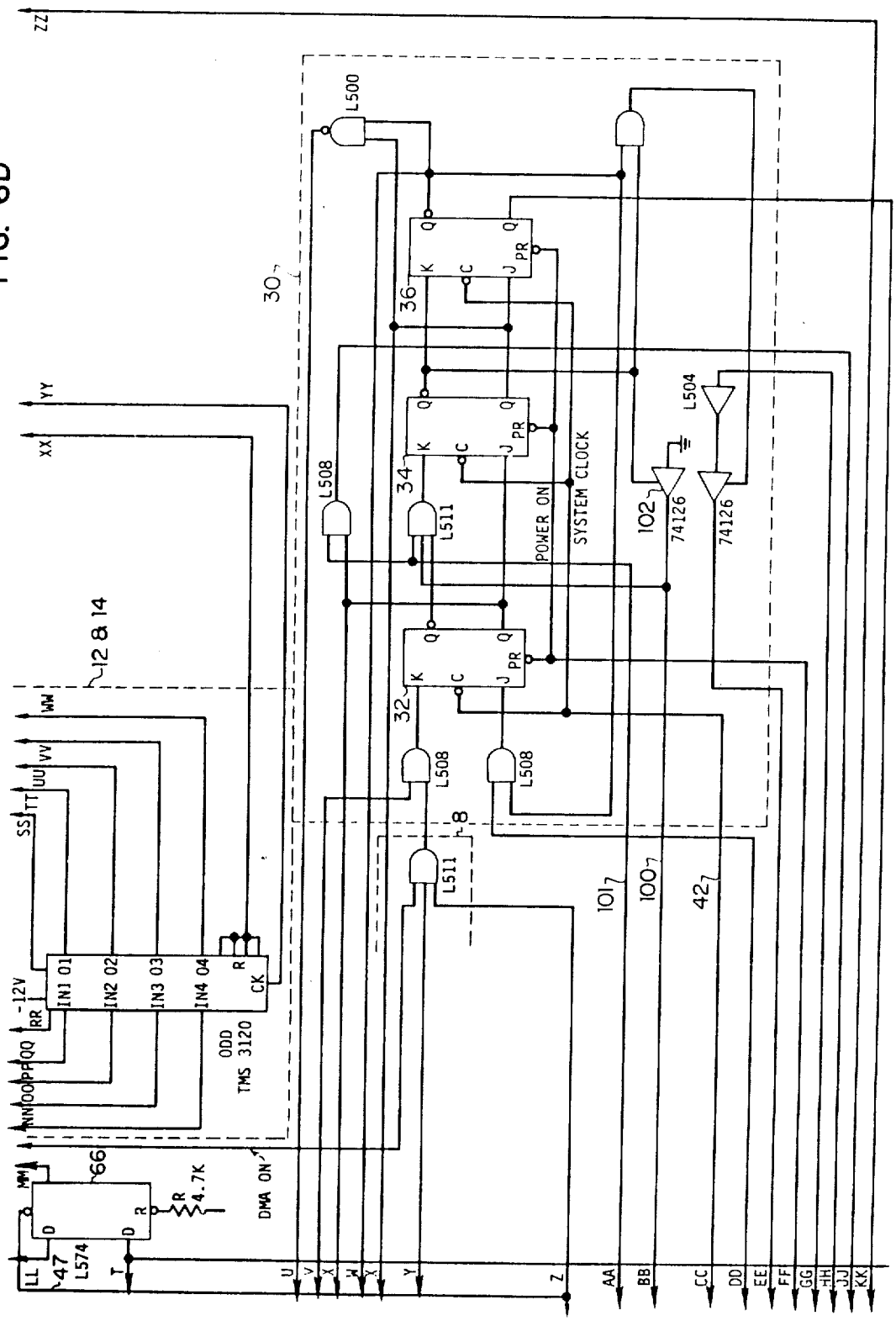

BUS
L500
L5197
80 CHARACTER COUNTERS
L502
L504
L508
END OF PAGE
END OF LINE
LINK
L5113
L511
L138
INTERRUPT
S WAIT
Y REQUEST
POWER ON
PRIORITY OUT

Figure 6C

FIG. 6D


ZZ
YY
XX
WW
VV
UU
TT
SS
RR
QQ
PP
OO
NN
MM
LL
30
36
34
32
8
L500
L508
L511
L504
74126
74126
POWER ON
SYSTEM CLOCK
12 & 14
IN1 01
IN2 02
IN3 03
IN4 04
R
CK
-12V
ODD
TMS 3120
DMA ON
66
4.7K
47
L574
101
100
42
102
U
V
X
W
X
Y
Z
AA
BB
CC
DD
EE
FF
GG
HH
JJ
KK

BUS CYCLE FLIP FLOPS

32	34	36	MEANING	BUSY	REQUEST	PRIORITY OUT	INPUT TO STATE
0	0	0	IDLE	0	0	PRIORITY IN	STATE 001
1	0	0	REQUEST BUS	0	0	0	$\overline{80}$ DMA ON
1	1	0	GET BUS	1	0	0	STATE 100 $\overline{BUSY}$. PRIORITY IN
1	1	1	REQUEST	1	1	0	STATE 110
0	1	1	DECODE INPUT BYTE	1	1	PRIORITY IN	$\overline{WAIT}$. STATE 111
0	0	1	RELEASE BUS	0	0	PRIORITY IN	STATE 011

FIGURE 7

CHARACTER ENCODING

	BIT	7	6	5	4	3	2	1	Ø	FUNCTION
DISPLAY CHARACTER		0	X	X	X	X	X	X	X	DATA (128 BITS)
CONTROL ENCODING CHARACTERS		1	0	X	X	X	X	X	X	CONTROL (64 BITS)
		1	1	1	X	X	X	X	X	LINK
		1	1	0	1	X	X	X	X	LINK
		1	1	0	0	0	X	X	X	FLAGS
		1	1	0	0	1	1	0	0	END OF LINE
		1	1	0	0	1	1	1	0	END OF PAGE

FUNCTION	EXPLANATION
DATA	128 ASCII FIGURES
CONTROL	2 CHARACTER SETS, HALF BRIGHT, UNDER LINE, INVERSE VIDEO, BLINK, ETC.
LINK	MOST SIGNIFICANT BYTE, LEAST SIGNIFICANT BYTE OF LOCATION OF NEXT CHARACTER
FLAGS	USED FOR PROTECTING FIELDS
END OF LINE	BLANK TO END OF LINE
END OF PAGE	BLANK TO END OF PAGE

FIGURE 8

LINKED LIST DATA ENCODING METHOD AND CONTROL APPARATUS FOR A VISUAL DISPLAY

CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation in part of co-pending U.S. patent application Ser. No. 508,600, filed Sept. 23, 1974 now U.S. Pat. No. 3,972,026 issued July 27, 1976 entitled "Linked List Data Encoding Method & Control Apparatus for Refreshing a Cathode Ray Tube Display" by Thomas E. Waitman, et al.

BACKGROUND AND SUMMARY OF THE INVENTION

Visual display apparatuses such as cathode ray tube terminals, impact and thermal printers, laser beam raster scanned displays and the like can have a number of hardware and software specialized functions which describe the displayed image besides the normal characters. For example, in a CRT terminal the characters can be blinking, half-bright, inverse video or underlined. The characters may be protected so they may not be altered. In addition, the display structure itself may be alterable. All three of these types of information: hardware display parameters, software parameters, and display structures are examples of information which must be embedded in the display text without causing blanks to be inserted in the visual display.

A typical solution is to use a wide display character which has appended to it one bit for each function. Each additional bit represents a different control function. Referring to FIG. **1**, there is shown a typical method wherein parallel definition of display parameters is utilized. Such a method would require, for example, if ASCII were the coding utilized, the width of the characters to be 7-bits. One bit in addition would be required for each enhancement mode. Six enhancement modes would require an additional six bits for each character displayed. If one were to add a protected field feature, the total required width necessary would be 14 bits per character. This would require a display memory having a capacity greater than or equal to 14 bits per character. If a particular enhancement feature, for example, underlining, were desired, the enhancement bit would be on for characters displayed with underlining and off for non-underlining. Therefore, whether an ehhancement feature is used or not, the extra bits of display storage are required.

Referring to FIG. *2a*, there is shown a second method having advantages over the first. In this second technique every character is made 8-bits wide. The characters are of two types: 8-bit data characters and 8-bit control characters. Data characters are directly displayable whereas control characters indicate a change in mode of enhancement or other control function.

Referring to FIG. *2b*, assume it is desired to display the word "FIELD" and to underline each character of the word. The traditional technique discussed above would add a bit to each of the displayed data characters indicating that that character is to be underlined. In contrast, the second method would precede the displayable word in the character stream with a control character to "start underlining." This control character would then be followed by the five display characters. After the final data character to be displayed another control character indicating "stop underline" would be sent. It can be seen that the second method requires data storage in the memory only when enhancements are actually used. The second method has advantages over the first in that the control characters are needed only if the current control state is to be changed. No unnecessary memory is required. Further, the number of control functions is not limited.

DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an encoding method heretofore known in the art utilizing parallel definition of display parameters wherein extra bits of display storage are required whether an enhancement feature is used or not.

FIGS. **2A** and **2B** illustrate a novel encoding method wherein data representing figures to be displayed and control functions are configured as 8-bit data and control characters.

FIG. **3** is a block diagram of a preferred embodiment for use with a CRT made in accordance with the invention.

FIG. **4** illustrates a manner of storing data in a memory in a linked list for use with the embodiment of FIG. **3.**

FIG. **5** illustrates the interrelationship between data blocks, links, and a visual display per scanned line.

FIG. **6** shows the relationship of FIGS. **6A** to **6D** which together are a detailed schematic diagram showing commercially available hardware for implementation of the preferred embodiment of FIG. **3.**

FIG. **7** illustrates the coding sequence of the bus cycle flip-flops of the preferred embodiment.

FIG. **8** illustrates a method of encoding data for use with the preferred embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. **3**, there is shown a display apparatus which reads characters from a random access memory **6**, accesses data via input register **43**, buffers them in 80-character shift register **12** and **14**, and sends them to selector register **16** and then to character dot generation circuitry **18** which drives display device **200**. The system responds to interrupt set signals **2** and vertical sync signals **4** from Timing and Control Circuitry **20** within character generator **18**. Interrupt set signal **2** indicates that a new line of figures to be displayed is to be fetched from the terminal memory **6**. Vertical sync signal **4** indicates a beginning of a visual display device scan. Interrupt set signal **2** triggers this system to access 80 displayable characters from memory **6** via a terminal data bus **10**. The data is placed into one of two 80-character buffers **12** and **14**. The buffer which is not being loaded by the system is being rotated at a 2.34 MHz rate and supplies one character for every nine dot positions being scanned across the face of a display device **200**. From the system a character may go, for example, through the character generator **18** to a parallel to serial converter and finally to a cathode ray tube monitor or the like. If the character position is, for example, 15 scan lines high, the 80-character buffers are rotated fifteen times before a switch to a new displayable line is signaled by the toggling of an even/odd line **19** from the timing and control board circuitry **20**.

This cycle repeats with the two 80-character buffers **12** and **14** ping-ponging, the first buffer refreshing while the other loads from the terminal memory **6**, and then their roles reverse.

Referring to FIG. **3**, control and data characters are input by entry means **202** such as, for example, a key-

board and stored in the terminal random access memory 6 in descending memory address order. The first character fetched is, for example, at an octal address 37777, shown 37777_8 in FIG. 4, which is the highest or most significant memory address in the terminal. The next character is 37776_8, etc.

Referring to FIG. 3, at the beginning of a display of a page the terminal memory address register 22 is set to location 37777_8. A data control 8 accesses data characters, decrementing address register 22 after each character and executing the following display and control functions: LINK, wherein two characters are fetched from the terminal memory and become a next location address from which data is to be read. END OF LINE, wherein the remainder of a line to be displayed is written with blanks. END OF PAGE, wherein the remainder of a page to be displayed is written with blanks. FLAG, which is used for protecting data fields. DISPLAY ENHANCEMENT, wherein the control system uses one of the display enhancement bits, an INVERSE VIDEO bit, and passes it on to the Timing and Control Circuitry 20 along with characters to be displayed. CHARACTER, wherein a 7-bit code, for example ASCII or the like, represents 1 of 128 characters to the character generator means 18. Eighty displayable characters per line are accessed, after which data control 8 turns off and awaits a signal from Timing and Control Circuitry 20 to start a new line. After 24 lines have been fetched from the terminal memory 6, the cycle repeats with the terminal memory address register 22 being set again to 37777_8.

Referring to FIG. 8, there is shown a novel encoded instruction scheme for use with the embodiment of FIG. 3. Assume a visual display device is scanned one whole frame every 1/60th second. During this time data characters and control characters are retrieved from the memory 6. As each 8-bit character is accessed, address register 22 is decremented. If the character is a display character, a character counter 26 is incremented. This keeps track of the remaining number of characters to be accessed from the memory 6 of a line to be displayed. However, if the character is a control character, the address counter 22 is incremented but not the character counter 26. Eight-bit characters continue to be accessed from memory 6 until 80 display characters have been accessed. Since control characters don't count in this accumulation, the number of control characters is variable.

The problem of decoding the novel encoded instruction set shown in FIG. 8 is neatly resolved with a priority encoder and decoder. Referring to FIG. 3, the data in register 43 goes into a priority encoder 46, which may be a Texas Instruments type 74147 integrated circuit, or the like. Encoder 46 has the characteristic that a 3-bit number 47 which comes out represents the highest bit position input which has a zero. The 3-bit number 47 goes into a decoder 48, which may be a Texas Instruments type LS 138, or the like. The result is that one pin of the decoder 48 goes low depending upon which type of character was fetched from memory. Thus, if the character fetched were an END OF LINE function, the number 5 output of the decoder 48 would go low. If the data were an ASCII character, the number 7 output would go low.

Referring to FIG. 4, data is usually stored in terminal memory 6 in a LINKED LIST. A link may be, for example, a 2-character control sequence, as shown in FIG. 4, which is interpreted by the data control 8 to change the terminal memory address of the next character to be fetched. The links allow the terminal memory 6 to be organized and used in a uniquely efficient manner and allow the tying together of data representing displayable lines of a visual display scan into displayable pages.

Referring to FIG. 5, the first two locations fetched, 37777_8 and 3776_8, are a link to the first 16-character block of information stored in terminal memory 6. In this first block of a line are links to the next block of that line and a link to the first block of the previous line and the next line.

Referring to FIG. 6, as the 24th character row of a visual display device is scanned a short vertical sync pulse 4 is received by address counter 22. This resets the address counter 22 to 37777_8 and resets an END OF PAGE flip-flop 24 within the Data Control 8.

At the same time, the Interrupt Set signal 2 clears the character counter 26 to 0.

The output of the character counter 26 is detected by the Data Control 8 as not being equal to 80. If a DMA on flip-flop 28 is set, then flip-flop 28 goes high and a bus cycle is started.

With a dynamically allocated display structure to which there is simultaneous access by more than one process, a lockout procedure is required. The shape of the structure must be changeable without destroying the continuity of other processes' access. With the linked list memory structure employed, the Data Control 8 picks up characters from the terminal memory 6 at regular intervals. A processor may, for example, be changing the structure of inserting and deleting lines. If the processor, for example, would start to change a link character and the data control 8 would ty to use the link, it would find one new character and one old one. This would errantly point the data control 8 off into memory, causing a flash on the screen. By turning the terminal bus control 30 off this flashing is minimized. The processor turns the bus control 30 off before changing a link and turns it on again after the change by means of flip-flop 28. Flip-flop 28 is clocked by a strobe signal 29 from a processor.

The bus cycle circuit 30 has three flip-flops, 32, 34 and 36. Referring to FIG. 7, the first flip-flop 32 is set when flip-flop 28 goes high and the flip-flops have a combined state of 000. When flip-flop 32 goes high, this is ANDed with two bus pins, BUSY 100 and PRIORITY IN 101. If these are both high, this indicates that the control apparatus may take control of the bus. Referring again to FIG. 6, it does this by setting flip-flop 34. This sets the bus signal BUSY 100 low through a tri-state gate 102.

The bus cycle flip-flops are all clocked off the trailing edge of a bus clock signal 42. After flip-flop 34 goes high, the combined state 110, shown in FIG. 7, flip-flop 36 is set. This enables a REQUEST signal 38 on the bus. If the logic is executing an END OF PAGE or END OF LINE function, the request signal 38 is held off.

The terminal memory 6 decodes its address and starts a timer upon receiving REQUEST 38. It immediately sets a WAIT signal 40 low to indicate that the REFRESH control apparatus should wait for the memory access time. When the memory's timer times out, it sets the WAIT line 40 high and the REFRESH apparatus proceeds to reset flip-flop 32. At this moment data is clocked off the data bus into the 4-bit register 42 and 44 of input register 43. If the function being executed were an END OF LINE or END OF PAGE, however, a

1-bit is inserted in bit 4 by priority encoder 46, which amounts to loading in of a "blank" character when interpreted by character generator 18.

The terminal bus control logic 30 resets flip-flops 34. This takes REQUEST 38 off the bus. The terminal memory 6 will discontinue output of data when it sees this.

Two hundred nanoseconds later, the address is taken off the terminal bus 10 as flip-flop 36 goes low. The terminal bus control 30 has now completed a six-state sequence, as shown in FIG. 7, and is ready to start over.

If the function decoded were a LINK, a link flip-flop 50 is set. On the next fetch from the terminal memory 6, the clocking in of data into the input holding register 42 and 44 is disabled by the link flip-flop 50 and, instead, data is loaded into the address counter 22 (lower half) consisting of address registers 52 and 54. The data in the character buffer register 43, comprising 42 and 44, is loaded into the address counter (upper half) 56 and 58. Thus, a two-character LINK operation has established a new terminal memory address in the address counter 59 and 60 (52, 54, 56 and 58). To summarize, the LINK command character becomes the high order bits of the new address and the second character fetched becomes the lower order bits of the new address.

The LINK flip-flop 50 is reset upon clocking the two characters into the address registers 59 and 60, completing the link operation.

If the control character is an END OF LINE, an end of line flip-flop 62 is set. Subsequent fetches from the terminal memory 6 are disabled by disabling the REQUEST signal 38. This causes dummy reads from memory. Since there is no request, no memory data is gated to the input register 43. Memory output remains at its quiescent state which is all zero. At the time data is clocked into the input holding register 43, the null input character is converted to a blank by character generator 18. Thus, it seems to the logic that blanks are being read from the memory 6. The address register 60 is inhibited from decrementing addresses so that the data control does dummy reads repeatedly from the same address. When all 80 characters have been input, the address counter 60 rolls over to 80. This holds off further data input. When the next interrupt set signal 2 from the Timing and Control Circuitry 20 resets the 80 character counter 26, the END OF LINE flip-flop 62 is also reset thereby returning the logic to the normal character input mode.

The END OF PAGE operates identically to the END OF LINE except that the END OF PAGE flip-flop 24 is reset by a vertical sync flip-flop 64. Thus, after an END OF PAGE function is input from the terminal memory 6, blanks are delivered to the screen to the bottom of the screen. At the end of the screen display, the vertical sync signal 4 resets the END OF PAGE flip-flop 24 thereby returning the logic to its normal character mode.

Flags are functions disregarded by the REFRESH control apparatus. When a flag is fetched from the terminal memory 6 only the terminal address counter 60 is decremented and the REFRESH control goes on to fetch the next character from terminal memory 6.

Referring to FIG. 8, displayable characters are those with a zero in bit 7 (the most significant bit) of the character. These are transferred to the 80-character circulating memory 12 and 14 from the input holding register 43. At the same time, the 80-character counter 26 is decremented.

Display enhancements select the character set and the enhancement modes of, for example, inverse video, half-bright, underline and blinking. They have a zero in bit 6 and a 1 in bit 7 as shown in FIG. 8. The REFRESH control clocks inverse video into inverse video flip-flop 66 and sends this clocking signal on to a Display Option board 67. The Display Option board 67 clocks in the other 5 bits of a Control character. The output of the inverse video flip-flop 66 is entered into the 80-character shift register 12 and 14 when the next character is entered. In the data stream, a Control character which changes the enhancements always precedes the data characters.

During the display of odd number lines on a visual display device, the REFRESH display circuitry is reading characters for the next even numbered row. There are 24 rows total. An even line, labeled as EVEN 8* in FIG. 6B, from the Timing and Control circuitry 20 indicates whether the display is on an even or odd line. This signal controls whether a rotating memory circulator clock signal shown as 0 CIRC K* and 0 CIRCEN L* in FIG. 6B from the Timing Control 20 is to be sent to the even or odd 80 character buffers 12 and 14. Thus during a display line on the screen, one set of the 80 character shift registers 12 and 14 is being loaded with new data from the terminal memory 6 while the other is being rapidly clocked. Characters for refreshing the screen are selected and clocked into an internal 8 bit register 16. The data is then sent to a ROM character generator 18.

Although preferred embodiments have been described for use with CRT displays, methods and apparatus incorporating the invention are useful in combination with many types of visual display apparatus including, but not limited to, for example, impact printers, thermal printers, laser beam raster scanned xerographic displays and the like.

We claim:

1. A method for displaying visual information comprising the steps of:
- encoding data representing figures to be displayed as data characters;
- encoding data representing enhancement features and execution path instructions as control characters;
- combining the data and control characters to form linked list data blocks;
- interpreting the linked list data blocks to form data representative of displayable lines; and
- applying said data representative of displayable lines to a display apparatus.

2. A method as in claim 1 wherein the step of combining the data and control characters comprises the steps of:
- storing the encoded data in a fixed memory scheme in accordance with a logic instruction;
- accessing the stored data from the fixed memory in response to execution path instructions contained within the data control characters; and
- applying the accessed data to a holding register.

3. A method as in claim 1 wherein the step of encoding data representing figures to be displayed comprises the steps of:
- configuring information representing figures to be displayed in an 8-bit coding scheme wherein a most significant bit is a zero; and
- identifying a particular displayable figure by the seven next significant bits.

4. A method as in claim 1 wherein the step of encoding data representing enhancement features and execution path instructions comprises the steps of:
configuring information representing enhancement features and execution path changes in an 8-bit coding scheme wherein a most significant bit is a 1; and
identifying a particular enhancement feature or control function by the remaining seven bits.

5. A method as in claim 2 wherein the step of interpreting the linked list data blocks comprises the steps of:
identifying data within a linked list data block representing a logic instruction address of a next data block to be accessed;
accessing the identified data block;
determining if the identified data block contains control characters or data characters;
applying a data character to character generation means;
identifying data within a control character as representing a change in an enhancement feature or an execution path instruction;
applying identified data representing a change in an enhancement feature to character generation means; and
changing character interpretation in response to identified data representing an execution path instruction.

6. Visual display apparatus comprising:
a memory having data and control characters;
a holding register coupled to the memory to receive data and control characters;
data decoding means coupled to receive a control character representing a link operation from the holding register for producing a line signal;
control means coupled to receive the link signal from the data decoding means for altering the addressing of a next character to be fetched from memory in response to the link signal; and
display means coupled to the holding register for displaying characters corresponding to said data characters.

7. Visual display apparatus as in claim 6 wherein the display means are coupled to the holding register with a buffer, the buffer comprising:
a first circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a displayable line of figures in response to a first applied signal;
a second circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a displayable line of figures in response to a second applied signal;
timing and control means for applying a first signal to the first circulating memory in response to an odd line being displayed and for applying a second signal to the second circulating memory in response to an even line being displayed; and
a selector register coupled to the display means and to receive data from the first and second circulating memories for selectively applying data from the first and second circulating memories to the display means in response to an applied timing signal.

8. Visual display apparatus as in claim 6 wherein data decoding means comprise:
encoding means coupled to receive a control character for producing a binary number representing the highest bit position of a selected logic level appearing in an applied control character input; and
decoding means coupled to receive said binary number for producing a link signal in response to a control character representing a link operation being applied as an input to the encoding means.

9. Visual display apparatus as in claim 6 wherein control means comprise:
an address register;
logic means coupled to receive the link signal for changing an output from a first to a second logic state in response to receiving the link signal;
a data control responsive to the second logic state of the logic means for accessing a second character from the memory and loading the control character representing a link operation and the second character into the address register; and
means coupled to the logic means for changing its output from the second logic state to the first logic state in response to the control character representing a link operation and said second character being loaded into the address register.

10. Visual display apparatus as in claim 6 wherein display means comprise a cathode ray tube display.

11. Visual display apparatus as in claim 6 wherein display means comprise an impact printer.

12. Visual display apparatus as in claim 6 wherein display means comprise a thermal printer.

13. Visual display apparatus as in claim 6 comprising means coupled to the memory for entering data characters.

14. Visual display apparatus as in claim 6 comprising means coupled to the memory for entering control characters.

15. Visual display apparatus as in claim 6 wherein display means comprise a printer having a laser beam which raster scans a photoconductive material.

16. Visual display apparatus as in claim 8 wherein the selected logic level is a logic zero.

17. Visual display apparatus comprising:
a memory having data and control characters;
a holding register coupled to the memory to receive data and control characters;
data decoding means coupled to receive a control character representing the end of a line of data figures to be displayed from the holding register for producing an end of line signal;
logic means coupled to receive the end of line signal from the data decoding means for inhibiting the fetching of characters from the memory and loading a selected data character onto the holding register in response to the end of line signal; and
display means coupled to receive data characters from the holding register for displaying visual images corresponding to said data characters.

18. Visual display apparatus as in claim 17 wherein data decoding means comprise:
encoding means coupled to receive a control character for producing a binary number representing the highest bit position of a selected logic level appearing in an applied control character input;
decoding means coupled to receive said binary number for producing an end of line signal in response to a control character representing an end of line

operation being applied as an input to the encoding means.

19. Visual display apparatus as in claim 17 wherein the selected data character represents a displayable blank.

20. Visual display apparatus as in claim 17 wherein display means comprise a CRT display.

21. Visual display apparatus as in claim 17 wherein display means comprise an impact printer.

22. Visual display apparatus as in claim 17 wherein display means comprise a thermal printer.

23. Visual display apparatus as in claim 17 wherein display means comprise a printer having a laser beam which raster scans a photoconductive material.

24. Visual display apparatus as in claim 17 comprising means coupled to the memory for entering data characters.

25. Visual display apparatus as in claim 17 comprising means coupled to the memory for entering control characters.

26. Visual display apparatus as in claim 18 wherein the display means are coupled to the holding register by a buffer, the buffer comprising:

a first circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a displayable line of figures in response to a first applied signal;

a second circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a displayable line of figures in response to a second applied signal;

timing and control means for applying a first signal to the first circulating memory in response to an odd line being displayed and for applying a second signal to the second circulating memory in response to an even line being displayed; and

a selector register coupled to the display means and to receive the data from the first and second circulating memories for selectively applying data from the first and second circulating memories to the display means in response to an applied timing signal.

27. Visual display apparatus comprising:

a memory having data and control characters;

a holding register coupled to the memory to receive data and control characters;

data decoding means coupled to receive a control character representing the end of a displayable page from the holding register for producing an end of page signal;

control means coupled to receive the end of page signal from the data decoding means for altering the address of a next character to be fetched from memory in response to the end of page signal; and

display means coupled to receive data characters from the holding register for producing images corresponding to said data characters.

28. Visual display apparatus as in claim 27 wherein data decoding means comprise:

encoding means coupled to receive a control character for producing a binary number representing the highest bit position of a selected logic level appearing in an applied control character input;

decoding means coupled to receive said binary number for producing an end of page signal in response to a control character representing an end of page operation being applied as an input to the encoding means.

29. Visual display apparatus as in claim 27 wherein the selected data character represents a displayable blank.

30. Visual display apparatus as in claim 27 wherein the display means are coupled to the holding register by a buffer, the buffer comprising:

a first circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a displayable line of figures in response to a first applied signal;

a second circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a displayable line of figures in response to a second applied signal;

timing and control means for applying a first signal to the first circulating memory in response to an odd line being displayed and for applying a second signal to the second circulating memory in response to an even line being displayed; and

a selector register coupled to the display means and to receive the data from the first and second circulating memories for selectively applying data from the first and second circulating memories to the display means in response to an applied timing signal.

31. Visual display apparatus as in claim 27 wherein display means comprise a CRT display.

32. Visual display apparatus as in claim 27 wherein display means comprise an impact printer.

33. Visual display apparatus as in claim 27 wherein display means comprise a thermal printer.

34. Visual display apparatus as in claim 27 wherein display means comprise a printer having a laser beam which raster scans a photoconductive material.

35. Visual display apparatus as in claim 27 comprising means coupled to the memory for entering data characters.

36. Visual display apparatus as in claim 27 comprising means coupled to the memory for entering control characters.

37. Visual display apparatus comprising:

a memory having data and control characters;

a holding register coupled to the memory to receive data and control characters;

data decoding means coupled to receive a control character representing an inverse video enhancement for producing an inverse video signal;

logic means coupled to receive the inverse video signal from the data decoding means for loading a selected bit onto the holding register in response to the inverse video signal; and

display means coupled to receive data characters from the holding register for producing images corresponding to said data characters.

38. Visual display apparatus as in claim 37 wherein the display means are coupled to the holding register by a buffer, the buffer comprising:

a first circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a display-

able line of figures in response to a first applied signal;

a second circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a displayable line of figures in response to a second applied signal;

timing and control means for applying a first signal to the first circulating memory in response to an odd line being displayed and for applying a second signal to the second circulating memory in response to an even line being displayed; and

a selector register coupled to the display means and to receive the data from the first and second circulating memories for selectively applying data from the first and second circulation memories to the display means in response to an applied timing signal.

39. Visual display apparatus as in claim **38** wherein display means comprise a CRT display.

40. Visual display apparatus as in claim **38** wherein display means comprise an impact printer.

41. Visual display apparatus as in claim **38** wherein display means comprise a thermal printer.

42. Visual display apparatus as in claim **38** wherein display means comprise a printer having a laser beam which raster scans a photoconductive material.

43. Visual display apparatus as in claim **38** comprising means coupled to the memory for entering data characters.

44. Visual display apparatus as in claim **38** comprising means coupled to the memory for entering control characters.

45. Visual display apparatus comprising:

a memory having data and control characters;

a holding register coupled to the memory to receive data and control characters;

data decoding means coupled to receive a control character representing a desired logic path execution change instruction for producing a control signal;

control means coupled to receive the control signal from the data decoding means for altering logic path execution in response to the control signal; and

display means coupled to receive data characters from the holding register for producing images corresponding to said data characters.

46. Visual display apparatus as in claim **45** wherein data decoding means comprise:

encoding means coupled to receive a control character for producing a signal representing the highest bit position of a selected logic level appearing in an applied control character input; and

decoding means coupled to receive the signal for producing a control signal in response to said signal.

47. Visual display apparatus as in claim **45** wherein the display means are coupled to the holding register by a buffer, the buffer comprising:

a first circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a displayable line of figures in response to a first applied signal;

a second circulating memory connected to receive data characters and having data storage positions equal to data necessary to display one line of displayable figures for producing data representing a displayable line of figures in response to a second applied signal;

timing and control means for applying a first signal to the first circulating memory in response to an odd line being displayed and for applying a second signal to the second circulating memory in response to an even line being displayed; and

a selector register coupled to the display means and to receive the data from the first and second circulation memories for selectively applying data from the first and second circulating memories to the display means in response to an applied timing signal.

48. Visual display apparatus as in claim **45** including lockout means coupled to the memory for disabling acquisition of data from the memory during alteration of logic path execution in response to the data decoding means receiving a control character representing a desired logic path execution change instruction.

49. Visual display apparatus as in claim **45** wherein display means comprise a CRT display.

50. Visual display apparatus as in claim **45** wherein display means comprise an impact printer.

51. Visual display apparatus as in claim **45** wherein display means comprise a thermal printer.

52. Visual display apparatus as in claim **45** wherein display means comprise a printer having a laser beam which raster scans a photoconductive material.

53. Visual display apparatus as in claim **45** comprising means coupled to the memory for entering data characters.

54. Visual display apparatus as in claim **45** comprising means coupled to the memory for entering control characters.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,047,248

DATED : September 6, 1977

INVENTOR(S) : Richard Ricker Lyman, Thomas Frank Waitman

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 4, line 8, cancel "3776_8" and insert -- 37776_8 --;

Column 4, line 66, cancel "register" and insert -- registers --;

Column 6, line 10, cancel "register" and insert -- registers --;

Column 7, line 35, before the word "signal", cancel "line" and insert -- link --.

Signed and Sealed this

Eleventh Day of April 1978

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

LUTRELLE F. PARKER
Acting Commissioner of Patents and Trademarks