
# SYSTEM DESCRIPTION AND MAINTENANCE MANUAL

# 9002

## MICROCOMPUTER TERMINAL SYSTEM

*Zentec Corporation*

Zentec Part No. 88-401-01

# SYSTEM DESCRIPTION AND MAINTENANCE MANUAL

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## MICROCOMPUTER TERMINAL SYSTEM

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Issued: April 1975

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# introduction

This manual describes the Zentec 9002 Microcomputer Terminal System, manufactured by Zentec Corporation, 2390 Walsh Avenue, Santa Clara, California, 95050, Telephone (408) 246-7662.

The manual contains information both for the end user, as well as for OEM system design and maintenance personnel. First, the manual serves as a general introduction to the 9002 system and as a reference of various system hardware and software options. Second, any reader who already has an operating knowledge of the system can learn more about system architecture – its hardware and software – by reading Section I of Chapter 4. This information is intended for system programmers and analysts, maintenance, and OEM design personnel. Section II of Chapter 4 provides additional detail about hardware for maintenance personnel. Chapter 5 contains hardware maintenance information, which allows maintenance of the system to a circuit card or major assembly replacement level. Chapter 6 contains information about various hardware options available to the OEM system designer and instructions on how to interface peripheral equipment to the 9002 system.

The following is a list of other manuals available on the 9002 system:

| Title | Zentec Part No. |
|---|---|
| 9002B Operator's Manual | 88-404-01 |
| Programmer's Language Manual | 88-403-01 |


Figure 1-1. The 9002 Microcomputer Terminal System.

# chapter 1 general information

## 1-1. GENERAL DESCRIPTION.

The Zentec 9002 Microcomputer Terminal System, see Figure 1-1, is a new generation data handling and processing device that can function either as a complete standalone computer system, or as an interactive intelligent data terminal. It is a general purpose system, that can be used for text or forms generation and editing, or can be programmed for other data processing or communication tasks.

The 9002 system consists of a desktop CRT display console and a separate keyboard from which data can be entered by the operator for display on the CRT screen. The system also can be interconnected via a telecommunications line to a host computer, which can send data for processing and display on the CRT screen, or receive data from the 9002 system. A variety of peripheral devices can be connected to the system to expand its data handling capabilities, or store programs and data for a particular processing application. Typical peripheral devices are a hard copy printer, or auxiliary memory devices such as a disc, cassette, or reel-to-reel tape drive.

The basic 9002 system components are a keyboard, a CRT display, and telecommunications interface electronics, all functionally organized around a microcomputer that controls data communications into and out of the system, and performs all internal data processing operations. The microcomputer and other components are described in more detail in paragraph 1-3 below.

## 1-2. APPLICATIONS.

The Zentec 9002 Microcomputer Terminal System can be used in two basic ways:

- as a standalone computer system (see Figure 1-3), or
- as a general purpose or dedicated data terminal (see Figure 1-4).

Every key on the keyboard is under software control and therefore, the user (through programming) has complete control over the functions performed by the 9002 system. As a standalone computer, the 9002 system can be used as a small general purpose computer, or it can be programmed and dedicated to a specific task. It can be equipped with auxiliary memory and input/output devices, see Figure 1-3, as required to support its computing functions. As a terminal, the 9002 system can be used with a host computer for simple data entry or display purposes, interactive on-line communications with the computer, or be programmed to perform data preprocessing prior to its transmission to the host computer. It can be connected to the host computer via a modem and a standard RS-232C telecommunications line, or directly. When used as a terminal, it can manage an auxiliary buffer memory also (see Figure 1-4).

Some specific uses of the 9002 system, in either the standalone computer or terminal capacity, are described below:

- As a small computer, the 9002 system can be used with an auxiliary memory for manuscript generation, storage, and editing. It can be programmed to receive input from, or output stored text to certain kinds of typewriter or typesetting equipment.
- As a small business computer the 9002 system can be programmed to perform accounting, inventory control, order processing, or payroll functions.
- As a small computer, the 9002 system can be used with an auxiliary memory for forms data entry, records storage, and updating purposes. It can be programmed to perform range checking, or other verification of data entered on the keyboard, data sorting, and classification tasks.
- As a terminal, the 9002 system can be used on line as a video teleprinter, to interact with the host computer on a character-by-character basis. For this purpose it can be connected to the host computer directly or via a modem and a telecommunications line.

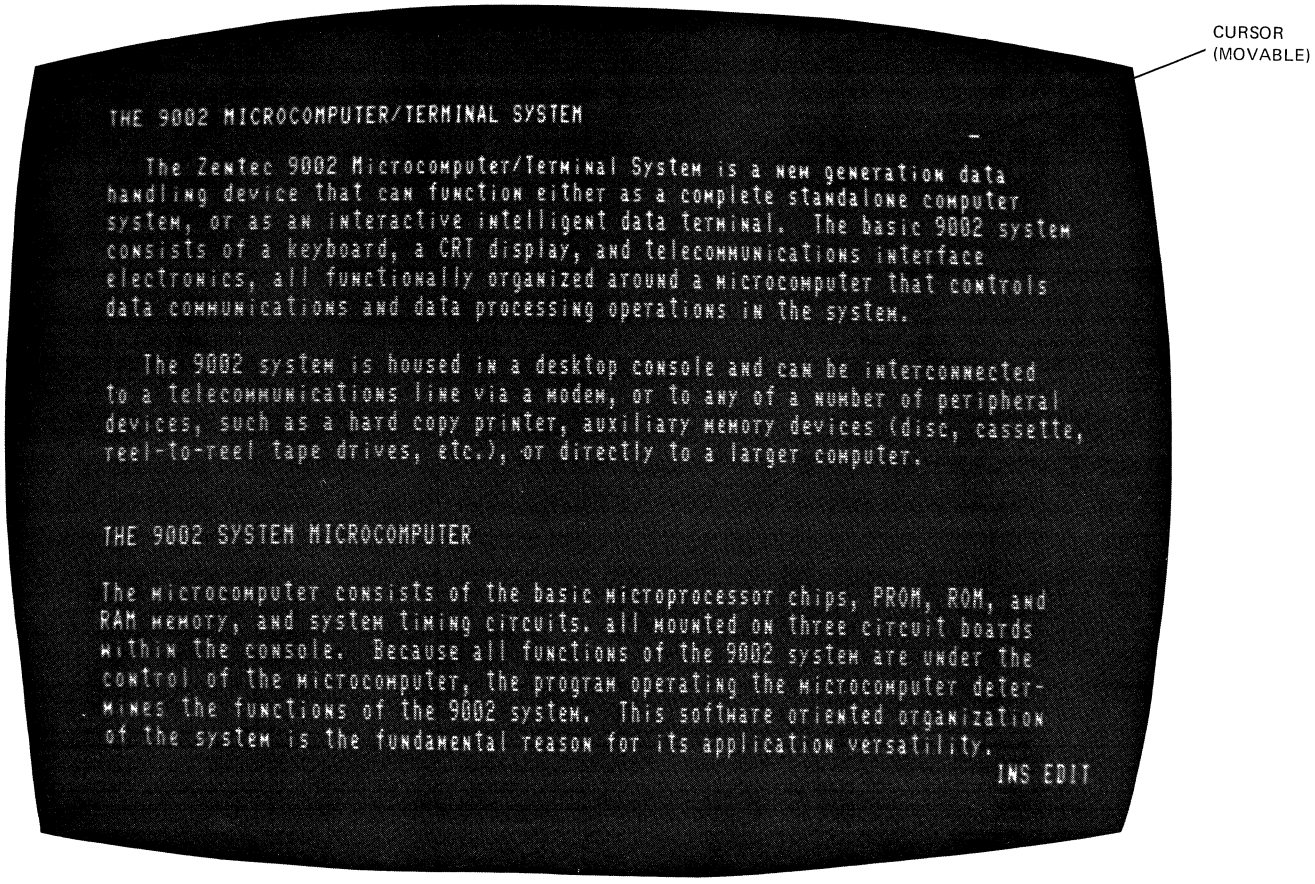
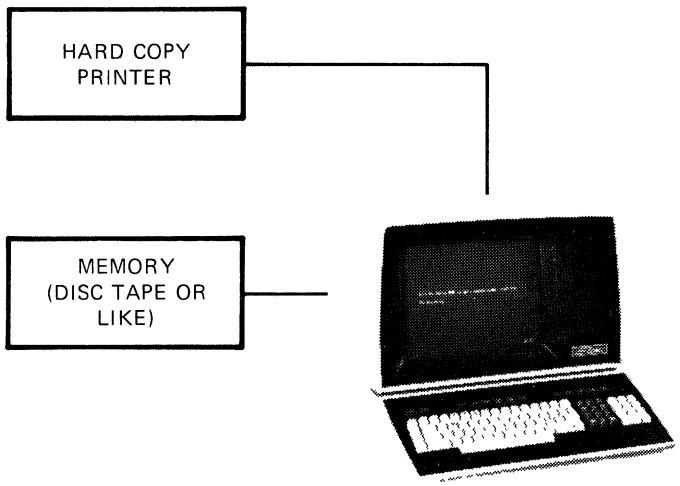
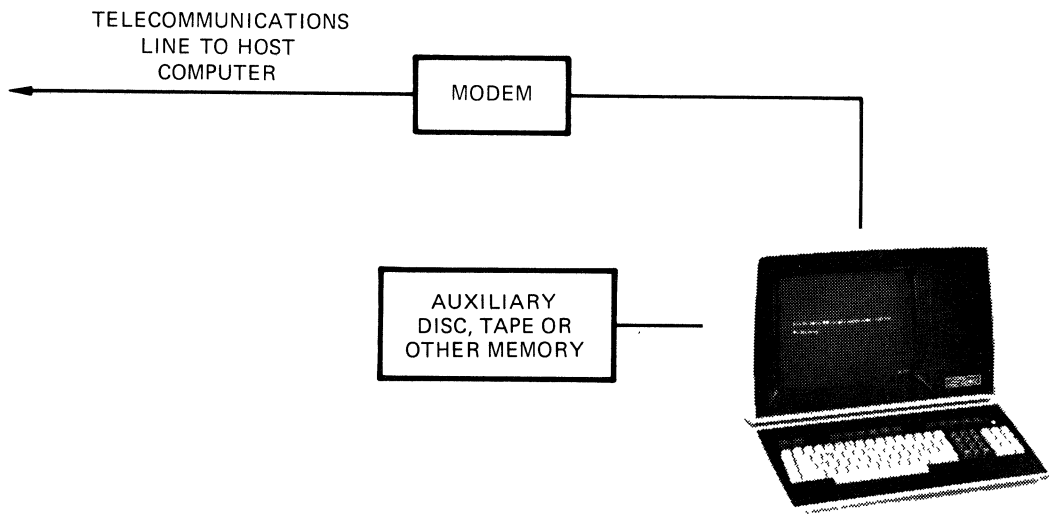



Figure 1-2. Typical Text Display on the 9002 System CRT Display.




*(9002 system functions as a standalone computer)*

Figure 1-3. The 9002 System Installation for Typical Standalone Computing Purposes.




*(9002 system functions as a data terminal)*

Figure 1-4. Typical 9002 System Telecommunications Installation.

- As a terminal, the 9002 system can be used on line for interactive text editing, forms data entry, inventory control, or in passenger/ accommodation reservation systems.

- With an auxiliary buffer memory, the 9002 system can be used as an input/output terminal in batch processing systems – either as a standalone terminal or in polled networks, as in banking or other financial applications.

## 1-3. FUNCTIONAL DESCRIPTION OF SYSTEM.

Functionally, the 9002 system consists of the microcomputer and input/output devices, see Figure 1-5. The microcomputer itself consists of an integrated circuit microprocessor, microprocessor timing and control circuitry, and ROM/PROM and RAM integrated circuit memory. These circuits, along with the input/output interface circuits, are mounted on three circuit cards located inside the CRT display console.

Because all basic functions of the 9002 system are under the control of the microcomputer, the program operating the microcomputer determines the functions of the 9002 system at any time. This software oriented organization of the system is the fundamental reason for its versatility in applications. One or more operating programs available from Zentec can be stored in the microcomputer memory and programs can generally be changed, or additional user programs can be installed into the microcomputer by the interchange or addition of memory circuits.

**1-4. The Microcomputer.** The microcomputer, Figure 1-5, is constructed around a general purpose microprocessor that can handle 8-bit words, has a repertoire of 48 instructions, and can address up to 16K of memory. It connects to a direct memory access data input/output bus, to which the keyboard, the CRT display, and the telecommunications interface electronics are all connected also. These circuits can perform their functions independently, while interfacing with the microprocessor or the memory on a priority basis. Optional interface circuits, peripheral devices available from Zentec, or devices added by the user, all can be connected to the I/O bus to operate in accordance with the priority discipline. Thus, the system can be expanded in a modular manner.

**1-5. The 9002 Microcomputer Memory.** The basic microcomputer memory consists of random access read-only and read/write semiconductor integrated circuits. The read-only segment of the memory (usually both ROM and PROM) contains the system operating program(s), but the read/write segment (RAM) is used to store video display information that is repeatedly read out of the memory to

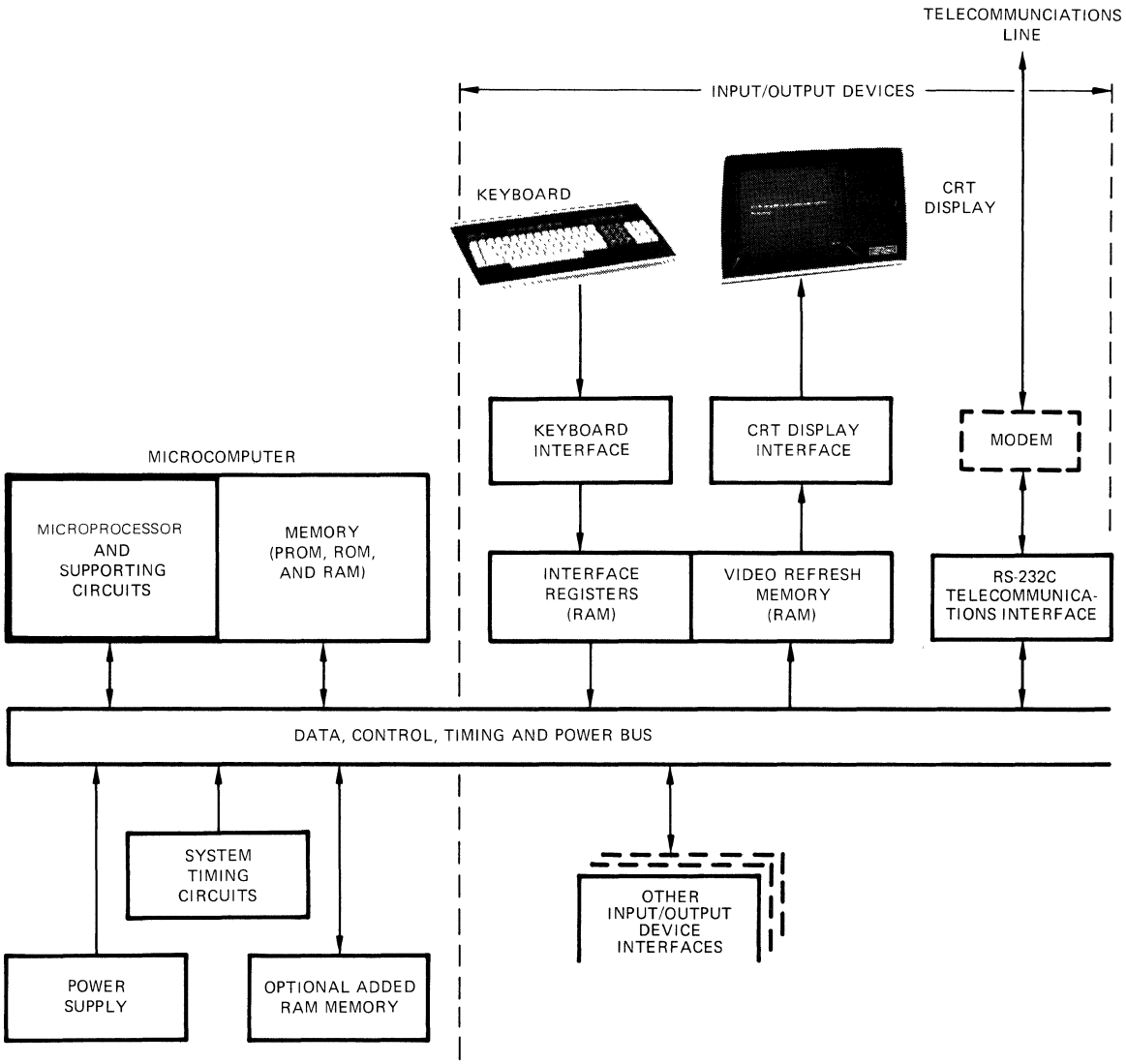


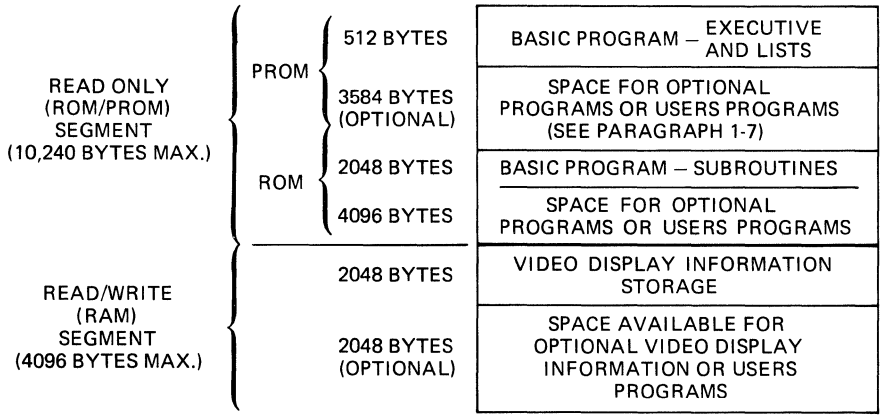

Figure 1-5. Functional Block Diagram of the 9002 Microcomputer Terminal System.

refresh the CRT display screen, and can also be used to store microcomputer programs or other data, if the application requires it. Figure 1-6 shows a diagram of the standard 9002 microcomputer memory.

The exact size of the memory depends on the size of the microcomputer programs stored in the system, and the amount of video display memory used, but in the standard system space is provided for the installation of 10,240 8-bit bytes of ROM and/or PROM program memory and up to 4096 8-bit bytes of RAM memory (part of which is available for optional programs

or expansion of video display information storage). With the addition of one circuit board, the total memory capacity can be expanded to 16,384 8-bit bytes. The additional memory is read/write RAM, that can be used for additional program storage, video display information storage, telecommunications data storage, or any other purpose useful in any particular system.

**1-6. Input/Output Interface Circuits.** Each of the 9002 system input/output devices is connected to the system bus through an interface circuit (and generally a RAM interface register). These circuits change the data signals from various forms useful to the external devices to a common form compatible with the memory or microprocessor. The keyboard, CRT display, and the RS-232C telecommunications I/O interface circuits each access a reserved




*Note: Excluding all options, the minimum combined PROM, ROM and RAM memory installed at the factory is 4608 bytes.*

Figure 1-6. Diagram of Standard 9002 Microcomputer Memory.

location in the RAM segment of the memory, but any optional peripheral devices can access the remaining parts of the RAM by addressing any of those locations. Some of the optional input/output interface circuits are designed to interface directly with the microprocessor.

## 1-7. SOFTWARE.

The 9002 system software includes a Basic Program, and a number of optional programs. The optional programs can be used to extend the general purpose capabilities of the Basic Program, to make the system suitable for special applications, or to aid the user in assembling his own programs.

The structure of all programs in the 9002 system is such that every program consists of an executive, pointer address lists, and a set of closed subroutines. In operation, the executive accesses the lists, locates the subroutine addresses, which then are accessed and executed. At the completion of any subroutine program control is always returned to the executive. One purpose of the list oriented program structure is to allow the user to easily insert other application oriented subroutines, that can be branched to simply by adding or changing addresses in the lists.

All of the fundamental programs are stored in ROM or PROM integrated circuits on the microprocessor circuit card, but additional RAM space is available for user programs. The additional RAM space can be used for application programs as well as for data storage and can be expanded up to a maximum of 10,240 8-bit bytes (depending on the exact configuration of other parts of the memory).

The general purpose programs currently available from Zentec are listed below and described in the following paragraphs, but other programs for special applications, maintenance, and programming purposes are also available. (Note that certain hardware options, described later in this chapter, are associated with program modifications also; these program modifications are not described separately here, but are described as a part of the hardware option.)

1. Basic Program (included with every system)
2. TELCOM (Telecommunications Support Programs)
3. Extended Text Editor (Catalog No. 24-004-01)
4. ZIM (Catalog No. 24-008-01)

## 1-8. BASIC PROGRAM.

The Basic Program comprises the essential software used to operate the 9002 system. This program provides fundamental text and forms handling functions and serves as a base for extending system capabilities with supplemental programs – either those described below or application programs created by the user.

The Basic Program is for off-line operations involving only the keyboard and the screen. There are two types of operations that can be performed with the Basic Program: generating or editing of text, while viewing it on the screen; or filling in and correcting the contents of a form displayed on the screen. For each of the above operations there is a particular mode; thus there are two data modes: a text mode and a forms mode. A third control mode, includes the capability to generate the headings for new forms.

## 1-9. TELCOM PROGRAMS.

The TELCOM programs include several different telecommunications support programs. Generally, these programs extend the Basic Program in that they include the Basic Program subroutine set and add the capability for communications between the 9002 system and a host computer via the RS-232C interface circuit.

For example, the TCOM I program (Catalog No. 24-003-01) allows either single character or block transmission and reception. There are five basic operating states of the terminal, while it is under the control of the TCOM I program: local, on-line, transmit, receive, and print. These states are described in more detail in the 9002 Operators Manual, Zentec Part No. 88-402-02.

## 1-10. EXTENDED TEXT EDITOR PROGRAM.

The Extended Text Editor program enhances the text mode capabilities of the Basic Program and can be installed in conjunction with the Basic or TELCOM programs. Its purpose is to give added capabilities for the editing of text displayed on the screen. For example, the Extended Text Editor enables the operator to insert or delete words or sentences and have the line(s) of text, or entire paragraphs, reformated. Thus, the Extended Text Editor program is useful for composing original copy or manuscript editing on the screen, in a more convenient manner than possible either on a typewriter or manually with paper and pencil.

### 1-11. ZIM (Zentec Interrogation Module) PROGRAM.

The ZIM program provides a means for visual access to the contents of ROM, PROM, and RAM memories in the system. The contents of each location in the memory is displayed on the screen in hexadecimal coded form and various sections of the memory can be moved on or off the screen with the cursor controls. In addition, contents of any memory location in the RAM segment can be altered from the keyboard when operating under the control of ZIM program. Consequently, ZIM program is useful for programming, program debugging, as well as maintenance purposes.

Installation of the ZIM program requires that the page two video display option (paragraph 1-13) is present in the system.

## 1-12. OPTIONS.

Because the 9002 system functions are programmable, the addition of any given optional function may require either a change in software (programs), addition of hardware (circuits), or both. The following paragraphs 1-13 through 1-24 describe those options that require hardware changes, whereas paragraph 1-7 describes the optional as well as standard software. Note, however, that even those options limited to software do require the change of ROM or PROM integrated circuits that store the control program, and may or may not require the expansion of memory capacity (by installation of additional memory circuits).

The standard 9002 system includes the Basic Program (see paragraph 1-8), at least 4608 bytes of combined ROM, PROM, and RAM memory, and the circuits for one RS-232C telecommunications interface. All these circuits are located on three circuit cards inside the display console.

### 1-13. PAGE TWO VIDEO DISPLAY OPTION (Catalog No. 01-402-01).

This option provides 2048 bytes of additional memory and supporting software for one full page (24 lines) of video display information. Thus, when the option is installed the operator can choose to display on the CRT display screen either of two full pages of video. With the paging and scrolling controls on the keyboard the operator can also choose to either scroll line by line through the two pages (always displaying 24 lines), or switch from one page to the other. Scrolling is defined as moving the display material across the screen one line at a time (with the scrolling controls); paging is defined as switching from one page to another (with the PAGE controls on the keyboard).

To implement this option, RAM and supporting circuits must be added on the video/RAM card and program modifications must be made on the microprocessor card.

## 1-14. GENERAL PURPOSE 2K MEMORY OPTION (Catalog No. 01-402-02).

This option adds an identical amount of 2048 bytes of memory to the system, as the page two video display option does, except it does not include any video display supporting software. This option can be installed in lieu of the page two option (but not concurrently with it) and the 2048 bytes of memory can be used as general purpose memory for the microprocessor.

## 1-15. RAM CARD (Catalog No. 02-401-01 through -04).

This option provides space for up to 8192 bytes of RAM memory, in addition to the ROM, PROM, and RAM memory provided in the standard 9002 system. It is located on one circuit card, which is installed in the display console circuit card chassis. Any number of bytes of memory in increments of 2048, can be installed on this card. The added memory space is under direct microprocessor control and can be used for additional program, video display, RS-232C interface, or keyboard data storage.

## 1-16. PRINTER SUBSYSTEM (Catalog No. 00-401-00).

The printer subsystem option enables the 9002 system to communicate with and print out data on a peripheral hard copy printer. The subsystem consists of a free-standing impact printer, a cable interconnecting the printer to the 9002 system display console, a printer interface card inside the display console, and software required to operate the printer as a 9002 system peripheral device. The printer operates at up to 45 characters per second and can input data into the 9002 system, receive data from the system, or operate off line. The printer is connected to the system bus via the printer interface card, similar to the manner shown in Figure 1-5.

## 1-17. DUAL RS-232 CARD. (Catalog No. 01-407-01).

This option provides two RS-232C telecommunication interface circuits, in addition to the one provided in the standard 9002 system. The two added interfaces are located on a single circuit card that is installed in the display console circuit card chassis. Along with this circuit card, the page two video option or the general purpose 2K memory option must be installed in the system.

If the dual RS-232 option is installed, there are three interfaces available for connecting to telecommunications lines or external equipment. The dual RS-232 circuits operate in such a manner that either can be receiving or transmitting data at any one time, but not both simultaneously. Switching between the two circuits must be done under software control. No supporting software is normally provided with this option.

An optional current loop circuit (Catalog No. 01-408-01 or -02) is available with the dual RS-232 interface, to allow operation with a teletypewriter or similar equipment.

### 1-18. DUAL DISC DRIVE SUBSYSTEM (Catalog No. 00-402-01).

This option is a disc memory peripheral device, complete with interfacing hardware and supporting system software. The subsystem consists of a free-standing disc memory, a cable that connects the disc memory to the CRT display console, a disc memory interface card inside the display console, and a disc handler program.

The disc memory consists of two separate disc drives and a controller, all housed in a common enclosure. The disc memory has a total capacity of 500,000 bytes, uses removable flexible ('floppy') discs, and records in IBM compatible format. It connects to the system bus through the interface card and communicates both directly with the microprocessor and reads and writes into the system memory.

### 1-19. CURRENT LOOP OPTION (Catalog No. 01-404-01 or -02).

The current loop option enables the 9002 system to be connected to any current operated peripheral device, such as a teletypewriter. The -01 version of this option can source or sink 20 milliamps of current, but the -02 version can source or sink 60 milliamps.

The current loop option utilizes the same basic data handling circuits as the RS-232C interface, with current sourcing and sinking circuits.

### 1-20. BAUD RATE OPTION (Catalog No. 01-403-01).

This option modifies the RS-232C telecommunication interface circuits so that the system can communicate data to and from the telecommunications line at a 4800 baud rate. The option involves a strapping change on the timing card and affects the operation of the BAUD RATE switch on the rear connector panel of the display console. If no baud rate option is installed in the system, placing the BAUD RATE switch in the SEL position enables the system to receive and transmit data at 2400 baud; if the option is installed, the corresponding rate is 4800 baud instead.

### 1-21. FULL INTERLACE DISPLAY OPTION (Catalog No. 01-409-01).

The standard 9002 system uses a video raster pattern in which half of the 500 visible scan lines overlay the other half, so that there are only 250 visible lines, with one line wide space between any two lines. This raster pattern provides good detail of displayed characters and a steady display, with no flickering. The full interlace display option modifies the timing card so that there is no overlaying and all 500 scan lines become individually visible (the physical positions of half of the scan lines are shifted so that the two video fields that constitute the raster are interlaced instead of overlaying each other). This raster pattern increases the detail of displayed characters, but a slight amount of flickering of the display may become visible to the human eye. Therefore, when the full interlace option is installed, the type P-39 long persistence phosphor should be specified for the CRT display screen (see paragraph 1-22 below).

### 1-22. TYPE P-39 PHOSPHOR CRT OPTION (Catalog No. 01-405-01).

This option constitutes a modification to the CRT display, such that type P-39 long persistence phosphor CRT tube is used (instead of type P4). This option should be specified if full interlace of the video raster is used in the system (paragraph 1-21 above).

### 1-23. DISPLAY FORMAT OPTION (Catalog No. 01-406-01 through -04).

The display format options are associated with the number of lines displayed on the CRT screen. In the standard 9002 system 24 operator controlled and a 25th program controlled line are displayed on the screen. If any of the display format options are installed, the number of operator controlled display lines are changed to the following:

-01 version – 12 lines

-02 version – 16 lines

-03 version – 20 lines

-04 version – 40 lines

To install any display format option, modifications must be made to the system timing card and the microprocessor card.

If the -04 version is installed, it also requires the presence of page two video display option, full interlace, and type P-39 phosphor. All versions require program modifications.

### 1-24. POWER OPTION – 220 V, 50 Hz (Catalog No. 01-401-01).

This option changes the operating power requirements of the 9002 system to 220 volts, 50 Hz. It cannot be installed in any system that has the full interlace display option in it.

## Table 1-1. Performance Specifications and Leading Particulars

| CHARACTERISTIC | VALUE |
|---|---|
| SYSTEM | |
| DIMENSIONS | |
| CRT Display Console | 21 in. W. * 16 in. H * 18 in. D |
| Keyboard | 20 in. W. * 3.5 in. H * 13 in. D |
| FINISH | textured vinyl, beige color |
| POWER REQUIREMENTS | 115 V ac ± 10%, 60 Hz; 220 V, 50 Hz optional |
| MICROPROCESSOR | |
| TYPE | Intel 8008; general purpose parallel processor with interrupt capability; inputs and outputs TTL compatible. |
| WORD SIZE | 8-bits |
| INSTRUCTION SET | |
| MEMORY ADDRESSING | Can address up to 16K bytes directly |
| MEMORY | |
| | Note: Maximum combined capacity of ROM, PROM and RAM cannot exceed 16,384 bytes. |
| ROM/PROM | |
| Capacity | Up to 10,250 bytes (2560 bytes are used by Basic Program) |
| Type | ROM: 2048 x 8, AMI S9996 or equivalent; PROM: 256 x 8, Intel 1702, 1702A, or equivalent. |
| RAM | |
| Capacity | Up to 4096 bytes can be installed in standard system, up to 12,288 bytes with addition of optional RAM card (2048 bytes s are used for video display in a standard system). |
| Type | 2048 x 1 dynamic. |
| KEYBOARD | |
| OUTPUT CODE | 128 ASCII and 43 special codes |
| Alphanumeric | 96 ASCII characters, upper and lower case |
| Control | 32 ASCII basic, 32 special, as modified by CTRL and SHIFT keys |
| Numeric | 10 special coded numbers and one special code for decimal point. |

## Table 1-1. Performance Specifications and Leading Particulars (Cont.)

| CHARACTERISTIC | VALUE |
|---|---|
| CRT DISPLAY | |
| CRT | |
| Size | 8 in. x 11 in., 15 in. diagonal |
| Phosphor | P4 (white); P-39 optional |
| SCAN METHOD | Noninterlaced, RS-330, 525 line compatible |
| SCAN RATE | 60 fields per second |
| CHARACTER FORMAT | |
| Display Matrix | 10 x 10 dot matrix of which a 7 x 9 matrix is used for character formation. |
| Size | 0.2 in. high by 0.09 in. wide |
| PAGE FORMAT | 80 characters on each line, 25 lines on full screen (defined as one page). Note: of the 25 lines, 24 are operator accessible, the 25th is used only by the microprocessor. |
| TELECOMMUNICATIONS INTERFACE | |
| TYPE | RS-232C, asynchronous, full or half duplex. |
| TRANSMISSION RATE | Selectable at 110, 300, 1200, or 2400 baud; the 2400 baud rate can optionally be changed to 4800 or 9600 baud. |
| CHARACTER SIZE | 8 data bits, with one start and one or two stop bits. |
| PARITY | Odd, even, or none |

# chapter 2 installation

## 2-1. INTRODUCTION.

In planning a 9002 system installation different considerations may need to be made by the user, depending on the type and complexity of the installation. Because the system is expandable by the addition of external peripheral devices, considerations may need to be made on how external devices are connected to the system I/O bus, and what future expansion space is necessary. This chapter describes some hardware considerations that must be made in planning location of the equipment and cabling interconnections.

## 2-2. PLANNING OF SYSTEM INSTALLATION.

### 2-3. GENERAL CONSIDERATIONS.

The Zentec 9002 Microcomputer Terminal System may be placed on a table surface or any other vibration free horizontal surface that is free from lint and dust and may be used under normal room lighting conditions, although a slightly subdued light will improve the display appearance. The display enclosure and keyboard together require 27 x 21 x 16 inch space envelope (see Figure 2-1) and the keyboard can be moved away from the CRT display console, within the radius of the 2 foot attaching cable. The equipment may be installed adjacent to most other types of electrical or electronic equipment, provided that it is not located in a strong magnetic field. Installation within a strong magnetic field may disturb operation of the display. No special cooling provisions need

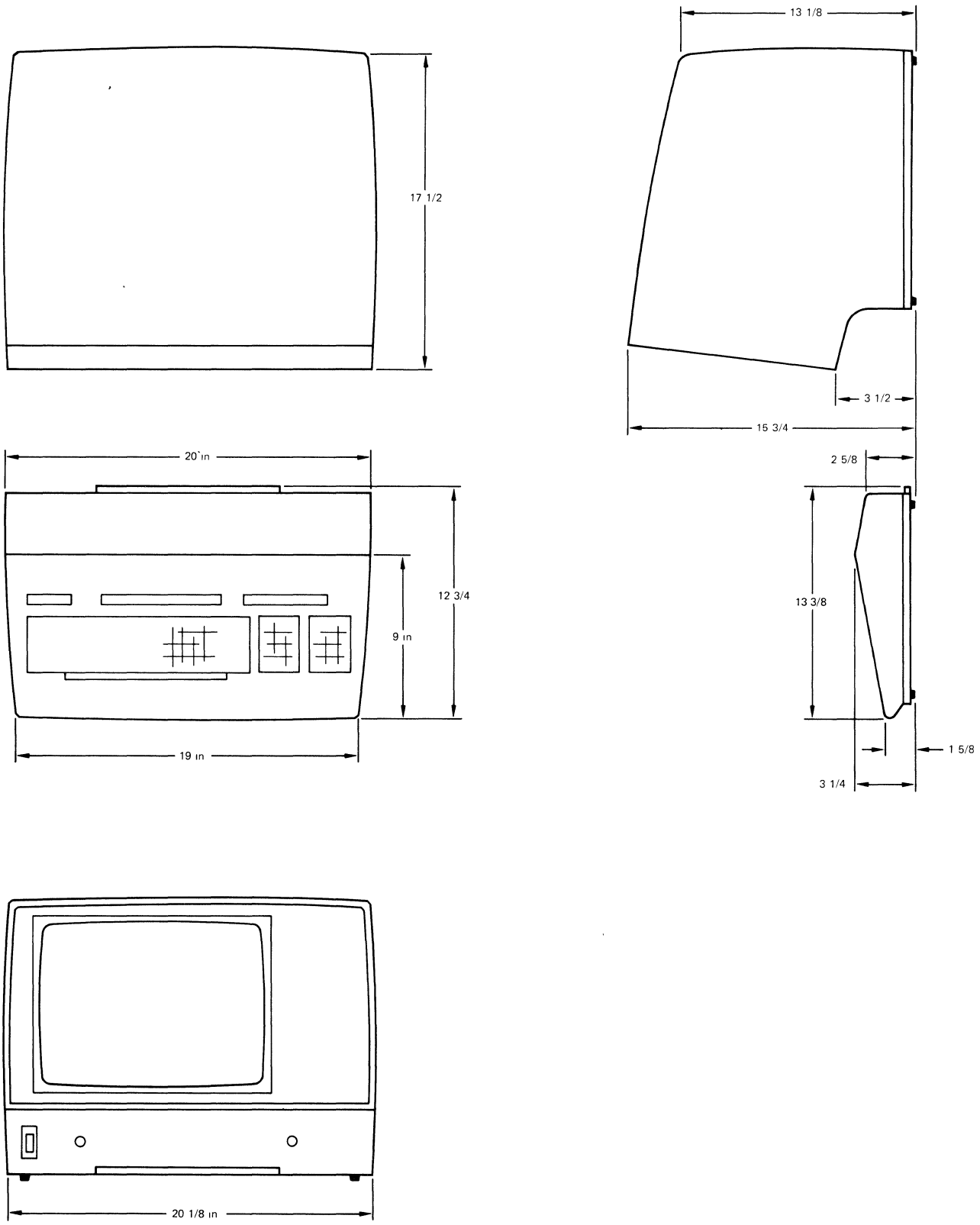



Figure 2-1. Mounting Dimensions of Display Console and Keyboard.

be made, but free flow of air must be allowed around the monitor chassis. The fan exhaust on back of the CRT display console may not be blocked. The display console is equipped with a 6-foot length of 3-wire power cord and requires 115 Vac power.

## 2-4. CABLING CONSIDERATIONS.

If the equipment is used as a standalone computer system, it requires 115 Vac power and the space and cabling provisions for connecting any optional input/output devices, such as a disc memory, or a hard copy printer. Cabling for input/output devices is generally connected to the rear connector panel of the display enclosure as shown in Figures 2-2 and 2-3; standard cables shipped with the disc memory or printer options are either 10 or 25 feet in length.

If the 9002 system is used as a data terminal, in addition to the 115 Vac power input, it must also have an interconnection to the host computer. This involves a cable connection from J1 on the rear of the 9002 display enclosure to some communication line. Commonly the connection is made via a modem and a common carrier telecommunications line (as shown in Figure 2-2), although in special cases a cable may be connected directly to the host computer, or some intermediate communications equipment. The standard cable available for connecting to a modem is Part No. 93-402-01 or -02, 10 feet and 25 feet in length, respectively. This cable has connectors on both ends, as specified by EIA Standard RS-232-C.

If a connection is to be made to equipment other than an RS-232C compatible modem, the user has to fabricate the necessary cabling. The cable should not exceed 50 feet in length and its connector pin assignments must be made in accordance with Table 2-1.

## 2-5. UNPACKING.

The 9002 system components are shipped in a special carton that provides protection against shipping damage. The display console and the keyboard are shipped in the same enclosure, with the interconnecting cable installed. Any additional items (such as extra cables for options, small maintenance tools, etc.) usually are packed in the same carton.

When unpacking the equipment, check each item in the packing case against the tabulation on the packing slip. If any breakage or physical damage is apparent, file a claim with the carrier immediately and notify Zentec Corporation. Use extreme care to prevent damage to the units during unpacking and removal from the shipping carton. Once removed, use a lint-free cloth or light air pressure to remove dust and packaging residue. Prior to installation, visually inspect the components for damage.

Save the special shipping carton, if reshipment of the 9002 system is anticipated.

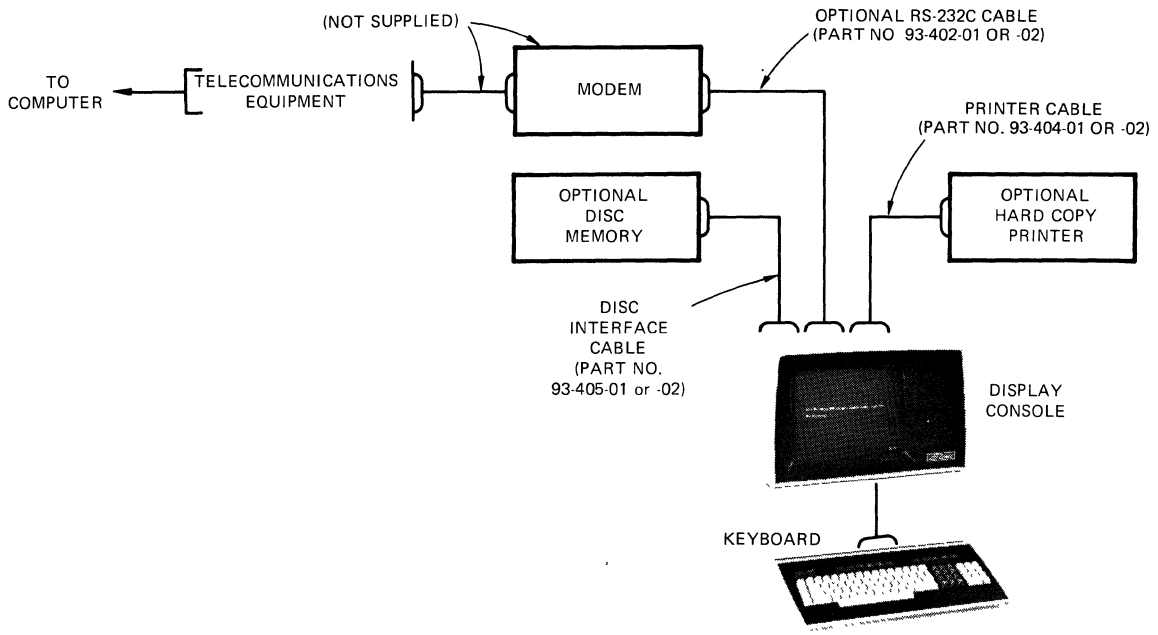



Figure 2-2. Typical System Cabling Diagram (showing a Telecommunications Interconnection).

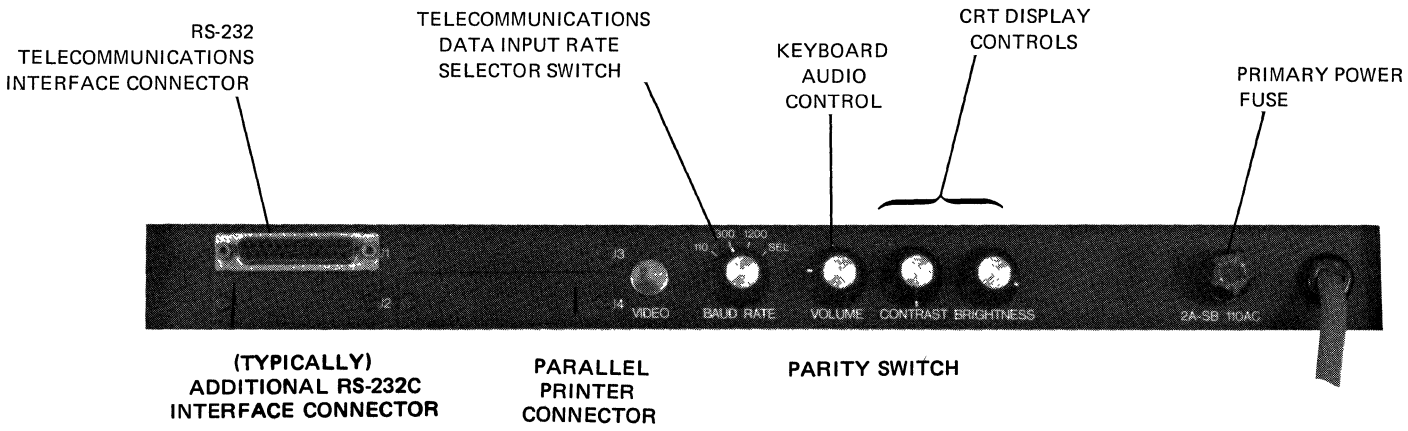



Figure 2-3. Rear Panel of Display Console.

Table 2-1. Pin Assignments of the Rear Panel Telecommunications Connector.

| PIN NO. | FUNCTION |
|---|---|
| 1 | Safety Ground |
| 2 | Data Out |
| 3 | Data In |
| 4 | Request to Send |
| 5 | Clear to Send |
| 6 | Data Set Ready |
| 7 | Electronic Ground |
| 8 | Received Signal Detect |
| 14 | Reverse Channel Transmit |
| 16 | Reverse Channel Receive |
| 20 | Data Terminal Ready |
| 22 | Ring Indicator |

## 2-6. INSTALLATION.

To install the 9002 system, first complete all cable connections. Figure 2-2 is a typical interconnection diagram, showing how the system is connected to a telecommunications line via a modem and to optional peripheral devices.

Prior to turning on system power check that the fuse on back of the display enclosure is of the proper rating (2 amps, slo-blo) and is properly installed.

# chapter 3 operation

The functions performed by the 9002 Microcomputer Terminal System are dependent primarily on the program stored in the microcomputer. Therefore, operation of the 9002 system is described in separate documents, related to particular programs and hardware options. Refer to the 9002 Operator's Manual, Part No. 88-402-02 and other documents listed in the Introduction of this manual.

# chapter 4 principles of operation

## 4-1. INTRODUCTION.

This chapter contains information about how the 9002 Microcomputer Terminal System works. First, in Section I the major functional parts of the system are identified, and the overall operation of the system is explained. This includes a description of how the hardware and software function together under the control of the Basic Program and brief overview of the 9002 system software. Then, Section II is a description of the system hardware. It starts with an overall physical and functional description of the system and proceeds to a block diagram level description of each of the major circuits in the system.

## SECTION I

## SYSTEM AND SOFTWARE DESCRIPTION

## 4-1. SYSTEM ARCHITECTURE.

The 9002 system is a general purpose 8-bit microcomputer, with input/output devices and programs that make it suitable either for display, editing, and other handling of various text and forms data, or for use as an intelligent terminal with buffered communication and preprocessing capabilities.

The input/output devices communicate with the microcomputer in 8-bit byte format to either supply or receive data and instructions from the microcomputer. For example, the keyboard inputs data and instructions to the microprocessor, but the CRT display only receives.

Depending on what specific programs are operating the microcomputer, it can perform different processing functions and can communicate with different input/output devices. If the microcomputer is operated by the Basic Program, it can receive data only from the keyboard, perform simple text editing and forms generation tasks, and output results only to the CRT display. If the Extended Text Editor program is addes, the microcomputer can still communicate only with the keyboard and CRT display, but can perform more elaborate text editing functions. If TELCOM is added, the microcomputer can also communicate with the RS-232C interface, through which it can receive and transmit data and instructions – either by character or in a block mode.

Figure 4-1 is a block diagram of the 9002 system, in which the microcomputer, all input/output devices, and other circuitry are shown. Note that in the figure the microcomputer is identified as a separate entity, although its circuits physically share space on circuit boards with input/output circuitry. The microcomputer consists of a microprocessor integrated circuit (with its supporting control circuitry) and ROM/PROM and RAM segments of a system memory. The system memory is described separately in paragraph 4-3.

An important feature of the system architecture is that all input/output devices communicate with the microcomputer via a system bus. This bus is connected directly to the microprocessor (CPU), the microcomputer memory, each of the input/output device interfaces, and various supporting circuits. The bus carries 8 parallel bits of data or instructions, up to 16 bits of microcomputer memory address (also on parallel lines), various internal commands and status signals, and allows any input/output device direct memory access. In addition, the bus also distributes power.

The major function of the system bus is to allow the communication of data between the input/output devices and the microcomputer. Data is usually not communicated from an input/output device directly to the CPU, but rather through the RAM segment of the microcomputer memory. The RAM can be read and written into either by the CPU or any input/output device, simply by requesting a memory cycle, with a memory cycle request signal placed on the system bus.

Any of the input/output device interface circuits, or the microcomputer, can request a memory cycle, but the requests are ordered in priority in the sequence shown in Table 4-1. The list in Table 4-1 shows that the microcomputer circuits always have the two highest priorities, but among the input/output devices the CRT display has the highest (because of the real time requirements of the

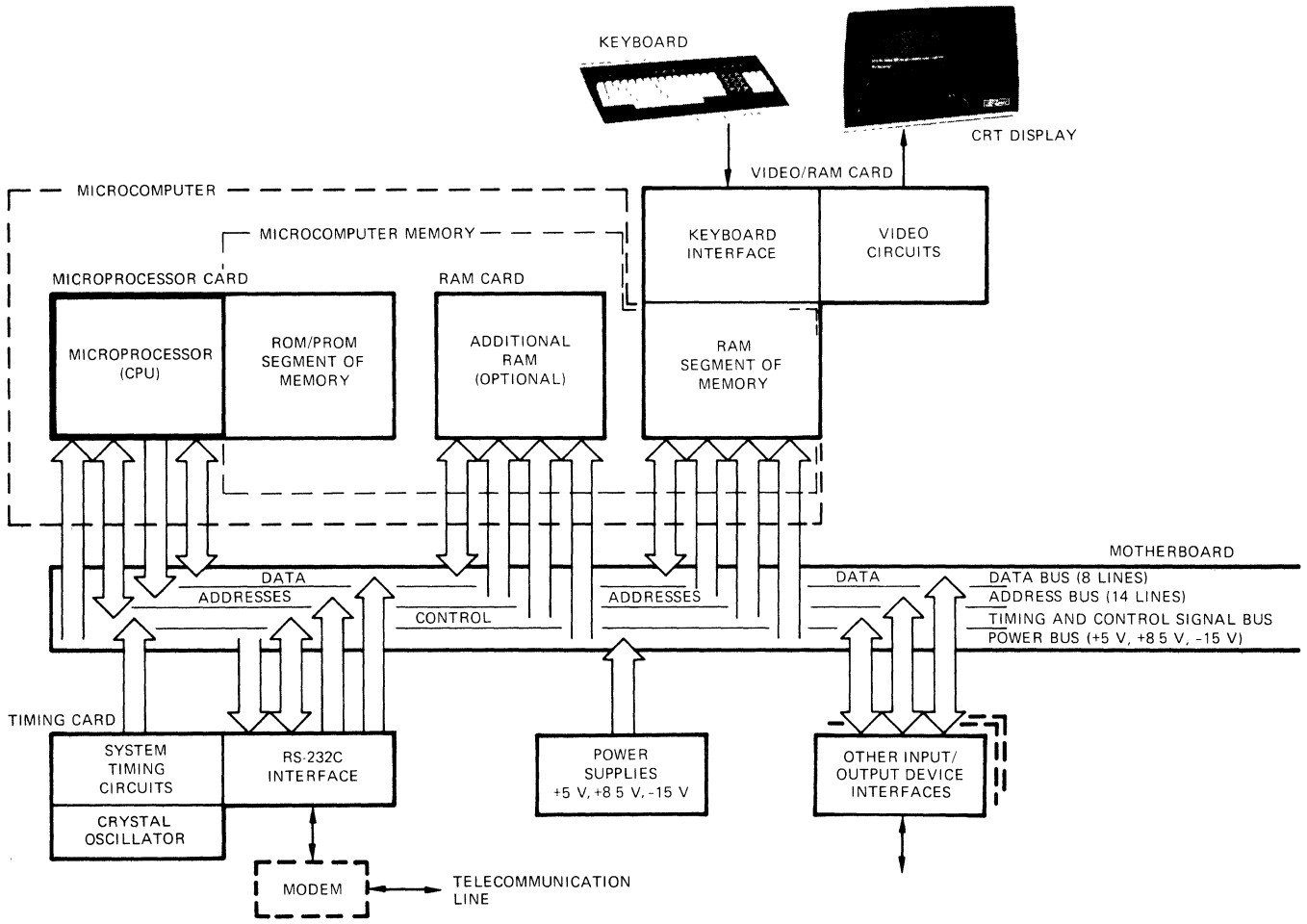



Figure 4-1. Block Diagram of 9002 System.

Table 4-1. RAM Access Priority List

| PRIORITY | FUNCTION AND SOURCE OF REQUEST |
|---|---|
| 1 | CPU (Microprocessor Card) |
| 2 | RAM Refresh (System Timing Circuits) |
| 3 | Video Refresh, including keyboard input (Video Circuits) |
| 4, 5, etc. | All Peripheral Devices (each peripheral device generates its own RAM cycle request; all requests are ordered by card positions, as described in Chapter 2.) |

moving electron beam in the CRT tube). If optional input/output devices are installed, their priorities can be ordered by the positions in which circuit cards are installed within the circuit chassis of the display console (refer to Chapter 6).

Among the input/output devices, the keyboard inputs 8-bit bytes of standard ASCII coded alphanumeric or control character data in a serial manner, in response to the operator depressing a key on the keyboard. This data is entered along with a strobe signal into the keyboard interface circuit and from there into the RAM segment of the system memory, where it is available to the microcomputer for processing.

As the microprocessor completes a data processing sequence, under the Basic Program control (as well as under the control of most other programs), it writes an ASCII coded alphanumeric character and control information back into the RAM for display on the CRT display screen. The video circuits repeatedly read this information out of the RAM, convert the ASCII coded character into a video signal, use the control information to determine the location at which the character is to be displayed on the screen, and output a composite video signal to the CRT display.

The RS-232C interface operates under the control of the TELCOM programs. The circuit communicates data between an external telecommunications line and the RAM. In the receive mode, it receives serial data from the telecommunications line and writes 8-bit bytes into the RAM, but in the transmit mode it reads 8-bit bytes out of the RAM and supplies data serially to the telecommunications line. The RS-232C interface can operate either in a single character or block transfer mode.

Other input/output devices, provided either by Zentec or by the user, can be connected to the system bus through appropriate interface circuits. Such devices can also communicate directly with the RAM, subject to the memory access priority scheme. Some devices, such as the optional hard copy printer, or the

disc memory, use the direct input/output provisions of the microprocessor circuit and bypass the RAM entirely.

In addition to the microcomputer, input/output devices, and the system bus, there are also system timing circuits and power supplies. There are circuits that do not become directly involved in data handling and therefore are described in Section II of this chapter.

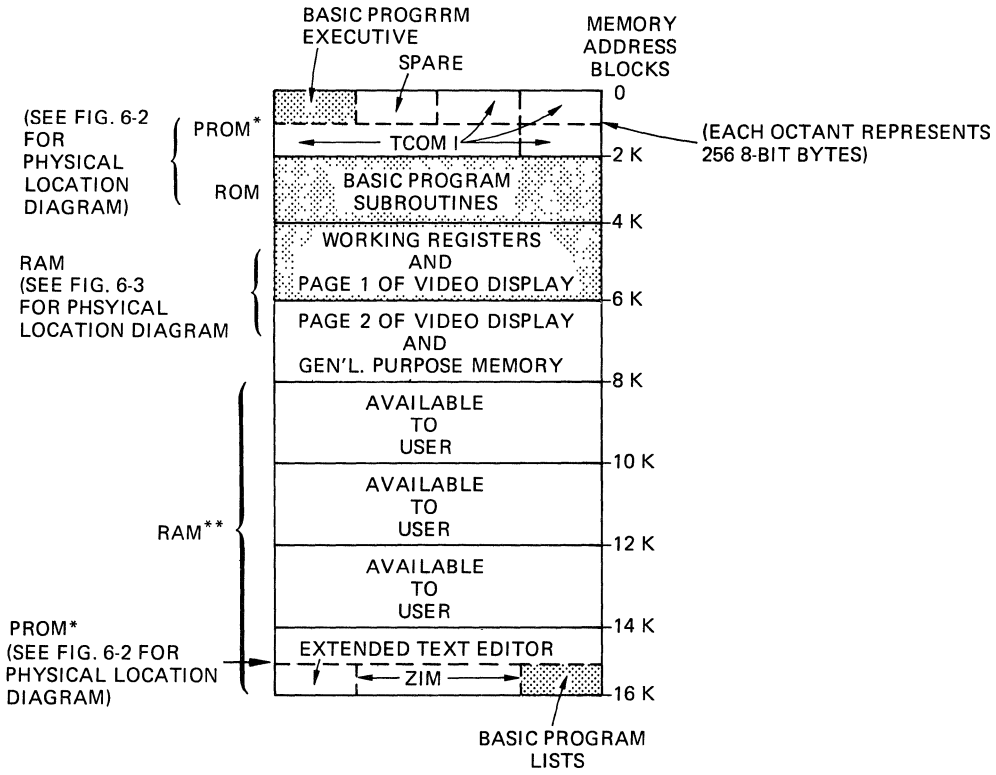
## 4-3. SYSTEM MEMORY.

The 9002 system memory consists of groups of integrated circuits, located on the microprocessor card, on the video/RAM card, and on the optional RAM card (if the latter is installed in the system). These circuits include read/write RAM, ROM, and PROM types, in various combinations, depending on the exact size and program content of the memory. The RAM circuits are dynamic 2048 x 1 bit type, with eight integrated circuits connected in parallel for reading and writing 8-bit words. The ROMs are 2048 x 8 bit factory mask programmed type, and the PROMs are 256 x 8 bit erasable and field programmable.

The 9002 memory is organized into two major segments: a read-only (ROM/PROM) segment, and a read/write (RAM) segment (see Figure 4-2 and also paragraph 1-5). The ROM/PROM segment is located on the microprocessor card and its sole function is to store programs for the microprocessor, but the RAM segment is on the video/RAM card and it stores data to be displayed on the video screen, provides various working registers (that are utilized both by the operating program and the input/output hardware circuits), and also provides general purpose memory for user applications.

For addressing purposes the overall memory is divided into 2K (2048) 8-bit byte sections or blocks, as shown in Figure 4-2. The usage of certain 2K memory blocks is preassigned at the factory to conform to the assembly sequence of the Basic Program and other programs, but all other blocks can be assigned by the user. Address lines of the factory preassigned memory blocks are generally hardwired (by traces on the circuit boards), but other locations can be assigned by the user by means of wiring solderable straps on the circuit boards (see Chapter 6). Thus, the 9002 system memory provides considerable flexibility to the user in utilizing available memory space.

The exact size of the system memory can vary up to a maximum of 16K, as shown in Figure 4-2, and depends on several factors. If only the Basic Program is stored in the system and there are no options, there must be a minimum of 2550 bytes of ROM and PROM and 2048 bytes of RAM. As soon as optional programs, video display memory, or hardware options are added, the size must increase, as shown in Figure 4-2. The maximum size is 16K (16,384) bytes, because that is the upper limit of the direct addressing capability of the CPU.




*Note: Shaded areas are used by the Basic program; their locations are pre-assigned at the factory and thus are not available to the user.*

**This segment can be either PROM or ROM, as long as the integrated circuits are electrically interchangeable The factory installed type is shown here.*

***These segments (located on the optional RAM board) can also be ROM or PROM, provided physical space on the microprocessor board is available.*

Figure 4-2. Typical Map of the 9002 System Memory

Accessing of the system memory is either via the system bus or directly by the CPU. In the case of the ROM/PROM segment, which stores only CPU programs, accessing is done directly, without involving the system bus. This segment cannot be accessed to be read by any of the input/output devices, except through the CPU, by means of special programs designed for the purpose. The RAM segment can be accessed either by the CPU or by input/output devices, but always only via the system bus.

To access any memory location a 14-bit address must be used. This address is partially partially by each memory circuit and partially by decoding circuitry on each circuit card. One noteworthy feature is that under certain circumstances two memory locations can be accessed simultaneously. This occurs when the CPU is reading the ROM/PROM segment. The memory address is routed directly from the CPU to the ROM/PROM segment, but is not placed onto the system bus. Therefore, the bus is available and can be used simultaneously by an input/output device to read or write anywhere in the RAM.

## 4-4. SYSTEM OPERATION.

To access any memory location a 14-bit address must be used. This address is decoded how the software and hardware in the system interface and interact. To make such an analysis, the 9002 system may be considered to consist of the data input/output interface hardware, the microprocessor with its software, and the RAM, as shown in Figure 4-3. Because internal operation of the microprocessor is entirely under the control of its operating program, the microprocessor and its program can together be generally referred to as the software section of the system. On the other hand, the input/output interface circuits, together with the keyboard, the CRT monitor, and any peripherals, can be referred to as the hardware of the system; they operate without the direct intervention of the program.

The RAM functions as a physical interface between hardware and software. It consists of hardware and software registers (together referred to as the working registers) and a video display section. It can be accessed via the system bus either by the microcomputer or by the input/output hardware and thus effects a separation between the two – in the same manner as the input/output unit does in any general purpose computer system. This separation of hardware and software functions is a basic part of the 9002 system design and the scheduling of RAM access time distribution among the microcomputer and all input/output hardware devices plays an important part in the system operation and servicing of input/output devices.

To describe the 9002 system operation, we will first analyze the sequence in which hardware and software function to process a typical input from an I/O device and then direct our attention to the details of the system bus usage. After that, the RAM and its working registers will be described in detail.

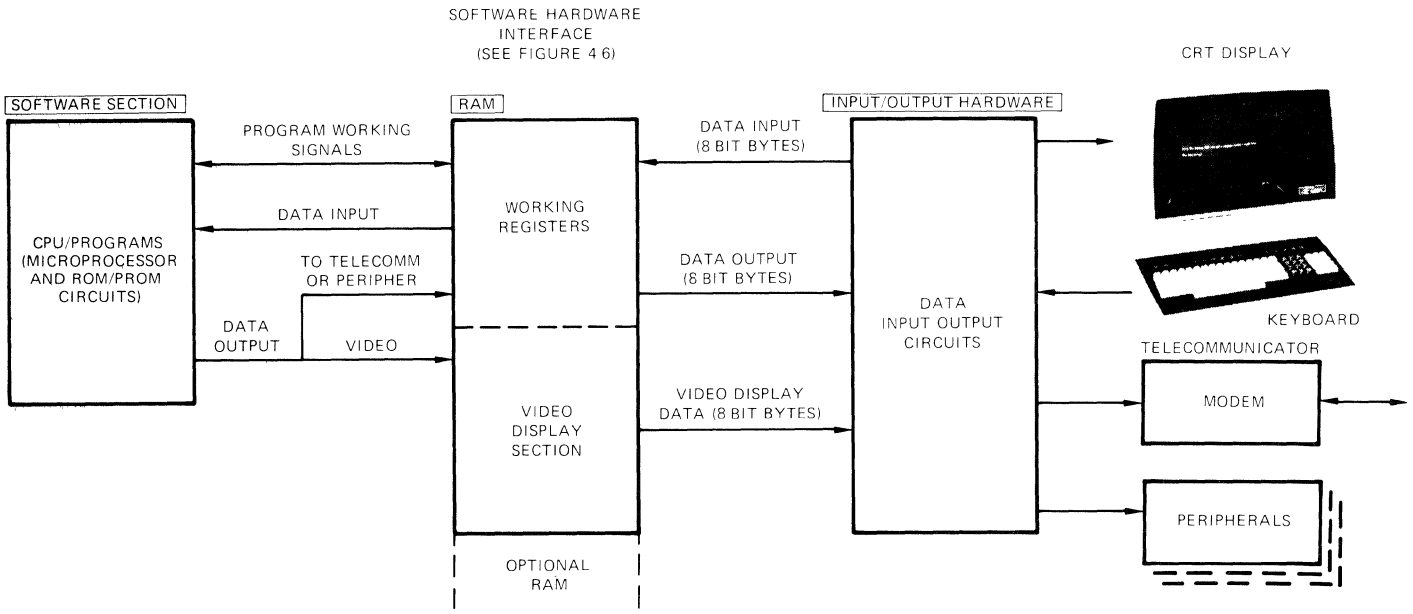



Figure 4-3. Diagram of Operational Sections of the 9002 System

## 4-5. DATA INPUT/OUTPUT AND PROCESSING SEQUENCE.

To describe the operation of the 9002 system software section, the input/output hardware, and the RAM, the path of a character, generated on the keyboard, is analyzed in this paragraph. This analysis is typical of input/output and processing operations, and demonstrates how software and hardware interact in the system. Note that the sequence described in this paragraph is specifically as it occurs under the control of the Basic Program. Refer to Figure 4-4.

When a key is depressed on the keyboard, it causes a keyboard encoder circuit to output an 8-bit code – in ASCII format. This 8-bit code is buffer stored in the keyboard interface circuit and from there written into a keyboard input register in the RAM. The RAM location is periodically monitored by the microprocessor, under control of the Basic Program. The character is fetched by the microprocessor circuits and its processing is started. From there on, until the results have been loaded back into the RAM, processing is entirely

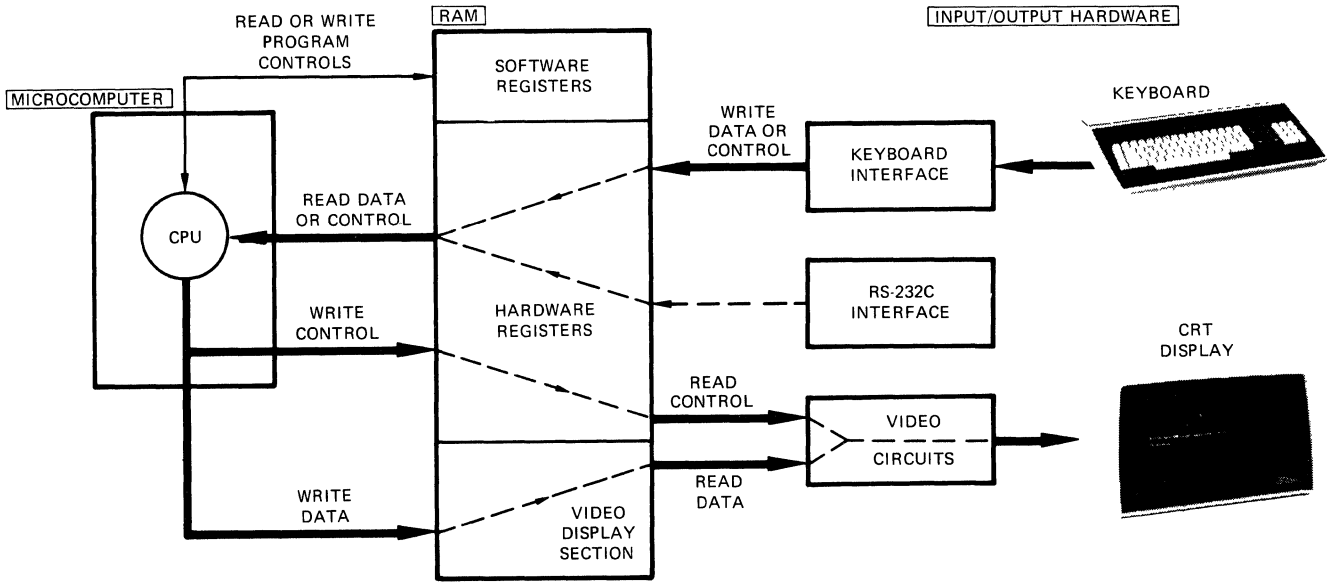



Figure 4-4. Diagram of the Path of a Typical Data Character in the 9002 System

under the control of the Basic Program and proceeds in the sequence described in paragraph 4-18 below.

If the keyboard entry is a data character – any one of 96 ASCII letters of the alphabet, numerals, punctuation marks, or symbols – the results of its processing are displayed on the screen. To accomplish this, the ASCII code is loaded by the microprocessor into the video display section of the RAM, at a location corresponding to where the cursor appears on the screen at that instant. This RAM location, along with all others in the video display section, is periodically read by the video circuitry, translated into a video signal and displayed as a dot pattern on the CRT display screen. Note that loading of the displayable character into the RAM is a software function, but reading it out and all subsequent functions associated with displaying it are hardware performed.

Instead of the 96 basic ASCII characters, the keyboard entry can also be any one of the 32 control characters (or selected variations of the 32). A control character may be associated with relocation of the cursor, moving or erasure of a display segment on the screen, selection of the operating mode or submode of the system, etc. In these instances processing of the keyboard character can have varied

results. For example, if the control character is a command to erase the entire screen, the microprocessor will load blank characters in all locations of the display section of the RAM and also change the cursor location address in the hardware registers to the value for home position. Then, during the next video refresh cycle, the input/output circuitry will pick up this revised information, display a blank screen and the cursor at home position.

If, on the other hand, the control character is a command to change the operating mode of the system, the microprocessor may not output any revised information to the display sections or hardware registers of the RAM at all (except display information for the 25th line on the screen). Instead, the mode change may simply cause the microprocessor program to store a new code in a software register. This new code then, can cause subsequent keyboard inputs to be handled in a different manner, as required by the new mode.

The above sequence describes the processing of a keyboard input under the Basic program, but it actually is typical of handling data inputs from the RS-232C interface, or other peripheral devices under the control of their respective programs. If more than one input/output device is attached to the system bus, several data input registers are utilized in the RAM to receive the data. One data register is assigned to receive an 8-bit character from each of the peripherals and the microprocessor then samples all input registers in sequence. As in the case of the RS-232C interface, the data input/output protocol may also require a flag bit and the communication of status and command words, but the general principles are the same. (The RS-232C interface actually uses two registers for data input and two for data output, as described in paragraph 4-14 below.)

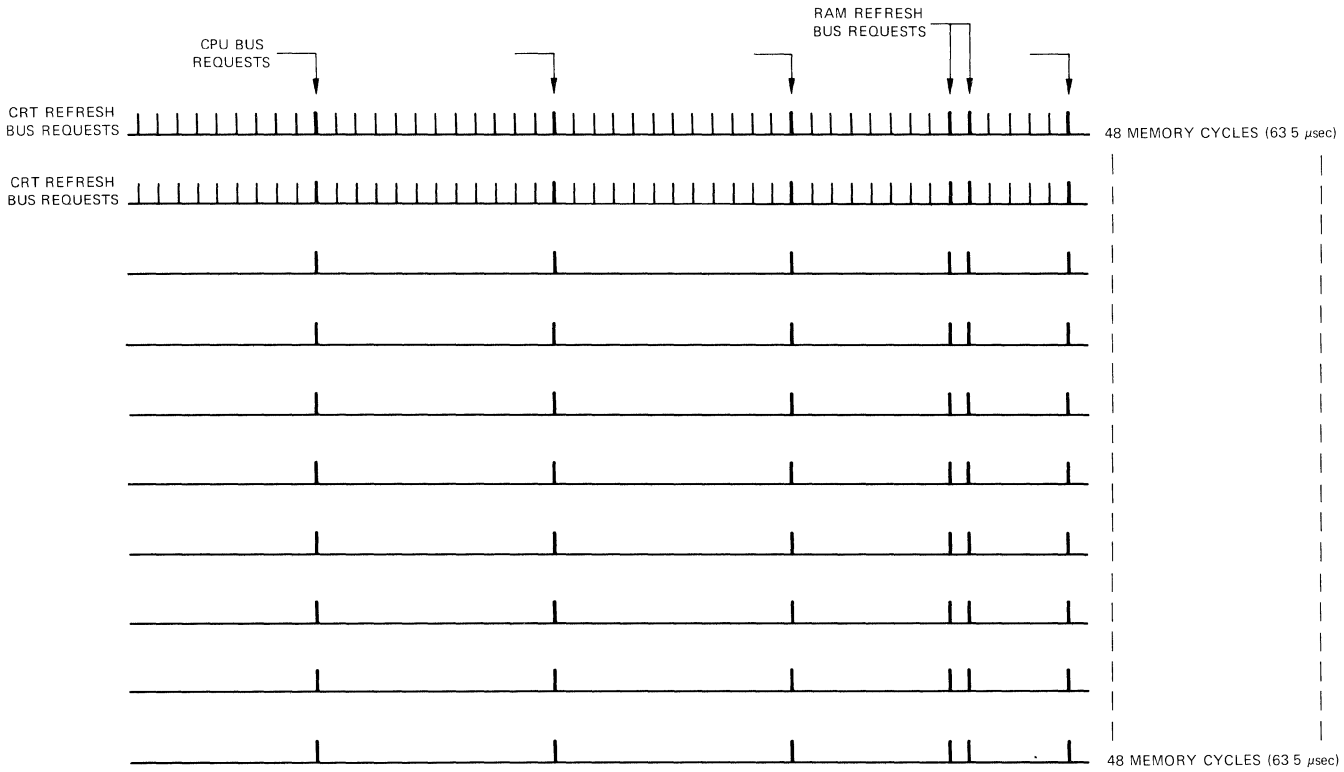
Some exceptions to the data input and output methods arise when communicating with some high speed peripheral interfaces, such as those of the disc memory or printer options; these are described separately, in documentation supplied with the options.

## 4-6. SYSTEM BUS USAGE.

One important aspect of the data input/output and processing sequence described in paragraph 4-5 above is the allotment of memory cycles on the system bus. This is important both for the understanding of how the 9002 system operates and for programming the system.

The system is designed so that the CPU can obtain a memory cycle at any time (see Table 4-1), in order to maximize the CPU thruput rate. However, the refreshing of the dynamic RAM circuits and the refreshing of the CRT display screen both present real-time requirements, which must receive a predetermined number of memory cycles during a certain time period and cannot conflict with CPU cycle requirements. In addition, enough additional memory cycles must be available to service all input/output devices connected to the system bus.

To satisfy all of the above requirements, several accommodations in the hardware design have been made. First, the RAM segment of the system memory is cycled at approximately 12 times the rate of the CPU. This means that for every cycle that the CPU is able to use, there are 11 other cycles available for other devices. Second, there are specific design characteristics of the video circuits that help to minimize the RAM read time required for CRT refresh and allow this reading to occur earlier or later during any given time period. These design characteristics are discussed in more detail in Section II of this chapter but the net result is shown in Figure 4-5.




*Note: Each line represents the time period of one typical CRT scan line (including horizontal retrace); the set of ten lines represent one display row.*

Figure 4-5. Diagram of the RAM Memory Cycle Allotments on the System Bus

In this figure the division of a typical 635 microsecond time period into ten equal segments, each corresponding to the length of one scan line by the CRT electron beam, is shown. Because the RAM memory cycle is 1.3 microseconds long, each scan line period represents 48 memory cycles that can be allotted to all devices connected to the system bus.

During each scan line period the CPU can access the RAM no more than four times, as shown in the figure. The RAM refresh circuitry is designed to use up two more memory cycles out of every scan line, thus leaving 42 memory cycles for all other devices.

The CRT refresh requirements are such that 80 memory cycles are needed during every ten scan line period, to read out the data for one row of display. The video circuits can be allotted these 80 cycles anytime during the first nine scan lines, but in fact it always occurs during the first two scan lines. (There are 96 memory cycles in two scan lines; the CPU and RAM refresh requires six cycles during each scan line, together 12, the CRT refresh requires 80, for a total of 92 memory cycles during all of the first two scan lines.)

As a result of the above allotments, there are at least 42 memory cycles available during each of eight scan line periods, in every ten scan line time intervals. In fact, the CPU cannot on the average require as many as four memory cycles out of every 48, because many of the program subroutines that it must carry out are more than 12 memory cycles long. Also, whenever the CPU reads out of the ROM/PROM segment of the system memory, which is physically located on the same circuit card with the CPU, it reads directly, without using the system bus. Consequently, during these read operations the system bus can be used by another device to read or write into the RAM. That is, under certain conditions two simultaneous memory accesses can occur in the 9002 system.

Another minor exception occurs at the beginning of every video field (every 60th of a second). At this time six additional memory cycles are required to establish various conditions for the entire video field. For example the cursor location, any special display effects, RAM address of the first row of characters to be displayed on the screen, and other prerequisite information is read out of the RAM.

## 4-7. SOFTWARE/HARDWARE INTERFACE.

The software/hardware interface, represented by one section of RAM, serves an important function, because it allows the microprocessor and the input/output hardware to perform their internal operations independently of each other. It allows the microprocessor to use different programs to perform different data processing functions, while the basic functions and operation patterns of the input/output hardware must remain fixed by its circuitry. It also allows the microprocessor and hardware to operate at their own clock rates, without direct timing synchronization between the two. The only communication between the

software and hardware is through the RAM, which can be accessed via the system bus, virtually at any time. Thus, as long as both the microprocessor and the input/output hardware observe the system bus protocol and RAM data register location preassignments, they can operate independently of each other in all other respects.

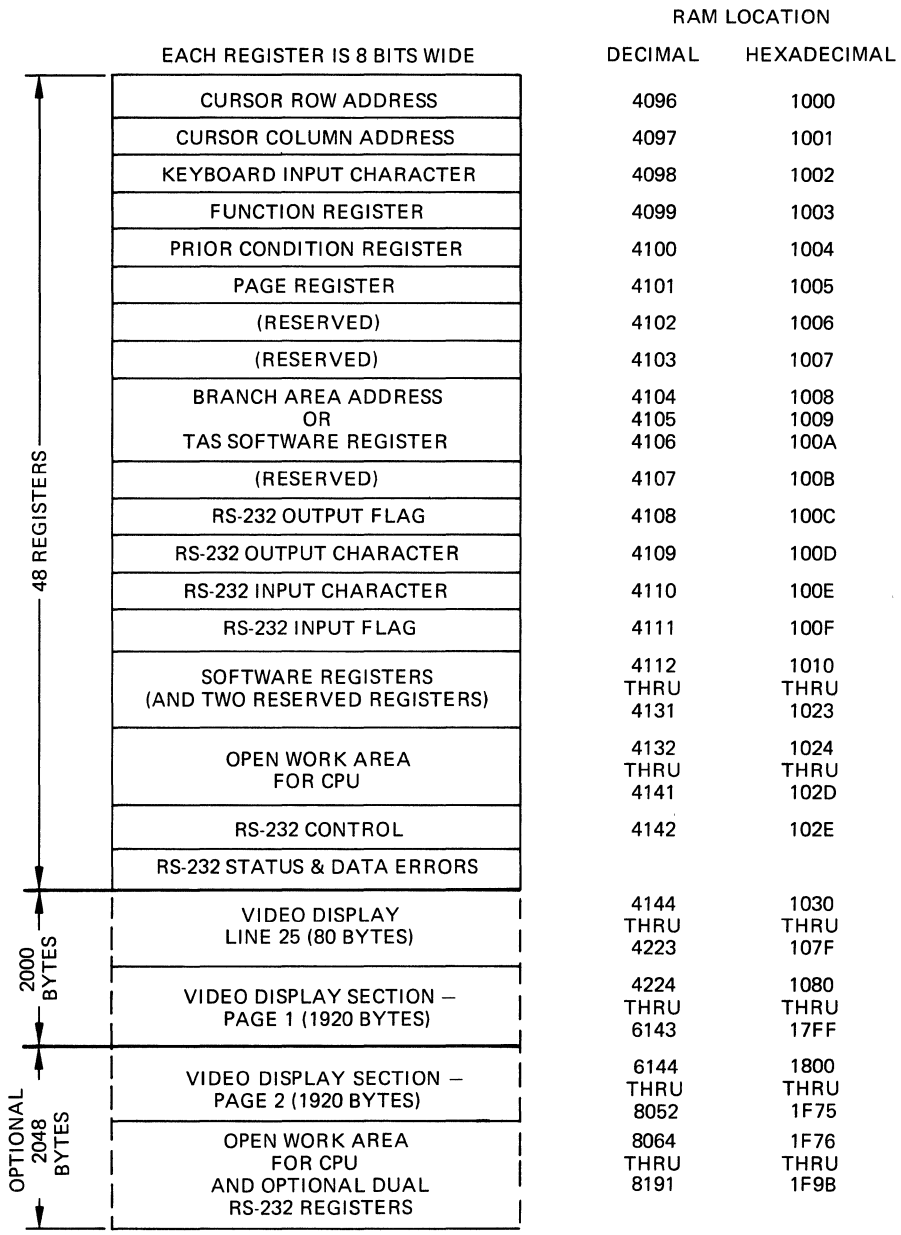
The RAM is a segment of the 9002 system memory, described in paragraph 4-3. It consists of 48 8-bit working registers and 2000 bytes (also 8 bits each) of memory space for video display information, as shown in Figures 4-3 and 4-6. If programs other than Basic Program are installed in the system, and the page two video option is installed, the RAM can expand to 4096 bytes. Together, the working registers and the video display section constitute the software/hardware interface.

## 4-8. WORKING REGISTERS.

The working registers are 8-bits wide and all are located in the RAM. They include two types – software registers and hardware registers. Software registers hold information used actively by the CPU during data processing, but their contents are not accessible to any other circuits. For example, the current operating mode is identified by one register, the current cursor address by two other registers, and program branching addresses occupy three registers. There are a total of 23 software registers, 13 of which have assigned functions in the Basic Program and the remaining 10 are unnamed temporary work spaces for the CPU. The software registers derive their name from the fact that they are written into and read out only by the CPU.

Hardware registers are also written into and read out by the CPU, but their main usage is in communication with input/output hardware. Typically, the CPU stores in a hardware register the results of some data processing routine which is then read and interpreted by a hardware circuit as an instruction to perform a specific task. Alternatively, a hardware circuit writes data into a register and the CPU fetches the data and processes it. For example, a 2-byte register is used to communicate the current cursor column and row addresses, from the CPU to the video circuits, a single-byte register is used by the CPU to actuate the audible tone alarm circuit, and a single byte register is used to receive data from the keyboard for the CPU to process.

Because software registers relate only to the microprocessor and its programs, they are described in more detail in the Programmer's Language Manual, Zentec Part No. 88-403-01. Hardware registers relate to both the software as well as hardware and therefore are described, along with the video display section of the system memory, in the following paragraphs 4-9 through 4-15. Note that because hexadecimal notation is used in 9002 system programs, RAM locations and other numerical quantities are usually expressed in hexadecimal notation, rather than decimal. Every hexadecimal number is either preceded by the letter X or in some other way identified as hexadecimal. Example: decimal 4096 = X1000.




**Not used by the Basic Program or any of the optional programs listed in this manual.*

Figure 4-6. Diagram of Working Registers and Video Display Section Registers

**4-9. Cursor Address Registers.** There are two cursor address registers that identify the locations of the cursor on the CRT display screen. One register, at location 4096 (X1000), identifies the cursor row and the other, at location 4097 (X1001), identifies the cursor column.

The cursor address registers are always loaded by the microprocessor and are read by the video circuits. The values contained in the two registers are derived by the CPU from the contents of the FAS software registers and can range from X00 to X19 for the row address register and X00 to X 4F for the column address. If the system contains the Page Two Video Display Option, row addresses can extend to X30. Note, however, that row address X00 corresponds to the 25th line on the screen, which is not normally accessible. Row address X01 corresponds to row 1 of the first video display page and column address X00 corresponds to the first column on the left of the screen. From these values on, all addresses are contiguous.

**4-10. Keyboard Input Character Register.** The keyboard input character register always receives data from the keyboard, via the keyboard interface circuit, and always outputs data to the microprocessor. It is located at address X1002 and contains 8 significant bits, as shown in Figure 4-7. There are only 171 different codes that are actually written into the register: 128 standard ASCII alphanumeric characters, punctuation marks, and symbols are defined by the first seven bits, and the eighth bit is used to identify inputs from the numeric pad (11 keys) and 32 codes generated by selected keys while the CTRL key is held depressed (@, A - Z, [, \, ], ^, –).

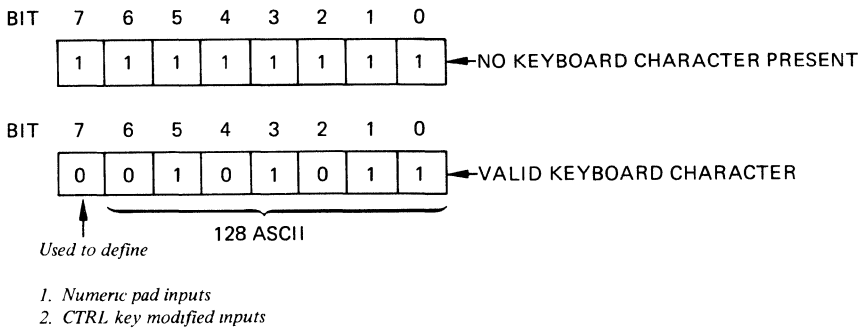



Figure 4-7. Diagram of Keyboard Input Character Register, Location X1002

The register can be loaded asynchronously by the keyboard interface circuit and is monitored periodically by the mciroprocessor. The interface protocol is such that the keyboard is allowed to write any code other than XFF into the register. After the microprocessor reads a valid character code out of the register it writes all 1 bits (XFF) into the register. Thus, when the microprocessor monitors the register, it interprets XFF as the absence of a keyboard character, but any other bit combination is read and processed.

**4-11. Function Register.** The function register has only one use – to actuate the audible tone alarm. The register, located at address X1003, is always loaded by the microprocessor and is read by the video circuits. A tone, approximately two seconds in duration, is produced by this circuit whenever the eighth bit in the function register changes state. That is, whenever the eighth bit changes from 1 to a logic 0 state, or vice versa, the tone alarm circuit is actuated. All other bits in the function register are reserved for program usage, but do not affect the tone alarm circuit.

**4-12. Page Register.** The page register stores the address of that 80-byte segment of the video display section of the RAM which appears as the top line on the CRT screen. The register, located at X1005, is always loaded by the microprocessor and is read once every video scan field by the video circuitry. Its contents must be X01, if there is only one page of video data in the RAM, but can be any number between X01 and X19, if the Page Two option is installed in the system. If the second page option is in the system, the page register is also used for scrolling. In this case, it can contain any value between X00 and X19. (Even though it is not of any evident practical value, the page register can also be programmed to contain the address X00, which is the 25th line. In that case the control line is displayed both on top and bottom of the screen.)

**4-13. RS-232C Interface Registers.** There is a total of six hardware registers in the RAM for the purpose of communicating data, control, and status information between the microprocessor and the RS-232C interface circuit (See Figure 4-8). These registers are generally written into and read both by the microprocessor and the RS-232C interface circuit.

The RS-232 input character register at location X100E is used to receive telecommunications data and store it for the microprocessor. Whenever a word is received by the system, the RS-232C interface circuit requests a memory cycle and the word is loaded into the input character register. Immediately thereafter, the RS-232 interface circuit also sets a flag bit in the register at location X100F, to indicate to the CPU that a data word is at location X100E. After the CPU reads the input character register, it resets the flag bit at location X100F.

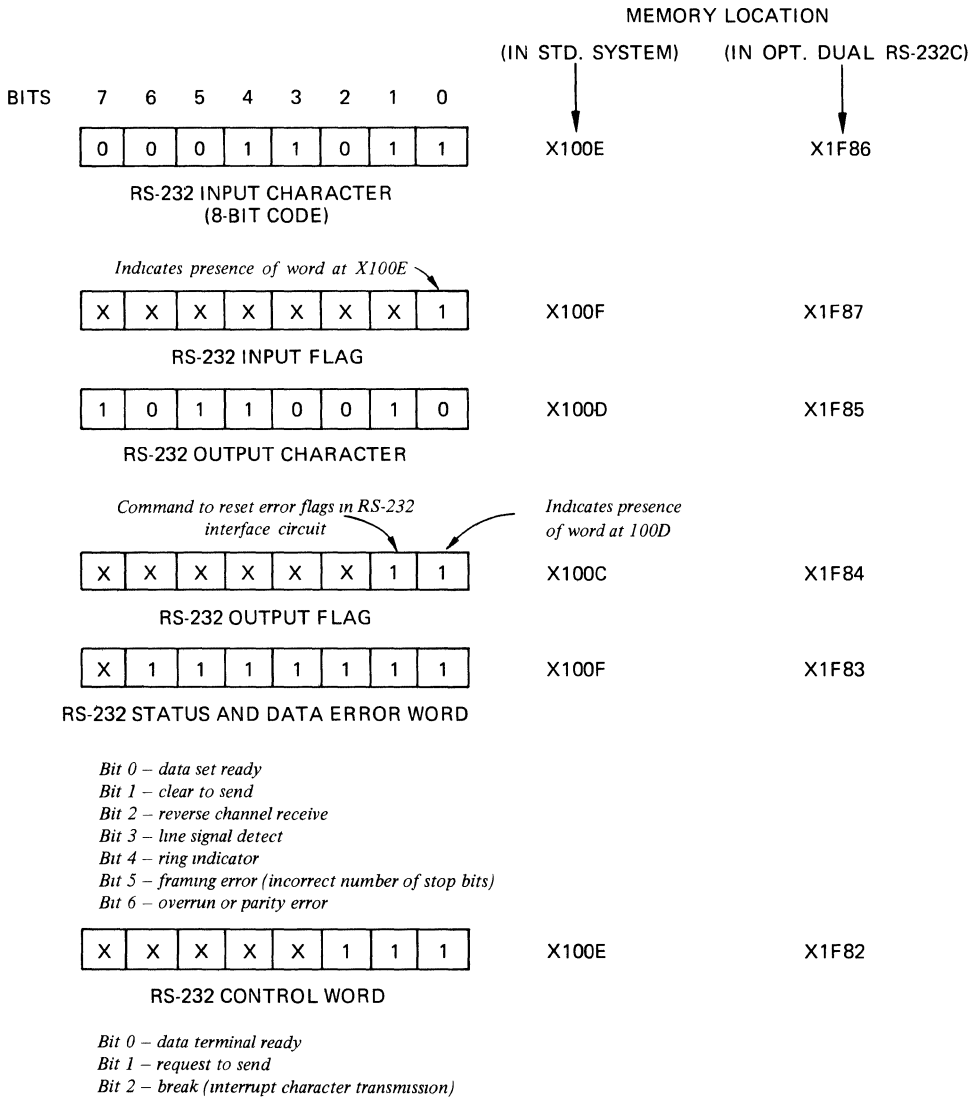



Figure 4-8. RS-232 Interface Registers

A similar protocol is used to transmit data from the CPU to the RS-232C interface circuit. To do this, the CPU writes a data word in the RS-232 output character register at location X100D and sets a flag bit at X100C. When the UART in the RS-232 interface circuit reads this word, it resets the flag.

The register at location X102F is known as the status word register and contains standard RS-232C interface signals. The status word register is always written into by the CPU and is monitored by the RS-232 interface circuit.

The register at location X102E is known as the control word register and also contains standard RS-232C interface signals. It is always set by the RS-232C interface circuit and is monitored by the CPU.

## 4-14. OPTIONAL DUAL RS-232C INTERFACE REGISTERS.

There are six optional dual RS-232C interface registers. These registers are present in the 9002 system only if the dual RS-232 option is installed. In that case, the registers are located in the added 2K RAM section, in the locations shown in Figure 4-6. Their functions are identical to those of the basic RS-232C interface registers described in paragraph 4-13 and shown in Figure 4-8.

## 4-15. VIDEO DISPLAY SECTION.

The video display section of the RAM stores one byte for every character position on the screen. Whenever a displayable character or special display effects control code is entered from the keyboard (or another source), the CPU processes that character and writes it in the video display section. From there, it is read out periodically by the video circuitry, transformed into a video signal and displayed on the screen of the CRT display. Thus, the CPU writes into the video display section, as needed to alter the display image, but the video circuitry continuously reads it out.

In the video display section there is space for a total of 1920 bytes of data representing the 80 characters on each of 24 display lines. An additional 80 bytes are reserved for the 25th line, which identifies the current operating mode (See Figure 4-6). Thus, one page of video display information occupies 2000 bytes of space in the RAM. The Page Two option requires only 1920 bytes more, because line 25 is common to both pages.

Any byte stored in the video display section of the RAM is interpreted by the video circuits either as a data character or as a control code. If a byte is interpreted as a data character, it is simply displayed on the screen at the cursor location, but if it is a control code, it specifies the special display effect which applies to all following data characters. For example, it can specify that all characters following are to be dimmed, or displayed on a reversed background, etc.

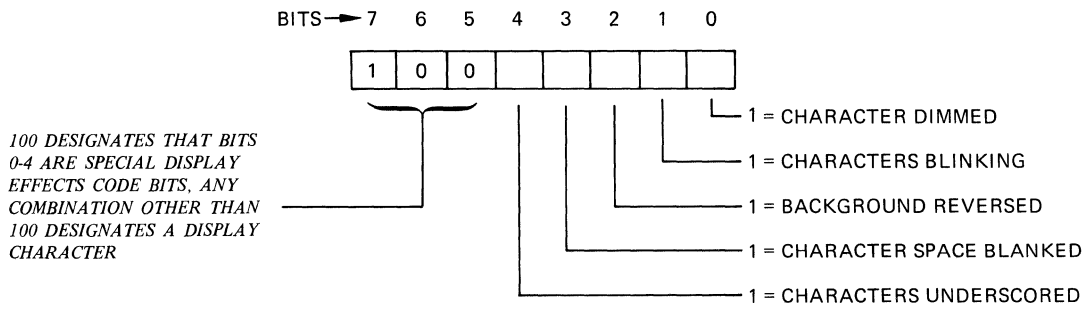
Whether or not any given byte is a control code is determined by its three most significant bits. If bits 7, 6, and 5 and 100, respectively, that byte is interpreted as a control code; if bits 7, 6, and 5 and 5 are any combination other than 100, the word is interpreted as a data character. A control code specifies special display effects for all data characters from that location on until the end of the screen, or until another control character is encountered. Figure 4-9 shows the special display effects code stored in bits 0 through 4.

## 4-16. PROGRAMS.

### 4-17. GENERAL STRUCTURE OF PROGRAMS.

The 9002 system programs are list structured. They are built around a core of closed subroutines, which are always accessed through the lists under the control of an executive (see Figure 4-10). The list structure is a fundamental feature of all 9002 programs; it provides maximum flexibility in expansion of any particular system with optional programs purchased from Zentec, and also allows the user to create his own programs, while making use of the basic subroutines already exising in the 9002 system.

The basic subroutine set is used in the Basic Program. These subroutines allow keyboard entry and display of characters on the CRT screen, erasure of characters and various manipulations required for very basic text editing and forms display. When optional programs are added, the basic subroutines are complemented by other subroutines that enhance some existing capability of the system, or introduce a new one. Likewise, the user can add application oriented subroutines that




*Note: Any of the special display effects can also be combined. All 0 bits in positions 0 thru 4 will cause the display to appear normal.*

Figure 4-9. Special Display Effects Control Code

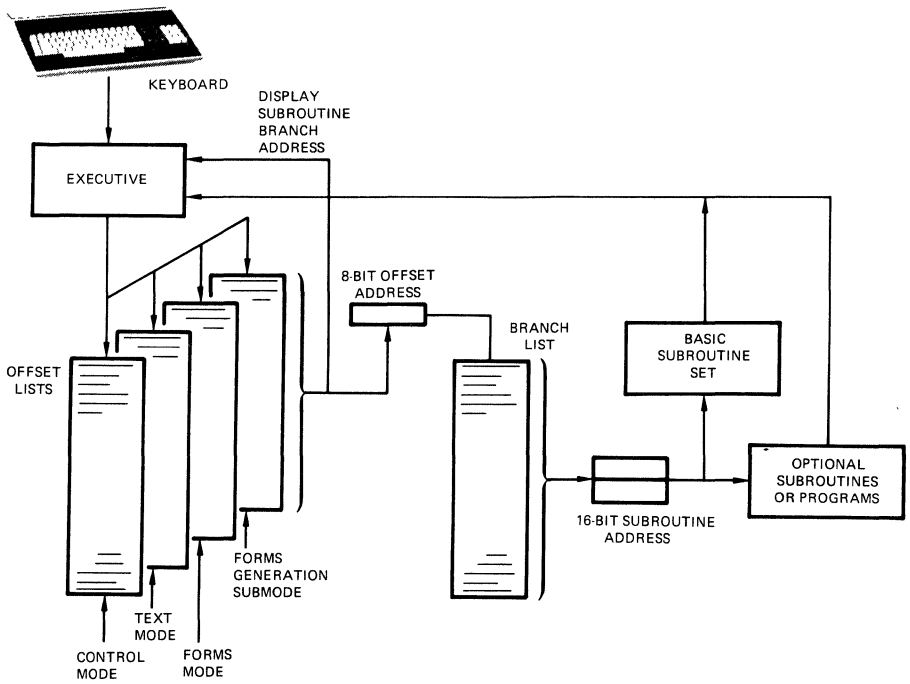



Figure 4-10. Diagram of the 9002 System Program Construction
(Basic Program shown as an example.)

can be used in conjunction with the basic subroutines and those of other programs.

All programs are written in the Zentec Assembler Language and are stored in a ROM/PROM segment of the system memory, described in paragraph 4-3. The basic subroutines are stored in a 2048-byte ROM, while the lists and an executive are stored in 256-byte PROMs. Therefore, to expand or modify the Basic Program PROMs can be added, or replaced with others, while leaving the basic subroutines intact. The PROMs can be used as needed to add new subroutines, altered lists, etc. Figure 6-2 is a physical map of the ROM/PROM segment of the system memory.

Note that hexadecimal notation is used in all 9002 system programs. In this manual every hexadecimal number is preceded by X, to differentiate it from decimal numbers.

## 4-18. BASIC PROGRAM.

All programs in the 9002 system library are constructed in a similar manner. Therefore, the following description of the Basic Program is typical of all other programs also. This description identifies the major functional parts of the Basic Program and follows through the primary sequence of its execution. For more details and specific information for programmers, refer to the Program Logic Manual, Zentec Part No. 88-403-01.

The 9002 system Basic Program consists of several parts, each of which functions at various times in controlling the microprocessor. The parts of the Basic Program are: a group of closed subroutines, five offset lists and one branch list, and an executive. Each major part carries out specific tasks, in response to an input from the keyboard; the sequence of tasks is ordered as shown in Figure 4-4 and explained below.

After a character is input from the keyboard into the RAM, it is initially transferred into the microprocessor and held, in preparation for accessing one of the offset lists. There are four offset lists – one for each of the three operating modes of Basic Program and one separate list for forms generation submode. Each list consists of 33 addresses, organized so that each of 32 addresses corresponds to one of the 32 basic keyboard control characters and the 33rd address corresponds to all of the 96 alphanumeric and symbol characters as a group. The executive determines which of the offset lists is to be accessed, and then uses the keyboard character in the microprocessor to locate the corresponding address in that list.

If the keyboard character is one of the 96 alphanumeric or symbol characters, the offset list address causes branching to a display subroutine contained within the executive (this is the only subroutine contained within the executive). This subroutine transfers the character into the display section of the RAM and thus completes the software processing. Note that in this simple character display

routine the basic subroutines stored in the ROM do not even become involved.

If, on the other hand, the keyboard character is one of the 32 control characters, the address obtained from the offset list is used to locate another address in the branch list. To do this, the offset list address is added to the starting location of the branch list and in this manner a two-byte (16-bit) subroutine address is located within the branch list. The subroutine address is loaded into the microprocessor and a call is performed into the subroutine itself. In this case the call can be into any of the subroutines stored in the ROM, corresponding to the control code input from the keyboard. Note also that any subroutine may itself serve as a further branching point into other subordinate subroutines, or even whole programs. After the subroutine is accessed and its tasks are completed, it automatically returns program control to the executive. In the absence of another input from the keyboard, the executive repeatedly monitors the keyboard input register in the RAM. If it does find a valid character it loads that character into the microprocessor and begins processing again. It also loads a XFF into the keyboard register. This code then acts as a program instruction to cause the microprocessor to cycle and monitor the register continuously.

## SECTION II

## SYSTEM HARDWARE

### 4-19. DESCRIPTION OF SYSTEM COMPONENTS.

All 9002 system components are contained within the display console and the keyboard unit. The display console, Figure 4-11, consists of a circuit card chassis with three circuit cards, three power supplies, and the CRT display. In addition, there is a rear connector panel, to which a cooling fan assembly and a small speaker are attached. All display console components are mounted on a common chassis and are covered by a two-part enclosure – one part forms the top, sides, and rear of the console and the other is a faceplate.

The three circuit cards within the display console (see Figure 4-11) are:

- the microprocessor card
- the video/RAM card
- the system timing card

They are interconnected by a common motherboard which also is connected to the power supplies, the CRT display, and the rear connector panel.

The microprocessor card has the microprocessor integrated circuit with various control, timing and data routing circuits on it, along with all integrated circuits that constitute the ROM/PROM segment of the system memory. The video/RAM card consists of the video circuits, which generate a video signal for the CRT display, the keyboard interface circuits, and the RAM segment of the system memory, along with the read, write, and addressing circuits for the RAM. The system timing card has a crystal oscillator on it, from which timing reference signals are derived for the entire system. To derive these signals there are counter and decoding circuits on the system timing card. In addition, the RS-232C interface circuits and the keyboard audio response circuits are located on the system timing card also. The system block diagram in Figure 4-1 shows the major functions on all three circuit cards and in the remaining part of this chapter the circuits are described in more detail.

The three power supplies in the display console provide operating voltages of +5V, +8.5V, and –15V to all system circuits.

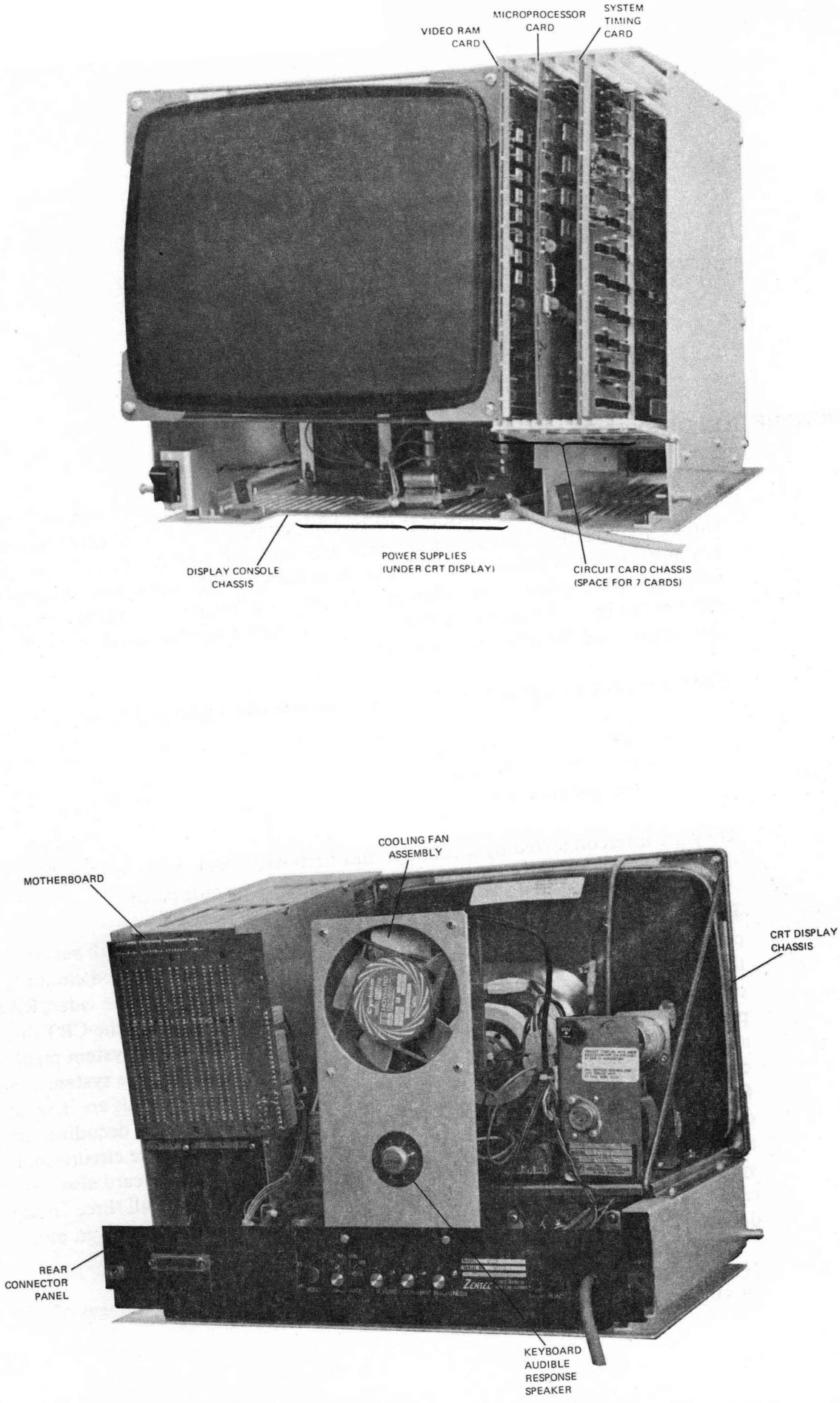



Figure 4-11. Internal Components of the 9002 System

The keyboard consists of an enclosure within which a single circuit card is mounted. The keyboard encoder, along with an oscillator and other circuits, is located on this circuit card. The card also provides mounting space for all keys and has an edge connector to which the cable from the display unit connects. This cable carries all data signals from the keyboard directly to the video/RAM card, as well as power and timing signals.

## 4-20. MICROPROCESSOR AND SUPPORTING CIRCUITS.

The microprocessor (CPU) and its supporting circuits perform all program controlled data processing functions in the system, also read or write into the RAM segment of the system memory, communicate directly with peripheral devices, establish initial microprocessor and program conditions after system power turn-on, and perform other minor functions. This paragraph describes the operation of all microprocessor supporting circuitry, as it relates to the various input and output lines of the microprocessor circuit. The reader, however, needs to be familiar with the internal operation of the microprocessor integrated circuit before reading the following text. (Refer to the 8008 8-Bit Parallel Central Processor Unit User's Manual, November 1974, Intel Corporation, Santa Clara, California 95051.)

Figure 4-12 shows a block diagram of the microprocessor and its supporting circuitry, along with the ROM/PROM segment of the system memory. The various buffer registers shown in Figure 4-12 communicate data or addresses between the microprocessor I/O lines and the system bus. The timing and control logic synchronizes the data, address, and instruction input/output operations with the internal states of the microprocessor operating cycle and outputs various commands to the system bus. The interrupt and initialization logic performs two functions: first, it communicates external interrupt commands from the system bus to the CPU, and the response of the CPU back to the system bus; second, it receives power-up or reset commands initiated by the operator and goes through a countdown and microprocessor instruction input sequence that initializes the microprocessor circuit and its program.

To understand how the microprocessor interacts with its supporting circuitry, five different types of input and output operations must be analyzed. First, consider a typical address and data output to the system bus, during a write operation (write into the RAM). During state T1 of the microprocessor cycle the lower order eight address bits are output by the microprocessor and are loaded into the address buffer register with the T1 load strobe from the timing and control circuits. During state T2, the high order six address bits and two control bits, that define the operation to be a write operation, are output to the address buffer register. These bits are clocked into the register by the timing and control circuits. Then, during state T3, eight bits of data are output by the microprocessor and are loaded into the output data buffer register. Thus, after the T3 time, 14 address bits and 8 data bits are available at the outputs of the buffer registers to be gated out onto the system bus.

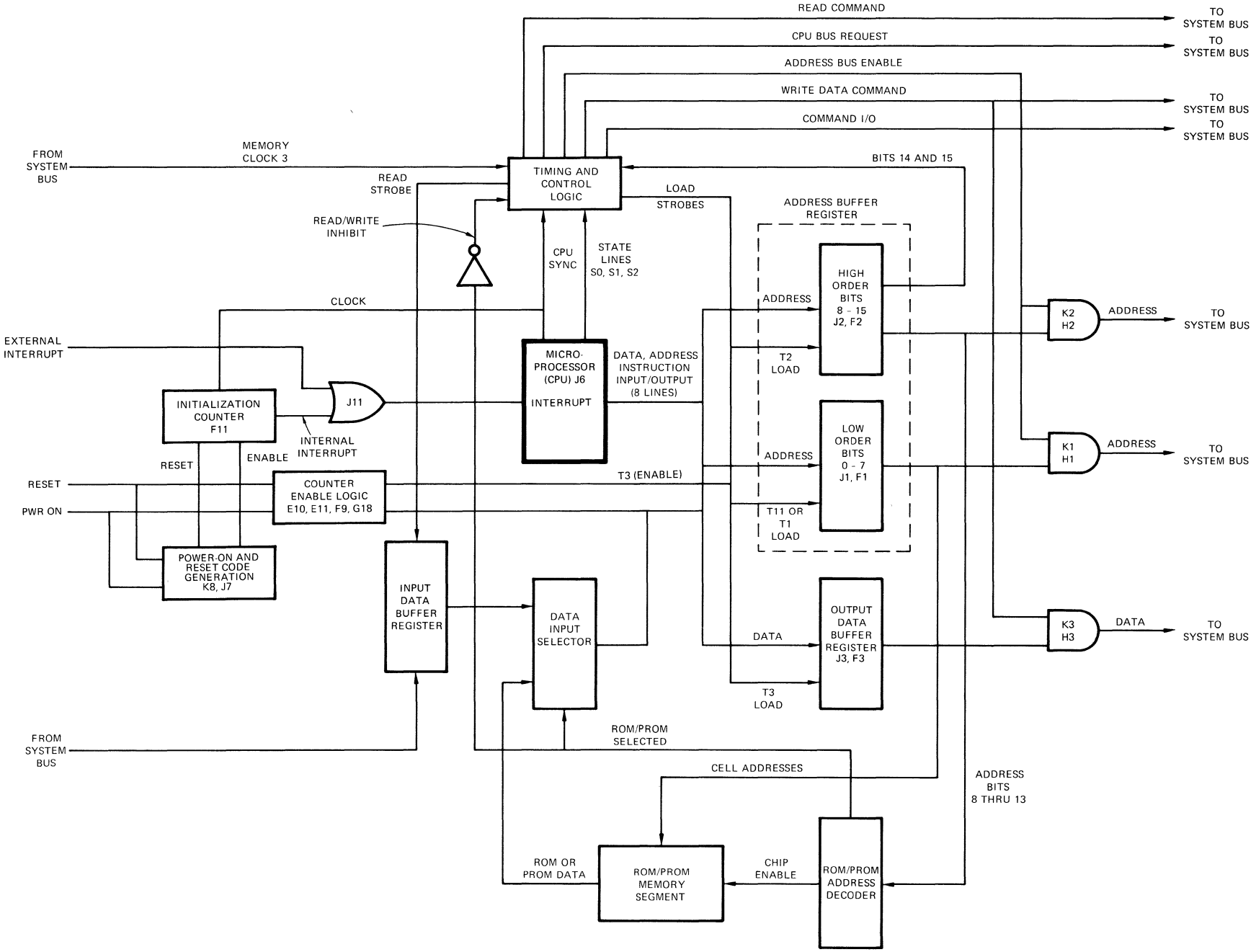



Figure 4-12. Block Diagram of Microprocessor Supporting Circuits

In order to gate the address and data out to the bus, the timing and control logic must supply several signals. After time T2, when the high order address bits are in the address buffer register, bits 14 and 15 are decoded in the timing and control circuits to set a flip-flop that defines the write operation. The setting of the write flip-flop is synchronized with the trailing edge of the system memory clock 3 (the trailing edge defines the end of one memory cycle and the beginning memory cycle. The output of the flip-flop is used to generate a CPU bus request signal, an address bus enable signal and a write data command. These signals are used to gate addresses and data out to the system bus, and the bus request and write commands are output onto the system bus also. This completes a write operation. (Note that the CPU can seize any memory cycle without regard to any other bus requests present on the bus, because it has the highest priority, see Table 4-1.)

When the CPU is performing a read operation, it selects one of two possible sources of data – either the RAM, in which case data comes via the system bus, or the ROM/PROM segment, in which case data is read directly from a ROM or PROM circuit, without use of the system bus. (In fact, while the CPU is reading out of a ROM or PROM, the system bus is available for use by other devices.) The selection between RAM and ROM/PROM is described below.

The start of a read operation is the same as that of a write operation – during T1 and T2 time all address bits are loaded into the address buffer register. In a manner similar to a write operation, bits 14 and 15 are decoded and a read flip-flop is set, synchronous with state T2 signal and with memory clock 3. Concurrent with the decoding of bits 14 and 15, address bits 8 through 13 are supplied to the ROM/PROM address decoder. If these bits are decoded into a ROM or PROM address, a ROM/PROM selected signal is generated. This signal causes the data input selector to switch to the ROM or PROM data line and also causes a gate carrying the output of the read flip-flop to be turned off, so that all normal read operation command signals (CPU bus request, address bus enable, or read command) are inhibited. Instead, the program data from the ROM or PROM circuits is allowed to enter into the CPU.

If bits 8 through 13 are not decoded into a ROM or PROM address, the normal read operation command signals are generated and the address buffer register outputs are gated out onto the system bus, along with the CPU bus request and a read command. In addition, a read strobe is generated and used to load data from the RAM into the input data buffer register. In the absence of the ROM/PROM selection signal, the data input selector allows the system bus data to pass through to the CPU input/output lines. This completes the read operation.

In instances where the CPU must communicate directly with an optional or user installed input/output peripheral device (instead of through the RAM), the command I/O signal is used (it defines the third type of operation). Such a communication can be either a read or a write, but it differs from a normal memory read or write operation. First, the address buffer register is loaded in the normal manner and bits 14 and 15 are decoded during T2 time as a command I/O signal;

this signal is output to the system bus. In the process, the read flip-flop is set and its output causes the address bus enable signal to be generated. This allows the address bits to be gated out onto the system bus and remain active. The read command itself, however, is not allowed to go out onto the bus – it is inhibited by the command I/O signal.

This precludes the reading of the RAM, and instead, the address bits are decoded by any peripheral device that is responsive to the command I/O signal (such as a hard copy printer interface). The address bits contain two or three types of information for the command I/O device. Bits 6 through 11 contain the device identifying code, with which one of several command I/O devices can be activated. Bits 12 and 13 contain the operation code, which informs the command I/O device whether it is to receive data directly from the CPU (output operation) or supply data directly to the CPU (input operation). The command I/O device must respond accordingly throughout T3 time. In the case of an input operation, the I/O device must supply data over the eight data lines of the system bus, but during an output operation the CPU supplies data as bits 0 through 7 of the 14-bit address word.

The fourth type of CPU operation is that associated with an external interrupt. An external interrupt can be generated by any input/output device and causes the CPU to abandon its present program execution and respond to the interrupt on the next CPU cycle. Although this signal is not presently utilized by any of the standard or optional 9002 system input/output devices, the capability exists and therefore is described here.

In response to the external interrupt, the CPU outputs a T1I state signal. The T1I state signal is unique, because it occurs only in response to external interrupts. It takes the place of T1, in that T1 does not occur, and all normal functions that take place during T1 are carried out by the T1I signal. In addition, T1I, synchronized by the CPU sync signal, presets a program interrupt flip-flop, whose output (signal name PINT) is gated out onto the system bus, as an acknowledgement of the interrupt. At this time the originating device must place a program instruction on the system bus, which is gated into the CPU during T3 time and to which the CPU responds. In this manner the CPU operation can be interrupted at any time and the CPU caused to branch to a different program location.

The fifth and last CPU operation is associated with an internal interrupt, which is generated as the result of a system power-on or a manual (operator generated) reset signal. When power is first turned on, a 4-bit initialization counter is reset to zero and then is allowed to count to 15, clocked by the CPU sync signal. During this time, the CPU performs internal initialization, such as clearing of internal memories and the instruction register. After count 15 is reached, the counter overflows and thus generates the internal interrupt signal. As a result, the CPU goes to the T1I state and on to T2 and T3 states. During T3 time, the output of the power-on and reset code generator is entered into the CPU and serves as the first program instruction (it forces the CPU to go to program address 0000). From there on, the Basic Program executive performs erasure of the video display section

of the RAM, a clear of the CRT screen, entry into the REP FORM submode, and other functions that prepare the system for operation.

When the reset signal is input from the keyboard, it likewise starts the initialization counter and allows it to count to 15, to generate an internal interrupt signal. The only significant difference between the power-up and reset sequence is that during the latter the CPU is forced to go to program address 0008. This causes the CPU to skip the erasing of the video display section of the RAM. Instead, reset causes only clearing of the screen and the return to REP FORM submode.

## 4-21. RAM READ AND WRITE CONTROL CIRCUITS.

The RAM is located on the video/RAM card and data can be either written into it, read out, or the RAM cells can be refreshed. Data written into the RAM can come either from the system bus or directly from the keyboard, and data read out can go onto the system bus or directly to the video circuits. During refresh there is no alteration of the contents of the RAM.

To regulate the alternation between read, write, and refresh cycles, as well as to route data to and from the RAM, various data switching and control circuits are used. Together, these circuits are referred to as the RAM read and write control circuits and are illustrated in Figure 4-13. To explain the functions of these circuits each of the three different cycles will be described separately.

During a write data cycle, the three memory clocks, an address, and a write command all must be supplied to the RAM. If the data is coming from the system bus, so must the address. The data input selector circuit and the RAM address selector are used to route the data and an address to the RAM. The upper three bits (11, 12, and 13) of the address lines are decoded to generate a card select signal. This signal is used to gate the three clock signals through the clock gate to the RAM. The write command from the bus is routed through logic gating directly to the RAM.

If keyboard data is to be written into the RAM, the data and address selectors are switched to sense their alternate inputs and the character refresh signal is used to control gating of the clocks. (Note: writing of keyboard data is performed during video refresh cycles, see paragraph 4-27.) The write keyboard data signal is used to generate the write command.

During a read cycle the data output from the RAM can go onto the system bus, or directly to the video signal generating circuitry. If the data is to go onto the bus, a read address is supplied from the bus and is decoded and routed the same as during a write cycle.

The card select signal is again used to gate the clocks through. The read data command from the bus is used to enable the data output gate and thus place the RAM output onto the bus.

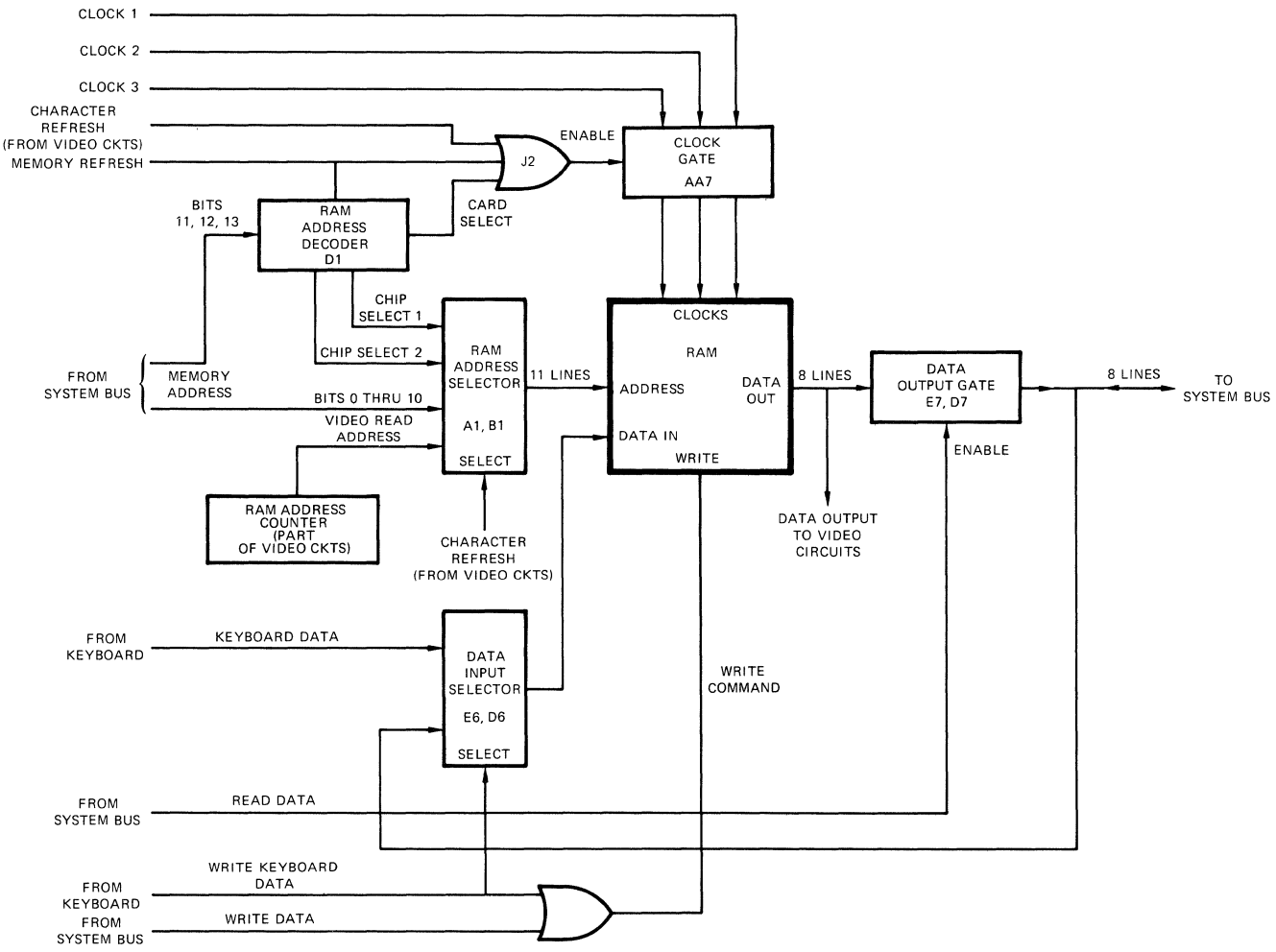



Figure 4-13. Block Diagram of RAM Read and Write Control Circuits

If the data is for the video circuits, the character refresh signal is used to route the RAM address counter output to the RAM, as well as to gate the clock signals. The RAM output is loaded directly into one of the video circuit registers (refer to paragraph 4-27).

During a refresh cycle all data input and output circuits are inactive. Instead, only the clock 3 signal and the lower six bits of the address are required. The memory refresh signal is used to gate clock 3 and the RAM address decoder and RAM address selector are used to route the address bits. Paragraph 4-22 describes how the refresh signals are generated and used during refresh cycles.

## 4-22. SYSTEM TIMING GENERATION AND RAM REFRESH CIRCUITS.

The timing generation and RAM refresh circuits are located on the system timing card and perform two basic functions. First, they serve as the source of various frequencies used by all other circuits in the system and second, they control refreshing of the dynamic memories in the RAM segment of the system memory.

The timing generation circuits, shown in Figure 4-14, consist of a crystal oscillator, followed by a chain of frequency dividers (counters), from which the needed frequencies are read off at various points. In this manner all CPU clocks, dynamic RAM clocks, video synchronization signals, and character or display row related signals are derived from one source and are mutually synchronized. In addition, several secondary signals, such as the cursor and character blinking rate signals are derived from the same timing chain.

The crystal oscillator has a nominal 15.1488 MHz output frequency in standard systems (that do not interface the two fields of a video scan and operates on 60 Hz line power). This frequency is the system bit clock – it determines the duration (width) of a picture element in characters displayed on the screen. This signal, divided by 10, becomes the character clock, which determines the width of characters displayed on the screen. Both, the bit clock and character clock (named SHIFT CLOCK) are connected to the system bus for distribution to other circuits in the system.

To generate the RAM refresh addresses a two-stage 6-bit counter is used. This counter continuously generates the lower six address bits of the memory addresses, which define one of 32 cell columns within any given RAM integrated circuit. These six bits are gated out with the memory refresh request signal onto the address bus and routed to all RAM integrated circuits. The memory refresh request signal is also used to enable all RAM integrated circuits and supply the necessary clock signals, so that the same cell column is refreshed simultaneously in all RAM circuits (ref. also paragraph 4-21).

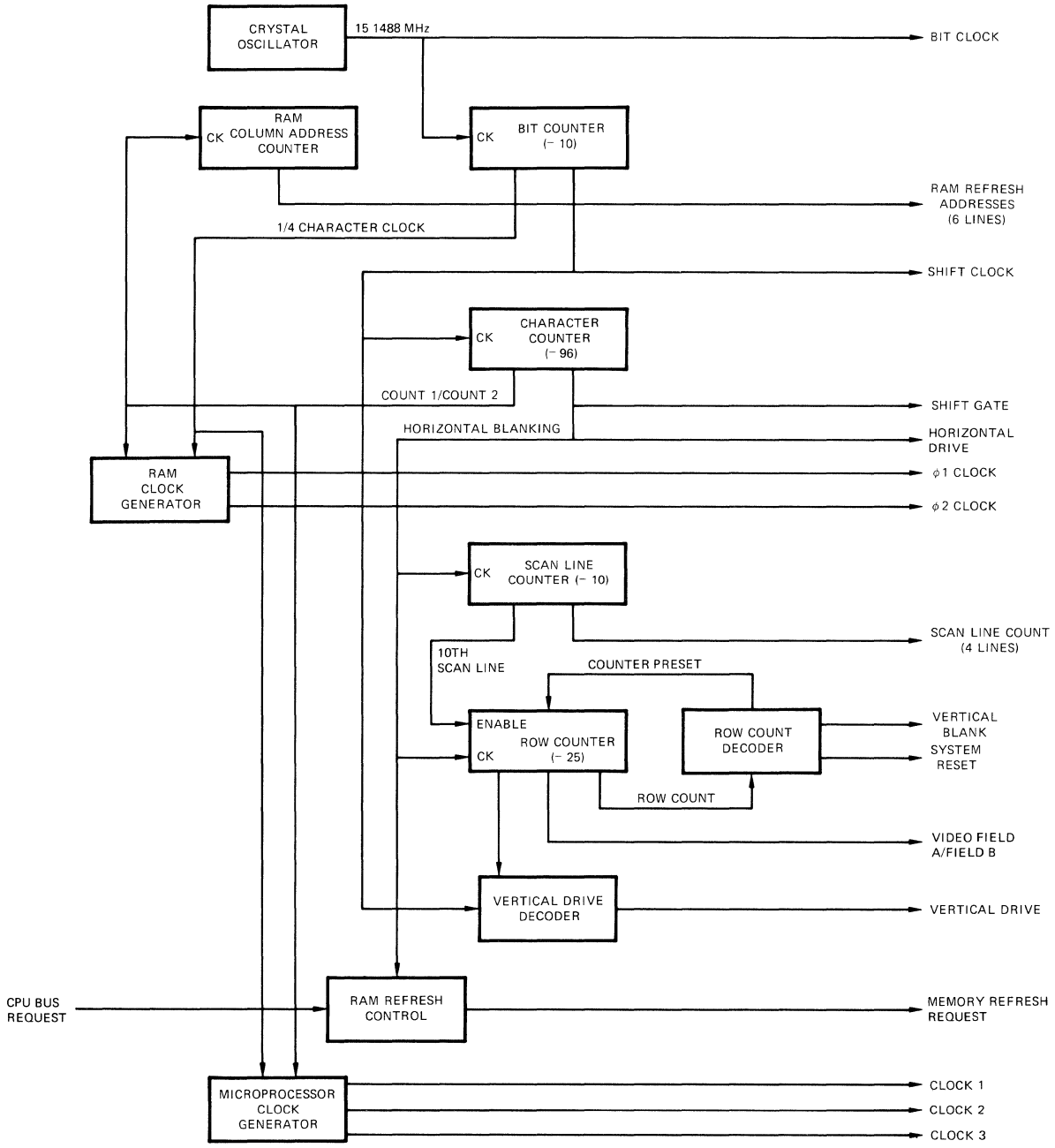



Figure 4-14. Block Diagram of System Timing Circuits

## 4-23. KEYBOARD AND KEYBOARD INTERFACE CIRCUITS.

The keyboard circuits generate an 8-bit character code, whenever a key on the keyboard is depressed, and supply this code ready for writing into the keyboard input character register in the RAM. The keyboard circuits are physically located in two places. The keyboard encoder, an oscillator that generates the character strobe pulses, and supporting logic are all located within the keyboard enclosure. A keyboard input register, character strobe synchronization circuitry, and automatic character repeat circuitry are all located in the display enclosure, on the video/RAM card. A cable between the keyboard enclosure and the video/RAM card interconnects the two physical locations. Figure 4-15 illustrates all keyboard circuits and Table 4-2 lists all codes output by the keyboard.

Whenever a key is depressed, the closed key switch contacts are sensed by the keyboard encoder. The keyboard encoder continuously scans all key switch locations and when it senses a closed contact, responds by outputting a 10-bit code, related to that particular key location. The scanning rate is determined by the oscillator frequency and the code output is synchronous with a single pulse character strobe, also derived from the oscillator signal. In addition to the 10-bit code and the character strobe pulse, the keyboard circuits also output a key down logic level signal, which is used by the keyboard interface circuit as described below. The RESET key on the keyboard does not generate a code, it simply acts as a ground return switch on the reset signal line.

The 10-bit code output by the keyboard encoder consists of an 8-bit word supplied to the RAM, and two control bits used by the keyboard and keyboard interface circuits. The 8-bit word includes a 7-bit ASCII code and one additional bit, as explained in paragraph 4-10. The ninth bit is a logic 0 for all letters of the alphabet and is used to gate the input from the ALL CAPS key on the keyboard. The tenth bit is asserted with all codes that represent a repeatable key. This bit is used in the keyboard interface circuit to perform the repeated writing of a code into the RAM, as described below. Bits 6, 7, and 8 are always routed through the control and caps logic and are modified if either the CTRL key or the ALL CAPS key is depressed. If the CTRL key is depressed, bits 6, 7, and 8 are forced to 001 in all codes in which bit 7 is output as a logic 1 level from the keyboard encoder. If the ALL CAPS key is depressed, bit 6 is forced to a logic 0 in all codes that represent letters of the alphabet (those in which bit 9 is a logic 0).

On the video/RAM card the character code lines are connected directly to the keyboard input register, which is loaded asynchronously with the character strobe. The character strobe is also delayed and stored in a flip-flop, whose output becomes one input to an AND gate. The other AND gate input is a signal called *write keyboard gate*. This signal comes from the video signal generating circuitry and determines when during any given video field the keyboard character code is written into the RAM. (As described in paragraph 4-27, the writing occurs as a part of the video refresh cycle, once every video scan field.)

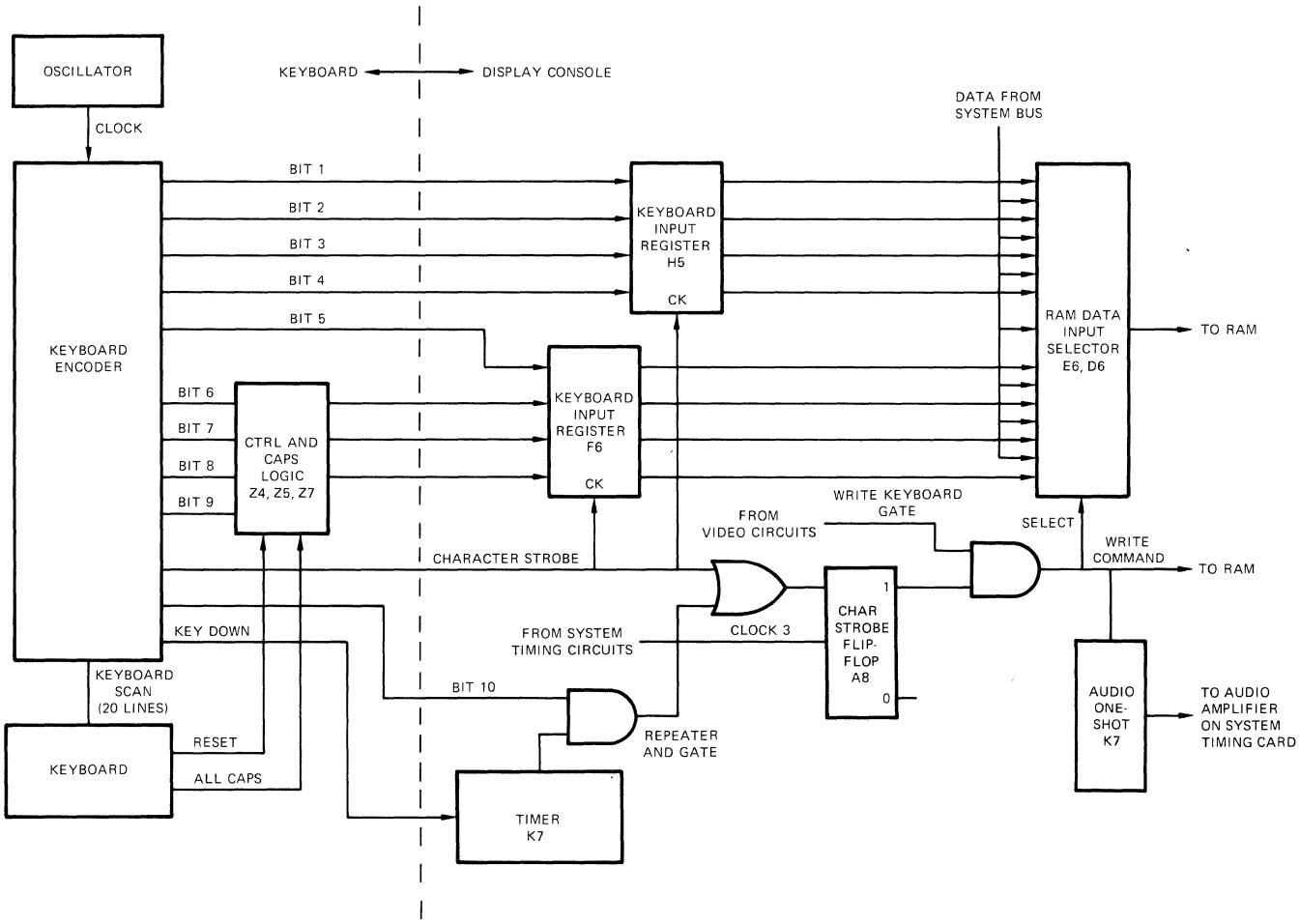
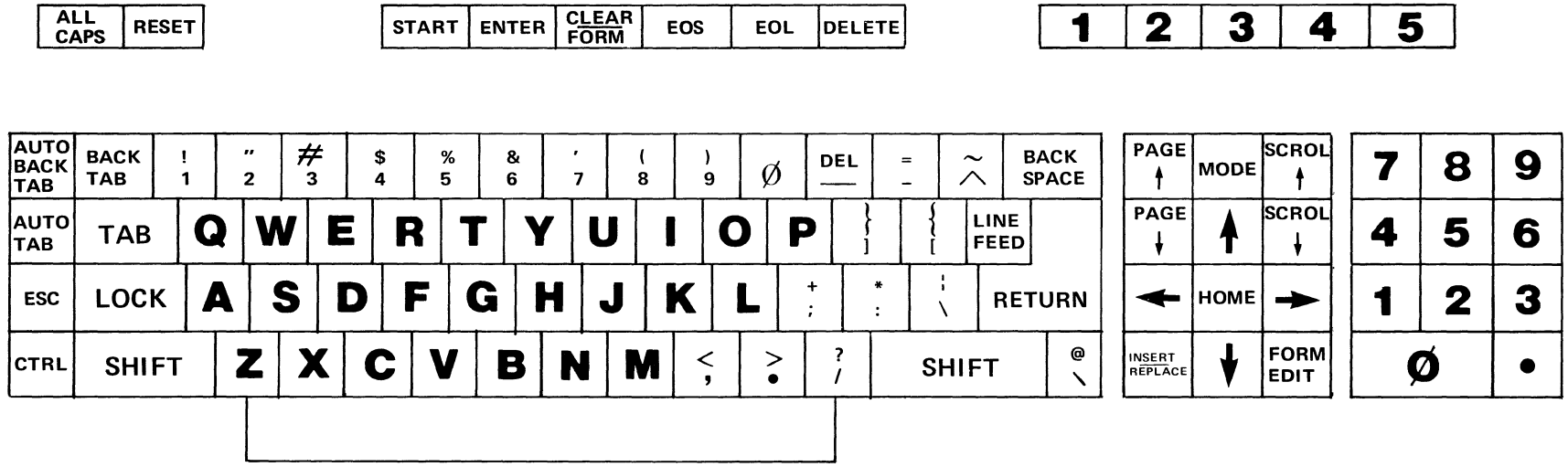



Figure 4-15. Block Diagram of Keyboard and Keyboard Interface Circuits


ALL CAPS
RESET
START
ENTER
CLEAR FORM
EOS
EOL
DELETE
1 2 3 4 5
AUTO BACK TAB
BACK TAB
! 1
" 2
# 3
$ 4
% 5
& 6
' 7
( 8
) 9
Ø
DEL
= -
~ ^
BACK SPACE
AUTO TAB
TAB
Q W E R T Y U I O P
LINE FEED
ESC
LOCK
A S D F G H J K L
+ ;
* :
RETURN
CTRL
SHIFT
Z X C V B N M
< ,
> .
? /
SHIFT
@ \
PAGE ↑
MODE
SCROL ↑
PAGE ↓
SCROL ↓
HOME
INSERT REPLACE
FORM EDIT
7 8 9
4 5 6
1 2 3
Ø
•

| Bit No. 7 6 5 / 4 3 2 1 | 0<br>000 | 1<br>0001 | 2<br>0010 | 3<br>0011 | 4<br>0100 | 5<br>0101 | 6<br>0110 | 7<br>0111 | 8 | 9 | A | B |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 0000 | FORM | CLEAR | SP | 0 | @ | P | ` | *p* | CTRL @ | CTRL P | | NP Ø |
| 1 0001 | ENTER | 1 | ! | 1 | A | Q | *a* | *q* | CTRL A | CTRL Q | | NP 1 |
| 2 0010 | DELETE | 2 | " | 2 | B | R | *b* | *r* | CTRL B | CTRL R | | NP 2 |
| 3 0011 | 5L | 3 | # | 3 | C | S | *c* | *s* | CTRL C | CTRL S | | NP 3 |
| 4 0100 | 4 | RETURN | S | 4 | D | T | *d* | *t* | CTRL D | CTRL T | | NP 4 |
| 5 0101 | LINE FEED | MODE | % | 5 | E | U | *e* | *u* | CTRL E | CTRL U | | NP 5 |
| 6 0110 | START | ↑ SCROL | & | 6 | F | V | *f* | *v* | CTRL F | CTRL V | | NP 6 |
| 7 0111 | ERASE END DISP | ↓ SCROL | ' | 7 | G | W | *g* | *w* | CTRL G | CTRL W | | NP 7 |
| 8 1000 | ← BACK SPACE | → | ( | 8 | H | X | *h* | *x* | CTRL H | CTRL X | | NP 8 |
| 9 1001 | TAB | BACK TAB | ) | 9 | I | Y | *i* | *y* | CTRL I | CTRL Y | | NP 9 |
| A 1010 | ↓ | ↑ | * | : | J | Z | *j* | *z* | CTRL J | CTRL Z | | |
| B 1011 | HOME | ESC | + | ; | K | [ | *k* | { | *CTRL K* | *CTRL* ⊏ | | |
| C 1100 | ↑ PAGE | ↓ PAGE | , | < | L | \ | *l* | \| | CTRL L | CTRL \ | | |
| D 1101 | AUTO TAB | AUTO BACK TAB | - | = | M | ] | m | } | CTRL M | CTRL ⊐ | | |
| E 1110 | 5U | INS REP | . | | N | ^ | *n* | ~ | CTRL N | CTRL ^ | NP • | |
| F 1111 | ERASE END LINE | FORM EDIT | / | ? | O | — | *o* | DEL | CTRL O | CTRL – | | |

* SOFTWARE TREATS NUMERIC PAD KEYS (COLUMN A,B)
AS COLUMN 2 & 3 KEYS
SOFTWARE TREATS CTRL KEYS (COLUMN 8 & 9)

**HARDWARE KEYBOARD CODE**

Table 4-3, Character Generator Chart

| $4_3 2_1$ \ $7 6_5$ | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
|---|---|---|---|---|---|---|---|---|
| 0000 | □ | ▬ | | ⊙ | @ | P | ' | p |
| 0001 | ⊥ | ⌈ | ! | 1 | A | Q | a | q |
| 0010 | T | ⌋ | " | 2 | B | R | b | r |
| 0011 | ≥ | ≤ | # | 3 | C | S | c | s |
| 0100 | ω | ·· | $ | 4 | D | T | d | t |
| 0101 | □ | □ | % | 5 | E | U | e | u |
| 0110 | ϵ | — | & | 6 | F | V | f | v |
| 0111 | ρ | α | ' | 7 | G | W | g | w |
| 1000 | ← | → | ( | 8 | H | X | h | x |
| 1001 | △ | ▽ | ) | 9 | I | Y | i | y |
| 1010 | ↓ | ↑ | * | : | J | Z | j | z |
| 1011 | ∑ | ∧ | + | ; | K | [ | k | { |
| 1100 | ζ | ÷ | , | < | L | \ | l | ¦ |
| 1101 | ≠ | X | – | = | M | ] | m | } |
| 1110 | ∫ | ∩ | • | > | N | ∧ | n | ~ |
| 1111 | ⊂ | ⊃ | / | ? | O | — | o | ■ |

Whenever the write keyboard gate signal occurs, the RAM data input selector routes the keyboard character code to the RAM input lines, and a write command is also supplied to the RAM. The write address is supplied from the RAM address counter in the video signal generating circuitry.

Another feature that is a part of the keyboard circuitry is the repeated writing of a character code into the RAM. This occurs when a key is held depressed for more than one half of a second, except if the key, by the nature of its usage, is specifically excluded. Whether or not a key is included as a part of the repeating set, is determined by the code it generates.

Whenever a key is held depressed, the key down signal triggers a timer. After 0.5 second the timer outputs a pulse to an AND gate. The other input to the same AND gate is bit 10, which determines whether the code stored in the keyboard input register is a repeatable one. If it is, a true input is provided to the AND gate and its output sets the character strobe flip-flop. Thereafter, the next occurrence of the write keyboard gate signal causes the character code to be written into the RAM. If the operator holds the key depressed, the write cycle will be repeated once every video scan field, when the write keyboard gate signal is true.

## 4-24. VIDEO SIGNAL GENERATION AND DISPLAY CIRCUITS.

### 4-25. CRT DISPLAY.

The CRT display is a 15-inch video monitor, with simplified horizontal and vertical sync signal requirements and 0-4 volt video input signal amplitude range. It receives a video signal from the video/RAM card and horizontal and vertical drive signals from the system timing card.

All circuitry of the CRT display is described in CRT Data Display, 15", Instruction Manual, issued by the Miratel Division of Ball Brothers Research Corporation (Miratel Part No. IM1009, Rev. A, August 1973). Only the video raster and character matrix patterns, peculiar to the 9002 system, are described in the following paragraphs.

The character set for the 9002 is shown in Table 4-3.

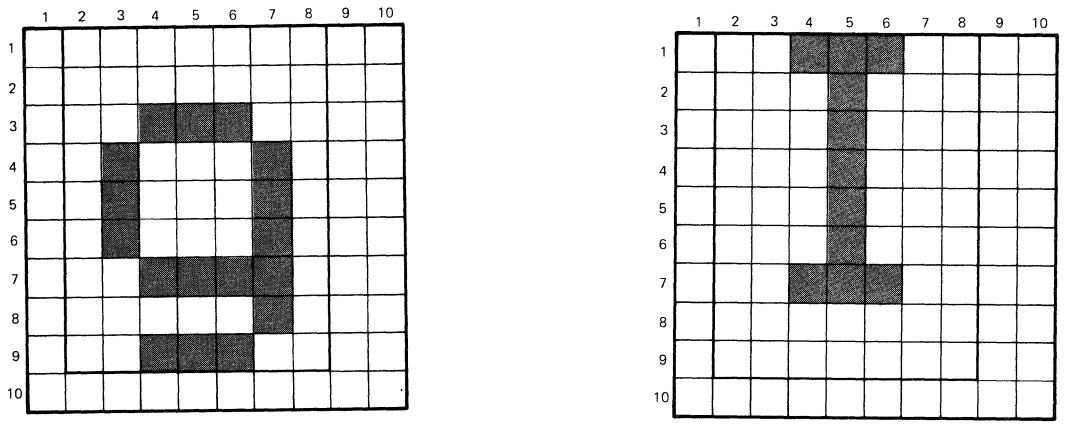
### 4-26. VIDEO RASTER SCAN FORMAT.

The video raster is scanned in a horizontal direction from left to right and from top to bottom. The raster normally consists of 526 scan lines, commonly referred to as a frame. Each frame consists of two fields, A and B, with 263 scan lines per field of which 250 are visible, whereas the others occur during vertical retrace time. The two fields are scanned on the television monitor CRT one after another in such a manner that the 250 visible scan lines in one field physically

overlay those of the other field. The rate at which the fields are scanned is 60 per second and therefore, appear to the human eye as a single display.

Each scan line is divided horizontally into 800 elements, each element representing one bit as it is read out of the video display section of the RAM. There are 526 scan lines of 800 elements each, but data is written on a 500 x 800 matrix of picture elements, which constitutes the visible part of every frame. Because in the standard configuration of the 9002 system every other scan line is overlayed by its adjacent scan line, the matrix, as it appears to the eye, is 250 x 800. If the interface option is installed, the full 500 x 800 matrix is visible. This matrix is used for writing all displays and constitutes the 25 display rows of 80 characters each.

Each alphanumeric character normally occupies an area ten picture elements wide by 10 high. On this area of 10 x 10 picture elements, or dots, any character is constructed by writing individual dots with the CRT beam—as shown in Figure 4-16. One left hand column and two right hand columns, as well as the bottom row of the 10 x 10 base matrix, are always reserved for spacing between characters and are not written upon. On the remaining 7 x 9 matrix various characters are constructed in different ways. A typical upper case letter is constructed on a 7 x 7 matrix, but the two rows on the bottom of the 7 x 9 matrix are reserved for the descenders of such lower case letters as "g", "j", etc.




*Note: The above illustrations show the typical method of constructing characters from rectangular video picture elements, but are not intended to accurately represent the construction details of characters of the 9002 system.*

Figure 4-16. Character Display Matrix Diagram.

## 4-27. VIDEO CIRCUITS.

The video circuits, shown in the block diagram of Figure 4-17, read binary coded digital information out of the RAM, generate a video signal from this information and output the signal, together with horizontal and vertical blanking pulses, to the CRT display. In the CRT display the video signal and blanking pulses are combined with horizontal and vertical drive signals, supplied separately from the timing card, and are used to drive the cathode ray beam.

There are two types of information that are read out of the RAM. Once every ten scan lines on the CRT screen, the video circuits read 80 characters out of the RAM, and prior to the beginning of every video scan field they read such information as the location of the cursor on the screen, which line of 80 characters stored in the RAM is to be the start of the video display on the screen, special display effects information, etc. The binary coded character data is transformed in a signal that represents the character dot pattern on the CRT screen (see Figure 4-16), combined with the cursor and special display effects information and output as a TTL level (0-4 volts) video signal.

To perform the above tasks, the video circuits use a series of registers that store various data output from the RAM, a character generator that generates the dot pattern for all characters displayed on the screen, and supporting logic that generates various RAM addressing, timing, and access control signals. These circuits are represented in the block diagram of Figure 4-17.

At the beginning of every video field (during vertical retrace) a system reset signal is supplied from the display row counter (on the timing card) to the timing and control logic. This signal presets the RAM address counter in preparation for the start of a reading sequence at RAM address X1000. At the same time a memory cycle request and read command are generated to begin reading. (Note that the video circuitry memory cycle requests conform to the RAM access priority list in Table 4-1, therefore, can be generated only in the absence of CPU and RAM refresh cycle requests.)

From this time on, six RAM registers are read out in sequence (except for one write operation, explained below), with the RAM address counter being advanced by one count every time a readout is completed, and a new memory cycle again generated before each new readout.

The first two RAM registers read out are those containing the cursor row and column addresses (locations X1000 and X1001, see Figure 4-6). This data is located into two registers in the cursor generator and determines the row and character column at which the cursor is to appear on the screen during the next television field (refer to paragraph 4-9). Next, a write operation is performed at location X1002, if a character input from the keyboard is available. This write operation is described in more detail in paragraphs 4-21 and 4-23.

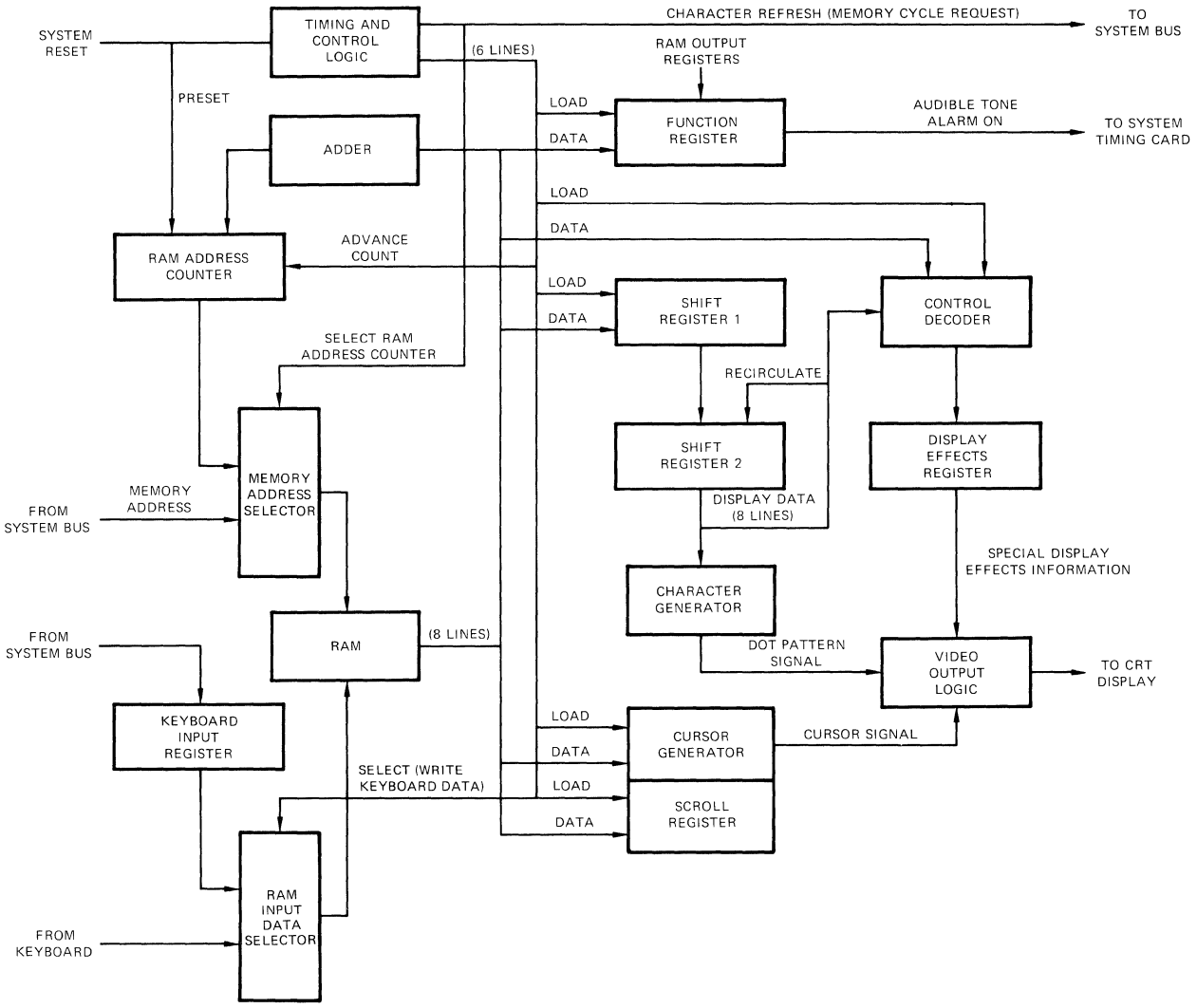



Figure 4-17. Block Diagram of Video Circuits.

After the write operation at location X1002, the RAM register at X1003 is read. The data is stored in the function register and contains information that actuates the audible tone alarm under certain conditions (refer to paragraph 4-29). Next, location X1004 is read and its contents are decoded by the control decoder and stored in the display effects register. This data determines whether the display is started (i.e., the first row on the screen) with any of the special display effects identified in Figure 4-9 and described in paragraph 4-15.

Last, the page start row address is read out of location X1005 in the RAM, entered into the scroll register, as well as added to address X1004 already stored in the adder and entered into the RAM address counter. This completes the initial RAM reading sequence and at this time all necessary preconditions are established for the displaying of the next full video scan field. The address of the first row of 80 characters to be displayed is contained in the RAM address counter and with the next available memory cycle reading of display data begins.

Reading of display data out of the RAM is performed during 25 different intervals and during each interval 80 RAM locations are read. Thus, for one full video scan field, a total of 25 x 80 = 2000 locations are read. These locations represent the 80 character spaces on each of 25 display lines on the screen. The first 24 display lines are read out of 1920 contiguous RAM locations, starting at the address entered into the RAM address counter, but the 25th line, which always identifies the operating mode of the 9002 system, is read starting at location X1030 and continuing consecutively through location X107F.

The reading of the first 80 characters is performed starting with the first available memory cycle after reading of location X1005 (page start row address), and is always completed during the vertical retrace period. The 80 characters are serially loaded into shift register 1 and from there into shift register 2. At the time when vertical retrace is completed and scanning of the first video line starts, each of the 80 characters is consecutively output from shift register 2 into the character generator, where it causes the generation of the first (topmost) scan line dot pattern signal. (The dot patterns for each of ten scan lines of a typical character are shown in Figure 4-16). In addition, the characters are also supplied from shift register 2 to the control decoder. Depending on whether bits 7, 6, and 5 are 100 or not, the word is interpreted as a special display effects code, rather than a displayable character. In case it is a special display effects code, the character generator does not respond to it and instead the display effects register is loaded with the special display effects information. See Figure 4-9 for a legend of the special display effects code, as it is written by the CPU into the video display section of the RAM.

At the same time as the 80 characters are sequentially presented to the character generator, and the control decoder. They also are recirculated back to the input of shift register 2. Therefore, at the completion of scan line 1, the character generator has output the first scan line dot pattern for each of the 80 characters and shift register 2 has fully recirculated, so that its contents are exactly the same as they were just before the start of scan line 1.

Now, with the start of scan line 2, the sequence of outputs to the character generator, as well as the recirculation of shift register 2 is repeated again. This time the character generator outputs the dot pattern for scan line 2 of all 80 characters. The above sequence is repeated a total of ten times, causing the character generator to output the dot pattern for all 10 scan lines of each character.

While the dot patterns are generated and shift register 2 is being recirculated, shift register 1 is being loaded with the next 80 characters for the second row of the display. These characters are read out of the RAM and again serially loaded into shift register 1.

During scan line 10 of row 1, the data in shift register 2 is not recirculated anymore and instead, the data from shift register 1 is transferred into shift register2, in preparation for scan line 11, which marks the top of the second display row.

This sequence of recirculating shift register 2, simultaneous reloading of shift register 1, and transfer of data during scan line 10 takes place during every video display row on the screen—a total of 25 times. Allowing for interruptions by the CPU and RAM refresh cycle requests from the timing card, the reloading of shift register 1 takes place during the first 2.5 scan lines of the first display row. Therefore, during the last 7.5 scan lines of the first row, shift register 1 is dormant and memory cycles are available to all peripheral devices.

The output of the character generator is entered into the video logic, where it is combined with the cursor signal, altered, if necessary, to create any special display effects, mixed with horizontal and vertical blanking information, and output as a video signal that ranges between 0 and 4 volts in amplitude.

## 4-28. RS-232C INTERFACE CIRCUIT.

The RS-232C interface circuit receives data from a telecommunications modem and writes it into the RAM, or it reads data out of the RAM and transmits it to the modem. In order to carry out its receiving and transmitting tasks, the circuit utilizes a UART (universal asynchronous receiver-transmitter), with various supporting logic. The supporting logic paces the UART through sequential data input/output steps as well as controls the communication of data and control signals between the UART and the 9002 system bus. Figure 4-18 shows a block diagram of the RS-232C interface circuit.

The UART consists of a receiver and transmitter section. It serves as a data interface between the telecommunications modem and the 9002 system bus. As such it performs three distinct functions: (1) it communicates serial data to and from the modem, observing the asynchronous telecommunications line protocol; (2) reformats the data; and (3) communicates data to and from the 9002 system bus, while observing the bus protocol.

To communicate with the modem, the UART is clocked by the telecom clock (see Figure 4-18) at a particular rate, so that it operates at the same speed as data is communicated on the telecommunication line—either 110, 300, 1200, or another selectable baud rate. In receiving, it looks for an incoming start bit and interprets the following 8 serial bits as data bits. It converts the 8 bits into a parallel word and holds it in an 8-bit register, ready to be transferred onto the 9002 system bus, holds it in a shift register and then outputs it to the modem at the selected baud rate, preceded by a start bit and followed by one or two stop bits (depending on the baud rate).

Data communication between the UART and the system bus is controlled by the read/write cycle counter and other logic shown in Figure 4-18. Once every 63 microseconds the read/write cycle counter is triggered and clocked through a sequence up to nine steps long, during which data is first transferred from the RAM into the UART and then other data is read out of the UART and transferred into the RAM. The nine steps of the read/write counter are listed in Table 4-3 and are described in more detail below.

During the greater part of any 63 microsecond period, the read/write cycle counter is inactive—it is in state 0. When the counter is triggered by a signal called *reset refresh,* it moves to state 1 and the read/write cycle begins. During the cycle the counter outputs are supplied to the read/write logic and the address bus logic, which develop the necessary RAM read or write commands, memory addresses, and together with the bus request logic gate data or information out through the data output buffer.

During state 1 the read/write logic outputs the status/error select signal to the data/status selector and thus causes it to route the modem status and data error signals to the data output buffer. If the bus request logic outputs an enable signal, the status and data error information is supplied to the system bus, along with a write command from the read/write logic and an address from the address output buffer. The status and data error word is written into the RAM, from where it can be read and interpreted by the microprocessor. Figure 4-8 shows the contents of this word.

During state 2 a control word is read out of the RAM and transferred to the modem. This word is used by the microprocessor to advise the modem that the 9002 system is ready to receive or send data, or to request a break in the incoming data stream. The control word is illustrated in Figure 4-8.

During state 3 no read or write operations are performed. There is, however, a secondary function that is carried out by the read/write logic. In anticipation of state 4, the UART transmitter ready line is sampled and if the UART is ready to receive data from the RAM the cycle counter is allowed to advance to state 4. If the UART is not ready (its input holding register is still full), the counter is automatically advanced to state 7 by the load counter signal.

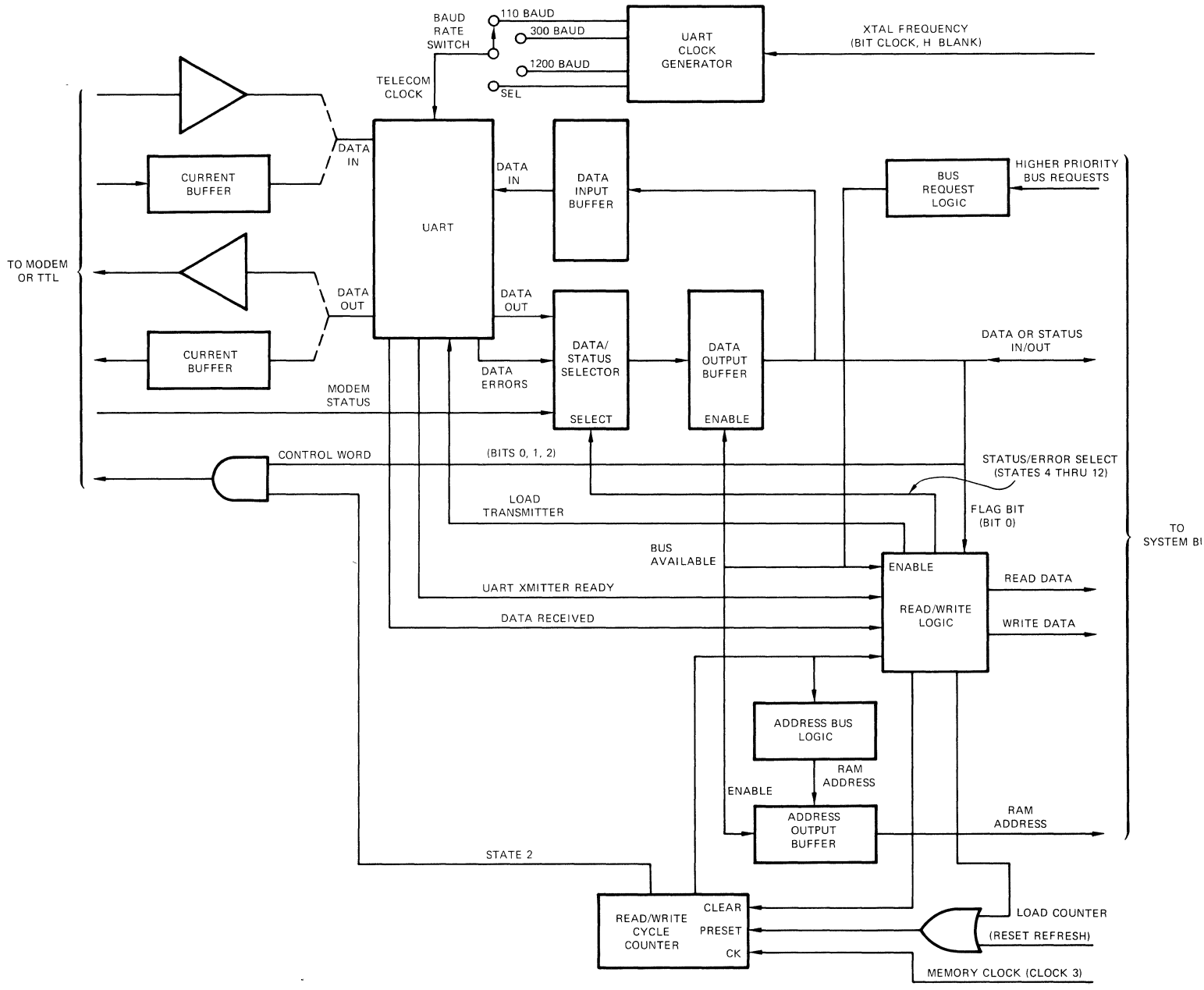



Figure 4-18. Block Diagram of RS-232C Interface Circuit.

Table 4-3. RS-232C Interface Read/Write Counter States

| COUNTER OUTPUT STATE | FUNCTION |
|---|---|
| $\overline{0}$ | Inactive standby state |
| $\overline{1}$ | Read status of modem and UART error flags and write status word into RAM. |
| $\overline{2}$ | Read microprocessor control commands out of RAM and output to the modem. |
| $\overline{3}$ | Unused state (spare) |
| $\overline{4}$ | Test data output flag bit in RAM to determine if data is available from the microprocessor. |
| $\overline{5}$ | Read microprocessor output data from the RAM (if available) and transfer into the UART. |
| $\overline{6}$ | Reset data output flag bit in RAM to indicate the completion of data readout. |
| $\overline{7}$ | Test data input flag bit in RAM to determine if data input register in RAM is clear. |
| $\overline{8}$ | Transfer data word from UART (if available) into data input register in the RAM. |
| $\overline{9}$ | Set data input flag bit in RAM, to indicate to the microprocessor the presence of a data word from UART. |

During state 4 a flag bit is read out of the RAM, to determine whether the microprocessor is ready to send out data. If this bit is 1 (Figure 4-8), the counter is allowed to advance to state 5, but if it is 0, the counter is jumped to state 6.

During state 5 the data word is read out of RAM and supplied to the UART via the data input buffer.

During state 6, the data output flag is reset–a 0 bit is written into the RAM. As a secondary function, the UART data received line is sampled. If the UART indicates that it has data ready to be output to the RAM, the counter is allowed to advance to state 7; if no data is ready, the counter is reset to state 0 and the read/write cycle is complete.

During state 7 the data input flag in the RAM is read, to determine if the microprocessor has cleared the previous input word out of the RAM. If this flag bit is 0, the counter is allowed to advance to state 8; if the flag bit is 1, the counter is reset and the read/write cycle is complete.

During state 8 the data input word is routed from the UART to the RAM and written into the RAM register.

During state 9 the data in put flag in the RAM is set to indicate to the microprocessor that a data word has just been loaded into the RAM, ready to be processed. This completes the read/write cycle and the counter is reset to state 0.

Although the read/write cycle sequence always remains the same, there are several data formatting options available in the RS-232C interface circuit. These are mostly associated with the UART and can be effected by changing connections (straps) on the timing card. First, the UART can be strapped to check parity in incoming words and generate a parity bit for all outgoing words. If this option is implemented, a parity error indicator bit is output by the UART, as a part of the status and data error word.

Second, the UART can be strapped to generate 1, 1.5, or 2 full stop bits for all outgoing data words. (In fact, the word length itself can be varied between 5 and 8 data bits, although the 9002 system circuits require an 8 bit word format.)

Finally, the UART input and output lines can be arranged to interface either with a voltage sensitive device, such as a modem, or a current mode operated device, such as a teletypewriter. In the latter case a current buffer circuit is connected in the data input, as well as data output line of the UART.

## 4-29. KEYBOARD AUDIBLE RESPONSE CIRCUITS.

There are two audible responses that the 9002 system emits in response to certain keyboard operations. First, a clicking sound is generated whenever a key on the keyboard is depressed, and an audio frequency tone is generated if the keyboard input software registers overflow, because of excessive incoming data rate. To generate these responses, an oscillator and amplifier circuit, on the system timing card, is used to generate a signal for a speaker attached to the chassis, near the back of the display console (see Figure 4-11).

To generate the clicking sound in response to the depression of a key on the keyboard a one-shot on the video/RAM card is triggered with the same command signal that writes the keyboard character into the RAM (see Figure 4-15). The one-shot outputs a pulse which is amplified on the system timing circuit and output to the speaker.

To generate the tone, the microprocessor alters bit 8 in the function register of the video circuits (see Figure 4-17) and this triggers a timing one-shot on the system timing card. In response to the one-shot output, the oscillator is turned on and outputs an audio frequency signal to the chassis mounted speaker, via the same amplifier described above.

## 4-30. BUS REQUEST LOGIC.

The bus request logic implements the subordination of memory cycle requests by the microprocessor, the timing circuits, and all input/output devices. The subordination is listed in Table 4-1, and is accomplished by a series of interconnections between circuit cards (and spare card locations) and simple decoding circuits on each of the three circuit cards. Figure 4-19 shows the bus request logic circuits.

The CPU has top priority in accessing of the RAM. Therefore, the CPU bus request is sent out via pin A31 to all other circuit card slots, while the CPU accepts none of the other bus request signals, because it does not have to subordinate its bus request to any other.

Memory refresh is the second function in the priority list after CPU and therefore, its bus request signal is sent out via pin A39 to all circuit card slots other than that of the CPU. Likewise, the video refresh bus request, which is third in priority, is sent out via pin A40 to all circuit card slots, except that of the CPU. Except for the fact that the RS-232C interface circuit is on the system timing card, the video refresh bus request would not need to be sent to slot 5 either.

Note that because the keyboard character input function is performed as a part of the video refresh cycle, the keyboard input circuits do not need to generate a separate bus request.

The peripheral device bus requests are subordinated by means of one line, which is connected to all slots serially, starting with pin A48 of slot 6 and ending with pin A38 of slot 5. With this line a priority is assigned to each circuit card slot, in the order 6, 7, 2, 3, 4, and 5. The bus request logic on each optional circuit card inserted in any of these slots is such that it subordinates its own function to the signal coming in on pin A38 from the previous card. In this manner, the proper subordination is achieved. (Refer also to Chapter 6 for additional information about the peripheral device bus request priorities).

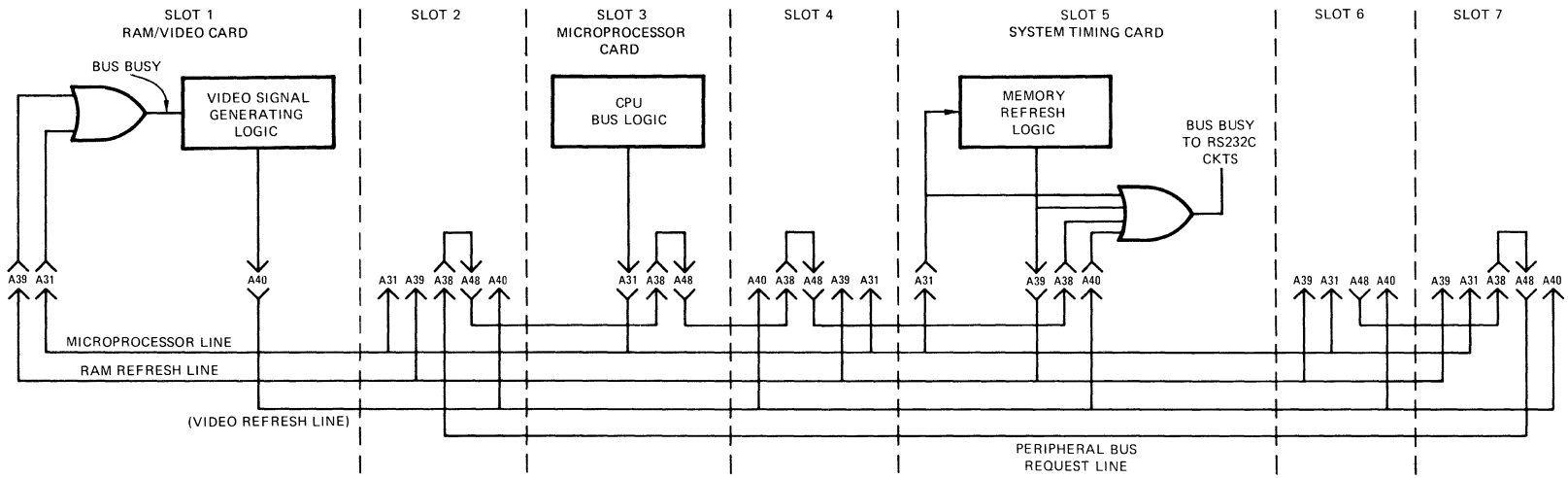



Figure 4-19. Simplified Diagram of Bus Request Logic

## 4-31. MOTHERBOARD.

The motherboard is located at the back of the circuit card chassis and interconnects all other circuit cards in the display unit.

The mother board contains the address, timing, command data, power, and ground return lines that constitute various parts of the system bus. It also provides connectors for harness cables to the rear connector panel and to the CRT display, and auxiliary power and control signal outputs.

All address, all data, and most of the system timing, control and command signals are connected in parallel to all circuit cards, as are most of the bus request signals (see Figure 4-19). Other signals, associated with functions pertaining to selected cards only are not bussed, but are connected between specific cards or to an edge connector of the motherboard. There are several spare pins available on most all circuit card connectors on the motherboard.

## 4-32. POWER SUPPLIES.

The three modular power supplies in the display console supply dc operating power to all circuits in the 9002 system. The supplies, see Figure 5-3, are +5V, -15V, and +3.5V. The latter is referenced to the +5V supply and thus supplies +8.5V to the system.

All three power supplies are regulated and have current limiting and overvoltage protection circuits. The output voltage, limiting current, and external overvoltage limit all are adjustable.

# chapter 5 maintenance

## 5-1. INTRODUCTION.

This chapter contains information required for maintenance of the 9001 Microcomputer Terminal System. The chapter contains preventive maintenance information, adjustment procedures, troubleshooting procedures for isolating malfunctions in the system to a circuit card level, and parts replacement instructions. Before performing any maintenance described in this chapter, the maintenance technician must have a thorough knowledge of the material contained in Chapter 4.

## 5-2. MAINTENANCE TEST EQUIPMENT.

To perform the maintenance procedures in this chapter, a multiple trace oscilloscope (such as Tektronix Type 465), a digital logic probe, and/or circuit tracer, and d DVM are required.

## 5-3. PREVENTIVE MAINTENANCE.

The microcomputer/terminal requires a minimum of preventive maintenance: periodic cleaning of the outside surfaces of the equipment may be performed, along with checks of the condition of the interunit cabling and internal components of the chassis. To clean the CRT screen, display enclosure, and keyboard use a lightly moistened lint-free cloth or vacuum cleaner. A mild household cleaner can be used to clean the outside surfaces of the control console and keyboard.

The circuit boards in the display unit and keyboard operate at low power levels. Consequently, their contacts are sensitive to dust, oil, moisture, and corrosion. When the circuit cards are removed, the contacts should be cleaned before re-inserting. Use a lint-free cloth moistened with trichloroethylene or another suitable solvent, then remove the film left by the cleaning fluid.

## 5-4. CHECKOUT AND ALIGNMENT.

Checkout of the microcomputer/terminal system can be done with a special diagnostic card has a microprocessor on it and a diagnostic program. This program is sufficiently comprehensive to exercise every operating mode and various combinations of special display effects, etc. The diagnostic card may then be used to initially check out the system after installation, or periodically thereafter. In normal use, correct operation of the system will be a sufficient indication that it is functioning properly; in instances where only some other modes are used during normal operation, or where a thorough check of the system is important for some other reason, the complete diagnostic program may be run at any time. Note that the checkout program is also useful for troubleshooting purposes.

## 5-5. POWER SUPPLY ADJUSTMENT.

The following procedure is used to adjust the three system power supply voltages: +5.0 V, +8.5 V, and -15 V. The +5.0 V supply provides standard logic levels to all digital circuits in the system, but +8.5 V and -15 V are used by the dynamic RAMs. If the +5.0 V supply is out of tolerance, all digital circuits in the system will be affected, but if either the +8.5 or -15 V supplies are out of tolerance, the dynamic RAMs may output randomly erroneous data. A check of the power supply voltages should always be one of the first considerations when a system malfunction is observed. A DVM or a multimeter is required to perform this procedure.

a. Turn off equipment power.

b. Remove the front panel of the display enclosure (remove two screws in recessed area behind the keyboard, adjacent to the Power switch).

c. Remove the main enclosure from the display unit (two screws on back of the unit, on either side of connector panel).

d. Identify the system timing card and the video/RAM card in the circuit card chassis. See Figure 1-2, 5-1, and 5-2.

e. Connect the DVM (or multimeter) to the +5V test point on the system timing card, or on the video/RAM card. (Note that all circuit cards have a ground bus along the length of the front of the card; this bus can be used for connecting the negative lead of the measuring instrument.)

WARNING

Lethal voltages exist in the CRT monitor chassis. When the main enclosure is removed, extreme care should be exercised to avoid contact with the components and wiring carrying high voltages. Use plastic tools, if possible.

f. Turn on system power and observe the voltage on the DVM. If it is not 5.00 ±0.15 volts, adjust potentiometer R16 (see Figure 5-3).

g. Turn off system power and reconnect the DVM to the +8.5 volt test point on the video RAM card (pin 1 on any RAM, see Figure 5-2).

h. Turn on power and observe the DVM reading—it should be 8.50 ± 0.30 volts. If necessary, adjust R7 (see Figure 5-3).

NOTE

The 8.5 volts is derived from a 3.5 volt supply circuit that is referenced to the +5 V supply. Therefore, the +5 V supply must always be adjusted first and its adjustment always will affect the 8.5 V reading.

i. Turn off power and reconnect the DVM to the −15 V test point on the RAM refresh card (Figure 5-2).

j. Turn on power and observe the DVM reading—it should be −15.00 ± 0.45 volts. If necessary, adjust R14 (see Figure 5-4).

k. Turn off power and disconnect the test equipment.

## 5-6. CLOCK ADJUSTMENT PROCEDURE.

The following procedure is used for adjusting the clock 1, clock 2, and clock 3 signals generated on the system timing card. The adjustment is made to establish the pulse duration of each clock signal, as well as their phase relationships. These signals are used to operate the dynamic RAMs on the video RAM card and if they are not adjusted correctly, erroneous data may be read out of the RAMs.

A multiple trace oscilloscope is required to perform the adjustment procedure.

a. Turn off equipment power and remove the faceplate of the display enclosure to expose the circuit cards and chassis (remove two screws in the recessed area behind the keyboard, adjacent to the Power switch).

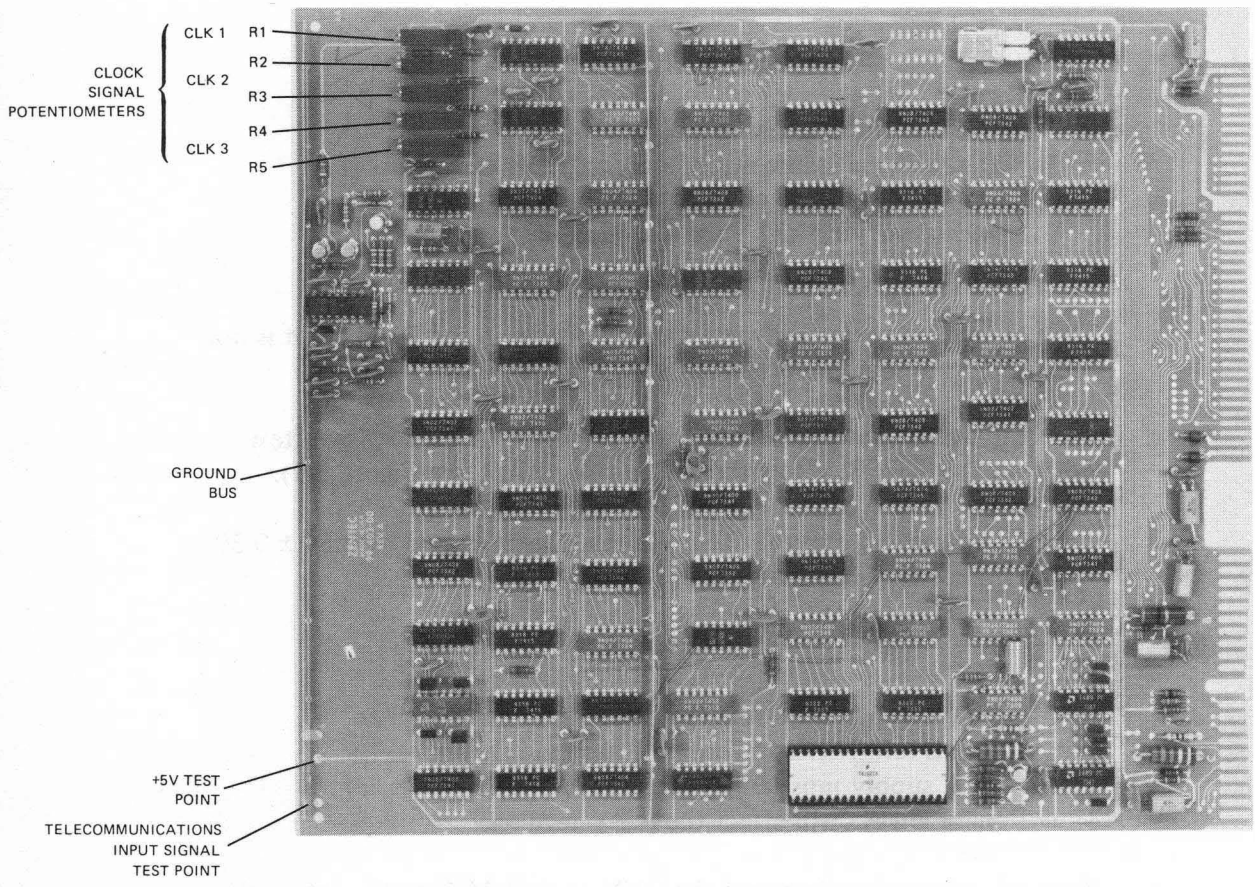



Figure 5-1. System Timing Card

b. Identify the system timing card and the video/RAM card in the circuit card chassis (see Figure 4-11, 5-1, and 5-2).

c. Connect channel 1 of the oscilloscope to TP1 (clock 1) on the video/RAM card. Turn on system power and set the oscilloscope controls to trigger the oscilloscope on clock 1.

d. Connect channel 2 of the oscilloscope to TP2 (clock 2) on the video/RAM card.

NOTE

If the oscilloscope has more than two channels, the third channel can be connected to clock 3 (TP3). This procedure, however, assumes the use of a two-channel oscilloscope.

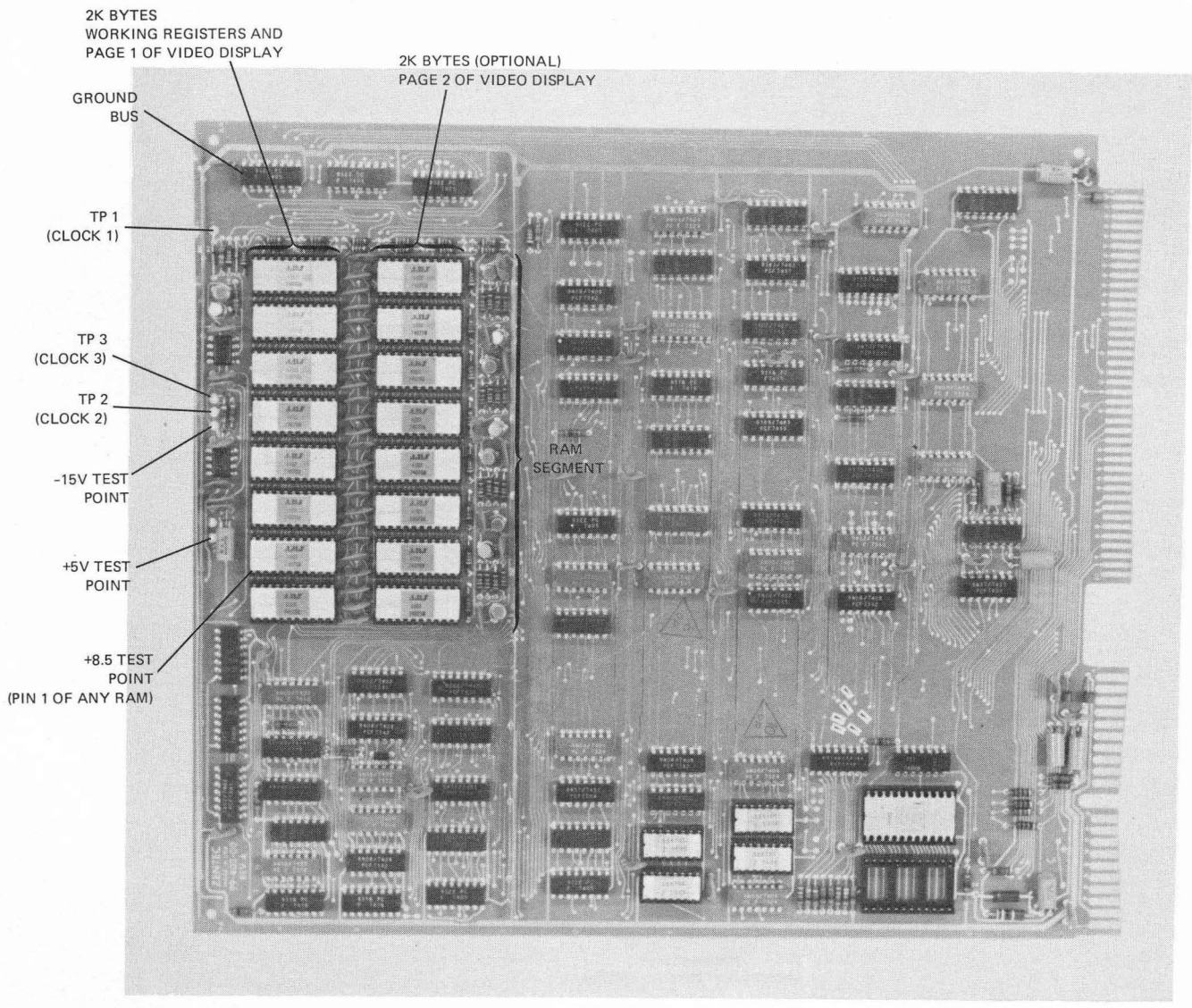



Figure 5-2. Video/RAM Card

e. While observing the clock 1 signal on the oscilloscope, adjust R1 on the system timing card (see Figures 5-1 and 5-4) so that the clock 1 signal pulse is 200 ns at its 50% amplitude level. Note that R1 affects only the trailing edge of the pulse.

f. While observing clock 2 signal, adjust R2 on the timing card so that the leading edge of the clock 2 signal pulse is 200 ns from the trailing edge of clock 1 (see Figure 5-3).

g. Adjust R3 to set the trailing edge of the clock 2 pulse so that the pulse is 300 ns wide.

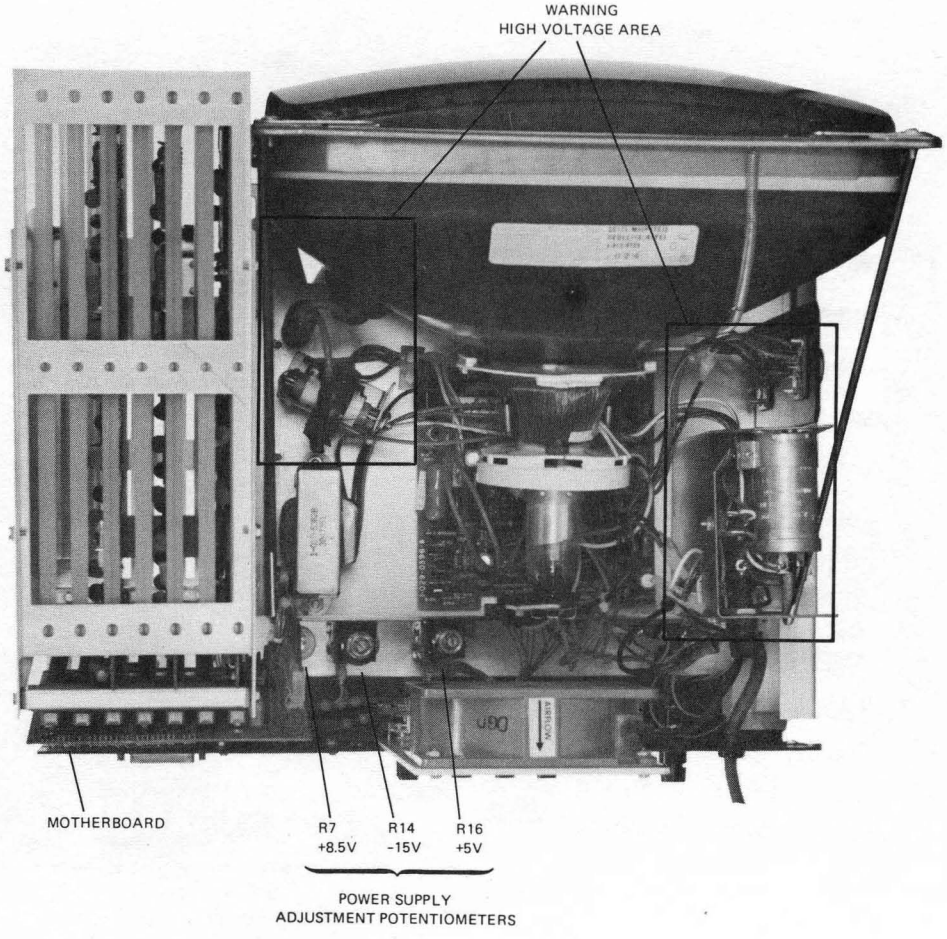



Figure 5-3. Interior of CRT Display Chassis.

h. Reconnect channel 1 of the oscilloscope to TP3 (clock 3) on the RAM refresh card. Change the oscilloscope triggering to clock 2.

i. Adjust R4 to set the leading edge of clock 3 pulse 100 ns from the trailing edge of clock 2.

j. Adjust R4 to set the trailing edge of clock 3 so that the pulse is 200 ns wide.

k. This completes the adjustment procedure. Turn off equipment power, disconnect the oscilloscope and replace the faceplate of the display enclosure.

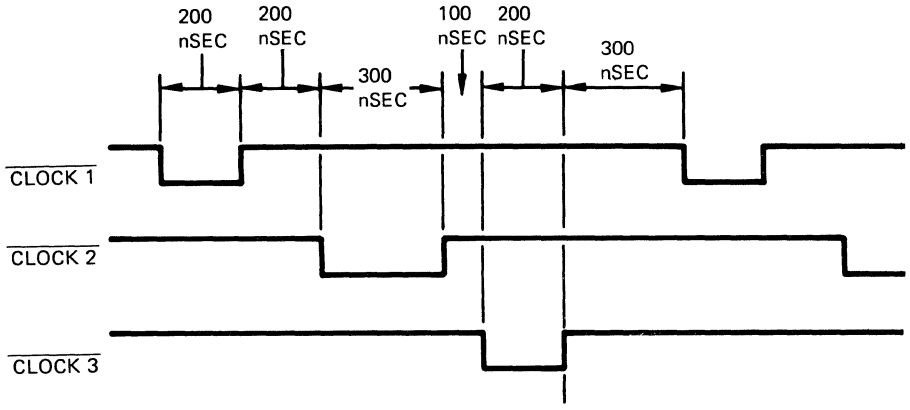



Figure 5-4. Timing Diagram of RAM Clock Signals.

## 5-7. TROUBLESHOOTING.

Troubleshooting of the 9002 system can be performed on either of two functional levels—a circuit card and major assembly level, or on a detailed circuit component level. Troubleshooting at the circuit card level is described in this manual and requires an overall block diagram level knowledge of the system. Troubleshooting on a more detailed level requires thorough understanding of the circuits and individual signal functions within circuits. Therefore, it requires additional training, test equipment, and general experience with microcomputer and digital logic circuits.

Troubleshooting on the circuit card and major assembly level consists of two basic steps. First, a series of preliminary checks are performed to eliminate malfunctions that are only apparent and actually are caused by external equipment, incorrect control settings, loose cables, etc. Second, tests, measurements and substitution of circuit cards can be performed to isolate the malfunction to a circuit card or another major assembly.

## 5-8. PRELIMINARY CHECKS.

Before troubleshooting individual circuits or circuit cards within the 9002 system, always perform the following checks to eliminate apparent malfunctions caused

by external equipment, incorrect control settings, loose cables, and other similar causes. Consider also the environment in which the system is operating. A strong magnetic field or electrical interference may cause the CRT display to behave erratically.

a. Verify that the power fuse on the rear panel is not burned out and is of the proper rating. (2 amps slo-blo for systems operating on 115 V ac power). Check condition of the power cable and the front panel Power switch.

b. Turn off system power and check that all cables and cable connector pins are in good condition. This includes the cables connecting to the rear panel of the display console, as well as the keyboard cable.

c. Verify the physical configuration of the system and how it is programmed, to ascertain that the operator is using the system correctly.

d. If the malfunction is associated with picture quality on the CRT screen, adjust the CRT display controls.

e. The malfunction could be cause by peripheral equipment. Disconnect that equipment, and operate the system without it to observe any changes. If an identical device can be substituted for that disconnected, try it and again observe any changes. Such substitution can be performed with any peripheral device connected to the rear panel and also with the keyboard. To disconnect the keyboard cable, remove the cover plate on the bottom of the keyboard and disconnect the cable from the circuit board inside.

CAUTION

Remove shorting blocks from MOS integrated circuits on the substitute keyboard and install on the keyboard just removed from the system. If the shorting blocks are left off, the integrated circuits may be damaged by a static charge.

f. Turn off system power. Release the two screws in the recessed part at bottom front of the display enclosure; remove the faceplate. Then remove two screws on back of display console, on either side of back connector panel, slide the enclosure off.

g. Inspect the chassis, wiring, circuit cards, and power supplies for burned, broken or loose wiring, overheating of components, or corroded contacts. Pull out each circuit card individually and inspect it.

h. Check that all circuit card edge connector pins and the motherboard connectors are in good condition.

i. If parts have been replaced in the system, or if other maintenance has been performed recently, verify that correct number and configuration of circuit cards are installed in their correct locations (See Figures 4-11 and 6-1).

j. If the system has any circuit cards in it other than the three basic cards (Figure 4-11), consider removing them, disconnecting the associated equipment and operating the 9002 system with only the three basic cards. Always turn off power when removing or inserting a circuit card.

k. If all of the above steps have not identified the cause of the malfunction, check all power supply voltages, in accordance with the procedures in paragraph 5-5.

l. Check the adjustment of the clock 1, 2, and 3 one-shot adjustment on the system timing card (refer to paragraph 5-6).

## 5-9. SYSTEM LEVEL TROUBLESHOOTING

**5-10. CARD SUBSTITUTION.** The object of system level troubleshooting is to isolate a malfunction to one circuit card or major assembly in the display console or the keyboard. To help do this, the basic method is substitution of circuit cards in the display console circuit card chassis. In addition, some deductive reasoning can be performed by observing the CRT display screen under various system operating conditions.

Card substitution can be performed successfully only in a system that has no more than the three basic cards in it (listed below). If there are any optional cards installed, turn off power, remove the cards and check to see if the system is operating correctly with only the three basic cards. In this manner, the malfunction may be identified with the optional cards as a group and they may be reinstalled one at a time to localize the fault further. Always turn off power when removing or inserting a card.

If the above removal and reinsertion of cards either is not applicable or does not isolate the malfunction, proceed to substitute the three basic cards. To do that, three known good cards must be available:

- microprocessor card
- video/RAM card
- system timing card

The clock 1, 2, and 3 signals must have been properly adjusted on the system timing card that is used as the substitute. (It may serve as a good precaution to check these signals right after the card is inserted in the system.)

Turn off system power, take out only one of the suspect cards and replace with the substitute card. Then, turn system power back on, check operation of the system, and observe any changes. If the system is still not operating correctly, turn off power and proceed to substitute the next card. In this manner all three cards can be substituted and system operation checked between substitutions. The order of substitution is unimportant, as long as one card is substituted at a time.

**5-11. OBSERVATION OF CRT SCREEN.** There are certain conclusions that can be drawn about the source of a malfunction, by entering characters on the keyboard and observing their display on the screen. Between the keyboard and the CRT screen all characters follow the path:

KEYBOARD (Figure 4-15)
↓
KEYBOARD INPUT REGISTER (Figure 4-15)
↓
RAM (Loc. X1002)
↓
MICROPROCESSOR
↓
RAM (Video Display Section)
↓
VIDEO CIRCUITS (Figure 4-17)
↓
CRT DISPLAY

Certain circuits in this path cause specific symptoms that can be identified.

First, if all characters on the screen are displayed erratically, the fault can be in RAM, system timing circuits, or the microprocessor. If the RAMs or microprocessor are not receiving proper timing signals, they will function completely erratically and will provide an incoherent display. Microprocessor faults can also cause an erratic display, but tend to be more regular in appearance, rather than entirely random.

If, after initial power turn-on, no characters can be properly displayed on the screen, and the preliminary checks have verified that power, clock signals, and keyboard circuits are all functioning correctly, the system is likely unable to write into the RAM. This may be caused by the microprocessor, RAM write enable circuits, data, or address circuits.

If errors on the screen appear with some regularity (for example, every other or every fourth character is wrong), the address during reading or writing in the RAM is incorrect. If every other character is incorrect, it indicates that the lowest address during reading or writing in the RAM is incorrect. If every other character is incorrect, it indicates that the lowest address bit may always be a 1 or always a 0. If every other pair of characters is wrong, the second address bit is always in the same state, etc. Such faults can be seen best if the same character is written across the entire screen (for example if all 0s or 1s are written on the screen).

Much more can be concluded about the system, if ZIM is available as a trouble-shooting aid. With the ZIM program any location in the memory—either RAM or ROM/PROM can be observed on the screen. With this method, the keyboard input register at RAM location X1002 can be observed, for example, to check the character coming in from the keyboard. Likewise, any location in the video display section of the RAM can be observed to see its contents. When using ZIM, however, one must be aware that the ZIM program is executed by the same basic circuits—the microprocessor, RAM, and video circuits.

## 5-12. PARTS REPLACEMENT.

For the purpose of parts replacement, a maintenance policy should be established. Such a plan must be determined by the maintenance capability of the user - skill level of maintenance personnel and the ability to maintain a spare parts inventory. Two distinct levels of maintenance, which present a choice, are: (1) replacement of entire circuit boards and major assemblies and return of defective parts to the factory for repair, (2) replacement of all parts not requiring factory installation, in particular, all circuit components. However, this manual contains information for troubleshooting and parts replacement to the major assembly level. Typical assemblies are complete circuit cards and power supply modules in the display console. Any parts replacement beyond this level requires various drawings, parts lists, and other information from Zentec Corporation by special arrangement.

# chapter 6 system and interface design

## 6-1. INTRODUCTION

This chapter contains information for the OEM system designer, who needs to make modifications to the 9002 system hardware and design circuits which interface a peripheral device to the 9002 system. In the first part of the chapter the utilization of spare circuit card locations is discussed, then the strappable options in the system memory and on other circuit cards are discussed, and last, interface design requirements are described. For further information about system or interface design for the 9002 system, please contact the Application Engineering Department of Zentec Corporation.

## 6-2. UTILIZATION OF SPARE LOCATIONS IN THE DISPLAY CONSOLE CARD CHASSIS.

In the circuit card chassis within the display console there is space for seven circuit cards, see Figure 4-11. Because the minimum number of cards required by a standard 9002 system is only three, there are up to four open spaces for optional circuit cards. These typically can be filled by the RAM card, the dual RS-232, or any interface card for a peripheral device.

When installing more than one peripheral interface card, the question of system bus priorities arises. This is determined by the location in which each card is installed. To understand how cards should be located in the circuit card chassis, refer to Figure 6-1. In this figure it can be seen that the three basic cards are in slots 1, 3, and 5. These cards must always be located in those slots, except that the microprocessor card can optionally be located in slot 4. If any peripheral interface cards are added, they must be installed starting with the first open slot to

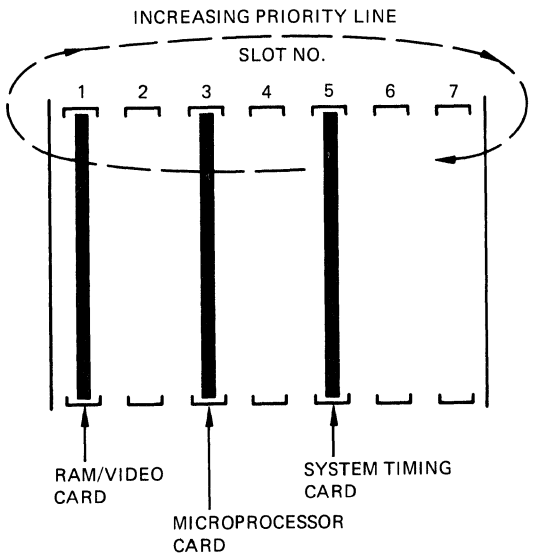



Figure 6-1. Diagram of System Bus Priority Assignments for Circuit Cards in the Display Console.

the left of the timing card and progressing with the arrows on the increasing priority line in Figure 6-1. Starting with 4, all slots along the line must be filled in sequence.

This installation sequence orders all system bus priorities, except those of the microprocessor, RAM refresh, and video refresh. The latter three always remain in the top priority positions, as listed in Table 4-1.

For example, if a printer interface card is installed in slot 4, it has a higher priority than the RS-232C interface on the system timing card. If a disc interface card is

then installed in slot 2, it has a higher priority than the printer, which still maintains a higher priority than the RS-232C interface. Slots 7 and 6 are the next usable locations, each being of successively higher priority. Thus, priorities can be easily selected by choosing locations along the priority line.

If the optional RAM card is to be installed, it can be in any slot, without affecting priorities, because it generates no cycle requests of its own.

## 6-3. STRAPPABLE OPTIONS.

## 6-4. MEMORY UTILIZATION OPTIONS.

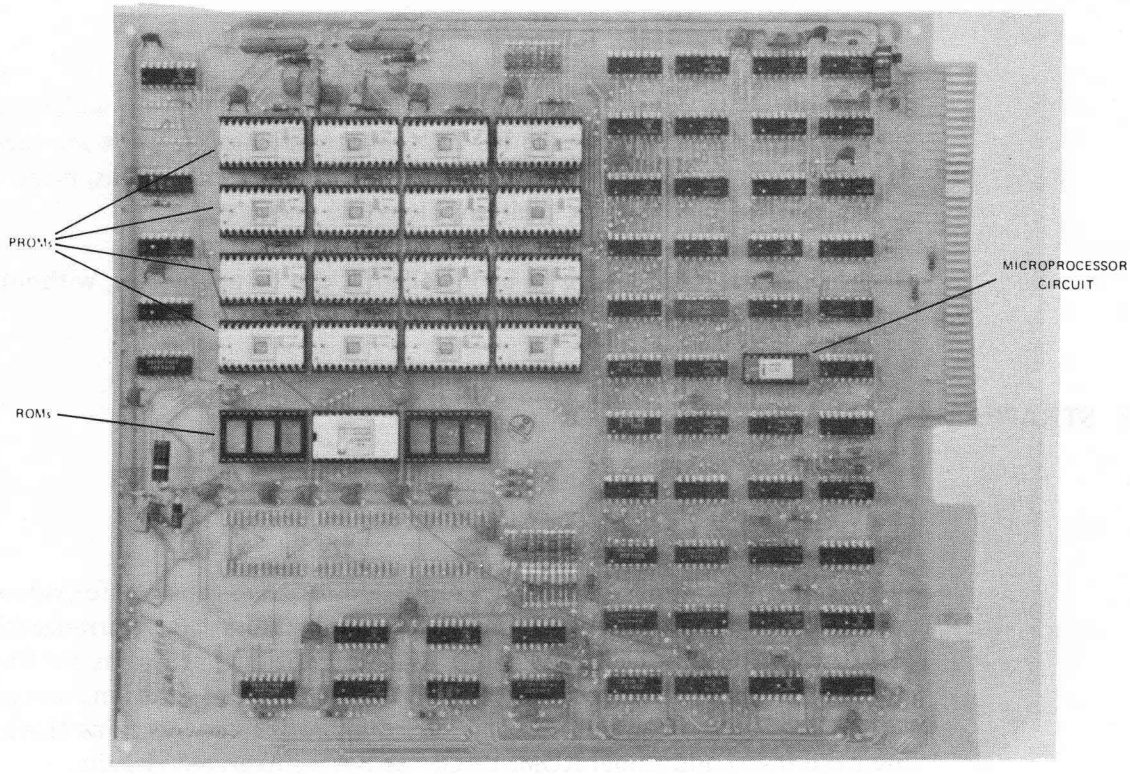
To install application oriented programs, add program capacity for video display, or for any other purposes, the microcomputer memory can be arranged in a variety of configurations. The Basic Program and any optional programs are stored within integrated circuits that are located at certain preassigned locations on circuit cards in the display console, but there also are numerous spare locations at which the user can insert additional ROM, PROM or RAM integrated circuits.

Before planning the utilization of available memory space, the user should be thoroughly familiar with the memory architecture and nature of the 9002 system programs. These are described in Chapter 1 and 4 of this manual, as well as in the Programmer's Language Manual, Part. No. 88-403-01.

The ROM/PROM segment of the memory is located on the microprocessor card [(a) of Figure 6-2] but up to 4K of the RAM segment is on the video/RAM card, Figure 5-2. Any additional memory is located on the optional RAM card.

The ROM/PROM segment stores microcomputer programs, but the RAM segment contains either a 2K or 4K block for storage of video display data, various preassigned working registers (used for purposes such as cursor control, special display effects, receiving data from the keyboard, etc.), and a small amount of general purpose memory. Figures 6-2(b) and 6-3 show the physical circuit layout in the ROM/PROM and RAM segments, as they are in a typical 9002 system. The layouts show location of the Basic Program integrated circuits chips, as well as those of a number of optional programs. Likewise, the map indicates all spare locations available for user programs.

Note that integrated circuit layout may vary from system to system, depending on the exact programs installed, as well as on other factors. The configuration shown in Figures 6-2 and 6-3 represents the Basic Program integrated circuits and those of some optional programs; the configuration is certain to be different if any special programs have been installed at the factory. Therefore, it is necessary to obtain a factory record of the configuration of each system that is to be modified and such information can be used in conjunction with that in this chapter.



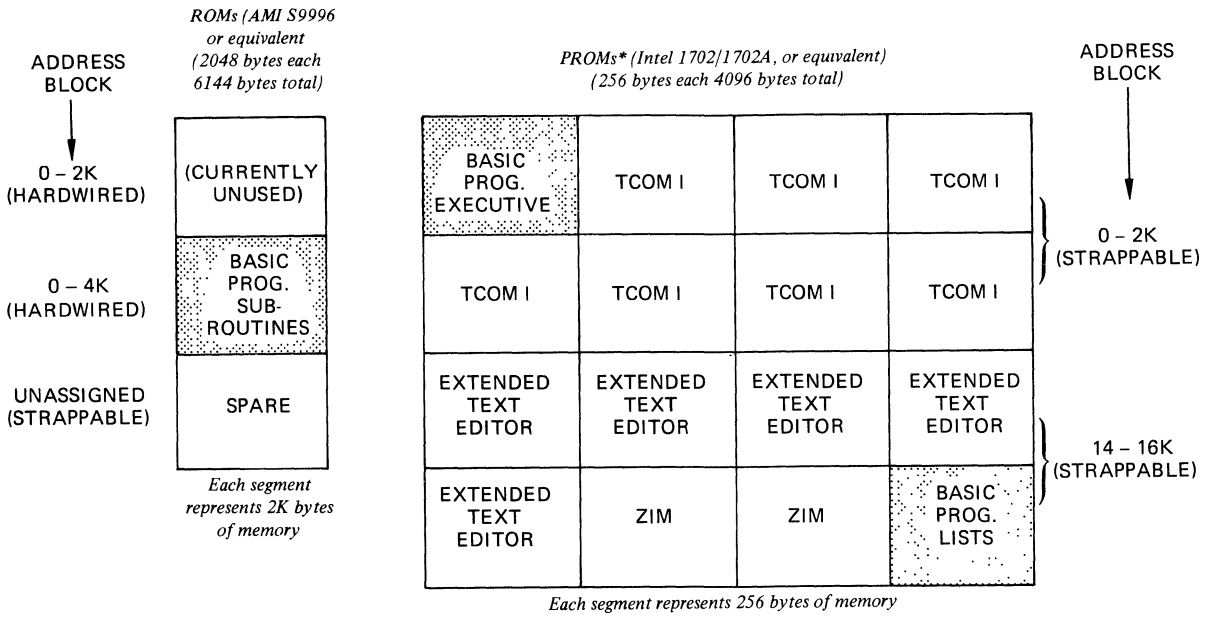

(a) Microprocessor Card

Figure 6-2. Read-only (ROM/PROM) Memory Segment.
(Sheet 1 of 2)

As shown in the memory map of Figure 4-3, the entire microcomputer memory is divided into address blocks each of 2K size. In Figure 6-2 and 6-3, the corresponding physical location of each address block is shown also. It is an important feature of the 9002 memory, however, that the physical integrated circuits can, with some exceptions, be reassigned to any address block within the memory by means of soldered interconnections (straps) on the circuit cards.

All strap locations are identified on Zentec Drawing No. 24-001-01, which is included at the rear of this manual.

As an example, the eight PROMs, identified as the 0-2K address block in (b) of Figure 6-2 can be reassigned as a group to any unoccupied 2K block of the entire 16K memory map. Likewise, any other group marked as strappable in Figures 6-2 and 6-3, can be reassigned to any location in the memory map. On the other hand, the two ROM locations, shown in Figure 6-2 as the 0-2K and 2-4K blocks, cannot be reassigned—they are hardwired to those particular address blocks.




*This memory can also consist of ROMs, provided they are electrically interchangeable with the PROMs.

(b) Typical Physical Layout of ROM/PROM Segment of Microcomputer Memory.

Figure 6-2. Read-only (ROM/PROM) Memory Segment. (Sheet 2 of 2)

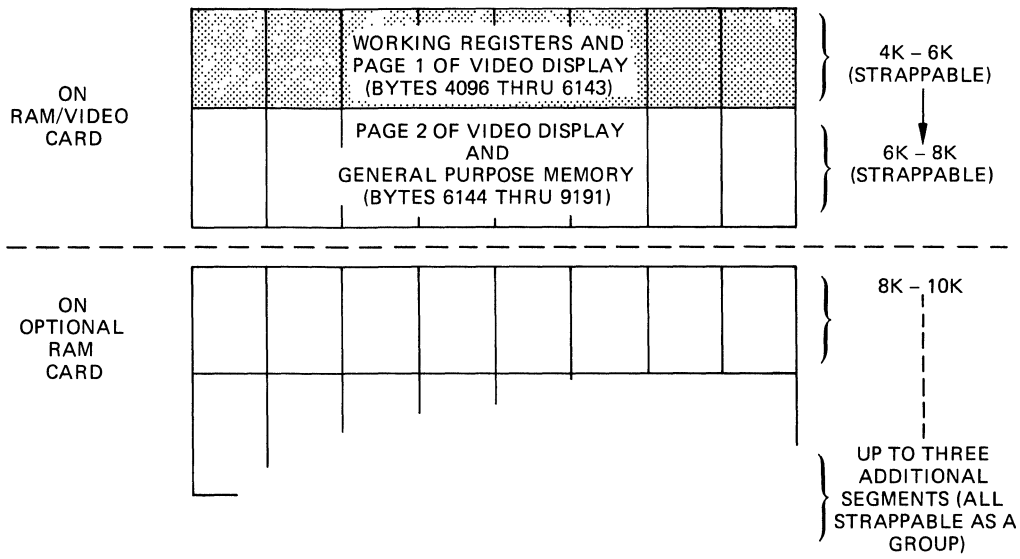
In considering the usage and address assignment of any RAM, ROM or PROM integrated circuits, several requirements must be observed. Most important, the Basic Program requires the assignments shown in the shaded circuit areas. That is, the Basic Program executive must always be in the first 256 bytes of the 0-2K memory block, the standard video display section must always be located in the 4-6K address block, and so on. (Any violation of these assignments would require a major reassembly of the Basic Program.)

All circuit locations not shaded in Figures 6-2 and 6-3 are available to the user, as long as the indicated options are not installed. Note, however, that since the PROMs must be assigned to address blocks in groups of eight, all PROM addresses are predetermined in the memory configuration shown in Figure 6-2. Likewise, the 2-4K lbock is always occupied by the ROM. This leaves the third ROM location and all of the optional RAM available for user assignment. All options

shown are bound to the locations indicated also, although in some cases their programs may be altered more easily, if necessary.

There is one further feature that adds flexibility to memory usage in certain situations. It is referred to as memory overlaying. The way memory overlaying works can best be shown by an example. Suppose, in a particular system there is only the Basic Program, but the optional RAM card is installed and one group of integrated circuits on the RAM card is assigned to the 14-16K address block. Because the second group of eight PROMs is also assigned to the 14-16K address block (Figure 6-2), the Basic Program lists overlay the last 256 bytes of that 2K memory block. That is, if the microprocessor addresses any one of the last 256 memory locations, it will access the PROM, rather than RAM location. In all remaining areas of the block, where there are no PROMs installed, the microprocessor will access the RAM.

In general, memory overlaying works in such a manner that any PROM takes precedence over any RAM or ROM assigned to the same location and any ROM takes precedence over any RAM at the same location. (In the particular configuration shown in Figure 6-2, overlaying of a ROM by a PROM is not practical, unless a ROM is installed in the strappable location and assigned to the 14-16K block.) There is one last requirement related to the use of PROMs, that should




*Notes: 1. Each rectangle represents one 2048 x 1 RAM (AMS 6003, or equivalent).*
*2. See Figure 5-2 for a photograph of the RAM/video card.*

Figure 6-3. Physical Layout of RAM Segment of Microcomputer Memory

be clearly understood. To make any PROM circuit active, in addition to the address strap for the groups of eight, each PROM circuit must also be individually enabled by a separate strap. Therefore, there are two group address straps and 16 individual enable straps associated with the PROMs. This allows PROMs to be installed and individually used to overlay any number of 256 byte segments of a ROM or a RAM. The enable straps are identified on Drawing 24-001-01 also.

## 6-5. OTHER STRAPPABLE OPTIONS

Strappable options associated with circuits other than memory are listed below. Detailed information regarding implementing these options is available from Applications Engineering Department at Zentec. (Note that still other options which may involve strapping are described in Chapter 1.)

**RS-232C Options.** In the RS-232C interface circuits on system timing card, both parity and word length can be selected with straps. There can be even, odd, or no parity. Word length can be either 5, 6, 7, or 8 bits, although all other circuits in the 9002 system are for 8-bit words.

**Fixed Baud Rate Option.** To disable the back panel BAUD RATE select switch and fix the baud rate to one certain value between 110 and 9600 baud, a strap is available on the system timing card.

**Character Generator Options.** In the standard 9002 system the character generator is one ROM integrated circuit. There is, however, space for installing two integrated circuits. This is usually done to increase the number of displayable characters, or to change the character set. These straps are located on the video/RAM card.

**Control Word Disable Option.** To disable the special display effects codes (see Figure 4-9), a strap on the video/RAM card can be used. This will eliminate all codes shown in Figure 4-9 and the characters will be displayed in normal manner. This option can be used with an expanded character set (and a special character generator).

**Control Character Display Option.** There is a strap on the video/RAM card which allows the special display effects control characters shown in Figure 4-9 and any other characters preceded by 100 in the most significant bit positions to be displayed on the screen. This requires a special character generator to interpret the codes.

## 6-6. INTERFACE DESIGN

There are three operations the user can perform using the system bus:

RAM Access
CPU Input/Output
CPU Interrupt

The following paragraphs describe these operations and define the rules any user must follow to use the system bus.

## 6-7. RAM ACCESS.

The 9002 system bus, see Figure 4-1, consists of a 16-bit address lines and 8-bit data lines, along with timing and control signal lines. The address and data lines operate at TTL data levels, open collector. The polarity of the signals is ground true; OV = logic 1, and +5V = logic 0.

The address and data bus timing is structured around the RAM memory cycles. The three clocks required for a memory cycle are Clock 1, Clock 2, and Clock 3. Referring to Figure 6-4 a memory cycle is defined as an interval from the lagging edge of Clock 3 to the lagging edge of the next Clock 3. Any device may read from or write in the RAM bysputting the address on the bus during a memory cycle which is not being used by any other device along with a Read Data signal or a Write Data signal. A bus priority structure exists to inform the user when the bus is free.

The CPU has first priority and whenever the CPU is using the bus, it outputs CPU Bus Request signal on the bus in the same memory cycle as it outputs Read Data or Write Data. The CPU Bus Request signal informs all other users to relinquish that cycle.

Second priority is assigned to the Memory Refresh Request signal. This signal is issued to refresh the MOS RAM integrated circuits and all peripheral users must relinquish the bus during its presence.

The third priority item is Character Refresh. During this time, all peripheral users must relinquish the bus. Character Refresh may occur up to 80 memory cycles in a row, and thus uses approximately 20 percent of the available memory cycles (see also Figure 4-5).

All users accessing the RAM must output a Peripheral Bus Request, along with a Read Data or Write Data signal. To resolve contention among users, a priority scheme exists. Figure 6-5 shows a circuit for resolving bus priorities. This circuit allows any peripheral device to use any memory cycle during which the bus is not occupied by a higher priority circuit. If one peripheral in a slot to the left of the

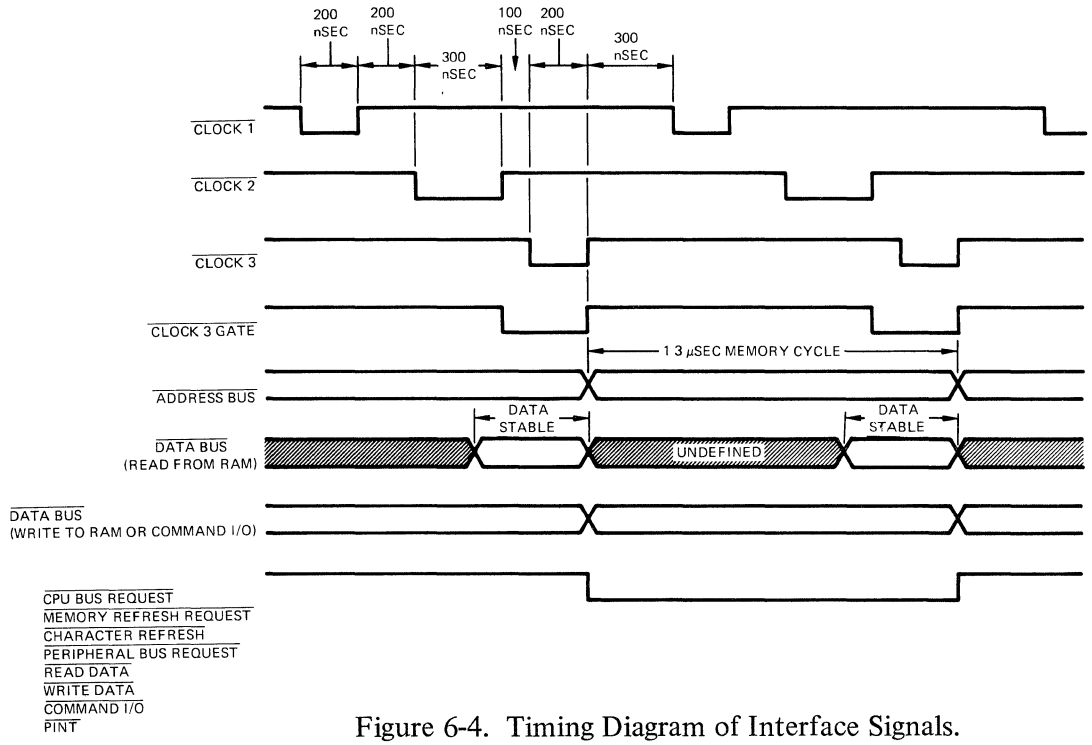



Figure 6-4. Timing Diagram of Interface Signals.

second peripheral (when viewing the card cage from the front, as in Figure 6-1) transmits a Peripheral Bus Request signal, the second peripheral interface circuit must pass this signal through pin A48 to the next card. If the first peripheral does not transmit a Peripheral Bus Request, the second may use the bus and must generate a Peripheral Bus Request of its own to output on pin A48 to the next card.

In the 9002 system, slot 5 is reserved for the system timing card, and its peripheral circuit (RS-232C interface) has the lowest priority. The peripheral priorities in ascending order are: slot 5, 4, 3, 2, 7, and 6, see Figure 6-1. Slot 1 is reserved for the video/RAM card and has no peripherals interfaces on it. Slot 3 is reserved for the microprocessor card and the Peripheral Bus Request on this card is a straight wire from pin A38 to A48. Any user designed card not using the Peripheral Bus Request (such as a card using only Command I/O) must pass the Peripheral Bus Request through in a like manner.

In order to use the bus, the user must apply the Address, Peripheral Bus Request and Read Data or Write Data signals, all for one entire memory cycle. If it is a write data operation, the data must be applied to the bus for the entire interval. If it is a Read Data operation, the data is not be valid until just prior to the lagging edge of clock 2 and remains valid until just past the lagging edge of clock 3.

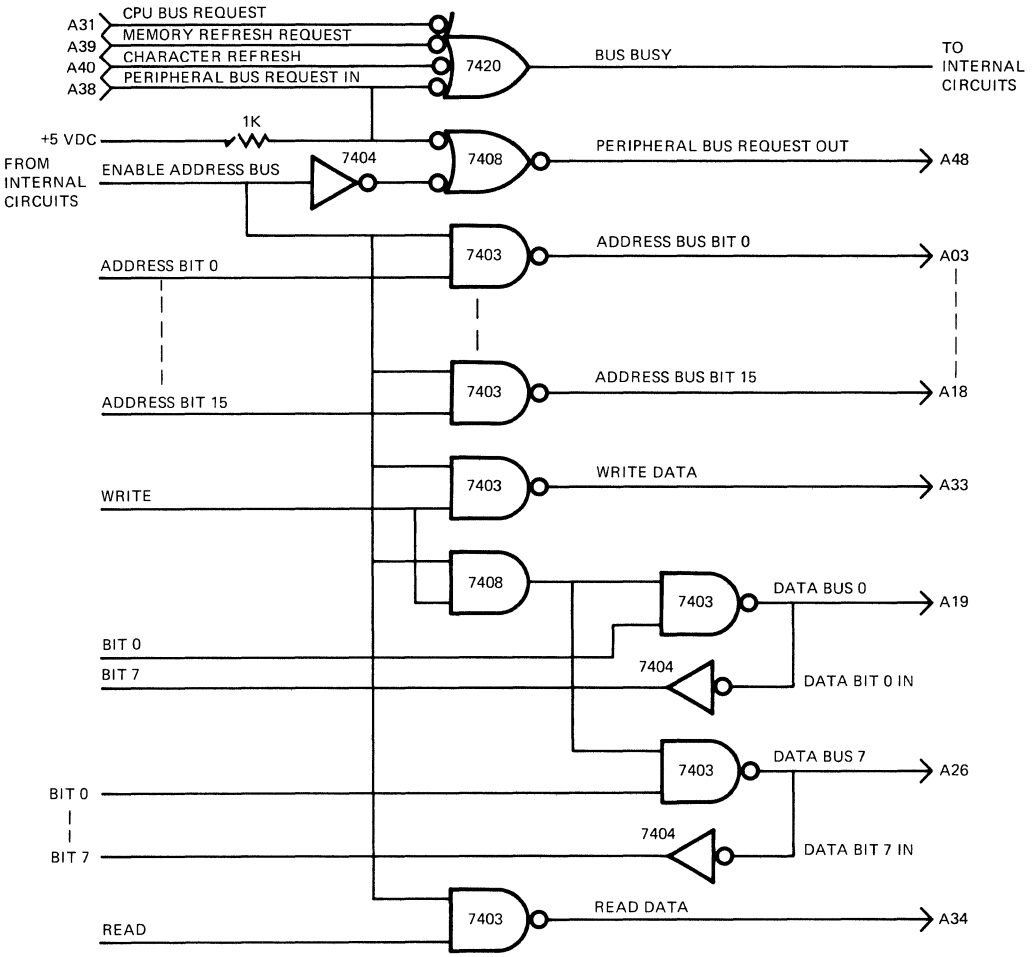
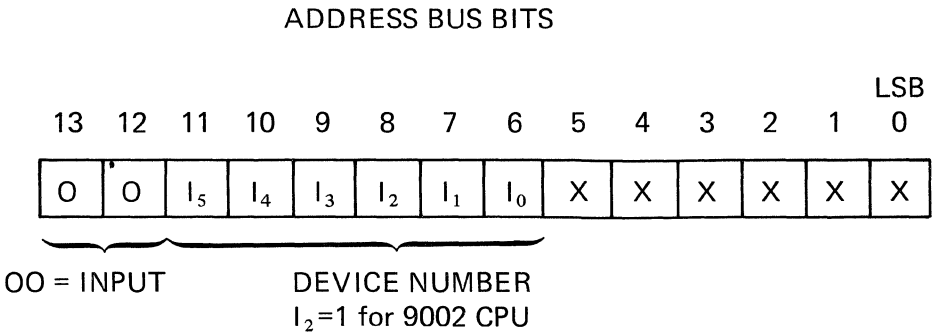


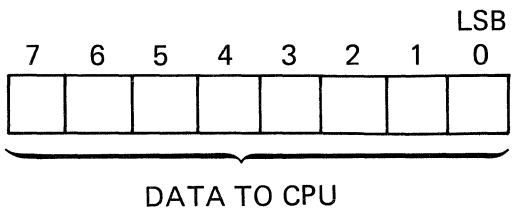

Figure 6-5. Logic Diagram of Bus Request, Address, and Data Circuits.

## 6-8. COMMAND INPUT/OUTPUT OPERATION.

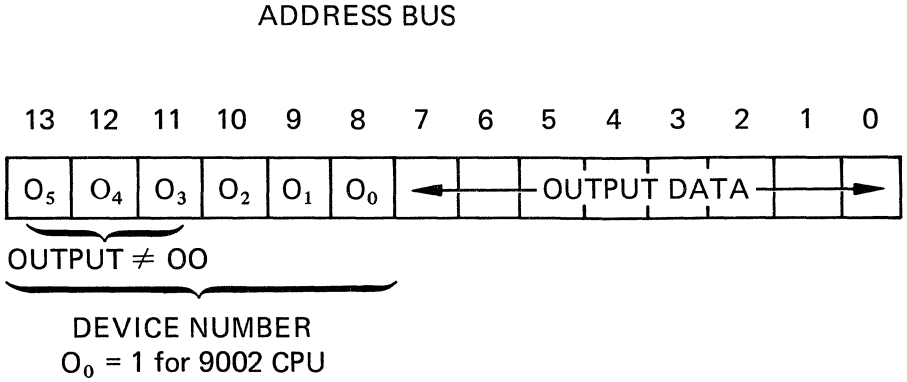
The user may make use of the Command Input/Output instructions of the 9002 CPU. When the CPU executes a Command Input/Output instruction, as a result of a users Command I/O Interrupt, it outputs CPU bus request, along with Command I/O signal (see Figure 6-4). The user must decode bits 12 and 13 of the address bus to determine if it is a CPU input or an output.

When the user has received Command I/O and has decoded bits 12 and 13 and determined that a CPU input command exists, bits $I_0$ through $I_5$ must be decoded to determine if the command is for the user's device. If it is, the data shall be returned to the CPU via the data bus all during the Command I/O time. Note that address bus bits 0 through 7 are the contents of the accumulator at the time the input command is executed. Care must be taken to load the accumulator with the proper value before starting the Command I/O operation, because bits 7 and 6 are part of the device number.




Shown below is the format for the output command:




When a Command I/O is received by the user, and bits 12 and 13 are not both zero, it is a ZPU output command and the user must decode $O_0$ through $O_5$ to determine if the command is for his device. If it is, the data from the CPU is on bits 0 through 7 of the address bus. The data is stable well before the leading edge of clock 1 and remains stable until after the lagging edge of clock 3.

## 6-9. INTERRUPT.

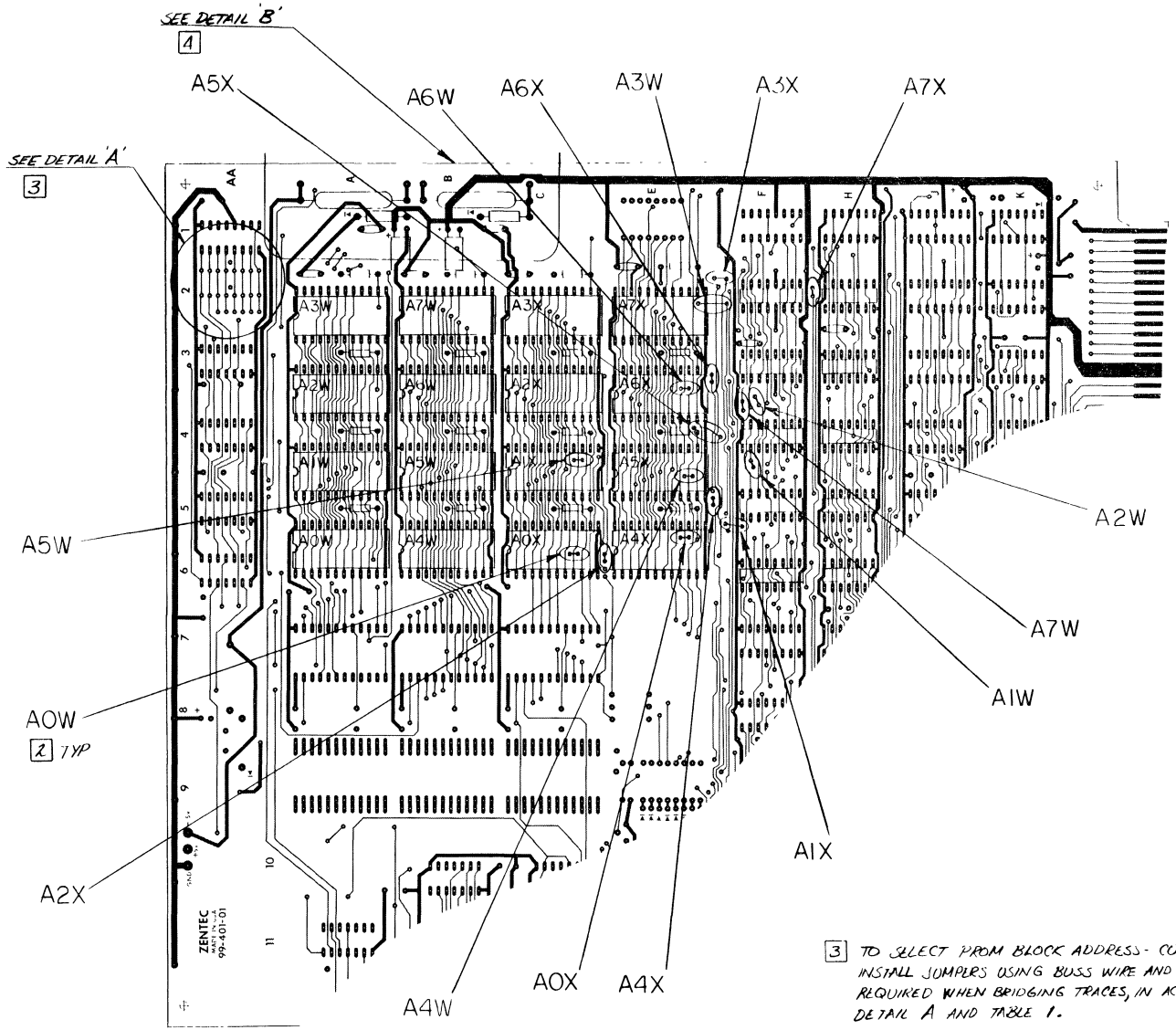
The interrupt capability is presently not used in the 9002 system. It can be implemented by the user to perform a one-wrod interrupt (usually restart). To

use the interrupt, the user must set the outgoing interrupt line (pin A50) synchronously with the lagging edge of clock 3. When a signal called PINT is received, the user must reset the interrupt line and send the interrupt instruction over the data bus during the PINT interval. For users not using interrupt, the card must feed through the interrupt signal from pin A37 to pin A50.

## 6-10. GENERAL PURPOSE CARD.

Zentec Corporation has a general purpose wirewrap card (Assy. 99-409-01) available, built to fit the 9002 display console card cage. It will hold standard dual-in-line sockets with pins on 0.1 inch centers, spaced in multiples of 0.3 inches.

This card is shown in the corresponding assembly drawing in back of the manual. The A connector mates with the system bus, and the B and C connectors can be used to interface with external equipment—either directly or via the back panel connector panel of the display console.




NOTES:

1. ALL OF THE COMPONENTS NORMALLY INSTALLED ON THE MICROPROCESSOR ASSY. ARE NOT NECESSARILY SHOWN.

2. PROM ENABLING JUMPERS TO BE INSTALLED USING BUSS WIRE AND SLEEVING, AS REQUIRED WHEN BRIDGING TRACES, IN LOCATIONS INDICATED. ONE JUMPER REQUIRED FOR EACH PROM LOCATION USED. JUMPER IDENTIFICATION IS REFERENCED TO PROM REFERENCE DESIGNATION (i.e. A0W).

3. TO SELECT PROM BLOCK ADDRESS - CUT TRACES AND INSTALL JUMPERS USING BUSS WIRE AND SLEEVING, AS REQUIRED WHEN BRIDGING TRACES, IN ACCORDANCE WITH DETAIL A AND TABLE 1.

4. SELECT VALUE OF RESISTORS R1 & R6 IN ACCORDANCE WITH DETAIL B AND TABLE 2.

| APPLICATION | |
|---|---|
| NEXT ASSY | USED ON |
| 10-XXX-XX | 9002 |

UNLESS OTHERWISE NOTED
DIMENSIONS ARE IN —
ANG | 2 PLC | 3 PLC | —
± — | ± — | ± —
SCALE 1:1
MATERIAL SEE [illegible] IN NEXT ASSY

DWN [illegible] 11/5/74
CHK [illegible] 11/8/74
ENGR [illegible] 11/8/74
APPD [illegible]
APPD [illegible] 12/4/74
APPD [illegible] 11/15/74
FINISH —

| ENGR CHANGES | | | | |
|---|---|---|---|---|
| REV | CHG NO | DATE | APPD | |
| | | | | |

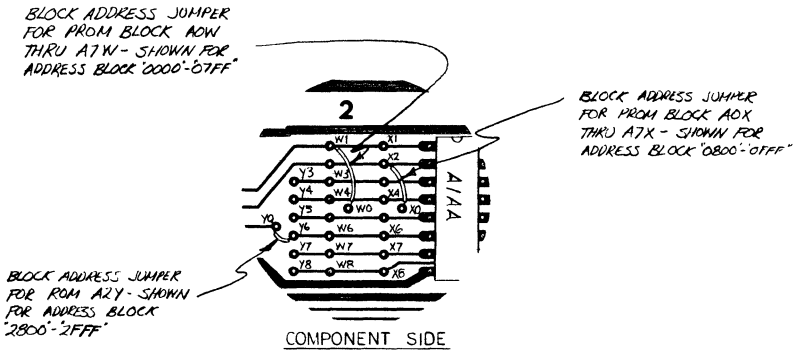
DO NOT SCALE DRAWING

ZENTEC ZENTEC CORPORATION SANTA CLARA CALIFORNIA

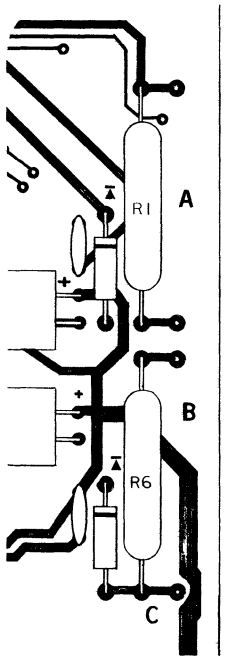
TITLE INSTRUCTION, MICROPROCESSOR PROM ADDRESSING

SIZE C | SHT 1 OF 2 | DRAWING NO 24-001-01 | REV A

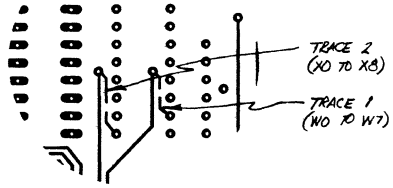
FORM NO 75-000-08




COMPONENT SIDE




DETAIL 'B'




SOLDER SIDE

DETAIL 'A'

TABLE 1

| BLOCK ADDRESS (HEXIDECIMAL) | PROM BLOCK (A0W THRU A7W) ADD JUMPER FROM | PROM BLOCK (A0W THRU A7W) ADD JUMPER TO | PROM BLOCK (A0X THRU A7X) ADD JUMPER FROM | PROM BLOCK (A0X THRU A7X) ADD JUMPER TO | ROM (A2Y) ADD JUMPER FROM | ROM (A2Y) ADD JUMPER TO |
|---|---|---|---|---|---|---|
| '0000'-'07FF' | W0 | W1 | X0 | X1 | N/A | N/A |
| '0800'-'0FFF' | ↑ | W2 | ↑ | X2 | N/A | N/A |
| '1000'-'17FF' | ↑ | W3 | ↑ | X3 | Y0 | Y3 |
| '1800'-'1FFF' | ↑ | W4 | ↑ | X4 | ↑ | Y4 |
| '2000'-'27FF' | ↑ | W5 | ↑ | X5 | ↑ | Y5 |
| '2800'-'2FFF' | ↑ | W6 | ↑ | X6 | ↑ | Y6 |
| '3000'-'37FF' | ↓ | *W7 | ↓ | X7 | ↑ | Y7 |
| '3800'-'3FFF' | W0 | W8 | X0 | **X8 | Y0 | Y8 |

* USE TRACE 1 ** USE TRACE 2

TABLE 2

| PROM BLOCK & RES. REF. | LOCATIONS A0W THRU A7W — R1 — | | LOCATIONS A0X THRU A7X — R6 — | |
|---|---|---|---|---|
| NO. OF PROMS | P/N | DESCRIPTION | P/N | DESCRIPTION |
| 0, 1, 2 | 80-250-03 | RES, WIRE WOUND, 30Ω, 5W, 5% | 80-250-03 | RES, WIRE WOUND, 30Ω, 5W, 5% |
| 3, 4, 5 | 80-250-01 | 20Ω | 80-250-01 | 20Ω |
| 6, 7, 8 | 80-250-04 | 15Ω | 80-250-04 | 15Ω |

| APPLICATION NEXT ASSY | APPLICATION USED ON | UNLESS OTHERWISE NOTED DIMENSIONS ARE IN — | DWN | ENGR CHANGES REV | CHG NO | DATE | APPD |
|---|---|---|---|---|---|---|---|
| | | ANG ± — 2 PLC ± — 3 PLC ± — | CHK | | | | |
| | | SCALE | ENGR | | | | |
| | | MATERIAL | APPD | | | | |
| | | | APPD | | | | |
| | | | APPD | | | | |
| | | | FINISH | DO NOT SCALE DRAWING | | | |

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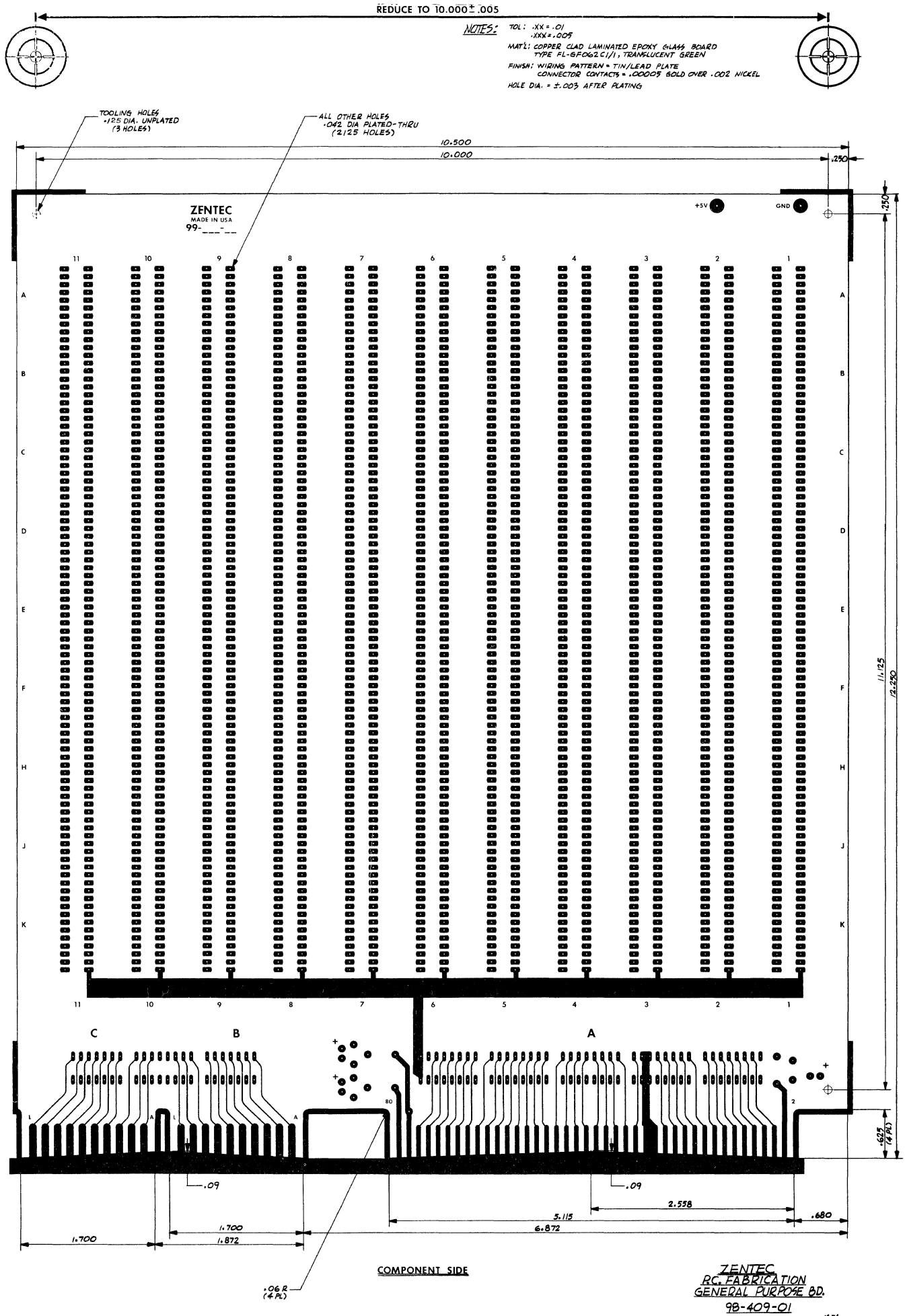
TITLE: INSTRUCTION, MICROPROCESSOR PROM ADDRESSING

SIZE C | SHT 2 OF 2 | DRAWING NO 24-001-01 | REV A

FORM NO 75-000-08


REDUCE TO 10.000 ± .005
NOTES:
TOL: .XX = .01
.XXX = .005
MAT'L: COPPER CLAD LAMINATED EPOXY GLASS BOARD
TYPE FL-GFOG2 C1/1, TRANSLUCENT GREEN
FINISH: WIRING PATTERN = TIN/LEAD PLATE
CONNECTOR CONTACTS = .00003 GOLD OVER .002 NICKEL
HOLE DIA. = ±.003 AFTER PLATING
TOOLING HOLES
.125 DIA. UNPLATED
(3 HOLES)
ALL OTHER HOLES
.042 DIA PLATED-THRU
(215 HOLES)
10.500
10.000
.250
ZENTEC
MADE IN USA
99-___-___
+5V
GND
11 10 9 8 7 6 5 4 3 2 1
A B C D E F H J K
C B A
11.125
12.250
.625
(4 PL)
.09
.09
2.558
5.115
6.872
.680
1.700
1.700
1.872
.06 R
(4 PL)
COMPONENT SIDE
ZENTEC
RC. FABRICATION
GENERAL PURPOSE BD.
98-409-01