NoteTaker

A Portable Computing System

XEROX PALO ALTO RESEARCH CENTER
Systems Science Laboratory
LSI Systems Area
March 6, 1978

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Subject: **NoteTaker Project Plan**

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This is a plan to design and prepare for production a portable computing system called NoteTaker. The custom LSI processor components of this system will be suitable for emulating both Mesa and Smalltalk. As such they can form the nucleus of a D0/LSI system as well. There are several significant problems addressed by this project of which the following are most important.

- Many groups within PARC, principally LRG, have long expressed an interest in obtaining a portable computing system of substantial power to further study how individuals can make use of computers as personal tools. This is such a system.

- The need for a low cost alternative to the D0/MSI system is real and immediate.

- The LSI group needs to go through the process of developing a significant LSI based system to truly understand the problems of design and testing.

- The reality of a powerful but small LSI computing system will better bring home the potential of custom LSI to PARC and the rest of the Corporation.

This project is a significant undertaking but will be well worth the time and energies spent. The project will offer a unique opportunity for members of different organizations to collaborate on a common project. It is anticipated that participants will come from SSL, CSL, ADL, EOD, and ASD.

Because in some respects the needs of the NoteTaker program and those of the D0/LSI program are in conflict, we can anticipate some problems. One need is to develop a set of LSI components which can be included in the NoteTaker system during the second quarter of 1979. The second requirement is that these LSI components be suitable as building blocks for the D0/LSI system. This latter system will not be available until 1980 or '81, however. In addition, the NoteTaker is not required to meet the stringent performance requirements of the D0. The necessity to resolve the differing time and performance goals of these systems can benefit both groups if handled reasonably. The D0 effort will keep the NoteTaker from addressing too narrow of problem space, while the time demands of the NoteTaker project will force D0 design decisions to be made in a timely fashion.

A description of the system and its design goals, as well as the design team, follows.

1.0 System Components

The basic components of the NoteTaker system will be as follows:

- 16 bit microporgrammed LSI processor with instruction fetch unit and cache memory

- A minimum of 128K words (16 bits) of main memory

- A mini-floppy disk capable of storing about 340K bytes of data.

- A 7" diagonal CRT displaying 640 dots horizontally and 480 dots in the vertical direction. This provides a resolution of about 118 dots/inch.

- A standard keyboard, essentially identical to the Alto I keyboard.

- A pointing device, hopefuly a tablet.

- A power system capable of powering all components which are included within the package. The peak demand of the system is about 80 watts. There will be space for batteries within the package. It is expected that The system can be run on the batteries for about 3 hours at a time. A recharging system will be built into the power supply.

- An EIA interface for general purpose communications needs.

- A modem capable of operation at up to 600 bps (possibly 1200bps). It is intended that this modem have an attachment which will allow it to connect directly to the mouthpiece of any standard telephone.

- An external bus interface which will allow other devices to be connected to the NoteTaker. One of the most important of these devices is an Ethernet interface. This interface is planned to be external because it will only be needed when the unit is actually near the ethernet itself. There seems no point in carrying the interface and its power requirements with the machine all the time.

- The architecture of the system wll be such that a small number of processors can be operated in parallel. Although these extra processors will not fit within the package, the system will offer a useful test-bed for experimenting with multi-processor architectures.

- The package will be about 18" wide, 14" deep, and 6" high. The total weight without batteries will be less than 25 lbs. A goal is to make the weight 20 lbs. or less.

2.0 System Architecture

A preliminary block diagram of the NoteTaker system is shown in Appendix A. There are three basic subsystems. One is the LSI processor which will be constructed principally from custom LSI chips. This subsystem will be composed of an ALU chip, perhaps two control chips, two address mapping chips, an IFU, and a cache holding 1K-2K words of local state. The custom chips will contain their own RAM control memory. The cache itself will likely consist of standard components. Of the other four chip types, only three will be designed and fabricated during the first phase of the project. These are the ALU, the Control, and address mapping chips. The IFU will be added as time is available. For a description of the basic architectural principals of this processor, see the memo "A VLSI Microprogrammed Processor", by C. Thacker.

The memory subsystem is the second important element in the NoteTaker. This main memory will be constructed of 16K dynamic RAMs and will include single-bit error correction and double-bit detection. There will be a minimum of 128K words of memory. This number will grow to 512K when 64K memory chips become available. The memory controller will consist of standard integrated circuits.

The memory will be organized as 32K quadwords (64 bits). The error correction will thus be done over a 64 bit word. Transfers between processors or the I/O system and memory will be either single words(16 bits) or integer numbers of quadwords. The

memory can transfer data at the rate of about 1 word every 100ns. The fraction of this 160 mbs bandwidth which will actually be available is not specified yet.

The third important building block of the system is the I/O section. Here we will make use of as many standard LSI components as possible. The I/O system will be controlled by a processor such as the Intel 8086. This I/O processor will handle much of the overhead associated with setting up and completing I/O transfers. The communication between the I/O section and the emulation (custom LSI) processor will be handled through main memory.

The system will be designed such that one can attach multiple processors to the common memory bus. This capability will allow us to explore the problems and opportunities of a multiprocessor system.

The performance of this system in terms of instruction execution speed will be in the same class as the current D0/MSI machine. The micro-cycle will be less than 150 ns. and could possibly be under 100 ns. when the design matures and circuit bottlenecks are removed.

3.0 The LSI design team

This project offers an exceptional opportunity for the systems, circuit, and process designers in PARC and EOD to work together *from the beginning* to develop a powerful set of LSI components.

This will be a very important project for the LSI effort at PARC. The LSI group at PARC has been working in integrated circuit design for about 1 1/2 years. The time is right to apply the tools and knowledge we have developed to a significant problem. We have much to discover about how such an LSI project should be organized, what types of documentation are most useful to the designer, where the real bottlenecks in design process are when using the structured design approach, and what the tradeoffs are in the area of structured design vs. the desire for maximum speed and density.

The small group that is being put together for this project will include individuals from various backgrounds and skills. We feel this experiment of using a tightly coupled group to do a major LSI project will be most educational to all participants. It is just this type of effort which will be essential in developing the truly powerful integrated systems of the future.

4.0 Design Strategy

All the chips will be layed out using the ICARUS design system. The design rules chosen will most likely be those of the NSIL II process. They may be scaled up initially to meet the requirement that we be able to run under a relaxed set of rules if the new process is not available in time.

There will be a conversion program developed to allow the transfer of data from the ICARUS system to the Calma system. This will provide a convenient backup position if ICARUS should become a limitation and it will also allow us to make use of the design rule checking and pattern generation programs which are available in El Segundo.

The overall chip size will be about 40 mm^2 (6.25 mm on a side). This size is chosen on the basis of yield considerations and power dissipation. Each chip can't be allowed to dissipate greater than about 1 watt. In connection with this, there is consideration being given to running the chips at 3 volts instead of 5 volts to minimize power dissipation and increase speed.

In order to debug the design and checking process, which will involve conversion of ICARUS files to Calma format and checking them, we will want to design one or two relatively small circuits to run through the process in mid-summer. These chips will be a display controller chip and a preliminary version of the memory mapping chip. These circuits will be designed using the NSIL I design rules, as it is likely that the new process

will not be available by then.

4.1 IC Fabrication

As has been the case with other circuits designed at PARC and in EOD/MEC, we do not wish to so closely tailor our designs to a process that the chips can only be fabricated on one line. The MEC line will be runnning the new NSIL II process by the time we need to actually fabricate chips in the fall. Dirk Bartelink will likely have such a process available at about the same time. We would be happy to make use of whichever line is available at the time. We also anticipate that in 1979 that there will be lines in other semiconductor processing firms which are capable of processing our chips as well. Eventually we will want to move the production of the chips to an outside facility as was done with the LCC.

5.0 The NoteTaker Design Team

Designing the appropriate LSI chips is only part of the NoteTaker design problem. I will be relying on a great deal of help from EOD/SPG in the area of system electronics and packaging design. The principals in the project from that group are Ed Wakida, Bob Nishimura, Jim Leung, and Ron Freeman. These people have already designed and built a mockup of the NoteTaker system with essential components in place. They have handled investigations into hybrid technology as well as keyboards, displays, power supplies, and packaging options.

The system electronics other than the processor will be designed by Ron Freeman and Jim Leung. Interaction with vendors on such components as power supplies and monitor will be handled by Ed Wakida. Design of an LSI controller for the CRT monitor will be done by Jim Leung.

6.0 System Packaging

A principal goal of the NoteTaker packaging effort is to avoid the mistakes made in the Alto packaging. The Alto terminal housings were engineered for very small lot production and were thus a constant headache when multiple builds of the machine occurred. The NoteTaker packaging is being done with the idea that at least 200 units will be built, possibly many more.

A mockup of the unit has already been completed. This mockup will be analyzed and modified over the next couple of months to determine the best overall packaging scheme. We will then build a prototype of the unit which will be as close to the final unit in terms of shape and materials as possible. We will exercise or simulate all the major components in this package to insure that we have adequately solved such problems as heat dissipation.

This prototype will again be analyzed and evaluated before final drawings and subsequent tooling is done. The final package design will be engineered for moderate volume production requirements.

7.0 Component and System Testing

The chips to be designed are large and very complex. Because of this, the testing strategy will have to be built into the chips.

The chips will be functionally tested on the Alto using the general purpose LSI system tester which will be built in the next three months. Detailed testing and characterization will probably be done on the Sentry system in El Segundo.

Checkout of the NoteTaker system excluding the processor can be done from the Alto as well. The memory and I/O system will be designed and checked out before the LSI processor chips are ready to plug in.

8.0 Design vs. Buy

The question of why we don't just buy what we want often comes up. The usual answer is of course that the systems we envision are not available on the market and are not likely to be in the near future. This is certainly true in this case with respect to the package, memory and I/O system, although it might still be argued that there will soon be an LSI processor available which might do our task sufficiently well.

This latter statement may be true in the case of the NoteTaker, at least to a limited degree. We could package the new Intel 8086 processor into the system which I have just described. This processor would not offer the performance of the Alto but it might be adequate for a limited set of applications. It is apparent that we can design a processor of significantly greater power ourselves, however. We will also learn a great deal about the design issues and we will have developed a base on which to design even more powerful processing elements in the future.

An alternative way of asking this question is "why not build our own chips"? The most common answer is that it is so difficult, time consuming, and expensive. We are interested in applying a more structured approach to the problem to see what benefits this technique offers. If it turns out that IC design can be simplified, and design time reduced, some of the reasons for not taking advantage of power of LSI in the future will be nullified.

9.0 Manpower Requirements

The basic manpower requirements of the project are shown below:

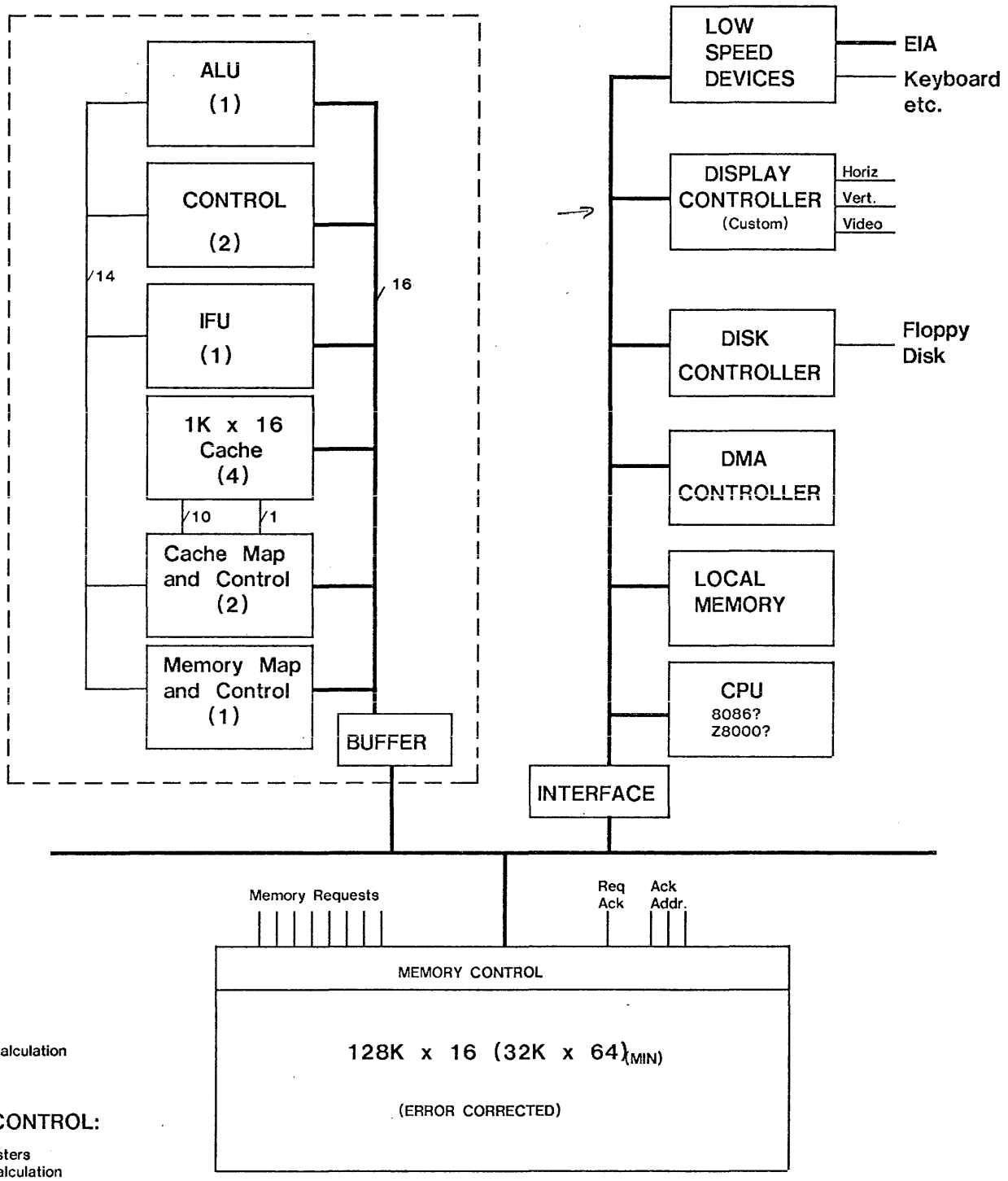
3 LSI designers - 24 man-months
2 Logic designers - 12 man-months
(System design, tester design, etc.)
2 Physical/Electrical packaging - 10 man-months
2 Programmers - 18 man-months
(Microcode, system simulations, I/O controller software, tester software.)
1 - Project coordinator - 6 man-months
1 - Engineer/Technician - 6 man-months
1 - Expiditer - 3 man-months

10.0 Schedule

The present schedule calls for the total package to be put together with the first working versions of the processor chips in April 1979. By this time, we should be set up to make several dozen of these machines.

The greatest uncertainties lie with the LSI chips. The schedule allows for the first batch to be wrong and four months to correct problems and turn the new designs around. The other system components and the packaging will be designed and readied for production so the systems can be produced when the first LSI chips become available.

Appendix A - Preliminary NoteTaker Block Diagram



ALU:

- Mesa Stack
- Shifter/Masker
- Arithmetic Unit
- 2 Registers

CONTROL:

- Next Address Calculation
- Subroutines

CACHE MAP/CONTROL:

- Mesa base registers
- Adder for VA calculation
- Map for cache: (21A+7D)64

CACHE:

- Can be either custom or off the shelf RAM.

MEMORY MAP/CONTROL

- Mesa base registers
- Adder for VA calculation
- Map for memory: (16A+12D)64W
- Strobes out memeory address in 8 bit bytes

IFU:

- Cache for 4 to 8 bytecodes
- Ability to put translate from bytecodes to microcode addresses
- Ability to place needed offsets on D bus from bytecode stream

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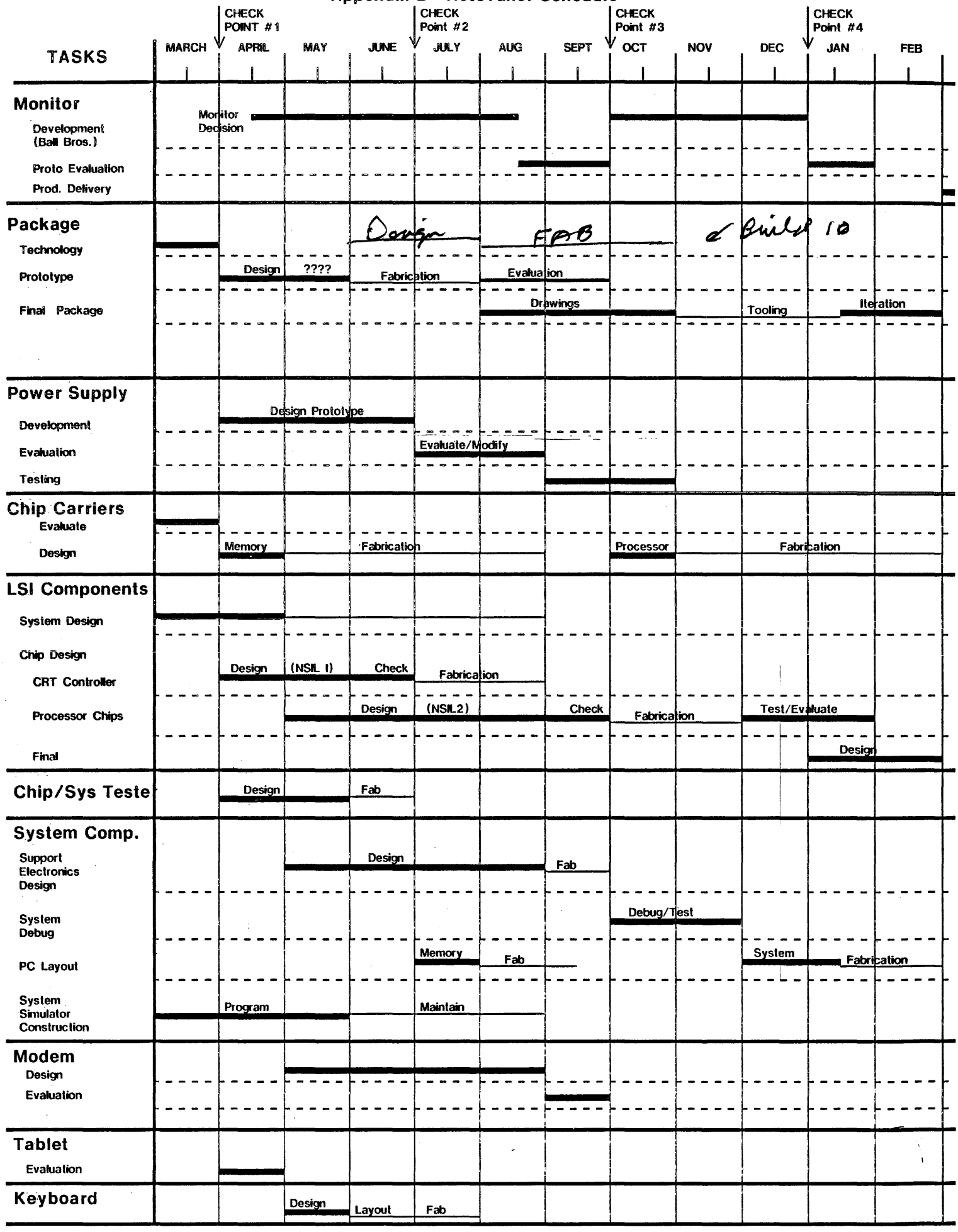
Appendix B - NoteTaker Schedule



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Appendix B - NoteTaker Schedule

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TASKS	MARCH	CHECK POINT #1 APRIL	MAY	JUNE	CHECK Point #2 JULY	AUG	SEPT	CHECK Point #3 OCT	NOV	DEC	CHECK Point #4 JAN	FEB
Monitor												
Development (Ball Bros.)		Monitor Decision										
Proto Evaluation												
Prod. Delivery												
Package												
Technology												
Prototype		Design	????	Fabrication		Evaluation						
Final Package						Drawings				Tooling	Iteration	
Power Supply												
Development		Design Prototype										
Evaluation					Evaluate/Modify							
Testing												
Chip Carriers												
Evaluate												
Design		Memory		Fabrication				Processor		Fabrication		
SI Components												
System Design												
Chip Design												
CRT Controller		Design	(NSIL 1)	Check	Fabrication							
Processor Chips				Design	(NSIL2)		Check	Fabrication		Test/Evaluate		
Final											Design	
Chip/Sys Tester		Design		Fab								
System Comp.												
Support Electronics Design				Design			Fab					
System Debug								Debug/Test				
PC Layout					Memory	Fab				System	Fabrication	
System Simulator Construction		Program			Maintain							
Modem												
Design												
Evaluation												
Tablet												
Evaluation												
Keyboard			Design	Layout	Fab							

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Appendix C - Preliminary NoteTaker Power Requirements

Subsystem	+5	+12(max/typ)	-5	Watts
Memory - 128K x 16 @ 400ns cycle	64 ma.	2.52A/1.9A	29ma	31/23w
@1 usec. cycle	32 ma.	1.5A/1A	29ma	18/12w
organized (32K x 64+8) (above assumes 72 chips cycle at once)				
Memory Interface	1A			5w
Mini-foppy disk drive	500ma.(typ)	1.35(typ)	0	18.7w(typ)*
Disk Interface	300ma.			1.5w*
Processor				
ALU	200ma.(max)			1w
Cache Control	200ma.(max)			1w
Cache Map	200ma.(max)			1w
Cache Mem (4 4K RAMs)	400ma.(max)			2w
Memory Map	200ma.(max)			1w
IFU	200ma.(max)			1w
Display		1A/750ma		12/9w
Controller	300ma.			1.5w
Keyboard	150ma.			.75w*
Low Speed Device Controller, etc.	500ma.			2.5w
Total: 400 ns memory cycle	4.22A	4.9A/4A	29ma.	80/69
1 usec. memory cycle	4.18A	3.9A/3.15		68/58w

The items marked with an * are those items which can be turned off for most of the time and will not affect long-term battery life if batteries are included. The total power at the slow memory cycle with these devices off is only 36 watts.

Power for - 80186
- I/O controllers
- Buffers on CSI Processor.

Appendix D - Preliminary System Weight Breakdown

Power Supply ----------	4.0 lbs.
Shugart MiniFloppy disk ----------	3.0 lbs.
7" Display Monitor w/ electronics -----	5.0 lbs.
Keyboard ----------	2.5 lbs.
4 PCBs with components ----------	3.0 lbs.
Backwiring board with connectors ------	1.0 lbs.
Pointing device ----------	0.5 lbs.
Harness and misc. hardware ----------	1.0 lbs.
Package ----------	5.0 lbs.
Total:	25.0 lbs.

Appendix E - Preliminary NoteTaker Cost Projections

	1979	1980(volume production)*
Monitor	$300	$100
Floppy Disk	$300	$200
Keyboard	$150	$100
Power Supply	$400	$200
Integrated Circuits		
144 16K RAMs	$1150	$750
6 LSI I/O	$300	$50
150 TTL @$2.00	$300	$100(more LSI perhaps)
Custom ICs		
1 ALU, 1 Control, 2 Maps, 1 Display Control @ $50	$250	$75
Housing	$250	$75
Printed Circuit Boards (4)	~~$300~~ 400	$150
Misc. Hardware (connectors, etc.)	$200	$150
Modem	$250	$50
Assembly and Test	$400	$200
Total:	$4550.-	$2200.-

*I include these 1980 figures for curiosity's sake.