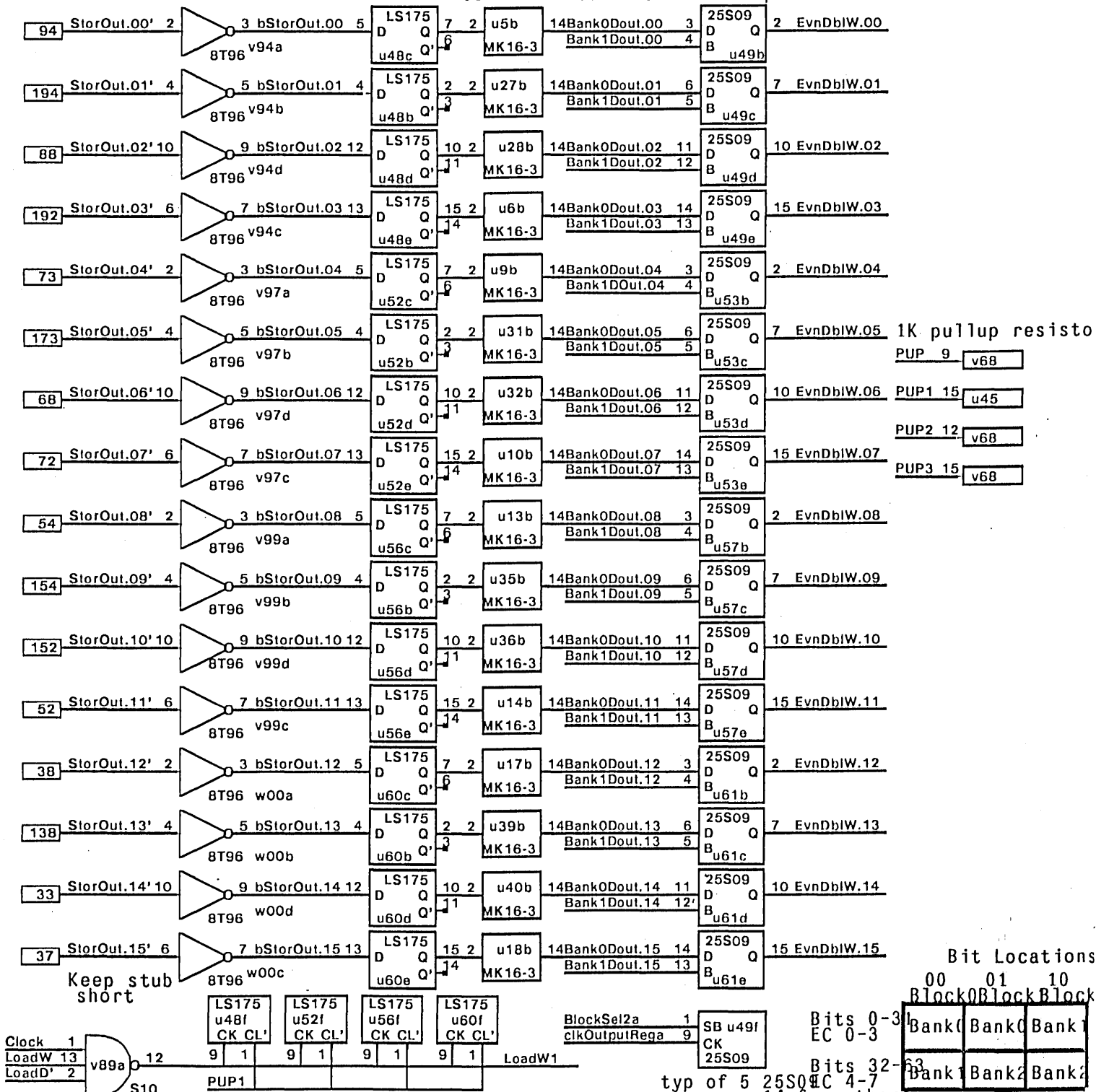
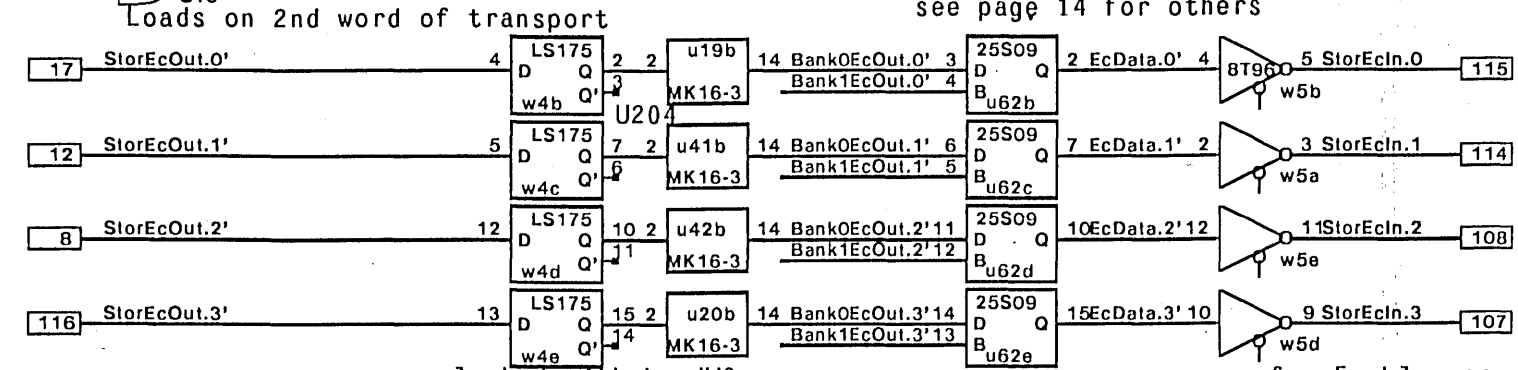


Block 0&1 bits 16-31 5 chips



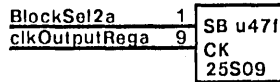
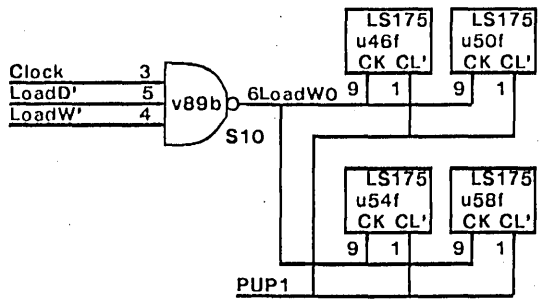
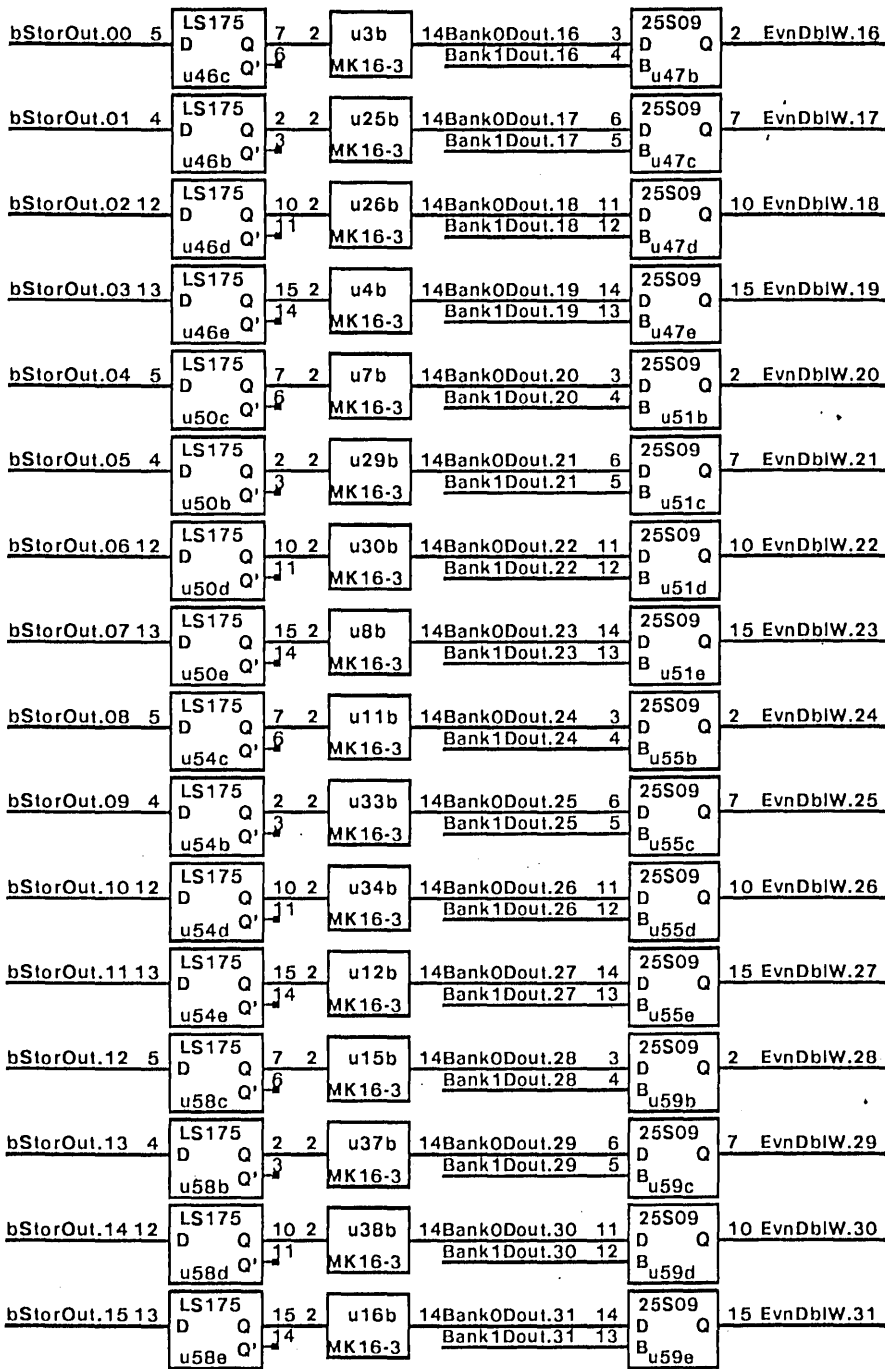
Bit Locations

00	01	10
Block0	Block0	Block1
Bank0	Bank0	Bank1
Bank1	Bank2	Bank2

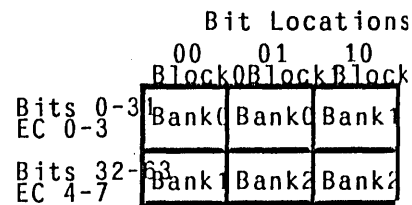


XEROX EOD	Project DO	Storage Card Bank 0, Most Significant Bits	File D0stor01.sil	Designer Rosen	Rev B	Date 1/26/80	Page 01
-----------	------------	--	-------------------	----------------	-------	--------------	---------

Block 0&1 bits 0-15

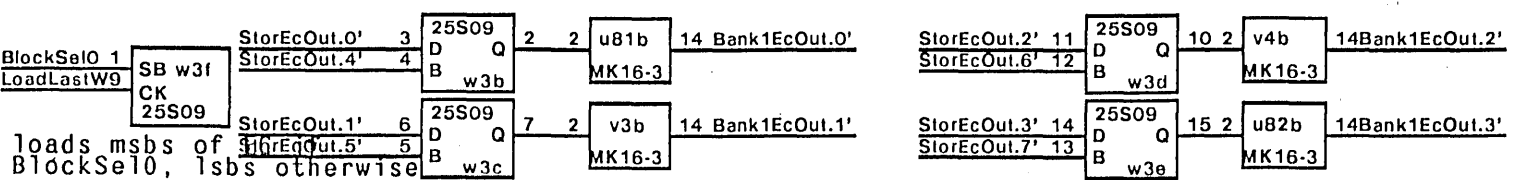
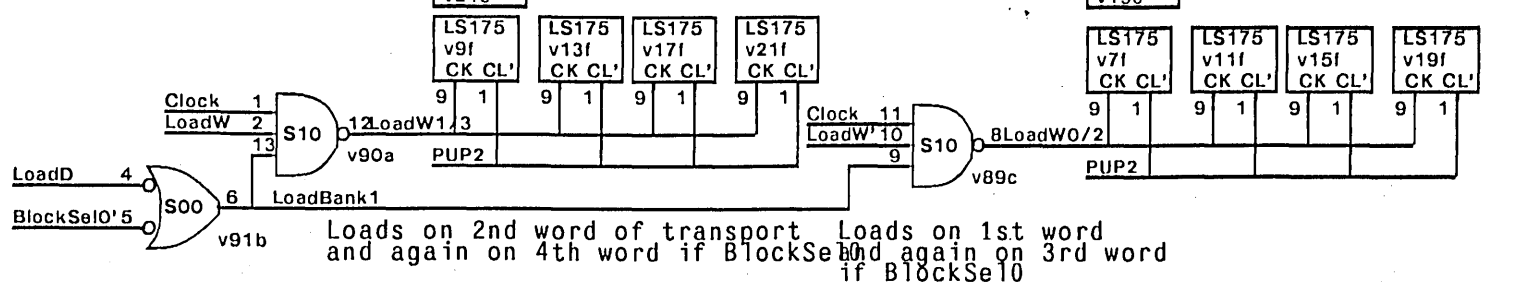
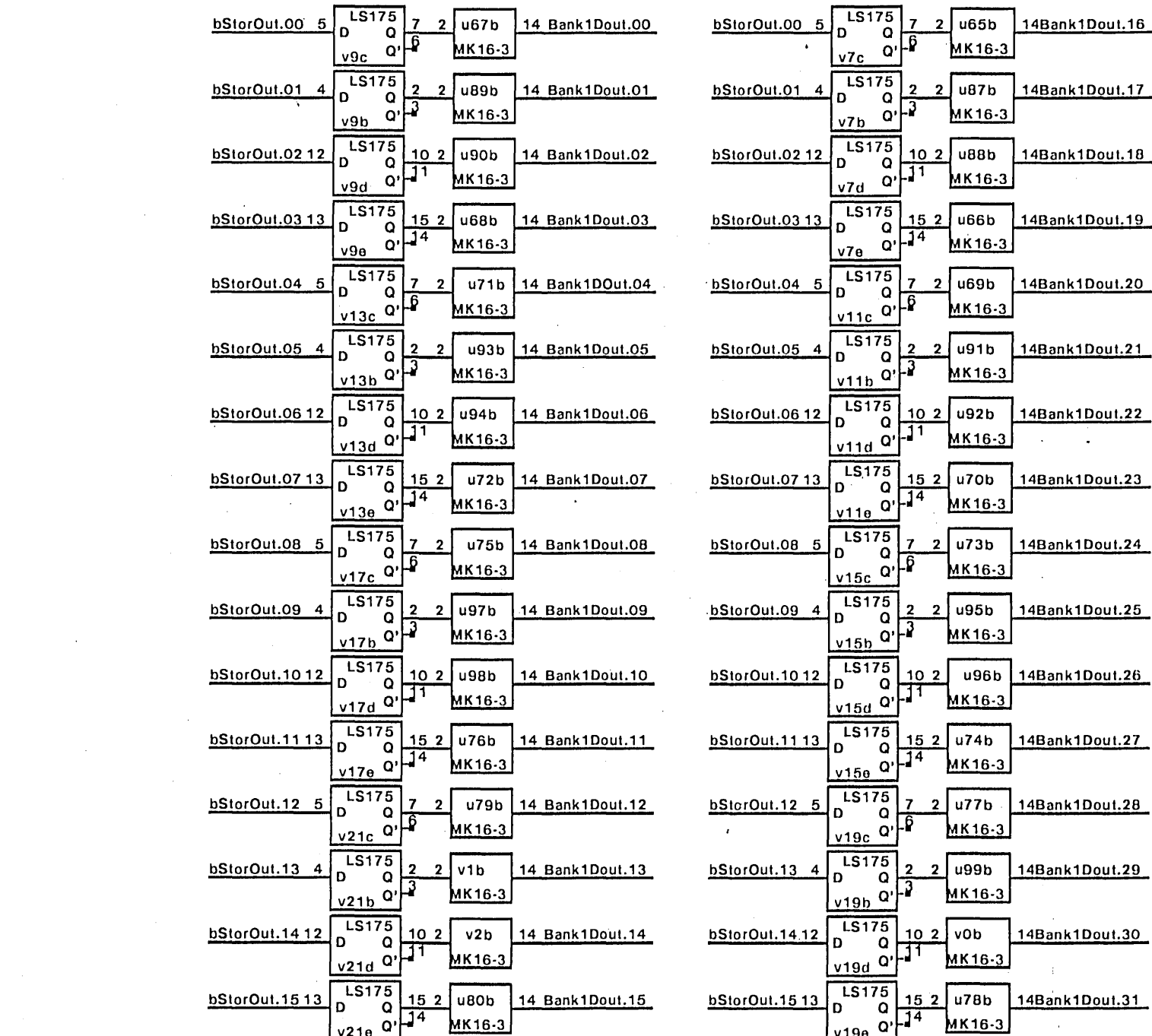


typ of 4 25S09  
see page 14 for others



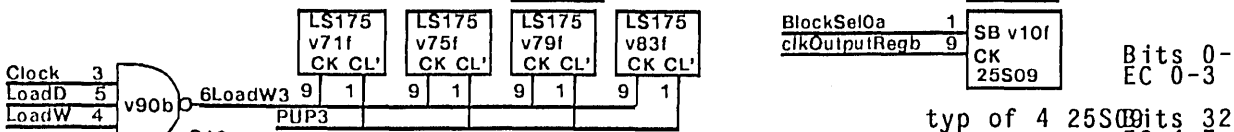
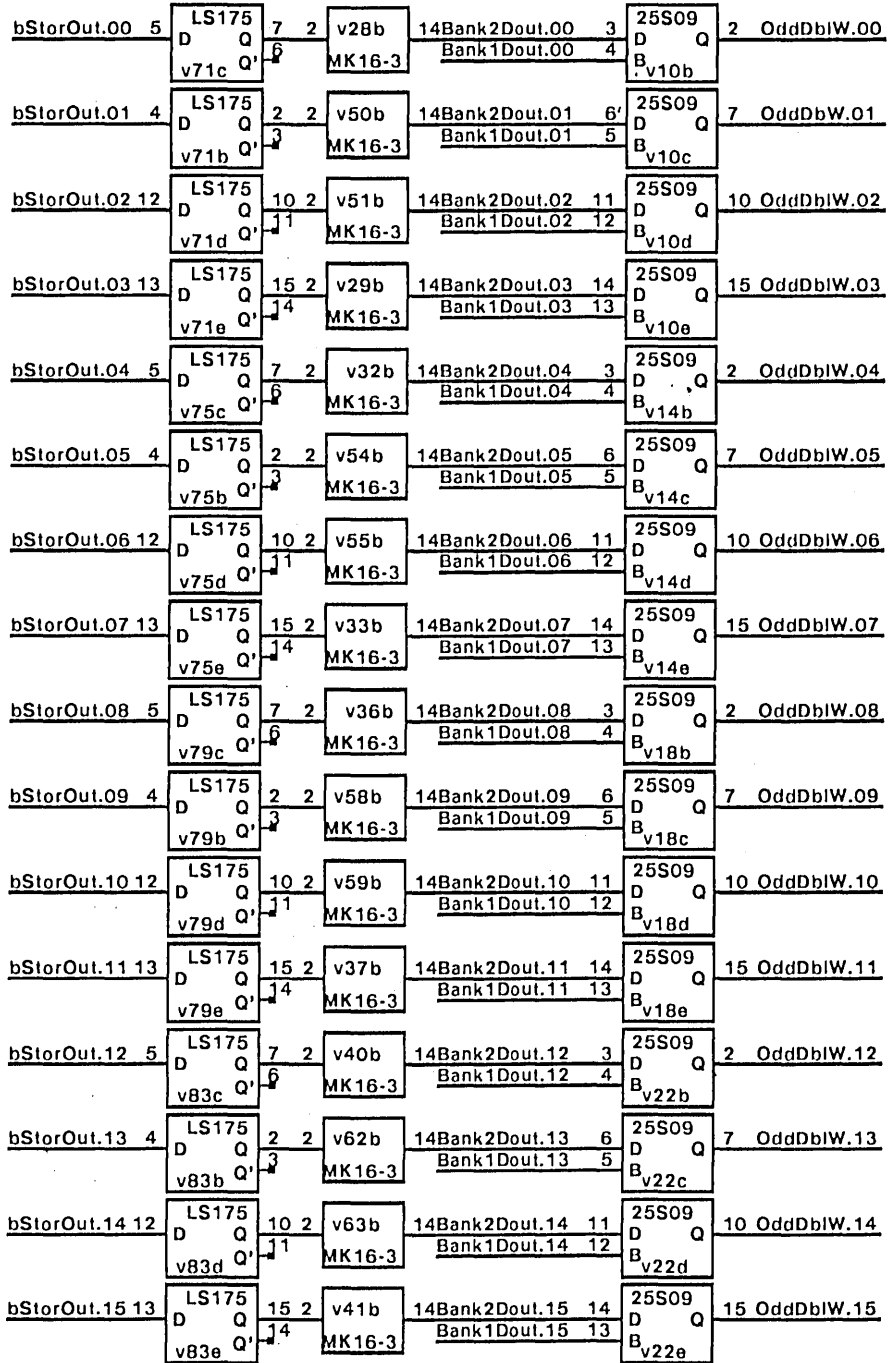
Block 0 bits 48-63  
Block 2 bits 16-31

Block 0 bits 32-47  
Block 2 bits 0-15

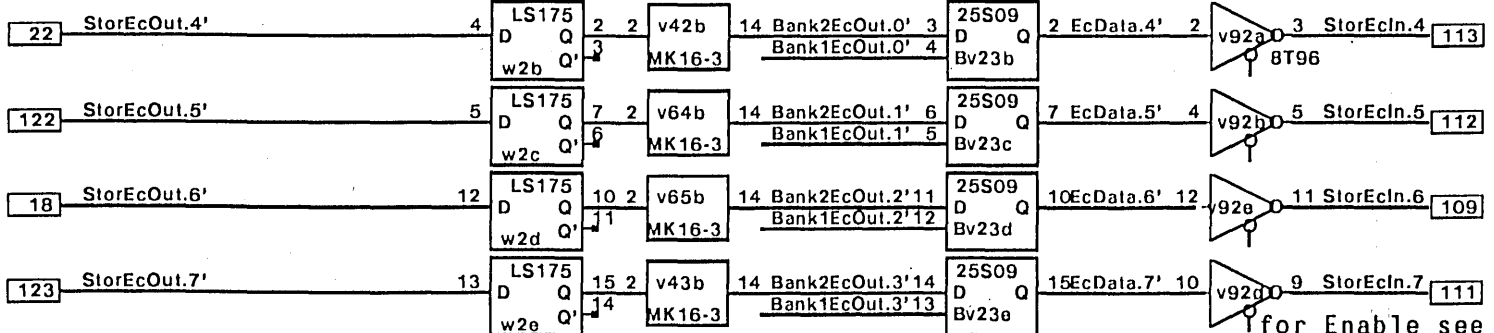
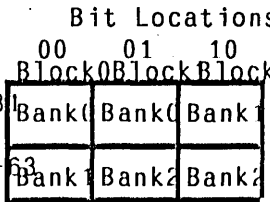


XEROX EOD	Project DO	Storage Card Bank 1	File D0stor03.sil	Designer Rosen	Rev B	Date 1/26/80	Page 03
--------------	---------------	------------------------	----------------------	-------------------	----------	-----------------	------------

Blocks 1&2 bits 48-63

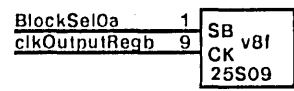
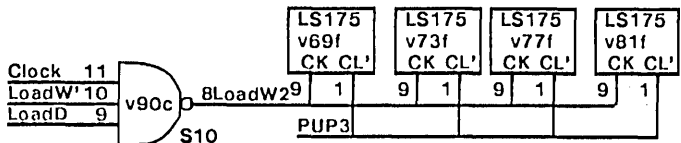
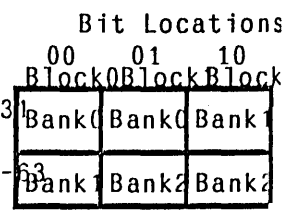
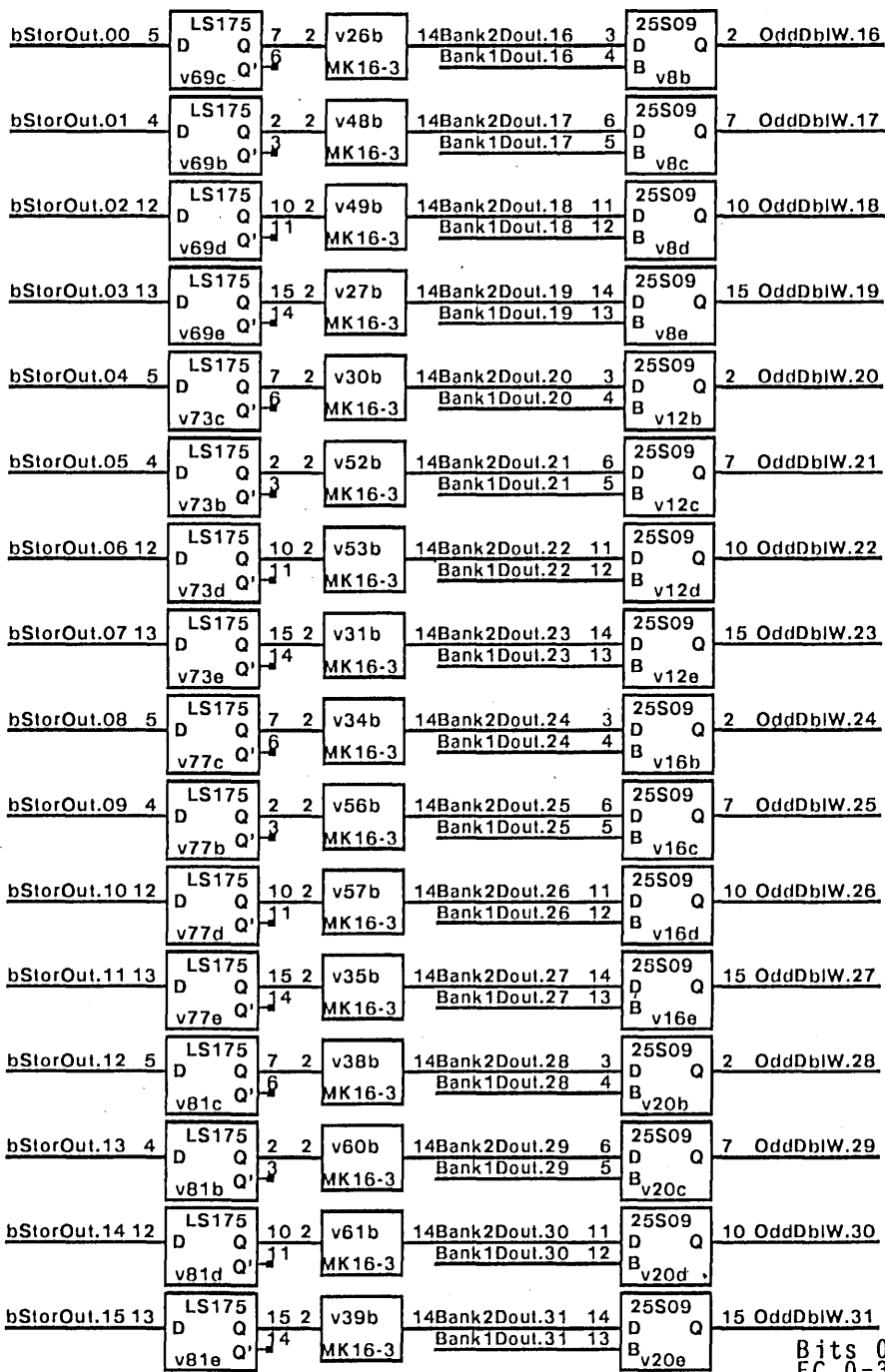


Loads on 4th word of transport  
 Clocked same time as last Data Word see page 14 for others

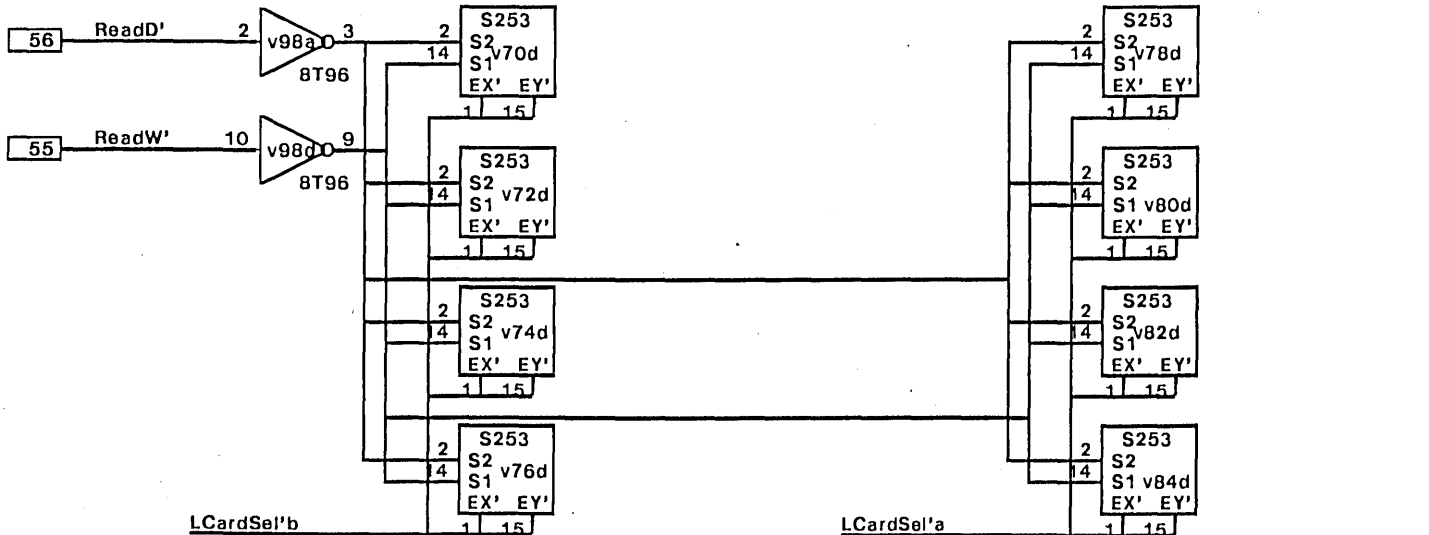
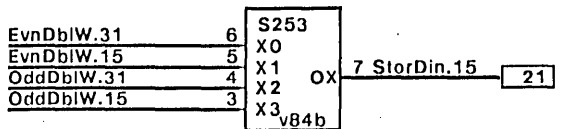
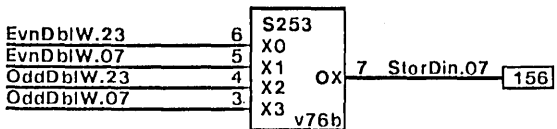
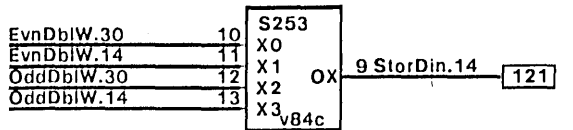
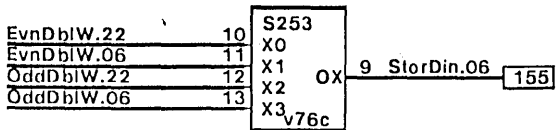
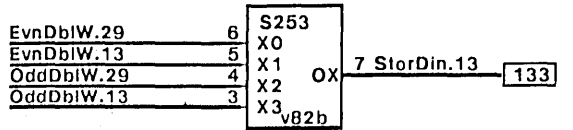
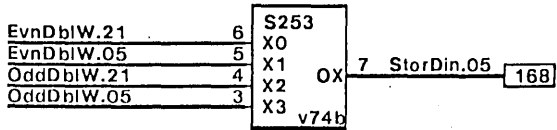
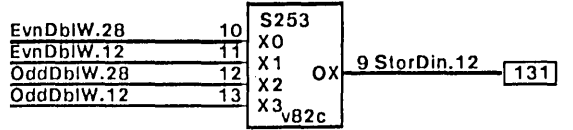
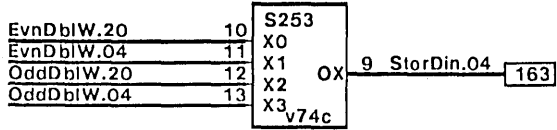
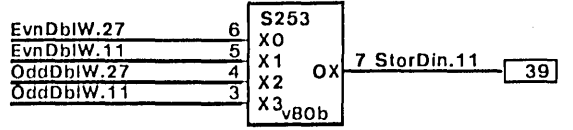
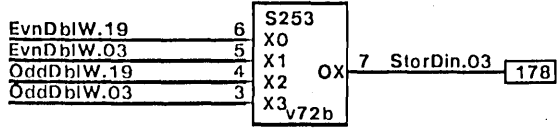
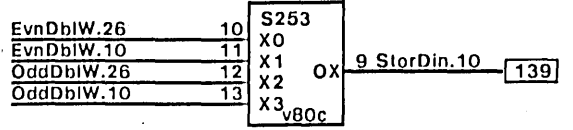
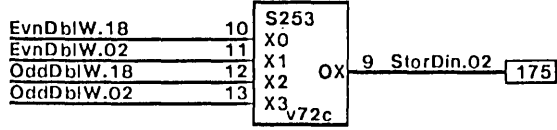
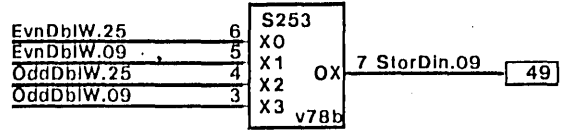
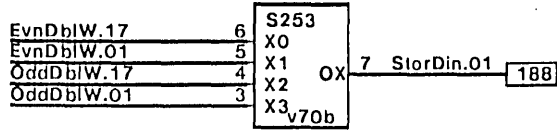
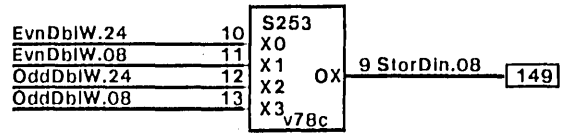
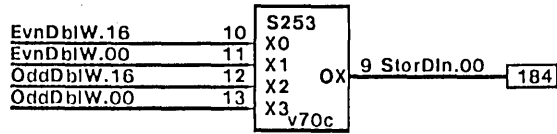


for Enable see

Blocks 1&2 bits 32-47

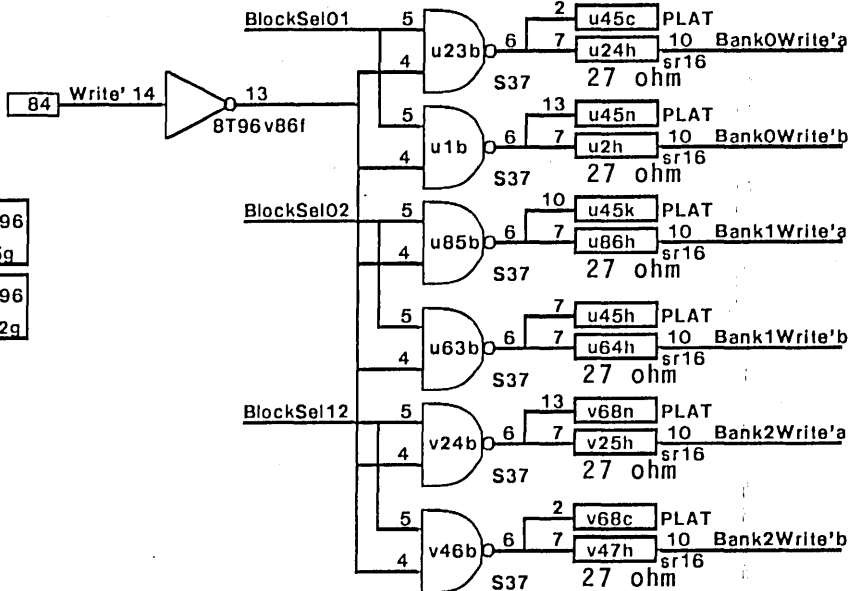
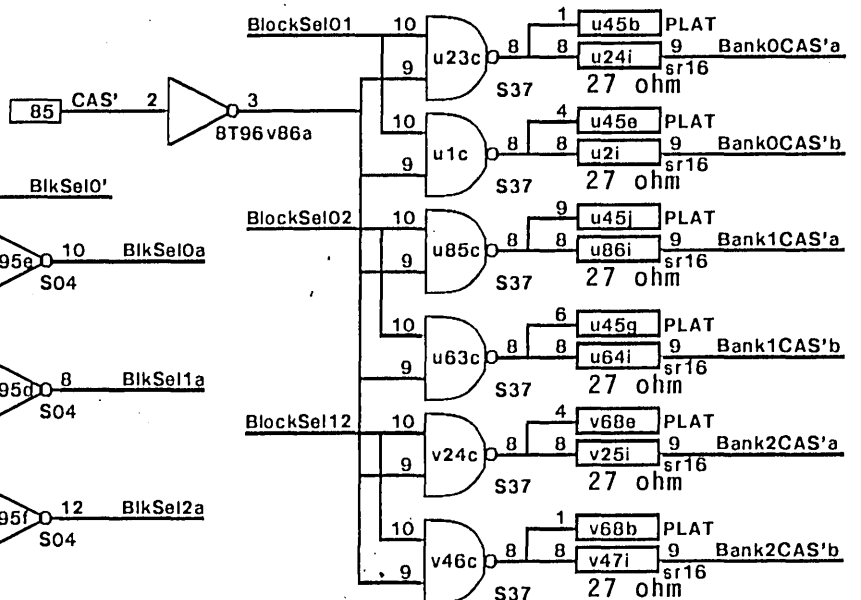
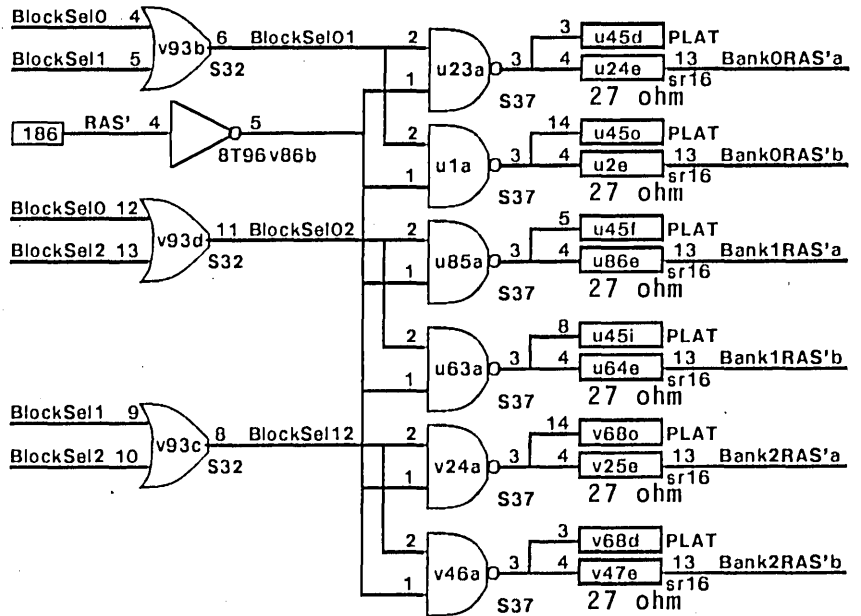
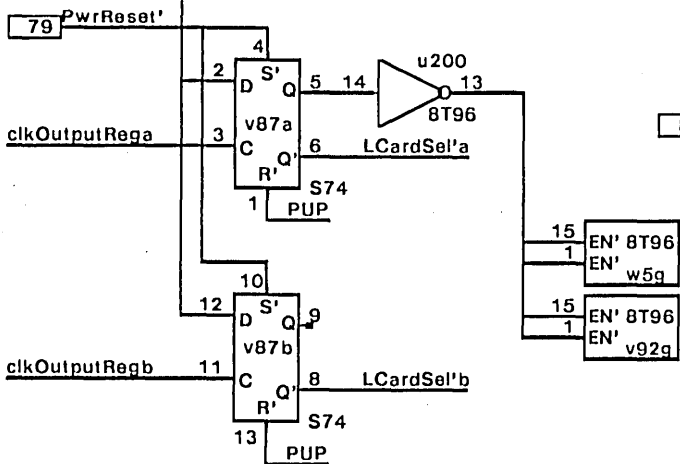
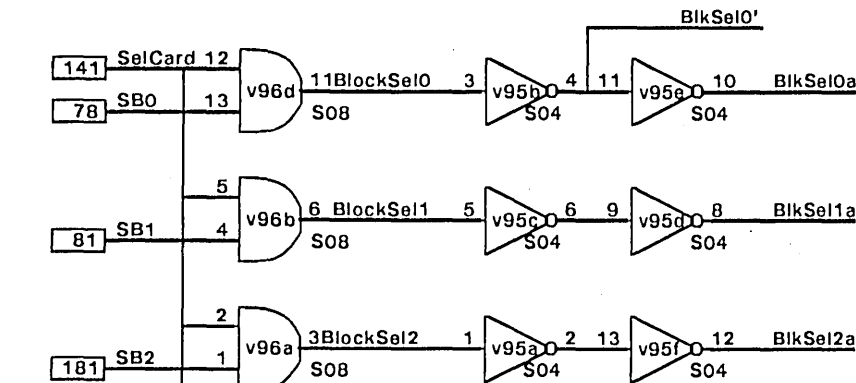
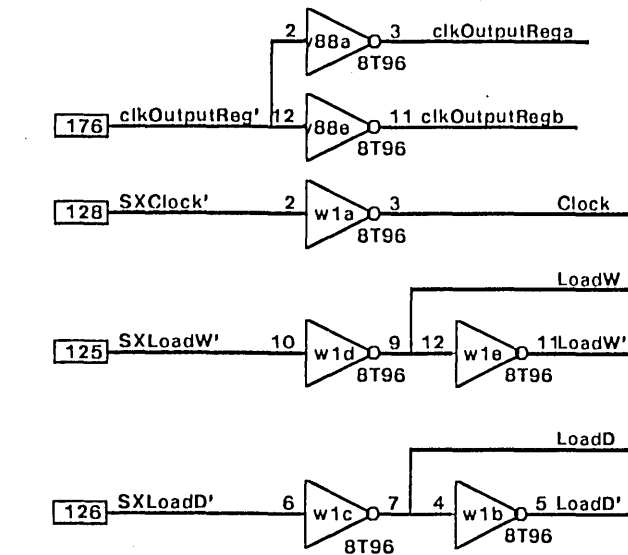


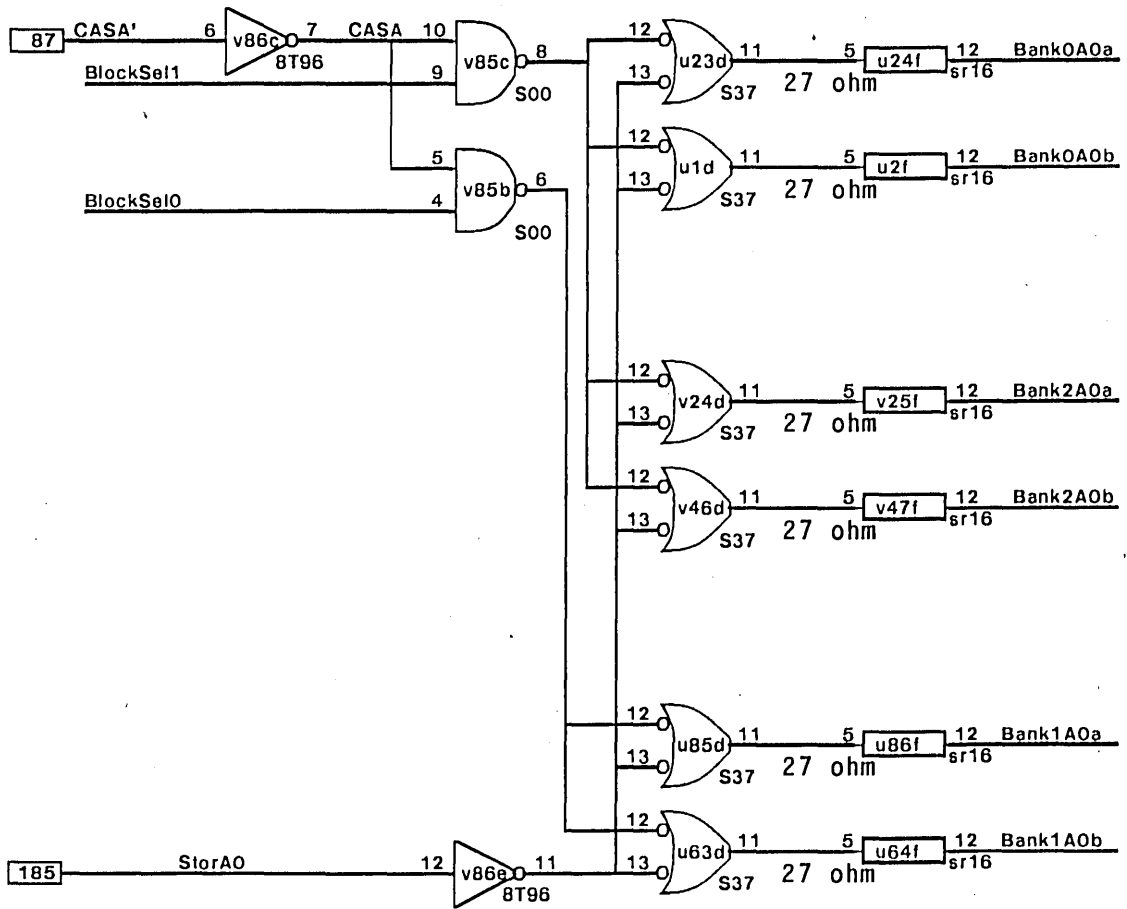
Loads on 3rd word of transport typ of 4 25S09 see page 14 for others



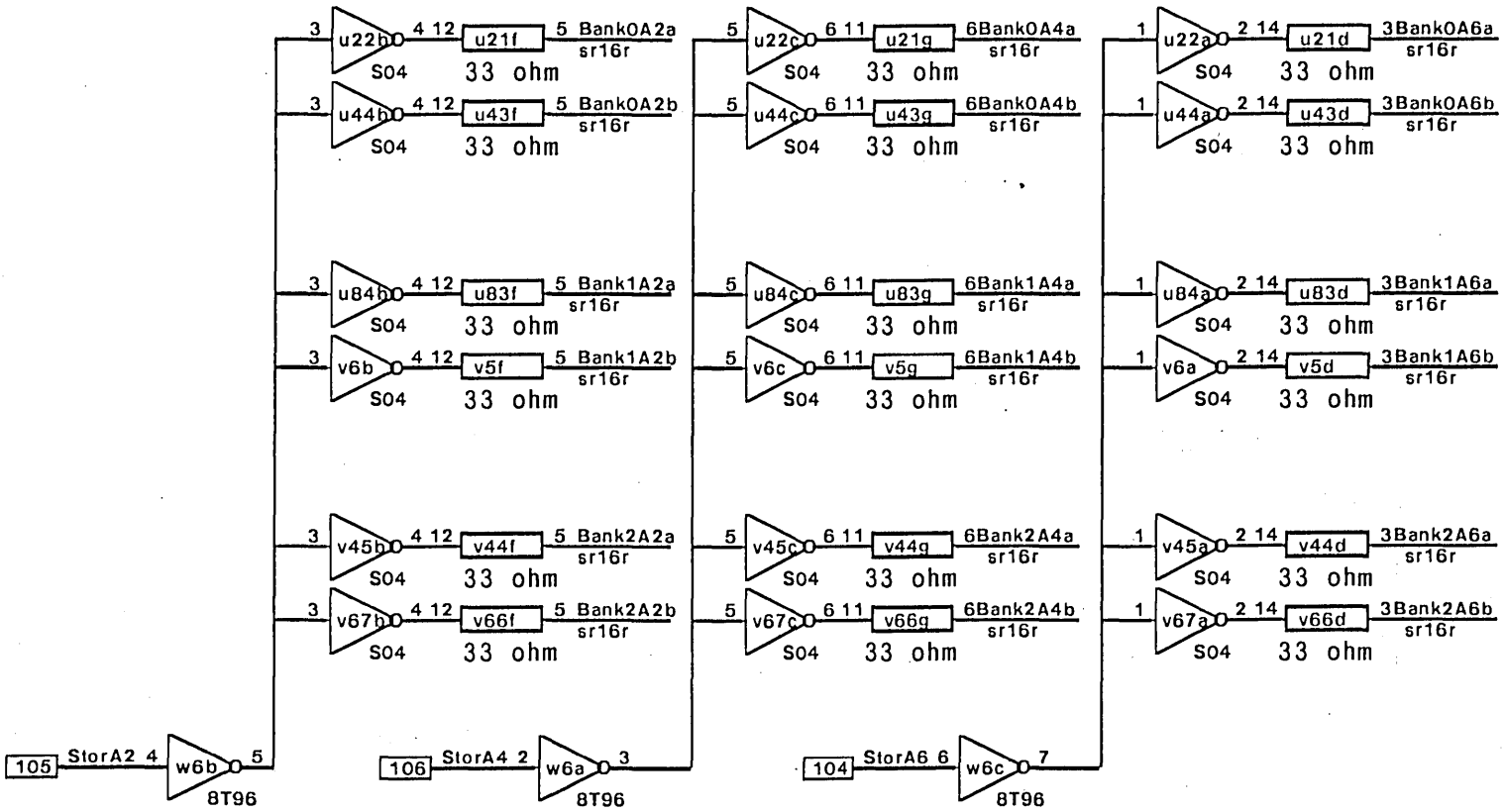
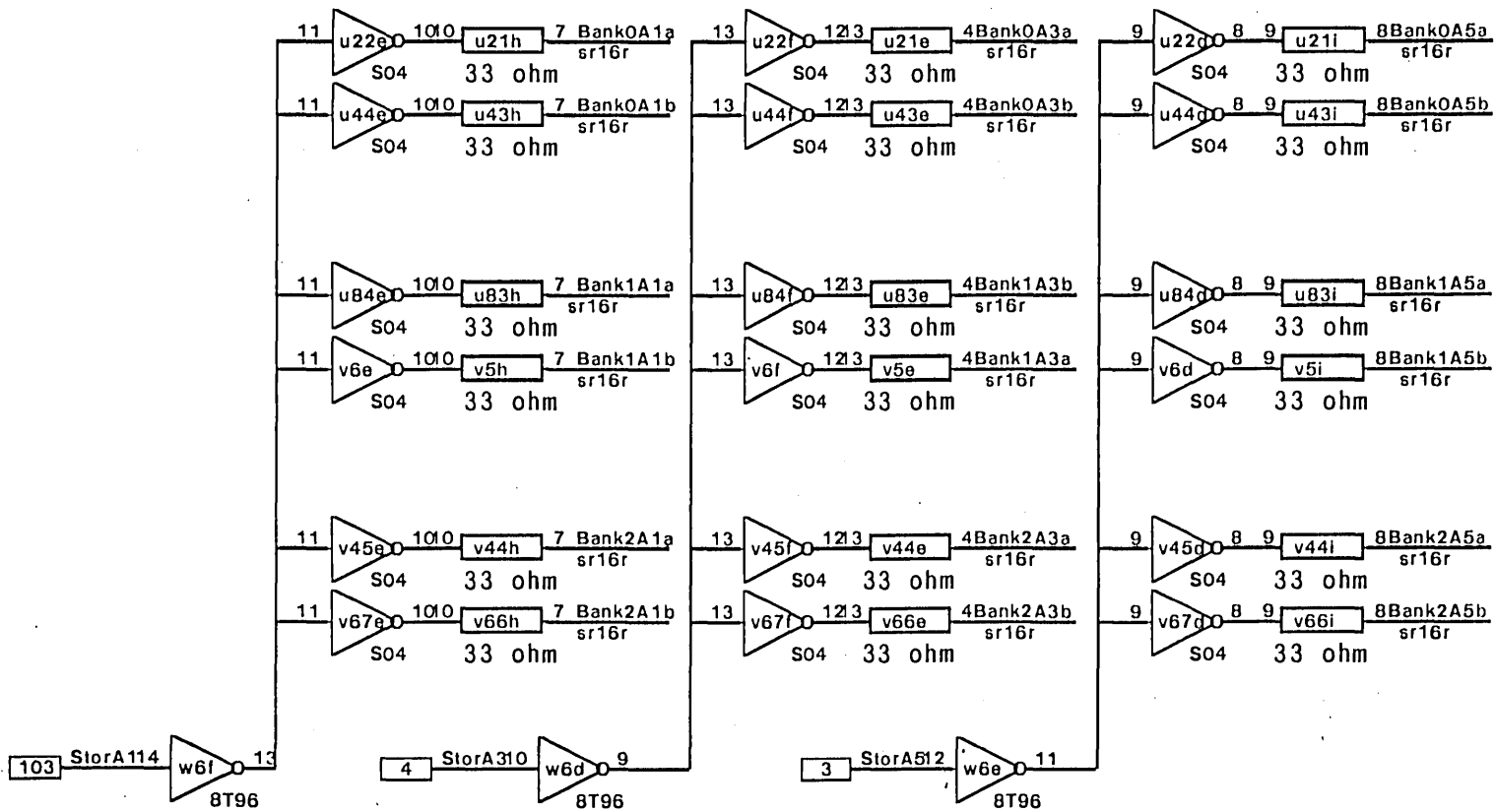
174 SB3  
Shown for completeness only  
Not used on 96k storage card

36 SRI<sub>n</sub>  
136 SRO<sub>n</sub> Jumper for I/O Boards







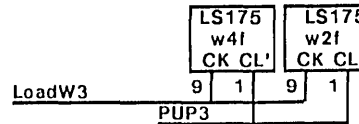
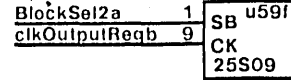
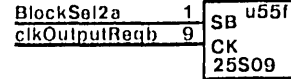
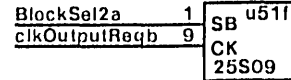
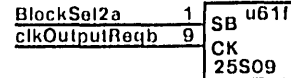
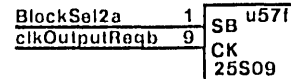
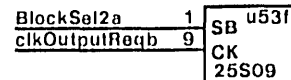
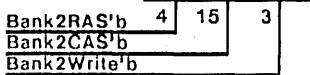
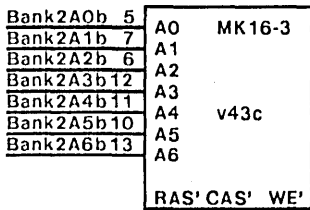
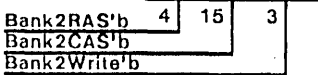
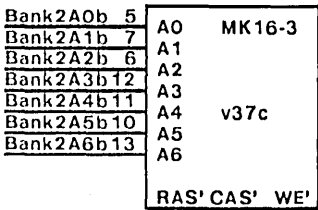
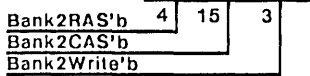
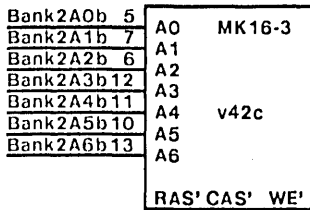
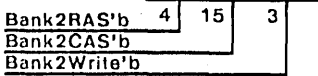
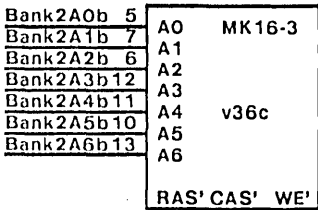
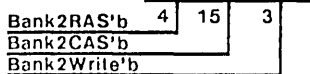
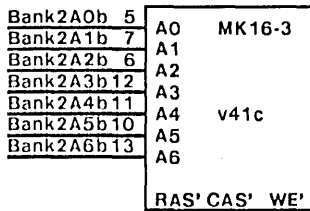
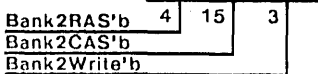
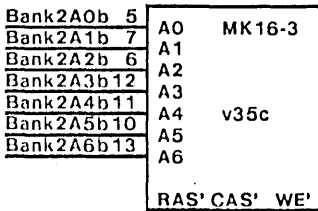
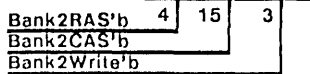
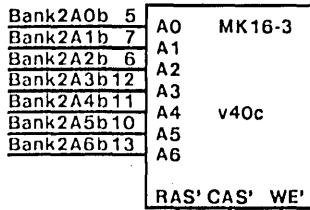
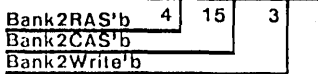
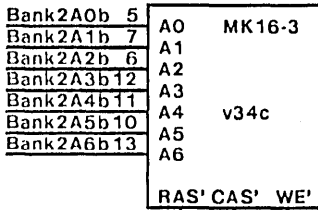
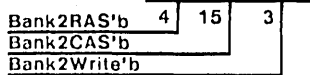
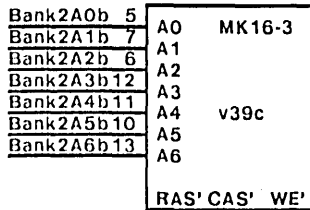
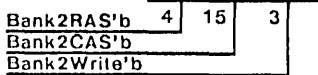
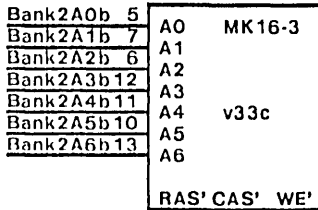
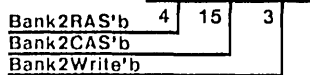
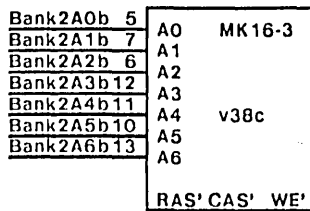
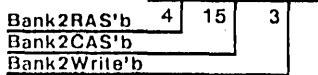
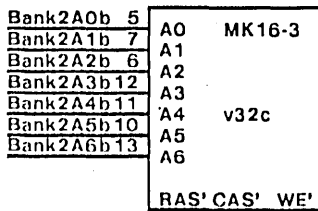












Part of EC input register, which is sha banks 0 and 2

