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MAINTENANCE MANUAL

VISUAL 102

WARNING

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to communications. It has been tested and found to comply with the limits for class A computing devices pursuant to Subpart J Part 15 of FCC rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

VISUAL TECHNOLOGY INCORPORATED, 540 MAIN STREET, TEWKSBURY, MA 01876

VISUAL V102
VIDEO DISPLAY TERMINAL
MAINTENANCE MANUAL

DECEMBER 1983

SAFETY WARNING

Hazardous voltages 115, 220 VAC and 15 KV DC are present when the terminal is on, and may remain after power is removed. Use caution when working on internal circuits, and do not work alone.

Caution is required when handling the cathode ray tube as the internal phosphor is toxic. Safety goggles and gloves must be used whenever the CRT tube is handled. If the tube should break, and skin or eyes are exposed to the phosphor, rinse the affected area with cold water and consult a physician.

This terminal is supplied with a cord set which includes a safety ground. Do not use this terminal with an ungrounded outlet, missing ground pin, or use any adaptor which will defeat the safety ground.

Insure that the power is turned off before connecting or disconnecting the keyboard cable.

This manual is published and distributed by Visual Technology Inc. Every effect has been exercised to insure its accuracy and completeness. The contents are subject to change without notice and this manual may not reflect the latest changes. Consult the sales department for latest changes.

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LIST OF ILLUSTRATIONS

1. ARCHITECTURE

The Visual 102 is a (Z80) microprocessor-based terminal composed of SSI, MSI, and LSI logic elements. The communications, keyboard/printer receiver and video refresh are interrupt driven. The video refresh uses a DMA cycle in order to minimize the processor overhead.

Program memory consists of a maximum of 32K bytes of either PROM or ROM, organized as 2-16Kx8, 1-16Kx8 1-4Kx8, or 1-16Kx8 1-8Kx8.

Alpha memory, 4K×8, is organized in two 2K×8 groups, one for data and the other for attributes. The optional graphic upgrade memory consists of four 16K×4 RAMS for a total memory of 16K×16, which provides a full bit map and is not connected to the Z80 but rather to the graphic video bus. The optional Graphic upgrade also provides 2-1Kx4 static RAMS for additional scratch pad memory.

All timing is derived from a crystal oscillator. Each frame is refreshed at 50 or 60 Hz in an overlapped manner rather than by an interlace scan. This provides all of the video information required and allows refresh to occur twice as often as with a conventional television, resulting in reduced flicker while allowing the use of faster, brighter phosphor.

Each character is created by a dot matrix as follows: in 80 character mode, each character has a 10×12 field; upper case characters are 7×9 and lower case characters 7×11. In 132 character mode, each character has a 6×12 field; upper case characters are 5×9 and lower case are 5×11. While 80 (or 132) characters are displayed on each line, the timing allows 97 (or 154) character times per line including Horizontal Sync. timing, resulting in the display being centered horizontally on the screen.

Vertically, each frame consists of 25 lines, each 12 raster lines tall. While this requires 300 raster lines, the Visual 102 generates 319 lines (60 Hz) or 383 lines (50 Hz) to center the display vertically and to provide proper synchronizing with the power line frequency. The following calculations describe the above relationships:

80 character 60 Hz mode
60 Hz (10 dots/character) (97 characters/line) (319 lines/frame) = 18.75 MHz

80 character 50 Hz mode
50 Hz (10 dots/character) (97 characters/line) (383 lines/frame) = 18.75 MHz

132 character 60 Hz mode
60 Hz (6 dots/character) (154 characters/line) (319 lines/frame) = 18.75 MHz

132 character 50 Hz mode
50 Hz (6 dots/character) (154 characters/line) (383 lines/frame) = 18.75 MHz

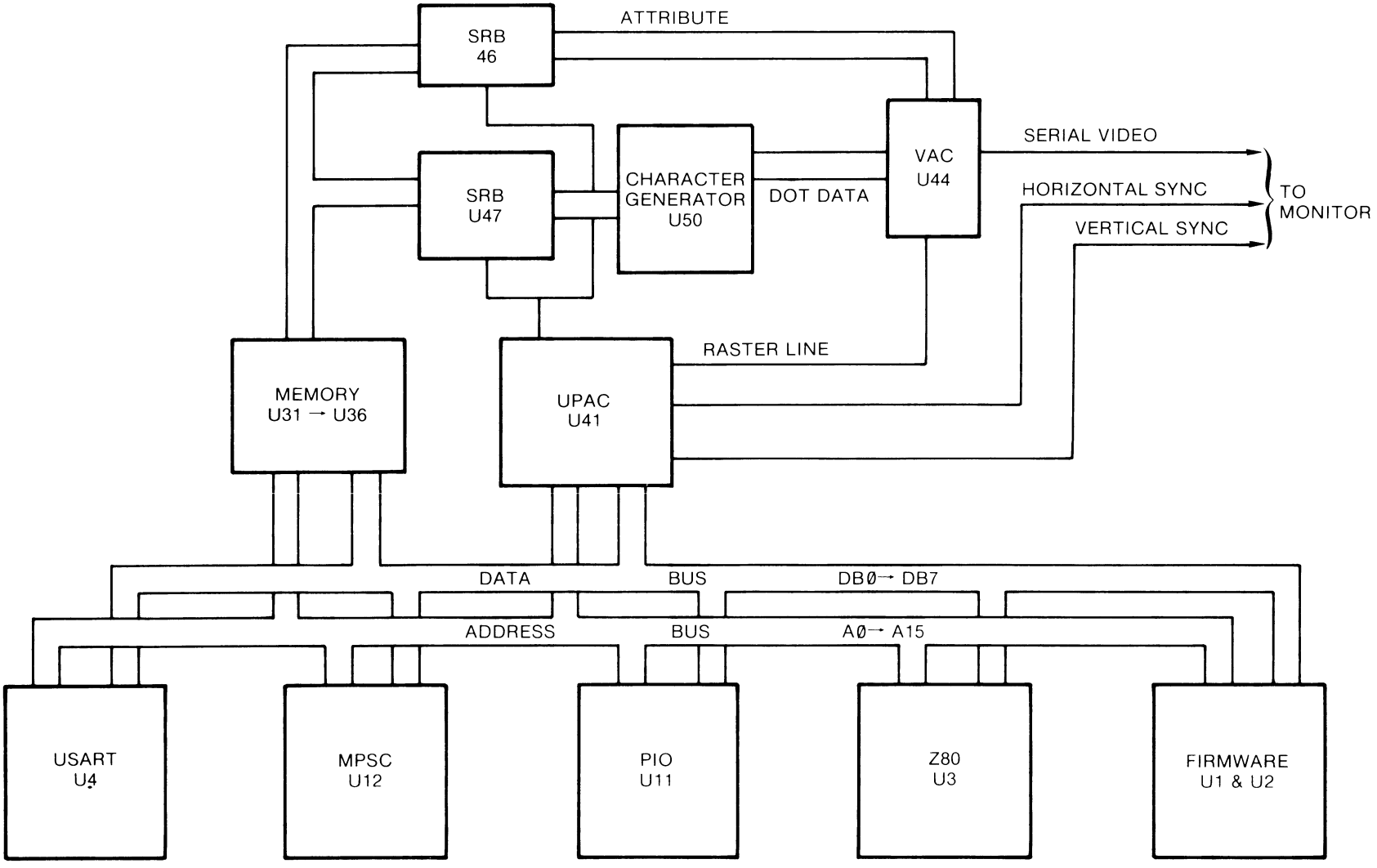


Figure 1-1. Main PCB

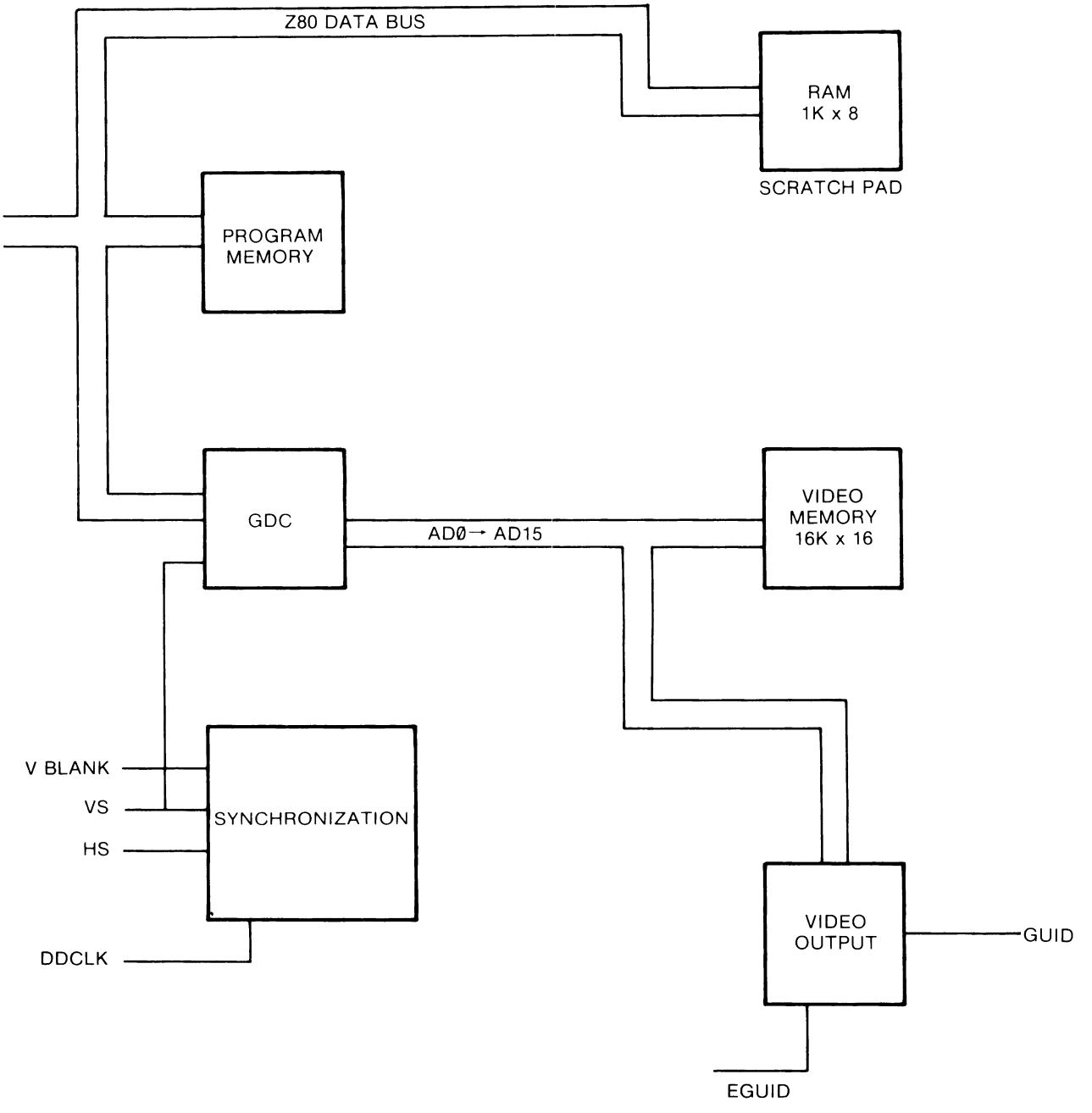


Figure 1-2. Graphic Option Board

2. THEORY OF OPERATION

The Visual 102 electronics are located on four Printed Circuit Boards; power supply, logic, T.V. and optional graphic board. The logic PCB and graphic PCB are organized in columns of IC's designated by U numbers. These IC's are numbered sequentially starting in the top left corner from top to bottom and from left to right. The schematics diagrams contained in this manual utilize this numbering system, which eliminates the need for a parts location diagram.

2.1 MASTER TIMING

Sheet 1 of the schematics shows the crystal oscillator which operates at 18.75 MHz and provides all of the timing for the unit. The Dot Clock (DCLK) operates at 18.75 MHz. U18 is used to divide the DCLK by 6 to form the PClock (PCLK) which is used by the Z80 microprocessor. U16 is used to divide the DCLK by 10 in 80 character mode or by 6 in 132 character mode to form the Character Clock (CCLK).

2.2 MICROPROCESSOR OPERATION

On sheet 1 of the schematics, the microprocessor (Z80) is shown as chip U7. The Z80 generates 16 bits of address (AB0–AB15) for all operations except during the DMA cycle. These addresses are decoded by decoders to determine memory or device addresses.

Maskable interrupts are serviced in mode 1 by generating a CALL to the program location. Interrupts are generated by the keyboard, printer, EIA, and Video Processor Controller (VPAC), which makes use of the Z80's maskable interrupt input, causing a CALL to location 0038.

2.3 PROGRAM MEMORY

The Visual 102 has been designed to allow the use of 4K×8, 8K×8 or 16K×8 EROMS. U1 will always be 16K×8. When U2 is a 2732, it is neccessary to install the PROM so that the right-most set of the pins are used (pins 1, 2, 27, 28, of the 28 pin socket are vacant when a 24 pin device is installed).

On sheet 2 of the schematics, U10 decodes the select for each of the ROMs. In addition, U10 is used to decode RAM and bank switch RAM.

Figure 2-1 illustrates the relationship between size, address and the jumper configuration. See Figure 2-4 for jumper locations.

Type U1	Type U2	U1 Address	U2 Address	Jumpers	
				W1	W2
27128	2732	0000-3FFF	4000-4FFF	1	0
27128	2764	0000-3FFF	4000-5FFF	1	0
27128	27128	0000-3FFF	4000-7FFF	0	1

1 = INSTALL 0 =OMIT

Figure 2-1. PROM Addressing

NOTE

U2 is used for the V102 options.

2.4 NON-VOLATILE RAM

The non-volatile static RAM is an X2804 which has memory of 512×8 bits. When writing data into the non-volatile RAM, a write enable low is applied to a selected device with output enable high initiating a cycle that writes data at the I/O pins into the location selected by the address pins. A byte write cycle, once initiated, will automatically continue to completion in less than 10 ms. Reading data from the non-volatile RAM is analogous to reading from a static RAM. Data is read from a selected device with a write enable high and output enable low.

2.5 I/O BUS RAM

The Visual 102 has two 2K×8 I/O RAMs. These RAMs are required to provide a receive FIFO, transmit FIFO, stack and scatchpad. U33 and U34, on sheet 3 are utilized for this purpose. U33 and U34 are located at address 8000-8FFF.

2.6 CTC CHIP

The Counter Timer Chip provides the clocks. The keyboard which is 600 baud and the independent setting of transmit and receive Baud Rate to the communications port. There are sixteen Baud Rate settings from 50 baud to 19.2K baud.

2.7 DEVICE ADDRESSING

On sheet 6 of the schematics, chip U28 decodes all device addresses for the PIO, communications USART, printer and keyboard USART, character generator, AUX 3 and the VPAC.

Address	Mnemonic	Function
ØØ-3F	SVPAC	Select VPAC
4Ø-5F	SDUART	Select the 7201 USART Keyboard and Printer
6Ø-7F	SUART	Select the 8251 USART Communications Port
8Ø-9F	SBRG	Select the 8253-5 CTC Transmit and Receive speed
AØ-BF	SPIO	Select the 8255 PIO Port A=AØ Port B=A1 Port C=A2 Control word=A3
CØ-DF	SCHGR	Select Character Generator
EØ-FF	AUX3	Select the Option Board

Figure 2-2

2.7.1 PIO

The Parallel Input/Output chip (PIO), U11, is shown on schematic sheet 6. Within the Visual 102, the PIO is programmed so that ports A and B operate in an output mode while port C is configured in the input mode. Five bits of port A (IØ-I4) provide 32 steps of video brightness. These five bits drive a ladder network shown on sheet 5 which controls the DC video level sent to the monitor PCB. One bit of port A (8Ø/132) is used to select 8Ø or 132 characters per line. One bit of port A (PREV) is used as selection for page reverse video and the last bit of port A (CHARWR) is used to select character write. Port B provides signals which are used for Block Cursor (BLOCKC), Blink Cursor (BLINKC), Page Blank (PBLANK), Enable Graphic Video (EGVID), Auxiliary Clear To Send (ACTS), Secondary Request To Send (SRTS) and Speed Select (SPDS).

Port C uses the signals from the modem. These signals are Data Carrier Detect (DCD), Secondary Carrier Detect (SDC) and ring indicator.

2.7.2 MPSC

The Multi-Protocol Serial Controller (MPSC) is a dual channel serial controller, shown on sheet 6 as U12. It is used as a serial transmitter and receiver for the keyboard, which is operating at 6ØØ baud, and for the printer. The printer rate can be set from 5Ø baud to 19ØØØ baud.

2.7.3 USART

The Visual 102 utilizes Universal Synchronous, Asynchronous Receiver Transmitter chip (USART) for the communications port, shown on sheet 6 as U4. The USART converts parallel data to serial data for transmission, and serial data to parallel for receive. The USART also provides Clear to Send (CTS), Data Terminal Ready (DTR) and Request to Send (RTS).

2.7.4 VPAC

The CRT Video Processor and Controller (VPAC), shown on sheet 6 as U41, has a fully programmable display format from 8 to 240 characters per data row, raster scan lines from 1 to 32 per data row and data rows per frame from 2 to 256. The VPAC provides the horizontal synchronization, vertical synchronization, cursor, composite synchronization, and vertical blanking. The VPAC is configured with two single row buffers, one for the data and the other for attributes. Refer to Section 2.7.5 for a description of the Single Row Buffer.

2.7.5 SRB

The Single Row Buffer (SRB) 9006 shown on sheet 4 as U46 and U47, provides an 8 bit wide variable length serial memory, which provides active video on all the scan lines. The SRB allows a variable number of characters per line to a maximum number of 132. The SRB is a RAM-based buffer which is loaded with character data from the system memory during the first scan of each data row. While this data is being written into the RAM, it is also being output through the multiplexer to the data output lines. During the subsequent scan lines in the data row, the system will then disable Write Enable and cause data to be read out from the internal RAM for the CRT screen refresh.

2.7.6 VAC

The Video Attributes Controller (VAC), on sheet 5 shown as U44 is a device containing graphics, data and attributes, cursor controller, and high speed video shift register. The VAC takes parallel video data and converts it to serial data along with the corresponding attributes. This data is then presented to the monitor.

2.7.7 Keyboard Logic

The keyboard on the Visual 102 operates in a serial fashion, over a telephone type modular cable. The V102 issues scanning commands and bell commands to the keyboard. Scanning and code generation and serialization is accomplished on the keyboard through the use of a microprocessor (8035) and a firmware PROM. When the keyboard has a character code, an interrupt is sent to the Z80.

2.8 VIDEO OPERATION

The Visual 102 writes alpha and attribute data into video memory, shown on sheet 3 as U31 through U36. During horizontal sync, the VPAC, shown on sheet 4 as U41, issues a Bus Request, the beginning of the DMA cycle, to the Z80, which in turn issues a Bus Acknowledge and a Memory Request to the Device Decoder, shown on sheet 2 as U10. The Device Decoder then selects the RAM Decoder, shown on sheet 3 as U23. That RAM Decoder then selects the appropriate memory IC for selecting the data and attribute memory. During the first scan line of each row, whether 80 to 132 characters, data and attributes are read from memory into the serial row buffers, U47 for data and U46 for attributes, shown on sheet 4 of the schematics. The character Clock strobes the data through U47 to U40, which buffers the data before it is sent to the character generator. The raster line data from U45, along with the data from U40, are loaded

into the Character Generator, shown as U50 on sheet 4. The Character Generator now combines the raster line data and the Dot Ø through Dot 7 to form dot data (DotØ-Dot7). That dot data, along with the attribute data, is loaded into and out of the Video Attribute Control (VAC), shown on sheet 5 as U44, by a load shift (LD/SH) command generated by U16 on sheet 1. The VAC converts the dot data and attributes data to serial form and sends it to the video mixer circuit, shown on sheet 5 as U48. The Video Mixer Circuit now sends the data to transistor Q4, which presents the video to the monitor.

2.9 GRAPHIC OPTION

2.9.1 Program Memory

The program memory of the graphic option board occupies memory area of the Z80 from 4ØØØH to 7FFFH. The IC can be a 27128 (U2) or two 2764 (U1) and U2. Jumper 1 will affect which size PROM is to be used.

2.9.2 Scratchpad RAM

The graphic option board has 1K×8 scratchpad RAM which stores graphics working parameters. The location of the scratchpad RAMs are U3 and U4. The memory location in the ZØØ is from CØØØH to C3FFH.

2.9.3 GDC (Graphic Display Controller)

The GDC receives commands and parameters from the Z80. The GDC passes the parameters back to the Z80. The GDC controls the read and write to the graphic video memory. Note that the graphic video memory and the alpha memory are completely independent. The Z80 cannot access the graphic video memory directly. It receives it only through the GDC.

2.9.4 Video Memory

The graphic video memory consists of 4 16K×4 chips for total of 16K×16 of video memory. These are dynamic RAMS and the RAS (Row Address Strobe) and the CAS (Column Address Strobe) through the multiplexers U17 and U19 on sheet 2 of the graphic option board. Refreshing is handled by the GDC. Input and output data are on the same pins; hence the RAMS are normally set to receive data and they output data when RAMOE is on.

2.9.5 Graphic Video Operation

The GDC modifies data in the graphic memory in three ways. First the proper address is latched in; then the GDC reads the current data at that location into the internal registers. Next, the data is modified and written into memory. Data may only be changed during blanking time.

When the ZØ issues a Write (WR) command to the GDC, the GDC generates a DBIN (Read Data to Display Memory). DBIN through flop U1Ø sheet 4 of graphic option schematics, and combined with 2XWCLK through gate U31 sheet 4, issues a GMWR (Graphic Memory Write) which enables pin 4 of the graphic memory U11 through U14, sheet 3. Then the graphic data ADØ through AD15 is written into graphic memory.

The ORAS (read out of memory) is output regardless of whether the cycle is RMW (Read Modify Write) or Display. The ORAS is combined with ARAS (Allow Row Address Strobe) and 2XWCLK shown on sheet 4 U27 to form RAS (Row Address Strobe) first, which enables the graphic memory U11 through U14. Then MUX U28 is generated to switch the address bits to Graphic Memory Address GMA0 through GMA7 through the multiplexers U17 and U19 sheet 2. Next a CAS (Column Address Strobe) by U28 if this valid memory address between 0000 through 3FFF will enable the RAMS U11 through U14. The graphic data is then loaded into the parallel-in, serial-out shift registers U18 and U20 to form video, on sheet 3, which is combined with alpha and is sent to the monitor after the brightness control is added. In the same manner, both graphics and alpha data can be displayed simultaneously.

2.10 SELF TEST

The Visual 102 executes a self test each time it is powered on. A checksum is calculated and checked against the checksum stored in the last two locations of the Firmware PROMS; a RAM test is executed and the non-volatile RAM is checked. If all are correct, the screen is initialized and a cursor is displayed. If either the firmware checksum or RAM test fails, the screen is not initialized. If non-volatile RAM fails, the screen is initialized, default parameters are selected and the bell is sounded several times. In this situation operation is allowed. However, it will be necessary to set manually any parameters which differ from default parameters.

2.11 JUMPER LOCATIONS

2.11.1 Jumpers on Main PCB

Jumpers W1 and W2 are determined by the size of the firmware. PROM and jumper configurations are defined in section 2.4. W3 and W4 are for active current loop. W5 and W6 are for the VAC and are always in. W7 thru 10 determined the size of the character generator.

2.11.2 Jumper on Main PCB

Jumper W1 is determined by the size of the firmware used on the Graphic Option Board.

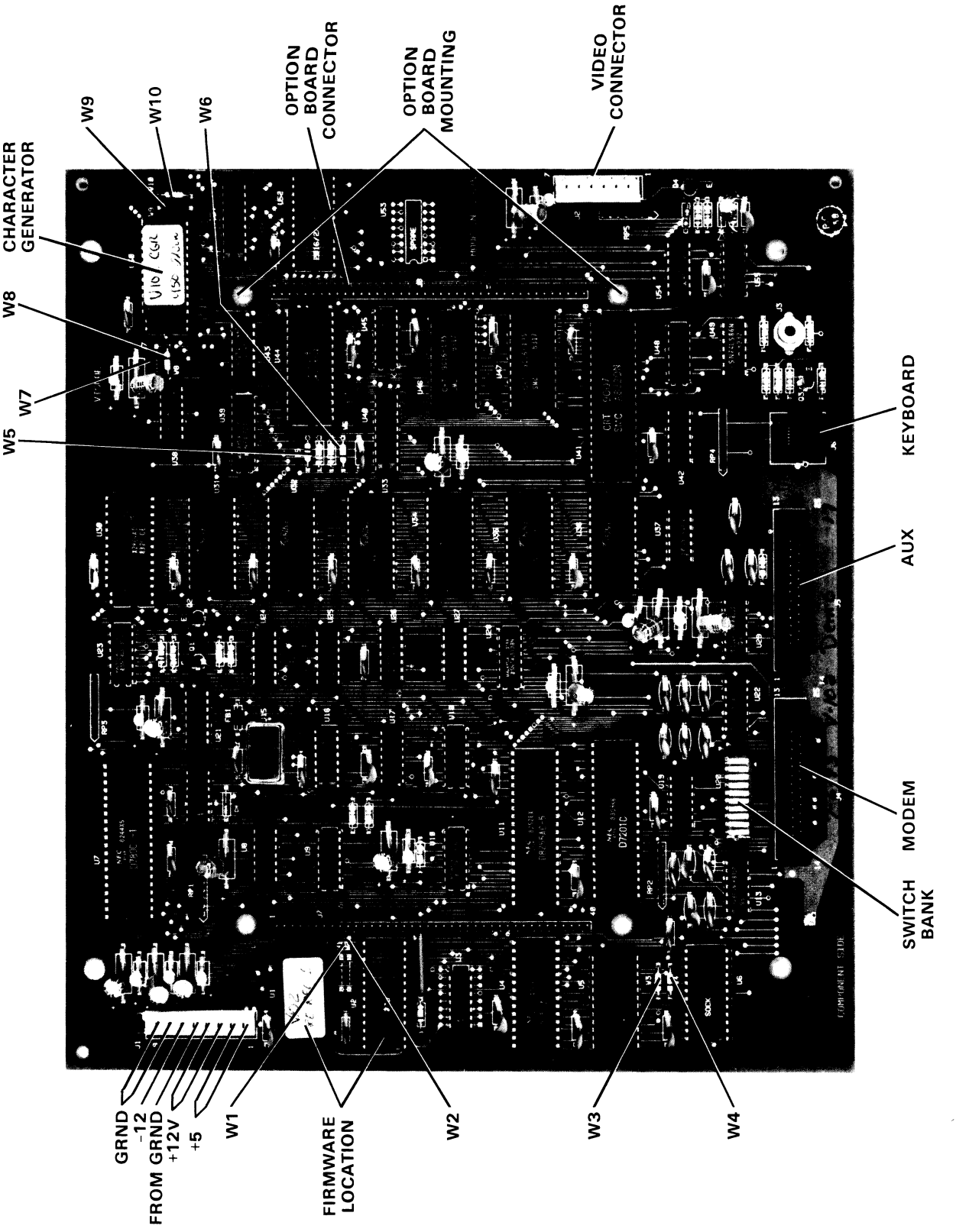


Figure 2-3. Main PCB

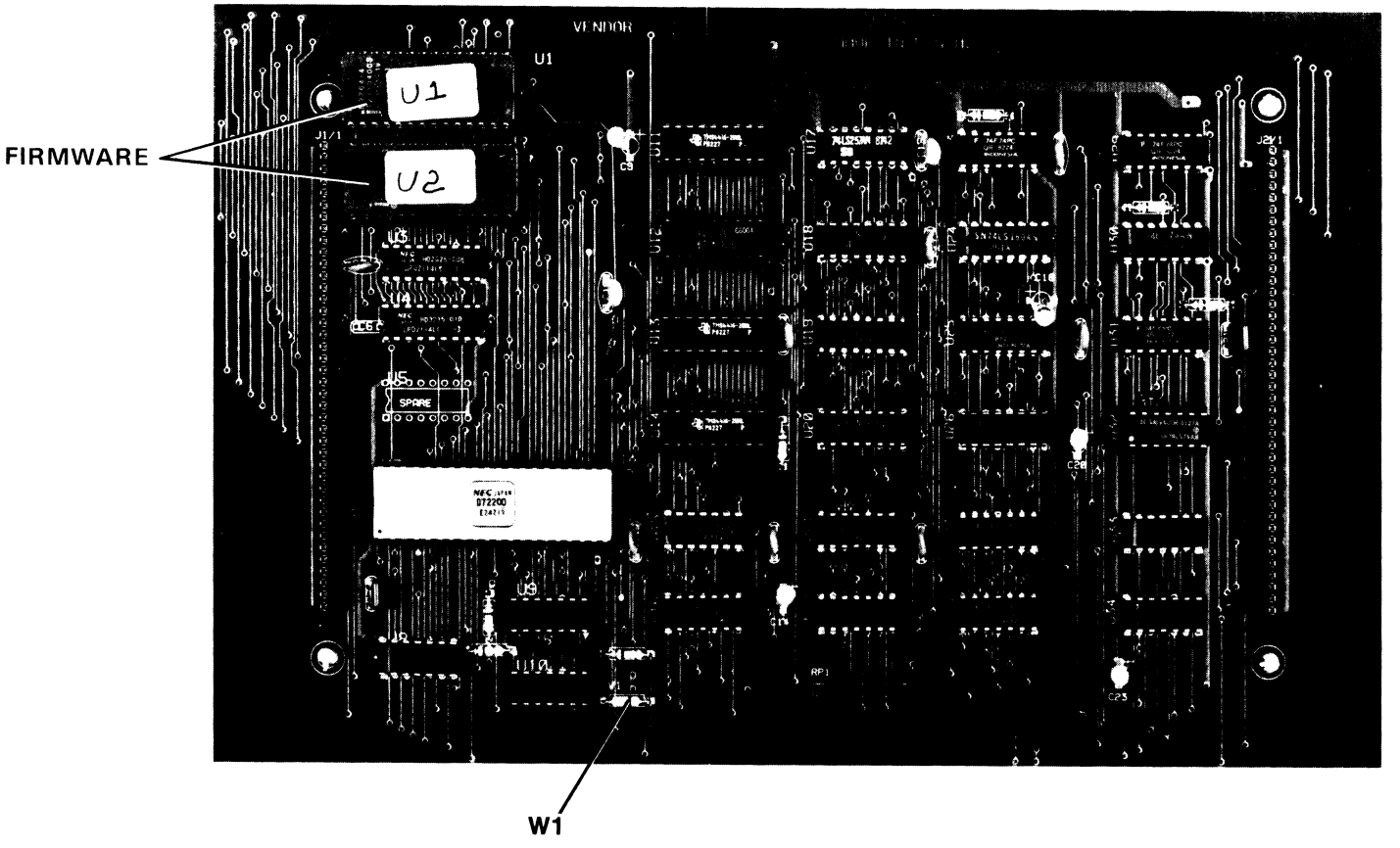


Figure 2-4. Graphic Option

3. SPARE PARTS AND TOOLS

3.1 SPARE PARTS

Each Visual 102 terminal is composed of four major subassemblies designed to be serviced on site, by replacement of the appropriate subassembly.

3.1.1 TV Monitor Subassembly

The Zenith model DJ14NK53 monitor is provided in the V102.

Description	Zenith PN	Visual PN
Monitor Kit (total)	DJ14NK53	MN113-Ø1Ø
TV PCB & Flyback	A-122Ø4	MN113-Ø12
Yoke	8321	MN113-Ø13
CRT	1Ø1-694Ø-22	MN113-Ø14

3.1.2 Keyboard Assembly

One keyboard is used on the Visual 102. It is manufactured by Keytronic Corp. and is manufactured in standard US version only. If your keyboard is configured in a foreign national version, it will be necessary to exchange keycaps at the time a spare keyboard is installed. The KTC part number for the keyboard is 65-02335 and Visual's part number is KBØ1Ø-Ø11.

3.1.3 Main PCB and Graphic Option

The main logic board contains all the active components for the alpha numeric data. The graphic option contains the logic for 4Ø1Ø emulation. The power supply provides all the voltages for the unit.

Description	Visual PN
Main PCB	PAØ24-AØ1
Graphic Option	PAØ25-AØ1
Power Supply	PAØ22-AØ1

PROMS and ROMS which are used on the main PCB are listed below with their function.

FIRMWARE

Function	Location	Visual PN
Firmware	U1	IC245-ØØ1
Character PROM	U5Ø	IC260-ØØ1
Optional Character Prom	U52	IC260-ØØ2

3.2 SPARE SUBASSEMBLY RECOMMENDATIONS

To service 100 terminals by subassembly exchange, the following subassemblies should be stocked in the quantities shown:

Quantity	Description	Part Number
5	Main PCB	PAØ24-BØ1
3	TV PCB	MN113-Ø12
3	Keyboards	KB01Ø-Ø11
3	Power Supply	PAØ22-A01

3.2.1 Active Components Recommendations

The following list contains the active components found on the main PCB and on the keyboard. Total quantities per terminal and stocking recommendations are indicated. Components used on each of the monitor models are found in Section 7. The recommendations are based on one depot repairing subassemblies for approximately 100 terminals. Components which are either custom or are sufficiently unique so that they are not found on distribution shelves are indicated with an *.

Visual P/N	Part	Qty./Unit	Recommended Spare/100
CC004-006	6 Pos PC Mnt Jack	1	5
CC010-025	25 Pos PC Mnt Plug	2	5
CP100-391	Cap 390 PF	15	10
CP140-475	Cap 47 PF	1	5
CP140-475	Cap 4.7 μf	11	10
CP220-226	Cap 22 μf 16v	13	10
CP240-103	Cap .01 μf	33	15
CR001-007	7 Pin Header	1	2
CR001-010	10 Pin Header	1	2
CR004-040	40 Pin Header	2	4
DA000-001	Diode 1N914	7	20
FB001-001	Ferrite Bead	3	2
IC000-000	74LS00	2	15
IC000-004	74LS04	2	15
IC000-008	74LS08	4	20
IC000-014	74LS14	1	10
IC000-086	74LS86	2	15
IC000-160	74LS160	1	10
IC000-138	74LS138	3	20

Visual P/N	Part	Qty./Unit	Recommended Spare/100
IC000-245	74LS245	1	10
IC000-374	74LS374	2	15
IC000-378	74LS378	1	10
IC010-016	7416	1	10
IC010-017	7417	1	10
IC050-004	74F04	1	10
IC050-160	74F160	1	10
IC050-175	74F175	1	10
IC140-021	RAM 2K x 8	4	20
IC340-001	1488	2	15
IC340-002	1489	2	15
IC342-006	*18.575 MHz Osc	1	10
IC440-002	*8255-A	1	10
IC440-005	8251-A USART	1	10
IC440-015	CTC 8253-5	1	10
IC440-017	*Z-8Ø CPU	1	10
IC440-018	*9007 VPAC	1	10
IC440-010	*7201 Dual USART	1	10
IC440-019	*9006 Single Row Buffer	2	15
IC270-003	*NVR	1	10
IC440-024	*SMC 9021 VAC	1	10
KTC 2208048-161	*8048	1	10
KTC 2207414-001	74LS74	1	10
KTC 2274373-001	74LS273	1	10
2200950-003	Keytronic	1	10
2200908-003	Keytronic	1	10

3.3 TOOLS

In order to gain access to the Visual 102 and replace any subassembly, only a cross head and a straight blade screwdriver are necessary.

In order to repair any subassembly, only an oscilloscope such as a Tektronic 465 is required. Although not required, a Z80 in-circuit emulator may lessen the time required to isolate RAM failures.

4. MNEMONIC LIST

Mnemonic	Sheet	IC	Definition
AB0-AB15	several		Address bus 0-15
ARAS	*2	U34	Allow Row Address Strobe
ACTS	6	U11	Allow Clear to Send
AUX1	2	U10	Select Option Firmware
AUX2	2	U10	Select Option RAM
AUX3	6	U28	Select Option I/O
AUX1BS	*1	U9	Aux 1 Bank Select
AVID	5	U48	Alpha Video
BLANK	4	U46	Video Blank Attribute
BLINK	4	U46	Video Blink Attribute
BLINKC	6	U11	Blink Cursor
BLOCKC	6	U11	Block Cursor
BOLD	4	U46	Video Bold Attribute
BS1SEL	*1	U8	Select BS1
BUSAK	1	U7	Bus Acknowledge
BUSRQ	4	U41	Bus Request
CAS	*4	U28	Column Address Strobe
CBLANK	4	U41	Composite Blank
CCLK	1	U16	Character Clock
CHARWR	6	U11	Character Write
CSYNC	4	U41	Composite Sync
CTS	6	U12	Clear to Send
CURSOR	4	U41	Cursor
DBIN	*1	U7	Data Bus Input
DCD	7	U13	Data Carrier Detect
DCLK	1	U17	Dot Clock
D0-D7	several		Data Bus
DSR	7	U13	Data Set Ready
DTR	6	U4	Data Terminal Ready
DWR	1	U26	Delayed Write
EGVID	6	U11	Enable Graphic Video
GBLANK	*1	U7	Graphic Blank
GDCSEL	*1	U32	GDC select

NOTE: * Denotes the graphic option board schematics.

Mnemonic	Sheet	IC	Definition
GMA0-GMA3	*2	U19	Graphic Memory Address
GMA4-GMA7	*2	U17	Graphic Memory Address
GMWR	*4	U31	Graphic Memory Write
GSRLD	*4	U16	Graphic Shift Register Load
GCLD	*2	U22	Graphic Counter Load
GVID	*3	U25	Graphic Video
HALFVS	3	U27	Half Vertical Sync
HSYNC	4	U41	Horizontal Sync
IØ-14	6	U11	Intensity Data Bits
INT	several		Interrupt
IOREQ	1	U7	I/O Request
KBRD	6	U12	Keyboard Receive Data
KBTXD	6	U12	Keyboard Transmit Data
LD/SH	1	U16	Load/Shift
MREQ	1	U7	Memory Request
MUX	*4	U28	Multiplex Address Select
M1	1	U7	Machine Interrupt
ORAS	*1	U7	Output Row Address Strobe
PBUSY	7	U29	Printer Busy
PHASE	*2	U31	Phase
PRXD	6	U12	Printer Receive Data
PRC	6	U12	Printer Clock
PTXD	7	U13	Printer Transmit Data
PREV	6	U11	Page Reverse
PCLK	1	U17	Processor Clock
RAM	2	U10	Ram Enable
RAMOE	*4	U22	Graphic Ram Output Enable
RAS	*4	U27	Row Address Strobe
RD	1	U7	Read
RESET	1	U14	Reset
RFSH	1	U1	Refresh
RI	7	U29	Ring Indicator
RTS	6	U4	Request to Send
RVID	4	U46	Reverse Video
RXD	7	U13	Receive Data

NOTE: * Denotes the graphic option board schematics.

Mnemonic	Sheet	IC	Definition
RXC	1	U5	Receive Clock
SCHRG	6	U28	Select Character Generator
SBRG	6	U28	Select Baud Rate Generator
SDUART	6	U28	Select Printer USART
SUART	6	U28	Select MPSC
SLD	4	U41	Scan Line Data
SLG	4	U41	Scan Line Gate
SPIO	6	U28	Select PIO
SNVIN	3	U3	Select Non Volatile In
SNVOUT	3	U3	Select Non Volatile Out
SRTS	6	U11	Secondary Request to Send
SPDS	6	U11	Speed Select
SCD	6	U11	Secondary Carrier Detect
SVPAC	6	U28	Select VPAC
SETRAS	*4	U23	Set Row Address Strobe
TXD	6	U4	Transmit Data
TXC	1	U5	Transmit Clock
UNDRL	4	U46	Underline Attribute
VBLANK	4	U41	Vertical Blanking
VIDEO	5	Q4	Video Output to Monitor
VLT	4	U41	Visible Line Time
VS	4	U41	Vertical Sync
WR	1	U7	Write
WCLK	*2	U21	Word Clock

NOTE: * Denotes the graphic option board schematics.

5. I.C. DATA SHEETS

Included in this section are the specifications for the following I.C.'s.

Z80 (UPD 780)	Z80 CPU
UPD 8253-5	CTC
UPD 8251	USART
UPD 8255A	PIO
7201	Dual USART
4416	Memory
7220	GDC
9006	Single Row Buffer
9007	VPAC
9021	VAC
IC260-001	Character Generator

8-BIT N-CHANNEL MICROPROCESSOR COMPLETELY Z80™ COMPATIBLE

DESCRIPTION

The μPD780 and μPD780-1 processors are single chip microprocessors developed from third generation technology. Their increased computational power produces higher system through-put and more efficient memory utilization, surpassing that of any second generation microprocessor. The single voltage requirement of the μPD780 and μPD780-1 processors makes it easy to implement them into a system. All output signals are fully decoded and timed to either standard memory or peripheral circuits. An N-channel, ion implanted, silicon gate MOS process is utilized in implementing the circuit.

The block diagram shows the functions of the processor and details the internal register structure. The structure contains 26 bytes of Read/Write (R/W) memory available to the programmer. Included in the registers are two sets of six general purpose registers, which may be used as 8-bit registers individually, or as 16-bit register pairs. Also included are two sets of accumulator and flag registers.

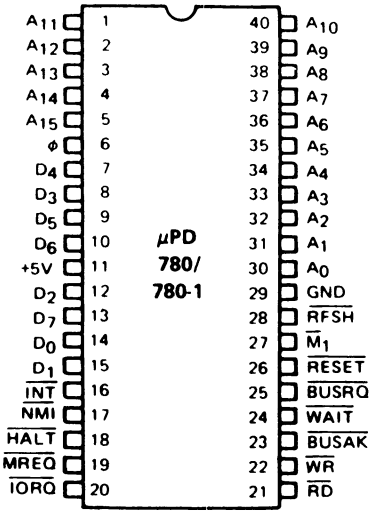
Through a group of exchange instructions the programmer has access to either set of main or alternate registers. The alternate register permits foreground/background mode of operation, or may be used for fast interrupt response. A 16-bit stack pointer is also included in each processor, simplifying implementation of multiple level interrupts, permitting unlimited subroutine nesting, and simplifying many types of data handling.

The two 16-bit index registers simplify implementation of relocatable code and manipulation of tabular data. The Refresh register will automatically refresh external dynamic memories. A powerful interrupt response mode will use the I register to form the upper 8-bits of a pointer to an interrupt service address table, while the interrupting apparatus supplies the lower 8-bits of the pointer. An indirect call will then be made to service this address.

FEATURES

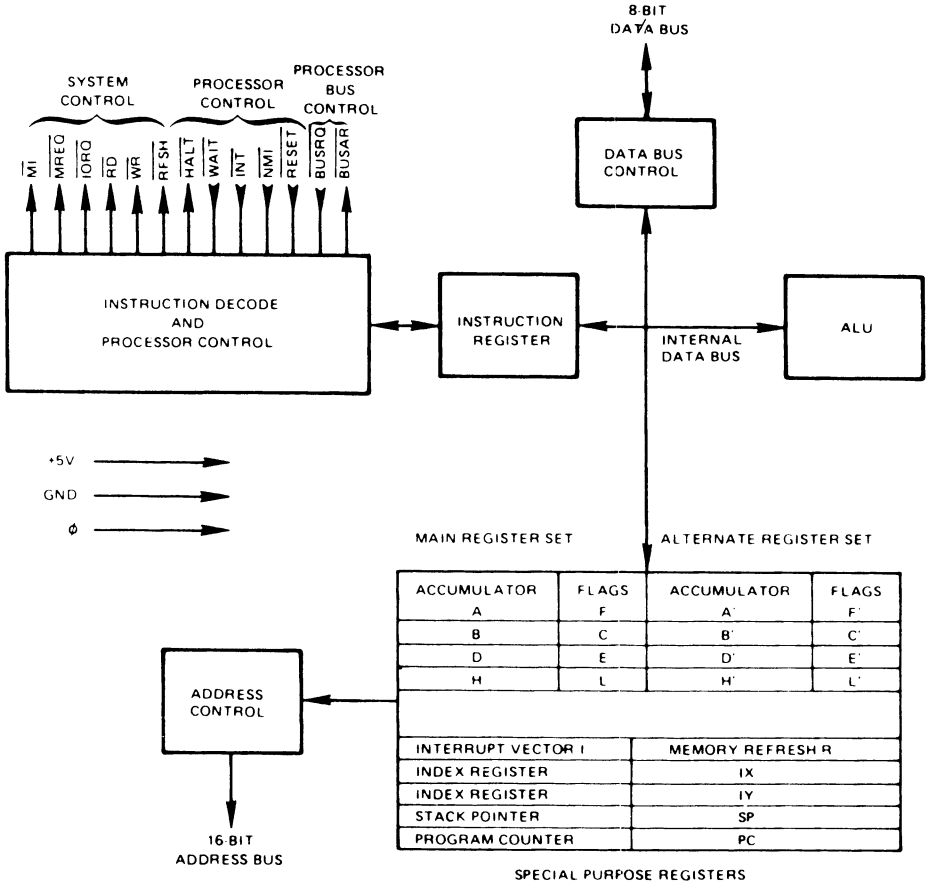
- Single Chip, N-Channel Silicon Gate Processor
- 158 Instructions – Including all 78 of the 8080A Instructions, Permitting Total Software Compatibility
- New 4-, 8-, and 16-Bit Operations Featuring Useful Addressing Modes such as Indexed, Bit and Relative
- 17 Internal Registers
- Three Modes of Rapid Interrupt Response, and One Non-Maskable Interrupt
- Directly Connects Standard Speed Dynamic or Static Memories, with Minimum Support Circuitry
- Single-Phase +5 Volt Clock and 5 VDC Supply
- TTL Compatibility
- Automatic Dynamic RAM Refresh Circuitry
- Available in Plastic Package

PIN CONFIGURATION



TM: Z80 is a registered trademark of Zilog, Inc.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1-5, 30-40	A_0-A_{15}	Address Bus	3-State Output, active high. Pins A_0-A_{15} constitute a 16-bit address bus, which provides the address for memory and I/O device data exchanges. Memory capacity 65,536 bytes. A_0-A_7 is also needed as refresh cycle.
7-10, 12-15	D_0-D_7	Data Bus	3-State input/output, active high. Pins D_0-D_7 compose an 8-bit, bidirectional data bus, used for data exchanges with memory and I/O devices.
27	$\overline{M_1}$	Machine Cycle One	Output, active low. $\overline{M_1}$ indicates that the machine cycle in operation is the op code fetch cycle of an instruction execution.
19	$\overline{MREQ}$	Memory Request	3-State output, active low. $\overline{MREQ}$ indicates that a valid address for a memory read or write operation is held in the address.
20	$\overline{IORQ}$	Input/Output Request	3-State output, active low. The I/O request signal indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. The $\overline{IORQ}$ signal is also used to acknowledge an interrupt command, indicating that an interrupt response vector can be placed on the data bus.
21	$\overline{RD}$	Memory Read	3-State output, active low. $\overline{RD}$ indicates that the processor is requesting data from memory or an I/O device. The memory or I/O device being addressed should use this signal to gate data onto the data bus.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
22	$\overline{WR}$	Memory Write	3-State output, active low. The memory write signal indicates that the processor data bus is holding valid data to be stored in the addressed, memory or I/O device.
28	$\overline{RFSH}$	Refresh	Output, active low. $\overline{RFSH}$ indicates that a refresh address for dynamic memories is being held in the lower 7-bits of the address bus. The $\overline{MREQ}$ signal should be used to implement a refresh read to all dynamic memories.
18	$\overline{HALT}$	Halt State	Output, active low. $\overline{HALT}$ indicates that the processor has executed a HALT software instruction, and will not resume operation until either a non-maskable or a maskable (with mask enabled) interrupt has been implemented. The processor will execute NOP's while halted, to maintain memory refresh activity.
24	$\overline{WAIT}$	Wait	Input, active low. $\overline{WAIT}$ indicates to the processor that the memory or I/O devices being addressed are not ready for a data transfer. As long as this signal is active, the processor will reenter wait states.
16	$\overline{INT}$	Interrupt Request	Input, active low. The $\overline{INT}$ signal is produced by I/O devices. The request will be honored upon completion of the current instruction, if the interrupt enable flip-flop (IFF) is enabled by the internal software. There are three modes of interrupt response. Mode 0 is identical to 8080 interrupt response mode. The Mode 1 response is a restart location at 0038_H. Mode 2 is for simple vectoring to an interrupt service routine anywhere in memory.
17	$\overline{NMI}$	Non-Maskable Interrupt	Input, active low. The non-maskable interrupt has a higher priority than $\overline{INT}$. It is always acknowledged at the end of the current instruction, regardless of the status of the interrupt enable flip-flop. When the $\overline{NMI}$ signal is given, the μPD780 processor automatically restarts to location 0066_H.
26	$\overline{RESET}$	Reset	Input, active low. The $\overline{RESET}$ signal causes the processor to reset the interrupt enable flip-flop (IFF), clear PC and I and R registers, and set interrupt to 8080A mode. During the reset time, the address bus and data bus go to a state of high impedance, and all control output signals become inactive, after which processing continues at 0000H.
25	$\overline{BUSRQ}$	Bus Request	Input, active low. $\overline{BUSRQ}$ has a higher priority than $\overline{NMI}$, and is always honored at the end of the current machine cycle. It is used to allow other devices to take control over the processor address bus, data bus signals; by requesting that they go to a state of high impedance.
23	$\overline{BUSAK}$	Bus Acknowledge	Output, active low. $\overline{BUSAK}$ is used to inform the requesting device that the processor address bus, data bus and 3-state control bus signals have entered a state of high impedance, and the external device can now take control of these signals.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin	-0.3 to +7 Volts ①
Power Dissipation	1.5W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

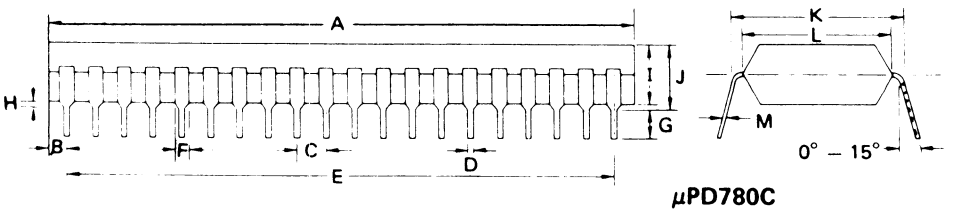
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage		V_{ILC}	-0.3		0.45	V	
Clock Input High Voltage		V_{IHC}	V_{CC}-0.2		V_{CC}	V	
Input Low Voltage		V_{IL}	-0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}	V	
Output Low Voltage		V_{OL}			0.4	V	I_{OL} = 1.8 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = -250 μA
Power Supply Current	μPD780	I_{CC}			150	mA	t_c = 400 ns
	μPD780-1	I_{CC}		90	200	mA	t_c = 250 ns
Input Leakage Current		I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOH}			10	μA	V_{OUT} = 2.4 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOL}			-10	μA	V_{OUT} = 0.4 V
Data Bus Leakage Current in Input Mode		I_{LD}			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ			35	pF	f_c = 1 MHz
Input Capacitance	C_{IN}			5	pF	Unmeasured Pins
Output Capacitance	C_{OUT}			10	pF	Returned to Ground

PACKAGE OUTLINES
μPD780C/D



μPD780C
μPD780C-1
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

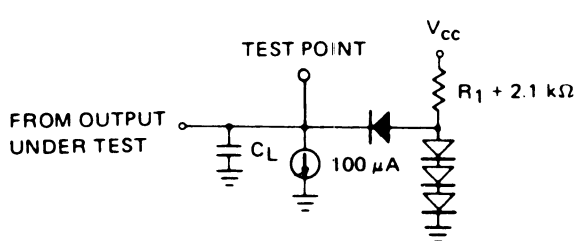
AC CHARACTERISTICS

T_a 0 C to +70 C, V_{CC} +5V ± 5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS μPD780 MIN	LIMITS μPD780 MAX	LIMITS μPD780-1 MIN	LIMITS μPD780-1 MAX	UNIT	TEST CONDITIONS
Clock Period	t_c	0.4	⑫	0.25	⑫	μs	
Clock Pulse Width, Clock High	$t_{w(\Phi H)}$	180		110		ns	
Clock Pulse Width, Clock Low	$t_{w(\Phi L)}$	180	2000	110	2000	ns	
Clock Rise and Fall Time	t_r, t_f		30		30	ns	
Address Output Delay	$t_{D(AD)}$		145		110	ns	
Delay to Float	$t_{F(AD)}$		110		90	ns	
Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	t_{acm}	①		①		ns	C_L = 50 pF
Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	t_{aci}	②		②		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$	t_{ca}	③		③		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$ During Float	t_{caf}	④		④		ns	
Data Output Delay	$t_{D(D)}$		230		150	ns	
Delay to Float During Write Cycle	$t_{F(D)}$		90		90	ns	
Data Setup Time to Rising Edge of Clock During M1 Cycle	$t_{su(D)}$	50		35		ns	
Data Setup Time to Falling Edge of Clock During M2 to M5 Cycles	$t_{su(D)}$	60		50		ns	C_L = 200 pF
Data Stable Prior to $\overline{WR}$ (Memory Cycle)	t_{dcm}	⑤		⑤		ns	
Data Stable Prior to $\overline{WR}$ (I/O Cycle)	t_{dci}	⑥		⑥		ns	
Data Stable from $\overline{WR}$	t_{cdf}	⑦		⑦		ns	
Any Hold Time for Setup Time	t_H	0			0	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ Low	$t_{DL\overline{\Phi}(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Rising Edge of Clock to $\overline{MREQ}$ High	$t_{DH\Phi(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ High	$t_{DH\overline{\Phi}(MR)}$		100		85	ns	
Pulse Width, $\overline{MREQ}$ Low	$t_{w(MRL)}$	⑧		⑧		ns	
Pulse Width, $\overline{MREQ}$ High	$t_{w(MRH)}$	⑨		⑨		ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\Phi(IR)}$		90		75	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\overline{\Phi}(IR)}$		110		85	ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ High	$t_{DH\Phi(IR)}$		100		85	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ High	$t_{DH\overline{\Phi}(IR)}$		110		85	ns	C_L = 50 pF
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ Low	$t_{DL\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ Low	$t_{DL\overline{\Phi}(RD)}$		130		95	ns	
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ High	$t_{DH\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ High	$t_{DH\overline{\Phi}(RD)}$		110		85	ns	
$\overline{WR}$ Delay from Rising Edge of Clock to $\overline{WR}$ Low	$t_{DL\Phi(WR)}$		80		65	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ Low	$t_{DL\overline{\Phi}(WR)}$		90		80	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ High	$t_{DH\Phi(WR)}$		100		80	ns	
Pulse Width to $\overline{WR}$ Low	$t_{w(WRL)}$	⑩		⑩		ns	
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ Low	$t_{DL(M1)}$		130		100	ns	C_L = 30 pF
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ High	$t_{DH(M1)}$		130		100	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ Low	$t_{DL(RF)}$		180		130	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ High	$t_{DH(RF)}$		150		120	ns	
$\overline{WAIT}$ Setup Time to Falling Edge of Clock	$t_{s(WT)}$	70		70		ns	
$\overline{HALT}$ Delay Time from Falling Edge of Clock	$t_{D(HT)}$		300		300	ns	C_L = 50 pF
$\overline{INT}$ Setup Time to Rising Edge of Clock	$t_{s(IT)}$	80		80		ns	
Pulse Width, $\overline{NMI}$ Low	$t_{w(NML)}$	80		80		ns	
$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	$t_{s(BQ)}$	80		50		ns	
$\overline{BUSAK}$ Delay from Rising Edge of Clock to $\overline{BUSAK}$ Low	$t_{DL(BA)}$		120		100	ns	C_L = 50 pF
$\overline{BUSAK}$ Delay from Falling Edge of Clock to $\overline{BUSAK}$ High	$t_{DH(BA)}$		110		100	ns	
$\overline{RESET}$ Setup Time to Rising Edge of Clock	$t_{s(RS)}$	90		60		ns	
Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	$t_{F(C)}$		100		80	ns	
$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	t_{mr}	⑪		⑪		ns	

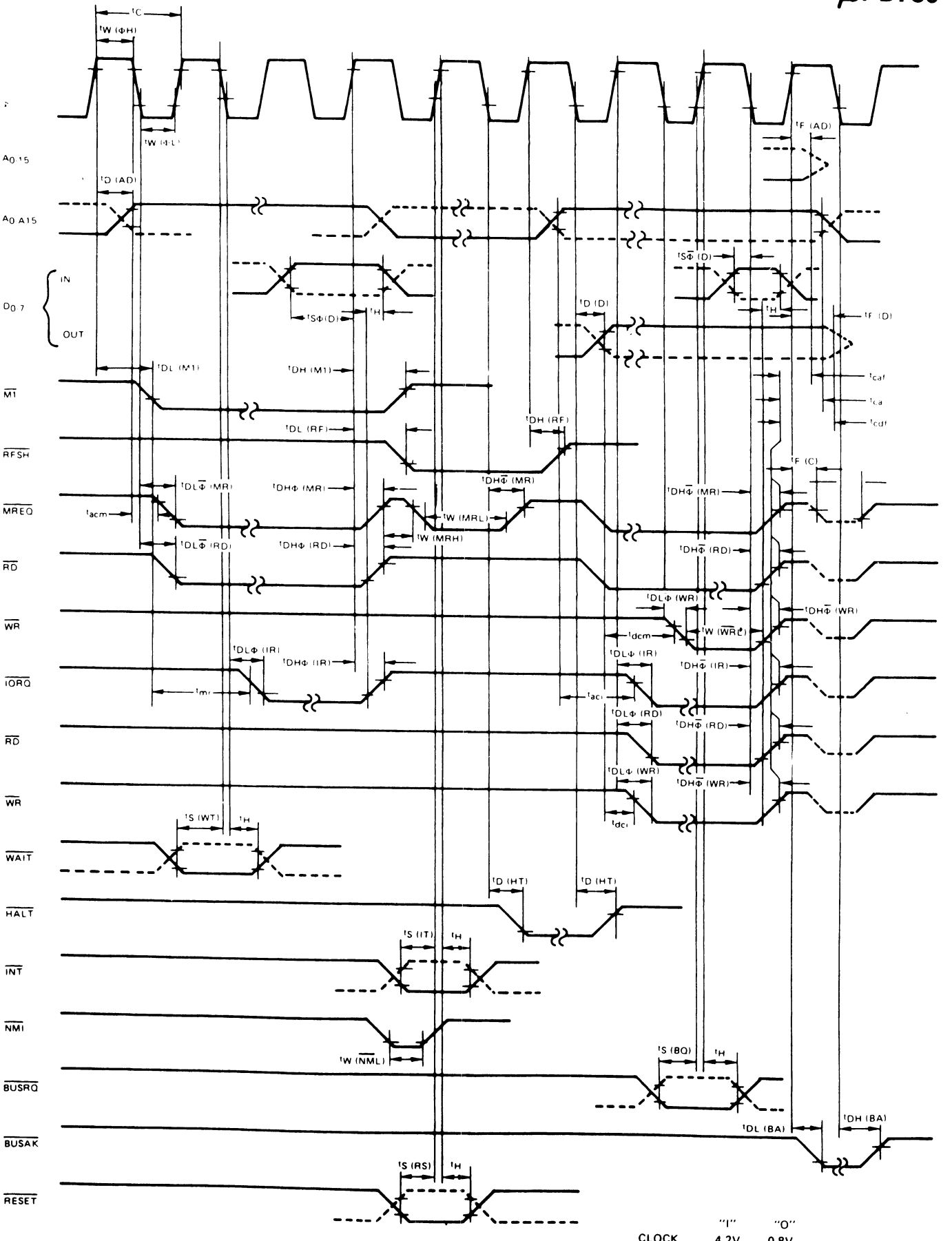
Notes
① $t_{acm} = t_{w(\Phi H)} + t_f - 65$ (75)*
② $t_{aci} = t_c - 70$ (80)*
③ $t_{ca} = t_{w(\Phi L)} + t_r - 50$ (40)*
④ $t_{caf} = t_{w(\Phi L)} + t_r - 45$ (60)*
⑤ $t_{dcm} = t_c - 170$ (210)*
⑥ $t_{dci} = t_{w(\Phi L)} + t_r - 170$ (210)*
⑦ $t_{cdf} = t_{w(\Phi L)} + t_r - 70$ (80)*
⑧ $t_{w(MRL)} = t_c - 30$ (40)*
⑨ $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 20$ (30)*
⑩ $t_{w(WR)} = t_c - 30$ (40)*
⑪ $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$ (80)*
⑫ $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

*These values apply to the μPD780.



LOAD CIRCUIT FOR OUTPUT

TIMING WAVEFORM ①

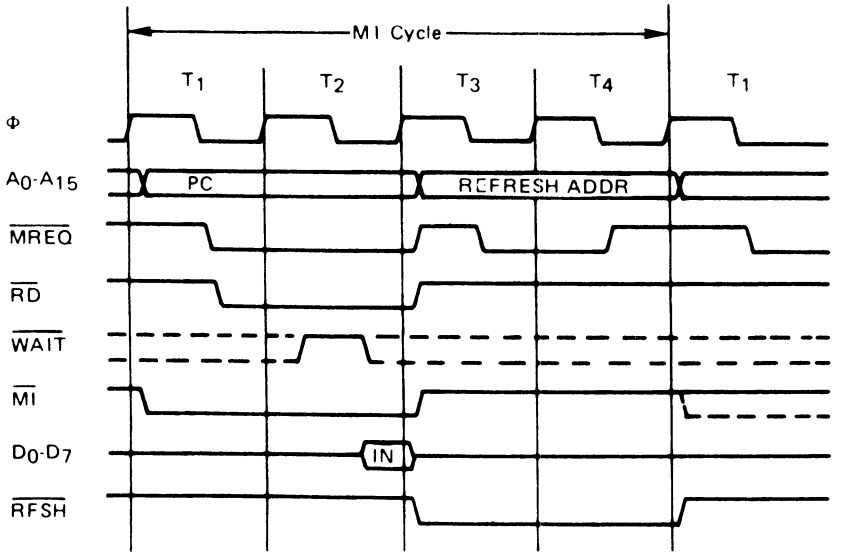


Note: ① Timing measurements are made at the following voltages unless otherwise specified:

	"I"	"O"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	±0.5V

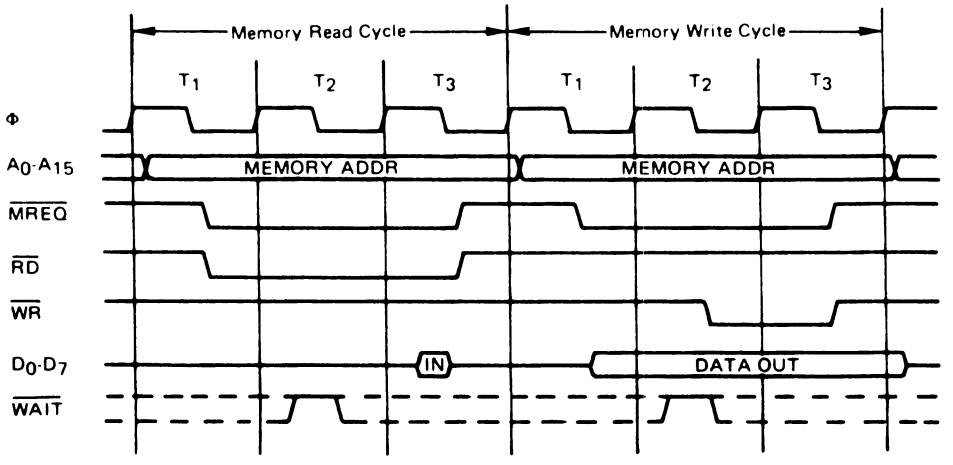
Instruction Op Code Fetch

The contents of the program counter (PC) are placed on the address bus at the start of the cycle. $\overline{MREQ}$ goes active one-half clock cycle later, and the falling edge of this signal can be used directly as a chip enable to dynamic memories. The memory data should be enabled onto the processor data bus when $\overline{RD}$ goes active. The processor takes data with the rising edge of the clock state T_3. The processor internally decodes and executes the instruction, while clock states T_3 and T_4 of the fetch cycle are used to refresh dynamic memories. The refresh control signal $\overline{RFSH}$ indicates that a refresh read should be done to all dynamic memories.



Memory Read or Write Cycles

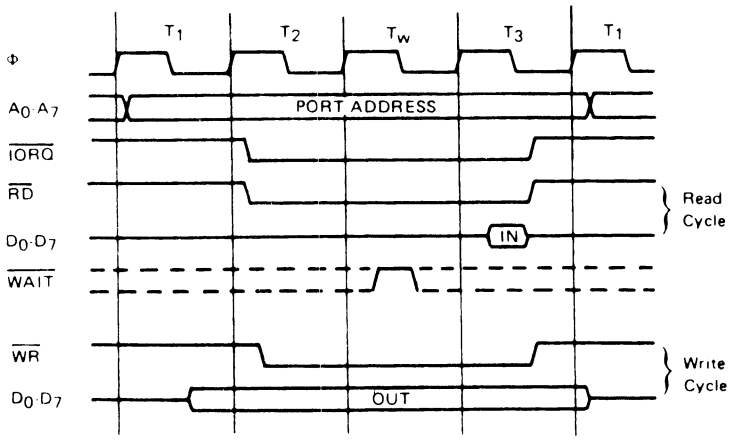
This diagram illustrates the timing of memory read or write cycles other than an op code fetch (M_1 cycle). The function of the $\overline{MREQ}$ and $\overline{RD}$ signals is exactly the same as in the op code fetch cycle. When a memory write cycle is implemented, the $\overline{MREQ}$ becomes active and is used directly as a chip enable for dynamic memories, when the address bus is stable. The $\overline{WR}$ line is used directly as a R/W pulse to any type of semiconductor memory, and is active when data on the data bus is stable.



TIMING WAVEFORMS (CONT.)

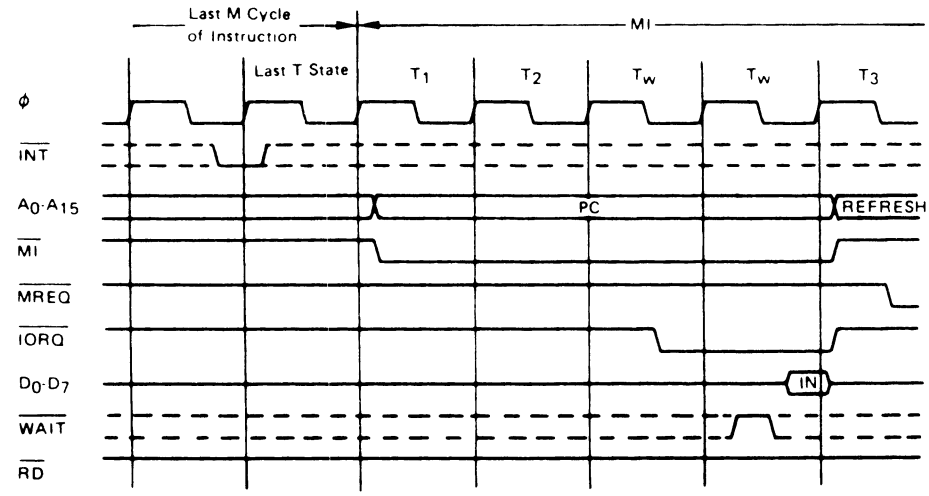
Input or Output Cycles

This illustrates the timing for an I/O read or I/O write operation. A single wait state (T_W) is automatically inserted in I/O operations to allow sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line, if necessary.



Interrupt Request/Acknowledge Cycle

The processor samples the interrupt signal with the rising edge of the last clock at the end of any instruction. A special M_1 cycle is started when an interrupt is accepted. During the M_1 cycle, the $\overline{IORQ}$ (instead of $\overline{MREQ}$) signal becomes active, indicating that the interrupting device can put an 8-bit vector on the data bus. Two wait states (T_W) are automatically added to this cycle. This makes it easy to implement a ripple priority interrupt scheme.



INSTRUCTION SET

The following summary shows the assembly language mnemonic and the symbolic operation performed by the instructions of the μPD780 and μPD780-1 processors. The instructions are divided into 16 categories:

Miscellaneous Group	8-Bit Loads
Rotates and Shifts	16-Bit Loads
Bit Set, Reset and Test	Exchanges
Input and Output	Memory Block Moves
Jumps	Memory Block Searches
Calls	8-Bit Arithmetic and Logic
Restarts	16-Bit Arithmetic
Returns	General Purpose Accumulator and Flag Operations

The addressing Modes include combinations of the following:

Indexed	Immediate
Register	Immediate Extended
Implied	Modified Page Zero
Register Indirect	Relative
Bit	Extended

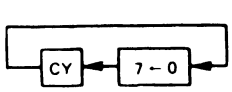
INSTRUCTION SET TABLE

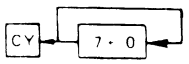
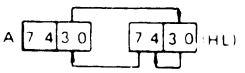
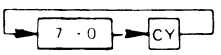
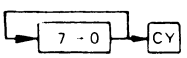
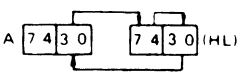
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
ADC HL, ss	HL ← HL + ss + CY	Add with carry reg. pair ss to HL	1	11	↕	↕	V	↕	0	X	11 101 101 Ⓐ 01 ss1 010
ADC A, r	A ← A + r + CY	Add with carry Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 001 rrr Ⓑ
ADC A,n	A ← A + n + CY	Add with carry value n to ACC		7	↕	↕	V	↕	0	↕	11 001 110 nn nnn nnn
ADC A, (HL)	A ← A + (HL) + CY	Add with carry loc. (HL) to ACC		7	↕	↕	V	↕	0	↕	10 001 110
ADC A, (IX + d)	A ← A + (IX + d) + CY	Add with carry loc. (IX + d) to ACC		19	↕	↕	V	↕	0	↕	11 011 101 10 001 110 dd ddd ddd
ADC A, (IY + d)	A ← A + (IY + d) + CY	Add with carry loc. (IY + d) to ACC		19	↕	↕	V	↕	0	↕	11 111 101 10 001 110 dd ddd ddd
ADD A, n	A ← A + n	Add value n to ACC	2	7	↕	↕	V	↕	0	↕	11 000 110 nn nnn nnn
ADD A, r	A ← A + r	Add Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 000 rrr Ⓑ
ADD A, (HL)	A ← A + (HL)	Add location (HL) to ACC	1	7	↕	↕	V	↕	0	↕	10 000 110
ADD A, (IX + d)	A ← A + (IX + d)	Add location (IX + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 011 101 10 000 110 dd ddd ddd
ADD A, (IY + d)	A ← A + (IY + d)	Add location (IY + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 111 101 10 000 110 dd ddd ddd
ADD HL, ss	HL ← HL + ss	Add Reg. pair ss to HL	1	11	↕	•	•	•	0	X	00 ss 1 001 Ⓐ
ADD IX, pp	IX ← IX + pp	Add Reg. pair pp to IX	2	15	↕	•	•	•	0	X	11 011 101 Ⓒ 00 pp1 001
ADD IY, rr	IY ← IY + rr	Add Reg. pair rr to IY	2	15	↕	•	•	•	0	X	11 111 101 Ⓓ 00 rr1 001
AND r	A ← A∧r	Logical 'AND' of Reg. r ∧ ACC		4	0	↕	P	↕	0	↕	10 100 rrr Ⓑ
AND n	A ← A∧n	Logical 'AND' of value n ∧ ACC		7	0	↕	P	↕	0	↕	11 100 110 nn nnn nnn
AND (HL)	A ← A∧(HL)	Logical 'AND' of loc. (HL) ∧ ACC		7	0	↕	P	↕	0	↕	10 100 110
AND (IX + d)	A ← A∧(IX + d)	Logical 'AND' of loc. (IX + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 011 101 10 100 110 dd ddd ddd
AND (IY + d)	A ← A∧(IY + d)	Logical 'AND' of loc. (IY + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 111 101 10 100 110 dd ddd ddd
BIT b, (HL)	$Z \leftarrow \overline{(HL)}_b$	Test BIT b of location (HL)	2	12	•	↕	X	X	0	1	11 001 011 Ⓔ 01 bbb 110
BIT b, (IX + d)	$Z \leftarrow \overline{(IX + d)}_b$	Test BIT b at location (IX + d)	4	20	•	↕	X	X	0	1	11 011 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, (IY + d)	$Z \leftarrow \overline{(IY + d)}_b$	Test BIT b at location (IY + d)	4	20	•	↕	X	X	0	1	11 111 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, r	$Z \leftarrow \overline{r}_b$	Test BIT of Reg. r	2	8	•	↕	X	X	0	1	11 001 011 Ⓑ Ⓔ 01 bbb rrr
CALL cc, nn	If condition cc false continue, else same as CALL nn	Call subroutine at location nn if condition cc is true	3	10	•	•	↔	•	•	•	11 ←cc→ 100 Ⓗ nn nnn nnn nn nnn nnn
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	Unconditional call subroutine at location nn	3	17	•	•	•	•	•	•	11 001 101 nn nnn nnn nn nnn nnn
CCF	CY ← CY	Complement carry flag	1	4	↕	•	•	•	0	X	00 111 111
CP r	A − r	Compare Reg. r with ACC		4	↕	↕	V	↕	1	↕	10 111 rrr Ⓑ
CP n	A − n	Compare value n with ACC		7	↕	↕	V	↕	1	↕	11 111 110 nn nnn nnn
CP (HL)	A − (HL)	Compare loc. (HL) with ACC		7	↕	↕	V	↕	1	↕	10 111 110
CP (IX + d)	A − (IX + d)	Compare loc. (IX + d) with ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 111 110 dd ddd ddd
CP (IY + d)		Compare loc. (IY + d) with ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 111 110 dd ddd ddd
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	Compare location (HL) and ACC, decrement HL and BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 101 001
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, decrement HL and BC, repeat until BC = 0	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 111 001

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
CPI	A – (HL) HL ← HL + 1 BC ← BC – 1	Compare location (HL) and ACC, increment HL and decrement BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 100 001
CPIR	A – (HL) HL ← HL + 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, increment HL, decrement BC Repeat until BC = C	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 110 001
CPL	A ← Ā	Complement ACC (1's comp.)	1	4	•	•	•	•	1	1	00 101 111
DAA		Decimal adjust ACC	1	4	↕	↕	P	↕	•	↕	00 100 111
DEC r	r ← r – 1	Decrement Reg. r		4	•	↕	V	↕	1	↕	00 rrr 101Ⓑ
DEC (HL)	(HL) ← (HL) – 1	Decrement loc. (HL)		11	•	↕	V	↕	1	↕	00 110 101
DEC (IX + d)	(IX + d) ← (IX + d) – 1	Decrement loc. (IX + d)		23	•	↕	V	↕	1	↕	11 011 101 00 110 101 dd ddd ddd
DEC (IY + d)	(IY + d) ← (IY + d) – 1	Decrement loc. (IY + d)		23	•	↕	V	↕	1	↕	11 111 101 00 110 101 dd ddd ddd
DEC IX	IX ← IX – 1	Decrement IX	2	10	•	•	•	•	•	•	11 011 101 00 101 011
DEC IY	IY ← IY – 1	Decrement IY	2	10	•	•	•	•	•	•	11 111 101 00 101 011
DEC ss	ss ← ss – 1	Decrement Reg. pair ss	1	6	•	•	•	•	•	•	00 ss1 011Ⓐ
DI	IFF ← 0	Disable interrupts	1	4	•	•	•	•	•	•	11 110 011
DJNZ, e	B ← B – 1 if B = 0 continue if B ≠ 0 PC ← PC + e	Decrement B and jump relative if B = 0	2	8	•	•	•	•	•	•	00 010 000 ◄—e-2—►
EI	IFF ← 1	Enable interrupts	1	4	•	•	•	•	•	•	11 111 011
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	Exchange the location (SP) and HL	1	19	•	•	•	•	•	•	11 100 011
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	Exchange the location (SP) and IX	2	23	•	•	•	•	•	•	11 011 101 11 100 011
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	Exchange the location (SP) and IY	2	23	•	•	•	•	•	•	11 111 101 11 100 011
EX AF, AF'	AF ↔ AF'	Exchange the contents of AF AF'	1	4	•	•	•	•	•	•	00 001 000
EX DE, HL	DE ↔ HL	Exchange the contents of DE and HL	1	4	•	•	•	•	•	•	11 101 011
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	Exchange the contents of BC, DE, HL with contents of BC', DE', HL', respectively	1	4	•	•	•	•	•	•	11 011 001
HALT	Processor Halted	HALT (wait for interrupt or reset)	1	4	•	•	•	•	•	•	01 110 110
IM 0		Set Interrupt mode 0	2	8	•	•	•	•	•	•	11 101 101 01 000 110
IM 1		Set Interrupt mode 1	2	8	•	•	•	•	•	•	11 101 101 01 010 110
IM 2		Set Interrupt mode 2	2	8	•	•	•	•	•	•	11 101 101 01 011 110
IN A, (n)	A ← (n)	Load ACC with input from device n	2	11	•	•	•	•	•	•	11 011 011 nn nnn nnn
IN r, (C)	r ← (C)	Load Reg. r with input from device (C)	2	12	•	↕	P	↕	0	↕	11 101 101① 01 rrr 000
INC (HL)	(HL) ← (HL) + 1	Increment location (HL)	1	11	•	↕	V	↕	0	↕	00 110 100
INC IX	IX ← IX + 1	Increment IX	2	10	•	•	•	•	•	•	11 011 101 00 100 011
INC (IX + d)	(IX + d) ← (IX + d) + 1	Increment location (IX + d)	3	23	•	↕	V	↕	0	↕	11 011 101 00 110 100 dd ddd ddd
INC IY	IY ← IY + 1	Increment IY	2	10	•	•	•	•	•	•	11 111 101 00 100 011
INC (IY + d)	(IY + d) ← (IY + d) + 1	Increment location (IY + d)	3	23	•	↕	V	↕	0	↕	11 111 101 00 110 100 dd ddd ddd
INC r	r ← r + 1	Increment Reg. r	1	4	•	↕	V	↕	0	↕	00 rrr 100Ⓑ
INC ss	ss ← ss + 1	Increment Reg. pair ss	1	6	•	•	•	•	•	•	00 ss0 011Ⓐ
IND	(HL) ← (C) B ← B – 1 HL ← HL – 1	Load location (HL) with input from port (C), decrement HL and B	2	16	•	↕③	X	X	1	X	11 101 101 10 101 010

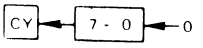
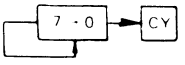
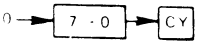
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
INDR	(HL) ← (C) B ← B − 1 HL ← HL − 1 until B = 0	Load location (HL) with input from port (C), decrement HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 111 010
INI	(HL) ← (C) B ← B − 1 HL ← HL + 1	Load location (HL) with input from port (C), and increment HL and decrement B	2	16	•	③	X	X	1	X	11 101 101 10 100 010
INIR	(HL) ← (C) B ← B − 1 HL ← HL + 1 until B = 0	Load location (HL) with input from port (C), increment HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 110 010
JP (HL)	PC ← HL	Unconditional jump to (HL)	1	4	•	•	•	•	•	•	11 101 001
JP (IX)	PC ← IX	Unconditional jump to (IX)	2	8	•	•	•	•	•	•	11 011 101 11 101 001
JP (IY)	PC ← IY	Unconditional jump to (IY)	2	8	•	•	•	•	•	•	11 111 101 11 101 001
JP cc, nn	If cc true PC ← nn else continue	Jump to location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 010 Ⓗ nn nnn nnn nn nnn nnn
JP nn	PC ← nn	Unconditional jump to location nn	3	10	•	•	•	•	•	•	11 000 011 nn nnn nnn nn nnn nnn
JR C, e	If C = 0 continue If C = 1 PC ← PC + e	Jump relative to PC + e, if carry = 1	2	7 if condition met 12, if not	•	•	•	•	•	•	00 111 000 ←— e-2 —→
JR e	PC ← PC + e	Unconditional jump relative to PC + e	2	12	•	•	•	•	•	•	00 011 000 ←— e-2 —→
JR NC, e	If C = 1 continue If C = 0 PC ← PC + e	Jump relative to PC + e if carry = 0	2	7	•	•	•	•	•	•	00 110 000 ←— e-2 —→
JR NZ, e	If Z = 1 continue	Jump relative to PC + e if non-zero (Z = 0)	2	7	•	•	•	•	•	•	00 100 000 ←— e-2 —→
JR Z, e	If Z = 0 continue	Jump relative to PC + e if zero (Z = 1)	2	7	•	•	•	•	•	•	00 101 000 ←— e-2 —→
LD A, (BC)	A ← (BC)	Load ACC with location (BC)	1	7	•	•	•	•	•	•	00 001 010
LD A, (DE)	A ← (DE)	Load ACC with location (DE)	1	7	•	•	•	•	•	•	00 011 010
LD A, I	A ← I	Load ACC with I	2	9	•	↕	IFF	↕	0	0	11 101 101 01 010 111
LD A, (nn)	A ← (nn)	Load ACC with location nn	3	13	•	•	•	•	•	•	00 111 010 nn nnn nnn nn nnn nnn
LD A, R	A ← R	Load ACC with Reg. R	2	9	•	↕	IFF	↕	0	0	11 101 101 01 011 111
LD (BC), A	(BC) ← A	Load location (BC) with ACC	1	7	•	•	•	•	•	•	00 000 010
LD (DE), A	(DE) ← A	Load location (DE) with ACC	1	7	•	•	•	•	•	•	00 010 010
LD (HL), n	(HL) ← n	Load location (HL) with value n	2	10	•	•	•	•	•	•	00 110 110 nn nnn nnn
LD ss, nn	ss ← nn	Load Reg. pair ss with value nn	4	20	•	•	•	•	•	•	00 ss0 001 Ⓐ nn nnn nnn nn nnn nnn
LD HL, (nn)	H ← (nn + 1) L ← (nn)	Load HL with location (nn)	3	16	•	•	•	•	•	•	00 101 010 nn nnn nnn nn nnn nnn
LD (HL), r	(HL) ← r	Load location (HL) with Reg. r	1	7	•	•	•	•	•	•	01 110 rrr Ⓑ
LD I, A	I ← A	Load I with ACC	2	9	•	•	•	•	•	•	11 101 101 01 000 111
LD IX, nn	IX ← nn	Load IX with value nn	4	19	•	•	•	•	•	•	11 011 101 00 100 001 nn nnn nnn nn nnn nnn
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	Load IX with location (nn)	4	20	•	•	•	•	•	•	11 011 101 00 101 010 nn nnn nnn nn nnn nnn
LD (IX + d), n	(IX + d) ← n	Load location (IX + d) with value n	4	19	•	•	•	•	•	•	11 011 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IX + d), r	(IX + d) ← r	Load location (IX + d) with Reg. r	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 110 rrr dd ddd ddd

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
LD IY, nn	IY ← nn	Load IY with value nn	4	14	•	•	•	•	•	•	11 111 101 00 100 001 nn nnn nnn nn nnn nnn
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	Load IY with location (nn)	4	20	•	•	•	•	•	•	11 111 101 00 101 010 nn nnn nnn nn nnn nnn
LD ss, (nn)	ss_H ← (nn + 1) ss_L ← (nn)	Load Reg. pair dd with location (nn)	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss1 011 nn nnn nnn nn nnn nnn
LD (IY + d), n	(IY + d) ← n	Load (IY + d) with value n	4	19	•	•	•	•	•	•	11 111 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IY + d), r	(IY + d) ← r	Load location (IY + d) with Reg. r	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 110 rrr dd ddd ddd
LD (nn), A	(nn) ← A	Load location (nn) with ACC	3	13	•	•	•	•	•	•	00 110 010 nn nnn nnn nn nnn nnn
LD (nn), ss	(nn + 1) ← ss_H (nn) ← ss_L	Load location (nn) with Reg. pair dd	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss0 011 nn nnn nnn nn nnn nnn
LD (nn), HL	(nn + 1) ← H (nn) ← L	Load location (nn) with HL	3	16	•	•	•	•	•	•	00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	Load location (nn) with IX	4	20	•	•	•	•	•	•	11 011 101 00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	Load location (nn) with IY	4	20	•	•	•	•	•	•	11 111 101 00 100 010 nn nnn nnn nn nnn nnn
LD R, A	R ← A	Load R with ACC	2	9	•	•	•	•	•	•	11 101 101 01 001 111
LD r, (HL)	r ← (HL)	Load Reg. r with location (HL)	1	7	•	•	•	•	•	•	01 rrr 110 Ⓑ
LD r, (IX + d)	r ← (IX + d)	Load Reg. r with location (IX + d)	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, (IY + d)	r ← (IY + d)	Load Reg. r with location (IY + d)	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, n	r ← n	Load Reg. r with value n	2	7	•	•	•	•	•	•	00 rrr 110 Ⓑ nn nnn nnn
LD, r, r'	r ← r'	Load Reg. r with Reg. r'	1	4	•	•	•	•	•	•	01 rrr r'r' Ⓕ
LD SP, HL	SP ← HL	Load SP with HL	1	6	•	•	•	•	•	•	11 111 001
LD SP, IX	SP ← IX	Load SP with IX	2	10	•	•	•	•	•	•	11 011 101 11 111 001
LD SP, IY	SP ← IY	Load SP with IY	2	10	•	•	•	•	•	•	11 111 101 11 111 001
LDD	(DE) ← (HL) DE ← DE - 1 HL ← HL - 1 BC ← BC - 1	Load location (DE) with location (HL), decrement DE, HL and BC	2	16	•	•	↕	•	0	0	11 101 101 10 101 000
LDDR	(DE) ← (HL) DE ← DE - 1 HL ← HL - 1 BC ← BC - 1 until BC = 0	Load location (DE) with location (HL)	2	21	•	•	0	•	0	0	11 101 101 10 111 000
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC - 1	Load location (DE) with location (HL), increment DE, HL; decrement BC	2	16	•	•	↕①	•	0	0	11 101 101 10 100 000
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC - 1 until BC = 0	Load location (DE) with location (HL), increment DE, HL; decrement BC and repeat until BC = 0	2	21 if BC ≠ 0 16 if BC = 0	•	•	0	•	0	0	11 101 101 10 110 000
NEG	A ← 0 - A	Negate ACC (2's complement)	2	8	↕	↕	V	↕	1	↕	11 101 101 01 000 100

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
NOP		No operation	1	4	•	•	•	•	•	•	00 000 000
OR r	A ← AV r	Logical 'OR' of Reg. r and ACC		4	0	↕	P	↕	0	↕	10 110 r r r Ⓑ
OR n	A ← AV n	Logical 'OR' of value n and ACC		7	•	↕	P	↕	0	↕	11 110 110 n n n n n n n n
OR (HL)	A ← AV (HL)	Logical 'OR' of loc. (HL) and ACC		7	•	↕	P	↕	0	↕	10 110 110
OR (IX + d)	A ← (IX + d)	Logical 'OR' of loc. (IX + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 011 101 10 110 110 d d d d d d d d
OR (IY + d)	A ← AV (IY + d)	Logical 'OR' of loc. (IY + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 111 101 10 110 110 d d d d d d d d
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 until B = 0	Load output port (C) with contents of location (HL), decrement HL and B, repeat until B = 0	2	21 if B ≠ 0 16 if B = 0	•	1	x	x	1	x	11 101 101 10 111 011
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 until B = 0	Load output port (C) with location (HL), increment HL, decrement B, repeat until B = 0	2	21 if B ≠ 0 16 if B = 0	•	1	x	x	1	x	11 101 101 10 110 011
OUT (C), r	(C) ← r	Load output port (C) with Reg. r	2	12	•	•	•	•	•	•	11 101 101 Ⓑ 01 r r r 001
OUT (n), A	(n) ← A	Load output port (n) with ACC	2	11	•	•	•	•	•	•	11 010 011 n n n n n n n n
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕③	x	x	1	x	11 101 101 10 101 011
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕③	x	x	1	x	11 101 101 10 100 011
POP IX	IX_H ← (SP + 1) IX_L ← (SP)	Load IX with top of stack	2	14	•	•	•	•	•	•	11 011 101 11 100 001
POP IY	IY_H ← (SP + 1) IY_L ← (SP)	Load IY with top of stack	2	14	•	•	•	•	•	•	11 111 101 11 100 001
POP qq	qq_H ← (SP + 1) qq_L ← (SP)	Load Reg. pair qq with top of stack	1	10	•	•	•	•	•	•	11 qq0 001 Ⓖ
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H	Load IX onto stack	2	15	•	•	•	•	•	•	11 011 101 11 100 101
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H	Load IY onto stack	2	15	•	•	•	•	•	•	11 111 101 11 100 101
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H	Load Reg. pair qq onto stack	1	11	•	•	•	•	•	•	11 qq0 101 Ⓖ
RES b, r	S_b ← 0	Reset Bit b of Reg. r		8	•	•	•	•	•	•	11 001 011 Ⓑ 10 b b b r r r Ⓔ
RES b, (HL)	S_b ← 0, (HL)	Reset Bit b of loc. (HL)		15	•	•	•	•	•	•	11 001 011 10 b b b 110
RES b, (IX + d)	S_b ← 0, (IX + d)	Reset Bit b of loc. (IX + d)		23	•	•	•	•	•	•	11 011 101 11 001 011 d d d d d d d d 10 b b b 110
RES b, (IY + d)	S_b ← 0, (IY + d)	Reset Bit b of loc. (IY + d)		23	•	•	•	•	•	•	11 111 101 11 001 011 d d d d d d d d 10 b b b 110
RET	PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine	1	10	•	•	•	•	•	•	11 001 001
RET cc	If condition cc is false cont. else (PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine if condition cc is true	1	5 if CC false 11 if CC true	•	•	•	•	•	•	11 ←cc→ 000 Ⓗ
RETI		Return from interrupt	2	14	•	•	•	•	•	•	11 101 101 01 001 101
RETN		Return from non-maskable interrupt	2	14	•	•	•	•	•	•	11 101 101 01 000 101
RL r		Rotate left through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 010 r r r
RL (HL)		Rotate left through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 010 110
RL (IX + d)	 m = r, (HL), (IX + d), (IY + d), A	Rotate left through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 d d d d d d d d 00 010 110
RL (IY + d)		Rotate left through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 d d d d d d d d 00 010 110
RLA		Rotate left ACC through carry	1	4	↕	•	•	•	0	0	00 010 111

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
RLC (HL)		Rotate location (HL) left circular	2	15	↕	↕	P	↕	0	0	11 001 011 00 000 110
RLC (IX + d)		Rotate location (IX + d) left circular	4	23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 000 110
RLC (IY + d)	 m = r, (HL), (IX + d), (IY + d), A	Rotate location (IY + d) left circular	4	23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 000 110
RLC r		Rotate Reg. r left circular	2	8	↕	↕	P	↕	0	0	11 001 011 (B) 00 000 r r r
RLCA		Rotate left circular ACC	1	4	↕	•	•	•	0	0	00 000 111
RLD		Rotate digit left and right between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 101 111
RR r		Rotate right through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 011 r r r
RR (HL)		Rotate right through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 011 110
RR (IX + d)		Rotate right through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 011 110
RR (IY + d)	 m = r, (HL), (IX + d), (IY + d), A	Rotate right through carry loc (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 011 110
RRA		Rotate right ACC through carry	1	4	↕	•	•	•	0	0	00 011 111
RRC r		Rotate Reg. r right circular		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 001 r r r
RRC (HL)		Rotate loc. (HL) right circular		4	↕	↕	P	↕	0	0	11 001 011 00 001 110
RRC (IX + d)		Rotate loc. (IX + d) right circular		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 001 110
RRC (IY + d)	m = r, (HL), (IX + d), (IY + d), A	Rotate loc. (IY + d) right circular		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 001 110
RRCA		Rotate right circular ACC	1	4	↕	•	•	•	0	0	00 001 111
RRD		Rotate digit right and left between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 100 111
RST t	(SP - 1) ← PC_H (SP - 2) ← PC_L PC_H ← 0, PC_L ← T	Restart to location T	1	11	•	•	•	•	•	•	11 t t t 111
SBC A, r	A ← A - r - CY	Subtract Reg. r from ACC w/carry	1	4	↕	↕	V	↕	1	↕	10 011 r r r (B)
SBC A, n	A ← A - n - CY	Subtract value n from ACC with carry		7	↕	↕	V	↕	1	↕	11 011 110 n n n n n n n n
SBC A, (HL)	A ← A - (HL) - CY	Sub. loc. (HL) from ACC w/carry		7	↕	↕	V	↕	1	↕	10 011 110
SBC A, (IX + d)	A ← A - (IX + d) - CY	Subtract loc. (IX + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 011 101 10 011 110 dd ddd ddd
SBC A, (IY + d)	A ← A - (IY + d) - CY	Subtract loc. (IY + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 111 101 10 011 110 dd ddd ddd
SBC HL, ss	HL ← HL - ss - CY	Subtract Reg. pair ss from HL with carry	2	15	↕	↕	V	↕	1	X	11 101 101 (A) 01 s s 0 010
SCF	CY ← 1	Set carry flag (C = 1)	1	4	1	•	•	•	0	0	00 110 111
SET b, (HL)	$(HL)_b$ ← 1	Set Bit b of location (HL)	2	15	•	•	•	•	•	•	11 001 011 (E) 11 b b b 110
SET b, (IX + d)	$(IX + d)_b$ ← 1	Set Bit b of location (IX + d)	4	23	•	•	•	•	•	•	11 011 101 (E) 11 001 011 dd ddd ddd 11 b b b 110

INSTRUCTION SET TABLE (CONT.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	Set Bit b of location (IY + d)	4	23	•	•	•	•	•	•	11 111 101 Ⓔ 11 001 011 dd ddd ddd 11 bbb 110
SET b, r	$r_b \leftarrow 1$	Set Bit b of Reg r	2	8	•	•	•	•	•	•	11 001 011 Ⓑ 11 bbb rrr
SLA r		Shift Reg r left arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 100 rrr
SLA (HL)		Shift loc (HL) left arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 100 110
SLA (IX + d)		Shift loc (IX + d) left arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 100 110
SLA (IY + d)	m = r, (HL), (IX + d), (IY + d)	Shift loc (IY + d) left arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 100 110
SRA r		Shift Reg r right arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 101 rrr
SRA (HL)		Shift loc (HL) right arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 101 110
SRA (IX + d)		Shift loc (IX + d) right arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 101 110
SRA (IY + d)	m = r, (HL), (IX + d), (IY + d)	Shift loc (IY + d) right arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 101 110
SRL r		Shift Reg r right logical		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 111 rrr
SRL (HL)		Shift loc (HL) right logical		15	↕	↕	P	↕	0	0	11 001 011 00 111 110
SRL (IX + d)		Shift loc (IX + d) right logical		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 111 110
SRL (IY + d)	m = r, (HL), (IX + d), (IY + d)	Shift loc (IY + d) right logical		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 111 110
SUB r	A ← A − r	Subtract Reg r from ACC		4	↕	↕	V	↕	1	↕	10 010 rrr Ⓑ
SUB n	A ← A − n	Subtract value n from ACC		7	↕	↕	V	↕	1	↕	11 010 110 nn nnn nnn
SUB (HL)	A ← A − (HL)	Subtract loc (HL) from ACC		7	↕	↕	V	↕	1	↕	10 010 110
SUB (IX + d)	A ← A − (IX + d)	Subtract loc (IX + d) from ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 010 110 dd ddd ddd
SUB (IY + d)	A ← A − (IY + d)	Subtract loc (IY + d) from ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 010 110 dd ddd ddd
XOR r	A ← A∀r	Exclusive 'OR' Reg r and ACC		4	↕	↕	P	↕	1	↕	10 101 rrr Ⓑ
XOR n	A ← A∀n	Exclusive 'OR' value n and ACC		7	↕	↕	P	↕	1	↕	11 101 110 nn nnn nnn
XOR (HL)	A ← A∀(HL)	Exclusive 'OR' loc (HL) and ACC		7	↕	↕	P	↕	1	↕	10 101 110
XOR (IX + d)	A ← A∀(IX + d)	Exclusive 'OR' loc (IX + d) and ACC		19	↕	↕	P	↕	1	↕	11 011 101 10 101 110 dd ddd ddd
XOR (IY + d)	A ← A∀(IY + d)	Exclusive 'OR' loc (IY + d) and ACC		19	↕	↕	P	↕	1	↕	11 111 101 10 101 110 dd ddd ddd

FLAG NOTES

① P/V flag is 0 if B-1=0, else P/V=1

② Z=1 if A=(HL), else Z=0

③ If B-1=0, Z flag set, else reset

FLAG DEFINITIONS

• = Flag not affected

0 = Flag reset

1 = Flag set

X = Flag unknown

↕ = Flag affected according to result of operation

V = Overflow set

P = Parity set

IFF = Interrupt flip-flop set

Ⓐ

Reg	ss
BC	00
DE	01
HL	10
SP	11

Ⓑ

Reg	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓒ

Reg	pp
BC	00
DE	01
IX	10
SP	11

Ⓓ

Reg	rr
BC	00
DE	01
IY	10
SP	11

Ⓔ

Bit	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Ⓕ

Reg	r,r'
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓖ

Reg	qq
BC	00
DE	01
HL	10
AF	11

Ⓗ

CC	Condition		Relevant Flag
000	NZ	Non Zero	Z
001	Z	Zero	Z
010	NC	Non Carry	C
011	C	Carry	C
100	PO	Parity Odd	P/V
101	PE	Parity Even	P/V
110	P	Sign Positive	S
111	M	Sign Negative	S

Ⓘ

Reg	r
B	000
C	001
D	010
E	011
H	100
L	101
F	110
A	111

FLAG DESCRIPTION

C = Carry/Link
Z = Zero
P/V = Parity/Overflow
S = Sign
N = Add/Subtract
H = Half Carry

PRINTED IN USA

SP780-7-78-3K-GN

PROGRAMMABLE INTERVAL TIMER

DESCRIPTION

The NEC μPD8253 contains three independent, programmable, multi-modal 16-bit counter/timers. It is designed as a general purpose device, fully compatible with the 8080 family. The μPD8253 interfaces directly to the busses of the processor as an array of I/O ports.

The μPD8253 can generate accurate time delays under the control of system software. The three independent 16-bit counters can be clocked at rates from DC to 2 MHz. The system software controls the loading and starting of the counters to provide accurate multiple time delays. The counter output flags the processor at the completion of the time-out cycles.

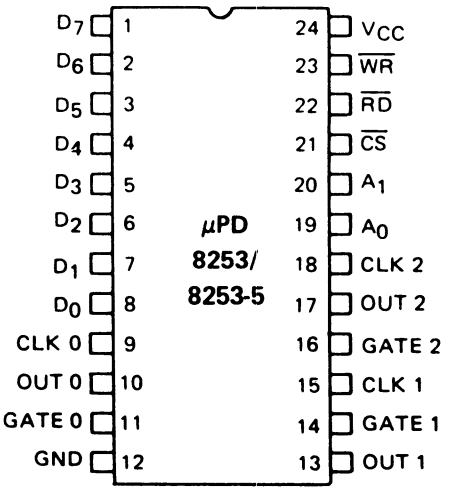
System overhead is greatly improved by relieving the software from the maintenance of timing loops. Some other common uses for the μPD8253 in microprocessor based systems are:

- Programmable Baud Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

FEATURES

- Three Indpendent 16-Bit Counters
- Clock Rate: DC to 3 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5 Volt Supply
- 24 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8-Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0, A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

FUNCTIONAL DESCRIPTION

Data Bus Buffer

The 3-state, 8-bit, bi-directional Data Bus Buffer interfaces the μPD8253 to the 8080A microprocessor system. It will transmit or receive data in accordance with the INput or OUTput instructions executed by the processor. There are three basic functions of the Data Bus Buffer.

1. Program the modes of the μPD8253
2. Load the count registers.
3. Read the count values.

Read/Write Logic

The Read/Write Logic controls the overall operation of the μPD8253 and is governed by inputs received from the processor system bus.

Control Word Register

Two bits from the address bus of the processor, A_0 and A_1, select the Control Word Register when both are at a logic "1" (active-high logic). When selected, the Control Word Register stores data from the Data Bus Buffer in a register. This data is then used to control:

1. The operational MODE of the counters.
2. The selection of BCD or Binary counting.
3. The loading of the count registers.

$\overline{RD}$ (Read)

This active-low signal instructs the μPD8253 to transmit the selected counter value to the processor.

$\overline{WR}$ (Write)

This active-low signal instructs the μPD8253 to receive MODE information or counter input data from the processor.

A_1, A_0

The A_1 and A_0 inputs are normally connected to the address bus of the processor. They control the one-of-three counter selection and address the control word register to select one of the six operational MODES.

$\overline{CS}$ (Chip Select)

The μPD8253 is enabled when an active-low signal is applied to this input. Reading or writing from this device is inhibited when the chip is disabled. The counter operation, however, is not affected.

Counters #0, #1, #2

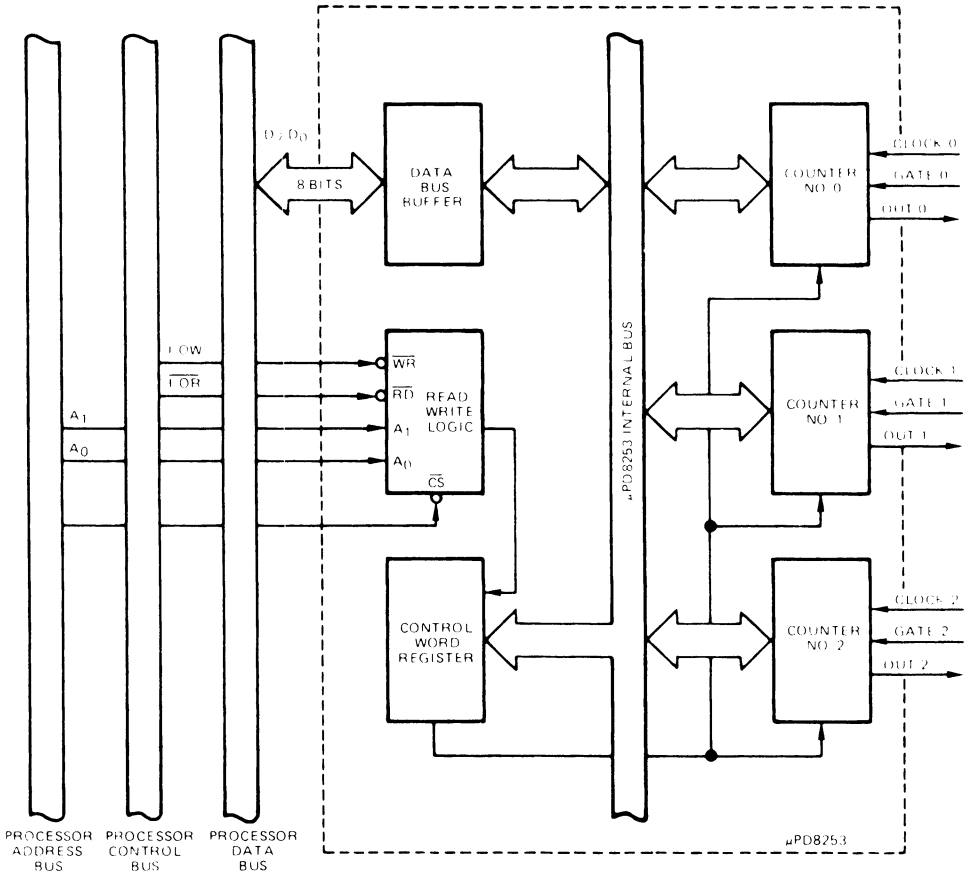
The three identical, 16-bit down counters are functionally independent allowing for separate MODE configuration and counting operation. They function as Binary or BCD counters with their gate, input and output line configuration determined by the operational MODE data stored in the Control Word Register. The system software overhead time can be reduced by allowing the control word to govern the loading of the count data.

The programmer, with READ operations, has access to each counter's contents. The μPD8253 contains the commands and logic to read each counter's contents while still counting without disturbing its operation.

The following is a table showing how the counters are manipulated by the input signals to the Read/Write Logic.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	FUNCTION
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation, 3-State
1	X	X	X	X	Disable, 3-State
0	1	1	X	X	No-Operation, 3-State

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	65°C to +125°C
Voltage on Any Pin	0.5 to +7 Volts (1)

Note: (1) With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device realiability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Input Load Current	I_{IL}			±10	μA	V_{IN} = V_{CC} to 0 V
Output Float Leakage Current	I_{OFL}			±10	μA	V_{OUT} = V_{CC} to 0 V
V_{CC} Supply Current	I_{CC}			95	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Input/Output Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

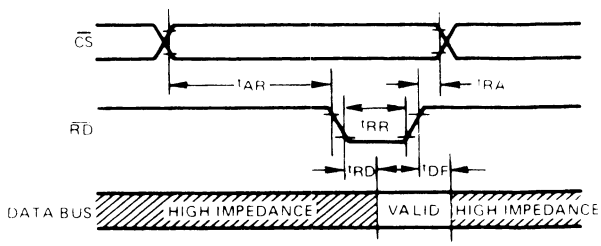
AC CHARACTERISTICS ①

T_a = 0° C to +70° C; V_{CC} = +5V ± 5%; GND = 0V

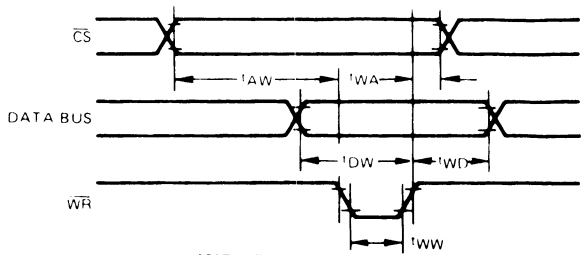
PARAMETER	SYMBOL	LIMITS μPD8253 MIN	μPD8253 TYP	μPD8253 MAX	μPD8253-5 MIN	μPD8253-5 TYP	μPD8253-5 MAX	UNIT	TEST CONDITIONS
READ									
Address Stable Before $\overline{READ}$	t_{AR}	50			50			ns	
Address Hold Time for $\overline{READ}$	t_{RA}	5			5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	400			300			ns	
Data Delay from $\overline{READ}$	t_{RD}			300			200	ns	CL = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}	25		125	25		100	ns	CL = 100 pF
WRITE									
Address Stable Before $\overline{WRITE}$	t_{AW}	20			20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			300			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	200			200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			30			ns	
Recovery Time Between $\overline{WRITES}$	t_{RV}	1			1			μs	
CLOCK AND GATE TIMING									
Clock Period	t_{CLK}	300		DC	300		DC	ns	
High Pulse Width	t_{PWH}	200			200			ns	
Low Pulse Width	t_{PWL}	100			100			ns	
Gate Pulse Width High	t_{GW}	150			150			ns	
Gate Set Up Time to Clock ↑	t_{GS}	100			100			ns	
Gate Hold Time After Clock ↑	t_{GH}	50			50			ns	
Low Gate Width	t_{GL}	100			100			ns	
Output Delay from Clock ↓	t_{OD}			300			300	ns	CL = 100 pF
Output Delay from Gate	t_{ODG}			300			300	ns	CL = 100 pF

Note: ① AC Timing Measured at V_{OH} = 2.2V; V_{OL} = 0.8V.

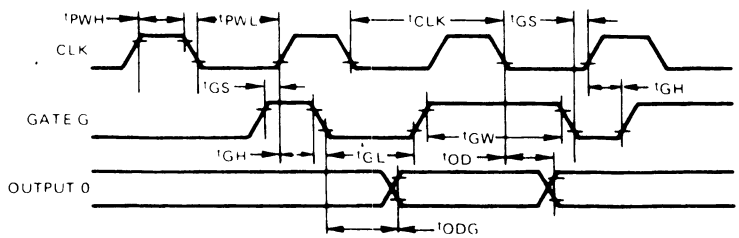
TIMING WAVEFORMS



READ TIMING



WRITE TIMING



CLOCK AND GATE TIMING

PROGRAMMING THE μPD8253

The programmer can select any of the six operational MODES for the counters using system software. Individual counter programming is accomplished by loading the CONTROL WORD REGISTER with the appropriate control word data (A_0, A_1 = 11).

CONTROL WORD FORMAT

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

SC – Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Invalid

RL – Read/Load

RL1	RL0	
0	0	Counter Latching Operation
1	0	Read/Load Most Significant Byte Only
0	1	Read/Load Least Significant Byte Only
1	1	Read/Load Least Significant Byte First, Then Most Significant Byte

BCD

0	Binary Counter, 16-Bits
1	BCD Counter, 4-Decades

M-Mode

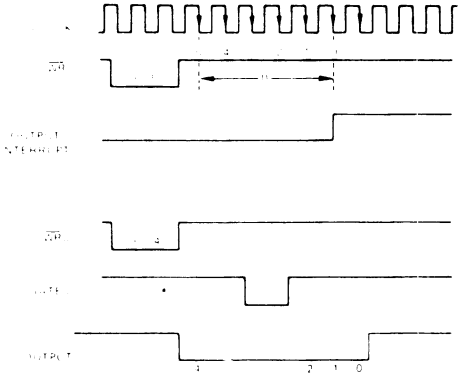
M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

OPERATIONAL MODES ①

Each of the three counters can be individually programmed with different operating MODES by appropriately formatted Control Words. The following is a summary of the MODE operations.

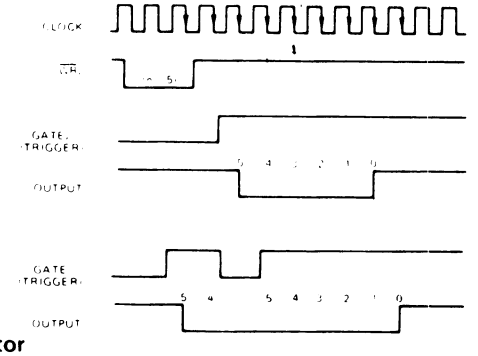
Mode 0: Interrupt on Terminal Count

The initial MODE set operation forces the OUTPUT low. When the specified counter is loaded with the count value, it will begin counting. The OUTPUT will remain low until the terminal count sets it high. It will remain in the high state until the trailing edge of the second $\overline{WR}$ pulse loads in COUNT data. If data is loaded during the counting process, the first $\overline{WR}$ stops the count. Counting starts with the new count data triggered by the falling clock edge after the second $\overline{WR}$. If a GATE pulse is asserted while counting, the count is terminated for the duration of GATE. The falling edge of CLK following the removal of GATE restarts counting from the terminated point.



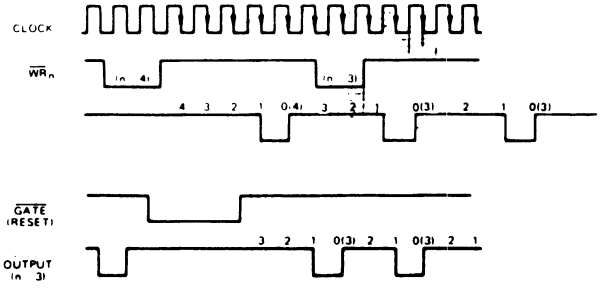
Mode 1: Programmable One-Shot

The OUTPUT is set low by the falling edge of CLOCK following the trailing edge of GATE. The OUTPUT is set high again at the terminal count. The output pulse is not affected if new count data is loaded while the OUTPUT is low. The new data will be loaded on the rising edge of the next trigger pulse. The assertion of a trigger pulse while OUTPUT is low, resets and retriggers the One-Shot. The OUTPUT will remain low for the full count value after the rising edge of TRIGGER.



Mode 2: Rate Generator

The RATE GENERATOR is a variable modulus counter. The OUTPUT goes low for one full CLOCK period as shown in following timing diagram. The count data sets the time between OUTPUT pulses. If the count register is reloaded between output pulses the present period will not be affected. The subsequent period will reflect the new value. The OUTPUT will remain high for the duration of the asserted GATE input. Normal operation resumes on the falling CLOCK edge following the rising edge of GATE.



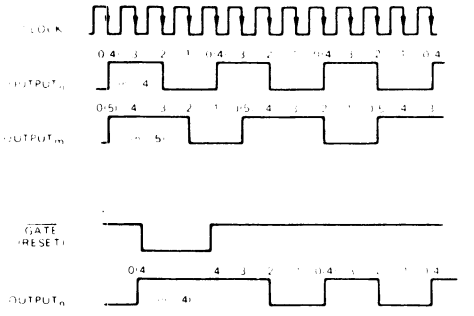
Note: ① All internal counter events occur at the falling edge of the associated clock in all modes of operation.

OPERATIONAL MODES (Cont.)

Mode 3: Square Wave Generator

MODE 3 resembles MODE 2 except the OUTPUT will be high for half of the count and low for the other half (for even values of data). For odd values of count data the OUTPUT will be high one clock cycle longer than when it is low (High Period → $\frac{N+1}{2}$ clock cycles; Low Period → $\frac{N-1}{2}$ clock periods, where N is the decimal value of count data). If the count register is reloaded with a new value during counting, the new value will be reflected immediately after the output transition of the current count.

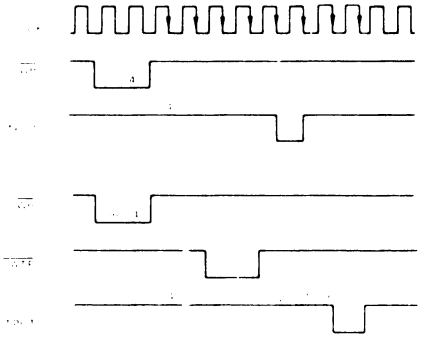
The OUTPUT will be held in the high state while GATE is asserted. Counting will start from the full count data after the GATE has been removed.



Mode 4: Software Triggered Strobe

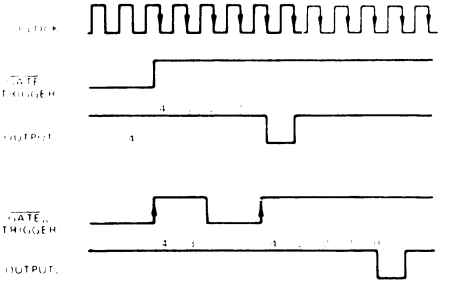
The OUTPUT goes high when MODE 4 is set, and counting begins after the second byte of data has been loaded. When the terminal count is reached, the OUTPUT will pulse low for one clock period. Changes in count data are reflected in the OUTPUT as soon as the new data has been loaded into the count registers. During the loading of new data, the OUTPUT is held high and counting is inhibited.

The OUTPUT is held high for the duration of GATE. The counters are reset and counting begins from the full data value after GATE is removed.

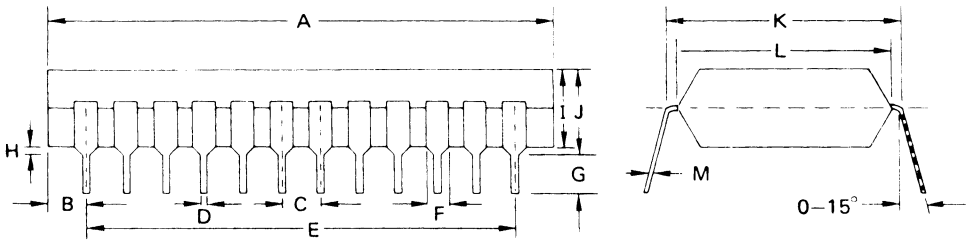


Mode 5: Hardware Triggered Strobe

Loading MODE 5 sets OUTPUT high. Counting begins when count data is loaded and GATE goes high. After terminal count is reached, the OUTPUT will pulse low for one clock period. Subsequent trigger pulses will restart the counting sequence with the OUTPUT pulsing low on terminal count following the last rising edge of the trigger input (Reference bottom half of timing diagram).



PACKAGE OUTLINE
μPD8253C
μPD8253C-5



ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.003}$

PROGRAMMABLE COMMUNICATION INTERFACE

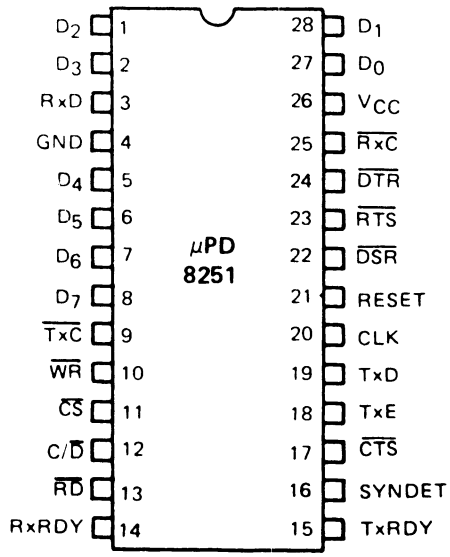
DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the μPD8080 or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART STATUS including data format errors and control signals such as TxE and SYNDET is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate – Synchronous – DC to 56K Baud
  – Asynchronous – DC to 9.6K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply
- Separate Device, Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

D_7 D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

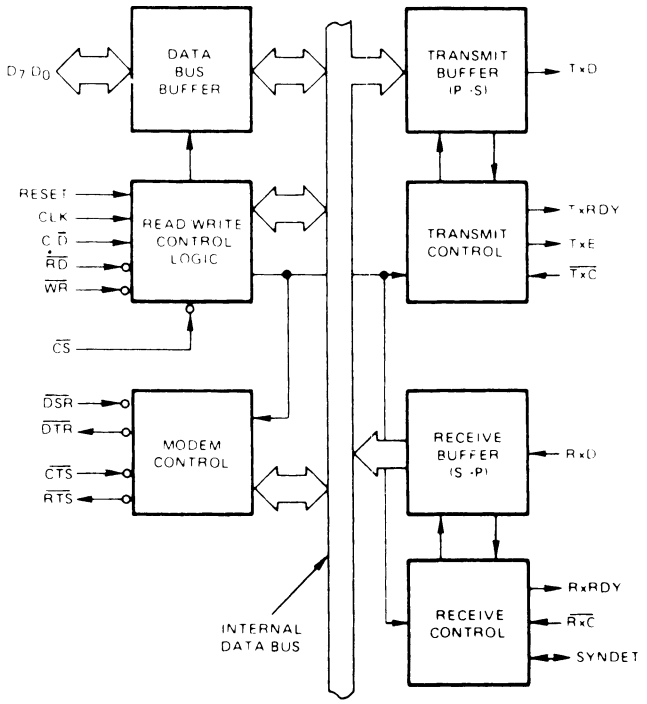
Five Militia Drive/Lexington, Massachusetts 02173 Telephone 617/862-6410 Telex 92-3434 TWX-710-326-6520

FUNCTIONAL DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter is designed specifically for 8080 microcomputer systems but works with most 8-bit processors. Operation of the 8251, like other I/O devices in the 8080 family, is programmed by system software for maximum flexibility.

In the receive mode, a communication interface device must convert incoming serial format data into parallel data and make certain format checks on the data. And in the transmit mode, the device must format data into serial data. The device must also supply or remove characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

BLOCK DIAGRAM



BASIC OPERATION

C/D	RD	WR	CS	
0	0	1	0	8251 → Data Bus
0	1	0	0	Data Bus → 8251
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . - 0°C to +70°C
Storage Temperature . . . . . - 65°C to +125°C
All Output Voltages . . . . . - 0.5 to +7 Volts
All Input Voltages . . . . . - 0.5 to +7 Volts
Supply Voltages . . . . . - 0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

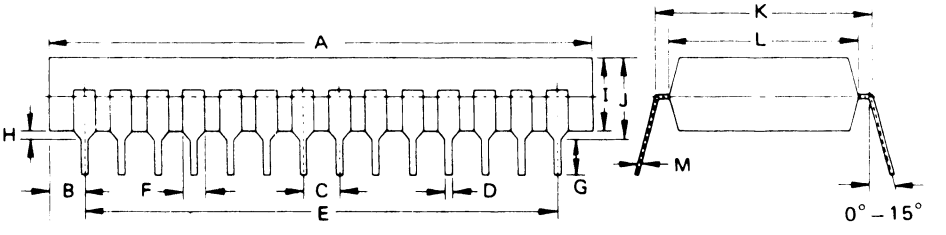
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	GND -.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -100 μA
Data Bus Leakage	I_{DL}			-50	μA	V_{OUT} = 0.45V
				10		V_{OUT} = V_{CC}
Input Load Current	I_{IL}			10	μA	@5.5V
Power Supply Current	I_{CC}		45	80	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE μPD8251C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

BUS PARAMETERS ①

T_a = 0°C to 70°C, V_{CC} = 5.0V ± 5%, GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	50			ns	
Address Hold Time for $\overline{READ}$ ($\overline{CS}$, $\overline{CD}$)	t_{RA}	5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	430			ns	
Data Delay from $\overline{READ}$	t_{RD}			350	ns	C_L = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}			200	ns	C_L = 100 pF
		25				C_L = 15 pF
Recovery Time Between WRITES ②	t_{RV}	6			t_{CY}	
WRITE						
Address Stable before $\overline{WRITE}$	t_{AW}	20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			ns	
OTHER TIMING						
Clock Period ③	t_{CY}	420		1 35	µs	
Clock Pulse Width	$t_{\phi W}$	220		0.7t_{CY}	ns	
Clock Rise and Fall Time	$t_{R,TF}$	0		50	ns	
TxD Delay from Falling Edge of $\overline{TxC}$	t_{DT_x}			1	µs	C_L = 100 pF
Rx Data Set Up Time to Sampling Pulse	t_{SR_x}	2			µs	C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HR_x}	2			µs	C_L = 100 pF
Transmitter Input Clock Frequency	f_{T_x}					
1X Baud Rate		DC		56	KHz	
16X and 64X Baud Rate		DC		520	KHz	
Transmitter Input Clock Pulse Width	t_{TPW}					
1X Baud Rate		12			t_{CY}	
16X and 64X Baud Rate		1			t_{CY}	
Transmitter Input Clock Pulse Delay	t_{TPD}					
1X Baud Rate		15			t_{CY}	
16X and 64X Baud Rate		3			t_{CY}	
Receiver Input Clock Frequency	f_{R_x}					
1X Baud Rate		DC		56	KHz	
16X and 64X Baud Rate		DC		520	KHz	
Receiver Input Clock Pulse Width	t_{RPW}					
1X Baud Rate		12			t_{CY}	
16X and 64X Baud Rate		1			t_{CY}	
Receiver Input Clock Pulse Delay	t_{RPD}					
1X Baud Rate		15			t_{CY}	
16X and 64X Baud Rate		3			t_{CY}	
TxRDY Delay from Center of Data Bit	t_{T_x}			16	t_{CY}	C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{R_x}			20	t_{CY}	
Internal Syndet Delay from Center of Data Bit	t_{IS}			25	t_{CY}	
External Syndet Set Up Time before Falling Edge of $\overline{RxC}$	t_{ES}	16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{T_xE}			16	t_{CY}	C_L = 50 pF
Control Delay from Rising Edge of WRITE (t_{TxE}, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}				t_{CY}	
Control to READ Set Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	16			t_{CY}	

Notes ① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.3, and with load circuit of Figure 1.

② This recovery time is for initialization only; when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

③ The TxC and RxC frequencies have the following limitations with respect to CLK:
For 1X Baud Rate, f_{T_x} or $f_{R_x} \leq 1/30\ t_{CY}$
For 16X and 64X Baud Rate, f_{T_x} or $f_{R_x} \leq 1/4.5\ t_{CY}$

④ Reset Pulse Width = 6 t_{CY} minimum.

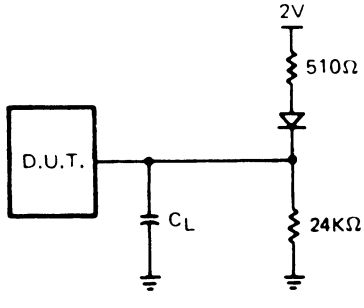
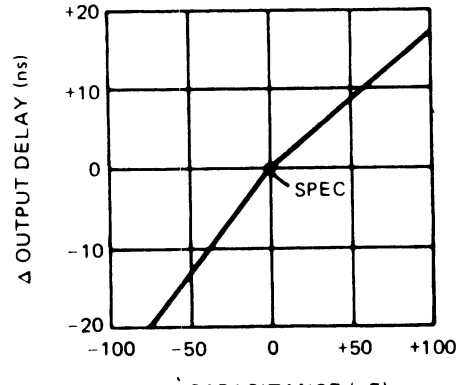


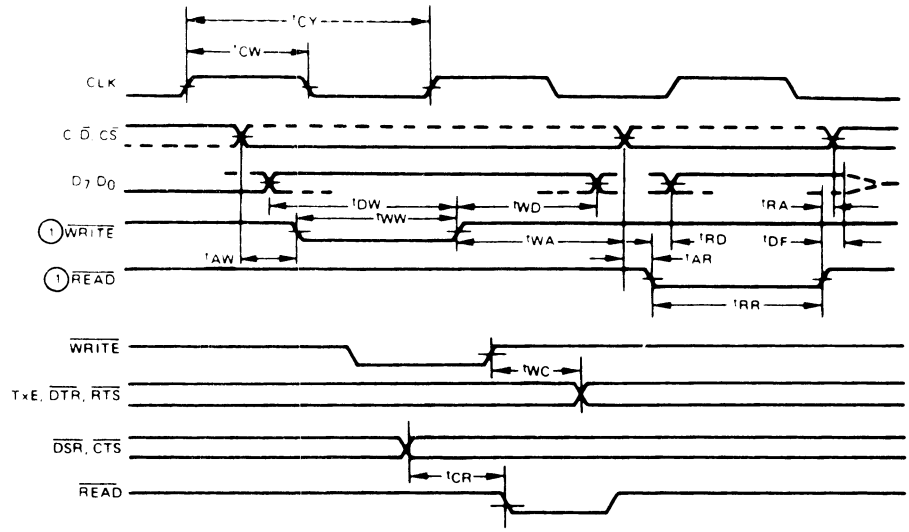
Figure 1.

TEST LOAD CIRCUIT

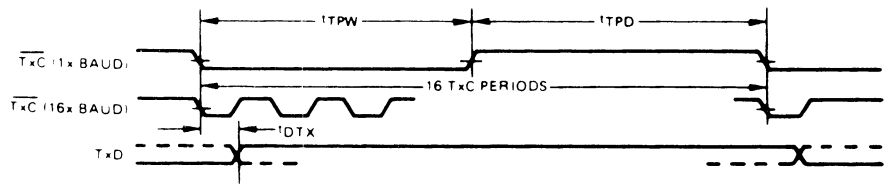


Typical Δ Output Delay Versus Δ Capacitance (pF)

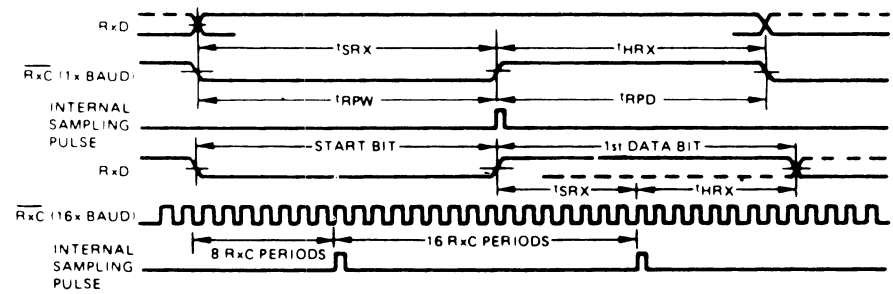
TIMING WAVEFORMS



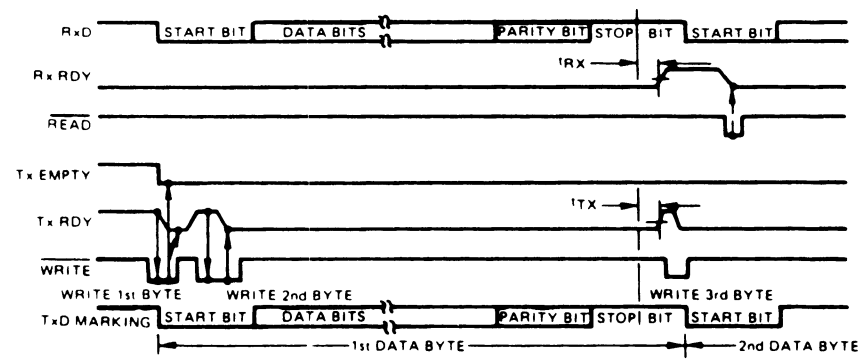
READ AND WRITE TIMING



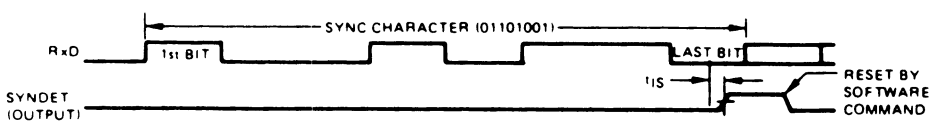
TRASNMITTER CLOCK AND DATA



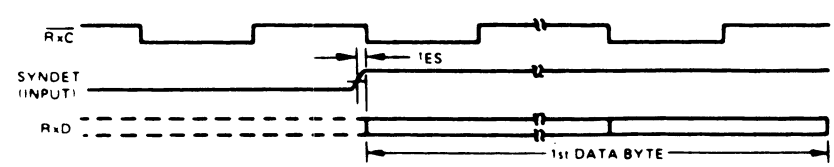
RECEIVER CLOCK AND DATA



TxRDY AND RxRDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT

Note: (1) Write and Read pulses have no timing limitation with respect to CLK.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the 8251 to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the μPD8251 to accept the data or control word which the processor is writing out to the USART via the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the μPD8251 to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART for reading and writing to the processor.
Modem Control			The μPD8251 has a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

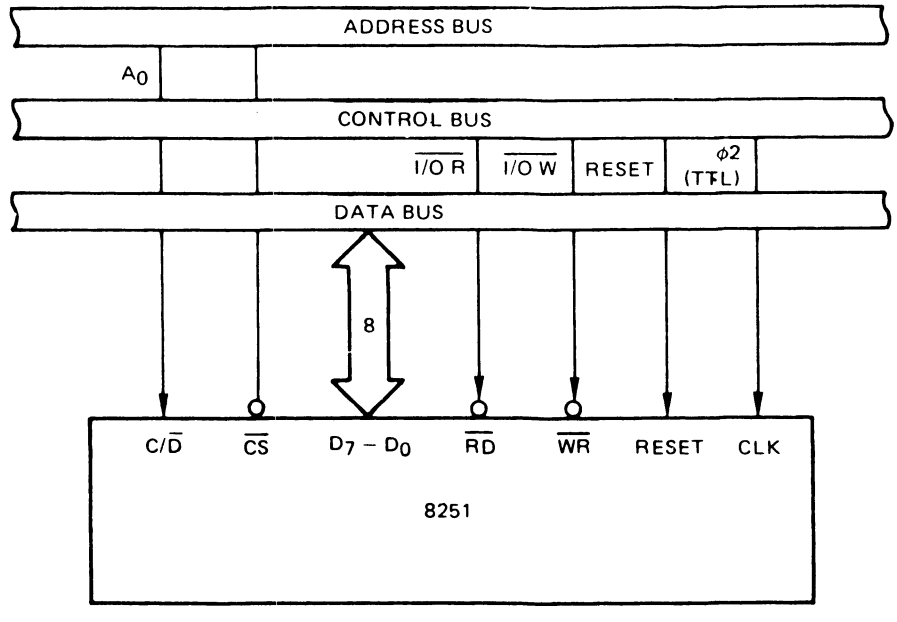
TRANSMIT BUFFER/ CONVERTER

The Transmit Buffer/Converter receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD output.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for Polled operation. Loading a character from the processor automatically resets TxRDY.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

8251 INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVER BUFFER

The Receiver Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 sets the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1,16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 on the rising edge of $\overline{RxC}$. (1)
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.

Note: (1) Since the μPD8251 will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):
- $\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)

If the Baud Rate equals 300:
- $\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
- $\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
- $\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 to define the desired mode and communications format. The control words will specify the BAUD RATE FACTOR (1x, 16x, 64x), CHARACTER LENGTH (5 to 8), NUMBER OF STOP BITS (1, 1-1/2, 2), ASYNCHRONOUS or SYNCHRONOUS MODE, SYNDET (IN or OUT), PARITY, etc.

After receiving the control words, the μPD8251 is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new Command Words.

μPD8251 PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A Reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the 8251.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

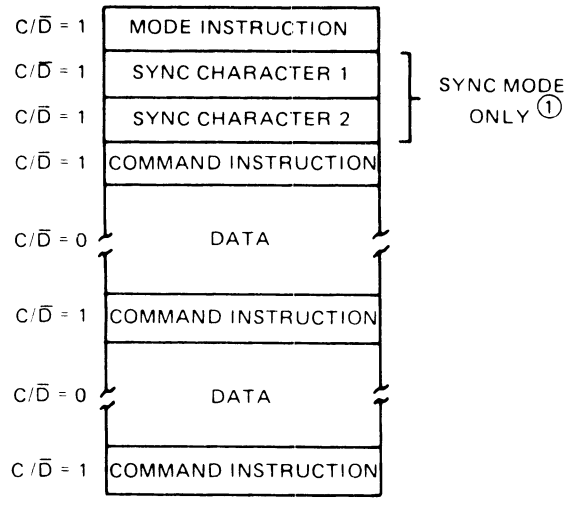
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the SYNCHRONOUS or ASYNCHRONOUS MODE, BAUD RATE FACTOR, CHARACTER LENGTH, PARITY, and NUMBER OF STOP BITS. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE (1) The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

ASYNCHRONOUS TRANSMISSION

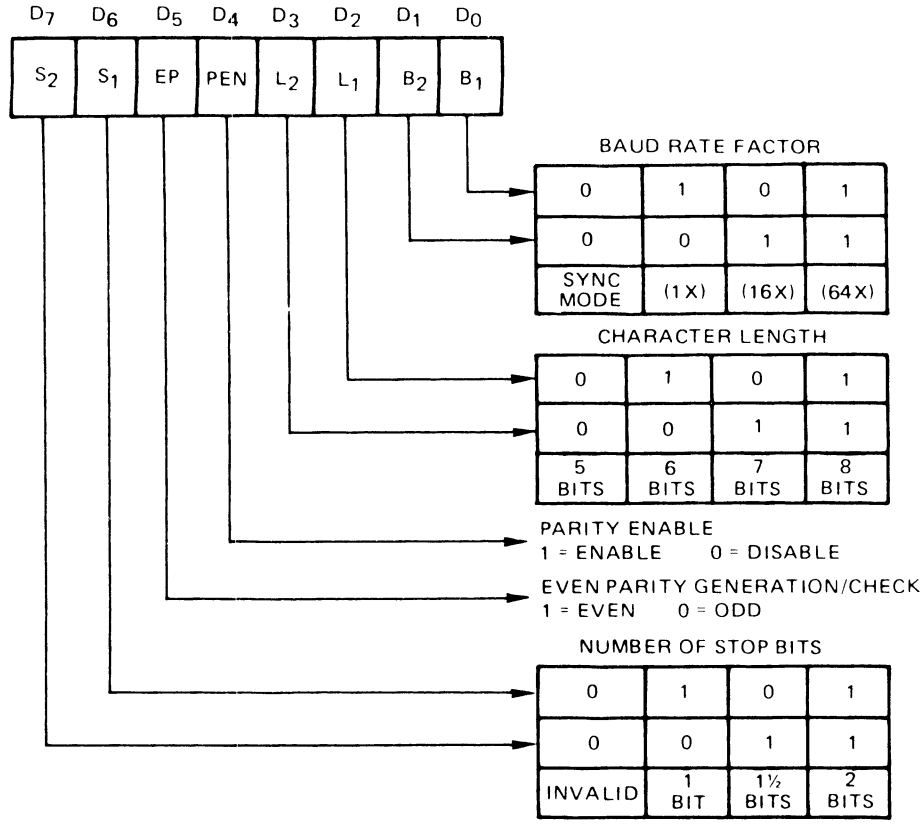
When a data character is written into the μPD8251, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bits(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}/16$ or $\overline{TxC}/64$, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

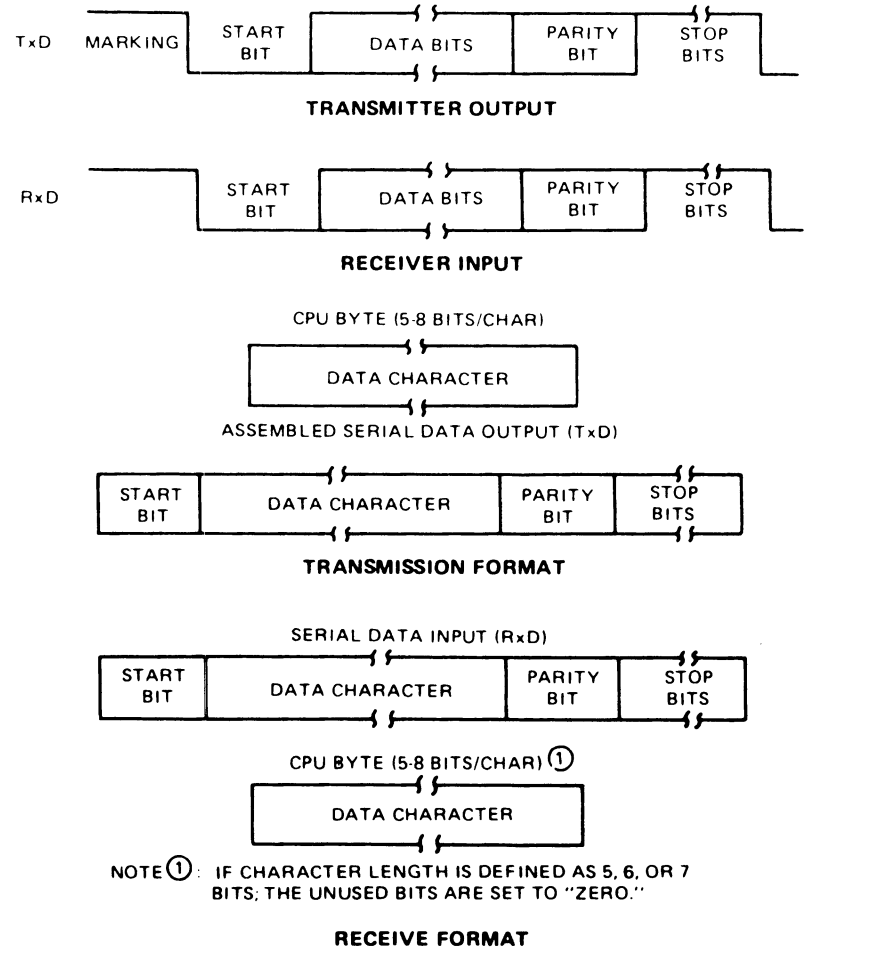
ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

MODE INSTRUCTION FORMAT ASYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



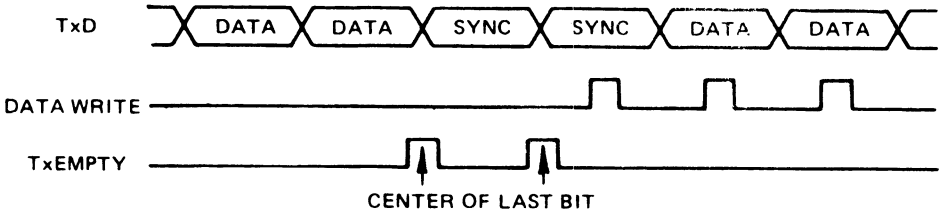
SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 receives the first character from the processor which is usually a SYNC character. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

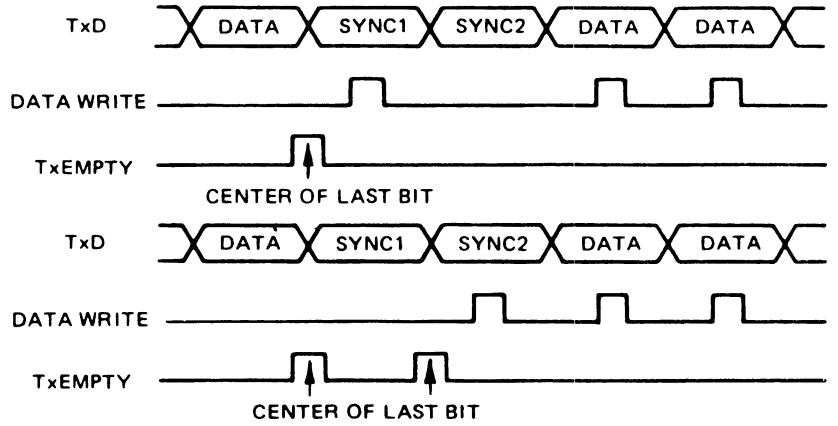
Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 Transmitter Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

TxEMPTY go high at the middle of the last data bit when the Transmit Register is EMPTY. TxEMPTY goes low again as sync characters are transmitted. See figure below.

FOR SINGLE SYNC CHARACTER OPERATION



FOR DOUBLE SYNC CHARACTER OPERATION (BISYNC)



SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

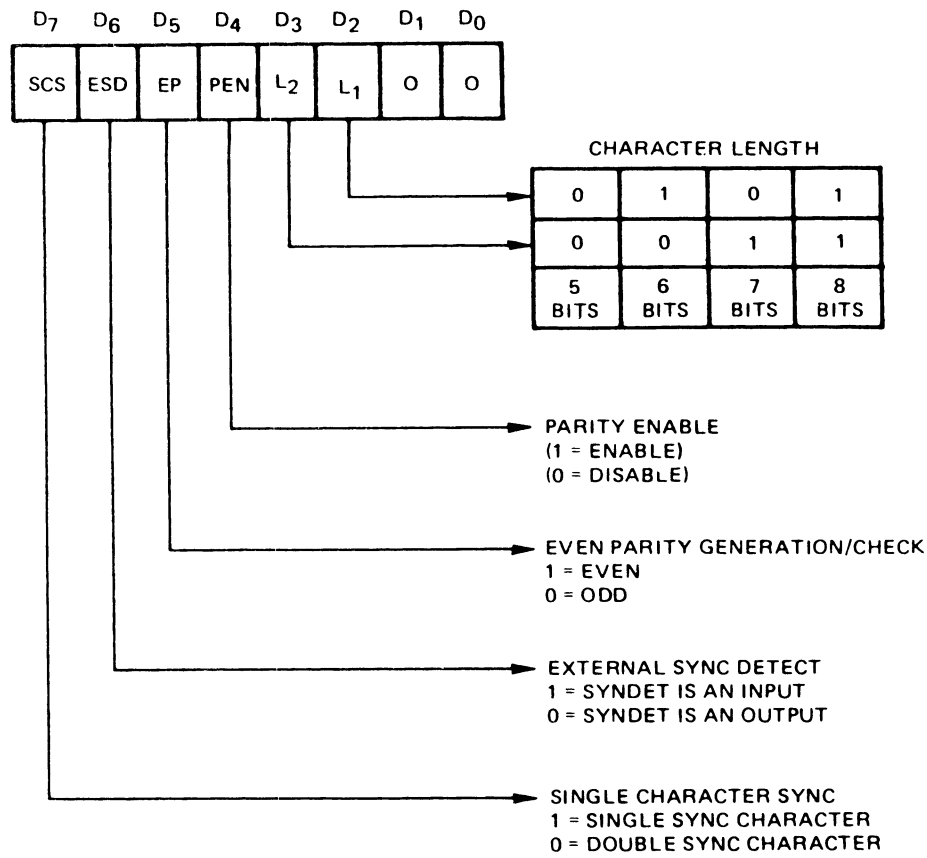
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receiver Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

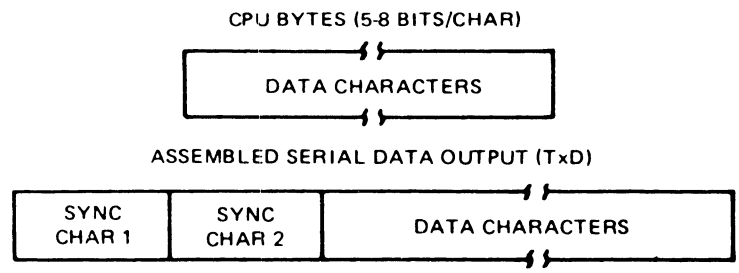
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

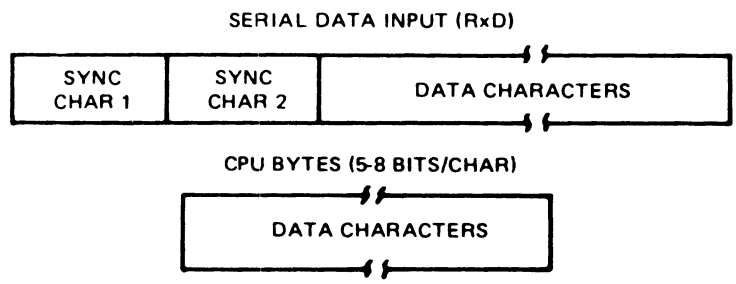
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 has been specified by the Mode Instruction and the SYNC character(s) have been entered, if in SYNC mode, the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s), as needed, are loaded, all subsequent "control writes" ($C/\overline{D}$ = 1) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The μPD8251 has features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of a 16 clock period.

PARITY ERROR

When a parity error is detected, the PE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

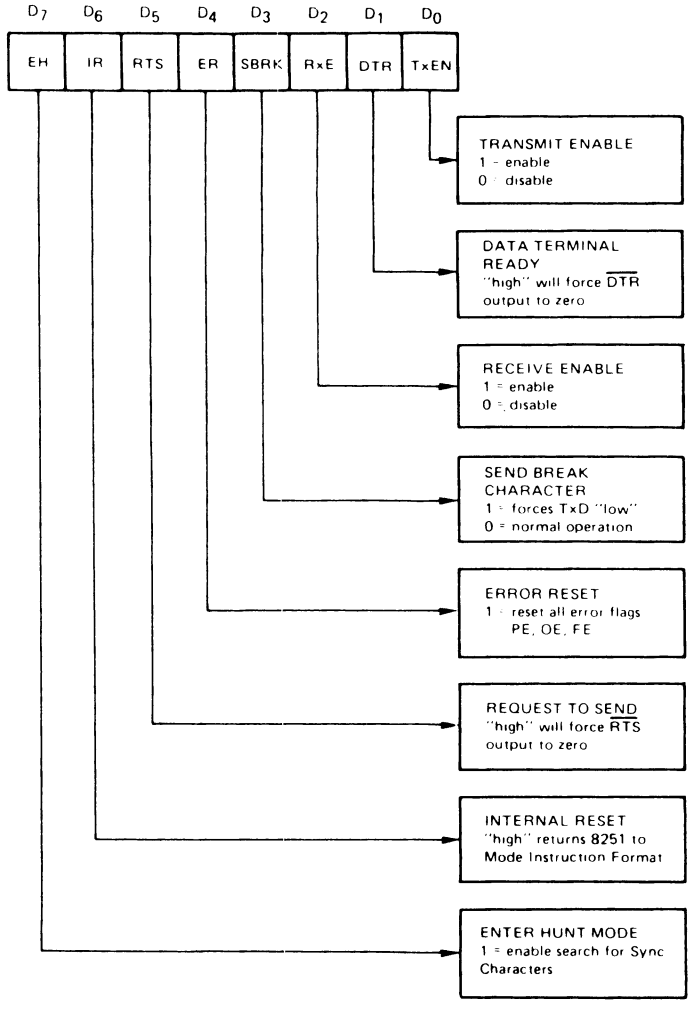
If the processor fails to read a data character before the one following is available, the OE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

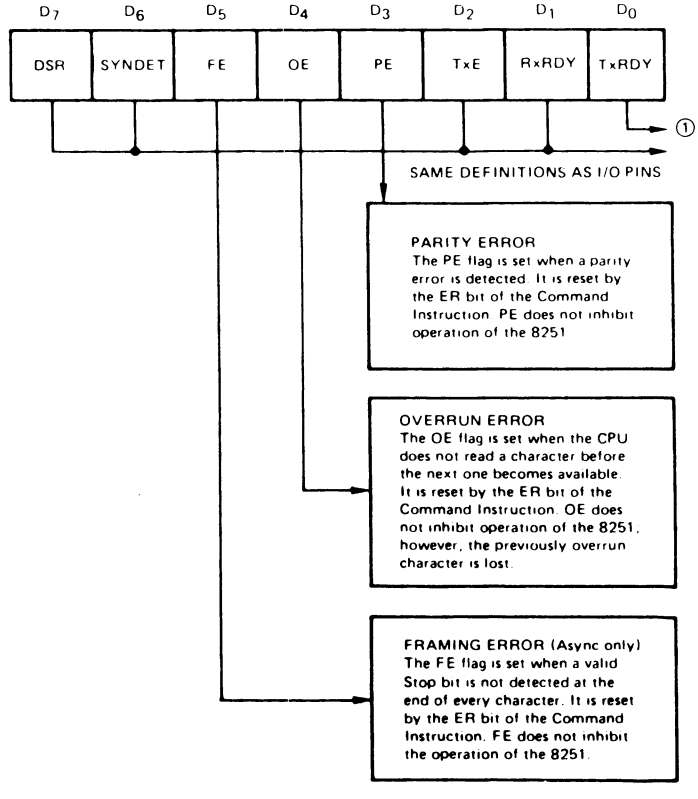
If a valid STOP bit is not detected at the end of a character, the FE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

COMMAND INSTRUCTION FORMAT



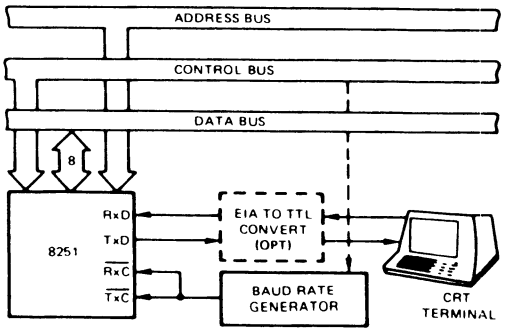
STATUS READ FORMAT



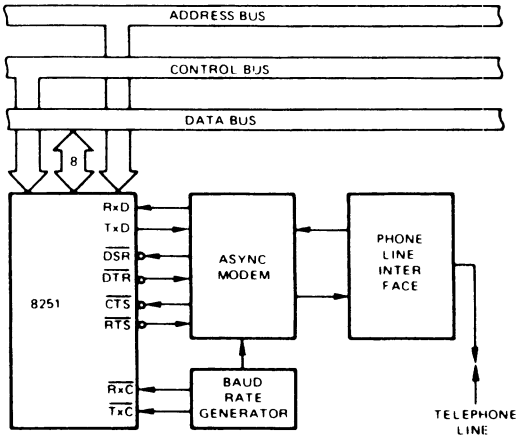
Note: ① TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY status bit = DB Buffer Empty

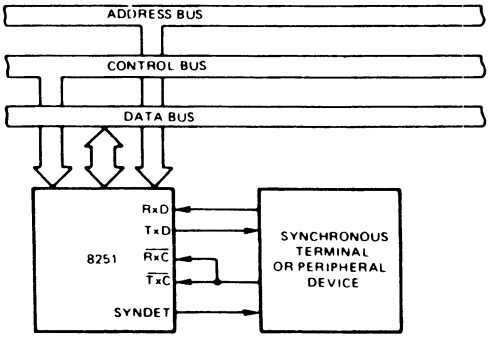
TxRDY (pin 15) = DB Buffer Empty • CTS • TxEn



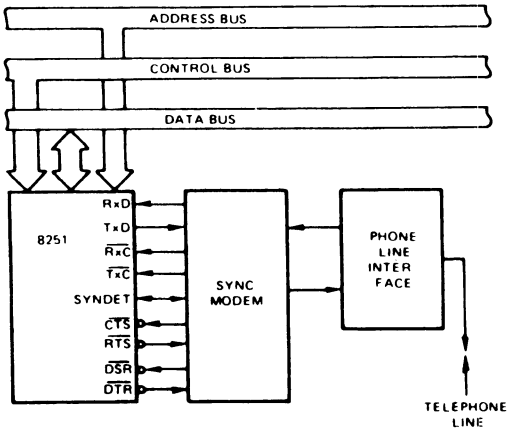
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

PROGRAMMABLE PERIPHERAL INTERFACES

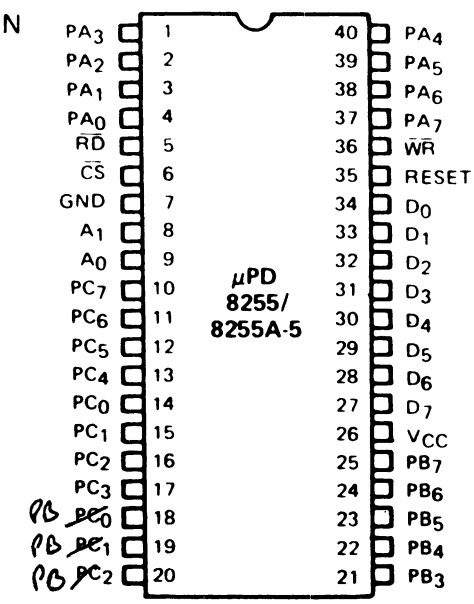
DESCRIPTION

The μPD8255 and μPD8255A-5 are general purpose programmable INPUT/OUTPUT devices designed for use with the 8080A/8085A microprocessors. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bidirectional Bus mode, (MODE 2), uses the 8 lines of Port A for a bidirectional bus, and five lines from Port C for bus control signals. The μPD8255 and μPD8255A-5 are packaged in 40 pin plastic dual-in-line packages.

FEATURES

- Fully Compatible with the 8080A/8085 Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 2 mA Darlington Drive Outputs for Printers and Displays (μPD8255)
- 8 – 4 mA Darlington Drive Outputs for Printers and Displays (μPD8255A-5)
- LSI Drastically Reduces System Package Count
- Standard 40 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

*All data pertaining to the μPD8255A-5 is preliminary.

FUNCTIONAL DESCRIPTION

General

The μPD8255 and μPD8255A-5 Programmable Peripheral Interfaces (PPI) are designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the μPD8255 and μPD8255A-5. The μPD8255 and μPD8255A-5 are functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, eight bit Data Bus Buffer (D_0-D_7) of the μPD8255 and μPD8255A-5 can be directly interfaced to the processor's system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 for communication with the 8080A/8085A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9

Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255 and μPD8255A-5. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C (PC_7-PC_4)
Group II – Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents cannot be read back to the processor.

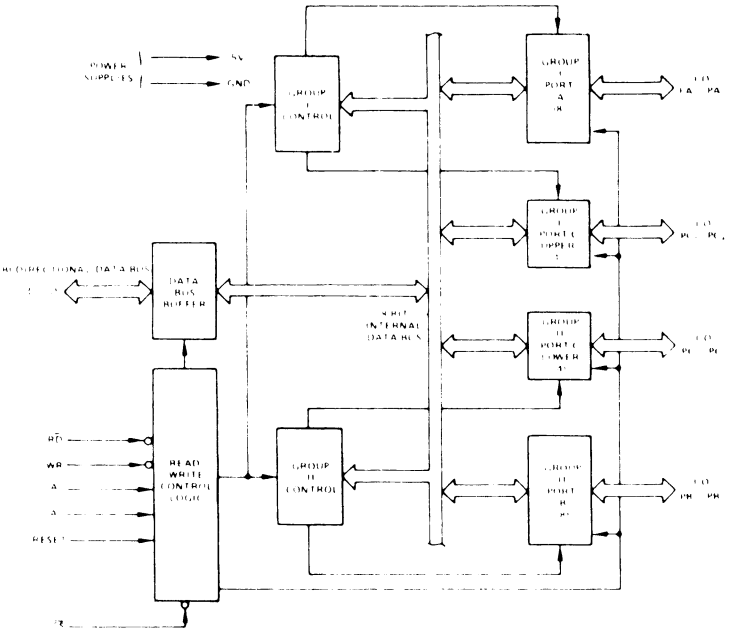
Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255 and μPD8255A-5 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255 and μPD8255A-5 is further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.
Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with Ports A and B.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages ①	-0.5 to +7 Volts
All Input Voltages ①	-0.5 to +7 Volts
Supply Voltages ①	-0.5 to +7 Volts

Note: ① With respect to V_{SS}

COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	μPD8255 TYP	μPD8255 MAX	LIMITS μPD8255A-5 MIN	μPD8255A-5 TYP	μPD8255A-5 MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS}-0.5		0.8	-0.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4			0.45	V	②
Output High Voltage	V_{OH}	2.4			2.4			V	③
Darlington Drive Current	I_{OH} ①	-1	-2	-4	-1	-2	-4	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
Power Supply Current	I_{CC}		40	120		40	120	mA	V_{CC} = +5V, Output Open
Input Leakage Current	I_{LIH}			10			10	μA	V_{IN} = V_{CC}
Input Leakage Current	I_{LIL}			-10			-10	μA	V_{IN} = 0.4V
Output Leakage Current	I_{LOH}			10			10	μA	V_{OUT} = V_{CC}, $\overline{CS}$ = 2.0V
Output Leakage Current	I_{LOL}			-10			-10	μA	V_{OUT} = 0.4V, $\overline{CS}$ = 2.0V

Notes ① Any set of eight (8) outputs from either Port A, B, or C can source 2 mA into 1.5V for μPD8255, or 4 mA into 1.5V for μPD8255A-5.

② For μPD8255 I_{OL} = 1.7 mA
For μPD8255A-5 I_{OL} = 2.5 mA for DB Port, 1.7 mA for Peripheral Ports

③ For μPD8255 I_{OH} = -100 μA for DB Port, -50 μA for Peripheral Ports
For μPD8255A-5 I_{OH} = -400 μA for DB Port, -200 μA for Peripheral Ports

CAPACITANCE

T_a = 25°C, V_{CC} = V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

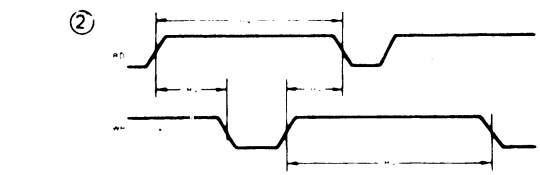
AC CHARACTERISTICS

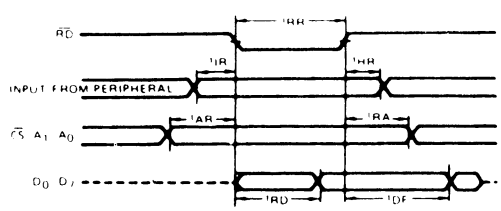
T_a = 0°C to +70°C V_{CC} = +5V ± 5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	LIMITS μPD8255 MAX	LIMITS μPD8255A-5 MIN	LIMITS μPD8255A-5 MAX	UNIT	TEST CONDITIONS
READ							
Address Stable Before $\overline{READ}$	t_{AR}	50		0		ns	
Address Stable After $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	405		300		ns	
Data Valid From $\overline{READ}$	t_{RD}		295		200	ns	8255 C_L = 100 pF 8255A-5 C_L = 150 pF
Data Float After $\overline{READ}$	t_{DF}	10	150	10	100	ns ns	C_L = 100 pF C_L = 15 pF
Time Between $\overline{READ}$s and/or $\overline{WRITE}$s	t_{RV}	850		850		ns	②
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	20		0		ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		300		ns	
Data Valid To $\overline{WRITE}$ (L.E.)	t_{DW}	10		100		ns	
Data Valid After $\overline{WRITE}$	t_{WD}	35		30		ns	
OTHER TIMING							
$\overline{WR}$ = 0 To Output	t_{WB}		500		350	ns	8255 C_L = 50 pF 8255A-5 C_L = 150 pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral Data After $\overline{RD}$	t_{HR}	50		0		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	500		300		ns	
$\overline{STB}$ Pulse Width	t_{ST}	350		500		ns	
Per Data Before T.E. Of $\overline{STB}$	t_{PS}	60		0		ns	
Per Data After T.E. Of $\overline{STB}$	t_{PH}	150		180		ns	
$\overline{ACK}$ = 0 To Output	t_{AD}		400		300	ns	8255 C_L = 50 pF 8255A-5 C_L = 150 pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}	20	300	20	250	ns	8256 C_L = 50 pF 8256 C_L = 15 pF
$\overline{WR}$ = 1 To $\overline{OBF}$ = 0	t_{WOB}		300		650	ns	
$\overline{ACK}$ = 0 To $\overline{OBF}$ = 1	t_{AOB}		450		350	ns	
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}		450		300	ns	8255 C_L = 50 pF
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}		360		300	ns	
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}		450		400	ns	
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}		400		300	ns	8255A-5 C_L = 150 pF
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}		400		350	ns	
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}		850		850	ns	

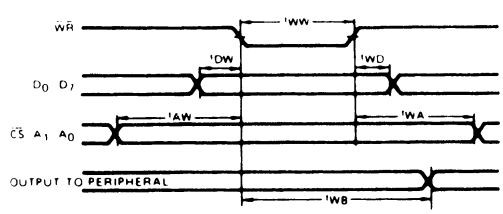
Notes: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

TIMING WAVEFORMS
MODE 0

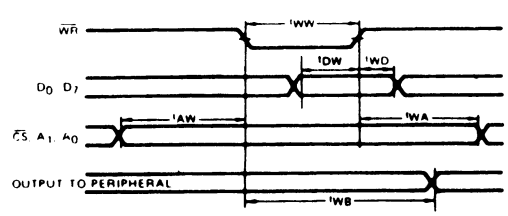




BASIC INPUT



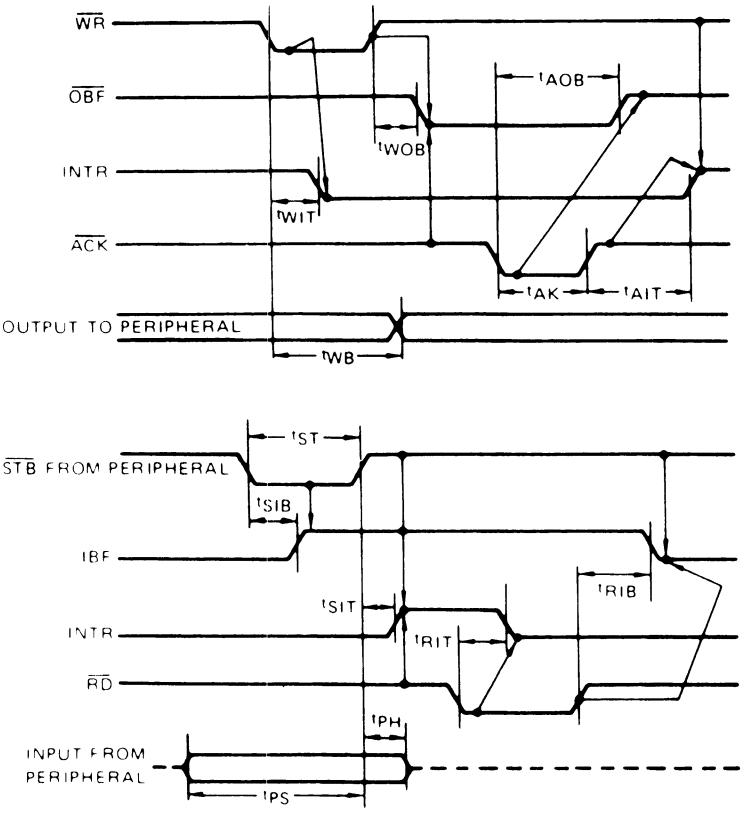
BASIC OUTPUT – μPD8255



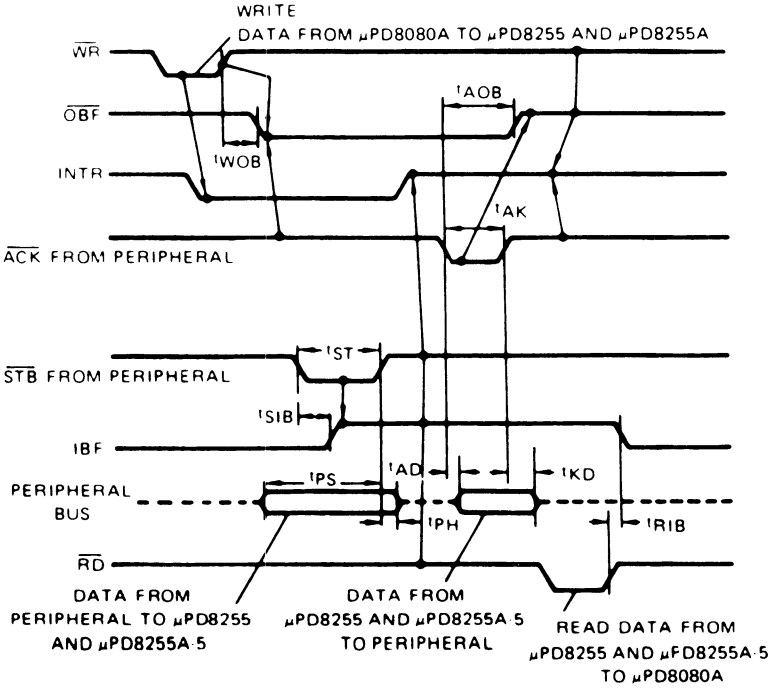
BASIC OUTPUT – μPD8255A-5

TIMING WAVEFORMS (CONT.)

MODE 1



MODE 2



Note: ① Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

② When the μPD8255A-5 is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

μPD8255/8255A-5

MODES

The μPD8255 and μPD8255A-5 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

  16 different configurations in MODE 0

  Two 8-bit ports and two 4-bit ports

  Inputs are not latched

  Outputs are latched

MODE 1

MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C

Two I/O Groups (I and II)

Both groups contain an 8-bit data port and a 4-bit control/data port

Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.

An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})

Both inputs and outputs are latched

An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

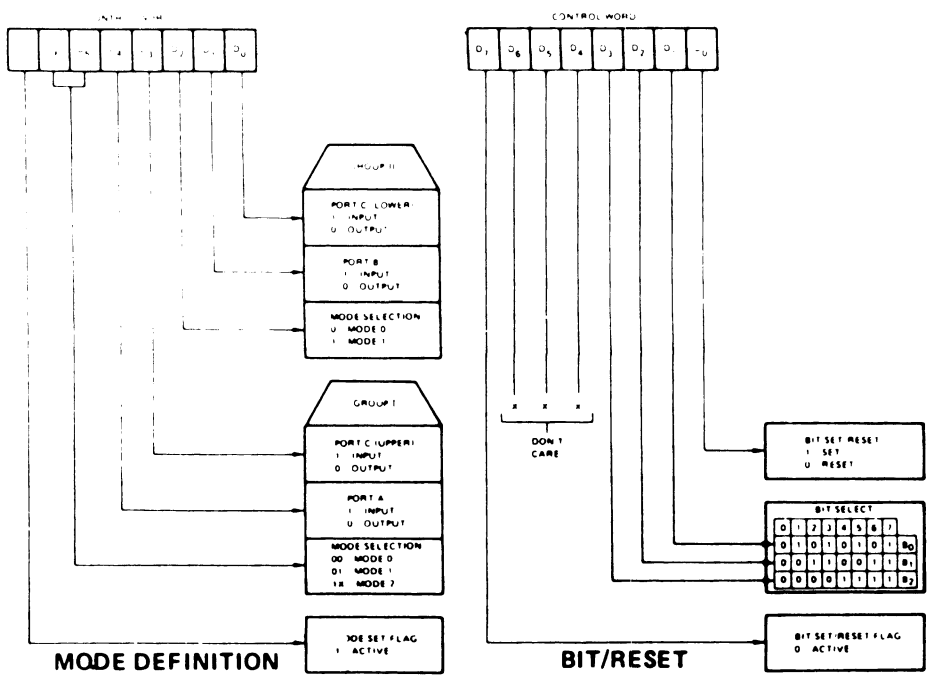
OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

NOTES ① X means "DO NOT CARE"

② All conditions not listed are illegal and should be avoided

FORMATS

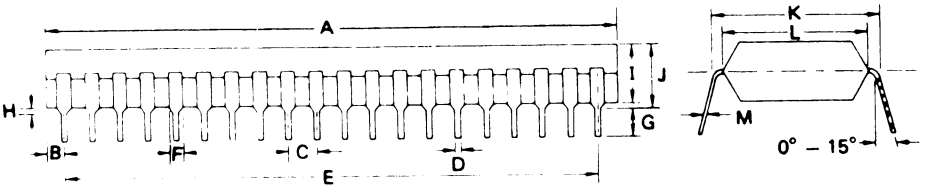


MODE DEFINITION

BIT/RESET

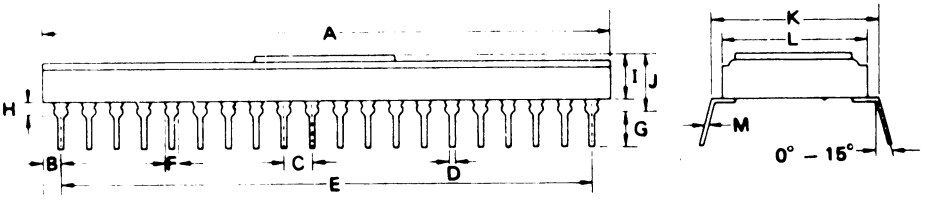
PACKAGE OUTLINE
μPD8255C/D
μPD8255AC/D-5

Members of the μPD8085 Family are housed in both plastic and ceramic 40 pin packages. The drawings and tables below apply to all five of the NEC Microcomputer parts covered in this data sheet.



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

MULTI-PROTOCOL SERIAL CONTROLLER

DESCRIPTION

The μPD7201 is a dual-channel multi-function peripheral controller designed to satisfy a wide variety of serial data communication requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller and within that role it is configurable by systems software so its "personality" can be optimized for a given serial data communications application.

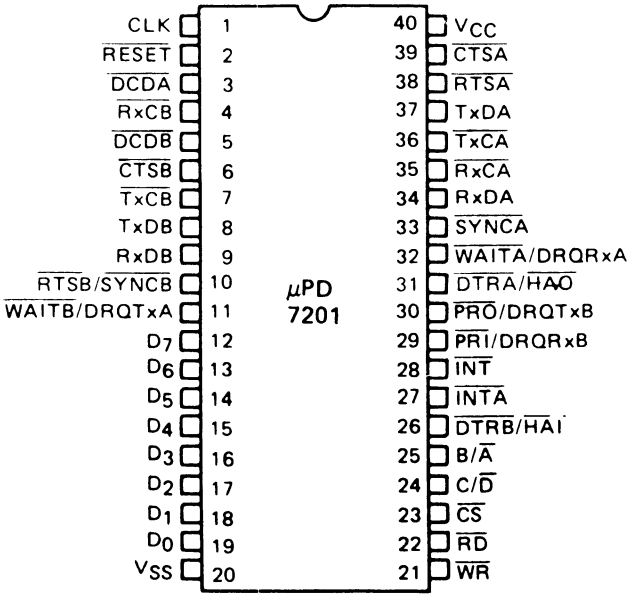
The μPD7201 is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for applications other than data communications.

The μPD7201 can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

FEATURES

- Two Fully Independent Duplex Serial Channels
- Four Independent DMA Channels for Send/Received Data for Both Serial Inputs/Outputs
- Programmable Interrupt Vectors and Interrupt Priorities
- Modem Controls Signals
- Variable, Software Programmable Data Rate, Up to 880K Baud at 3 MHz Clock
- Double Buffered Transmitter Data and Quadruply Buffered Received Data
- Programmable CRC Algorithm
- Selection of Interrupt, DMA or Polling Mode of Operation
- Asynchronous Operation:
  - Character Length: 5, 6, 7 or 8 Bits
  - Stop Bits: 1, 1-1/2, 2
  - Transmission Speed: x1, x16, x32 or x64 Clock Frequency
  - Parity: Odd, Even, or Disable
  - Break Generation and Detection
  - Interrupt on Parity, Overrun, or Framing Errors
- Monosync, Bisync, and External Sync Operations:
  - Software Selectable Sync Characters
  - Automatic Sync Insertion
  - CRC Generation and Checking
- HDLC and SDLC Operations:
  - Abort Sequence Generation and Detection
  - Automatic Zero Insertion and Detection
  - Address Field Recognition
  - CRC Generation and Checking
  - I-Field Residue Handling
- N-Channel MOS Technology
- Single +5V Power Supply; Interface to Most Microprocessors Including 8080, 8085, 8086 and Others.
- Single Phase TTL Clock
- Available in Plastic and Ceramic Dual-in-Line Packages

PIN CONFIGURATION



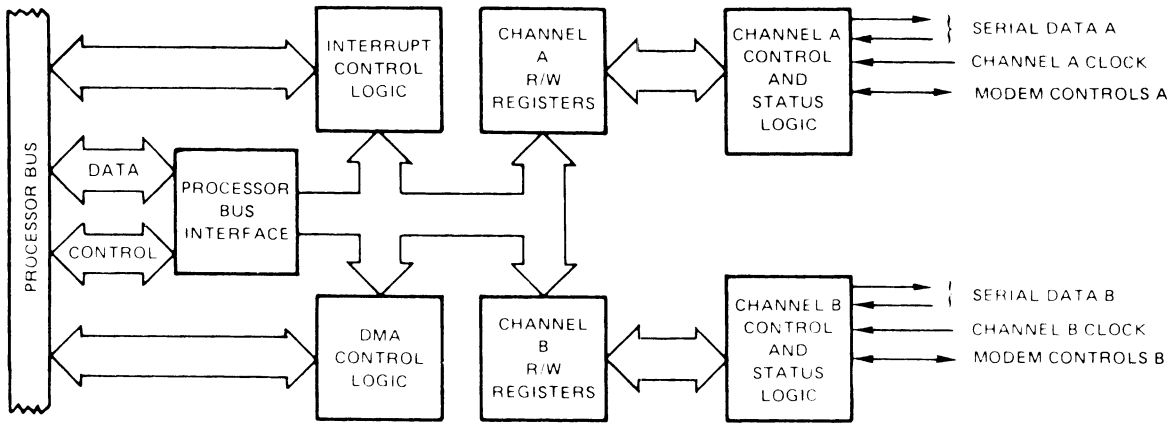
PIN DESCRIPTION

NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
12-19	D_0 D_7	System Data Bus (bidirectional, 3-state)	The system data bus transfers data and commands between the processor and the μPD7201. D_0 is the least significant bit.
25	B/$\overline{A}$	Channel A or B Select (input, High selects Channel B)	This input defines which channel is accessed during a data transfer between the processor and the μPD7201.
24	C/$\overline{D}$	Control or Data Select (input, High selects Control)	This input defines the type of information transfer performed between the processor and the μPD7201. A High at this input during a processor write to or read from the μPD7201 causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A low at C/$\overline{D}$ means that the information on the data bus is data.
23	$\overline{CS}$	Chip Select (input, active Low)	A low level at this input enables the μPD7201 to accept command or data inputs from the processor during a write cycle, or to transmit data to the processor during a read cycle.
1	CLK	System Clock (input)	The μPD7201 uses standard TTL clock.
22	$\overline{RD}$	Read (input active Low)	If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with C/$\overline{D}$, B/$\overline{A}$ and $\overline{CS}$ to transfer data from the μPD7201 to the processor or the memory.
21	$\overline{WR}$	Write (input, active Low)	The $\overline{WR}$ signal is used to control the transfer of either command or data from the processor or the memory to the μPD7201.
2	$\overline{RESET}$	Reset (input, active Low)	A low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls high and disables all interrupts. The control registers must be rewritten after the μPD7201 is reset and before data is transmitted or received. $\overline{RESET}$ must be active for a minimum of one complete CLK cycle.
10,38	$\overline{RTSA}$, $\overline{RTSB}$	Request to Send (outputs, active Low)	When the $\overline{RTS}$ bit is set, the $\overline{RTS}$ output goes Low. When the $\overline{RTS}$ bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the state of the $\overline{RTS}$ bit. Both pins can be used as general-purpose outputs.
10,33	$\overline{SYNCA}$, $\overline{SYNCB}$	Synchronization (inputs/outputs, active Low)	These pins can act either as inputs or outputs. In the Asynchronous Receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven Low on the second rising edge of $\overline{RxC}$ after that rising edge of $\overline{RxC}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced Low, it is wise to keep it Low until the processor informs the external sync logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode. In the Internal Synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.
26,31	$\overline{DTRA}$, $\overline{DTRB}$	Data Terminal Ready (outputs, active Low)	These outputs follow the state programmed into the DTR bit. They can also be programmed as general-purpose outputs.

PIN DESCRIPTION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
27	$\overline{INTA}$	Interrupt Acknowledge (input, active Low)	This signal is generated by the processor and is sent to all peripheral devices. It serves to acknowledge the interrupt and to allow the highest priority interrupting device to put an 8-bit vector on the bus. $\overline{INT}$ and $\overline{INTA}$ are compatible with the fully nested option of the μPD8259A-5.
29	$\overline{PRI}$	Priority In (input, active Low)	These signals are daisy chained through the peripheral device controllers. The signal on these lines is intact until a device with a pending interrupt request is found on the chain. After that device, this signal holds off lower priority device interrupts. A higher priority device can interrupt the processing of an interrupt from a lower priority device, provided the processor has interrupts enabled. $\overline{PRI}$ is used with $\overline{PRO}$ to form a priority daisy chain when there is more than one interrupt-driven device. A Low on this line indicates that no other device of higher priority is being serviced by a processor interrupt service routine. $\overline{PRO}$ is Low only if $\overline{PRI}$ is Low and the processor is not servicing an interrupt from the μPD7201. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its processor interrupt service routine.
30	$\overline{PRO}$	Priority Out (output, active Low)	
11,29, 30,32	DRQTxA, DRQTxB DRQRxA, DRQRxB	DMA Request (outputs, active High)	These signals are generated by the receiver or transmitter of Channel A and Channel B. These signals can be connected to an 8257 DMA Controller and are used for handshaking during DMA transfer.
26	$\overline{HAI}$	DMA Acknowledge (input, active Low)	Typically, the HLDA signal driven from the processor is input to the $\overline{HAI}$ terminal of the highest priority μPD7201, and the $\overline{HAO}$ output of that μPD7201 is daisy chained to the $\overline{HAI}$ input of the lower priority μPD7201 and propagated downstream. $\overline{HAI}$ and $\overline{HAO}$ signals provide acknowledgement for the highest priority outstanding DMA request.
31	$\overline{HAO}$	DMA Acknowledge (output, active Low)	
28	$\overline{INT}$	Interrupt Request (output, open collector, active Low)	When the μPD7201 is requesting an interrupt, it pulls $\overline{INT}$ low.
11,32	$\overline{WAITA}$, $\overline{WAITB}$	(Outputs, open drain)	Wait lines for both channels that synchronize the processor to the μPD7201 data rate. The reset state is open drain.
6,39	$\overline{CTSA}$, $\overline{CTSB}$	Clear to Send (inputs, active Low)	When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime inputs. The μPD7201 detects pulses on these inputs and interrupts the processor on both logic level transitions. The Schmitt-trigger inputs do not guarantee a specified noise-level margin.
3,5	$\overline{DCDA}$, $\overline{DCDB}$	Data Carrier Detect (inputs, active Low)	These signals are similar to the $\overline{CTS}$ inputs, except they can be used as receiver enables.
9,34	RxDA, RxDB	Receive Data (inputs, active High)	
8,37	TxDA, TxDB	Transmit Data (outputs, active High)	
4,35	$\overline{RxCA}$, $\overline{RxCB}$	Receiver Clocks (inputs)	The Receiver Clocks may be 1, 16, 32, or 64 times the data rate in asynchronous modes. Receive data is sampled on the rising edge of $\overline{RxC}$.
7,36	$\overline{TxCA}$, $\overline{TxCB}$	Transmitter Clocks (inputs)	In asynchronous modes, the Transmitter Clocks may be 1, 16, 32, or 64 times the data rate. The multiplier for the transmitter and the receiver must be the same. Both $\overline{TxC}$ and $\overline{RxC}$ inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise margin is specified). TxD changes on the falling edge of $\overline{TxC}$. Note that $\overline{TxC}$ and $\overline{RxC}$ in Channel B are on a common pin, $\overline{RxCB}/\overline{TxCB}$.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature . . . . . 0° to +70° C
Storage Temperature . . . . . −65° to +125° C
Voltage on Any Pin . . . . . −0.5 to +7 Volts ①

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5	+0.8	V	
Input High Voltage	V_{IH}	+2.0	V_{CC}+0.5	V	
Output Low Voltage	V_{OL}		+0.45	V	I_{OL} = +2.0 mA
Output High Voltage	V_{OH}	+2.4		V	I_{OH} = −200 μA
Input Leakage Current	I_{IL}		±10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{OL}		±10	μA	V_{OUT} = V_{CC} to 0V
V_{CC} Supply Current	I_{CC}		180	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

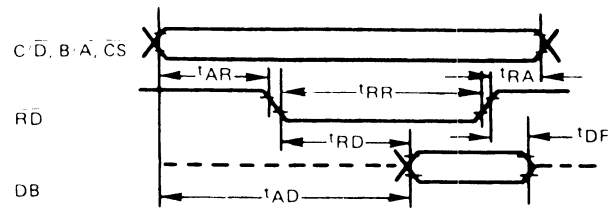
PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		10	pF	fc = 1 MHz
Output Capacitance	C_{OUT}		15	pF	Unmeasured pins Returned to GND
Input/Output Capacitance	$C_{I/O}$		20	pF	

AC CHARACTERISTICS T_a = 0°C to +70°C; V_{CC} = +5V ±10%

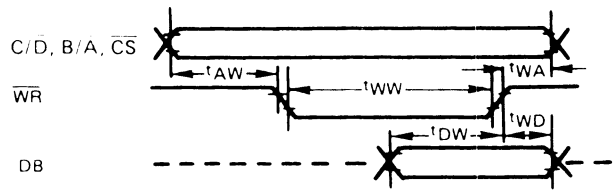
PARAMETER	SYMBOL	LIMITS		UNIT
		MIN	MAX	
Clock Cycle	t_{CY}	250	4000	ns
Clock High Width	t_{CH}	105	2000	ns
Clock Low Width	t_{CL}	105	2000	ns
Clock Rise and Fall Time	t_r, t_f	0	30	ns
Address Setup to $\overline{RD}$	t_{AR}	0		ns
Address Hold from $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ Pulse Width	t_{RR}	250		ns
Data Delay from Address	t_{AD}		200	ns
Data Delay from $\overline{RD}$	t_{RD}		200	ns
Output Float Delay	t_{DF}	10	100	ns
Address Setup to $\overline{WR}$	t_{AW}	0		ns
Address Hold from $\overline{WR}$	t_{WA}	0		ns
$\overline{WR}$ Pulse Width	t_{WW}	250		ns
Data Setup to $\overline{WR}$	t_{DW}		150	ns
Data Hold from $\overline{WR}$	t_{WD}	0		ns
$\overline{PRO}$ Delay from $\overline{INTA}$	t_{IAPO}		200	ns
$\overline{PRI}$ Setup to $\overline{INTA}$	t_{PIN}	0		ns
$\overline{PRI}$ Hold from $\overline{INTA}$	t_{IP}	0		ns
$\overline{INTA}$ Pulse Width	t_{II}	250		ns
$\overline{PRO}$ Delay from $\overline{PRI}$	t_{PIPO}		100	ns
Data Delay from $\overline{INTA}$	t_{ID}		200	ns
Request Hold from $\overline{RD}$/$\overline{WR}$	t_{CO}		150	ns
$\overline{HAI}$ Setup to $\overline{RD}$/$\overline{WR}$	t_{LR}	300		ns
$\overline{HAI}$ Hold from $\overline{RD}$/$\overline{WR}$	t_{RL}	0		ns
$\overline{HAO}$ Delay from $\overline{HAI}$	t_{HIHO}		100	ns
Recovery Time Between Controls	t_{RV}	300		ns
$\overline{WAIT}$ Delay from Address	t_{CW}		120	ns
Data Clock Cycle	t_{DCY}	400		ns
Data Clock Low Width	t_{DCL}	180		ns
Data Clock High Width	t_{DCH}	180		ns
Tx Data Delay	t_{TD}		300	ns
Data Set up to $\overline{RxC}$	t_{DS}	0		ns
Data Hold from $\overline{RxC}$	t_{DH}	140		ns
$\overline{INT}$ Delay Time from $\overline{TxC}$	t_{ITD}		4 ~ 6	t_{CY}
$\overline{INT}$ Delay Time from $\overline{RxC}$	t_{IRD}		7 ~ 11	t_{CY}
Low Pulse Width	t_{PL}	200		ns
High Pulse Width	t_{PH}	200		ns
External $\overline{INT}$ from $\overline{CST}$, $\overline{DCD}$, $\overline{SYNC}$	t_{IPD}		500	ns
Delay from $\overline{RxC}$ to $\overline{SYNC}$	t_{DRxC}		100	ns

TIMING WAVEFORMS

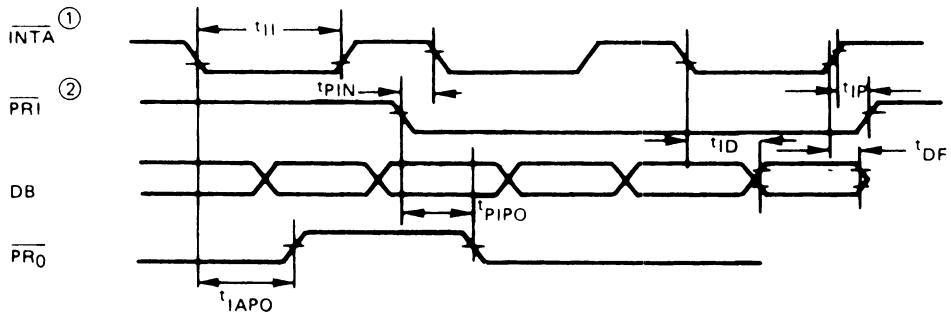
READ CYCLE



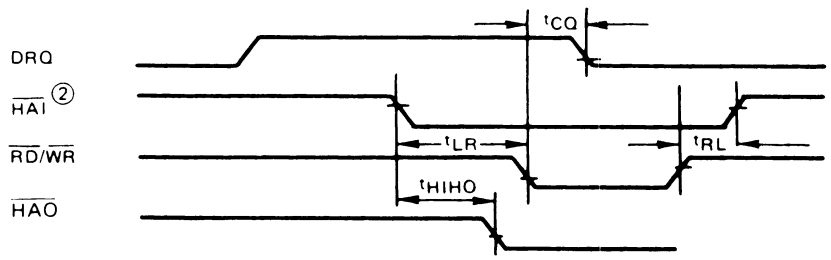
WRITE CYCLE



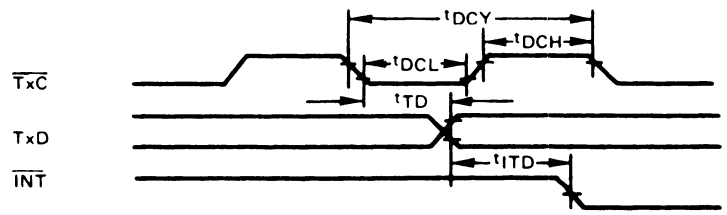
INTA CYCLE



DMA CYCLE



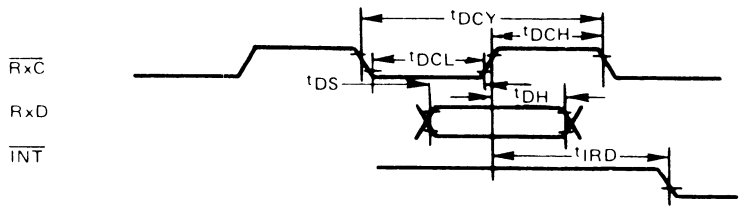
TRANSMIT DATA CYCLE



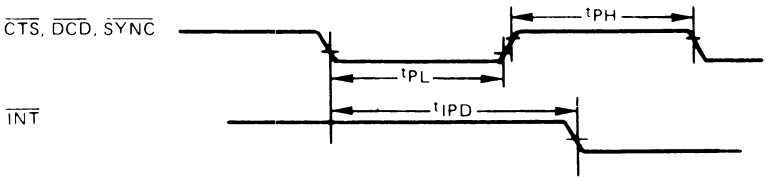
Notes: ① INTA signal acts as RD signal.
② PRI and HAI signals act as CS signal.

TIMING WAVEFORMS (CONT.)

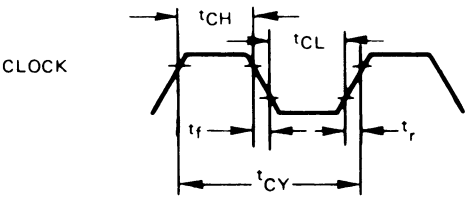
RECEIVE DATA CYCLE



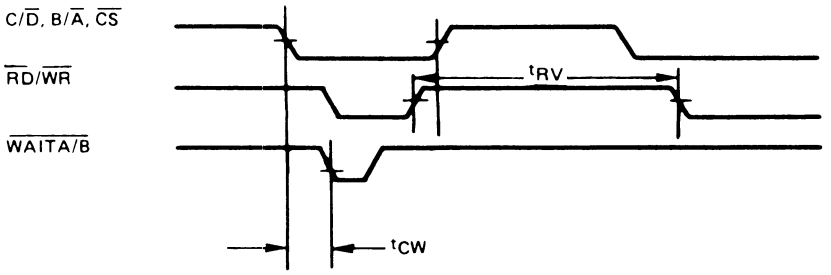
OTHER TIMING



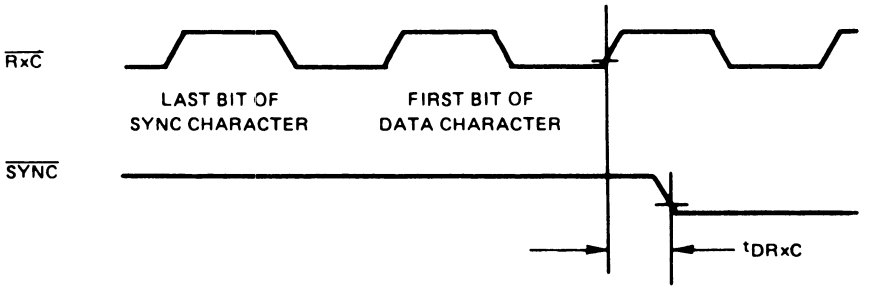
CLOCK



READ/WRITE CYCLE (SOFTWARE BLOCK TRANSFER MODE)

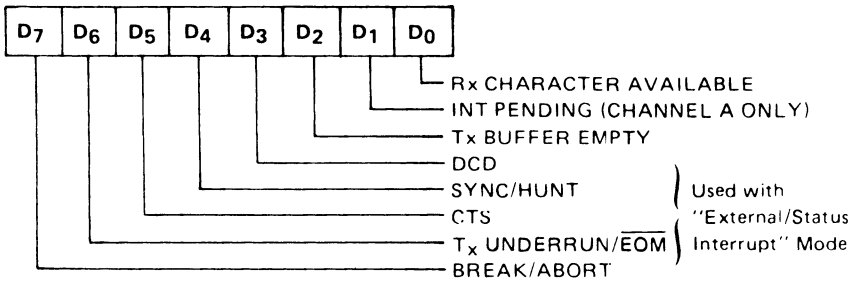


SYNC PULSE GENERATION (EXTERNAL SYNC MODE)

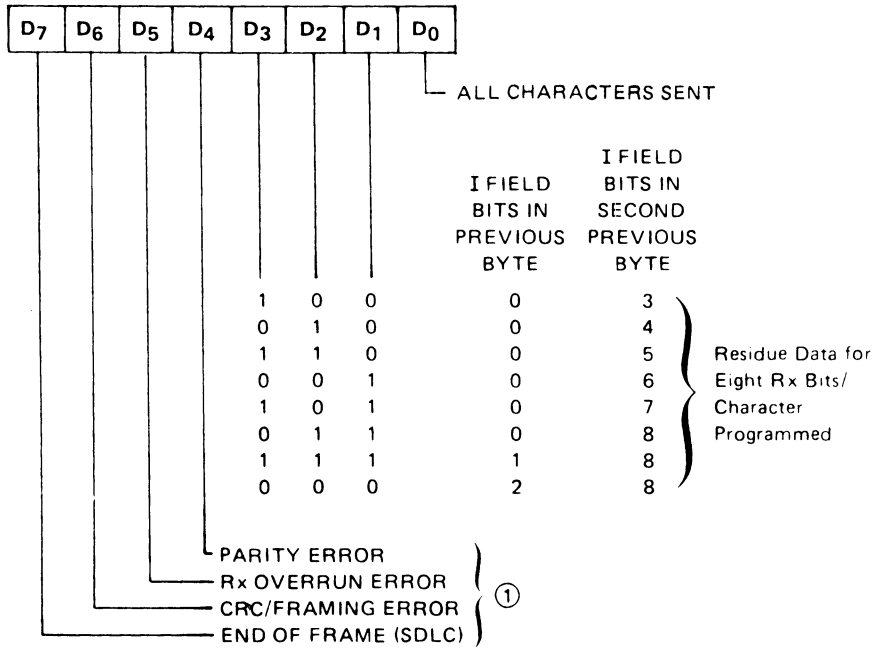


READ REGISTER BIT FUNCTIONS

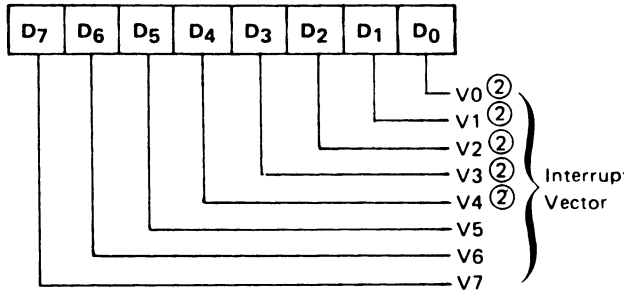
READ REGISTER 0



READ REGISTER 1 ①



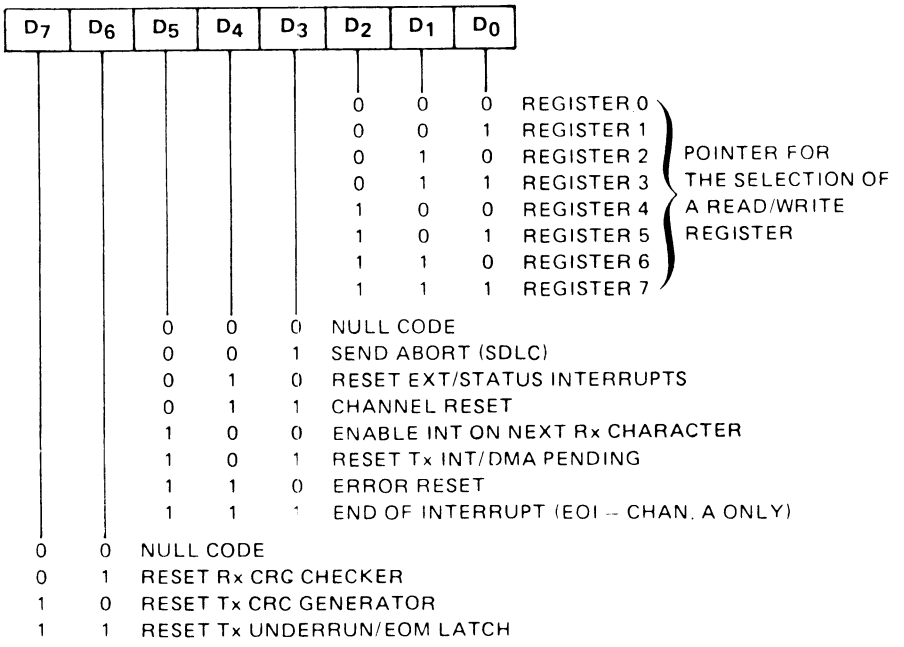
READ REGISTER 2



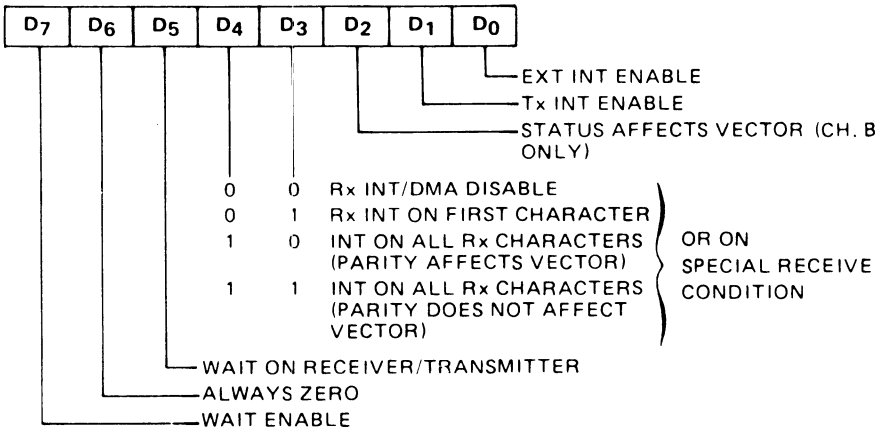
Notes: ① Used with Special Receive Condition Mode.
② Variable if "Status Affects Vector" is programmed.

WRITE REGISTER BIT FUNCTIONS

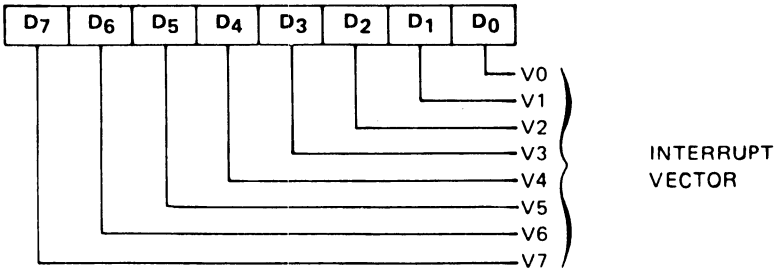
WRITE REGISTER 0



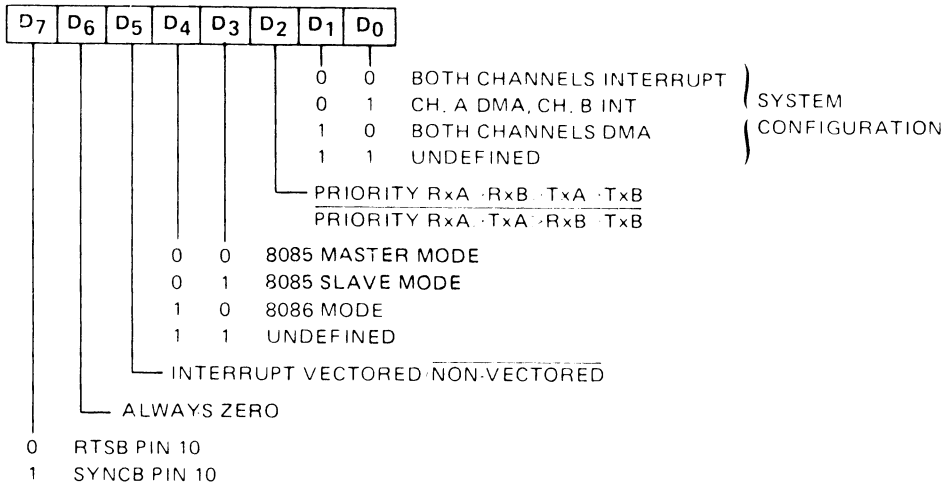
WRITE REGISTER 1



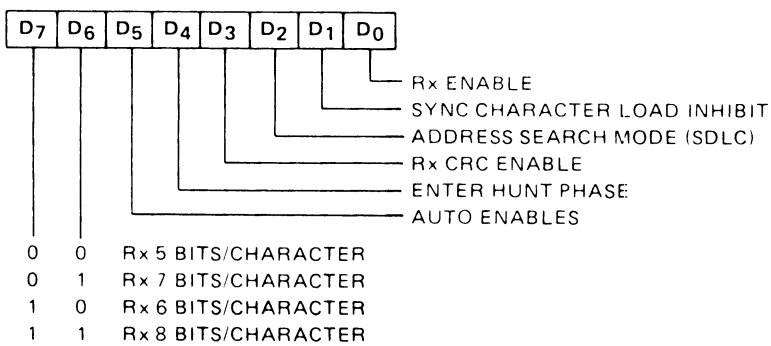
WRITE REGISTER 2 (CHANNEL B)



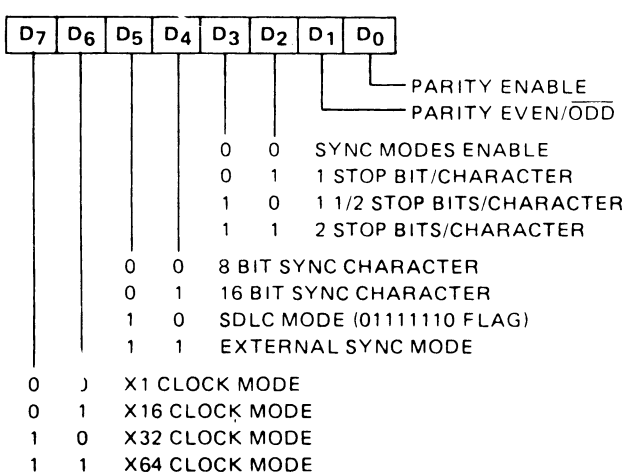
WRITE REGISTER 2 (CHANNEL A)



WRITE REGISTER 3

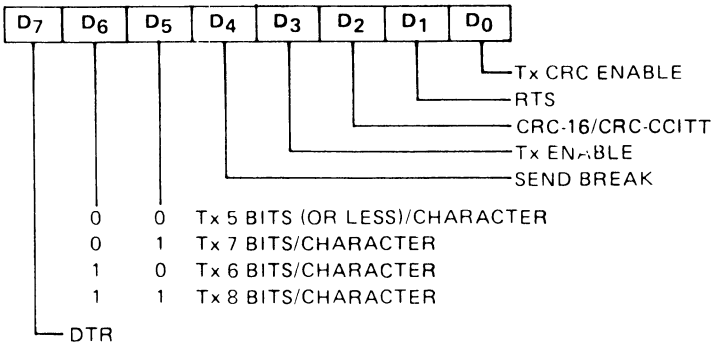


WRITE REGISTER 4

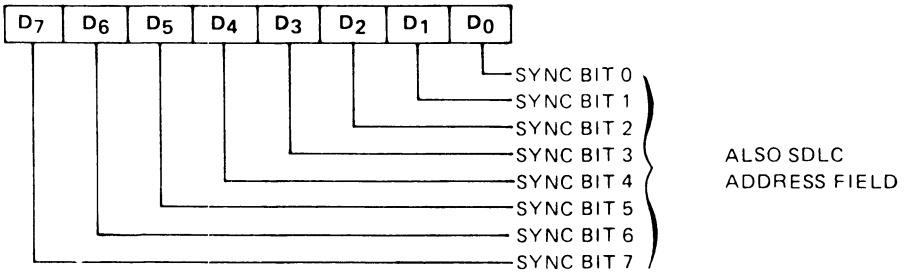


WRITE REGISTER BIT FUNCTIONS (CONT.)

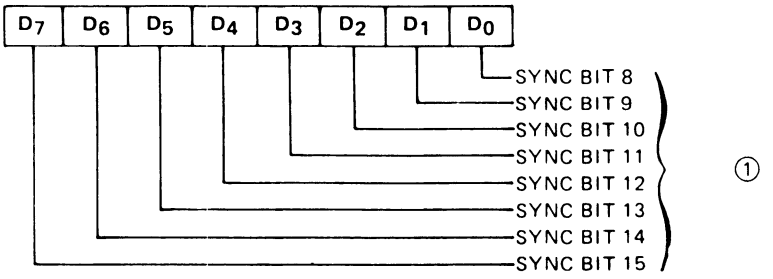
WRITE REGISTER 5



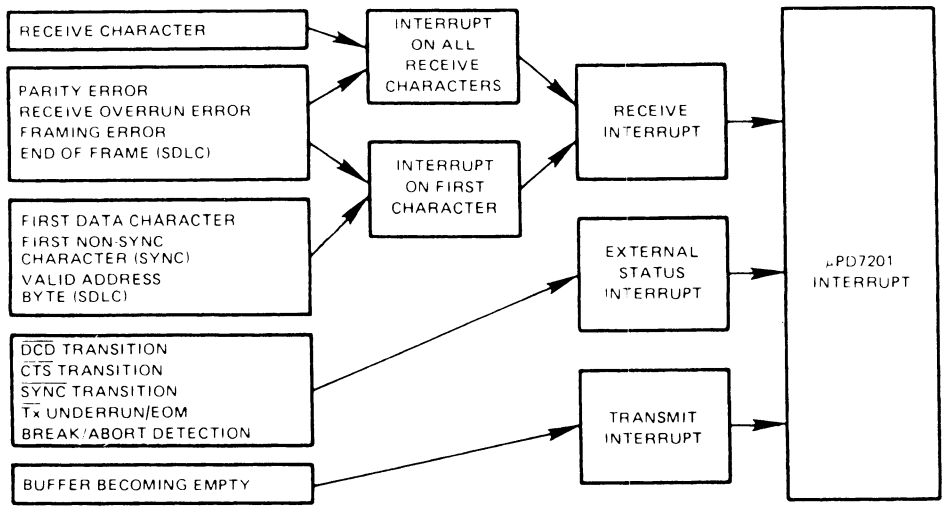
WRITE REGISTER 6



WRITE REGISTER 7



Note: ① For SDLC it must be programmed to "01111110" for flag recognition.



INTERRUPT STRUCTURE

WR2s BITS IN CH. A			PRIN	MODE	CONTENTS ON DATA BUS DRIVEN BY THE μPD7201 AT EACH INTA SEQUENCE																			
					1st $\overline{INTA}$								2nd $\overline{INTA}$								3rd $\overline{INTA}$ (*)							
D_5	D_4	D_3			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	x	x	x	Non-vectored	High-Z								High-Z								High-Z							
1	0	0	0	8085 Master	(Call) 1	1	0	0	1	1	0	1	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	0	0	0	0	0	0	0	0
1	0	0	1	8085 Master	1	1	0	0	1	1	0	1	High-Z								High-Z							
1	0	1	0	8085 Slave	High-Z								V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	0	0	0	0	0	0	0	0
1	0	1	1	8085 Slave	High-Z								High-Z								High-Z							
1	1	0	0	8086	High-Z								V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0								
1	1	0	1	8086	High-Z								High-Z															

(*) 3rd $\overline{INTA}$ is 8085 Mode

NEC Microcomputers, Inc.

NEC

μPD416
μPD416-1
μPD416-2
μPD416-3
μPD416-5

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

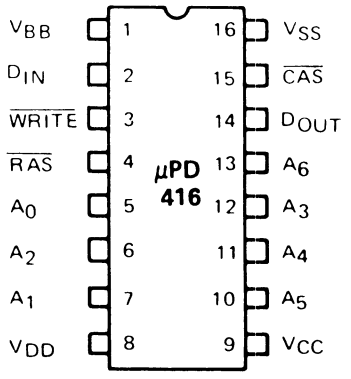
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, -5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 20 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 5 Performance Ranges:

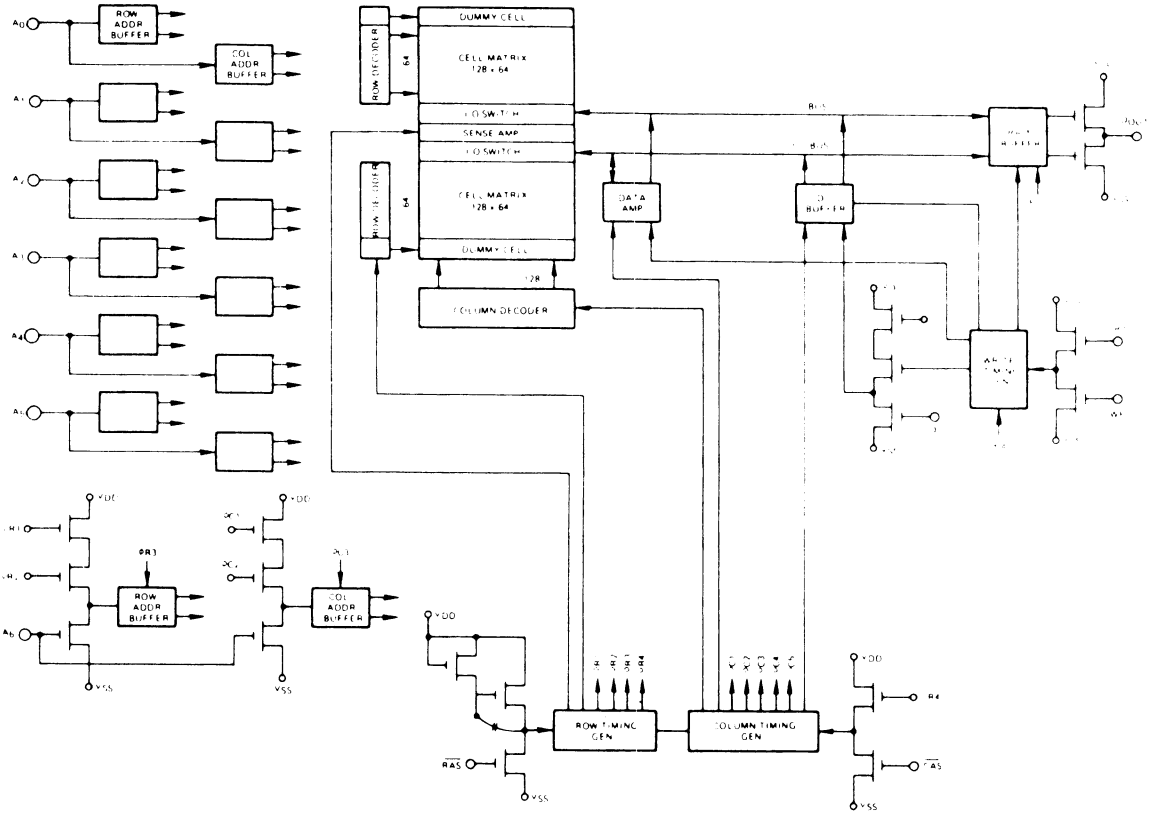
	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	575 ns
μPD416-1	250 ns	410 ns	465 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	375 ns	375 ns
μPD416-5	120 ns	320 ns	320 ns

PIN CONFIGURATION



A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

DC CHARACTERISTICS

T_a = 0°C to +70°C (1), V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	(2)
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	(2) (3)
Supply Voltage	V_{SS}	0	0	0	V	(2)
Supply Voltage	V_{BB}	-4.5	-5.0	-5.5	V	(2)
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	(2)
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	(2)
Input Low (Logic 0) Voltage, all inputs	V_{IL}	1.0		0.8	V	(2)
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} Min. (4)
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{DD} Current — All Speeds except μPD416-5	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns (4)
Refresh V_{DD} Current — μPD416-5	I_{DD3}			27	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns (4)
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = 225 ns (4)
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = 375 ns (5)
Standby V_{CC} Current	I_{CC2}	10		10	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = 225 ns (5)
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	-10		10	μA	V_{BB} = -5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	-10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = -5 mA (3)
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: (1) T_a is specified here for operation at frequencies to t_{RC} = t_{RC} (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

(2) All voltages referenced to V_{SS}.

(3) Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

(4) I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

(5) I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

DERATING CURVES

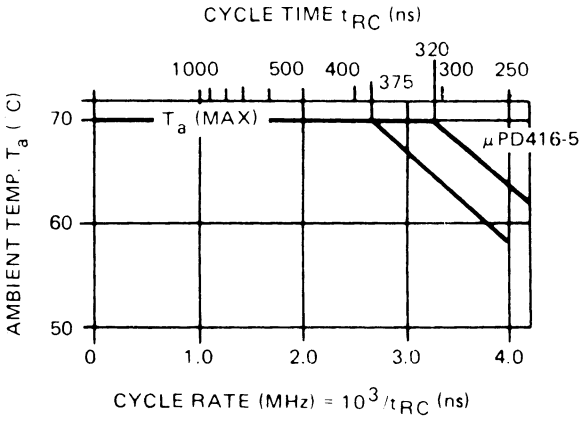


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375 ns) is determined by T_a (max) [°C] = 70 − 9.0 x (cycle rate [MHz] −2.66). For μPD416-5, it is T_a (max) [°C] = 70 − 9.0 (cycle rate [MHz] − 3.125).

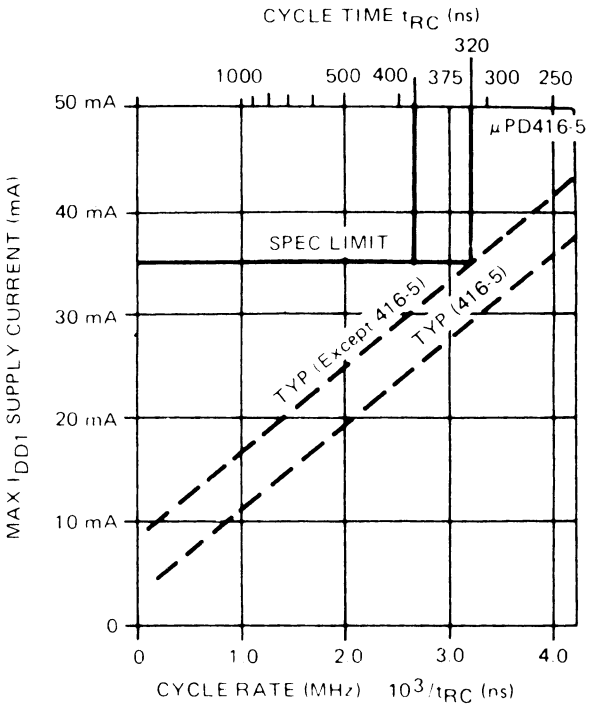


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

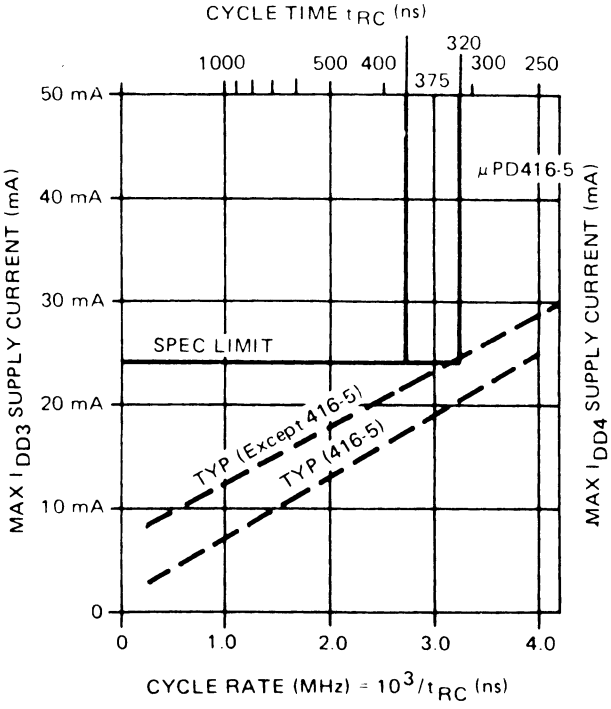


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

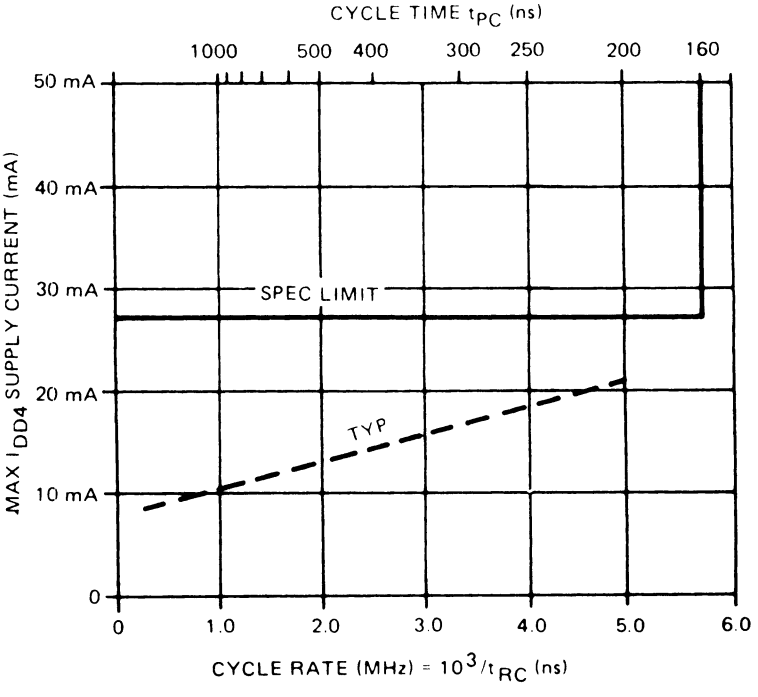


FIGURE 4

Maximum I_{DD4} versus cycle rate for device operation in page mode.

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		μPD416		μPD416-1		μPD416-2		μPD416-3		μPD416-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	510		410		375		375		320		ns	③
Read write cycle time	t_{RWC}	575		465		375		375		320		ns	③
Page mode cycle time	t_{PC}	330		275		225		170		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150		120	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		165		135		100		80	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	60	0	50	0	40	0	35	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		150		120		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	10,000	250	10,000	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		165		135		100		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	165	10,000	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	20		20		20		20		0		ns	
Row address set up time	t_{ASR}	0		0		0		0		0		ns	
Row address hold time	t_{RAH}	40		35		25		20		15		ns	
Column address set up time	t_{ASC}	10		10		10		10		10		ns	
Column address hold time	t_{CAH}	90		75		55		45		40		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		80		ns	
Read command set-up time	t_{RCS}	0		0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		80		ns	
Write command pulse width	t_{WP}	90		75		55		45		40		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		100		80		60		60		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		100		80		60		60		ns	
Data-in set-up time	t_{DS}	0		0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		40		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		80		ns	
CAS precharge time (for page-mode cycle only)	t_{CP}	120		100		80		60		60		ns	
Refresh period	t_{REF}		2		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	20		20		20		20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	140		125		95		70		80		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	240		200		160		120		120		ns	⑩

Notes:

① AC measurements assume t_T = 5 ns.

② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑥ Measured with a load equivalent to 2 TTL loads and 100 pF.

⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

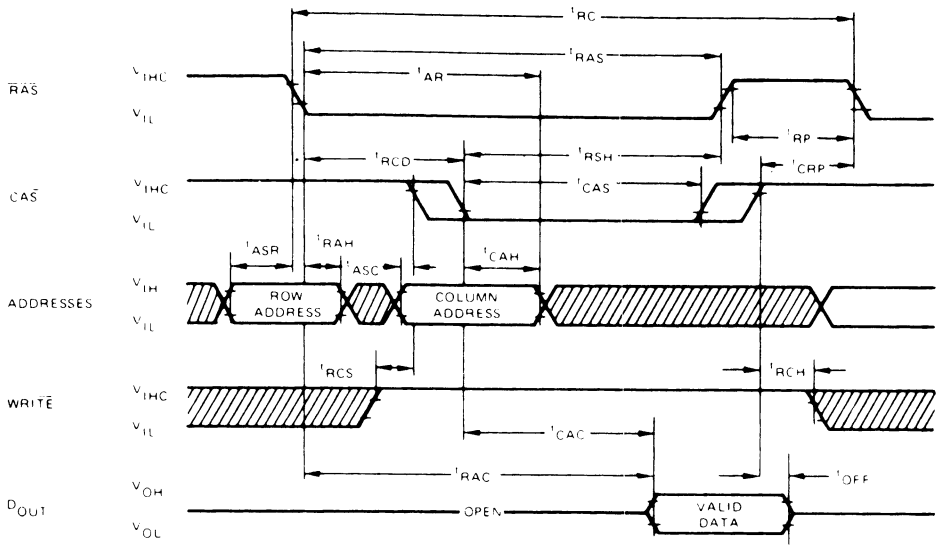
⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

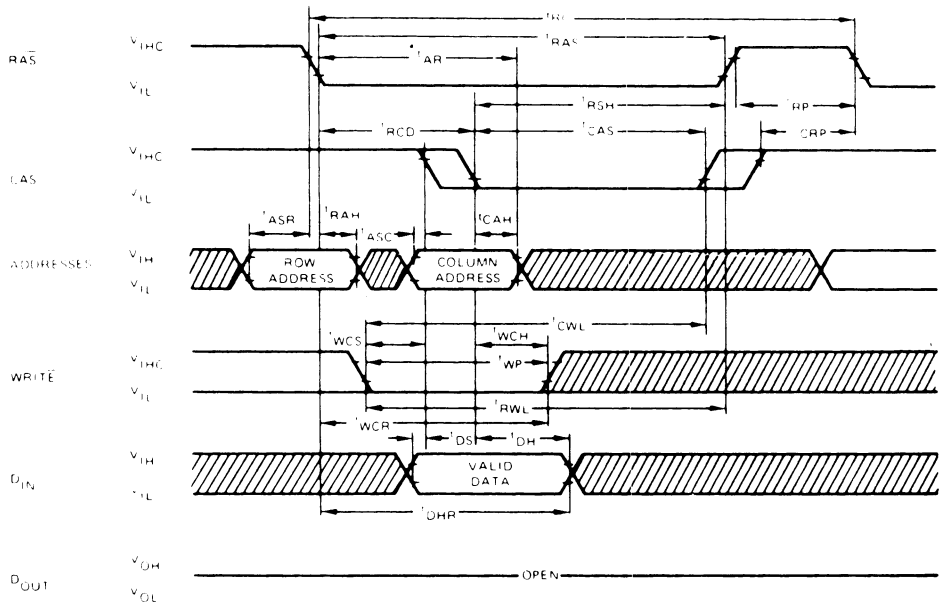
⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) ≥ t_{RWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

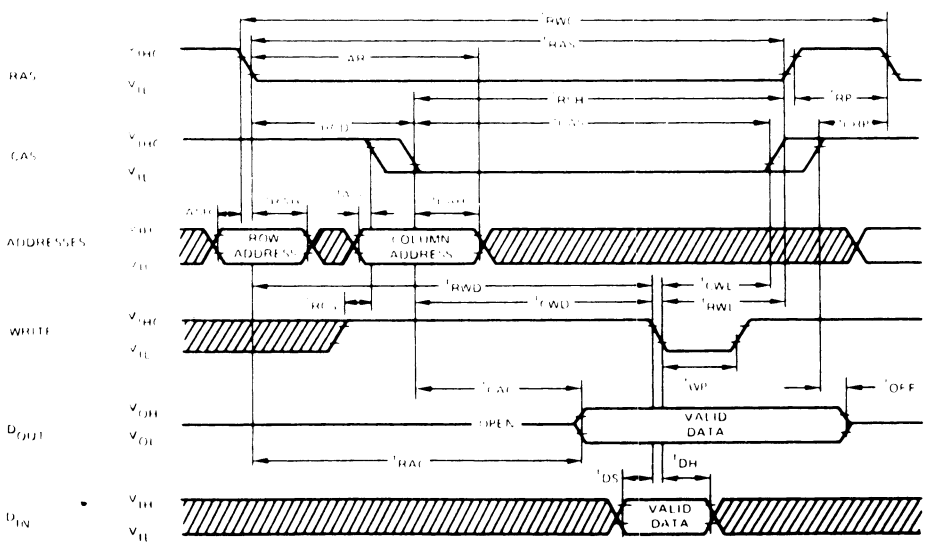
READ CYCLE



WRITE CYCLE

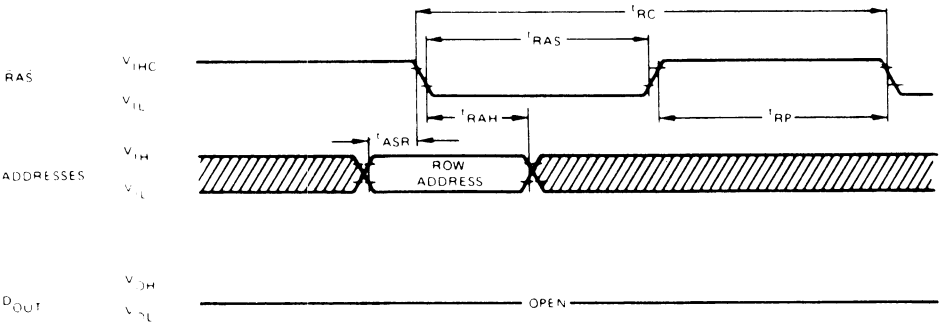


READ-WRITE/READ-MODIFY-WRITE CYCLE



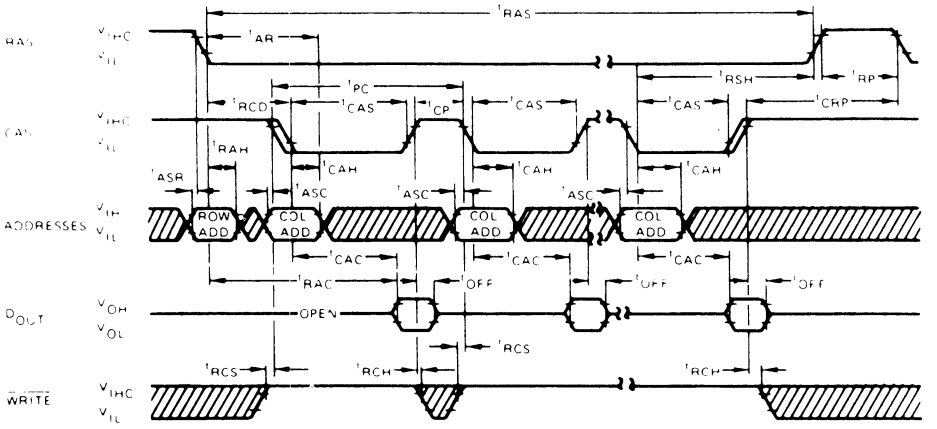
TIMING WAVEFORMS (CONT.)

"$\overline{RAS}$-ONLY" REFRESH CYCLE

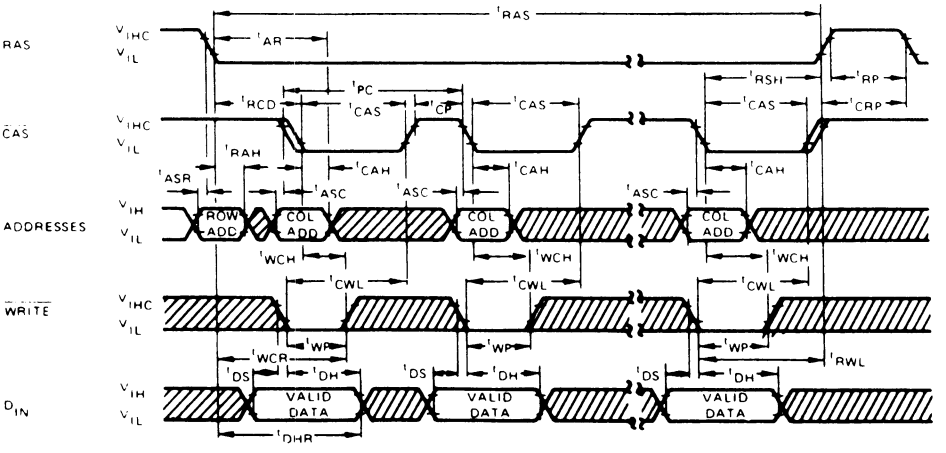


Note: CAS = V_{IHC}, $\overline{WRITE}$ = Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only"-cycles can be used for simple refreshing operation.

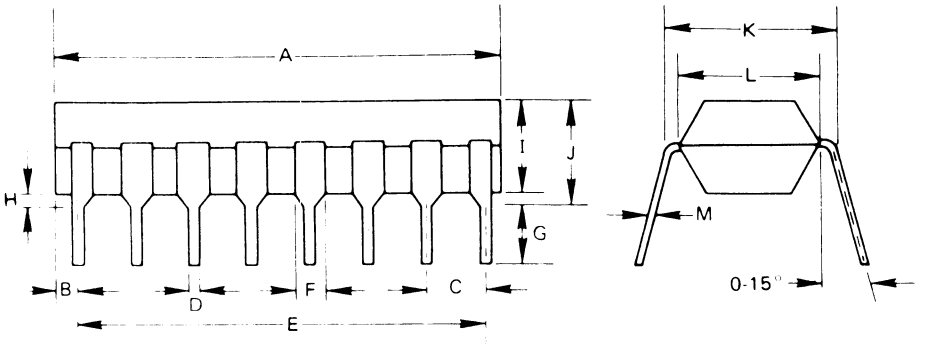
CHIP SELECTION

Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

POWER SEQUENCING

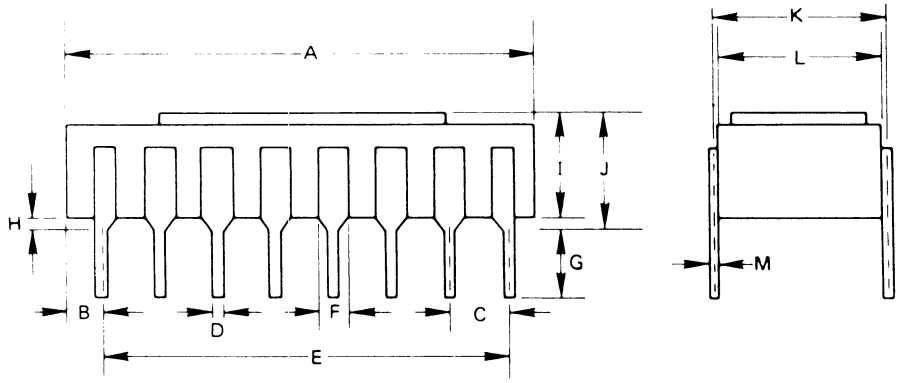
In order to assure long term reliability, V_{BB} should be applied first during power up and removed last during power down.

PACKAGE OUTLINE
μPD416C/D



μPD416C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



μPD416D
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

NEC

NEC Microcomputers

A Division of NEC Electronics U.S.A. Inc.

μPD7220/GDC GRAPHICS DISPLAY CONTROLLER PRELIMINARY

Description

The μPD7220 Graphics Display Controller (GDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the GDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the GDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the GDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the GDC is ideal for advanced computer graphics applications.

Features

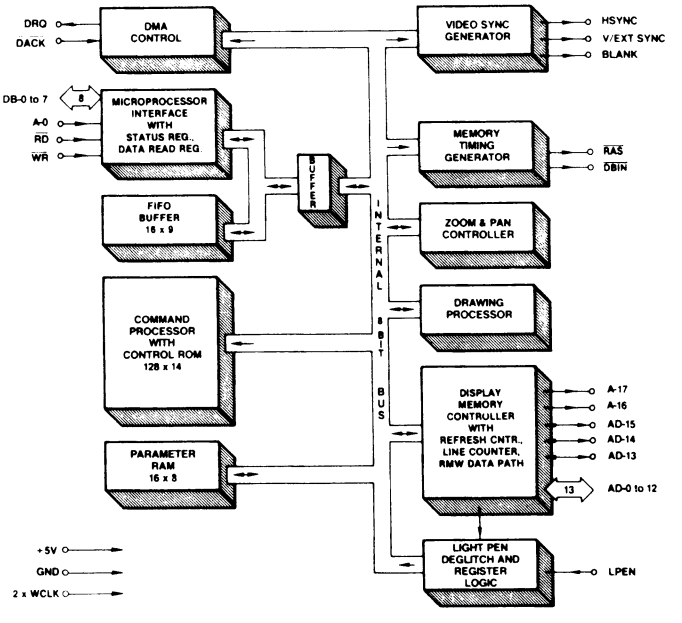
- ☐ Microprocessor Interface
  - DMA transfers with 8257 or 8237-type controllers
  - FIFO Command Buffering
- ☐ Display Memory Interface
  - Up to 256K words of 16 bits
  - Read-Modify-Write (RMW) Display Memory cycles in under 800ns
  - Dynamic RAM refresh cycles for non-accessed memory
- ☐ Light Pen Input
- ☐ External video synchronization mode
- ☐ Graphics Mode:
  - Four megabit, bit-mapped display memory
- ☐ Character Mode:
  - 8K character code and attributes display memory
- ☐ Mixed Graphics and Characters Mode
  - 64K if all characters
  - 1 megapixel if all graphics
- ☐ Graphics Capabilities:
  - Figure drawing of lines, arc/circles, rectangles, and graphics character in 800ns per pixel
  - Display 1024 by 1024 pixels with 4 planes of color or grayscale
  - Two independently scrollable areas
- ☐ Character Capabilities:
  - Auto cursor advance
  - Four independently scrollable areas
  - Programmable cursor height
  - Characters per row: up to 256
  - Character rows per screen: up to 100
- ☐ Video Display Format
  - Zoom magnification factors of 1 to 16
  - Panning
  - Command-settable video raster parameters
- ☐ Technology
  - Single +5 volt, NMOS, 40-pin DIP
- ☐ DMA Capability:
  - Bytes or word transfers
  - 4 clock periods per byte transferred

System Considerations

The GDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the GDC's design, each of the system components is used to the maximum extent through six-level hierarchy of simultaneous tasks. At the lowest level, the GDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the GDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the GDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the GDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

GDC Components

The GDC block diagram illustrates how these tasks are accomplished.



Microprocessor Bus Interface

Control of the GDC by the system microprocessor is achieved through an 8-bit bi-directional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal GDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

Command Processor

The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destina-

tions within the GDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

DMA Control

The DMA control circuitry in the GDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a μPD8257 or μPD8237 DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

Parameter RAM

The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

Video Sync Generator

Based on the clock input, the sync logic generates the raster timing signals for almost any interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple GDCs.

Memory Timing Generator

The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the GDC's RAS and DBIN outputs.

Zoom & Pan Controller

Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independent of the other display areas.

Drawing Processor

The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing processor needs no further assistance to complete the figure drawing.

Display Memory Controller

The display memory controller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMs. The memory controller apportions the video field time between the various types of cycles.

Light Pen Deglitcher

Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address.

Programmer's View of GDC

The GDC occupies two addresses on the system microprocessor bus through which the GDC's status register and FIFO are accessed. Commands and parameters are written into the GDC's FIFO and are differentiated based on address bit A0. The status register or the FIFO can be read as selected by the address line.

A0	READ	WRITE
0	STATUS REGISTER	PARAMETER INTO FIFO
1	FIFO READ	COMMAND INTO FIFO

GDC Microprocessor Bus Interface Registers

Commands to the GDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacts the parameters, loads them into the appropriate registers within the GDC, and initiates the required operations.

The commands available in the GDC can be organized into five categories as described in the following section.

GDC Command Summary

Video Control Commands

1. RESET: Resets the GDC to its idle state and specifies the video display format.
2. VSYNC: Selects master or slave video synchronization mode.
3. CCHAR: Specifies the cursor and character row heights.

Display Control Commands

1. START: Starts the display scanning process.
2. ZOOM: Specifies zoom factors for the display and graphics characters writing.
3. CURS: Sets the position of the cursor in display memory.
4. PRAM: Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
5. PITCH: Specifies the width of the X dimension of display memory.

Drawing Control Commands

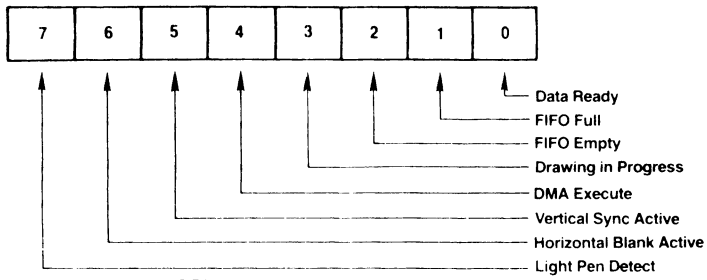
1. WDAT: Writes data words or bytes into display memory.
2. MASK: Sets the mask register contents.
3. FIGS: Specifies the parameters for the drawing processor.
4. FIGD: Draws the figure as specified above.
5. GCHRD: Draws the graphics character into display memory.

Data Read Commands

1. RDAT: Reads data words or bytes from display memory.
2. CURD: Reads the cursor position.
3. LPRD: Reads the light pen address.

DMA Control Commands

1. DMAR: Requests a DMA read transfer.
2. DMAW: Requests a DMA write transfer.



Status Register (SR)

Status Register Flags

SR-7: Light Pen Detect

When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

SR-6: Horizontal Blanking Active

A 1 value for this flag signifies that horizontal retrace blanking is currently underway.

SR-5: Vertical Sync

Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

SR-4: DMA Execute

This bit is a 1 during DMA data transfers.

SR-3: Drawing in Progress

While the GDC is drawing a graphics figure, this status bit is a 1.

SR-2: FIFO Empty

This bit and the FIFO Full flag coordinate system microprocessor accesses with the GDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the GDC have been processed.

SR-1: FIFO Full

A 1 at this flag indicates a full FIFO in the GDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked before each write into the GDC.

SR-0: Data Ready

When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

FIFO Operation & Command Protocol

The first-in, first-out buffer (FIFO) in the GDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the GDC's command set. The microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the GDC requires the differentiation of the first byte of a command sequence from the succeeding bytes. This first byte contains the operation code and the remaining bytes carry parameters. Writing into the GDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the GDC tests this bit as it interprets the entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the GDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the GDC always put the FIFO into write mode if it wasn't in it already. If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require a GDC response, such as RDAT CURD and LPRD, put the FIFO into read mode after the command is interpreted by the GDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

Read-Modify-Write Cycle

Data transfers between the GDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four clock period timing of the RMW cycle is used to: 1) output the address, 2) read data from the memory, 3) modify the data, and 4) write the modified data back into the initially selected memory address. This type of memory cycle is used for all interactions with display memory including DMA transfers, except for the two clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the GDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic Unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT command or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic Unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic Unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with 1s in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a four-bit dAD field to specify the dot address. The command processor converts this parameter into the one-of-16 format used in the Mask register for figure drawing. A full 16 bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

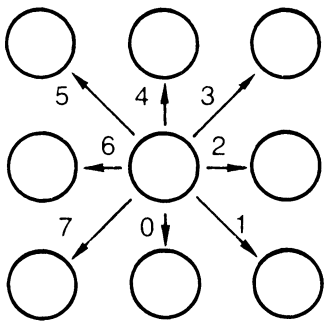
The Logic Unit combines the data read from display memory, the Pattern Register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the modify data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

Figure Drawing

The GDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 5MHZ, this is equal to 800ns. During the RMW cycle the GDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the GDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the GDC's internal RMW logic.

During the drawing process, the GDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The GDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counterclockwise.



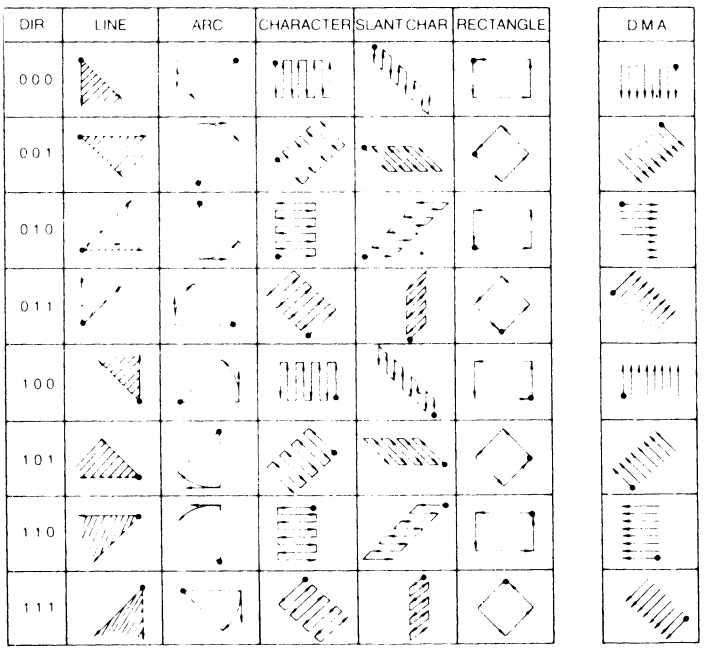
Drawing Directions

Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer register to the right or left. The table below summarizes these operations for each direction.

Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to effect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

DIR	OPERATIONS TO ADDRESS THE NEXT PIXEL
000	EAD ± P → EAD
001	EAD ± P → EAD dAD (MSB) 1 EAD ± 1 → EAD dAD → LR
010	dAD (MSB) 1 EAD ± 1 → EAD dAD → LR
011	EAD ± P → EAD dAD (MSB) 1 EAD ± 1 → EAD dAD → LR
100	EAD ± P → EAD
101	EAD ± P → EAD dAD (LSB) 1 EAD ± 1 → EAD dAD → RR
110	dAD (LSB) 1 EAD ± 1 → EAD dAD → RR
111	EAD ± P → EAD dAD (LSB) 1 EAD ± 1 → EAD dAD → RR

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:



Drawing Parameters

In preparation for graphics figure drawing, the GDC's Drawing Processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the GDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The GDC Drawing Processor coordinates the RMW circuitry and address registers to draw the specified figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specific details about the figure to be drawn are reduced by the microprocessor to a form conducive to high-speed address calculations within the GDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

	DC	D	D2	D1	DM
Initial Value	0	8	8	−1	−1
Line	ΔX	2|ΔY|−|ΔX|	2|ΔY|−2|ΔX|	2|ΔY|	-
Circle	r/√2*	r-1	2(r-1)	−1	0
Arc	r/√2*	r-1	2(r-1)	−1	r sin Θ .
Rectangle	3	A*	B*	−1	A*
Character	7	-	-	-	-
Area Fill	B**	A**	-	-	-
DMA	L	I	-	-	-
R/W DAT	W	-	-	-	-

Graphics Figure Drawing Parameters

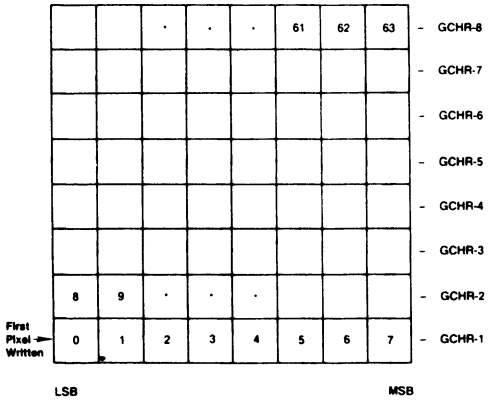
WHERE:

- ΔX = # of pixel positions in the line horizontally.
- ΔY = # of pixel positions in the line vertically.
- r = Radius of the curve, in pixels.
- ↑ = Rounded up to the next higher integer.
- Θ = The angle subtended from the octant axis to the arc.
- A* = The length − 1, in pixels, in the direction initially specified.
- B* = The length − 1, in pixels, in the direction at right angles to the initial direction.
- A** = # of pixels in the initial direction.
- B** = # of pixels in the right angle direction − 1.
- L = # of word address in the perpendicular direction for DMA.
- I = # of DMA transfers in the initially specified direction.
- W = # of word addresses to be written into.
- DC = Drawing Count.
- DM = Dots Masked Count.

Graphics Character Drawing

Graphics characters can be drawn into display memory pixel-by-pixel. The 8-by-8 character is loaded into the GDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

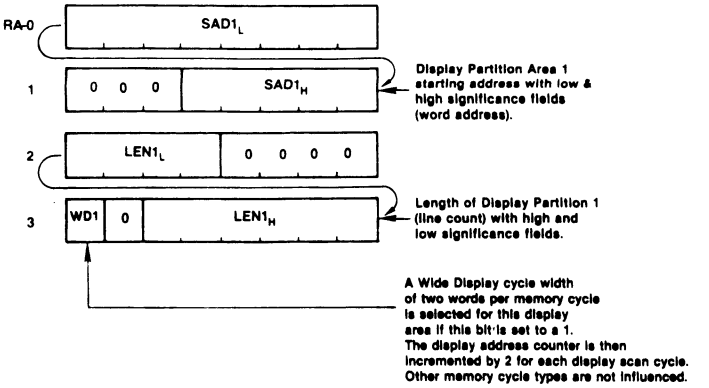
Once the parameter RAM has been loaded with the eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the eight bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the zoom command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor. As seen in display memory, the writing is started in the lower left corner of the eventual 8-by-8 block and proceeds right to left and bottom to top. The LSBs of the stored character bytes are written first, and parameter RAM location 15 is the first byte to go out.

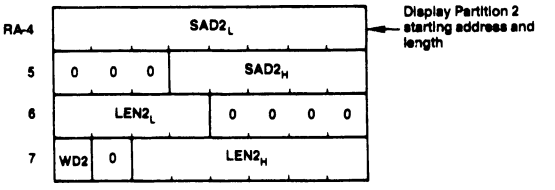


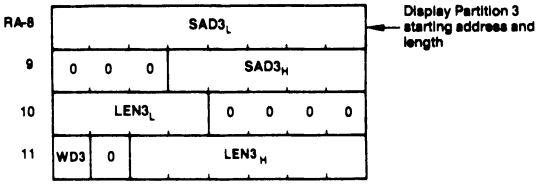
Display Memory

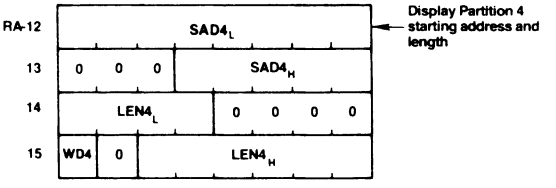
Parameter Ram Contents

Character Mode: RAM Address RA 0 to 16

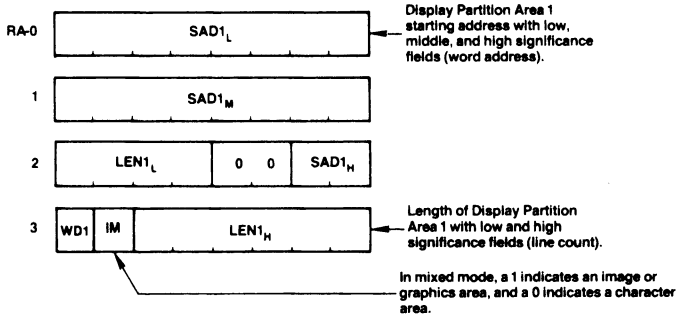


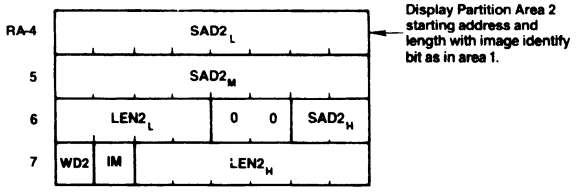


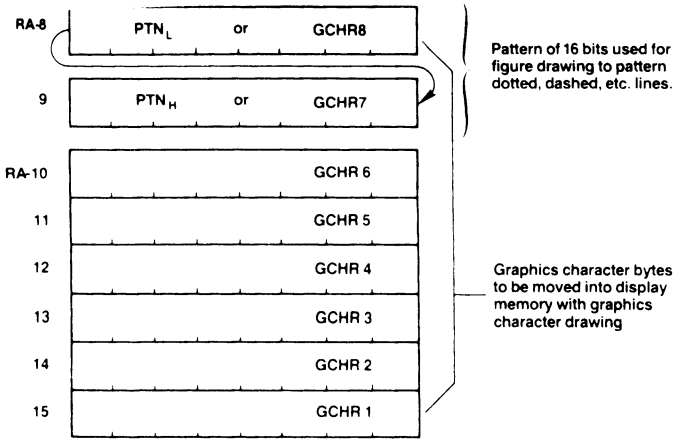




Graphics and Mixed Graphics and Characters Mode







Command Bytes Summary

RESET:	0	0	0	0	0	0	0	0
VSYNC:	0	1	1	0	1	1	1	M
CCHAR:	0	1	0	0	1	0	1	1
START:	0	1	1	0	1	0	1	1
ZOOM:	0	1	0	0	0	1	1	0
CURS:	0	1	0	0	1	0	0	1
PRAM:	0	1	1	1	SA			
PITCH:	0	1	0	0	0	1	1	1
WDAT:	0	0	1	TYPE		0	MOD	
MASK:	0	1	0	0	1	0	1	0
FIGS:	0	1	0	0	1	1	0	0
FIGD:	0	1	1	0	1	1	0	0
GCHRD:	0	1	1	0	1	0	0	0
RDAT:	1	0	1	TYPE		0	0	0
CURD:	1	1	1	0	0	0	0	0
LPRD:	1	1	0	0	0	0	0	0
DMAR:	1	0	1	TYPE		1	0	0
DMAW:	0	0	1	TYPE		1	MOD	

Video Control Commands

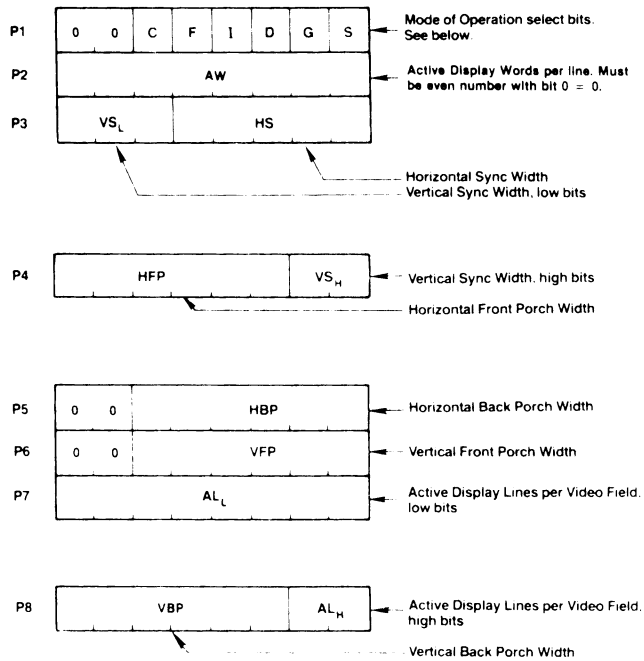
Reset

RESET:	0	0	0	0	0	0	0	0

Blank the display, enter idle mode, and initialize within the GDC:
- FIFO
- Command Processor
- Internal Counters

This command can be executed at any time and does not modify any of the parameters already loaded into the GDC.

If followed by parameter bytes, this command also sets the sync generator parameters as described below.
Idle mode is exited with the START command.



In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any.
The number of active words per line must be an even number from 2 to 256.
An all-zero parameter value selects a count equal to 2^n where n = number of bits in the parameter field.
All horizontal widths are counted in display words.
All vertical widths are counted in lines.

Modes of Operation Bits

C	G	Display Mode
0	0	Mixed Graphics & Character
0	1	Graphics Mode
1	0	Character Mode
1	1	Invalid

I	S	Video Framing
0	0	Non-Interlaced
0	1	Invalid
1	0	Interlaced Repeat Field for Character Displays
1	1	Interlaced

Repeat Field Framing: 2 Field Sequence with ½ line offset between otherwise identical fields.
Interlaced Framing: 2 Field Sequence with ½ line offset. Each field displays alternate lines.
Non-interlaced Framing: 1 field brings all of the information to the screen.

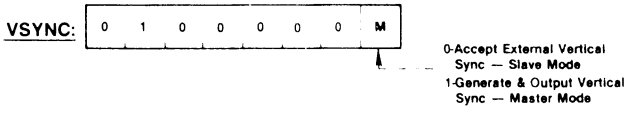
D	Dynamic RAM Refresh Cycles Enable
0	No Refresh — STATIC RAM
1	Refresh — Dynamic RAM

Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

F	Drawing Time Window
0	Drawing during active display time and retrace blanking
1	Drawing only during retrace blanking

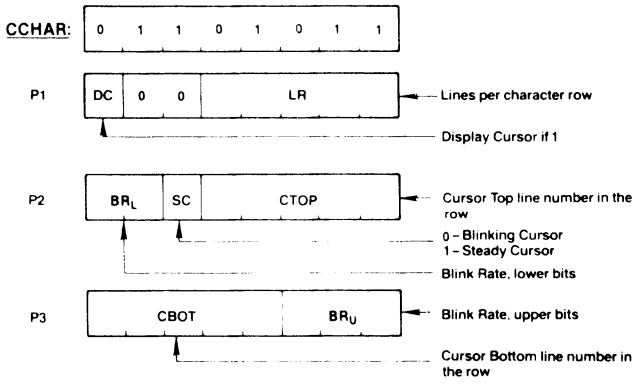
Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.

Vertical Sync Mode



When using two or more GDCs to contribute to one image, one GDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all GDCs are connected together.

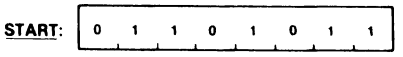
Cursor & Character Characteristics



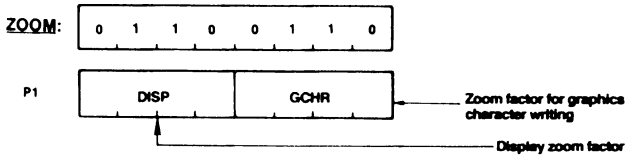
In graphics mode, LR should be set to 1.
The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always ½ the cursor rate but with a ¾ on-¼ off duty cycle.

Display Control Commands

Start Display & End Idle Mode

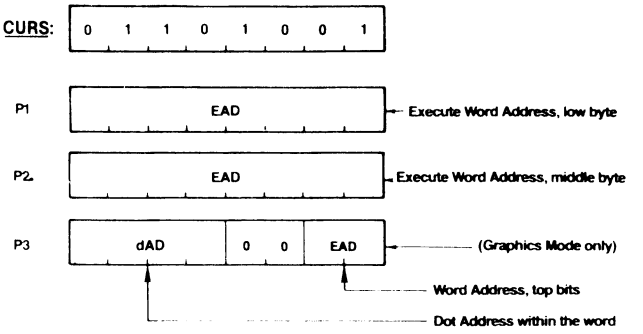


Zoom Factors Specify



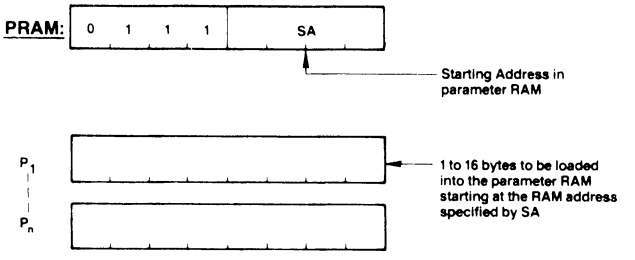
Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.

Cursor Position Specify



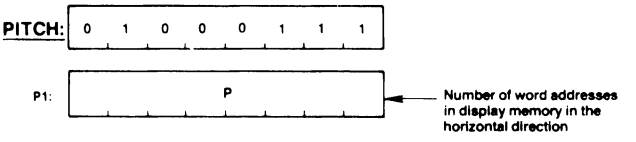
In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address.
In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.

Parameter RAM Load



From the starting address, SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is terminated by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.

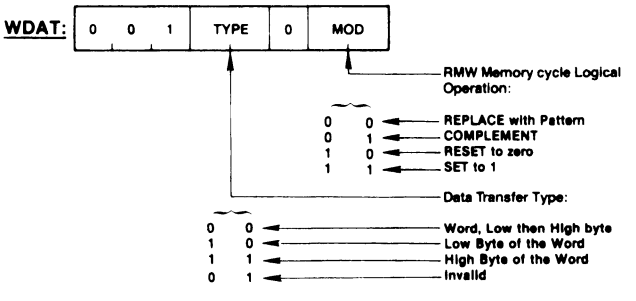
Pitch Specification

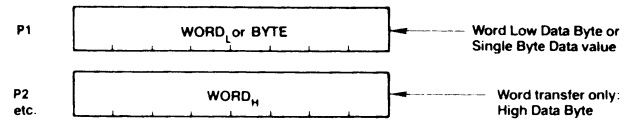


This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

Drawing Control Commands

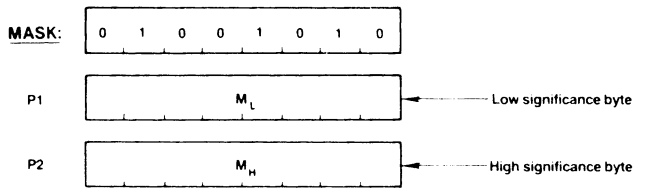
Write Data into Display Memory





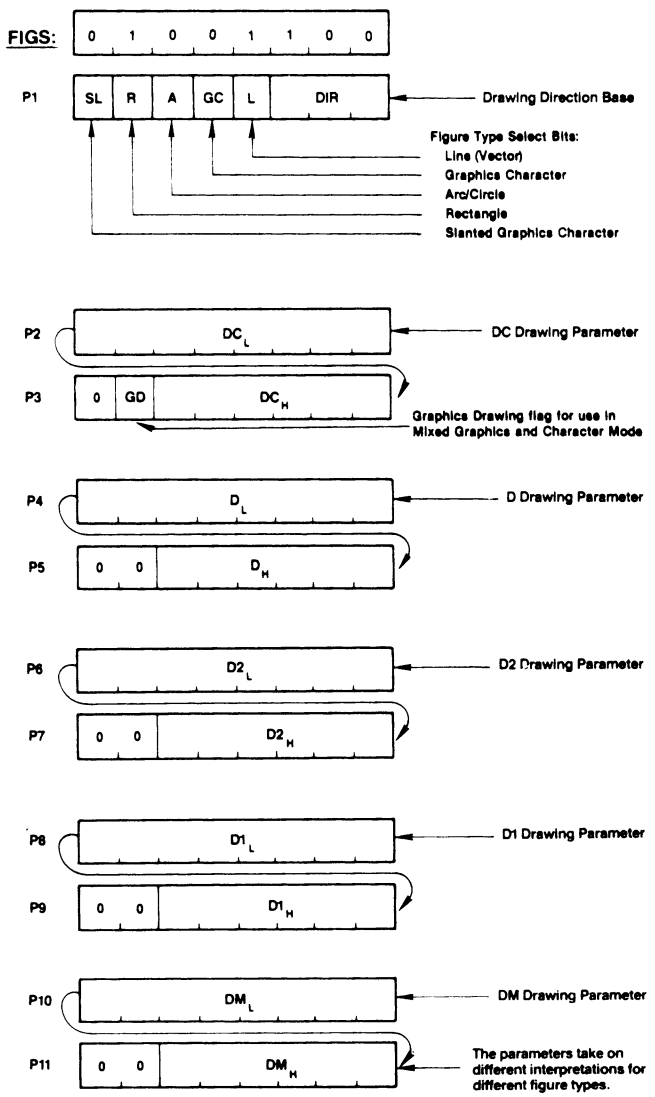
Upon receiving a set of parameters (two bytes for a Word transfer, one for a byte transfer), one RMW cycle into Video Memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.
For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

Mask Register Load



This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

Figure Drawing Parameters Specify



Valid Figure Type Select Combinations

SL	R	A	GC	L	Operation
0	0	0	0	0	Character Display Mode Drawing and Individual Dot Drawing
0	0	0	0	1	Straight Line Drawing
0	0	0	1	0	Graphics Character Drawing and Area filling with graphics character pattern
0	0	1	0	0	Arc and Circle Drawing
0	1	0	0	0	Rectangle Drawing
1	0	0	1	0	Slanted graphics character drawing and slanted area filling

Only these bit combinations assure correct drawing operation.

Figure Draw Start

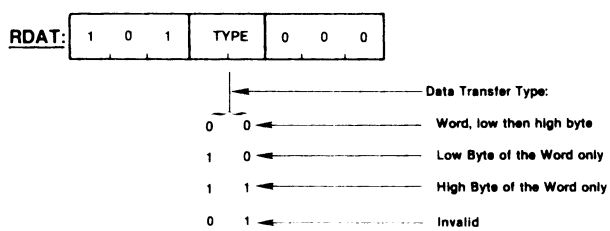
On execution of this instruction, the GDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.

Graphics Character Draw Start

Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in Parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

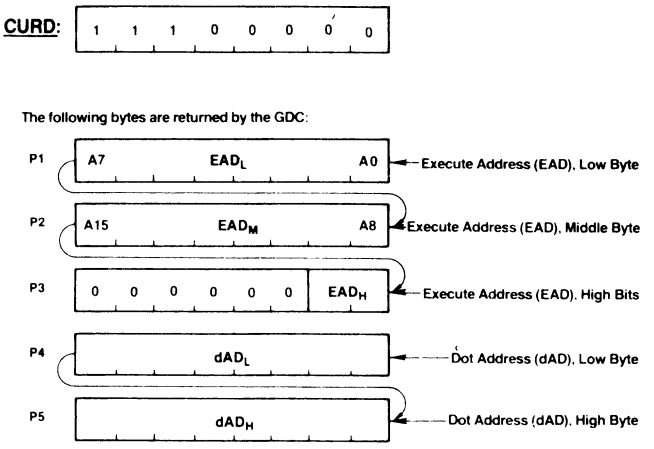
Data Read Commands

Read Data from Display Memory



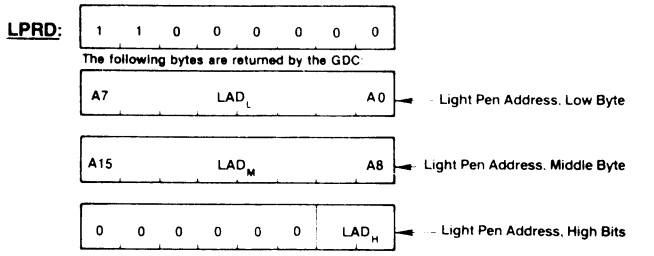
Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes + 1).
As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the GDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost.

Cursor Address Read



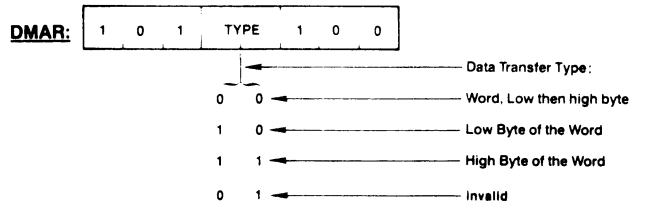
The Execute Address, EAD, points to the display memory word containing the pixel to be addressed.
The Dot Address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

Light Pen Address Read

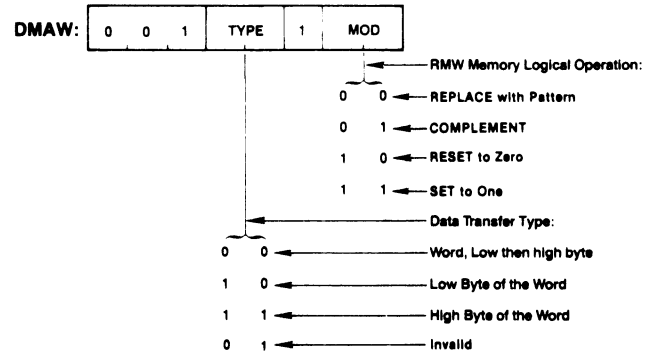


The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.
The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

DMA Read Request



DMA Write Request



Absolute Maximum Ratings* (Tentative)

Ambient Temperature under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on any Pin with respect to Ground	−0.5V to +7V
Power Dissipation	1.5 Watt

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0°C$ to $70°C$; $Vcc = 5V \pm 10\%$

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5	0.8	V	
Input High Voltage	V_{IH}	2.0	Vcc + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −400 uA
Input Low Leak Current	I_{IL}		- 10	uA	V_I = 0V
Input High Leak Current	I_{IH}		+10	uA	V_I = Vcc
Output Low Leak Current	I_{OL}		−10	uA	V_O = 0V
Output High Leak Current	I_{OH}		+10	uA	V_O = Vcc
Clock Input Low Voltage	V_{CL}	−0.5	0.6	V	
Clock Input High Voltage	V_{CH}	3.9	Vcc + 1.0	V	
Vcc Supply Current	I_{CC}		270	mA	

Capacitance

$T_A = 25°C$; $Vcc = GND = OV$

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}		10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$		20	pF	V_I (unmeasured) = 0V

AC Characteristics

TA = 0°C to 70°C; Vcc = 5V ± 10%

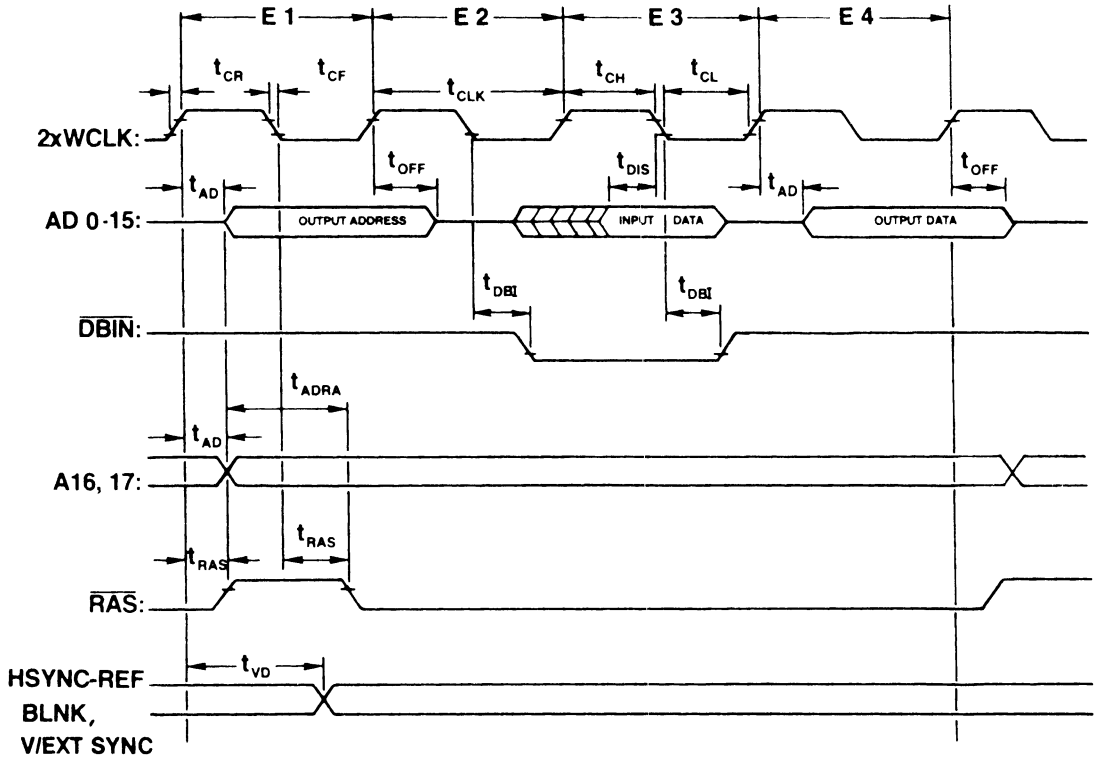
PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Clock Cycle Period	t_{CLK}	167	2000	nS	C_L = 100 pF
Clock High Time	t_{CH}	70		nS	
Clock Low Time	t_{CL}	70		nS	
Clock Rise Time	t_{CR}		10	nS	
Clock Fall Time	t_{CF}		10	nS	
DMA Cycle Time	t_E	$4xt_{CLK}$		nS	
Data In Set Up Time	t_{DIS}	40		nS	
Data Set Up Time for $\overline{WR}$	t_{DW}	150		nS	
Data Hold Time for $\overline{WR}$	t_{WD}	0		nS	
$\overline{DACK}$ High Level Width	t_{DK}	t_{CLK}		nS	

Timing Requirements

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Address Output Delay	t_{AD}	20	80	nS	C_L = 100 pF
Data Bus In Delay	t_{DBI}		80	nS	
Address Active to $\overline{RAS}$ Low	t_{ADRA}	60		nS	
Video Signal Delay	t_{VD}		120	nS	
$\overline{RD}$ Low to DB Delay	t_{RD}		120	nS	
$\overline{RD}$ High to DB Floating	t_{DF}		120	nS	
$\overline{DACK}$ Low to DRD Delay	t_{DR}		120	nS	
$\overline{RAS}$ Output Delay	t_{RAS}		80	nS	
AD Floating Delay	t_{OFF}		80	nS	

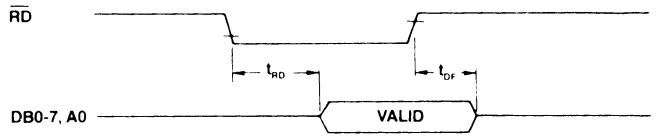
Timing Responses

Display Memory Bus Timing

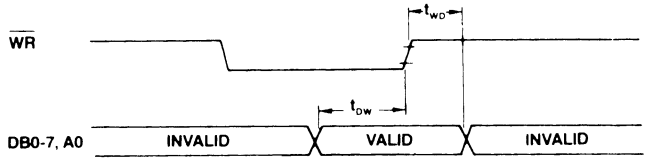


Read Modify-Write Cycle

Microprocessor Bus Timing

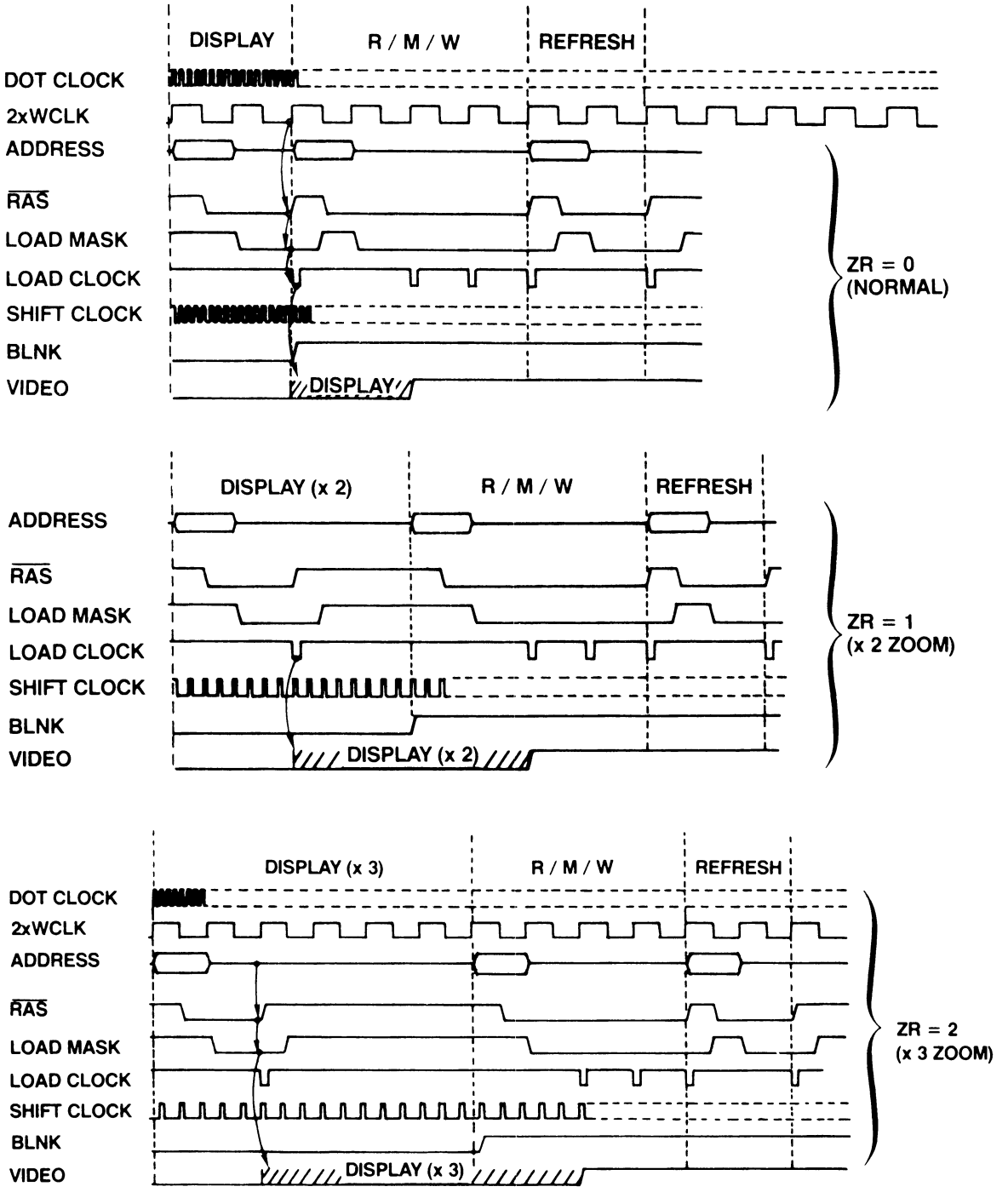


Read Timing

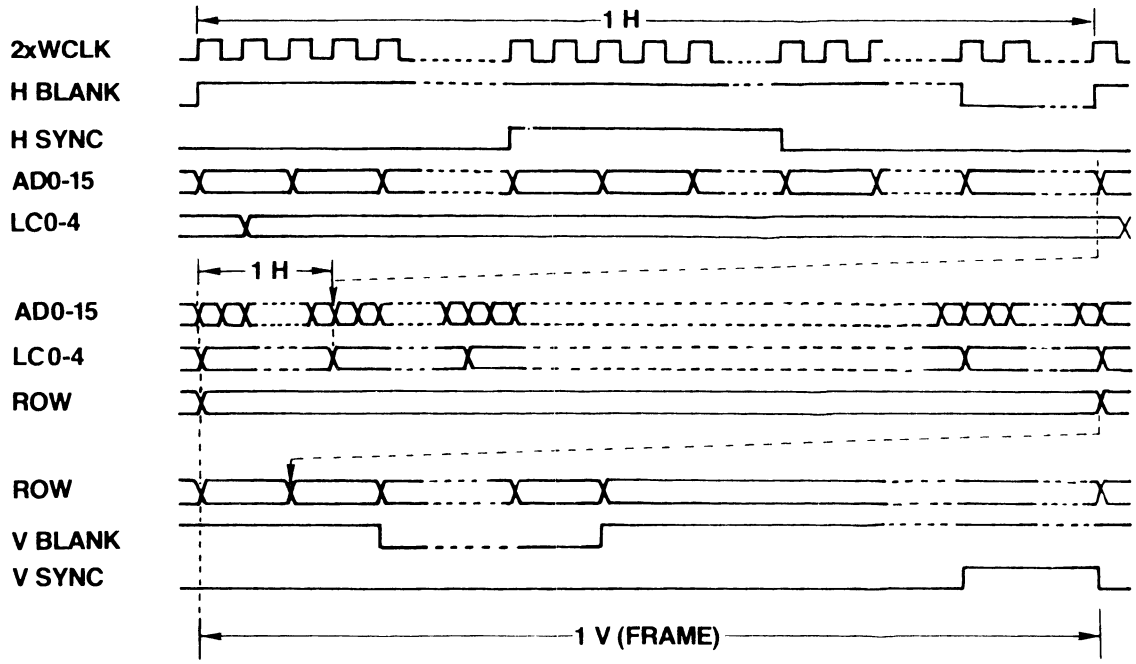


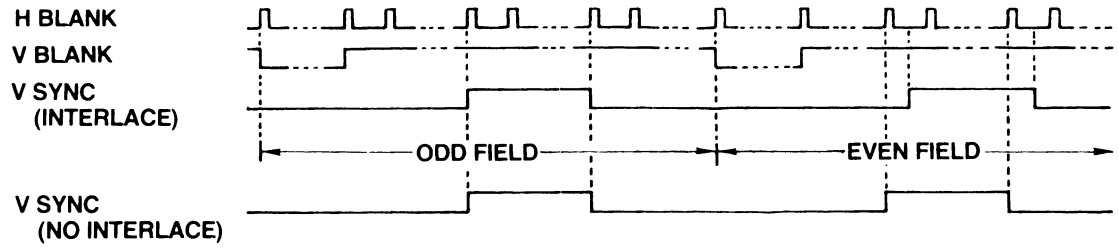
Write Timing

Zoomed Display Timing

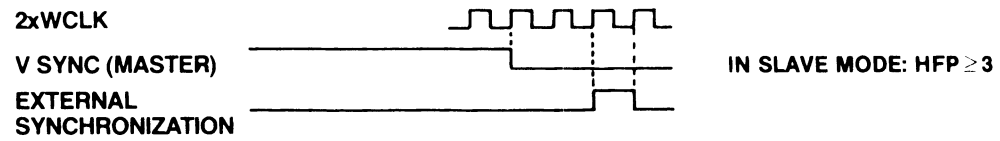


Video Sync Signals Timing

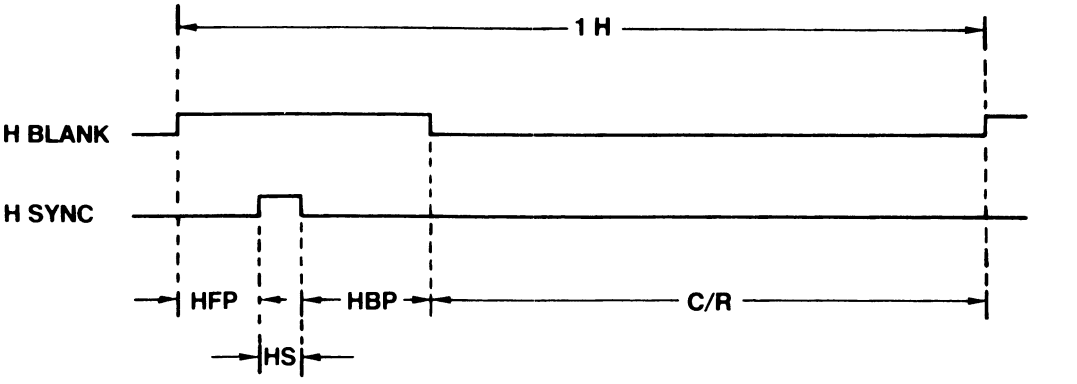


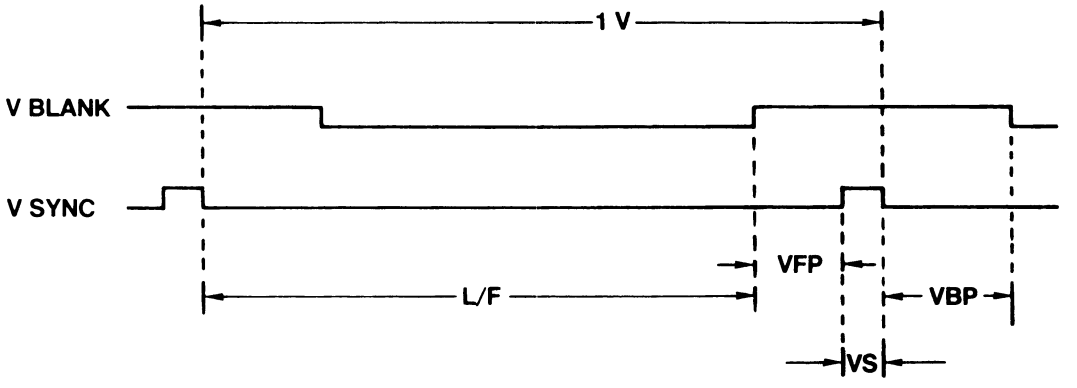


Interlaced Video Timing



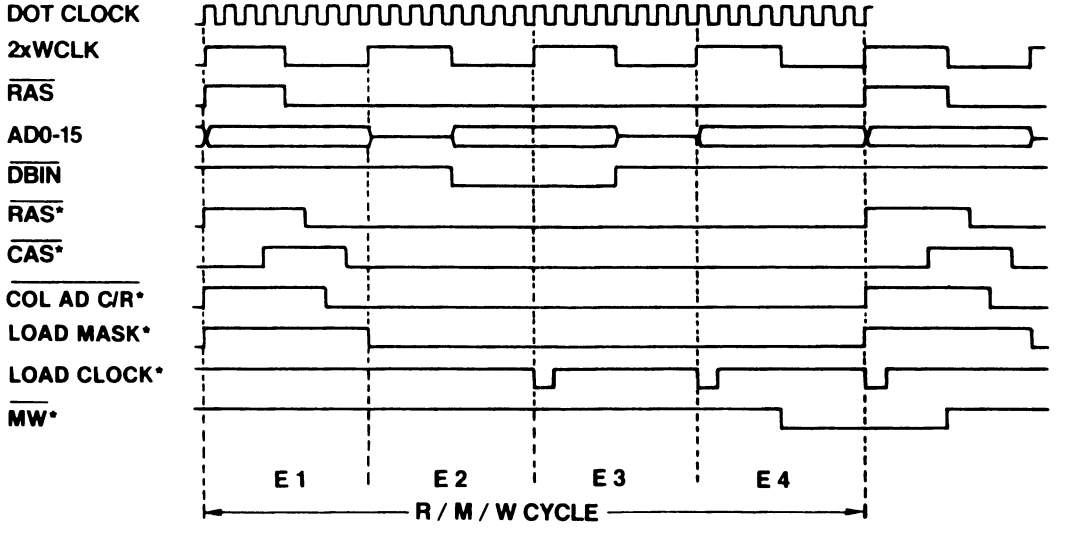
External Synchronization





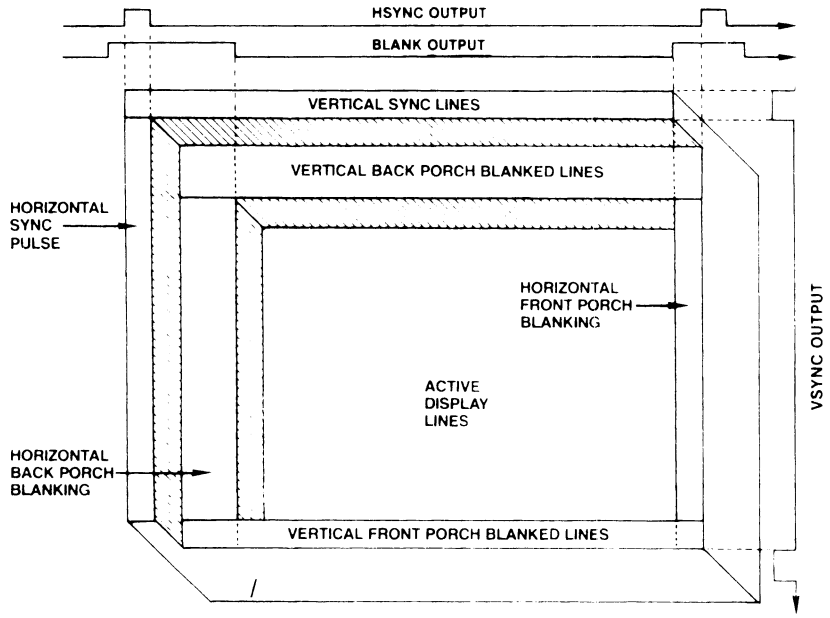
Video Sync Generator Parameters

Read-Modify-Write Cycle Timing

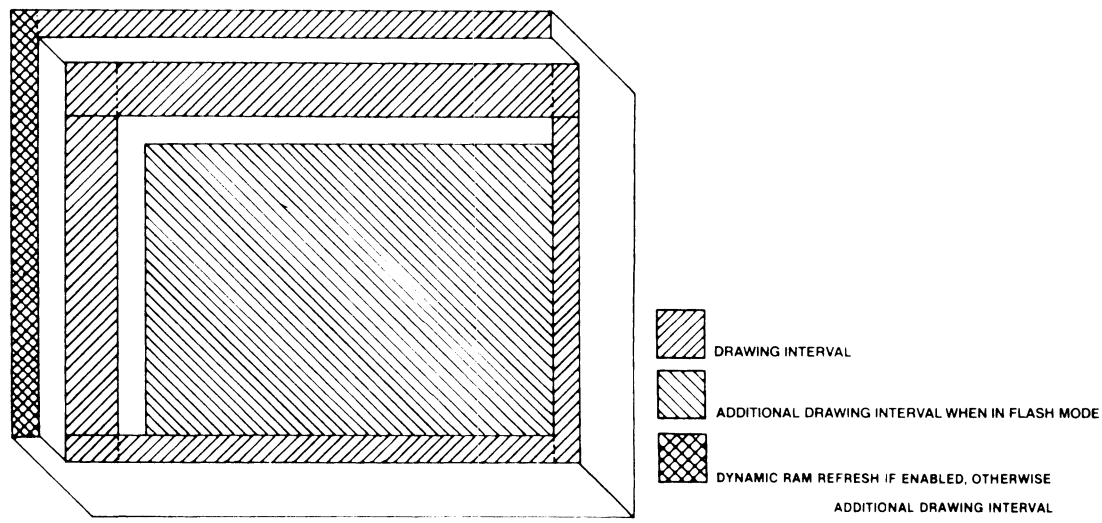


**externally generated signals*

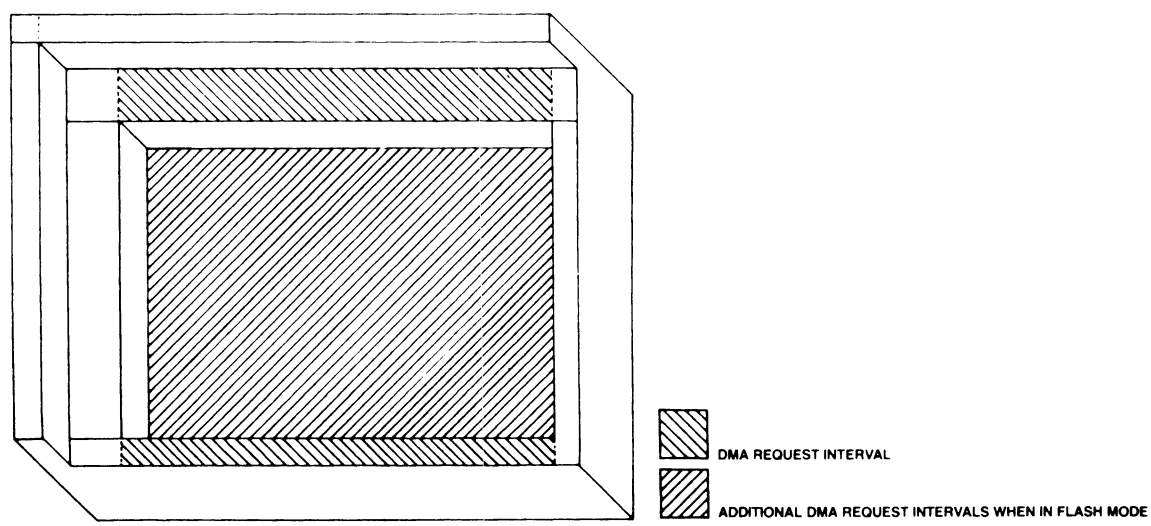
Video Field Timing



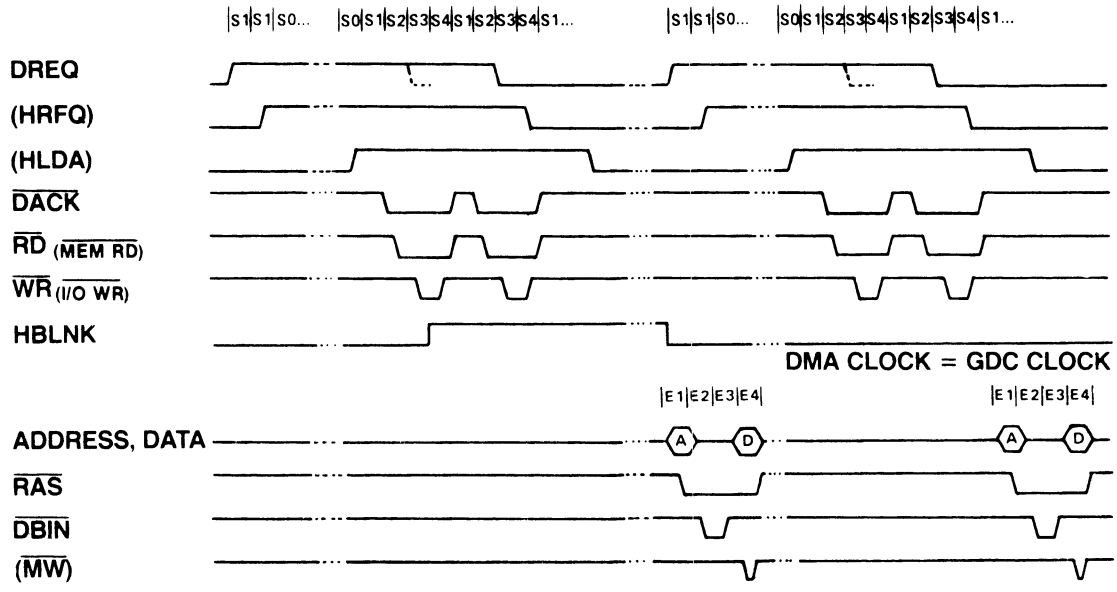
Drawing Intervals



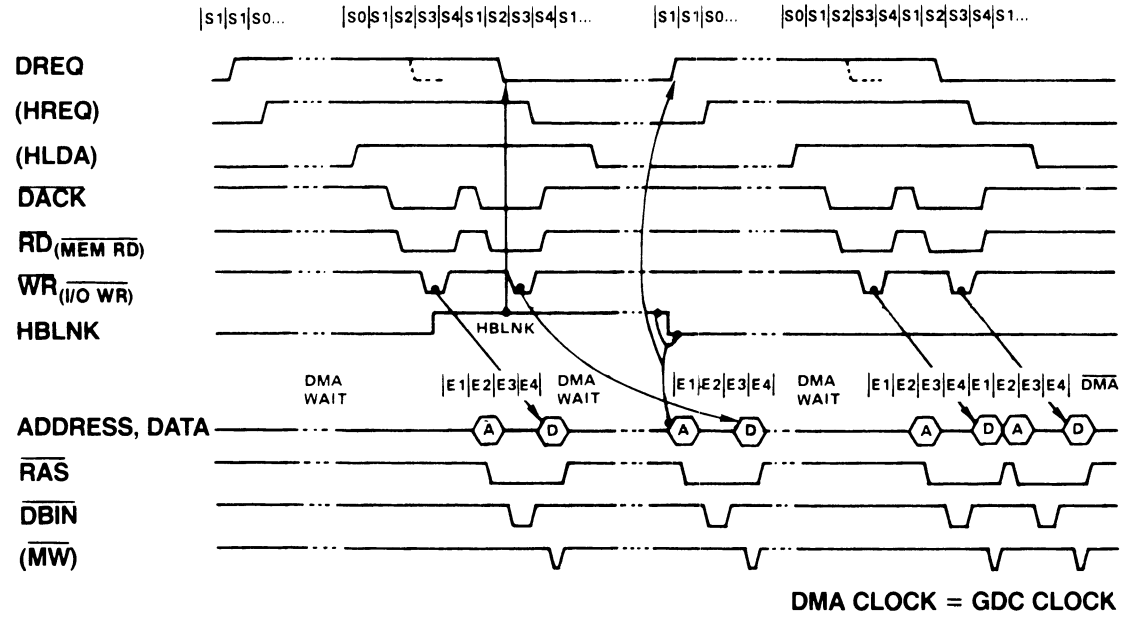
DMA Request Intervals



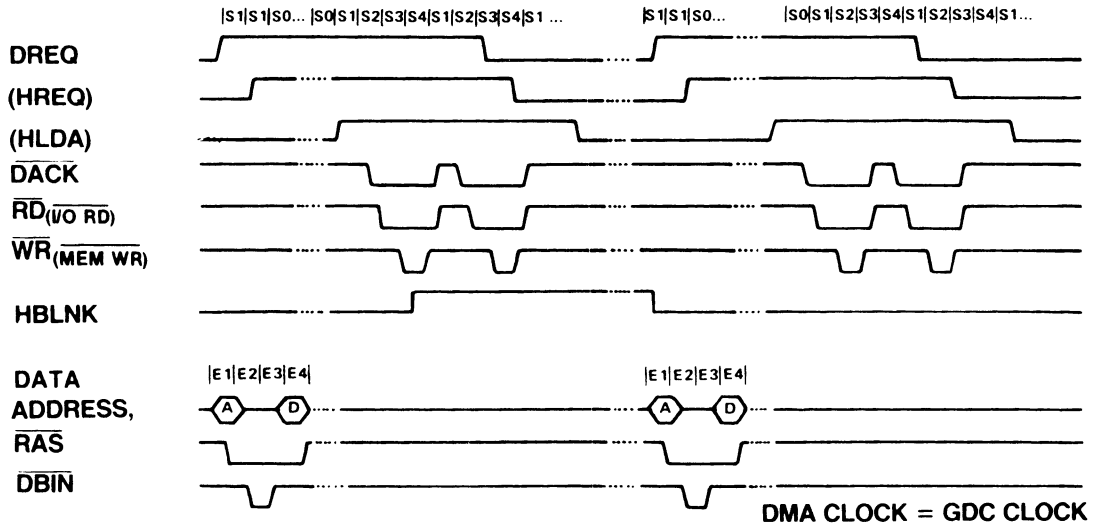
DMA Write (Word) Timing



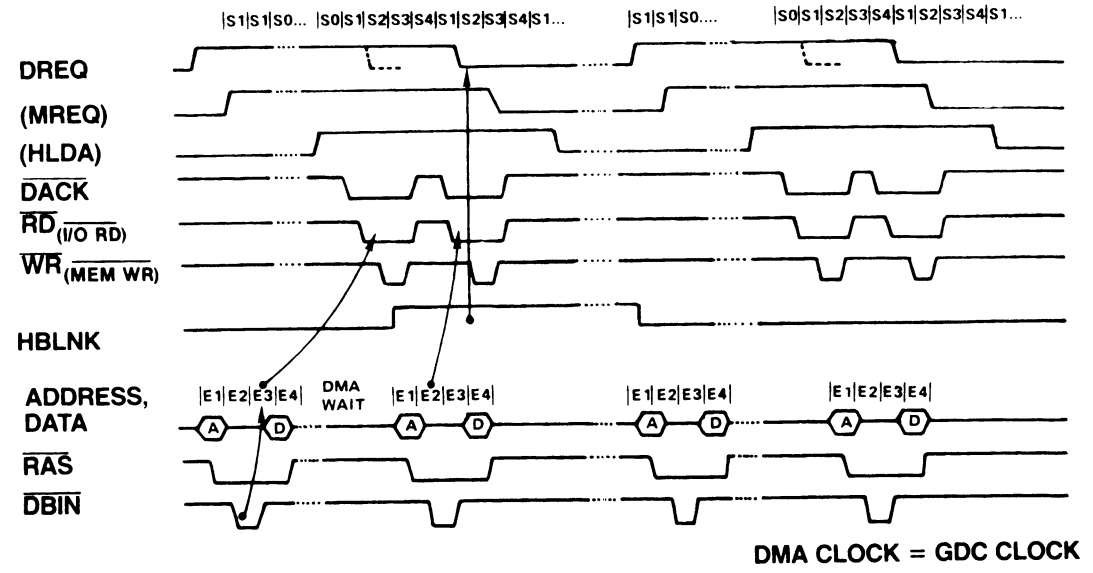
DMA Write (Low Byte, High Byte) Timing



DMA Read (Word) Timing

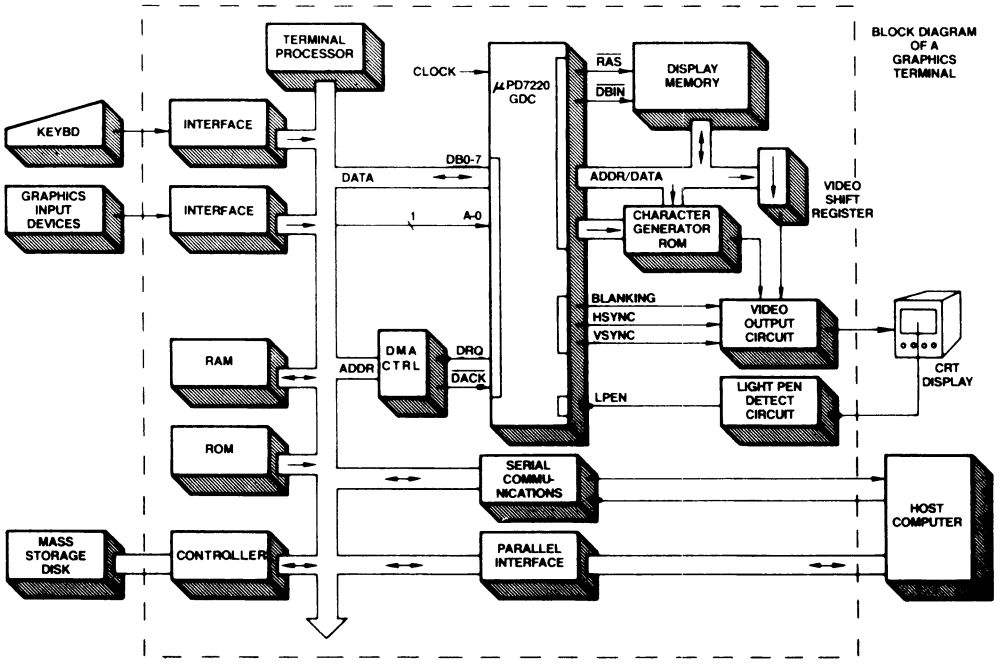


DMA Read (Low Byte, High Byte) Timing

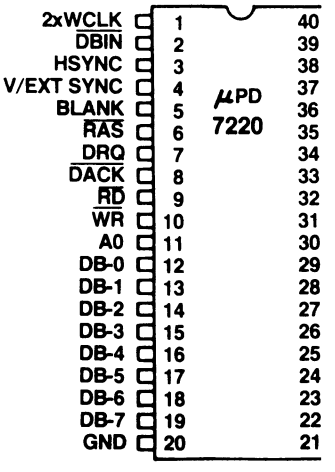


PIN #	PIN NAME	DIRECTION	MODES OF OPERATION		
			GRAPHICS	CHARACTER	MIXED
7	DRQ	OUT	DMA Request Output		
8	$\overline{DACK}$	IN	DMA Acknowledge Input		
12 to 19	DB-0 to 7	IN/OUT	Data Bus to Microprocessor		
11	A0	IN	Address Select Input for Microprocessor Interface		
9	$\overline{RD}$	IN	Read Strobe Input for Microprocessor Interface		
10	$\overline{WR}$	IN	Write Strobe Input for Microprocessor Interface		
3	HSYNC	OUT	Horizontal Video Sync Output		
4	V/EXT SYNC	IN/OUT	Vertical Video Sync Output or External Sync Input		
5	BLANK	OUT	CRT Beam Blanking Output		
1	2xWCLK	IN	Clock Input		
6	$\overline{RAS}$ (ALE)	OUT	Row Address Strobe and Address Latch Enable		
2	$\overline{DBIN}$	OUT	Display Memory Data Bus "Input" Read Cycle Output		
39	A-17	OUT	Address Bit 17 Output	Cursor Output	Cursor & Image Mode Flag
38	A-16	OUT	Address Bit 16 Output	Line Counter Bit 3	Attribute Blink & Clear Line Counter
35 to 37	AD-13 to 15	IN/OUT	Address Bits 13 to 15	Line Counter Bits 0 to 2	Address Bits 13 to 15
22 to 34	AD-0 to 12	IN/OUT	Address and Data Lines to Video Display Memory		
21	LPEN	IN	Light Pen Detect Input		
40	V_{CC}	IN	+5V		
20	GND	IN	Ground		

GDC Pin Names



Block Diagram of a Graphics Terminal



Pin Configuratio

NEC
NEC Microcomputers
A Division of NEC Electronics U.S.A. Inc.

173 Worcester Street
Wellesley, Massachusetts 02181
Tel: 617-237-1910 TWX 710-383-1745

7220DS-6-81

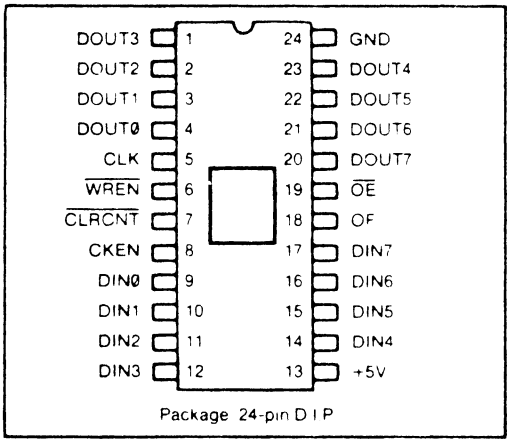
CRT 9006-135
CRT 9006-83
μPC FAMILY

Single Row Buffer
SRB

FEATURES:

- Low Cost Solution to CRT Memory Contention Problem
- Provides Enhanced Processor Throughput for CRT Display Systems
- Provides 8 Bit Wide Variable Length Serial Memory
- Permits Active Video on All Scan Lines of Data Row
- Dynamically Variable Number of Characters per Data Row — ...64, 80, 132,...up to a Maximum of 135
- Cascadable for Data Rows Greater than 135 Characters
- Stackable for Invisible Attributes or Character Widths of Greater than 8 Bits
- Three-State Outputs
- 3.3MHz Typical Read Write Data Rate
- Static Operation
- Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- 24 Pin Dual In Line Package
- +5 Volt Only Power Supply
- TTL Compatible Inputs and Outputs
- Available in 135 Byte Maximum Length (CRT 9006-135) or 83 Byte Maximum Length (CRT 9006-83)

PIN CONFIGURATION



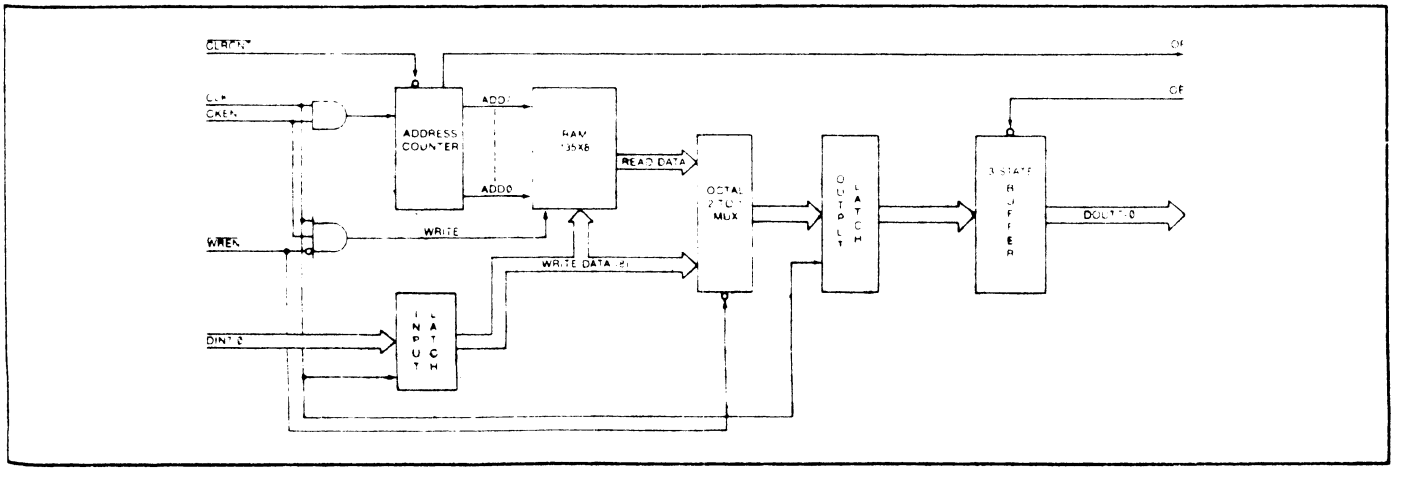
Package 24-pin D I P

APPLICATIONS:

- ☐ CRT Data Row Buffer
- ☐ Block-Oriented Buffer
- ☐ Printer Buffer
- ☐ Synchronous Communications Buffer
- ☐ Floppy Disk Sector Buffer

GENERAL DESCRIPTION

The SMC Single Row Buffer (SRB) provides a low cost solution to memory contention between the system processor and CRT controller in video display systems.
The SRB is a RAM-based buffer which is loaded with character data from system memory during the first scan line of each data row. While data is being written into the RAM it is also being output through the multiplexer onto the Data Ouput (DOUT) Lines. During subsequent scan lines in the data row, the system will disable Write Enable ($\overline{WREN}$) and cause data to be read out from the internal RAM for CRT screen refresh, thereby releasing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row. The SRB enhances processor throughput and permits a flicker-free display of data.



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-4	DATA OUTPUTS	DOUT3-DOUT0	Data Outputs from the internal output latch.
5	CLOCK	CLK	Character clock. The negative-going edge of CLK clocks the latches. When CKEN (pin 8) is high, CLK will increment the address counter.
6	WRITE ENABLE	$\overline{WREN}$	When $\overline{WREN}$ is low, data from the input latch is transferred directly to the output latch and simultaneously written into sequential locations in the RAM.
7	CLEAR COUNTER	$\overline{CLRCNT}$	A negative transition on $\overline{CLRCNT}$ clears the RAM address counter. $\overline{CLRCNT}$ is normally asserted low near the beginning of each scan line.
8	CLOCK ENABLE	CKEN	When CKEN is high, CLK will clock the address counter. The combination of CKEN high and WREN low will allow the writing of data into the RAM.
9-12	DATA INPUTS	DIN0-DIN3	Data Inputs from system memory.
13	POWER SUPPLY	V_{CC}	+5 Volt supply.
14-17	DATA INPUTS	DIN4-DIN7	Data Inputs from system memory.
18	OVERFLOW FLAG	OF	This output goes high when the RAM address counter reaches its maximum count. If cascaded operation of multiple CRT 9006's is desired for more than 135 bytes, OF may be used to drive the CKEN input of the second row buffer chip.
19	OUTPUT ENABLE	$\overline{OE}$	When $\overline{OE}$ is low, the data outputs DOUT0-DOUT7 are enabled. When $\overline{OE}$ is high, DOUT0-DOUT7 present a high impedance state.
20-23	DATA OUTPUTS	DOUT7-DOUT4	Data Outputs from the internal output latch.
24	GROUND	GND	Ground.

OPERATION

For CRT operation, the Write Enable ($\overline{WREN}$) signal is made active for the duration of the top scan line of each data row. Clear Counter ($\overline{CLRCNT}$) typically occurs at the beginning of each scan line (HSYNC may be used as input to $\overline{CLRCNT}$). Data is continually clocked into the input latch by CLK. When Clock Enable (CKEN) occurs, the data in the input latch (Write Data) is written into the first location of RAM. At the negative-going edge of the next clock, the address counter is incremented, the next input data is latched into the input latch, and the new data is then written into the RAM. Loading the RAM continues until one clock after CKEN goes inactive or until the RAM has been fully loaded (135 bytes). While data is being written into the RAM, it is also being output through the multiplexer onto the Data Output (DOUT) lines. Each byte is loaded into the output latch one clock time later than it is written into the RAM. Output of the data during the first scan line permits the Video Display Controller (such as the CRT 8002) to display video on the first scan line. During subsequent scan lines in the data row, the system will disable Write Enable ($\overline{WREN}$) and cause data to be read out from the internal RAM, thereby freeing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° C to + 70° C
Storage Temperature Range ..... -55° C to + 150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = +5 ±5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level V_{IL}			0.8	V	
High Level V_{IH}	2.0			V	
Output Voltage Levels					
Low Level V_{OL}			0.4	V	I_{OL} = 2mA
High Level V_{OH}	2.4			V	$I_{OH} = -100\mu A$
Input Current Leakage, I_{IL}			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Output '1' Leakage			10	μA	
Output '0' Leakage (Off State)			10	μA	
Input Capacitance					
CLK		30	45	pF	
All other inputs		10	15	pF	
Power Supply Current					
I_{CC} (SRB-135)			115	mA	
I_{CC} (SRB-83)			100	mA	
AC CHARACTERISTICS					
t_{cy}					
(SRB135)	300	250		ns	
(SRB83)	400	330		ns	
t_{CKL}					
(SRB135)	240	190	DC	ns	
(SRB83)	320	250	DC	ns	
t_{CKH}					
(SRB135)	28		5000	ns	
(SRB83)	34		5000	ns	
t_{CKR}					
(SRB135)			10	ns	t_{CKH} = 28ns
(SRB83)			10	ns	t_{CKH} = 34ns
t_{CKF}					
(SRB135)			10	ns	t_{CKL} = 240ns
(SRB83)			10	ns	t_{CLK} = 320ns
t_{DSET}	65			ns	
t_{DHOLD}	0			ns	
t_{ENCKP}	0			ns	
t_{ENCKN}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{ENHOLD}	0			ns	
t_{WRCKN}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{WENHLD}	0			ns	
t_{DOUT}			175	ns	C_L = 50pF
t_{TSON}			175	ns	
t_{TSOFF}			175	ns	
t_{OFON}			175	ns	C_L = 30pF
t_{CLRS}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{CLRH}	0			ns	

FIGURE 1: AC CHARACTERISTICS

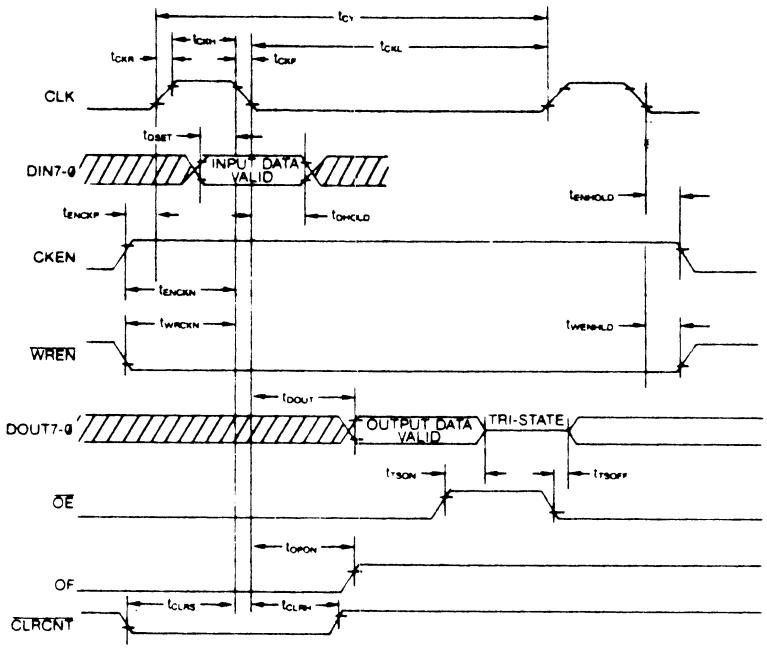
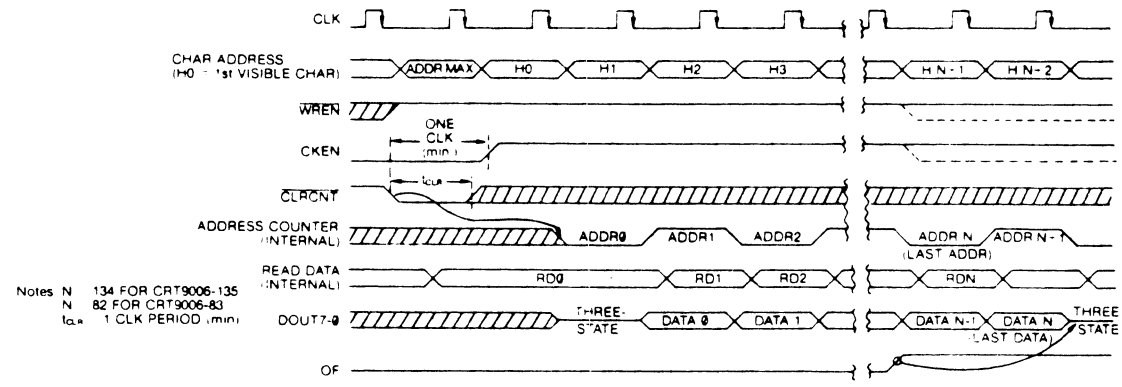
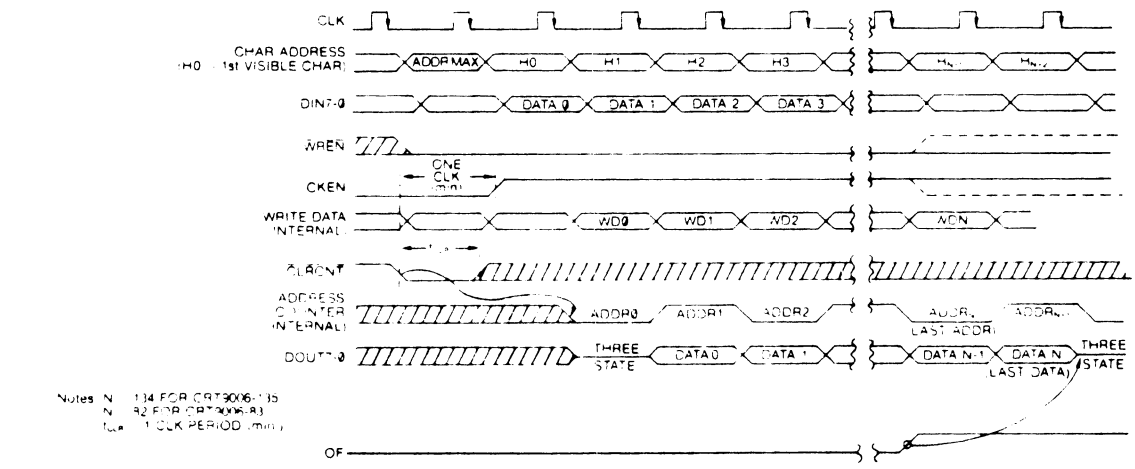


FIGURE 2: SINGLE ROW BUFFER READ TIMING



Notes N = 134 FOR CRT9006-135
N = 82 FOR CRT9006-83
t_{CLR} = 1 CLK PERIOD (min)

FIGURE 3: SINGLE ROW BUFFER WRITE TIMING



Notes N = 134 FOR CRT9006-135
N = 82 FOR CRT9006-83
t_{CLR} = 1 CLK PERIOD (min)

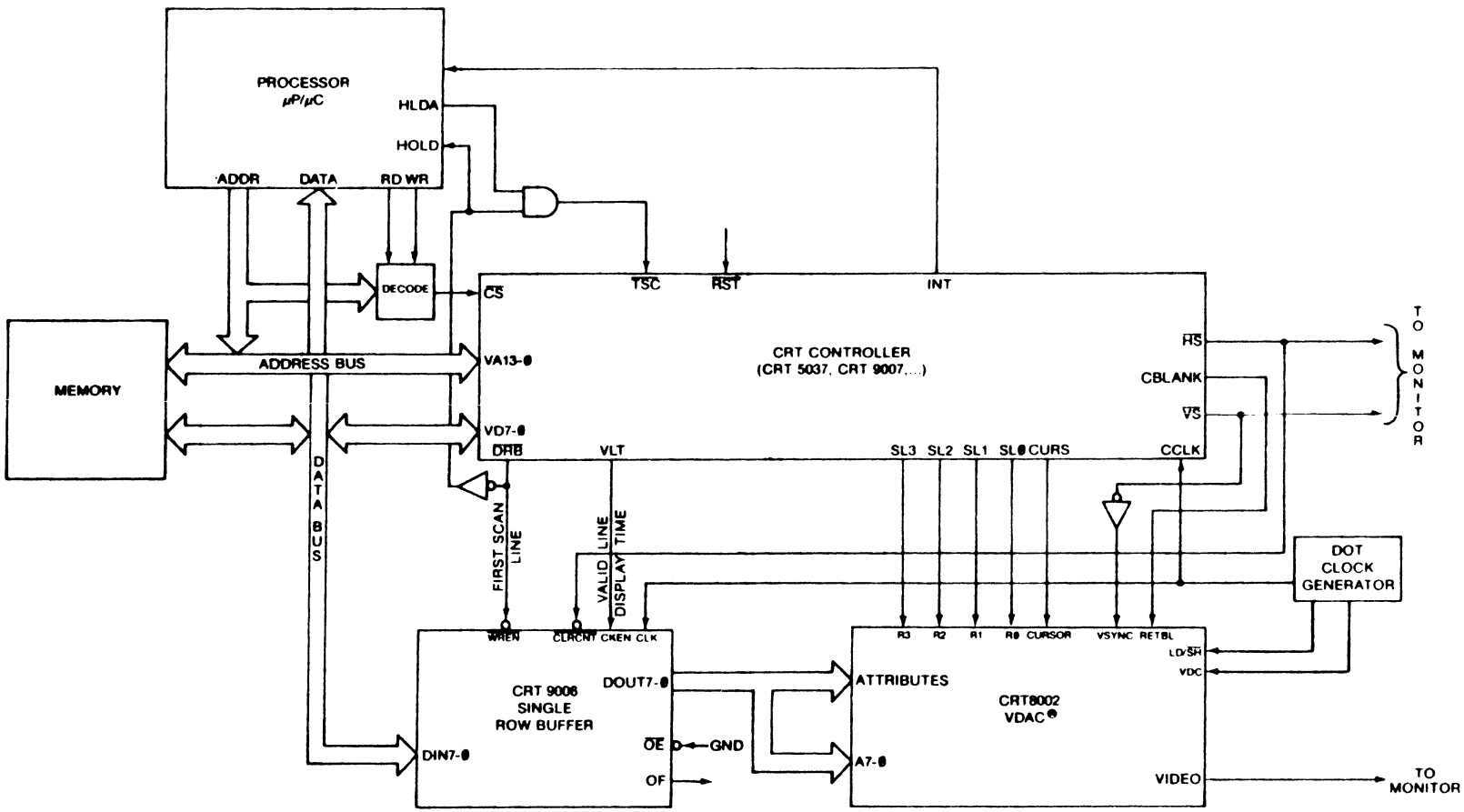
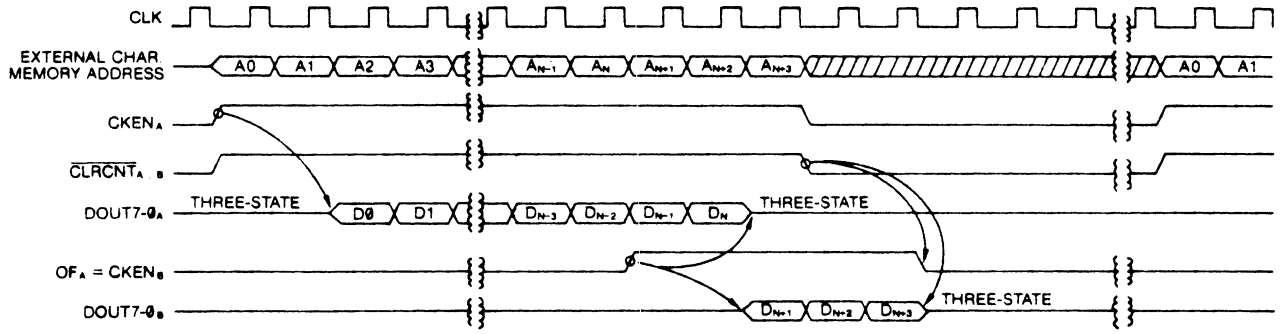


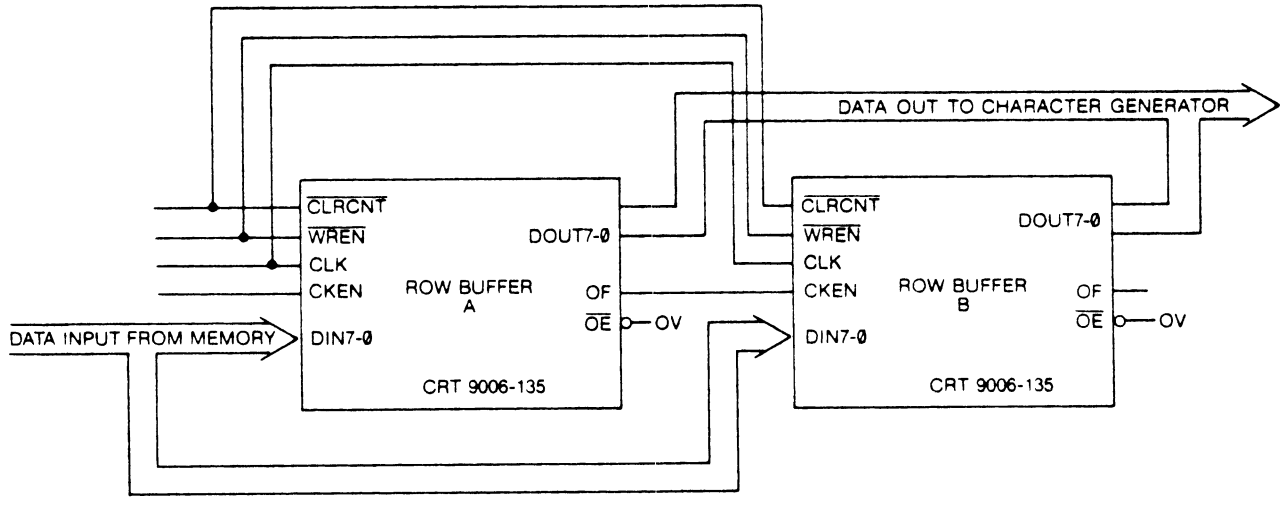
FIGURE 2: TYPICAL CRT CONTROLLER CONFIGURATION WITH SINGLE ROW BUFFER

FIGURE 4:
TYPICAL READ TIMING FOR SRB CASCADED CONFIGURATION



Notes: N = 134 FOR CRT9006-135
N = 82 FOR CRT9006-83
EXAMPLE IS FOR N+3 CHARACTERS TOTAL
A, B REFER TO DEVICES A&B IN FIGURE 5

FIGURE 5:
TYPICAL CASCADE OF SINGLE ROW BUFFERS—270 BYTES TOTAL



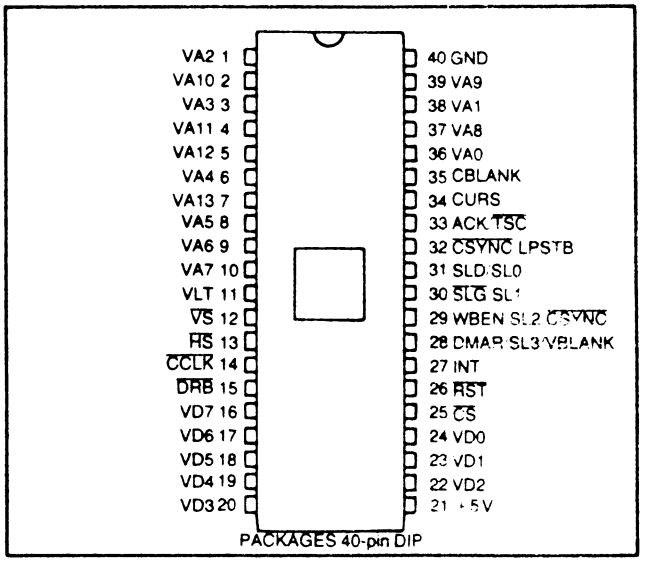
CRT 9007
μPC FAMILY

CRT Video Processor and Controller
VPAC™

FEATURES

- Fully Programmable Display Format
  - Characters per Data Row (8-240)
  - Data Rows per Frame (2-256)
  - Raster Scans per Data Row (1-32)
- Programmable Monitor Sync Format
  - Raster Scans/Frame (4-2048)
  - Front Porch — Horizontal (Negative or Positive)
    - Vertical
  - Sync Width — Horizontal (1-128 Character Times)
    - Vertical (2-256 Scan Lines)
  - Back Porch — Horizontal
    - Vertical
- Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Composite Blanking
  - Cursor Coincidence
- Binary Addressing of Video Memory
- Row-Table Driven or Sequential Video Addressing Modes
- Programmable Status Row Position and Address Registers
- Bidirectional Partial or Full Page Smooth Scroll
- Attribute Assemble Mode
- Double Height Data Row Mode
- Double Width Data Row Mode
- Programmable DMA Burst Mode
- Configurable with a Variety of Memory Contention Arrangements
- Light Pen Register
- Cursor Horizontal and Vertical Position Registers
- Maskable Processor Interrupt Line
- Internal Status Register
- Three-state Video Memory Address Bus
- Partial or Full Page Blank Capability
- Two Interlace Modes: Enhanced Video and Alternate Scan Line

PIN CONFIGURATION



PACKAGES 40-pin DIP

- Ability to Delay Cursor and Blanking with respect to Active Video
- Programmable for Horizontal Split Screen Applications
- Graphics Compatible
- Ability to Externally Sync each Raster Line, each Field
- Single +5 Volt Power Supply
- TTL Compatible on All Inputs and Outputs
- VT-100 Compatible
- RS-170 Interlaced Composite Sync Available

GENERAL DESCRIPTION

The CRT 9007 VPAC™ is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the VPAC™ provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The VPAC™ works with a variety of memory contention schemes including operation with a Single Row Buffer such as the CRT 9006, a Double Row Buffer such as the CRT 9212, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and VPAC™ status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".

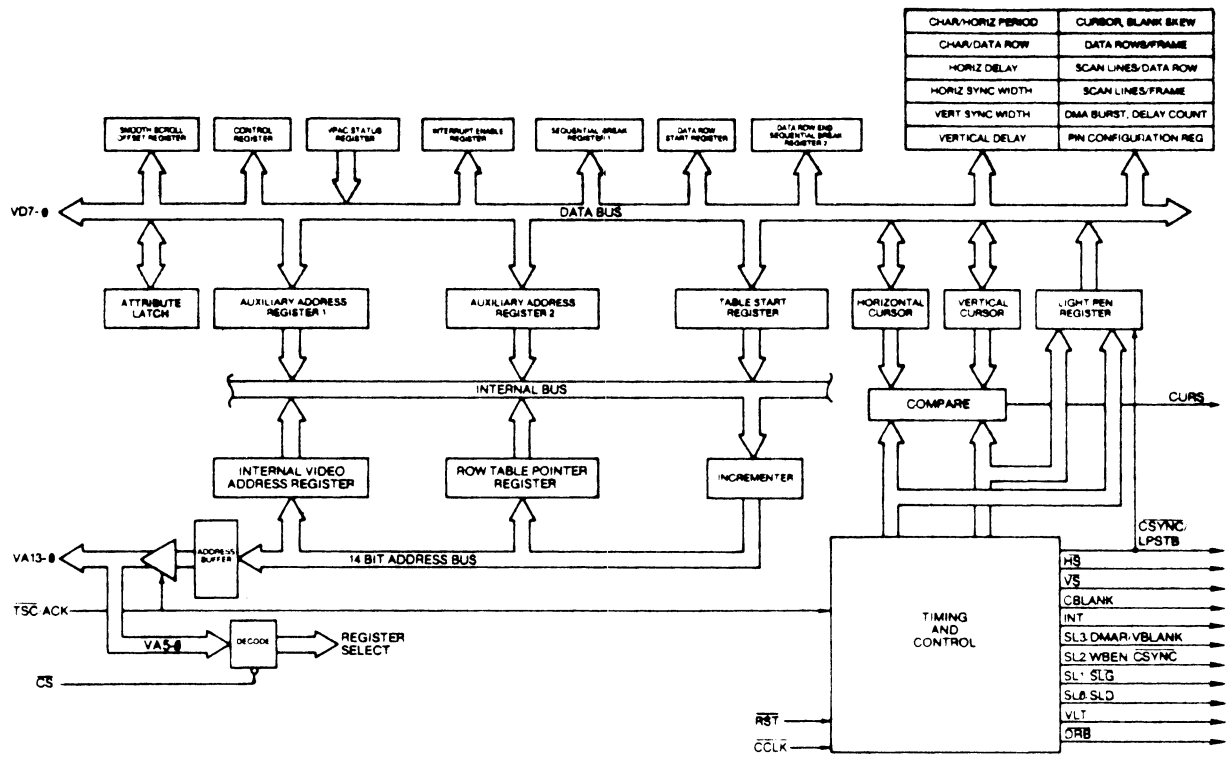


FIGURE 1: CRT 9007 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PROCESSOR INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
7, 5, 4, 2, 39, 37, 10, 9, 8, 6, 3, 1, 38, 36	Video Address 13-0	VA13-VA0	These 14 signals are the binary address presented to the video memory by the CRT 9007. The function depends on the particular CRT 9007 mode of operation. VA13-6 are outputs only. VA5-0 are bidirectional. —Double Row Buffer Configuration: VA13-0 are active outputs for the DMA operations and are in their high impedance state at all other times. —Single Row Buffer Configuration: VA13-0 are active outputs during the first scan line of each data row and are in their high impedance state at all other times. —Repetitive Memory Addressing Configuration: VA13-0 are active outputs at all times except during horizontal and vertical retrace at which time they are in their high impedance state. If row table addressing is used for either single row buffer or repetitive memory addressing modes, VA13-0 are active outputs during the horizontal retrace at each data row boundary to allow the CRT 9007 to retrieve the row table address. For processor read/write operations VA5-0 are inputs that select the appropriate internal register.
16, 17, 18, 19, 20, 22, 23, 24	Video Data 7-0	VD7-VD0	Bidirectional video data bus: during processor Read/write operations data is transferred via VD7-VD0 when chip strobe ($\overline{CS}$) is active. These lines are in their high impedance state when $\overline{CS}$ is inactive. During CRT 9007 DMA operations, data from video memory is input via VD7-VD0 when a new row table address is being retrieved or when the attribute latch is being updated in the attribute assemble mode. VD7-VD0 are outputs when the external row buffer is updated with a new attribute in the attribute assemble mode.
25	Chip strobe	$\overline{CS}$	Input: this signal when active low, allows the processor to read or write internal CRT 9007 registers. When reading from an internal CRT 9007 register, the chip strobe ($\overline{CS}$) enables the output drivers. When writing to an internal CRT 9007 register, the trailing edge of this signal latches the incoming data. Figure 2 shows all processor read/write timing.
26	Reset	$\overline{RST}$	Input: this active low signal puts the CRT 9007 into a known, inactive state and insures that the horizontal sync ($\overline{HS}$) output is inactive. Activating this input has the same effect as a RESET command. After initialization, a START command causes normal CRT 9007 operation. See processor addressable registers section, Register 16 for the reset state definition.
27	Interrupt	INT	Output: an interrupt to the processor from the CRT 9007 occurs when this signal is active high. The interrupt returns to its inactive low state when the status register is read.

DESCRIPTION OF PIN FUNCTIONS CONT'D

CRT INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
11	Visible Line Time	VLT	Output; this signal is active high during all visible scan lines and during the horizontal trace times at vertical retrace. This signal can be used to gate the character clock ($\overline{CCLK}$) when supplying data to a character generator from a single or double row buffer.
12	Vertical Sync	$\overline{VS}$	Open drain output, this signal determines the vertical position of displayed text by initiating a vertical retrace. Its position and pulse width are user programmable. The open drain allows the vertical frame rate to be synchronized to the line frequency when using monitors with DC coupled vertical amplifiers. If the $\overline{VS}$ output is pulled active low externally before the CRT 9007 itself initiates a vertical sync, the CRT 9007 will start its own vertical sync at the next leading edge of horizontal sync ($\overline{HS}$).
13	Horizontal Sync	$\overline{HS}$	Open drain output; this signal determines the horizontal position of displayed text by initiating a horizontal retrace. Its position and pulse width are user programmable. During hardware and software reset, this signal is inactive high. The open drain allows the horizontal scan rate to be synchronized to an external source. If the $\overline{HS}$ output is pulled low externally before the CRT 9007 itself initiates a horizontal sync, the CRT 9007 will start its own horizontal sync on the next character clock ($\overline{CCLK}$).
14	Character Clock	$\overline{CCLK}$	Input; this signal defines the character rate of the screen and is used by the CRT 9007 for all internal timing. A minimum high voltage of 4.3V must be maintained for proper chip operation.
15	Data Row Boundary	$\overline{DRB}$	Output: this signal is active low for one full scan line (from VLT trailing edge to VLT trailing edge) at the top scan line of each new data row. This signal can be used to swap buffers in the double row buffer mode. It indicates the particular horizontal retrace time that the CRT 9007 outputs addresses (VA13-VA0) for single row buffer operation. There will always be one extra $\overline{DRB}$ signal which will become active during the first scan line of the vertical retrace interval.
34	Cursor	CURS	Output; this signal marks the cursor position on the screen as specified by the horizontal and vertical cursor registers. The signal is active for one character time at the particular character position for all scan lines within the data row. For double height or width characters, this signal is active for 2 consecutive $\overline{CCLK}$'s in every scan line within the data row. For double height characters, this signal can be programmed to be active at the proper position for 2 consecutive data rows. CURS is also used to signal either a double height or double width data row by becoming active during the horizontal retrace (CBLANK active) prior to a double height or double width scan line. The time of activation and deactivation is a function of the addressing mode, buffer configuration and the scan line number. See section of Double height/width for details.
35	Composite Blank	CBLANK	Output. This signal when active high, indicates that a retrace (either horizontal or vertical) will be performed. The signal remains active for the entire retrace interval as programmed. It is used to blank the video to a CRT.

USER SELECTABLE PINS: (see Tables 4 and 5)

PIN NO.	NAME	SYMBOL	FUNCTION
28, 29, 30, 31	Scan Line 3-Scan Line 0	SL3-SL0	Output; these 4 signals are the direct scan line counter outputs, in binary form, that indicate to the character generator the current scan line. These signals continue to be updated during the vertical retrace interval. SL3 and SL0 are the most and least significant bits respectively.
28	Direct Memory Access Request	DMAR	Output; this signal is the DMA request issued by the CRT 9007. It will only become active if the acknowledge (ACK) input is inactive. It remains active high throughout the entire DMA operation.
28	Vertical Blank	VBLANK	Output; this signal is active high only during the vertical retrace period.
29	Write Buffer Enable	WBEN	Output; this active high signal is used to gate the clock feeding the write buffer in a double row buffer configuration.
29 or 32	Composite Sync	$\overline{CSYNC}$	Output; this signal provides a true RS-170 composite sync waveform with equalization pulses and vertical serrations in both interlace and noninterlace formats. Figure 3 illustrates the $\overline{CSYNC}$ output in both interlaced and noninterlaced formats.
30	Scan Line Gate	$\overline{SLG}$	Output; this active low signal is used as a clock gate. It captures the correct 5 or 6 $\overline{CCLK}$'s and, in conjunction with $\overline{SLD}$ (pin 31), allows scan line information to be loaded serially into an external shift register.
31	Scan Line Data	SLD	Output; this signal allows one to load an external shift register with the current scan line count. The count is presented least significant to most significant bit during the 5 or 6 $\overline{CCLK}$'s framed by $\overline{SLG}$. With this form of scan line representation, it is possible to define up to 32 scan lines per data row. The external shift register must be at least 5 bits in length. Even though 6 shifts can occur one should only use the 5 last bits shifted to define the scan line count. The extra shift occurs in interlace or double height character mode to allow the scan line count to be adjusted to its proper value. Figures 4 and 5 illustrate the serial scan line timing.
32	Light Pen Strobe	LPSTB	Input; this signal strobes the current row/column position into the light pen register at its positive transition.
33	Acknowledge	ACK	Input; this active high signal acknowledges a DMA request. It indicates that the processor bus has entered its high impedance state and the CRT 9007 may access video memory. It is not recommended to deactivate this signal during a CRT 9007 DMA cycle because the CRT 9007 will not shut down in a predictable amount of time.
33	Three State Control	$\overline{TSC}$	Input; this signal, when active low, places VA13-VA0 in their high impedance state.

OPERATION MODES

Single Row Buffer Operation

The CRT 9007 configured with a CRT 9006 Single Row Buffer is shown in figure 6. The use of the CRT 9006 Single Row Buffer requires that the buffer be loaded at the video painting rate during the top scan line of each data row. However, after the CRT 9006 is loaded, the CRT 9007 address lines enter their high impedance state for the remaining N-1 scan lines of the data row, thereby permitting full processor access to memory during these scan lines. The percentage of total memory cycles available to the processor is approximately [(N-1)/N] × 100 where N is the total number of scan lines per data row. For a typical system with 12 scan lines per data row this percentage is 92%. Figure 7 illustrates typical timing for the CRT 9007 used with the CRT 9006 Single Row Buffer.

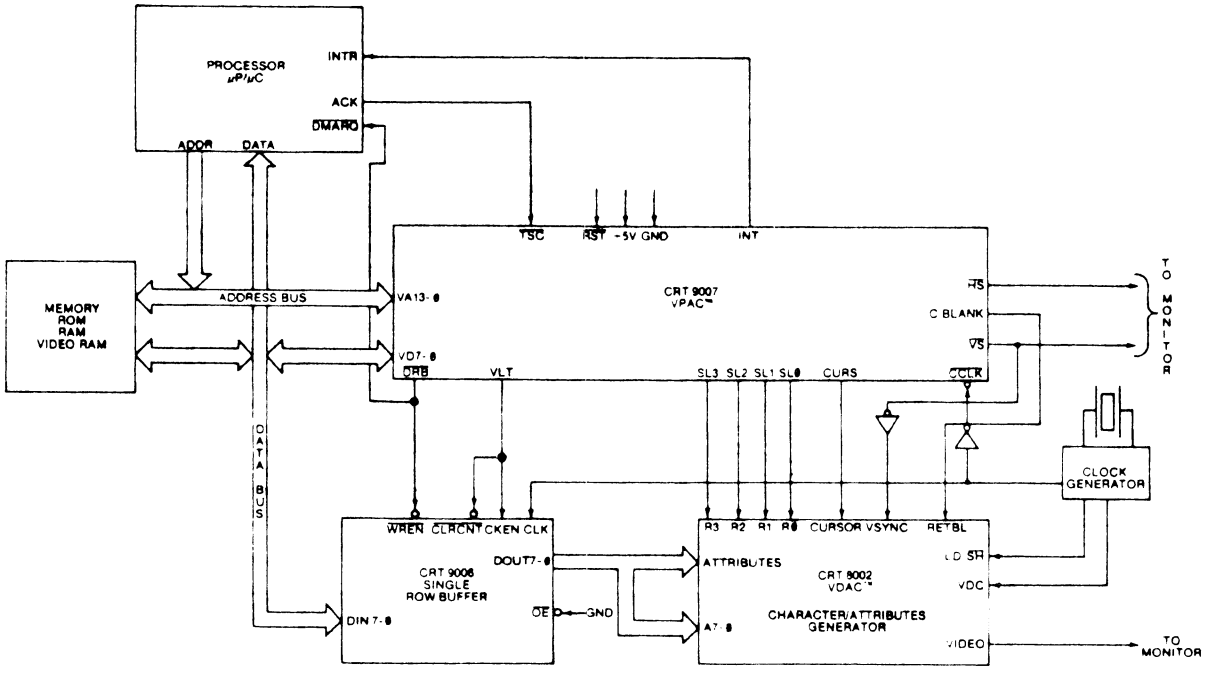


FIGURE 6: CRT 9007 CONFIGURATION WITH SINGLE ROW BUFFER

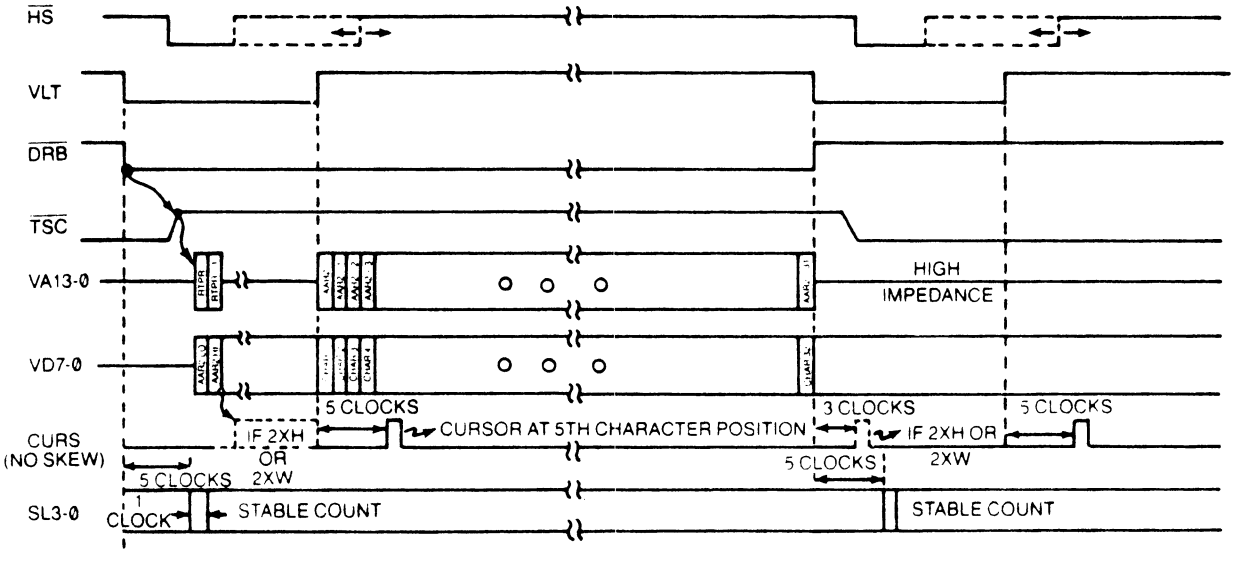


FIGURE 7: CRT 9007 SINGLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

Double Row Buffer Operation

Figure 8 shows the CRT 9007 used in conjunction with a CRT 9212 Double Row Buffer. The Double Row Buffer has a read buffer which is read at the painting rate of the CRT during each scan line in the data row. While the read buffer is being read and supplying data to the character generator for the current displayed data row, the write buffer is being loaded with the next data row to be displayed. This arrangement allows for relaxed write timing to the write buffer as it may be filled in the time it takes for N scan lines on the CRT to be painted where N is the number of scan lines per data row. Used in this configuration, the CRT 9007 takes advantage of the relaxed write buffer timing by stealing memory cycles from the processor to fill the write buffer (Direct memory access operation). The CRT 9007 sends the DMAR (DMA request) signal, awaits an ACK (acknowledge) signal and then drives out on VA13-VA0 the address at which the next video data resides. The CRT 9007 then activates the WBEN (write buffer enable) signal to write the data into the buffer. If for example there are 80 characters per data row, the CRT 9007 performs 80 DMA operations. The user has the ability to program the number of DMA cycles performed during each DMAR-ACK sequence, as well as the delay between each DMAR-ACK sequence, via the DMA CONTROL REGISTER (RA). If 8 DMA operations are performed for each ACK received, 10 such DMAR-ACK sequences must be performed to completely fill the write buffer. The programmed delay allows the user to evenly distribute the DMA operations so as not to hold up the processor for an excessive length of time. This feature also permits other DMA devices to be used and allows the processor to respond to real time events. In addition, the user has the ability to disable the CRT 9007 DMA mechanism. Figure 9 illustrates typical timing for the CRT 9007 used with the CRT 9212 Double Row Buffer.

Since the CRT 9212 Double Row Buffer has separate inputs for read and write clocks (RCLK, WCLK), it is possible to display proportional character widths (variable number of dots per character) by reading out the buffer at a character clock rate determined by the particular character. The writing of the buffer can be clocked from a different and constant character clock. Figure 10 illustrates the CRT 9007 used with two double row buffers and a CRT 9021 Video Attributes Controller chip to provide proportional character display.

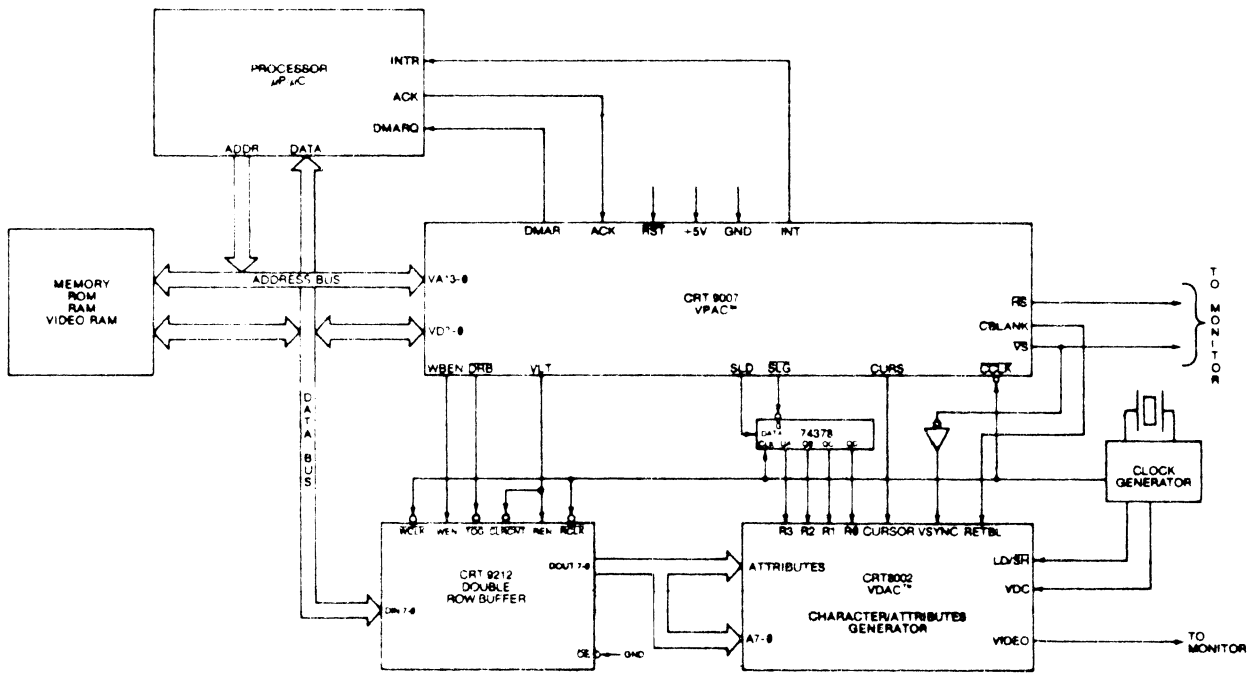


FIGURE 8: CRT 9007 CONFIGURATION WITH DOUBLE ROW BUFFER

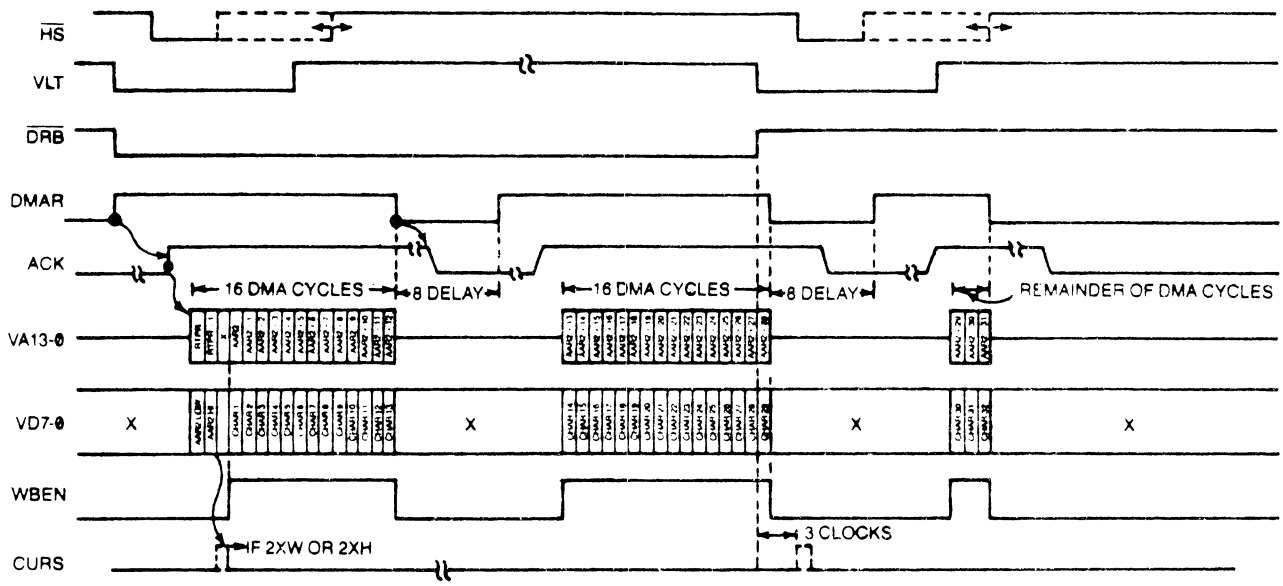


FIGURE 9: CRT 9007 DOUBLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

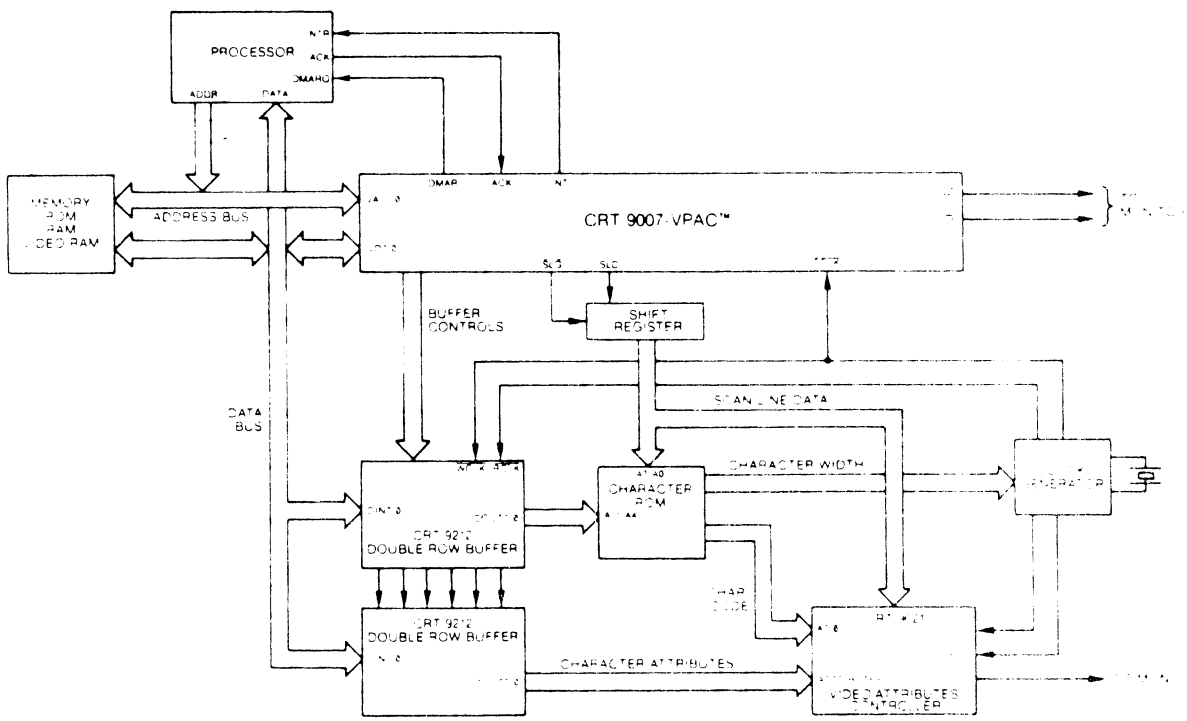


FIGURE 10: CRT 9007 CONFIGURATION FOR PROPORTIONAL CHARACTER DISPLAY

Repetitive Memory Addressing Operation

In this operation mode, the CRT 9007 will repeat the sequence of video addresses for every scan line of every data row. The CRT 9007 address bus will enter its high impedance state during all horizontal retrace intervals (except the retrace interval at a data row boundary if the CRT 9007 is configured in a row driven addressing mode). This arrangement allows for such low end contention schemes as retrace intervention (the processor is only allowed access to video memory during retrace intervals) and processor priority (the processor has an unlimited access to video memory). A high end contention scheme can be employed which uses a double speed memory such that in a single character period both the processor and the CRT 9007 are permitted access to video memory at predetermined time slots. Figure 11 illustrates the CRT 9007 configured with a double speed memory. Typical timing for this mode is illustrated in figure 12.

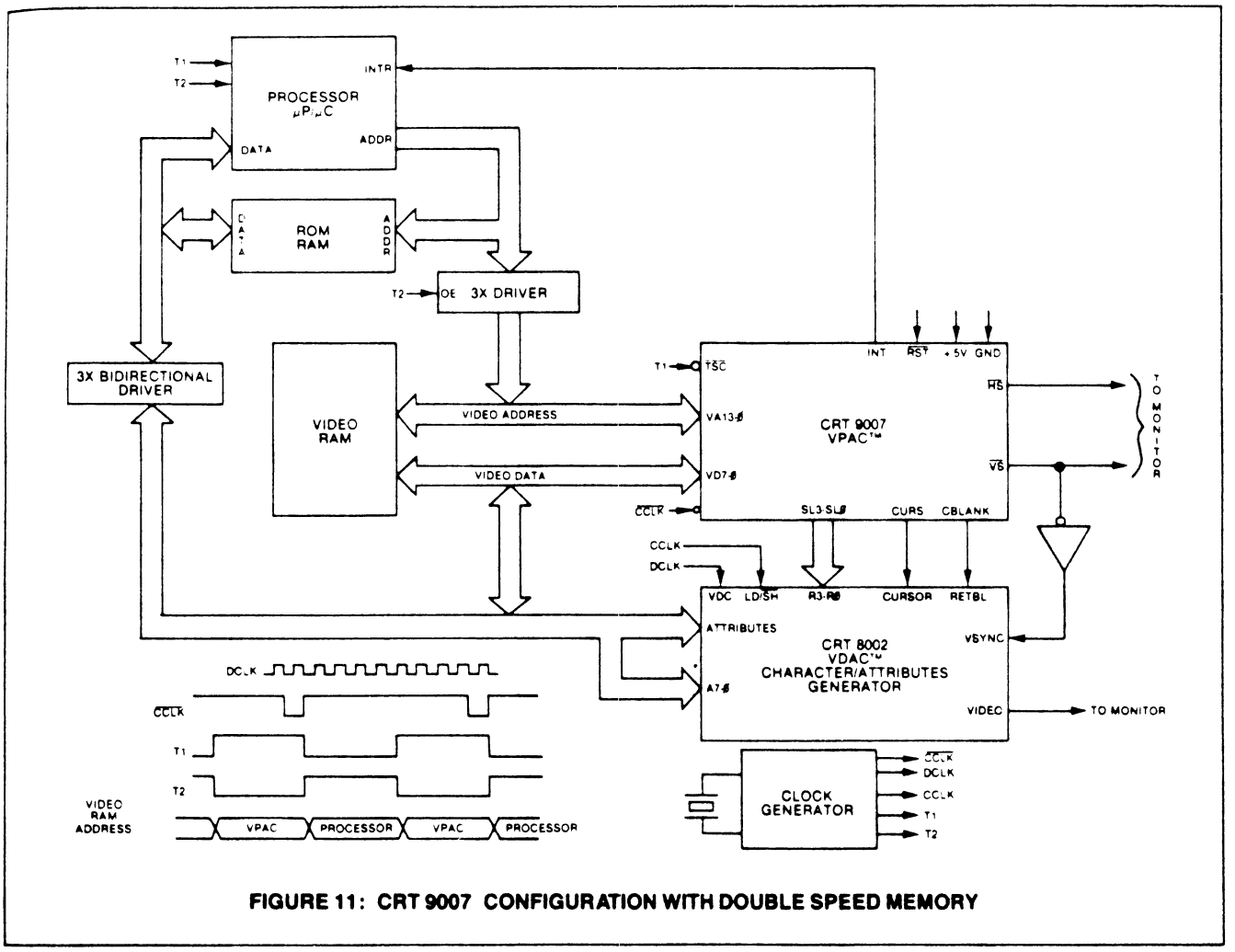


FIGURE 11: CRT 9007 CONFIGURATION WITH DOUBLE SPEED MEMORY

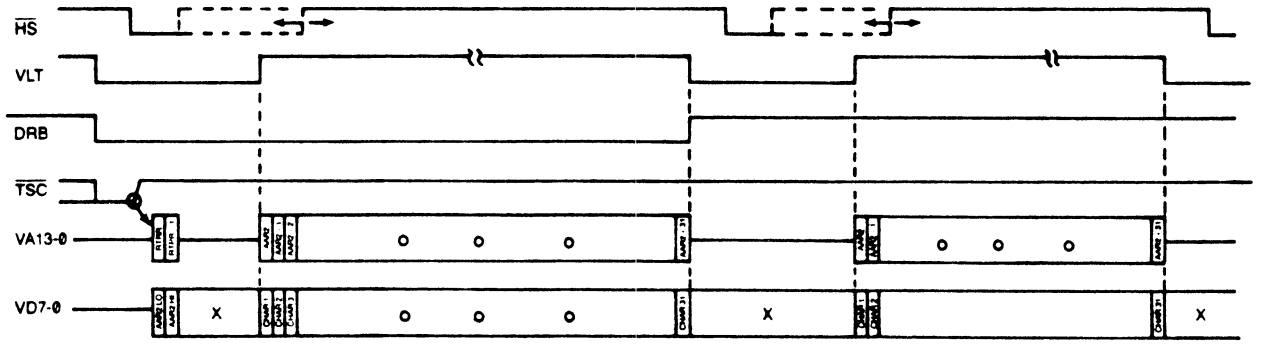


FIGURE 12: CRT 9007 REPETITIVE MEMORY ADDRESS TIMING (32 CHARACTERS PER DATA ROW)

Attribute Assemble Operation

This configuration allows the user to retain an 8 bit wide video memory in which attributes occupy memory locations but not positions on the CRT. This mode assumes that every other display position in video memory contains an attribute. During one clock cycle, attribute data is latched into the CRT 9007; during the next clock cycle a character location is addressed. The attribute data is driven out along with a WBEN signal allowing the character plus its associated attribute to be written simultaneously to two 8 bit double row buffers. Figure 13 illustrates the memory organization used for the Attribute Assemble mode. The first entry in each data row must begin with an attribute.

Figure 14 shows the CRT 9007 configured in the Attribute Assemble mode used with two CRT 9212 Double Row Buffers and 8, 16Kx1 dynamic RAMS. This mode, since it retains an 8 bit wide memory while providing all the advantages of a 16 bit wide memory, lends itself to some cost effective designs using dynamic RAMS. The CRT 9007 will refresh dynamic RAMS because twice the number of the programmed characters per data row are accessed sequentially for each data row.* Figure 15 illustrates typical timing of the CRT 9007 used in the Attribute Assemble mode.

Memory Address (typ)	Memory Data (8 bits)
0D00	Attribute 0
0D01	Character 0
0D02	Attribute 1
0D03	Character 1
0 0 0	0 0 0
2N	Attribute N
2N + 1	Character N

Figure 13: Attribute Assemble Memory Organization

*Note: For 50 Hz operation there usually is about 3 milliseconds extra vertical blanking where refreshing might fail. In this situation the CRT 9007 can be programmed with about 5 more "dummy" data rows while extending the vertical blank signal. This allows the CRT 9007 to start addressing video memory much earlier within the vertical blanking interval and hence provide refresh to the dynamic RAMS. When displaying double height or double width data rows, only half as many sequential locations are accessed each data row and dynamic RAM refresh might fail.

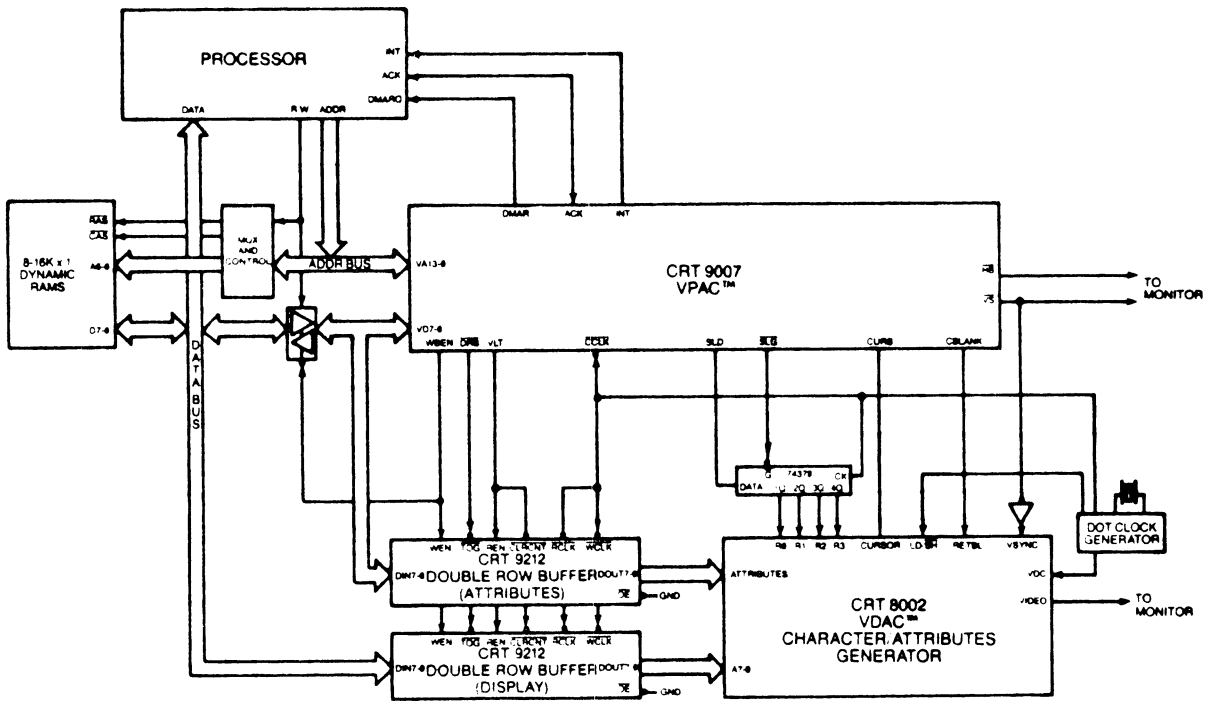
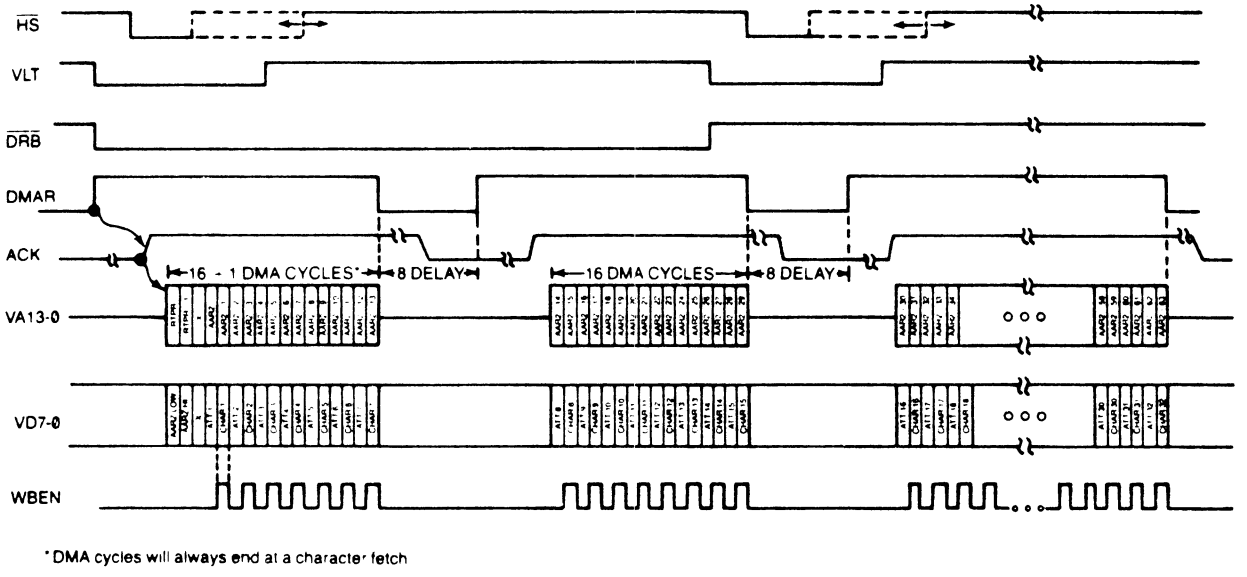


FIGURE 14: CRT 9007 CONFIGURATION FOR ATTRIBUTE ASSEMBLE MODE

Smooth Scroll Operation

Smooth scroll requires that all or a portion of the screen move up or down an integral number of scan lines at a time. 2 user programmable registers allow one to define the "start data row" and the "end data row" for the smooth scroll operation. A SMOOTH SCROLL OFFSET REGISTER (R17), when used in conjunction with a CRT 9007 vertically timed interrupt, allows the user to synchronize the update of the offset register to the vertical frame rate. The offset register causes the scan line counter outputs of the CRT 9007 to start at the programmed offset value rather than zero for the data row that starts the smooth scroll interval. To allow complete flexibility in smooth scroll direction and rate, one can update the offset register in the positive as well as negative direction and can also offset any number of scan lines each frame. Since a smooth scroll can momentarily result in a partial data row consisting of one scan line, the loading of the write buffer under DMA operations for the start and end data row of the smooth scroll operation is forced to occur in one scan line. This condition overrides the programmable DMA CONTROL REGISTER (RA).



*DMA cycles will always end at a character fetch

FIGURE 15: CRT 9007 ATTRIBUTE ASSEMBLE TIMING (32 CHARACTERS PER DATA ROW)

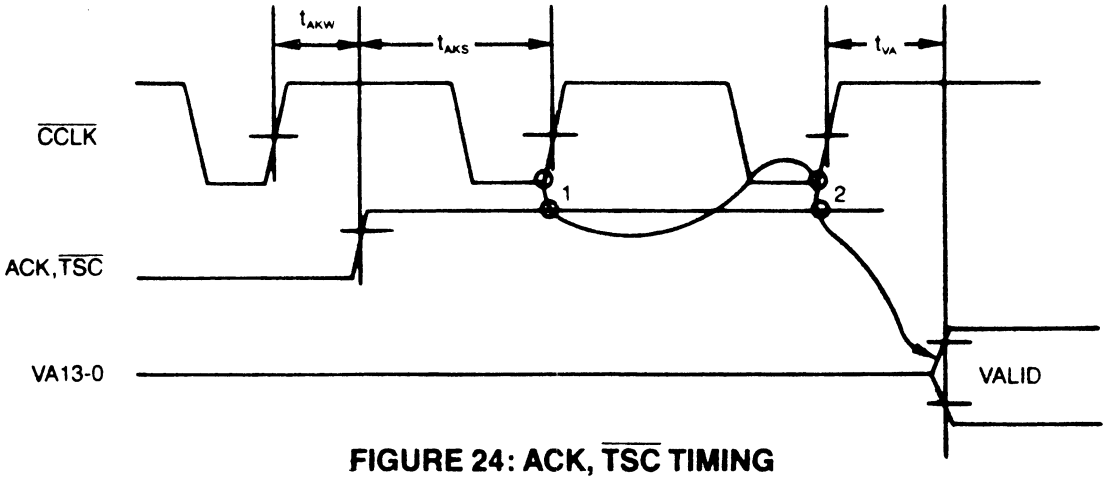


FIGURE 24: ACK, TSC TIMING

Row Table Addressing

In this addressing mode, each data row in video memory is designated by its own starting address. This provides greater flexibility with respect to screen operations than with other addressing schemes used by previous CRT controllers. The row table, which is a list of starting addresses for each data row, can be configured in one of 2 ways. The choice of row table format is highly dependent upon the particular application and the programmer's preference since each format allows full utilization of the CRT 9007 features.

Contiguous Row Table Format

In this format, the TABLE START REGISTER (RC and RD) points to the address where the row table begins. The contents of the first 2 locations define the starting address of the first data row. These 2 bytes define a 14 bit address where the first byte is the low order 8 bits and the second byte is the high order 6 bits. The 2 most significant bits of the second byte define double height/width characteristics to the current data row. The contents of the third and fourth locations define the address where the second data row begins. Figure 16 illustrates the contiguous row table organization in video memory.

Linked List Row Table Format

In this format the TABLE START REGISTER (RC and RD) points to the memory location which starts the entire addressing sequence into operation. The first byte read is the lower 8 bits and the second byte read is the upper 6 bits of the next data row's start address. The 2 most significant bits of the second byte define double height/width characteristics for the data row about to be read. The third, fourth, fifth, etc., bytes read are the first, second, third, etc., characters of the current data row. Figure 17 illustrates the linked list row table organization in video memory.

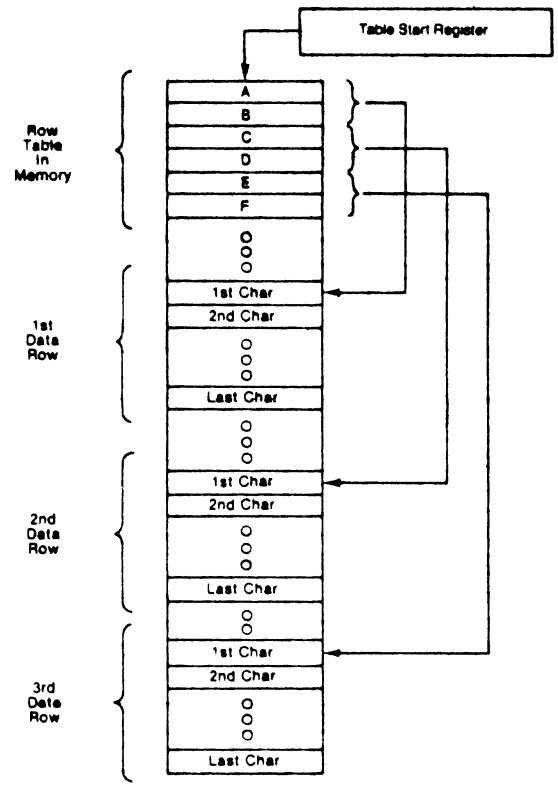


FIGURE 16:
CONTIGUOUS ROW TABLE ADDRESS FORMAT

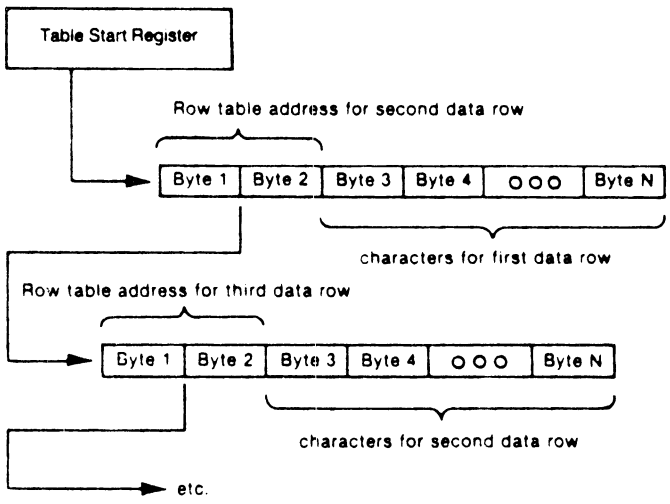


FIGURE 17: LINKED LIST ROW TABLE ADDRESS FORMAT

Sequential Addressing[1]

In this addressing mode, characters on the display screen are located in successive memory locations. The TABLE START REGISTER (RC and RD) points to the address of the first character of the first data row on the screen. In this mode the TABLE START REGISTER does not point to the start of a table but the start of the screen. As each character is read by the CRT 9007 for display refresh, the internal video address register is incremented by one to access the next character.

For more versatile systems operation in the sequential addressing mode, SEQUENTIAL BREAK REGISTER 1 (R10) and SEQUENTIAL BREAK REGISTER 2 (R12) may be used to define the data rows at which two additional

[1]SEQUENTIAL BREAK 2 is not functional in the repetitive memory addressing mode. It is fully functional in all other operation modes.

sequential display areas begin. Note that DATA ROW END REGISTER (R12) is defined as SEQUENTIAL BREAK REGISTER 2 (R12) for the sequential addressing mode only. The starting addresses for these two additional display areas are defined by AUXILIARY ADDRESS REGISTER 1 (RE and RF) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14). When the raster begins painting a data row equal to the number programmed in one of the sequential break registers, the CRT 9007 addresses the video memory sequentially starting with the address specified by the corresponding auxiliary address register. Figure 18 illustrates a display with 80 characters per data row having sequential breaks at data rows 3 and 6.

Using the sequential addressing mode with 2 breaks, it is possible to roll a portion of the screen and keep the rest of the screen stable. Double height/width characteristics can be attached to the 2 sequentially addressed screens defined by SEQUENTIAL BREAK REGISTERS 1 and 2 by using the 2 most significant bits of AUXILIARY ADDRESS REGISTERS 1 and 2. See the description of these 2 registers for their bit definition.

TABLE START REGISTER = 1000
AUXILIARY ADDRESS REGISTER 1 = 2000
AUXILIARY ADDRESS REGISTER 2 = 0800
SEQUENTIAL BREAK REGISTER 1 = 3
SEQUENTIAL BREAK REGISTER 2 = 6

Data Row	Address range	
0	1000 to 104 F	
1	1050 to 109F	
2	10A0 to 10EF	
3	2000 to 204F	(Break 1)
4	2050 to 209F	
5	20A0 to 20EF	
6	0800 to 084F	(Break 2)
7	0850 to 089F	
8	08A0 to 08EF	
	○	
	○	
	○	

Figure 18: Sequential Addressing Example With Two Breaks

Double Height/Width Operation

When double height width characters (2XH/2XW) are displayed, the following will occur:

1. the CRT 9007 will address half as many characters for each data row by incrementing its address every other character clock.
2. the high speed video shift register supplying serial video to the CRT must shift out dots at half frequency.
3. For double height, the scan line counter outputs (SL3-SL0 or $\overline{SLG}$, $\overline{SLD}$) are incremented every other scan line.

The CRT 9007 is informed of the double height or double width display modes via the 2 most significant bits of the row table address or the 2 most significant bits of the AUXILIARY ADDRESS registers depending on the selected addressing mode. In any case, once the information is obtained by the CRT 9007, it must initiate the 3 tasks listed above. Tasks 1 and 3 are performed as appropriate and task 2 is performed using the CURS output of the CRT 9007 during CBLANK (horizontal retrace) to signal the external logic that a change in the dot shift frequency is required. The exact time of activation and deactivation of the CURS signal during horizontal retrace is a function of addressing mode, operation mode and actual scan line number to be painted. Tables 1 and 2 show the cursor activation and deactivation times as a function of the buffer configuration and addressing mode for the top scan line of a new data row. Tables 1 and 2 assume a cursor skew of zero. A cursor skew will effect the cursor position during trace as well as retrace time. For all subsequent scan lines, the CURS signal is activated 3 $\overline{CCLK}$'s after VLT trailing edge and stays active for exactly 1 $\overline{CCLK}$ assuming no cursor skew. When the cursor is placed on a double height or double width data row, it will become active for 2 $\overline{CCLK}$'s to allow the cursor to be displayed as double width. If the cursor position is programmed to reside in the top half of a double height data row, it may become active for all scan lines in both the current and next data row to allow the cursor to be displayed as double height.

For row driven addressing, a particular data row or pair of data rows can appear in one of the following ways as a function of the two most significant bits of the row table address (bits 15 and 14).

—Single height, single width (Row table address bits 15, 14 = 00). The CRT 9007 will display the particular data row as single height, single width.

—Single height, double width (Row table address bits 15, 14 = 01). The CRT 9007 will display the particular data row as single height double width by accessing half as many characters as appear in a single width data row. The CURS signal becomes active during horizontal retrace in the manner described previously.

—Double height, double width top half (Row table address bits 15, 14 = 10). In addition to providing the special timing associated with single height double width data rows, the scan line counter is started from zero and incremented every other scan line until N scan lines are painted (N is the number of scan lines per single height data row). In this way, new dot information appears every other scan line and the top half of the data row appears in N scan lines.

—Double Height, Double Width Bottom Half (Row table address bits 15, 14 = 11)—Same as Double Height, Double Width Top except the scan line counter is started from N/2 (or (N-1)/2 if N is odd), and incremented every other scan line until N scan lines are painted. In single row buffer operation, a double height bottom data row can only stand alone during a smooth scroll operation; otherwise it is assumed to follow a double height top data row.

OPERATION MODE	ADDRESSING MODE	
	Row Driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Single row buffer	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Double row buffer	1 CCLK after high byte of row table read	1 CCLK after ACK leading edge

Table 1: Double Height/Width CURS activation for top scan line of new data row.

OPERATION MODE	ADDRESSING MODE	
	Row driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	at the leading edge of VLT	at the leading edge of VLT
Single row buffer	at the leading edge of VLT	at the leading edge of VLT
Double row buffer	1 CCLK after leading edge of CURS	1 CCLK after leading edge of CURS

Table 2: Double Height/Width CURS deactivation for top scan line of new data row.

PROCESSOR ADDRESSABLE REGISTERS

All CRT 9007 registers are selected by specifying the address on VA5-0 and asserting $\overline{CS}$. All 14 bit registers are written or read as two consecutive 8 bit registers addressed low byte first. Only the VERTICAL CURSOR REGISTER and the HORIZONTAL CURSOR REGISTER are read/write registers with 2 different addresses for read or write operations. The register address assigned to each register represents the actual address in hexadecimal form that must appear on VA5-0. Figure 2 illustrates all processor to CRT 9007 register timing. Tables 3a, 3b, and 3c summarize all register bits and provide register addresses.

HORIZONTAL TIMING REGISTERS

The following 4 registers define the horizontal timing parameters. Figure 19 relates the horizontal timing to these registers.

CHARACTERS PER HORIZONTAL PERIOD (R0)

This 8 bit write only register, programmed in units of character times, represents the total number of characters in the horizontal period (trace plus retrace time). This register is programmed with the binary number N where N is the total characters in the horizontal period. The horizontal period should not be programmed for less than 12 characters.

CHARACTERS PER DATA ROW (R1)

This 8 bit write only register, programmed in units of character times, represents the number of displayable characters during the horizontal trace interval. The difference R0 minus R1 represents the number of character times reserved for horizontal retrace. This register is programmed with the binary number (N-1) where N is the displayable characters per data row.

HORIZONTAL DELAY (R2)

This 8 bit write only register, programmed in units of character times, represents the time between the leading edge of horizontal sync and leading edge of VLT. This register is programmed with N where N represents the time of horizontal delay. By programming this time greater than the horizontal blank interval, one can obtain negative front porch (horizontal sync begins before the horizontal blank interval).

HORIZONTAL SYNC WIDTH (R3)

This 8 bit write only register defines the horizontal sync width in units of character times. The start of the sync pulse is defined by the HORIZONTAL DELAY REGISTER and the end is independent of the start of the active display time. This register is programmed with N where N is the horizontal sync width. However this register must be programmed less than or equal to [(A/2)-1] where A is the programmed contents of REGISTER 0 rounded to the smallest even integer.

VERTICAL TIMING REGISTERS

The following 5 registers define the vertical timing parameters. Figure 20 relates the vertical timing to these registers.

VERTICAL SYNC WIDTH (R4)

This 8 bit write only register defines the vertical sync width in units of horizontal periods. The start of this signal is defined by the delay register (R5) and the end is independent of the start of the active display time. This register is programmed with N where N is the vertical SYNC width.

VERTICAL DELAY (R5)

This 8 bit write only register, programmed in units of horizontal periods, represents the time between the leading edge of vertical sync and the leading edge of the first VLT after the vertical retrace interval. This register is programmed with (N+1) where N represents the time of the vertical delay.

VISIBLE DATA ROWS PER FRAME (R7)

This 8 bit write only register defines the number of data rows displayed on the screen. This register is programmed with (N-1) where N is the number of data rows displayed.

SCAN LINES PER DATA ROW (R8)

The 5 LSBs of this write only register define the number of scan lines per data row. These 5 bits are programmed with (N-1) where N is the number of scan lines per data row. When programming for scan lines per data row greater than 16, only the serial scan line pin option (SLD, $\overline{SLG}$) can be used.

SCAN LINES PER VERTICAL PERIOD (R8; R9)

Registers R9 and the 3 most significant bits of R8 define the number of scan lines for the entire frame. R8 contains the 3 most significant bits of the 11 bit programmed value and R9 contains the 8 least significant bits of the 11 bit programmed value. The 11 bits are programmed with N where N is the number of scan lines per frame. In the 2 interlace modes, the programmed value represents the number of scan lines per field.

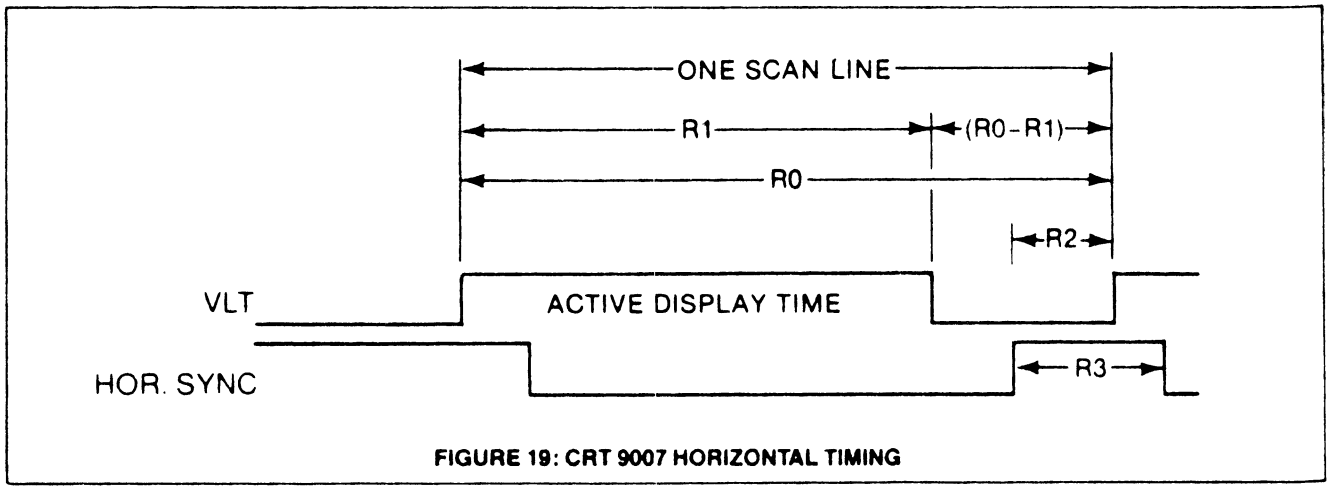


FIGURE 19: CRT 9007 HORIZONTAL TIMING

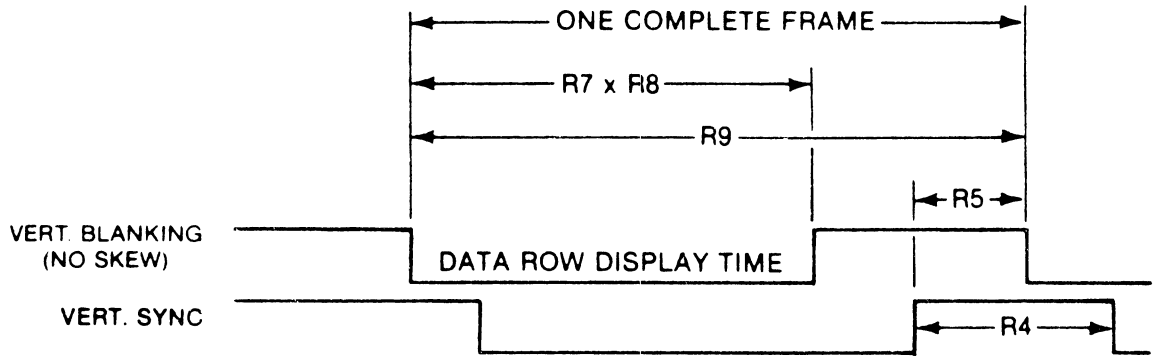


FIGURE 20: CRT 9007 VERTICAL TIMING

PIN CONFIGURATION/SKEW BITS REGISTER (R6)

This 8 bit write only register is used to select certain pin configurations and to skew (delay) the cursor and the blank signals independently with respect to the video signal sent to the monitor. The bits take on the following definition:

Bit 7, 6 (Pin Configuration)

These 2 bits, as illustrated in tables 4 and 5, define all pinout configurations as a function of double row buffer mode and non double row buffer mode. (The buffer mode is defined in the CONTROL REGISTER bits 3, 2, and 1.) The attribute assemble mode is assumed to be a double row buffer mode and obeys table 4.

Bits 5, 4, 3 (Cursor skew)

These three bits define the number of character clocks the cursor signal is skewed (delayed) from the VLT signal. The VLT signal is active for all characters within a data row and a non skewed cursor will always become active within the active VLT time at the designated position. The cursor can be skewed from 0 to 5 character clocks (Bits 5, 4 and 3 programmed from 000 to 101, bit 5 is the most significant bit; bit 3 is the least significant bit). For double height/width data rows, the cursor signal appearing during horizontal retrace is also skewed as programmed.

Bits 2, 1, 0 (Blank skew)

These three bits define the number of character clocks the horizontal blank component of the CBLANK signal is skewed (delayed) from the VLT signal. The edges of VLT will line up exactly with the edges of the horizontal component of the CBLANK signal if no skew is programmed. The CBLANK can be skewed from 0 to 5 character clocks (Bits 2, 1 and 0 programmed from 000 to 101, bit 2 is the most significant bit; bit 0 is the least significant bit).

REGISTER R6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	1	DMAR	WBEN	$\overline{SLG}$	SLD	$\overline{CSYNC}$	ACK
1	1	DMAR	WBEN	$\overline{SLG}$	SLD	LPSTB	ACK
0	0	NOT PERMITTED					
1	0	NOT PERMITTED					

Table 4: Pin configuration for double row buffer and attribute assemble modes.

REGISTER 6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	0	SL3	SL2	SL1	SL0	$\overline{CSYNC}$	$\overline{TSC}$
1	0	SL3	SL2	SL1	SL0	LPSTB	$\overline{TSC}$
1	1	VBLANK	$\overline{CSYNC}$	$\overline{SLG}$	SLD	LPSTB	$\overline{TSC}$
0	1	NOT PERMITTED					

Table 5: Pin configuration for Single Row Buffer and Repetitive Memory Addressing Modes.

DMA CONTROL REGISTER (RA)

This 8 bit write only register allows the user to set up a DMA burst count and delay as well as disable the DMA mechanism of the CRT 9007. The register bits have the following definition:

Bit 7 (DMA Disable)

A logic one will immediately force the CRT 9007 DMA request to the inactive level and the CRT 9007 address bus (VA13-VA0) will enter its high impedance state. After enabling the DMA mechanism by setting this bit to a logic zero, a start command must be issued (see START COMMAND, R15).

Bits 6, 5, 4 (DMA Burst Delay)

These 3 bits define the number of clock delays ($\overline{CCLK}$) between successive DMAR–ACK sequences. Bit 6 is the most and bit 4 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will delay for 4 (N + 1) clock cycles before initiating another DMA request. If 111 is programmed, however, this will result in a zero delay allowing all characters to be retrieved from video RAM in one DMA burst regardless of the value programmed for the DMA burst count.

Bits 3, 2, 1, 0 (DMA Burst Count)

These 4 bits define the number of DMA operations in one DMAR-ACK sequence. Bit 3 is the most and bit 0 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will produce 4 (N + 1) DMA cycles before relinquishing the bus. When programmed with 0000, the minimum DMA Burst will occur (4 × 1 = 4) and when programmed with 1111 the maximum DMA Burst will occur (4 × 16 = 64). When bits 6, 5, and 4 are programmed with 111, no DMA delay will occur and the Burst count will equal the number of programmed characters per data row as specified in R1. Refer to figures 9 and 15 which illustrate a DMA burst of 16 and a DMA delay of 8 for double row buffer and attribute assemble modes respectively. For single row buffer operation, no DMA delay is permitted and bits 6, 5, 4 must be programmed with 000.

CONTROL REGISTER (RB)

This 7 bit write only register controls certain frame operations as well as specifying the operation mode used. Internal to the CRT 9007, this register is double buffered. Changes in the register are reflected into the CRT 9007 at a particular time during vertical retrace. This allows the user to update the CONTROL REGISTER at any time without running the risk of destroying the frame or field currently being painted.

The bits take on the following definition:

Bit 6 (PB/$\overline{SS}$)

= 0; The smooth scroll mechanism is enabled permitting the SMOOTH SCROLL OFFSET REGISTER (R17) to be loaded in the scan line counter (SL3-0 or SLG, SLD signals) allowing for a scroll on the screen of a predetermined number of scan lines per frame or field. The starting and ending of the smooth scroll operation is defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

= 1; The page blank mechanism is enabled. The CBLANK signal is made active high for a continuous period of time starting and ending at the data row defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

Bits 5, 4 (Interlace)—these 2 bits define one of 3 displayed modes as illustrated in figure 21

= 00; Non interlaced display

= 10; Enhanced video interlace. This display mode will produce an interlaced frame with the same dot information painted in adjacent odd/even scan lines.

= 11; Normal video interlace. This display mode will produce an interlaced frame with odd scan lines of characters displayed in odd fields and even scan lines displayed in even fields. This mode can be used to allow the screen to show twice as many data rows at half the height since it effectively doubles the character density on the screen.

= 01; This combination is not permitted.

Bits 3, 2, 1 (Operation modes): These 3 bits define the various buffer configuration modes as follows:

= 000; (Repetitive memory addressing)—In this mode the address information (VA13-VA0) appears during every visible scan line and the address bus enters its high impedance state during all retrace intervals. When using a row driven addressing mode (linked list or contiguous), the address bus is in the high impedance state for all retrace intervals except the horizontal retrace interval prior to the top scan line of a new data row. This period can be distinguished from other retrace intervals because the $\overline{DRB}$ (data row boundary) signal is active.

= 001; (Double row buffer)—In this mode, the CRT 9007 will address a particular data row from video memory one data row prior to the time when it is displayed on the CRT. During vertical retrace, the first data row is retrieved and loaded into the double row buffer. At the next data row boundary (in this case at the end of vertical retrace), the first data row feeds the character generator while the second data row is retrieved from video memory. The address bus will enter its high impedance state in accordance with the DMA mechanism for address bus arbitration.

= 100; (Single row buffer)—In this mode, during the first scan line of each data row, the CRT 9007 will address video memory, load the buffer and feed the character generator at the painting rate of the CRT. If the CRT 9007 is used in a row driven addressing mode, it will drive the address bus during the retrace period prior to the first scan line of each data row in order to retrieve the row table address. It will automatically enter the high impedance state at the end of the first visible scan line of each data row. If the CRT 9007 is used in a sequential addressing mode, it will drive the address bus only during the visible line time of the first scan line of each data row.

= 111; (Attribute assemble)—In the attribute assemble mode, character data and attribute data are shared in consecutive alternating byte locations in memory. When the CRT 9007 reads an attribute byte, it loads it into its internal attribute latch. During the next memory access, a character byte is fetched. At this time the CRT 9007 isolates its bus from the main system bus and outputs the previously latched attribute. A WBEN signal is produced during every character byte fetch to allow the character and its associated attribute to be simultaneously latched into two double row buffers. This mode assumes that there exists twice as many byte locations as there are displayable character positions on the CRT. The first byte of every data row is assumed to be an attribute.

All other combinations of the CONTROL REGISTER bits 3, 2, 1 are not permitted.

Bit 0 ($\overline{2XC}$/1XC): This bit allows for either single or double height cursor display when the cursor is placed within a double height data row as follows:

= 1; (Single height cursor)—The CURS signal will appear during every scan line for single height data rows and will appear only during the top half or bottom half of a double height data row depending upon where the VERTICAL CURSOR REGISTER (R18, R38) defines the CURSOR data row.

= 0; (Double height cursor)—If the VERTICAL CURSOR REGISTER (R18, R38) places the cursor in the top half of a double height data row, the CURS signal will appear during every scan line of the top half (the current data row) and the bottom half (the next data row) of the double height data row. If the cursor is placed in the bottom half of a double height data row or if it is placed in a single height data row, the CURS signal will only appear during the one particular data row.

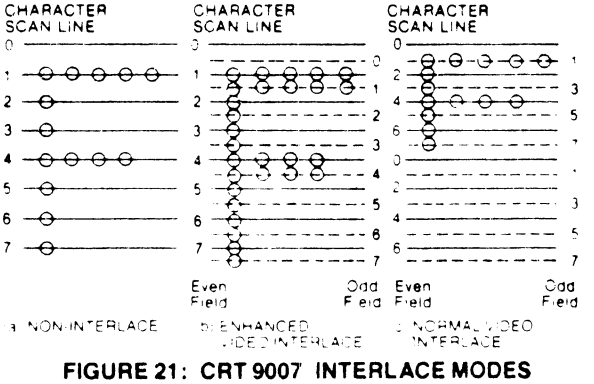


FIGURE 21: CRT 9007 INTERLACE MODES

TABLE START REGISTER (RC AND RD)

This 16 bit write only register contains a 14 bit address which is used in a variety of ways depending on the addressing mode chosen; the 2 remaining bits define the addressing mode. Register C contains the lower 8 bits of the 14 bit address. The 6 least significant bits of register D contain the upper 6 bits of the 14 bit address. The 2 most significant bits of register D define four addressing modes as follows:

Register D bits 7, 6:

= 00; (Sequential addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. 2 sequential breaks are allowed as defined by SEQUENTIAL BREAK 1 (R10) using AUXILIARY ADDRESS REGISTER 1 (RE and RF) and SEQUENTIAL BREAK 2 (R12) using AUXILIARY ADDRESS REGISTER 2 (R13 and R14).

= 01; (Sequential roll addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. SEQUENTIAL BREAK REGISTER 1 and AUXILIARY ADDRESS REGISTER 1 can be used to cause one sequential break as described in the sequential addressing mode. A second break in the sequential addressing can be defined by SEQUENTIAL BREAK REGISTER 2 (R12) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14) permitting up to 3 separate sequentially addressed screens to be painted.

= 10; (Contiguous row table mode)—The CRT 9007 will address video memory according to the contiguous row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define an address that points to the beginning of the contiguous row table.

= 11; (Linked list row table mode)—The CRT 9007 will address video memory according to the linked list row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define the address at which the second row table entry and the first data row reside.

AUXILIARY ADDRESS REGISTER 1 (RE and RF)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER F contain the upper order 6 bits of the 14 bit address and REGISTER E contains the 8 lower order bits of the 14 bit address. When the current data row equals the value programmed in SEQUENTIAL BREAK REGISTER 1 (R10) the remainder of the screen is addressed sequentially starting at the 14 bit address specified in this register. This sequential break overrides any row driven addressing mode used prior to the sequential break.

The 2 most significant bits of REGISTER F allow one to attach double height and or double width characteristics to every data row in this sequentially addressed area in the following way:

For Double row buffer or attribute assemble mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; even data rows are double height double width top half odd data rows are double height double width bottom half

= 11; odd data rows are double height double width top half even data rows are double height double width bottom half

For Single row buffer or repetitive memory addressing mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; odd data rows are double height double width top half even data rows are double height double width bottom half

= 11; even data rows are double height double width top half
odd data rows are double height double width bottom half

SEQUENTIAL BREAK REGISTER 1 (R10)

This 8 bit write only register defines the data row number in which a new sequential video address begins as specified by AUXILIARY ADDRESS REGISTER 1 (RE and RF). To disable the use of this break, the register should be loaded with a data row count greater than the number of displayable data rows on the screen.

DATA ROW START REGISTER (R11)

This 8 bit write only register defines the first data row number at which a page blank or smooth scroll operation will begin. Bit 6 of the CONTROL REGISTER determines if a page blank or smooth scroll operation will occur.

DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12)

This 8 bit write only register has a dual function depending on the addressing mode used. For row driven addressing (contiguous or linked list as specified by the 2 most significant bits of the TABLE START REGISTER) this register defines the data row number which ends either a page blank or smooth scroll operation. The row numerically one less than the row defined by this register is the last data row on which the page blank or smooth scroll will occur. To use the page blank feature to blank a portion of the screen that includes the last displayed data row, this register must be programmed to zero. For sequential addressing, this register can cause a break in the sequential addressing at the data row number specified and a new sequential addressing sequence begins at the address contained in AUXILIARY ADDRESS REGISTER 2.

AUXILIARY ADDRESS REGISTER 2 (R13 and R14)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER 14 contain the upper order 6 bits of the 14 bit address and REGISTER 13 contains the 8 lower order bits of the 14 bit address. In the row driven addressing mode, this register is automatically loaded by the CRT 9007 with the current table address. The two most significant bits of REGISTER 14 specify one of four combinations of row attributes (for example double height

double width) on a row by row basis. Refer to the section entitled Double Height/Double Width operation for the meaning of these 2 bits. In the sequential addressing mode, this register can be loaded by the processor with a 14 bit address and a 2 bit row attributes field. The bit positions are identical for the row driven addressing mode. When the current data row equals the value programmed in DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12), the remainder of the screen is addressed sequentially starting at the location specified by the programmed 14 bit address. The 2 most significant bits of register 14 allow one to attach double height and or double width characteristics to every data row in this sequentially addressed area. The bit definitions take on the same meaning as the 2 most significant bits of AUXILIARY ADDRESS REGISTER 1 and affect the display in an identical manner.

START COMMAND (R15)

After all vital screen parameters are loaded, a START command can be initiated by addressing this dummy register location within the CRT 9007. A START command must be issued after the DMA mechanism is enabled (DMA CONTROL REGISTER bit 7).

RESET COMMAND (R16)

The CRT 9007 can be reset via software by addressing this dummy location. Activation of the $\overline{RST}$ input pin or initiating this software command will effect the CRT 9007 in an identical manner. The reset state of the CRT 9007 is defined as follows:

CRT 9007 outputs	Reset state
VA13-0	High impedance
VD7-0	High impedance
$\overline{HS}$	High
$\overline{VS}$	High
CBLANK	High
CURS	Low
$\overline{VLT}$	Low
$\overline{DRB}$	High
INT	Low
Pin 28	Low
Pin 29	Low
Pin 30	Low
Pin 31	Low
Pin 32	Low

SMOOTH SCROLL OFFSET REGISTER (R17)

This register is loaded with the scan line offset number to allow a smooth scroll operation to occur. The offset register causes the scan line counter output of the CRT 9007 to start at the programmed value rather than zero for the data row that starts the smooth scroll interval. The start is specified in the DATA ROW START REGISTER (R11). Typically, this register is updated every frame and it ranges from zero (no offset) to a maximum of the programmed scan lines per data row (maximum offset). For example, if 12 scan lines per data row are programmed (scan line 0 to scan line 11) an offset of zero will cause an unscrolled display. An offset of one will cause a display starting at scan line 1 and ending at scan line 11 (eleven scan lines total). An offset of eleven will cause a display starting at scan line eleven.

The next scan line will be zero, starting the subsequent data row. To allow smooth scroll of double height rows, the programmed range of the register is from zero to twice the programmed scan lines per data row. Whenever the offset register if greater than the programmed scan lines per data row, bit 7 of the register must be set to a logic 1 (offset overflow). It must be set to a logic zero at all other times. The 6 bit offset value occupies bits 6 through 1. Bit 0 must always be programmed with a logic zero. By setting the offset overflow (bit 7) to a logic 1, it is possible to have the bottom half of a double height data row stand alone in Single Row Buffer Mode by programming the scrolled data row as double height top half and loading R17 with the proper value.

VERTICAL CURSOR REGISTER (R18 or R38)

This 8 bit read/write register specifies the data row in which the cursor appears. To write into this register it is addressed as R18 and to read from this register it is addressed as R38.

HORIZONTAL CURSOR REGISTER (R19 or R39)

This 8 bit read/write register specifies the character position in which the cursor appears. To write into this register it is addressed as R19 and to read from this register it is addressed as R39.

It should be noted that the vertical and horizontal cursor is programmed in an X-Y format with respect to the screen and not dependant upon a particular location in video memory. The cursor will remain stationary during all scroll operations.

INTERRUPT ENABLE REGISTER (R1A)

This 3 bit write only register allows each of the three CRT 9007 interrupt conditions to be individually enabled or disabled according to the following definition:

Bit 6 (Vertical retrace interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when a vertical retrace (i.e., the start of the vertical blanking interval) begins.

Bit 5 (Light pen interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when the LIGHT PEN REGISTER (R3B, R3C) captures an X-Y coordinate. This interrupt, which occurs at the beginning of vertical retrace, reflects the occurrence of a LPSTB input on the frame or field just painted. This interrupt need not be enabled when other CRT 9007 interrupt conditions are enabled since the STATUS REGISTER (R3A) will flag the occurance of a light pen update and servicing can be done off of other interrupts.

Bit 0 (Frame timer)—This bit, when set to a logic one, allows the CRT 9007 to activate the INT signal once every frame or field at a time when a potential smooth scroll update may occur. In this way the user can use the frame timer interrupt as both a real time clock and can service smooth scroll updates and other frame oriented operations by using the appropriate status bits. This interrupt will occur after the last row table entry is read by the CRT 9007. In single row buffer operation, this will occur one data row before the start of vertical retrace. In double row buffer operation, this will occur two data rows before the start of vertical retrace.

STATUS REGISTER (R3A)

This 5 bit register flags the various conditions that can potentially cause an interrupt regardless of whether the corresponding condition is enabled for interrupt. In this way some or all of the conditions can be reported to the processor via the STATUS REGISTER. If some of the conditions are enabled for interrupt, the processor, in response to an interrupt, simply has to read the STATUS REGISTER to determine the cause of the interrupt. The bit definition of the STATUS REGISTER is as follows:

Bit 7 (Interrupt Pending)—This bit will set when any other status bit, having its corresponding interrupt enabled, experiences a 0 to 1 transition. In this manner, when the processor services a potential CRT 9007 interrupt, it only has to test the interrupt pending bit to determine if the CRT 9007 caused the interrupt. If it did, the individual bits can then be tested to determine the details of the CRT 9007 interrupt. Any noninterruptable status change (corresponding interrupt enable bit reset to a logic 0) will not be reflected in the interrupt pending bit and must be polled by

the processor in order to provide service. The interrupt pending bit is reset when the status register is read. All other bits except Light Pen Update are reset to a logic 0 at the end of the vertical retrace interval. The light pen update bit is reset to a logic 0 when the HORIZONTAL LIGHT PEN REGISTER is read.

Bit 6 (Vertical Retrace)—A logic 1 indicates that a vertical retrace interval has begun.

Bit 5 (Light Pen Update)—A logic 1 indicates that a new coordinate has been strobed into the LIGHT PEN REGISTER. It is reset to a logic zero when the HORIZONTAL LIGHT PEN REGISTER is read. The light pen coordinates may have to be modified via software depending on light pen characteristics.

Bit 2 (odd/even)—For a normal video interlaced display, this bit is a logic 1 when the field about be painted is an odd field and is a logic zero when the field about be painted is an even field.

Bit 0 (Frame timer occurred)—This bit becomes a logic 1 either one or two data rows before the start of vertical retrace. Since this bit is set when the CRT has finished reading the row table for the frame or field just painted, it permits row table manipulation to start at the earliest possible time.

VERTICAL LIGHT PEN REGISTER (R3B)

This 8 bit read only register contains the vertical coordinate captured at the time the CRT 9007 received a light pen strobe signal (LPSTB).

HORIZONTAL LIGHT PEN REGISTER (R3C)

This 8 bit read only register contains the horizontal coordinate captured at the time the CRT 9007 received a light pen strobe signal. When a coordinate is captured, the appropriate status bit is set and further transitions on LPSTB are ignored until this register is read. The reading of this register will reset the light pen status bit in the STATUS REGISTER. The captured coordinate may have to be modified in software to allow for light pen response.

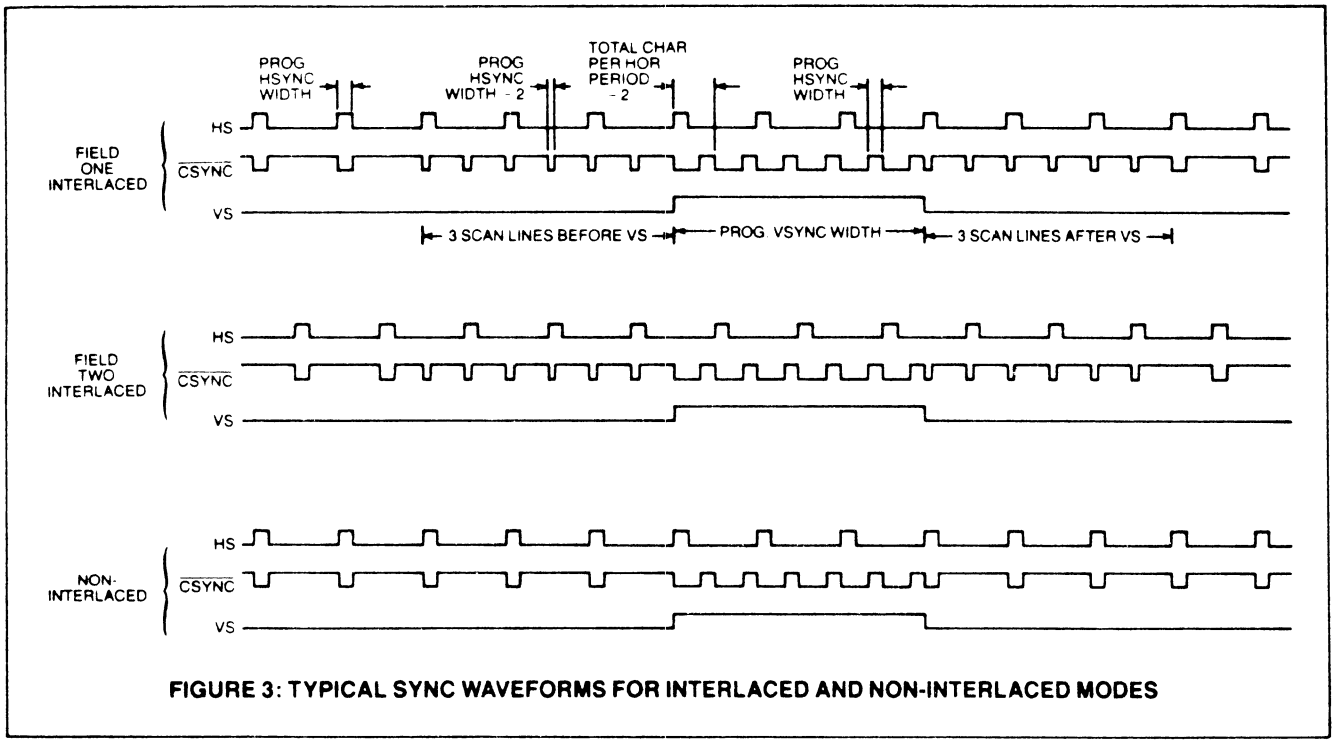


FIGURE 3: TYPICAL SYNC WAVEFORMS FOR INTERLACED AND NON-INTERLACED MODES

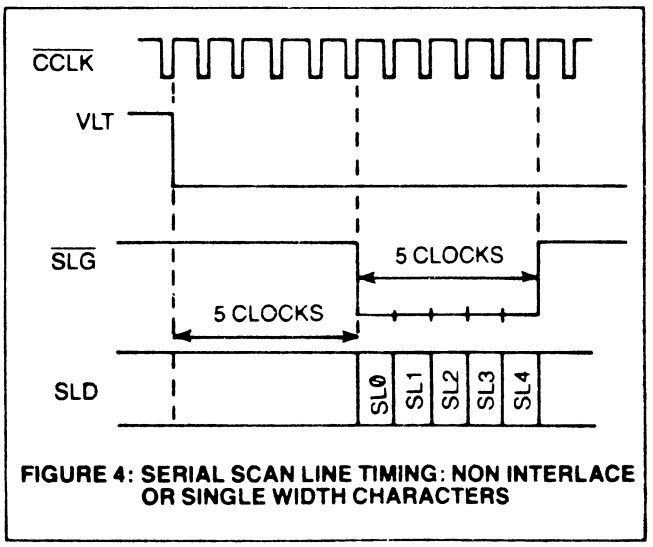


FIGURE 4: SERIAL SCAN LINE TIMING: NON INTERLACE OR SINGLE WIDTH CHARACTERS

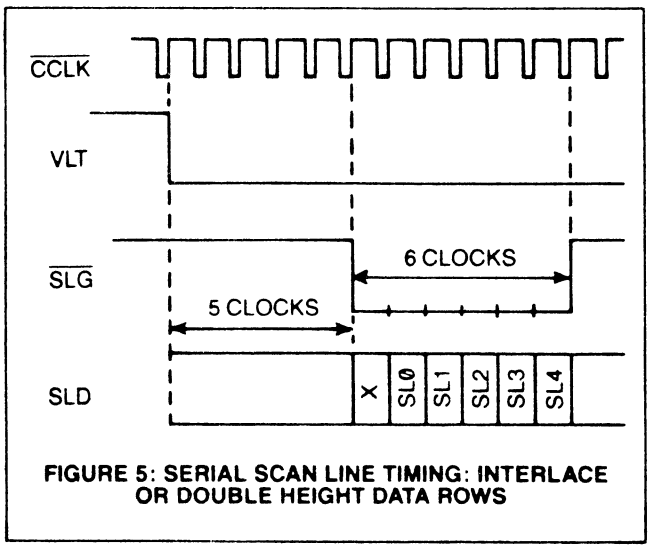


FIGURE 5: SERIAL SCAN LINE TIMING: INTERLACE OR DOUBLE HEIGHT DATA ROWS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH1}	High	2.0			V	all inputs except $\overline{CCLK}$
V_{IH2}	High	4.3			V	$\overline{CCLK}$ input; see note 4
	Output voltage					
V_{OL}	Low			0.4	V	I_{OL} = 1.6 mA
V_{OH}	High	2.4			V	I_{OH} = 100μA
	Input leakage current					
I_{L1}				10	μA	$0 \leq V_{IN} \leq 3.5V$; excluding $\overline{CCLK}$
I_{L2}				50	μA	V_{IN} = 5V; for $\overline{CCLK}$
I_{L3}				−200	μA	V_{IN} = 0V; for $\overline{CCLK}$
	Input capacitance					
C_{IN1}			10	15	pF	all inputs except $\overline{CCLK}$ at 1 MHZ
C_{IN2}			25	50	pF	$\overline{CCLK}$ input at 1 MHZ
	Power supply current					
I_{CC}			100	170	mA	

AC ELECTRICAL CHARACTERISTICS[3] $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Clock					
t_{CY}	clock period	330		1200	ns	for double row buffer or attribute assemble
		300		1200	ns	for all other operation modes
t_{CKL}	clock low	90			ns	
t_{CKH}	clock high	150			ns	
t_{CKR}	clock rise time			15	ns	measured from 0.8V to 3.5V level
t_{CKF}	clock fall time			10	ns	measured from 90% to 10% points
	Output delay[1]					
t_{D1}				150	ns	
t_{D2}				150	ns	
t_{D3}				150	ns	
t_{D4}				150	ns	
t_{VA}		25		115	ns	measured to the 2.3V or 0.5V level on VA13-VA0
t_{DSL}				500	ns	
t_{D5}				185	ns	
t_{D6}				185	ns	
t_{DSY}				185	ns	
t_{VDS}		50			ns	valid for loading auxiliary address register 2 or the attribute latch
t_{VDH}		10			ns	
t_{VD0}				185	ns	C_L = 50pF
t_{SLG}				185	ns	
t_{SLD}				185	ns	
t_{D7}				240	ns	cursor skew of zero
t_{D7}				185	ns	cursor skew of one through five
t_{D8}				300	ns	
	Processor Read write[2]					
t_{AS}		110			ns	
t_{AH}		0			ns	
t_{PW}		165			ns	
t_{CSH}		650			ns	
t_{PDS}		100			ns	
t_{PDH}		0			ns	
t_{PDA}				140	ns	
t_{PDO}		10		85	ns	
t_{IRR}				400	ns	
	Miscellaneous timing					
t_{AKS}		25		115	ns	measured from the 0.4V level of ACK or $\overline{TSC}$ falling edge
t_{RW}		$4t_{CY}$			ns	measured from the 0.4V level falling edge to 0.4V level rising edge
t_{AKW}		50			ns	see figure 24
t_{AKS}		50			ns	see figure 24

NOTE:
1. Timing measured from the 1.5V level of the rising edge of $\overline{CCLK}$ to the 2.4V (high) or 0.4V (low) voltage level of the ouput unless otherwise noted.
2. Reference points are 2.4V high and 0.4V low.
3. Loading on all outputs is 30 pF except where noted.
4. This level must be reached before the next falling edge of $\overline{CCLK}$.

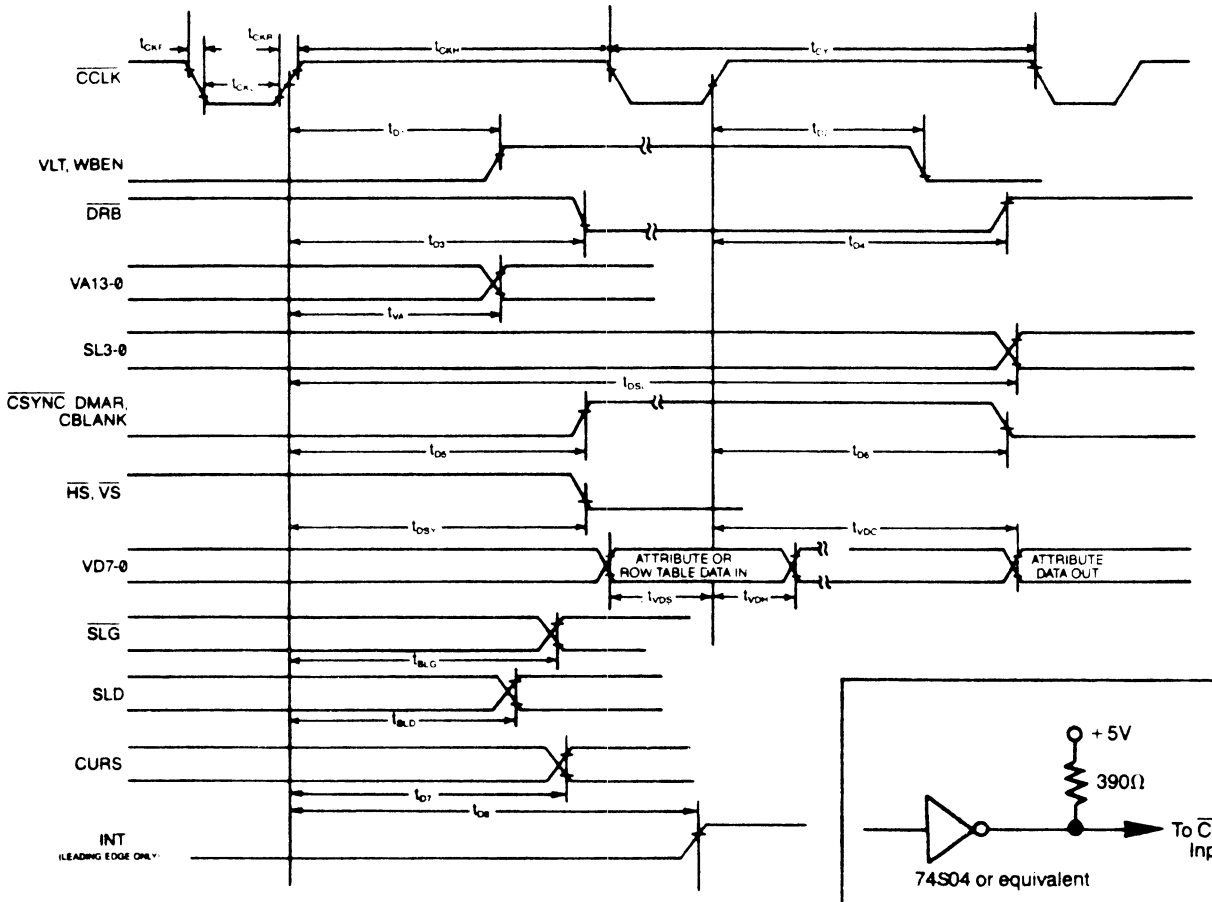


FIGURE 22: CRT 9007 TIMING PARAMETERS: OUTPUT SIGNALS

FIGURE 25: RECOMMENDED CCLK DRIVER CIRCUIT

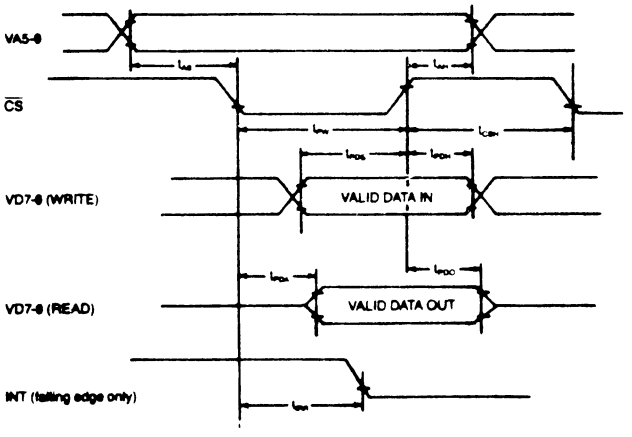
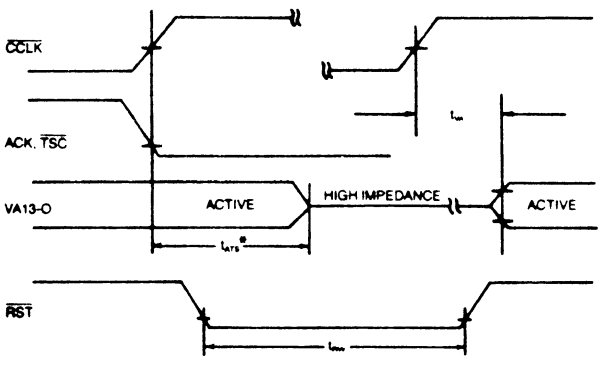


FIGURE 2: CRT 9007 PROCESSOR READ AND WRITE TIMING PARAMETERS



* t_{ATS} is controlled directly from ACK or TSC or from the particular CCLK that ends a DMA burst cycle

FIGURE 23: CRT 9007 MISCELLANEOUS TIMING PARAMETERS

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	0	0	0	0	MSB	CHARACTERS PER HORIZONTAL PERIOD						LSB	R0
WRITE	0	0	0	0	0	1	MSB	CHARACTERS PER DATA ROW						LSB	R1
WRITE	0	0	0	0	1	0	MSB	HORIZONTAL DELAY						LSB	R2
WRITE	0	0	0	0	1	1	MSB	HORIZONTAL SYNC WIDTH						LSB	R3
WRITE	0	0	0	1	0	0	MSB	VERTICAL SYNC WIDTH						LSB	R4
WRITE	0	0	0	1	0	1	MSB	VERTICAL DELAY						LSB	R5
WRITE	0	0	0	1	1	0	PIN CONFIG-URATION	CURSOR SKEW MSB			LSB	BLANK SKEW MSB		LSB	R6
WRITE	0	0	0	1	1	1	MSB	VISIBLE DATA ROWS PER FRAME						LSB	R7
WRITE	0	0	1	0	0	0	SCAN LINES FRAME (B10))	(B8)	MSB	SCAN LINES PER DATA ROW				LSB	R8
WRITE	0	0	1	0	0	1	(B7)	SCAN LINES PER FRAME						LSB (B0)	R9

Table 3a: CRT 9007 Screen Format Registers

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	1	0	1	0	DMA DIS-ABLE	DMA BURST DELAY MSBA		LSB	DMA BURST COUNT MSB			LSB	RA
WRITE	0	0	1	0	1	1	X	PB/SS	INTERLACE MODES		OPERATION MODES			2XC/1XC	RB
WRITE	0	0	1	1	0	0	MSB	TABLE START REGISTER (LS BYTE)						LSB	RC
WRITE	0	0	1	1	0	1	ADDRESS MODE	TABLE STRT REGISTER (MS BYTE) MSB						LSB	RD
WRITE	0	0	1	1	1	0	MSB	AUXILIARY ADDRESS REGISTER 1 (LS BYTE)						LSB	RE
WRITE	0	0	1	1	1	1	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 1 (MS BYTE) MSB						LSB	RF
WRITE	0	1	0	0	0	0	MSB	SEQUENTIAL BREAK REGISTER 1						LSB	R10
WRITE	0	1	0	0	0	1	MSB	DATA ROW START REGISTER						LSB	R11
WRITE	0	1	0	0	1	0	MSB	DATA ROW END/SEQUENTIAL BREAK REGISTER 2						LSB	R12
WRITE	0	1	0	0	1	1	MSB	AUXILIARY ADDRESS REGISTER 2 (LS BYTE)						LSB	R13
WRITE	0	1	0	1	0	0	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 2 (MS BYTE) MSB						LSB	R14

Table 3b: Control and Memory Address Registers

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
READ OR WRITE	0	1	0	1	0	1	START COMMAND								R15
READ OR WRITE	0	1	0	1	1	0	RESET COMMAND								R16
WRITE	0	1	0	1	1	1	OFFSET OVER-FLOW	OFFSET VALUE MSB					LSB	0	R17
WRITE	0	1	1	0	0	0	MSB	VERTICAL CURSOR REGISTER (ROW COORD)						LSB	R18 or R38
READ	1	1	1	0	0	0									
WRITE	0	1	1	0	0	1	MSB	HORIZONTAL CURSOR REGISTER (COL COORD)						LSB	R19 or R39
READ	1	1	1	0	0	1									
WRITE	0	1	1	0	1	0	X	VER-TICAL RE-TRACE	INTERRUPT ENABLE REGISTER LIGHT PEN	X	X	X	X	FRAME TIMER	R1A
READ	1	1	1	0	1	0	INT PEND-ING	VER-TICAL RE-TRACE	LIGHT PEN	STATUS REGISTER			ODD/ EVEN	X	FRAME TIMER	R3A
READ	1	1	1	0	1	1	MSB	VERTICAL LIGHT PEN REGISTER (ROW COORD)						LSB	R3B
READ	1	1	1	1	0	0	MSB	HORIZONTAL LIGHT PEN REGISTER (COL COORD)						LSB	R3C

Table 3c: Cursor, Light Pen, Offset, and Status Registers

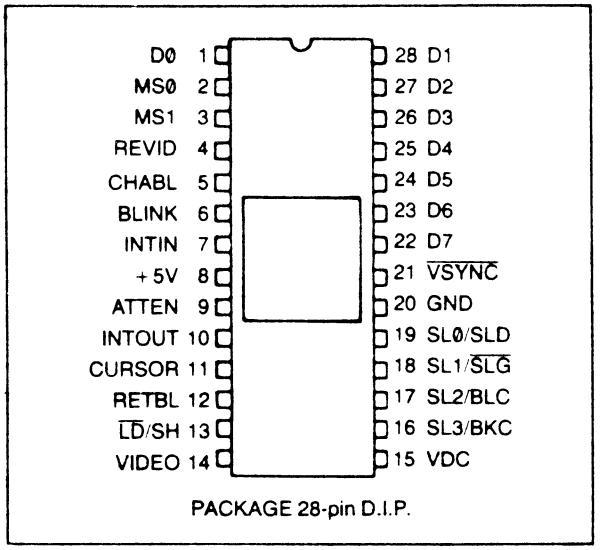
CRT 9021A
CRT 9021B
μPC FAMILY

CRT Video Attributes Controller
VAC

FEATURES

- ☐ On chip video shift register
  Maximum shift register frequency
  CRT 9021A 30 MHz
  CRT 9021B 28.5 MHz
- ☐ On chip attributes logic
  Reverse video
  Character blank
  Character blink
  Underline
  Full/half intensity
- ☐ Four modes of operation
  Wide graphics
  Thin graphics
  Character mode without underline
  Character mode with underline
- ☐ On Chip logic for double height/double width characters
- ☐ Accepts scan line information in parallel or serial format
- ☐ Four cursor modes dynamically selectable via 2 input pins
  Underline
  Blinking underline
  Reverse video
  Blinking reverse video
- ☐ Programmable character blink rate

PIN CONFIGURATION



PACKAGE 28-pin D.I.P.

- ☐ Programmable cursor blink rate
- ☐ On chip data and attribute latches
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS n-Channel silicon gate COPLAMOS® process
- ☐ Compatible with CRT 5037 VTAC®; CRT 9007 VPAC™

GENERAL DESCRIPTION

The SMC CRT 9021 Video Attributes Controller (VAC) is an n-channel COPLAMOS MOS/LSI device containing Graphics logic, attributes logic, data and attributes latches, cursor control, and a high speed video shift register. The CRT 9021, a character generator ROM and a CRT controller such as the CRT 9007 provide all of the major circuitry for the display portion of a CRT video terminal.

The CRT 9021 serial video output may be connected directly to a CRT monitor's video input. The maximum video shift register frequency of 28.5 MHz or 30 MHz allows for CRT displays of up to 132 characters per data row.

The CRT 9021 attributes include: reverse video, underline, character blank, character blink, and full/half intensity selection. In addition, when used in conjunction with the CRT 9007 VPAC,™ the CRT 9021 will provide double height or double width characters.

Four programmable cursor modes are provided on the CRT 9021. They are: underline, blinking underline, reverse video character block, and blinking reverse video character block. When used in the serial scan line input mode, the cursor mode may be selected via two input pins. When used in the parallel scan line input mode, the cursor mode is a mask program option and is fixed at the time of manufacture.

Two graphics modes are provided. In the wide graphics mode, the CRT 9021 produces a graphic entity the size of the character block. The graphic entity contains eight parts, each of which is associated with one bit of the input byte, thereby providing 256 unique graphic symbols. The thin graphics mode enables the user to create thin line drawings and forms.

In both graphics modes, continuous horizontal and vertical lines may be drawn. Additional flexibility is provided by allowing the mask programming of the placement and dimensions of the blocks or lines within a character block. In the thin graphics mode, mask programming allows serrated horizontal or vertical lines.

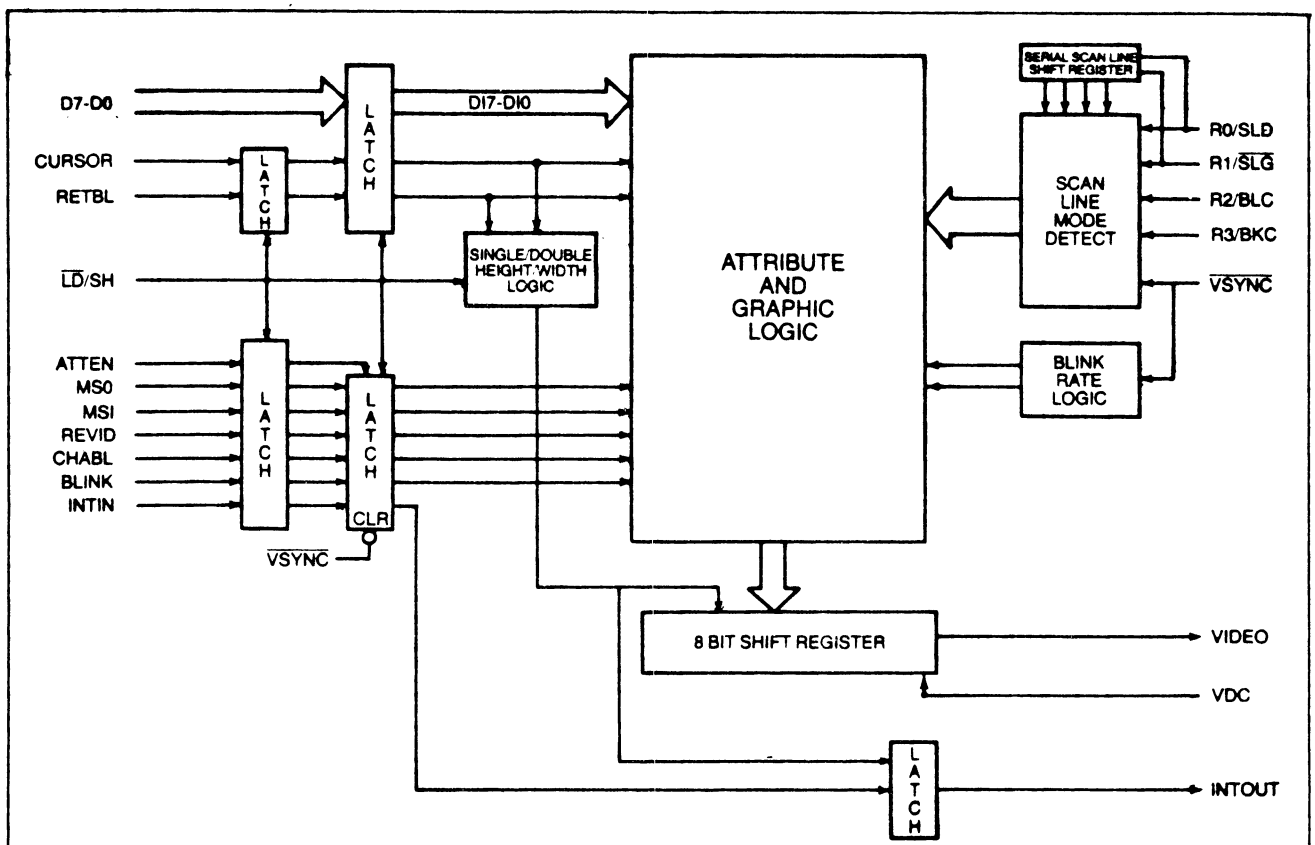


FIGURE 1: CRT 9021 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1, 28, 27, 26, 25, 24, 23, 22	Data	D7-D0	In the character mode, the data on these inputs is passed through the Attributes logic into the 8 bit high speed video shift register. The binary information on D7 will be the first bit output after the LD/SH input goes low In the thin or wide graphics mode these 8 inputs will individually control the on/off condition of the particular portion of the character block or line drawing. Figures 2 and 3 illustrate the wide and thin graphics modes respectively and their relationships to D7-D0
2 3	Mode Select 0 Mode Select 1	MS0 MS1	These 2 inputs define the four modes of operation of the CRT 9021 as follows: MS1, MS0 = 00; Wide graphics mode = 10; Thin graphics mode = 01; Character mode without underline = 11; Character mode with underline See section entitled Display Modes for details.
4	Reverse Video	REVID	When this input and Retrace Blank (RETBL) are both low, data from the Attributes and Graphics logic is presented directly to the video shift register. When this input is high and RETBL is low, the Attribute and Graphics logic will invert the data before presenting it to the video shift register.
5	Character blank	CHABL	When this input is high, the parallel inputs to the video shift register are all set low (or high depending on the state of REVID) thus providing a constant video level for the entire length of the character block.
6	Blink	BLINK	When this input is high and both the RETBL and CHABL inputs are low, the character will blink at the programmed character blink rate. Blinking is accomplished by causing the video to go to the background level during the "off" portion of the Character Blink cycle. This video level may be either the white or black level depending on state of REVID. The duty cycle for the character blink is 75:25 (on:off). This input is ignored if it coincides with the CURSOR input and the cursor is formatted to blink.
7	Intensity In	INTIN	The INTIN input along with the INTOUT output provides a user controlled general purpose attribute. Data input to INTIN will appear at INTOUT with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to raise or lower the voltage level of the video output to produce such attributes as "half intensity" or "intensity".

DESCRIPTION OF PIN FUNCTIONS CONT'D

PIN NO.	NAME	SYMBOL	FUNCTION
8	Supply Voltage	+5V	+5 volt power supply
9	Attribute Enable	ATTEN	When this input is high, the internal attribute latch is updated at the positive going edge of the LD/SH input with data appearing on the REVID, CHABL, MS1, MS0, BLINK and INTIN inputs. By selectively bringing this input high, the user will update the attribute only at specific character times. all subsequent characters will carry with them the attributes last updated thus allowing "field" or "embedded" attributes. When using a wide video memory where attribute bits are attached to every character, the internal attribute latch may be updated at each character by tieing this input high (thus allowing for "invisible" attributes).
10	Intensity Out	INTOUT	This output is used in conjunction with the INTIN input to provide a three character pipeline delay to allow for general purpose attributes (such as intensity) to be implemented. See INTIN (pin 7).
11	Cursor	CURSOR	When this input is high and RETBL is low, the programmed cursor format will be displayed. When this input is high, and RETBL is high, the CRT 9021 enters the double width mode. See section entitled cursor formats for details.
12	Retrace Blank	RETBL	When this input is high, the parallel inputs to the video shift register are unconditionally cleared to all zeros and loaded on the next LD/SH pulse. This forces the VIDEO output to a low voltage level, independent of all attributes, for blanking the CRT during horizontal and vertical retrace time.
13	Load/Shift	LD/SH	The 8 bit video shift register parallel-in load or serial-out shift operation is established by the state of this input. When high, this input enables the shift register for serial shifting with each video dot clock pulse (VDC input). When low, the video shift register is parallel loaded on the next video dot clock pulse and all data and attributes are moved to the next position in the internal pipeline. In addition, input data and attributes are latched on the positive transition of LD/SH.
14	Video	VIDEO	The Video output provides the serial dot stream to the CRT. Video is shifted out on the rising edge of the video dot clock VDC. The timing of the LD/SH input will determine the number of backfill dots. See figure 5.
15	Video Dot Clock	VDC	This input clock controls the rate at which video is shifted out on the VIDEO output.
16	Scan line 3/Block Cursor	SL3/BKC	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the most significant bit of the binary scan line row address. *Serial scan line mode*—This input controls the cursor's physical dimensions. If high the cursor will appear as a reverse video block (the entire character cell will be displayed in reverse video). If low, the cursor will appear as an underline on the scan line(s) programmed.
17	Scan line 2/Blink Cursor	SL2/BLC	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the second most significant bit of the binary scan line row address. *Serial scan line mode*—This input if low, will cause the cursor to alternate between normal and reverse video at the programmed cursor blink rate. The duty cycle for the cursor blink is 50/50 (on/off). If this input is high, the cursor will be non-blinking.
18	Scan Line 1/Scan Line Gate	SL1/SLG	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the next to the least significant bit of the binary scan line row address. *Serial scan line mode*—This input will be low for 5 or 6 LD/SH pulses to allow the scan line information to be serially shifted into the serial scan line shift register. If this signal is low for 7 or more LD/SH pulses, the CRT 9021 will assume the parallel input scan line row address mode.
19	Scan line 0/Scan Line data	SL0/SLD	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. Refer to figure 6. *Parallel scan line mode*—This input is the least significant bit of the binary scan line row address. *Serial scan line mode*—This input will present the scan line information in serial form (least significant bit first) to the CRT 9021 and permits the proper scan line information to enter the serial scan line shift register during the LD/SH pulses framed by SLG (pin 18).
20	Ground	GND	Ground
21	Vertical Sync	VSYNC	This input is typically connected to the vertical sync output of the CRT controller and is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will always be twice the character blank rate (75/25 duty cycle). In addition, the internal attributes are reset when this input is low. The VSYNC input is also used to determine the scan line mode (parallel or serial) used. See the section "Scan Line Input Modes".

ATTRIBUTES FUNCTION

Retrace Blank —The RETBL input causes the VIDEO to go to the zero (black) level regardless of the state of all other inputs.

Reverse Video —The REVID input causes inverted data to be loaded into the video shift register.

Character Blank —The CHABL input forces the video to go to the current background level as defined by Reverse Video.

Underline —MS1, MSØ = 1, 1 forces the video to go to the inverse of the background level for the scan line(s) programmed for underline.

Blink —The BLINK input will cause characters to blink by forcing the video to the background level 25% of the time and allowing the normal video for 75% of the time. When the cursor is programmed to blink (not controlled by the BLINK input), the video alternates from normal to reverse video at 50% duty cycle. The cursor blink rate always overrides the character blink rate when they both appear at the same character position.

Intensity (Half Intensity) —The INTIN input and the INTOUT output allow an intensity (or half intensity) attribute to be carried through the pipeline of the CRT 9021. An external mixer can be used to combine VIDEO and INTOUT to create the desired video level. See figure 8.

Table 1 illustrates the effect of the REVID, CHABL, UNDLN attributes as a function of the cursor format and the CURSOR and RETBL inputs.

TABLE 1: CRT 9021 ATTRIBUTE COMBINATIONS

CURSOR FORMAT	CRT 9021 INPUTS					VIDEO SHIFT REGISTER LOADED WITH:	
	RETBL	CURSOR	REVID	CHABL	UNDLN		
X	1	X	X	X	X	all zero's	
	0	0	0	0	0	data	
	0	0	0	0	1	One's for selected scan line(s). Data for all other scan lines.	
	0	0	0	1	X	All zero's	
	0	0	1	0	0	data	
	0	0	1	0	1	Zero's for selected scan line(s). data for all other scan lines	
	0	0	1	1	X	One's for all scan lines.	
UNDERLINE[2]	0	1	0	0	X[1]	One's for selected scan line(s) for cursor; data for all other scan lines	
	0	1	0	1	X[1]	One's for selected scan line(s) for cursor; zero's for all other scan lines	
	0	1	1	0	X[1]	Zero's for selected scan line(s) for cursor; Data for all other scan lines	
	0	1	1	1	X[1]	Zero's for selected scan line(s) for cursor; one's for all other scan lines	
BLINKING[3] UNDERLINE[2]	0	1	0	0	X[1]	One's for selected scan line(s) blinking; Data for all other scan lines	
	0	1	0	1	X[1]	One's for selected scan line(s) blinking; zero's for all other scan lines	
	0	1	1	0	X[1]	Zero's for selected scan line(s) blinking; Data for all other scan lines	
	0	1	1	1	X[1]	Zero's for selected scan line(s) blinking; one's for all other scan lines	
REVID BLOCK	0	1	0	0	0	Data for all scan lines	
	0	1	0	0	1	Zero's for selected scan line(s) for underline; data for all other scan lines	
	0	1	0	1	X	One's for all scan lines.	
	0	1	1	0	0	Data for all scan lines	
	0	1	1	0	1	One's for selected scan line(s) for underline, data for all other scan lines.	
	0	1	1	1	X	Zero's for all scan lines	
BLINKING[3] REVID BLOCK	0	1	0	0	0	On: Data for all scan lines	Off: Data for all scan lines
	0	1	0	0	1	Zero's for selected scan line(s) for underline. Data for all other scan lines	One's for selected scan line(s) for underline. Data for all other scan lines.
	0	1	0	1	X	One's for all scan lines.	Zero's for all scan lines.
	0	1	1	0	0	Data for all scan lines	Data for all scan lines
	0	1	1	0	1	One's for selected scan line(s). Data for all other scan lines.	Zero's for selected scan line(s). Data for all other scan lines
	0	1	1	1	X	Zero's for all scan lines	One's for all scan lines.

1 - if the programmed scan line(s) for cursor and underline coincide, the cursor takes precedence, otherwise both are displayed
2 - at programmed scan line(s) for underline
3 - at cursor blink rate
Note—cursor blink rate overrides character blink rate

DISPLAY MODES

Inputs MS1 and MS0 select one of four display modes. All attributes except underline operate independent of the display mode used. Figures 8a and 8b illustrate a typical CRT 9021 configuration which operates in all display modes for both the parallel and serial scan line modes respectively.

MS1, MS0 = 00 —Wide Graphics Mode.
In this display mode, inputs D7-D0 define a graphics entity as illustrated in figure 2. Note that individual bits in D7-D0 will illuminate particular portions of the character block. Table 2 shows all programming ranges possible when defining the wide graphic boundaries. No underline is possible in this display mode.

MS1, MS0 = 10 —Thin Graphics Mode.
In this display mode, inputs D7-D0 define a graphic entity as illustrated in figure 3. Note that individual bits in D7-D0 will illuminate particular horizontal or vertical line segments within the character block. Table 3 shows all programming ranges possible when defining the thin graphics boundaries. No underline is possible in this display mode.

MS1, MS0 = 01 —Character Mode Without Underline.
In this display mode, inputs D7-D0 go directly from the input latch to the video shift register via the Attributes and Graphics logic. This mode requires either a bit mapped system RAM (1 bit in RAM equals 1 pixal on the CRT) or an external character generator as shown in figures 8a and 8b.

MS1, MS0 = 11 —Character Mode With Underline.
Same operation as MS1, MS0 = 01 with the underline attribute appearing on the scan line(s) mask programmed.

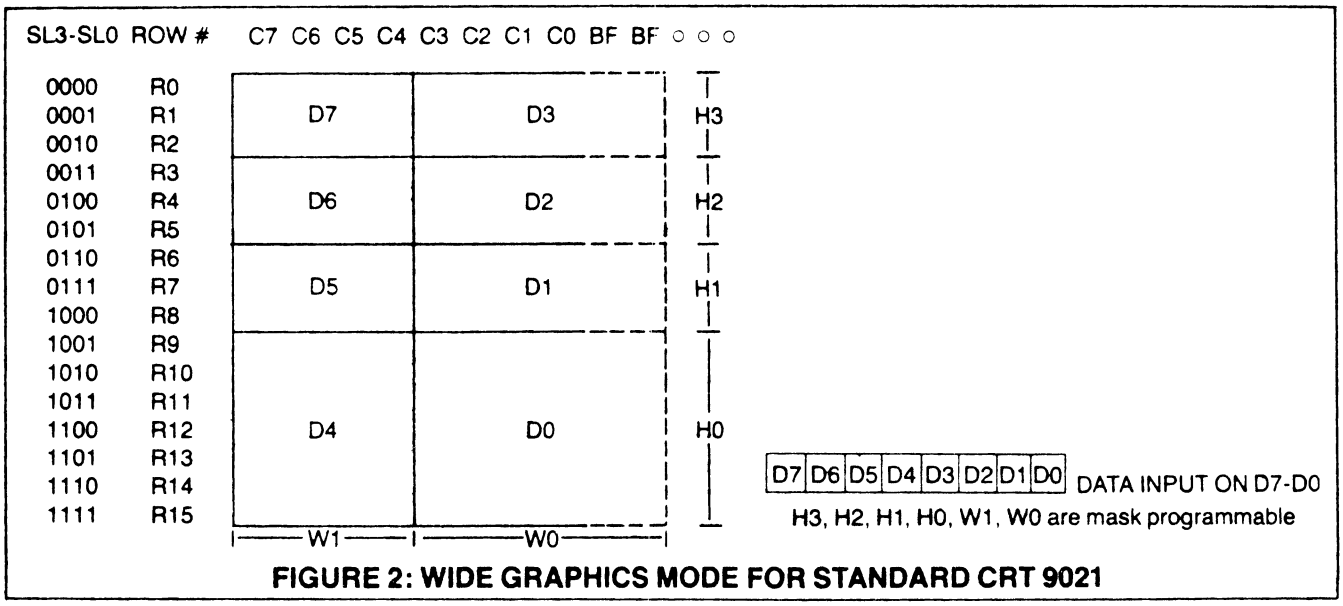


FIGURE 2: WIDE GRAPHICS MODE FOR STANDARD CRT 9021

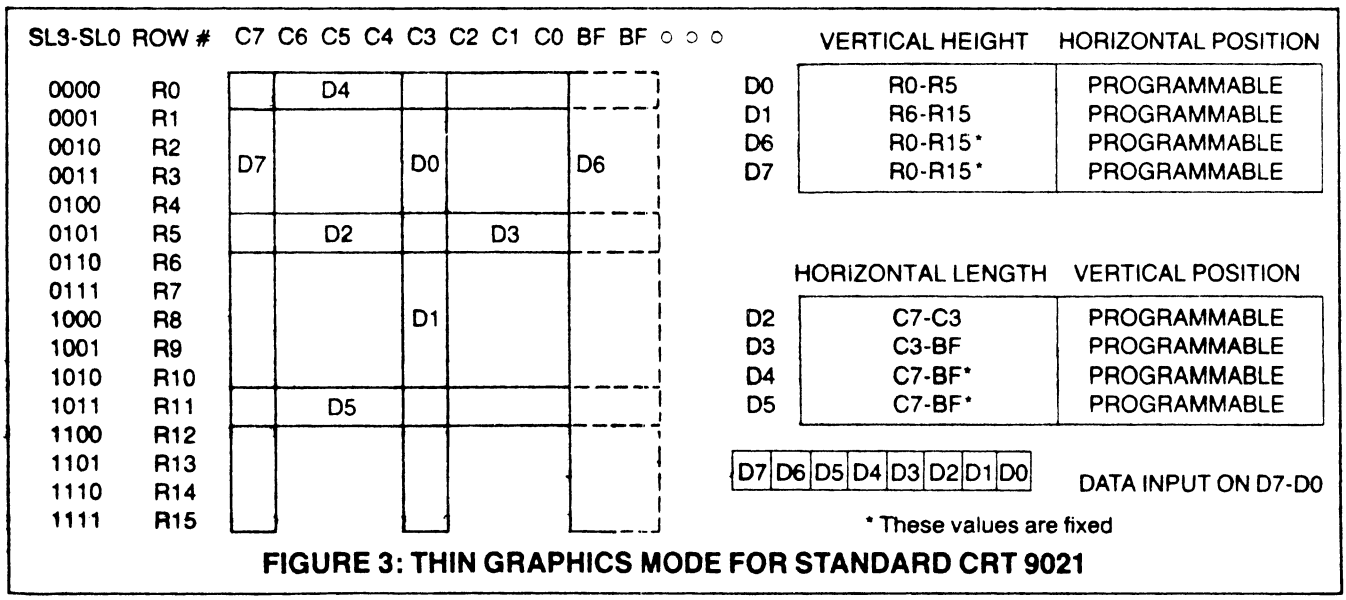


FIGURE 3: THIN GRAPHICS MODE FOR STANDARD CRT 9021

BACKFILL

Backfill is a mechanism that allows a character width of greater than 8 dots and provides dot information (usually blanks) for all dot positions beyond 8. The character width is defined by the period of the $\overline{LD}$/SH input. For the character modes, backfill is added to the tail end of the character by two methods which are mask programmable.

Method A — The backfill (BF) dots will be the same as the dot displayed in position C7.

Method B — The backfill (BF) dots will be the same as the dot displayed in position C0.

For the wide graphics mode, the backfill dots will always be the same as the dot displayed in position C0 (method B) with no programmable option.

CURSOR FORMATS

Four cursor formats are possible with the CRT 9021. If the parallel scan line input mode is used, one of four cursor formats may be selected as a mask programmed option. If the serial scan line input mode is used, the cursor format is selected via input pins 16 and 17 (SL3/BKC, SL2/BLC). See Table 5. The four cursor modes are as follows:

Underline — The cursor will appear as an underline. The position and width of the cursor underline is mask programmed.

Blinking Underline — The cursor will appear as an underline. The underline will alternate between normal and reverse video at the mask programmed cursor blink rate.

Reverse Video Block — The cursor will appear as a reverse video block (The entire character cell will be displayed in reverse video).

Blinking Reverse Video Block — The cursor will appear as a reverse video block and the entire block (character plus background) will alternate between normal and reverse video at the masked programmed cursor blink rate.

Scan Line Input Mode	Pin 17	Pin 16	Cursor Function
Serial	1	0	Underline
	1	1	Reverse Video Block
	0	0	Blinking Underline
	0	1	Blinking Reverse Video Block
Parallel	X	X	Mask programmable Only

TABLE 5: CURSOR FORMATS

DOUBLE WIDTH MODE

In order to display double width characters, video must be shifted out at half frequency and the video shift register must receive new information (parallel load) every other $\overline{LD}$/SH input pulse. In order to divide the video dot clock (VDC) and the $\overline{LD}$/SH pulse internally at the proper time, the cursor input should be pulsed during RETBL prior to the scan line to be displayed as double width. The CURSOR input must remain low for a minimum of 1 $\overline{LD}$/SH period from the leading edge of RETBL. The CURSOR input can stay high for the entire RETBL time but should not extend into active video. If it does, a cursor will be displayed. It is assumed that the CRT controller knows when a particular scan line should be double width and it should activate the CURSOR in the manner just described. Double height double width characters can also be displayed if the scan line count is incremented by the CRT controller every other scan line. With respect to the CRT 9021, no distinction between double width and double height display is necessary. Figure 4 illustrated timing for both single and double width modes. The CRT 9007, which supports double height double width characters, will produce the CURSOR signal as required by the CRT 9021 with no additional hardware.

SCAN LINE INPUT MODES

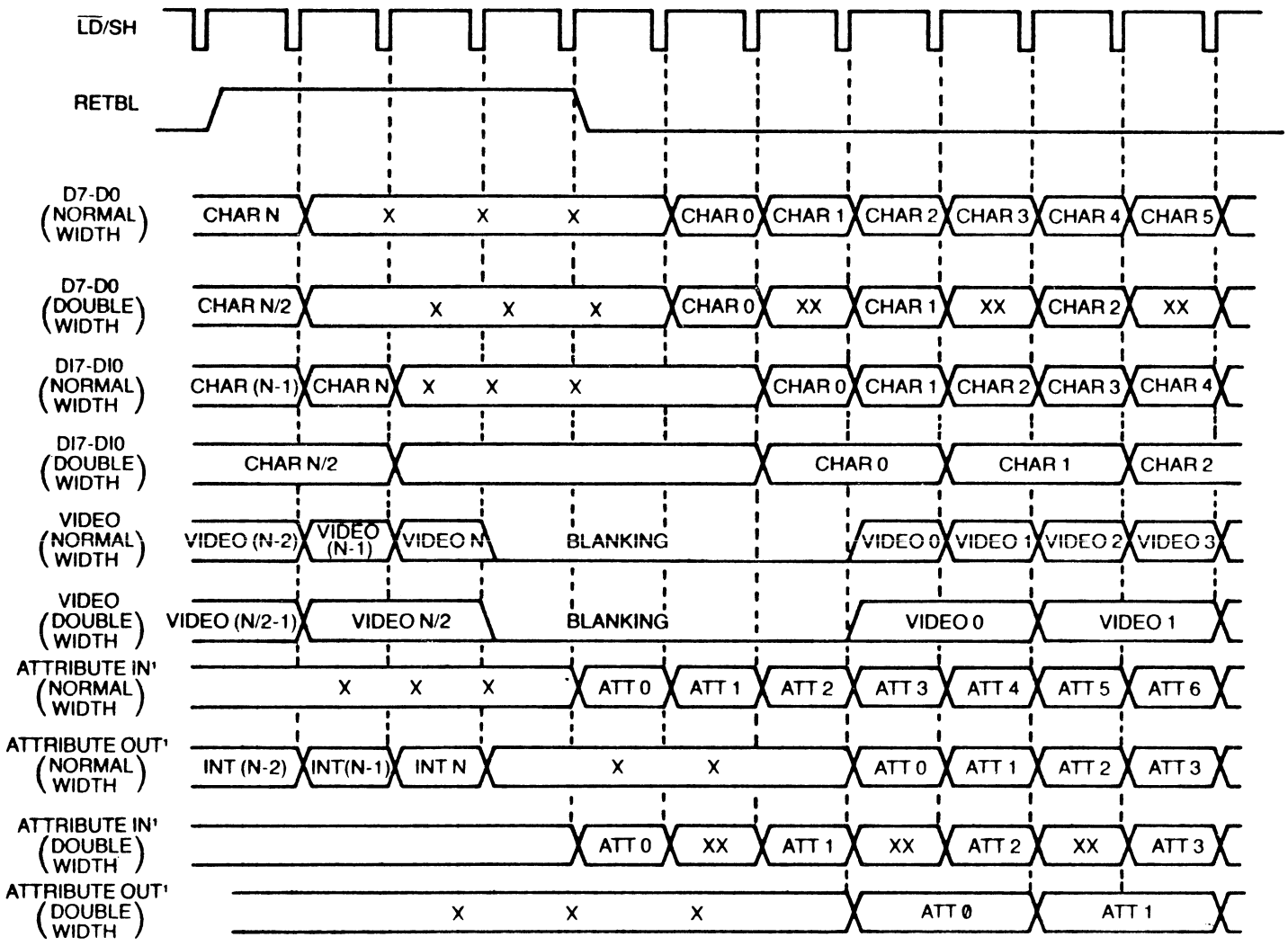
Scan line information can be introduced into the CRT 9021 in parallel format or serial format. Table 6 illustrates the pin definition as a function of the scan line input mode. The CRT 9021 will automatically recognize the proper scan line mode by observing the activity on pin 18. In parallel mode, this input will be stable for at least 1 scan line and in serial mode this input will remain low for about 5 or 6 $\overline{LD}$ SH periods. If pin 18 goes active low for less than seven but more than two continuous $\overline{LD}$/SH periods during the last scan line that has an active low on the $\overline{VSYNC}$ input, the serial mode will be locked in for the next field. The parallel scan line input mode will be selected for the next field if the following two conditions occur during $\overline{VSYNC}$ low time. First, at least one positive transition must occur on pin 18 and second, pin 18 must be low for seven or more $\overline{LD}$ SH periods. Refer to figure 7 for timing details.

Scan Line Input Mode	CRT 9021 Pin Number			
	19	18	17	16
Serial	SLD	$\overline{SLG}$	BLC	BKC
Parallel	SL0	SL1	SL2	SL3

TABLE 6: PIN DEFINITION FOR PARALLEL AND SERIAL SCAN LINE MODES

PROGRAM OPTIONS

The CRT 9021 has a variety of mask programmed options. Tables 2 and 3 illustrate the range of these options for the wide and thin graphics modes respectively. Table 4 illustrates the range of the miscellaneous mask programmed options. In addition, Tables 2, 3 and 4 show the mask programmed options for the standard CRT 9021.



1-Attributes include MS0 , MSI, BLINK, CHABL, INTENSITY, REVID

FIGURE 4: CRT 9021 FUNCTIONAL I/O TIMING

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	.15V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	All inputs except VDC, $\overline{LD}$/SH
High Level V_{IH2}	4.3			V	For VDC, $\overline{LD}$/SH input
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 0.4 mA
High Level V_{OH}	2.4			V	I_{OH} = 100μA
INPUT LEAKAGE CURRENT					
Leakage I_{L1}			10	μA	$0 \leq V_{IN} < V_{CC}$, excluding VDC, $\overline{LD}$/SH
Leakage I_{L2}			50	μA	$0 \leq V_{IN} \leq V_{CC}$; for VDC $\overline{LD}$/SH
INPUT CAPACITANCE					
C_{IN1}		10		pf	Excluding VDC, $\overline{LD}$/SH
C_{IN2}		20		pf	For $\overline{LD}$/SH
C_{IN3}		25		pf	For VDC
POWER SUPPLY CURRENT					
I_{CC}		50		mA	

AC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VDC[1]					
$1/t_{CY1}$ VDC frequency	1.0		30.0	MHZ	CRT 9021A; see note 1
	1.0		28.5	MHZ	CRT 9021B
t_{CKL} VDC low	10				
t_{CKH} VDC high	10			ns	
t_{CKR} VDC rise time	10		10	ns	Measured from 10% to 90% points
t_{CKF} VDC fall time			10	ns	Measured from 90% to 10% points
$\overline{LD}$/SH					
t_{CY2}	290			ns	CRT 9021A; see note 1
	315			ns	CRT 9021B
t_{S1}	7			ns	
t_{H1}	0			ns	
INPUT SETUP AND HOLD					
t_{S2}	35			ns	
t_{H2}	0			ns	
MISCELLANEOUS TIMING					
t_{PD}			35	ns	C_L = 15 pf
t_{DW}	t_{CY2}				

1-These parameters are Preliminary.

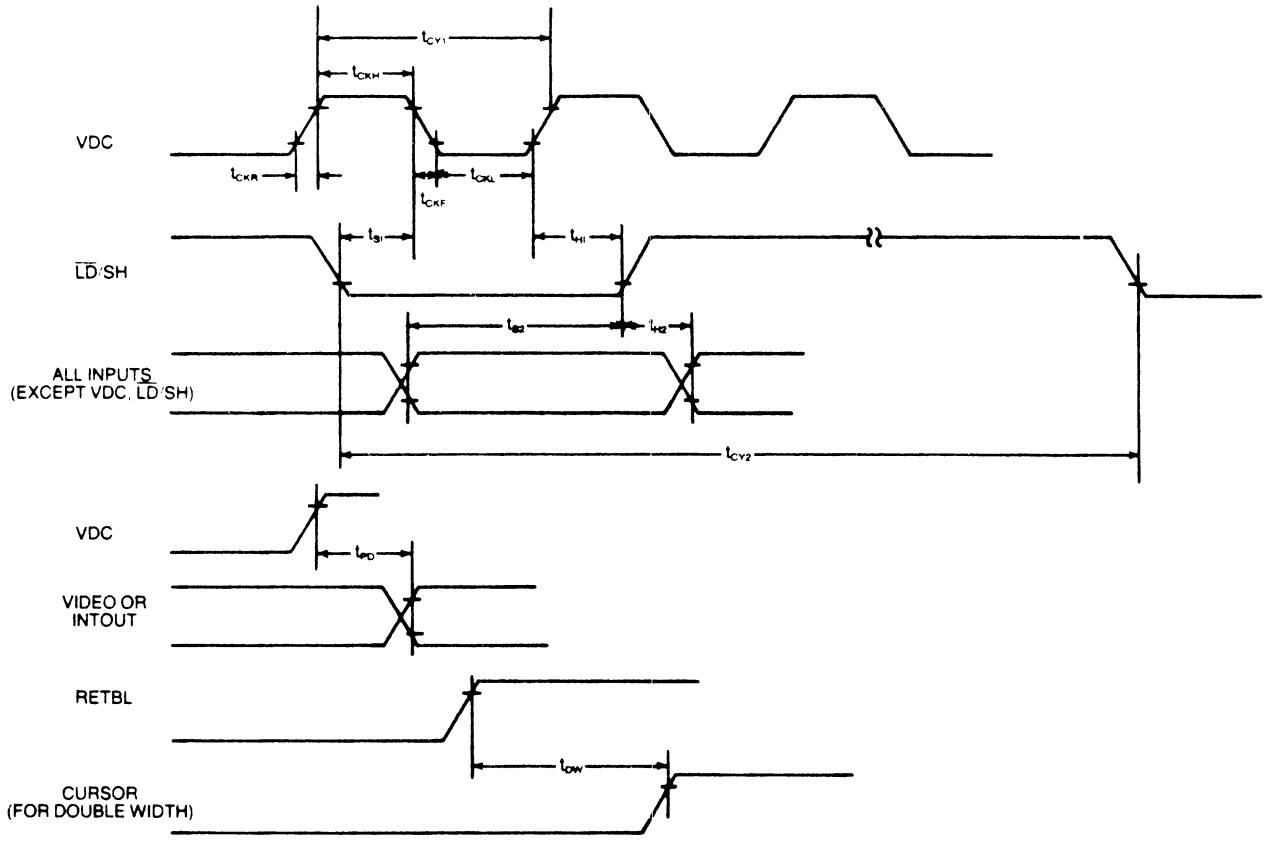


FIGURE 5: CRT 9021 INPUT/OUTPUT TIMING

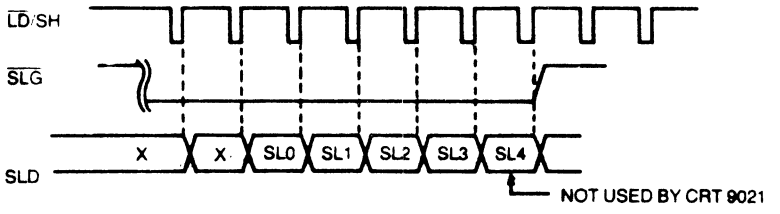


FIGURE 6: SERIAL SCAN LINE MODE TIMING

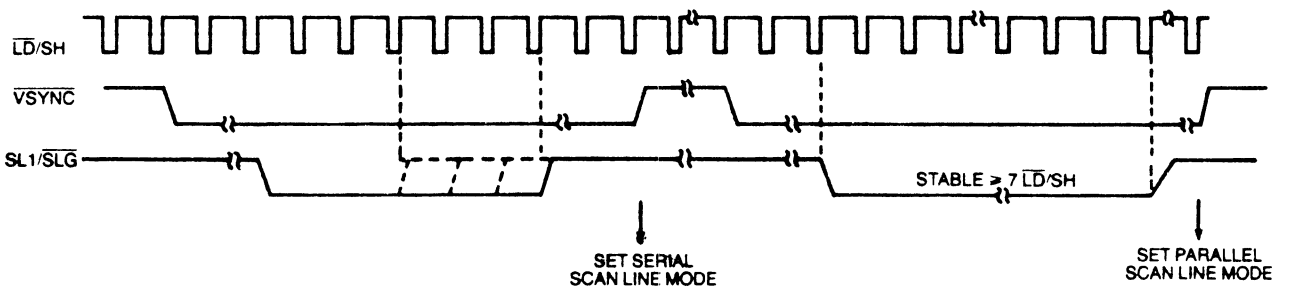


FIGURE 7: SERIAL/PARALLEL SCAN LINE MODE SELECTION TIMING

TABLE 2
WIDE GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Height of graphic block*		
D7 and D3	any scan line(s)	R0, R1, R2
D6 and D2	any scan line(s)	R3, R4, R5
D5 and D1	any scan line(s)	R6, R7, R8
D4 and D0	any scan line(s)	R9, R10, R11, R12, R13, R14, R15
Width of D7, D6, D5, D4**	any number of dots 0 to 8	C7, C6, C5, C4
Width of D3, D2, D1, D0**	any number of dots 0 to 8	C3, C2, C1, C0, BF

* Any graphic block pair can be removed by programming for zero scan lines.

** Total number of dots for both must be equal to the total dots per character with no overlap.

TABLE 3
THIN GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Backfill	C1 or C0	C0
Horizontal position for		
D2 and D3	any scan line(s) R0-R15	R5
D4	any scan line(s) R0-R15	R0
D5	any scan line(s) R0-R15	R11
Horizontal length for		
D2[2]	any continuous dots C7-C0, BF	C7-C3
D3[2]	all dots not covered by D2	C3-BF
Blanked dots for serrated horizontal lines		
D2	any dot(s) C7-C0, BF	none
D3	any dot(s) C7-C0, BF	none
D4 and D5	any dot(s) C7-C0, BF	none
Vertical position for		
D0 and D1	any dot(s) C7-C0, BF	C3
D6[1]	any dot(s) C6-C0, BF	BF
D7[1]	any dot(s) C7-C0	C7
Vertical length for		
D0	any scan line(s)	R0 to R5
D1	all scan lines not used by D0	R6 to R15
D6	no choice; always R0-R15	R0 to R15
D7	no choice; always R0-R15	R0 to R15

1-D7 must always come before D6 with no overlap; otherwise D6 is lost.

2-D2 and D3 must always overlap by one and only one dot.

TABLE 4
MISCELLANEOUS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Backfill in character mode	C7 or C0	C7
Character blink rate (division of $\overline{\text{VSYNC}}$ frequency)	8 to 60; divisible by 4 (7.5 Hz to 1 Hz)[1]	32 (1.875 Hz)[1]
Cursor blink rate[2]	Twice the character blink rate	16 (3.75 Hz)[1]
character underline position	any scan line(s) R0-R15	R11
cursor underline[3]	any scan line(s) R0-R15	not applicable
cursor format[4]	underline Blinking underline Reverse video block Blinking reverse video block	Blinking reverse video block

1 - Assumes $\overline{\text{VSYNC}}$ input frequency of 60 Hz.

2 - Valid only if the cursor is formatted to blink.

3 - Valid only if the cursor is formatted for underline.

4 - Valid for the parallel scan line mode only.

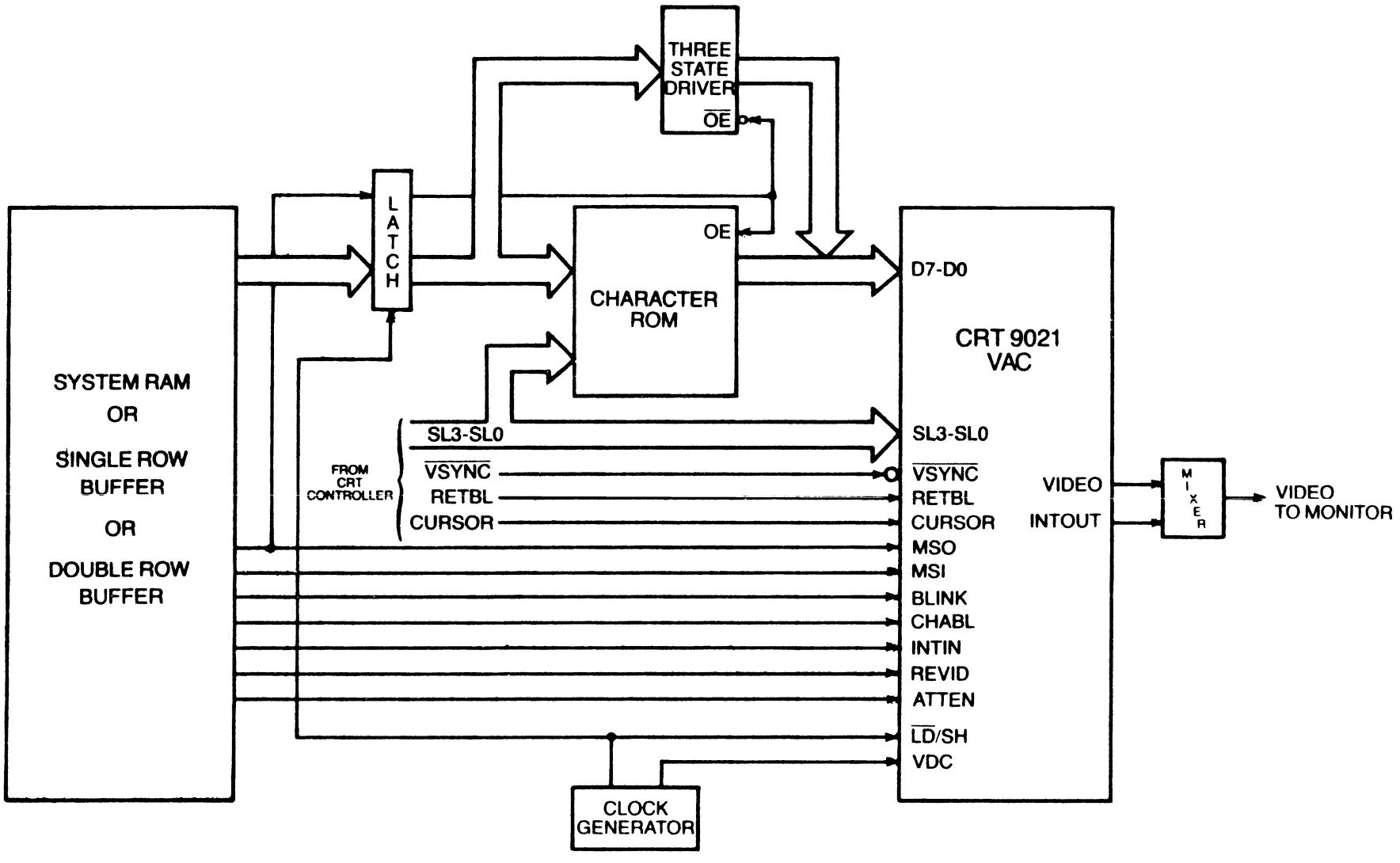


FIGURE 8a: CRT 9021 SYSTEM CONFIGURATION IN PARALLEL SCAN LINE MODE

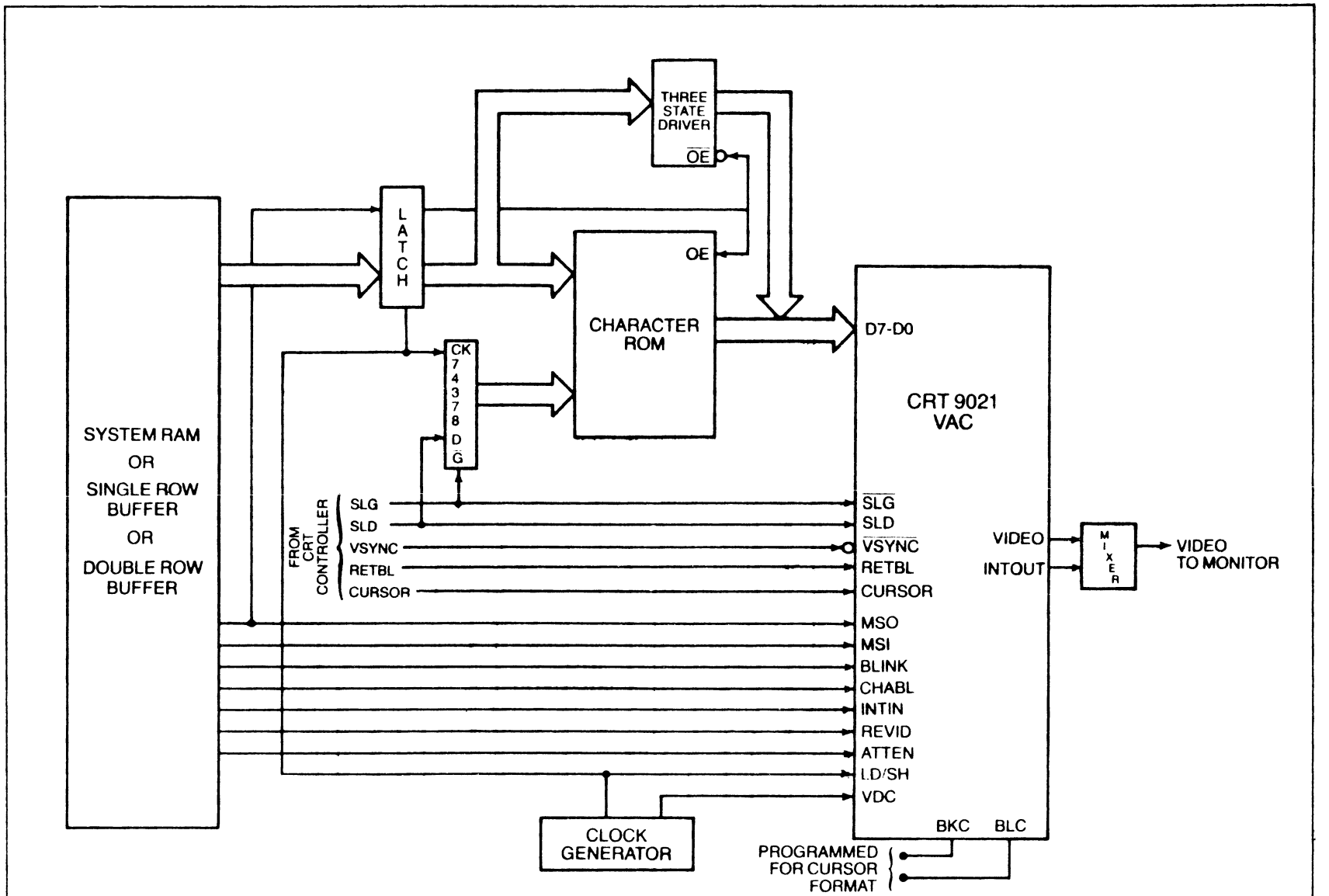
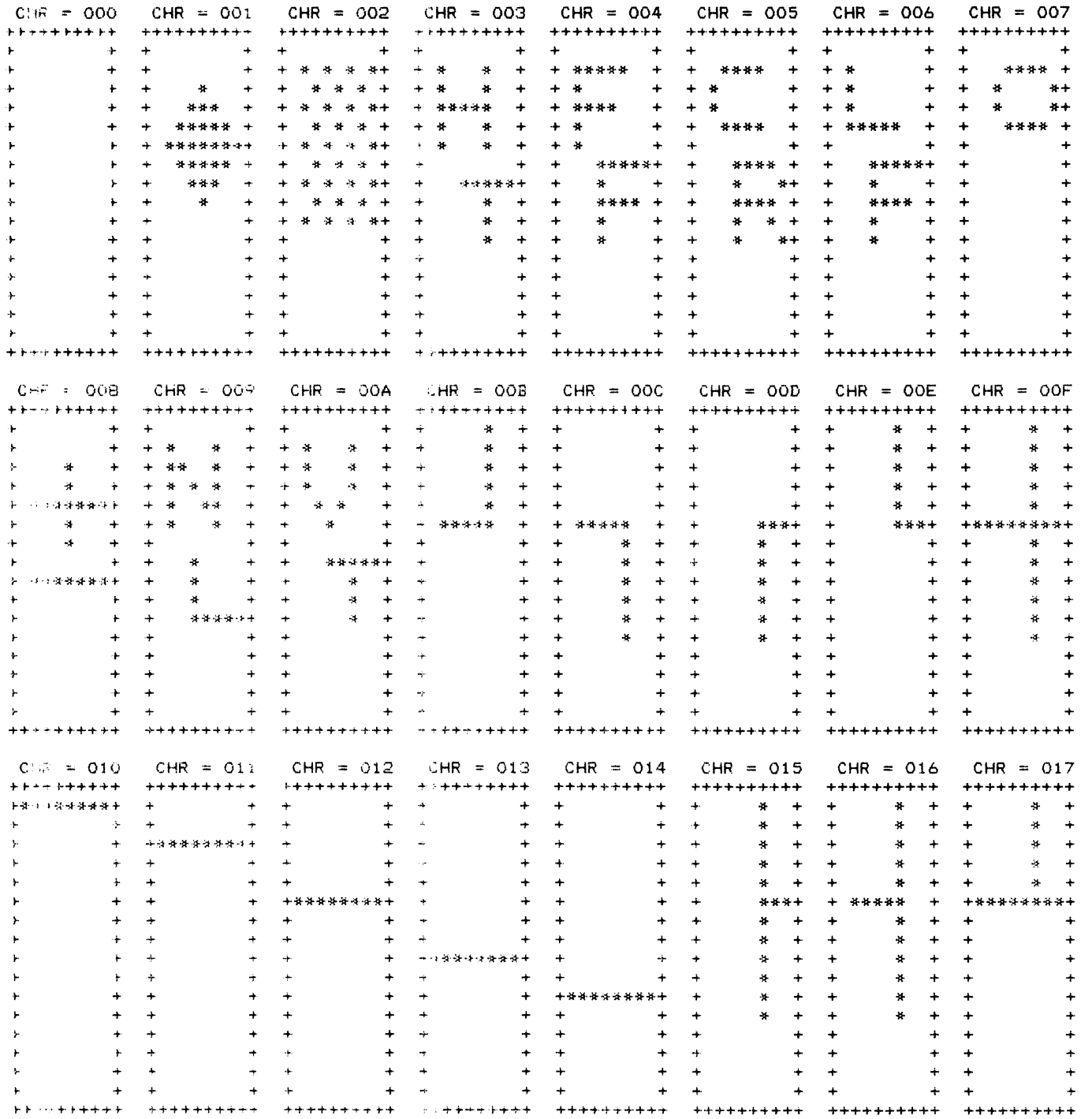
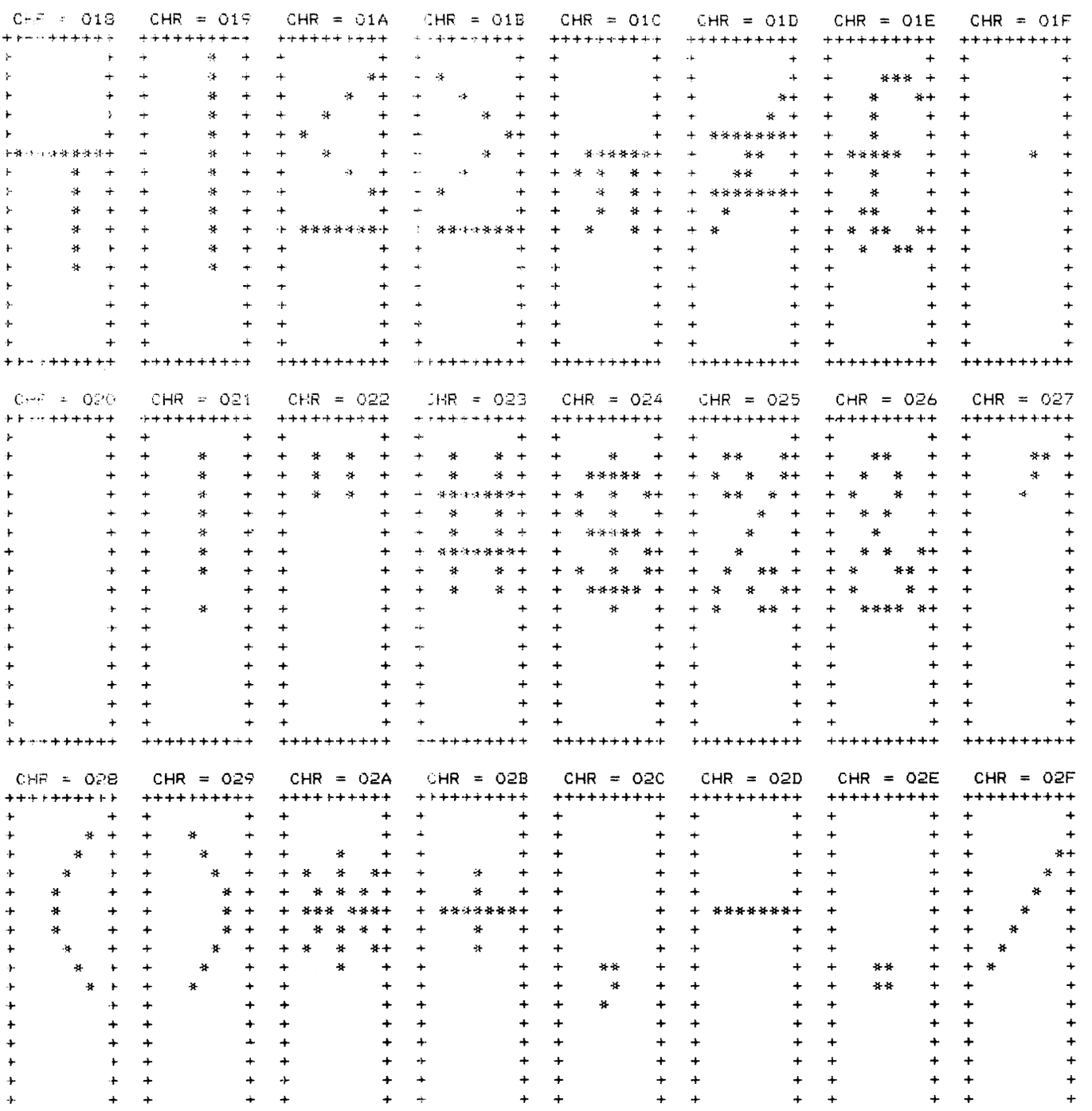


FIGURE 8b: CRT 9021 SYSTEM CONFIGURATION IN SERIAL SCAN LINE MODE

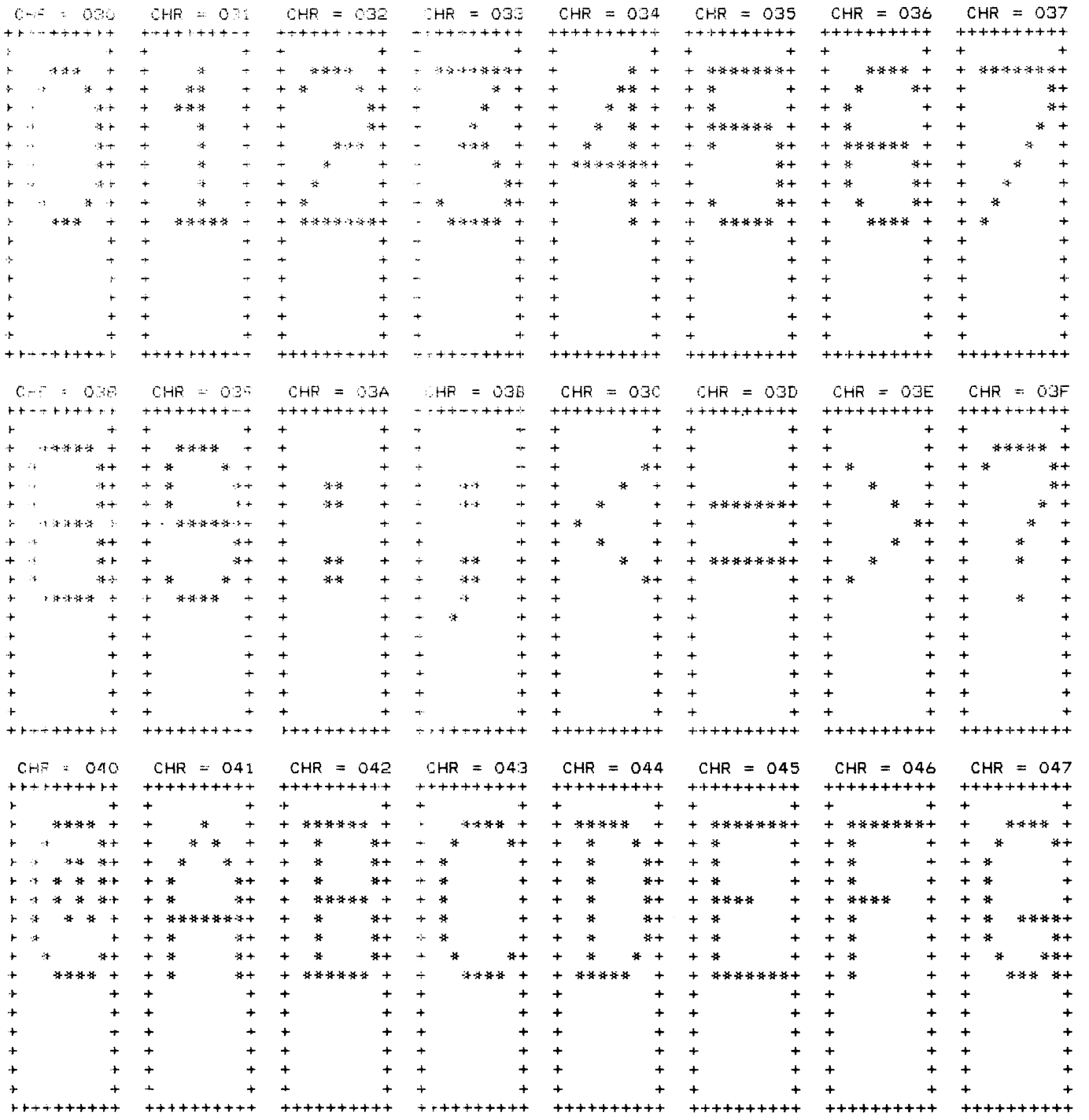
FILE: cgr.obj TITLE: Standard & Alternate Character set. DATE: OCT-14-1983 11:15:55



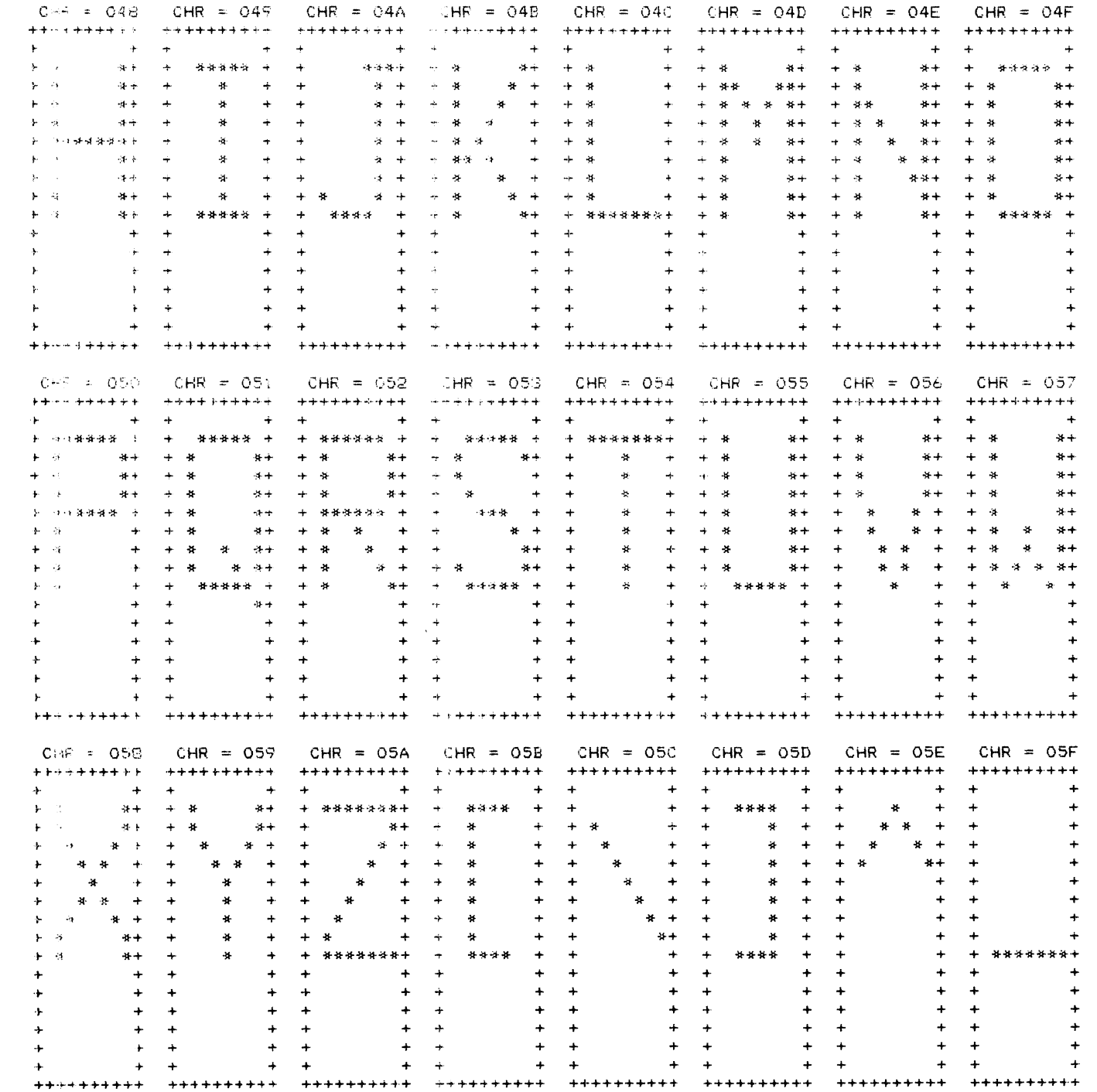
FILE :gr.obj TITLE:Standard & Alternate Character set. DATE:OCT-14-1983 11:15:55



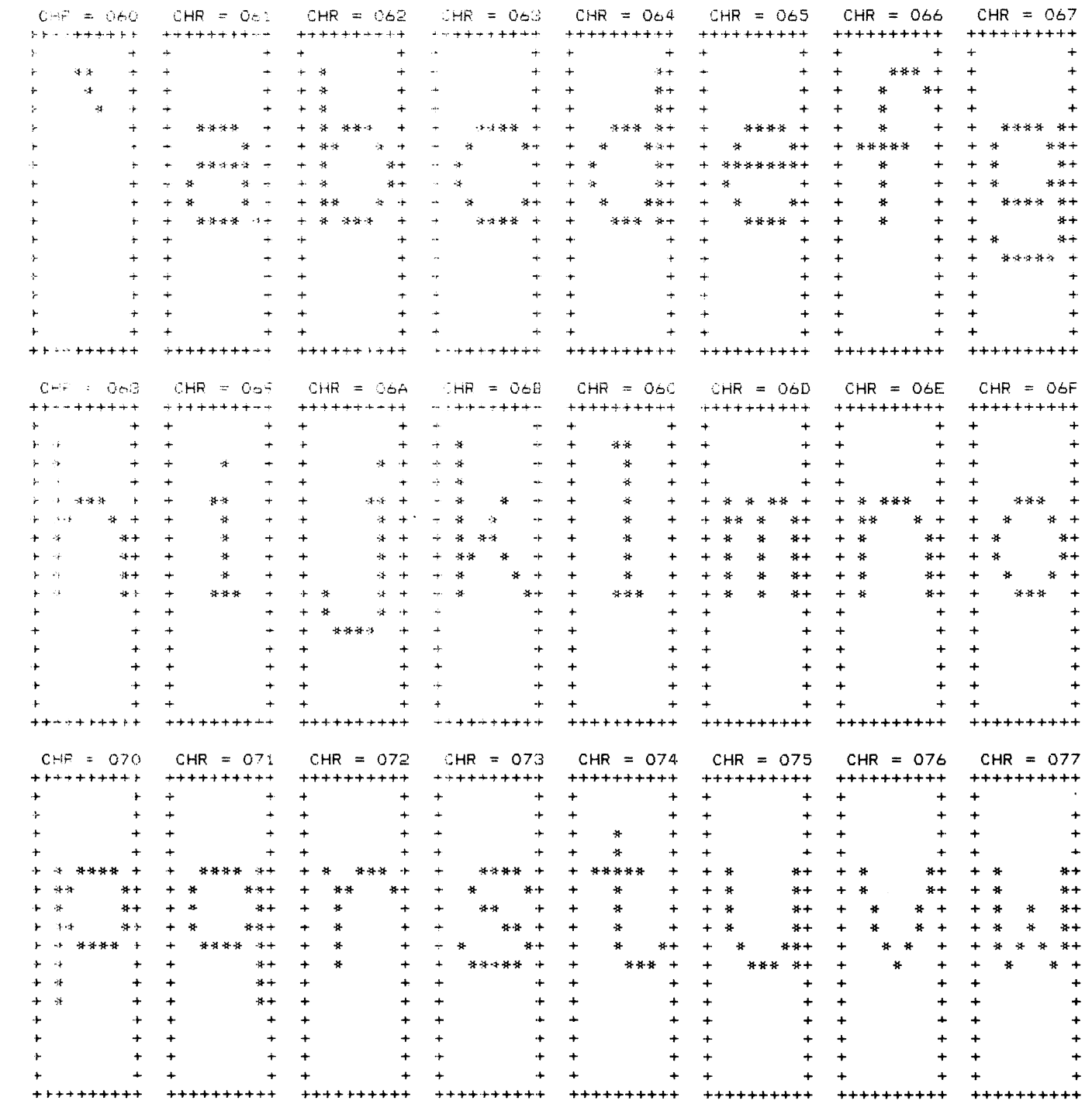
FILE: gr_obj TITLE: Standard & Alternate Character set DATE: OCT-14-1983 11:15:55



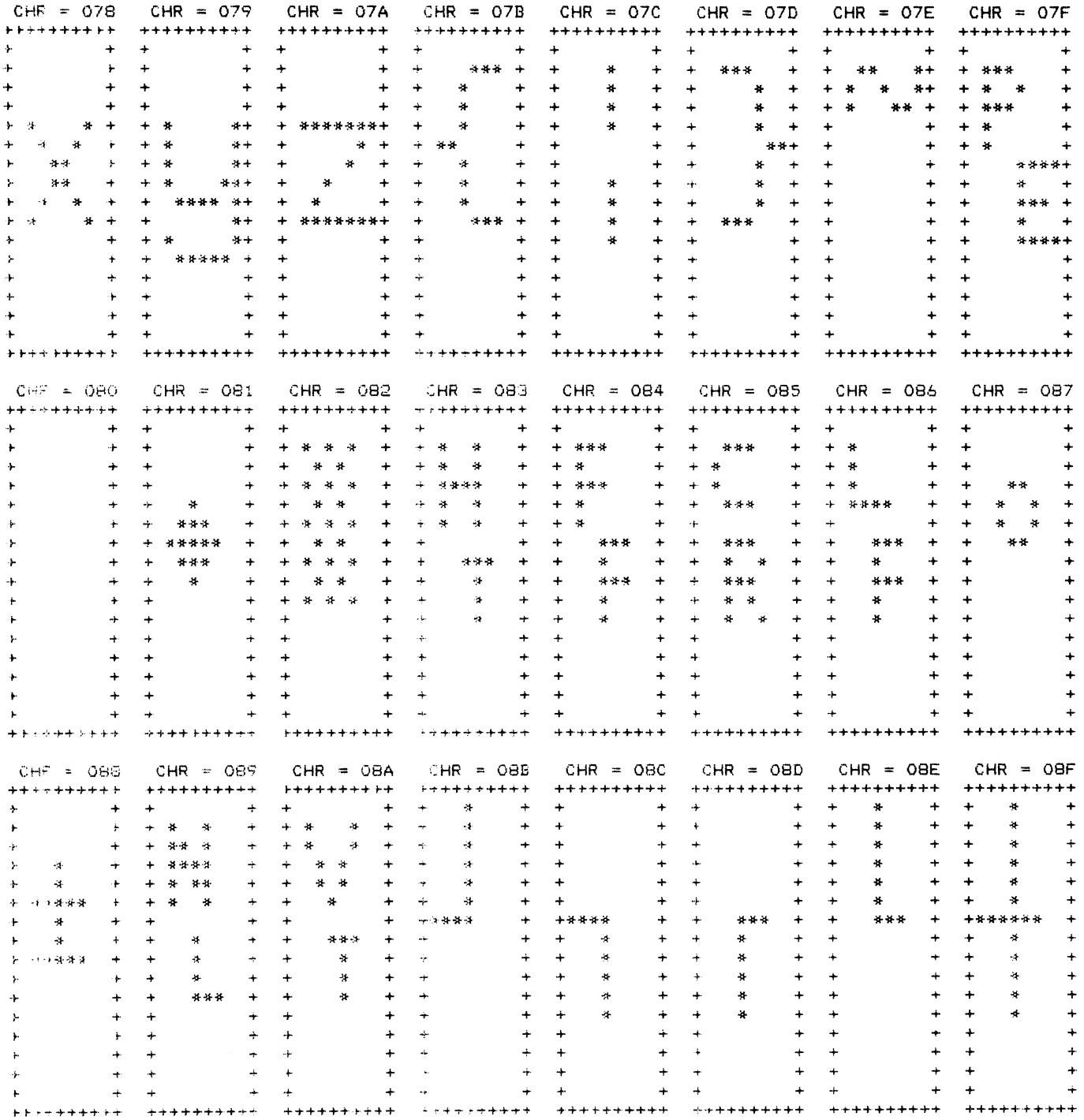
FILE: gr.obj TITLE: Standard & Alternate Character set DATE: OCT-14-1983 11:15:55



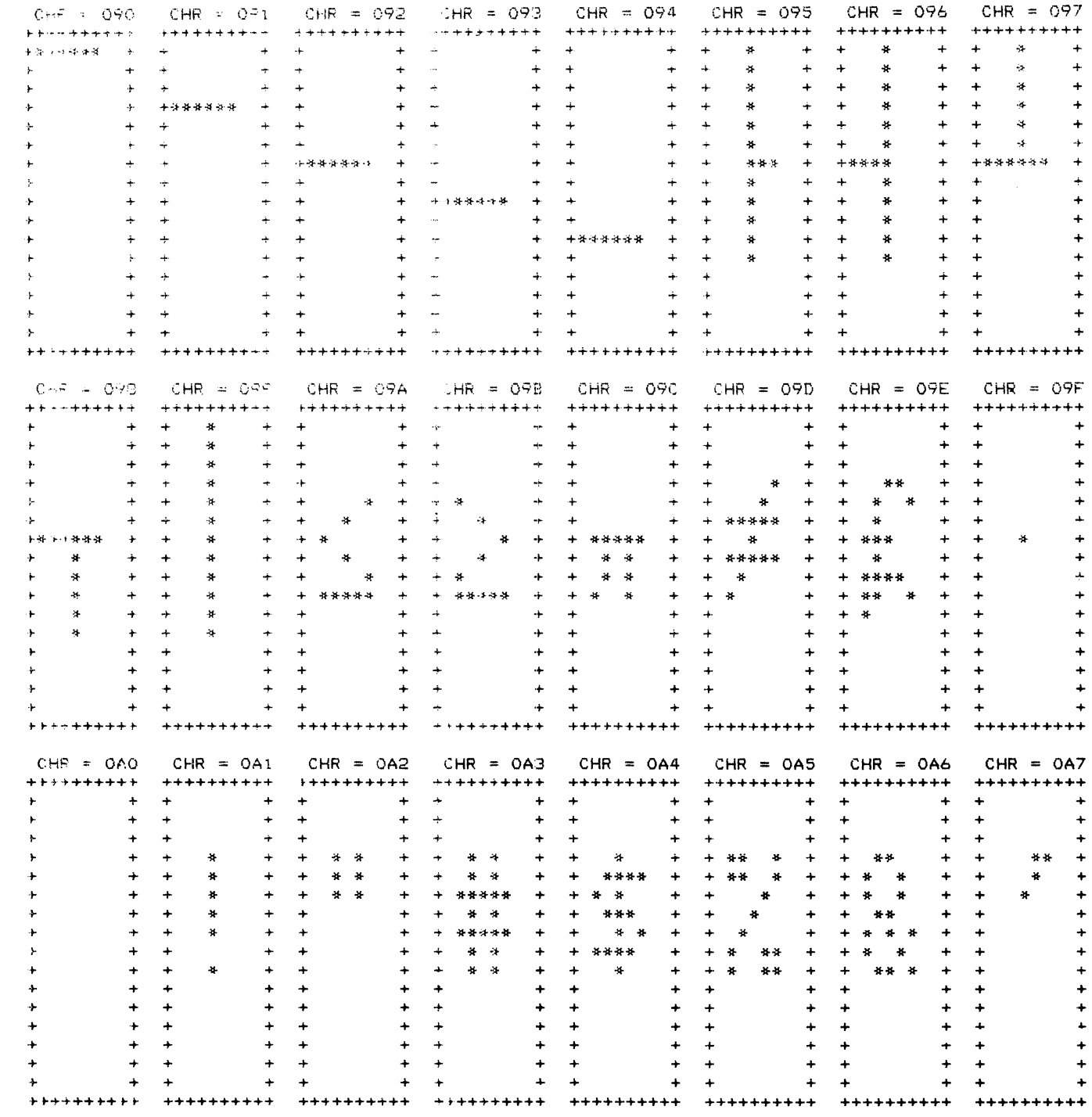
FILE: gr_ob_j TITLE: Standard & Alternate Character set. DATE: OCT-14-1983 11:15:55



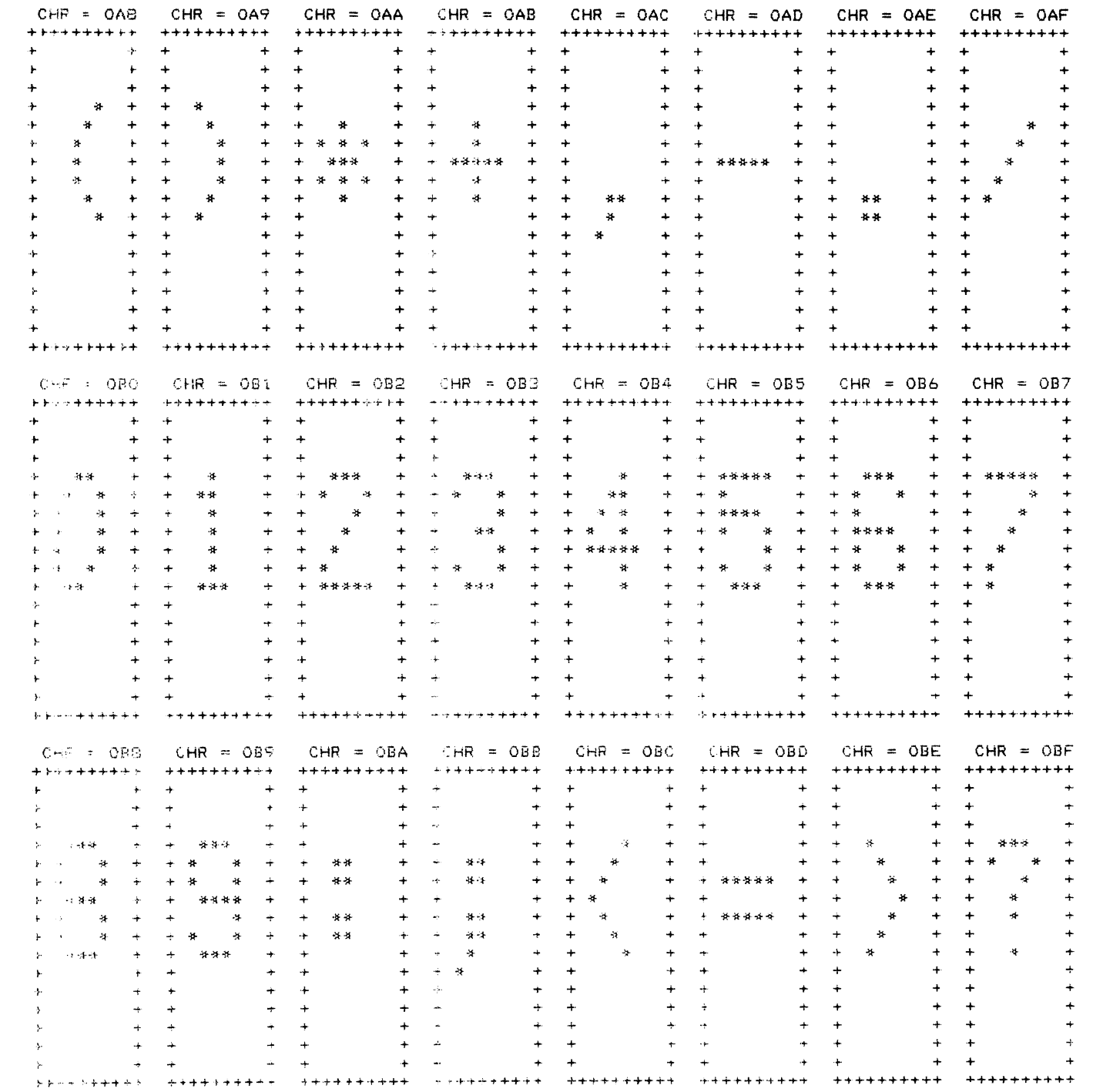
FILE cgr.obj TITLE: Standard & Alternate Character set. DATE: OCT-14-1983 11:15:55



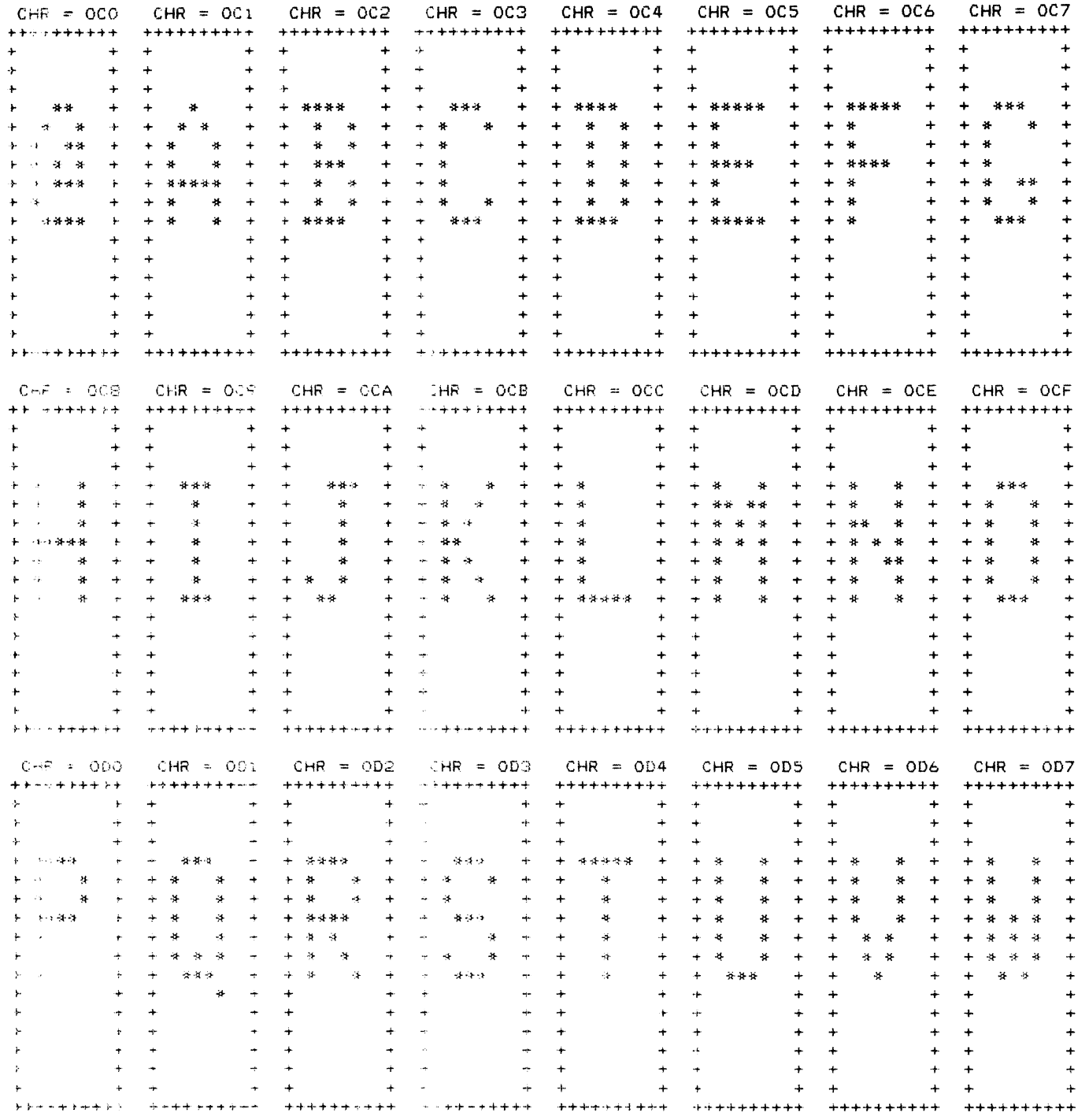
FILE: gr.obj TITLE: Standard & Alternate Character set. DATE: OCT-14-1983 11:15:55



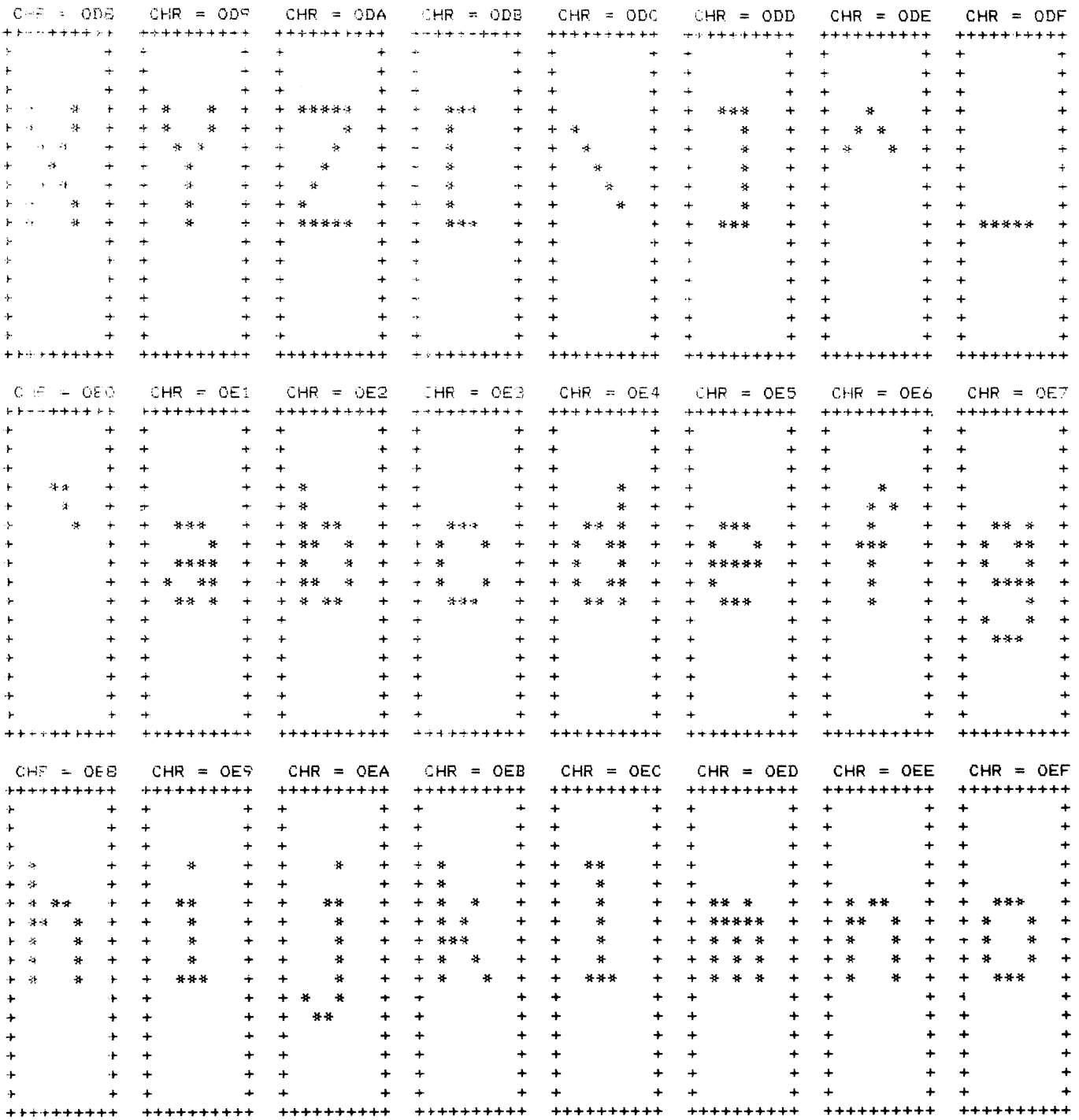
FILE cgr.obj TITLE:Standard & Alternate Character set. DATE:OCT-14-1983 11:15:55



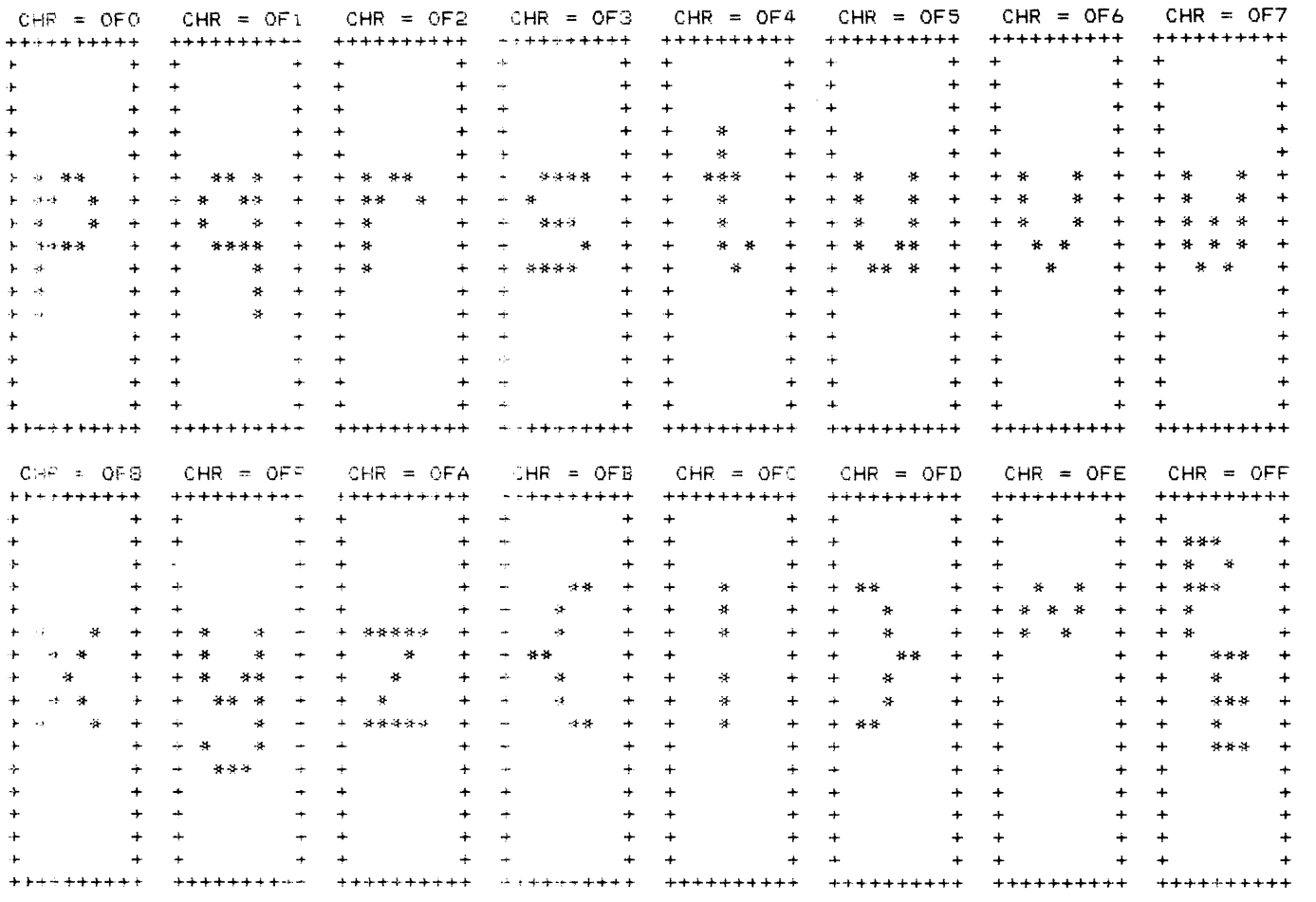
FILE: cgr.obj TITLE: Standard & Alternate Character set. DATE: OCT-14-1983 11:15:55



FILE: gr_obj TITLE: Standard & Alternate Character set DATE: OCT-14-1983 11:15:55



FILE: cgr.obj TITLE: Standard & Alternate Character set. DATE: OCT-14-1983 11:15:55



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