PRODUCT Analog-to-Digital Converter

MODEL 620-85A

DATE September 1, 1971

620 series Dataspec.

varian data machines

ANALOG-TO-DIGITAL CONVERTER MODULES

INTRODUCTION

The Model 620-85A Analog-to-Digital Converter Module (ADCM) is an option for use with the Varian Data 620 series computers. The ADCM provides an analog-to-digital converter (ADC), sample and hold amplifier, and programmable timer.

The ADCM accepts a high-level analog signal which it samples and holds for conversion by the ADC. The ADC outputs a 13-bit word in binary two's complement format to a 620 computer. The timer can be used to establish time intervals for system control.

GENERAL DESCRIPTION

The ADC employs the successive approximation technique for conversion. It's conversion rate is 13 microseconds for 13 bits, with a sample and hold amplifier settling time of 6 microseconds. The ADC can be initiated by the computer, the programmable timer, or an external pulse. The programmable timer provides an internal and external control capability. Under internal control, the timer sets a timing interval through a data word which it receives from the computer. The timer decrements the data word at 1 microsecond per count until the zero state is reached. The timer then emits a pulse, restores the original data word, and again initiates the cycle. Under external control, the timer can be inhibited at any time by an external signal which holds the timer at its load point. Timing intervals start at the instant the external signal level is removed or set to a high logic state. New timing intervals can be sent by the computer while the timer is externally inhibited.

ADCM data transfers can occur by programmed output command execution or under the optional Buffer Interlace Controller (BIC) control. When operating under program control, data transfers are initiated by the computer and are executed under input/output instruction control. The BIC permits automatic, high-speed, block data transfers between ADCM and the 620 computer memory without disturbing the sequence of the main program.

The Model 620-85A ADCM provides for a single analog input. This configuration can be readily expanded to multiple input channels by the addition of a Multiplexer Module, Model 620-860 or 861.

PREREQUISITES

- 620 System Computer
- 620 Expansion Chassis (requirements determined on individual system basis)
- 620-88 Analog Power Supply (requirements determined on individual system basis)
- 620 Peripheral Backplane Wiring Panel (requirements determined on individual system basis)

SOFTWARE

A comprehensive software package is provided comprising a test program and an I/O Driver Program. The test program is an effective tool for determining the operational status of the ADCM.

The I/O Driver Program provides convenient access to the ADCM without detailed knowledge of the hardware. The program can be used by itself or embedded in an operating system. The I/O Driver Program consists of two routines: Programmed Data Transfers and Direct Memory Access Data Transfers. These routines permit the user to specify the following parameters:

- Destination array and quantity of incoming data.
- Time between acquisition frames (a frame is defined to be the period of time required to input data)
- An error address to which control will pass when any one of several error conditions are detected.

SPECIFICATION

Programmable Timer

Clock frequency	1.0 MHz ±0.01%
Clock drift	±1 PPM/°C
Clock stability	±0.01% PPM/DAY
Resolution	16 Binary Bits (Computer E-Bus $2^0 - 2^{15}$)
Programmed PRF	1 MHz to 15.26 Hz 1 microsecond to 65.535 milliseconds
Timer Output	100 nanosecond pulse to ground. 1K ohms to +5V sinks 100 mA. Maximum capacity load 1000 pF.
CLK Output	100 nanoseconds pulse from low to high. TTL output. Available fanout: 6 logic loads. PRF = 1.0 MHz ±.01%.
Timer Clock Input	1 TTL load. Maximum PRF = 10 MHz. Increments counter on low to high transition.

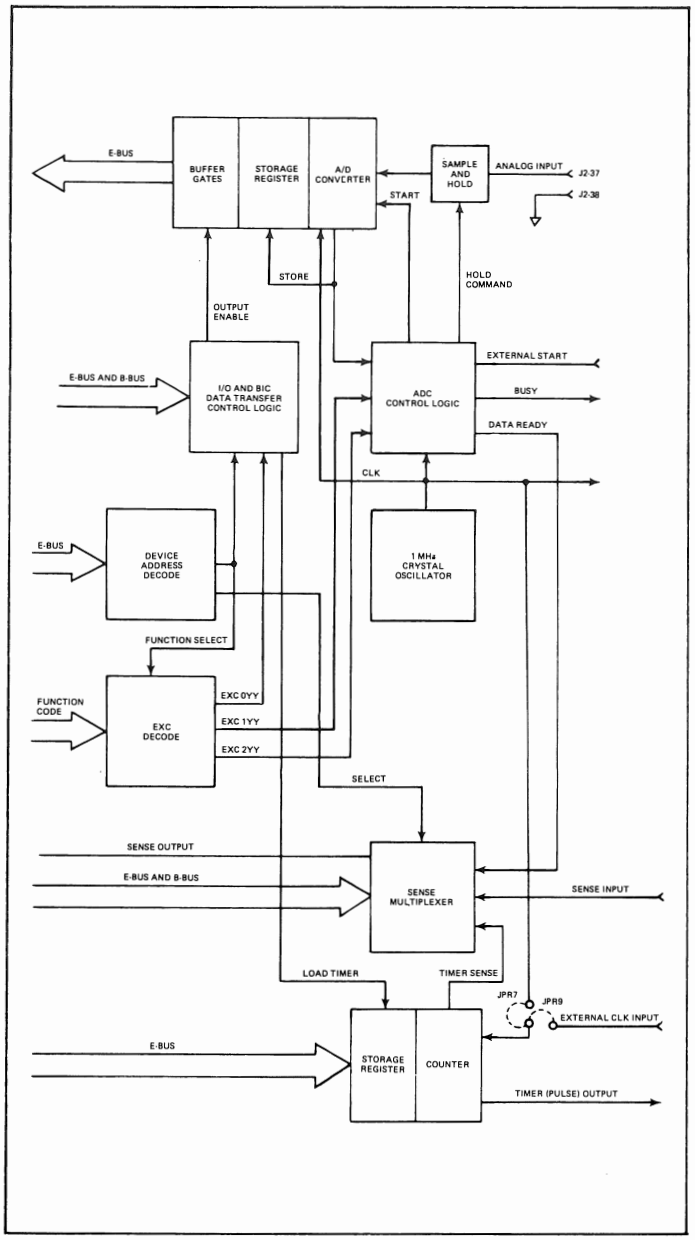
Sample & Hold

Gain and Accuracy

Voltage Gain	+1
Accuracy	±.01%
Gain Temp Coefficient	±10 PPM/°C

Track Mode

Full Power Response (20V peak-to-peak sine wave)	75 kHz
Slew rate	4V/microsecond
Settling Time to	±1 mV 6 microseconds



Input Characterisitics, Single Ended
- Signal Range ..... ±10V
- Maximum Rating, without damage ..... ±15V
- Input Impedance ..... 10^{11} ohms in parellel with 5000 pF
- Offset Voltage ..... ±2 mV maximum
- VS Temperature ..... ±50μV/°C

Input Characterisitics, Differential
- Signal Range ..... ±10V
- Maximum Rating, without damage ..... ±30V
- Input Impedance ..... 50K ohms
- Common Mode Rejection ..... 80 dB, 0 to 60 Hz
- Offset Voltage ..... ±2 mV, maximum
- VS Temperature ..... ± 100 μV/°C

Output Characteristics
- Signal Range ..... ±10V
- Noise, RMS Wide Band, (Hold Mode) ..... 1 mV peak-to-peak
- Decay Rate in, Hold Mode ..... ±10 mV/Second
- Feedthrough 20V Step, (Hold Mode) ..... -80 dB

Switching Characteristics
- Aperture Time, Maximum ..... 100 nanoseconds
- Offset Pedestal, Maximum ..... ±2 mV
- Acquisition Time, Maximum ..... 6 microseconds

Analog to Digital Converter
- Resolution ..... 13 binary bits
- Output Format ..... twos complement
- Conversion Accuracy ..... ±.012% of 20V Full Scale, ±½ LSB
- Conversion Time ..... 13 microseconds, maximum
- Temperature Coefficient ..... ±50 μV/°C maximum
- Warm up Time ..... Essentially Zero
- Full Scale Range ..... ±10V

Digital Outputs
- BUSY ..... High (true) during Analog-to-Digital Conversion. Available fanout: 8 logic loads. Maximum capacitive load: 100 pF.
- STORE ..... Low (true) during the last 1 microsecond of the BUSY signal. Available fanout: 10 logic loads. Maximum capacitive load: 1000 pF.
- Output Enable ..... High (true) during the time ADC data is on the E-Bus (1.90 microseconds). Available fanout: 20 logic loads. Maximum capacitive load: 100 pF.

Digital Inputs
- EXT START ..... 1 K ohms to +5V, Lower to start ADC must raise and relower to restart ADC.
- EXT SENSE ..... 5.6 ohms to +5V, Low true sense input. Computer may test the status of this input with a SEN 2YY instruction.

Power ..... +15 Vdc ±0.1%; 150 mA
-15 Vdc ±1%; 150 mA
-22 Vdc ±2%; 2 mA
+5 Vdc ±5%; 1275 mA

Temperature Range
- Specification ..... 0°C to 50°C
- Operating ..... -10°C to 70°C
- Storage ..... -55°C to 85°C

Physical Characteristics: Dimensions: One printed circuit board 7¾ x 12 x ½ inches
Connectors: One 122-terminal Card Edge connector
Two 44-terminal Card Edge connectors

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