VARIAN 620/L-100

MAINTENANCE MANUAL

Specifications Subject to Change Without Notice

varian data machines/a varian subsidiary

98 A 9905 151

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FOREWORD

This manual contains hardware maintenance information for the Varian Data machines 620/L-100 computer system. The manual is intended to be used in conjunction with the 620-100 Reference Handbook (document number 98 A 9905 003) and the 620 Test Programs Manual (98 A 9952 060). The reference handbook contains information on overall system capabilities and a comprehensive description of the 620/L software. The test programs manual describes the various test programs that are available for testing and maintaining the 620/L-100 computer system.

This manual is divided into chapters. Chapter I contains computer specifications and documentation.

Installation information found in chapter II consists of system layout, physical descriptions, interconnection information, and system interrupt priority data.

Chapter III provides operations information including preliminary operating procedures and control panel operation information.

Chapters IV and V contain a functional description, and theory of operation and maintenance information for the central processing unit (CPU) and memory.

Chapter VI describes the direct memory access and interrupt circuits, and consists of functional descriptions, interface data, theory of operation, and maintenance information.

The theory of operation and maintenance information for the power supply are present in chapter VII.

FOREWORD

Chapter VIII contains a description of the signal mnemonics found in the 620/L-100 logic diagrams.

Timing waveforms for various instructions and operations executed by the computer are in chapter IX.

Chapter X describes the multiply/divide and extended addressing feature.

Volume 2 of this manual is assembled at the time of computer shipment to reflect a particular system configuration. It consists of engineering documents such as assembly and installation drawings, logic diagrams, and wire lists.

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CHAPTER I

INTRODUCTION

SECTION 1
SPECIFICATIONS

Specifications for the 620/L-100 computer are listed in table I-1.

Table I-1. 620/L-100 Computer Specifications

Parameter	Description	
Type	A system computer, general-purpose, digital, designed for on-line data system requirements	
Memory	Magnetic core, 16 bits, 950 nanoseconds full cycle, 425 nanoseconds access time, 4,096 words minimum, expandable to 32,768 words	
Arithmetic	Parallel, binary, fixed point, two's complement	
Word Length	16 bits	
Speed (Fetch and Execute)	Add or Subtract	1.9 microseconds
	Multiply	9.5 microseconds
	Divide	9.5 to 13.2 microseconds
	Register change	0.95 microsecond
	I/O from A or B Register	1.9 microseconds
	I/O from Memory	2.85 microseconds
Addressing Modes	Direct, to 2,048 words Relative to P Register, to 512 words Indexed with X or B Register (does not add to execution time) Multi-level indirect Immediate Extended	

Table I-1. 620/L-100 Computer Specifications *(continued)*

Parameter	Description
Instruction Types	Single Double word Generic Micro-command
Instruction	Over 100 standard commands, plus more than 128 macro-instructions
Operation Registers	A Register: 16-bit register used as the high-order accumulator and for I/O transfers
	B Register: 16-bit register used as the low-order accumulator, index register, and for I/O transfers
	X Register: 16-bit index register
	P Register: 16-bit program counter
	U Register: 16-bit instruction register
Auxiliary Registers	L Register: 15-bit memory address register
	W Register: 16-bit memory data register
	S Register: 5-bit shift register
	R Register: 16-bit operand register
Logic and Signals	Integrated circuits, 4.211-MHz clock. Internal logic levels: 0 volt is false (ZERO), +5 volts is true (ONE). Memory data logic levels: 0 volt is true (ONE), +5 volts is false (ZERO). I/O bus logic levels: +3 volts is false (ZERO), 0 volts is true (ONE)

Table I-1. 620/L-100 Computer Specifications *(continued)*

Parameter	Description
Control Panel	Register entry switches and display indicators for all operation registers; three sense switches; instruction repeat, single step, run, system reset, disable, and power on/off switches
Input/Output	Programmed I/O operations include external control, program sense, input data transfer, and output data transfer. Direct memory access facility provides automatic data transfer (382,720 words maximum per second) between memory and peripherals. I/O interrupts allow computer options to interrupt the CPU
Computer Options	620/L-05 Memory Protection 620/L-15 Loader Protection
Software	SYMBOLIC ASSEMBLER: Modular two-pass symbolic assembler operating in the basic 4,096-word memory, includes 17 basic pseudo-operations; the 8,192-word memory version includes over 30 pseudo-operations FORTRAN: Modular one-pass compiler; subset of ANSI FORTRAN for 8,192-word memory

Table I-1. 620/L-100 Computer Specifications *(continued)*

Parameter	Description
	AID: Program analysis package that assists programmers in operating the machine and debugging other programs, includes basic operational executive subroutines
	DIAGNOSTICS: Software package that provides fast off-line verification of computer and peripheral operation and assists in isolating and correcting suspected faults
	SUBROUTINES: Complete library of basic mathematical, fixed- and floating-point, single- and double-precision, number conversion and peripheral communication subroutines plus provisions for adding application-oriented routines
	MOS: The master operating system (MOS) provides for automatic batch processing that includes a minimum 8K core
	BASIC: BASIC is an easy-to-use programming language for business and scientific applications, permitting an inexperienced operator to program the system with only a few hours training
	RPG IV (optional): The report program generator (RPG IV) system, a hardware/software package, produces reports, financial statements, sales records, and other commerical documents in tabular form

Table I-1. 620/L-100 Computer Specifications *(continued)*

Parameter	Description
Dimensions	The mainframe and expansion chassis are 10.5 inches (26.6 cm) high, 13 inches (32.9 cm) deep, and 19 inches (48.1 cm) wide. The power supply is 10.5 inches (26.6 cm) high 7.5 inches (18.9 cm) deep, and 17.75 inches (44.9 cm) wide
Weight	The mainframe and expansion chassis each weigh approximately 35 pounds (without circuit cards); the power supply weighs approximately 36 pounds
Input Voltage	105 to 125V ac or 210 to 250V ac at 50 or 60 Hz (For compatibility with the Teletype, frequency must be either 50 or 60 (+1/2, 0) Hz.)
Input Current	The power supply requires 5 amperes of ac current at 115 volts, and 3 amperes at 230 volts
Temperature	
Operating	0 to 50 degrees C
Storage	20 to 70 degrees C
Humidity	
Operating	To 90 percent without condensation
Storage	To 95 percent without condensation
Vibration	3 to 10 Hz at 1g force or 0.25 double amplitude, whichever is less. Exponentially raised frequency from 3 to 10 Hz and back to 3 Hz over a 10-minute period, three complete cycles. This specification applies for all three principal axes
Shock	4g for 5 to 11 milliseconds, essentially sine shock waveform (all three principal axes, both directions in each axes)

SECTION 2
TECHNICAL MANUALS

To ensure full utilization of the 620/L-100 computer, technical manuals (including this manual) are provided with each computer. The applicable manuals and corresponding part numbers are listed below.

Title	Document No.
620-100 Reference Handbook	98 A 9905 003
620/L-100 Maintenance Manual	98 A 9905 151
620 Test Programs Manual	98 A 9952 061
620/L-100 Teletype Controller Manual	98 A 9905 160

Information for the computer options and peripheral controller options is provided in the corresponding 620/i option manuals with addendum sheets indicating minor differences for the 620/L-100 computer system. In addition, manufacturers' technical manuals for peripheral devices such as Teletypes and magnetic tape units are also provided.

CHAPTER II

INSTALLATION

SECTION 1
SYSTEM LAYOUT AND PLANNING

1.1 COMPUTER CHASSIS

There are two types of chassis in the 620/L-100: the mainframe chassis and the expansion chassis.

1.1.1 Mainframe

The mainframe contains the basic computer hardware: the CPU, memory, and control panel. Mainframe memory size can be either 8,192 words (8K) or 4,096 words (4K). The mainframe can also accommodate the internal computer options and various peripheral controllers.

1.1.2 Expansion Chassis

Three versions of the expansion chassis are available for additional memory, peripheral controllers, or a combination of both. A single expansion chassis can accommodate up to 24K of memory, or up to 22 peripheral controller cards. For further I/O expansion, more than one I/O expansion chassis can be installed in a single computer system.

1.2 POWER AND ENVIRONMENTAL REQUIREMENTS

One power supply provides power for the CPU, 32K of memory, and all the internal options. A second power supply is normally required when peripheral controller cards are added.

The power supplies are contained in individual chassis. They connect to a standard 115-volt, 60-Hz power source. Also available, for European installations, are power supplies for use with 230-volt, 50-Hz sources. Power regulation is not required under normal commercial power conditions. With maximum loads, the power supply draws approximately 5 amperes of ac line current.

Ambient temperature at the installation site can vary between 0 and 50 degrees C with no adverse effects on computer operations. To extend the life expectancy of the computer, however, it is recommended that ambient temperature be maintained between 15 and 30 degrees C.

Relative humidity can be up to 90 percent (without condensation).

1.3 SPACE REQUIREMENTS

The mainframe, expansion chassis, and power supply are contained in individual cabinets suitable for rack-mounted or table-top installation. For equipment-rack installation, the power supply is normally mounted in a hinged, swing-down chassis at the rear of the mainframe or expansion chassis. The power supply should be mounted to provide easy access to adjustment controls, test points, and power switch (see installation drawing 93D0275 in volume 2).

Both the mainframe and expansion chassis are 10.5 inches (26.6 cm) high, 13 inches (23 cm) deep, and 19 inches (48.1 cm) wide. The power supply is 6.0 inches (15.2 cm) high, 10.2 inches (26 cm) deep, and 17.75 inches (45 cm) wide. The standard 33 ASR TTY unit with stand is approximately 33 inches (83.5 cm) high, 19 inches (48.1 cm) deep, and 22 inches (55.7 cm) wide.

The memory expansion chassis must be located directly above or below the mainframe. An expansion chassis containing only peripheral controllers; however, does not have to be located directly adjacent to the mainframe as I/O expansion cables are available in various lengths up to 20 feet (6m). The dc power cable connecting the power supply to the mainframe (or expansion chassis) is 6 feet (1.8m) in length.

SECTION 2
PHYSICAL DESCRIPTION

2.1 MAINFRAME

The mainframe (part number 01P1035) contains a control panel, a connector panel, and card slots for CPU, memory, internal options, and various peripheral controller cards. A fan is located underneath the left portion of the mainframe (viewed from the front) to provide cooling for the electronic components. All wiring for the circuit cards is contained on a wiring plane located behind the control panel.

2.1.1 Control Panel

The molded plastic control panel contains all controls and indicators necessary to operate the computer. The printed circuit display card (part number* 44P0515) mounted behind the panel contains lamps, switches, and associated circuitry for the control indicators. The lamps can be replaced without soldering. As illustrated in figure II-1, the display card connects to the CPU via two flat cables that connect to J27 and J28 on the mainframe backplane.

* The words *part number* will not precede the number in the remaining text.

The control panel is hinged to the front of the mainframe. To unlatch the panel, push the pushbutton fastener on the left side. The control panel can then be opened to expose the mainframe wiring.

2.1.2 Connector Panel

The connector panel (figure II-2) is located at the rear of the mainframe and contains power connector J30 and Teletype connector J31. An optional I/O feature consists of an internal I/O harness assembly (53P0571) that is wired between slot 26 and an optional I/O connector J32. This feature allows the user to connect his own equipment directly to the 620/L I/O lines. Additional connectors can be added to the connector panel for special user requirements.

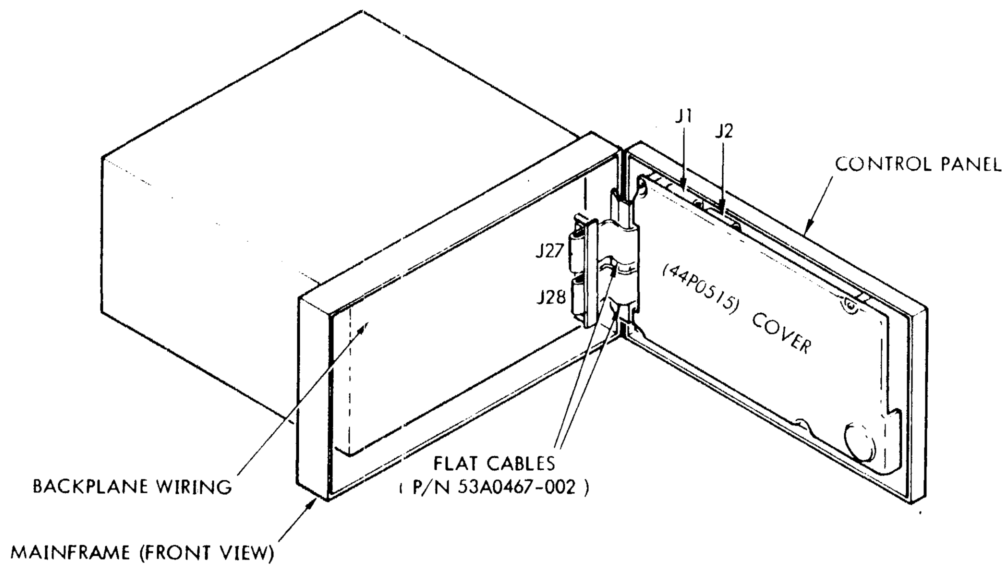

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Figure II-1. Mainframe With Open Panel

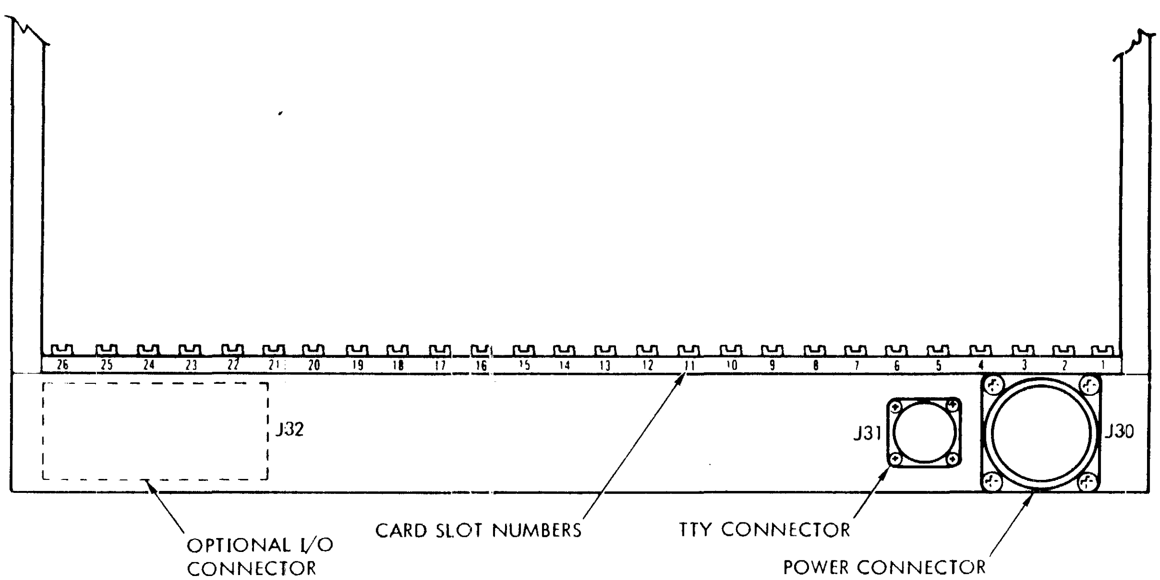

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Figure II-2. Mainframe Connector Panel

2.1.3 Circuit Cards

The mainframe contains 26 card slots to accommodate circuit cards and circuit-card connectors for expansion cables (refer to figure II-3). Card slot assignments are listed in table II-1.

Except for the memory stack card, the cards are 7-3/4-by-12-inches (19.7 x 30.3 cm), each containing a 122-pin connector for mounting into the mainframe/backplane connectors. The cards are installed through the rear of the mainframe with the component side on the left (except for the memory stack card for which the component side is on the right). Card slot 18 is normally not wired; however, it can be used for special options (such as memory protection) or peripheral controllers that require an additional slot.

The connectors at both ends of the memory expansion cable consist of printed circuit cards. One circuit card connector plugs into slot 1 of the mainframe, the other into slot 2 of the expansion chassis. The same type of cable is used for I/O expansion. The I/O expansion cable plugs into slot 26 of the mainframe and slot 13 of the right half of the expansion chassis (viewed from the front).

Table II-1. Mainframe Card Slot Assignments

Card Slot	Part No.	Card Name
1*	---	Memory expansion connector and memory stack
2	44P0506	Sense/inhibit
3	44P0578	Driver/sink switch
4*	---	Memory stack
5	44P0506	Sense/inhibit
6	44P0599	Memory timing control
7	44P0592	Register
8	44P0592	Register
9	44P0592	Register

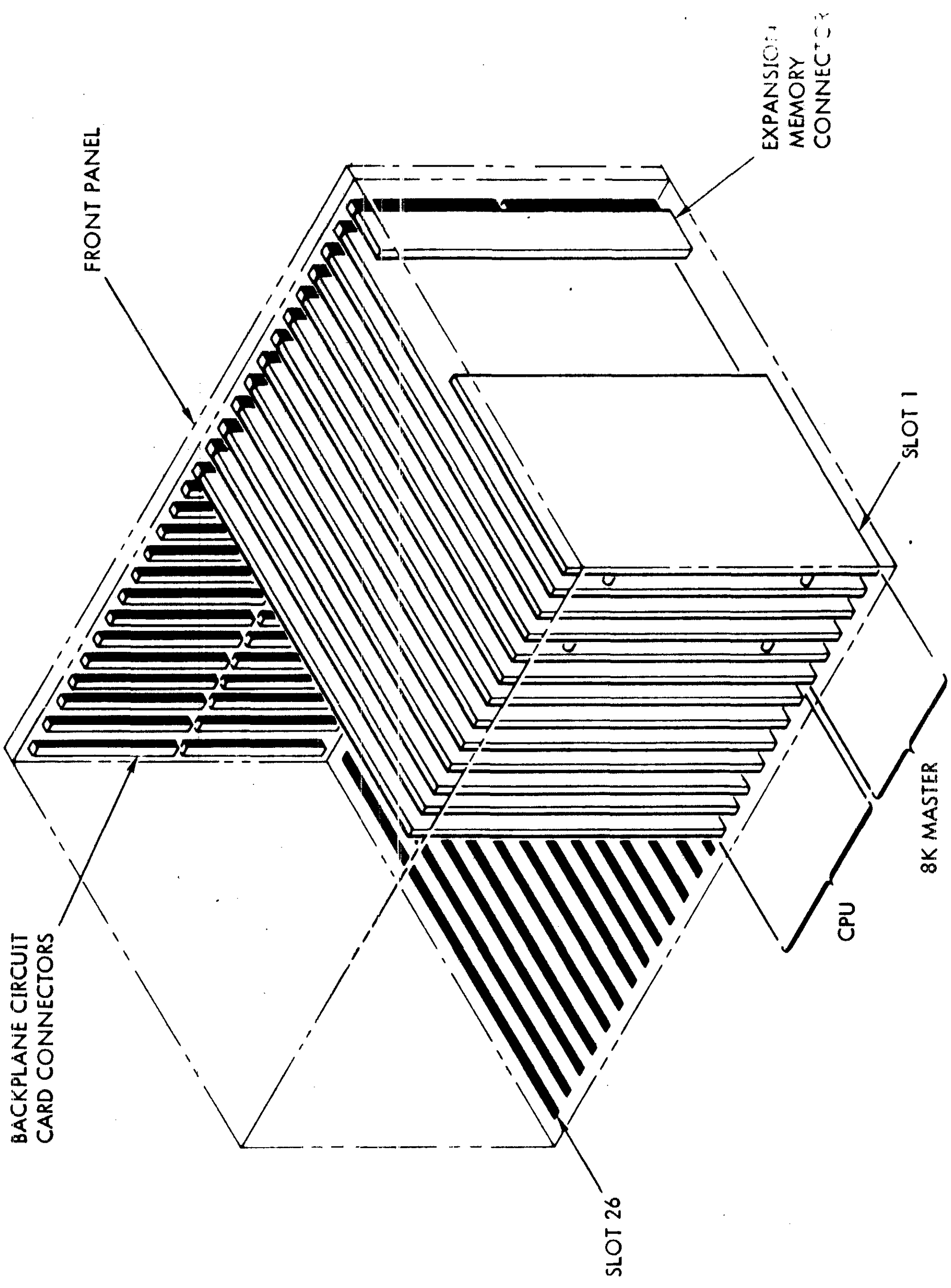

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Figure II-3. Mainframe Circuit Card Installation

Table II-1. Mainframe Card Slot Assignments *(continued)*

Card Slot	Part No.	Card Name
10	44P0595	Processor control 1
11	44P0596	Processor control 2
12	44P0597	Processor control 3
13	44P0593	Processor control 4
14	44P0594	Multiply/divide and extended addressing
15	44P0598	Direct memory access and interrupt
16	44P0237	Automatic memory enable/disable, or optional power failure/restart and real-time clock
17	44P0013	Teletype controller
18	---	Not wired
19-25	---	Peripheral controllers
26	---	I/O expansion connector

* The memory stack card occupies this card slot space but does not plug into the slot connector; it plugs into a right-angle connector mounted on the sense inhibit card.

2.2 EXPANSION CHASSIS

The expansion chassis contains a front panel, a connector panel, and card slots for memory and/or peripheral controller cards. Fans are installed in the bottom of the expansion chassis to provide cooling for the memory cards; one fan for the first 8K memory, and an additional fan if the chassis contains 16K or 24K. No fans are provided in an expansion chassis containing only peripheral controllers.

The card-slot numbers in the expansion chassis are divided into two sets of 13. When viewed from the rear, the numbers run 1 through 13 from right to left. The circuit cards are installed in the expansion chassis in the same manner as in the mainframe (refer to section 2.1.3).

2.2.1 Front Panel

The front panel is blank and mounted on hinges. To unlatch the front panel, press the pushbutton fastener on the left side. The panel can then be opened to expose the chassis wiring.

2.2.2 Connector Panel

The connector panel (figure II-4) is located at the rear of the expansion chassis and contains power connector J30 which routes power to the expansion memories and peripheral controllers. An optional I/O feature consists of an internal I/O harness assembly (53P0571) that is wired to the optional I/O connector J32 This feature allows the user to connect his own equipment directly to the 620/L-100 I/O lines. Additional connectors can be added to the connector panel for special user requirements.

2.2.3 Memory Expansion

Memory is expanded with 8K or 4K slave memory modules which are installed in the expansion chassis. An 8K slave module is the same as the 8K master module (in the mainframe) except that it has no timing and control circuit card (44P0599). A 4K slave module is the same as an 8K slave module except it has only one sense/inhibit card (44P0599) and one stack card. A memory buffer card (44P0521) is required for a memory size larger then 8K.

Computer systems with memory sizes of 12K, 16K, 20K, or 24K require an expansion chassis that contains left-half memory-expansion wiring (01P1312). Computer systems with memory sizes of 28K and 32K require that the expansion chassis also contain right-half memory-expansion wiring (01P1314). Table II-2 lists the hardware required in the mainframe and expansion chassis for the various memory sizes. Table II-3 lists the card slot assignments for the expansion chassis memory cards.

Table II-2. Memory Expansion Hardware

	Mainframe			Expansion Chassis				
Hardware	**4K**	**8K**	**12K**	**16K**	**20K**	**24K**	**28K**	**32K**
4K data module, 01C1065*	1	1	1	1	1	1	1	1
Timing card, 44P0599	1							
Driver/sink card, 44P0578	1		1		1		1	
Buffer card, 44P0521**			1					
Expansion cable, 53P0547**			1					
Left-half memory expansion, 01P1312**			1					
Right-half memory expansion, 01P1314***							1	

* A 4K data module consists of one sense inhibit card and one stack card.

** Part of Memory Backplane Option-LH (01P1311)

***Part of Memory Backplane Option-RH (01P1313)

Table II-3. Expansion Memory Card Slot Assignment

	Slot	Card		
	1	Blank		
	2	Memory expansion connector		
	3	Memory buffer card		
	4*	Memory stack card	1st	
Left-half	5	Sense inhibit card	4K	1st
memory expansion,	6	Driver/sink switch card		8K
01P1312	7*	Memory stack card	2nd	
	8	Sense inhibit card	4K	
	9*	Memory stack card	3rd	
	10	Sense inhibit card	4K	2nd
	11	Driver/sink switch card		8K
	12*	Memory stack card	4th	
	13	Sense inhibit card	4K	
Right-half	6*	Memory stack card	5th	
memory expansion,	7	Sense inhibit card	4K	3rd
01P1314	8	Driver/sink switch card		8K
	9*	Memory stack card	6th	
	10	Sense inhibit card	4K	

* The memory stack card occupies this card slot space but does not plug into the slot connector; it plugs into a right-angle connector mounted on the sense inhibit card.

2.2.4 I/O Expansion

An expansion chassis equipped with right-half I/O wiring (01A1116) can be used to provide 12 controller card slots. If additional space is required, the chassis can also be equipped with left-half I/O wiring (01A1117) to provide an additional ten controller card slots.

The standard computer contains drivers and receivers to accommodate ten peripheral controllers. For additional drivers and receivers, a I/O buffer card (44P0254) is available and is normally installed in slot 18 of the mainframe. The last card slot must contain an I/O termination shoe (44P0530) which consists of 150-ohm resistors connected to +3 volts.

2.3 POWER SUPPLY

The power supply provides power for the CPU, 32K of memory, and all internal options. The power supply is contained in a standard rack-mountable chassis, normally installed behind or near the mainframe or expansion chassis. A fan at one end of the power supply provides cooling for the electronic components.

The top panel of the power supply (figure II-5) contains test points and adjustment controls for the +5, -5, +12, and -12 voltages. The bottom panel of the power supply (figure II-6) contains the on-off switch, the ac power cord, and the terminal board that connects to the dc power cable (53P0569). The terminal board pin assignments are as follows:

Pin	Function
1	115V fan
2	115V fan
3	AC return
4	AC out
5	Relay coil
6	Relay Return
7	+12V
8	Common

Pin	Function
9	Common
10	- 12V
11	+ 5V
12	+ 5V
13	- 5V
14	Data guard

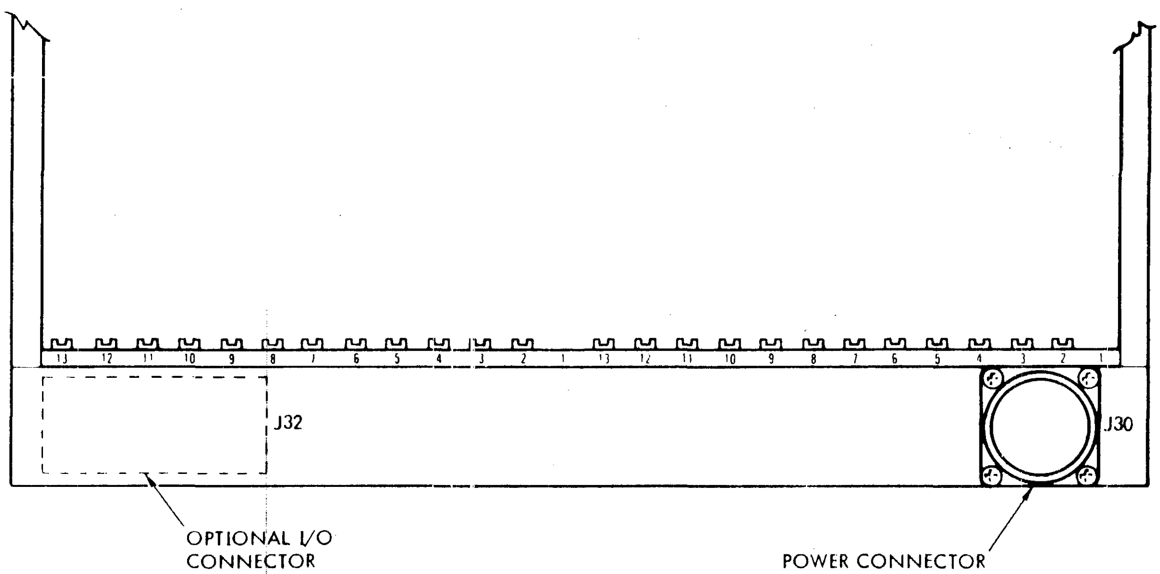

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Figure II-4. Expansion Chassis Connector Panel

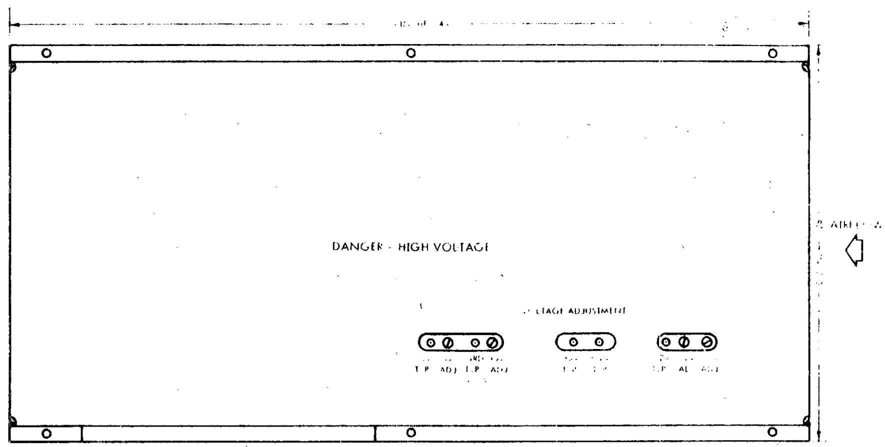

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Figure II-5. Power Supply Top Panel

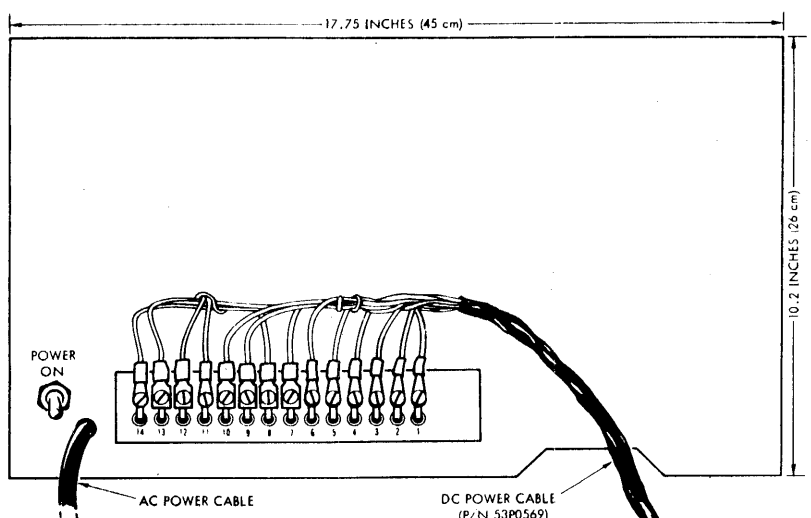

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Figure II-6. Power Supply Bottom Panel

SECTION 3
SYSTEM INTERCONNECTION

3.1 MEMORY EXPANSION INTERCONNECTION

As illustrated in figure II-7 the memory expansion chassis is connected to the mainframe by a short flat cable with a 122-pin card connector at both ends. The cable (53P0547) plugs into card slot 1 of the mainframe and card slot 2 of the expansion chassis. Only one memory expansion chassis is required in each system, and it must be located directly above or below the mainframe.

3.2 I/O EXPANSION INTERCONNECTION

The I/O expansion chassis is connected to the mainframe by the type of cable (53P0547) used in memory expansion (refer to figure II-8). However, the cable used for I/O expansion is available in various lengths up to 20 feet (6m). The cable plugs into card slot 26 of the mainframe and slot 13 of the expansion chassis. An I/O termination shoe card (44P0530) is installed in the last card slot of the expansion chassis.

3.3 POWER SUPPLY INTERCONNECTION

The power supply is connected to the mainframe and expansion chassis by a dc power cable (53P0569) as illustrated in figures II-7 and II-8. The power cable is 34 inches long and connects J30 on the rear of the mainframe or expansion chassis to the terminal board on the power supply. When one power supply provides power for both the mainframe and an expansion chassis (as in the two illustrations), two power cables are connected to the terminal board of the power supply.

3.4 TELETYPE INTERCONNECTION

The Teletype cable (53P0016) is normally 20 feet (6m) long and connects J31 on the rear of the mainframe to the Teletype unit.

For the model 33 ASR, the cable connects to an S connector labled 2 in the Teletype unit. The S connector location is at the right rear, top row, second connector from the right.

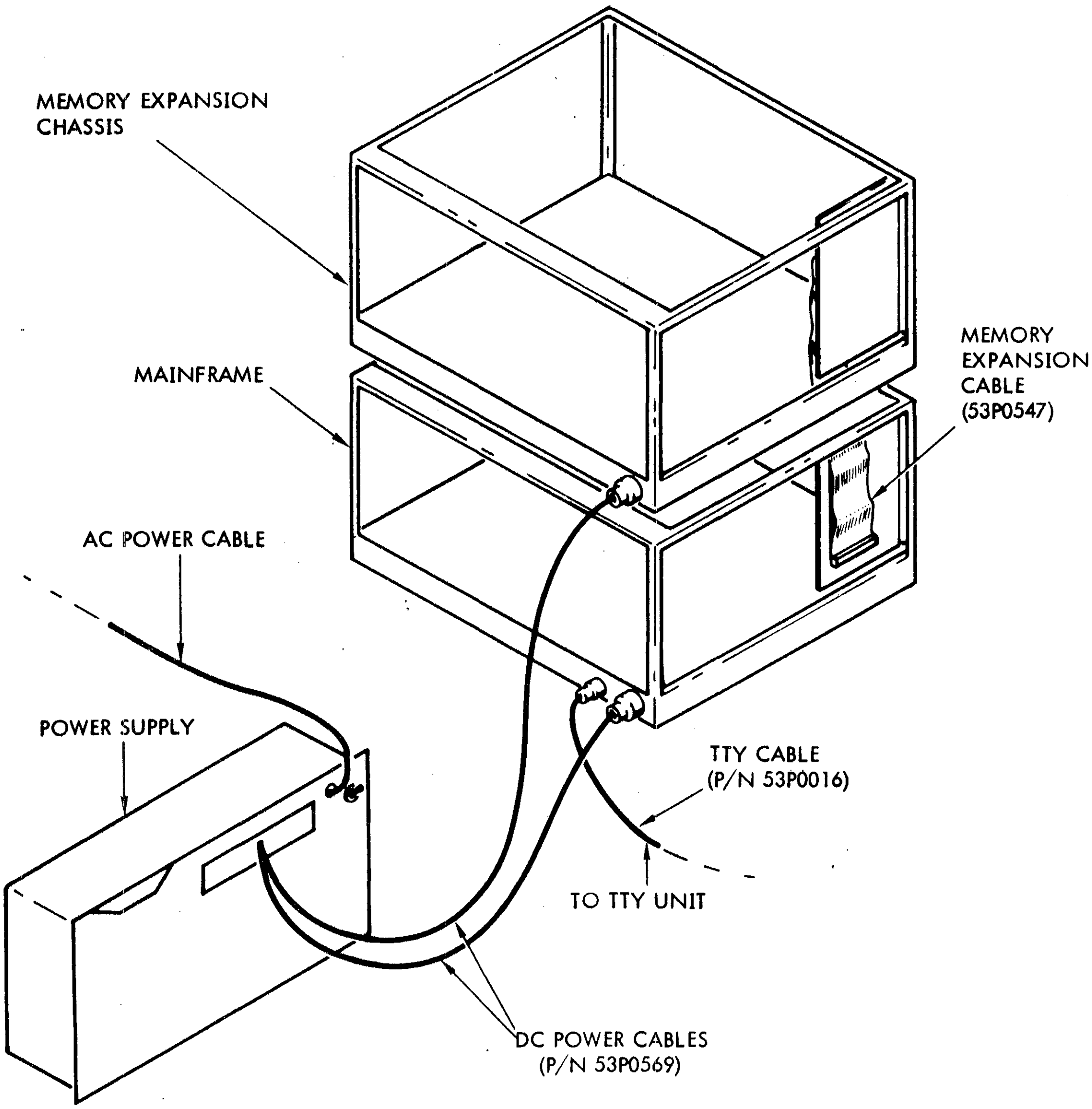

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Figure II-7. Memory Expansion Interconnection

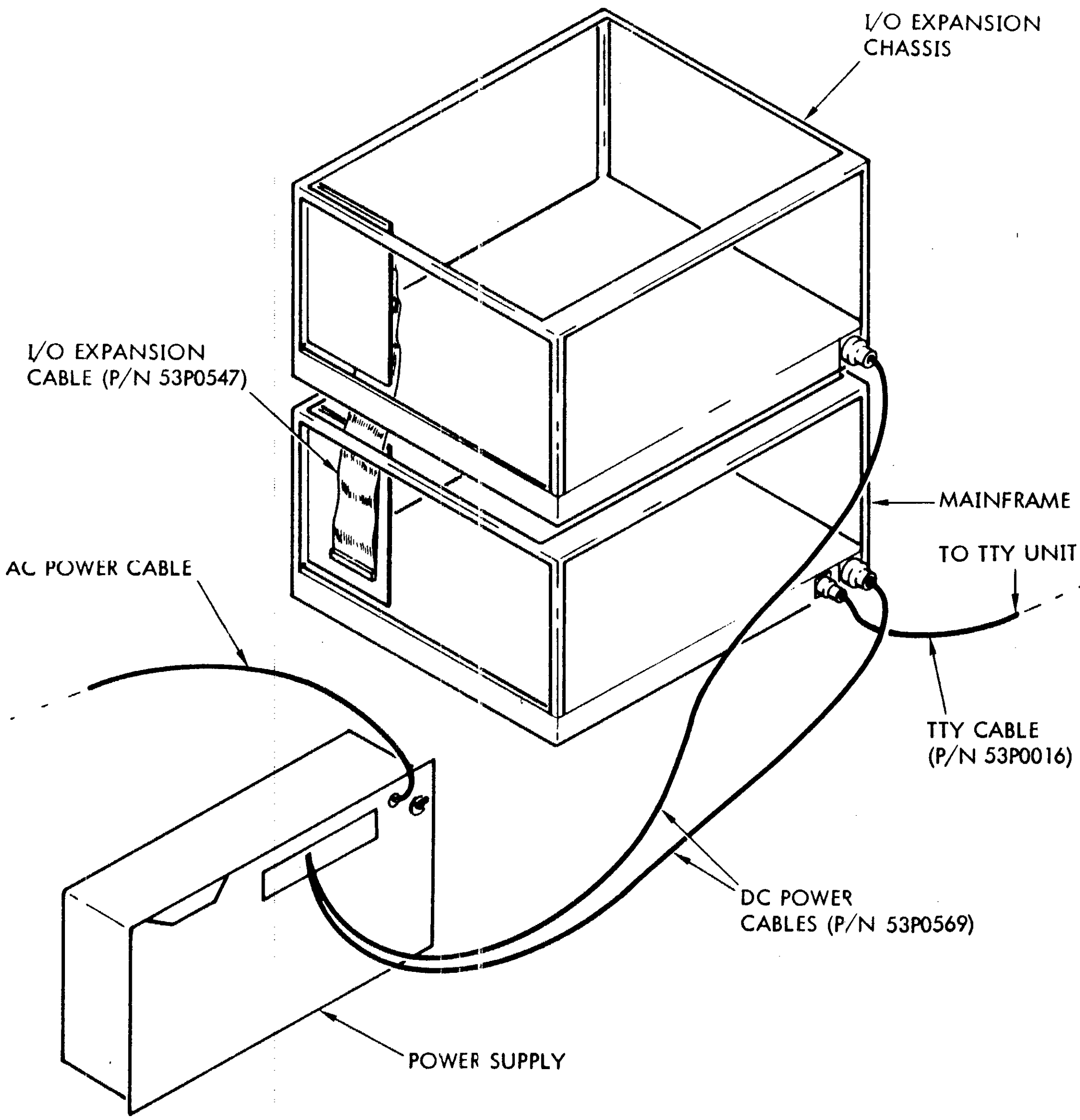

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Figure II-8. I/O Expansion Interconnection

For models 35 ASR and 35 KSR, the cable is wired directly to a power terminal block in the Teletype unit. The terminal block is located at the right lower rear of the cabinet behind the Teletype print mechanism.

3.5 CABLE PIN ASSIGNMENTS

Tables II-4 through II-8 list pin assignments for the following system interconnection cables:

a. Memory expansion
b. I/O expansion
c. DC power
d. 33 ASR Teletype
e. 35 ASR and 35 KSR Teletypes

Table II-4. Memory Expansion Cable Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	GRD	21	GRD	41	GRD
2	---	22	L09X +	42	W03X –
3	GRD	23	GRD	43	GRD
4	L00X +	24	L10X +	44	W04X –
5	GRD	25	GRD	45	GRD
6	L01X +	26	L11X +	46	W05X –
7	GRD	27	GRD	47	GRD
8	L02X +	28	L12X +	48	W06X –
9	GRD	29	GRD	49	GRD
10	L03X +	30	L13X +	50	W07X –
11	GRD	31	GRD	51	GRD
12	L04X +	32	L14X +	52	---
13	GRD	33	GRD	53	GRD
14	L05X +	34	---	54	---
15	GRD	35	GRD	55	GRD
16	L06X +	36	W00X –	56	SASX –
17	GRD	37	GRD	57	GRD
18	L07X +	38	W01X –	58	RXXX –
19	GRD	39	GRD	59	GRD
20	L08X +	40	W02X –	60	WRTX +

Table II-4. Memory Expansion Cable Pin Assignment *(continued)*

Pin	Signal	Pin	Signal	Pin	Signal
61	GRD	82	W13X –	103	GRD
62	---	83	GRD	104	RSTM –
63	GRD	84	W14X –	105	GRD
64	SSL1 –	85	GRD	106	---
65	GRD	86	W15X –	107	GRD
66	SSL2 –	87	GRD	108	---
67	GRD	88	MSCE +	109	GRD
68	SSL3 –	89	GRD	110	INHE – 1
69	GRD	90	MSPX +	111	GRD
70	SSL4 –	91	GRD	112	INHE – 0
71	GRD	92	WSTX –	113	GRD
72	W08X –	93	GRD	114	---
73	GRD	94	RWT1 –	115	GRD
74	W09X –	95	GRD	116	---
75	GRD	96	FCYX +	117	GRD
76	W10X –	97	GRD	118	---
77	GRD	98	TCRX –	119	GRD
78	W11X –	99	GRD	120	---
79	GRD	100	RWT2 –	121	GRD
80	W12X –	101	GRD	122	GRD
81	GRD	102	---		

Table II-5. I/O Expansion Cable Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal
1	GRD	24	RT06 –	47	IUJX – I
2	EB00 – I	25	---	48	GRD
3	RT01 –	26	RT07 –	49	TRQX – B
4	EB01 – I	27	FRYX – I	50	TROX – B
5	RT02 –	28	RT08 –	51	RT15 –
6	EB02 – I	29	DRYX – I	52	BCDX – B
7	RT03 –	30	RT09 –	53	RT16 –
8	EB03 – I	31	SERX – I	54	CDCX – B
9	RT04 –	32	RT10 –	55	RT17 –
10	EB04 – I	33	TPIX – I	56	DCEX – B
11	EB05 – I	34	RT11 –	57	RT18 –
12	EB06 – I	35	TPOX – I	58	TAKX – B
13	EB07 – I	36	RT12 –	59	RT19 –
14	EB08 – I	37	---	60	DESX – B
15	EB09 – I	38	RT13 –	61-73	---
16	EB10 – I	39	---	74	DAG5
17	EB11 – I	40	RT14 –	75-99	---
18	EB12 – I	41	---	100	GRD
19	EB13 – I	42	---	101-115	---
20	EB14 – I	43	SYRT – I	116	+3V dc
21	EB15 – I	44	IUAX – I	117-121	---
22	RT05 –	45	IUCX – I	122	GRD
23	---	46	IURX – I		

Table II-6. DC Power Cable Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal
1	---	7	Relay coil	13	− 12V
2	---	8	AC return	14	+ 5V
3	AC out	9	---	15	− 5V
4	Relay return	10	Data guard	16	Common
5	115V fan	11	---	17	Common
6	115V fan	12	+ 12V		

Table II-7. 33 ASR Teletype Cable Pin Assignment

J31 End	Teletype End (P2)	Controller Pin	Signal
1	9	113	Return
2	6	112	Receive
3	8	114	Send

Table II-8. 35 ASR and 35 KSR Teletype Cable Pin Assignment

J31 End	Teletype TB End	Controller Pin	Signal
1	4	113	Return
2	5	112	Receive
3	7	114	Send

SECTION 4
SYSTEM INTERRUPT PRIORITY

4.1 GENERAL

System interrupt priority is established by the connecting of various computer devices in a priority chain. Devices that can be included in the priority chain are: power failure/ restarts (PF/R), memory protection (MP), real-time clock (RTC), priority interrupt module (PIM), and buffer interlace controller (BIC). Peripheral controllers do not generate interrupt requests; this function is performed with the PIM.

Normally, the priority assignments are wired at the factory before the equipment is delivered; however, a description is presented in this section for the user who wishes to augment or change his system. The interrupt priority assignment is unique for each computer system and specific information concerning each system is included as part of the installation instructions delivered with the equipment.

4.2 INTERCONNECTION

Interconnection of devices located in the same chassis is accomplished by connecting the priority-out signal (PRNX-I) of the first priority device to the priority-in signal (PRMX-I) of the next lower-priority device. This process continues until all subsequent priorities within the chassis are assigned. The priority-in signal of the first-priority device is connected to ground.

To establish a priority chain for devices in separate chassis, four priority lines are available in the I/O expansion cable and are wired into the computer as required. The designation and cable pin assignments of the priority lines are as follows:

Signal	I/O Cable Pin
PR1X - I	37
PR2X - I	39
PR3X - I	41
PR4X - I	42

Figure 11-9 illustrates typical interrupt priority connections for a computer system containing the PF/R, RTC, and PIM in the mainframe, and two BICs in an expansion chassis.

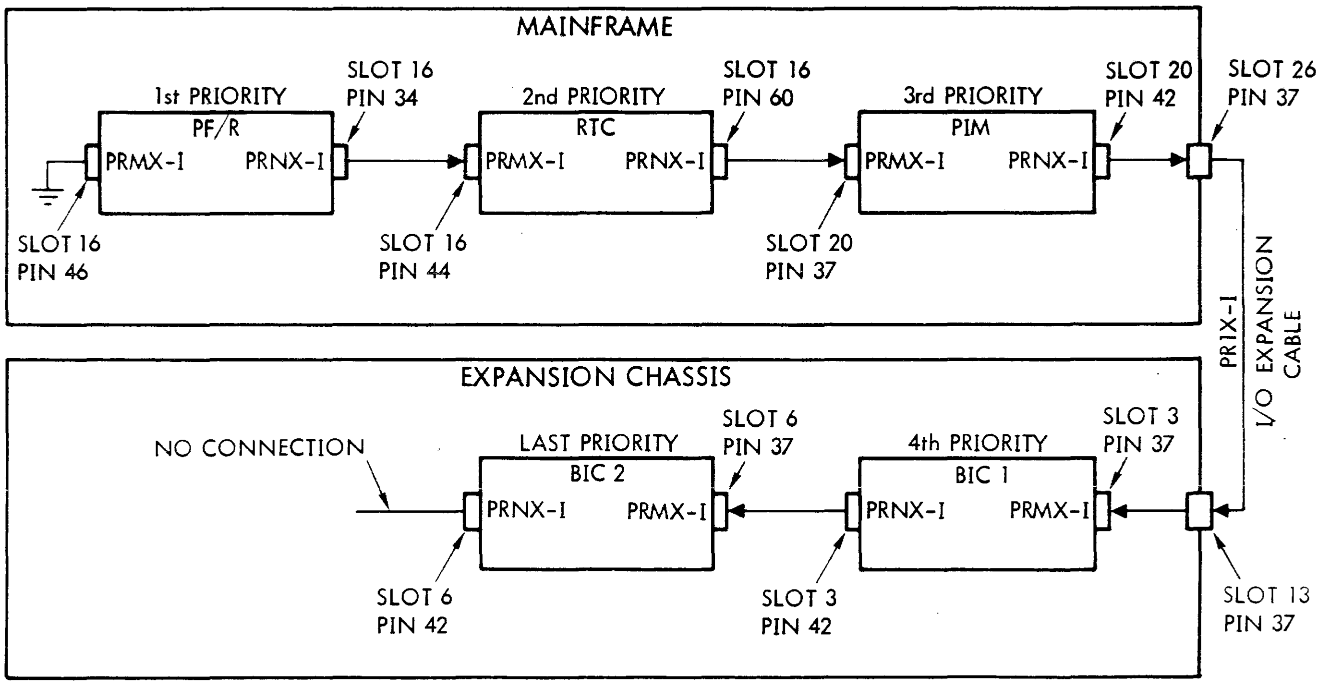

Figure II-9. Typical System Interrupt Priority Connector

CHAPTER III

OPERATION

SECTION 1
CONTROL PANEL OPERATION

1.1 GENERAL

This section describes the operation of the 620/L-100 control panel switches and indicators (refer to figure III-1).

1.2 POWER SWITCH

The power switch is a key-operated switch controlling the application of ac line voltage to the computer power supply. In the OFF position, no ac line voltage is applied to the computer power supply. In the PWR ON position, ac line voltage is applied to the computer power supply which in turn applies dc power to the computer. In the CONSOLE DISABLE position, dc power is applied to the computer; however, all control panel switches are disabled except the power switch itself. Pressing any other switch while the power switch is in CONSOLE DISABLE has no affect. The control panel indicator lights are functional when the power switch is in either the PWR ON or CONSOLE DISABLE position.

The key can be removed from the power switch in any of the three positions. To turn off the computer, place the power switch in the PWR ON position, press the STEP switch, then turn the power switch to OFF.

1.3 STEP SWITCH AND INDICATOR

The STEP switch is a momentary, spring-loaded switch. Pressing it when the computer is in run mode causes the computer to halt after execution of the current instruction. Pressing the STEP switch when the computer is halted executes the instruction in the U register.

When the STEP switch is activated, the STEP indicator lights. The STEP indicator goes out when the RUN switch is activated.

1.4 RUN SWITCH AND INDICATOR

The RUN switch is a momentary, spring-loaded switch. Pressing it starts the program at the location specified by the P register, after execution of the instruction in the U register.

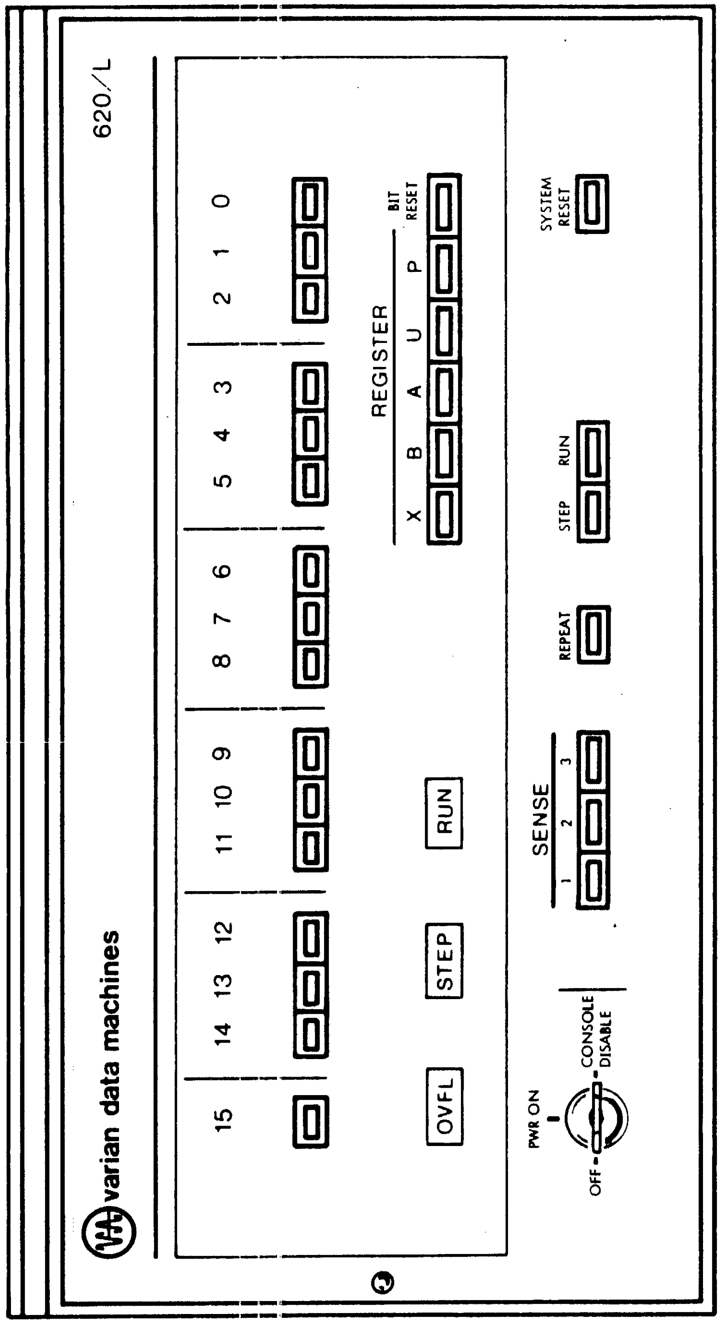

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Figure III-1. 620/L Computer Control Panel

When the RUN switch is activated, the RUN indicator lights. The RUN indicator goes out when the STEP switch is activated.

1.5 REGISTER SWITCHES

The REGISTER switches consist of five toggle switches used to select one of five registers (X, B, A, U, and P) for display or entry. A register is selected by pressing down on the appropriate REGISTER SWITCH. Only one register can be selected at a time; selection of two or more registers simultaneously disables the selection logic and the register display.

1.6 BIT RESET SWITCH

The BIT RESET switch is a momentary, spring-loaded switch. Pressing it when the computer is in step mode causes all bits of the selected register to be reset and all the register display indicators to go out.

1.7 REGISTER ENTRY SWITCHES AND DISPLAY INDICATORS

The 16 indicators across the top of the control panel display the contents of a selected register. Data are entered into registers on the corresponding register entry switches located under the indicators. The indicators and switches are read from left to right, bits 15 to 0. An illuminated indicator shows that that bit contains a one. For negative data, the sign bit (bit 15) is a one. The indicators and switches are divided into groups of three for ease in reading octal configurations.

1.7.1 Register Display

To display the contents of a register, press the STEP switch and press down the REGISTER switch for the desired register. The display indicators light when the register bits are set to one. To remove the display, pull up on the REGISTER switch.

1.7.2 Data Or Instruction Entry

To enter data or instructions in a register:

a. Display the contents of the selected register (section 1.7.1).

b. Clear the register by pressing the BIT RESET switch.

c. Enter ones by pressing the register entry switches corresponding to the bits to be set. For each switch pressed, the associated indicator lights. The register bits are reset by pressing the BIT RESET switch.

1.8 REPEAT SWITCH

The REPEAT switch is a toggle switch that permits manual repetition of an instruction in the U register. With the REPEAT switch in the down position, depressing the STEP switch executes an instruction and advances the P register; however, the contents of the U register are left unchanged. The REPEAT switch is disabled when the computer is in run mode.

1.9 SENSE SWITCHES

SENSE switches 1, 2, and 3 (S24, S25, S26) are toggle switches which are activated when placed in the down position. When the computer is operating in either run or step mode, the SENSE switches allow the operator to modify the program and cause the computer to perform special functions. Statements can be included in a program to test the condition of these switches and to vary program execution based on the switch settings. The three SENSE switches produce a logical AND function with bits 6 through 8 of the jump, jump and mark, or execute instruction word; consequently, they can provide various logical branches that are selected from the control console. The SENSE switches permit manual program control whenever SENSE switch jump, jump and mark, or execute instructions (JSS1, JSS2, JSS3, JS1M, JS2M, JS3M, XS1, XS2, and XS3) are performed. The indicated jump and execute operations are performed only if the corresponding SENSE switch is activated.

1.10 SYSTEM RESET SWITCH

The SYSTEM RESET switch is a momentary, spring-loaded switch used to initialize and halt the computer and its peripherals. This switch does not clear the registers.

1.11 OVFL INDICATOR

The OVFL indicator lights whenever an overflow condition exists.

SECTION 2
MANUAL OPERATIONS

2.1 GENERAL

With the computer in step mode, data or instructions can be manually transferred to or from memory, or stored programs can be manually executed.

Note that the U register contains the instruction being executed, while the P register points to the address of the instruction.

Refer to the 620-100 Reference Handbook (98 A 9905 003) for octal codes of the 620/L instructions.

2.2 LOADING WORDS INTO MEMORY

To load instruction or data words into memory, enter the desired word into the A, B, or X register. Enter the appropriate store instruction (STA, STB, or STX) with the desired operand address in the U register. Then press the STEP switch to execute the store operation.

Direct addressing is used if the specified address is located within the first 2,048 (9 through 2,047) memory locations; for memory addresses of 2,048 and above, relative addressing is used.

2.3 DISPLAYING CONTENTS OF A MEMORY CELL

To display the contents of any memory cell in the A, B, or X register, enter the appropriate load instruction (LDA, LDB, or LDX) with the proper memory address into the U register. Then press the STEP switch to load the selected word into that register. By pressing the appropriate REGISTER switch, the contents of the selected register are displayed on the register display indicators.

2.4 MANUAL PROGRAM EXECUTION

To manually execute a program stored in memory, enter the starting address of the program into the P register. Clear the U register and press the STEP switch; this loads the first instruction of the program into the U register. By pressing the STEP switch again, the instruction is executed. Pressing the STEP switch repeatedly allows the program to be stepped through one instruction at a time. All operations such as multilevel indirect addressing are performed for each instruction as the STEP switch is activated.

2.5 INSTRUCTION REPEAT

In step mode, the U register contains the next instruction to be executed when the STEP switch is activated. The P register contains the address of the next instruction to be transferred to the U register after the current instruction is executed. In some cases, it is desirable to manually execute an instruction several times. When the STEP switch is pressed with the REPEAT switch activated, U register loading is inhibited although the instruction counter is advanced each time. This mode is particularly useful for loading words into sequential memory addresses or for displaying the contents of sequential memory addresses.

2.6 LOADING WORDS INTO SEQUENTIAL MEMORY CELLS

To load a group of sequential memory cells, enter the appropriate store instruction (STA, STB, or STX) into the instruction register with the relative addressing mode* in the M field and the base address in the A field. Repeated operation of the STEP switch will store the contents of the A, B, or X register into sequential memory locations. The word loaded can be changed on each step by entering the desired value into the operation register (A, B, or X) for each step.

2.7 DISPLAYING SEQUENTIAL MEMORY CELL CONTENTS

To display the contents of a group of sequential memory cells, enter the appropriate load instruction (LDA, LDB, or LDX) in the U register in the relative addressing mode*, with the base address in the P register, and the A field of the U register equal to zero. The contents of the sequential locations are displayed in the selected operation register each time the STEP switch is activated.

* See table F-1 in appendix F for a description of the relative addressing mode.

SECTION 3
PRELIMINARY OPERATING PROCEDURES

3.1 GENERAL

This section provides preliminary operating procedures to place the computer system in a ready-to-use condition. These procedures consist of the power on, bootstrap loader, and binary load/dump routines. The bootstrap loader and binary load/dump routines must be used when a cold start is required; i.e., when the specific contents of memory are unknown to the operator.

3.2 POWER ON ROUTINE

To perform the power on routine:

a. Turn the power switch key to the PWR ON position.

b. Press the SYSTEM RESET switch to initialize the computer control circuits.

c. Clear all registers by momentarily placing each REGISTER switch in the down position and pressing the BIT RESET switch each time.

3.3 BOOTSTRAP LOADER ROUTINE

After the power on procedure is complete, the bootstrap loader routine is performed. This routine consists of manually loading several instruction codes into designated memory addresses. To load the bootstrap loader routine:

a. Load instruction 054000 (store A relative to P) in the U register.

b. Place the REPEAT switch in the down position.

c. Load the starting memory address (007756) of the bootstrap loader routine into the P register.

d. Manually load the instruction codes of the bootstrap loader routine into the A register. As each instruction is loaded, press the STEP switch. This causes the computer to load the A register contents into the address specified by the P register, which is incremented by one after each instruction is loaded.

Bootstrap loader routine instructions (BLD II) are:

Address	Paper Tape Reader Code	TTY Code	Mnemomic
007756	102637	102601	CIB
007757	004011	004011	ASLB
007760	004041	004041	LRLB
007761	004446	004446	LLRL
007762	001020	001020	JBZ
007763	007772	007772	Memory address
007764	055000	055000	STA
007765	001010	001010	JAZ
007766	007000*	007000*	Memory address
007767	005144	005144	IXR
007770	005101	005101	INCR
007771	100537	102601	CIB
007772	101537	101201	SEN
007773	007756	007756	Memory address
007774	001000	001000	JMP
007775	007772	007772	Memory address

* Data to be 07600 for use with Maintain II.

To determine that the bootstrap loader is correctly loaded, perform the following:

a. Initialize the computer by pressing the SYSTEM RESET switch.

b. Clear all registers by momentarily placing each REGISTER switch in the down position and pressing the BIT RESET switch each time.

c. Load instruction 014000 (load A relative to P) into the U register.

d. Load the starting memory address (007756) in the P register, keeping the REPEAT switch in the down position.

e. Select the A register and press the STEP switch. The contents of each memory address are displayed sequentially each time the STEP switch is pressed.

f. If an error is found, reload the erroneous instruction codes into memory.

NOTE

The P register error message is always the error address plus one.

3.4 BINARY LOAD/DUMP (BLD II)

The binary load/dump program (BLD II) allows the user to load object programs from a high-speed paper tape reader or a Teletype paper-tape reader, or to punch the binary contents of memory on paper tape in a reloadable format.

BLD II (part number 92A1007-001) is on paper tape in two sections: a binary load section and a binary dump section. The binary load section is in a special format to allow loading of a program tape via the bootstrap loader routine. After the binary load section is placed in memory, control transfers to it and it then loads the binary dump section. The binary dump section allows a program stored in memory to be punched on paper tape in standard binary format.

3.4.1 Location of BLD II

Once loaded into memory, BLD II relocates itself into the upper part of the highest 4K memory module unless the operator specifies a different 4K memory module.

Initially, BLD II occupies addresses 07000 to 07755. By residing in these locations, it does not interfere with the bootstrap loader occupying addresses 07756 to 07776. Immediately after loading, BLD II relocates to occupy addresses 0x7000 through 0x7755. x denotes the 4K memory module in which BLD II relocated as follows:

x =	Memory Module
0	4K
1	8K
2	12K
3	16K
4	20K
5	24K
6	28K
7	32K

Entry to BLD II to read object tapes is always 0x7600, and entry to punch object tapes is 0x7404.

3.4.2 Options Prior To Loading

The operator has four options prior to loading the BLD II tape.

a. No SENSE switches set: The program accepts input from the devices specified in the entered bootstrap routine and stores the program in the highest 4K memory module. After reading the program in, the computer halts with the P register set to the entry address (0x7600) and the A, B, and X registers cleared.

b. SENSE switch 1 set: This allows the operator to select any 4K memory module in which the program is to operate. After reading the program in, the computer halts with the P register set to 07013. The operator must enter in the A register a number (0 through 7) specifying the memory module in which the program is to reside. By pressing RUN, the operator initiates the relocation and the computer halts as in item a above.

c. SENSE switch 2 set: This adjusts the loader to accept high-speed paper tape reader input and adjusts the dump routine for TTY punch output.

d. SENSE switch 3 set: This allows the operator to splice an object program to the BLD II program tape, load the BLD II program and the object program and execute the object program without further intervention.

3.4.3 Object Program Loading Options

BLD II establishes the input reader (TTY or high-speed paper tape) and the output punch devices by interrogating the bootstrap loader. For this reason, BLD II is adjusted to accept object program tapes from only the reader specified by the bootstrap routine.

However, setting SENSE switch 2 prior to loading BLD II adjusts the program for high-speed paper tape reader input and TTY punch output regardless of the bootstrap-routine-specified I/O devices.

3.4.4 Punching Tapes of Memory Contents

To punch a tape from memory to the high-speed paper tape punch, SENSE switch 2 must not be set when BLD II is entered. To punch a tape from memory to the TTY punch, SENSE switch 2 must be set when BLD II is entered. The operator can specify that tapes be punched in binary format to load using the binary loader, or punch the binary loader in bootstrap-loadable format.

To punch a tape in binary format:

a. Set the P register to 0x7404.

b. Set the A register to the address of the first word to be punched.

c. Set the B register to the address of the last word to be punched.

d. Set the X register to the execution address.

To punch the BLD II in a bootstrap-loadable format, set the P register to 0x7400.

3.4.5 Loading BLD II

a. Enter the bootstrap loader.

b. Clear the U register.

c. Set the P register to 007770.

d. Set the X register to 007000.

e. Set SENSE switches, if required (section 3.4.2).

f. Turn on the paper tape reader (for the 33 ASR or 35 TTY, turn control knob to LOCAL and press the CRTL, D, T, and Q keys, then place control knob to LINE).

g. Position the BLD II tape in reader with the first data frame after the eight-level punches under the high-speed reader head or with the first character under the reading station of the TTY reader (place the TTY reader control switch to STOP).

h. Press RUN switch. Load is complete when the computer changes to step mode. For TTY, place reader control switch to RUN (START).

i. If SENSE switch 1 is set (section 3.4.2), reset SENSE switch 1 and clear the A register.

j. Enter in the A register the appropriate octal value to relocate BLD II, if applicable. Press RUN.

k. The computer will halt in step mode with the P register containing 0x7600 unless SENSE switch 3 was set. With SENSE switch 3 set, the computer will load and execute the object program.

l. Remove the BLD II program tape and reset SENSE switch 2, if applicable.

3.4.6 Loading The Object Program Tape

Object program tapes can be loaded immediately after BLD II because the P register is set to the load starting address (0x7600). For all subsequent loadings, assure that P is set to 0x7600.

3.4.6.1 VERIFICATION

To ensure that an object tape contains no errors before loading into core memory, BLD II has an option that performs only check-sum error-checking. To use this option:

a. Turn on the reader and position the object tape in the reader.

b. Enter 0100000 in the A register. Set the P register to 0x7600.

c. Clear the U register.

d. Press RUN.

e. Verification with no errors is indicated by the computer halting with:

   P register = 0x7600
   A register = 100000
   B register = 000000
   X register = execution address

f. Verification with a check-sum error is indicated by the computer halting with:

   P register = 0x7600
   A register = 100000
   B register = 177777
   X register = load address of last correct address read.

g. To retry the check-sum error record, reposition the object program tape at the previous visual aid and press RUN. If a check-sum error is read again, check each character in the record. An error has been made in punching or the tape may be slightly torn.

3.4.6.2 LOAD PROGRAM AND HALT

To load the object program and halt:

a. Turn on the reader and position the object tape in the reader.

b. Clear the A, X, and U registers.

c. Set the P register to 0x7600.

d. Press RUN.

e. Correct loading will be indicated by:

P register = 0x7600
A register = 000000
B Register = 000000
X register = program execution address

f. A check-sum error is indicated by the same conditions as in section 3.4.6.1, step f.

3.4.6.3 LOAD AND EXECUTE PROGRAM

Programs can be loaded and executed using the steps in section 3.4.6.2 except, in step b, set the A register to 000001 (any positive number).

3.4.7 Punching Program Tapes

With BLD II loaded and the paper tape punch on, areas of memory can be punched in object-tape-loadable format.

a. Set the A register to the beginning address of the area to be punched.

b. Set the B register to the last address to be punched.

c. Set the X register to the address of the next instruction to be executed; or, if noncontiguous memory areas are to be punched, set the X register to -1 (177777).

d. Set the P register to 0x7404.

e. Clear the U register.

f. Press SYSTEM RESET and RUN.

g. Tape will be punched and the computer halts with registers unaltered. If additional areas are to be punched, perform steps a through f above, entering the new areas in the A and B registers. Prior to punching the last area, set the X register to the execution address.

CHAPTER IV

CENTRAL PROCESSING UNIT

SECTION 1
FUNCTIONAL DESCRIPTION

1.1 GENERAL

The circuits of the CPU are contained on eight circuit cards consisting of three register cards, four processor control cards, and the AMED circuit card. The names and part numbers of these circuit cards are:

Register cards (3)	44P0592
Processor control 1	44P0595
Processor control 2	44P0596
Processor control 3	44P0597
Processor control 4	44P0593
AMED	44P0237

1.2 DESIGN FEATURES

The CPU incorporates two design features which provide wiring simplicity and simplified troubleshooting operations: the " bit-slice" design concept in the structural organization of the gating and storage elements, and the transmission bus technique for data transfers.

1.2.1 Bit Slice

Each of the three register cards (44P0592) contains circuits for six bits of all registers (except the L and S registers). Circuits for bits 0 through 5 are on card (44P0592) in mainframe card slot 7, bits 6 through 11 are in card slot 8, and bits 12 through 15 are in card slot 9. The last two bits in card slot 9 are not wired to the mainframe backplane. The (44P0592) cards are, therefore, interchangeable which simplifies troubleshooting operations by allowing a malfunctioning bit slice to be isolated without regard to the failure of a specific functional area.

1.2.2 Transmission Bus

A transmission bus technique is employed throughout the CPU. The term bus, as used in this manual, refers to any group of parallel signal paths. This may be any part or combination of the following:

a. Circuit paths on a printed circuit board (or group of boards) which carry the same parallel bits of data words or related control signals.

b. An entire wire harness assembly (or a group of wires in such an assembly) which carries parallel bits of data words or related control signals.

c. An entire cable (or a group of wires in a cable) which carries parallel bits of data words or related control signals.

d. A group of jumper wires or patch cords which carry parallel bits of data words or related control signals.

1.3 FUNCTIONAL ELEMENTS

A block diagram of the CPU is presented in figure IV-1. The CPU contains the following functional elements.

a. Timing and control

b. Arithmetic/logic

c. Operation registers

d. Controls and indicators

e. Input/output

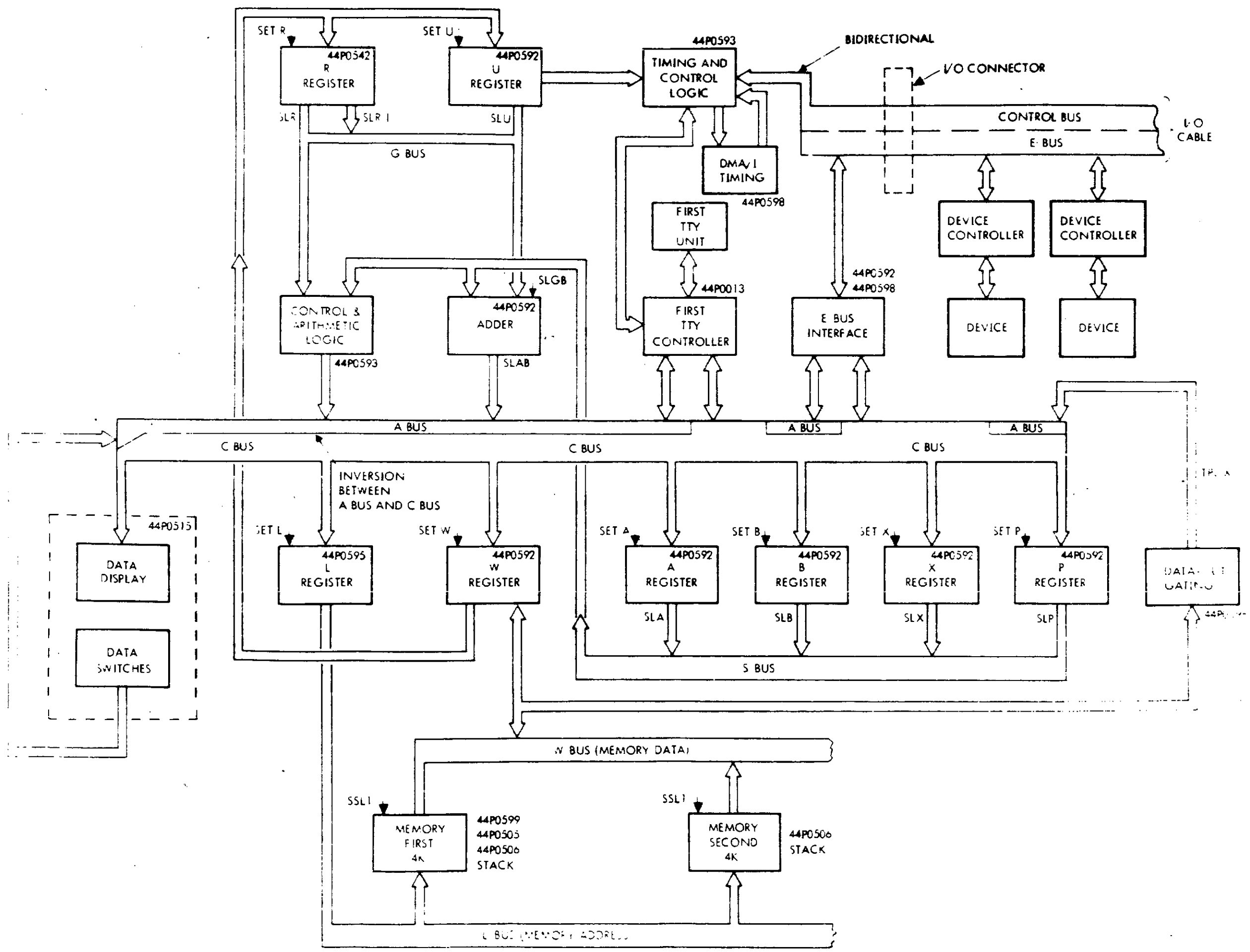

Figure IV-1. 620/L CPU Block Diagram

1.3.1 Timing and Control

The timing and control section provides timing for all computer functions, and buffers and decodes program instructions to coordinate timing and control sequences.

1.3.2 Arithmetic/Logic Section

The arithmetic/logic section contains the circuitry required for data manipulation under supervision of the timing and control section.

1.3.3 Operation Register Section

The operation register section includes the A, B, X, and P registers. All operation registers are full-length. The A, B, and X registers are directly accessible to the computer programmer, while the contents of the P register are available to the programmer through instructions which modify the program sequence (basically, jumps). The A and B registers comprise the computer accumulator, the X register serves as an indexing register for operand addresses, and the P register holds the address of the next instruction to be executed. The P register is incremented before the present instruction is executed. The A register is the accumulator, storing the results of logical and addition/subtraction operations. During multiplication and division, the A register forms the upper half of the accumulator storing the most significant half of the double-length product in multiplication and the remainder in division. The B register forms the lower half of the accumulator, storing the least significant half of the double-length product in multiplication and the quotient in division. Both the A and B registers may be used for input/output transfers under program control. The B register may also be used for indexed address modifications, if desired. Using the B or X register for address modifications adds no time to instruction execution.

1.3.4 Controls and Indicators

The control panel circuits and indicators with their associated circuits are contained on the display card (44P0515). The contents of the operation registers and instruction register can be routed from the C bus and displayed on the control panel. Conversely, data signals from the control panel register-entry switches can be loaded into a selected operation register via the A and C buses.

1.4 PROGRAMMED I/O OPERATIONS

The computer communicates with peripheral devices on a 16-bit parallel-word I/O bus. Each information transfer occurs under the control of a stored program. Information exchanges with peripheral devices are synchronized by peripheral controllers; a controller can control one or more similar peripheral devices. Each controller and the device(s) it controls comprise a peripheral device option.

Four types of I/O operations can be performed under program control:

a. *External Control.* An external control code is transmitted under program control from the computer to a peripheral controller.

b. *Program Sense.* The status of a selected peripheral controller sense line is interrogated by the computer under program control.

c. *Single-Word Input Transfer.* A single word of data is transferred under program control from a peripheral controller to the A register, B register, or any location in memory.

d. *Single-Word Output Transfer.* A single word of data is transferred under program control to a peripheral controller from the A register, B register, or any location in memory.

1.4.1 I/O Bus Signal Interface

The computer can communicate directly with all peripheral devices under program control. The computer initiates operation of a peripheral device by transmitting an external control code and a proper device address to the selected controller via the I/O bus. The computer first determines when a device is ready to send or receive information by interrogating its associated sense line. The device is then requested to place a word of data on the I/O bus during a computer input transfer or to accept a word of data placed on the bus by the computer during an output transfer.

The standard I/O bus consists of the E bus and five I/O control lines: FRYX-I, DRYX-I, SERX-I, IUAX-I, and SYRT-I.

1.4.1.1 E BUS (EB00-I THROUGH EB17-I)

The E bus is a 16-bit, parallel, bidirectional I/O channel used to transmit control codes, device addresses, and data from the computer to the peripheral devices. In turn, the bus is used by the options to transmit data to the computer. Ten drivers and ten receivers may be connected to each line. An E bus signal is logically true when it is at 0V dc and logically false when it is at +3V dc. A typical E bus configuration is shown in figure IV-2

1.4.1.2 FRYX-I

Signal FRYX-I is generated by the computer to indicate that the computer has placed a device address and a control code on the E bus. Each peripheral controller examines the device address, and upon the true-to-false transition of FRYX-I, the addressed device responds to the control code. FRYX-I is logically true at 0V dc and logically false at +3V dc. Ten receivers may be connected to the line. A typical FRYX-I line configuration is shown in figure IV-3.

1.4.1.3 DRYX-I

Signal DRYX-I is generated by the computer. During an output data transfer, DRYX-I indicates that the computer has placed data on the E bus and that the peripheral device previously addressed should strobe the data into its input buffer. During an input data transfer, DRYX-I indicates that the computer has accepted the data placed on the E bus by the peripheral device, and that, following the true-to-false transition of DRYX-I, the device should remove the data. DRYX-I is logically true at 0V dc and logically false at +3V dc. Ten receivers may be connected to the line. A typical DRYX-I line configuration is shown in figure IV-3.

1.4.1.4 IUAX-I

Signal IUAX-I is generated by the computer to acknowledge that either a DMA access or interrupt operation is in progress. Each peripheral device controller uses IUAX-I to inhibit normal device address decoding. In a basic I/O interface, without the DMA option, IUAX-I is held false (+3V dc). Ten receivers may be connected to the line. A typical IUAX-I line configuration is shown in figure IV-3.

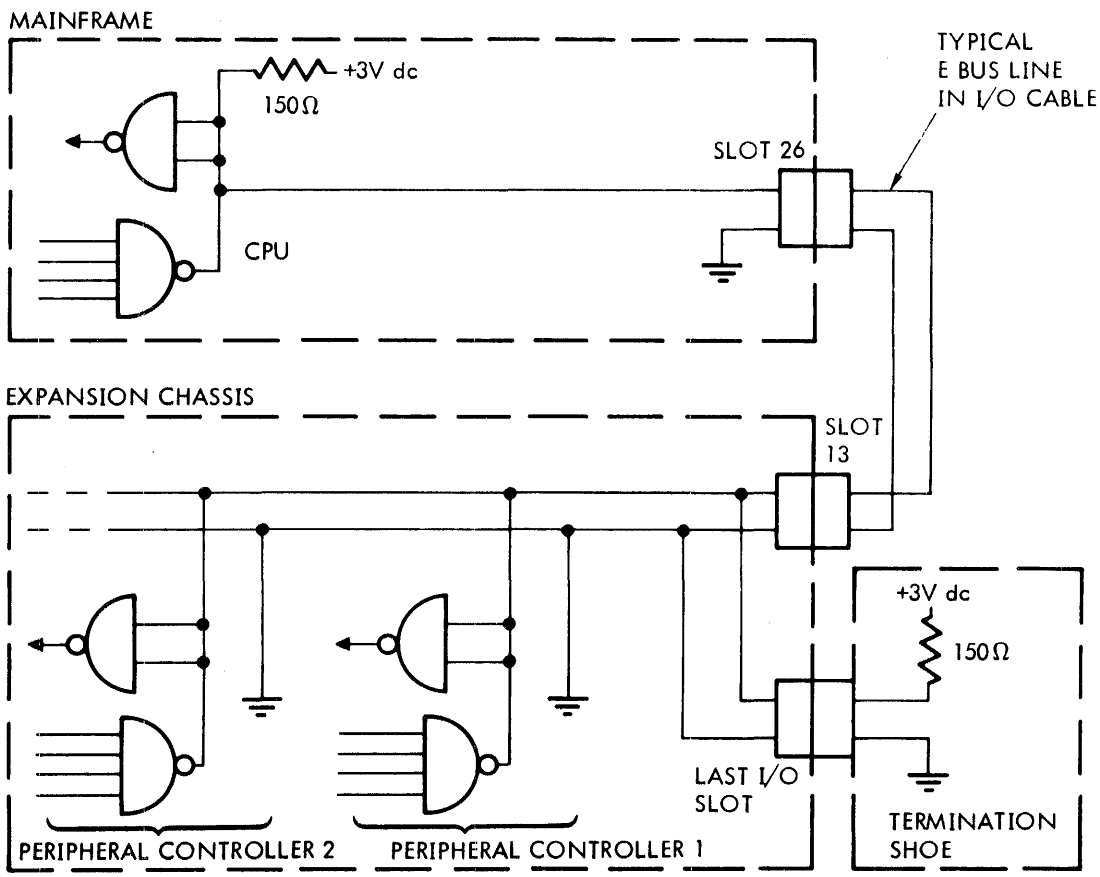

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Figure IV-2. Typical E Bus Line Configuration

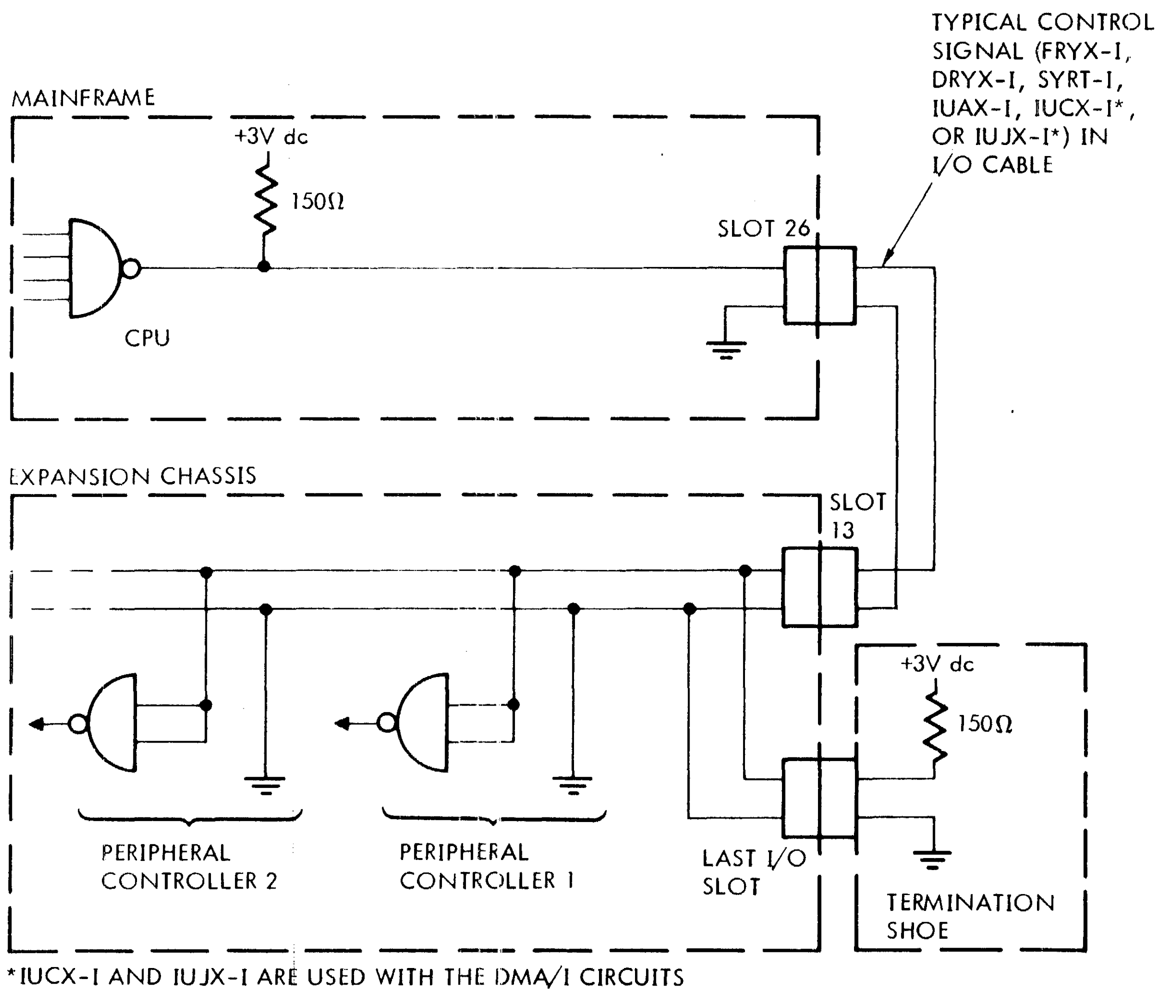

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Figure IV-3. Typical Control Signal From the CPU to the Controller

1.4.1.5 SYRT-I

Signal SYRT-I is used to initialize each peripheral device controller connected to the I/O bus. SYRT-I becomes true when the SYSTEM RESET switch on the control panel is pressed. SYRT-I is logically true at 0V dc and logically false at +3V dc. Ten receivers may be connected to the line. A typical SYRT-I line configuration is shown in figure IV-3.

1.4.1.6 SERX-I

During the execution of a program Sense (SEN) instruction, the computer places a function code and a device address on the E bus. The addressed controller is instructed to indicate the status of the specific device condition identified by the function code. If the specified condition is true, the controller responds by setting the SERX-I line true. If the condition is false, SERX-I is left false. SERX-I is logically true at 0V dc and logically false at +3V dc. Ten drivers may be connected to the line. A typical SERX-I line configuration is shown in figure IV-4.

1.4.2 I/O Instructions

The basic computer provides four types of I/O instructions for program control of peripheral devices connected to the I/O bus:

a. External control

b. Program sense

c. Single-word input transfer

d. Single-word output transfer

Table IV-1 summarizes E bus and control signals used during these instructions. The E bus signals used for the execution of each command are shown in table IV-2. These tables appear at the end of this section. The following paragraphs describe the operations associated with each instruction type and the manner in which the I/O bus signals are used.

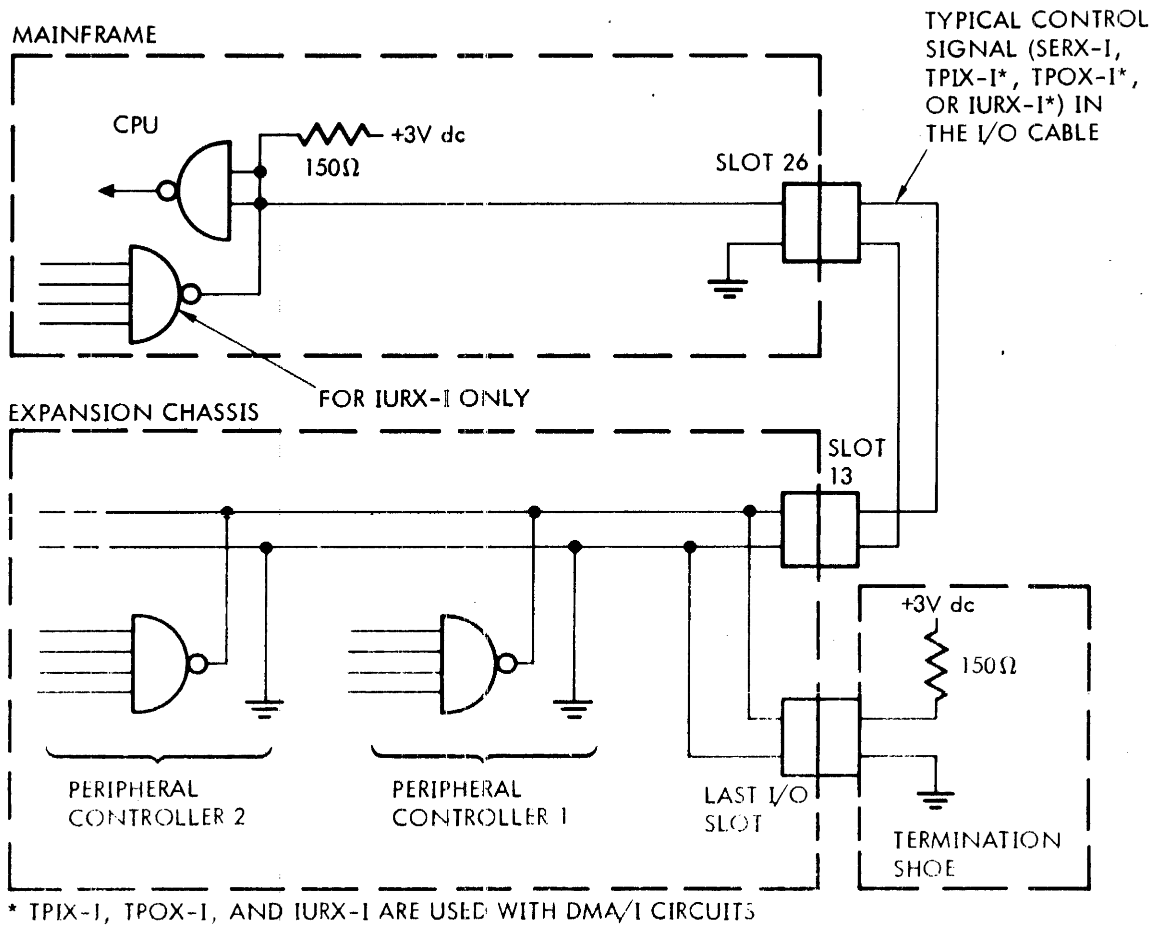

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Figure IV-4. Typical Control Signal to the CPU From the Controllers

1.4.2.1 EXTERNAL CONTROL

The External Control (EXC) instruction is used to initiate a specific mode of operation in a peripheral device. An example is the use of an EXC instruction to cause a magnetic tape transport to advance the tape one record. The EXC instruction word format is shown below, where YY contains the device address and X contains the function code.

```
15   14 13 12   11 10 9    8  7  6    5  4  3   2  1  0
------10-----   ---0---    ---X---    -------YY--------
```

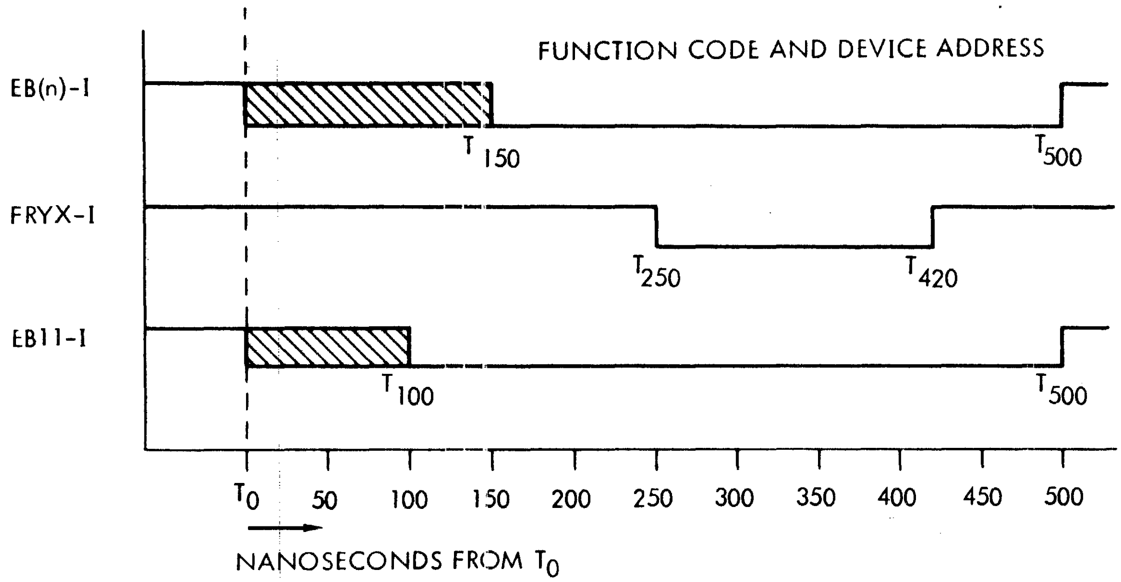
EXC causes the function codes and device address portions of the instruction word to be placed on the E bus. EXC I/O timing is shown in figure IV-5. Signal lines EB00-I through EB05-I indicate the device address; EB06-I through EB08-I indicate the function code. EB11-I is held true, indicating that an EXC function is being performed. The device controller decodes the binary function code, and, following the true-to-false transition of FRYX-I, initiates the specified mode of operation in the addressed device. During the execution of EXC, no data are exchanged between the computer and the device controller, and no response signal is expected from the controller.

When additional function codes are required, the extended EXC instruction (instruction code 104) can be used. This command is identical to the normal EXC instruction (instruction code 100) in timing and function, but it is identified by EB15-I instead of EB11-I as shown in tables IV-1 and IV-2.

Figure IV-6 shows typical implementation of the logic required in a peripheral controller to receive, decode, and perform an EXC instruction.

1.4.2.2 PROGRAM SENSE

The program Sense (SEN) instruction is used to test the status of a specific device condition, and, if a true condition is detected, execute a program jump. If a false condition is detected, the next instruction in sequence is executed. An example of SEN instruction usage is a test to determine if a magnetic tape transport is rewinding.



T_0 is the start of the execute phase of the external control instruction.

Logic levels: true = 0V dc,
false = +3V dc.

 = time when signal is settling.

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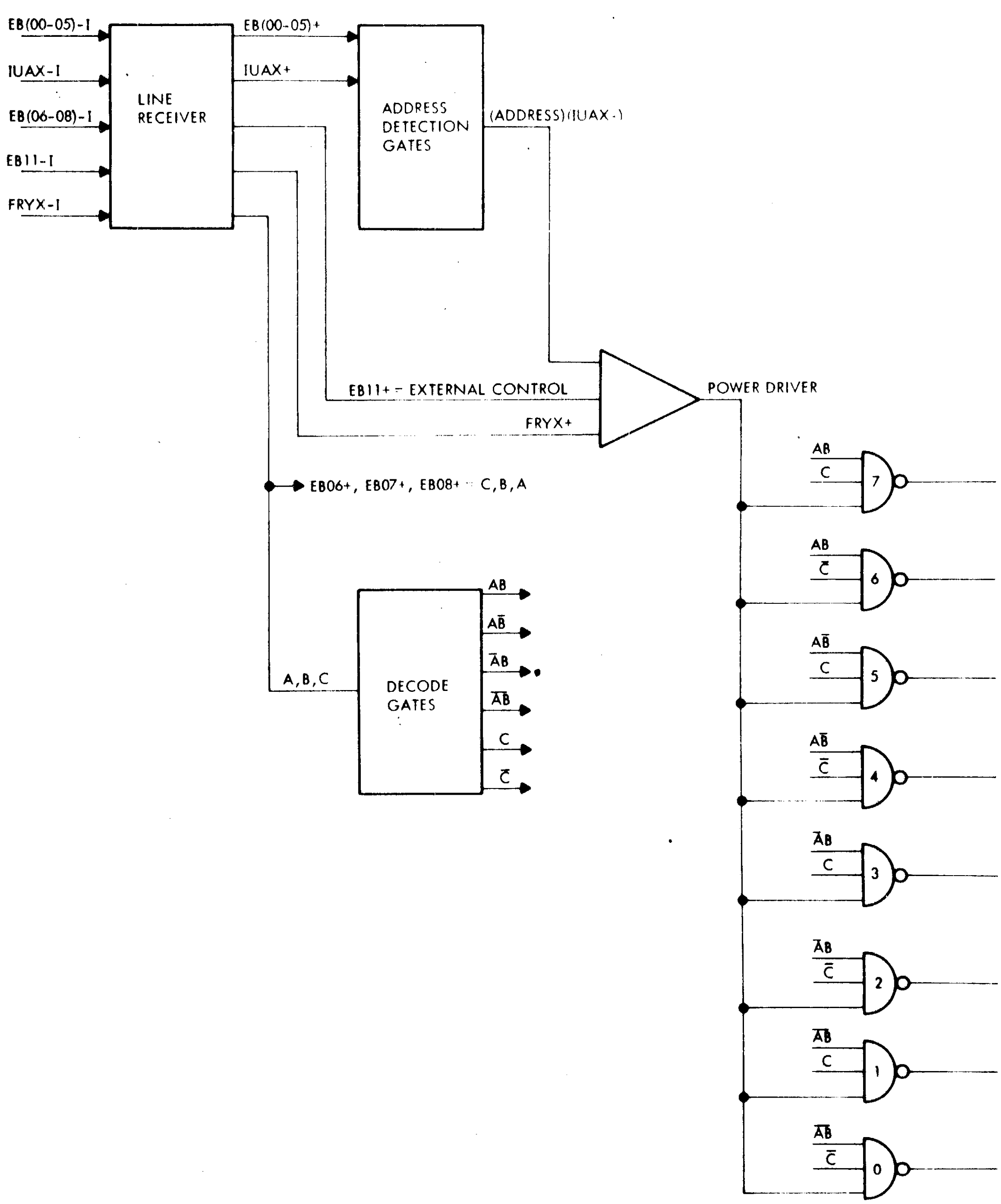
Figure IV-5. External Control Timing



VTII-0377

Figure IV-6. Typical Peripheral Controller Logic: EXC Instruction

The SEN instruction format is shown below, where YY contains the device address and X contains the function code which defines the specific condition to be tested.

```
15    14 13 12   11 10   9   8   7   6    5   4   3    2   1   0
------10-----   ----1---   ---X---    -------YY--------
0     ----------------JUMP ADDRESS-------------------
```

The SEN instruction causes the function code and device address portions of the instruction word to be placed on the E bus. The SEN I/O timing is shown in figure IV-7. Signal lines EB00-I through EB05-I indicate the device address. EB12-I is held true to indicate that a SEN instruction is in progress.

Figure IV-8 shows typical implementation of the logic required in a peripheral controller to receive, decode, and respond to a SEN instruction. Note that the device address (usually ANDed with IUAX-I) can be used directly to enable the sense line response (SERX-I). EB12-I need not be used to enable SERX-I, since the computer samples the SERX-I line only when a SEN instruction is executed.

1.4.2.3 SINGLE-WORD INPUT TRANSFER

Five instructions provide a single-word input transfer:

a. Input to A register (INA)*

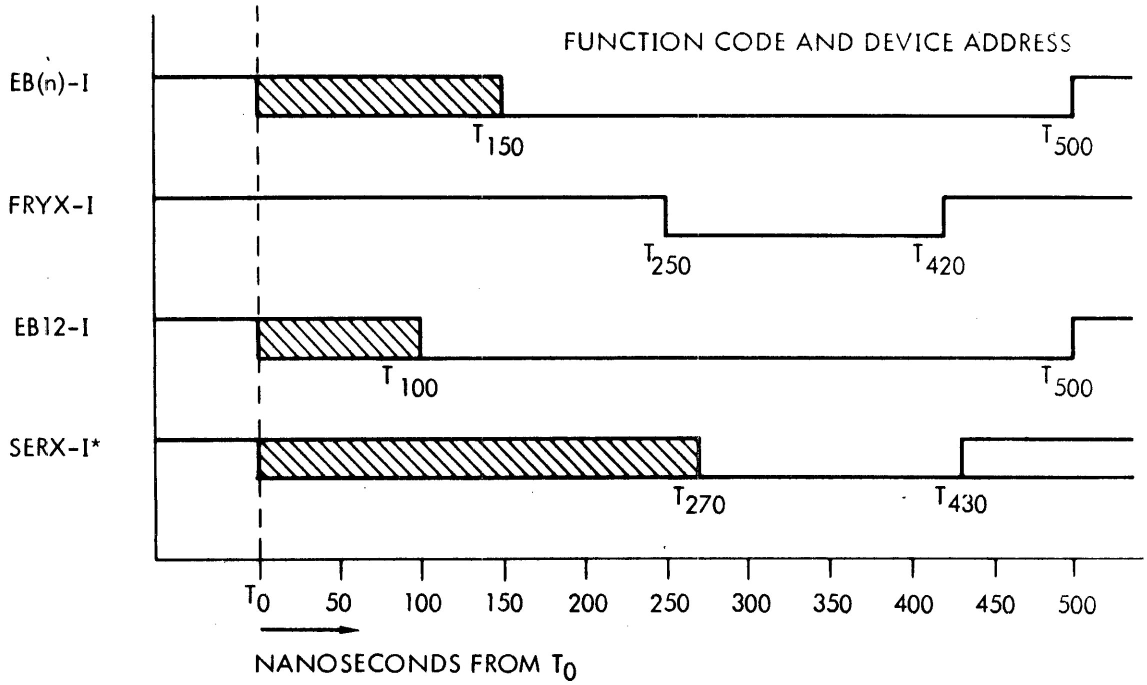
b. Input to B register (INB)*

c. Input to memory (IME)

d. Clear and input to A register (CIA)

e. Clear and input to B register (CIB)

* Inclusive-OR of the data lines and the specified register contents.



T_0 is the start of the execute phase of the sense instruction.

Logic levels: true = 0V dc,
false = +3V dc.

 = time when signal is settling.

* SERX-I is normally on at T_{270} ; it must be on by T_{410}.

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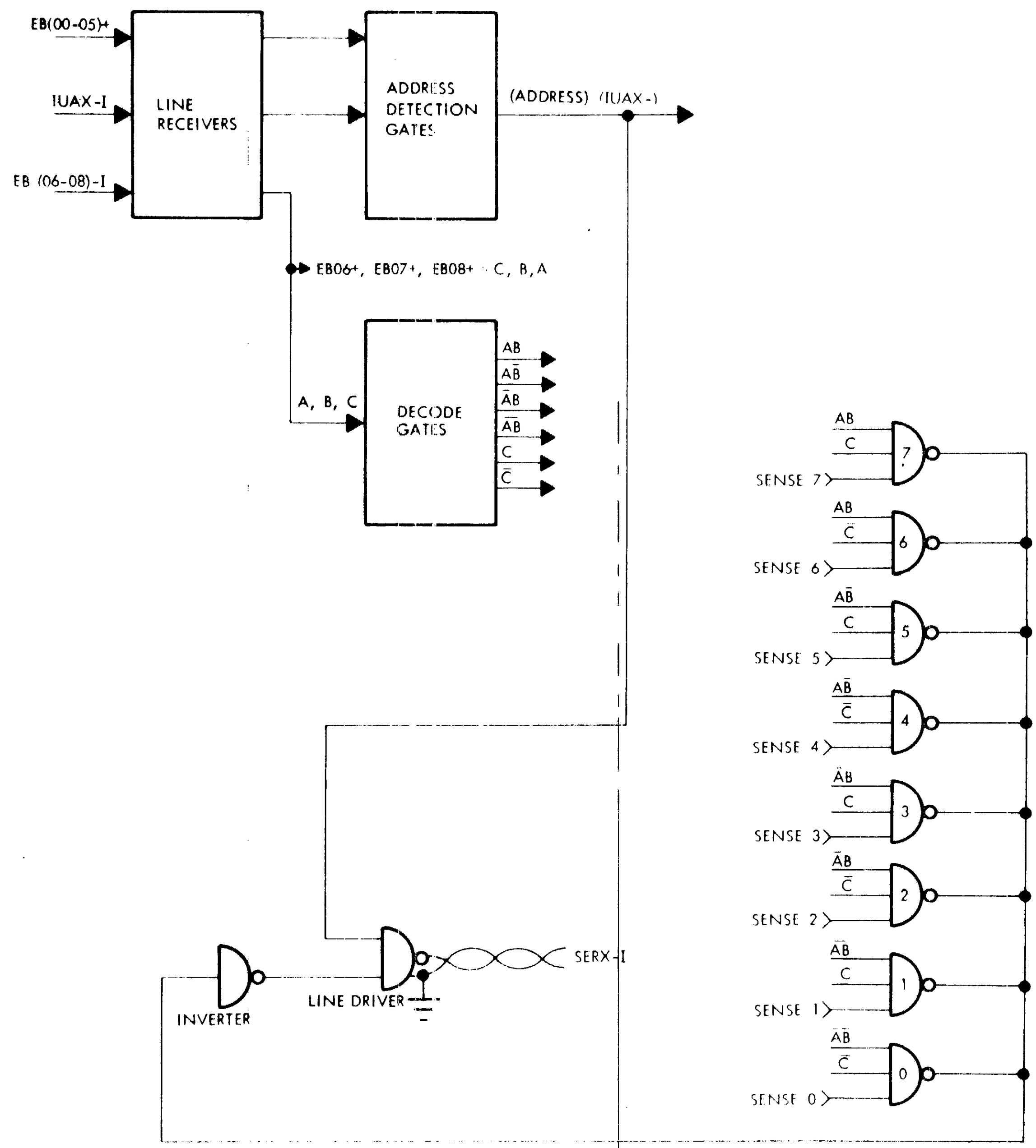
Figure IV-7. Sense Response Timing



VT11-0378

Figure IV-8. Typical Peripheral Controller Logic: SEN Instruction

The instruction word format for INA, INB, CIA, and CIB is shown below, where YY contains the device address and X defines each individual instruction.

```
15    14 13 12   11 10   9   8   7   6    5   4   3    2   1   0
------10-----   ----2---  ---X---    -------YY--------
```

The instruction word format for IME includes a second word that specifies the input data word destination.

```
15    14 13 12   11 10   9   8   7   6    5   4   3    2   1   0
------10-----   ----2---  ---0---    -------YY--------
0     ----------------DATA ADDRESS-------------------
```

Execution of any one of the five single-word input transfer instructions produces the same sequence of operations on the I/O bus. Consequently, in responding to the bus signals, a peripheral device controller makes no distinction between the input transfer instructions.

Execution of an input transfer instruction is a two-phase operation. The first phase selects the peripheral device controller that will participate in the second-phase data transfer. The transfer timing is shown in figure IV-9. The first phase is initiated by the computer, which places the device address on E bus lines EB00-I through EB05-I. EB13-I is held true during this phase to indicate that an input transfer instruction is in progress. Since the E bus is time-shared, a flip-flop in the peripheral controller for the selected device is set to indicate that the controller was selected and that data are to be transferred to the computer. This flip-flop, Data Transfer In (DTIX+), is set at the true-to-false transition (trailing edge) of FRYX-I (if the controller controls more than one device, an additional flip-flop for each device is required to identify the selected device). As the computer removes the device address and control code information, the selected controller uses DTIX+ to enable the input data onto the E bus. The controller must enable data from the selected device onto the bus no later than 480 nanoseconds after the trailing edge of FRYX-I to strobe the input data. The controller uses the trailing edge of DRYX-I to reset DTIX+; thus removing the input data from the E bus.

When the computer is transferring I/O data under program control, the transfers must be synchronized with the communicating peripheral controller. This synchronization is accomplished by sampling the state of the controller for a ready condition by issuing SEN prior to the data transfer instruction.

Figure IV-10 shows typical implementation of the logic required in a peripheral controller to perform an input data transfer.

1.4.2.4 SINGLE-WORD OUTPUT TRANSFER

There are three single-word output instructions:

a. Output from A register (OAR)

b. Output from B register (OBR)

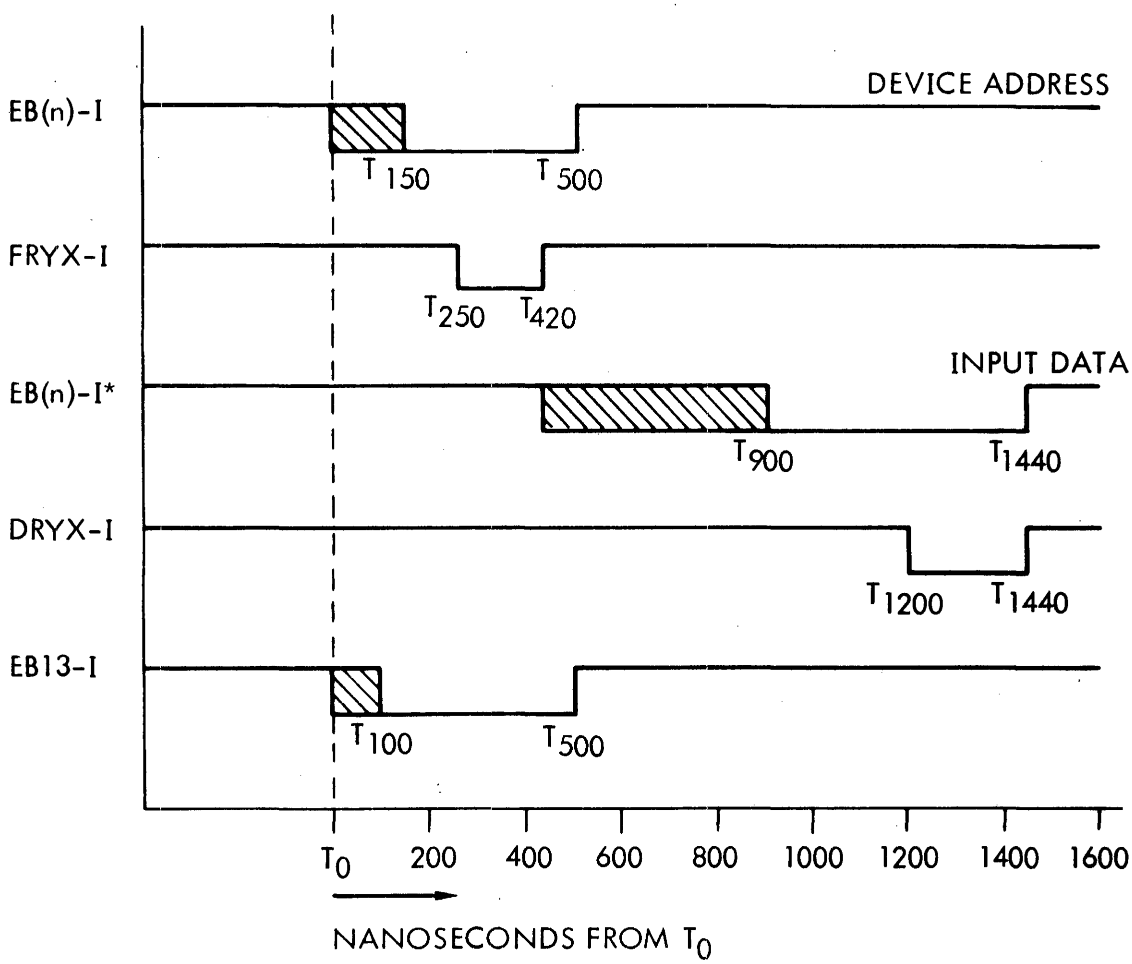
c. Output from memory (OME)

The instruction word format for OAR and OBR is shown below, where YY contains the device address and X distinguishes between the two instructions.

```
15    14 13 12   11 10  9   8  7  6    5  4  3   2  1  0
------10-----    ----3---   ---X---    -------YY--------
```

This instruction word format for OME includes a second word that specifies the output data word source location.

```
15    14 13 12   11 10  9   8  7  6    5  4  3   2  1  0
------10-----    ----0---   ---0---    -------YY--------
0     ---------------DATA ADDRESS--------------------
```



T_0 is the start of the execute phase of the data transfer in instruction.

Logic levels: true = 0V dc,
false = +3V dc.

= time when signal is settling.

* EB(n)-I (input data) must be off by T_{1600}

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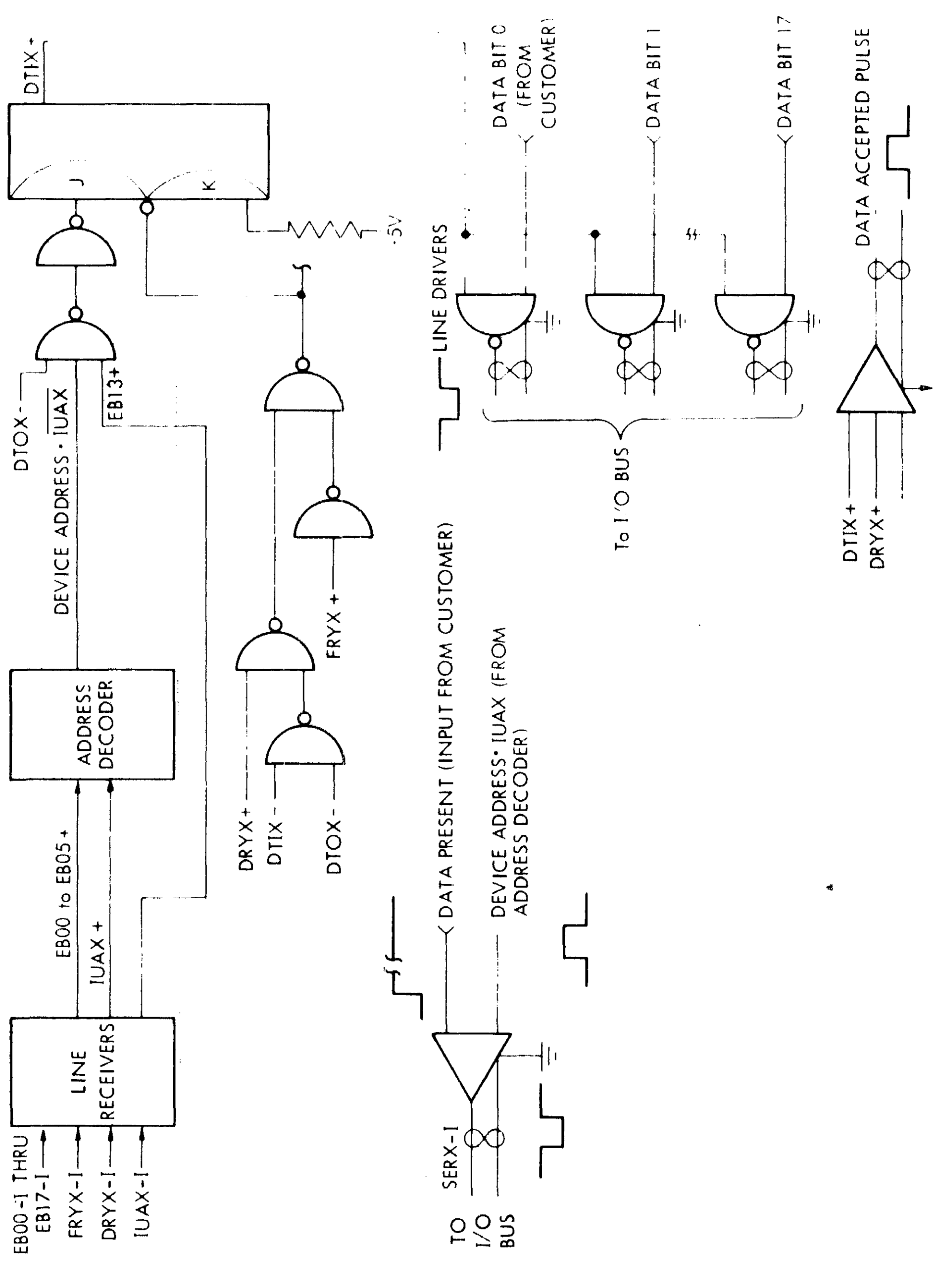
Figure IV-9. Data Transfer-In Timing



VT11-0379

Figure IV-10. Typical Peripheral Controller Logic: Input Data Transfer

The sequence of signals placed on the I/O bus is the same for each of the three output instructions, and the participating peripheral controller makes no distinction between the output instructions.

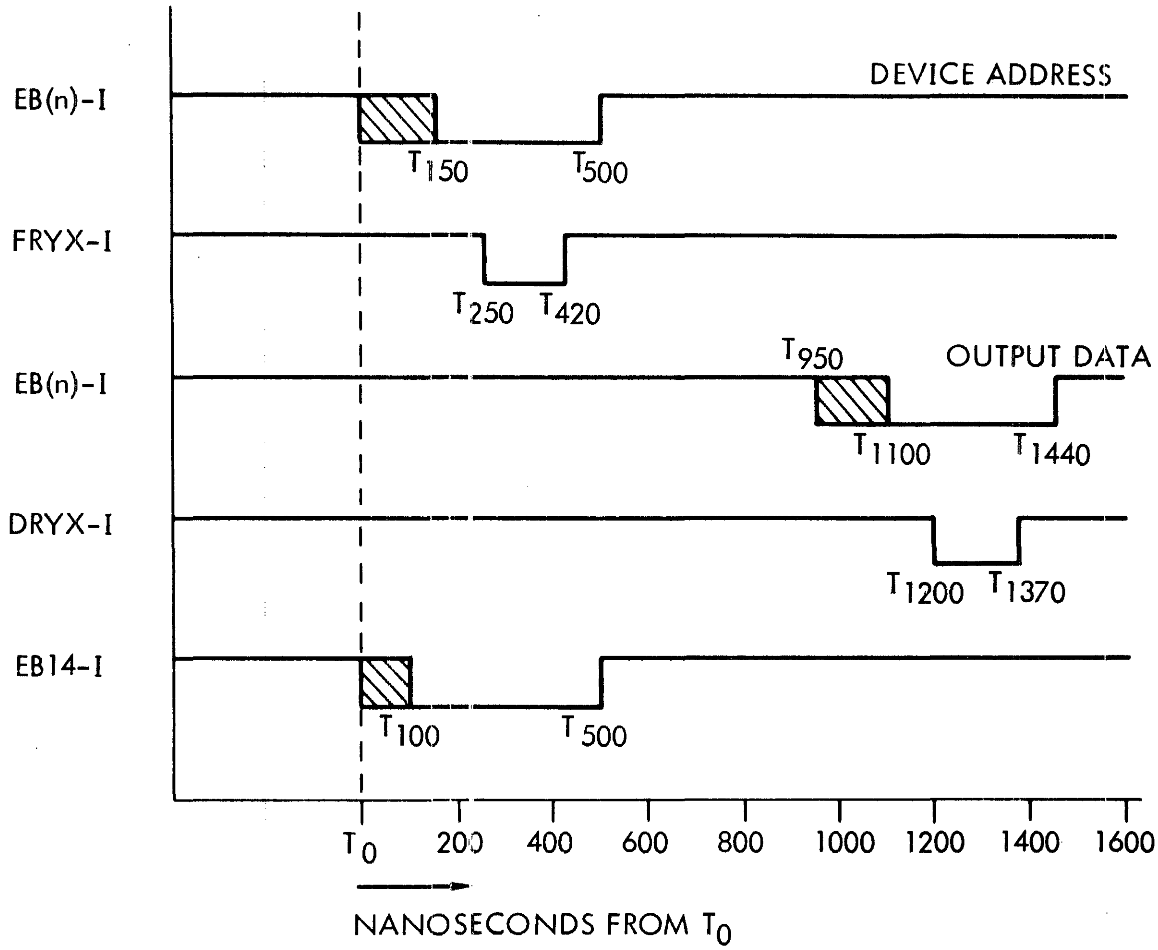
The execution of an output instruction is a two-phase operation similar to that described for an input instruction. The first phase selects the peripheral device which will participate in the second-phase data transfer. The transfer timing is shown in figure IV-11. The first phase is initiated by the computer, which places the device address on E bus lines EB00-I through EB05-I. EB14-I is held true during this phase to indicate that an output transfer instruction is being executed. A flip-flop, Data Transfer Out (DTOX +), in the controller for the selected device is set at the trailing edge of FRYX-I (if the controller controls more than one device, an additional flip-flop for each device is required to identify the selected device). Following FRYX-I, the computer removes the device address and control code, and places the output data on the E bus lines. DTOX + is used by the controller to gate the contents of the E bus into an input buffer at the trailing edge of DRYX-I. The trailing edge of DRYX-I is also used to reset DTOX + .

When the computer is transferring I/O data under program control, the transfers must be synchronized with the communicating peripheral controller. This synchronization is accomplished by sampling the state of the controller for a ready condition by issuing a SEN instruction prior to the data transfer instruction.

Figure IV-12 shows typical implementation of the logic required in a peripheral controller to perform an output data transfer.

1.4.3 Device Address Codes

Device address codes have been assigned to the standard peripheral devices, as shown in table IV-3. All device address codes are in the range 00 to 77. Each peripheral device belongs to a class, according to its function; each class is assigned a block of codes, and specific code assignments are given to devices in that class.



T_0 is the start of the execute phase of the data transfer out instruction.

Logic levels: true = 0V dc,
false = +3V dc.

= time when signal is settling.

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Figure IV-11. Data Transfer-Out Timing

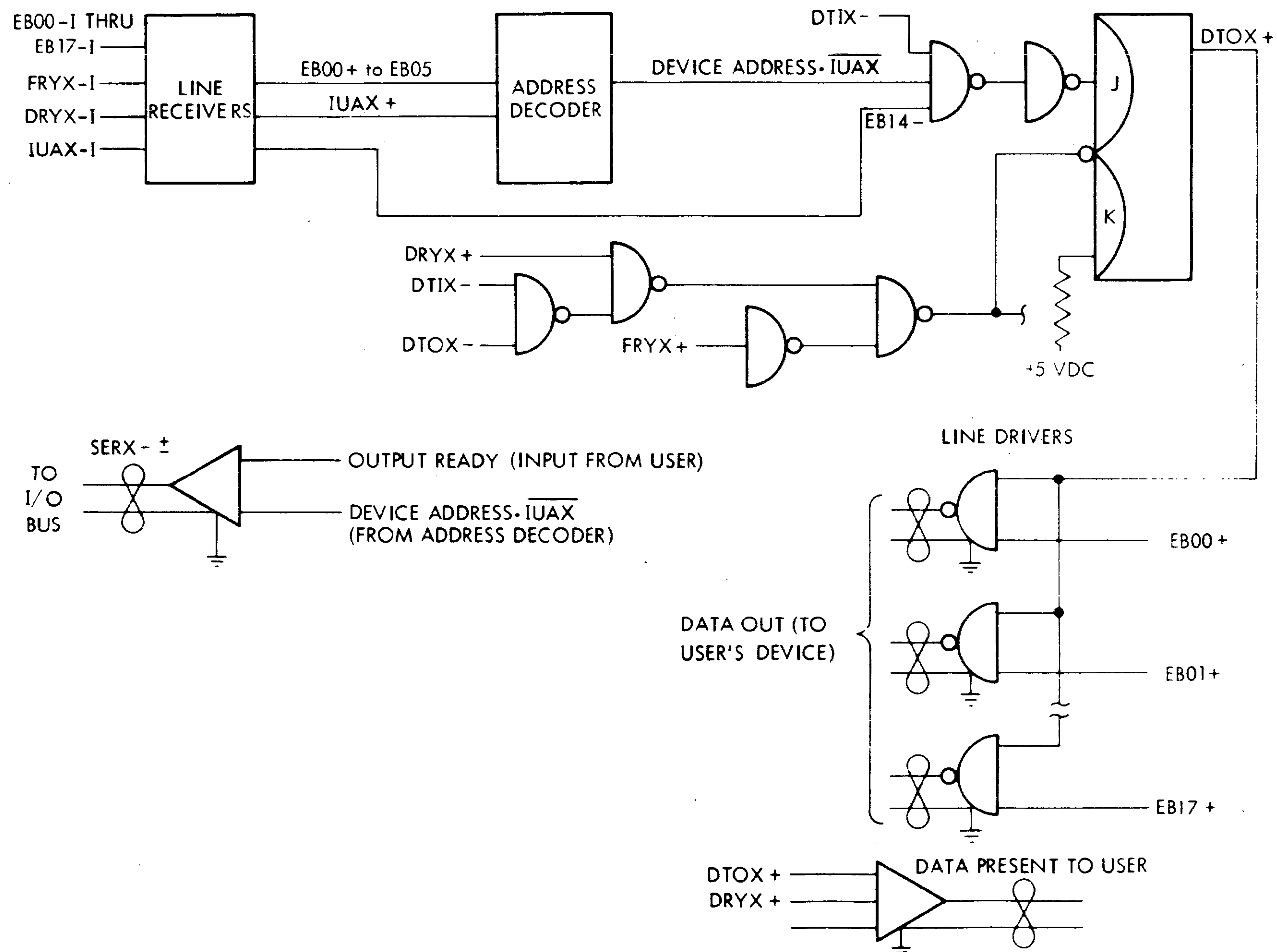

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Figure IV-12. Typical Peripheral Controller Logic: Output Data Transfer

Table IV-1. E Bus and I/O Control Signals

OPERATION >	External Control	Sense	Data Transfer (Single-word I/O)		Trap Sequence (BIC Control) TPOX-I or TPIX-I		Interrupt Sequence
CONTROL LINE >	FRYX-I* (Phase 1)	FRYX-I* SERX-I* (Phase 1)	FRYX-I* (Phase 1)	DRYX-I (Phase 2)	IUAX-I FRYX-I (Phase 1)	IUAX-I DRYX-I (Phase 2)	IURX-I IUAX-I (Phase 1)
EB00-I							
EB01-I							
EB02-I	Device address	Device address	Device address				
EB03-I							
EB04-I							Pairs of signals used for specific interrupts
EB05-I				Data	Address	Data	
EB06-I							
EB07-I	Function code	Function code					
EB08-I			Not used				
EB09-I	Not used	Not used					
EB10-I							

Table IV-1. E Bus and I/O Control Signals *(continued)*

OPERATION >	**External Control Sense**		**Data Transfer (Single-word I/O)**		**Trap Sequence (BIC Control) TPOX-I or TPIX-I**		**Interrupt Sequence**
CONTROL LINE >	**FRYX-I*** **(Phase 1)**	**FRYX-I*** **SERX-I*** **(Phase 1)**	**FRYX-I*** **(Phase 1)**	**DRYX-I** **(Phase 2)**	**IUAX-I** **FRYX-I** **(Phase 1)**	**IUAX-I** **DRYX-I** **(Phase 2)**	**IURX-I** **IUAX-I** **(Phase 1)**
EB11-I	External control command	Zero	Zeros				
EB12-I		Sense command					Pairs of signals
EB13-I	Zeros		Data in	Data	Address	Data	used for specific
EB14-I		Zeros	Data out				interrupts.
EB15-I	See note 3		Zero				

NOTES:

1. Phase 1 is device or memory selection.
2. Phase 2 is the data transmission.
3. For extended external control, control and data lines are the same as external control except EB11-I is zero and EB15-I is one.

* IUAX interlock; used in address decoding.

Table IV-2. E Bus Signals

Signal	EXC	SEN	IME	IAR	IBR	OME	OAR	OBR	EXC2
EB15-I	0	0	0	0	0	0	0	0	1
EB14-I	0	0	0	0	0	1	1	1	0
EB13-I	0	0	1	1	1	0	0	0	0
EB12-I	0	1	0	0	0	0	0	0	0
EB11-I	1	0	0	0	0	0	0	0	0
EB10-I EB09-I	Unused								
EB08-I	Unused		0	*	*	0	Unused		
EB07-I	Function code		0	0	1	0	0	1	Function code
EB06-I	Function code		0	1	0	0	1	0	Function code
EB05-I to EB01-I	Device Address (00-63)								

* If EB08-I is true, the selected register in the computer is cleared before input. If EB08-I is false, the selected register is not cleared. The result after input is the logical-OR of the original register and the input signals.

NOTE

Bits EB06-I through EB08-I are ignored by the I/O controller during data transfers.

Table IV-3. Standard Device Address Codes

Octal Class Codes	Assigned Octal Addresses	Peripheral or Internal Options
00-07	01-07	Teletype controller (620-06 through -08)
10-17	10-13	Magnetic tape controller (620-30, -31)
	14	Fixed-head rotating memory (620-38, -42 through -49)
	15	Movable-head rotating memory (620-40, -41)
	16, 17	Movable-head rotating memory (620-39) (620-37)
20-27	20, 21	First buffer interlace controller (620-20)
	22, 23	Second buffer interlace controller
	24, 25	Third buffer interlace controller
	26, 27	Fourth buffer interlace controller
30-37	30	Card reader (620-25)
	31	Card punch (620-27)
	32	Digital plotter (620-72)
	33	Electrostatic plotter
	34	Second paper tape system
	35,36	Line printer (620-77)
	37	First paper tape system (620-50 through 55)
40-47	40-43, 46	Priority interrupt module (620-16)
	44	All PIM enable/disable
	45	Memory protection (620-05) (620/L-05)
	47	Real-time clock (620-13) (620/i 1-13)

Table IV-3. Standard Device Address Codes *(continued)*

Octal Class Codes	Assigned Octal Addresses	Peripheral or Internal Options
50-57	50-53	Special application
	54-57	Analog system (620-850/870)
60-67	60-67	Digital I/O (620-81), Buffered I/O (620-80)
70-77	70-73	Communications controller (620-60, -61, -65, -66, -68)
	74-77	Relay I/O (620-83)

SECTION 2
THEORY OF OPERATION

2.1 GENERAL

The theory of operation for the CPU is divided into the following sections: timing and control logic, decoding logic, arithmetic and logical section, registers, memory interface, and typical operating sequences. Logic diagrams of the CPU circuit cards should be referred to during the theory of operation; the document numbers for the logic diagrams are:

Part Number	Logic Diagram
44P0592	91D0356
44P0508	91D0359
44P0596	91D0360
44P0597	91D0361
44P0593	91D0357

2.2 TIMING AND CONTROL

All operations performed by the CPU are controlled by the timing logic generated in the timing and control section. Basic timing signals are derived from a master clock circuit located on processor control card 4 (44P0593). The master clock is generated by a crystal-controlled oscillator operating at a frequency of 4.211 MHz which is counted down and passed through a pulse-width-adjustable one-shot to produce a continuous train of pulses typically 56 nanoseconds wide and spaced 450 nanoseconds apart. This output(MCLX +) generates the various clock signals shown in figure IV-13.

The CPU has a basic machine cycle of 950 nanoseconds. A full memory cycle (read/restore or clear/write) is performed within this period, except for special cases described in subsequent sections. All operations performed by the computer are accomplished in some multiple of the master clock timing cycle. During execution of various instructions, up to four suboperations can be performed during the basic machine cycle of 950 nanoseconds.

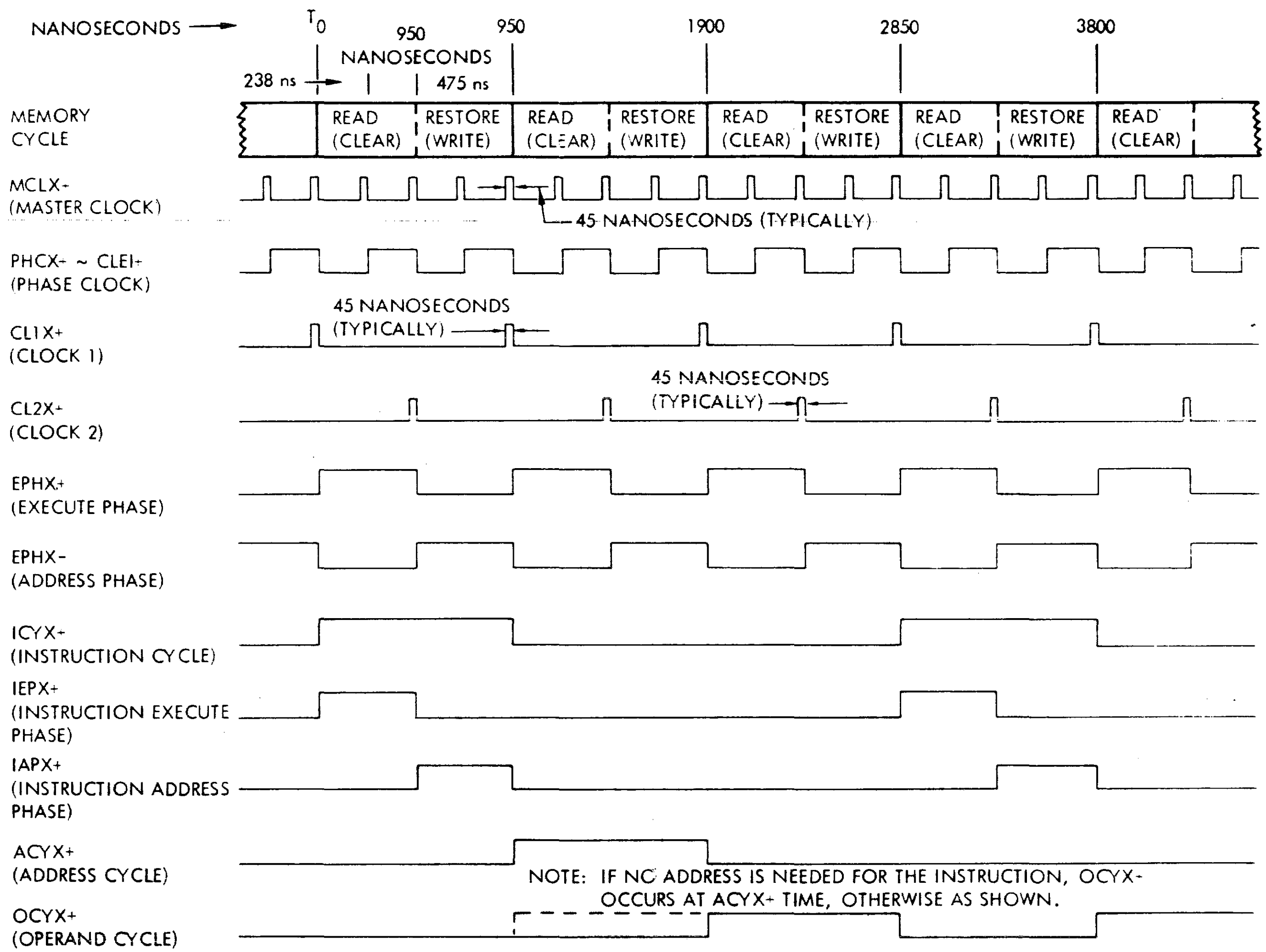

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Figure IV-13. Clock and Phase Timing

Functions performed by the CPU are divided into two basic phases:

a. Execute phase, the operation upon words read from memory or the storing of words into memory.

b. Address phase, the transfer of instructions or operand addresses into memory.

These phases are related to the basic clocks as described in table IV-4. Timing of the basic clocks and the two basic phases can be determined by referring to figure IV-13.

Table IV-4. Timing Signals

Signal	Description
Master Clock (MCLX +)	Basic 4.211-MHz crystal-controlled timing signal for the entire system.
Phase Clock (PHCX +)	2.105-MHz timing signal derived from, and in phase with, the master clock. This clock is used to time the address and execute phases.
Execute Phase (EPHX +)	Timing signal synchronous with the read or clear half cycle of memory. This signal is used to time all transfers of data to and from memory, and the execution of instructions.
Address Phase (EPHX −)	Timing signal synchronous with the restore or write half cycle of memory. This signal is used to time all transfers of instruction and operand addresses to memory.
Clock 1 (CL1X +)	Timing signal used to initiate a memory cycle and all operations synchronous with the start of a memory cycle.

Table IV-4. Timing Signals *(continued)*

Signal	Description
Clock 2 (CL2X+)	Timing signal used to initiate all operations synchronous with the start of a memory write or restore half cycle.

2.2.1 Sequence Control

The basic clocks generated from the master clock are used to time three operating sequences: instruction cycle, address cycle, and operand cycle. All operations performed by the computer are timed by one or more of these sequences.

2.2.1.1 INSTRUCTION CYCLE (ICYX+)

During this cycle, the next instruction to be executed is read from memory and transferred to the instruction register (U register) in the control section. The instruction cycle period is equal to a complete memory cycle (950 nanoseconds) and consists of two phases: instruction execute (IEPX+) and instruction address (IAPX+). These phases are synchronous with the execute and basic address phases (EPHX+ and EPHX-), respectively. During the first half of the instruction cycle, the execute phase, which is an operation specified by a previous instruction word, is performed (e.g., add, load operation register, etc.). although this phase is normally 475 nanoseconds, it may be extended by a clock modifier. Such phase timing modification is explained in section 2.2.2.

2.2.1.2 ADDRESS CYCLE (ACYX+)

The 950-nanosecond address cycle is synchronous with the basic memory cycle. When a single-word instruction indirectly addresses an operand, the instruction specifies the location of an address word in the memory. The same is true for double-word instructions where the second word is an address (e.g., jump instructions). This address word can contain the location of the operand, or another indirect address.

During the first half of the address cycle, the address word is read from memory and transferred to the R register. During the second half, bit 15 is examined to determine whether the next word accessed will be another indirect address or an operand. Several address cycles can be performed between instruction and operand cycles.

During the instruction address phase, the location of a word in memory (if specified by the current instruction in the U register) is generated and transferred to the memory L register. Generation of the address can involve modification of a basic address contained in the instruction (e.g., indexing, relative addressing, etc.).

2.2.1.3 OPERAND CYCLE (OCYX+)

This 950-nanosecond cycle follows the instruction cycle, unless the final operand is indirectly addressed, in which case, the operand cycle follows the address cycle. After the previous two cycles have determined that the data referenced in the current instruction is an operand and not an indirect address, the operand is either read from memory and stored in the R register or is transferred from the computer to the W register and stored in the memory.

2.2.2 Clock Modifiers

The execute or address phase can be modified by certain program instructions or by signals received from devices external to the computer. The conditions under which the clocks are modified are:

a. *Shift*. During shifting operations with words contained in the A or B register, EPHX+ is extended by the number of master clock periods (237.5 nanoseconds) equal to the specified number of shifts.

b. *Interrupt*. When an external interrupt is received, EPHX- is extended 475 nanoseconds to accommodate delays in receiving the interrupt address from the external device.

c. *Trap*. When a buffer interlace controller (BIC) requests a transfer to or from memory, EPHX- is extended 1.66 microseconds to permit the execution of the full trap sequence (routing of address and data from the external device).

d. *Halt*. On a halt instruction, clocks CL1X+ and CL2X+ are inhibited, preventing further computer operations until the STEP or RUN switch is pressed.

Modification of the execute phase of an instruction is illustrated in figure IV-14 This modified sequence is typical of a shift instruction. At time T0, the instruction is accessed from memory. starting at time T950, the instruction is executed; however, the normal 237.5-nanosecond execute phase is extended 237.5 nanoseconds for each shift (four, in this illustration). Note that clocks CL1X + and CL2X + are inhibited during the extended execution period. In a similar manner, the address phase is extended when required by the conditions defined above.

2.3 DECODING LOGIC

Words stored in the U register must be decoded to determine program processing requirements. This decoding procedure is accomplished on processor control cards 2 and 3 (44P0596 and 44P0597). Outputs are used to enable arithmetic and logical operations, memory access, and I/O circuits according to results of the decoding operation.

The 16 bits of an instruction word are divided into three fields: op code field (bits 12-15), M field (bits 09-11), and A field (bits 00-08). Each of these fields contains information which directs the various computer processes.

2.3.1 Op Code Field Decoding

Information contained in the op code field is decoded in three functional categories: class, set, and group.

Class decoding separates instructions into the following classes:

a. Single-word addressing instructions

b. I/O instructions

c. Other (includes single-word nonaddressing and double-word)

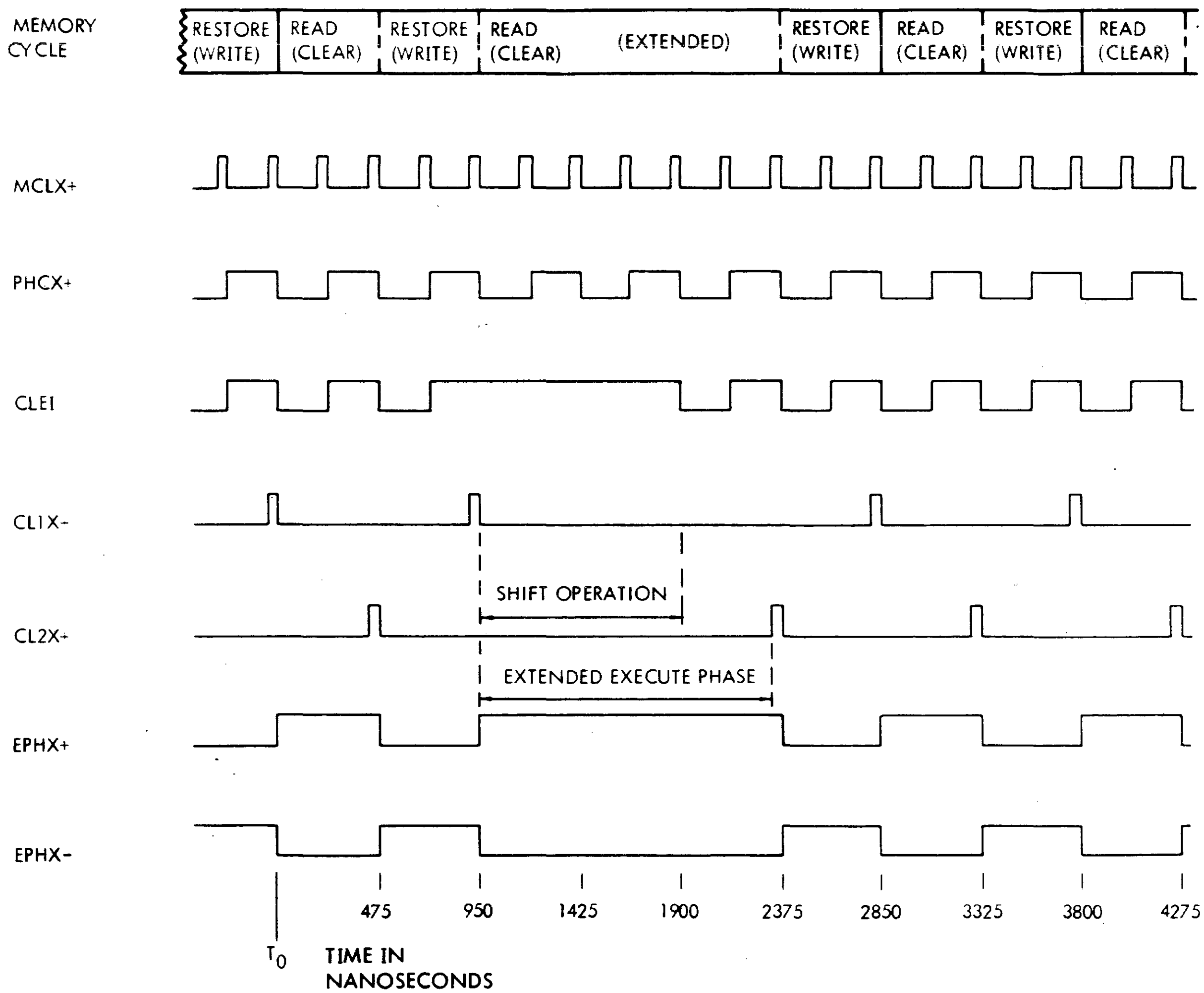

Figure IV-14. Example Of A Modified Clock Sequence

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Table IV-5 lists the op codes, signal names derived by decoding these codes, and class descriptions.

Table IV-5. Op Code Classes

Code (Bits 12-15)	Signal Name	Description
01-07	K1XX+	All single-word addressing instructions
00	K2XX+	Single-word nonaddressing and double-word instructions.
10	K3XX+	All I/O instructions.

Set decoding divides the single-word addressing instructions into subcategories: load, store, and arithmetic and logic. Table IV-6 lists these sets, the signal name derived from decoding, and set descriptions.

Table IV-6. Op Code Sets

Code (Bits 12-15)	Signal Name	Description
00-03	H1XX+	Instruction cycle execute phase of all load instructions.
04-07	H2XX+	Operand cycle execute phase of all store instructions and INR.
11-15 16-17	H3XX+ H4XX+	Instruction cycle execute phase of all arithmetic and logic instructions (except INR).

Group decoding is structured to gate various computer operations according to the desired function. Table IV-7 lists these groups, signal names derived from decoding, and instruction types. One of these groups is true for all single-word addressing instructions.

Table II-7. Op Code Groups

Code (Bits 12-15)	Signal Name	Instruction Type
01, 05, 11, 15	G1XX+	LDA, STA, ORA, ANA
02, 06, 12, 16	G2XX+	LDB, STB, ADD, MUL(*)
03, 07, 13, 17	G3XX+	LDX, STX, ERA, DIV(*)
04, 14	G4XX+	INR, SUB

2.3.2 M Field Decoding

The M field (bits 09-11) of the instruction word is decoded to determine the addressing mode for class K1 (single-word addressing instructions) and the instruction type for all other instructions. Note that class K3 contains all I/O instructions and the M field specifies a subtype. Address modes or instructions determined by decoding the M field are listed in table IV-8, arranged by op code class.

Table IV-8. M Field Decoding

Class	M Field Code	Signal Name	Address Mode or Instruction Type
K1 (K1XX+)	0-3	AC0X+ to AC3X+	Direct address
	4	AC4X+	Relative Address
	5	AC5X+	Index X
	6	AC6X+	Index B
	7	AC7X+	Indirect address

Table IV-8. M Field Decoding *(continued)*

Class	M Field Code	Signal Name	Address Mode or Instruction Type
K2 (K2XX+)	0	AC0X+	Control (HLT only)
	1	AC1X+	Jump
	2	AC2X+	Jump and mark
	3	AC3X+	Execute
	4	AC4X+	Shift
	5	AC5X+	Register change
	6	AC6X+	Immediate or extended (optional)
	7	AC7X+	Set or reset overflow
K3 (K3XX+)	0	AC0X+	External control
	1	AC1X+	Sense
	2	AC2X+	Data input
	3	AC3X+	Data output
	4	AC4X+	Auxiliary external control

2.3.3 A Field Decoding

For single-word addressing instructions, the A field is decoded to provide:

a. An effective address, or

b. A number, which when combined with the contents of the B, X, or P register, provides an effective address.

For single-word nonaddressing instructions, the A field specifies additional details for the instruction type determined by the M field. See tables 2, 3, and 4 in appendix G for types of additional instructions determined by the A field.

For double-word addressing instructions, the A field determines conditions to be met if the instruction is to be executed. Tables 5, 6, 7, and 8 in appendix G list the A field content for these conditions.

For extended addressing optional double-word instructions, bits 0-2 of the A field determine the address mode. Octal codes for this bit group are the same as the M field for single-word addressing instructions. Bits 3 through 8 contain the same octal codes specified in table IV-7 for op code groups for single-word addressing instructions. Note that for this set of codes, the most significant digit is never greater than one; consequently, bits 7 and 8 are always zero.

Double-word nonaddressing instructions are the immediate type and are identical with the extended addressing optional instructions described above, except that bits 0-2 always contain zero. The A field is used in I/O instructions to specify the logical unit number (bits 6-8) and device address (bits 0-5). See table 9 in appendix G for details of this assignment.

2.4 ARITHMETIC AND LOGICAL SECTION

The arithmetic and logical section consists of the R register, R register gates, arithmetic bus (A bus), adder, logic gates, and S register. Physically, all of these circuits except the S register are located on the three register cards (44P0592), six bits per card. The S or shift register is located on processor control card 4 (44P0593).

The R register receives operands or addresses from memory via the W register and holds these words during execution of an arithmetic or logical instruction. The R register gates enable either the set or reset output of the R register or the output of the U register onto the G bus, depending on whether an operand (or address) stored in the R register or the A field of the instruction word stored in the U register is to be used. The G bus provides this data to the adder in the case of arithmetic operations, or through a set of logic gates to the C bus, depending on the operation in progress. An additional input to the adder is from the S bus carrying data from the operation registers. The adder can provide the logical product of the contents of the R register and one of the operation registers, if required by the program instruction being executed. S register outputs are provided to the logic gates, allowing shifting of the data either right or left as specified.

The A bus is an intermediate bus used for arithmetic output to the C bus or for external data input to the logic gates and operation registers. It also provides an alternate path for transferring memory words to the C bus. Outputs from the adder and from the logic gates are provided to the C bus.

2.5 REGISTERS

The CPU contains nine registers. Each register bears a letter reference designation to facilitate identification: U, R, A, B, X, P, S, L, and W.

2.5.1 U Register

The U register is the instruction register in the control section of the CPU. It is a full-word register, 16 bits long, and is physically located on circuit card 44P0592. (44P0592 contains six bits each of all registers except the S and L register. The three cards are interchangeable.) The U register is clocked by SETU + from pin 31 of circuit card 44P0597, which occurs at the leading edge of IEPX +. The bits of the U register are set or reset by the corresponding output bits from the W register.

This register receives each instruction from memory through the W bus and holds the instruction during its execution. The control fields of the instruction word are routed to the decoding and timing logic where the codes determine the required timing and control signals. The address field from the U register, used for various addressing operations, is routed to the arithmetic/logic section of the CPU.

2.5.1.1 TRANSFER FROM MEMORY TO U REGISTER

During the instruction cycle, the instruction word located by the address in the L register is read out to the W register and transferred to the U register through the W bus.

2.5.1.2 TRANSFER FROM THE U REGISTER TO MEMORY

For many instructions requiring an operand, the address of the operand is contained in the instruction word held in the U register. This operand address is transferred to the L register through gates in the arithmetic/logic section and the C bus. The address from the U register can be modified during transfer to the L register as follows:

a. *Direct address.* No modification; bits 0-10 are transferred from the U register (SLU1 and SLU2 true) to the L register directly; addresses the operand in the first 2,048 memory addresses.

b. *Relative address.* The effective operand address transferred to the L register is formed by adding bits 0-8 (SLU1 true) from the U register to the contents of the P register. Addition is performed by selecting the contents of the P and U registers and bringing them into arithmetic logic. This permits addressing any word up to 512 addresses ahead of the current program address.

c. *Index address.* The effective operand address transferred to the L register is formed by adding bits 0-8 from the U register (SLU1 true) to the contents of either the X or the B register.

d. *Indirect address.* Same transfer as direct address except the word read from memory will be the address of an operand instead of the operand.

2.5.2 R Register

The R register is the operand register in the arithmetic/logic section of the CPU. It is a full-word register, 16 bits long, and is located on circuit card 44P0592. The R register is clocked by SETR + (pin 2 of circuit card 44P0597) at clock 2 (CL2X +) time. The bits of the R register are set or reset by the corresponding outputs from the W register.

The R register receives data words read from memory through the W bus and holds these words during execution of an arithmetic or logical instruction.

Operands are stored in the R register while an arithmetic or logical operation is being performed. For indirect addressing and for instructions with an operand address stored in the memory address following the instruction word, the operand address is read from memory into the W register and then transferred to the R register. The operand address is then routed to the L register through gates in the arithmetic/logic section and the C bus. I/O transfers bypass the R register. This allows momentary halting of the multiply and divide operations while the I/O transfer proceeds, without disturbing the multiplier held in the R register.

2.5.3 A Register

The A or accumulator register is one of the four operation registers. For multiplication operations, it forms the high-order half of the accumulator. It is a full-word register, 16 bits long, and is located on circuit card 44P0592.

The A register is clocked by SETA+ (pin 56 of card 44P0597) which occurs during program data in, load A register, shift, and certain register change instructions, and during the instruction cycle execute phase of all arithmetic and logical instructions. The bits of the A register are set or reset by the corresponding bits of the input words from the E, A, and C buses.

The register accumulates the results of logical and addition/subtraction operations, the most significant half of the double-length product in multiplication, and the remainder in division. It can also be used for I/O transfers under program control.

Input words can be transferred directly to the A register through the E, A, and C buses. These transfers are always controlled by an instruction. Output words can be transferred from the A register to the I/O cable through the S, A, and C buses. These transfers are controlled by an instruction which selects the A register onto the S bus.

2.5.4 B Register

The B register is the low-order half of the accumulator. It is one of the four operation registers. It is a full-word register, 16 bits long, and is located on circuit card 44P0592. The B register is clocked by SETB+ (pin 38 of card 44P0597) which occurs during program data in, load B register, shift, and certain register change instructions. The bits of the B register are set or reset by the corresponding bits of the input words from the A and C buses.

This register accumulates the least significant half of the double-length product in multiplication and the quotient in division. It can also be used for I/O transfers under program control and as a second hardware index register.

Information transfer to and from the B register is accomplished in the same way as described for the A register.

2.5.5 X Register

The X or index register is one of the four operation registers. It is a full-word register, 16 bits long, and is located on circuit card 44P0592. The X register is clocked by SETX+ (pin 11 of 44P0597) which occurs during load X register and certain register change instructions. The bits of the X register are set or reset by the corresponding bits of the input words from the A and C buses.

This register permits indexing operand addresses without adding time to the execution of indexed instructions by holding the value which modifies a base address contained in an instruction.

2.5.6 P Register

The operation P register is the program instruction counter. It is a full-word register, 16 bits long, and is located on circuit card 44P0592. The P register is clocked by SETP+ (pin 12 of card 44P0597) which occurs during the instruction cycle execute phase of I/O, execute jump immediate, single-word nonaddressing, and double-word instructions. SETP+ also occurs during mark and fetch instructions and execute jump or sense conditions. The bits of the P register are set or reset by the corresponding bits of the input words from the E, A, and C buses.

This register holds the address of the current instruction +1 and is incremented before each new instruction is fetched. The P register contents can be modified directly by a word received from the memory during a jump instruction.

Before the next instruction cycle begins, the address of the next instruction is transferred from the P register to the L register. The contents of the P register are transferred through the S bus to arithmetic/logic. Arithmetic/logic increments the address with the arithmetic gates and transfers the incremented count to the C bus. The incremented count is then restored to the P register and to the L register. At this time, the L register contains the address of the next instruction word to be fetched from memory and the P register holds the updated address.

2.5.7 S Register

The S register is the shift counter in the arithmetic/logic section of the central processor. It is a five-bit register and is physically located on card 44P0593. The S register is reset by reset shift register (RSHX+) from pin 29 on circuit board module 44P0596. The S register is set by shift control pulses derived from the U register.

This register controls the length of shift instructions in combination with the U register.

2.5.8 L Register

The L register is the memory word location register in the memory section of the CPU. It is a full-word register, 16 bits long, and is located on circuit card 44P0595. The L register is clocked by SETL+ (pin 29 of card 44P0593) which occurs on every clock 1 (CL1X+) except during increment memory and replace. The L register is set by the CB00+ through CB15+ bits from the C bus.

This register contains the address of the word to be accessed in memory during either a clear/write or read/restore cycle.

Input data from the E bus can be routed directly to memory through the A, C, and W buses. Data transfer must be preceded by an address transfer instruction to load the memory address into the L register. When the transfer is under the control of an instruction, the memory address will be generated as a normal operand address. Output words can be transferred directly from memory to the I/O cable through the A, C, and W buses, but a storage address must first be transferred to the L register by an address tranfer instruction or from the peripheral device.

2.5.9 W Register

The W register is a word register which holds data words for transmission to memory and stores data words transmitted to the CPU from the memory. It is a full-word register, 16 bits long, and is located on card 44P0592. The W register is clocked by SETW+ (pin 26 of card 44P0593) which occurs during the operand cycle execute phase of all store-type instructions and during the operand cycle of a program data in instruction. The bits of the W register are set or reset by the corresponding bits of the C bus. They are also collector-set independent of the SETW+ clock by the true bits from memory on the W bus during a memory read/restore cycle.

2.5.10 Register Change Instructions

The contents of an operation register may replace or modify the contents of that or another register. The process of incrementing and restoring the contents of the P register has been described in section 2.5.6. The contents of the A, B, and X registers may be transferred, incremented, complemented, decremented, or shifted. All these operations involve selecting the register onto the S bus, processing in the arithmetic/logic section, and transferring the new data through the C bus to the proper registers. Shifting is also performed in this transfer path. The contents of the selected register are shifted left or right as they are gated from the control and arithmetic logic to the A bus. Note that this transfer path is involved in all register change instructions. The register change instruction format is shown in figure IV-15.

The op code field equals 00 and M field equals 5 for this type of instruction. The A field enables the register change operation to be microprogrammed by arbitrary selection of source, destination, and type of transfer. The types of transfer, designated by the control function in bits 6-8, are summarized in table IV-9.

The normal operation involves designating one source and one or more destinations (note that if no source is designated, the selected destinations will be cleared). If more than one source is designated, the result will involve the logical-OR of the sources; complementing will produce the NOR of the selected sources. This microprogrammed register change type of instruction provides 64 combinations of sources and destinations, each of which can occur in eight different ways. Thus, a total of 512 different register change operations may be executed.

Table IV-9. Transfer Control Function Codes

Bit 8	7	6	Control Function
0	0	0	Transfer source, unconditional
0	0	1	Increment source and transfer, unconitional
0	1	0	Complement source and transfer, unconditional
0	1	1	Decrement source and transfer, unconditional
1	0	0	Transfer source, if overflow is set
1	0	1	Increment source and transfer, if overflow is set
1	1	0	Complement source and transfer, if overflow is set
1	1	1	Decrement source and transfer, if overflow is set

OP CODE FIELD				M FIELD			A FIELD								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1									
							Control Function			X	B	A	X	B	A
										Source			Destination		

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Figure IV-15. Register Change Instruction Format

2.6 MEMORY INTERFACE

The memory section consists of one to eight 4,096-word memory increments. Each memory increment has the following characteristics:

a. Full-cycle time of 950 nanoseconds.

b. Half-cycle time of 500 nanoseconds.

c. Access time of 425 nanoseconds.

d. Random access

e. Magnetic core, with four-wire, 3-D memory

Normal operation is full-cycle, either read/restore or clear/write. Half-cycle is used only in write operations and is required only for trap-in functions (refer to chapter VI).

The memory blocks share the L and W registers; only one memory increment at a time is cycled. The memory increments connect to the L and W buses and to four memory control lines. Each memory increment has a unique start pulse, allowing the CPU to select the memory increment to be cycled.

2.6.1 Memory Address

The memory is addressed through the 15-line L bus (high level = true). L-bus bits 0 through 11 are used to directly address up to 4,096 words in a memory increment. L-bus bit 12 is used to select the lower or upper 4K stack of an 8K memory increment. L-bus bits 13 and 14 are transferred to the memory control logic on card 44P0593 where they are decoded to determine which 8K memory increment is to be selected.

2.6.2 Control and Data Lines

In addition to the memory stack select pulse, three other control lines are used in the memory. These are the read-restore/clear-write, the full/half cycle, and the data guard control lines.

The read-restore/clear-write control line enables the performance of selected operating functions of the memory.

The full/half cycle control line enables selected cycling of the operating sequence to be performed.

The data guard control line inhibits memory drive current, preventing the memory core stack from being disturbed.

Word transfer to and from the memory is accomplished through the W bus, a 16-line (ground = true) bus.

2.7 TYPICAL OPERATING SEQUENCES

An understanding of the operating sequences will enable the technician to quickly understand the timing and waveforms of each instruction sequence. These operating sequences can vary, depending on the particular instruction being executed.

The three typical operating sequences are:

a. Access operand in memory

b. Store operand in memory

c. Indirect operand access

2.7.1 Access Operand in Memory

The access operand in memory is the simplest and most basic operating sequence. In this sequence, a single-word directly addressed operand is read from memory. This operating sequence is used for load, logic, and arithmetic (except multiply and divide) instructions. The timing of the suboperations of this sequence is illustrated in figure IV-16.

At time 0 (in microseconds), the instruction cycle (ICYX+) for the nth instruction is initiated. The n - 1 instruction is executed (IEPX+) while the current instruction (n) is read from the memory. at time 475, the n instruction is transferred to the U register. The instruction address phase (IAPX+) occurs while the n instruction is being restored in memory. The operand address is generated during IAPX+.

The operand cycle (OCYX+) is initiated at time 950. After the operand has been read from memory and stored in the R register, the address of the next instruction (n + 1) is generated (normally by adding 1 to the P register) and transferred to the memory L register. This suboperation is performed while the operand is being restored in memory. ICYX+ for n + 1 is then initiated at time 1900.

The operation to be performed upon the operand now contained in the R register occurs during the IEPX+ part of the ICYX+ for n + 1. This operand operation could be an ADD instruction, such as adding the operand value to the A register and storing the result in the A register, or simply a transfer of the operand to one of the operation registers (LDA, LDB, or LDX).

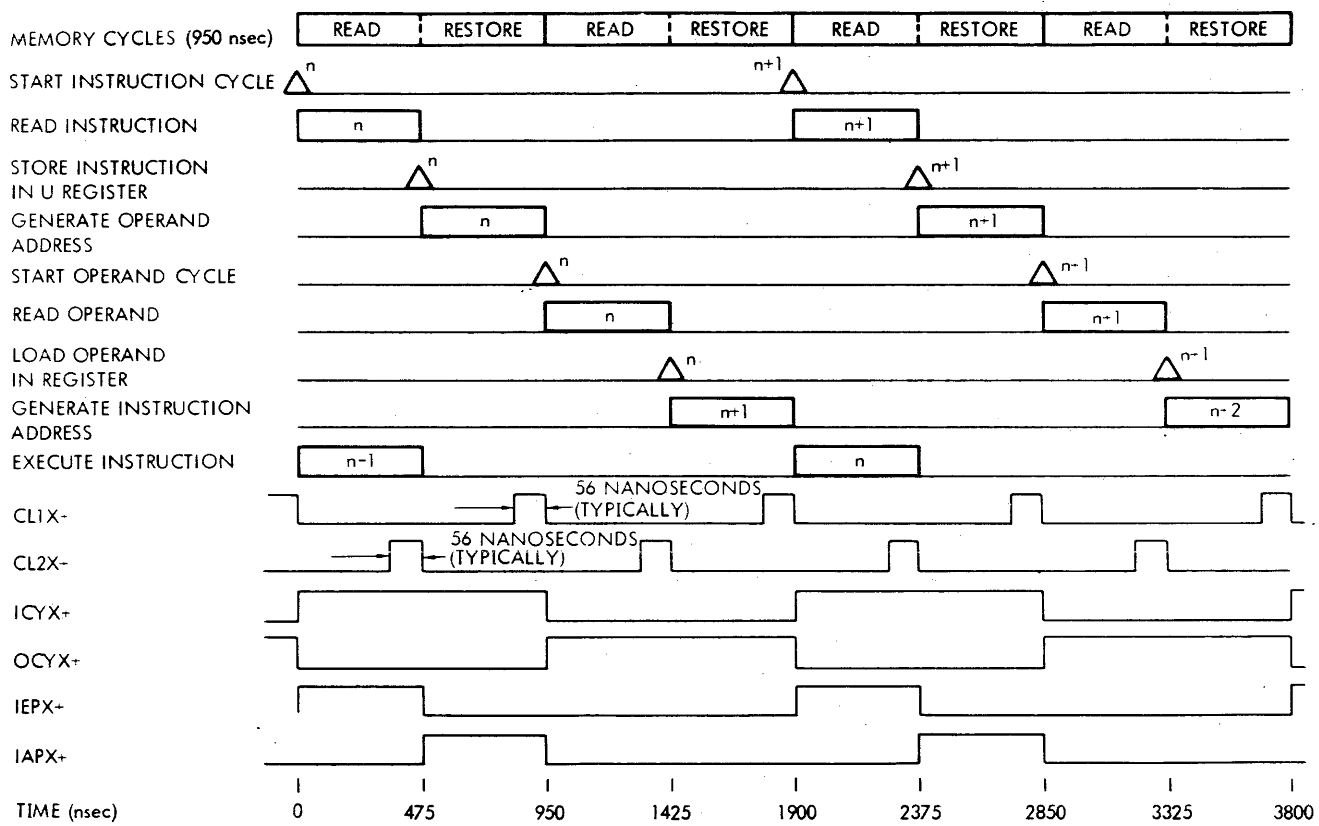

Figure IV-16. Sequence for Operand Access From Memory

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2.7.2 Store Operand in Memory

The store operand in memory (STA, STB, or STX) sequence is essentially identical to that for accessing an operand except the addressed memory cell is cleared and the operand is written into it. The timing of the suboperations of this sequence is illustrated in figure IV-17.

The nth instruction is accessed and the operand address generated during ICYX+ as before; execution of the n - 1 instruction occurs during IEPX+ of the nth cycle as indicated. However, during OCYX+, the operand is transferred to memory while the referenced cell is being cleared. During the last half of the cycle, the operand is stored into the cell just cleared. During this time, the address for the next instruction is generated. Note that there is no execution, as such, for this type of instruction (indicated by dashed lines in figure IV-17) because the execution has already been accomplished, in effect, by the transfer and storage of the operand in memory.

2.7.3 Indirect Operand Access

The indirect operand access operating sequence involves indirectly accessing an operand in memory by a single-word instruction. In this case, an address cycle (ACYX+) is required to read the indirect address word from memory before OCYX+ can be initiated. The timing of the suboperations of this sequence is illustrated in figure IV-18.

During ICYX+, the nth instruction is read from memory and stored in the U register as before. The previous instruction, n - 1, is executed during IEPX+. During IAPX+, the location of the indirect address word is generated. This address word is read from memory and stored in the R register as indicated in the timing diagram. For the case illustrated, the accessed address word contains the address of the operand (otherwise, another address cycle would be initiated to access a second address word, and so on). The operand address is transferred to the memory L register during the last half of ACYX+ to locate the operand read out during the succeeding OCYX+.

The generation of the address for instruction n + 1 and the execution of the instruction are then performed as in the case for the simple operand access previously described.

2.8 AUTOMATIC MEMORY ENABLE/DISABLE CIRCUIT

The automatic memory enable/disable (AMED) circuit is contained on the card 44P0237. Its function is to protect the contents of the computer memory during power turn on and turn off (before initiating power off, place computer in step mode).

When power is turned on, the SEN+5 signal is supplied to the AMED circuit (refer to

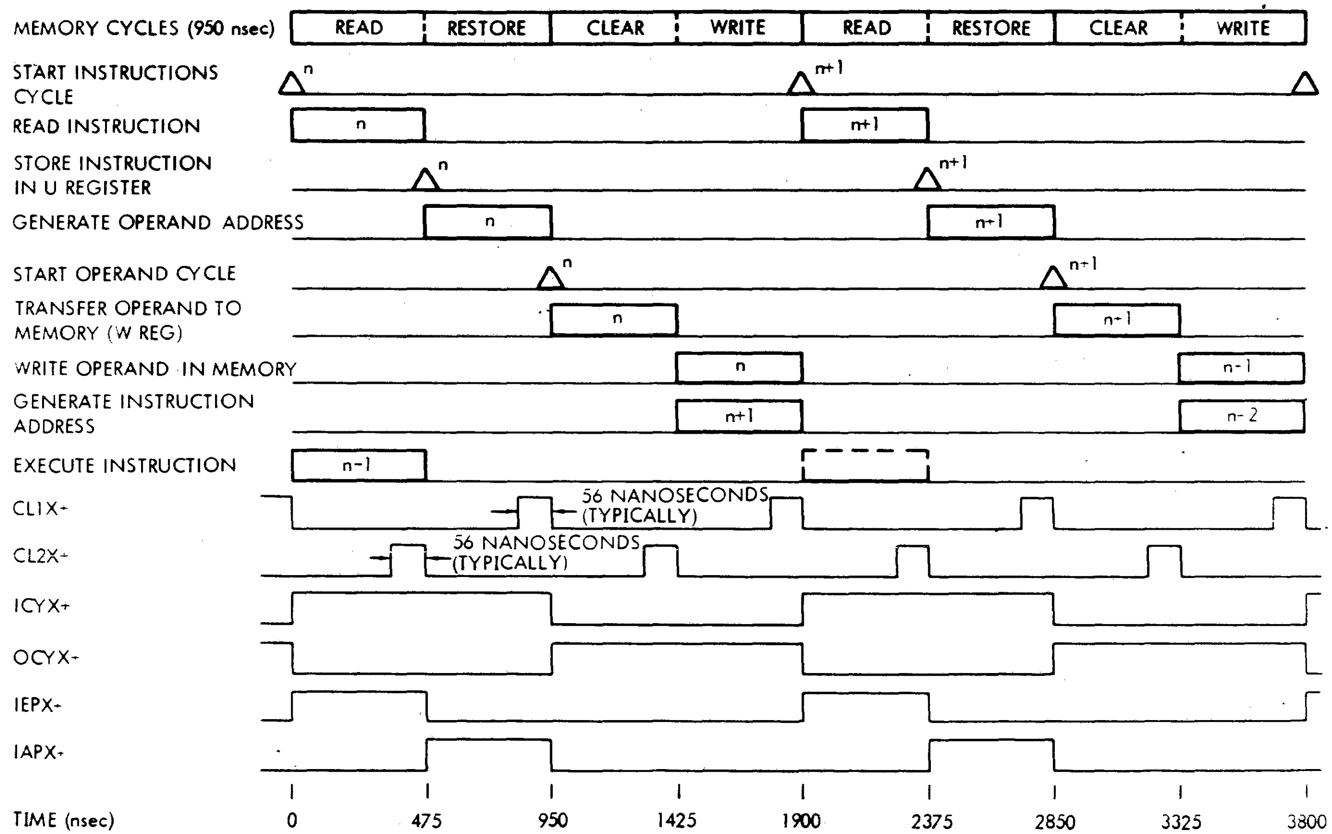

Figure IV-17. Sequence For Operand Storage In Memory

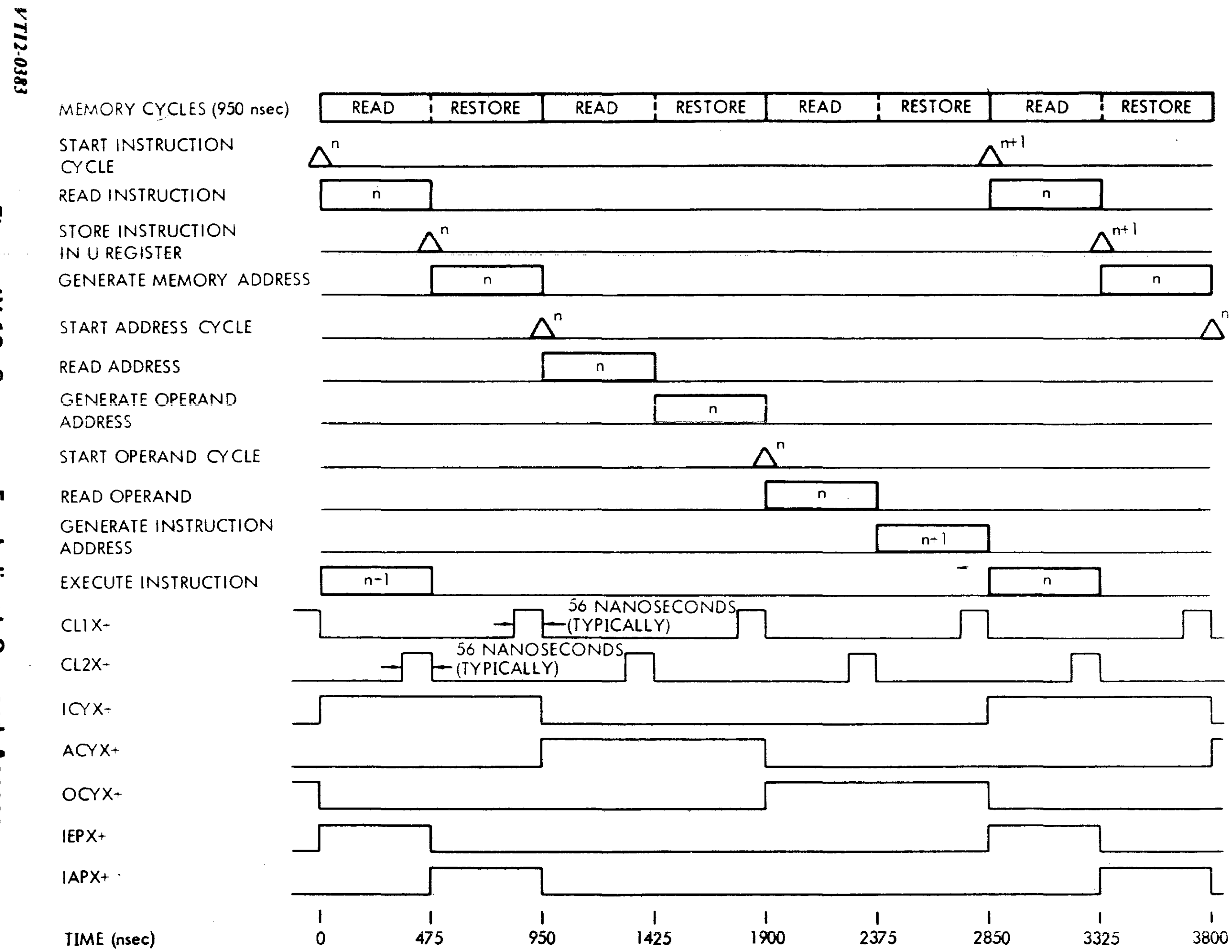

Figure IV-18. Sequence For Indirect Operand Access

logic diagram 95C0235). After a short delay time caused by the charging of capacitor C, pin 8 of IC1 goes to a low logic level. This energizes relay K1 which causes TCRX-, DAGS-, and SYRT- to go high.

When power is turned off, the SEN + 5 signal is removed from the AMED circuit. After a short delay time caused by the discharge of C1, pin 8 of IC1 goes to a high logic level. This de-energizes relay K1 which causes TCRX-, DAGS-, and SYRT- to go low.

SECTION 3
MAINTENANCE

3.1 GENERAL

The time required to correct system malfunctions will depend upon the efficiency of the procedures used. Although various specified techniques may be applied, there is no real substitute for logical analysis of the problem and isolation of the cause to the level of the replaceable component. Such an analysis can be based only upon knowledge of the equipment design.

Maintenance information for peripheral devices in the computer system is contained in the manufacturer's instruction manuals supplied with the equipment.

Integrated circuit (IC) design reduces the occurrence of computer malfunctions. The power failure/restart (PF/R) option provides an orderly shutdown in case of power failure or turn-off and restarts the program when power is restored. To prevent accidental setting of control panel controls during computer operation, all switches can be disabled with the power switch.

To ensure effective maintenance of the computer:

a. Study the documentation furnished with equipment.

b. Assess system performance with adequate test equipment.

c. Implement the available maintenance aids.

d. Apply orderly and logical troubleshooting techniques.

3.2 TEST EQUIPMENT

Table IV-10 lists the test equipment and tools required to maintain the CPU. These items also satisfy all maintenance requirements for the peripheral device controllers.

Table IV-10. Required Test Equipment

Equipment	Description
Oscilloscope	Tektronix, type 547 (or equivalent) with dual-trace plug in unit
Multimeter	Simpson, 260 or equivalent
Card extended	VDM, card 44P0540
Card puller	Titchener, 1731
Wire-wrap gun	Gardener-Denver, 14R2 or equivalent
Soldering iron	39-watt pencil type
Wire stripper	Thermo-strip type
Assorted hand tools	Screwdrivers, spin-tight wrenches, long-nosed pliers, etc.

3.3 TEST PROGRAMS

The MAINTAIN II test program system verifies correct system operation, including internal instructions, memory, internal options, and peripherals and their controllers. Malfunctions can be isolated to a specific area of the system and corrected.

MAINTAIN II is described in detail in the 620 test programs manual (document number 98 A 9952 060). Table IV-11 lists the Maintain II test programs.

3.4 TROUBLESHOOTING USING CONTROL PANEL

This section provides troubleshooting procedures for using the control panel to locate the basic problem area.

Table IV-11. Maintain II Test Programs

Program	Part Number
Test executive	91A0107-001
Instructions Test	92A0107-002
Memory test	92A0107-004
Teletype test	92A0107-005
Power failure/restart test	92A0107-008
Priority interrupt module test	92A0107-009
Memory protection test	92A0105-002
Real-time clock test	92A0105-001
Buffered I/O test	92A0107-010

a. Using the REGISTER and register entry switches on the control panel, set ones into all bit positions of the A, B, X, P, and U registers; then reset the registers to display zeros in all bit positions by pressing the BIT RESET switch. This operation checks the basic set and reset functions for all register flip-flop circuits in the CPU, but does not check gating into these registers from the internal buses.

b. Load all ones into the A register. Store the contents of the A register into memory address 0 by entering STA (050000) into the U register and pressing STEP. Clear the U register. Place the contents of memory address 0 back into the A register by entering LDA (010000) in the U register and pressing STEP. Display the contents of the A register. The A register contents should reflect the configuration that was loaded originally. These operations check communication between the A register and memory.

c. Set the U register to increment the A register and place the CPU in the repeat mode by pressing REPEAT. Then:

(1) Set the A register to all ones except the least significant bit. Press the STEP switch twice and note results. On the second step, the A register contents should be changed to all zeros.

(2) Set the U register to all zeros and set the P register to all ones except the least significant bit. Press STEP twice and note results. On the second step, the P register contents should be changed to all zeros.

This operation provides a major check of the arithmetic section of the CPU.

d. Load all ones into the A, B, and X registers. Complement each register by using the corresponding register complement instruction (CPA, CPB, and CPX). After executing the complement instructions the contents of the A, B, and X registers should be all zeros (one's complement of all ones). These operations check the A, B, and X set functions and gates (SETA, SETB, and SETX) and the A, B, and X select functions and gates (SELA, SELB, and SELX).

e. Load all ones into the A register. Store the contents of the A register in memory address zero (U = 050000). AND (ANA) the contents of memory address 0 with the contents of the A register (U = 150000). The result (should be all ones) is placed in the A register. Next, exclusively-OR (ERA) the contents of memory address 0 with the contents of the A register (U = 130000). The result (should be all zeros) is placed in the A register. Finally, OR (ORA) the contents of memory address 0 with the contents of the A register (U = 110000). The result (should be all ones) is placed in the A register. These operations check gates in the arithmetic unit of the CPU.

f. Load bit pattern 1010101010101010 into the A register. Logically rotate the contents of the A register one bit position to the left (LRLA, U = 004241). The A register contents should now be 0101010101010101. Rotate left again; the bit pattern should now be 1010101010101010. Logically shift the contents of the A register one bit position to the right (LSRA, U = 004341). The A register contents should now be 0101010101010101. Shift right again; the bit pattern should now be 0010101010101010. These operations check the shift gates in the arithmetic unit of the CPU.

g. Load all ones into the A register. Load highest numbered memory address into P register (0X7777).* Load 054000 (STA relative to P register) into the U register, then press STEP. The REPEAT switch must be OFF. The U register contents should now be all ones. Load all zeros into the A register. Load highest numbered memory address into P register (0X7777).* Load 054000 (STA relative to P register) into the U register, then press STEP. The REPEAT switch must be OFF. The U register contents should now be all zeros. These operations check communication between the U register and memory.

* X represents any digit 0 through 7 depending on computer memory size. X = 0 for 4K, X = 1 for 8K, X = 2 for 12K, X = 3 for 16K, X = 4 for 20K, X = 5 for 24K, X = 6 for 28K, X = 7 for 32K.

NOTE

To perform repeat operations in run mode, connect a jumper between pin 1 (ground) and pin 24 (RPCX-) of slot 12 of mainframe backplane.

3.5 CIRCUIT CARD TROUBLESHOOTING

Circuit cards can be made accessible for troubleshooting by installation on an extender card 44P0540 to extend the circuit card outside the rear of the computer frame. Signal waveforms can then be monitored at the IC terminals for troubleshooting purposes.

The physical location of specific ICs can be determined by referring to the assembly drawing of the particular circuit card The pin numbers and mnemonics associated with the IC are presented in the circuit card logic diagram, and a description of the IC is provided in the cirucuit card parts list. Assembly drawings, logic diagrams, and parts lists for the basic computer are provided in chapter X.

3.6 GENERAL TROUBLESHOOTING TECHNIQUES

The general steps in troubleshooting are shown in figure IV-19 and described in the following sections.

3.6.1 Define the Problem

Define the problem thoroughly. For example, if the ADD instruction does not produce the correct results, is the fault a function of the sign (plus or minus), of the carries, or of some other element. Are the operation registers being loaded properly. Use the displays, connector pins, and integrated-circuit terminals for gathering the necessary data.

3.6.2 Look for Obvious Solutions

Make sure that a malfunction has actually occurred. Relate problems to recent events, such as cleaning or servicing. Look for improperly set controls or test equipment and accidental disconnections of plugs, etc. Consider miscellaneous temporary failure, such as mechanical jamming of peripheral equipment.

3.6.3 Isolate to a Functional Area

Isolate the fault to a functional area, such as memory, control, arithmetic logic, operation register, I/O, peripheral controller, or peripheral device. The process of isolating the malfunctioning area is generally a straightforward process of eliminating areas that are operating properly.

3.6.4 Analyze the Area

When the fault has been isolated to a functional area, use the logic and timing diagrams, and observe circuit waveforms to isolate the problem to an individual replaceable element. Put the computer in step mode (STEP indicator on) before removing input power.

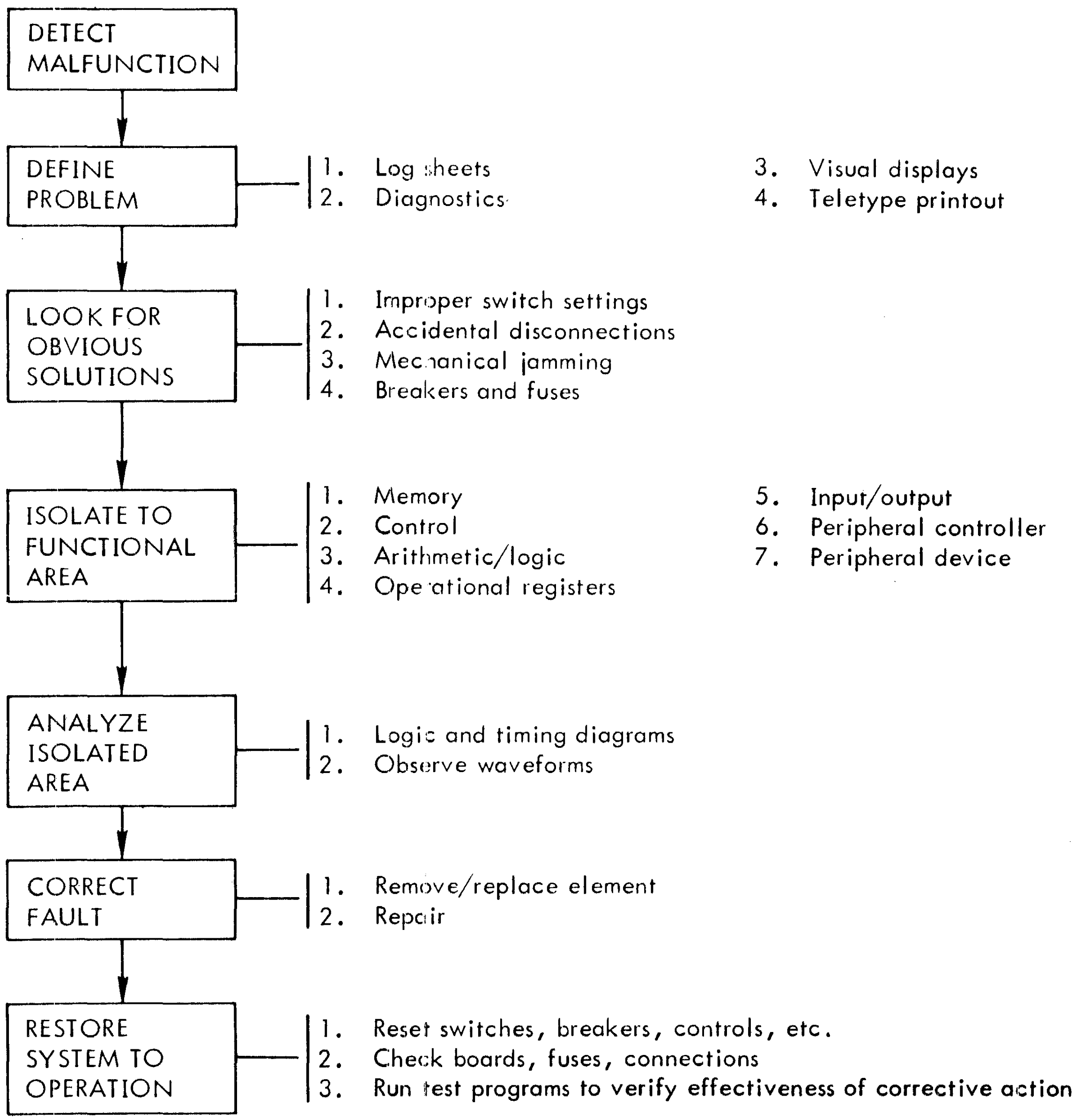

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Figure IV-19. General Troubleshooting Steps

3.6.5 Correct the Fault

Replace the faulty card or component. Before restoring power, take any necessary measures to prevent recurrence of the failure.

3.6.6 Restore the System to Normal Operation

When the system appears to be operating properly, return it to normal operating conditions. If circuit cards have been unseated, be sure all are properly reseated in the connectors. Set all controls and place the power switch in the PWR ON position. Finally, verify proper operation by running the test programs.

3.7 GENERAL TROUBLESHOOTING PROCEDURES

When it has been determined that the computer is not operating properly, the general characteristics of the failure will, in most cases, immediately indicate the faulty section of the system. A typical failure in the CPU will produce failures in a large percentage of the test programs. Memory failures of a single bit or word are rare and generally require special test procedures which may result in clearing the section of the memory involved.

If the failure is catastrophic and all instructions fail, the cause is usually in the timing, decoding, and control section.

Incorrect arithmetic operations or incorrect incrementing of the P register indicates that the failure is in the arithmetic and registers section.

Memory failures may be evidenced by repeated halts or by completely random instruction sequencing.

I/O failures are restricted to I/O instructions and are associated only with the logic of the I/O device. An I/O failure can be easily diagnosed if failure occurs in I/O routines and not in internal routines.

CHAPTER V

MEMORY

SECTION 1
FUNCTIONAL DESCRIPTION

1.1 GENERAL

The 620/L-100 memory is a parallel, random-access, three-wire/three-dimensional, magnetic core memory used to store all instructions and data. The memory can be expanded to 32,768 words (32K) in 4,096-word (4K) increments; each word contains 16 bits.

1.2 FULL CYCLE

During a full memory cycle, the memory performs a reading sequence followed by a writing sequence. When a word is transferred from the CPU to memory, the memory cycle is a clear/write operation. When a word is transferred from memory to the CPU, the memory cycle is a read/restore operation. Both full-cycle operations require 950 nanoseconds, and memory access time is 425 nanoseconds.

1.2.1 Clear/Write

A clear/write operation loads the memory. The clear portion of the operation resets the addressed cores to zero; the write sequence then loads data in the addressed cores.

During the clear sequence, the X and Y drive wires of an addressed word are activated (read current) to magnetize the cores to zero. Addressed cores already at zero are not changed.

During writing, the X and Y drive wires of an address word are activated (write current) to magnetize the cores to one. If a core must be zero, the associated inhibit wire generates an inhibit current that cancels X drive current, preventing the core from switching. The word, with correct bit configuration, is thus loaded into memory.

1.2.2 Read/Restore

A read/restore operation reads information from memory. The read portion of the operation unloads the addressed word from memory; the restore immediately reloads (writes) the word in the same core location.

CHAPTER V
MEMORY

During reading, the X and Y drive wires of an addressed word are activated (read current) to magnetize the cores to zero. Addressed cores already at zero are not changed. If an addressed core is one, a voltage is induced in the associated sense wire when the core switches to zero. The sense voltage is then interrogated and amplified to provide a memory read bit.

During the restore sequence, the X and Y drive wires of an addressed word are activated (write current) to magnetize the cores to one. If a core must be zero, the associated inhibit wire generates an inhibiting current that cancels X drive current, preventing the core from switching. The word, with correct bit configuration, is thus loaded into the same core location.

1.3 HALF CYCLE

The memory is also capable of performing a half-cycle operation which is required for trap-in functions (refer to chapter VI). After the first half cycle (clear or read), the memory will stop until it receives another memory start signal to initiate the second half cycle (usually write, for trap in). The write half cycle can be initiated 475 nanoseconds (minimum) after the start of the first half cycle and is completed in 475 nanoseconds. Access time for the half-cycle operation is the same as in full-cycle operation.

1.4 MAGNETIC CORE OPERATION

The basic information storage element of the memory is the magnetic core. The core is a toroid of ferrite that can be magnetized in two discrete directions representing the presence or absence of a binary bit. The magnetization is a result of current passing through the core. Total current must reach a minimum strength before the core becomes magnetized. The direction of current flow through the core determines the direction of magnetization; the two possible directions of current flow are called read and write.

The memory uses the coincident-current technique to magnetize cores. Two perpendicular wires, X drive and Y drive, pass through each core. During memory operations, the current on any drive wire is approximately one-half of the current necessary to magnetize a core. Because of the orientation of the cores and wires in a plane, only the core at the intersection of two activated drive wires becomes magnetized. For simple analysis, a three-core-by-three-core matrix is shown in figure V-1. The figure indicates the total driving current received by each core when wires X2 and Y2 are activated. Only the center core is magnetized, since it is the only one that receives the full driving current, I.

1.5 MEMORY CIRCUIT CARDS

The memory circuits are contained on five types of circuit cards:

a. *The memory stack card* contains a diode-decoding matrix, a 4-by-16K magnetic core array, and a sensistor. One memory stack card is required for each 4K memory increment.

b. *The driver/sink switch card (44P0578)* contains 16 driver and 16 sink switch pairs, address multiplexer and decoder, driver/sink switch timing, and current source circuits. One driver/sink switch card is required for each 8K memory increment.

c. *The sense/inhibit card (44P0506)* contains 16 sense amplifiers and 16 inhibit drivers. One sense/inhibit card is required for each 4K memory increment.

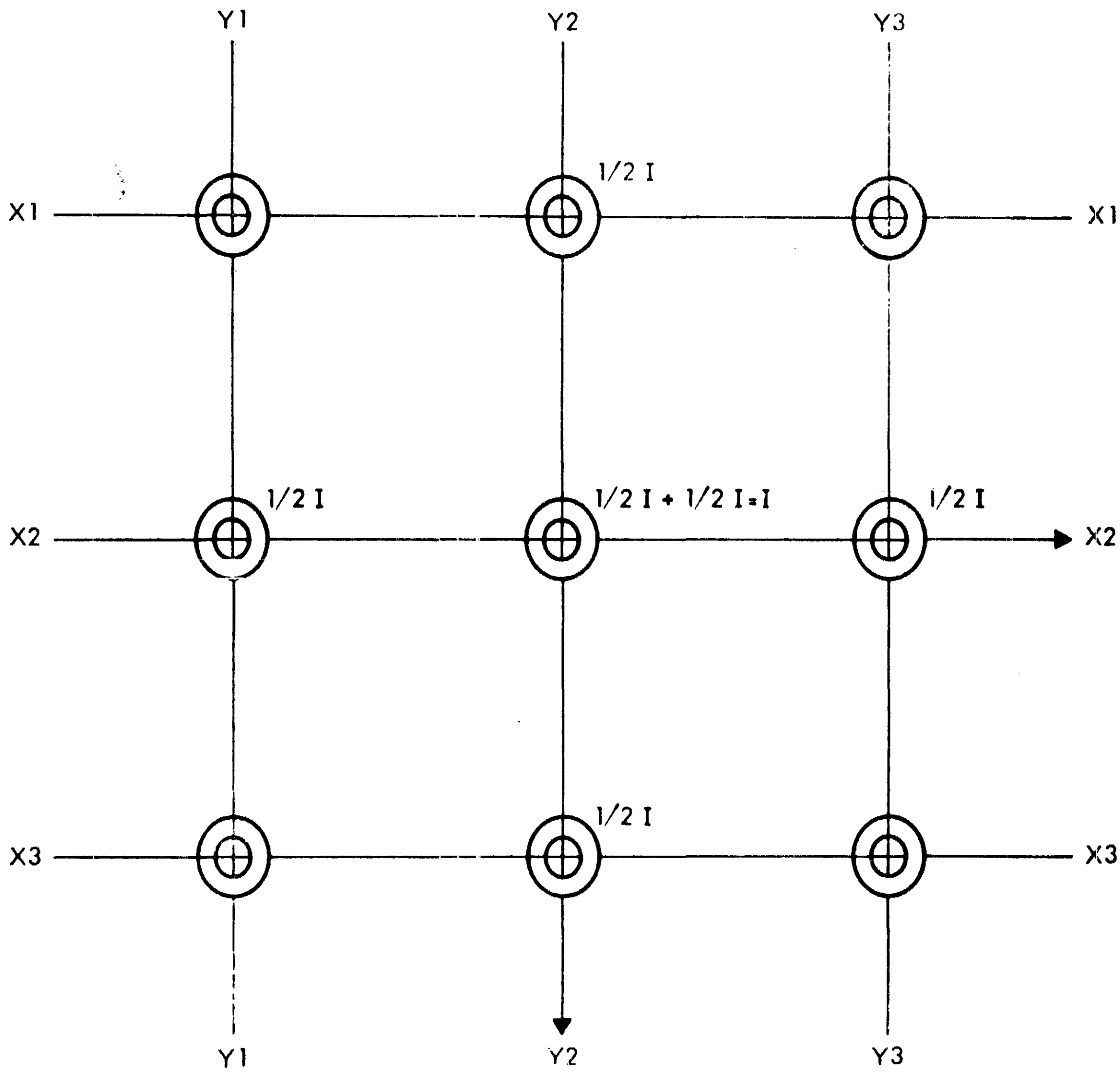
d. *The memory timing control card (44P0599)* generates control signals for the total memory system. Only one memory timing control card is required for any size memory system.

e. *A memory buffer card (44P0521)* is installed in memory systems larger than 8K to buffer L and W bus signals.

Figure V-2 illustrates the functional circuit blocks of the memory in relation to the five circuit cards.

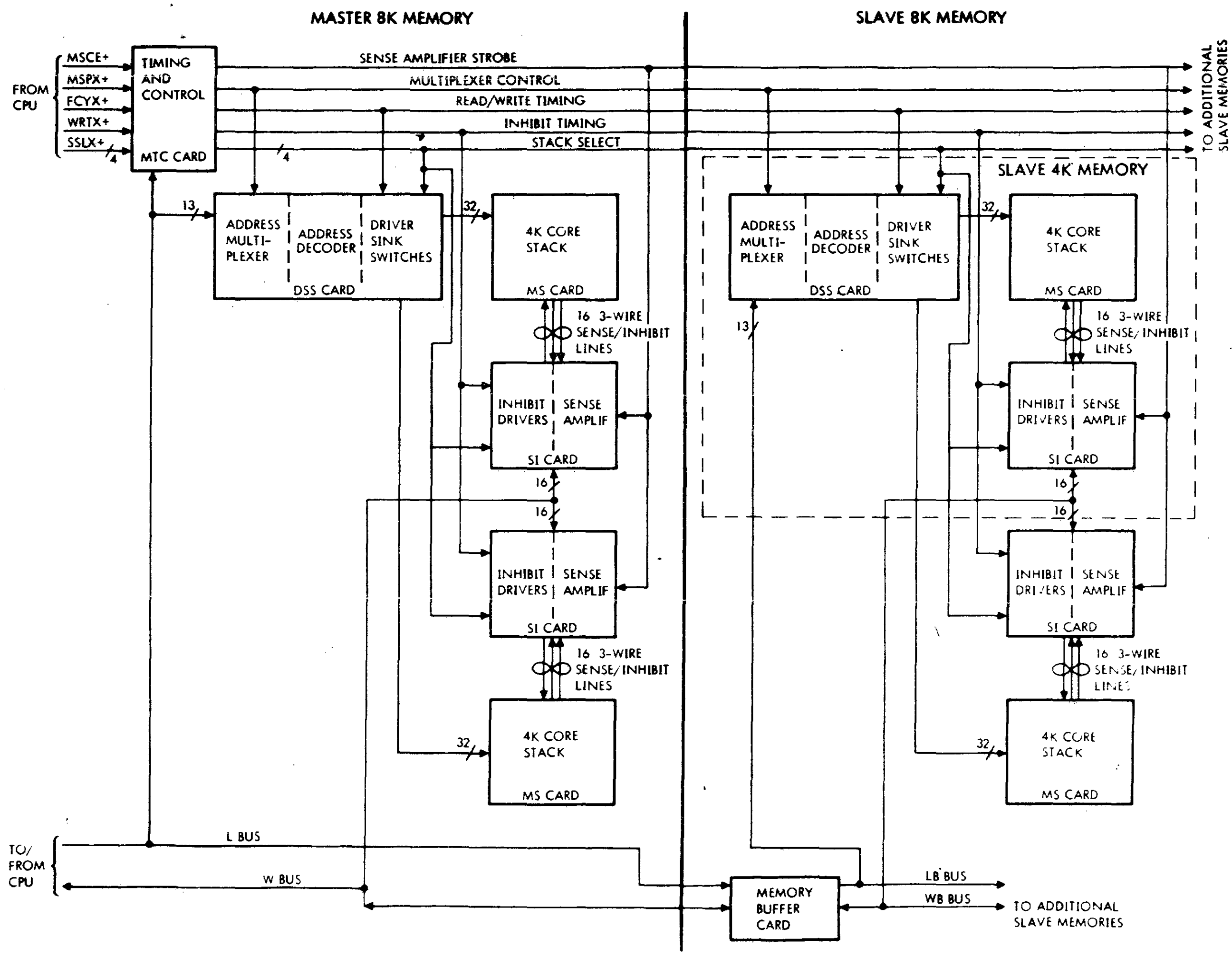
1.6 MEMORY STACK CARD

The memory stack card consists of a diode-decoding matrix and a planar magnetic core array composed of sixteen 4K mats. Each mat, which is one bit of the 16-bit word, contains 64 rows (X lines) and 64 columns (Y lines) of magnetic cores (refer to figure V-3). Selection of one of the 64 X or 64 Y lines is implemented with two diodes per line and an 8-by-8 driver/sink switch matrix. The diode end of the matrix is designated the drive end and the nondiode end, the sink end (figure V-4). These drive and sink ends are driven by the driver/sink switch card circuits. There are 256 diodes for each 4K stack.



VT11-0570A

Figure V-1. Three-Core-by-Three-Core Matrix



VT13-0274

Figure V-2. 620/L Memory Block Diagram

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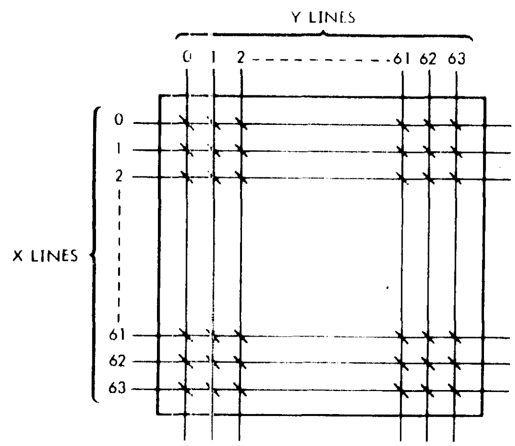
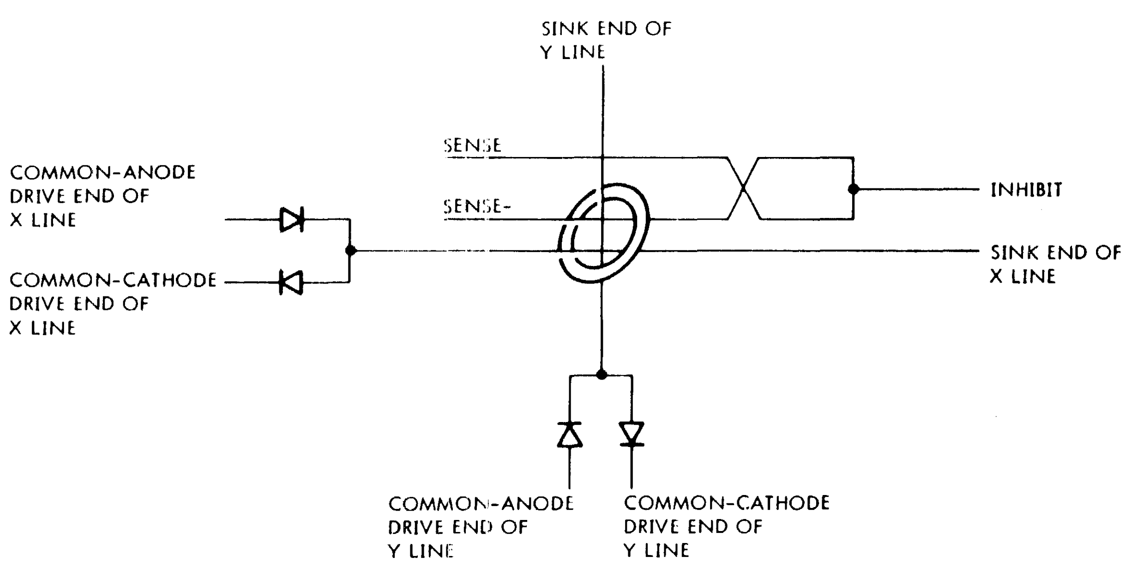
MEMORY



NOTE: A SENSE/INHIBIT LINE, NOT SHOWN ABOVE, ALSO PASSES THROUGH ALL CORES OF A 4K MAT PARALLEL TO THE X LINES.

VT11-1202

Figure V-3. 4K Core Mat



VT11-1203

Figure V-4. Memory Control Lines

1.6.1 Control Lines

Three control lines (X, Y, and sense/inhibit) pass through each magnetic core.

a. *X Lines.* Each X line passes through the same row of core in all sixteen 4K mats. The current in the selected X line will be one-half the current required to switch the state of a core. The direction of the current depends on whether memory is being written into or read from.

b. *Y Lines.* Each Y line passes through the same column of core in all sixteen 4K mats. The current in the selected Y line will be one-half the current required to switch the state of a core. The direction of the current depends on whether memory is being written into or read from.

c. *Sense/Inhibit Lines.* A sense/inhibit line passes through all cores of a 4K mat, parallel to the X lines and perpendicular to the Y lines. Each mat has an individual sense/inhibit line. The sense/inhibit line senses the state of the cores. If a core is one, an induced voltage is applied to the associated sense amplifier; if a core is zero, no voltage is induced. During reading, the sense amplifier outputs are strobed onto the W bus.

   The sense/inhibit line also routes an inhibit current through an addressed core into which a zero is to be written. During write operations, half-current is applied to the selected X and Y lines to set the addressed cores to one. For zero cores, the inhibit current cancels the X line current to prevent the addressed core from switching to one. Thus, a zero bit from the W bus generates inhibiting current; a one does not.

1.7 DRIVER/SINK SWITCH CARD

The 16 driver and 16 sink switch pairs contained on this card provide X and Y drive for two 4K memory stack cards. This is accomplished by timesharing read/write driver switch pairs for the X and Y lines, and making the X and Y sink switch pairs common to both stack cards. A low address bit 12 (L12X+) selects eight driver switch pairs for the lower 4K stack (4K-A); a high address bit 12 selects eight driver switch pairs for the upper 4K stack (4K-B). Address bits 0 through 5 are multiplexed with the Read/Write (RXXX −) signal, and then decoded to select the proper driver switches for the 4K-A or 4K-B cores. Address bits 6 through 11 are decoded to select the proper sink switches which are common to both 4K-A and 4K-B cores.

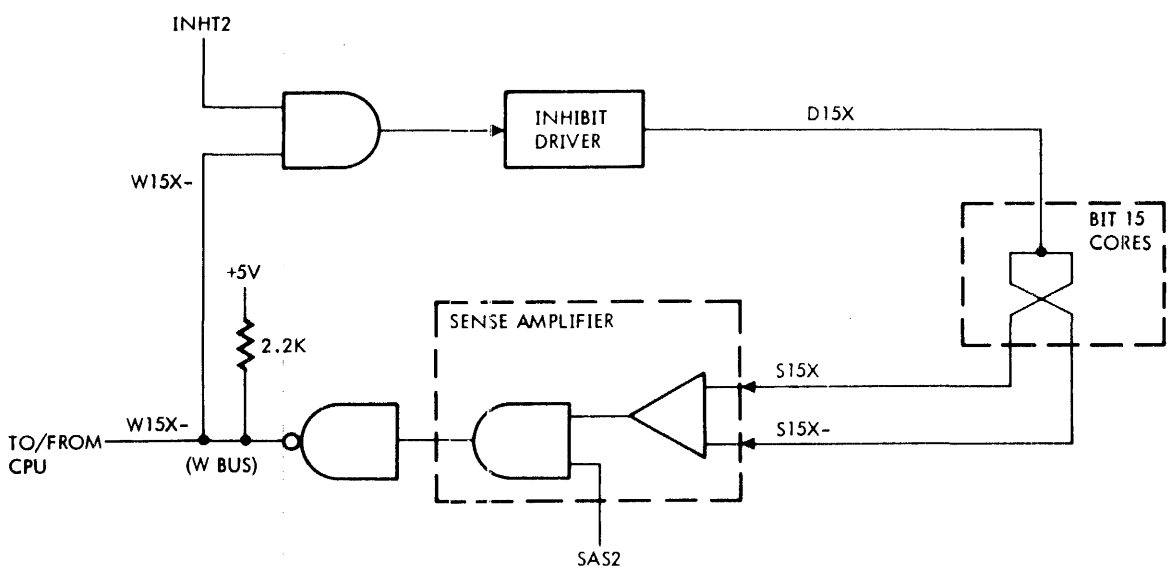
The driver/sink switch timing provides stack select and read/write timing for the driver and sink switch circuits.

The driver/sink switch card also contains two sense-type current sources with the level adjustable by two potentiometers on the module. Two thermistors, located on the DSS, control the current level with respect to the ambient temperature to provide the optimum core drive.

1.8 SENSE/INHIBIT CARD

The sense/inhibit card contains 16 sense amplifiers and 16 inhibit drivers, referred to as 16 pairs. Each pair is associated with a sense inhibit line on the stack module to form one sense/inhibit loop for a single bit. A sense/inhibit data loop for bit 15 is illustrated in figure V-5.

The sense amplifier senses the state of the core by comparing the sense line voltage with a predetermined threshold voltage. The output of the sense amplifier is strobed by a sense amplifier strobe and buffered by an open-collector gate onto the W bus.



VT11-1204

Figure V-5. Sense/Inhibit Data Loop for Bit 15

The inhibit drivers, controlled by inhibit timing, receive data from the W bus during the write half cycle to provide inhibit current for a data bit of zero; no inhibit current is supplied for a data bit of one.

1.9 MEMORY TIMING CONTROL CARD

The memory timing control card accepts memory start and operational control signals from the CPU and provides all timing and control signals required to perform the memory operation. Control signals generated on this card are precisely timed by a tapped delay line (refer to figure V-6). When a memory start signal is received, a pulse is sent into the delay line and, at precise intervals along the delay line, signals are tapped off. Selected tapped signals combine with control signals to generate internal memory timing signals. During a half-cycle operation, the delay line is prohibited from initiating a second delay line start pulse to time the second half-cycle of a full-cycle memory operation. Internal memory timing signals are:

a. Sense Amplifier Strobe (SASX-).

b. X, Y Read Sink Switch Timing (RSTM-).

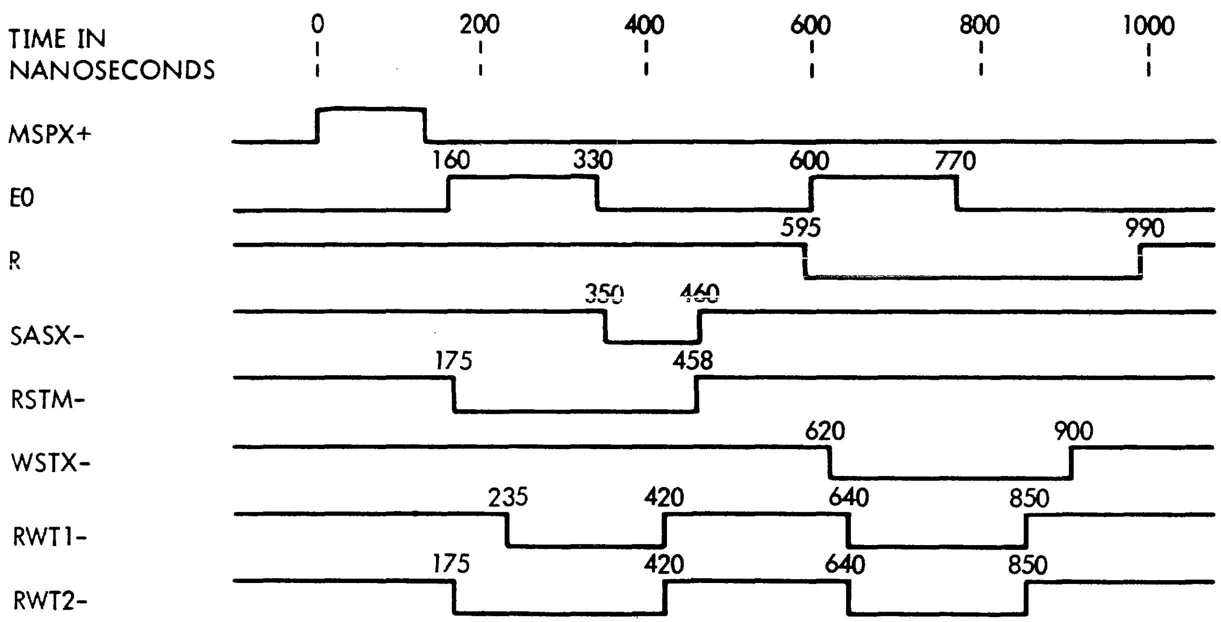
c. X, Y Write Sink Switch Timing and Inhibit Driver Timing (WSTX-).

d. X, Y Read and Write Driver Switch Timing (RWT1-, RWT2-).

Operational signals from the CPU include: Memory Start (MSPX+), Full Cycle (FCYX+), and Read/Write (WRTX+). FCYX+ controls a flip-flop on the memory timing control card which indicates whether a full-cycle or half-cycle memory operation is to be performed. WRTX+ controls a gate on the memory timing control card which generates a sense strobe (SASX-) signal indicating whether a read/restore or clear/write operation is to be performed.

1.10 MEMORY BUFFER CARD

The memory buffer card provides memory signals with the drive current required for routing to and from all memory increments above 8K by applying each of the signals to driver circuits. The memory signals to these driver circuits consist of the W register bits (W00X- through W15X-), the first 13 L register bits (L00X+ through L12X+), and the Read Sink Timing (RSTM-) signal. Refer to logic diagram 91D0297 in chapter X during the following memory buffer card description.



NOTES: 1. E0 IS FIRST TRAP OF DELAY LINE
2. TIMING SHOWN IS TYPICAL

Figure V-6. Nominal Timing Control Waveforms

Signals L00X+ through L12X+ are routed through driver circuits to become LB00+ through LB12+. These signals are then routed to driver/sink switch cards in the expansion memories.

W00X- through W15X- are routed through the memory buffer card both to and from the expansion memories. During a clear/write operation, these W register bits are transferred from the CPU (cards 44P0592) and enter the memory buffer card. These signals are amplified by open-collector gates to become WB00- through WB15-. These buffered signals are then routed to the sense/inhibit cards in the expansion memories.

During a read/restore operation, signals WB00- through WB15- are transferred from the expansion memories and enter the memory buffer card. These signals are then inverted and gated by the RSTM- signal through open-collector NAND gates to become the W00X- through W15X- which are routed to the W register in the CPU (cards 44P0592).

1.11 MEMORY INTERFACE OPERATION

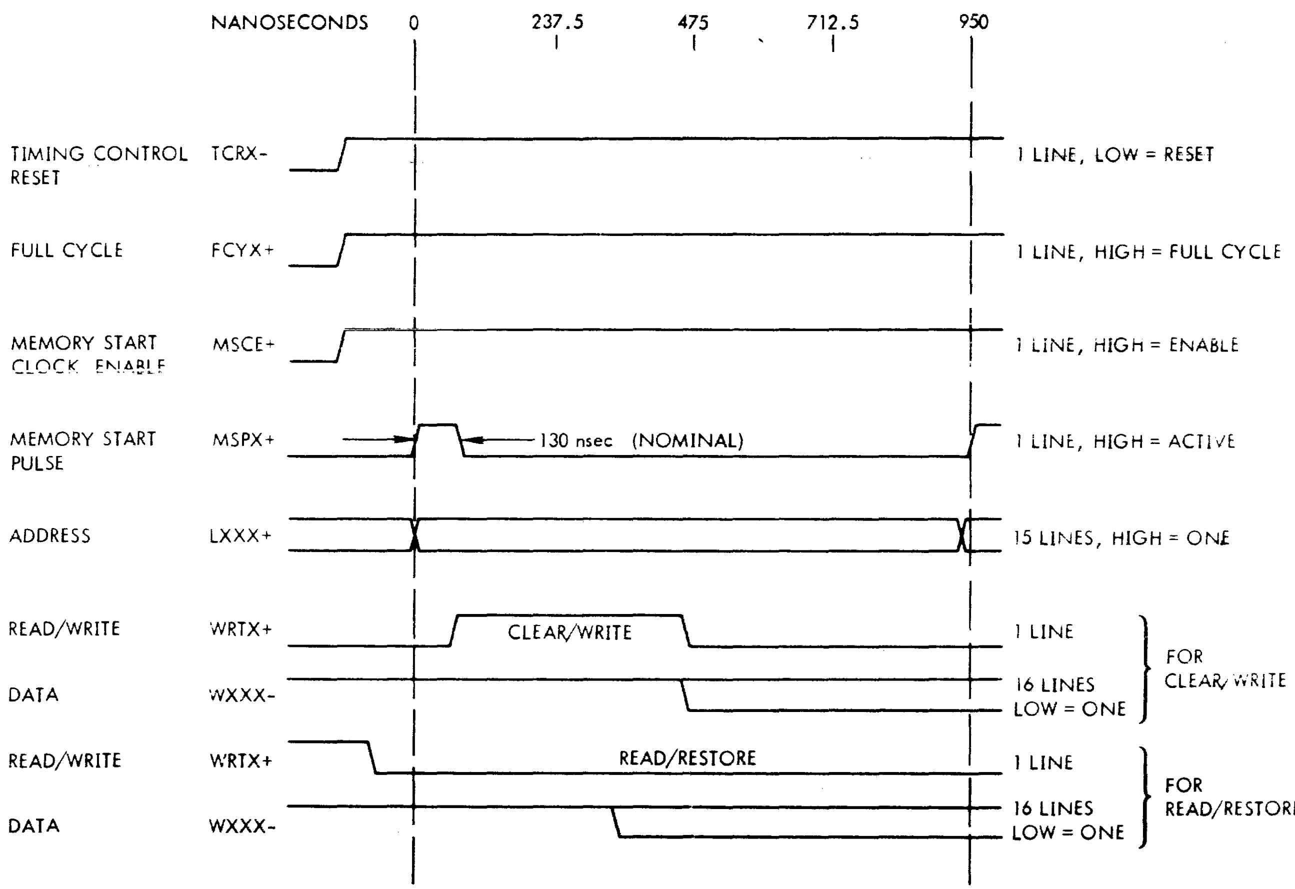
Addresses are sent to memory via the L bus, and data are sent to or from memory by the W bus. Refer to figures V-7 and V-8 for full- and half-cycle interface waveforms.

The CPU requests access to memory by raising a memory start pulse. The memory cycle begins after a decode delay. The memory performs either a read/restore or clear/write operation depending on the level of the control line write/read (WRTX+). For the read/restore cycle, data are available on the W bus 420 nanoseconds after the leading edge of the memory start pulse. During the time interval of 550 to 950 nanoseconds after the leading edge of the memory start pulse, data on the W bus are written into memory in the write half cycle.

The memory can perform half-cycle or full-cycle operations, depending on the level of FCYX+. For a half-cycle operation, control line FCYX+ from the CPU is at a low level causing the memory to stop after the read half cycle. The memory waits for the second memory start pulse before performing the write half cycle.

1.12 WRAP-AROUND ADDRESSING

Wrap-around addressing is available upon request as a standard feature in the 620/L-100 memory. This feature automatically prevents the CPU from trying to address data to or from nonexistent memory locations. Without the wrap-around feature, data read out of a nonexistent memory location result in zero and data written in are lost.



VT11-1385

Figure V-7. Full-Cycle Interface Waveforms

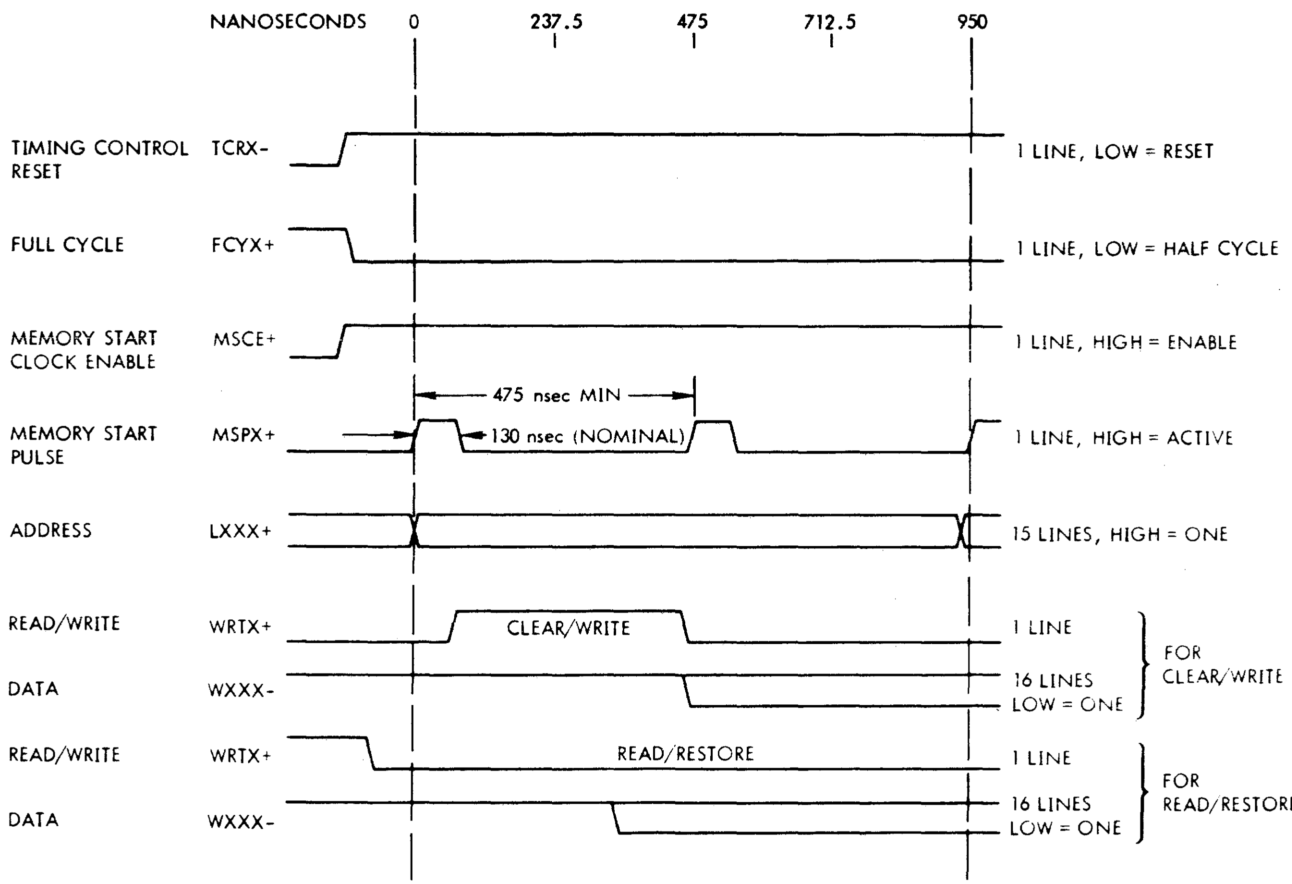


Figure V-8. Half-Cycle Interface Waveforms

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CHAPTER V
MEMORY

Wrap-around addressing is implemented with jumper connections on the backplane connector of the memory timing control card (44P0599, slot 6) and the processor control 4 card (44P0593, slot 13). The jumpers connect to the memory address bits (L12X, L13X, and L14X) used in selecting a particular 4K memory increment. By grounding some or all of these memory address bits, wrap-around addressing of 4K, 8K, or 16K can be implemented. For 4K wrap-around, all three address bits are grounded; for 8K wrap-around, the two most significant address bits are grounded; for 16K wrap-around, only the most significant address bit is grounded. The wrap-around jumper pin assignments for the various memory sizes are listed in table V-1.

In a computer with a 4K memory (addresses 0 through 4,095) wired for 4K wrap-around addressing, each existing memory location can be addressed by its own address plus seven corresponding addresses in nonexistent memory. That is, location 0 is addressed by 0, 4,096, 8,192, 12,288, 16,384, 20,480, 24,576, and 28,672. For 8K wrap-around addressing, each existing memory location can be addressed by its own address plus three nonexistent memory addresses and, for 16K wrap-around addressing, its own address plus one nonexistent memory address.

Table V-1. Wrap-Around Addressing Connections

Memory Size	Grounded Pins
4K	Slot 13, pin 52 (L14X +) Slot 13, pin 50 (L13X +) Slot 6, pin 8 (L12X +)
8K	Slot 13, pin 52 (L14X +) Slot 13, pin 50 (L13X +)
16K	Slot 13, pin 52 (L14X +)

Note: Remove wire from the pins before they are grounded.

1.13 LOADER PROTECTION

Loader protection is an optional feature to prevent writing into memory locations that contain the bootstrap loader and binary load/dump routines. (These memory locations can be read; however, provided there are no jump instructions included that would alter the contents.) The bootstrap loader and binary load/dump routines occupy the last 400 octal addresses of the computer memory. The first memory location occupied by these routines is X7400, where X represents 0 through 7 depending on the memory size of the computer system.

A toggle switch located behind the control panel in the lower left corner of the mainframe is used to enable and disable the loader protection circuit. When the switch is in the disable position, the loader protection circuit is disabled and all memory locations are available for storage. However, when the switch is in the enable position, this circuit prevents writing into the memory locations (X7400 through X7777) containing the bootstrap loader and binary load/dump routines.

The loader protection option, when enabled, may be operated in any one of the operating modes by modifying the wiring on the 620/L-100 backplane:

(1) Upon detection of an error, the write cycle is changed to a read cycle.
(2) Upon detection of an error, the write cycle is changed to a read cycle and the CPU goes to STEP.
(3) Upon detection of an error, the write cycle is changed to a read cycle and an interrupt is generated to the PIM.

The loader protection circuit is located on the memory timing and control card (refer to the lower-left portion of sheet 1, logic diagram 91D0363). Signals L08X+ through L14X+ are routed to the loader protection circuit. Signals L08X+ through L11X+ are at a high logic level for octal addresses 7400 and higher. Signals L12X+ through L14X+ are high when the address indicates the last 4K increment in the memory system. L12X+, L13X+, and L14X+ pass through jumpers A, B, and C (which are installed at the factory according to the computer memory size as indicated in table V-2).

With the loader protection switch in the disable position, the Loader Protection Enable (LPEX+) signal is at a low logic level to disable the loader protection circuit. With the switch in the enable position, LPEX+ is high to enable the circuit.

1.13.1 Store or Increment Memory Instructions

When executing the store or increment memory instructions with the loader protection circuit enabled, the following events occur if the memory location to be stored into is in the bootstrap and binary load/dump area. The read/write instruction (WRTX +) is forced to the low state. When the Set R Register (SETR +) signal changes to a high state, the SQP2 signal is in a low state and causes the computer to go into a step operation by generating the stop control (SOPX +) signal on card 44P0595.

1.13.2 Trap-In Operations

When executing a trap-in request with the loader protection circuit enabled, the following events occur if the memroy address provided by the trapping device is in the bootstrap and binary load/dump area. WRTX + and the Memory Start Pulse (MSPX +) are inhibited. When the Set W Register (STW1-) signal changes to a low state, the SQP2 signal is in a low state and causes the computer to go into a step operation by generating SOPX + .

Table V-2. Loader Protection Jumper Connections

Memory Size	Jumper
4K	None
8K	C to C
12K	B to B
16K	B to B and C to C
20K	A to A
24K	A to A and C to C
28K	A to A and B to B
32K	A to A, B to B, and C to C

SECTION 2
THEORY OF OPERATION

2.1 GENERAL

This section provides detailed circuit descriptions of the memory functional circuit blocks. Memory circuit card logic diagrams should be referred to during the descriptions; the document numbers are:

Card Type	Logic Diagram
Driver/sink switch (44P0578)	91C0346
Sense/inhibit (44P0506)	91D0285
Memory timing control (44P0599)	91D0363

2.2 TIMING CONTROL CIRCUITS

The timing control circuits are located on card 44P0599 and illustrated on sheet 1 of logic diagram 91D0363. The lower-left portion of sheet 1 illustrates the optional loader protection circuits (refer to section 1.13). Locations of mnemonics and circuit elements on logic diagram 91D0363 are provided in parentheses. For example, (1C8) indicates sheet 1, zone C8.

The input to the delay line (DL1) is designated E0; the delay line output taps are designated E1 through E25. Each output tap provides a 9-nanosecond delay.

2.2.1 Delay Line Timing

Refer to figure V-9 for delay line timing waveforms. When a high MSPX+ pulse (1C8) is received from the CPU, signal IC11-3 goes low (MSCE+ is always high). This negative-going pulse causes the IC14 one-shot to generate a positive pulse. This positive pulse is approximately 140 nanoseconds wide as determined by R6 and C26. The trailing edge of the one-shot pulse sets the delay line input latch (IC17-8 is high) to form the leading edge of the delay line input pulse E0. When this positive transition reaches delay line tap E17, IC11-11 goes low (1C7) causing the delay line input latch circuit to reset (IC17-8 goes low). This determines the width of delay line input pulse E0 (nominally 170 nanoseconds).

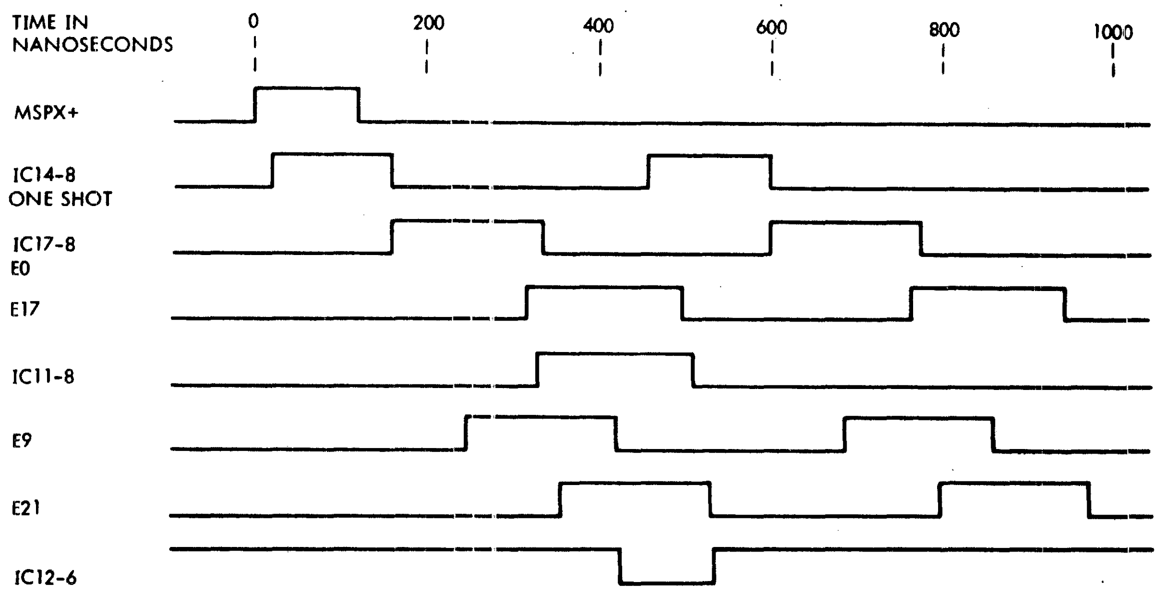

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Figure V-9. Delay Line Timing

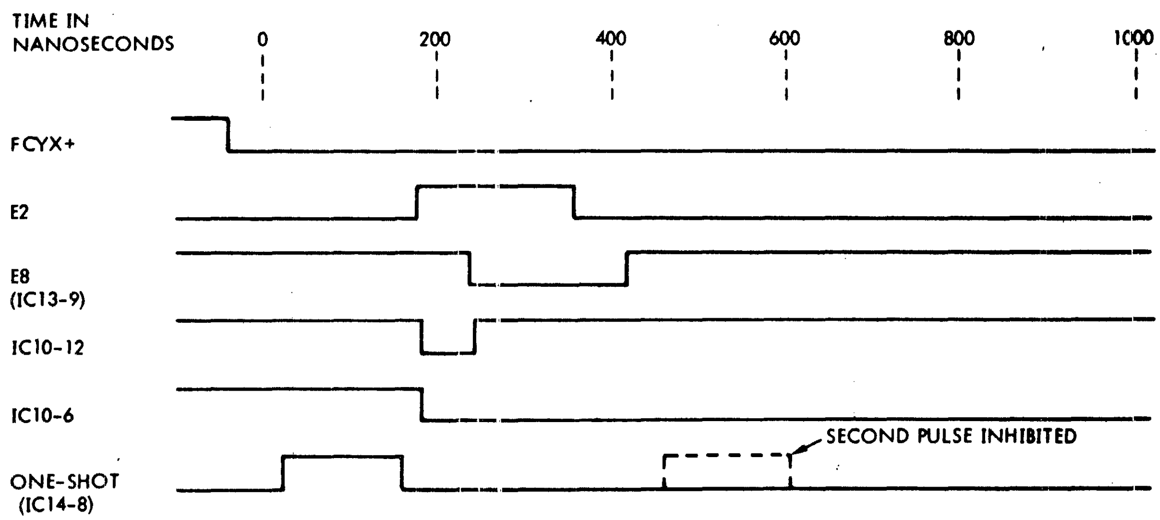

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Figure V-10. Half-Cycle Timing Waveforms

To provide timing for the last half of a full-cycle operation, a second delay line input pulse E0 is generated when delay line pulse E21 is gated with inverted delay line pulse E9 to produce a negative-going pulse at IC12-6 (1C8). This negative-going pulse causes the IC14 one-shot to generate another 140-nanosecond pulse. The trailing edge of the one-shot pulse again sets the delay line input latch to form the leading edge of the second E0 pulse. This second E0 pulse is then formed in the same manner as was the first.

During a half-cycle memory operation, only the delay line pulses for the first half of the memory cycle are generated. Refer to figure V-10 for the half-cycle timing waveforms. The low FCYX+ signal (1C8) is inverted and then gated with the E2 and inverted E8 delay line pulses at IC10-12 (1C6). The resulting negative-going pulse resets the full/half cycle latch causing IC10-6 to go low. This low signal disables the IC12 gate (1C8) which prevents the IC14 one-shot and the delay line from producing a second positive pulse.

2.2.2 Read/Write Timing

Refer to figure V-11 for the read/write timing waveforms. A low TCRX- signal (1C8) produces a high signa. at IC10-6 (1C5). When a high MSPX+ pulse (1C8) is received from the CPU, the signal at IC11-3 goes low (MSCE+ is always high, except during power up and power down) resulting in a low signal at IC10-8 to set flip-flop IC9 (1B4). With this flip-flop set, signal R is high and signal RXXX- is low indicating the read (or clear) portion of the memory cycle.

Flip-flop IC9 is toggled on the trailing edge of delay line pulse E25. This produces high W and RXXX- signals (1B3) indicating the write (or restore) portion of the memory cycle. The trailing edge of the second E25 pulse changes the state of flip-flop IC9 back to the set condition to begin the next memory cycle.

2.3 DRIVER/SINK SWITCH TIMING

The driver/sink switch timing circuits are located on card 44P0578 and illustrated on sheet 9 of logic diagram 91C0346. The timing circuits consist of gates IC1, IC7, and IC12, and the circuits associated with transistors Q7 through Q20. The circuit consisting of transistors Q1 through Q6 is a memory data protection circuit, which disables the timing circuits during power-up and power-down conditions.

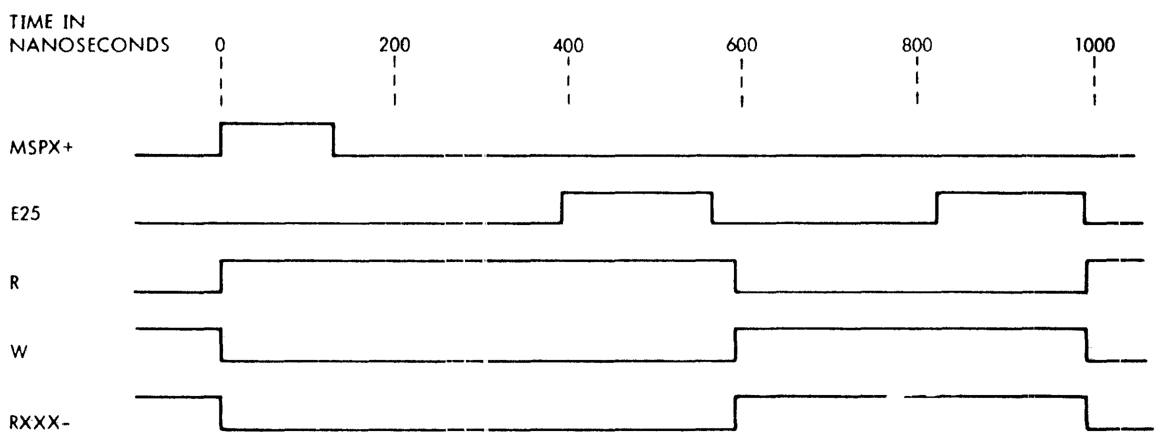

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Figure V-11. Read/Write Waveforms

The input signals are:

a. *SSLX-* Stack select signal, selects a particular 8K memory increment. X represents a number from 1 through 4.

b. *L12X+* Address bit 12, selects the first or second 4K stack of an 8K memory increment. L12X+ low selects the first 4K stack (4K-A); L12X+ high the second 4K stack (4K-B).

c. *RWT1- and RWT2-* Timing signals for the X/Y read and write driver switch circuits.

d. *RSTM-* Timing signal for the X and Y read sink circuits.

e. *WSTX-* Timing signal for the X and Y write sink circuits.

The eight output signals (A, B, C, D, E, F, H, and K) provide drive currents for transformers in the driver and sink switch circuits (sheets 7 and 8 of logic diagram 91C0346). A description of each output signal follows.

a. *Output A* is activated (Q7 conducts) when SSLX-, RWT2-, and L12X+ are low. The A output is routed to a group of eight positive-drive driver switches that are connected to the X and Y lines of a 4K-A stack. During the read portion of the memory cycle, one of these driver switches is selected to route current through a Y line. During the write portion, the same driver switch routes current through an X line.

b. *Output B* is activated (Q8 conducts) when SSLX-, RWT1-, and L12X+ are low. The B output is routed to a group of eight negative-drive driver switches that are connected to the X and Y lines of a 4K-A stack. During the read portion of the memory cycle, one of these driver switches is selected to route current through an X line. During the write portion, the same driver switch routes current through a Y line.

c. *Output C* is activated (Q10 conducts) when SSLX- and RWT2- are low, and L12X+ is high. The C output is routed to a group of eight positive-drive driver switches that are connected to the X and Y lines of a 4K-B stack. During the read portion of the memory cycle, one of these driver switches is selected to route current through a Y line. During the write portion, the same driver switch routes current through an X line.

d. *Output D* is activated (Q11 conducts) when SSLX- and RWT1- are low, and L12X+ is high. The D output is routed to a group of eight negative-drive driver switches that are connected to the X and Y lines of a 4K-B stack. During the read portion of the memory cycle, one of these driver switches is selected to route current through an X line. During the write portion, the same driver switch routes current through a Y line.

e. *Outputs E and F* are activated (Q15 and Q16 conduct) when SSLX- and RSTM- are low.

   The E output is routed to a group of eight sink switches that are connected to the X lines of the 4K-A and 4K-B stacks. During the read portion of the memory cycle, one of these sink switches is selected to route current through a selected X line of the 4K-A or 4K-B stack.

   The F output is routed to a group of eight sink switches that are connected to the Y lines of the 4K-A and 4K-B stacks. During the read portion of the memory cycle, one of these sink switches is selected to route current through a selected Y line of the 4K-A or 4K-B stack.

f. *Outputs H and K* are activated (Q19 and Q20 conduct) when SSLX- and WSTX- are low.

   The H output is routed to a group of eight sink switches that are connected to the X lines of the 4K-A and 4K-B stacks. During the write portion of the memory cycle, one of these sink switches is selected to route current through a selected X line of the 4K-A or 4K-B stack.

   The K output is routed to a group of eight sink switches that are connected to the Y lines of the 4K-A and 4K-B stacks. During the write portion of the memory cycle, one of these sink switches is selected to route current through a selected Y line of the 4K-A or 4K-B stack.

2.4 ADDRESS MULTIPLEXERS AND DECODERS

The address multiplexer and decoder circuits are located on card 44P0578 and illustrated on sheets 7 and 8 of logic diagram 91C0346. The multiplexer consists of the gate circuits IC3, 4, 7, and 8. The decoder circuits are designated IC2, 5, 9, and 11.

Address bits L00X+ through L05X+ are multiplexed with read/write signal RXXX-. During the read sequence of the memory cycle, RXXX- is low; during the write sequence, it is high. The output of the multiplexer consists of the complement of address bits L00X+ through L05X+. During the read sequence, the multiplexer applies the complement of L00X+ through L02X+ to decoder circuit IC9, and the complement of L03X+ through L05X+ to decoder circuit IC5. During the write sequence, the multiplexer applies the complement of L00X+ through L02X+ to decoder circuit IC5, and the complement of L03X+ through L05X+ to decoder circuit IC9. Figures V-12 and V-13 illustrate the multiplexing of address bits representing an octal 45 (100 101). The gates designated with an R are enabled during the read sequence and, the W gates, during the write sequence.

Each decoder circuit consists of a Texas Instruments SN7442N BCD-to-decimal decoder (figure V-14). One of the four inputs (pin 12) is connected to ground. Two of the ten outputs (pins 10 and 11) are not used.

Because the multiplexed codes are in complement form, the outputs of decoder circuits IC5 and IC9 are wired in the reverse order from the outputs of IC2 and IC11. Only one of the eight outputs of each decoder circuit is activated (low level) for a particular 3-bit input code. Figures V-15 and V-16 illustrate read and write decoding for an octal address of 2345. Mnemonics for the active output of each decoder circuit are indicated.

2.5 DRIVER/SINK SWITCHES

The driver/sink switches are located on card 44P0578, and illustrated in block diagram form on sheets 7 and 8 of logic diagram 91C0346. On the logic diagram, the driver switches are represented by the four circuit blocks designated circuit 1 through circuit 4. Descriptions for each of the four circuit blocks are listed below.

a. Circuit 1 consists of eight positive-drive, common-anode driver switches for the 4K-A stack. The positive-drive designation indicates that the collectors of the driver switches are connected to the positive current source. The common-anode designation indicates that the emitter of each driver switch is connected to the anodes of two groups of diodes in the 4K-A stack. One group consists of eight X line diodes; the other, eight Y line diodes. Circuit 1 is enabled when L12X+ and RWT2- are low. During the read sequence, one of these driver

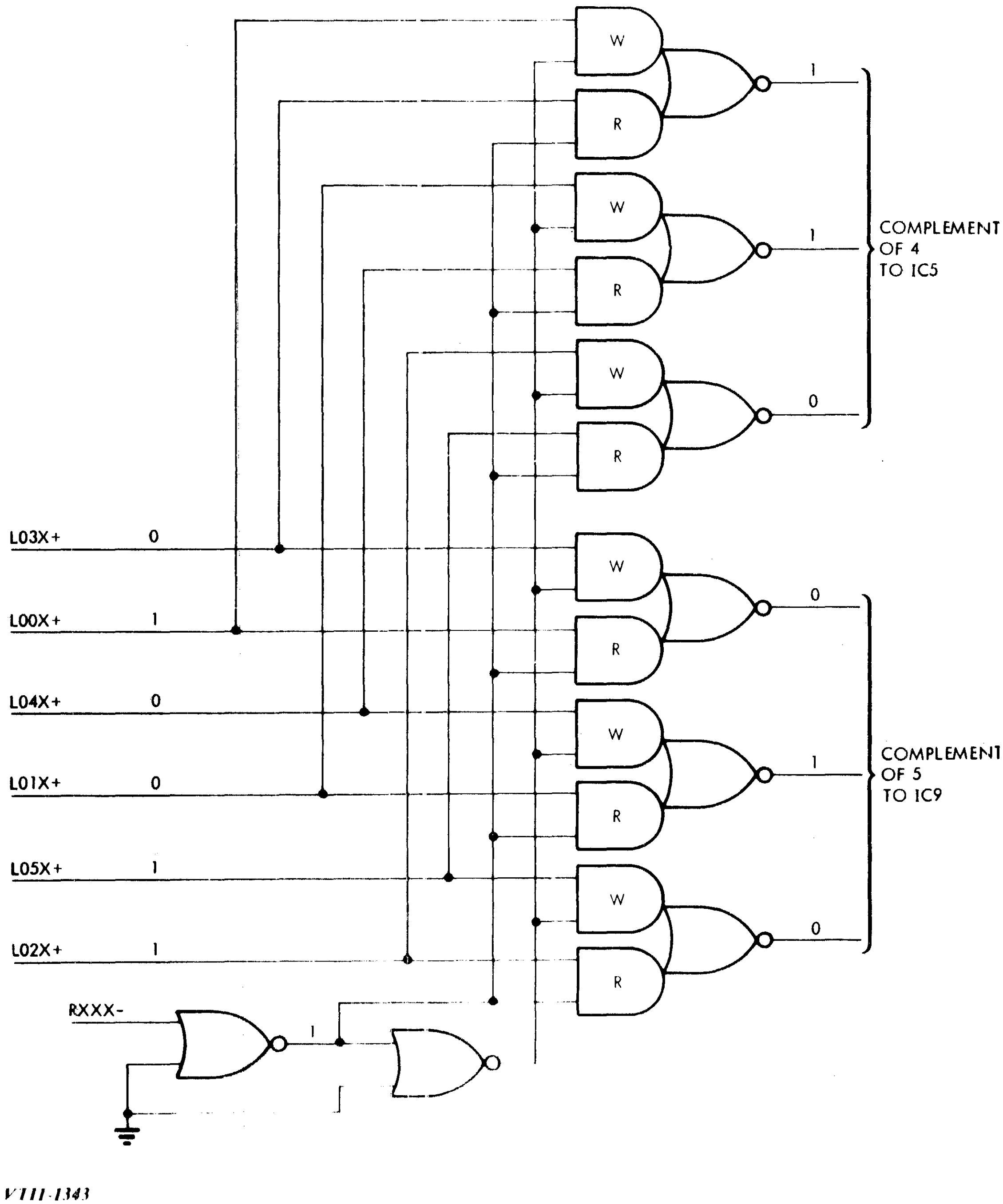
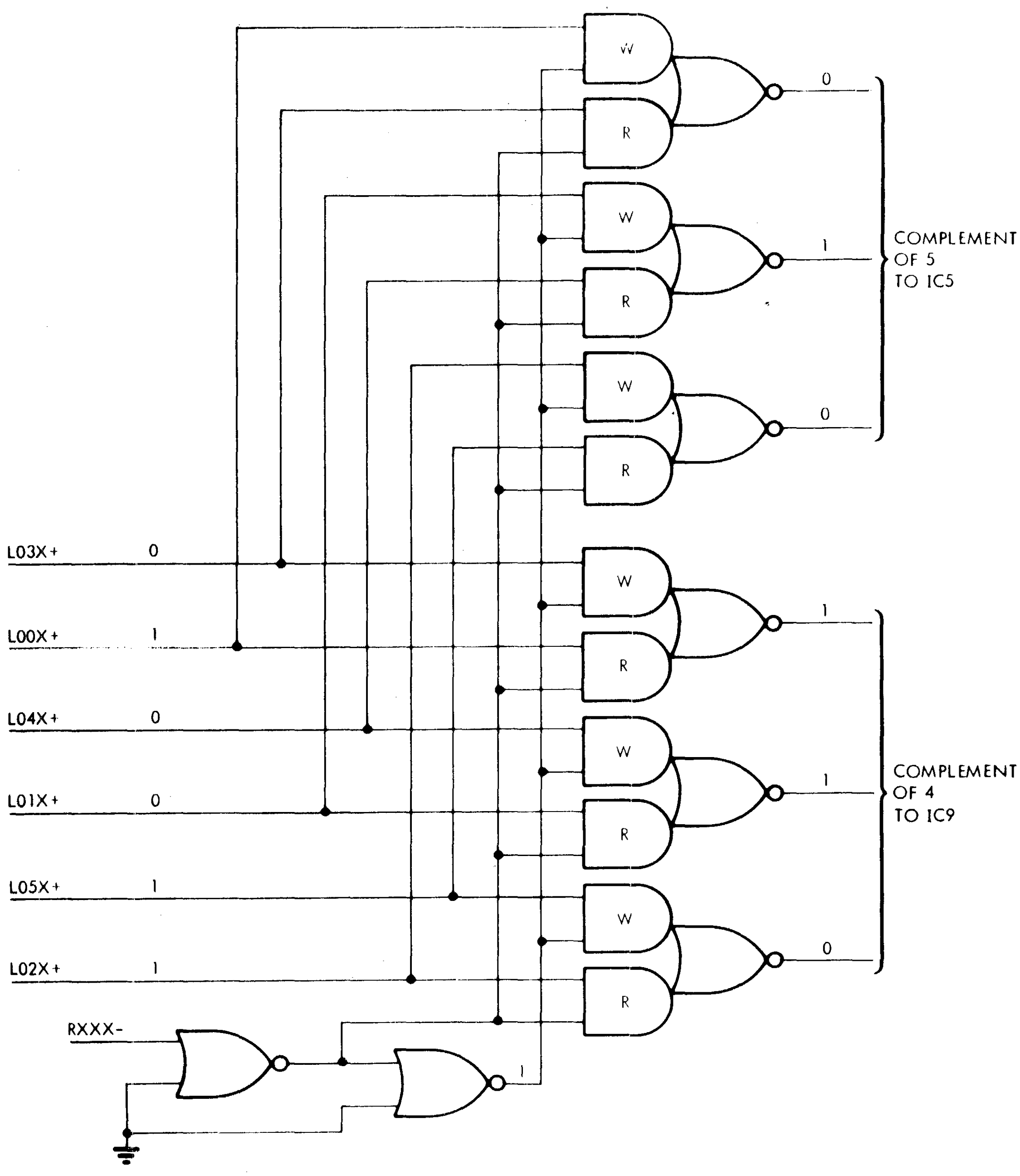
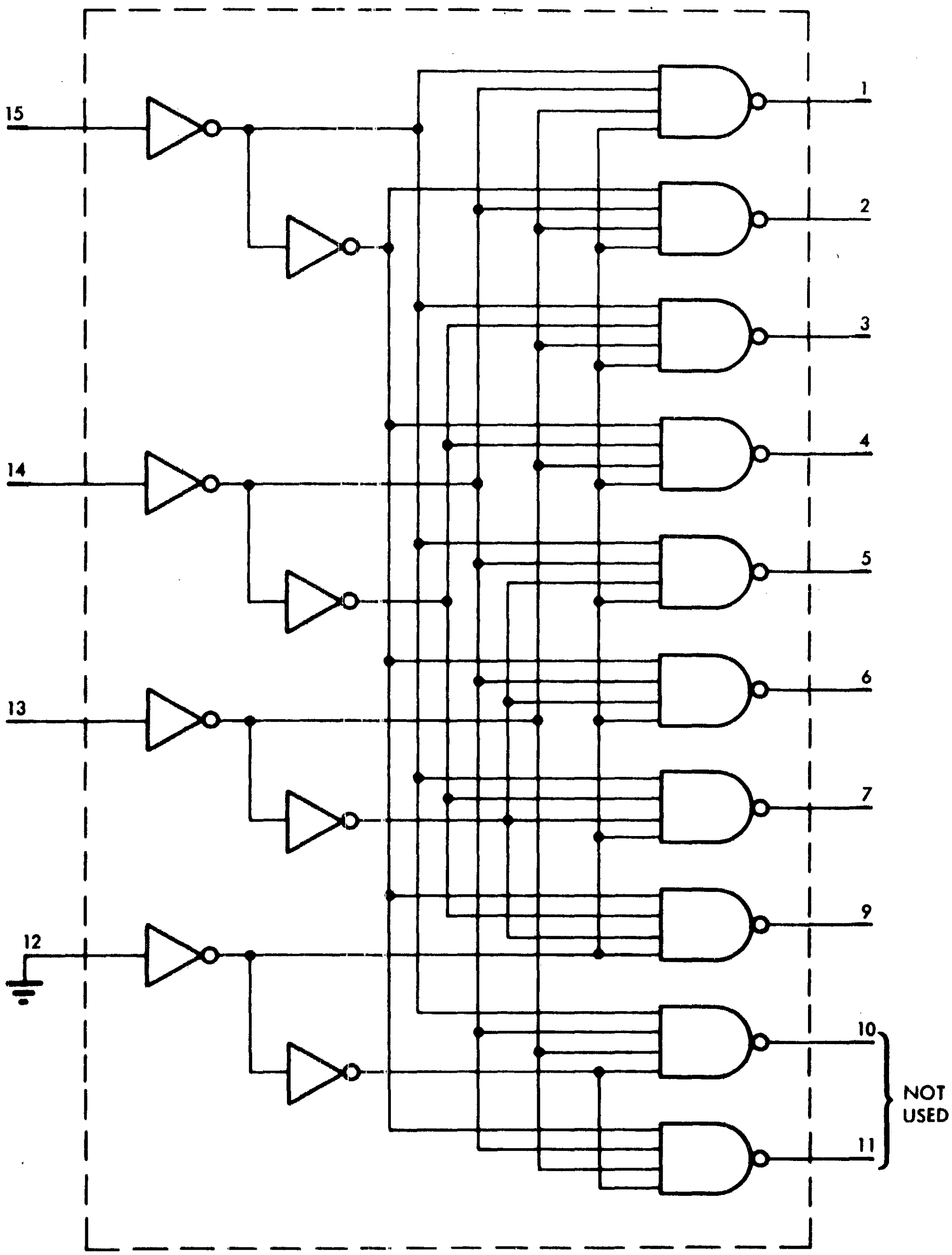


Figure V 12. Read Multiplexing For Octal 45



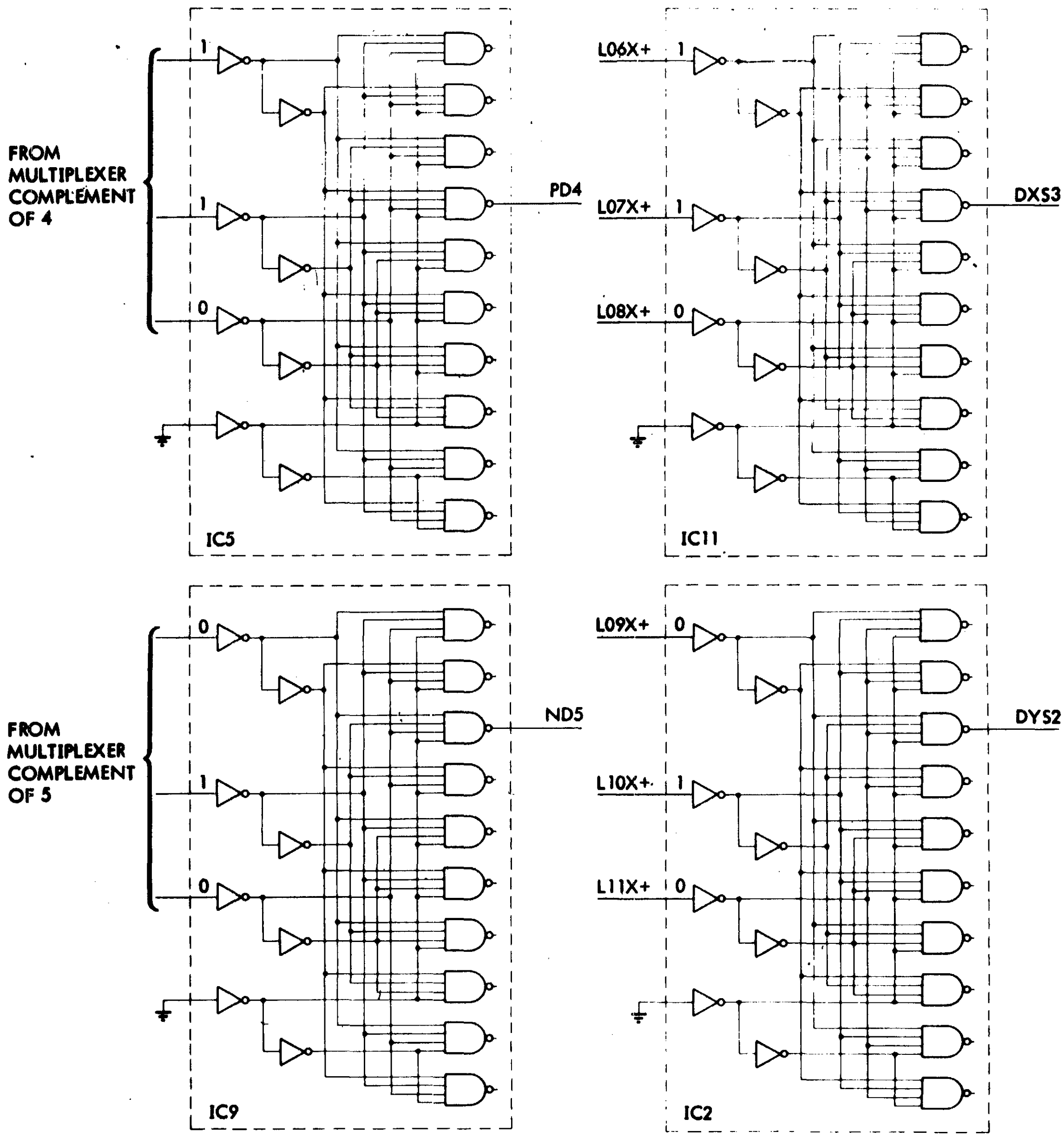
VT11-1344

Figure V-13. Write Multiplexing For Octal 45



VT11-1211

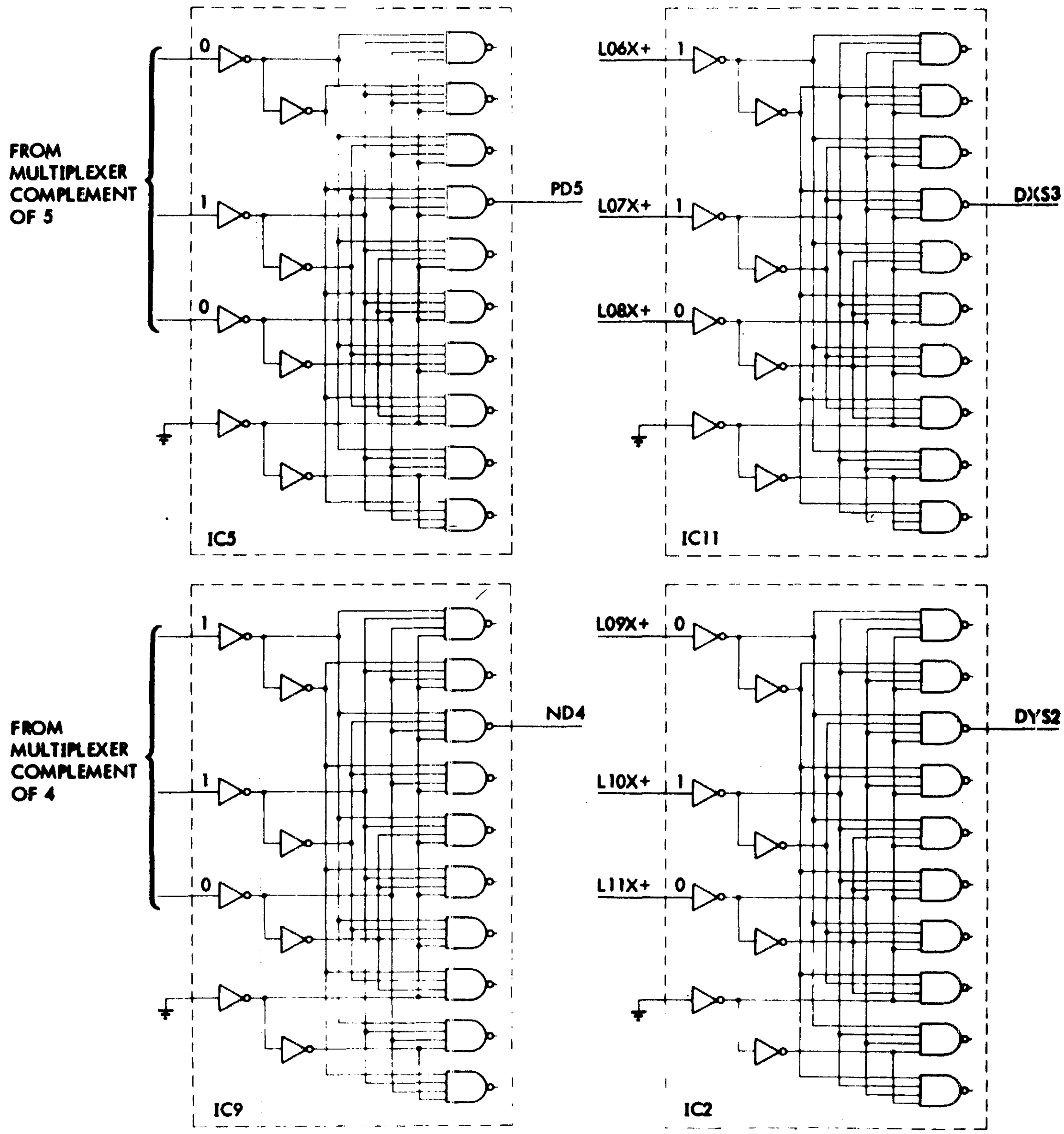
Figure V-14. Decoder Logic Diagram and Pin Assignment



NOTE: THE DESIGNATIONS IC2, IC5, IC9, AND IC11 REFER TO LOGIC DIAGRAM 91C0346

VT11-1345

Figure V-15. Read Decoding of Octal Address 2345



NOTE: THE DESIGNATIONS IC2, IC5, IC9, AND IC11 REFER TO LOGIC DIAGRAM 91C0346

VT11-1346

Figure V-16. Write Decoding of Octal Address 2345

switches is selected to route current through a Y line; during the write sequence, the same driver switch routes current through an X line.

b. Circuit 2 consists of eight positive-drive, common-anode driver switches for the 4K-B stack. The collectors of these driver switches are connected to the same positive current source used by circuit 1. The emitter of each driver switch is connected to the anodes of the two groups of diodes in the 4K-B stack. Circuit 2 is enabled when L12X+ is high and RWT2- is low. During the read and write sequences, the selected circuit 2 driver switch routes current through the X and Y lines in the same manner as the selected driver switch of circuit 1.

c. Circuit 3 consists of eight negative-drive, common-cathode driver switches for the 4K-A stack. The negative-drive designation indicates that the emitters of the driver switches are connected to the negative current source. The common-cathode designation indicates that the collector of each driver switch is connected to the cathodes of two groups of diodes in the 4K-A stack. One group consists of eight X line diodes; the other, eight Y line diodes. Circuit 3 is enabled when L12X+ and RWT1- are low. During the read sequence, one of these driver switches is selected to route current through a selected X line. During the write sequence, the same driver switch routes current through a Y line.

d. Circuit 4 consists of eight negative-drive, common-cathode driver switches for the 4K-B stack. The emitters of these driver switches are connected to the same negative current source used by circuit 3. The collector of each driver switch is connected to the cathodes of the two groups of diodes in the 4K-B stack. Circuit 4 is enabled when L12X+ is high and RWT1- is low. During the read and write sequences, the selected circuit 4 driver switch routes current through the X and Y lines in the same manner as the selected driver switch of circuit 3.

On the logic diagram, the sink switches are represented by the four circuit blocks designated circuits 5 through 8. Descriptions for each of the four circuit blocks are listed below.

a. Circuit 6 consists of eight X write sink switches for the 4K-A or 4K-B stacks. The emitters of these sink switches are connected to -12 volts. Circuit 6 is enabled when WSTX- is low to allow the selected sink switch to route write current through an X line of the 4K-A or 4K-B stack.

b. Circuit 8 consists of eight X read sink switches for the 4K-A or 4K-B stacks. The collectors of these sink switches are connected to +12 volts. Circuit 8 is enabled when RSTM- is low to allow the selected sink switch to route read current through an X line of the 4K-A or 4K-B stack.

c. Circuit 5 consists of eight Y read sink switches for the 4K-A or 4K-B stacks. The emitters of these sink switches are connected to -12 volts. Circuit 5 is enabled when RSTM- is low to allow the selected sink switch to route read current through a Y line of the 4K-A or 4K-B stack.

d. Circuit 7 consists of eight Y write sink switches for the 4K-A or 4K-B stacks. The collectors of these sink switches are connected to +12 volts. Circuit 7 is enabled when WSTX- is low to allow the selected sink switches to route write current through a Y line of the 4K-A or 4K-B stack.

Address bits 0 through 12 are decoded in four groups of three bits each. L00X+ through L02X+ select one of eight X read/X write driver switch pairs, L03X+ through L05X+ slect one of eight Y read/Y write driver switch pairs, L06X+ through L08X+ select one of eight X read/X write sink switch pairs, and L09X+ through L11X+ select one of eight Y read/Y write sink switch pairs. Through the diode-decoding matrix on the memory stack card, the eight pairs of XY driver switches and eight pairs of X sink switches select one of 64 X drive lines. The same eight pairs of XY driver switches and 8 pairs of Y sink switches select one of 64 Y drive lines. The word at the intersection of the X and Y drive lines is addressed.

2.5.1 Driver Switch Circuits

Detailed schematics of the driver switch circuits appear on sheets 3 and 4 of logic diagram 91C0346.

The circuits designated 1 and 2 have input signals consisting of:

a. Transformer drive current from the driver/sink switch timing circuits (outputs A or C) that is applied to one end of the transformer primaries via pin 17.

b. Decoded signals PD0 through PD7 that are applied to the other ends of the transformer primaries via pins 1 through 8.

One of the eight driver switches is activated when the transformer drive current is present at pin 17, and one of the decoded signals goes low. This allows current to flow in the transformer turning on the associated transistor. With the transistor on, the positive current source (pin 18) is routed through the Y line during a read sequence and the X line during a write sequence. Circuit 1 is used for the 4K-A stack and circuit 2 for the 4K-B stack.

The circuits designated 3 and 4 have input signals consisting of:

a. Transformer drive current from the driver/sink switch timing circuits (outputs B or D) that is applied to one end of the transformer primaries via pin 17.

b. Decoded signals ND0 through ND7 that are applied to the other ends of the transformer primaries via pins 1 through 8.

One of the eight driver switches is activated in the same manner as for circuits 1 and 2. When a transistor in circuit 3 or 4 turns on, the negative current source (pin 18) is routed through the X line during a read sequence and the Y line during a write sequence. Circuit 3 is used for the 4K-A stack and circuit 4 for the 4K-B stack.

2.5.2 Sink Switch Circuits

Detailed schematics of the sink switch circuits appear on sheets 5 and 6 of logic diagram 91C0346. Like the driver switches, the input signals of the sink switches consists of transformer drive currents (at pin 17) and decoded signals (at pins 1 through 8). A particular sink switch is activated in the same manner as the driver switches. When a transistor in circuit 5 turns on, a path is provided to sink the read current of a Y line in the 4K-A or 4K-B stack. When a transistor in circuit 6 turns on, a path is provided to sink the write current of an X line in the 4K-A or 4K-B stack. When a transistor in circuit 7 turns on, a path is provided to sink the write current of a Y line in the 4K-A or 4K-B stack. When a transistor in circuit 8 turns on, a path is provided to sink the read current of an X line in the 4K-A or 4K-B stack.

2.6 CURRENT SOURCE CIRCUITS

The current source circuits are located on card 44P0578 and illustrated on sheet 10 of logic diagram 91C0346. The circuits consist of positive and negative current source networks and associated temperature-compensating circuits.

The positive current source network consists of resistors R37, R40, R42, and transistor Q23. A nominal current source of 380 mA is produced at point L and is routed to the positive-drive driver switches. Transistors Q21 and Q22, zener diode CR7, thermistor RT1, resistors R36, R41, and potentiometer R39 form a temperature compensating network which causes the driver current to vary inversely with temperature.

Except for the direction of current flow, the negative current source circuit operates in the same manner as the positive current source circuit. A nominal negative 380 mA current is produced at point M and is routed to the negative-drive driver switches.

Using potentiometers R39 and R47, the positive and negative drive currents are adjusted at the factory for optimum memory operation.

2.7 SENSE/INHIBIT TIMING

The sense/inhibit timing circuit is located on card 44P0506. It is illustrated at the upper left of sheet 1, logic diagram 91D0285.

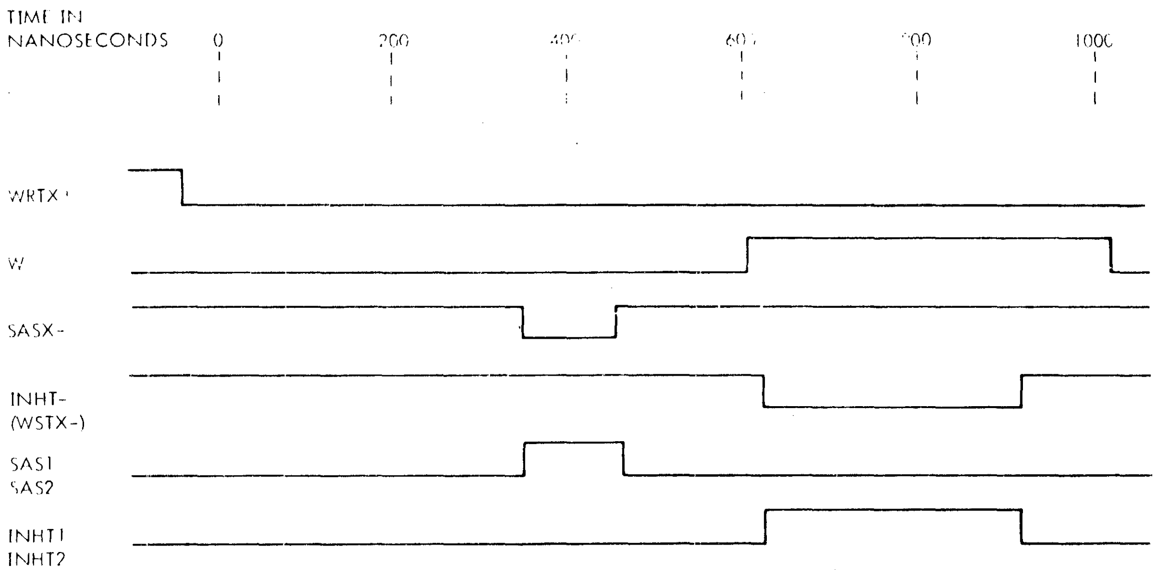
The circuit is enabled when its associated 4K memory stack is selected. The mnemonic SSLX- represents one of four stack select signals (SSL1- through SSL4-) that select a particular 8K memory increment. These signals originate on the DM112 card where they are designated MSC1+ through MSC4+. The mnemonic INHE-X represents one of two inhibit enable signals (INHE-0 and INHE-1) that select the 4K-A or 4K-B stack of the selected 8K increment.

The Sense Amplifier Strobe (SASX-) signal from the memory timing control card is used to produce the SAS1 and SAS2 signals. SAS1 strobes the outputs of the sense amplifiers for data bits 0 through 7; SAS2 strobes the outputs of the sense amplifiers for data bits 8 through 15.

The Inhibit Timing (INHT-) signal originates from the memory timing control card where it is designated WSTX-. INHT- is used to produce the INHT1 and INHT2 signals. INHT1 is a timing pulse for the inhibit drivers of data bits 0 through 7; INHT2 is a timing pulse for the inhibit drivers of data bits 8 through 15. Refer to figure V-17 for sense/inhibit timing waveforms.

2.8 SENSE/INHIBIT DATA LOOP OPERATION

The schematics and block diagrams for the sense amplifiers and inhibit drivers appear on sheets 2 and 3 of logic diagram 91D0285. The sense amplifiers and their associated networks are designated as circuits 1, 2, 4, 5, 7, 8, 10, and 11; the inhibit drivers as circuits 3, 6, 9, and 12. Sections 2.8.1 and 2.8.2 provide circuit descriptions of the sense/inhibit data loop for bit 15 (refer to figure V-5 in section 1.8).



V111-1390

Figure V-17. Sense/Inhibit Timing Waveforms

2.8.1 Read/Restore Operation

During a read/restore operation, the sense amplifier of circuit 11 senses the state of the bit 15 core by comparing the voltage on the sense lines (S15X and S15X-) with the predetermined threshold voltage. The threshold voltage originates from the +5-volt supply and potentiometer R3 (sheet 1 of 91D0285). R3 is adjusted at the factory for a reference voltage of 3.1 volts (at pin 3 of R3). The reference voltage is applied to pin 1 of the sense amplifier resistor network where it is divided to become the threshold voltage at pin 5 (approximately 20 millivolts). The output of the sense amplifier is strobed by the sense amplifier strobe signal SAS2 and buffered by an open-collector gate (IC11) to provide a wire-OR capability.

When the bit 15 core is one, the sense amplifier generates a narrow positive pulse at pin 7 of circuit 11. This produces a low signal at IC11-8 which sets the bit 15 flip-flop of the memory data register (card 44P0592) to a low state (one state). The low signal at IC11-8 also produces a low signal at IC12-12 which prevents the bit 15 inhibit driver from turning on. Thus, during the restore sequence, the write currents on the X and Y lines restore the core to the original one state.

When the bit 15 core is zero, the sense amplifier output at pin 7 of circuit 11 is low. This causes the signal at IC11-8 to remain at a high level, indicating that bit 15 is zero. During the restore sequence, the high signal at IC11-8 is gated with a high INHT2 signal to produce a positive pulse at IC12-12. This turns on the bit 15 inhibit pre-driver which enables the bit 15 inhibit driver to produce an inhibit current at pin 9 of circuit 12 (D15X). The inhibit current prevents the write currents on the X and Y lines from switching the bit 15 core to a one state.

2.8.2 Clear/Write Operation

During the clear/write operation, a high WRTX+ signal from card 44P0593 is sent to the memory timing control card (44P0599). This prevents the memory timing control circuits from generating the sense amplifier strobe signal SASX-. This disables the sense amplifier, and results in a low signal at pin 7 of circuit 11 and a high signal at IC11-8 (W15X- is zero) during the clear sequence.

During the write sequence, the state of W15X- is determined by the state of the bit 15 flip-flop in the memory data register (card 44P0592). If bit 15 is to be a one (W15X- low), a low signal is produced at IC12-12 to prevent the bit 15 inhibit driver from turning on. Thus no inhibit current is generated, and the bit 15 core is set to a one state. If bit 15 is to be a zero (W15X- high), a high signal is produced at IC12-12 to turn on the bit 15 inhibit driver. The inhibit current at pin 9 of circuit 12 (D15X) prevents the write currents on the X and Y lines from switching the bit 15 core to a one state.

SECTION 3
MAINTENANCE

3.1 GENERAL

This section provides preventive and corrective maintenance information for the 620/L memory system. Refer to the maintenance section of chapter IV for recommended test equipment and troubleshooting information.

3.2 PREVENTIVE MAINTENANCE

Preventive maintenance for the memory consists of inspection, cleaning, adjustments, and running the memory test program as described below.

a. Check memory circuit card connectors for proper seating.

b. Remove dust and dirt from the memory interior by applying a stream of low-velocity air. Use extreme care when cleaning in the area of the core stacks.

c. Check and adjust the power supply voltages using a voltmeter accurate to within 2 percent. The voltages can be measured at the driver/sink switch card backplane connector (slot 3 of mainframe) as follows:

   -5V at pin 115
   +5V at pin 116
   -12V at pin 113
   +12V at pin 119

d. Adjust potentiometer R3 on the sense/inhibit card for a 3.1-volt reference voltage at pin 3 of R3 (TPI).

e. Run the 620 memory test program (part number 92A0107-004). Refer to the 620 Test Programs Manual (98 A 9952 060) for operating instructions.

3.3 CORRECTIVE MAINTENANCE

A malfunction can be isolated to a particular 4K memory increment by running the memory test program. Fault isolation to a specific circuit card can then be accomplished by replacing cards of the malfunctioning memory increment with corresponding cards from a memory increment that operates correctly. Only one driver/sink switch card is required for an 8K memory increment. If this card is faulty, the memory test program can detect errors in two 4K memory increments. When the faulty memory card is found, it can be installed on an extender card 44P0540 to make it available for troubleshooting. Figure V-18 illustrates typical waveforms to be observed at test points on the memory timing control card. Figures V-19 through V-21 show photographed waveforms observed on cards 44P0599, 44P0506, and 44P0578.

CAUTION

Never remove or install any circuit card or remove or connect any connector while power is applied to the memory.

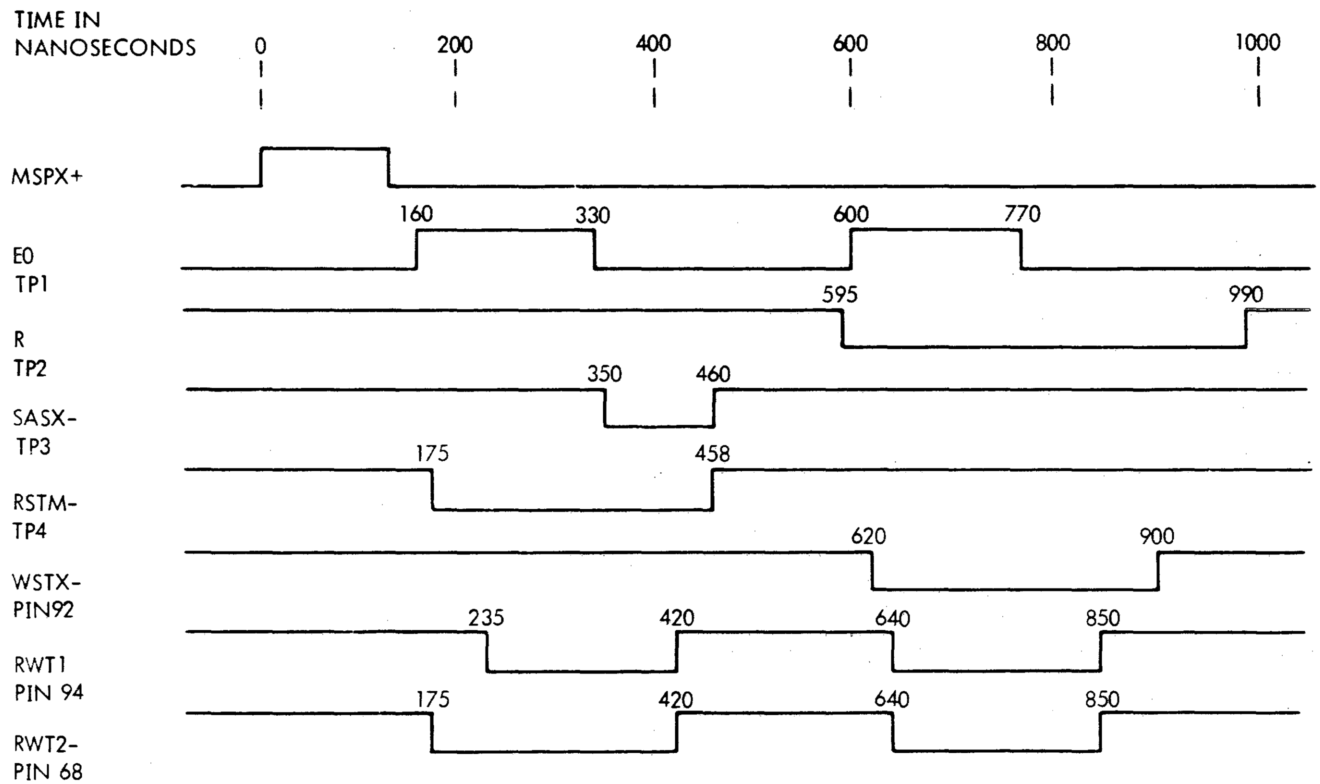
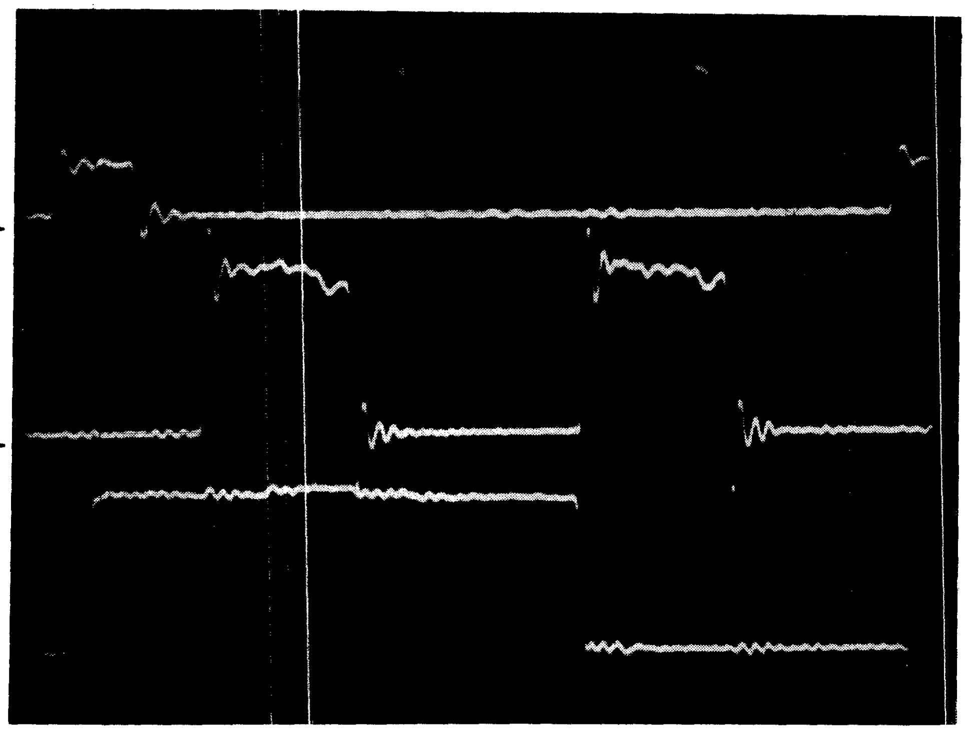


Figure V-18. Test Point Waveforms on Timing and Control Card



NOTE:

1. FOR THE ABOVE WAVEFORMS, THE OSCILLOSCOPE SWEEP TIME IS SET TO 100 NANOSECONDS/CM

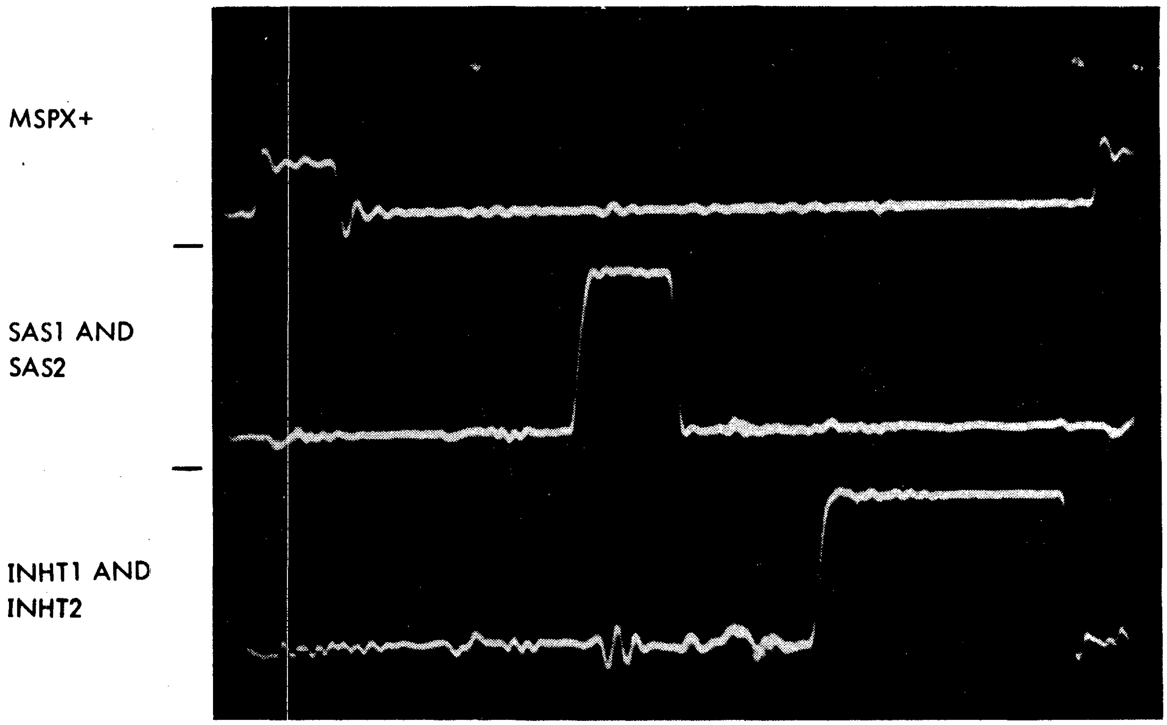
2. MSPX+ IS THE MEMORY START PULSE AT PIN 90 ON CARD 44P0599 (MAINFRAME SLOT 6). THE OSCILLOSCOPE IS SET TO 5 VOLTS/CM

3. E0 IS THE INPUT PULSE TO THE DELAY LINE AT TP1 ON CARD 44P0599. THE OSCILLOSCOPE IS SET TO 2 VOLTS/CM

4. R IS ONE OUTPUT OF THE READ/WRITE FLIP-FLOP AT TP2 ON CARD 44P0599. THE OSCILLOSCOPE IS SET TO 2 VOLTS/CM

VIII-1392

Figure V-19. Memory Timing Control Card Waveforms

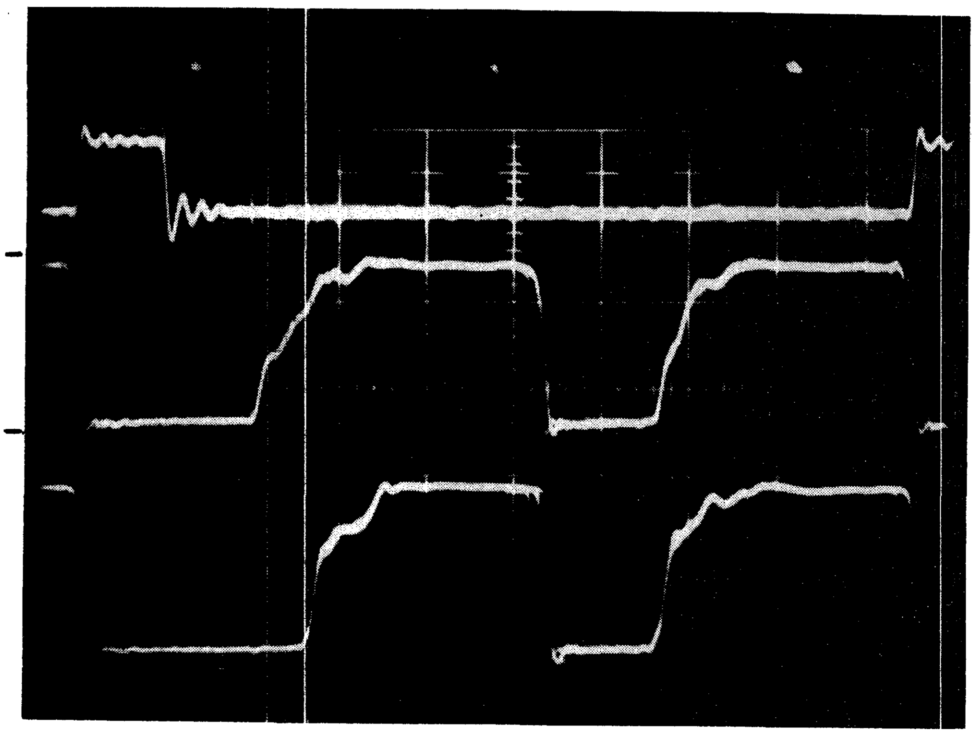


NOTES:

1. FOR THE ABOVE WAVEFORMS, THE OSCILLOSCOPE SWEEP TIME IS SET TO 100 NANOSECONDS/CM
2. MSPX+ IS THE MEMORY START PULSE AT PIN 90 ON CARD 44P0599 (MAINFRAME SLOT 6). THE OSCILLOSCOPE IS SET TO 5 VOLTS/CM
3. SAS1 IS THE SENSE AMPLIFIER STROBE PULSE AT TP8 ON CARDS 44P0506 (MAINFRAME SLOTS 2 AND 5). THE OSCILLOSCOPE IS SET TO 2 VOLTS/CM
4. INHT1 AND INHT2 ARE THE INHIBIT TIMING SIGNALS AT TP7 AND TP2 ON CARDS 44P0506 (MAINFRAME SLOTS 2 AND 5). THE OSCILLOSCOPE IS SET TO 2 VOLTS/CM

VT11-1393

Figure V-20. Sense/Inhibit Card Waveforms



NOTES:

1. FOR THE ABOVE WAVEFORMS, THE OSILLOSCOPE SWEEP TIME IS SET TO 100 NANOSECONDS/CM

2. MSPX+ IS THE MEMORY START PULSE AT PIN 90 ON CARD 44P0599 (MAINFRAME SLOT 6). THE OSCILLOSCOPE IS SET TO 5 VOLTS/CM

3. THE CURRENT SOURCE PULSES ARE THE POSITIVE AND NEGATIVE CURRENT SOURCES ON THE CARD 44P0578. THE SIGNALS ARE CURRENT PULSES FLOWING THROUGH THE WIRES CONNECTED TO POINTS L AND M ON SHEET 10 OF LOGIC DIAGRAM 91C0346. THE OSCILLOSCOPE IS SET TO 200 MILLIAMPERES/CM

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Figure V-21. Driver/Sink Switch Card Waveforms

CHAPTER VI

DIRECT MEMORY ACCESS AND INTERRUPT

SECTION 1 FUNCTIONAL DESCRIPTION

1.1 GENERAL

The direct memory access and interrupt circuits (DMA/I), contained on the circuit card 44P0023, allow I/O data transfers to occur under external control.

The direct memory access circuits (DMA), when used with the optional BIC, allow peripheral devices on the I/O bus to transfer data to or from computer memory while temporarily halting the processing of the stored program. The program remains halted for 1.66 microseconds or 1-3/4 computer cycles. The cycle-stealing procedure does not disturb the contents of the operation registers (A, B, X, and P); thus, the program can proceed normally at the conclusion of the data transfer. This process is referred to in this manual as trapping. To preclude excessive preemption of the computer time from the stored program, one program instruction is performed between each successive trap. Data can be transferred between the computer memory and devices with this method at rates up to 382,720 words per second.

The interrupt circuits allow certain computer options (PF/R, RTC, PIM, and BIC), on a priority basis, to request the computer to execute an instruction independent of the program in progress. When two or more interrupt requests are received simultaneously, the hard-wired system priority scheme determines which option has priority. During the interrupt, the computer is directed to a memory address specified by the interrupting option and, then, executes the instruction stored in that location. Execution of any instruction stored in memory, except an I/O command, can be requested. Normally, the instruction is a jump and mark (JMPM) command, which results in the processing of an I/O subroutine.

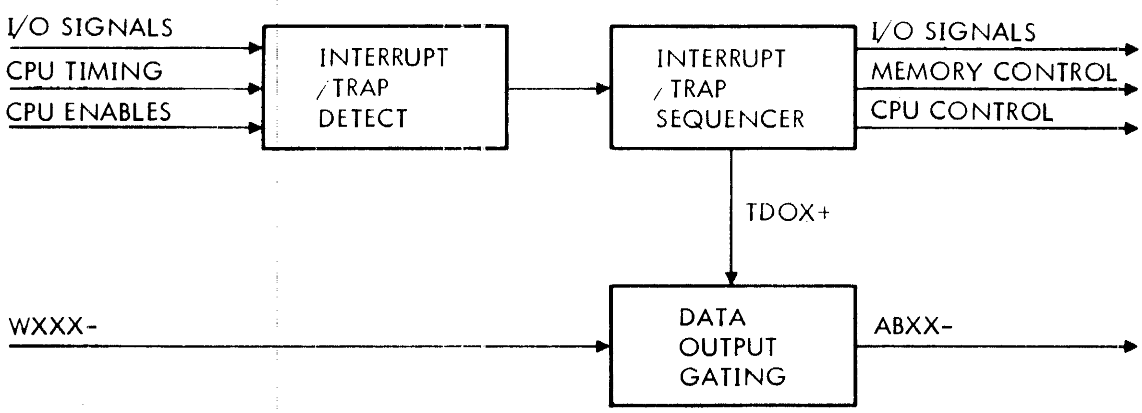
The DMA/I consists of an interrupt/trap detect, interrupt/trap sequencer, and data output gating sections as illustrated in figure VI-1. The interrupt/trap detect section detects the presence of a trap or interrupt request, provides proper detect timing, and inhibits detection of traps or interrupts under certain conditions. The interrupt/trap sequencer section controls critical CPU functions in the proper sequence to perform an interrupt, trap-in, or trap-out. The data output gating section controls the transfer of data during trap-out.

1.2 TRAPS

Traps from selected devices can be used to input a word of data directly to a selected memory address (trap-in) or to read out a word from the computer memory (trap-out); this delays the stored program for 1.66 microseconds. Data transferred in this manner does not disturb the contents of the operation registers, thus enabling the program to proceed normally at the conclusion of the transfer. Only one word of data can be transferred during each trap, and a minimum of 1.0 microsecond is required for the main program between trap sequences. Thus, the maximum data transfer rate is one word each 2.61 microseconds, or 382,720 words per seconds.

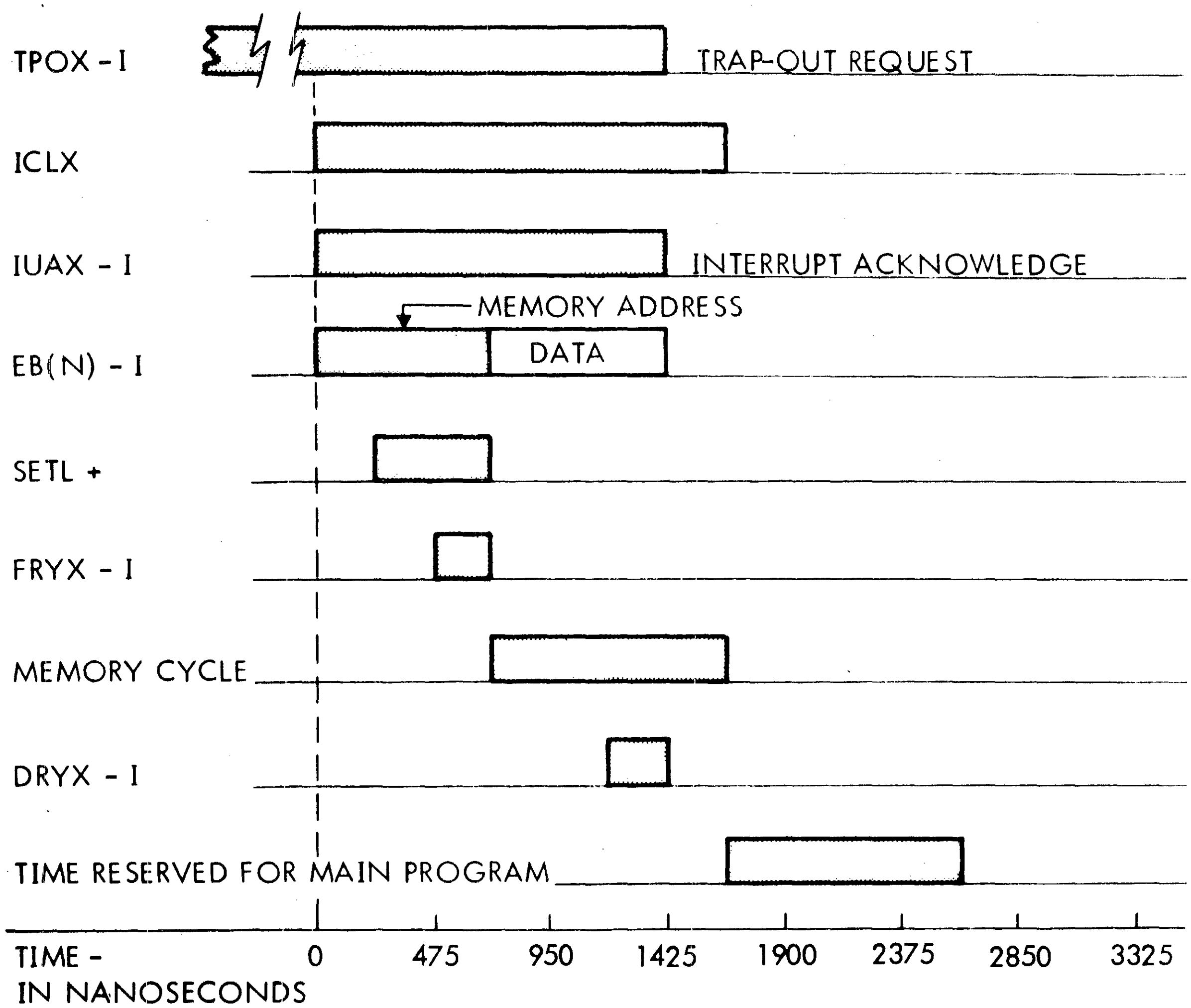
When a trap request from a device is received by the DMA, it is detected unless a specific inhibit signal is present. Figure VI-2 shows the general timing sequence used in detecting and processing a trap-out request.

When a Trap-Out Request (TPOX-I) is detected, the first sequence flip-flop (ICLX) is set. This sets the interrupt acknowledge flip-flop, placing signal IUAX-I on the I/O bus to notify the requesting device that its request has been acknowledged. The peripheral device then places the desired memory address on the E bus, from which it is gated by the computer into the L (memory address) register, via the C bus. A Function Ready (FRYX-I) signal is



VT11-0106

Figure VI-1. DMA/I Functional Block Diagram



VT11-1395

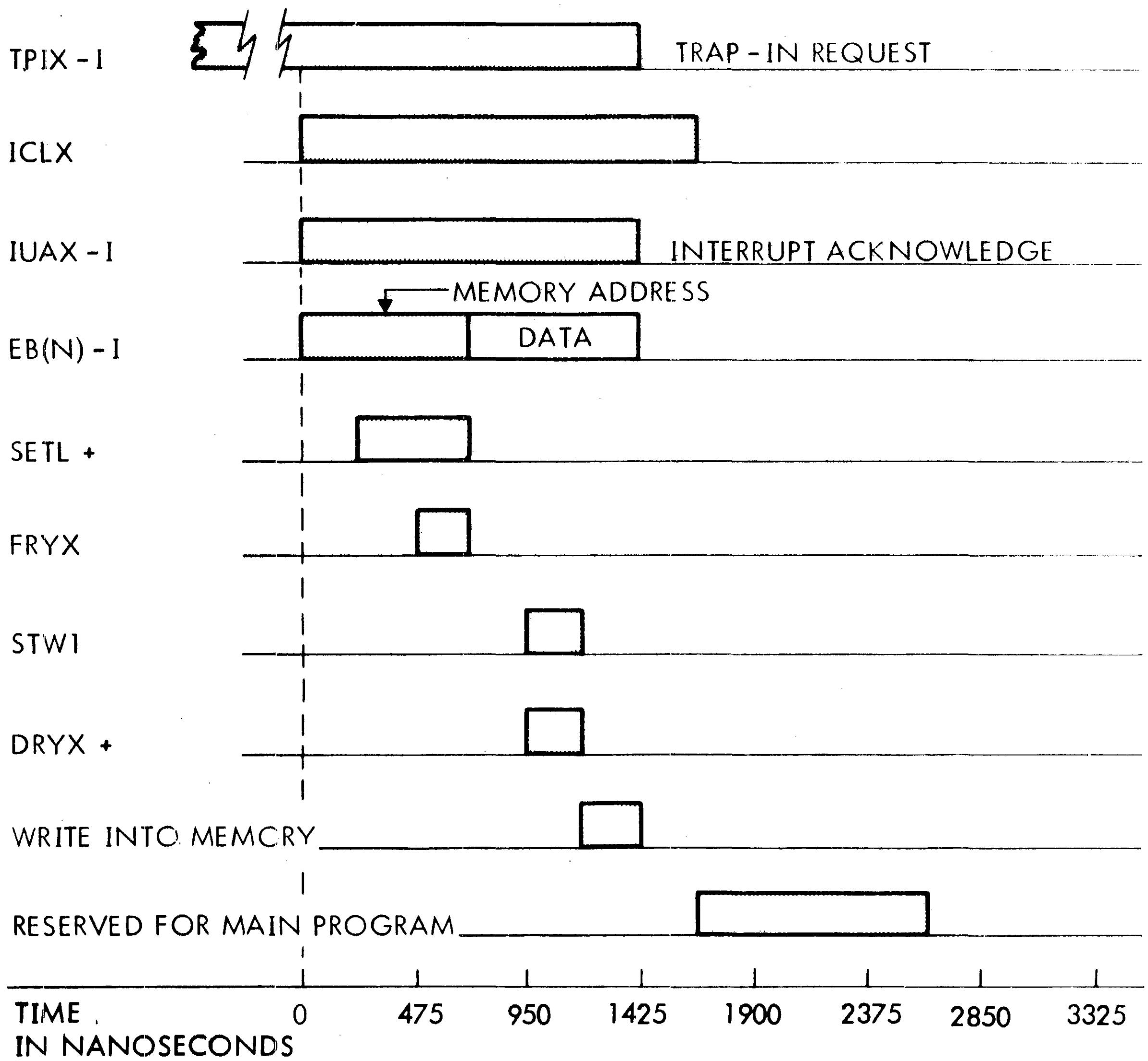
Figure VI-2. Trap-Out Timing Sequence

then placed on the E bus by the computer. The requesting device removes the memory address from the E bus on the trailing edge of FRYX-I. A memory cycle is initiated, bringing the desired data from memory into the W register, from which it is gated onto the E bus, via the A and C buses. A Data Ready (DRYX-I) signal then gates the data from the E bus into the data register of the requesting device, after which TPOX-I and IUAX-I are removed from the E bus, flip-flop ICLX is reset, and the trap sequence is ended.

Figure VI-3 shows the timing sequence for processing a trap-in request. When a Trap-In Request (TPIX-I) is detected, flip-flop ICLX is set, and IUAX-I is generated, acknowledging the request. The device then places the desired memory address on the E bus, from which it is gated by the computer into the L register, via the C bus. The device then removes the address from the E bus on the trailing edge of FRYX-I. The W register is cleared to receive the input data. The device places the data on the E bus, where it is gated onto the C bus. The data are then gated into the W register by DRYX- for storage in the memory address specified by the trap address in the L register. The signals on the I/O bus are then removed and flip-flop ICLX is reset, ending the trap-in sequence.

1.3 INTERRUPTS

Figure VI-4 shows timing sequences for detecting and processing interrupts. When an Interrupt Request (IURX-I) signal from an option is received, it is detected unless a specific inhibit signal is present. Detection of the interrupt request sets flip-flop ICLX +. This immediately sets the Interrupt Acknowledge (IUAX-I) flip-flop, notifying the interrupting device that its interrupt has been acknowledged. The device then places a memory address on the E bus, from which it is gated by the computer into the L register, via the C bus. A memory start clock signal is then initiated, bringing the contents of the memory address (the interrupt instruction) into the W register. During the first half of the memory cycle, the instruction that was interrupted is executed by the CPU. During the second half of the memory cycle, the interrupt instruction is transferred from the W register to the U register and examined to determine whether it is a one-word or two-word instruction. One-word instructions are executed at the completion of the memory cycle. If a two-word instruction is indicated, the memory address from the E bus is strobed onto the C bus, where it is incremented and placed in the L register. A new memory cycle is then initiated, bringing the second word to the U register. If the interrupt instruction is a JMPM, an Interrupt Jump (IUJX-I) signal is generated, inhibiting the interrupt request capability of the controllers until reenabled by the program.



VT11-1396

Figure VI-3. Trap-In Timing Sequence

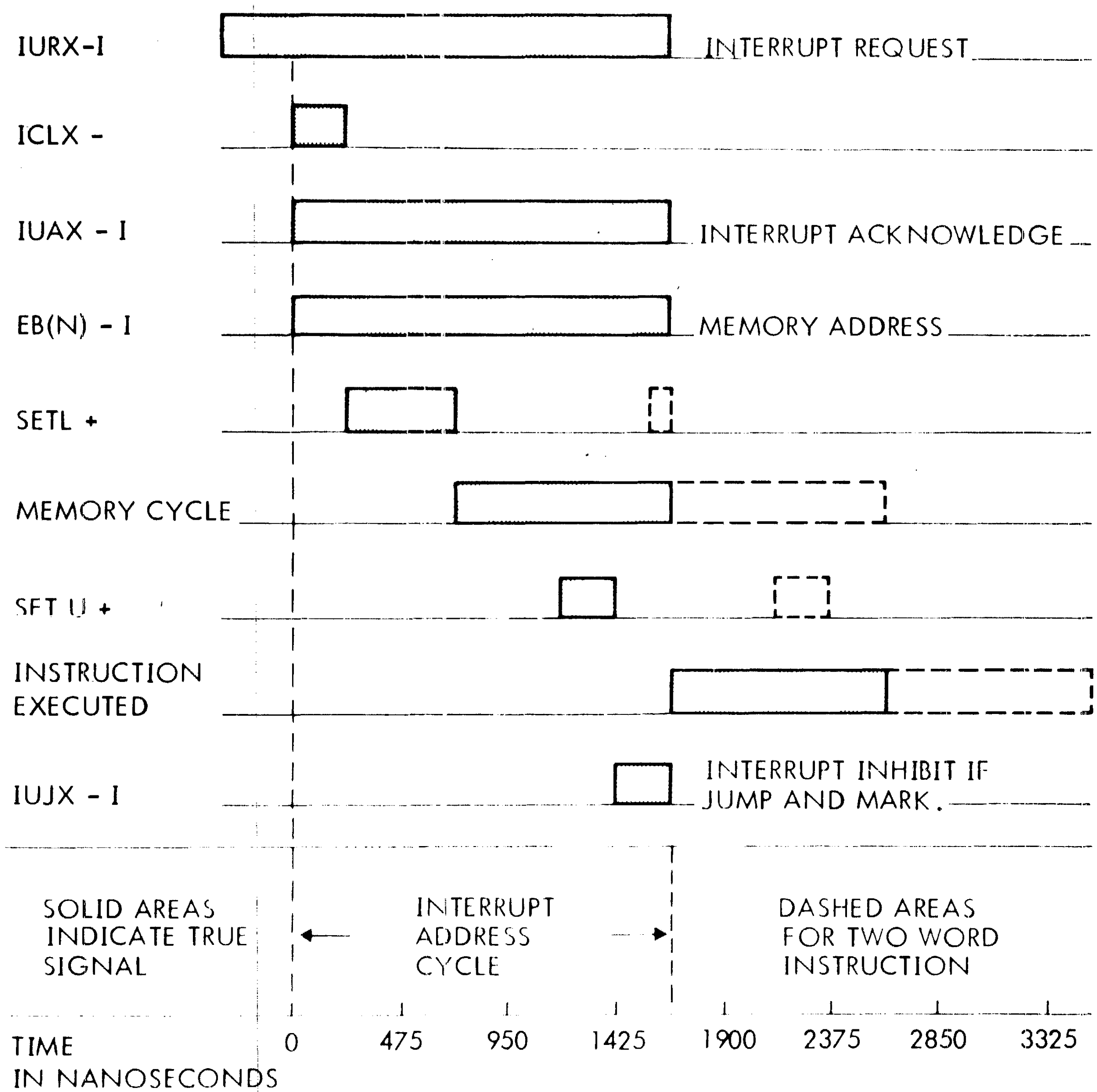


Figure VI-4 Interrupt Timing Sequence

1.4 DATA OUTPUT GATINGS

The data output gating section in the DMA provides sequence control signals for data being transferred from memory to an interrupting device (trap-out). The signal flow path is shown in figure VI-5.

The data word is transferred to the W register at the beginning of the memory cycle. TDOX+, a sequence signal generated by the DMA, gates the data word onto the A bus, and from there automatically to the C bus. It is then gated onto the E bus for transfer to the requesting device by EBDX+. This signal is generated in the CPU as a result of EBD1- from the DMA.

1.5 UNINTERRUPTABLE SEQUENCES

Certain restrictions regarding the use of traps or interrupts by devices must be considered by the programmer when preparing program routines involving traps or interrupts. This section describes the conditions under which interrupt and trap requests are not recognized.

If two or more trap or interrupt requests occur on the same trailing edge of the interrupt

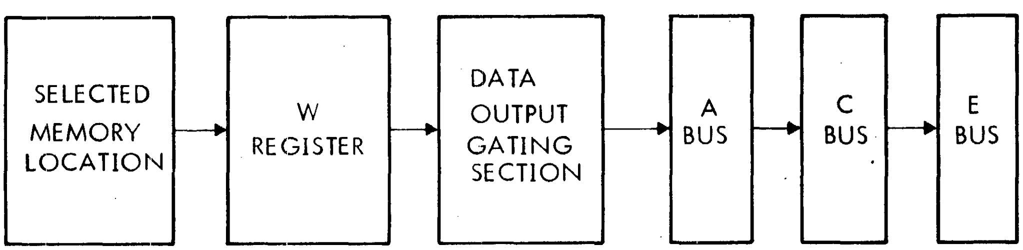


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Figure VI-5. Trap-Out Data Path

clock (IUCX-I), the system priority scheme determines which interrupting device has the highest priority and allows only that interrupt or trap request to remain.

Interrupt or trap requests can be raised by an external device only on the trailing edge of IUCX-I. When a trap or interrupt request has been recognized, IUCX-I is held true for the remainder of the trap or interrupt operation. Thus, it is impossible for a trap or interrupt request to occur while a current trap or interrupt is in process.

1.5.1 Interrupt Requests

When program loops contain only uninterruptable instructions, interrupts cannot occur. Thus, when recognition of an interrupt is imperative (such as with the PF/R), at least one No Operation (NOP) instruction must be added to such loops. Two NOP instructions are required after two or more external control (EXC) instructions.

The conditions under which interrupt requests are not recognized are listed below, with the significant inhibiting term in each case given in parentheses.

a. During the operand cycle of an Increment Memory and Replace (INR) instruction (FEIX +).

b. At the beginning of a Halt (HLT) instruction (FEIX +).

c. During addressing cycles (including indirect addressing) that occur during jump, jump and mark, execute, or sense instruction when the jump condition is met (JCMX-).

d. During any I/O instruction (K3XX-).

e. Until at least one interruptable instruction has occurred after an EXC instruction (FRCX-).

f. During any shift instruction [(K2XX + • AC4X +) negated].

g. During a shift that is a part of a multiply or divide operation (SHC3-).

h. For one cycle immediately following a shift operation during which a trap occurred (TOSX-).

i. During a manual step (SOPX-).

j. In step mode, i.e., when halted (ROHX-).

k. When a manual or programmed halt is in process (HTCX-).

l. Until run mode has been fully entered (STRX-).

m. At times other than during the timing window consisting of phase clock false and fetch instruction true (PHCX-, FEIX+).

1.5.2 Trap Requests

The following are the conditions under which trap requests are not recognized, with the significant inhibiting term in each case given in parentheses at the end of each statement.

a. During the data transfer portion of any I/O instruction (FRCX-).

b. During the operand access portion of an INR instruction (IMCX-).

c. During a manual step (SOPX-).

d. When halted (EPHX+).

e. At times other than during the timing window consisting of phase clock true and execute phase true (PHCX+, EPHX+).

SECTION 2
INTERFACE DATA

2.1 GENERAL

This section describes I/O interface, trap and interrupt sequences, and CPU interface signals.

2.2 I/O INTERFACE

The DMA/I interfaces with the devices via the I/O bus using the standard E bus lines (EBXX) plus the following control lines: IUAX-I, IURX-I, TPOX-I, TPIX-I, IUCX-I, and IUJX-I. The lines are logically true at 0V and logically false at +3V. A total of ten receivers or drivers can be connected to each control line.

2.2.1 Interrupt Acknowledge (IUAX-I)

This control signal is set true by the CPU to acknowledge the receipt of an interrupt, a trap-in, or a trap-out. The interrupting or trapping device can transfer an address to the computer and receive data from or send data to the computer only when this control signal is true. IUAX-I also inhibits device address decoding in every device during the address phase of an interrupt or DMA operation. This prevents the device from interpreting the lower-order bits of a memory address as a device address.

2.2.2 Interrupt Request (IURX-I)

By setting IURX-I true, the interrupting device requests the CPU to execute an instruction. The address of this instruction is placed on the E bus by the interrupting device upon receipt of IUAX-I from the computer.

2.2.3 Trap-out Request (TPOX-I)

By setting TPOX-I true, the trapping device requests the CPU to transfer one word of data from memory. The address of this word is placed on the E bus by the controller upon receipt of IUAX-I from the computer.

2.2.4 Trap-In Request (TPIX-I)

By setting TPIX-I true, the trapping device requests the CPU to transfer one word of data to memory. The address of this word is placed on the E bus by the device upon receipt of IUAX-I from the computer.

2.2.5 Interrupt Clock (IUCX-I)

This control signal is a 0.58-MHz clock from the CPU and is disabled by IUAX-I. When IUAX-I is false, the clock is present on the IUCX-I line. When IUAX-I is true, IUCX-I is held true. The true-to-false transition of IUCX-I sets the request flip-flops (IURX-I, TPOX-I, and TPIX-I) in the respective device.

2.2.6 Interrupt Jump (IUJX-I)

This control signal from the CPU inhibits interrupts from PIMs that occur after a jump and mark instruction when that instruction is the result of an interrupt request. This signal becomes true 1.425 microseconds from the false-to-true transition of IUAX-I and remains true for 237.5 nanoseconds (the PIM stays inhibited and is re-enabled under program control).

2.3 TRAP-OUT AND TRAP-IN SEQUENCES

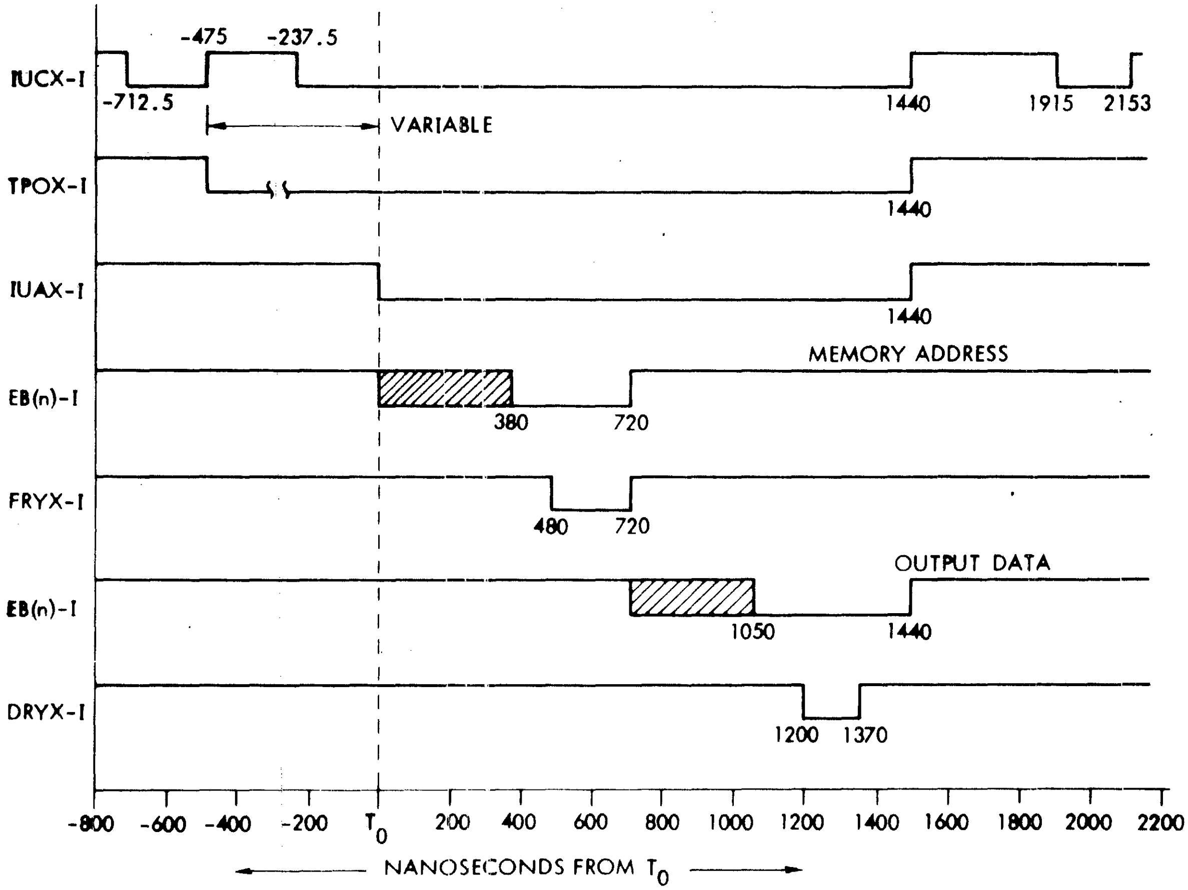
A controller communicating with the DMA must generate or respond to the following signals: IUAX-I, TPOX-I, TPIX-I, IUCX-I, FRYX-I, DRYX-I, and EBNX-I, plus Priority-In (PRMX-I) and Priority-Out (PRNX-I) signals. The trap-out and trap-in sequences contain three phases: request, address, and data. Refer to figures VI-6 and VI-7 during the description.

2.3.1 Request Phase

The requesting device having the highest priority generates a cycle-stealing request (sets TPOX-I or TPIX-I true) on the trailing edge of IUCX-I and waits for IUAX-I from the computer.

2.3.2 Address Phase

IUAX-I is received by the requesting device, thereby holding IUCX-I true. The device then places the memory address, into or from which data are to be read, on the E bus and waits for the trailing edge of FRYX-I.



T_0 is the start of the output sequence.

Logic levels: true 0V dc,
false +3V dc.

time when signal is settling.

TPOX-I is normally off at T_{1440}; it must be off by T_{1600}.

EB(n)-I (memory address) is normally on at T_0; it must be on by T_{380}. It is normally off at T_{720}; it must be off by T_{920}.

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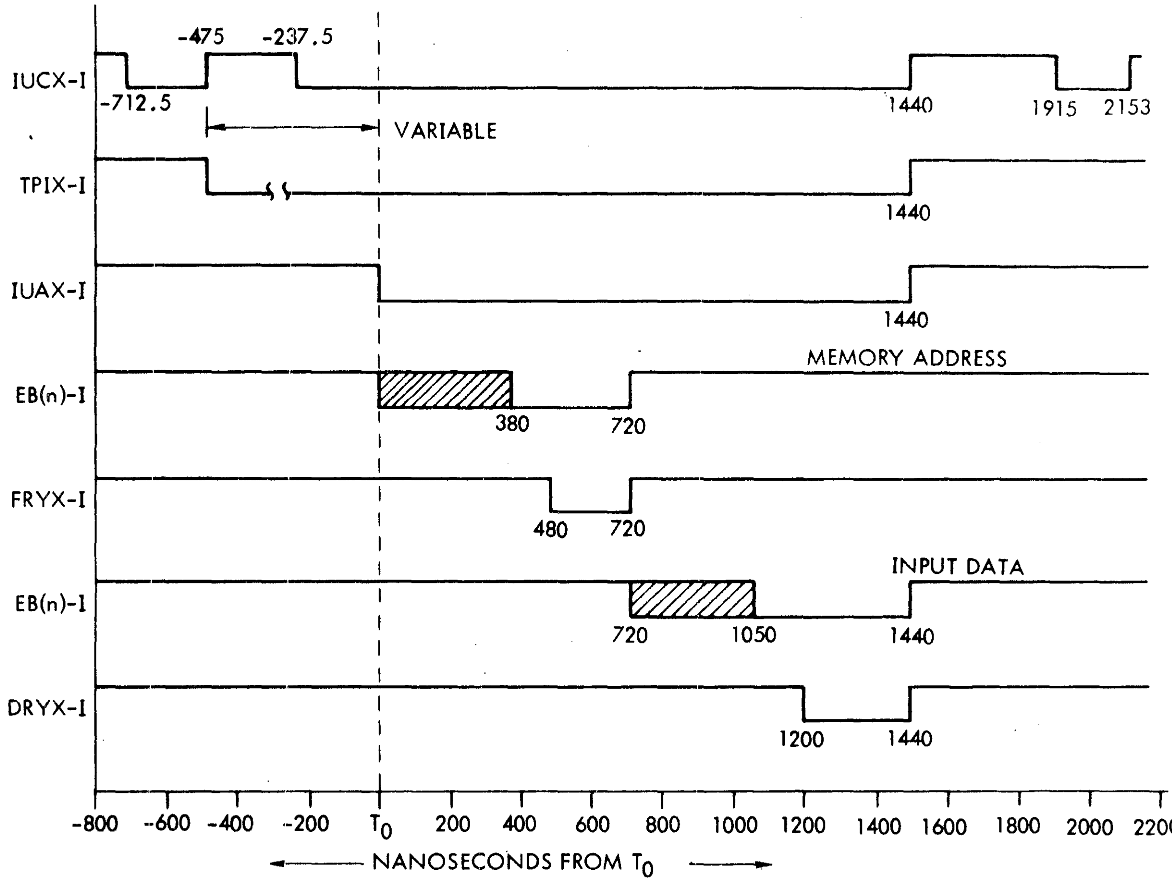
Figure VI-6. Trap-Out Timing



T_0 is the start of the input sequence.

Logic levels: true = 0V dc,
false = +3V dc.

TPIX-I is normally off at T_{1440}; it must be off by T_{1600}.

EB(n)-I (memory address) is normally on at T_0; it must be on by T_{380}. It is normally off at T_{720}; it must be off by T_{920}.

EB(n)-I (input data) is normally on at T_{720}; it must be on by T_{1000}. It is normally off at T_{1440}; it must be off by T_{1600}.

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Figure VI-7. Trap-In Timing

2.3.3 Data Phase

At the trailing edge of FRYX-I, the device removes the address from the E bus. Data are then placed on the E bus by either the computer or the requesting device. These data are gated into the device or into the computer at the trailing edge of DRYX-I. All signals are removed from the bus when IUAX-I goes false.

2.4 INTERRUPT SEQUENCES

A controller communicating with the interrupt circuits must generate or respond to the following signals: IUAX-I, IUCX-I, IURX-I, EBNX-I, PRMX-I, and PRNX-I. The interrupt sequence contains two phases: request and address. Refer to figure VI-8 during the description.

2.4.1 Request Phase

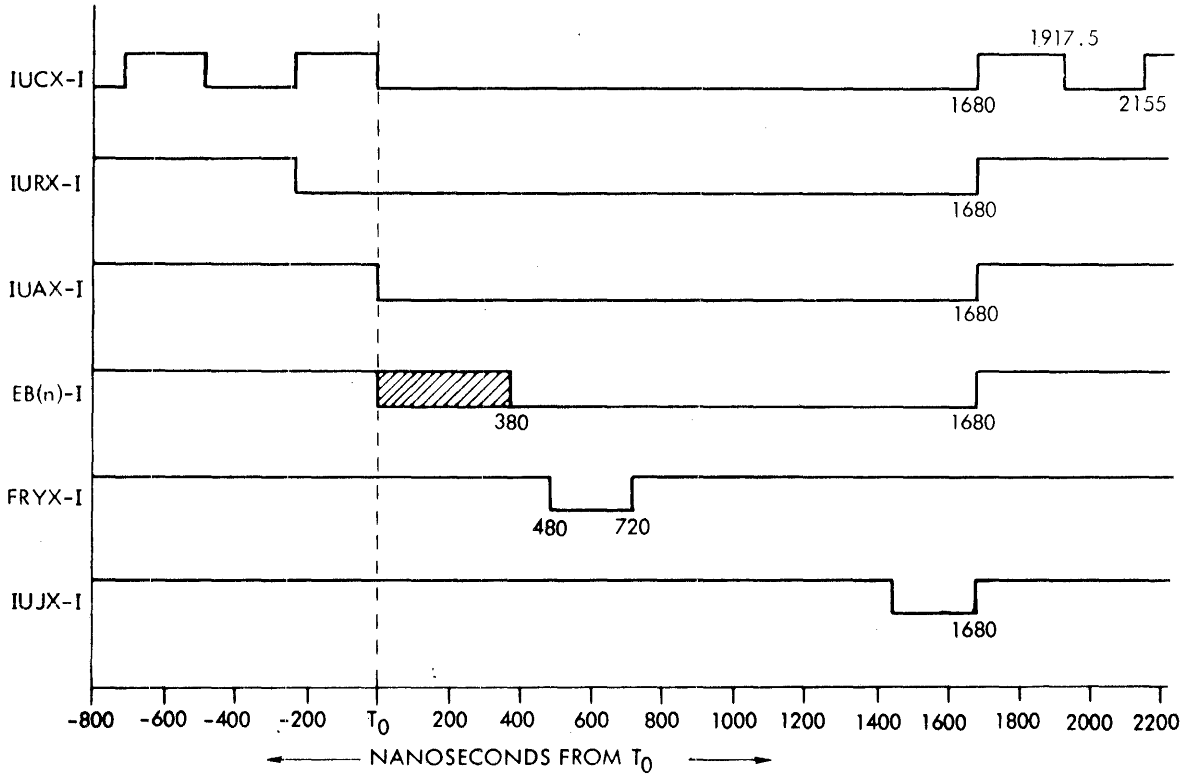
The requesting option having the highest priority generates an interrupt request (sets IURX-I true) on the trailing edge of IUCX-I. The option then waits for IUAX-I from the computer.

2.4.2 Address Phase

When the CPU recognizes the request, it sets IUAX-I true, thus holding IUCX-I true. Upon receipt of IUAX-I from the computer, the requesting option places the address containing the instruction to be executed on the E bus. The instruction at this address can be any except an I/O instruction. In the case of a two-word instruction, the CPU ORs a one into bit 0 of the second word, making this address an odd number. The address placed on the E bus by the requesting option must be an even number. If the instruction is JMPM, the device receives IUJX-I from the computer. IUJX-I resets the master enable in every option capable of making a request (except the RTC), thereby inhibiting further interrupts from these options during the subsequent subroutine. The address phase ends when IUAX-I becomes false. All signals are removed from the bus at this time.

2.5 CPU INTERFACE SIGNALS

Signals from the CPU to the DMA/I are described in table VI-1. Signals from the DMA/I to the CPU are listed in table VI-2.



T_0 is the start of the input sequence.

Logic levels: true = 0V dc,
false = +3V dc.

IURX-I is normally off at T_{1680}; it must be off by T_{1800}.

EB(n)-I is normally on at T_0; it must be on by T_{380}. It is normally off at T_{1680}; it must be off by T_{1800}.

IUJX-I is present for a jump and mark instruction.

Figure VI-8. Interrupt Timing

Table VI-1. DMA Signals from the CPU

Signal	Description
AC0X +	Address code 0
AC2X +	Address code 2
AC4X +	Address code 4
CL1X +	Clock 1
DRYX +	Data Ready
EJIX-	Execute jump instruction
EPHX-	Execute phase instruction
FEIX +	Fetch instruction
FRCX-	Function ready control
FRYX +	Function ready
HTCX-	Halt control
IAPX +	Instruction cycle address phase
IMCX-	Increment memory
JCMX-	Jump condition met
K1XX +	Class code 1
K2XX +	Class code 2
K3XX +	Class code 3 (any I/O instruction)
MCLX +	Master clock
PHCX-	Phase clock
ROHX +	Reset on halt
SHC3-	Shift control enable
SHFX-	Shift
SOPX-	Stop
SYRT +	System reset
WXXX-	W register bits 00 through 17

Table VI-2. DMA Signals to the CPU

Signal	Description
ABXX-	A bus bits 00 through 17
CW1X-	Clear W register
EBD1-	E bus drive
EBR1-	E bus receive
EMRX+, EMRX-	E and M bus receive
FCYX-	Full cycle
ICLX-	Inhibit clock
IIAX-	Increment interrupt address
IUAX+, IUAX-	Interrupt acknowledge
IUCX+	Interrupt clock
IUJX+	Interrupt jump
MDN2+	Multiply/divide negative
PHC3-	Phase clock inhibit
SW1X-	Set W register
TAIX-	Trap address in
TDIW-	Trap data in write
TOSX-	Trap on shift
TRSC-	Trap start clock

SECTION 3
THEORY OF OPERATION

3.1 GENERAL

The theory of operation for the DMA-I is divided into three functional elements: interrupt/trap detection, interrupt trap sequencer, and data output gating. The DMA/I logic diagram 91D0362 should be referred to during the description. Throughout the description, logic diagram locations of the mnemonics are given in parentheses. For example, TPRX- (1C1) means that TPRX- appears on sheet 1 in zone C1 of the logic diagram. The DMA/I mnemonics are described at the end of this section.

3.2 INTERRUPT/TRAP DETECTION

When IURX-I (1C4) is received on the I/O bus, it is inverted to form IURX+, which enables the interrupt detection logic. An interrupt will then be detected at the first Master Clock (MCLX+) (1C3) when Phase Clock Minus (PHCX-) (2D8) and Fetch Instruction Cycle (FEIX+) (1D5) are both true, provided no inhibiting condition exists. When detection occurs, the first sequencer flip-flop (ICLX) (1C3) is set.

When TPOX-I or TPIX-I (1C2) is received on the I/O bus, it produces TPOX+ or TPIX+, which enables the trap detection logic. A trap will then be detected at the first MCLX+ when PHCX+ (2D7) and Execute Phase (EPHX+) (1C5) are both true, provided no inhibiting condition exists. When detection occurs, flip-flop ICLX is set.

3.3 INTERRUPT/TRAP SEQUENCER

The interrupt/trap sequencer functions consist of three sections: interrupt, trap out, and trap in.

3.3.1 Interrupt

The description of the interrupt function of the interrupt/trap sequencer is presented in terms of MCLX+ periods. Refer to figures VI-9 and VI-10 for the interrupt flow diagram and the interrupt timing diagram, both of which reference the appropriate MCLX+ periods.

During clock period 1, both FEIX+ and PHCX- are true, IURX+ is true, and no interrupt inhibits are present.

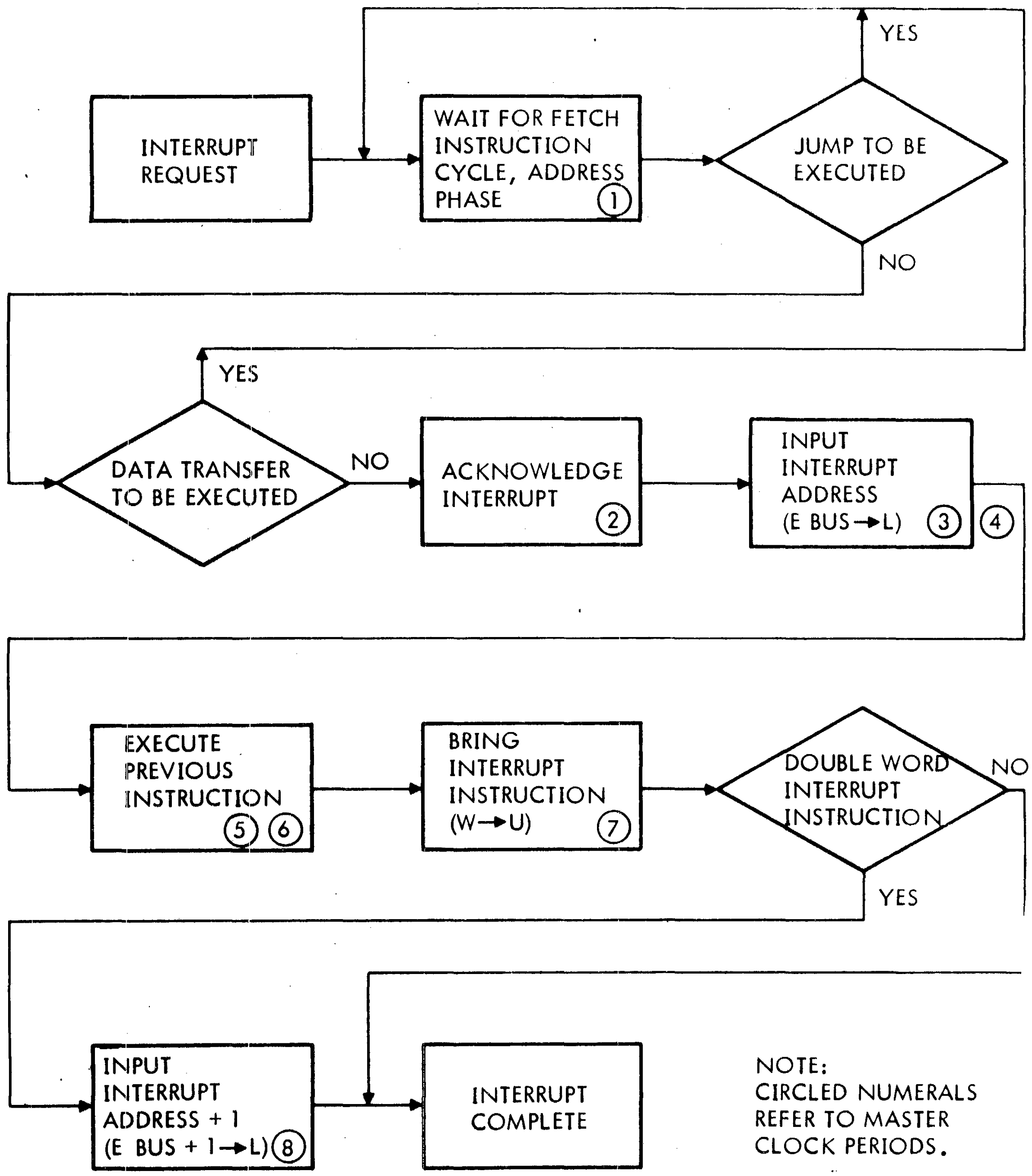


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Figure VI-9. Interrupt Flow Diagram

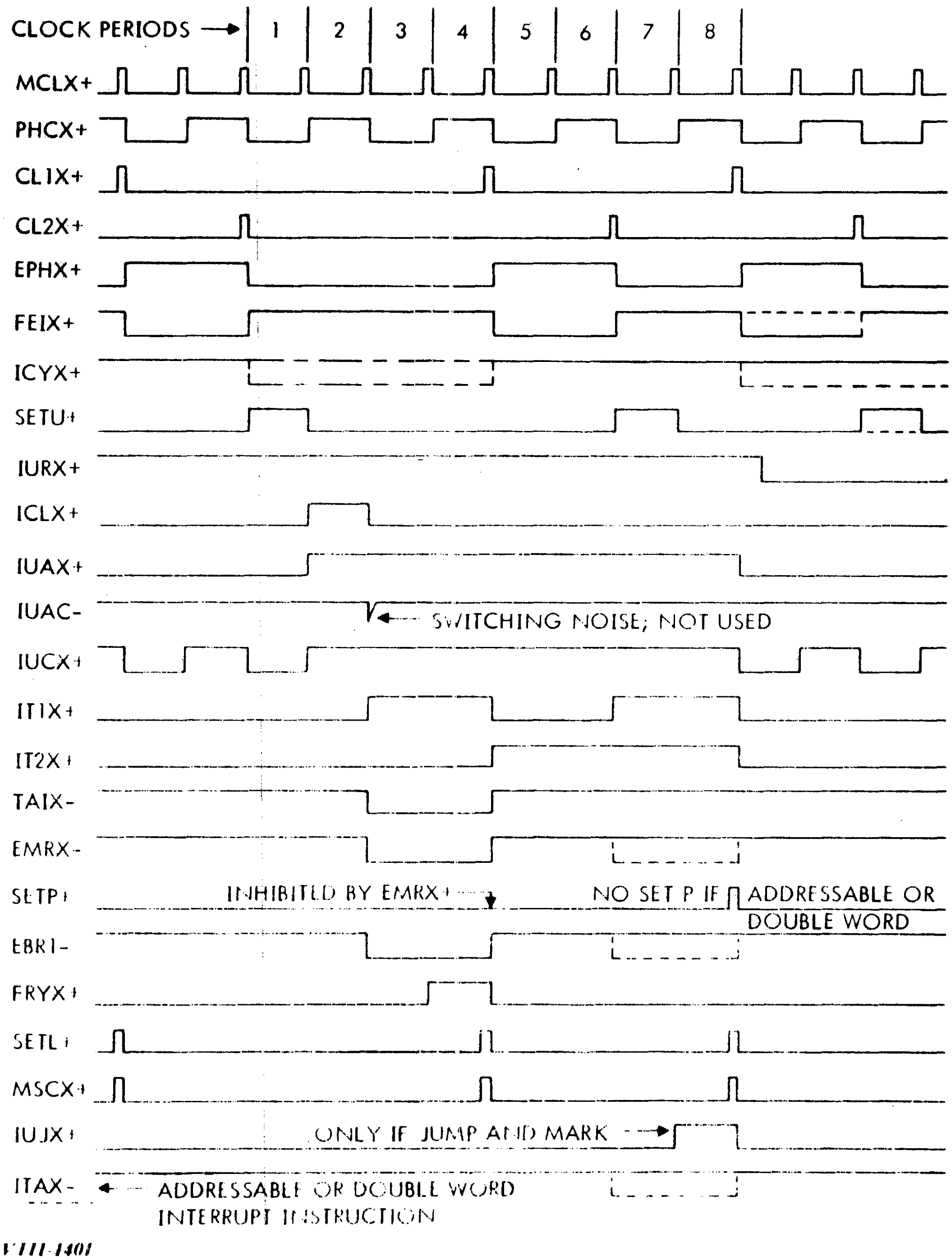


Figure VI-10. Interrupt Timing Diagram

On the trailing edge of MCLX+ at the beginning of period 2, the Inhibit Clock (ICLX) (1C3) flip-flop is set. The Interrupt Acknowledge (IUAX) (1C6) flip-flop is immediately set by ICLX+ (1C7) going true. Interrupt Clock (IUCX+) (1B4) is held true for the duration of IUAX+. ICLX- (1C3) prevents Clock 1 (CL1X+) (1B7) from occurring at the end of this period.

The ICLX flip-flop is reset on the trailing edge of MCLX+ at the beginning of the third period. This removes the dc set from the IUAX flip-flop and prevents the IUAX (1C6) flip-flop from setting. The IUAC flip-flop is not used in the interrupt sequence. Also, on the trailing edge of the third master clock pulse, Interrupt/Trap Timing flip-flop 1 (IT1X) (2D7) is set. This, in turn, causes the E and M Bus Receive (EMRX-) (1B2) signal and the Trap Address In (TAIX-) signal to go true. EMRX- clears the arithmetic unit of the computer momentarily to allow the interrupt address to be received from the I/O bus. TAIX- (2D5) generates the E Bus Receive (EBRX+) signal, which gates the interrupt address from the I/O bus onto the C bus. TAIX- also generates SETL+, which sets the interrupt address into the L register from the C bus.

Function Ready (FRYX+) goes true at the beginning of clock period 4. Neither the interrupt circuits nor the requesting option use FRYX+ during an interrupt.

On the trailing edge of the master clock at the beginning of clock period 5, flip-flop IT1X is reset and flip-flop IT2X (2D6) is set. EMRX- and TAIX- go false, removing EBRX+, SETL+, and FRYX+. A Memory Start Clock (MSCX+) is also issued on the trailing edge of master clock. This pulse initiates a memory cycle to bring the instruction at the interrupt address into the W register. During the first two of the four clock periods required for the memory cycle, the interrupted instruction is executed.

At the beginning of clock period 7, the interrupt instruction is set into the U register from the W register. Also, on the trailing edge of the master clock from the previous period, the IT1X flip-flop is again set. If the interrupt instruction is a one-word instruction, it is executed on the following cycle (beginning at the end of the eighth clock period). If the instruction is a two-word instruction, the Increment Interrupt Address (IIAX-) (2C6) signal and E1RX- go true. EMRX- again clears the arithmetic unit. IIAX- causes EBRX+ to again go true to gate the interrupt address onto the C bus from the I/O bus. At the same time, IIAX- ORs a one into bit 0 on the C bus via the A bus. By this method, the interrupt address is incremented to form the address of the second word of the two-word instruction. The address is placed in the L register at the end of the eighth period by CL1X+, which results in SETL+. If the two-word instruction is a JMPM instruction, Interrupt Jump (IUJX+) (1D6) is issued during the eighth period to inhibit the interrupt request capability of the controllers. The interrupt is complete at the end of the eighth period.

3.3.2 Trap Out

The description of the trap-out function of the interrupt/trap sequencer is presented in terms of MCLX + periods. Refer to figures VI-11 and VI-12 for the trap flow diagram and the trap timing diagram, both of which reference the appropriate MCLX + periods.

During clock period 1, both PHCX + and EPHX + are true, Trap Request (TPRX +) (1C1) is true, and no inhibits are present.

On the trailing edge of MCLX + at the beginning of period 2, flip-flop ICLX is set and it remains set for the duration of the trap. ICLX + is inverted to form the Multiply/Divide Negative (MDN2 +) (1D3) signal, which selects the arithmetic bus. It is also inverted to form ICLX- (1C2) which inhibits CL1X and CL2X + and holds PHCX + and EPHX + false. ICLX + going true immediately sets the IUAX flip-flop until the end of clock period 7. IUCX + is held true during this time by IUAX.

On the trailing edge of MCLX + at the beginning of period 3, flip-flop IUAC is set. This

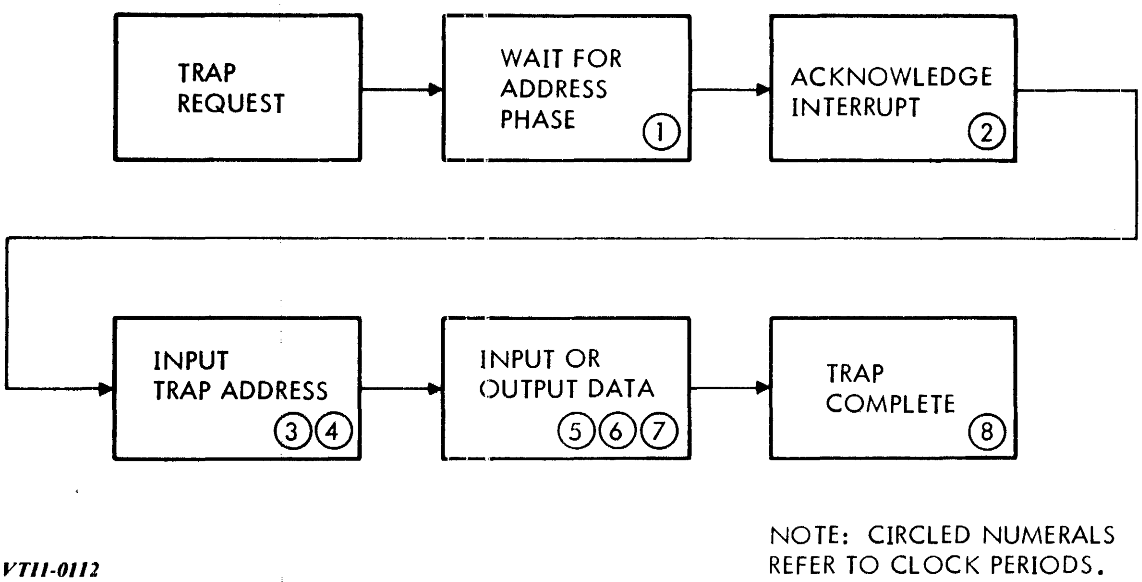


Figure VI-11. Trap Flow Diagram

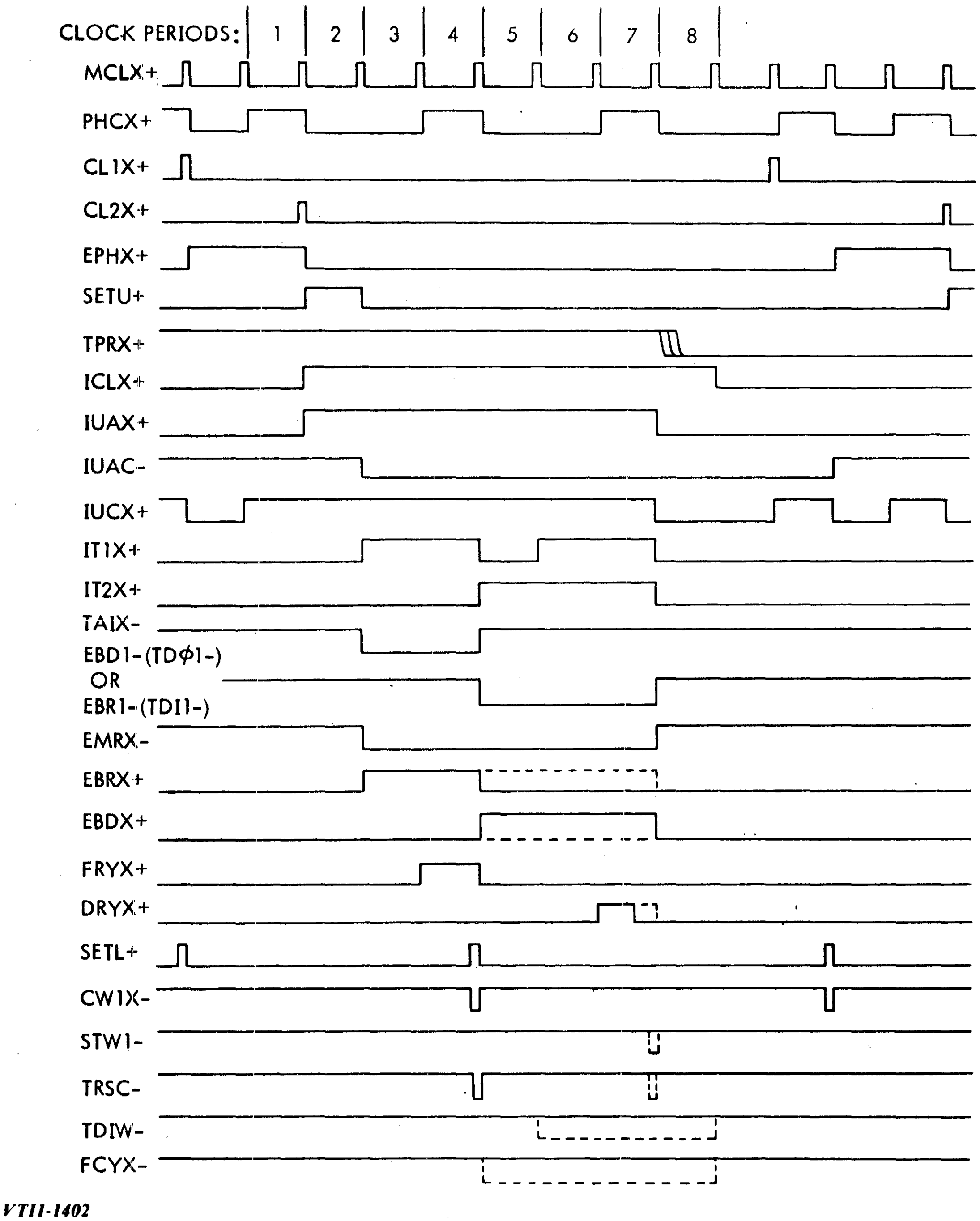


Figure VI-12. Trap Timing Diagram

allows the IUAX flip-flop to be reset near the end of the trap sequence while the ICLX flip-flop remains set. The trailing edge of MCLX+ also sets the first IT1X flip-flop. IT1X-produces Phase Clock 3 (PHC3-) (1B2). Also, with flip-flop IT2X false, IT1X produces TAIX. This, in turn, generates in EMRX-, EBRX+, and SETL+.

EMRX- clears the arithmetic unit of the computer momentarily to allow the trap address to be received from the I/O bus. EBRX+ gates the trap address from the I/O bus onto the C bus. SETL+ then sets the address into the L register from the C bus. PHC3-enables PHCX+ during period 4. TAIX- and the resulting signals remain true throughout periods 3 and 4.

During clock period 4, PHCX+ and TAIX- combine on processor card 4 (44P0593) to form FRYX+. FRYX+ is gated with MCLX+ in the trap sequencer to form the Clear W Register (CW1X-) (1A5) and Trap Start Clock (TRSC-) (1B4) signals. CW1X- clears the W register. TRSC- initiates a computer memory cycle. During the first two clock periods of the four required for this memory cycle, the contents at the trap address are brought out of memory and into the W register. FRYX+ also goes out on the I/O bus to signal the requesting device controller to remove the trap address from the E bus.

On the trailing edge of MCLX+ at the beginning of clock period 5, flip-flop IT1X is reset. Thus, TAIX- goes false and, as a result, EMRX-, EBRX+, SETL+, and PHC3- go false. Also, on the trailing edge of MCLX+, the second Interrupt/Trap Timing (IT2X) flip-flop (2D6) is set. IT2X+ results in EMRX-, Trap Data Out (TDO1-), and E Bus Drive 1 (EBD1-) signals. EMRX- again clears the computer arithmetic section. TDO1- enables the data output logic, which gates the contents of the W register onto the C bus via the A bus. EBD1- generates EBDX+, which gates the contents of the C bus into the I/O bus. IT2X+ and the resulting signals remain true until the end of period 7.

On the trailing edge of MCLX+ at clock period 6, flip-flop IT1X- is again set. IT1X, via PHC3-, enables PHCX+ on processor card 4.

During clock period 7, PHCX+ is true. PHCX+ and EBDX+ combine with timing signals on processor card 4 to form DRYX+. This signal is sent to the requesting device on the I/O bus to clock the data on the I/O E bus into the device. Note that DRYX+ for trap-out is 170 rather than the normal 237.5 nanoseconds. This ensures that the trailing edge of FRYX+ occurs before any data are removed from the I/O bus.

On the trailing edge of MCLX+ at the beginning of clock period 8, flip-flops IUAX, IT1X, and IT2X are reset. Thus, EBD1, TDOX-, EMPRX-, and EBDX+ go false. IUCX+ goes false as IUAX is reset. The requesting device removes TPRX+ (1C1) during this period following the trailing edge of DRYX+, which occurs before the end of period 7. The trailing edge of MCLX+ at the end of period 8 resets flip-flop ICLX to end the trap-out sequence.

3.3.3 Trap In

The description of the trap-in function of the interrupt/trap sequencer is presented in terms of MCLX+ periods. The trap-in function during the first three MCLX+ periods is the same as the trap-out function; therefore, this description starts with clock period 4. Refer again to figures VI-11 and VI-12 during this description.

At the start of clock period 4, PHCX+ and TAIX- combine on processor card 4 to form FRYX+. FRYX+ is gated with MCLX+ in the trap sequencer to form CW1X- and TESC-. CW1X- clears the W register and TRSC- initiates a memory cycle. However, this memory cycle serves no useful function in the trap-in sequence. FRYX+ also goes out on the I/O bus to signal the requesting device controller to remove the trap address from the E bus and to place the data onto the E bus.

On the trailing edge of MCLX+ at the beginning of clock period 5, flip-flop IT1X is reset. Thus, TAIX- goes false and, as a result, EMRX-, SETL+, and PHC3- go false. Also, on the trailing edge of MCLX+, flip-flop IT2X is set. IT2X+ results in EMRX-, Trap Data In (TDI1-) (2B7), and E Bus Receive (EBR1-) (2A7) signals. EMRX- again clears the computer arithmetic section. TDI1- generates the Not Full Cycle (i.e., half cycle) (FCYX-) (1A6) signal to the memory control card and enables logic for the generation of the Trap Data In Write (TDIW+) (1B7) and Set W Register (STW1-) (1A6) signals.

EBR1- generates EBRX+, which gates the contents of the I/O E bus onto the C bus. IT2X- and the resulting signals remain true until the end of period 7.

On the trailing edge of MCLX+ at the beginning of clock period 6, flip-flop IT1X is again set. IT1X, via PHC3-, enables PHCX+ on processor card 4. IT1X+ also sets the TDIW- (1A7) latch. TDIW- provides a write signal to memory during the remainder of the trap sequence.

During clock period 7, PHCX+ is true. PHCX+ and EBRX+ combine on processor card 4 to form DRYX+. DRYX+ and MCLX+ are gated by TDI1- in the trap sequencer to form STW1-, which transfers the data into the W register from the C bus. DRYX+ is also gated by MCLX+ to form TRSC-. TRSC- initiates a clear write half cycle memory operation that stores the contents of the W register in the location specified by the trap address in the L register during period 8.

On the trailing edge of MCLX + at the beginning of period 8, flip-flops IUAX, IUCX, IT1X, and IT2X, as well as TDIW-, are reset. Thus, EBR1-, TDIX-, EMRX-, EBRX +, and FCYX- go false. IUCX + goes false as IUAX is reset. The requesting device removes TPRX + (1C1) during this period following the trailing edge of DRYX +, which occurs at the end of period 7. The trailing edge of MCLX -- at the end of period 8 resets flip-flop ICLX to end the trap-in sequence.

3.4 DATA OUTPUT GATING

The data output gating section gates the contents of the W register onto the A bus during the data output portion of a trap-out. The Bar Output (WXXX-) (3BCD8) of each W register is first inverted and then NANDed with TDOX from the sequencer logic. The NAND gate output is ORed directly to the corresponding bit of the A bus (ABXX). The data go automatically from the A bus to the C bus. From there, it is gated onto the I/O bus by EBDX, which occurs as a result of a sequencer output (EBD1-) (2B7).

3.5 MNEMONICS

DMA/I mnemonics, with their definitions, are listed alphabetically in table VI-3.

Table VI-3. Mnemonic List

Mnemonic	Definition
AB00 through AB17	Arithmetic Bus Bit 0 through 17: This bus has memory data applied to it on trap-out.
AC0X +	Address Code 0: This signal, detecting XX0XXX, inhibits a trap request during a halt.
AC2X +	Address Code 2: This signal, detecting XX2XXX, gates the interrupt jump signal, (the interrupt instruction is a JMPM).
AC4X +	Address Code 4: This signal, detecting XX4XXX, inhibits an interrupt request if a shift instruction is in process.

Table VI-3. Mnemonic List *(continued)*

Mnemonic	Definition
CL1X +	Clock One: Resets trap on shift flip-flop.
DRYX +	Data Ready: Starts write cycle of trap data in and acts as a set strobe for the W register on trap-in operations.
EBR1-	E Bus Receive: Selects time when data are input on trap operation.
EBD1-	E Bus Drive: Selects time when data are output on trap operation.
EJIX-	Execute Jump Instruction: Decodes JMPM on interrupt.
EMRX-	E and M (Memory Bus) Receive: Clears the arithmetic unit momentarily for the passing of data from memory to I/O cable or I/O cable to memory.
EPHX	Execute Phase: Separates memory cycle into execution phase and address phase; used in timing trap detection.
FCYX-	Full Cycle (Memory): When this signal is false, the memory requires two start clocks for operation, first read and second read or write depending upon the operator. This signal delays the write operation on trap-in.
FEIX +	Fetch Instruction: Enables ICY and used in timing interrupt operations, to turn off trap-on shift, and to determine if interrupt instruction is single or double word.
FRCX-	Function Ready Control: Prevents interrupt on instructions following external control.
FRYX +	Function Ready: Gates memory start clock for trap output and input.

Table VI-3. Mnemonic List *(continued)*

Mnemonic	Definition
HTCX-	Halt Control: Output of halt control flip-flop; inhibits interrupts during a halt.
IAPX+	Instruction Address Phase: Decodes interrupt jump and inhibits interrupts during shift.
ICLX-	Inhibit Clock: Inhibits phase clock, clock 1, and clock 2 during selected portions of interrupt and trap. Gates set pulse to interrupt or trap acknowledge.
IIAX-	Increment Interrupt Address: Adds one to interrupt address when interrupting to double-word instructions.
IMCX-	Increment Memory Control: Inhibits trap request during increment memory operations.
IT1X+	Interrupt/Trap Timing 1: Provides timing for interrupt and trap operations.
IT2X+	Interrupt/Trap Timing 2: Provides timing for interrupt and trap operations.
IUAC-	Interrupt Acknowledge Control: Allows resetting of interrupt acknowledge prior to the resetting of inhibit clock during trap operations.
IUAX+	Interrupt Acknowledge: Provides timing for internal and external control during interrupt and trap operations.
IUCX+	Interrupt Clock: Provides external clock to control interrupt and trap request sequencing.
IUJX+	Interrupt Jump: An external signal gen-

Table VI-3. Mnemonic List *(continued)*

Mnemonic	Definition
	erated when the interrupt instruction is JMPM; disables the PIM.
IURX+	Interrupt Request: External input requesting interrupt sequence.
JCMX-	Jump Condition Met: Inhibits interrupts during JMP.
KIXX+	Class 1: True for all single-word addressing instructions; decodes IIAX.
K2XX+	Class 2: Decodes shift instructions so that interrupt sequences can be inhibited.
K3XX+	Class 3: Decodes all I/O instructions; prevents interrupt detection during I/O instructions.
MDN2+	Multiply Divide Negative: Selects arithmetic bus during interrupt or trap.
PHC3-	Phase Clock 3: Phase clock gate signal to control phase clock during trap operations.
PHCX-	Phase Clock: Decodes interrupt jump and timing of trap operations.
ROHX+	Reset on Halt: Resets control flip-flops.
SHC3-	Shift Control Gate 3: Enables SHCX+ on shift instructions to inhibit interrupt detection.
SHFX-	Shift: Enables shift operation on shift, multiply, and divide operations; enables trap-on shift flip-flop if a trap occurs during a shift operation.
SOPX-	Stop: Provides control for manual halt and step operations; inhibits interrupt during step operation.

Table VI-3. Mnemonic List *(continued)*

Mnemonic	Definition
STRX-	Start: Provides control for manual step and run; inhibits interrupt during step operation.
STW1-	Set W Register: Sets the W register during a trap-in.
SYRT+	System Reset: Front panel switch to initialize system.
TAIX-	Trap Address Input: Selects time when address is input on trap or interrupt operations.
TDIW-	Trap Data In Write: Provides write signal to memory on second half-cycle of trap-in.
TOSX-	Trap On Shift: Detects and stores trap on shift, multiply, or divide; readdresses next instruction.
TPIX+	Trap Input: External trap input signal.
TPOX+	Trap Output: External trap output signal.
TPRX+	Trap Request: Provides trap request signal from TPOX and TPIX.
TRSC-	Trap Start Clock: Initiates memory cycles during trap-in and trap-out.
W00X- through W17X-	Memory Word Buffer: Bits 00-17 gate data on trap output from memory data register to A bus.

SECTION 4
MAINTENANCE

4.1 GENERAL

There are no adjustable components, such as variable resistors or capacitors, on the DMA/I circuit card. This section provides simple test programs and procedures to assure satisfactory DMA/I operation. During the tests, disconnect the I/O cable from card slot 26 of the computer mainframe.

4.2 TRAP-OUT TEST

The trap-out test assures that the trap-out function of the DMA is operating satisfactorily.

a. Load the following program into the indicated memory addresses.

Memory Address	Octal Code	Description
000	052525	Bit pattern 0 101 010 101 010 101
100	005000	NOP
101	005000	NOP
102	005000	NOP
103	005000	NOP
104	001000	JMP to address 100
105	000100	

b. Set the P register to 000100 and start the program by pressing the RUN switch on the computer console.

c. Ground the TPOX-I signal at pin 37 of DMA/I card slot 15. This simulates a trap-out signal from a device requesting the computer to transfer one word of data from memory.

d. Sync oscilloscope to DRYX+ at pin 24 of slot 13 in the computer mainframe. With the oscilloscope, check logic levels of EB00-I through EB15-I to confirm the bit pattern (0101010101010101) stored at memory address 0. Refer to table VI-4 for I/O connector pins and logic levels of the E bus signals.

e. Halt the program and load the inverse bit pattern (1010101010101010) into memory address 0.

f. Start program by pressing the RUN switch on the computer control panel.

g. Confirm again the logic levels of EB00-I through EB15-I, this time for the inverse bit pattern.

Table VI-4. Pin Assignments and Logic Levels for I/O Lines

Signal	Slot 26	052525 Bit Pattern	0125252 Bit Pattern
EB00-I	2	1	0
EB01-I	4	0	1
EB02-I	6	1	0
EB03-I	8	0	1
EB04-I	10	1	0
EB05-I	11	0	1
EB06-I	12	1	0
EB07-I	13	0	1
EB08-I	14	1	0
EB09-I	15	0	1
EB10-I	16	1	0
EB11-I	17	0	1
EB12-I	18	1	0
EB13-I	19	0	1
EB14-I	20	1	0
EB15-I	21	0	1

4.3 TRAP-IN TEST

The trap-in test assures that the trap-in function of the DMA is operating satisfactorily.

a. Load the following program into the indicated memory addresses.

Memory Address	Octal Code	Description
100	005000	NOP
101	005000	NOP
102	005000	NOP
103	005000	NOP
104	001000	JMP
105	000100	

b. Set the P register to 000100 and start the program by pressing RUN on the control panel.

c. Ground the TPIX-I signal at pin 38 of DMA/I card slot 15. This simulates a trap-in signal from a device requesting the computer to transfer one word of data to memory.

d. Ground any line of EB00-I through EB15-I (except EB06-I) on card slot 26 (refer to table VI-4). EB06-I must not be grounded because the program is stored at that address (000100).

e. Halt the program by pressing STEP. Data should have been transferred from the E bus to memory. The data and memory addresses depend on the grounded EBXX-I pin. The data and memory addresses for the EBXX-I lines are listed in table VI-5.

Table VI-5. Memory Address and Data for Grounded EBxx-I Lines

Signal	Address	Data
EB00-I	000001	000001
EB01-I	000002	000002
EB02-I	000004	000004
EB03-I	000010	000010
EB04-I	000020	000020
EB05-I	000040	000040
EB06-I*	000100*	000100*
EB07-I	000200	000200
EB08-I	000400	000400
EB09-I	001000	001000
EB10-I	002000	002000
EB11-I	004000	004000
EB12-I	010000	010000
EB13-I	020000	020000
EB14-I	040000	040000
EB15-I	100000	100000

* Do not ground EB06-I.

4.4 INTERRUPT TEST

The interrupt test assures that the interrupt circuits are operating satisfactorily.

a. Load the following program into the indicated memory addresses.

Memory Address	Octal Code	Description
000	001000	JMP to address 50
001	000052	Address
050	004206	Shift A register left six places.
051	000000	Halt
052	000000	Halt
100	006010	Load A register immediate.
101	000707	Data
102	005000	NOP
103	000500	NOP
104	001000	Jump to address 100.
105	000100	Address

b. Clear the A, B, and X registers and set the P register to 00100.

c. Start the program by pressing RUN.

d. Momentarily ground IURX-I at pin 46 of slot 26. This simulates an interrupt request from an option. The program should stop and the A register should contain 070700.

CHAPTER VII

POWER SUPPLY

SECTION 1
THEORY OF OPERATION

1.1 GENERAL

The 620/L power supply (83P0035) provides all dc voltages required by the 620/L-100 computer. The regulated dc outputs of the supply are:

a. +5V at 0 to 17 amperes

b. −5V at 0 to 2 amperes

c. +12V at 0 to 6 amperes

d. −12V at 0 to 4 amperes

Application of dc power to the computer is controlled by the power switch on the computer control panel.

The power supply contains overcurrent protection circuits that prevent component damage in the event that one or more of the outputs is connected across a short circuit. When the short circuit is removed, the dc outputs automatically return to normal. The +5-volt output is also protected against an overvoltage condition whereby a low impedance is placed across the load when the output rises above 6.2 volts. A circuit breaker provides protection against overloads or shorts within the power supply.

1.2 SPECIFICATIONS

620/L power supply specifications are listed in table VII-1.

1.3 MAJOR ASSEMBLIES

The major electronic assemblies of the power supply are illustrated in figure VII-1. The power supply contains three types of circuit cards:

a. Regulator card (44P0528) - This card contains voltage regulator circuits for the four dc outputs.

b. Heat sink cards (44P0518) - The power supply contains four heat sink cards; each one contains two power transistors (or pass transistors) mounted on a heat sink.

c. Power supply card (44P0526) - This card contains various electronic components and card connectors J1 through J5 to accommodate the heat sink and regulator cards.

Table VII-1. Power Supply Specifications

Parameter	**Specification**
Ambient temperature range (free air, no forced air cooling)	0 to 55 degrees C
Adjustable voltage range	± 5 percent
Dc isolation	100 meg ohms minimum from primary to all other windings and chassis
Ripple	0.05 percent maximum peak-to-peak
Transient response	50 usec maximum for 50 percent change in load (note 1)
Input line frequency	47 to 63 Hz single phase
Input line voltage	105 to 125V ac or 210 to 250V ac
Input line current	5 amperes ac, full load
Line regulation (+12 and -12V dc)	10 mV maximum for 105 to 125V ac line change at one-half of full load
Line regulation (+5 and -5V dc)	10 mV maximum for 105 to 125V ac line change at one-half of full load
Load regulation (+5 and -5V dc)	35 mV maximum for 50 percent load change at 115V ac input (measured at power supply terminals)
Load regulation (+12 and -12V dc)	40 mV maximum for 50 percent load change at 115V ac input (measured at power supply terminals)

Table VII-1. Power Supply Specifications *(continued)*

Parameter	Specification
Relay turn on/off transient at output terminals	250V peak maximum
Fan output terminals	105 to 125V ac regardless of input AC voltage range
Total regulation	Regulation includes the combined effects of ripple, transient loads, dc loading from 0 to 100 percent, line voltage and frequency change, temperature, long term stability over 8 hours and all other sources
+5 and −5V dc	4 percent maximum
+12 and −12V dc	2 percent maximum
Power supply dissipation	450 watts maximum
Overload protection	Electronic current limit with automatic recovery
Over-voltage limit, including overshoot (+5V supply only)	5.7V dc minimum, 7.5V dc maximum
Short circuit current	Voltage / Short circuit current: +5: Less than 6 amperes −5: Less than 3 amperes +12: Less than 3 amperes −12: Less than 2 amperes The short circuit current shall in all cases be less than the full load current

Table VII-1. Power Supply Specifications *(continued)*

Parameter	Specification
Data guard sense voltage	15.5V ± 5 percent; measured open circuit at 105V ac input line voltage. The source will have a 1500-ohm series resistor and shall be capable of driving a minimum external load of 1800 ohms

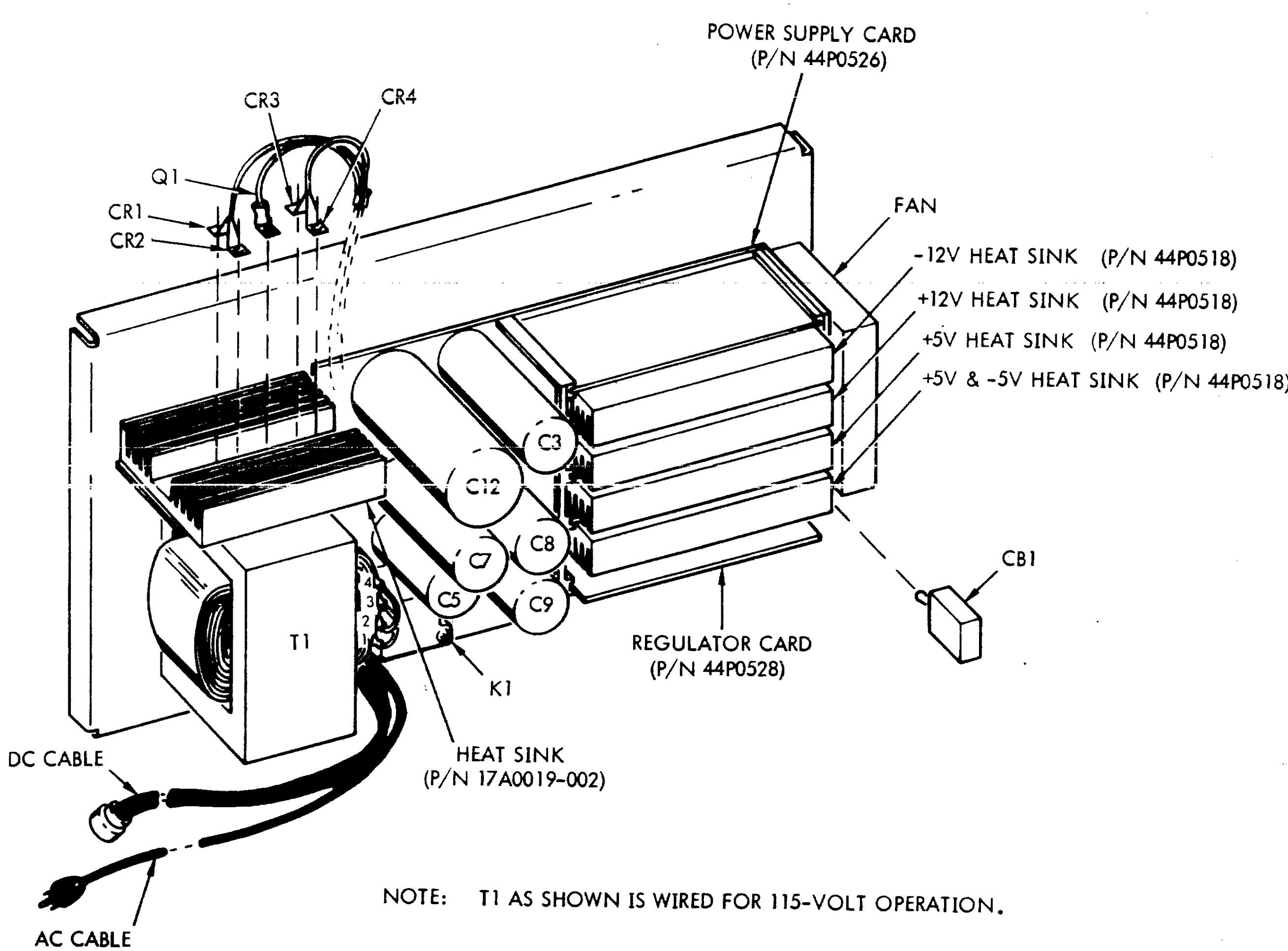
Note 1: Transient response is defined as the time required for the output voltage to return within the dc load regulation specification.

1.4 INPUT CIRCUIT

Refer to power supply schematic 95E0818 and the simplified input circuit schematic (figure VII-2). The ac power cable contains a black wire which is hot, a white wire which is neutral, and a green wire which is the chassis ground. Circuit breaker CB1 is connected to the black wire to provide protection against overloads or shorts within the supply. Capacitors C14 and C15 reduce input noise; and resistors R19 and R20 drain off the capacitor charge when the power cable is removed from the ac line voltage.

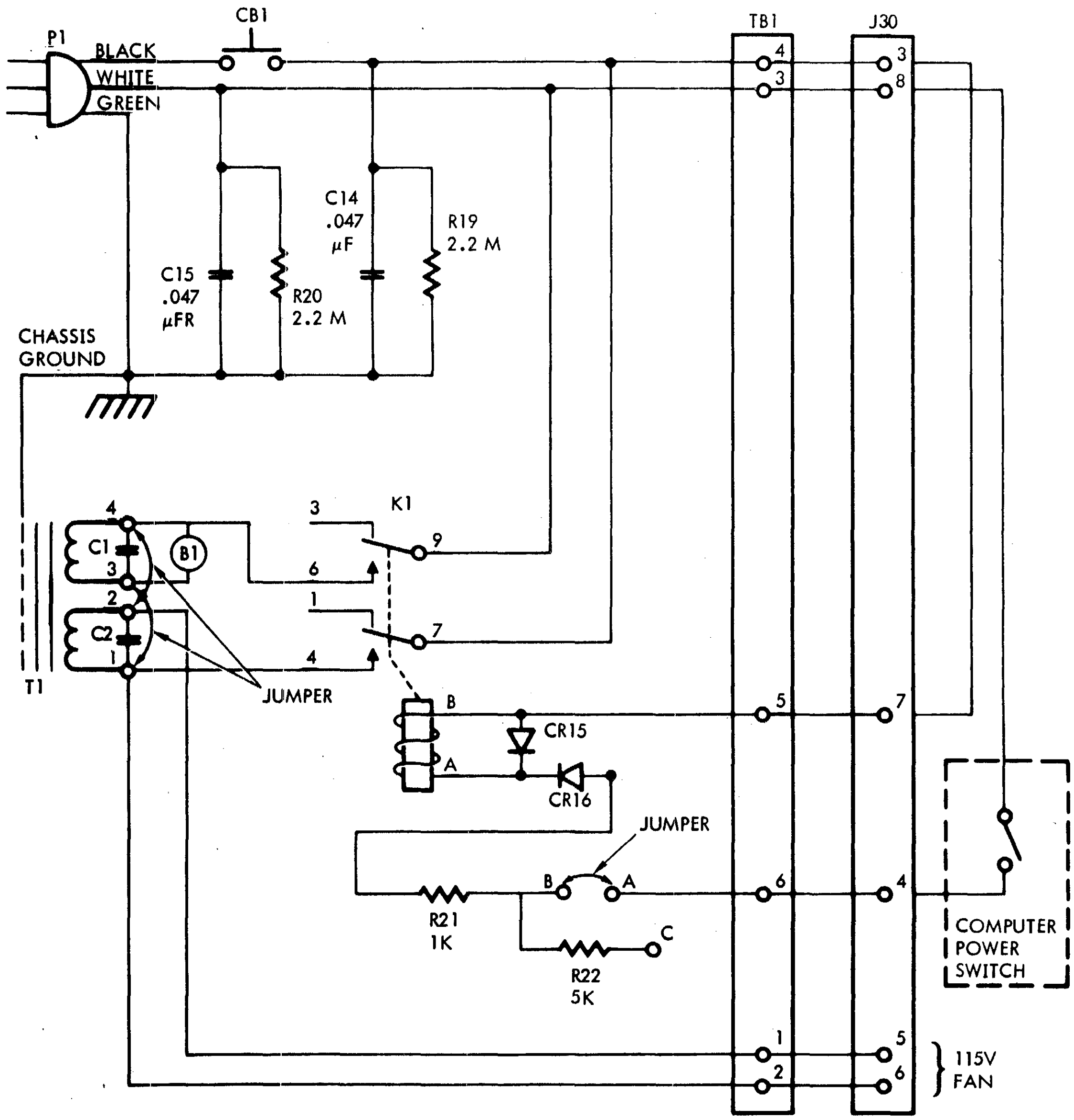
The ac line voltage is applied to pins 3 and 4 of terminal board TB1 enabling power relay K1 to be controlled by the power switch on the computer control panel. The hot ac line is routed through a jumper connected between pins 3 and 7 on the J30 connector to one end of the relay coil. The neutral ac line is routed through connector J30, the computer power switch, and the power supply jumper (A to B or A to C), to the other end of the relay coil. The power supply jumper is connected between points A and B for 115-volt operation, and between A and C for 230-volt operation. Relay K1, an ac relay, is energized with a pulsating dc voltage provided by diode CR16. Diode CR15 allows relay current to continue flowing during the off time of CR16.

When relay K1 is energized, ac line voltage is applied to the primary of power transformer



NOTE: T1 AS SHOWN IS WIRED FOR 115-VOLT OPERATION.

Figure VII-1. Power Supply Major Assemblies



NOTE: JUMPERS ARE CONNECTED FOR 115 VOLT OPERATION

VT11-1220

Figure VII-2. Simplified Input Circuit Schematic

T1. For 115-volt operation, jumpers connect pins 1 to 3 and 2 to 4 of the transformer; this places the two primary coils in parallel. For 230-volt operation, one jumper connects pin 2 to pin 3 of the transformer; this places the two primary coils in series, resulting in 115 volts across each.

Fan B1, which operates on 115 volts, is connected across one of the primary coils of T1 so that it receives 115 volts regardless of the transformer jumper connections. The other primary coil of T1 is connected across pins 1 and 2 of the terminal board to provide 115 volts for the fans in the computer. Capacitors C1 and C2 are connected across the transformer primaries to reduce the amount of radio frequency interference emanating from the supply.

1.5 RECTIFIER AND FILTER CIRCUITS

Refer to power supply schematic 95E0818 and the simplified schematic of figure VII-3. Power transformer T1, along with the rectifier and filter circuits, provides unregulated dc voltages (raw voltages) of the correct magnitude to drive the regulator circuits. Typical ac voltage values at the secondary taps of T1 (refer to figure VII-3) are:

a. Positive and negative 12-volt windings; 15.5V rms

b. Positive and negative 5-volt windings; 9.3V rms

c. Positive 12-volt boost winding; 7 rms with respect to the positive 12-volt output

The boost voltage provides operating power for the +12-volt regulator. The +12-volt regulator provides operating power for the +5-volt regulator which, in turn, provides power for the −5-volt and −12-volt regulators.

The rectifier and filter circuits convert the ac outputs of T1 to full-wave rectified voltages containing less than 2 volts peak-to-peak ripple at full load. The filter capacitors also provide the 2 milliseconds of energy storage required after a power-down condition.

Because of the large current requirements of the +5-volt and +12-volt outputs, the diodes for these circuits (CR1, CR2, CR3, and CR4) are mounted on a heat sink (part number 17A0019-002). The diodes for the Data Guard, −5-volt, and −12-volt circuits (CR12, CR14, CR8, CR9, CR5, and CR6) are located on the power supply card; the diodes for the boost voltage are on the regulator card.

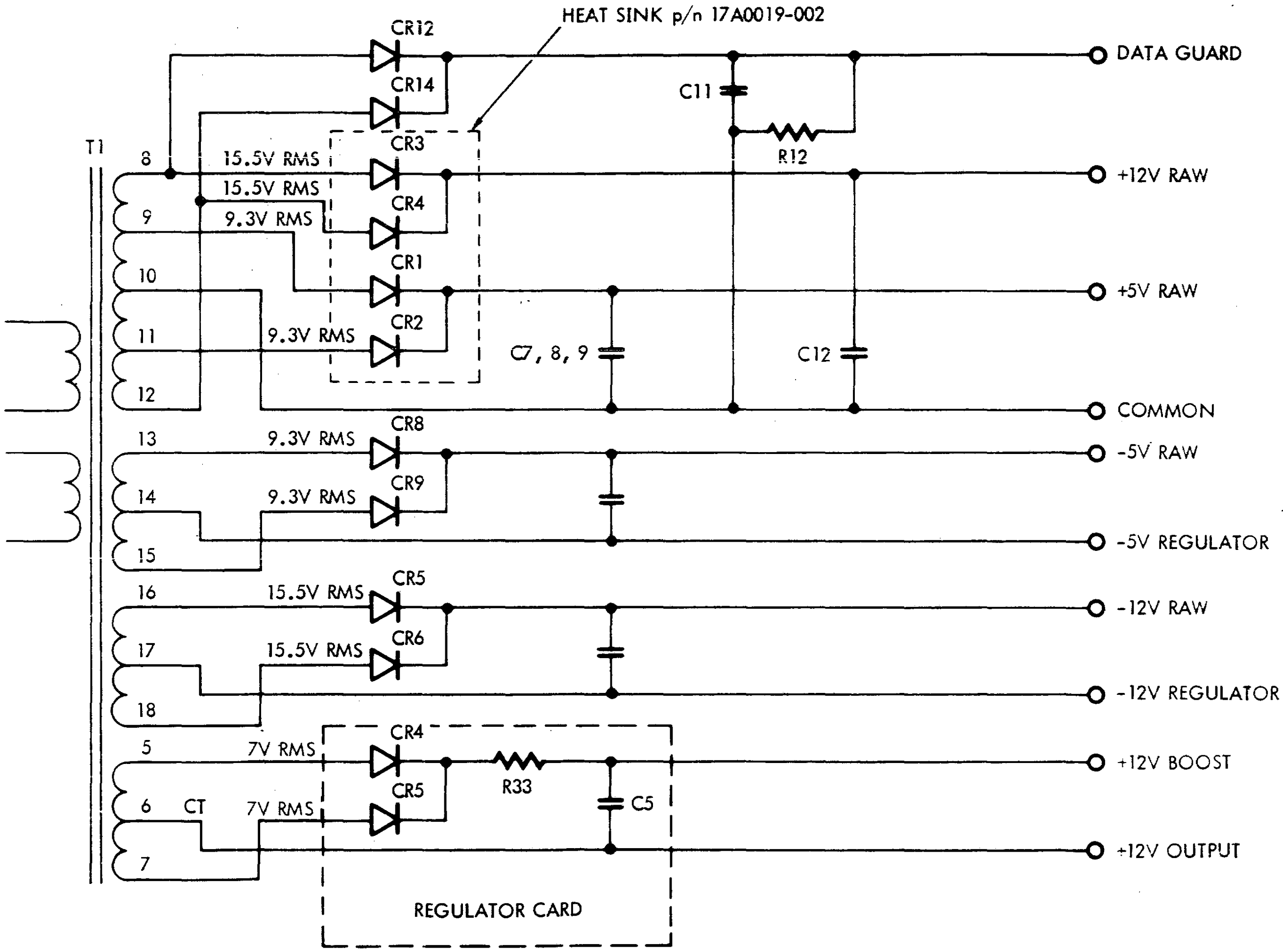


Figure VII-3. Rectifier and Filter Circuits

1.6 REGULATOR CIRCUITS

Drawing 91D0318 is the schematic for the regulator circuits. A regulator circuit is provided for each of the four dc outputs.

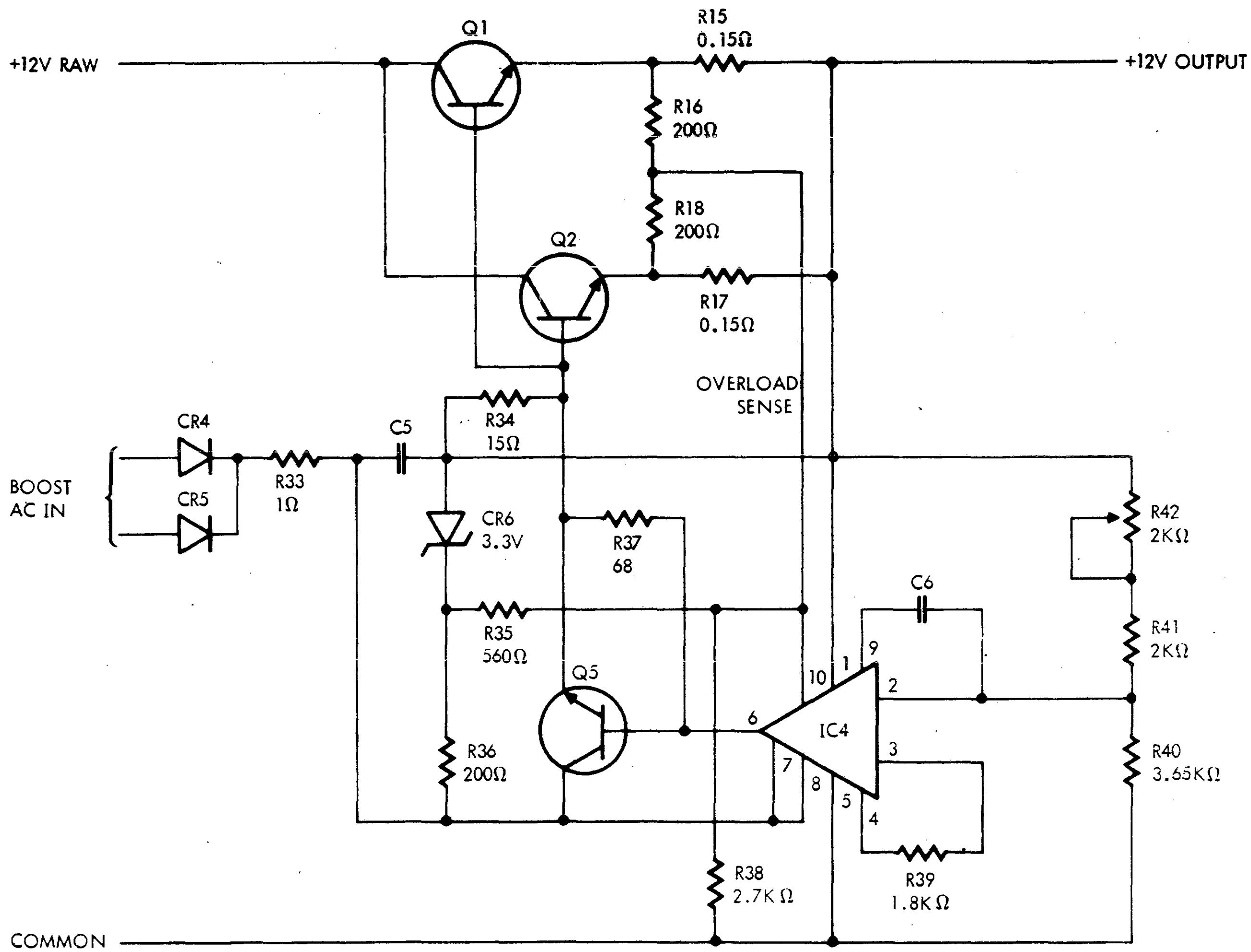
Each regulator circuit contains a Fairchild uA723C IC voltage regulator which drives the base of a transistor driver. The driver output is connected to the base of one or more pass transistors on the heat sink cards (44P0518). The +12-volt and -12-volt regulator circuits (IC4, Q5, and IC1, Q1) each drive two pass transistors. The +5-volt regulator circuit (IC3 and Q3) drives three pass transistors; the -5-volt regulator circuit (IC2 and Q2) drives one. Figure VII-4 is a schematic of the +12-volt regulator circuit and its associated pass transistors (Q1 and Q2).

A detailed block diagram of the IC voltage regulator is illustrated in figure VII-5. The temperature-compensated reference voltage from pin 4 of the IC is coupled through an external resistor to the noninverting input at pin 3. The voltage at pin 3 is compared with the regulator output that is fed back to the inverting input at pin 2. The reference voltage is a stable dc voltage in the 6.8 to 7.35 range (depending on the individual IC).

For the +5-volt and -5-volt regulators, the voltage at pin 3 of the IC is adjusted to 5 volts with a potentiometer. This causes the output current at pin 6 to produce a feedback voltage at pin 2 equal to the voltage at pin 3 (5 volts). At this time the regulator reduces its gain until the output current through the load is sufficient to develop 5 volts.

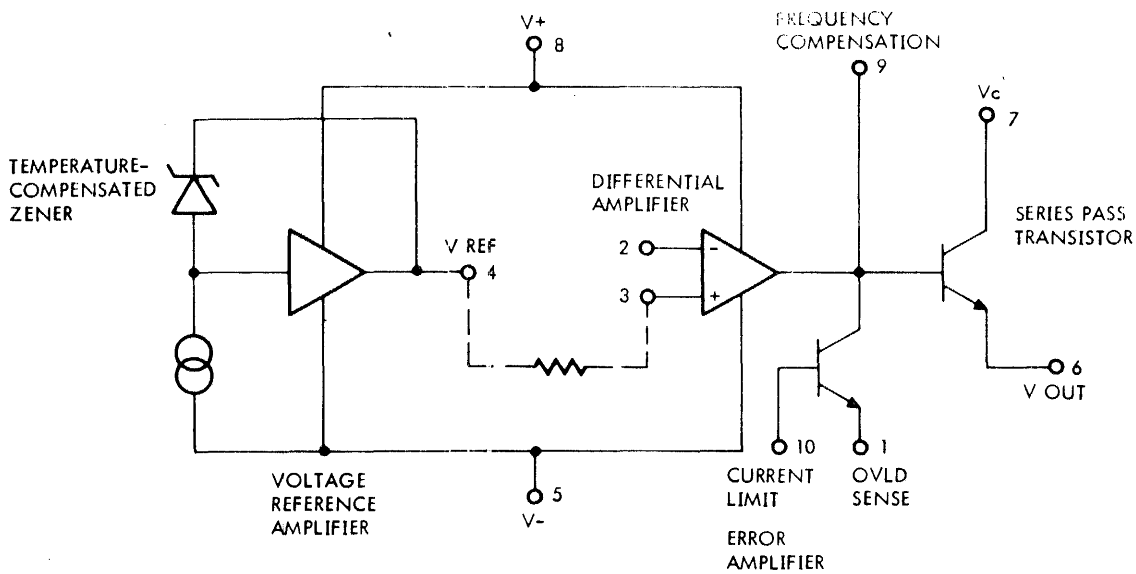
For the +12-volt and -12-volt regulators, the regulator output voltage (instead of the reference voltage) is adjusted with a potentiometer in the voltage divider network connected to pin 2 of the IC.

For the positive voltages (+5 and +12), pin 5 of the IC regulator is common and the outputs (emitters) of the pass transistors are the positive output voltages. For the negative voltages (-5 and -12), pin 5 of the IC regulator is the negative output voltage and the outputs (emitters) of the pass transistors are connected to common through the emitter resistors.



VIII-1222A

Figure VII-4. + 12-Volt Regulator Schematic



VIII-1223

Figure VII-5. IC Voltage Regulator Block Diagram

1.6.1 Overcurrent Protection

Overcurrent protection circuits are included in each regulator circuit. Because the overcurrent circuits are similar, only the one for the +12-volt regulator circuit is described (refer to figure VII-4).

The overcurrent circuit consists of the following components:

a. R15 and R17 to provide a voltage drop proportional to output current

b. R16 and R18 to isolate the Q1 and Q2 emitters, and sample each emitter voltage

c. R35 to provide a current path to the cathode of CR6

d. R38 to provide a current source for R16 and R18

e. CR6 to provide +3.3 volts with respect to +12 volt output

f. R36 to provide current to turn on Zener diode CR6

g. IC4 to sense an overload condition and remove regulator control

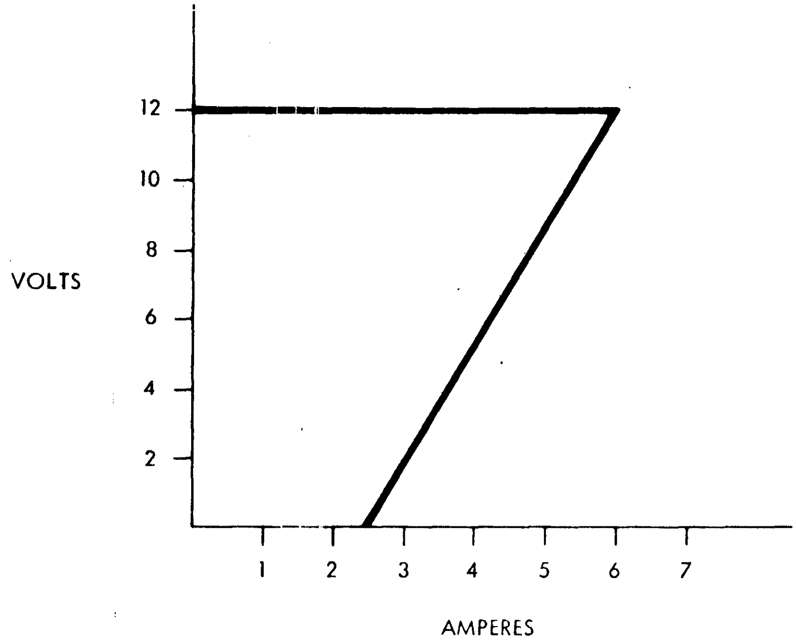
An overcurrent conditon for the +12-volt circuit occurs when the output current exceeds 8 amperes (6 amperes output current, 1 ampere to drive +5-volt regulator, and 1 ampere safety factor). Refer to section 1.1 for the maximum current ratings of the other dc outputs. The overcurrent condition produces +0.6 volts at IC4-10 with respect to IC4-1. This causes IC4 to reduce its drive current at pin 6.

The regulator circuit has foldback-current limiting which enables the circuit to produce less current when the output is shorted than that produced with a normal load. With a normal output of +12 volts, 12.60 volts is dropped across R38 causing approximately 4.7 milliamperes to flow through it. This current, which comes from the Zener diode through R35, would otherwise flow through R16 and R18, thus adding 0.47 volt to the IR drop of R15 and R17. With the +12-volt output shorted, the voltage across R38 is reduced to 0.6 volt so that only 0.27 milliampere flows through it. This causes the additional current to flow through R16 and R18, producing the foldback-current-limiting mode in which only 2.5 amperes of output current can flow before an overcurrent condition exists (0.6 volts between pins 1 and 10 of IC4). The curve for overcurrent characteristics of the +12-volt regulator circuit is illustrated in figure VII-6. The +5-volt and −12-volt regulators have similar overcurrent characteristics (refer to the specifications in table VII-1 for short-circuit currents). The −5-volt regulator circuit does not have foldback-current characteristics, but enters instead a constant-current mode. The curve for characteristics of this constant-current mode is illustrated in figure VII-7.

1.6.2 Overvoltage Protection

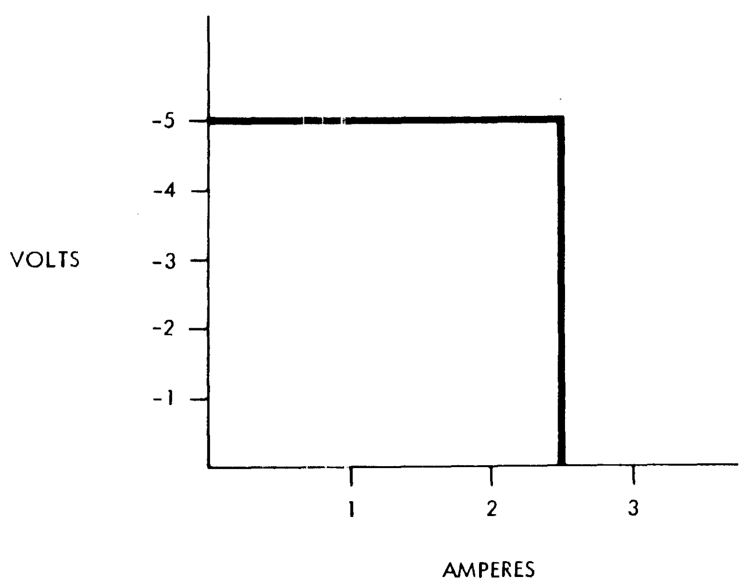
The +5-volt supply is protected against an overvoltage condition by an overvoltage protection circuit. The circuit senses the output voltage and, if it is greater than 6.2 volts, places a low impedance across the output load. The overvoltage circuit (figure VII-8) consists of a Zener diode and transistor circuit on the regulator card that drives an SCR mounted on the heat sink (17A0019-002).

Under normal conditions (+5-volt output), CR3 operates as a reverse-biased diode to provide a high impedance which keeps Q4 off. If the output voltage (+5V SENSE IN) rises to 6.2 volts, CR3 goes into its avalanche mode allowing enough current (6 milliamperes) to flow through R23 and R24 to turn on Q4. With Q4 conducting, the voltage developed at the junction of R25 and R26 turns on the SCR circuit (Q1) which provides a low impedance between the output terminals, reducing the output voltage to approximately 0.3 volts.



VIII-1224

Figure VII-6. Overcurrent Characteristics for the +12-volt Regulator



VIII-1225

Figure VII-7. Overcurrent Characteristics for the -5-volt Regulator

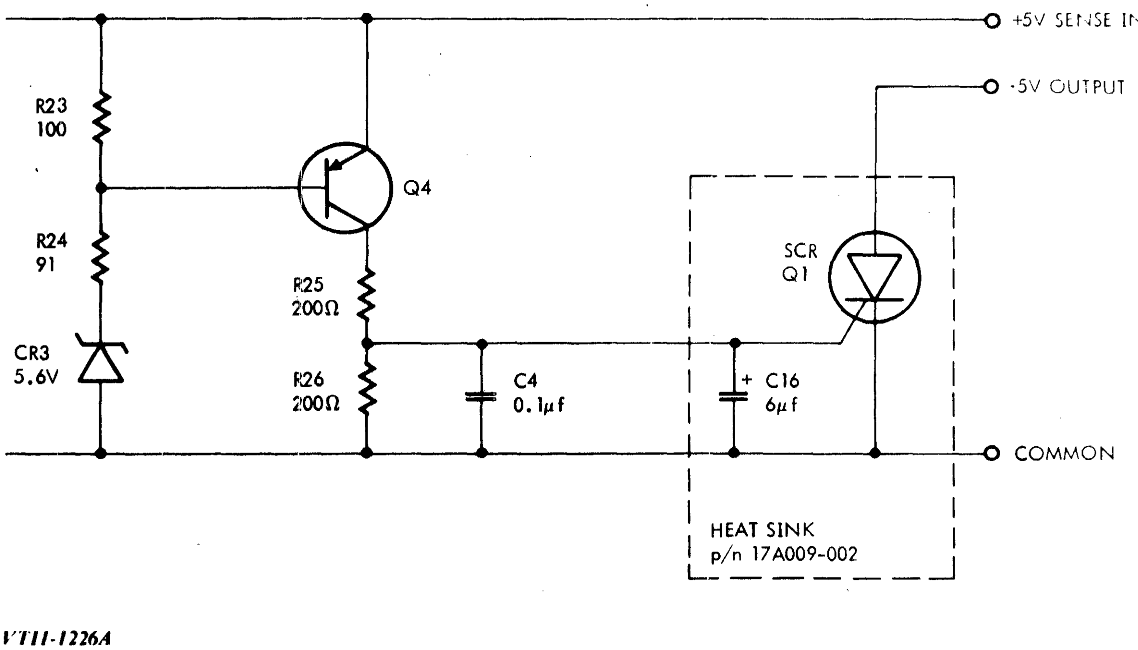


Figure VII-8. +5-Volt Overvoltage Protection Circuit

SECTION 2
MAINTENANCE

2.1 PREVENTIVE MAINTENANCE

Preventive maintenance for the power supply consists of cleaning, inspection, and checking of the test point voltages.

2.1.1 Cleaning

Severe accumulation of dust and dirt should be blown out of the supply interior with an air hose. Ensure that the wire screen adjacent to the fan is also clean and free of objects that might impair air flow. It is mandatory to remove any hardware (nuts, washers, etc.) that may accidentally drop into the supply. This hardware can usually be removed by tilting and shaking the supply. If the top cover is removed, be sure to remove the heat sink cards prior to shaking.

2.1.2 Inspection

With the supply de-energized and the top cover off, the regulator and heat sink cards can be removed for inspection. If the card-edge connectors are oxidized, they can be cleaned with a good quality contact cleaner. Allow the cleaner to dry before replacing the cards.

The only power supply devices that should show any wear are the power relay and the fan. The relay is filtered with a dust cover and normally does not require preventive maintenance. However, if the contacts become blackened by arcing, they can be cleaned with a good quality contact cleaner and/or a fine contact burnishing tool (remove the ac power cable before cleaning the contacts).

The fan requires no lubrication as it is lubricated for life at the factory. If fan operation tends to slow down or stall due to bearing wear, the fan should be replaced. Before replacing a fan, however, ensure that the abnormal operation is not due to some other reason such as an obstruction of the rotary blades, a disconnected fan plug, or the lack of ac voltage to the fan.

The supply must not be operated without the fan, although it can operate for up to an hour without the cover. During this type of operation, it is recommended that the supply be in a horizontal position to prevent the heat sink cards from slipping from their connectors. Before replacing the top cover, ensure that the regulator and heat sink cards are properly mated in their connectors.

The power cables should be inspected periodically to ensure that they are not under abnormal tension in any direction. Check that the cables do not become taut at any point when the supply is pivoted downward from its normal rack-mounted position.

2.1.3 Test Point Voltages

The four dc output voltages can be monitored and adjusted at test points and potentiometers on the regulator card. These test points and potentiometers are accessible through openings in the top cover of the supply; the reference designations are:

Test Point	Potentiometer	Voltage
TP1	R5	−12V
TP2	R17	−5V
TP3	R32	+5V
TP4	R42	+12V
TP5	---	Common

These test points and potentiometers are illustrated on regulator card assembly drawing 44D0528, logic diagram 91D0318, and in figure II-5 of chapter II. If the dc voltages cannot be adjusted to the proper values, refer to the corrective maintenance information that follows in section 2.2 of this chapter.

2.2 CORRECTIVE MAINTENANCE

Computer troubleshooting usually consists of isolating a malfunction to either the CPU, memory, or the power supply. Incorrect dc voltage readings do not always indicate a malfunctioning power supply. This condition could be a short circuit in the CPU or memory as well as a fault in the power supply.

Computer troubleshooting usually consists of isolating a malfunction to either the CPU, memory, or the power supply. Incorrect dc voltage readings do not always indicate a malfunctioning power supply. This condition could be a short circuit in the CPU or memory as well as a fault in the power supply.

2.2.1 Resistance Checks

Table VII-2 lists some resistance checks that are helpful in determining whether an incorrect dc voltage is caused by the power supply or the computer. The resistance values are approximate and can vary slightly depending on the memory size. The checks should be made with an ohm-meter at mainframe connector J30 with the dc power cable disconnected. If the resistance readings agree with the values listed in table VII-2 the malfunction is probably in the power supply.

Table VII-3 lists some resistance checks that are helpful in isolating a malfunction within the power supply. With the dc power cable disconnected from the mainframe, the checks should be made at cable connector P30 with ac power removed from the supply. If these resistance checks are correct, the malfunction is most likely one of the following:

a. An open pass transistor on one of the heat sink cards.

b. A bad regulator on the regulator card.

c. A shorted main filter capacitor (C1, C2, C3, C5, C7, C8, C9, C11, C12, C14, or C15) on the power supply card.

d. A bad rectifier (CR1, CR2, CR3, CR4, CR5, CR6, CR9, CR12, or CR14) on the power supply card.

If the resistance readings are considerably different than the values listed in table VII-3 the malfunction is most likely one of the following:

a. A bad output filter capacitor (C4, C6, C10, or C13) on the power supply card.

b. A bad safety diode (CR7, CR10, CR11, or CR13) on the power supply card.

Table VII-2. Mainframe Connector Resistance Checks

Function	J30 Pins	Ohms (approximate)
+12V	12 to 17	150, one direction 12, other direction
−12V	13 to 17	150, one direction 500, other direction
−5V	15 to 17	70, one direction 45, other direction
+5V	14 to 17	16, one direction 4, other direction
Data guard	10 to 17	Zero, power switch off 4,000, power switch on
Power switch	4 to 8	Zero, power switch on Open, power switch off
115V jumper	−3 to 7	Zero

Table VII-3. Power Supply Resistance Checks

Function	P30 Pins	Ohms (approximate)
+ 12V	12 to 17	500, one direction 9, other direction
− 12V	13 to 17	500, one direction 9, other direction
− 5V	15 to 17	1,000, one direction 9, other direction
+ 5V	14 to 17	200, one direction 9, other direction

2.2.2 Fault Isolation

When isolating malfunctions it is important to remember that the power supply design is based on dependency operation: the + 12-volt regulator depends on the boost voltage, the + 5-volt regulator depends on the + 12 volts, and the − 5-volt and − 12-volt regulators depend on the + 5 volts. Thus, if something happens to the + 12-volt circuits, the + 5-volt, − 5-volt, and − 12-volt circuits are affected. Furthermore, if something happens to the + 5-volt circuit, the − 5-volt and − 12-volt circuits are affected.

For example, if the output voltages are

+ 12V equal to + 12V
+ 5V equal to + 0.7V
− 5V equal to − 0.2V
− 12V equal to − 0.2V

and, if it has been determined that the computer is not causing the problem, the probable cause would be in the + 5-volt circuits which provide power for the − 5-volt and − 12-volt sections. In this example, the overvoltage protection circuit is the probable cause.

Possible power supply failures with probable causes are listed below.

a. If there are no dc outputs and the fan is inoperative, probable causes are:

1. No ac input voltage. Check for voltage at the ac power plug. If no voltage is present, check the power and main circuit breaker in the building. If voltage is present, ensure that the power supply circuit breaker is on, the computer power switch is on, and the dc power cable is connected to the computer.

2. Open wire or bad computer power switch. Make continuity check between pins 4 and 8 and pins 3 and 7 of mainframe connector J30 as listed in table VII-2. Check the computer power switch wiring.

3. Power relay K1 inoperative. Remove the top cover of the power supply and observe relay action when the computer power switch is activated. If the relay actuates, check the wiring from the relay to the power transformer (the push tabs should be fully inserted). If the relay coil does not actuate, check the jumper on the power supply card. For 115-volt operation, the jumper connects between terminals A and B; for 230-volt operation, between terminals A and C. Check the relay coil for continuity; replace the relay if the coil is open.

b. If there are no dc outputs, the fan operates properly, and the Data Guard signal is present (approximately 15 volts dc), the probable cause is in the +12-volt circuits. Variations of this malfunction are:

1. The dc outputs are very low or zero. The probable cause is an open +12-volt pass transistor on the heat sink card installed in J2 of the power supply card.

2. The dc output voltages are too high or zero. The probable cause is a faulty +12-volt regulator circuit.

3. High ripple or no dc outputs. One probable cause is an open rectifier (CR3 or CR4) on the heat sink (17A0019-002). For proper operation, approximately 20 volts dc should be present at the cathodes of CR3 and CR4 with respect to common. Another possible cause is a shorted rectifier (CR3 or CR4) or main filter capacitor (C12) on the power supply card. This condition should trip the power supply circuit breaker.

4. No dc outputs. The probable cause is the absence of the +12-volt boost voltage. There should be 14 volts rms across terminals E20 and E21 of the power supply card. Ensure that the transformer push tabs are fully inserted, and check the transformer windings for continuity.

c. **If there are no dc outputs except +12-volts, the probable cause is in the +5-volt circuits. Variations of this malfunction are:**

1. The +12-volt output is present but the other three outputs are very low or zero. A possible cause is an open +5-volt pass transistor on one of the heat sink cards installed in J3 and J4 of the power supply card.

2. The +12-volt output is present but the other three outputs are 0.7 volt. A possible cause is a shorted +5-volt pass transistor. This would activate the overvoltage protection circuit (SCR conducting).

3. The +12-volt output is present but the other three outputs are 0.7 or zero volt. A possible cause is a shorted SCR in the overvoltage protection circuit.

4. The +12-volt output is present but the other three outputs contain excessive ripple. The probable cause is one of the +5-volt rectifiers (CR1 or CR2) on the heat sink. For proper operation, approximately 13 volts dc should be present at the cathodes of CR1 and CR2.

5. The +12-volt output is present but the other three outputs are 0.7 volt, zero volt, or ripply only. A possible cause is a bad +5-volt regulator.

d. If all the dc outputs are present except the – 5-volt output, the probable cause is in the – 5-volt circuits. Variations of this malfunction are:

1. All dc outputs are present except – 5 volts, which is very low or zero. The probable cause is an open – 5-volt pass transistor on the heat sink card installed in connector J4 of the power supply card.

2. All dc outputs are present except – 5 volts, which is too high or zero. The probable cause is the – 5-volt regulator circuit on the regulator card.

3. All dc outputs are present but – 5 volts contains excessive ripple. The probable cause is an open – 5-volt rectifier (CR8 or CR9). For proper operation, approximately + 8 volts dc should be present at the cathodes of CR8 and CR9. Another probable cause is a shorted – 5-volt rectifier (CR8 or CR9) or a shorted filter capacitor (C5) on the power supply card. This condition should trip the power supply circuit breaker.

e. If all dc outputs are present except the – 12 volts, the probable cause is an open – 12-volt circuits. Variations of this malfunction are:

1. All dc outputs are present except – 12 volts, which is very low. The probable cause is an open – 12-volt pass transistor on the heat sink card installed in connector J1 of the power supply card.

2. All dc outputs are present except – 12 volts, which is too high or zero. The probable cause is a bad – 12-volt regulator circuit on the regulator card.

3. All dc outputs are present except – 12 volts, which is zero or contains excessive ripple. The probable cause is an open rectifier (CR5 or CR6) on the power supply card. For proper operation, approximately + 8 volts should be present at the cathodes of CR5 and CR6. Another probable cause is a shorted rectifier (CR5 or CR6) or filter capacitor (C3) on the power supply card. This condition should trip the power supply circuit breaker.

f. **If all the dc outputs are present but the Data Guard voltage is not, the probable cause is in the Data Guard circuit on the power supply card. Variations of this malfunction are:**

1. The Data Guard voltage has excessive 60-Hz ripple or is zero volts. The probable cause is an open rectifier (CR12 or CR14) on the power supply card. For proper operation, approximately 19 volts should be present at the cathodes of CR12 and CR14.

2. The Data Guard Voltage has excessive 120-Hz ripple. The probable cause is an open filter capacitor (C11) on the power supply card. For proper operation, the ripple at the junction of C11 and R12 on the power supply card should be less than 5 volts peak-to-peak.

CHAPTER VIII

MNEMONICS

CHAPTER VIII
MNEMONICS

This chapter presents an alphabetized list of the menmonics that appear on the 620/L-100 logic diagrams. Descriptions and source locations are also provided. The location information is in parenthesis; it consists of the circuit card number and, when applicable, the sheet number of the logic diagram.

Title	Part Number	Logic Diagram Number
Register card	44P0592	91D0356
Processor control 1	44P0595	91D0359
Processor control 2	44P0596	91D0360
Processor control 3	44P0597	91D0361
Processor control 4	44P0593	91D0357
DMA and Interrupt	44P0598	91D0362
Auto Memory Enable/ Disable	44P0237	95C0235
Memory timing control	44P0599	91D0363
Driver/sink switch	44P0505	91D0283
Sense/inhibit	44P0506	91D0285

CHAPTER VIII
MNEMONICS

620/L Mnemonics

Mnemonic	Description
AB00- to AB15- Register card	**A Bus Bits 0 to 15** -- Common bus where outputs of the adder, shift logic, E bus input, and console are ORed to drive the C bus (CB00+ to CB15+)
ACYX+ Processor control 2	**Address Cycle** -- Timing function identifying the memory cycles used to obtain an address word, i.e., jump, input and output memory, and indirect addressing
AC0X+ to AC6X+ Processor control 2	**Address Codes 0 to 6** -- Decodes the M field (U register bits 9-11)
ANDX+ Processor control 2	**AND** -- Decodes the U register for the AND and inclusive-OR instructions
BISE- Processor control 4	**Bit Store Enable** -- Ground true signal to set BISX on a long shift to transfer A0 or A15 to the B register
BISX Processor control 4	**Bit Store** -- Provides storage of an A register bit for transfer to the B register during long shifts and multiply or divide
CALX+ Register card	**Carry** -- Last bit of the adder, bit 15
CANL+ Register card	**Carry Next to Last** -- Bit 14 of the adder
CA0A to CA7A Driver/sink switch	**Common Anode Drive A** -- Signals from X write or Y read driver switches for 4K-A cores
CA0B to CA7B Driver/sink switch	**Common Anode Drive B** -- Signals from X write or Y read driver switches for 4K-B cores

620/L Mnemonics *(continued)*

Mnemonic	Description
CA05 + Register card	**Carry Bit 5** -- Output of bit 5 to bit 6
CA11 + Register card	**Carry Bit 11** -- Output of bit 11 to bit 12
CB00 + to CB15 + Register card	**C Bus Bits 0 to 15** -- Data bus in the computer that supplies data to the operation registers, console and outputs to the E bus
CBLX + Processor control 2	**Last C Bus Bit** -- Last bit of the C bus, CB15 +
CC0A to CC7A Driver/sink switch	**Common Cathode Drive A** -- Signals from X read or Y write driver switches for 4K-A cores
CC0B to CC7B Driver/sink switch	**Common Cathode Drive B** -- Signals from X read or Y write driver switches for 4K-B cores
CLEI + Processor control 4	**Clock Enable** -- Enables the primary system clock; provides synchronization with PHCX, off during HALT, and ICLX
CLRW- Processor control 4	**Clear W Register** -- Clears the memory data register at the start of a memory operation
CL1X + Processor control 4	**Clock 1** -- Major clock function, identifies the start of a memory cycle
CL2X + Processor control 4	**Clock 2** -- Major clock function, identifies the midpoints of a memory cycle when data are available, or when data can be set into the W register
DAGS- AMED	**Data Guard** -- Signal from the automatic memory enable/disable circuit; not used in the 620/L computer

620/L Mnemonics *(continued)*

Mnemonic	Description
DIVX- Processor control 4	**Divide** -- Indicates the occurrence of a divide operation
DRYX+ Processor control 4	**Data Ready** -- Provides data ready pulse to I/O bus; used to gate output data in external controllers
DRYX-I Processor control 4	**Data Ready** -- Pulse on I/O line that is used in external controllers to gate in data and to terminate the data phase
DSCX- Processor control 3	**Divide Sign Check** -- Result of a sign check during a divide operation
DXS0 to DXS7 Driver/sink switch	**Decoded X Sink** -- Decoded signals from address bits 6, 7, and 8
DYS0 to DYS7 Driver/sink switch	**Decoded Y Sink** -- Decoded signals from address bits 9, 10, and 11
D00X to D15X Sense/inhibit	**Data Outputs** -- Data output signals (inhibit lines) from the 16 inhibit drivers
EB00-I to EB15-I Register card	**E Bus Bit 0 to 15** -- Main input/output lines in the computer
EBDX+ Processor control 4	**E Bus Drive** -- Enables the E bus drivers; outputs C bus to E bus
EBRX+ Processor control 4	**E Bus Receive** -- Enables the E bus to be ORed to the C bus
EIMX+ Processor control 2	**Execute Immediate** -- Controls the transfer of U3-6 to U12-15 during an immediate instruction
EJIX- Processor control 2	**Execute Jump Instruction** -- Decodes jump, jump and mark, and execute instructions

620/L Mnemonics *(continued)*

Mnemonic	Description
EJRX+ Processor control 3	**Execute Jump or Register Change** -- Logical-OR of ERCX- and EJIX-
EJSX+ Processor control 2	**Execute Jump or Sense** -- Logical-OR of EJ1X- and ES1X-
EMRX- DMA and Interrupt	**E and W Bus Receive** -- Normally zero volt when trapping in or out
EPHX- Processor control 4	**Execute Phase** -- Major control function separates memory cycle into execute and address phase; execute phase occurs when EPHX+ is 5 volts
ERCX+ Processor control 2	**Execute Register Change** -- Provides timing and selection for register change instructions
ESIX- Processor control 2	**Execute Sense Instruction** -- Decode for sense instruction
EXCX- Processor control 1	**Execute** -- Provides selection of operand cycle during execute instruction
EXOR+ Processor control 2	**Exclusive-OR** -- Provides decoding of exclusive-OR, inclusive-OR, and register change complement instructions
FCDX- Processor control 4	**First Count Detect** -- Indicates that Shift counter SC00X and SC03X has reached a count of one
FCOX+ Processor control 2	**Function Code Zero** -- Denotes that the U register bits 6, 7, and 8 are equal to zero
FCYX+ DMA and Interrupt	**Full Cycle Command** -- When high, it enables a read or clear memory sequence followed by a restore or write memory sequence
FEAI Processor control 2	**Fetch Address** -- Enable for ACYX+ on all instructions that require an address cycle

620/L **Mnemonics** *(continued)*

Mnemonic	Description
FEIX+ Processor control 2	**Fetch Instruction** -- Enable for ICYX
FEOX+ Processor control 2	**Fetch Operand** -- Enable for OCYX
FRCX- Processor control 4	**Function Ready Control** -- Detects and controls the programmed function out sequence
FRYX-I Processor control 4	**Function Ready Control** -- Pulse used to terminate the address phase on the I/O line
FRYX+ Processor control 4	**Function Ready** -- Provides function ready to the I/O bus
G1XX+ to G4XX+ Processor control 2	**Group Decoding 1 to 4** -- Decodes U register bits 12 and 13
HLTX+ Processor control 1	**Halt** -- Controls execution (run) or non-execution (step) modes or computer operation
HTCX- Processor control 1	**Halt Control** -- Initiates halting of computer operation
H1XX+ to H4XX+ Processor control 2	**Set Decoding 1 to 4** -- Decodes U register bits 14 and 15
IAPX+ Processor control 2	**Instruction Address Phase** -- Provides timing function for address operations; occurs during the last half of instruction cycle
ICLX- Processor control 4	**Inhibit Clock** -- Inhibits CL1X+ and CL2X+ during an interrupt or trap operation
ICYX+ Processor control 2	**Instruction Cycle** -- Timing function identifying memory cycles used to obtain instruction words

620/L Mnemonics *(continued)*

Mnemonic	Description
IEPX+ Processor control 2	**Instruction Execute Phase** -- Provides timing function for instruction execution occurs during the first half of all instruction cycles
IIAX- Processor control 4	**Increment Interrupt Address** -- Adds one to the interrupt address when interrupting to double-word instructions
IMCX- Processor control 2	**Increment Memory Control** -- Provides control of the INR instruction
INCR+ Processor control 4	**Increment** -- Provides increment signal to the adder adds one to data at the adder
INHE-0 Memory timing cont.	**Inhibit Enable** -- Sent to sense/inhibit card of 4K-A stack
INHE-1 Memory timing cont.	**Inhibit Enable** -- Sent to sense/inhibit card of 4K-B stack
INHT- Sense/inhibit	**Inhibit Timing** -- Originates on the DM286 card where it is designated WSTX-
INHT1 Sense/inhibit	**Inhibit Timing 1** -- Enable signal for inhibit drivers of bits 0 through 7
INHT2 Sense/inhibit	**Inhibit Timing 2** -- Enable signal for inhibit drivers of bits 8 through 15
IXYD- Driver/sink switch	Not used
JCMX+ Processor control 1	**Jump Condition Met** -- Stores detection of jump condition met on jump, jump and mark, execute, and sense instructions
JCN1+ (DM109-1)	**Jump Condition Met, Gate 1** -- Logical-OR of all tests for jump, jump and mark, and execute condition met

620/L Mnemonics *(continued)*

Mnemonic	Description
K1XX + Processor control 2	**Class 1** -- Decodes U register bits 12, 13, and 14 for all single-word addressable instructions
K2XX + Processor control 2	**Class 2** -- Decodes U register op-code 00; selects all jump, jump and mark, execute and shift, register change, immediate, and set/reset overflow instructions
K3XX + Processor control 2	**Class 3** -- Decodes and selects all I/O instructions
K23X + Processor control 2	**Class 23** -- Provides decoding for K2 or K3 instructions
LDPINT- Memory timing cont.	**Loader Protect Interrupt** -- Not used
LSCX + Processor control 4	**Long Shift Control** -- Provides control of long shift, multiply, and divide sequences; the A register is selected when LSCX is on, and the B register when LSCX is off
L00X + to L15X + Processor control 1	**Memory Address Register** -- Contains the address of the data that memory is reading or writing
MCLX + Processor control 4	**Master Clock** -- Basic crystal-controlled 2.2-MHz clock for the system
MC2X + Processor control 4	**Master Clock 2** -- Controlled 2.2-MHz clock; gated off by inhibit clock (ICLX) and halt functional (HTCX, HLTX)
MDN2 + Processor control 2	**Multiply/Divide Not** -- Selects the A bus during interrupt, trap, or divide operations
MRKX + Processor control 2	**Mark** -- Provides the timing and control function for jump and mark instructions

620/L Mnemonics *(continued)*

Mnemonic	Description
MRSX + Processor control 1	**Manual Register Select** -- Enable for setting registers in the manual mode
MSAX- Processor control 3	**Manual Select A Register** -- Manual selection of the A register from the console
MSBX- Processor control 3	**Manual Select B Register** -- Manual selection of the B register from the console
MSCE + Memory timing cont.	**Memory Start Clock Enable** -- This signal not used
MSC1 + Processor control 4	**Memory Start Clock 1** -- Sent to the memory timing control card where it is designated SSL1 +; initiates a memory cycle for the first 8K of memory
MSC2 + Processor control 4	**Memory Start Clock 2** -- Sent to the memory timing control card where it is designated SSL2 +; initiates a memory cycle for the second 8K of memory
MSC3 + Processor control 4	**Memory Start Clock 3** -- Sent to the memory timing control card where it is designated SSL3 +; initiates a memory cycle for the third 8K of memory
MSC4 + Processor control 4	**Memory Start Clock 4** -- Sent to the memory timing control card where it is designated SSL4 + initiates a memory cycle for the fourth 8K of memory
MSPI- Processor control 1	**Memory Start Pulse Inhibit** -- Used in memory parity option to disable the setting of the memory start pulse flip flop

620/L Mnemonics *(continued)*

Mnemonic	Description
MSPX+ Processor control 1	**Memory Start Pulse** -- Delayed clock 1 for starting memory
MSPX- Processor control 3	**Manual Select P Register** -- Manual selection of the P register from the console
MSUX- Processor control 3	**Manual Select U Register** -- Ground true when selecting the U register from the console
MSXX- Processor control 3	**Manual Select X Register** -- Manual selection of the X register from the console
ND0 to ND7 Driver/sink switch	**Negative Drive Decoded Signals** -- Decoded signals from multiplexed address bits 0 through 5; sent to the negative-drive driver switches
OCYX+ Processor control 2	**Operand Cycle** -- Timing function identifying the memory cycles used to obtain an address word
OVXX+ Processor control 1	**Overflow** -- Detects and stores the overflow all tests for jump, jump and mark, and execute condition met
PDIX Processor control 4	**Program Data In** -- Provides the timing function for all programmed input operations
PDTX+ Processor control 4	**Program Data Transfer** -- Provides the timing function for all input/output instructions
PD0 to PD7 Driver/sink switch	**Positive Drive Decoded Signals** -- Decoded signals from multiplexed address bits 0 through 5; sent to the positive-drive driver switches
PFOX- Processor control 4	**Program Function Out** -- Timing function that controls the output of the function code of all I/O instructions

620/L Mnemonics *(continued)*

Mnemonic	Description
PHCX- Processor control 4	**Phase Clock** -- Basic timing function used to control basic clock functions, such as CL1X+ and CL2X+
REF VOLTAGE Sense/inhibit	**Reference Voltage** -- Provides the sense-amplifier threshold voltage
REPT- Processor control 1	**Repeat** -- Controlled by the instruction REPEAT switch on console; used to enable the setting of the RPCX flip-flop
ROHX+ Processor control 1	**Reset On Halt** -- Reset line to control the flip-flops on halt
RPCX- Processor control 1	**Repeat Control** -- Control function which inhibits set U register (SURX+) when stepping in repeat mode
RR15+ Processor control 2	**Repeated R15** -- Monitors bit 15 of the R register
RSHX+ Processor control 2	**Reset Shift Function** -- Resets the shift functions on halt and CL2
RSTM- Memory timing cont.	**Read Sink Timing** -- Provides timing for the X and Y read sink switches
RSTX Processor control 2	**Reset** -- Controlled by the display register RESET switch on the console; resets the bits of any register being displayed while in step mode
RUNX+ Processor control 1	**Run** -- Output of the RUN switch on the console; forms a pulse that places the computer in run mode
RWT1- Memory timing cont.	**Read/Write Timing 1** -- Timing signal for negative-drive driver switches

620/L Mnemonics *(continued)*

Mnemonic	**Description**
RWT2- Memory timing cont.	**Read/Write Timing 2** -- Timing signal for positive-drive driver switches
RXXX- Memory timing cont.	**Read** -- This signal is low for a read or clear sequence and high for a write or restore sequence
SASX- Memory timing cont.	**Sense Amplifier Strobe** -- Sent to the sense/inhibit card to produce SAS1 and SAS2
SAS1	**Sense Amplifier Strobe 1** -- Strobe signal for the sense amplifiers of memory data bits 0 through 7
SAS2	**Sense Amplifier Strobe 2** -- Strobe signal for the sense amplifiers of memory data bits 8 through 15
SBAX+ Processor control 2	**Sign Bit of A Register** -- Stores the sign bit of the A register for jump, multiply, and divide instructions
SBLX+ Processor control 2	**Select Bus Last Bit** -- Bit 15 on the S bus
SCMX+ Processor control 4	**Shift Count Met** -- Indicates that the count in the shift counter equals that in U register bits U0 to U4
SC0X+ to SC4X+ Processor control 4	**Shift Counter, Stages 0 to 4** -- Counts the shift cycles during multiply and divide instructions
SELA+ Processor control 1	**Select A Register** -- OUtput of the A REGISTER SELECT switch on the console; used to select the A register during step mode

620/L Mnemonics *(continued)*

Mnemonic	Description
SELB + Processor control 1	**Select B Register** -- Output of the B REGISTER SELECT switch on the console; used to select the B register during step mode
SELP + Processor control 1	**Select P Register** -- Output of the P REGISTER SELECT switch on the console; used to select the P register during step mode
SELU + Processor control 1	**Select U Register** -- Output of the U REGISTER SELECT switch on the console; used to select the U register during step mode
SELX + Processor control 1	**Select X Register** -- Output of the X REGISTER SELECT switch on the console; used to select the X register during step mode
SERX- Processor control 1	**Sense Response** -- Signal returned by a peripheral device to indicate the status of the device; occurs in response to a sense command
SETA + Processor control 3	**Set A Register** -- Clock used to set C bus data into the A register
SETB + Processor control 4	**Set B Register** -- Clock used to set C bus data into the B register
SETL + Processor control 4	**Set L Register** -- Clock used to set C bus data into the L register
SETP + Processor control 3	**Set P Register** -- Clock used to set C bus data into the P register
SETR + Processor control 3	**Set R Register** -- Clock used to set W bus data into the R register
SETU- Processor control 3	**Set U Register** -- Clock used to set W bus data into U register

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620/L Mnemonics *(continued)*

Mnemonic	Description
SETW+ Processor control 4	**Set W Register** -- Clock used to set C bus data into the W register
SETX+ Processor control 3	**Set X Register** -- Clock used to set C bus data into the X register
SGAX+ Processor control 4	**Shift Gate A** -- Provides bit 0 to the shift left gates of the arithmetic unit on shift left and multiply instructions
SGBX+ Processor control 4	**Shift Gate B** -- Provides bit 14 to the shift right gates of the arithmetic unit on shift right and multiply instructions
SGCX+ Processor control 4	**Shift Gate C** -- Provides bit 15 to the shift right gates of the arithmetic unit on shift right and multiply instructions
SGDX+ Processor control 4	**Shift Gate D** -- Provides bit 15 to the shift left gates on the arithmetic unit on shift left and divide instructions
SHCX+ Processor control 4	**Shift Control** -- Provides basic timing and control of the shift, multiply and divide instructions
SHFX- Processor control 4	**Shift** -- Enables shift operation of the shift, multiply and divide instructions
SHLX+ Processor control 4	**Shift Left** -- Enables the shift left gates on shift left and divide instructions
SHRX+ Processor control 4	**Shift Right** -- Enables all shift right gates for shift right and multiply instructions
SLAB+ Processor control 2	**Select Arithmetic Bus** -- Selects output of the adder to the C bus

620/L Mnemonics *(continued)*

Mnemonic	Description
SLAX + Processor control 3	**Select A Register** -- Gates the A register onto the S bus
SLBX + Processor control 3	**Select B Register** -- Gates the B register onto the S bus
SLGB + Processor control 2	**Select G Bus** -- Selects the G bus into the adder
SLPX + Processor control 3	**Select P Register** -- Gates the P register onto the S bus
SLP1 + Processor control 3	**Select P One** -- Signal used to enable INCR every time P is selected for normal update of P on each instruction
SLRI + Processor control 3	**Select R Inverted** -- Gates the output of R inverted to the G bus
SLRX + (DM111-3)	**Select R** -- Gates the output of the R register to the G bus
SLU1 + SLU2 + SLU3 + Processor control 3	**Select U** -- Selects the U register onto the G bus **SLU1 +** -- Selects U0-U8 **SLU2 +** -- Selects U9-U10 **SLU3 +** -- Selects U11-U15
SLXX + Processor control 3	**Select X Register** -- Gates the X register onto the S bus
SOP2 Processor control 1	**Step Pulse** -- Pulse initiated from the STEP switch on the console, allows one instruction to be performed

620/L Mnemonics *(continued)*

Mnemonic	Description
SOPX+ Processor control 1	**Stop** -- Provides control for the manual halt and step operations
SQP2- Memory timing cont.	**Loader Protection Step Control** -- Signal from loader protection circuit; when low, it causes the computer to go into step mode
SRSX+ Processor control 1	**Single Register Selected** -- Enables setting of MRSX when a single register is selected
SSAX+ Processor control 1	**Switch Select A Register** -- Flip-flop set up by the A register switch on the console; used to maually select the A register
SSBX+ Processor control 1	**Switch Select B Register** -- Manual selection of the B register from the console
SSLX- Driver/sink switch	**Stack Select** -- One of four stack select signals (SSL1-, SSL2-, SSL3-, SSL4-)
SSL1- Memory timing cont.	**Stack Select 1** -- Sent to the driver/sink switch card of the first 8K of memory
SSL2- Memory timing cont.	**Stack Select 2** -- Sent to the driver/sink switch card of the second 8K of memory
SSL3- Memory timing cont.	**Stack Select 3** -- Sent to the driver/sink switch card of the third 8K of memory
SSL4- Memory timing cont.	**Stack Select 4** -- Sent to the driver/sink switch card of the fourth 8K of memory
SSPX+ Processor control 1	**Switch Select P Register** -- Manual selection of the P register from the console
SSUX+ Processor control 1	**Switch Select U Register** -- Manual selection of the U register from the console

620/L Mnemonics *(continued)*

Mnemonic	Description
SSXX+ Processor control 1	**Switch Select X Register** -- Manual selection of the X register from the console
STB5- Processor control 3	**Set B Register** -- Pulse from the multiply/divide option used to set the B register
STEP+ Processor control 1	**Step Command** -- Output of the STEP switch on the console; used to initiate STEP mode
STP1 Processor control 3	**Set P Register** -- Output of set gates to select the P register
STRX+ Processor control 1	**Start** -- Provides control for manual step and run operations
SU00+ SU15+ Register card	**Sum 00 to 15** -- Output of the adder
SYRT-1 Processor control 1	**System Reset** -- Ground true signal in computer and on I/O bus to reset computer and I/O devices
S00X to S15X Sense/inhibit	**High Sense Bits 0 to 15** -- High lines to the differential inputs of the sense amplifiers
S00X- to S15X- Sense/inhibit	**Low Sense Bits 0 to 15** -- Low lines to the differential inputs of the sense amplifiers
TAIX- Processor control 4	**Trap Address Input** -- Signal from the DMA circuit (DM121) that selects the time when an address is inputted during a trap or interrupt operation
TCRX- AMED	**Timing and Control Reset** -- Reset to memory timing and control circuitry
TDIW- Processor control 4	**Trap Data In Write** -- Signal from the DMA circuit that initiates a write (WRTX+) signal to the memory on the second half cycle of trap in

620/L Mnemonics *(continued)*

Mnemonic	Description
TOSX Processor control 4	**Trap On Shift** -- Signal from the DMA circuit that detects and stores trap commands on shift, multiply, or divide instructions
TRSC Processor control 1	**Trap Start Clock** -- Signal from the DMA circuit that initiates a memory start pulse
TSHX Driver/sink switch	**Temperature Sense High** -- Signal from the high side of a sensistor
TSLX Driver/sink switch	**Temperature Sense Low** -- Signal from the low side of a sensistor
U00X + U15X + Register card	**U Register Bits 0 to 15** -- Provides storage of all instructions during the execute cycle
W00X + W15X + Register card	**Memory Data Register** -- Holds data for the memory read/write instructions
WRTX + Processor control 4	**Read/Write Command** a. Full cycle -- when true, enables clear/write operation of the memory; when false, enables read/restore operation b. Half Cycle -- When true, enables a write (only) operation; when false, enables a read (only) operation
WSTX- Memory timing cont.	**Write Sink Timing** -- Timing signal for X and Y write sink switches
XSOX to XS7X Driver/sink switch	**X Sink** -- Signals from X read or X write sink switches
YSOX to YS7X Driver/sink switch	**Y Sink** -- Signals from Y read or Y write sink switches

CHAPTER IX

WAVEFORMS

CHAPTER IX
WAVEFORMS

This chapter contains timing waveforms for various instructions and operations executed by the computer (figures IX-1 through IX-36).

Each drawing includes an identification of the instructions or operation involved, followed by waveforms of individual signals associated with the instructions or operation.

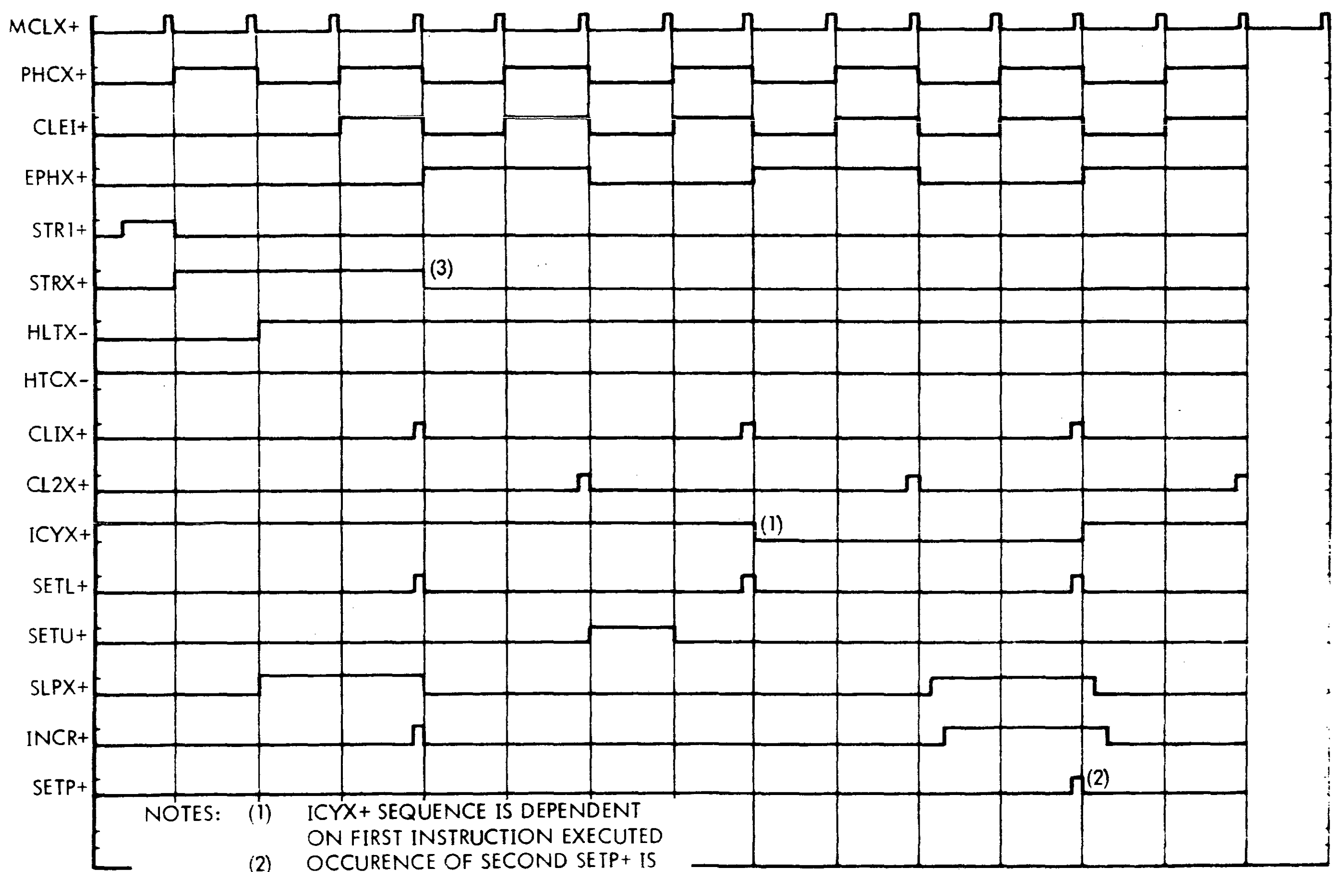
CHAPTER IX
WAVEFORMS

VT11-1403

INSTRUCTION: START SEQUENCE
MNEMONIC: (NONE) SINGLE - WORD
OCTAL CODE: (NONE) ADDRESSABLE
DIRECT-ADDRESSABLE

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTES:
(1) ICYX+ SEQUENCE IS DEPENDENT ON FIRST INSTRUCTION EXECUTED
(2) OCCURENCE OF SECOND SETP+ IS DEPENDENT ON INSTRUCTION
(3) RESETTING OF STRX+ IS DEPENDENT ON FIRST SETP+

NOTE: Distances along time scale are not proportionally accurate.

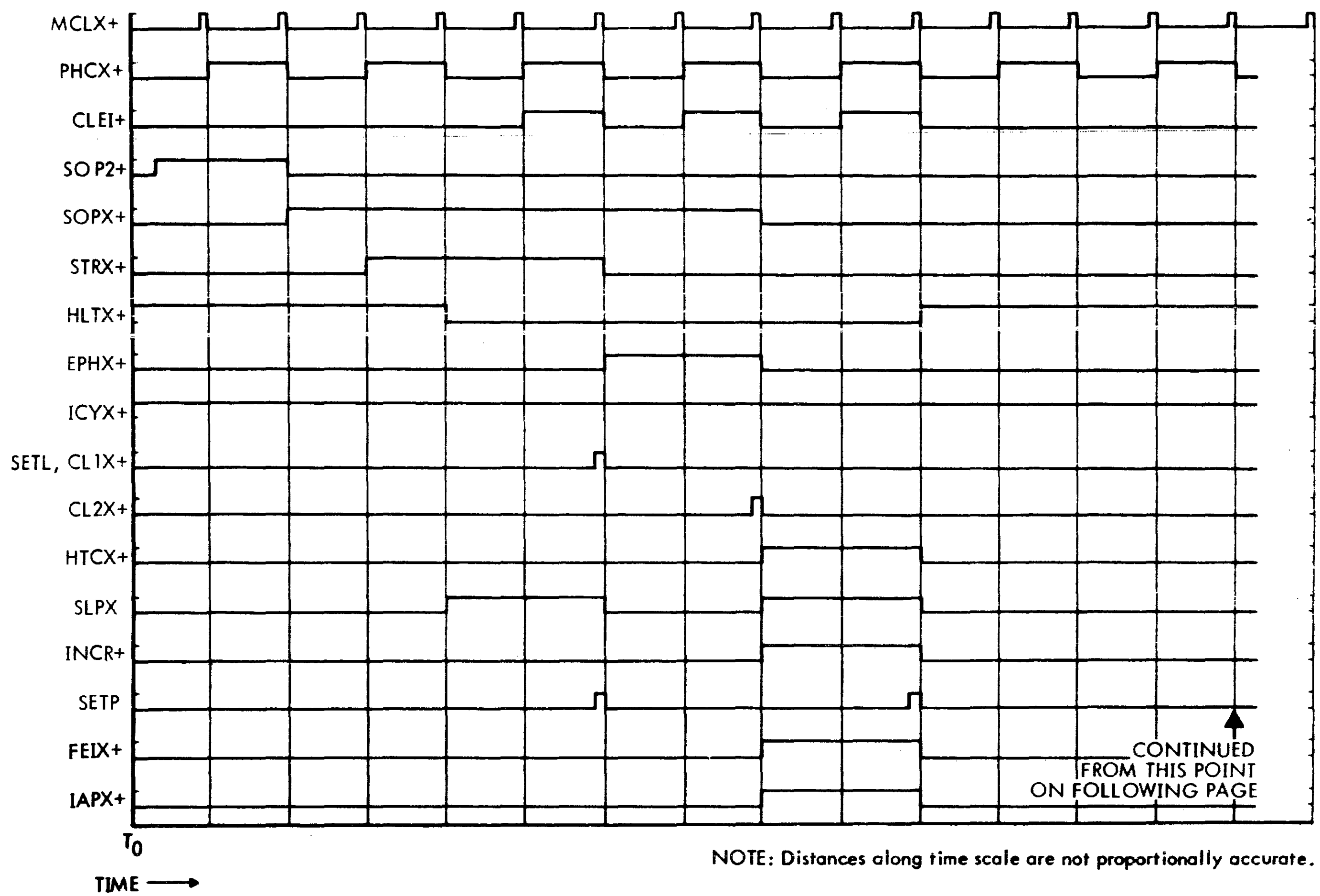
Figure IX-1. Start Sequence Timing

VTII-1404

INSTRUCTION: STEP SEQUENCE
MNEMONIC:(NONE)
OCTAL CODE:(NONE)
SINGLE - WORD ADDRESSABLE SHOWN

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



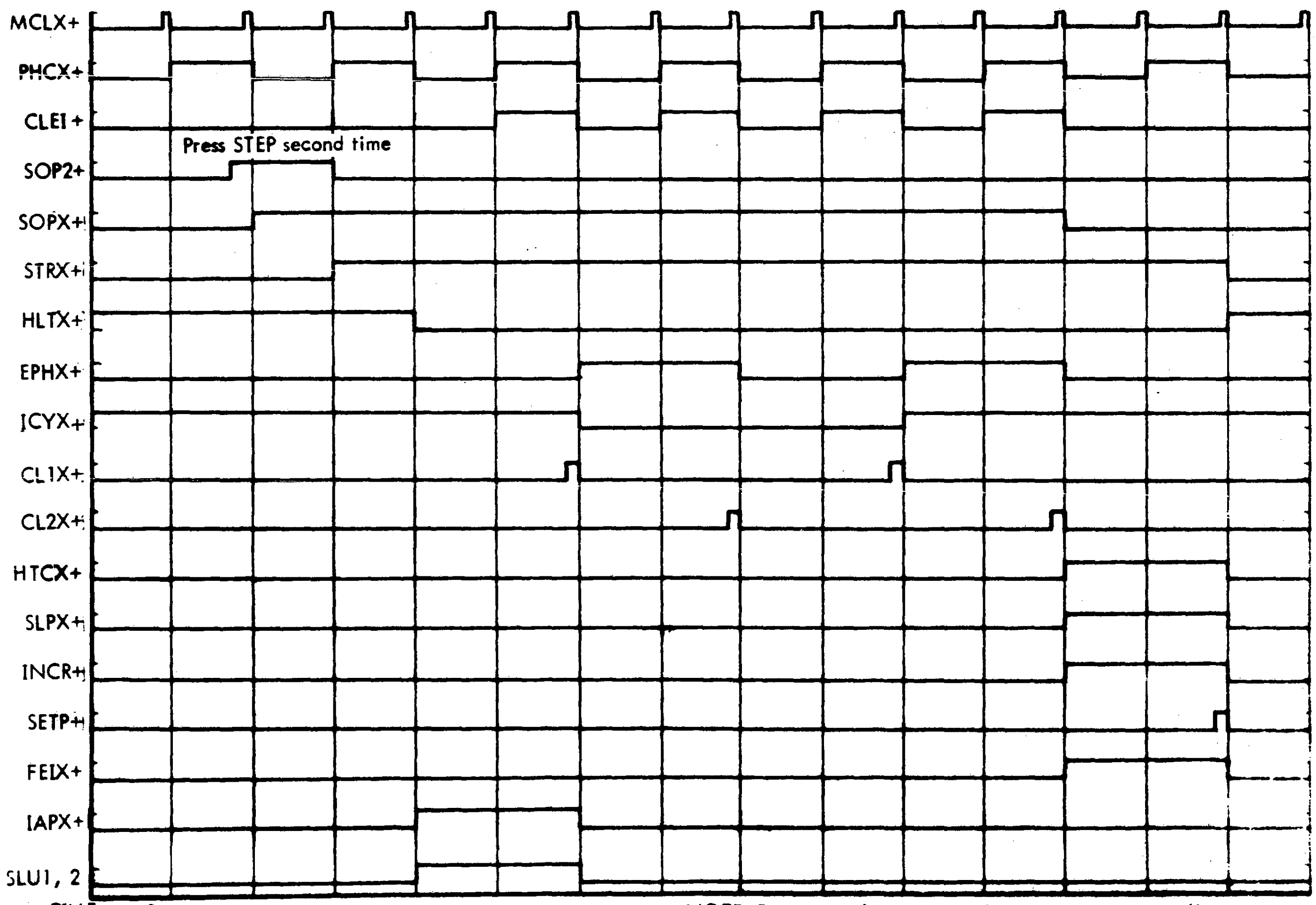
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-2. Step Sequence Timing

INSTRUCTION: STEP SEQUENCE **(CONT'D)**
MNEMONIC: **(NONE)**
OCTAL CODE: **(NONE)**

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



TIME → NOTE: Distances along time scale are not proportionally accurate.

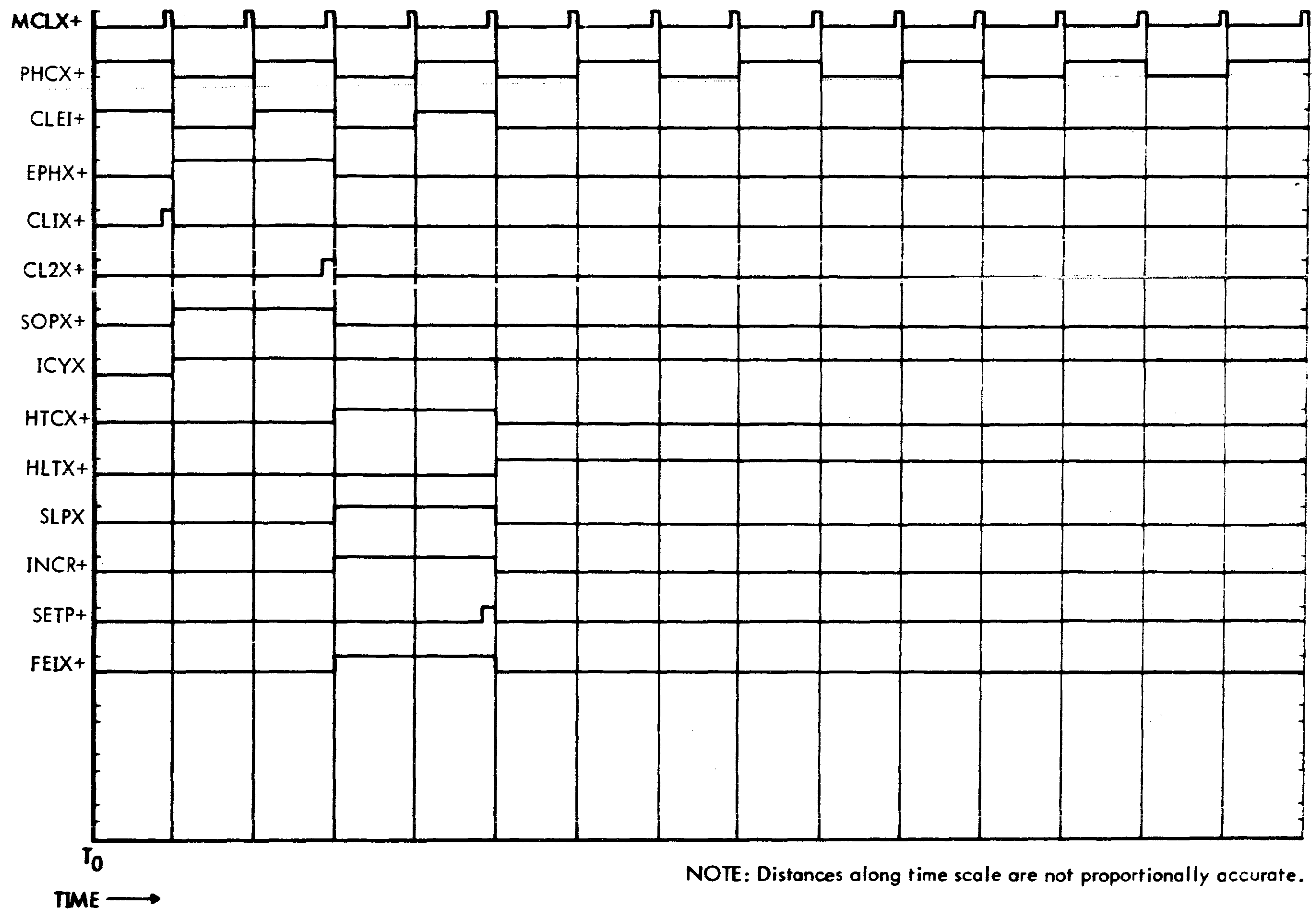
Figure IX-2. Step Sequence Timing (continued)

1111-1405

INSTRUCTION: MANUAL HALT SEQUENCE
MNEMONIC: (NONE)
OCTAL CODE: (NONE)

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



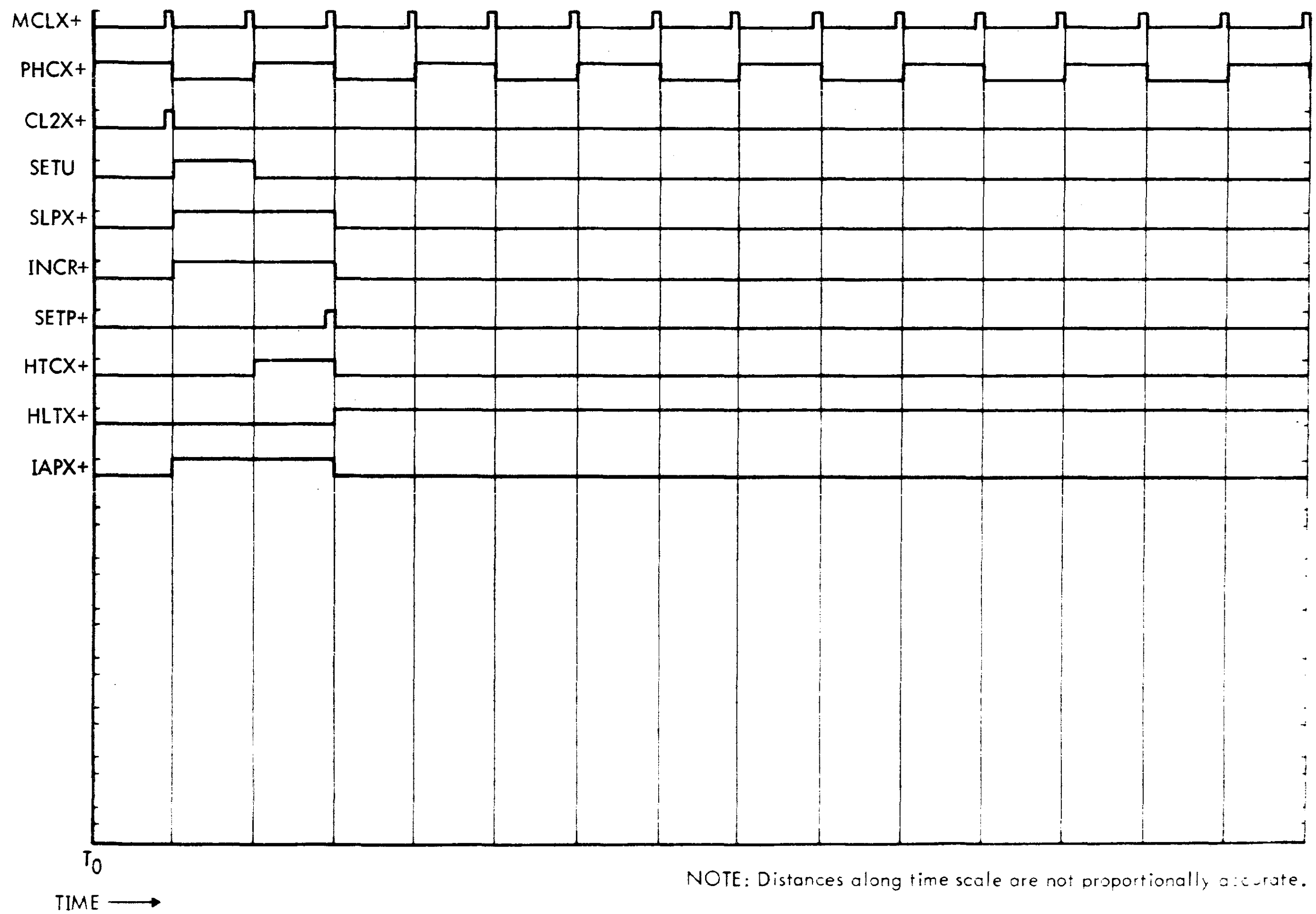
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-3. Manual Halt Sequence Timing

INSTRUCTION: PROGRAM HALT SEQUENCE
MNEMONIC: HLT
OCTAL CODE: 000XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



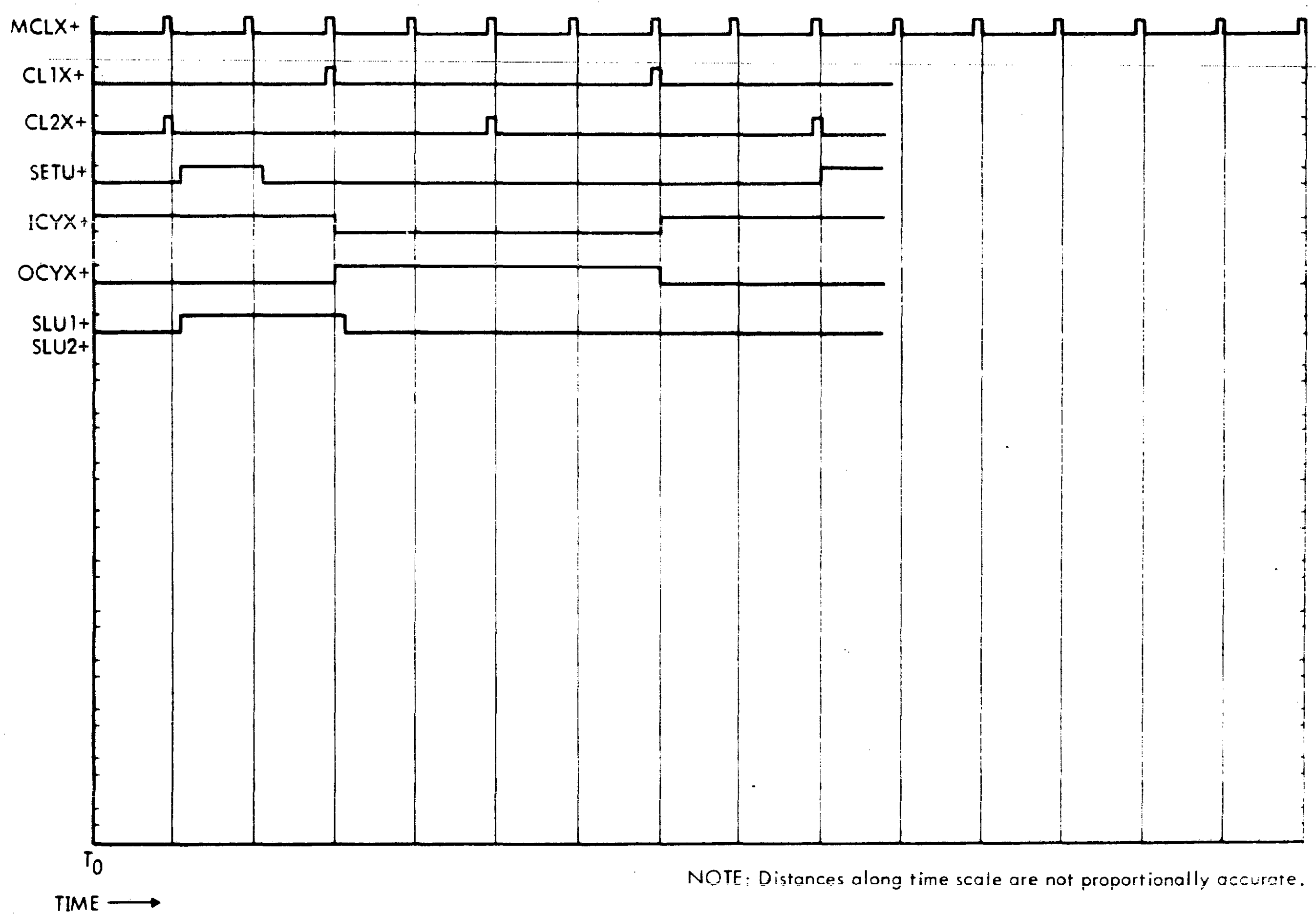
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-4. Program Halt Sequence Timing

INSTRUCTION: OPERAND ADDRESSING (DIRECT)
MNEMONIC: LDA DIRECT IS TYPICAL
OCTAL CODE: 01ZXXX (Z = $0XX_2$)

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



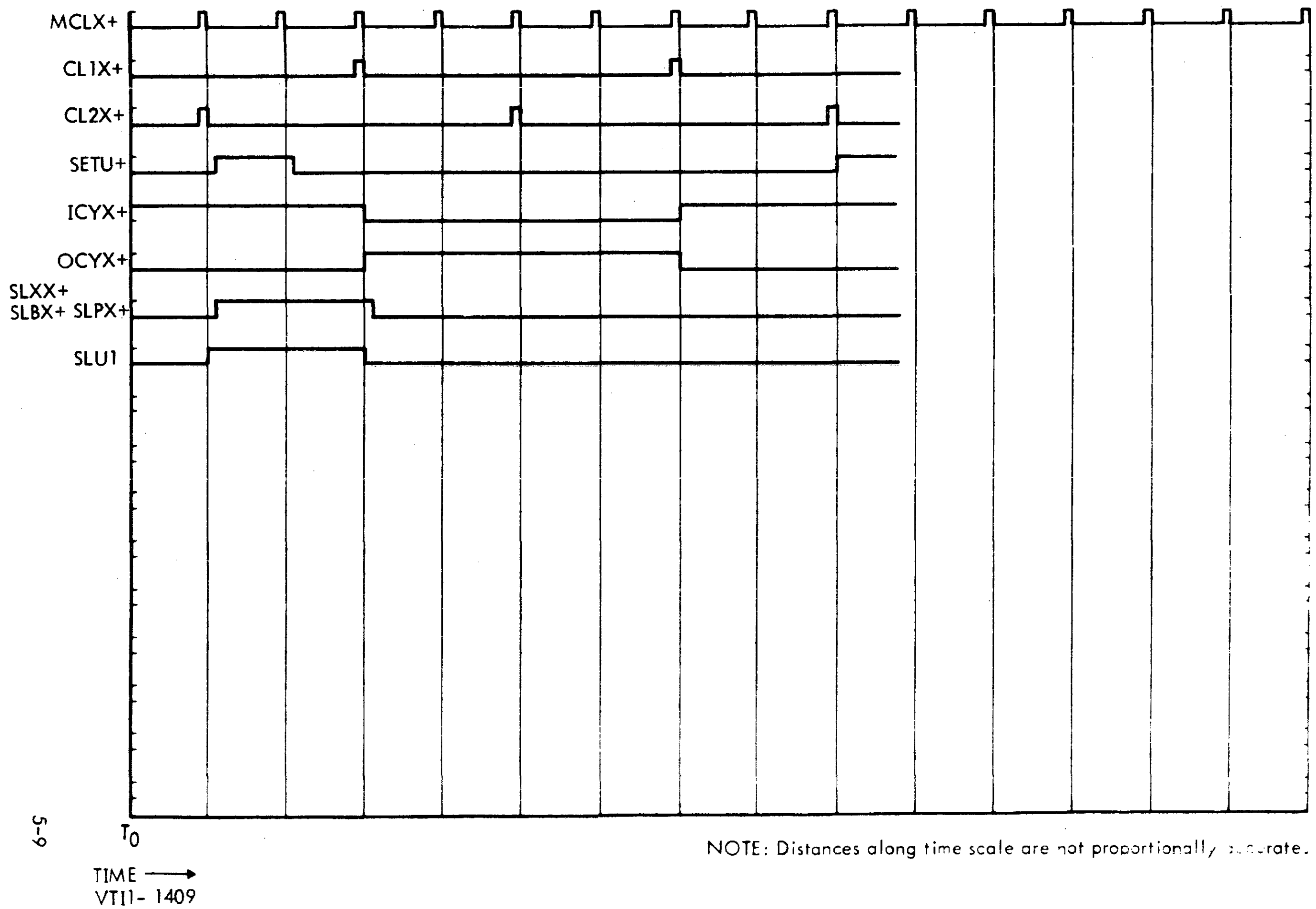
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-5. Operand Addressing (Direct) Timing

INSTRUCTION: INDEX AND RELATIVE ADDRESSING
MNEMONIC: LDA INDEXED IS TYPICAL
OCTAL CODE: 015XXX (INDEX X)
016XXX (INDEX B)
014XXX (RELATIVE TO P)

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

Figure IX-6. Index and Relative Addressing Timing

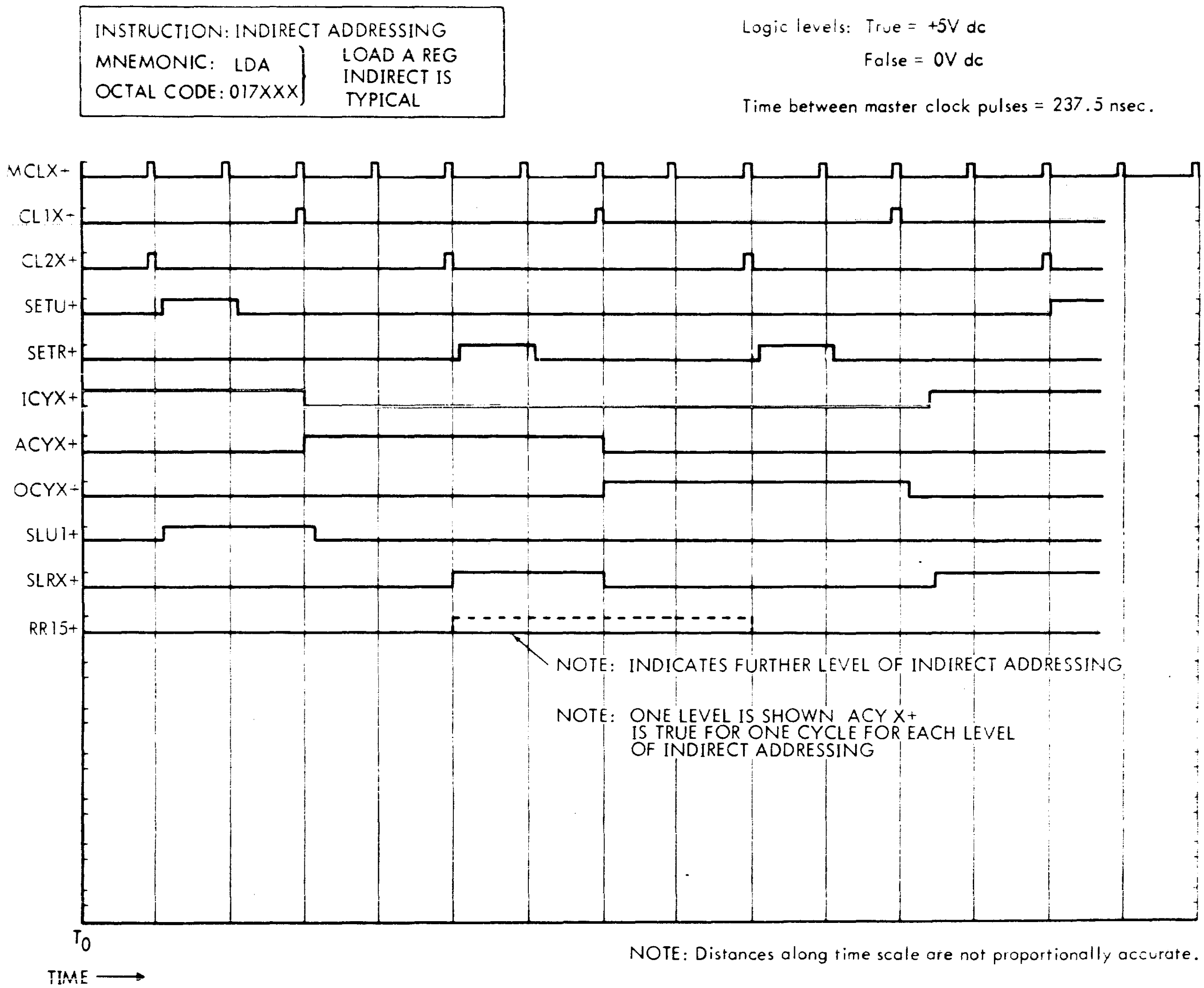


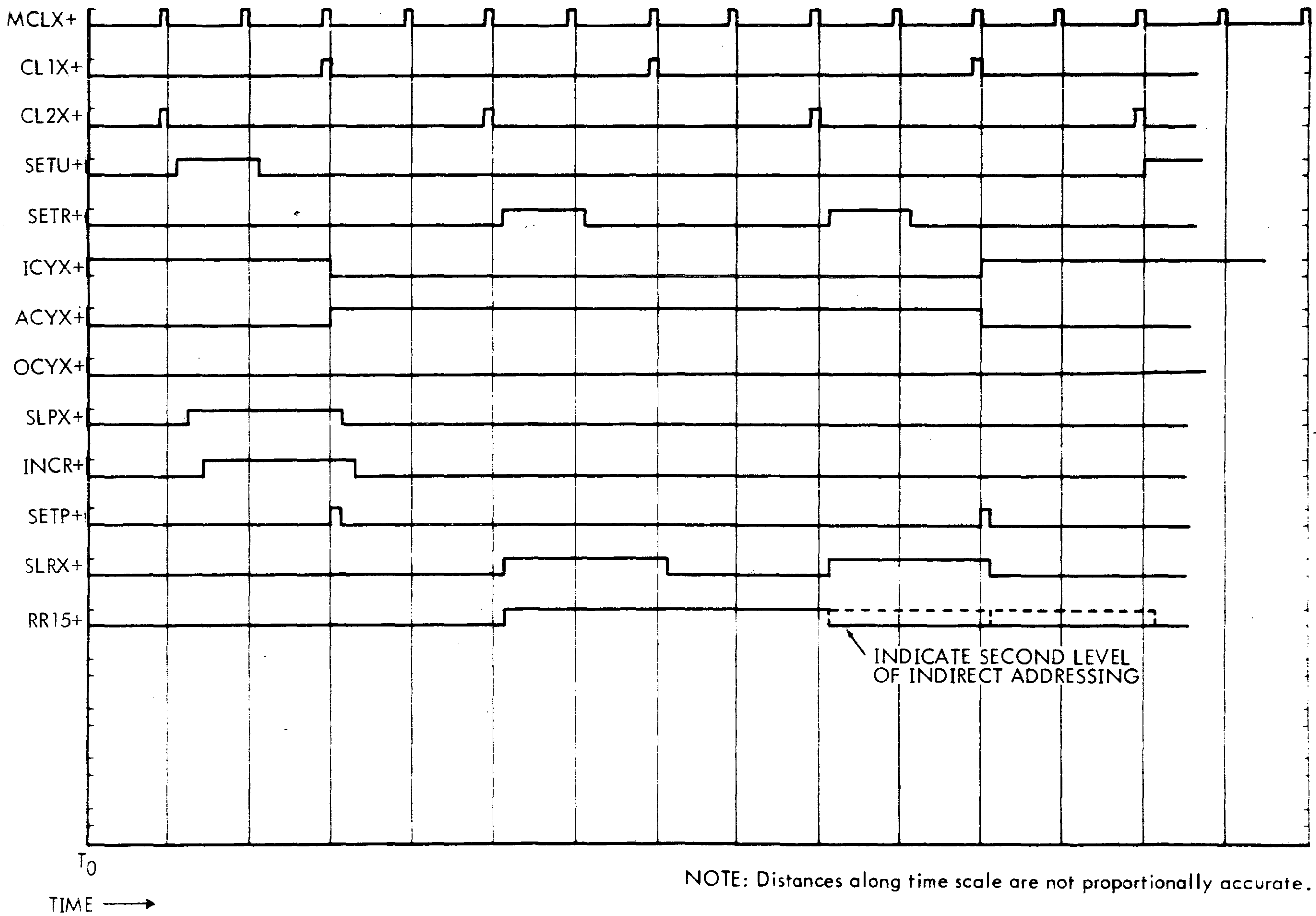
Figure IX-7. Indirect Addressing Timing

INSTRUCTION:	INDIRECT ADDRESSING DOUBLE-WORD INSTRUCTION
MNEMONIC:	JMP / JMP
OCTAL CODE:	001000 1XXXXX / UNCOND IS TYPICAL

Logic levels: True = +5V dc

False = 0V dc

Time between master clock pulses = 237.5 nsec.



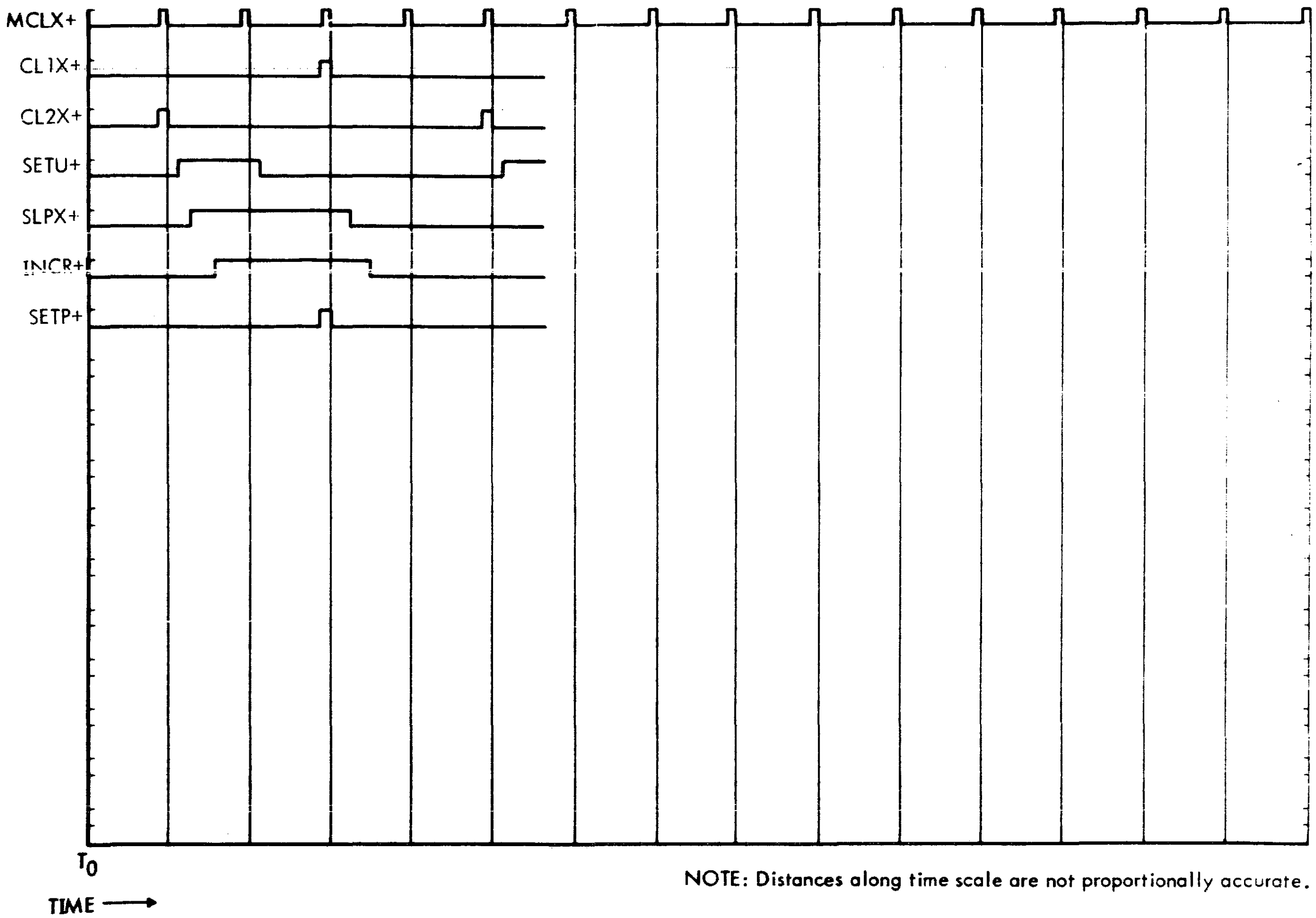
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-8. Indirect Addressing, Double-Word Instruction Timing

INSTRUCTION: NO OPERATION
MNEMONIC: NOP
OCTAL CODE: 005000

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



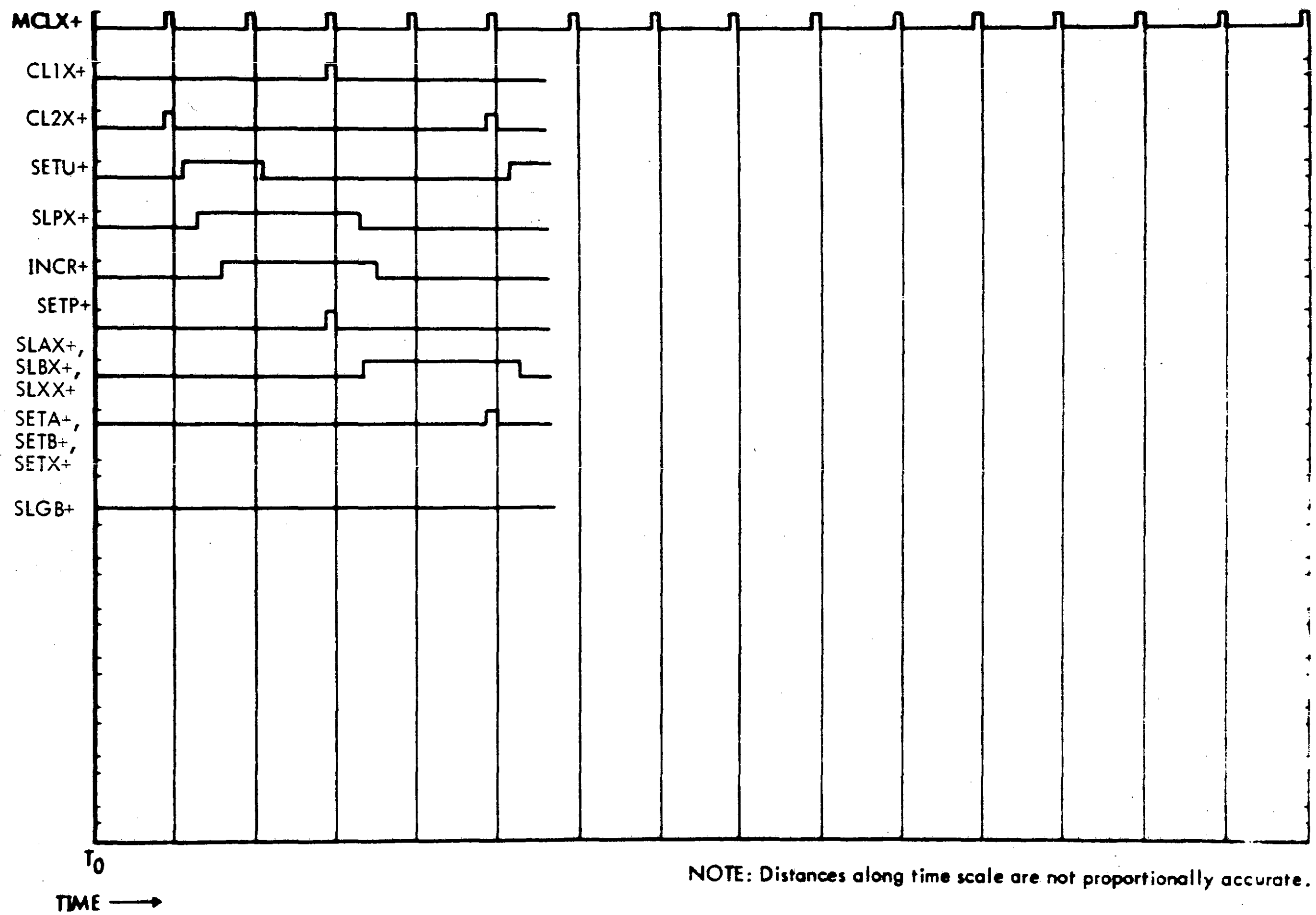
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-9. No Operation Timing

INSTRUCTION: REGISTER CHANGE (TRANSFER)
MNEMONIC: T - - (SEE SYSTEM REFERENCE MANUAL)
OCTAL CODE: 0050XX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

Figure IX-10. Register Change (Transfer) Timing

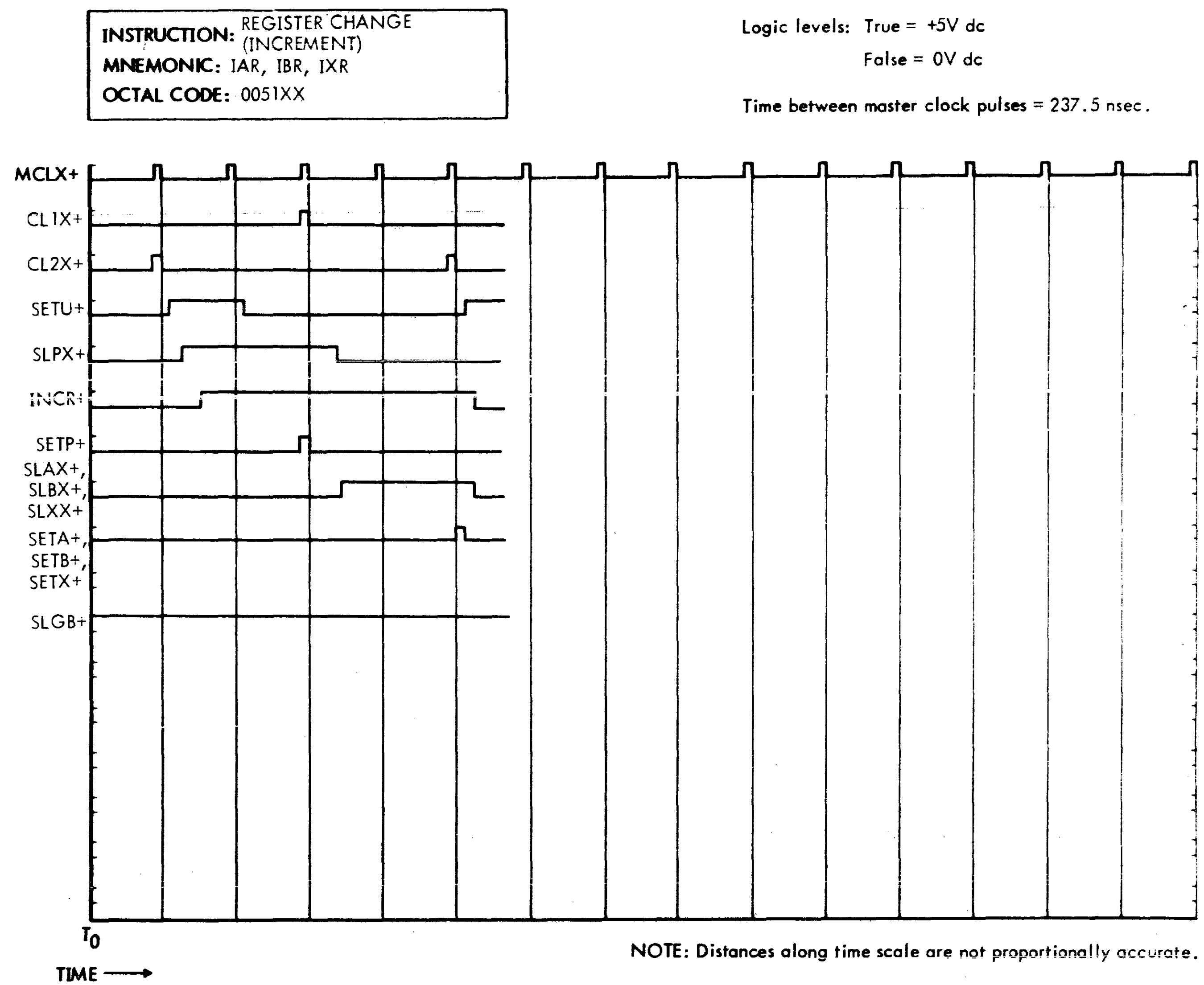


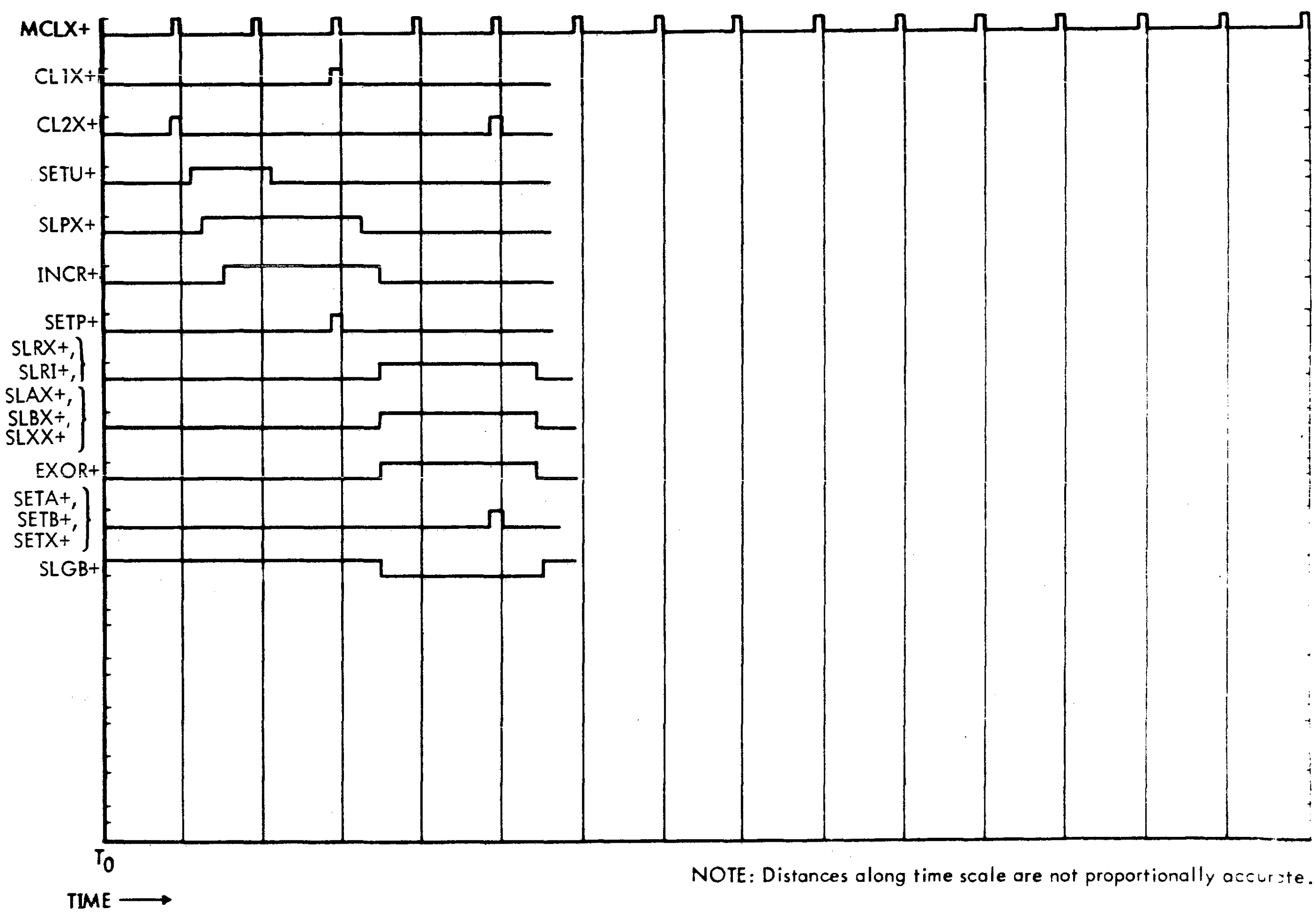
Figure IX-1.1. Register Change (Increment) Timing

VTII-1415

INSTRUCTION: REGISTER CHANGE (COMPLEMENT)
MNEMONIC: CPA, CPB, CPX
OCTAL CODE: 005211, 005222, 005244

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



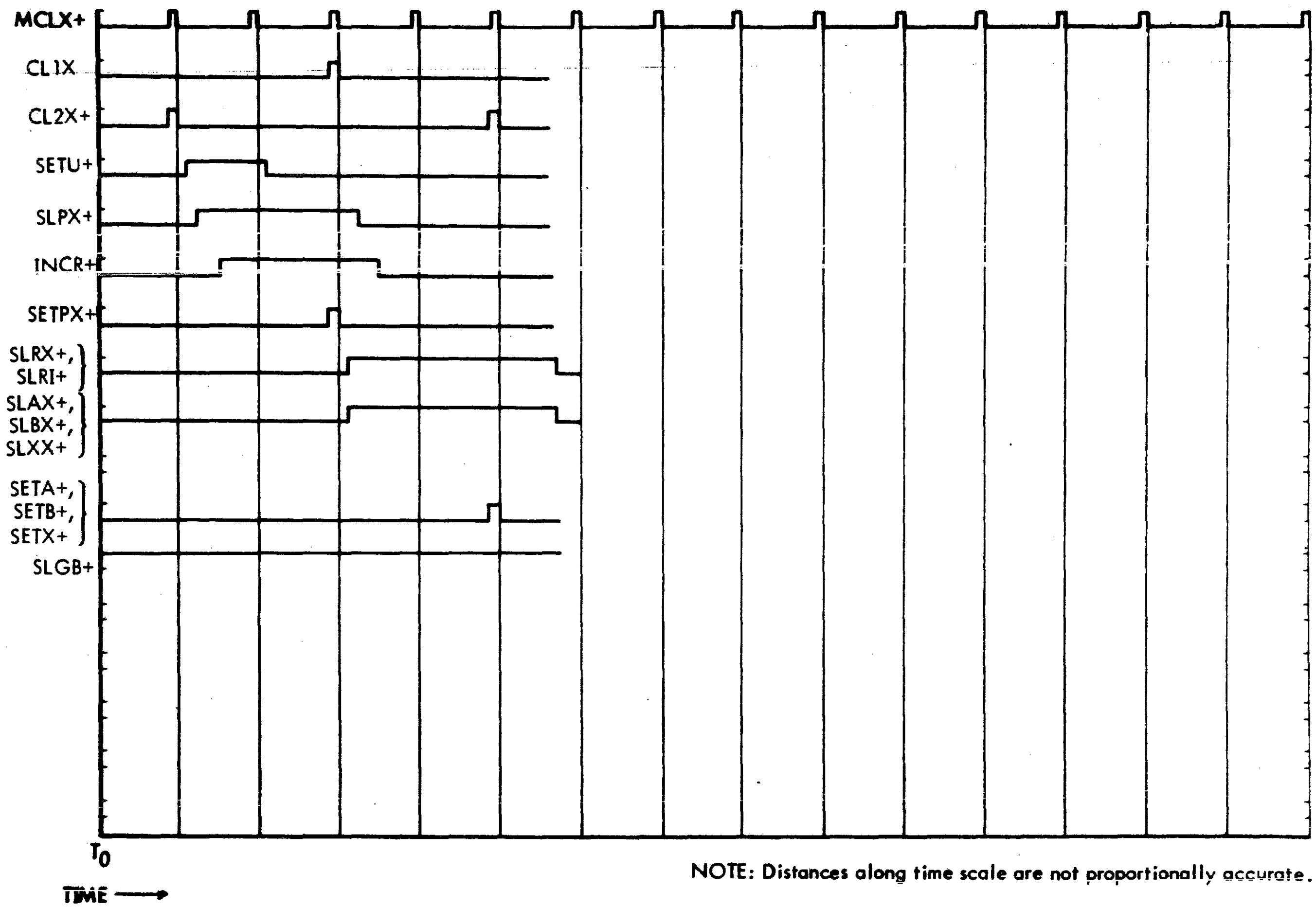
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-12. Register Change (Complement) Timing

INSTRUCTION: REGISTER CHANGE (DECREMENT)
MNEMONIC: DAR, DBR, DXR
OCTAL CODE: 005311 005322, 005344

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

Figure IX-13. Register Change (Decrement) Timing

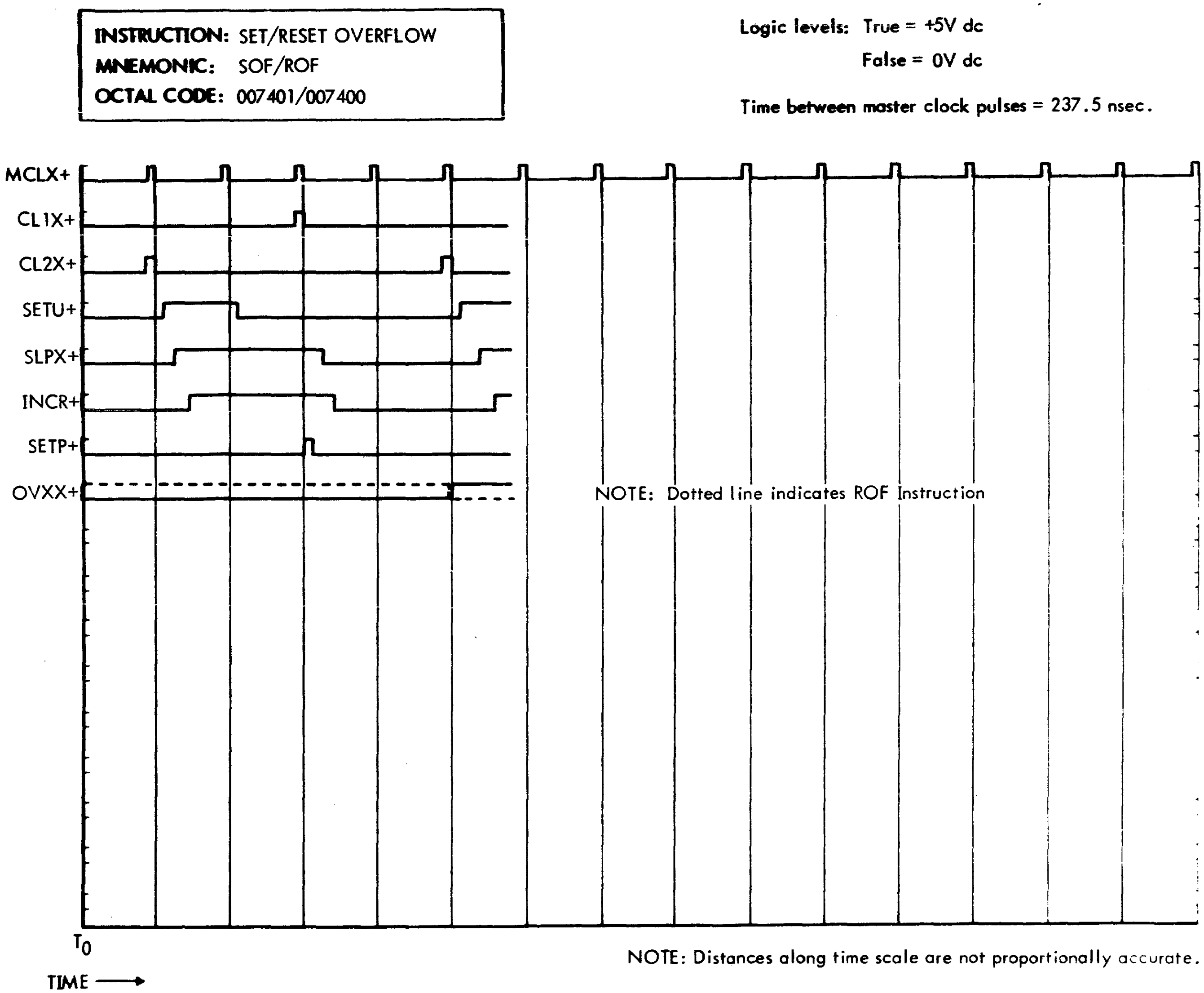


Figure IX-14. Set/Reset Overflow Timing

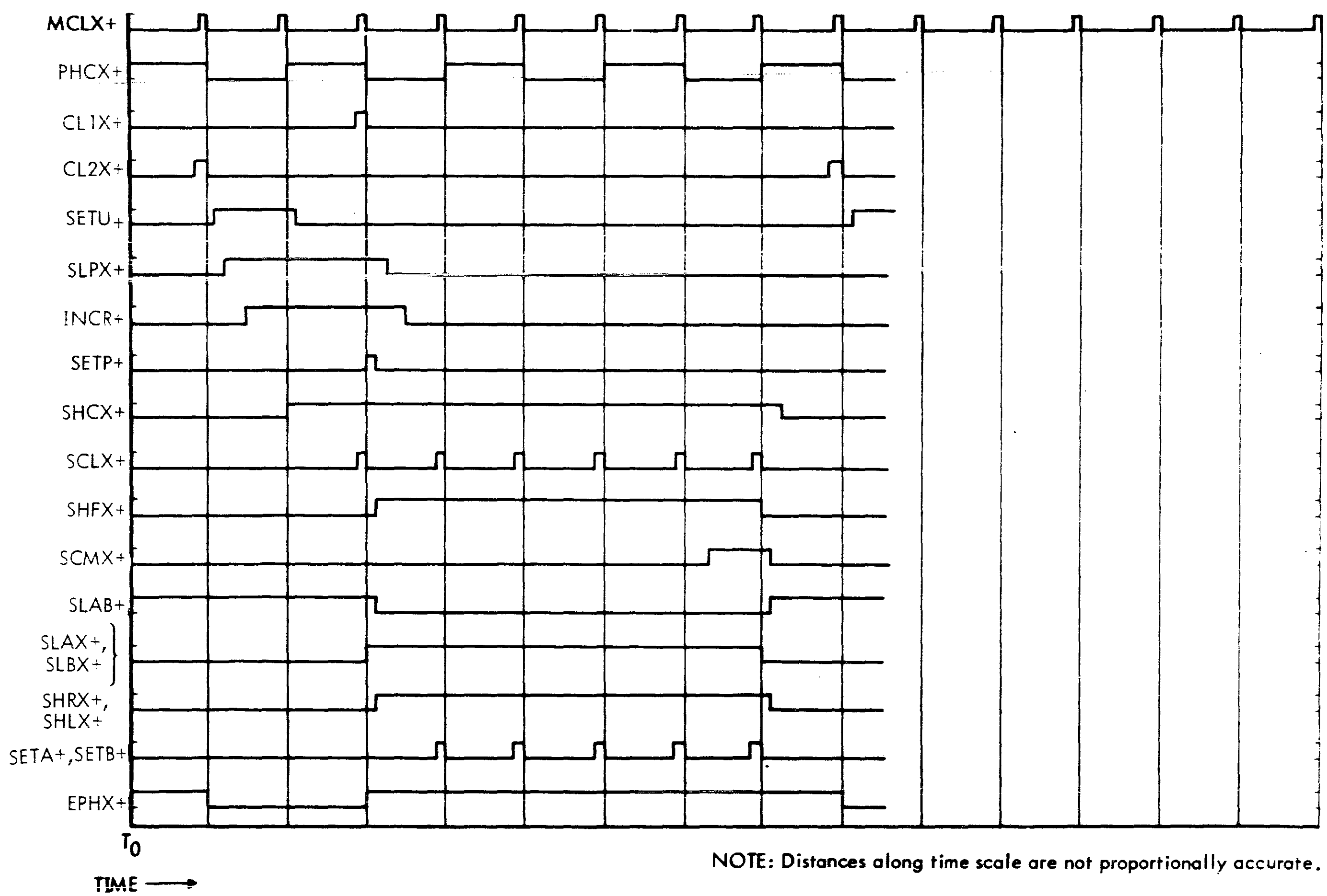
VTII-1418

INSTRUCTION: SHIFT SINGLE REGISTER
MNEMONIC: LRLA
OCTAL CODE: 004245

LOGICAL ROTATE LEFT A (5 PLACES) IS TYPICAL

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

Figure IX-15. Shift Single Register Timing

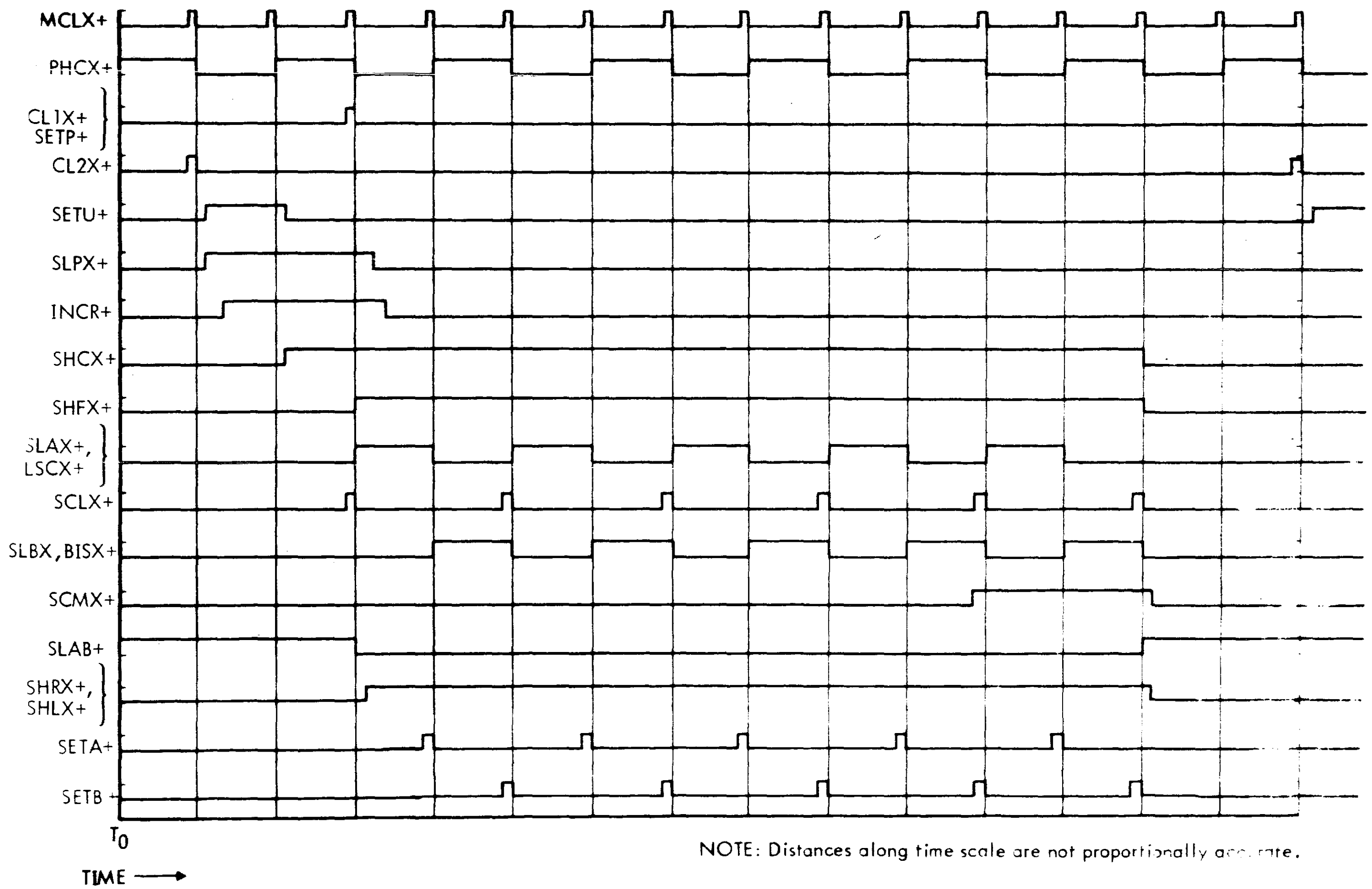
VTII-1419

INSTRUCTION: SHIFT DOUBLE REGISTER
MNEMONIC: LLRL
OCTAL CODE: 004445

} LONG LOGICAL ROTATE LEFT (5 PLACES) IS TYPICAL

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses – 237.5 nsec.



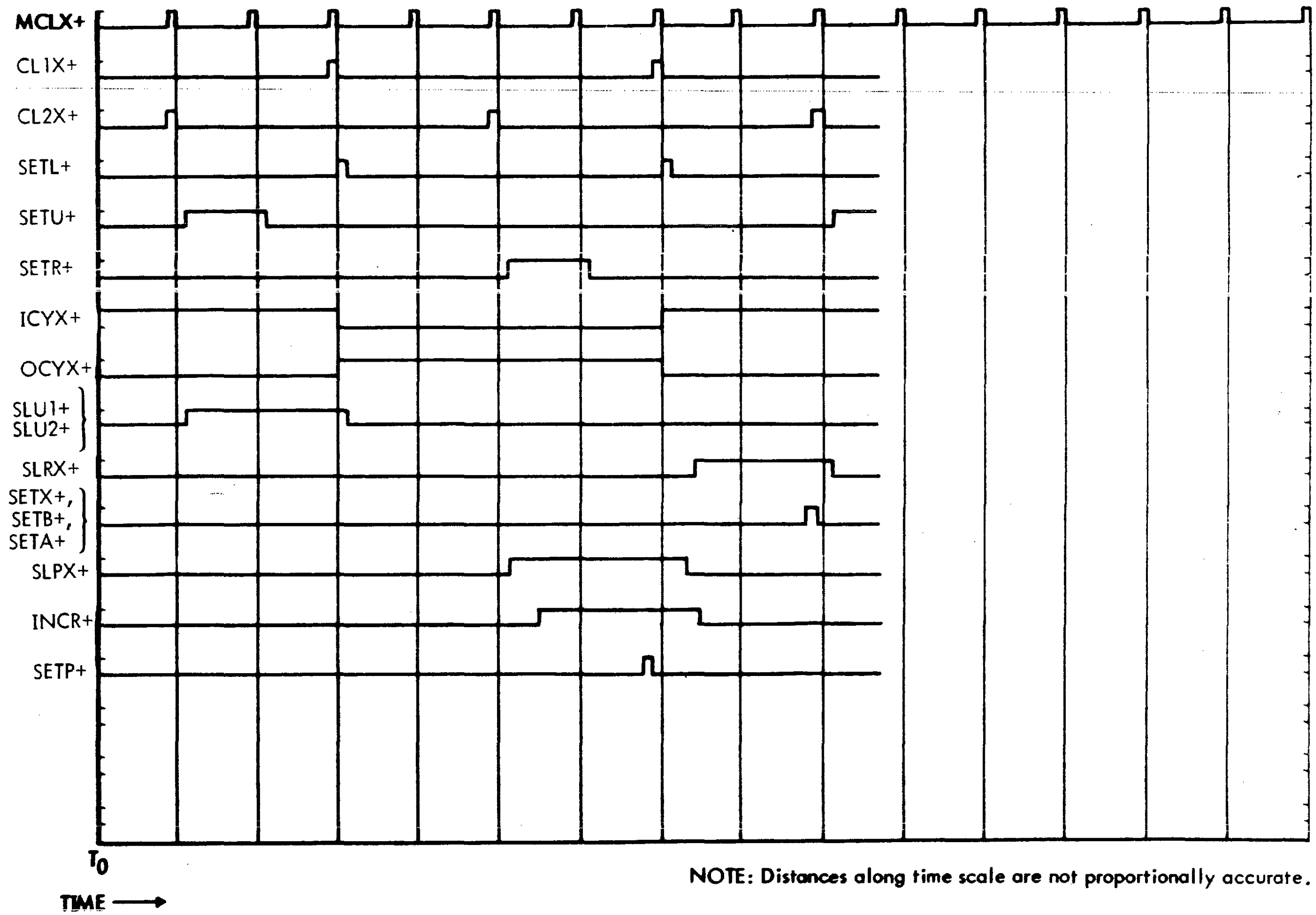
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-16. Shift Double Register Timing

INSTRUCTION: LOAD A (B,X) REGISTER
MNEMONIC: LDA (LDB, LDX)
OCTAL CODE: 010XXX (020XXX, 030XXX)

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



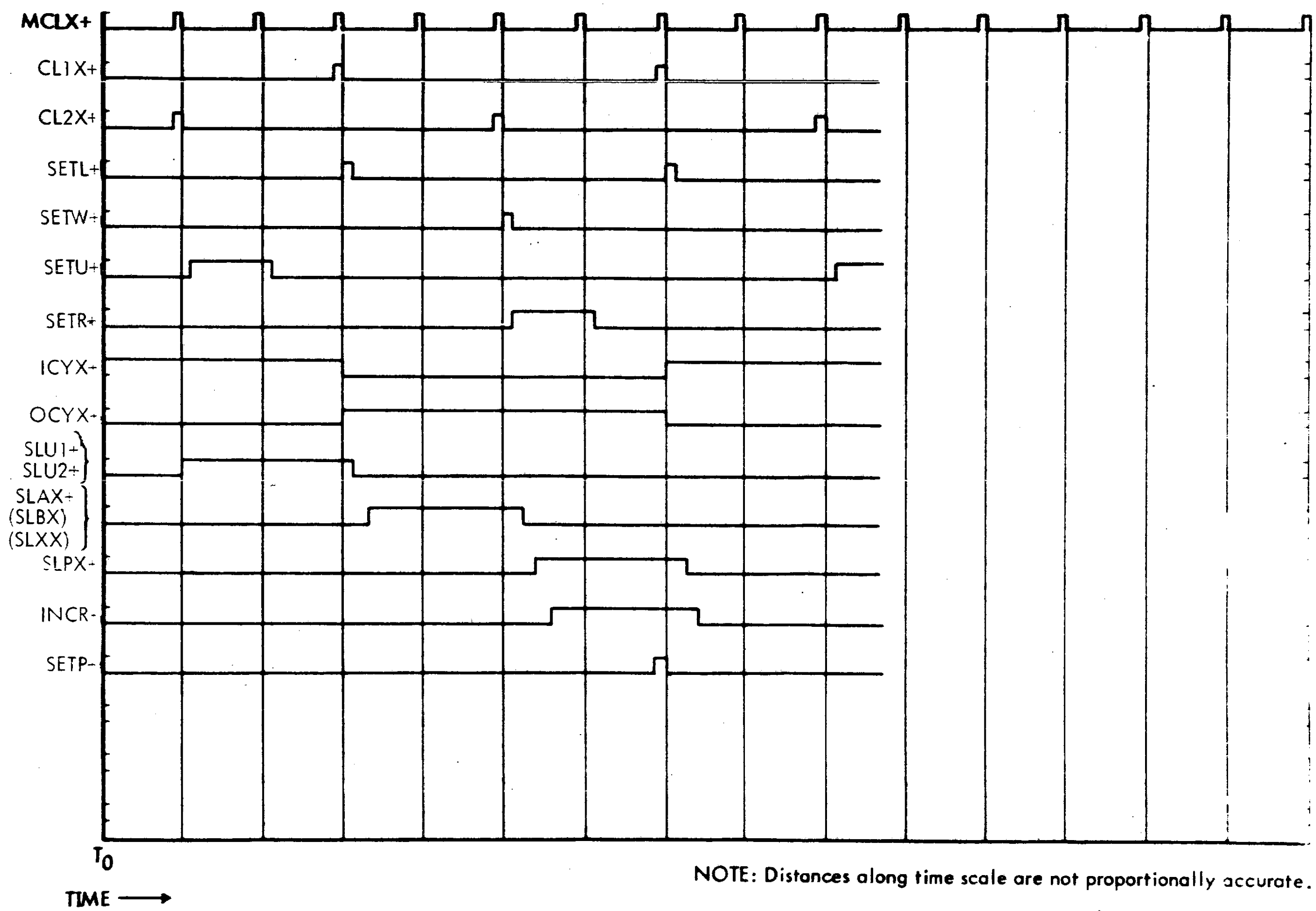
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-17. Load A (B, X) Register Timing

INSTRUCTION: STORE A (B, X) REGISTER
MNEMONIC: STA (STB, STX)
OCTAL CODE: 050XXX (060XXX, 070XXX)

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

Figure IX-18. Store A (B, X) Register Timing

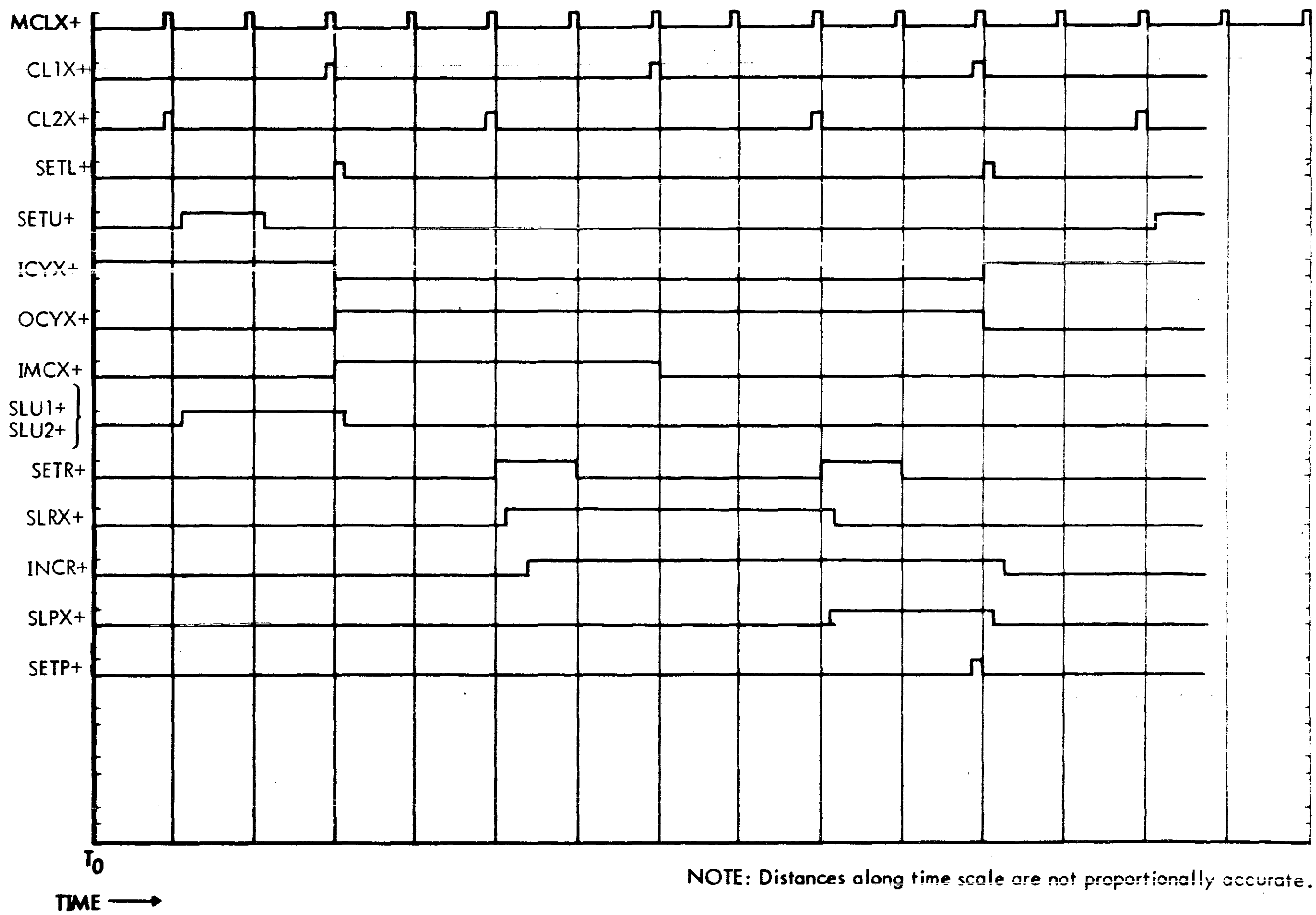
VTII-1421

VTII-1422

INSTRUCTION: INCREMENT AND REPLACE
MNEMONIC: INR
OCTAL CODE: 040XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

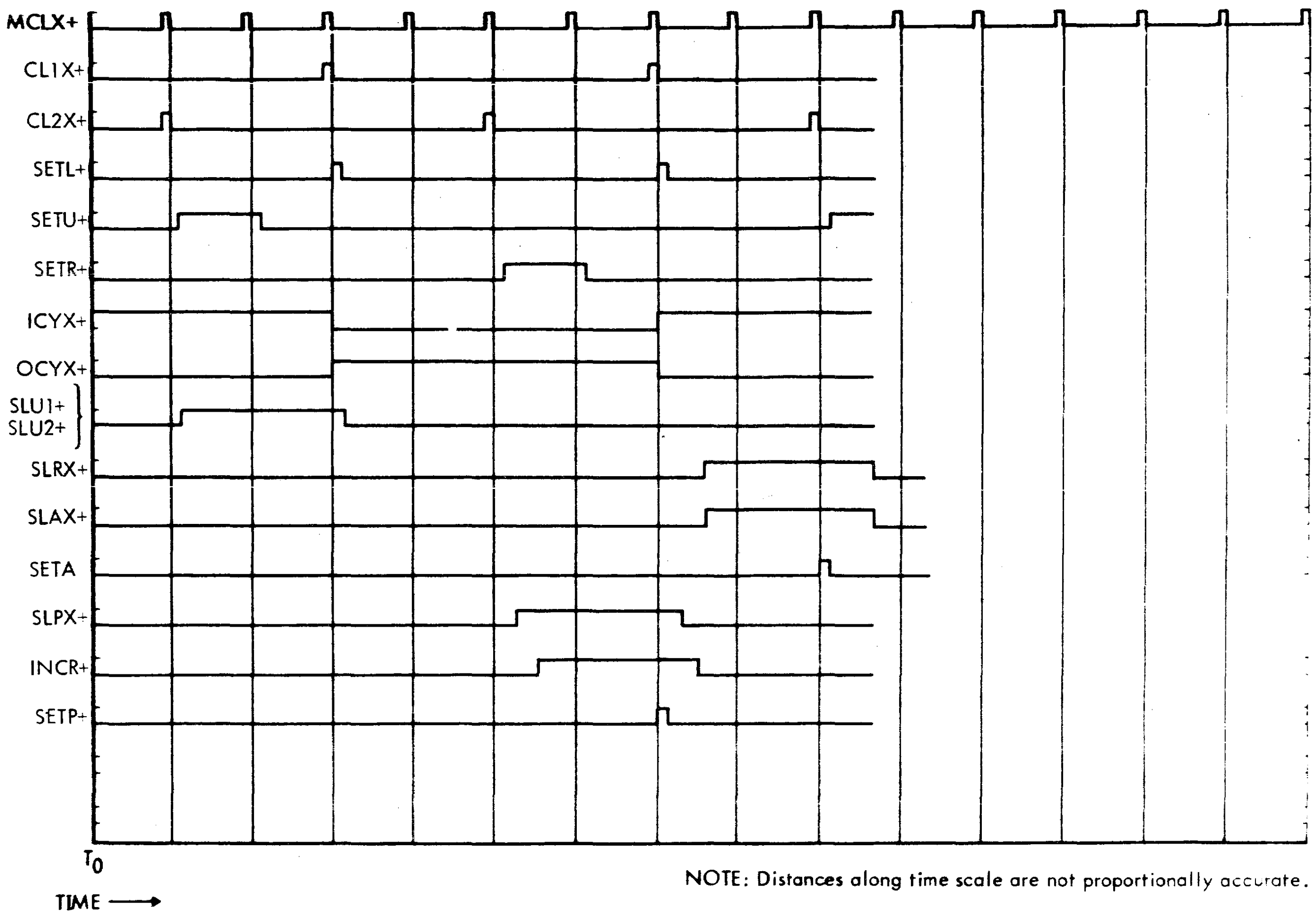
Figure IX-19. Increment and Replace Timing

VT11-1423

INSTRUCTION: ADD TO A REGISTER
MNEMONIC: ADD
OCTAL CODE: 120XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

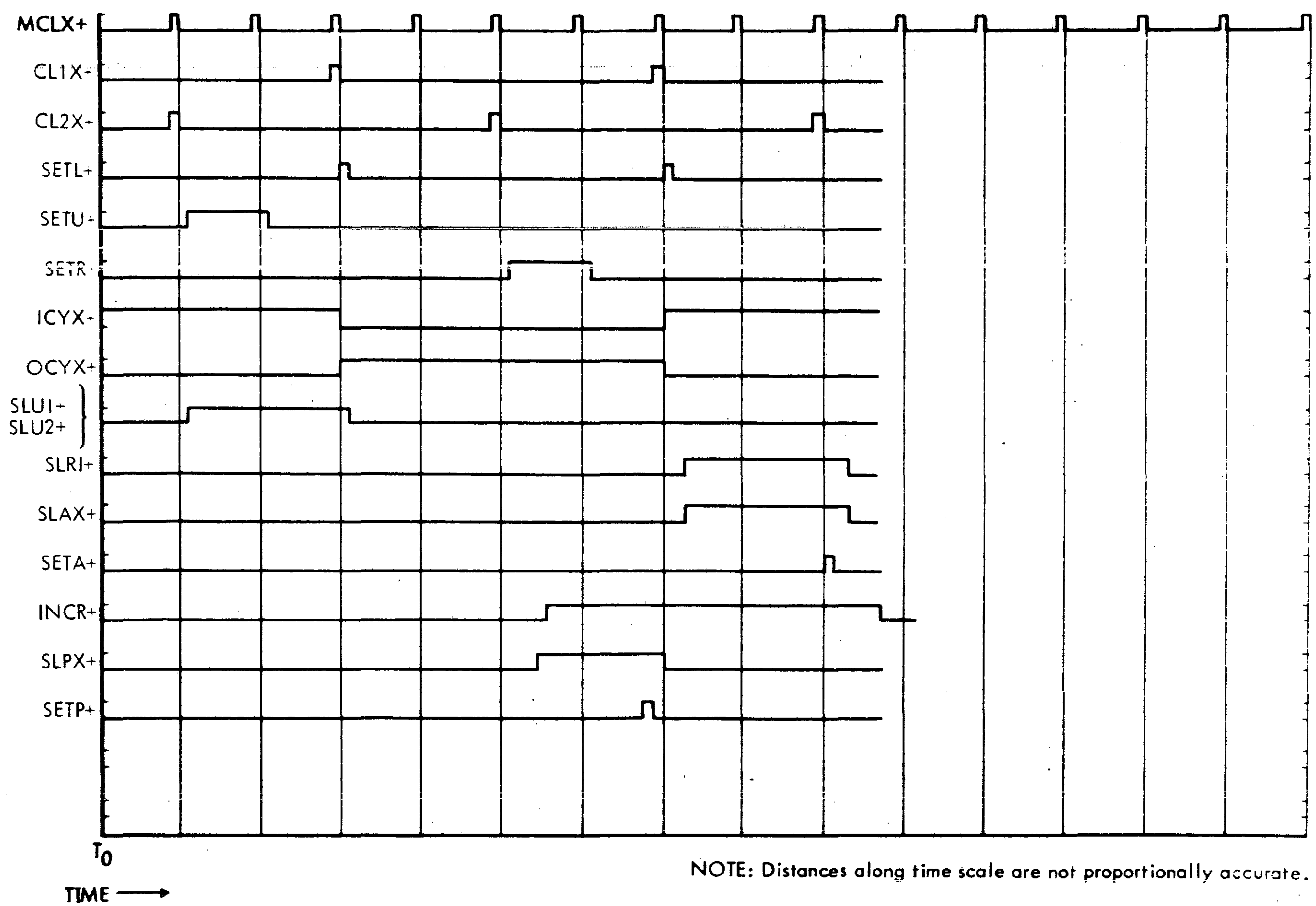
Figure IX-20. Add To A Register Timing

1111-1424

INSTRUCTION: SUBTRACT FROM A REGISTER
MNEMONIC: SUB
OCTAL CODE: 140XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



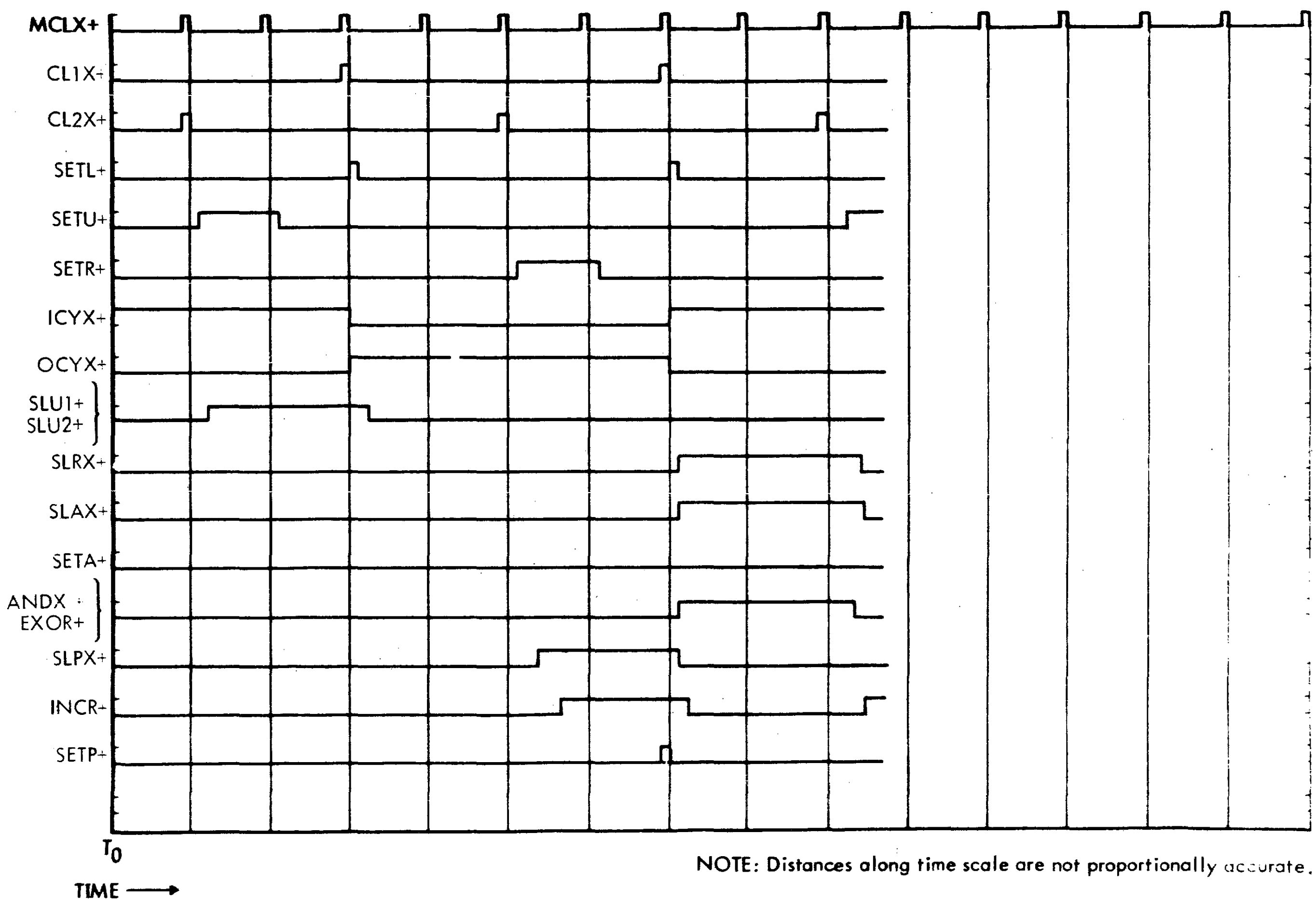
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-21. Subtract From A Register Timing

INSTRUCTION: INCLUSIVE OR TO A REGISTER
MNEMONIC: ORA
OCTAL CODE: 110XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

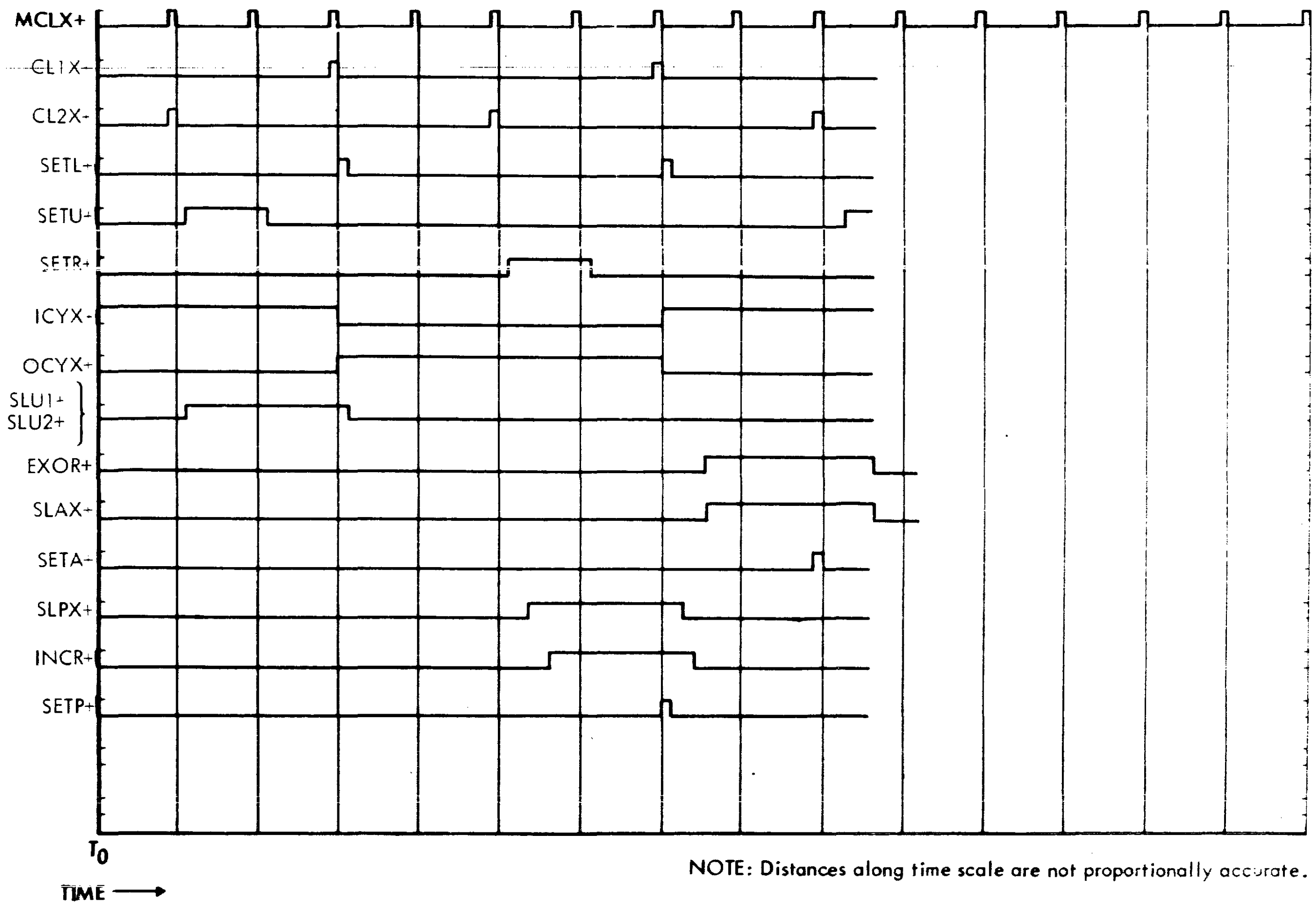
Figure IX-22. Inclusive-OR To A Register Timing

VT11-1425

INSTRUCTION: EXCLUSIVE OR TO A REGISTER
MNEMONIC: ERA
OCTAL CODE: 130XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



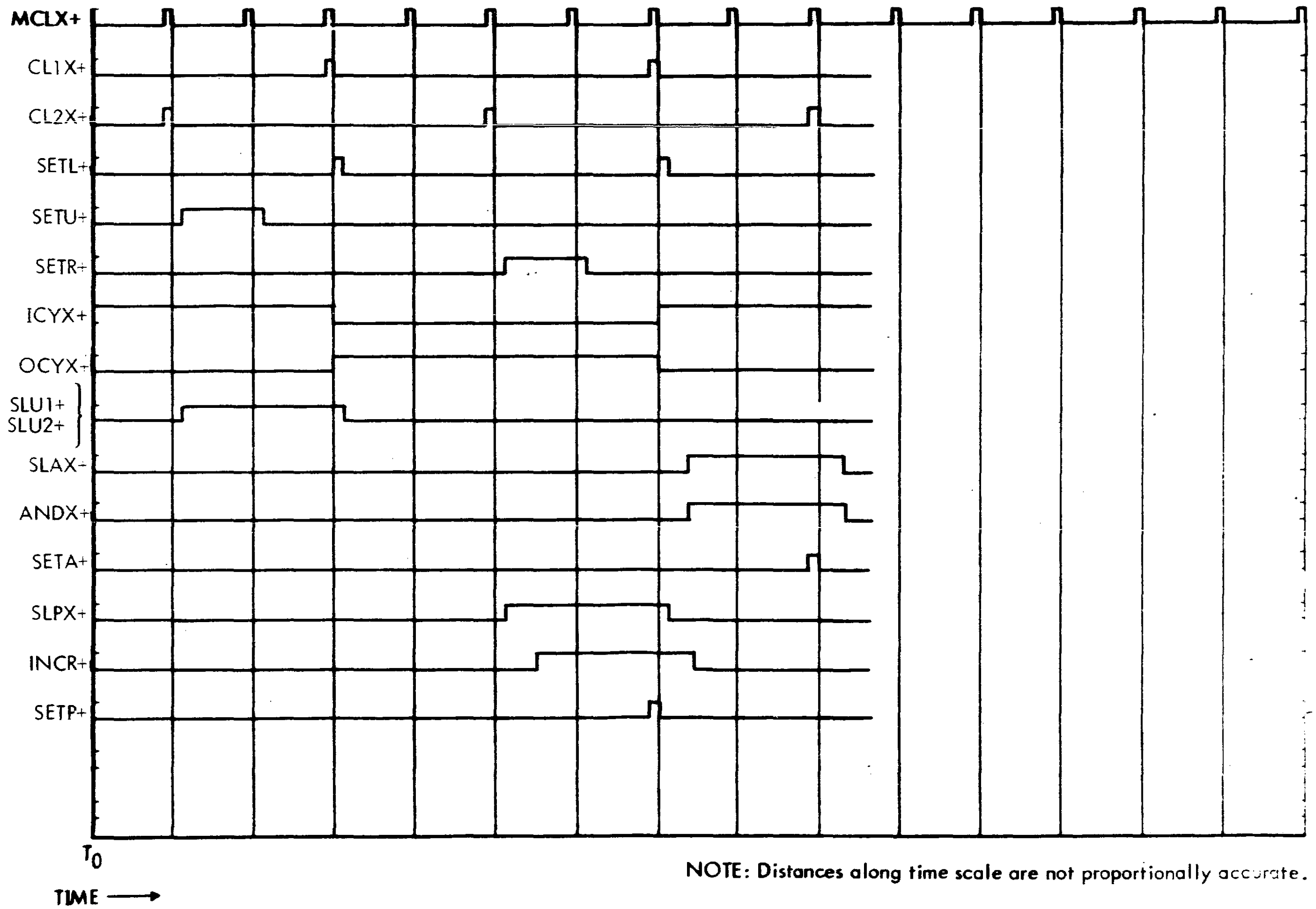
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-23. Exclusive-OR To A Register Timing

INSTRUCTION: AND TO A REGISTER
MNEMONIC: ANA
OCTAL CODE: 150XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

VTII-1427

Figure IX-24. AND to A Register Timing

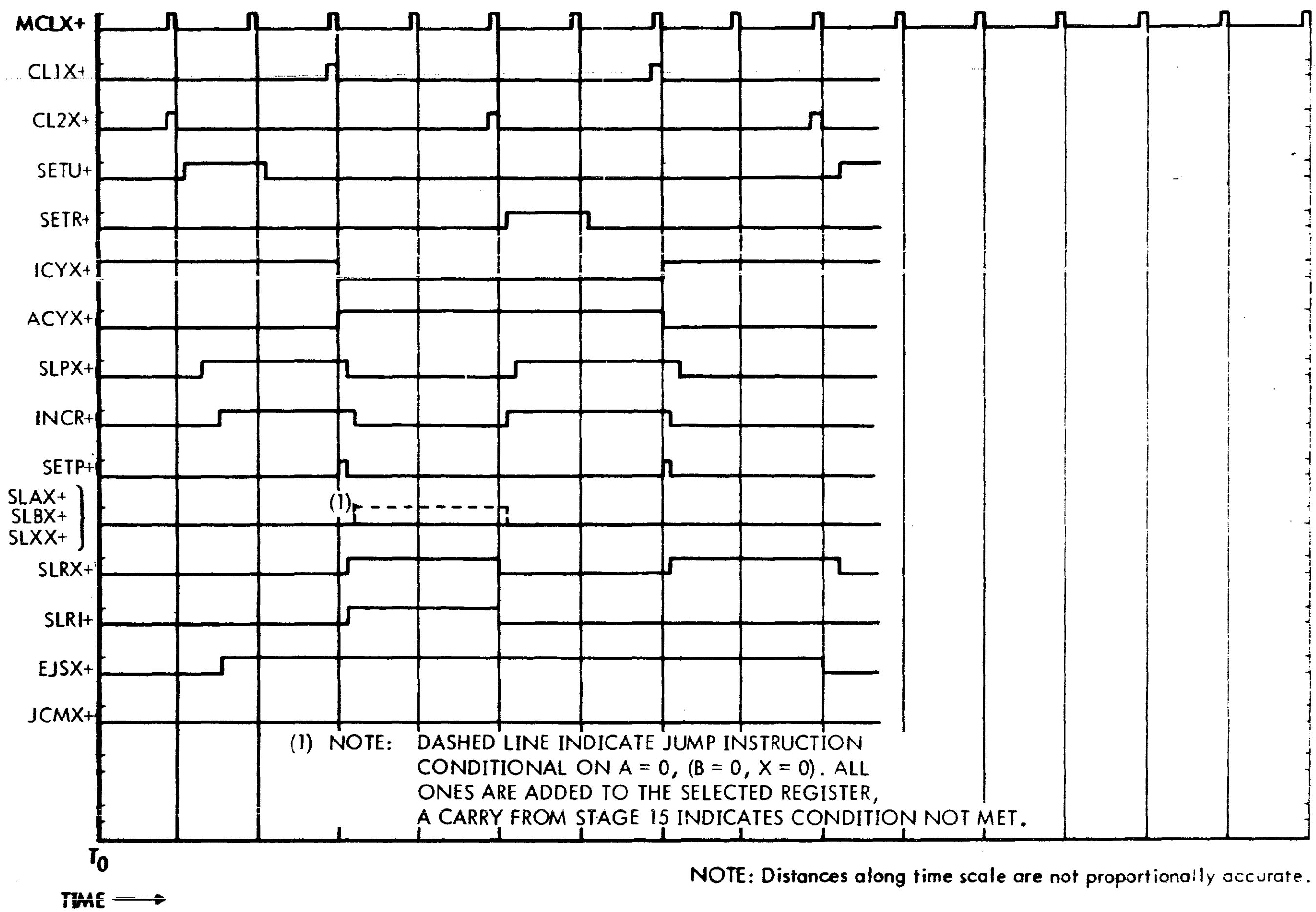
INSTRUCTION: JUMP CONDITION NOT MET, JUMP-AND-MARK CONDITION NOT MET, EXECUTE CONDITION NOT MET

MNEMONIC: JMP, JMPM, XEC

OCTAL CODE: 001XXX 002XXX 003XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

1711-1428

Figure IX-25. Jump, Jump-and-Mark Or Execute Condition Not Met Timing

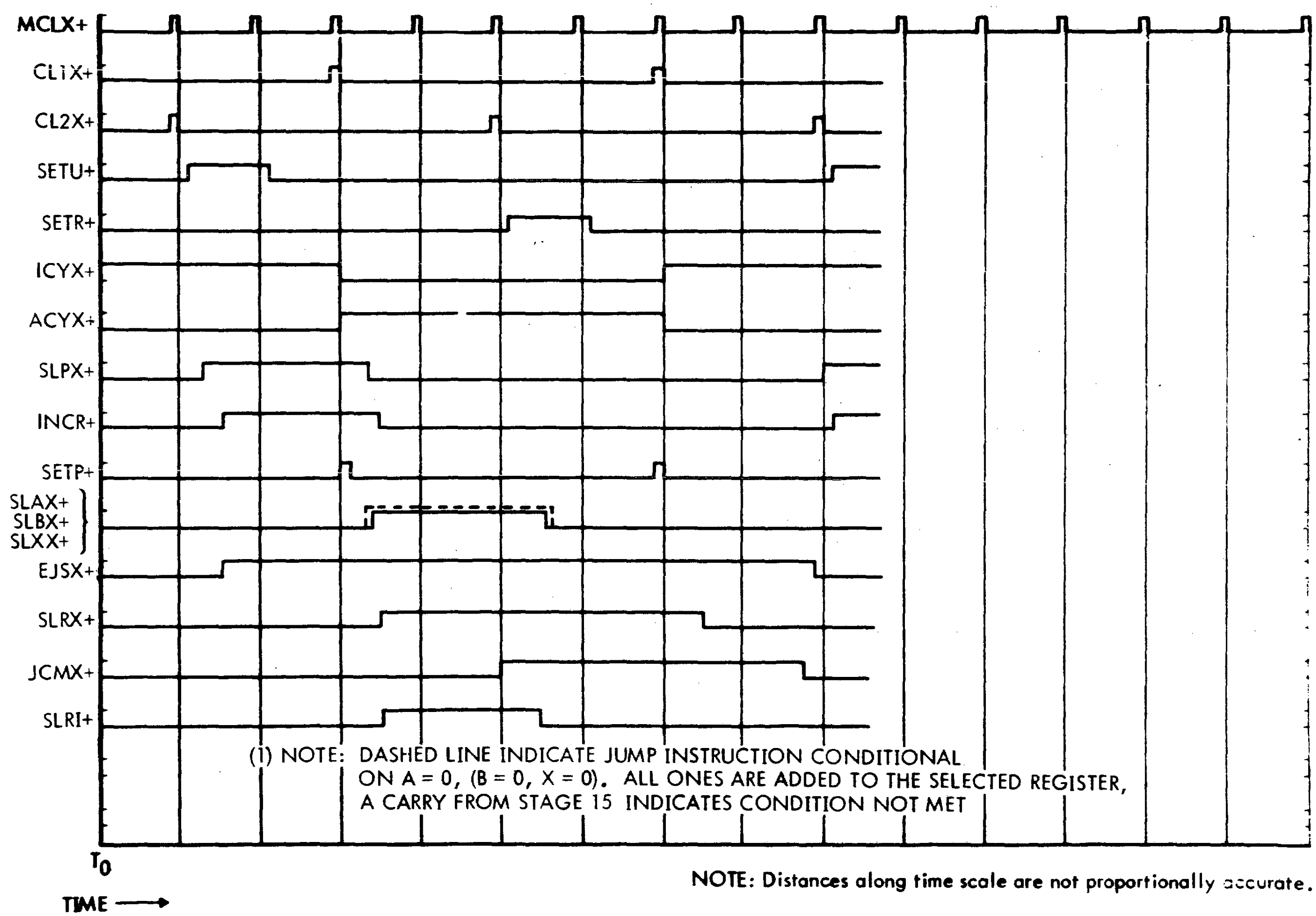
VTII-1429

INSTRUCTION: JUMP CONDITION MET
MNEMONIC: JMP
OCTAL CODE: 001XXX

JUMP UNCOND. IS TYPICAL

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



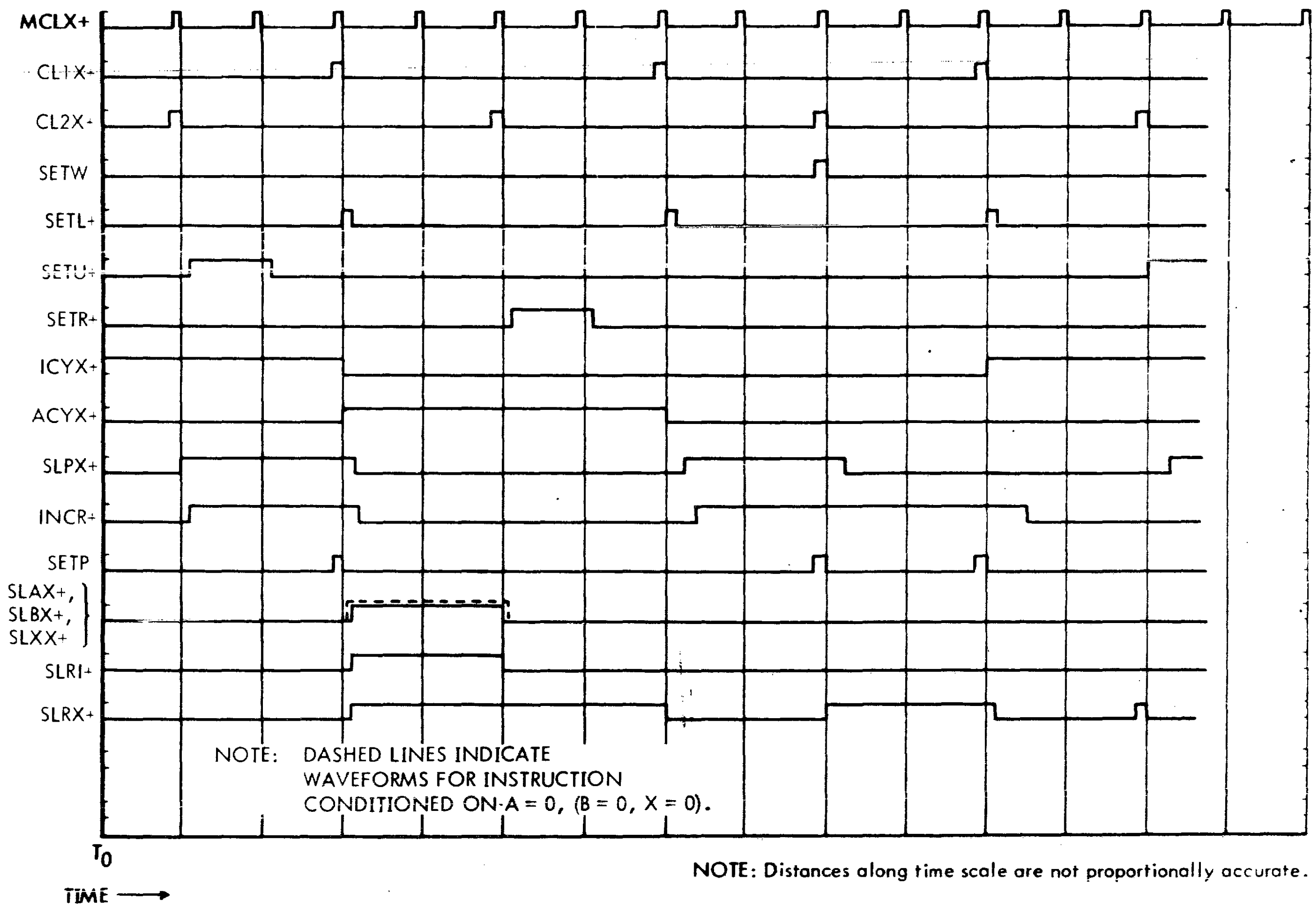
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-26. Jump Condition Met Timing

INSTRUCTION: JUMP-AND-MARK CONDITION MET
MNEMONIC: J--M
OCTAL CODE: 002XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



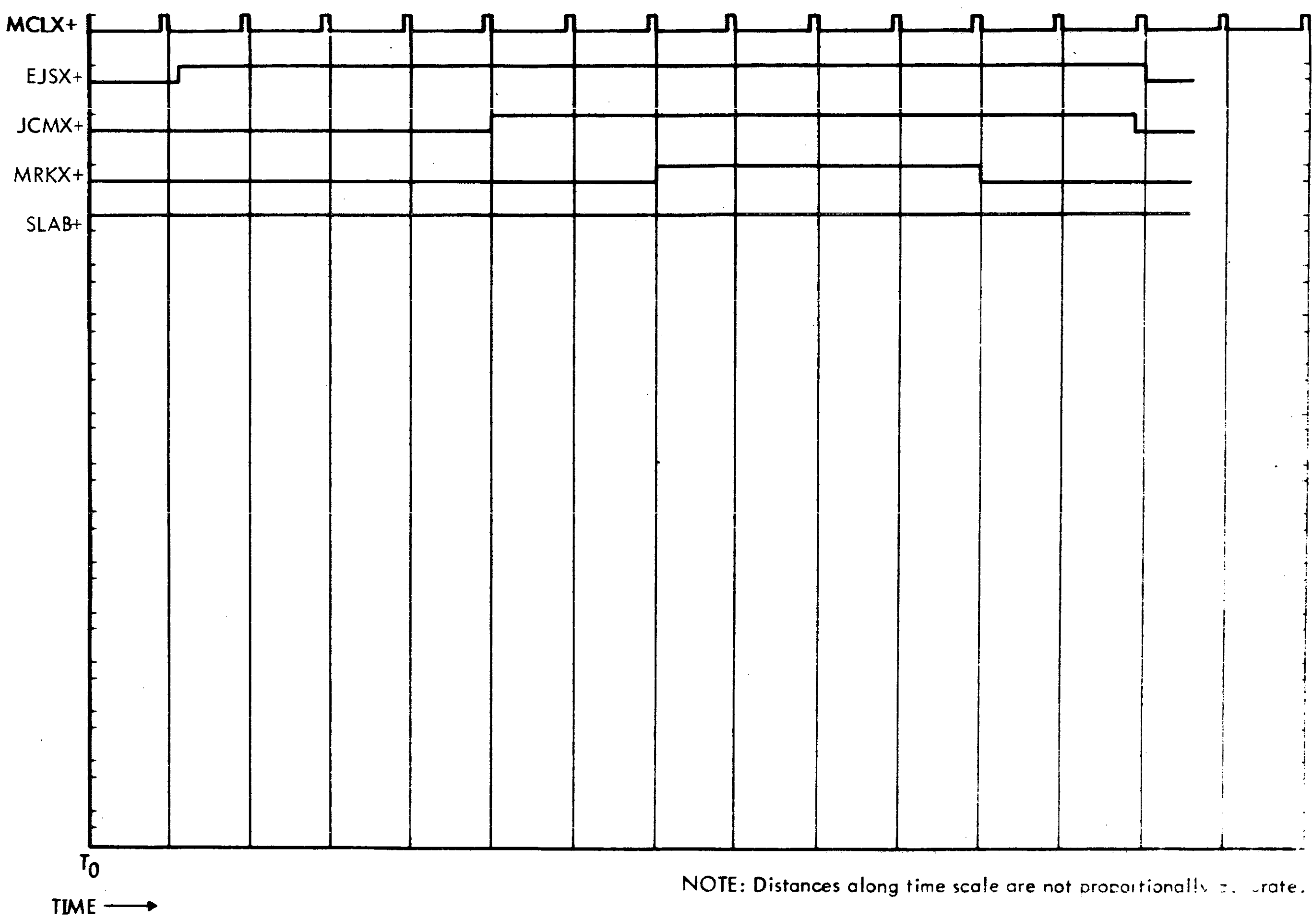
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-27. Jump-and-Mark Condition Met Timing

INSTRUCTION: JUMP-AND-MARK CONDITION MET
MNEMONIC: J--M (CONT'D)
OCTAL CODE: 002XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

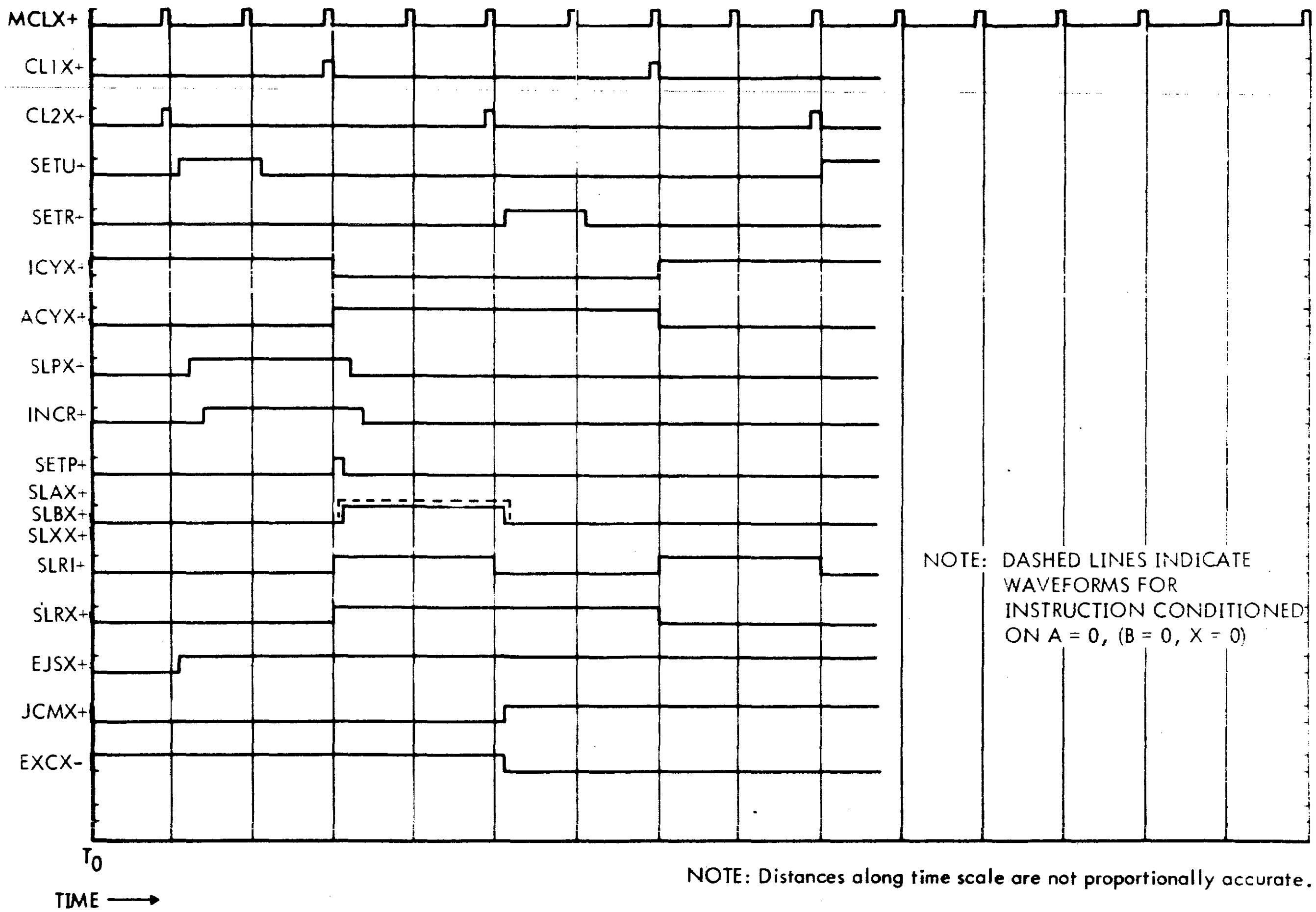
Figure IX-27. Jump-and-Mark Condition Met Timing *(continued)*

VT11-1431

INSTRUCTION: EXECUTE INSTRUCTION
MNEMONIC: X--
OCTAL CODE: 003XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

Figure IX-28. Execute Instruction Timing

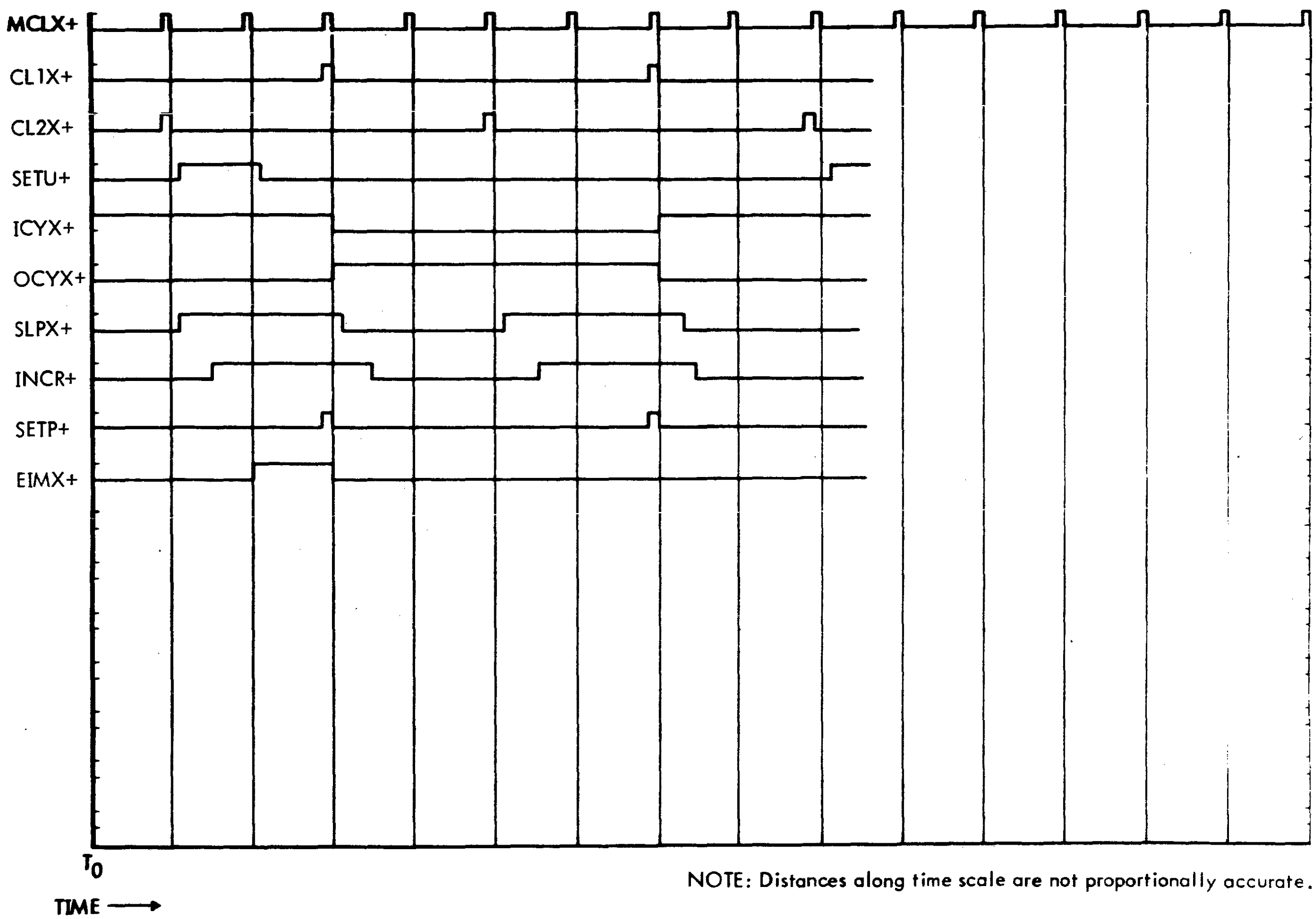
VTII-1433

INSTRUCTION: IMMEDIATE INSTRUCTION
MNEMONIC: LDAI
OCTAL CODE: 006010

LOAD A REGISTER IMMEDIATE IS TYPICAL

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



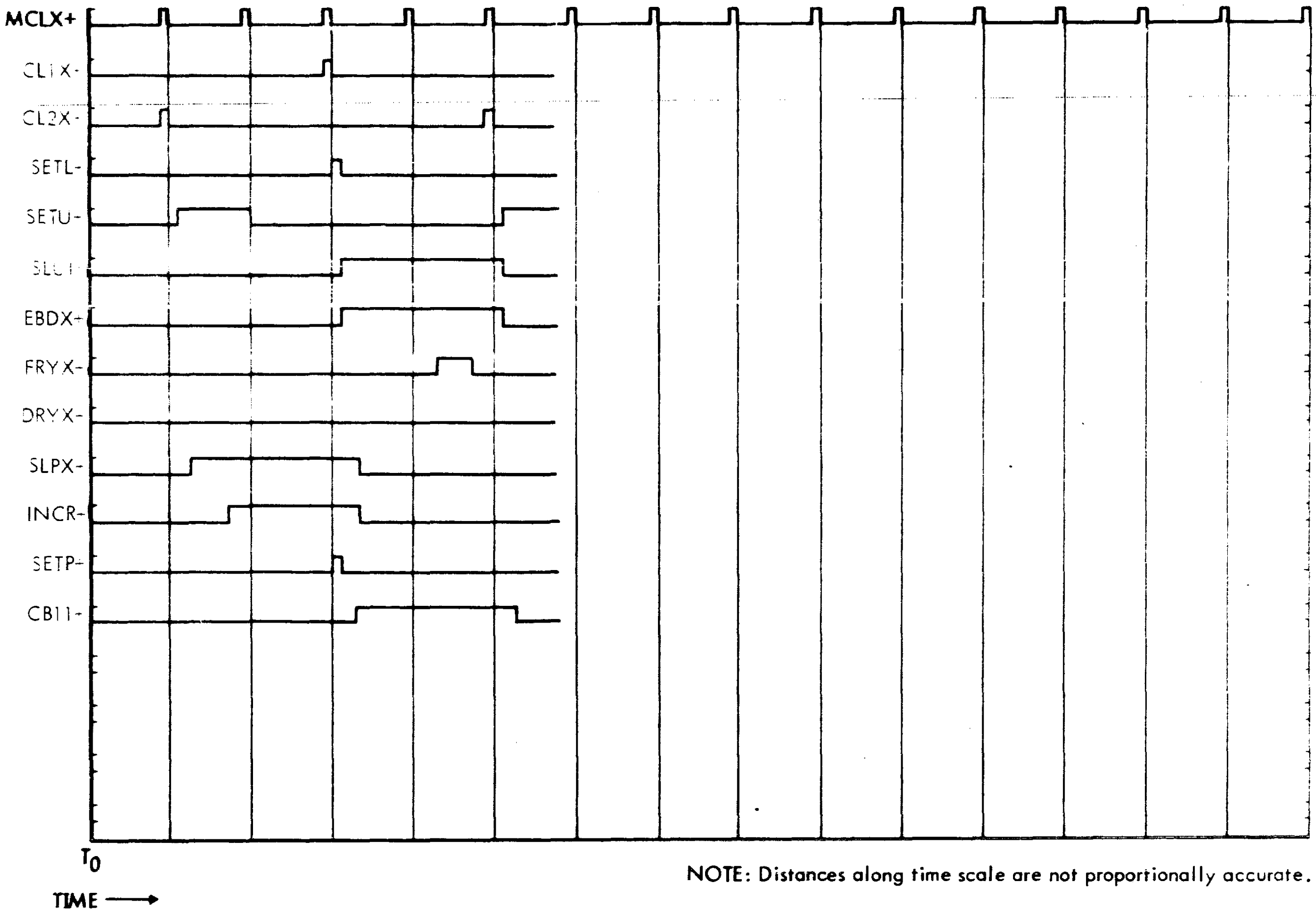
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-29. Immediate Instruction Timing

INSTRUCTION: EXTERNAL CONTROL
MNEMONIC: EXC
OCTAL CODE: 100XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



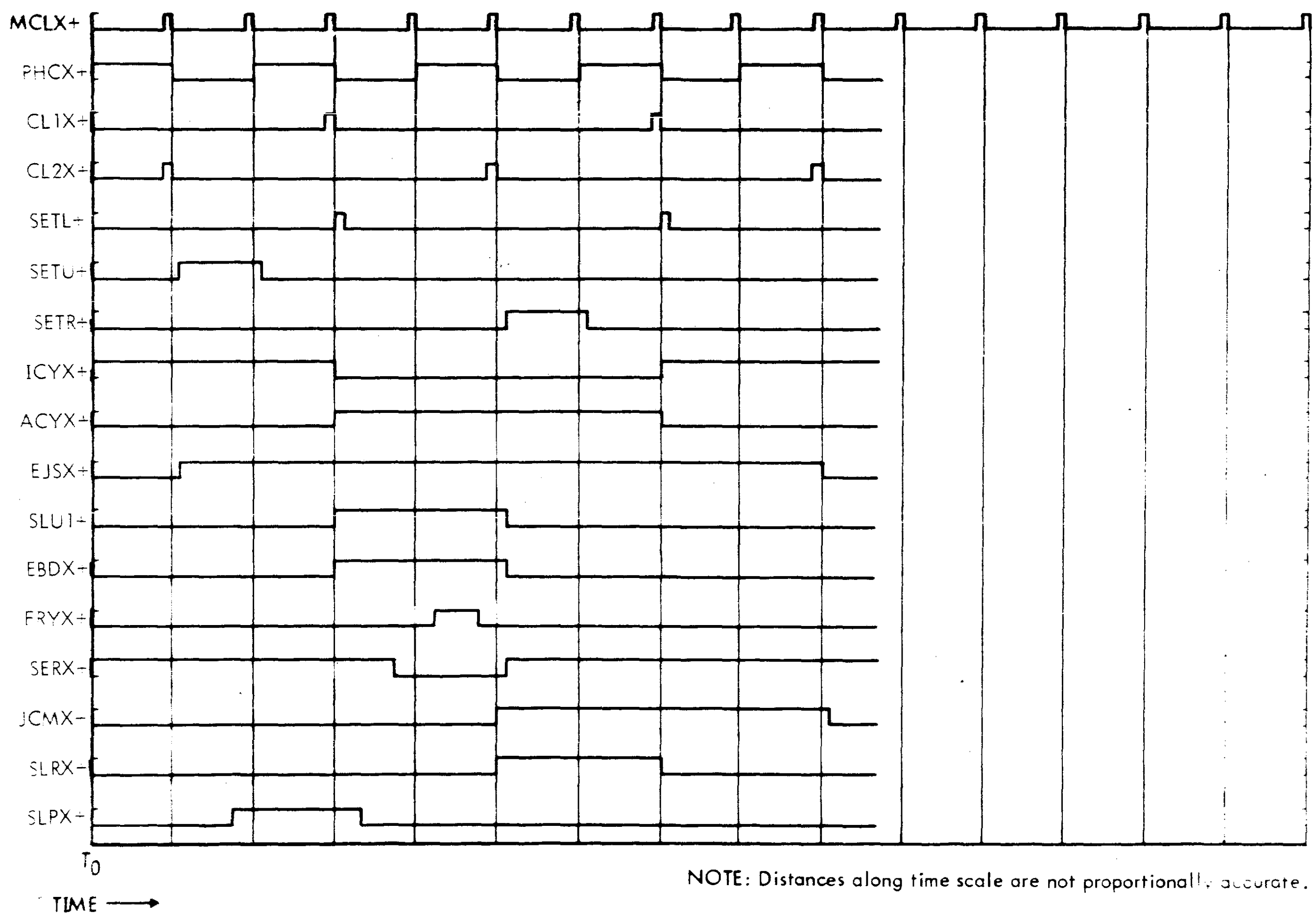
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-30. External Control Timing

INSTRUCTION: SENSE (WITH RESPONSE)
MNEMONIC: SEN
OCTAL CODE: 101XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

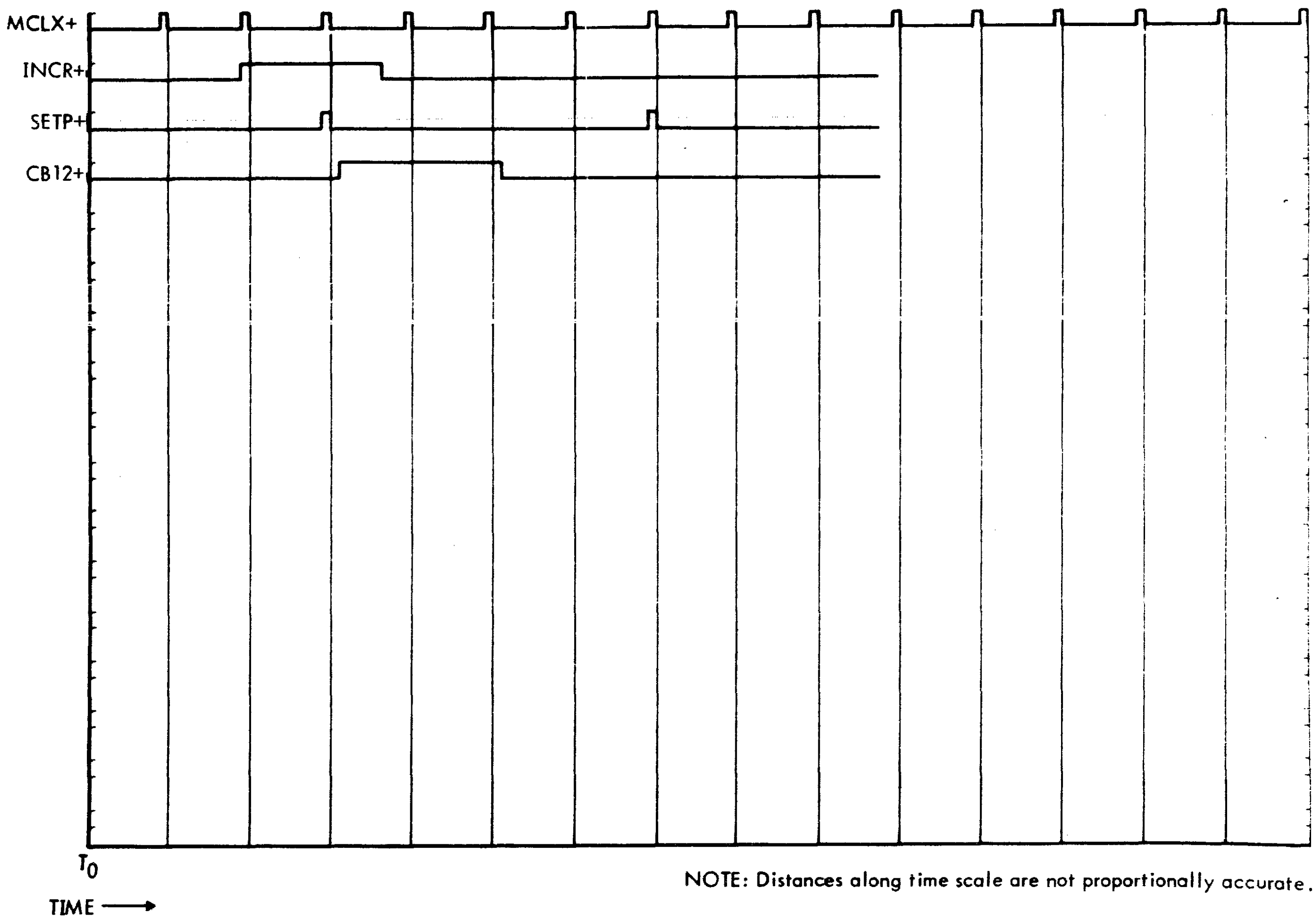
Figure IX-31. Sense (With Response) Timing

VT11-1436

INSTRUCTION: SENSE (WITH RESPONSE)
MNEMONIC: SEN (CONT'D)
OCTAL CODE: 101XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

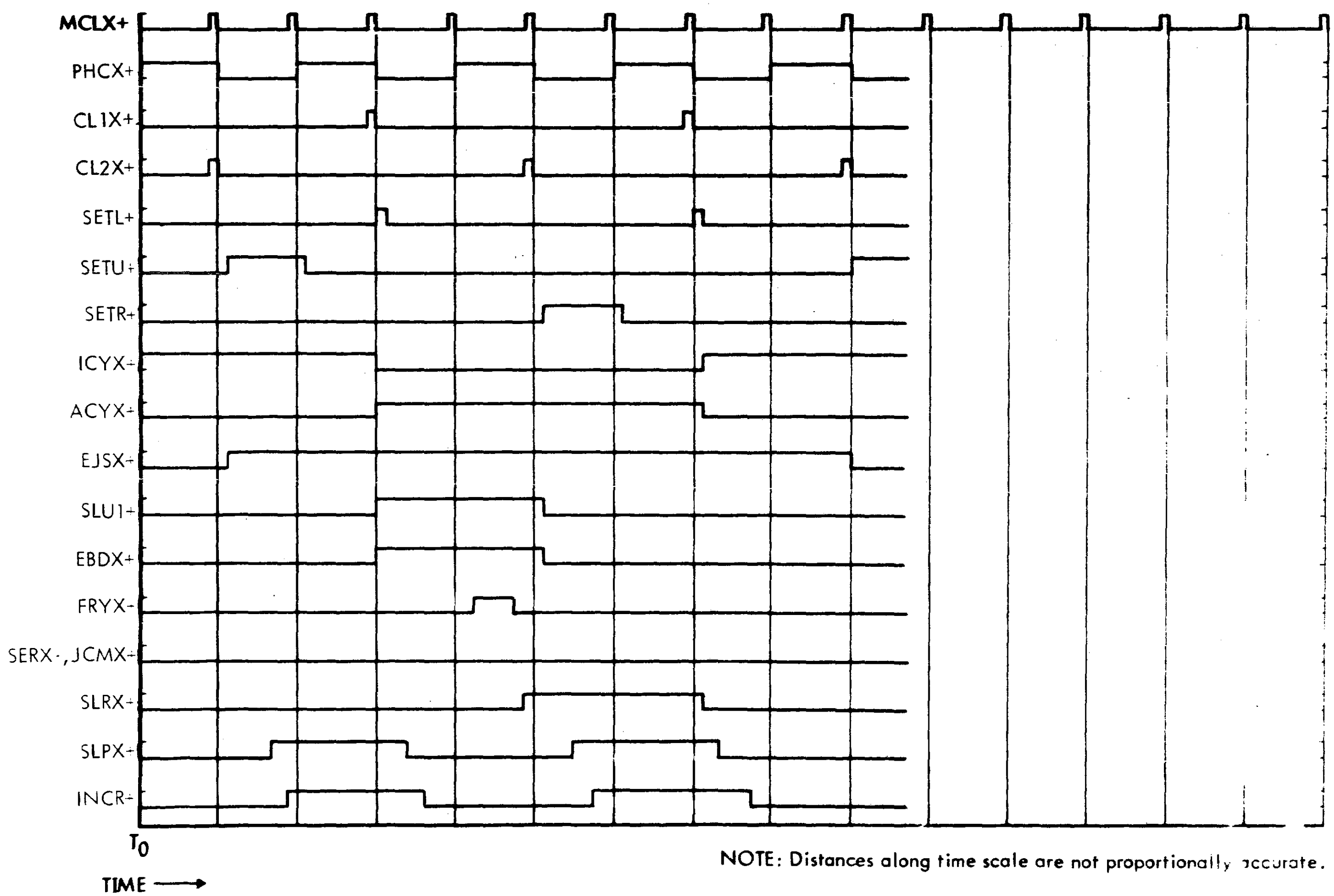
Figure IX-31. Sense (With Response) Timing (continued)

VTII-1437

INSTRUCTION: SENSE (NO RESPONSE)
MNEMONIC: SEN
OCTAL CODE: 101XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



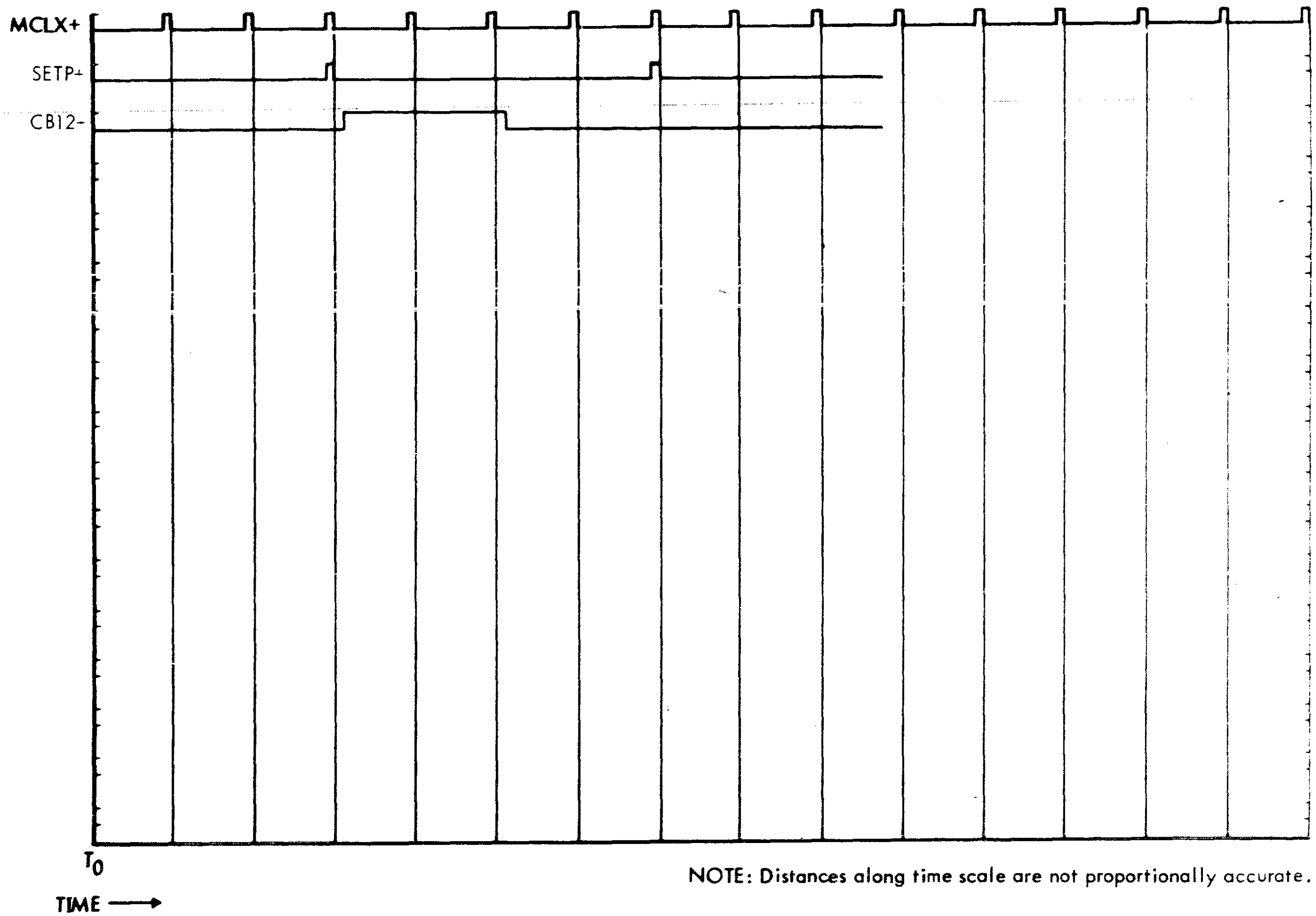
NOTE: Distances along time scale are not proportionally accurate.

Figure IX-32. Sense (No Response) Timing

INSTRUCTION: SENSE (NO RESPONSE)
MNEMONIC: SEN (CONT'D)
OCTAL CODE: 101XXX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

VT11-1438

Figure IX-32. Sense (No Response) Timing (continued)

VTII-1439

INSTRUCTION: INPUT TO (A,B) REGISTER
MNEMONIC: INA, INB
OCTAL CODE: 1021XX, 1022XX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.

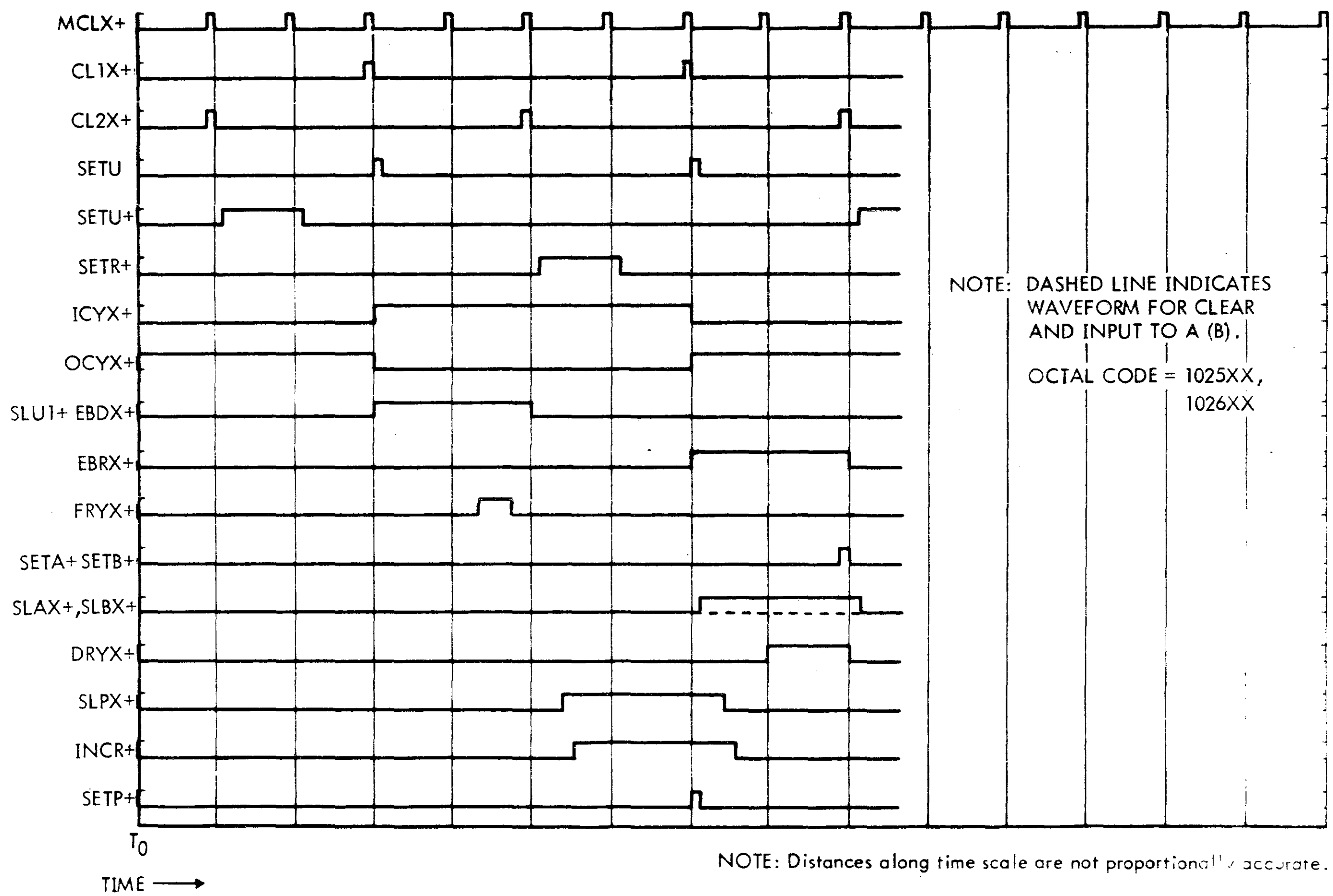


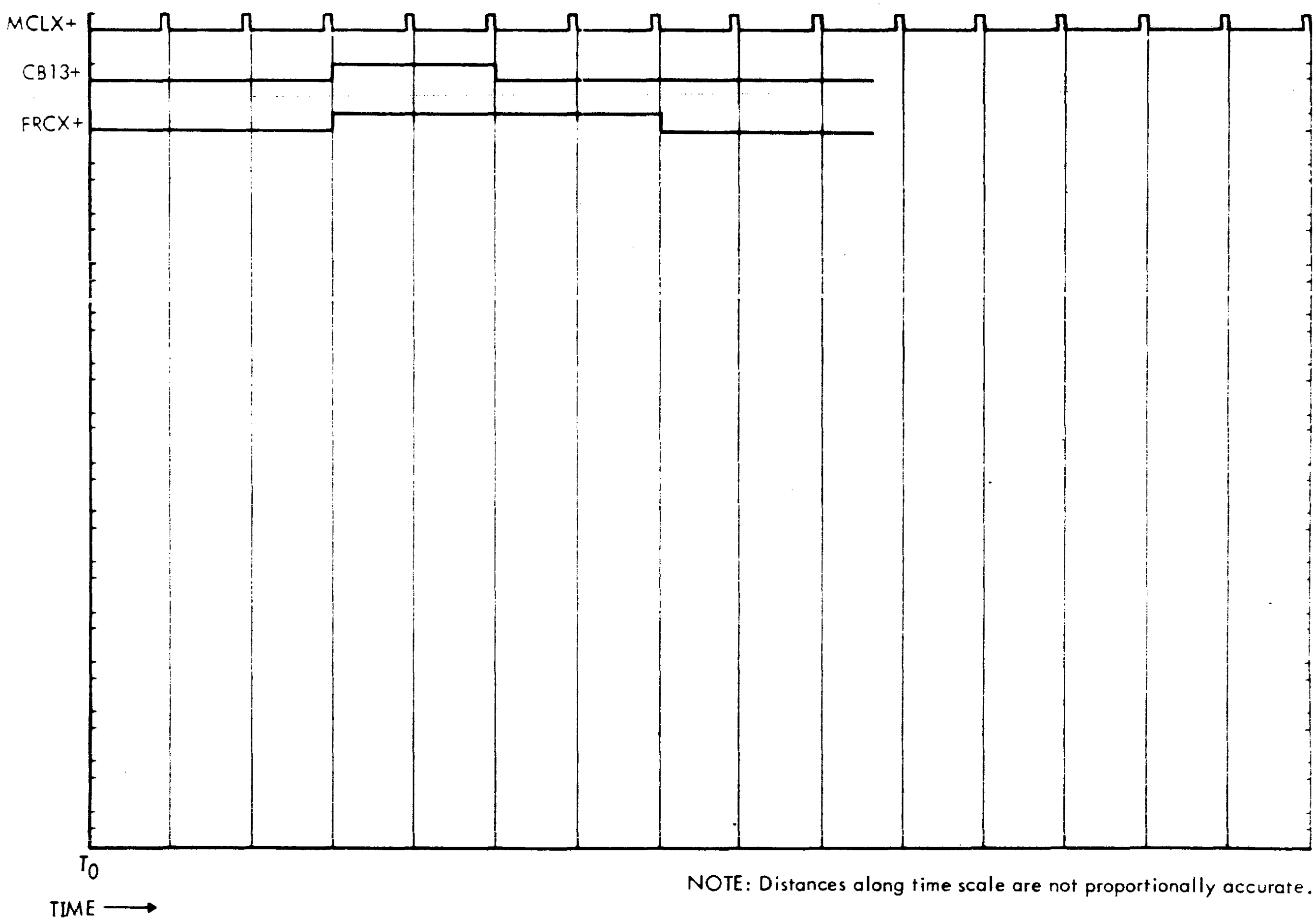
Figure IX-33. Input To (A, B) Register Timing

INSTRUCTION:	INPUT TO (A,B) REGISTER (CONT'D)
MNEMONIC:	INA, INB
OCTAL CODE:	1021XX, 1022XX

Logic levels: True = +5V dc

False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

Figure IX-33. Input To (A, B) Register Timing (continued)

VT11-1441

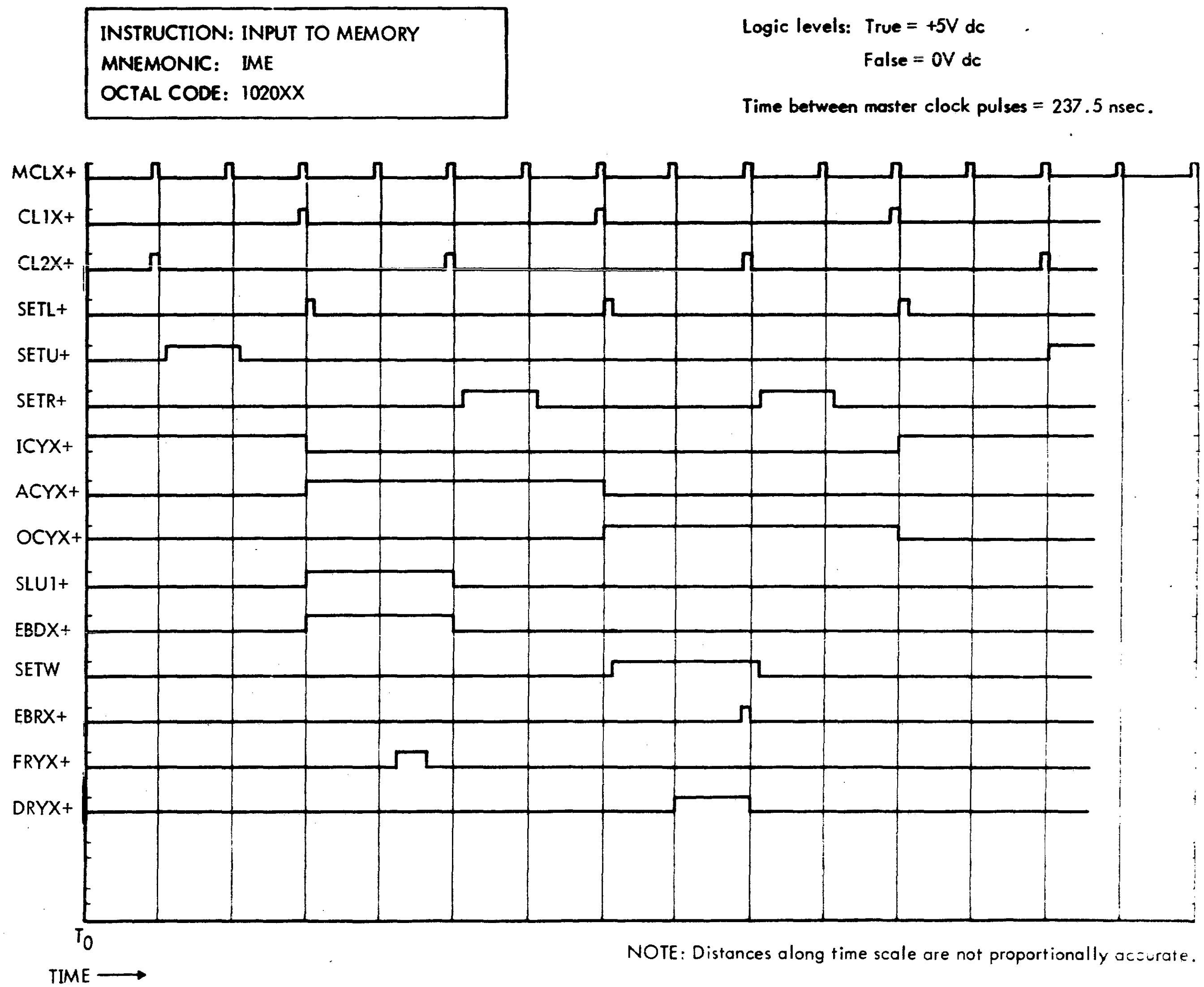
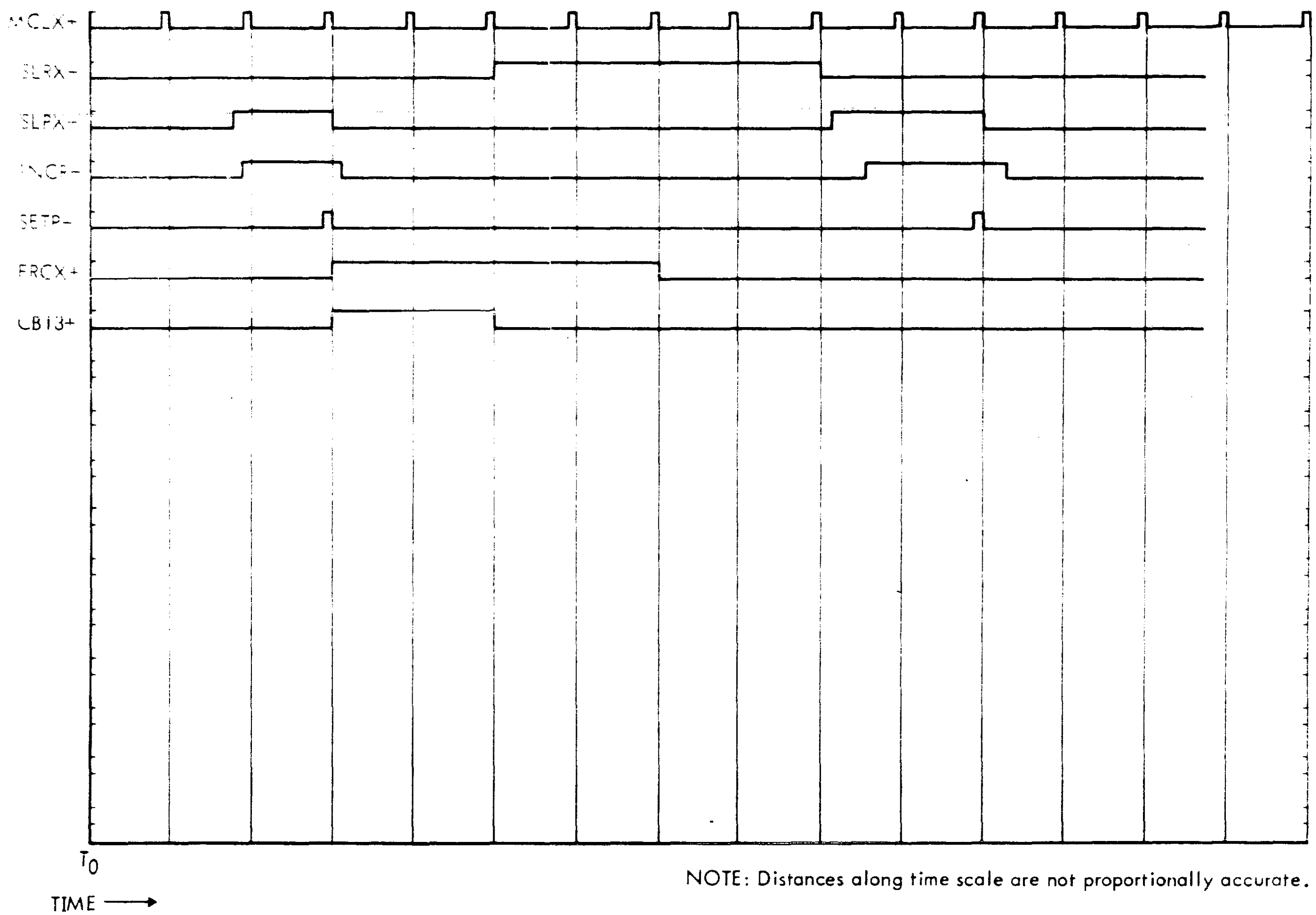


Figure IX-34. Input To Memory Timing

INSTRUCTION: INPUT TO MEMORY (CONTINUED)
MNEMONIC: ME
OCTAL CODE: 1020XX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

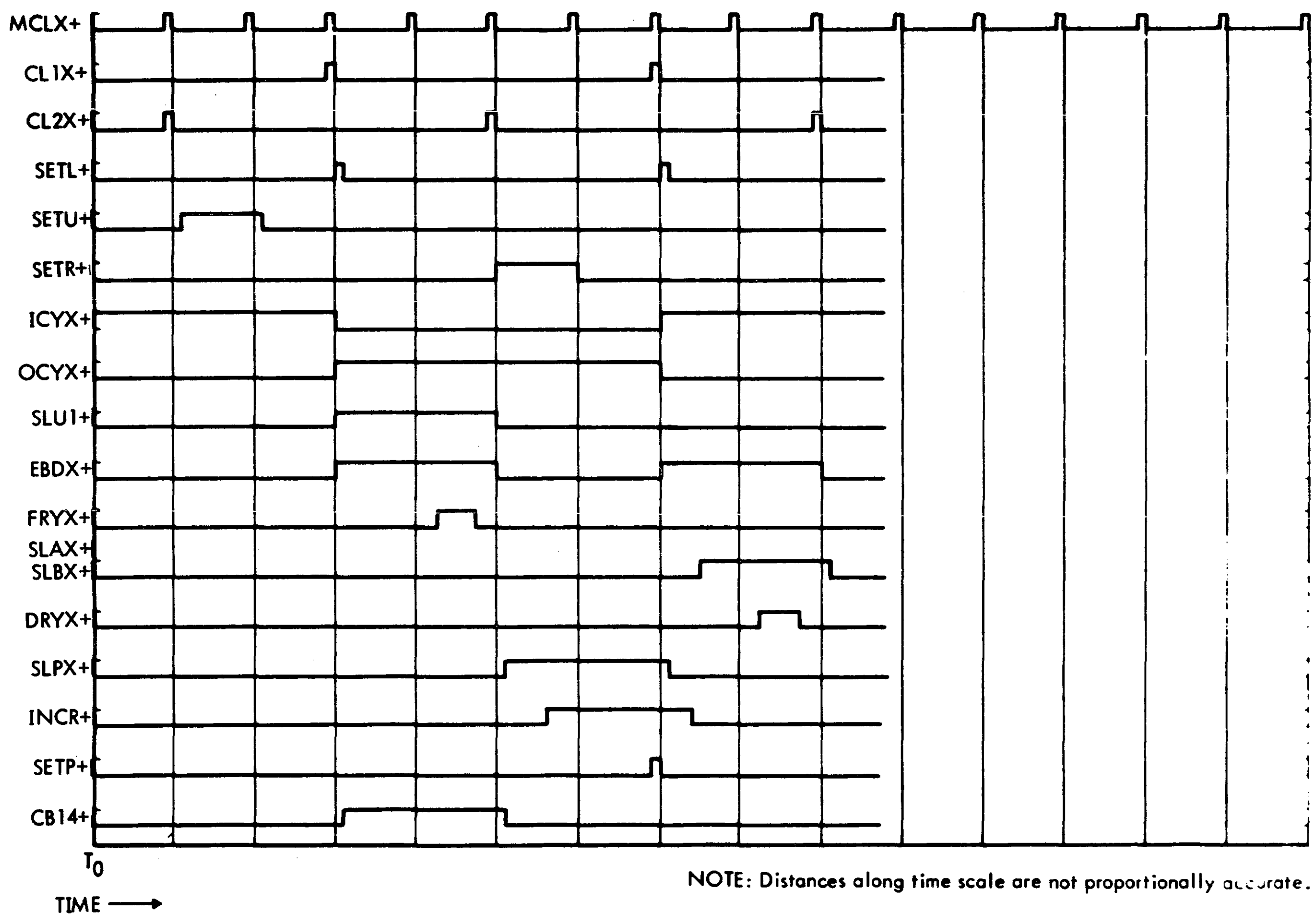
Figure IX-34. Input To Memory Timing *(continued)*

VTII-1443

INSTRUCTION: OUTPUT FROM A, B REGISTER
MNEMONIC: OAR, OBR,
OCTAL CODE: 1031XX, 1032XX

Logic levels: True = +5V dc
False = 0Vdc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

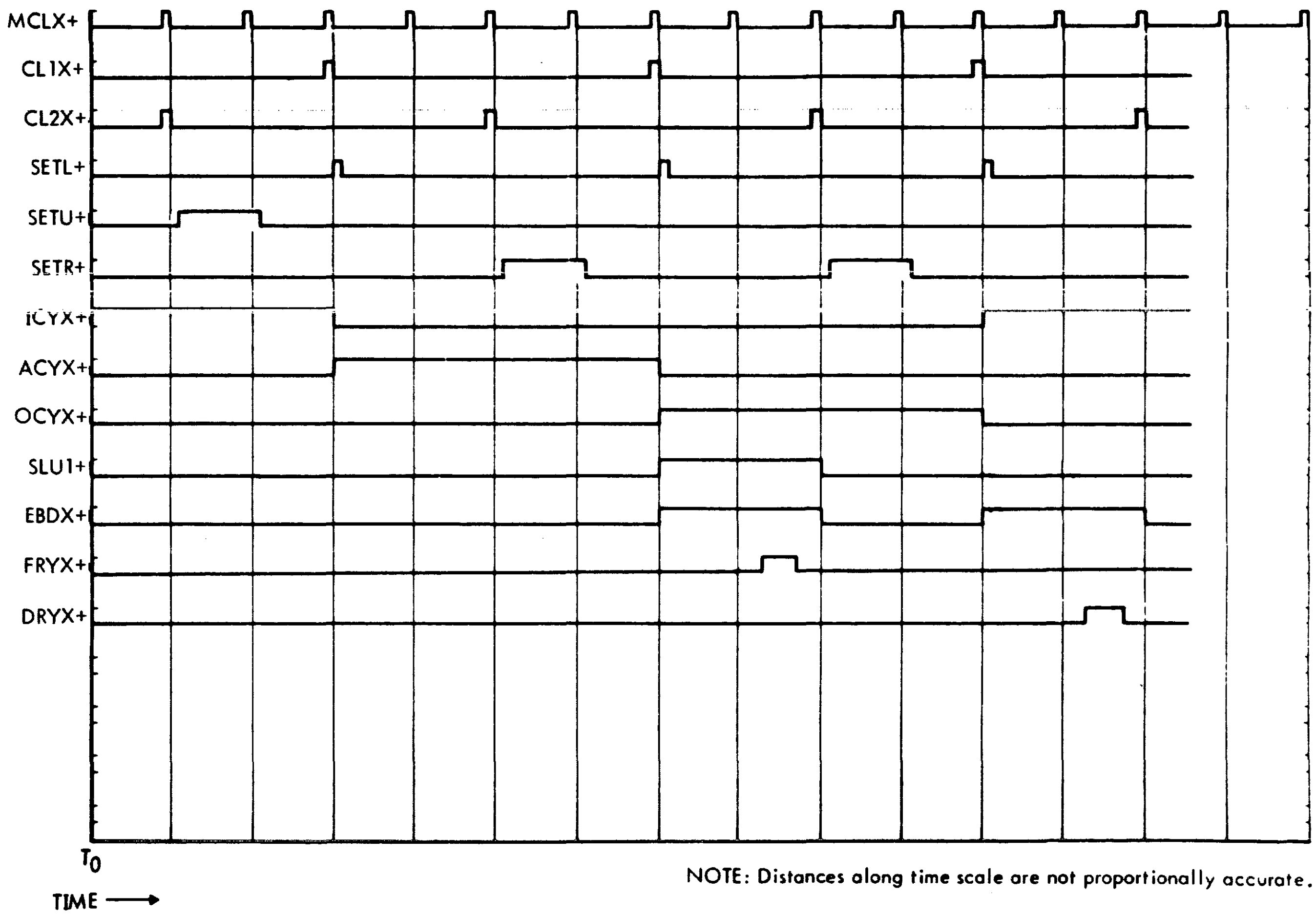
Figure IX-35. Output From A, B Register Timing

VT11-1444

INSTRUCTION: OUTPUT FROM MEMORY
MNEMONIC: OME
OCTAL CODE: 1030XX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

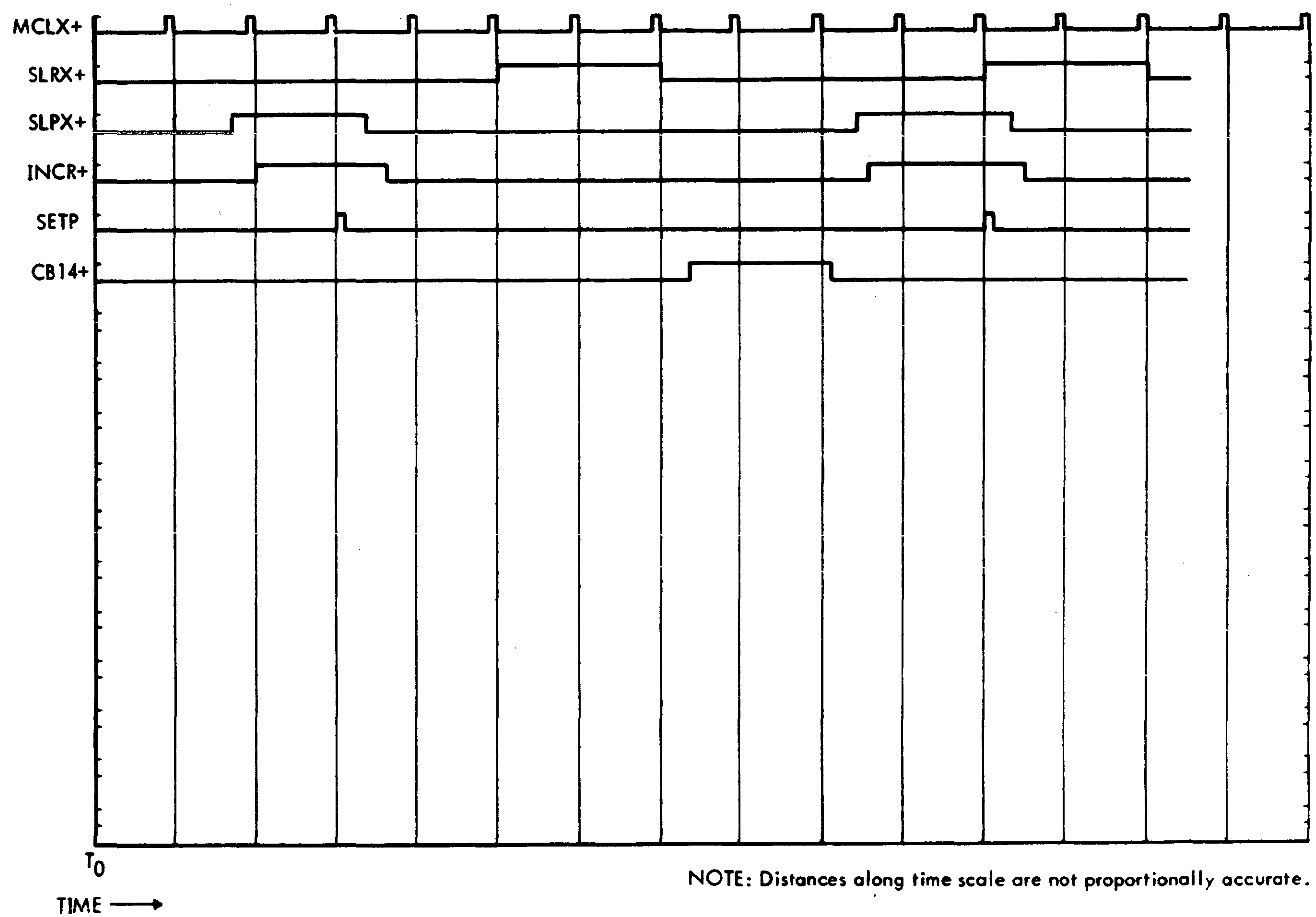
Figure IX-36. Output From Memory Timing

VTII-1448

INSTRUCTION: OUTPUT FROM MEMORY
MNEMONIC: OME (CONT'D)
OCTAL CODE: 1030XX

Logic levels: True = +5V dc
False = 0V dc

Time between master clock pulses = 237.5 nsec.



NOTE: Distances along time scale are not proportionally accurate.

Figure IX-36. Output From Memory Timing (continued)

CHAPTER X

MULTIPLY/DIVIDE AND EXTENDED ADDRESSING

SECTION 1
INTRODUCTION

The multiply/divide and extended addressing feature (M/D) reduces the steps required to prepare a multiplication or division subroutine, and permits extended addressing to specific instructions or data located anywhere in memory.

The M/D is contained on a single circuit card that plugs into the computer mainframe (see chapter II).

Multiplication in the computer system consists of successive additions of the multiplicand with appropriate shifts to the right. Likewise, division is accomplished by successive subtractions of the divisor from the dividend with appropriate left shifts of the partial quotient. Once a program instruction to accomplish multiplication or division is implemented, the necessary steps required to complete the operation are accomplished by the M/D without further program intervention.

The extended addressing in the M/D enables addressing of the entire memory, either indexed, direct, or indirect. Doubleword instruction is used, with the effective address contained in the second word. The same instruction format is used for immediate-type instructions; however, indirect addressing is not permitted, and the second word contains an operand. When traps or interrupts are in progress, the direct memory access circuit (DMA) applies an inhibiting signal to the extended addressing circuit.

1.1 FUNCTIONAL DESCRIPTION

The M/D consists of three major sections (figure X-1): multiplication, division, and extended addressing.

1.1.1 Multiplication

In a multiplication operation, the contents of the effective memory location are multiplied by the contents of the B register, and the contents of the A register are added to the product. The resultant is placed in the A and B registers, with the most significant half in the A register and the least significant half in the B register. A sign of the resultant is placed in bit 15 of the A register; bit 15 of the B register is always set at zero. The largest

CHAPTER X
MULTIPLY/DIVIDE AND EXTENDED ADDRESSING

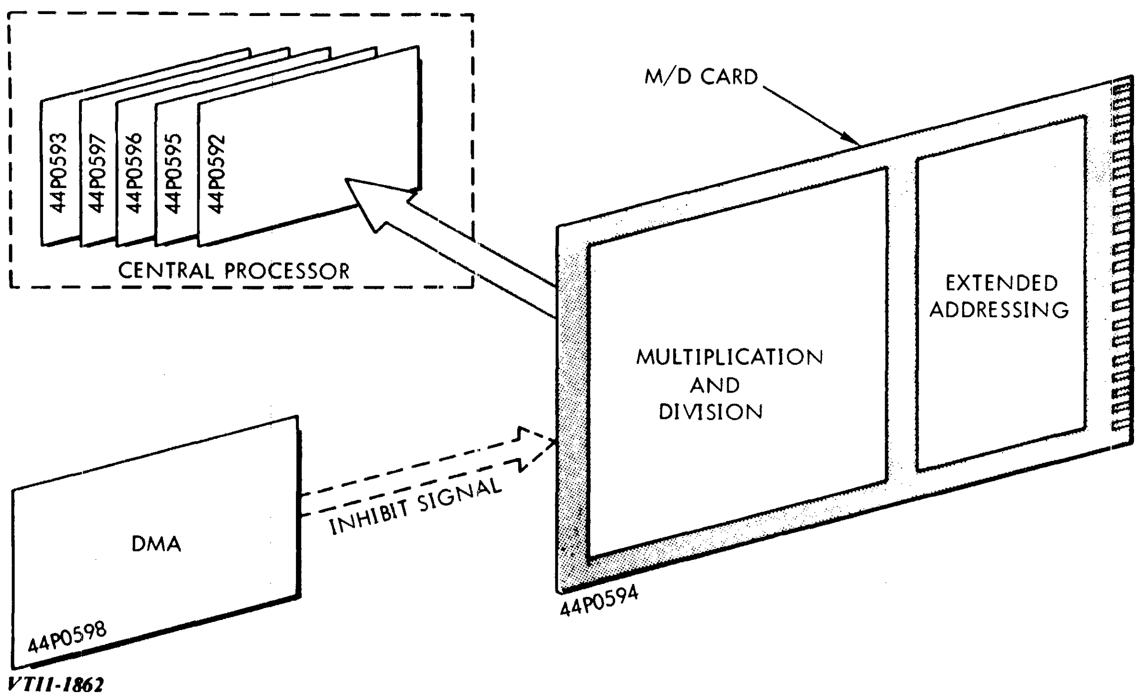


Figure X-1. M/D Functions

positive multiplier or multiplicand that can be contained in an operating register is 15 binary bits; the last bit contains the sign. The product of the largest positive multiplier and multiplicand is always smaller than the combined capacity of the A and B registers; therefore, that product will not set the overflow.

The product of the largest negative multiplier and multiplicand is one greater than the capacity of the combined A and B registers. In this case the overflow indicator will be set, and the combined A and B registers will indicate all zeros with a negative sign bit. This is the only case in which multiplication alone can cause the overflow indicator to be set.

1.1.2 Division

In a division operation, the dividend is contained in the combined A and B register, with the sign in bit 15 of the A register. The sign bit of the B register is not used. The divisor is contained in the effective memory location. The quotient and the sign of the quotient are placed in the B register, and the remainder is placed in the A register along with the sign of the dividend. If the quotient exceeds the capacity of the B register, the overflow indicator will be set. Also, the following special rules apply. A software solution to these rules is provided in figure X-2.

a. If the divisor is zero, the quotient will be the complement of the high-order 15 bits of the dividend with inverted sign. The remainder will be equal to the low-order 15 bits of the dividend. The overflow will always be set.

b. If the dividend is negative and an integer multiple of the divisor, the B register will indicate the quotient minus one, and the A register (the remainder) will be equal to the divisor. The sign of the remainder will equal the sign of the dividend. The following octal statements illustrate this rule.

c. – 010/02 = – 04 and a remainder of – 02

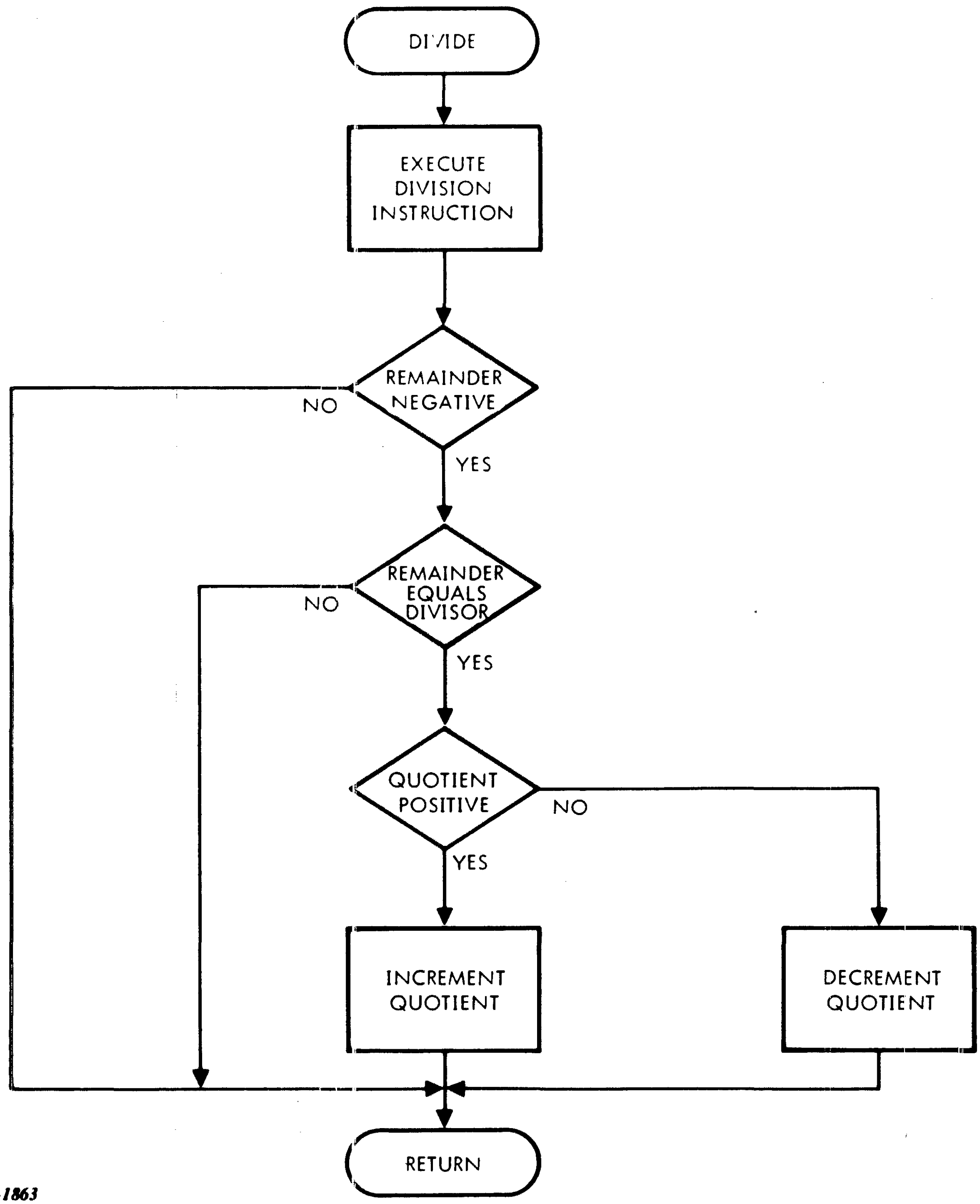
d. – 010/– 02 = + 04 and a remainder of – 02

1.1.3 Extended Addressing

Extended addressing allows addressing of all memory locations, either indexed, direct, or indirect. The second word of the double-word extended instruction contains the effective address. In direct addressing, the address of the operand is located in the second word. The operand is then one level removed from the instruction. Indirect addressing occurs when an operand is two or more levels removed from the instruction. In such cases, the address of the operand address (the indirect address) is contained in a memory location addressed by the instruction. The double-word instruction format, along with the addressing modes are shown in figure X-3.

When the indirect addressing mode is used, the second address in memory may also be a direct or an indirect address. If a loop of indirect addresses is formed, the processor will remain in the indirect mode until halted by a system reset signal. An example of the indirect addressing mode is shown below.

0500	0006YY7	Extended indirect
0501	0100502	Operand address at 0502
0502	0100503	Operand address at 0503
0503	0100501	Operand address at 0501



VT11-1863

Figure X-2. Flow Chart for Division Correction

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

15–12	11–8	7–4	3–0	
00	06	YY	X	First Word
1	Operand address			Second Word

YY equals any single word instruction in the OP CODE.

If X =	Address Mode	Effective Address
00 to 03	Immediate	Second word contains operand.
04	Relative to P	Contents of second word + (P register + 1).
05	Indexed with X	Contents of second word + X register.
06	Indexed with B	Contents of second word + B register.
07	Direct or indirect	Contents of second word may be a direct or indirect address depending on bit 15.

Figure X-3. Word Format for Extended Addressing

1.2 SPECIFICATIONS

The M/D specifications are listed in table X-1.

Table X-1. M/D Specifications

Parameter	Description
Multiplication Algorithm	A + (B•R) = A, B where A = initial A register content B = multiplier (in B register) R = multiplicand (in memory)

(continued)

Table X-1. M/D Specifications *(continued)*

Parameter	Description
	A, B = product (in A and B registers; most significant half in A, least significant half in B)
Multiplication Capability	Maximum multiplier: 32,767 or −32,768 Maximum multiplicand: 32,767 or −32,768 Maximum product: 1,073,741,824
Division Algorithm	A, B/R = B + A where A, B = dividend (in A and B registers; most significant half in A, least significant half in B) R = divisor (in memory) B = quotient (in B register) A = remainder (in A register)
Division Capability	Maximum divisor: 32,767 or −32,768 Maximum dividend: 1,073,741,823 or −1,073,741,824 Maximum quotient: 32,767 or −32,768
Extended Addressing Modes	Relative to P (contents of second word plus P register plus 1). Indexed with X (contents of second word plus X register). Indexed with B (contents of second word plus B register). Direct (second word is direct address if bit 15 is zero). Indirect (second word is indirect address if bit 15 is one).

SECTION 2
OPERATION

This section contains the M/D instructions and also multiplication/division procedures and examples.

2.1 INSTRUCTIONS

The M/D instructions are listed in table X-2.

Table X-2. Multiply/Divide and Extended Addressing Instructions

Mnemonic	Octal Code	Description	Machine Cycles
Multiply (one-word instruction)			
MUL	16xxxx	Multiply B register by contents of effective memory address	10
Divide (one-word instruction)			
DIV	17xxxx	Divide A and B registers by contents of effective memory address	10
Extended Address (two-word instruction)			
LDAE	00601x	Load A register extended	3
LDBE	00602x	Load B register extended	3
LDXE	00603x	Load X register extended	3
STAE	00605x	Store A register extended	3

Table X-2. Multiply/Divide and Extended Addressing Instructions*(continued)*

Mnemonic	Octal Code	Description	Machine Cycles
STBE	00606x	Store B register extended	3
STXE	00607x	Store X register extended	3
INRE	00604x	Increment and replace extended	4
ADDE	00612x	Add memory to A register extended	3
SUBE	00614x	Subtract memory from A register extended	3
MULE	00616x	Multiply B register extended	11
DIVE	00617x	Divide AB register extended	11
ORAE	00611x	Inclusive OR extended	3
ERAE	00613x	Exclusive OR extended	3
ANAE	00615x	AND extended	3

NOTES:

1. The xs in the DIV and MUL instructions represent the effective address.
2. The xs in the extended addressing instructions specifies the addressing mode (see figure 3-2).

2.2 MULTIPLICATION/DIVISION PROCEDURES

The following subsections provide manual procedures for performing multiplication and division operations. Section 2.3 contains examples that illustrate the operations; section 4 contains several sample problems and their solutions.

2.2.1 Multiplication

A multiplication operation can be performed as follows:

a. Perform power-on routine (chapter III).

b. Load the multiplier into the B register.

c. Load the multiplicand into the X register.

d. Load the store X instruction (070000) into the U register, and execute the instruction. The multiplicand is now in memory.

e. Load the multiply instruction (160000) into the U register, and execute the instruction.

f. Observe the result in the A and B registers. The most significant bits of the product can now be observed by displaying the contents of the A register; the least significant bits can be observed by displaying the contents of the B register.

2.2.2 Division

A division operation can be performed as follows:

a. Perform power-on routine (chapter III).

b. Load the most significant bits of dividend into the A register.

c. Load the least significant bits of dividend into the B register.

d. Load the divisor into the X register.

e. Load the store X instruction (070000) into the U register, and execute the instruction.

f. Load the divide instruction (170000) into the U register, and execute the instruction.

g. Observe the result in the A and B registers. The quotient can now be observed by displaying the contents of the B register; the remainder can be observed by displaying the contents of the A register. Note that the sign bit of the remainder is the same as the sign bit of the dividend.

CHAPTER X
MULTIPLY/DIVIDE AND EXTENDED ADDRESSING

2.3 MULTIPLICATION/DIVISION EXAMPLES

The following examples of multiplication and division are provided to illustrate the operations. The octal problem is preceded by its decimal equivalent for both examples. Negative numbers are in two's complement form. A, B, and R represent the contents of the A register, B register, and memory, respectively. The letter R represents memory because the R register contains the contents of the effective memory address during reading and writing operations.

EXAMPLE A. Multiplication:

(−56) (1212) = −67,872
(177710) (002274) = 17777573340

Before execution:	A = 000000	After execution:	A = 177775
	B = 177710		B = 073340
	R = 002274		R = 002274

EXAMPLE B. Division:

−1,234/616 = −2 with remainder −2
17777775456/001150 = 177776 with remainder 177776

Before execution:	A = 177777	After execution:	A = 177776
	B = 075456		B = 177776
	R = 001150		R = 001150

CHAPTER X
MULTIPLY/DIVIDE AND EXTENDED ADDRESSING

SECTION 3
THEORY OF OPERATION

3.1 GENERAL

Described in the following paragraphs are the three functional divisions of the M/D: multiplication, division, and extended address. Refer to logic diagram 91D0358 in volume 2. Three-digit numbers in parentheses indicate the location of circuit elements on the logic diagram. The first number locates the sheet; the following letter and number indicate the area on that sheet. Circuit elements that are not on the M/D board are followed by their circuit board number in parentheses.

Signals resulting from the outputs of flip-flops are designated FF set signal and FF reset signal if they are high when the flip-flop is respectively set or reset.

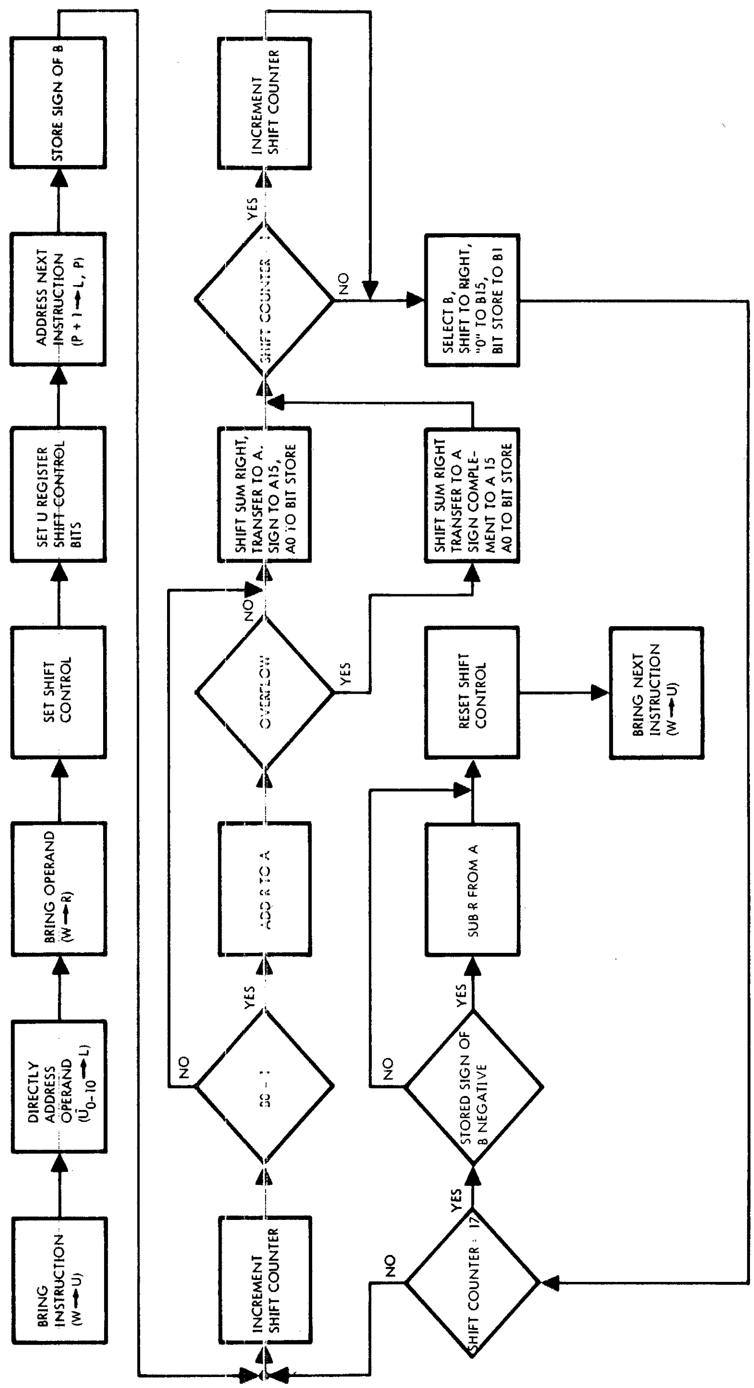
3.2 MULTIPLICATION

Multiplication is accomplished by successive additions of the multiplicand appropriately shifted to the right. A flow diagram illustrating this operation is shown in figure X-4. The timing of signals generated during multiplication is shown in figure X-5.

The multiplication instruction is stored in the U register (44P0592), and the address of the multiplicand is generated and placed in the L register (44P0595). The next memory cycle brings the multiplicand from memory and stores it in the R register (44P0592).

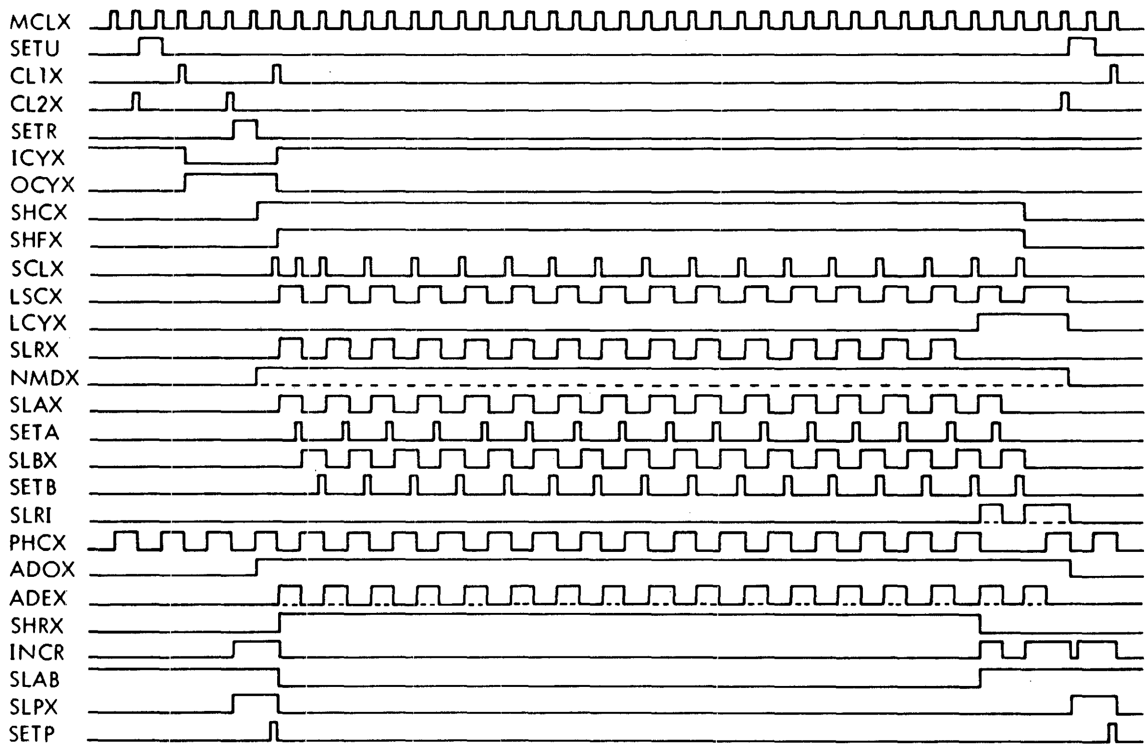
The contents of the U register are decoded in the M/D to form signal MPYX+ high (1C4). Signals MPYX+ high and RB17+ high (2D7) set flip-flop NMDX (1D3). Flip-flop NMDX stores the sign of the multiplier to provide for the correction cycle at the end of the operation.

Signals TOSX- high, FEIX+ high, and H4XX+ high form signal SHC3- low (3C7). Signal SHC3- sets flip-flop SHCX (44P0593). FF set signal SHCX+ high with signal H4XX+ high form signal UMDX- low (1C5). Signal UMDX+ high generates set or reset levels (2C6) for bits 5, 6, 7, and 8 of the U register. Changing the contents of the U register establishes control for the shift portion of the multiply operation. Signal SHCX high also sets flip-flops SHFX (44P0593) and LSXC (44P0593). The outputs of these two flip-flops allow master clock signal MC2X to increment the shift counter (44P0593).



VTII-1864

Figure X-4. Flow Diagram of the Multiplication Instruction



DECIMAL PROBLEM: 1 x -1 = -1

INITIAL CONDITIONS	PRODUCT
A = 000000	A = 177777
B = 177777	B = 077777
C = 000001	

VT11-1865

Figure X-5. Timing Diagram for Multiplication

Multiplication then proceeds by a series of addition-and-shift or shift-without-addition operations. The choice of these two types of operations depends on the state of flip-flop ADEX (2B6). During multiplication, flip-flop ADEX is controlled by the least significant bit of the B register after each shift. The contents of the A register are either increased by the addition of the multiplicand and then shifted right, or they are shifted right without addition. If no overflow results from the addition, the sign of the partial product (in the A register) becomes that of the sum. If an over-flow occurs, the sign bit in the A register becomes the complement sign of the sum. The addition and/or shift of the partial product is accomplished while signal LSCX– is high. The multiplier (in the B register) is shifted right one position each time signal LSCX– is low.

When the shift counter has been incremented to 15, flip-flop LCYX (1B2) is set. At this time if FF set signal NMDX is high, the multiplicand is subtracted from the product. This is accomplished by signals SR14– low (2B4) and INCR– low (2D4).

3.3 DIVISION

Division is accomplished by successive subtractions of the divisor from the dividend and shifts of the partial quotient to the left. A flow diagram illustrating this operation is shown in figure X-6. The timing of signals generated during division is shown in figure X-7.

The divide instruction is stored in the U register (44P0592), and the address of the divisor is generated and set into the L register (44P0595). The next memory cycle brings the divisor from memory and stores it in the R register (44P0592).

The divisor is subtracted from the dividend if the sign of the quotient is to be positive (the divisor is added to the dividend if the sign of the quotient is to be negative). If the sign of the difference is not equal to the sign of the A register, the divisor is removed from the adder input. This is done before the output of the adder is shifted to the left and placed in the A register. If the divisor is not added to the partial quotient (in the A register) and the quotient sign is negative, flip-flop BISX (44P0593) is set. If the divisor is added to the partial quotent and the sign is positive, flip-flop BISX is set. The content of bit 14 of the B register is placed in the least significant bit of the A register. The contents of the B register are then shifted left with signal BISX being shifted into the least significant bit of the B register.

The sign of the dividend is stored in flip-flop SBAX (44P0596). If FF set signal SBAX+ is high, flip-flop NMDX (1D3) is set when the divisor is clocked into the R register on signal SETR+. If the quotient is to be negative, flip-flop ADOX (1B5) is set at the same time as flip-flop NMDX.

The contents of the U register are changed to establish control for the shift portion of the division operation. Bit 13, 14 and 15 of the U register decode to form signal H4XX- low (1D5). Signal SHC3- low sets flip-flops SHCX, SHFX, and LSCX (44P0593). FF set signal SHCX+ high with signal H4XX- low form signal UMDX- low (1C5). Signal UMDX- low generates set or reset levels (2C6) for bits 5, 6, 7, and 8 of the U register. The outputs of flip-flops SHFX and LSCX control the incrementing of the shift counter (44P0593).

Flip-flop ADEX (2B6) is also set when FF set signal LSCX- goes high. Signal LSCX- high selects the A register to the adder, and signal SLR5- low (2B4) selects the operand. Signal SLR5- low is generated by signal DIVX+ high, signal SHFX+ high, FF set signal ADOX+ high, and FF set signal ADEX+ high.

The result of the first addition (subtraction if FF set signal ADOX+ was low) is compared with the condition of flip-flop NMDX to form signal DSCX- (2A7). Signal DSCX- high with

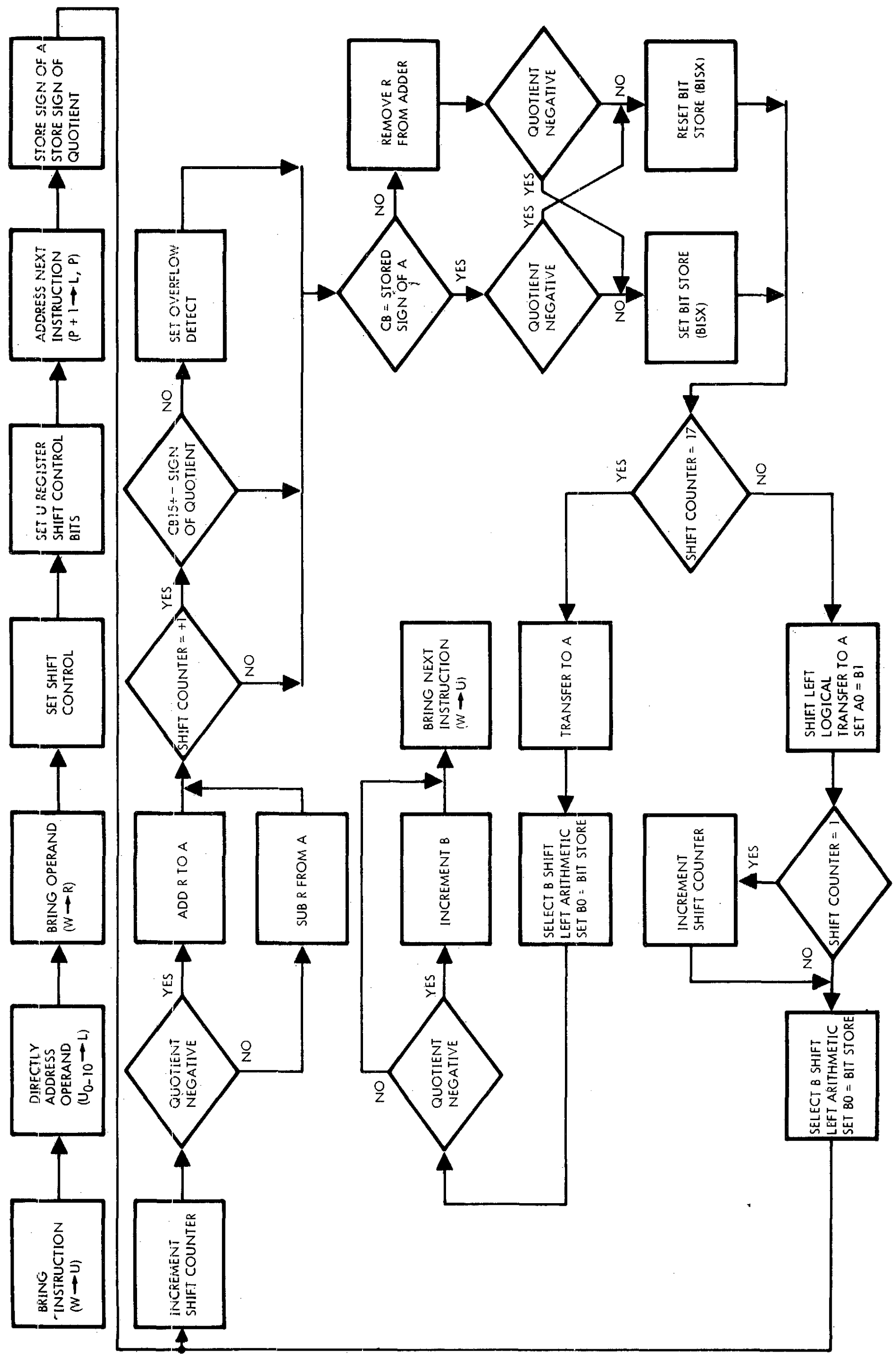


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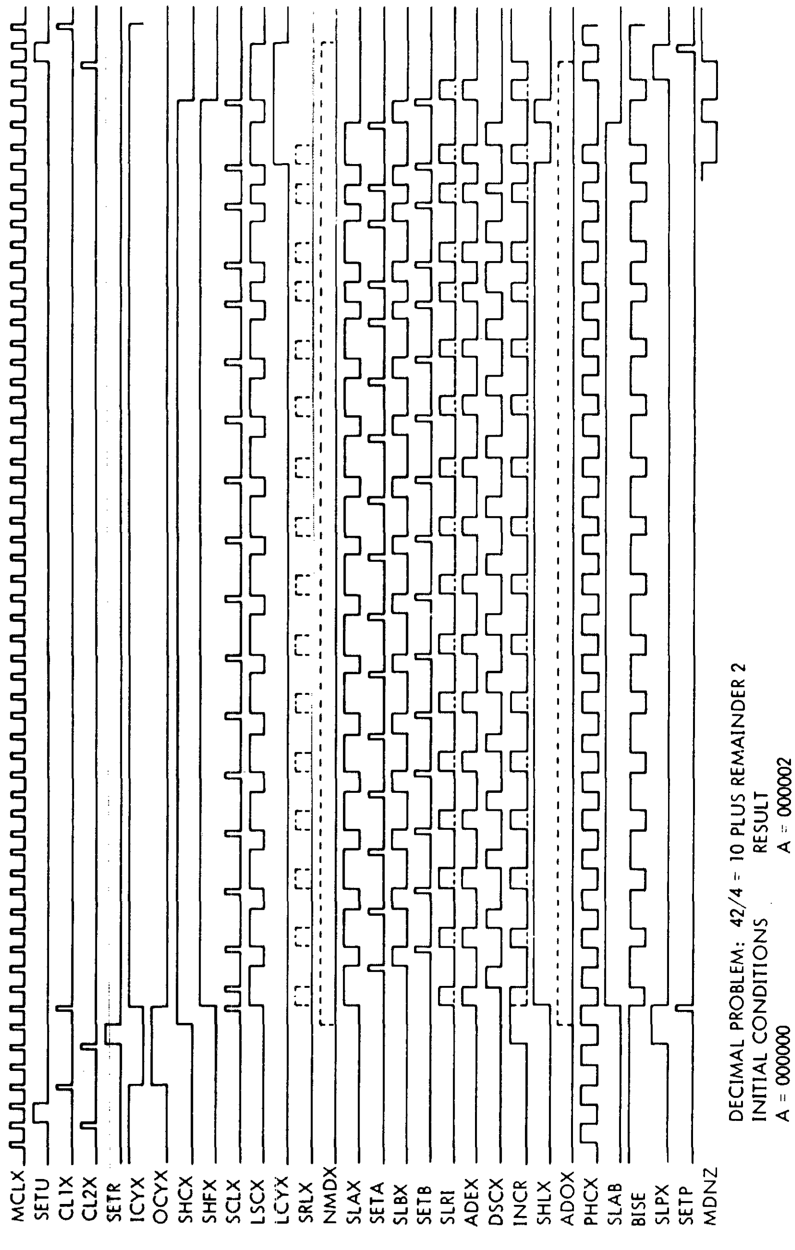
Figure X-6. Flow Diagram of the Division Instruction



VT11-1867

Figure X-7. Timing Diagram for Division

signal DIVX+ high, signal FCDX+ high, and FF reset signal LCYX– high set flip-flop DODX (1C2). This flip-flop enables the overflow indication. Signal DSCX– high also inhibits the set of the A register (44P0592) and the reset of flip-flop LSCX (44P0593).

The delayed reset of flip-flop LSCX allows the contents of the R register to be removed from the adder before the adder output is shifted left and placed in the A register. Bit 14 of the B register is shifted into bit zero of the A register. Flip-flop BISX is set if flip-flops ADOX and ADEX are both set or both reset.

Removing the contents of the R register from the adder allows signal DSCX– to go low and enables the reset of flip-flop LSCX. FF reset signal LSCX high selects the B register to the shift gates, and the contents are shifted left one position with FF set signal BIXE going to the least significant position. The shift counter is then incremented, and the cycle is repeated until the shift count is equal to 15.

Flip-flop LCYX (1B2) is set as the shift counter is incremented to 15. FF set signal LCYX+ high enables signal PHC3– low (2D7) and signal MDN2+ low (2A6). Signal PHC3– low inhibits the set of the phase clock flip-flop (44P0593) for one cycle. Signal MDN2+ low inhibits signals SHLX and SLAB while the result of the last subtraction is transferred to the A register. The contents of the B register are then shifted left and, if the quotient is to be negative, incremented to provide the final two's complement quotient.

3.4 EXTENDED ADDRESSING

The extended instruction is placed in the U register and decoded to form signals K2XX+ and AC6X+. If signal U02X+ is low, flip-flop EIM1 (44P0596) is set, and the second word of the immediate instruction is used as the operand. If signal U02X+ is high, flip-flop EIM2 (1D6) is set. FF set signal EIM2 high generates signal EIMX– low (1D6). Signal U02X+ high and FF set signal EIM2 high generate signal FEA1– low. Flip-flop ACYX (44P0596) is set on the next CL1X pulse.

FF set signal ACYX– high and FF set signal EIM2 high cause signal U02X+ to go low (1C7). These two signals also transfer the states of signals U00X and U01X to signals U09X respectively (1A7). The new states of signals U09X, U10X, and U10X and U11X are decoded to form signals AC4X, AC5X, AC6X, and AC7X. Signal EIMX low transfers the states of signals U03X through U06X to signals U12X through U15X, respectively.

The address code signals AC4X, AC5X, and AC6X select the contents of the P, X, or B register which is added to the second word of the instruction to form the effective memory address of the operand address. If signal R15X is high, the second word is an indirect address; the processor will remain in the address cycle and fetch the address specified by the contents of the R register. This second address may also be a direct or indirect address. If a loop of indirect addresses is formed, the processor will remain in the indirect addressing mode until halted by a system reset signal.

3.5 MNEMONICS

The M/D mnemonics are listed in table X-3.

Table X-3. Mnemonic Definitions

Mnemonic	Description
ACYX	Address cycle. Starts extended addressing using address code signals.
ACiX	Address code. Selects P, X, or B register as part of operand address.
ADEX	Add-enable flip-flop. Stores the requirement for an addition.
ADOX	Add-operand flip-flop. Stores sign of quotient.
BISE	Bit-store enabler. Sets bit-store flip-flop.
BISX	Bit store. Enables shift gate A during long shifts and division.
CBii	C-bus bits. Provides data for multiply/divide.
CL2X	Clock 2. Gates clear signal at proper point in memory cycle.
CLRX	Clear. Clears flip-flops DODX, LCYX, and NMDX.
DIVX	Divide. Indicates that a division operation is occurring.
DODX	Division overflow-detect flip-flop. Stores the occurrence of an overflow diring division.
DSCX	Division sign check. The result of a sign check during division.
EIMX	Execute immediate. Cutput of flip-flop EIMZ.

Table X-3. Mnemonic Definitions *(continued)*

Mnemonic	Description
EIM2	Execute immediate flip-flop 2. Stores requirement for extended addressing.
EMRX	E and W bus receiver. Enables decoding of address codes.
FCDX	First-count detector. Indicates that shift counter has reached a count of one.
FEA1	Fetch address. Enables address cycle.
FEIX	Fetch instruction. Enables shift control bit 3.
HLTX	Halt. Disables extended addressing and multiply/divide result.
H4XX	Is decoded from U-register bits and enables further decoding.
ICLX	Clock inhibitor. Inhibits signal PHC3 during interrupt or trap.
INCR	Increments adder during multiplication or division.
K2XX	Enables extended addressing upon decoding operation code.
LCYX	Last-cycle flip-flop. Stores the fact that the shift counter has reached its maximum.
LSCX	Long-shift control. Provides control of long shift, multiplication and division sequences.
MC2X	Master clock 2. Provides timing for M/D functions; clock input for flip-flops.
MDN2	Multiply/divide nonshift. Inhibits shift and A bus selection during transfer of remainder.
MPYX	Multiply. Indicates that a multiplication operation is occurring.
NMDX	Negative multiply/divide flip-flop. Stores the sign of multiplier.
OV1X	Overlfow. Output of flip-flop DODX.

Table X-3. Mnemonic Definitions *(continued)*

Mnemonic	Description
PHCX	Phase clock. Enables reset of flip-flop EIMZ.
PHC3	Phase clock inhibit. Enables completion of multiply/divide operation.
ROHX	Reset on halt. Enables clear signal on halt.
SBAX	Sign bit of A register. Enables setting of flip-flops ADOX and NMDX.
SCiX	Shift-counter bit. Indicates number of shift cycles.
SCLI	Inhibits the last shift count until flip-flop LCYX is set.
SCMX	Shift count met. Indicates that shift counter equals U-register bits 0 to 4.
SETB	Set B register. Clocks C-bus data into latches.
SETR	Set R register. Clocks W-bus data into latch; clocks setting of flip-flops ADOX and NMDX.
SGAB	Shift-gate A. Provides bit zero to shift-left gates of arithmetic unit.
SGBC	Shift-gate B. Provides bit 14 to shift-right gates of arithmetic unit.
SHCX	Shift control. Generates signal UMDX and enables setting of flip-flop ADEX.
SHCi	Shift-control bit. Controls the setting of the shift-control flip-flop.
SHFX	Shift. Enables shift operation during multiplication and division
SLBI	Selects B register inverted. Gates inverted B-register data to the G bus.
SLP2	Gates the P register to the G bus.

Table X-3. Mnemonic Definitions *(continued)*

Mnemonic	Description
SLRI	Selects R register inverted. Gates inverted R-register data to the G bus.
SLRX	Selects R register. Gates R-register data to the G bus.
SLR5	Selects R register 5. Gates R-register data to the G bus during division.
SLXI	Selects X register inverted. Gates inverted X-register data to the G bus.
SR14	Selects R-register bit 14. Gates bit 14 of the R register to the G bus during multiplication.
STB5	Set B register. Clocks the setting of the B register.
SUii	Sum bit. Sign bit of the adder.
SYRT	System reset. Clears flip-flop EIM2.
SYii	Sum sign. Enables shift gate A on decoding sum bit.
TOSX	Trap on shift. Enables shift-control signal on trap command.
UiiX	U-register bit. Indicates instruction stored.
UMDX	U-register multiply/divide. Controls the shift portion of the division operation.
WiiX	Memory-data register. Sign bit of the number stored in memory.

SECTION 4
MAINTENANCE

4.1 GENERAL

There are no adjustable components, such as variable resistors or capacitors, on the M/D circuit card. This section provides multiplication and division problems with solutions that can be used to check out the arithmetic and logic operations of the M/D circuits. Refer to section 2 for operating procedures.

The solutions displayed on the computer's control panel should be as indicated in the "results" column. Some of the solutions are not arithmetically correct, because the problem is beyond the machine's capacity. These problems are labeled LCO (logic check only). All problems are shown first in decimal form and repeated in octal form. Negative numbers are in two's complement form. A, B, and R represent the contents of the A register, B register, and memory, respectively.

4.2 MULTIPLICATION PROBLEMS

The format of each multiplication problem is:

Problem in decimal: (multiplier) (multiplicand) = product
Problem in octal: (multiplier) (multiplicand) = product

Before execution:	After execution:
A = all zeros	A = MSB of product
B = multiplier	B = LSB of product
R = multiplicand	R = multiplicand

where, A, B, and R represent the contents of the A register, B register, and memory respectively.

PROBLEM A. Largest positive number squared
(32,767) (32,767) = 1,073,676,289
(77,777) (77,777) = 7,777,600,001

(continued)

Problem:	Result:
A = 000000	A = 077776
B = 077777	B = 000001
R = 077777	

PROBLEM B. Largest negative number squared (LCO)
(−32,768) (−32,768) = 1,073,741,824
(100,000) (100,000) = 6,405,037,000

Problem:	Result:
A = 000000	A = 100000
B = 100000	B = 000000
R = 100000	Overflow

PROBLEM C. Largest negative product
(−32,768) (32,767) = 1,073,709,056
(100,000) (77,777) = 10,000,100,000

Problem:	Result:
A = 000000	A = 100001
B = 100000	B = 000000
R = 077777	

PROBLEM D. Multiplication of like signs
(25,761) (31,345) = 807,478,545
(62,241) (75,161) = 6,010,222,421

Problem:	Result:
A = 000000	A = 060102
B = 062241	B = 022421

PROBLEM E. Multiplication of unlike signs
(−25,761) (31,345) = 807,478,545
(115,537) (75,161) = 11,767,555,357

Problem:	Result:
A = 000000	A = 117675
B = 115537	B = 055357
R = 075161	

(continued)

4.3 DIVISION PROBLEMS

The format for each division problem is:

Problem in decimal: dividend/divisor = quotient + remainder
Problem in octal: dividend/divisor = quotient + remainder

Before execution:	After execution:
A = MSB of dividend	A = remainder
B = LSB of dividend	B = quotient
R = divisor	R = divisor

PROBLEM A. Largest square root
1,073,676,289/32,767 = 32,767
7,777,600,001/77,777 = 77,777

Problem:	Result:
A = 077776	A = 000000
B = 000001	B = 077777
R = 077777	

PROBLEM B. Largest positive dividend and negative divisor (LCO)
1,073,741,824/−32,768 = −32,768
6,405,037,000/100,000 = 100,000

Problem:	Result:
A = 064050	A = 037000
B = 037000	B = 113730
R = 100,000	

PROBLEM C. Division of largest negative numbers
−1,073,709,056/−32,768 = 32,767
10,000,100,000/100,000 = 77,777

Problem:	Result:
A = 100001	A = 100000
B = 000000	B = 077776
R = 100000	

(continued)

PROBLEM D. Division of positive numbers
807,478,545/31,345 = 25,761
6,010,222,421/75,161 = 62,241

Problem:	Result:
A = 060102	A = 000000
B = 022421	B = 062241
C = 075161	

PROBLEM E. Division of negative numbers
−807,478,545/−25,761 = 31,345
11,767,555,357/115,537 = 75,161

Program:	Result:
A = 117675	A = 115537
B = 055357	B = 075160
R = 115537	

PROBLEM F. Division of mixed-polarity numbers
−807,478,545/31,345 = −25,761
11,767,555,357/75,161 = 115,537

Problem:	Result:
A = 117675	A = 102617
B = 055357	B = 115540
R = 075161	

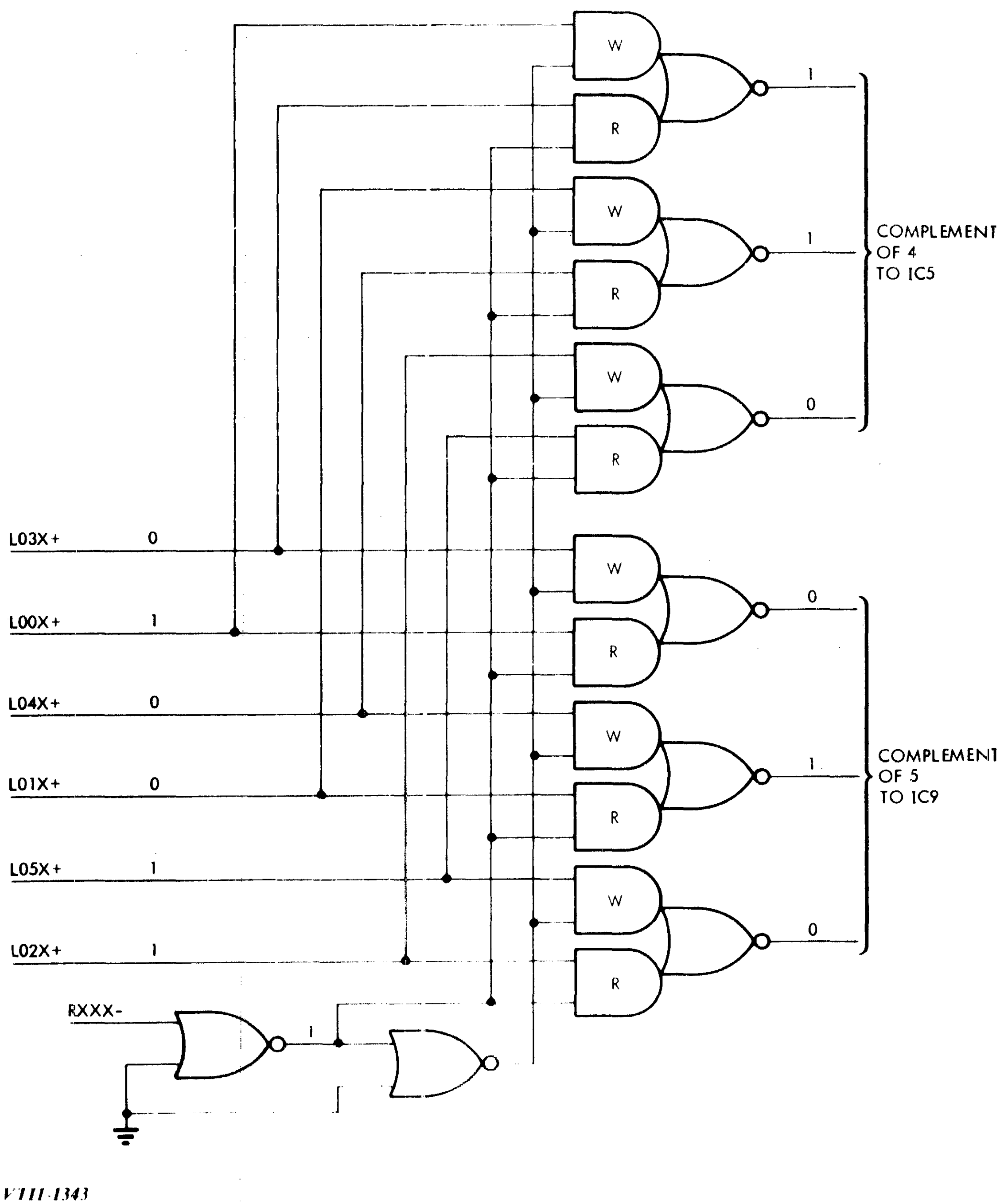


Figure V 12. Read Multiplexing For Octal 45

APPENDIX A

620/L NUMBER SYSTEM

620/L NUMBER SYSTEM

Binary numbers in the 620/L computer are represented in two's-complement form. Single-precision numbers are 15 bits plus the sign bit. The sign bit occupies the most-significant bit position (bit 15). A 0 in the sign position denotes a positive number; a 1 in the sign position denotes a negative number. The negative of a positive number is represented in two's-complement form.

The two's-complement of a number may be found in either of two ways:

a. Take the one's-complement of the number (i.e., complement each bit), and add 1 in the least-significant bit position.

   Example:

+9	0000000000001001
One's complement	1111111111110110
	+0000000000000001
Two's complement (-9)	1111111111110111

b. For an n-bit number (including sign), subtract it from 2^{n+1}.

   Example:

2^{n+1}	10000000000000000
-9(+9)	-0000000000001001
-9	11111111111111111

APPENDIX A
620/L NUMBER SYSTEM

It is generally convenient to express binary numbers by their octal equivalent. This conversion is easily performed by grouping the binary bits by threes, starting with the least-significant bit.

In this 16-bit-word configuration, the range of octal numbers is less than six full digits (000000-0177777). The octal equivalents for the above examples are:

DECIMAL	OCTAL
+9	0000011
-9	0177767

The range of numbers in the 620/L is from −32,768 to +32,767. The zero minus one and plus/minus full-scale numbers are:

BINARY	OCTAL	DECIMAL	
0111111111111111	0077777	+32,767	+FULL SCALE
0000000000000000	0000000	0	0
1111111111111111	0177777	-1	-1
1000000000000000	0100000	-32,768	-FULL SCALE

The negative of the octal equivalent number is found by subtracting the number from 0177777 and adding 1 in the least-significant digit.

Example:

	0177777
-(9)	-000011
	+ 1
(-9)	0177767

In addition or subtraction, it is possible for the results to exceed the ± full-scale range of the machine. For example:

DECIMAL	OCTAL
+21,980	0052734
+11,843	+027103
+33,823	0102037

The negative result is in error. The same type of error occurs if the sum of the two negative numbers exceeds the minus full-scale range:

DECIMAL	OCTAL	
-21,980	0125044	
(+)-11,843	0150675	
-33,823	(1)0075741	31,803

Note that the carry out of the most-significant octal digit position is generally lost. However, to inform the programmer that the true result of an addition/subtraction falls outside the range of the machine, an overflow indicator is provided. The overflow indicator is set if the sign bit changes when two numbers of the same sign are added together (where the sign of the subtrahend is changed in subtraction).

In multiplication, a double-length product is formed in the arithmetic registers (A or B). Since the product cannot exceed 32 bits, overflow will never occur as the result of a multiply. The sign of the product is automatically determined.

Example:

```
            DECIMAL            OCTAL

             21,980             +052734
            x11,843            x+027103
            -------            --------
             65,940             0200624
            87,920             052734
          175,840            0454404
         21,980             0125670
        21,980
        -----------       -------------
        260,299,140      +017410 | 00224
                               A       B
```

The double-length result is accumulated in the A and B registers.

In division, an overflow (underflow) can occur if the divisor is less than or equal to the dividend.

APPENDIX B

POWERS OF TWO

POWERS OF TWO

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

APPENDIX C

OCTAL/DECIMAL INTEGER CONVERSIONS

OCTAL/DECIMAL INTEGER CONVERSIONS

0000	0000
to	to
0777	0511
(Octal)	(Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

1000	0512
to	to
1777	1023
(Octal)	(Decimal)

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

APPENDIX C
OCTAL/DECIMAL INTEGER CONVERSIONS

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

2000 to 2777 (Octal)	1024 to 1535 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

3000 to 3777 (Octal)	1536 to 2047 (Decimal)

4000 to 4777 (Octal) | 2048 to 2559 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	2511
4720	2512	2513	2514	2515	2516	2517	2518	2519
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

5000 to 5777 (Octal) | 2560 to 3071 (Decimal)

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

APPENDIX C
OCTAL/DECIMAL INTEGER CONVERSIONS

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

6000 to 6777 (Octal)	3072 to 3583 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

7000 to 7777 (Octal)	3584 to 4095 (Decimal)

APPENDIX D

OCTAL/DECIMAL FRACTION CONVERSIONS

OCTAL/DECIMAL FRACTION CONVERSIONS

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	.203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	.277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	.212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
.076	.121093	.176	.246093	.276	.371093	.376	.496093
.077	.123046	.177	.248046	.277	.373046	.377	.498046

APPENDIX D
OCTAL/DECIMAL FRACTION CONVERSIONS

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
.000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000021	.000064	.000121	.000308	.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	.000226	.000572	.000326	.000816
.000027	.000087	.000127	.000331	.000227	.000576	.000327	.000820
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	.000233	.000591	.000333	.000835
.000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
.000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000042	.000129	.000142	.000373	.000242	.000617	.000342	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000175	.000156	.000419	.000256	.000663	.000356	.000907
.000057	.000179	.000157	.000423	.000257	.000667	.000357	.000911
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000163	.000438	.000263	.000682	.000363	.000926
.000064	.000198	.000164	.000442	.000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	.000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
.000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	.000957
.000074	.000228	.000174	.000473	.000274	.000717	.000374	.000961
.000075	.000232	.000175	.000476	.000275	.000720	.000375	.000965
.000076	.000236	.000176	.000480	.000276	.000724	.000376	.000968
.000077	.000240	.000177	.000484	.000277	.000728	.000377	.000972

APPENDIX D
OCTAL/DECIMAL FRACTION CONVERSIONS

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001743
.000412	.001014	.000512	.001258	.000612	.001502	.000712	.001747
.000413	.001018	.000513	.001262	.000613	.001506	.000713	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	.001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001068	.000530	.001312	.000630	.001556	.000730	.001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001339	.000637	.001583	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001438	.000671	.001682	.000771	.001926
.000472	.001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
.000474	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
.000476	.001213	.000576	.001457	.000676	.001701	.000776	.001945
.000477	.001216	.000577	.001461	.000677	.001705	.000777	.001949

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Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
ADD	120000	Add to A register	1	2	Yes
ADDE	00612z	Add to A register extended	2	3	Yes
ADDI	006120	Add to A register immediate	2	2	No
ANA	150000	AND to A register	1	2	Yes
ANAE	00615z	AND to A register extended	2	3	Yes
ANAI	006150	AND to A register immediate	2	2	No
AOFA	005511	Add OF to A register	1	1	No
AOFB	005522	Add OF to B register	1	1	No
AOFX	005544	Add OF to X register	1	1	No
ASLA	00420x + n	Arithmetic shift left A n places	1	1 + 0.25n	No
ASLB	00400x + n	Arithmetic shift left B n places	1	1 + 0.25n	No
ASRA	00430x + n	Arithmetic shift right A n places	1	1 + 0.25n	No

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Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
ASRB	00410x + n	Arithmetic shift right B n places	1	1 + 0.25n	No
CIA	1025xx	Clear and input to A register	1	2	No
CIAB	1027xx	Clear and input to A and B register	1	2	No
CIB	1026xx	Clear and input to B register	1	2	No
CPA	005211	Complement A register	1	1	No
CPB	005222	Complement B register	1	1	No
CPX	005244	Complement X register	1	1	No
DAR	005311	Decrement A register	1	1	No
DBR	005322	Decrement B register	1	1	No

x = 0 through 7; z = 4 through 7

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
DIV	170000	Divide AB register 16-bit	1	10-14	Yes
DIVE	00617z	Divide AB register 16-Bit	2	11-15	Yes
DIVI	006170	Divide AB register immediate 16-Bit	2	10-14	No
DXR	005344	Decrement X register	1	1	No
ERA	130000	Exclusive-OR to A register	1	2	Yes
ERAE	00613z	Exclusive-OR to A register extended	2	3	Yes
ERAI	006130	Exclusive-OR to A register immediate	2	2	No
EXC	100xxx	External control function	1	1	No
HLT	000000	Halt	1	1	No
IAR	005111	Increment A register	1	1	No
IBR	005122	Increment B register	1	1	No
IME	1020xx	Input to memory	2	3	No

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Menmonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
INA	1021xx	Input to A register	1	2	No
INAB	1023xx	Input to A and B registers	1	2	No
INB	1022xx	Input to B register	1	2	No
INR	040000	Increment and replace	1	3	Yes
INRE	00604z	Increment and replace extended	2	4	Yes
INRI	006040	Increment and replace immediate	2	3	No
IXR	005144	Increment X register	1	1	No
JAN	001004	Jump if A register negative	2	2	Yes
JANM	002004	Jump and mark if A register negative	2	2-3	Yes

x = 0 through 7; = 4 through 7

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
JAP	001002	Jump if A register positive or zero	2	2	Yes
JAPM	002002	Jump and mark if A register positive	2	2-3	Yes
JAZ	001010	Jump if A register zero	2	2	Yes
JAZM	002010	Jump and mark if A register zero	2	2-3	Yes
JBZ	001020	Jump if B register Zero	2	2	Yes
JBZM	002020	Jump and mark if B register zero	2	2-3	Yes
JMP	001000	Jump unconditionally	2	2	Yes
JMPM	002000	Jump and mark unconditionally	2	3	Yes
JOF	001001	Jump if overflow on	2	2	Yes
JOFM	002001	Jump and mark if overflow on	2	2-3	Yes
JS1M	002100	Jump and mark if SENSE switch 1 on	2	2-3	Yes

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Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
JS2M	002200	Jump and mark if SENSE switch 2 on	2	2-3	Yes
JS3M	002400	Jump and mark if SENSE switch 3 on	2	2-3	Yes
JSS1	001100	Jump if SENSE switch 1 on	2	2	Yes
JSS2	001200	Jump if SENSE switch 2 on	2	2	Yes
JSS3	001400	Jump if SENSE switch 3 on	2	2	Yes
JXZ	001040	Jump if X register zero	2	2	Yes
JXZM	002040	Jump and mark if X register zero	2	2-3	Yes
LASL	00440x + n	Long arithmetic shift left n places	1	1 + 0.50n	No
LASR	00450x + n	Long arithmetic shift right n places	1	1 + 0.50n	No

x = 0 through 7; z = 4 through 7

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
LDA	010000	Load A register	1	2	Yes
LDAE	00601z	Load A register extended	2	3	Yes
LDAI	006010	Load A register immediate	2	2	No
LDB	020000	Load B register	1	2	Yes
LDBE	00602z	Load B register extended	2	3	Yes
LDBI	006020	Load B register immediate	2	2	No
LDX	030000	Load X register	1	2	Yes
LDXE	00603z	Load X register extended	2	3	Yes
LDXI	006030	Load X register immediate	2	2	No
LLRL	00444x + n	Long logical rotate left n places	1	1 + 0.50n	No
LLSR	00454x + n	Long logical shift right n places	1	1 + 0.50n	No
LRLA	00424x + n	Logical rotate left A n places	1	1 + 0.25n	No

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Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
LRLB	00404x + n	Logical rotate left B n places	1	1 + 0.25n	No
LSRA	00434x + n	Logical shift right A n places	1	1 + 0.25n	No
LSRB	00414x + n	Logical shift right B n places	1	1 + 0.25n	No
MUL	160000	Multiply B register 16-Bit	1	10	Yes
MULE	00616z	Multiply B register extended 16-Bit	2	11	Yes
MULI	006160	Multiply B register immediate 16-Bit	2	10	No
NOP	005000	No operation	1	1	No
OAB	1033xx	Output from A and B registers	1	2	No
OAR	1031xx	Output from A register	1	2	No
OBR	1032xx	Output from B register	1	2	No

x = 0 through 7; z = 4 through 7

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
OME	1030xx	Output from memory	2	3	No
ORA	110000	Inclusive-OR to A register	1	2	Yes
ORAE	00611z	Inclusive-OR to A register extended	2	3	Yes
ORAI	006110	Inclusive-OR to A register immediate	2	2	No
ROF	007400	Reset overflow	1	1	No
SEN	101xxx	Sense input/output lines	2	2	Yes
SOF	007401	Set overflow	1	1	No
SOFA	005711	Subtract OFLO from A register	1	1	No
SOFB	005722	Subtract OFLO from B register	1	1	No
SOFX	005744	Subtract OFLO from X register	1	1	No
STA	050000	Store A register	1	2	Yes
STAE	00605z	Store A register extended	2	3	Yes

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Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
STAI	006050	Store A register immediate	2	2	No
STB	060000	Store B register	1	2	Yes
STBE	00606z	Store B register extended	2	3	Yes
STBI	006060	Store B register immediate	2	2	No
STX	070000	Store X register	1	2	Yes
STXE	00607z	Store X register extended	2	3	Yes
STXI	006070	Store X register	2	2	No
SUB	140000	Subtract from A register	1	2	Yes
SUBE	00614z	Subtract from A register extended	2	3	Yes

x = 0 through 7; z = 4 through 7

Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
SUBI	006140	Subtract from A register immediate	2	2	No
TAB	005012	Transfer A to B register	1	1	No
TAX	005014	Transfer A to X register	1	1	No
TBA	005021	Transfer B to A register	1	1	No
TBX	005024	Transfer B to X register	1	1	No
TXA	005041	Transfer X to A register	1	1	No
TXB	005042	Transfer X to B register	1	1	No
TZA	005001	Transfer zero to A register	1	1	No
TZB	005002	Transfer zero to B register	1	1	No
TZX	005004	Transfer zero to X register	1	1	No
XAN	003004	Execute if A register negative	2	2	Yes
XAP	003002	Execute if A register positive	2	2	Yes

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Mnemonic	Octal	Description	WDS/ Inst	Time Cycles	Indirect Address
XAZ	003010	Execute if A register zero	2	2*	Yes
XBZ	003020	Execute if B register zero	2	2	Yes
XEC	003000	Execute unconditionally	2	2	Yes
XOF	003001	Execute if overflow set	2	2	Yes
XS1	003100	Execute if SENSE switch 1 set	2	2	Yes
XS2	003200	Execute if SENSE switch 2 set	2	2	Yes
XS3	003400	Execute if SENSE switch 3 set	2	2	Yes
XXZ	003040	Execute if X register zero	2	2	Yes

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Table F-1. Single-Word Addressing Instructions

Op Code Code	Mnemonic	Instruction	Timing (cycles)
Load/Store Instruction Group			
01	LDA	Load A register	2
02	LDB	Load B register	2
03	LDX	Load X register	2
05	STA	Store A register	2
06	STB	Store B register	2
07	STX	Store X register	2
Arithmetic Instruction Group			
04	INR	Increment and replace	3
012	ADD	Add memory to A register	2
014	SUB	Subtract memory from A register	2
016	MUL	Multiplication	10
017	DIV	Division	10-14
Logical Instruction Group			
011	ORA	Inclusive-OR memory and A register	2
013	ERA	Exclusive-OR memory and A register	2
015	ANA	AND memory and A register	2

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Table F-1. Single-Word Addressing Instructions *(continued)*

Addressing Modes

M Field 11	10	9	Addressing Mode	Operation
0	x	x	Direct	Combine bits 9 and 10 with A field (0-8) to form the effective address (000000-002047)
1	0	0	Relative	Add the A field to the contents of the P register to form the effective address
1	0	1	Indexed (X register)	Add the A field to the contents of the X register to form the effective address
1	1	0	Indexed (B register)	Add the A field to the contents of the B register to form the effective address
1	1	1	Indirect	The A field specifies the location of an address word

Table F-2. Single-Word Nonaddressing Instructions

Op Code Code	Mnemonic	M Field	A Field	Instruction	Timing (cycles)
00	HLT	0	xxx	Halt	1
00	NOP	5	000	No operation	1
00	ROF	7	400	Reset overflow	1
00	SOF	7	401	Set overflow	1

Table F-3. Shift Group Instructions

Format

Op Code	M Field	A Field Bits 8	7	6	5	4-0
00	4	0 = A or B	0 = B	0 = left	0 = arithmetic shift	Shift Count (0-031)
		1 = A and B	1 = A	1 = right	1 = logical rotation	

Shift Instruction Codes

Mnemonic	A Field	Description	Timing (cycles)
ASLB	0000	Arithmetic left shift B	1 + 0.25 nsec
LRLB	0001	Logical left rotate B	1 + 0.25 nsec
ASRB	0010	Arithmetic left shift B	1 + 0.25 nsec
LSRB	0011	Logical right shift B	1 + 0.25 nsec
ASLA	0100	Arithmetic left shift A	1 + 0.25 nsec
LRLA	0101	Logical left rotate A	1 + 0.25 nsec
ASRA	0110	Arithmetic right shift A	1 + 0.25 nsec
LSRA	0111	Logical right shift A	1 + 0.25 nsec
LASL	1000	Long arithmetic left shift A and B	1 + 0.50 nsec
LLRL	1001	Long logical left rotate A	1 + 0.50 nsec
		and B	1 + 0.50 nsec
LLSR	1011	Long logical right shift A	1 + 0.50 nsec
		and B	1 + 0.50 nsec
	1100	Invalid	
	1101	Invalid	
	1110	Invalid	
	1111	Invalid	

Table F-4. Register Change Group Instructions

Format

			A Field Bits							
			Source				Destination			
M Field	8	7	6	5	4	3	2	1	0	Type
05	See	0	0	X	B	A	X	B	A	Unchanged
	note	0	1							Increment
	2	1	0							Complement
		1	1							Decrement

NOTES

1. Multiple source transfer results in an inclusive-OR; multiple source transfer complemented results in a complemented inclusive-OR.

2. Bit 8 = conditional indicator. If bit 8 is zero, the instruction is unconditionally executed. If bit 8 is one, the instruction is executed only if the overflow indicator is on.

Register Change Instruction Codes

Mnemonic	A Field	Description	Timing (cycles)
TZA	0001	Transfer zeros to A register	1
TZB	0002	Transfer zeros to B register	1
TZX	0004	Transfer zeros to X register	1
TAB	0012	Transfer A register to B register	1
TAX	0014	Transfer A register to X register	1
TBA	0021	Transfer B register to A register	1

Table F-4. Register Change Group Instructions *(continued)*

Mnemonic	A field	Description	Timing (cycles)
TBX	0024	Transfer B register to X register	1
TXA	0041	Transfer X register to A register	1
TXB	0042	Transfer X register to B register	1
IAR	0111	Increment A register	1
IBR	0122	Increment B register	1
IXR	0144	Increment X register	1
CPA	0211	Complement A register	1
CPB	0222	Complement B register	1
CPX	0244	Complement X register	1
DAR	0311	Decrement A register	1
DBR	0322	Decrement B register	1
DXR	0344	Decrement X register	1
AOFA	0511	Add overflow to A register	1
AOFB	0522	Add overflow to B register	1
AOFX	0544	Add overflow to X register	1
SOFA	0711	Subtract overflow from A register	1
SOFB	0722	Subtract overflow from B register	1
SOFX	0744	Subtract overflow from X register	1

Table F-5. Jump Group Instructions

Format

Op Code	M Field	A Field 8	7	6	5	4	3	2	1	0
00	1	SS3 on	SS2 on	SS1 on	X = 0	B = 0	A = 0	A< 0	A≥ 0	OF = 1

Note that the jump condition is the logical-AND of all A field bits.

Jump Instruction Codes

Mnemonic	A Field	Description	Timing (cycles)
JMP	0000	Jump unconditionally	2
JOF	0001	Jump if overflow is set	2
JAP	0002	Jump if A register is positive or zero	2
JAN	0004	Jump if A register is negative	2
JAZ	0010	Jump is A register is zero	2
JBZ	0020	Jump if B register is zero	2
JXZ	0040	Jump if X register is zero	2
JSS1	0100	Jump if SENSE switch 1 is set	2
JSS2	0200	Jump if SENSE switch 2 is set	2
JSS3	0400	Jump if SENSE switch 3 is set	2

Table F-6. Jump-and-Mark Group Instructions

Format

Op Code	M Field	A Field Bits 8	7	6	5	4	3	2	1	0
00	01	SS3 on	SS2 on	SS1 on	X = 0	B = 0	A = 0	A< 0	A≥ 0	OF = 1

Jump-and-Mark Group Instructions

Mnemonic	A Field	Description	Timing (cycles)
JMPM	0000	Jump and mark unconditionally	3
JOFM	0001	Jump and mark if overflow is set	2*
JAPM	0002	Jump and mark if A register is positive	2*

* If jump condition is met, 3 cycles.

Table F-6. Jump-and-Mark Group Instructions *(continued)*

Mnemonic	A Field	Description	Timing (cycles)
JANM	0004	Jump and mark if A register is negative	2*
JAZM	0010	Jump and mark if A register is zero	2*
JBZM	0020	Jump and mark if B register is zero	2*
JXZM	0040	Jump and mark if X register is zero	2*
JS1M	0100	Jump and mark if SENSE switch 1 is on	2*
JS2M	0200	Jump and mark if SENSE switch 2 is on	2*
JS3M	0400	Jump and mark if SENSE switch 3 is on	2*

*If jump condition is met, 3 cycles

Table F-7. Execution Group Instructions

Format

Op Code	M Field	8	7	6	5	4	3	2	1	0
					A Field Bits					
00	03	SS3 on	SS2 on	SS1 on	X = 0	B = 0	A = 0	A< 0	A≥ 0	OF = 1

* Note that the execution condition is the logical-AND of all A field bits. The executed instruction must be one word.

Execution Instructions

Mnemonic	A Field	Description	Timing (cycles)
XEC	0000	Execute unconditionally	2
XOF	0001	Execute if overflow is set	2
XAP	0002	Execute if A register is positive	2
XAN	0004	Execute if A register is negative	2
XAZ	0010	Execute if A register is zero	2
XBZ	0020	Execute if B register is zero	2
XXZ	0040	Execute if X register is zero	2
XS1	0100	Execute if SENSE switch 1 is set	2
XS2	0200	Execute if SENSE switch 2 is set	2
XS3	0400	Execute if SENSE switch 3 is set	2

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Table F-8. Immediate Group Instructions

Mnemonic	M Field	A Field	Description	Timing (cycles)
LDAI	06	0010	Load A register immediate	2
LDBI	06	0020	Load B register immediate	2
LDXI	06	0030	Load X register immediate	2
INRI	06	0040	Increment and replace immediate	3
STAI	06	0050	Store A immediate	2
STBI	06	0060	Store B immediate	2
STXI	06	0070	Store X immediate	2
ORAI	06	0110	Inclusive-OR immediate	2
ADDI	06	0120	Add immediate	2
ERAI	06	0130	Exclusive-OR immediate	2
SUBI	06	0140	Subtract immediate	2

Mnemonic	M Field	A Field	Description	Timing (cycles)
ANAI	06	0150	AND immediate	2
MULI	06	0160	Multiply immediate	10
DIVI	06	0170	Divide immediate	10-14

Table F-9. Input/Output Group Instructions

Mnemonic	M Field	A Field	Description	Timing (cycles)
Op Code = 010				
EXC	00	xzz*	External control	1
SEN	01	xzz	Program sense	2
IME	02	0zz	Input to memory	3
INA	02	01zz	Input to the A register	2
INB	02	02zz	Input to the B register	2
INAB	02	03zz	ORed input to ORed A and B registers	2
CIA	02	05zz	Clear and input to the A register	2
CIB	02	06zz	Clear and input to the B register	2
CIAB	02	07zz	Clear and input to the A and B registers	2
OME	03	00zz	Output from memory	3
OAR	03	01zz	Output from the A register	2
OBR	03	02zz	Output from the B register	2
OAB	03	03zz	Output inclusive-OR of A and B registers	2

* x = mode or logical unit number; z = device address

Table F-10. Optional Extended Addressing Instructions

Mnemonic	M Field	A Field	Description	Timing (cycles)
LDAE	06	001x	Load A register extended	3
LDBE	06	002x	Load B register extended	3
LDXE	06	003x	Load X register extended	3
STAE	06	005x	Store A register extended	3
STBE	06	006x	Store B register extended	3
STXE	06	007x	Store X register extended	3
INRE	06	004x	Increment and replace extended	3
ADDE	06	012x	Add memory to the A register extended	3
SUBE	06	014x	Subtract memory from the A register extended	3
MULE	06	016x	Multiply extended	11
DIVE	06	017x	Divide extended	11-15
ORAE	06	011x	Inclusive-OR extended	3
ERAE	06	013x	Exclusive-OR extended	3
ANAE	06	015x	AND extended	3

APPENDIX G

620 RESERVED INSTRUCTIONS

Table G-1. 620/L-06 Teletype Controller Instructions

	Mnemonic	Octal Code	Functional Description
A.	**External Control**		
	EXC 0101	100101	Connect write register to BIC
	EXC 0201	100201	Connect read register to BIC
	EXC 0401	100401	Initialize
B.	**Transfer**		
	OAR 01	103101	Transfer A register to write register
	OBR 01	103201	Transfer B register to write register
	OME 01	103001	Transfer memory to write register
	INA 01	102101	Transfer read register to A register
	INB 01	102201	Transfer read register to B register
	IME 01	102001	Transfer read register to memory
	CIA 01	102501	Transfer read register to cleared A register
	CIB 01	102601	Transfer read register to cleared B register
C.	**Sense**		
	SEN 0101	101101	Write register ready
	SEN 0201	101201	Read register ready

D. **Teletype Command Codes**

Function	Symbol	Code	Typed As
Print Enable	SOM	201	Control and A
Print Suppress	EOT	204	Control and D
Reader On	XON	221	Control and Q
Punch On	TAPE	222	Control and R
Reader Off	XOFF	223	Control and S
Punch Off	TAPE OFF	224	Control and T

Table G-1. 620/L-06 Teletype Controller Instructions *(continued)*

Teletype models are:

620-60B	(33 ASR TM)
620-61B	(35 ASR TM)
620-62B	(35 KSR TM)

Note: External control instructions are for use only with the BIC.

Table G-2. 620/L-10 Multiply/Divide and Extended Addressing Instructions

Mnemonic	Code	Description	Timing (cycles)
A. Divide (one-word instruction)			
DIV	0170000	Divide A and B registers	10-14
B. Multiply (one-word instruction)			
MUL	0160000	Multiply B register	10
C. Extended Addressing (two-word instruction)			
LDAE	000601x	Load A register extended	3
LDBE	000602x	Load B register extended	3
LDXE	000603x	Load X register extended	3
STAE	000605x	Store A register extended	3
STBE	000606x	Store B register extended	3
STXE	000607x	Store X register extended	3
INRE	000604x	Increment and replace extended	4
ADDE	000612x	Add memory to A register extended	3
SUBE	000614x	Subtract memory from A register extended	3

Table G-2. 620/L-10 Multiply/Divide and Extended Addressing *(continued)*

Mnemonic	Code	Description	Timing (cycles)
MULE	000616x	Multiply B register extended	11
DIVE	000617x	Divide A and B registers extended	11-15
ORAE	000611x	Inclusive-OR extended	3
ERAE	000613x	Exclusive-OR extended	3
ANAE	000615x	AND extended	3

Table G-3. 620/L-13 Real-Time Clock Instructions

Mnemonic	Code	Functional Description
EXC 0147	0100147	Enable RTC (enables both increment and overflow interrupts)
EXC 0447	0100447	Disable RTC/initialize (disables both increment and overflow interrupts and resets the interrupt register and divide-by-eight counter)
EXC 0247	0100247	Disable overflow (inhibits overflow interrupt requests)
EXC 0347	0100347	Enable increment/disable overflow (enables increment interrupts and inhibits overflow interrupts)

Table G-4. 620/L-16 Priority Interrupt Module Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 014X*	10014X*	Clear interrupt registers
	EXC 024X	10024X	Enable PIM
	EXC 034X	10034X	Clear interrupt registers and enable PIM
	EXC 044X	10044X	Disable PIM
	EXC 054X	10054X	Clear interrupt registers and disable PIM
B.	**Transfer**		
	OME 04X	10304X	Transfer memory to mask register
	OAR 04X	10314X	Transfer A register contents to mask register
	OBR 04X	10324X	Transfer B register contents to mask register

* X represents the last character of device address. Its value ranges from 0 through 4 or 6, and is determined by jumper connections on the PIM backplane.

Table G-5. 620-20 Buffer Interlace Controller Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 020	100020	Active enable
	EXC 021	100021	Initialize
B.	**Transfer**		
	OAR 020	103120	Load initial register from A
	OBR 020	103220	Load initial register from B
	OME 020	103020	Load initial register from memory
	OAR 021	103121	Load final register from A
	OBR 021	103221	Load final register from B
	OME 021	103021	Load final register from memory
	INA 020	102120	Read initial register into A
	INB 020	102220	Read initial register into B
	IME 020	102020	Read initial register into memory
	CIA 020	102520	Read initial register into cleared A
	CIB 020	102620	Read initial register into cleared B
C.	**Sense**		
	SEN 020	101020	Sense BIC not busy
	SEN 021	101021	Sense abnormal device stop

Table G-6. 620-22, -25 Card Reader Controller Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 0230	100230	Read one card
B.	**Transfer**		
	IME 030	102030	Transfer character to memory
	INA 030	102130	Transfer character to A register
	INB 030	102230	Transfer character to B register
	CIA 030	102530	Transfer character to A register, cleared
	CIB 030	102630	Transfer character to B register, cleared
C.	**Sense**		
	SEN 0130	101130	Sense character ready
	SEN 0230	101230	Sense reader error
	SEN 0330	101330	Sense hopper empty
	SEN 0630	101630	Sense reader ready

Table G-7. 620-30 Nine-Track Magnetic Tape Controller Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 010	100010	Read one record
	EXC 0210	100210	Write one record
	EXC 0410	100410	Write file mark
	EXC 0510	100510	Forward one record
	EXC 0610	100610	Backspace one record
	EXC 0710	100710	Rewind
B.	**Transfer**		
	OME 010	103010	Output memory to magnetic tape buffer
	OAR 0110	103110	Output A register to magnetic tape buffer
	OBR 0210	103210	Output B register to magnetic tape buffer
	IME 010	102010	Input magnetic tape buffer to memory
	INA 0110	102110	Input magnetic tape buffer to A register
	INB 0210	102210	Input magnetic tape buffer to B register
	CIA 0510	102510	Input magnetic tape buffer to A register, cleared
	CIB 0610	102610	Input magnetic tape buffer to B register, cleared
C.	**Sense**		
	SEN 010	101010	Sense tape error
	SEN 0110	101110	Sense buffer ready
	SEN 0210	101210	Sense tape unit ready
	SEN 0310	101310	Sense file mark
	SEN 0410	101410	Sense odd-length record
	SEN 0510	101510	Sense end of tape
	SEN 0610	101610	Sense beginning of tape
	SEN 0710	101710	Sense rewinding

Table G-7. 620-30 Nine-Track Magnetic Tape Controller *(continued)*

	Mnemonic	Code	Functional Description
D.	**Transport Select**		
	EXC2 0110	104110	Select tape drive number 1
	EXC2 0210	104210	Select tape drive number 2
	EXC2 0310	104310	Select tape drive number 3
	EXC2 0410	104410	Select tape drive number 4

Table G-8. 620-31 Seven-Track Magnetic Tape Controller Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 010	100010	Read one record binary
	EXC 0110	100110	Read one record BCD
	EXC 0210	100210	Write one record binary
	EXC 0310	100310	Write one record BCD
	EXC 0410	100410	Write file mark
	EXC 0510	100510	Forward one record
	EXC 0610	100610	Backspace one record
	EXC 0710	100710	Rewind

Table G-8. 620-31 Seven-Track Magnetic Tape Controller *(continued)*

	Mnemonic	Code	Functional Description
B.	**Transfer**		
	OME 010	103010	Output memory to magnetic tape buffer
	OAR 0110	103110	Output A register to magnetic tape buffer
	OBR 0210	103210	Output B register to magnetic tape buffer
	IME 010	102010	Input magnetic tape buffer to memory
	INA 0110	102110	Input magnetic tape buffer to A register
	INB 0210	102210	Input magnetic tape buffer to B register
	CIA 0510	102510	Input magnetic tape buffer to A register, cleared
	CIB 0610	102610	Input magnetic tape buffer to B register, cleared
C.	**Sense**		
	SEN 010	101010	Sense tape error
	SEN 0110	101110	Sense buffer ready
	SEN 0210	101210	Sense tape unit ready
	SEN 0310	101310	Sense file mark
	SEN 0410	101410	Sense odd-length record/sense high density
	SEN 0510	101510	Sense end of tape
	SEN 0610	101610	Sense beginning of tape
	SEN 0710	101710	Sense rewinding
D.	**Transport Select**		
	EXC2 0110	104110	Select tape drive number 1
	EXC2 0210	104210	Select tape drive number 2
	EXC2 0310	104310	Select tape drive number 3
	EXC2 0410	104410	Select tape drive number 4

Table G-9. 620-40, -41, -42, -43 Disc Memory Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 014	100014	Initialize and select interlace mode
	EXC2 014	104014	Initialize and select noninterlace mode
	EXC 0114	100114	Select read mode
	EXC 0214	100214	Select write mode
	EXC 0414	100414	Select address mode zone 0 (first 65K)
	EXC 0514	100514	Select address mode zone 1 (second 65K)
	EXC 0614	100614	Select address mode zone 2 (third 65K)
	EXC 0714	100714	Select address mode zone 3 (fourth 65K)
B.	**Transfer**		
	CIA 014	102514	Clear and input to A register
	CIB 014	102614	Clear and input to B register
	INA 014	102114	Input to A register
	INB 014	102214	Input to B register
	IME 014	102014	Input to memory
	OME 014	103014	Output from memory
	OAR 014	103114	Output from A register
	OBR 014	103214	Output from B register
C.	**Sense**		
	SEN 014	101014	Sense parity error
	SEN 0114	101114	Sense buffer ready
	SEN 0214	101214	Sense disc ready
	SEN 0414	101414	Sense disc register ready

Table G-10. 620-52 Paper Tape System Instructions

	Mnemonic	Code		Functional Description
A.	**External Control**			
	EXC 037	100037	004037	Connect punch to BIC
	EXC 0437	100437	004437	Stop reader
	EXC 0537	100537	004537	Start reader
	EXC 0637	100637	004637	Punch buffer
	EXC 0737	100737	004737	Read one character
B.	**Transfer**			
	OAR 037	103137	040137	Load buffer from A register
	OBR 037	103237	040237	Load buffer from B register
	OME 037	103037	040037	Load buffer from memory
	INA 037	102137	020137	Read buffer into A register
	INB 037	102237	020237	Read buffer into B register
	IME 037	102037	020037	Read buffer into memory
	CIA 037	102537	020537	Read buffer into cleared A register
	CIB 037	102637	020637	Read buffer into cleared B register
C.	**Sense**			
	SEN 0537	101537	010537	Sense buffer ready

Table G-11. 620-65 Dataset Coupler (Synchronous) Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 071	100071	Go to search
	EXC 0171	100171	Connect write buffer to BIC
	EXC 0271	100271	Connect read buffer to BIC
	EXC 0471	100471	Turn on request to send
	EXC 0571	100571	Turn off request to send
	EXC 0671	100671	Go to character format
B.	**Transfer**		
	IME 071	102071	Transfer read buffer to 8 LSB of memory
	INA 071	102171	Transfer read buffer to 8 LSB of A register
	INB 071	102271	Transfer read buffer to 8 LSB of B register
	CIA 071	102571	Transfer read buffer to 8 LSB of A register cleared
	CIB 071	102671	Transfer read buffer to 8 LSB of B register, cleared
	OME 071	103071	Transfer memory 8 LSB to write buffer
	OAR 071	103171	Transfer A register 8 LSB to write buffer
	OBR 071	103271	Transfer B register 8 LSB to write buffer
C.	**Sense**		
	SEN 0171	101171	Write buffer empty
	SEN 0271	101271	Read buffer full
	SEN 0371	101371	Carrier on
	SEN 0471	101471	Clear to send

Table G-11. 620-65 Dataset Coupler (Synchronous) Instructions *(continued)*

Mnemonic	Code	Functional Description

NOTES:

1. All commands listed are used for 201A3 dataset operation.

2. EXC 571 is not necessary for 201B1 (true) full-duplex operation.

3. SEN 371 and SEN 471 will always be ON if Request to Send is left on at both ends when using 201B1. Carrier On also comes ON when outputting using a 201A3 dataset.

4. 201A3 = half-duplex -- two wire. 201B1 = full-duplex -- four wire.

Table G-12. 620-66 Dataset Coupler Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 0471	100471	initialize
	EXC 0271	100271	Select load MCR
B.	**Transfer**		
	IME 071	102071	Transfer read buffer to memory
	INA 071	102171	Transfer read buffer to A register
	INB 071	102271	Transfer read buffer to B register
	CIA 071	102571	Transfer read buffer to A register, cleared
	CIB 071	102671	Transfer read buffer to B register, cleared
	OME 071	103071	Transfer memory to write or MCR buffer
	OAR 071	103171	Transfer A register to write or MCR buffer
	OBR 071	103271	Transfer B register to write or MCR buffer write or MCR

Table G-12. 620-66 Dataset Coupler Instructions *(continued)*

	Mnemonic	Code	Functional Description
C.	**Sense**		
	SEN 0171	101171	Output buffer ready
	SEN 0271	101271	Input buffer ready
	SEN 0371	101371	Call connect
	SEN 0471	101471	Call disconnect
	SEN 0571	101571	Carrier on

NOTES:

1. All commands listed are used for 103A2 dataset operation.

2. Request to Send and Clear to Send could be substituted for SEN 371 and SEN 471 commands if desired.

3. 103A = Dialup; 103F = Private Lines.

4. Device address listed is 71; any other device address may be used according to system requirements.

Table G-13. 620-71 Digital Plotter Controller Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 032	100032	BIC to DPC enable
B.	**Transfer**		
	OME 032	103032	Transfer memory to buffer
	OAR 032	103132	Transfer A register to buffer
	OBR 032	103232	Transfer B register to buffer
C.	**Sense**		
	SEN 0132	101132	Sense buffer ready

Table G-14. 620-80 Buffered I/O Controller Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 0X6Z*	100X6Z	Output control pulse on line selected by X from controller addressed by Z
B.	**Sense**		
	SEN 0X6Z	101X6Z	Test state of line selected by X from controller addressed by Z

Table G-14. 620-80 Buffered I/O Controller Instructions *(continued)*

	Mnemonic	Code	Functional Description
C.	**Transfer**		
	IME 06Z	10206Z	Read input buffer of controller addressed by Z into memory
	INA 016Z	10216Z	Read input buffer of controller addressed by Z into B register
	INB 026Z	10226Z	Read input buffer of controller addressed by Z into B register
	CIA 056Z	10256Z	Clear A register and read controller input buffer addressed by Z
	CIB 066Z	10266Z	Clear B register and read controller input buffer addressed by Z
	OME 06Z	10306Z	Load output buffer of controller addressed by Z from memory
	OAR 016Z	10316Z	Load output buffer of controller addressed by Z from A register
	OBR 026Z	10326Z	Load output buffer of controller addressed by Z from B register

* X = discrete control/sense line (0-07); 6Z = device address (060-067) determined on individual system basis by wiring on the backplane of the expansion chassis.

Table G-15. 620-81 Digital I/O Controller Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC	100XZZ*	Select device address of ZZ and initiate a control pulse on line X
B.	**Sense**		
	SEN	101XZZ	Select device address of ZZ and test logical state of sense response line X

* X = discrete control/sense line (0-07); ZZ = device address (060-067) determined on individual system basis by wiring on the backplane of the expansion chassis.

Table G-16. 620-83 Relay Contact I/O Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 0DA	1000DA	Clear All Outputs. Causes all 16 output contacts to open
	EXC 1DA	1001DA	Clear All Inputs. Returns all input bits that are not being set by contact closure to zero
B.	**Sense**		
	SEN 0DA	1010DA	Sense Contact Closed. This command is available as an option. A specified contact closure will cause a jump to the jump address to occur

Table G-16. 620-83 Relay Contact I/O Instructions *(continued)*

	Mnemonic	Code	Functional Description
C.	**Transfer**		
	INA 1DA	1021DA	Input to A register. Input relay buffered input data on module to A register
	CIA 5DA	1025DA	Clear and Input to A register. Input relay buffered input data on module to A register cleared
	INB 2DA	1022DA	Input to B register. Input relay buffered input data on module to B register
	CIB 6DA	1026DA	Clear and input to B register. Input relay buffered input data on module to B register cleared
	IME 0DA, ADDR	1020DA	Input to memory. Input relay buffered input data on module to memory
	OAR 1DA	1031DA	Output from A register. Output A register to the buffered relay output contacts
	OBR 2DA	1032DA	Output from B register. Output B register to buffered relay contact outputs
	OME 0DA, ADDR	1030DA	Output from memory. Output memory to buffered relay contact outputs

Table G-17. 620-85 Analog Input System Instructions

	Mnemonic	Code	Functional Description
A.	**External Control**		
	EXC 054	100054	Initializes the AIS system
	EXC 0154	100154	The program control mode
	EXC 0254	100254	Places the AIS in the scan mode
	EXC 0354	100354	Start conversion command for the first conversions in the scan mode
B.	**Sense**		
			conversion data is ready. The data must be taken within 40 microseconds of the start of the SEN or the data will be replaced by new conversion data if operating at maximum throughput
	SEN 0154	101154	This SEN instruction indicates that the AIS is requesting a new multiplexer address
	SEN 0254	101254	This SEN instruction indicates that the AIS has completed the multiplexer address scan
C.	**Transfer**		
	OAR, OBR, OME		Data Transfer Out -- In the program mode, DTO occurs for each multiplexing address given to the AIS. In the scan mode, DTO occurs for the first (preset) address

Table G-17. 620-85 Analog Input System Instructions *(continued)*

Mnemonic	Code	Functional Description
C. Transfer *(continued)*		
CIA 054 CIB 054 INA 054 INB 054 IME 054		Data Transfer In -- After each conversion, the data for that conversion is ready and a DTI transfers it into the 620/L if the throughput rate is 20,000. DTI must occur within 40 microseconds of the data ready signal

APPENDIX H

STANDARD CHARACTER CODES

STANDARD CHARACTER CODES

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
@	300	00	32	0-2-8	77
A	301	01	61	12-1	13
B	302	02	62	12-2	14
C	303	03	63	12-3	15
D	304	04	64	12-4	16
E	305	05	65	12-5	17
F	306	06	66	12-6	20
G	307	07	67	12-7	21
H	310	10	70	12-8	22
I	311	11	71	12-9	23
J	312	12	41	11-1	24
K	313	13	42	11-2	25
L	314	14	43	11-3	26
M	315	15	44	11-4	27
N	316	16	45	11-5	30
O	317	17	46	11-6	31
P	320	20	47	11-7	32
Q	321	21	50	11-8	33
R	322	22	51	11-9	34
S	323	23	22	0-2	35
T	324	24	23	0-3	36
U	325	25	24	0-4	37
V	326	26	25	0-5	40
W	327	27	26	0-6	41
X	330	30	27	0-7	42

APPENDIX H
STANDARD CHARACTER CODES

Standard Character Codes *(continued)*

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
Y	331	31	30	0-8	43
Z	332	32	31	0-9	44
[	333	33	75	12-5-8	76**
\	334	34	36	0-6-8	76**
]	335	35	55	11-5-8	76**
↑	336	36	17*	7-8	76**
←	337	37	20	2-8	76***
(blank)	240	40	20	No punch	00
!	241	41	52	11-2-8	51
"	242	42	35	0-5-8	62
#	243	43	37	0-7-8	63
$	244	44	53	11-3-8	60
%	245	45	57	11-7-8	64
&	246	46	77	12-7-8	65
'	247	47	14	4-8	66
(	250	50	34	0-4-8	52
)	251	51	74	12-4-8	53
*	252	52	54	11-4-8	47
+	253	53	60	12	45
,	254	54	33	0-3-8	54
-	255	55	40	11	46
.	256	56	73	12-3-8	51
/	257	57	21	0-1	50
0	260	60	12	0	01
1	261	61	01	1	02

Standard Character Codes *(continued)*

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
2	262	62	02	2	03
3	263	63	03	3	04
4	264	64	04	4	05
5	265	65	05	5	06
6	266	66	06	6	07
7	267	67	07	7	10
8	270	70	10	8	11
9	271	71	11	9	12
:	272	72	15	5-8	67
;	273	73	56	11-6-8	70
<	274	74	76	12-6-8	76**
=	275	75	13	3-8	55
>	276	76	16	6-8	76****
?	277	77	72	12-2-8	76

* End of file for magnetic tape.

** Undefined character (FORTRAN).

*** Form control -- return to column 1 (FORTRAN).

**** Tab control -- skip to column 7 (FORTRAN).

APPENDIX H
STANDARD CHARACTER CODES

TELETYPEWRITER CHARACTER CODES

Character	Internal Code	Character	Internal Code
0	260	P	320
1	261	Q	321
2	262	R	322
3	263	S	323
4	264	T	324
5	265	U	325
6	266	V	326
7	267	W	327
8	270	X	330
9	271	Y	331
A	301	Z	332
B	302	(blank)	240
C	303	!	241
D	304	"	242
E	305	#	243
F	306	$	244
G	307	%	245
H	310	&	246
I	311	'	247
J	312	(	250
K	313	)	251
L	314	*	252
M	315	+	253
N	316	,	254
O	317	-	255

Teletypewriter Character Codes *(continued)*

Character	Internal Code	Character	Internal Code
.	256	LINE FEED	212
/	257	V TAB	213
:	272	FORM	214
;	273	RETURN	215
<	274	SO	216
=	275	SI	217
>	276	DCO	220
?	277	X-ON	221
@	300	TAPE AUX	----
[	333	ON	222
\	334	X-OFF	223
]	335	TAPE OFF	----
↑	336	AUX	224
←	337	ERROR	225
RUBOUT	377	SYNC	226
NUL	200	LEM	227
SOM	201	S0	230
EOA	202	S1	231
EOM	203	S2	232
EOT	204	S3	233
WRU	205	S4	234
RU	206	S5	235
BELL	207	S6	236
FE	210	S7	237
H TAB	211		