UNIVAC® SOLID-STATE 90

Central Processor

Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION

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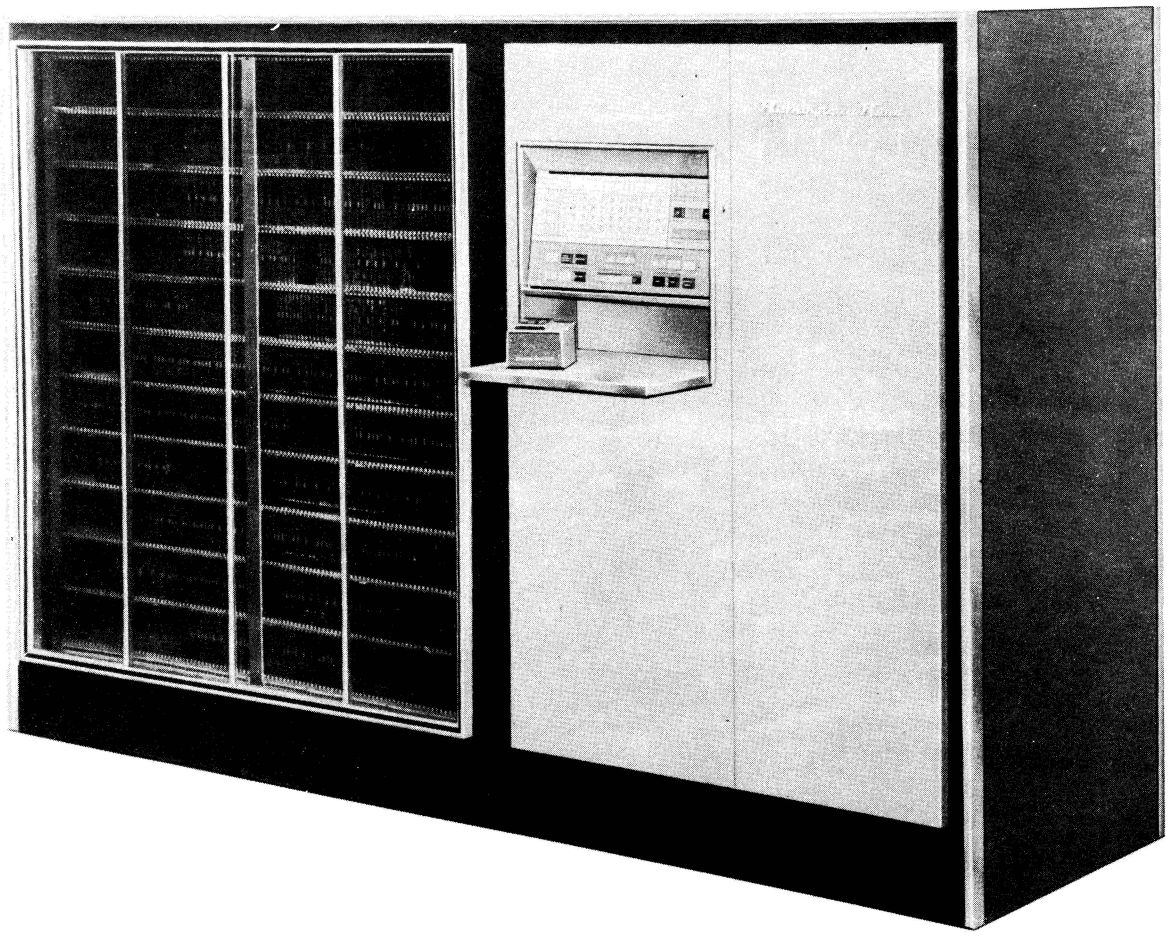


The **CENTRAL PROCESSOR** is the control center of the UNIVAC Solid-State Computer. It houses the arithmetic and logical circuitry, the data storage system, the power supply system, and the operator's panel and keyboard.

This manual provides a functional description of the three basic units which comprise the Central Processor. They are the Storage Unit, the Control Unit, and the Arithmetic Unit.

GENERAL DESCRIPTION

The Storage Unit of the UNIVAC Solid-State Computer is a 5,000 word high-speed magnetic drum. This drum, which is housed in the Central Processor, is used for storing instructions, input/output information and intermediate processing results.

Five thousand 10-digit words provide the drum with a storage capacity of 50,000 digits with an additional 5,000 digit locations available for storage of algebraic signs (plus or minus).

The drum is 5" x 8" in size and rotates at a rate of 17,667 revolutions per minute. This speed is attained by enclosing the drum in a helium atmosphere which acts as a lubricant as well as a coolant. The properties of the helium permit placing the read-write heads close to the drum for greater operating efficiency.

The 5,000 words of main storage include 4,000 fast access and 1,000 high-speed access words. The 5,000 words of main storage is in addition to the buffer storage, sprocket and addressing channels.

Data Rate

The data rate is approximately 707,000 characters per second, or a word time of .017 milliseconds.

Storage Bands

Main storage occupies 25 bands on the storage drum. Two hundred words are stored in each band. Five channels comprise a storage band, with the corresponding binary digits of a character recorded in parallel in these channels. The fifth channel is used to record the parity check bit for each character (See Figure 2).

Successive characters in a word appear in consecutive locations around the drum starting with the space between words, sign, and followed by the 10 character positions, least significant digit first.

Four channels of input-output buffer storage are provided. These channels are accessible only by use of the 81, 46, and 96 instructions. Two channels are used as the print buffer.

Twenty bands of addressable fast access storage are provided. Five bands of addressable high-speed access storage are available.

In addition to the main and buffer storages, one sprocket channel and one addressing band are provided on the storage drum.

Warm-up Time

Approximately eight minutes are required for the drum to reach its operating speed.

Checking

A parity bit for each character being stored is recorded in the main storage and addressing bands of the drum. This check bit is subsequently checked when the word is read. The check bit is never transferred to any of the registers.

BAND NOMENCLATURE AND DESCRIPTION

Figure 1 is a schematic drawing of the magnetic storage drum of the UNIVAC Solid-State Computer. It should be used as a reference when reading the following paragraphs.

Addressing

The memory locations are identified by 4-digit drum addresses numbered consecutively in each band as follows:

First Band	0000 - 0199
Second Band	0200 - 0399
⋮	
Twenty-Fourth Band	4600 - 4799
Twenty-Fifth Band	4800 - 4999
Buffer Bands	Not addressed

The two least significant decimal digits and the least significant bit of the third decimal digit of each drum address indicate the location of each word position around the drum. The two most significant decimal digits indicate the band on the drum.

Six channels are used in timing the machine and addressing the memory. One is a sprocket channel with a pulse recording for each character position around the drum.

The other five channels are used as a band to record serially the two decimal digits and one bit from the third decimal digit representing the address of each word position around the drum. These digits are recorded in the address band one word position ahead of the corresponding memory locations to permit reading or recording the data immediately after the memory search has located the desired address. Certain control signals are also recorded in this band, but they are of no concern to the programmer.

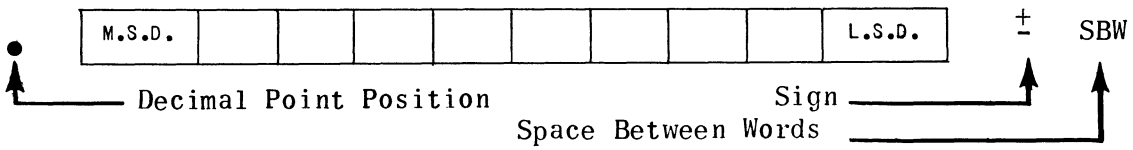
Access Times

Bands one through 20 are fast access bands. Average access time on these bands is 1.70 milliseconds. The maximum access time is only 3.40 milliseconds.

Bands 21 through 25 (4000-4999) are high-speed access bands. Average access time on these bands is .425 milliseconds. The maximum access time is only 85 milliseconds. This high-speed access is achieved by spacing four read-write heads, 50 words apart, around the high-speed access bands. The fast access bands are equipped with one read-write head per band.

Decimal Point

Information is stored on the drum in increments of 10-digit words (plus sign). The computer considers the decimal point to lie just to the left of the most significant digit. Thus, all words are less than unity in absolute value.



The Buffer Area

The buffer area of the magnetic drum contains the individual buffers for each station in the peripheral units. A common buffer is utilized for the Read-Punch Unit and the High-Speed Reader. Different locations within this buffer are assigned to the respective reading and punching stations. The High-Speed Printer utilizes a separate buffer.

Average access time for the buffer areas is .212 milliseconds. This rate is achieved by placing eight read-write heads around the periphery of each buffer band.

The function of the buffer area is to increase the transfer speed of information between the input/output units and the Central Processor. Once these data transfers have been effected, the control circuits (of the Central Processor) can then take over the job of independently reading, punching, moving the cards, and printing the results. During these latter operations, the Processor is free to continue simultaneous computing.

Figure 3 is a schematic drawing showing the interrelationships between the Central Processor, the buffer areas, and the peripheral units. Details of the buffer operations, including a discussion of the appropriate instruction commands, are found in other manuals of this series.

MACHINE LANGUAGE

The UNIVAC Solid-State Computer operates on numerical information represented in a bi-quinary type decimal system. Words in the machine consist of 10 decimal digits plus sign with a space between words. Numbers are carried as values less than one with a plus or minus sign. Data read from cards and data to be punched in cards are stored as a card image (two words per 10 columns). The manipulation of words containing both data and control punches is explained in subsequent sections.

Bit Combinations and Order of Magnitude

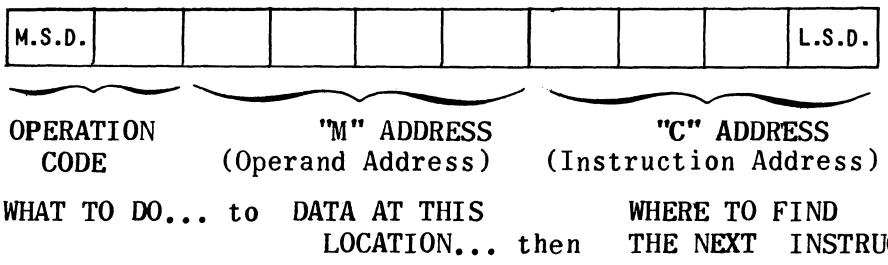
Alpha-numeric information from cards can be compared for equality and transferred in the Remington Rand code. Numeric data words must be translated from Remington Rand code to machine code before arithmetic and "greater than" comparison operations can be performed on them. The decimal digits are represented in machine language by four bits. The order of magnitude (from lowest to highest) of the 16 possible bit combinations is as follows:

0111	i	(ignore)	1000	5
0110	Δ	(delta)	1001	6
0101	-	(minus)	1010	7
0000	0		1011	8
0001	1		1100	9
0010	2		1111	. (period)
0011	2		1110	t (tabulator)
0100	4		1101	r (carriage return)

An odd parity bit is used with each digit stored on the drum. Checking takes place on transferring from the drum.

Instruction Code Format

The machine uses a 1½ address system with one instruction per 10-digit word (the sign digit is not used in instructions) in the form shown below:



The "m" address is usually the address of a word in storage. The "operation code" tells the computer what to do with this word; and the "c" address is the storage location of the next instruction word. These fields may have different significance for some special instructions.

When a word is transferred from a storage location or register, the contents of the storage location or register from which the word was transferred remain unchanged.

When a word is transferred into a storage location or register, the previous contents of the storage location or register are erased, except in the 20 and 35 instructions.

The complete instruction list and a detailed description of the instructions are contained in the manual in this series entitled "Instruction Codes."

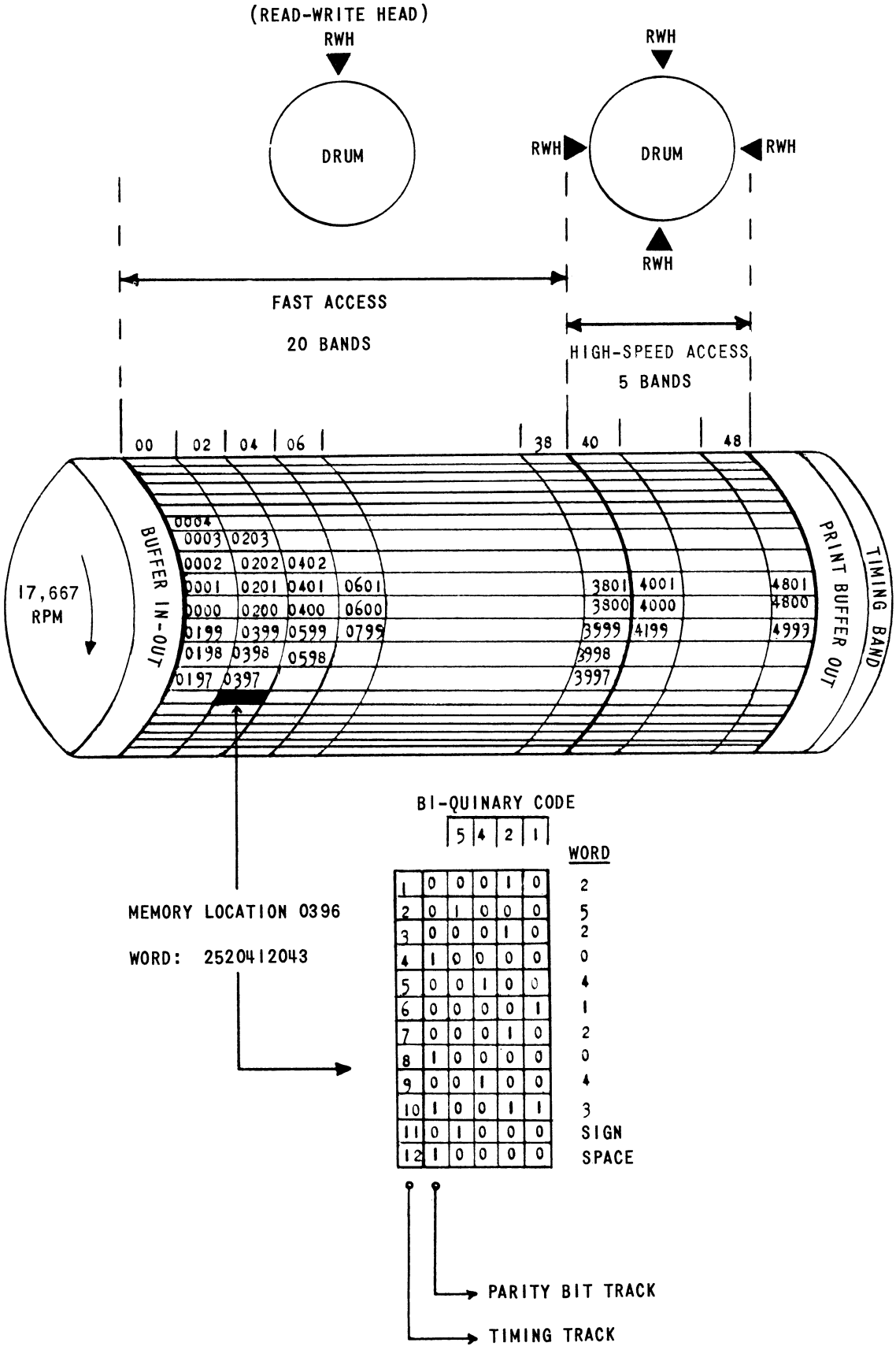


Figure 1. Magnetic Storage Drum

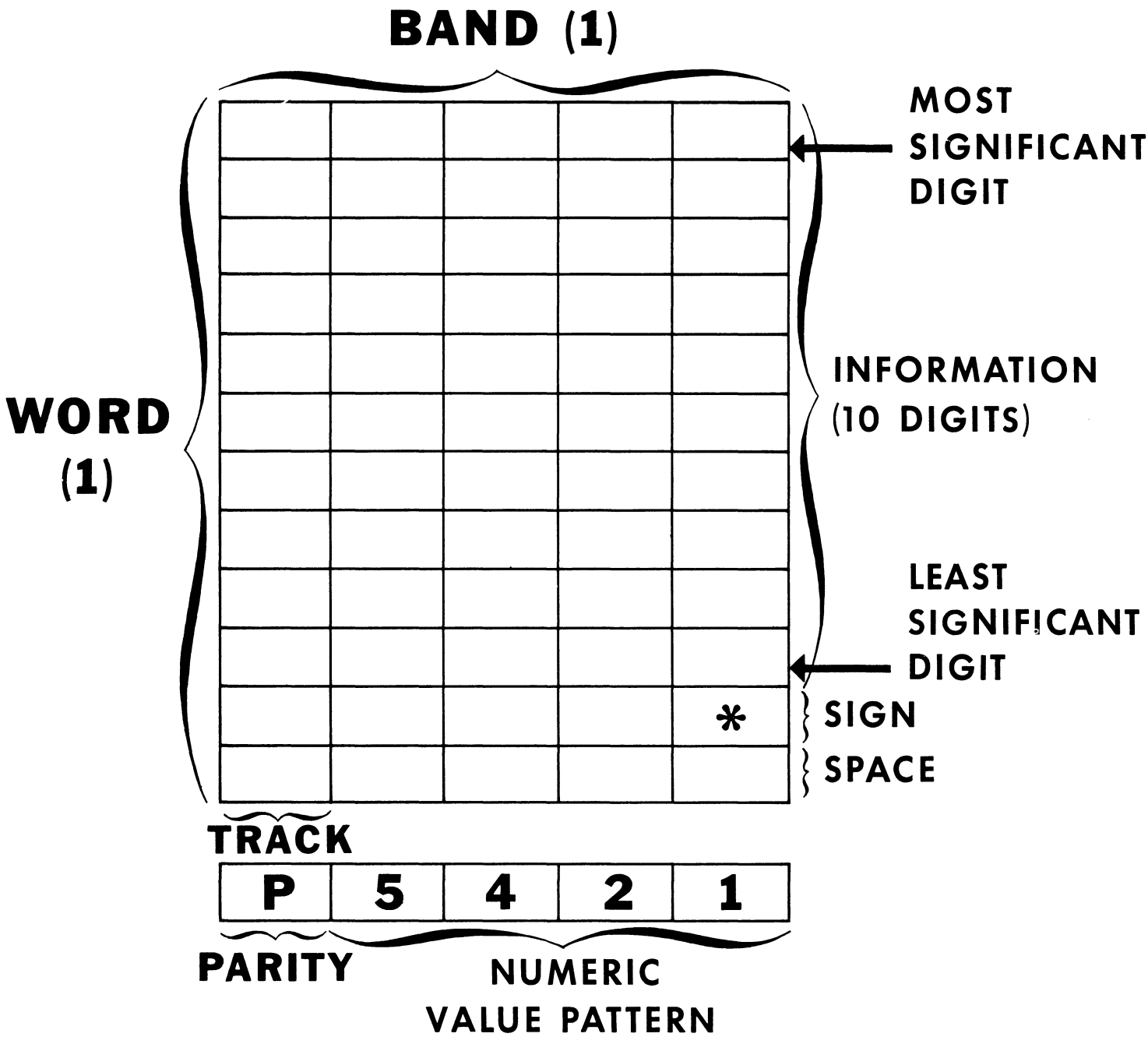


Figure 2. Storage Format

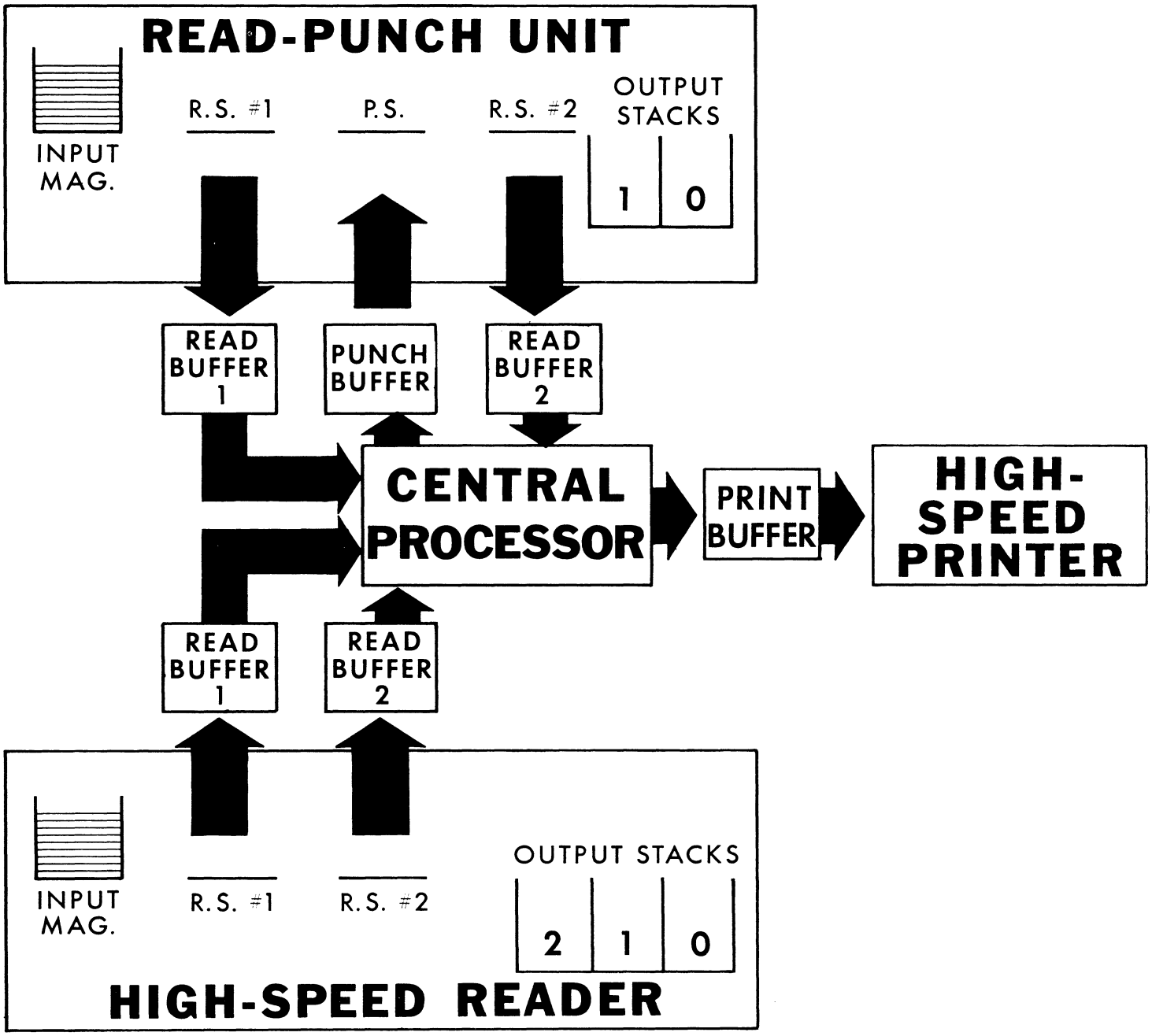


Figure 3. Buffer Operation

GENERAL DESCRIPTION

The Control Unit controls the operations of all units of the UNIVAC Solid-State Computer. The major components of the Control Unit are register C, the Static Register, the instruction decoder, the function encoder, and the operator control panel and keyboard.

Complete instruction words read from storage are stored in register C. Parts of these words are compared with storage addresses in the adder and comparator circuits in order to locate stored information or other instruction words. The two instruction code digits of the instruction word stored in register C are also stored in the Static Register (See Figure 4). These digits are interpreted by the instruction decoder and converted into a function signal. This function signal is converted into other function signals by the function encoder. The function signals control various computer circuits which cause the stored instruction to be executed.

The operator control panel contains pushbutton switches and indicators which enable the operator to manually control the automatic operation of the UNIVAC Solid-State Computer. Abnormal conditions in any of the units of the system are indicated on the panel. A keyboard on the panel enables the operator to type information into the Central Processor or alter the stored program. The operating panel and keyboard are not discussed in this manual but are subjects of another manual in this series.

INSTRUCTION CYCLE

A three or four step cycle is associated with each instruction, depending upon whether an operand is required from drum storage. If setting-up the instruction is considered the starting point, the instruction cycle is:

Staticize the Instruction	Search for the Operand	Execute the Instruction	Search for the next Instruction
(1)	(2)	(3)	(4)

Staticize the Instruction (1)

The instruction located by the previous search (4) is transferred from the drum location to the Static Register (operation code only) and register C (the entire word). This step requires one word time which is .017 milliseconds.

Search for the Operand (2)

If the first address part of the instruction does not refer to a drum storage location or register, this step is ignored and no time is required. If it does refer to drum storage, the address of the next available storage location on the drum is compared with the first address part of the contents of rC every word time until a match is obtained. Register C contains the entire instruction. If an operand is required from storage, this step requires a minimum of one word time and a maximum of 200 word times.

Execute the Instruction (3)

The operation indicated in the instruction is performed. The time required depends upon the type of operation to be performed.

Search for the Next Instruction (4)

Every word time, the address of the next available storage location on the drum is compared with the second address part of the contents of rC until a match is obtained. This step requires a minimum of one word time (when minimum latency coding is used) and a maximum of 200 word times.

CONTROL REGISTERS

The Static Register is a two digit register which contains only the actual instruction command, while register C contains the complete instruction word (See Figure 4).

PROGRAMMING CONTROL

Since all instructions, including those affecting the input/output units, are executed by the Control Unit of the Central Processor, the programmer retains complete control of all operations throughout the program.

GENERAL DESCRIPTION

All arithmetic and comparison operations are performed in the Arithmetic Unit of the Central Processor. Although the Arithmetic Unit has many components, the most important components are the three arithmetic registers, and the adder and comparator circuits (See Figure 4).

ARITHMETIC REGISTERS

The three arithmetic registers are registers A, L, and X. Each stores temporarily the 10 digits of a word, which is usually the operand in an arithmetic instruction. The operands are operated upon in the adder and comparator circuits, and the results are returned to one of the three registers.

All three arithmetic registers are directly addressable. The addresses used are as follows:

Register A	000K
Register L	000Y
Register X	000T

The letter designations facilitate key-punching and program loading. The registers can be addressed for data by many instructions and can be addressed for the next instruction by all the instructions. The only restrictions are that a register address cannot be used in the m portion of the 50, 60, and 65 instruction orders, nor in an m or c portion of an instruction which is <u>not</u> used to address a one word storage.

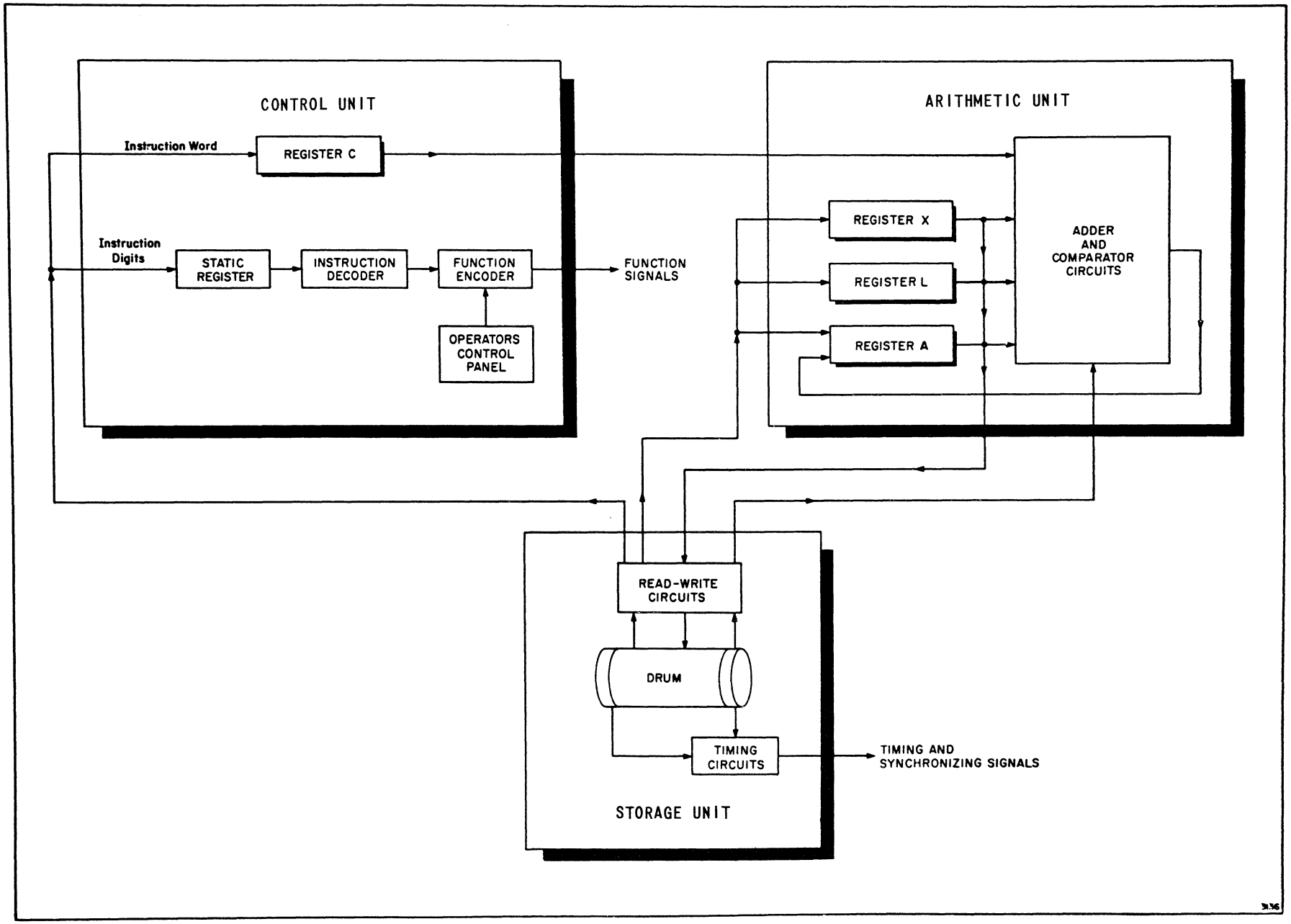


Figure 4. Central Processor Units

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