Copy # 85

UNIVAC III

REMINGTON RAND UNIVAC
Division of Sperry Rand Corporation
Philadelphia, Pa.

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00000 INTRODUCTION

Univac III is a medium cost, high performance electronic data processing system designed to provide maximum productivity in a wide variety of business applications. The system is modular throughout, flexible in the variety and numbers of peripheral units which can be attached, and utilizes in its construction solid state circuitry of proven reliability.

00100 UNIVAC III FEATURES

SOLID STATE CIRCUITRY	DECIMAL ARITHMETIC
AIR COOLING	BINARY ARITHMETIC
MODULARITY	MULTIPLE SHORT WORD OPERANDS
SINGLE ADDRESS INSTRUCTIONS	INDEX REGISTERS
FIELD SELECTION	HIGH SPEED MAGNETIC TAPES
INDIRECT ADDRESSING	SCATTER READ-WRITE

In addition an optional Uniservo II compatibility provision provides a means of communication with other Univac Computers and with existing off-line peripheral devices.

01000 SYSTEMS CONFIGURATIONS

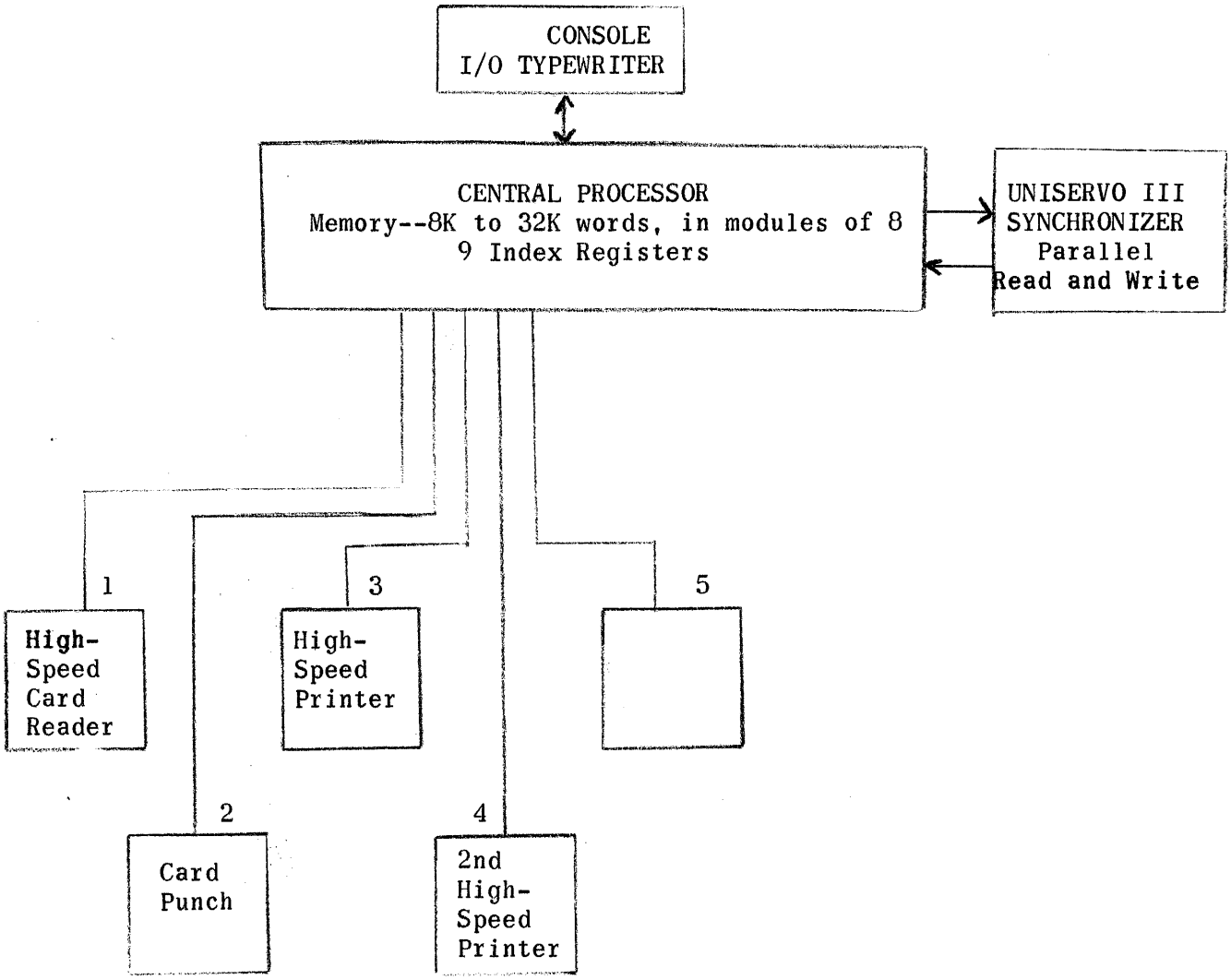
Minimal and Maximal Systems are shown in the first two of the following charts. The third chart shows the tape line configurations available.

It should be noted that a Uniservo Power Supply must be provided for each Uniservo III Synchronizer. One of these Power Supplies may also serve the tape units attached to the Uniservo II Synchronizer, though not more than 16 servos may be attached to a single Power Supply. The Uniservo II Synchronizer accomodates a maximum of six tape units.

These charts are functional only, and are not to be construed as indicative of packaging or floor arrangements, which are discussed in Installation Specifications (Section 90000).

01000 SYSTEMS CONFIGURATIONS

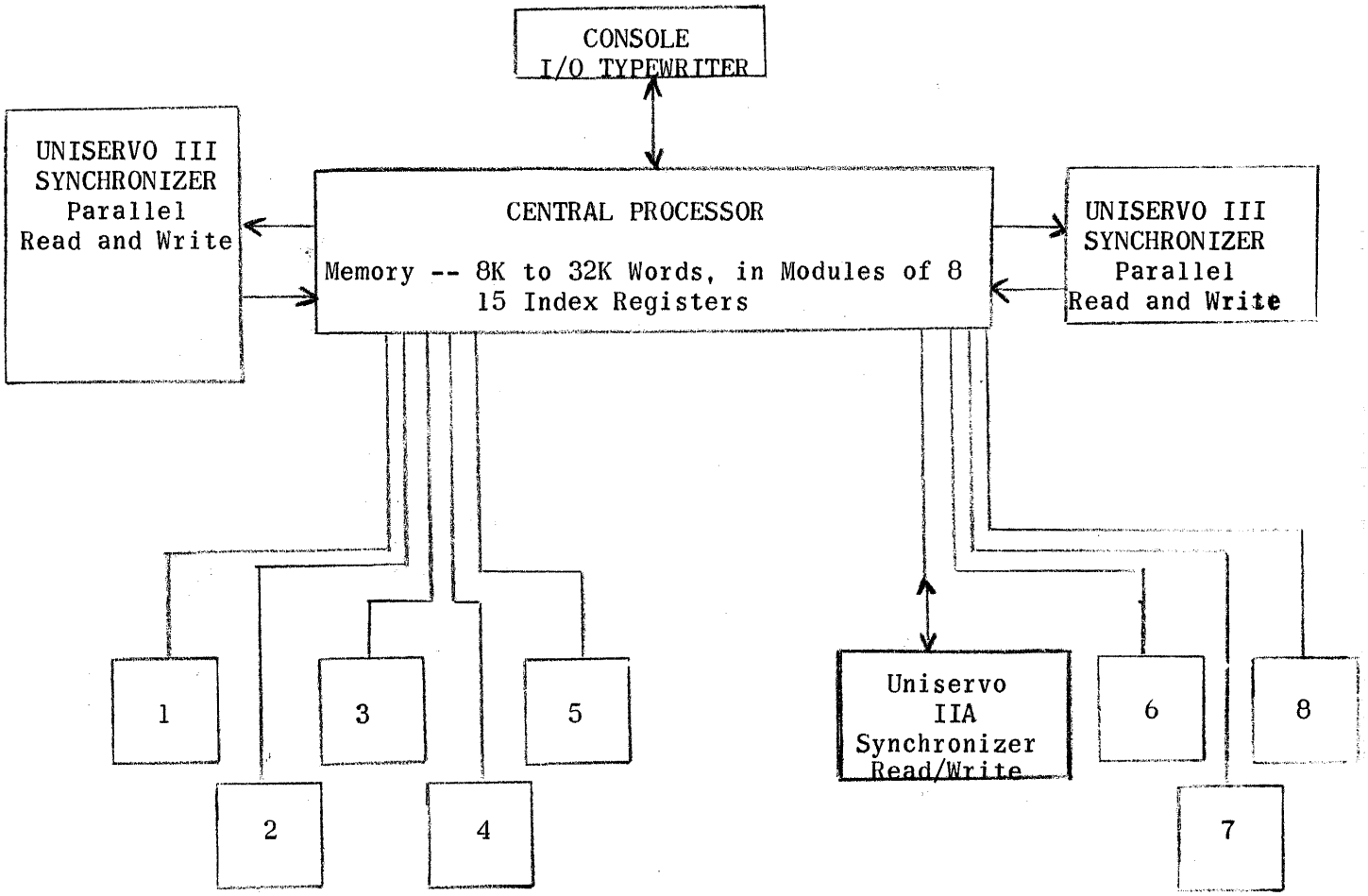
MINIMAL MARKETABLE SYSTEMS



The Input/Output units shown on the general purpose channels are merely intended to serve as examples. Any such unit may be attached to any of the channels.

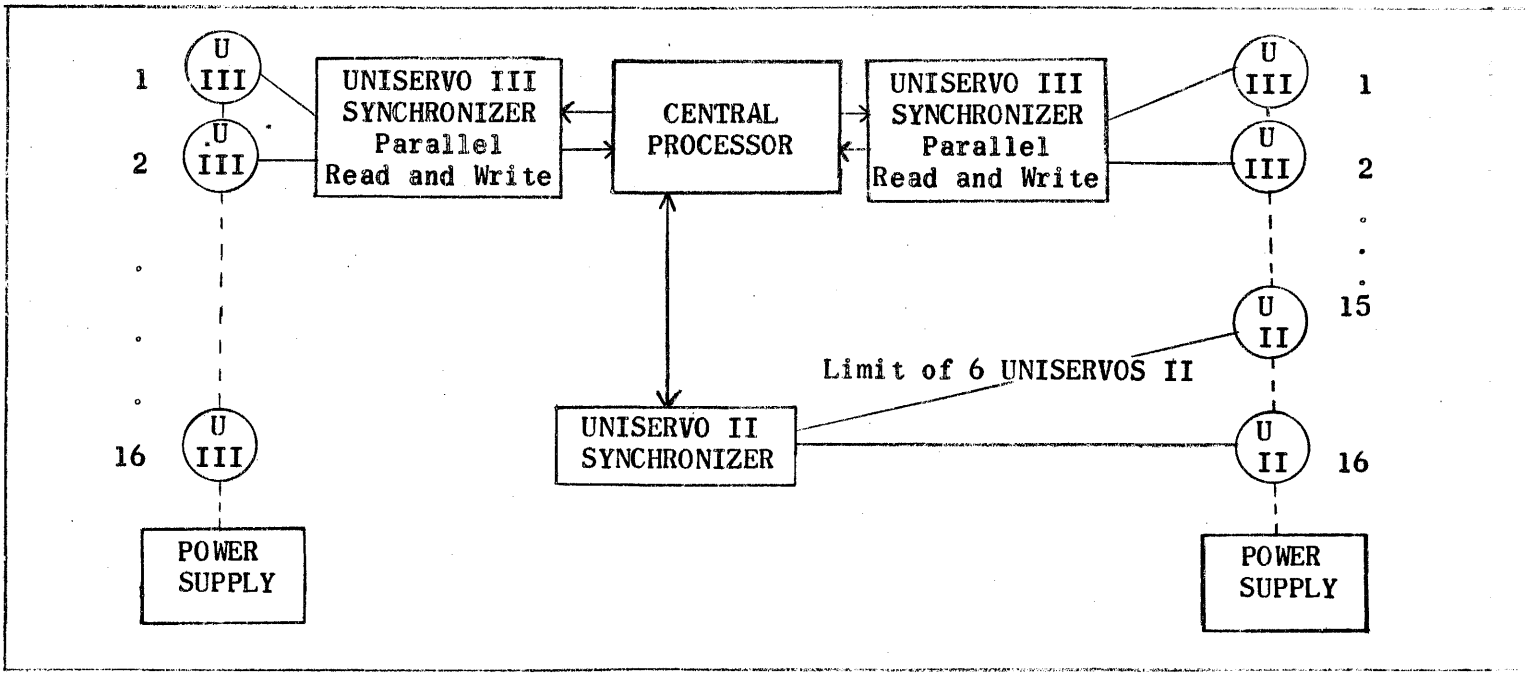
01000 SYSTEMS CONFIGURATIONS

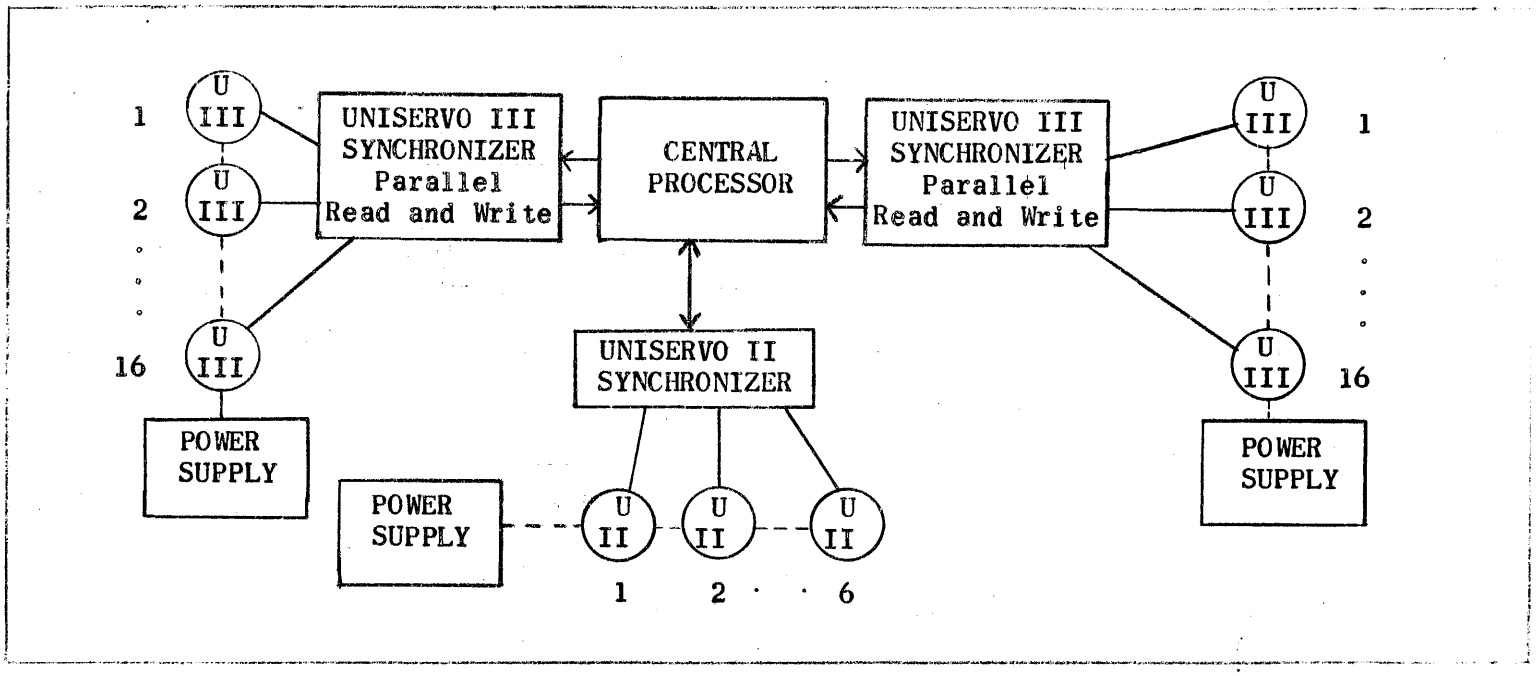
MAXIMUM SYSTEM



PERIPHERAL UNITS RATING CHART	
Maximum rating, all channels -- 90	
Unit	Rating
Uniservo III, Parallel Read-Write	31.0
Uniservo IIA, Read or Write	2.9
High-Speed Card Reader, 700 CPM	3.6
Card-Punch, 300 CPM	2.5
High-Speed Printer, 700 LPM	1.6
Punched Paper Tape Reader	1.0 *
Punched Paper Tape Punch	
Uniservo IIIC, Read or Write	9.1
FASTRAND	20.0
28 Channel Punched Paper Tape Reader	.04
* Maximum for non-stop read.	

01000 SYSTEMS CONFIGURATIONS --- TAPE LINE CONFIGURATIONS





11000 BASIC CENTRAL PROCESSOR CHARACTERISTICS

11100 CHARACTERISTICS OF MAGNETIC CORE STORAGE

11110 PRINCIPLE OF OPERATION

The core storage system used involves the magnetization of a very small (.05" OD) doughnut shaped core of ferrite material.

To store, a 1 or a 0 a ferrite core is magnetized in one of its two possible directions.

Recovery of the stored information is obtained by reverting the core to its 0 magnetization condition. If a 0 has been stored no change in state takes place. However, if a 1 has been stored the resultant change of direction to 0 is detected and interpreted as a 1.

11120 CONSTRUCTION

The ferrite cores are arranged in planes of 4,096 cores in a square of 64 x 64. Wires thread this area in cartesian coordinates such that the intersection of 2 wires determines a specific core. Another wire traverses all cores and is used to sense the stored information. Another wire which also threads all cores is used to determine whether the half currents present in the cartesian coordinate wires shall be capable or incapable of flipping a core.

Twenty-seven of these planes are arranged in a stack so that 27 planes are available to store the 25 information bits of the word together with 2 checking bits. Thus, there is within the stack the ability to store 4,096 words.

The memory is available in multiples of 8,192 words yielding a memory size of 8,192 words, 16,384 words, 24,576 words and 32,768 words.

11130 OPERATING SPEED

The memory cycle (address selection, read out, and regenerate) is accomplished in each 4 microsecond machine cycle.

11200 CHECKING PHILOSOPHY

11210 ERROR DETECTION--CENTRAL PROCESSOR

The Univac III word contains two bit-positions, in addition to the 25 positions for representation of data, which are used in checking data transfers and arithmetic. The two positions contain the bits required to produce a 27-bit binary number with residue 0, modulo 3. These so-called check bits occupy positions 26 and 27 of the Univac III word.

Congruence arithmetic provides the basis for checking arithmetic operations as the residue, modulo 3, of the result of an arithmetic operation performed on two numbers should be congruent to the result of performing the same operation on the residues of the two operands. This is the consideration upon which "casting out elevens", occasionally used in checking long-hand arithmetic, is based.

The addressing of the correct word in memory is checked by comparing an odd or even indication (a 28th bit sent from memory with the data accessed) with an odd or even indication developed by the Central Processor from the address in the Memory Switch Register.

In all cases, error detection causes an automatic program interrupt as discussed elsewhere.

11220 ERROR DETECTION--INPUT-OUTPUT EQUIPMENT

The Univac III high-speed magnetic tape system, employing Uniservo III, incorporates a check-read head and circuitry to read information and check its parity (The check-bits described in 11210, above), immediately after it is written, thus minimizing the possibility of producing an unreadable output tape.

The Univac III compatible tape equipment includes those checking features which are standard to all Univac systems. Card equipment and other peripheral devices are designed with special checking circuits to ensure good reliability.

Errors in input-output equipment operation are detected by program tests and in certain cases by program interrupts as discussed elsewhere.

11300 AUTOMATIC PROGRAM INTERRUPT

11310 GENERAL DEFINITION AND PURPOSE

The Program Interrupt Feature causes, upon recognition of various special conditions, automatic interruption of the program in progress, storage of the contents of the control counter so that the address of the program step following that after which interruption took place is available for a return jump, and transfer of control to a special sequence of instructions designed to investigate the reason for the interruption and to take suitable action.

This feature provides the programmer with an efficient technique for optimal use of the input/output units, and facilitates appropriate programmed data manipulation when an error is recognized anywhere in the system.

The three classes of interrupt included are, in descending order of priority, Processor Error Interrupt, Contingency Interrupt and Input/Output Interrupt, each of which is explained in a subsequent paragraph.

11320 DESCRIPTION OF OPERATION OF INTERRUPTS

When a condition causing interrupt arises, the following occurs:

1. One or more program testable indicators in the Central Processor are set to indicate the specific reason for interrupt. For all UNISERVO Models, the High Speed Printer and the Paper Tape Reader-Punch, the following conditions apply:

   a. If a Function Specification (FS) specifies program interrupt, it will occur upon the successful completion of the execution of that FS.

   b. The Successful Completion Interrupt Indicator (Bit 2) is not set in combination with Error and Fault Indicators as the result of execution (whether successful or not) of an FS.

   c. In the event that an FS is completed prior to the program resetting the Bit 2 indicator set by a previous FS completion, the Bit 2 indicator will not be set until the program has reset the first indication. No further FS's will be accessed by the synchronizer until such time as the delayed setting of the Bit 2 indicator takes place.

   For the Card Reader and Punch, if interrupt is specified, it occurs unconditionally when the execution of the FS is initiated.

   All General Purpose Channels have circuits to delay the setting of the Bit 2 indicator if the program has not reset the indicator for a previous successful completion. This provides the ability to connect those peripherals requiring the delay to any channel as well as to any future synchronizers which might be connected.

2. For each class of interrupt, there is an Interrupt Mode Indicator. When one of these is set, interruptions of that class, or of any class of lower priority, cannot take place, though indicator settings, as described in 1., above will take place when appropriate conditions arise. These Interrupt Mode Indicators cannot be set, reset or tested with instruction; their functions are controlled automatically.

11320 (Continued)

At the end of execution of each instruction in the processor, the Interrupt Indicators and the Error Indicators are examined, in groups according to class of interrupt, in descending order of priority. If any of these indicators is found to be set, and if the Interrupt Mode Indicators for that class and for classes of higher priority are not set, interruption will actually take place.

At this time, the Interrupt Mode Indicator, for the class of interrupt effective, is set automatically.

3. The address of the instruction which should follow the one completed when interruption actually takes place is stored in a fixed location in the core memory (the location is addressable), and positions 16 through 25 of this location are cleared to binary zeros. The contents of the control counter are changed to a specific value associated with the class of interrupt effective. The specific locations and decimal values are as follows:

Class of Interrupt	Memory Location for Storage of Control Counter	Address to Which Control Counter is Set
Processor Error	0016	0017 *
Contingency	0018	0019 *
Input/Output	0020	0021

*These locations will normally hold unconditional transfer instructions to the appropriate error or contingency routines.

Transfer is thus effected to a program which will investigate the nature of the interruption and take suitable action.

4. In the program for investigation of the nature of an input/output interruption, the indicators (Interrupt Indicators and Error Indicators) are tested, in an appropriate sequence to isolate the synchronizer which called for the interruption. These indicators are not reset by testing. Any combination of indicators for a single synchronizer may be tested simultaneously. If any one of the combination is found to be set, the contents of the control counter will be set to CC+1; if none is set, the control counter is changed to CC+2.

An attempt to test the condition of non-existent indicators will not cause an error condition, nor will it result in recognition of a set condition unless an actual indicator is tested simultaneously and found to be set. The indicators for any one synchronizer are addressed by "1" bits in the field comprising bit positions 1 through 10. Each indicator for the synchronizer is associated with a unique bit position, and these positions have been assigned so that the Interrupt Indicators for all synchronizers are associated with a unique bit position, as are the Standby Interlock Indicators (which do not cause interruptions). Hence, the isolation of the synchronizer calling for interrupt may be accomplished by performing a series of Indicator tests using a fixed pattern in positions 1 through 10--specifically, all "1" bits except in the position associated with the Standby Interlock Indicators.

11320 (Continued)

A suitable sequence for the test instructions follows:

a. For each synchronizer in turn, test the combination of all indicators. This may be accomplished by using a test instruction with "1's" in all positions from 1 through 10, except that related to the standby location interlock.
b. When a "set" condition is found, determine whether or not an error condition exists by testing all Error Indicators for the synchronizer involved by use of a test instruction with ones (1's) in all of positions 1 through 10 except those positions denoting the Interrupt Indicator and the Standby Location Interlock Indicator. If no Error Indicator is set, the synchronizer has successfully completed an instruction.
c. If an error condition is found to exist, it must be analyzed in further detail by testing of individual error indicators for the synchronizer.

During the analysis of indicators, none should be reset, as this might allow the synchronizer to attempt execution of the instruction in its standby location prior to completion of the routine which accomplishes adjustment for error. (For any specific synchronizer, various patterns of set error indicators indicate specific error conditions, as described in detail below, and these indicators are set simultaneously at the time of occurrence of an error. Hence no information relating to errors is lost to the programmer if the Error Indicators are allowed to remain set until completion of the error manipulations.)

When the above analysis of indicators, together with any necessary processing because of detected errors, has been completed, an input/output instruction may be loaded into the standby location associated with the synchronizer concerned if its Standby Location Interlock Indicator is not set.

This should be followed by resetting of all the resettable indicators for the specific synchronizer and an unconditional transfer to the address stored from the control counter at the time of interruption.

The reset instruction for Interrupt and Error Indicators automatically resets the Interrupt Mode Indicator for the class of interrupt involved, provided that the instruction actually reset one or more set indicators. Interrupts for all classes are inhibited during the execution of the Reset instruction (61 or 65) and until the end of the execution of the next instruction.

5. When the transfer back to the main program is attempted, as indicated in 4., above, the Interrupt Indicators and the Error Indicators for all classes of interrupt are automatically tested. If any is found to be set, the instruction in the memory location to which the program has been directed by the unconditional transfer will not take place. The contents of the control counter (the address of the instruction whose execution is blocked) is placed in the fixed memory location for the class of interrupt of highest priority for which Interrupt or Error Indicators were found set by the automatic testing process, and control is transferred to the location (see table 3., above) which holds the transfer to the appropriate interrupt routine.

11320 (Continued)

When this automatic process directs return to an interrupt routine, the appropriate Interrupt Mode Indicator (not testable) is set, to block further interruptions of the same class, or of classes with lower priority.

6. During the course of operation of any program within an Interrupt Mode established by setting of the Interrupt Mode Indicator for a class of interrupt, occurrence of an interrupt of higher priority is always possible. Such interruptions cannot be blocked by programming.

7. It is, however, possible to block the occurrence of input/output interruptions. A special Inhibit-Input/Output-Interrupt Indicator which can be set, reset and tested by program instructions, is provided for this purpose. When it is set, neither storage of the control counter nor transfer of control occurs automatically, as is the case when an actual interruption occurs, but when it is reset by the appropriate instruction, the condition of the other input/output indicators is automatically investigated, as in 5., above, and control is transferred to the input/output routine if any Input/Output Error or Interrupt Indicators were set during the time the Inhibit-Input/Output-Interrupt Indicator was set.

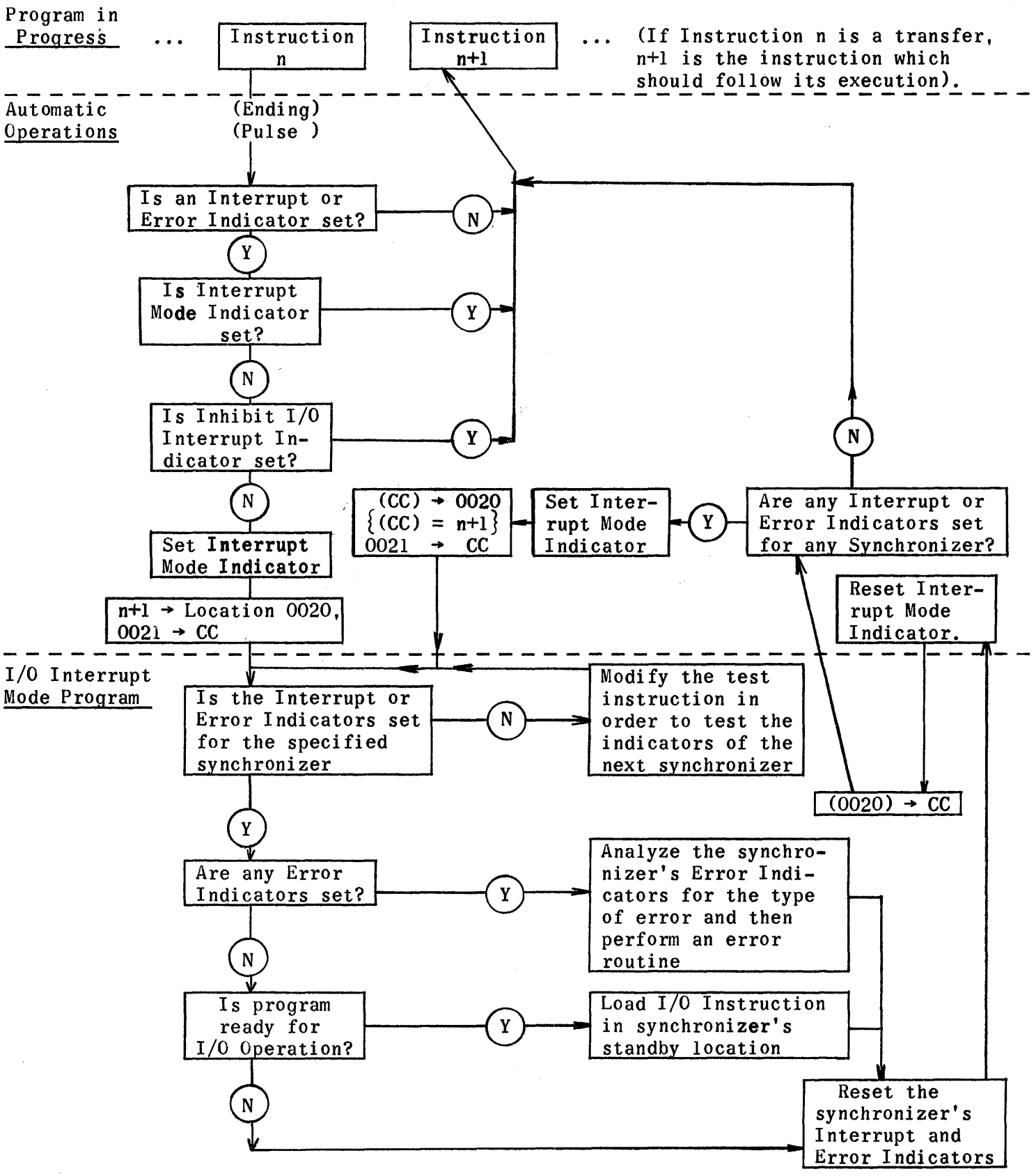
8. a. UNISERVO III/IIIA and II Synchronizers only.
Since it is possible for a successful completion interrupt to occur within 704 4-μs cycles when reading with the UNISERVO III Synchronizer (and even within 14 cycles if the second instruction successfully completed the initiation of a rewind operation), certain special provisions concerning UNISERVO Interrupts are provided, as follows:

The Interrupt Indicator is set ONLY for successful completion and when programmed; it does not become set when an error condition prevents successful completion. In the latter case, interrupt takes place in the same manner as if the error occurred during processing of an instruction which did not call for a programmed interrupt.

b. UNISERVO III/IIIA, UNISERVO IIA, High Speed Printer and Punched Paper Tape Reader and Punch.
Once the interrupt indicator (Bit 2) has been set as the result of a successful completion, the setting of the interrupt indicator for a second successful completion will be delayed until the interrupt program has reset the indicator from the prior successful completion. During the time that the second setting of the successful completion interrupt indicator is delayed, the synchronizer WILL BE INHIBITED from accessing its standby location. This permits the interrupt program to take more than 704 cycles without the possibility of the interrupt indicator being set twice for two successful completions, during the interim.

9. For UNISERVO III and IIA High Speed Printer and Punched Paper Tape Synchronizers, the standby location indicator is never reset until after the synchronizer has accepted the instruction it accessed from its standby location. For an instruction to be accepted, it must be a valid order capable of being initiated. For example, a "busy" indicator will be set without resetting the standby location indicator when the read instruction accessed from standby addresses a servo busy writing. For 80 and 90 Column Card Reader and Punch Synchronizers, the standby location indicator is unconditionally reset at instruction access time. This applies whether or not the instruction was accepted successfully.

11325 I/O INTERRUPT DIAGRAM



11330 PROCESSOR ERROR INTERRUPT

This class of Interrupt has highest priority. It includes the following types of errors (see paragraph 11902 A for Indicator Settings):

1. Memory Address Error on a Central Processor instruction read.
2. Memory Address Error on a Central Processor operand read or write.
3. Mod. 3 Error on a Central Processor instruction read.
4. Mod. 3 Error on a Central Processor operand read or write.
5. Mod. 3 Error on Adder Output. Only possible for three groups of instructions and only if Field Selection is not employed: Loads (12, 13), Adds and Subtracts (20, 21, 22, 23, 24, 25, 26, 27) and Compares (54, 55, 56, 57).
6. Mod. 3 Error occurring during the reading from memory of one of the following instructions: 06, 07, 60, 77.
7. Memory Address Error on all synchronizer write to memory operations.

The Central Processor will stall if a second error occurs while the Processor Error Interrupt Mode Indicator is set.

11340 CONTINGENCY INTERRUPT

A Program Interrupt of this class is caused by any of the following conditions (see paragraph 11902 B for Indicator Settings):

1. An overflow occurring in an addition or subtraction operation, or in execution of a divide order with the absolute value of the divisor not larger than that portion of the dividend in AR_1.
2. Attempted execution of an instruction whose operation code is not part of the repertoire. This interrupt facility provides for compatibility in the event that additions to the instruction repertoire are made in later versions of Univac III.
3. This interrupt occurs automatically whenever a key is released on the console typewriter keyboard and whenever a character is printed by the console typewriter.
4. Keyboard Request button is depressed.
5. Keyboard Release button on Console Keyboard is depressed.
6. The Program Stop button on the console is depressed (usually for bringing the computer to a programmed orderly halt).
7. If the Addressable Clock is accessed by a Load Time instruction and had not been reset since the last time power to it was dropped.

11350 INPUT-OUTPUT INTERRUPT

As indicated in the preceding paragraphs, input-output interrupt will occur as the result of either of the following:

a. Successful completion of an Input/Output Instruction which called for interrupt.
b. Occurrence of an error or of some condition requiring operator intervention, when the synchronizer attempts to perform the required instruction.

11351 INTERRUPTS UPON SUCCESSFUL COMPLETION OF INPUT-OUTPUT OPERATIONS

It must be noted that, except for Uniservo synchronizers, it is possible for two operations using a single synchronizer to be successfully completed in succession, without the occurrence of two interrupts, if the second operation is sufficiently brief that it can occur before programmed discovery of the first of the interrupts. The probability of such an occurrence will depend upon the complexity of the interrupt routines, and the brevity of the input-output operations. In the case of the Uniservo synchronizers, it is possible for a successful completion interrupt to occur within 704 4-μs cycles (and even within 14 cycles if the second instruction successfully completed the initiation of a rewind operation). For this reason, the Uniservo synchronizers are designed for the setting of the interrupt indicator for a second successful completion to be delayed until the first interrupt has been processed to the point of resetting the interrupt indicator. See Paragraph 11320, subparagraph 8.

If an instruction calling for interrupt is given to the Card Reader, the interrupt will occur when the instruction is successfully accepted for execution by the synchronizer and the standby location interlock indicator is reset. If, at any time, card feeding is terminated, the cards already committed to the reader transport mechanism will be read into memory when they pass the second read station. If additional instructions are not given to provide the synchronizer with addresses for the images of these committed cards, they will all be transmitted to the same area of memory, and no signal will be available to indicate the completion of each of these transfers. Hence, in normal card reading operations, the instruction which feeds the last card of a group will be followed by two instructions which lack the bit calling for <u>card feed</u>, so that image addresses can be supplied to the synchronizer, and so that interrupt pulses are available when each of the images is transferred to memory. (If stacker selection is also desired, additional instructions will be necessary to perform the selection of the committed cards).

11353 INPUT-OUTPUT ERROR INTERRUPTS

The Error Conditions, and the indicators set upon occurrence of the various errors, are described for the various input-output units.

A. UNISERVO III/IIIA TAPE UNIT ERRORS AND CONTINGENCIES

The information in this section applies to both the UNISERVO III and UNISERVO IIIA Tape Units unless otherwise noted.

If the Error A, Error B, Fault or Busy Indicator is set, the synchronizer is inhibited from accessing the standby location for an instruction.

I. Motion Controls (In each case, the instruction is aborted before actual tape operation begins.)

a.	UNISERVO Tape Unit Select Fault	UNISERVO Tape Unit selection fails. The Fault Indicator (Bit 7) is set.
b.	Improper Instruction	Occurs if a read synchronizer receives a write order, or vice versa (except when the write synchronizer contains the read option). The Fault Indicator is set.
c.	UNISERVO Tape Unit Unavailable	Occurs if the addressed servo requires manual intervention because power is off, UNISERVO tape unit is interlocked by previous instruction or write is specified on a tape when the reel does not contain a ring. The Fault Indicator is set.
d.	UNISERVO Tape Unit Busy	Occurs if addressed UNISERVO tape unit is rewinding (without interlock), or is being used by another synchronizer. The Busy Indicator (Bit 4) is set.
e.	Memory Mod 3 Error During Instruction Access	Occurs if a Mod 3 Error is detected when an instruction is read from memory. The Busy and Error B Indicators are set
f.	Memory Addressing Error During Instruction Access	Occurs if an addressing error is detected when an instruction is read from memory The Busy and Error B Indicators are set

II. Write Synchronizer

Testable error indicators will be set at the termination of execution of the instruction during which the error occurs. All errors detected during writing or write checking will set the Error A Indicator (Bit 3) and a bad spot pattern will be written. Loss of UNISERVO Tape Unit Interlock (writing beyond the end of tape or occurrence of a power loss) will set the Fault Indicator (Bit 7) in addition to Error A Indicator. Memory accessing is halted following the detection of the error. If the write synchronizer contains the read option (see paragraph 31050), the error conditions and indicator settings in paragraph 11353, A, III also apply to the write synchronizer when reading.

a.	Memory Addressing Error	Caused by a memory addressing error occurring during the reading of a data word from memory.
b.	Memory Mod 3 Error	Caused by a Mod 3 Error occurring during the reading of a data word from memory.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

A. UNISERVO III ERRORS AND CONTINGENCIES (Continued)

II. Write Synchronizer (Continued)

c. Improper or Loss of Start Sentinel	Caused when the write-check circuits are unable to detect correct start sentinels on tape.
d. Write-Check Error	Caused when the write-check circuits detect a Mod 3 Error of data on tape.
e. Overskew	Caused when more than four frames of skew are detected by the write-check circuits.
f. Uniservo Fault	Tape drive starts, but drops out prior to receiving the signal to stop from synchronizer. The Error A and Fault Indicators are set.
g. End of Tape Warning	A photocell for detecting Load Point and End of Tape Warning windows is located along the tape path at a point approximately 2 3/32" following the read gap (see Paragraph 31000, Note 1). Since the photocell is positioned following the write gap in the tape path, the window will be written over before it is detected by the photocell. This will cause a Bad Spot Pattern to be written and an Error A Interrupt to occur. The Error A can be recovered from by reissuing the last tape instruction. A flip-flop in the Uniservo is set when an End of Tape Warning window is detected. It is reset when the End of Tape Warning window passes the photocell while moving in a Backward direction. When the synchronizer addresses a Uniservo whose end of tape warning flip-flop is set, a filp-flop in the synchronizer is also set. At the completion of the instruction that addressed the Uniservo, an I/O Program Interrupt takes place with the program testable End of Tape Warning Indicator (Bit 6) set. The End of Tape Warning interrupt occurs approximately 724 μs prior to the time when a successful completion interrupt occurs. The synchronizer is inhibited from accessing the standby location for another instruction while the End of Tape Warning Indicator is set. Depending on block size, it is possible that several tape instructions for the same Uniservo may be executed between the time the window is written over and the time it is detected by the photocell.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

A. UNISERVO III ERRORS AND CONTINGENCIES (Continued)

II. Write Synchronizer (Continued)

h. Since the memory location specified in the address field of a stop control word is accessed on a gather-write instruction (though not actually used), it is possible that a Mod 3 or addressing error might occur when it is accessed. In this case an interrupt will occur with the Error A Indicator set and a bad spot pattern written after the last data word.

III. Read Synchronizer

Testable error indicators will be set at the end of the block within which the error occurs. The Error A Indicator will not be set on backward reads except when set in combination with the Fault Indicator to indicate a Uniservo fault condition. The occurrence of an Error A or B condition immediately halts memory transfers of data. Loss of Uniservo interlock sets the Error A and Fault Indicators the same as for the Write Synchronizer. If, after a first block read is executed, two backward read commands are given to the same Uniservo, an interrupt will occur with the Error A and Fault Indicators set and the tape positioned at the Load Point.

If the write-check circuits had detected an error after the reverse start sentinel had been written for a block, a Bad Spot Pattern was recorded followed by an Erased Tape Gap and tape movement stopped. An Error A Interrupt occurred notifying the program to reissue the same instruction and rewrite the block. Upon reading the block at some later time, it may or may not be read successfully. If an error is detected, an Error A Interrupt occurs as described in the second paragraph of 11353, A, III, g. If the read was successful, the read gap is positioned somewhere in the Bad Spot Pattern between the duplicate blocks. When the next Read Instruction is given, the duplicate block is automatically skipped and the next block is read.

a. Improper or Loss of Start Sentinel	Caused when the read circuits are unable to detect a correct Start Sentinel on tape. The Error B Indicator (Bit 5) is set.
b. Memory Parity Error	Caused when a Mod 3 error occurs during the writing of a data word into memory. The Error B Indicator is set.
c. Synchronizer Parity Error	Caused when a Mod 3 Error on a data word read from tape is detected by the synchronizer. The Error B Indicator is set.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

A. UNISERVO III ERRORS AND CONTINGENCIES (Continued)

III. Read Synchronizer (Continued)

d. Overskew	Occurs when more than four frames of skew are detected by the read circuitry. The Error B Indicator is set.
e. Bad Spot on Forward Read	The block currently being processed was found to be in error during the write-check operation and is marked with a Bad Spot Pattern. The Error A Indicator is set. In backward reading, the Bad Spot Pattern will be detected before valid data and the block will be automatically skipped without the setting of any error indicators or the occurrence of an interrupt.

Whenever instructions cannot be successfully completed because of error or contingency conditions listed above, the Standby Location Interlock for the appropriate synchronizer remains set, and the instruction in the Standby Location is not taken into the synchronizer for processing.

Whenever an error occurring on a specific Uniservo results in a lockout of the synchronizer involved, the Uniservo may be accessed by the other synchronizer without first resetting the error indicators of the first synchronizer.

g. Program recovery after Error B Interrupt

For forward tape reads without error, the end of the data block is recognized and the synchronizer is released upon detection of the reverse start sentinel. Upon release of the synchronizer, the completion interrupt will be issued if programmed, and (unless a new order continues the reading for the next block) the tape is halted <u>prior</u> to the read head reaching the erased tape gap (absence of writing in all channels). On the next read order, the forward start pattern and the forward start sentinel are recognized, and after the sentinel is detected, data transmission commences.

In reading, the detection of an Error B condition results in the tape stopping with the read head positioned in the erased tape gap or in the next block and an interrupt occurs with the Error B Indicator set. If a Bad Spot Pattern is detected prior to the erased tape gap, the Error B Indicator is <u>not</u> set and an interrupt occurs with the Error A Indicator set.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

B. UNISERVO IIA Tape Unit

I. FAULTS are abnormal conditions requiring operator intervention for recovery, except for the "UNISERVO Tape Unit Unavailable" condition of addressing a UNISERVO IIA tape unit in a state of rewinding. No unique indication is provided for this condition since its occurrence is rare. (UNISERVO IIA tape unit in the UNIVAC III System is included primarily as an input-output device and not as a working storage medium, thus tapes will usually be changed after having been read or written and will not be addressed for further use after rewinding.) In each case the instruction is aborted before execution begins and an interrupt occurs with the Fault Indicator (Bit 7) set. Instruction accessing is inhibited while the Fault Indicator is set.

Invalid UNISERVO Tape Unit Address	Synchronizer has accessed an instruction that contained an invalid UNISERVO tape unit address. (See paragraph 19699.2)
Invalid Operation Code	Synchronizer has accessed an instruction that contains an invalid bit combination in the operation code field. (See paragraph 19697.1)
UNISERVO Tape Unit Unavailable	Occurs due to one or more of the following conditions: 1. UNISERVO Tape Unit Main Interlock dropped. 2. UNISERVO Tape Unit rewinding, with or without interlock specified, or rewound with interlock. 3. A write instruction given to a UNISERVO Tape Unit whose tape reel carries a protective ring. 4. Power off the selected UNISERVO Tape Unit 5. Addressed UNISERVO Tape Unit not logically connected to the Synchronizer. 6. Blown fuse in UNISERVO tape unit. 7. Maintenance Interlock on the selected UNISERVO tape unit.

II. DATA ERRORS (Correctable by programming)

In the following cases, the ERROR A (Bit 5) Indicator is set and an interrupt takes place at the completion of instruction execution. Instruction accessing is inhibited while the ERROR A Indicator is set.

< 720 Characters Read	Occurs when a block from 709 to 719 characters have been read.
UNIVAC Tape Character Parity Error	Caused when a character read from UNIVAC tape does not have odd parity.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

B. UNISERVO IIA Tape Unit (Continued)

II. DATA ERRORS (Correctable by programming) (Continued)

Memory Parity Error	Caused when a Mod 3 Error is detected while reading data from memory (tape write) or writing data to memory (tape read).
Memory Addressing Error	Caused when an addressing error occurs during the reading of data from memory (tape write).
Synchronizer Parity Error	Caused by a Mod 3 Error occurring during the transmission of data from the central processor to synchronizer (tape write).

In the following cases, the Error B (Bit 6) Indicator is set and an interrupt takes place at the completion of instruction execution (in any case the Successful Completion Indicator (Bit 2) is not set, even if specified by the instruction). Instruction accessing is inhibited while the Error B Indicator is set.

> 720 Characters Read	Occurs when more than 720 characters are read in the UNIVAC Tape Mode. No more than 720 characters (180 UNIVAC III words) are transferred to memory by the execution of a read instruction. The program can, in most cases, determine whether a one or two block read had occurred by the following calculation: {Ending (MAC)} - {Starting (MAC) + 182} = X, If X is minus, a one block read occurred, If X is plus, a two block read occurred. See paragraph 32210, Synchronizer MAC.

III. INSTRUCTION ERRORS

In the following cases, Error A Indicator (Bit 5) and the FAULT Indicator (Bit 7) are set and an interrupt takes place immediately. The standby location interlock indicator remains set.

Memory Addressing Error	Caused by an Addressing Error occurring during the reading of an instruction from memory.
Memory Parity Error	Caused by a Mod 3 Error occurring during the reading of an instruction from memory.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

C. HIGH SPEED PRINTER

I. Instruction Errors

Instruction errors cause an interrupt with the Error (Bit 5) and the Standby Location Interlock (Bit 1) Indicators set. The synchronizer is inhibited from accessing memory while the Error Indicator is set. If an instruction error is detected, paper advancing and printing do not take place. Therefore, the program may reset the Error Indicator and reload the standby location with the same instruction and the synchronizer will again attempt to execute it. The following conditions are classed as instruction errors:

Memory Addressing Error	Caused when an addressing error occurs during the reading of an instruction from memory.
Memory Parity Error	Caused when a Mod 3 error occurs during the reading of an instruction from memory.
Synchronizer Parity	Caused when a Mod 3 error occurs during the transfer of an instruction from the Central Processor to the synchronizer.

II. Data Errors

Data errors cause an interrupt and set the Error Indicator (Bit 5). The Standby Location Interlock Indicator (Bit 1) is unconditionally reset. The synchronizer is inhibited from accessing memory while the Error Indicator is set. If a data error is detected, the paper has advanced, if specified, and part of the line may have been printed. However, any characters that have been printed are correct. Therefore the program can attempt to recover by reissuing the same instruction, except it should specify zero lines of paper advance. The following are classed as Data Errors:

Memory Addressing Error	Caused by an addressing error occurring during the reading of data from memory.
Memory Parity Error	Caused by a Mod 3 error occurring during the reading of data from memory.
Synchronizer Parity	Caused by a Mod 3 error occurring during the transfer of data from the Central Processor to the synchronizer.
Mod 3 Error on Data in the Buffer	Caused by the detection of a Mod 3 error on data in the printer buffer.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

C. HIGH SPEED PRINTER (Continued)

III. Out of Paper Warning

The Out of Paper Warning Indicator (Bit 6) is set and an interrupt occurs, at the completion of the current cycle, when the Printer is almost out of paper. The amount of blank paper remaining after the interrupt may be from 0" to 2.5" depending on the number of lines of paper advance specified by the last instruction executed. The synchronizer is inhibited from accessing memory until the Out of Paper Warning Indicator is reset by programming. This indicator may be set in combination with the Successful Completion Interrupt Indicator (Bit 2).

IV. Faults

Faults cause interrupt and set the Fault Indicator (Bit 7). The synchronizer is inhibited from accessing memory until the condition is manually corrected and the Abnormal Clear Button-Light on the printer control panel is depressed. It is possible that part of an incorrect line has been printed as the result of a fault condition occurring. The following conditions are classed as faults:

Motor Off	Caused by depression of the MOTOR ON button-light on the Printer Control Panel to turn off the printer motor.
Carriage Out	Caused when the carriage is not in printing position.
Ribbon Out	Caused when the Printer is out of ribbon or the ribbon has been ripped.
Logic Check	Caused when one of the checks made on the correct operation of the character code generator circuits do not pass.
Paper Runaway	Caused when paper feeding of more than a one second duration has taken place. This condition disengages the paper feed clutch and engages the brake.
Printer Interlock	Caused when a door on the printer cabinet is not properly closed.
Printer DC Power Off#	Caused by a DC power failure in the printer mechanism.
Printer Overheat#	Caused when the temperature within the printer cabinet is above the required limit.

The abnormal conditions listed below are classed as faults but do not cause interrupt because it is not logically possible to do so. Even though an interrupt does not occur, the fault will be indicated on the monitor panel at the Operator's Console and also at the High Speed Printer Control Panel.

Synchronizer Overheat#	Caused when the temperature within the synchronizer cabinet is above the required limit.
Synchronizer Interlock#	Caused when a door on the synchronizer cabinet is not properly closed.
Power Supply Fault#	Caused by a fault in the Printer Power Supply
Synchronizer DC Power Off#	Caused by the depression of the DC ON button-light on the Printer Control Panel to turn off the DC power.

#Turns Off DC Power.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

D. CARD READER

The information in this section applies to both the 80 and 90 column card readers unless otherwise stated.

I. Data Errors

Data errors cause an interrupt at 234^{0} of the card cycle and set the Data Error Indicator (Bit 5). Stacker selection of the card in error must be accomplished by programming. A Data Error will allow the instruction in the standby location to be transferred to the synchronizer and be executed in the normal manner. After that, the synchronizer is inhibited from accessing memory until the Data Error Indicator is reset. The following abnormal conditions are classed as Data Errors:

Check-Read Error	Caused when the hole counts accumulated for a given card, as it passed both read stations, do not agree.
Memory Addressing Error	Caused by an addressing error occurring during the reading of data from memory.
Mod 3 Error	Caused by a Mod 3 error occurring during the reading of data from or the writing of data to memory.
Synchronizer Mod 3 Error	Caused by a Mod 3 error occurring during the transmission of data from the Central Processor to the synchronizer.
Incorrect Number of Memory Accesses Granted	Caused when the synchronizer is not granted the correct memory accesses needed to read a card into memory. The correct number of accesses for the 80 column reader is 480; for the 90 column, it is 288.

II. Operator Contingencies

Operator contingencies are the result of some action the operator took, or failed to take. They cause an interrupt with the Operator Contingency Indicator (Bit 6) set upon detection of the condition, if the unit is on-line and the standby location interlock indicator is set or there are cards in the feed track. The synchronizer is inhibited from accessing memory until the condition is corrected and the Abnormal Clear Button on the Reader Control Panel is depressed. Cards at card station 1, 2, 3 and 4, when the interrupt occurs, are automatically selected into stacker 0. Cards in the stacker section, when the interrupt occurs, are selected into their previously program selected stackers. In the case where a Data Error occurs during the same cycle as an Operator Contingency, the conditions are treated as an Operator Contingency, i.e., the Operator Contingency Indicator is set and the Data Error Indicator is not set. If an Operator Contingency occurs during the same cycle as a fault, the indicator associated with the earlier detected condition is set.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

D. CARD READER (Continued)

II. Operator Contingencies (Continued)

The following conditions are classed as Operator Contingencies:

Motor Off	The Card Reader Drive Motor was turned off as the result of the operator having depressed the Motor On Button on the Card Reader Control Panel.
Full Stacker	One of the output stackers contains more than the maximum number of cards allowed.
Empty Input Magazine or Misfeed	Caused by the absence of a card at Card Station 1 at the completion of a Card Feed Instruction.
Interlock	Door or cover not properly in place.
Off-Line	When the Off-Line button-light is depressed, the unit is placed off-line immediately. Cards at stations 1, 2 and 3 will be automatically selected into stacker 0. The card at station 4 may or may not be selected into stacker 0,depending on what point during the cycle the button is depressed. Only the standby indicator must be set for this condition to cause interrupt.

III. Faults

Fault conditions set the Fault Indicator (Bit 7) and cause interrupt. These occur when the fault condition is detected, i.e., any time during the card cycle, if the unit is on-line and the standby location interlock indicator is set or there are cards in the feed track. Memory accesses are inhibited from the time of detection until the condition is corrected and the Abnormal Clear Button-Light on the reader is depressed. Cards at card stations 1, 2, 3 and 4, when the interrupt occurs, are automatically selected into stacker 0. Cards in the stacker section of the feed track, when the interrupt occurs, are selected into the proper program selected stackers. In the case where a Data Error occurs in combination with a fault, the conditions are treated as a fault, i.e., only the Fault Indicator is set. If an operator contingency occurs during the same cycle as a fault, the indicator associated with the earlier detected condition is set.

The following abnormal conditions are classed as Faults:

Feed Jam*	Occurs when a card at Read Station 2 is not in time with the Card Reader or is jammed.
Stacker Jam*	Caused by a card jam in the stacker section of the feed track.

*Turns Off Drive Motor

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

D. CARD READER (Continued)

III. Faults (Continued)

Logic Checks	One or more of several checks of the operation of the Card Reader Synchronizer do not pass.
Memory Addressing Error On Instruction Access	Caused by an Addressing Error occurring during the reading of an instruction from the memory.
Memory Mod 3 Error On Instruction Access	Caused by a Mod 3 Error occurring during the reading of an instruction from the memory.

The abnormal conditions listed below are classed as faults but do not cause interrupt because it is not logically possible to do so. Even though an interrupt does not occur, the fault will be indicated on the monitor panel at the Operator's Console and also at the Card Reader control panel.

Upon occurrence of a condition turning off DC power, all cards in the feed track not yet deflected into a stacker will be selected into Stacker 0.

Airflow#	Occurs when Blower is not supplying sufficient air to Card Reader.
Overheat#	Operating temperature is too high.
Power Supply Fault#	An abnormal condition exists in the Card Reader power supply.
DC Off#	The DC power to the Card Reader has been turned off as the result of the operator having depressed the DC ON Button on the Card Reader Control Panel.

#Turns off DC Power.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

E. CARD PUNCH

The information in this section applies to both the 80 and 90 column Card Punch Units unless otherwise noted.

I. Data Errors

Data errors cause an interrupt and set the Data Error Indicator (Bit 5) at 271^{0} of the card cycle. The synchronizer is inhibited from accessing memory while this indicator is set. It is reset by programming. The synchronizer must be loaded with an instruction specifying stacker selection and the Data Error Indicator reset within approximately 16 ms. after the interrupt, if the error card is to be selected into Stacker 1. The following conditions are classed as Data Errors:

Check-Read Error	Caused when the signal and hole counts accumulated for a given card at the punch and check-read stations do not agree.
Incorrect Number of Memory Accesses Granted	Caused when the synchronizer is not granted the correct number of memory accesses needed to punch a card from memory.
Incomplete Processing of a Memory Request or Access	Caused when a memory request is not granted or is granted and, due to a synchronizer malfunction, the data accessed is not processed by the time the next request must be made.
Memory Addressing Error	Caused by an addressing error occurring during the reading of data from memory.
Memory Mod 3 Error	Caused by a Mod 3 error occurring during the reading of data from memory.
Synchronizer Mod 3 Error	Caused by a Mod 3 error occurring during the transfer of data from the Central Processor to the synchronizer.

II. Operator Contingencies

Operator Contingencies are the result of some action the operator took or failed to take. They cause interrupt with the Operator Contingency Indicator (Bit 6) set upon detection, if the unit is on-line and the standby location interlock indicator is set or there are cards in the feed track. The synchronizer is inhibited from accessing memory until the condition is corrected and the Abnormal Clear Button on the Punch Control Panel is depressed. If a Data Error occurs during the same cycle as an Operator Contingency, the conditions are treated as a contingency, i.e., the Operator Contingency Indicator is set and the Data Error Indicator is not set.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

E. CARD PUNCH (Continued)

II. Operator Contingencies (Continued)

The following conditions are classed as Operator Contingencies:

Motor Off	The Card Punch Drive Motor was turned off as the result of the operator having depressed the Motor On Button on the Control Panel.
Full Stacker	One of the Output Stackers contains more than the maximum number of cards allowed.
Empty Input Magazine	Caused by the absence of cards in the input magazine.
Chip Box Full	Caused when the box under the punching mechanism is full of chips.
Interlock	Door, cover or punch mechanism not properly in place.
Off-Line	When the Off-Line Button-Light is depressed the unit is placed off-line immediately. The card moving through the check read station may or may not be selected into stacker 0, depending on what point during the cycle the button is depressed. The card moving through the post punch station will be selected into stacker 0. Only the standby indicator must be set for this condition to cause interrupt.

III. Faults

Faults cause an interrupt and set the Fault Indicator (Bit 7) upon detection, if the unit is on-line and the standby location interlock indicator is set or there are cards in the feed track. Memory accesses by the synchronizer are inhibited until the fault condition is corrected and the Abnormal Clear Button-Light on the Card Punch Control Panel is depressed. In the case where a data error occurs during the same cycle as a fault, the condition is treated as a fault with only the Fault Indicator set. If an operator contingency occurs during the same cycle as a fault, the indicator associated with the earlier detected condition is set.

Feed Jam*	Caused when a card in the feed track is not in time with the punch unit, is jammed, or by the absence of a card at Wait Station 1 after the execution of a Punch instruction.
Stacker Jam*	Caused by a card jam in the stacker section of the card path.
Logic Check	Caused when one or more checks on the operation of the synchronizer logic do not pass.
Memory Addressing Error On Instruction Access	Caused by an Addressing Error occurring during the reading of an instruction from the memory.
Memory Mod 3 Error On Instruction Access	Caused by a Mod 3 Error occurring during the reading of an instruction from the memory.

*Turns off Drive Motor.

11353 INPUT-OUTPUT ERROR INTERRUPTS (Continued)

E. CARD PUNCH (Continued)

III. Faults (Continued)

The abnormal conditions listed below are classed as Faults but do not cause interrupt because it is not logically possible to do so. (Even though an interrupt does not occur, the Fault will be indicated on the monitor panel at the Operator's Console.)

Upon occurrence of a condition turning off DC power, the card leaving the check-read station and any cards not yet deflected into a stacker will be selected into Stacker 0.

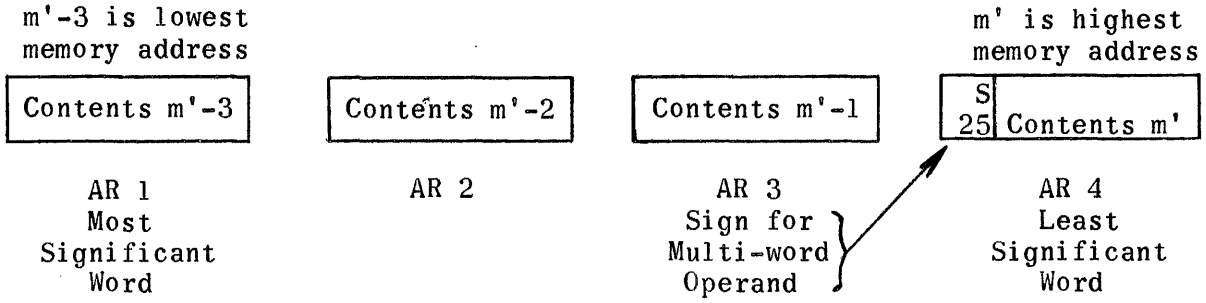
Airflow#	Occurs when blower is not supplying sufficient air to Card Punch.
Overheat#	Operating temperature is too high.
Power Supply Fault#	An abnormal condition exists in the Card Punch power supply.
DC Off#	The DC power to the Card Punch was turned off as a result of the operator having depressed the DC On Button on the Control Panel.

#DC Off

11400 MULTI-WORD OPERANDS

Digital, alphanumeric, and binary words can be grouped in sets of two, three, or four to form multi-word operands. Those instructions which handle multi-word operands are indicated in the List of Instructions (Section 11900). Bit positions 1 through 24 are used to expand the operand size. The sign of the expanded operand is the sign of its least significant word. In multi-word operands the left-most word, located in the low-order memory address, is most significant. Thus, in addition to its sign, a multi-word operand may consist of 12, 18 or 24 decimal digits; or 8, 12 or 16 alphanumeric characters; or 48, 72 or 96 bits (binary digits).

MULTI-WORD OPERAND IN ARITHMETIC REGISTERS



The core memory address of the multi-word operand is the address of the right-most and least significant word of the group, except in the case of the zero suppress instruction. The size of the multi-word operand addressed in this manner is controlled by specification of the accumulating registers in the instruction controlling the transfer. The accumulating registers are specified by bit positions 11 through 14 of the instruction; the method of causing multi-word operations is to specify more than one accumulating register by placing more than one bit in this field. These bits (and the related registers) need not be adjacent to each other, but the number of bits controls the number of adjacent words in memory involved in the transfer. The register designations are as follows:

Register	Designation in AR field
r1	1000
r2	0100
r3	0010
r4	0001

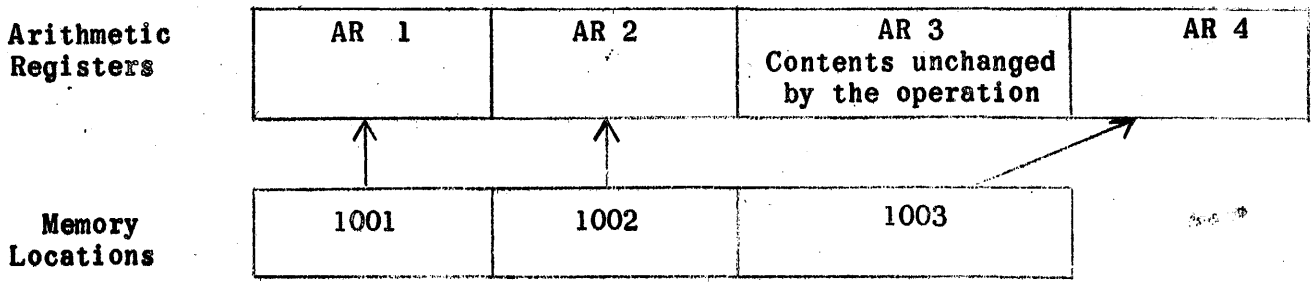
After arithmetic operations involving multi-word operands in accumulating registers the signs of all words of the operand are made to agree with the sign of the result.

Multi-word fetch and store operations leave signs unchanged. Fetch negative and store negative change the sign of each word of a multi-word operand -- these operations do not force the signs of the resulting multi-word portions to agree.

If a command includes an AR field consisting of 4 zeros, the non-existent register behaves as though it contained $-2^{25}-1$. (All 1's)

11400 (Cont'd)

As indicated on the previous page, multi-word operations are not restricted to adjacent registers, though reference to words in memory by such an operation invariably affects consecutive words. For example, a 3-word operand in location 1001, 1002, and 1003 will be brought to registers 1, 2 and 4 by a clear and fetch operation specifying those registers in the AR field (with the bit pattern 1101).



11400 MULTI-WORD OPERANDS (continued)

When multi-word arithmetic operations and shift instructions are performed, the registers involved act like a single large register, even if they are not adjacent. Carries from the left of the less significant registers are propagated in the more significant registers.

For example, in a two-word addition calling for registers 1 and 3, and memory locations M1 and M2:

Registers before execution

AR1	AR2	AR3	AR4
+148326	*******	+492851	*******

Memory Contents

M1	M2
+492618	+706214

Registers after execution

AR1	AR2	AR3	AR4
+640945	*******	+199065	*******

In a two-word alphanumeric left shift of 3 characters, again using registers 1 and 3, the following occurs:

	AR1	AR2	AR3	AR4
Registers before shift	+ABCD	*****	+EFGH	*****
Registers after shift	+DEFG	*****	+H000	*****

Binary zeros.

In both examples, the contents of registers indicated by **** are unchanged by the operations.

11500 INSTRUCTION INDEXING FACILITIES

All instructions automatically go through an indexing cycle to develop the operand address. This indexing cycle adds the contents of the Index Register, IR, addressed in bit positions 21-24 of the instruction, to the binary address, m, in bit positions 1-10 of the instruction to form m', an indexed operand address. If instruction bit positions 21-24 contain zeros, the indexing cycle is ineffectual and m = m'. The index registers actually contain 16 bits, but bit position 16 is always a zero. The full 16-bit contents are stored in memory by the STX (Store Index Register) instruction, but only 15 bits can be placed in an IR by the LX (Load Index Register) instruction.

11600 INDIRECT ADDRESSING AND FIELD SELECTION

Those instructions to which Indirect Addressing and Field Selection apply are noted in Section 11900. If bit 25 of the instruction is a "1", indirect addressing is indicated and (m') should have one of the two following formats:

Indirect Address Control Word:

IA	IR	ZEROS	*	m-ADDRESS
25	24 21	20 18	17 16	15 1

*Bit positions 16 and 17 are disregarded.

Field Select Control Word:

0	IR	LEFT BIT POSITION	RIGHT BIT POSITION	m-ADDRESS
25	24 21	20 16	15 11	10 1

11610 INDIRECT ADDRESSING

If the word accessed at the m' instruction address has a 0 (zero) in each of bit positions 18-20, indirect addressing is specified. The operand to be manipulated is to be found at the m' location specified by the Indirect Address Control Word (IACW). Further "cascading" of IACW's may be accomplished by placing a 1 in bit position 25 of the IACW and can continue indefinitely until a Field Select Control Word (FSCW) or an IACW with a zero in bit position 25 is accessed.

11620 FIELD SELECTION

If the word accessed at the location specified by the m' address of an instruction or at the m' address of an IACW does not have a 0 in each bit position 18-20, field selection is specified. The operand to be manipulated is to be found at the m' location specified by the FSCW and only that portion of the word defined by the left and right bit position fields is to be manipulated. Bit positions are indicated in a modified "excess-3" notation, for example, bit 1 is represented by 00100 (= 1 + 3), bit 20 by 10111 (= 20 + 3).

Conditions imposed by field selection are:

a. All selected fields are considered to be positive. It is <u>not</u> possible to field select bit position 25.

b. Portions of the word beyond the limits of the selected portion are treated as binary zeros when the field selected word is used as an operand. If this field selected word is the operand of a decimal addition or subtraction, the binary zeros beyond the limits of the field are treated as though they were excess-3 zeros.

c. For octal operation codes 12, 13, 14, 15, 16, 54, 55, 56 and 57, the field selected portion of the operand from memory affects only the same relative bit positions of the AR(s), except see "e" below. For octal operation codes 20, 21, 22, 23, 24, 25, 26 and 27, the entire operand from memory (the selected field with zeros to the left and right as specified by the boundary bits) is entered into the adder as is the entire AR operand (the contents of the AR before the operation started) to produce the result.

d. When field selection is specified with multi-word operands, the right bit position must lie within the least significant word of the field, the left bit position must lie within the most significant word of the field. Only when a single word operand is specified, may both right and left bit positions lie within one word.

e. Carries or borrows which occur as a result of the manipulation of field selected operands are propagated beyond the limits of the field up to the limits of the high order accumulating register. If the limit of the high order register is exceeded, an overflow is indicated.

11700 SCATTER-READ AND SCATTER-WRITE

Information on UNIVAC III tapes may be divided into blocks of variable sizes separated by inter-block gaps. Each block may in turn be divided into any number of segments of variable size (up to 511 words) separated by automatically inserted segment separator words. These segments may be located in memory at the discretion of the programmer. In specifying the number of words to be read from or written on tape, the actual number of words to be read from or written on tape, the actual number of words in each segment to be transferred is given in a control word stored in memory, except that zero in the count field calls for 4096 words.

11710 Gather-Write is governed by a sequential list of control words located in memory. Each control word contains a beginning memory location for a segment of information to be written, and the number of words to be transmitted. A segment separator is written on tape between each segment of data, but these are not transmitted to the memory when tape is read.

11720 Scatter-Read may be backward or forward. The location in memory of data read from tape is controlled by a list of control words in memory in the same fashion as in the collection of data to be written. This list of control words allows the following possibilities:

a. The various segments need not go to the same memory locations from which they were written.

b. Reading to memory is terminated short of encountering a segment separator on tape by a control count of less than the actual segment size. The tape is read to the beginning of the next segment without transfer of data words to memory, and the next control word in memory takes effect.

11720 (continued)

c. Reading to memory is terminated short of the read tape control word count by the detection of a write tape control word on tape. The next control word in memory takes effect.
d. The detection of a tape stop control word in memory during the reading of a block from tape will stop the transfer of data to memory. The tape will be read without transfer of data words until the next interblock gap is reached.

11800 WORD FORMATS

DIGITAL DATA WORD

S	Digit 6	Digit 5	Digit 4	Digit 3	Digit 2	Digit 1
25	24 21	20 17	16 13	12 9	8 5	4 1

ALPHANUMERIC DATA WORD

S	Char. 4	Char. 3	Char. 2	Char. 1
25	24 19	18 13	12 7	6 1

BINARY DATA WORD

S	24 Bit Binary Number
25	24 1

BASIC INSTRUCTION WORD

IA	IR	OPR	AR	m-Address
25	24 21	20 15	14 11	10 1

SHIFT INSTRUCTION WORD

IA	IR	OPR	AR	Shift Count
25	24 21	20 15	14 11	10 1

LOAD OR UNLOAD IR INSTRUCTION WORD

IA	IR	OPR	IR'	m-Address
25	24 21	20 15	14 11	10 1

11800 WORD FORMATS

INCREMENT IR INSTRUCTION WORD (cf. 11807)

IA	IR	OPR	IR'	m-ADDRESS
25	24 21	20 15	14 11	10 1

IR INCREMENT AND COMPARE INSTRUCTION WORD (cf. 11810)

IA	IR	OPR	IR'	m-ADDRESS
25	24 21	20 15	14 11	10 1

INITIATE I/O OPERATION INSTRUCTION WORD (cf. 11814)

IA	IR	OPR	SYNC.	m-ADDRESS
25	24 21	20 15	14 11	10 1

I/O INSTRUCTION WORD (NOT APPLICABLE TO PRINTER) (cf. 11812)

0	UNIT	OPR	m-ADDRESS
25	24 21	20 16	15 1

CONSOLE TYPEWRITER INSTRUCTION WORD (INPUT) (cf. 11816)

*	*	OPR	AR	*
25	21	20 15	14 11	10 1

CONSOLE TYPEWRITER INSTRUCTION WORD (OUTPUT) (cf. 11815)

IA	IR	OPR	CHAR. POSITION	m-ADDRESS
25	24 21	20 15	14 11	10 1

TEST OR RESET I/O INDICATOR INSTRUCTION WORD (cf. 11902, C, D, F, G)

IA	IR	OPR	SYNC.	IND.
25	24 21	20 15	14 11	10 1

*Not Used.

11800 WORD FORMATS

INDIRECT ADDRESS CONTROL WORD

IA	IR	ZEROS	*	m-ADDRESS
25	24 21	20 18	17 16	15 1

FIELD SELECT CONTROL WORD

0	IR	LEFT BIT POSITION	RIGHT BIT POSITION	m-ADDRESS
25	24 21	20 16	15 11	10 1

IR INCREMENT AND COMPARE CONTROL WORD

S	COMPARISON AMOUNT	INCREMENT AMOUNT
25	24 10	9 1

I/O CONTROL WORD

#	WORD COUNT	m-ADDRESS
25	24 16	15 1

PRINTER INSTRUCTION WORD

0	LINES OF VERTI-CAL SPACING	OPR	m-ADDRESS
25	24 19	18 16	15 1

A "1" in this bit position indicates a "STOP" Control Word.

* Not used.

11801 DIGITAL DATA WORD

S	Digit 6	Digit 5	Digit 4	Digit 3	Digit 2	Digit 1
25	24 21	20 17	16 13	12 9	8 5	4 1

S -- Bit 25 indicates the Sign, "1" for minus and "0" for plus.
Digit 6, 5, 4, 3, 2, 1 -- Each digit expressed in excess-3 form.

11802 ALPHANUMERIC DATA WORD

S	Char. 4	Char. 3	Char. 2	Char. 1
25	24 19	18 13	12 7	6 1

S -- Sign. (The sign bits of alphanumeric words obtained by expansion of numeric words will be the same as the sign bit for the low order numeric word.)

11803 BINARY DATA WORD

	24-Bit Binary Number
25	24 1

S -- Bit 25 indicates the Sign, "1" for minus and "0" for plus.
24-Bit Binary Number -- In a Binary Data Word the decimal numbers from zero through 16,777,215 can be expressed with sign.

11804 INSTRUCTION

IA	IR	OPR	AR	m-Address
25	24 21	20 15	14 11	10 1

This is the general Instruction Word Format. A "1" in bit position 25 specifies that the m' address gives the address of another word which, when accessed, gives either (1) the address of an operand (Indirect Addressing), or (2) the address of an operand, together with the beginning and ending bit positions of a field within that operand (Field Selection).

Bits 1 through 10 specify an address which is modified by the fifteen-bit contents of the Index Register specified by bit position 21 through 24, and the resulting modified address, m', is the address of the operand of the instruction.

Bits 11 through 14 specify the Arithmetic Registers in which the operation is to be accomplished. Multi-word operands are specified by using more than one register, as indicated by two or more bits in bit positions 11 through 14. In such cases, the address of the least significant word is the one specified by the instruction. Each of the four Arithmetic Registers is indicated by a bit in a discrete position of the AR field. Thus, for example, 1000 specifies AR1 (the "left-most" register) and 0110 specifies AR's 2 and 3. Multi-word arithmetic is not restricted to adjacent registers, but milti-word operands in memory must consist of adjacent words.

11805 SHIFT INSTRUCTION

IA	IR	OPR	AR	Shift Count
25	24 21	20 15	14 11	10 1

IA -- A "1" bit indicates that the number in the Shift Count field is an m-Address which designates an Indirect Address Control Word which in turn contains the Shift Count or the address of another IACW.
IR -- Specifies Index Register used to modify Shift-Count.
OPR -- Specifies the 6-bit Operation Code.
AR -- Designates the accumulating registers involved in the Shift Operation.
Shift Count -- Specifies the number of positions the operand is to be shifted.
If the shift is binary right circular, the number specifies the bit positions to be shifted.
If the shift is numeric, the number specifies the 4-bit digit positions to be shifted.
If the shift is alphanumeric, the number specifies the 6-bit character positions to be shifted.

11806 LOAD OR UNLOAD INDEX REGISTER INSTRUCTIONS

IA	IR	OPR	IR'	m-Address
25	24 21	20 15	14 11	10 1

IA -- A "1" bit indicates that the indexed m-Address refers to an Indirect Address Control Word rather than to an operand.
IR -- Specifies the Index Register whose contents modify the m-Address.
OPR -- Specifies the 6-bit Operation Code.
IR' -- Designates the Index Register into which the low order fifteen bits of (m') are to be loaded, or the Index Register to be unloaded into the low order 16 bit positions of m' (see paragraph 11500).
m-Address -- Contains the Memory Address of the Operand or Indirect Address Control Word before the Index Register Modification (by the register specified in the IR field).

11807 INCREMENT INDEX REGISTER INSTRUCTION

IA	IR	OPR	IR'	m-Address
25	24 21	20 15	14 11	10 1

IA -- A "1" bit indicates that the indexed m-Address refers to an Indirect Address Control Word rather than to an operand.
IR -- Specifies Index Register used to modify the m-Address.
OPR -- Specifies 6-bit Operation Code.
IR' -- Designates the Index Register to be incremented.
m-Address -- Contains the Memory Address of the Index Register Increment word or Indirect Address Control Word, which is modified into m' by the contents of the specified index register, as customary.

11808 INDIRECT ADDRESS CONTROL WORD

IA	IR	Zeros	*	m-Address
25	24 21	20 18	17 16	15 1

*Bit positions 16 and 17 are disregarded.

The Indirect Address Word is the one located at the m'-Address given in an instruction with a one bit in position 25 (or in a preceding indirect address word, when that preceding word itself had a one bit in position 25). Thus Indirect Addressing may cascade through several IA Words until one is reached without a bit in position 25, and the cascade may end in either an Indirect Address Word or a Field Select Word. The format of the Field Select Control Word is the same, except that the Indirect Address Word must have all zeros in positions 18 through 20. The 15 bit m-Address, as modified by the contents of the Index Register specified by bits 21 through 24, is the address of the Operand (or next IA/FS word if a one bit is in position 25) of the original instruction.

11809 FIELD SELECT CONTROL WORD

0	IR	Left Bit Position	Right Bit Position	m-Address
25	24 21	20 16	15 11	10 1

IR -- Specifies the Index Register whose contents modify the m-Address.
Left Bit Position -- Designates the leftmost bit position of the field-selected portion of the most significant Operand Word.
Right Bit Position -- Designates the rightmost bit position of the field-selected portion of the least significant Operand Word. In both bit position addresses each bit is designated by the binary value of the position, increased by binary 3. Thus the rightmost bit of a word, bit 1, is represented by 00100 (= 1+3) and the high-order bit position, exclusive of the sign, bit 24, is represented by 11011 (= 24+3).
m-Address -- Contains the memory address of the operand before index register modification.

11810 INDEX REGISTER INCREMENT AND COMPARE INSTRUCTION

IA	IR	OPR	IR'	m-Address
25	24 21	20 15	14 11	10 1

IA -- A "1" bit in this position indicates that the indexed m-Address refers to an Indirect Address Control Word rather than to an Operand.
IR -- Specifies the Index Register whose contents modify the m-Address.
OPR -- Specifies the 6-bit Operation Code.
IR' -- Designates the Index Register to be compared with the Comparison Amount and increased by the Increment Amount contained in the Index Register Increment and Control Word.
m-Address -- Contains the Memory Address of the operand (or Indirect Address Control Word if bit position 25 is 1) before Index Register Modification.

11811 INDEX REGISTER INCREMENT AND COMPARE CONTROL WORD

S	Comparison Amount	Increment Amount
25	24 10	9 1

S -- Sign of the Increment Amount. (A "1" bit in position 25 transforms the instruction to one which decrements an Index Register.)
Increment Amount -- Contains the binary value to be added to the contents of the Index Register specified by the IR Increment and Compare Instruction.
Comparison Amount -- Contains the binary value to be compared with the contents of the Index Register specified by the IR Increment and Compare Instruction.

11812 INPUT-OUTPUT INSTRUCTION WORD

0	UNIT	OPR	m-ADDRESS
25	24 21	20 16	15 1

0 -- This position must contain zero.
Unit -- Specifies the unit or type of unit to be used for the input-output operation.
Opr -- Specifies the operation or operations to be executed.
Address -- Specifies the memory location at which an I/O control word may be found. In the case of card punch or printer, this address specifies the memory location from which data is to be punched or printed; or, in the case of the card reader, the memory location into which the first word is to be placed.

11813 INPUT-OUTPUT CONTROL WORD

#	WORD COUNT	m-ADDRESS
25	24 16	15 1

-- A "1" in this bit position indicates a stop control word.
Word Count -- Specifies the number of sequential words to be written to or read from magnetic tape.
Address -- Specifies the first memory location from which or into which tape data is to be taken or placed. If bit 25 is a one, the control word specifies termination of data transfer, and is not transmitted.
Backward Stop Control Word -- is automatically transmitted at start of writing each block on tape.

11814 INITIATE INPUT-OUTPUT OPERATION INSTRUCTION WORD

IA	IR	OPR	SYNC.	m-ADDRESS
25	24 21	20 15	14 11	10 1

IA -- A 1 bit indicates that m' specifies the location of an IACW.
IR -- Specifies the index register whose contents are used to create m'.
Opr -- Specifies operation code.
Sync. -- Specifies which synchronizer the operation is to use and the specific standby memory location into which the Input-Output Instruction Word is to go.
Address -- Specifies the memory location at which the Input-Output Instruction Word is to be found or the location of an IACW, which is modified into m' by the contents of the specified index register, as customary.

11815 CONSOLE TYPEWRITER INSTRUCTION WORD (OUTPUT)

IA	IR	OPR	CHAR. POS.	m-ADDRESS
25	24 21	20 15	14 11	10 1

IA -- A "1" bit indicates that the indexed m-Address refers to an Indirect Address Control Word rather than an operand.
IR -- Specifies the index register used to modify the m-Address.
OPR -- Specifies the 6-bit operation code.
CHAR. POS. -- Specifies the position of the character to be printed from the word in memory. (cf. 19520)
m-ADDRESS -- Contains the memory address of the operand or Indirect Address Control Word before index register modification.

11816 CONSOLE TYPEWRITER INSTRUCTION WORD (INPUT)

*	OPR	AR	*
25 21	20 15	14 11	10 1

* -- Not used.
OPR -- Specifies operation code.
AR -- Specifies the arithmetic register into which the character is loaded on input.

11817 PRINTER INSTRUCTION WORD (cf. 19400)

0	LINES OF VERTICAL SPACING	OPR	m-ADDRESS
25	24 19	18 16	15 1

LINES OF VERTICAL SPACING -- Specifies the number of lines of vertical form movement which will occur before printing. The range is 0 to 63, expressed as binary numbers. If the instruction calls for printing (with an appropriate bit in the OPR field) specification of zero lines provides for printing without spacing.
OPR -- Operation Code
Bit 16: If "1", Interrupt after spacing and/or printing
Bit 17: Unassigned
Bit 18: If "1", Print; If "0", Space but do not print.
m-ADDRESS -- Specifies the location in core memory of the first (left most) word of the print image.

11816 CONSOLE TYPEWRITER INSTRUCTION WORD

*	OPR	AR	*
25 21	20 15	14 11	10 1

* -- Not used but may require specific bit configuration due to logical design requirement.
OPR -- Specifies operation code.
AR -- Specifies the arithmetic register to be used in the typewriter routine.

11817 PRINTER INSTRUCTION WORD

0	LINES OF VERTICAL SPACING	OPR	m-Address
25	24 19	18 16	15 1

Lines of vertical spacing -- Specifies the number of lines of vertical form movement which will occur before printing. The range is 0 to 63, expressed as binary numbers. If the instruction calls for printing (with an appropriate bit in the OPR field) specification of zero lines provides for printing without spacing.
OPR -- Operation Code
Bit 16: If "1", Interrupt after spacing and/or printing
Bit 17: Unassigned
Bit 18: If "1", Print; If "0", Space but do not print. It is not legitimate to call for zero lines if printing is not performed.
m-Address -- Specifies the location in core memory of the first word of the print image.

11900 INSTRUCTION EXECUTION TIMING CHART

INSTRUCTION	DIAGRAM	FIELD SELECTION		MACHINE CYCLES REQUIRED PER NUMBER OF WORDS IN OPERAND 1	2	3	4	OPERATION CODE OCTAL	OPERATION CODE MNEMONIC
LOGICAL INSTRUCTIONS (CF 14000)									
Superimpose	(ARi) ∪ (m') → ARi	x		2	3	4	5	15	SUP
Erase	(ARi) ∩ (m') → ARi	x		2	3	4	5	16	ERS
Set sense indicator		-		2	-	-	-	62	SSI
Reset sense indicator		-		2	-	-	-	61	RSI
Reset I/O Interrupt and Error Indicators		-		2	-	-	-	65	RIO
Reset Contingency Indicators		-		2	-	-	-	65	RCI
Reset Processor Error Indicators		-		2	-	-	-	65	RPE
Set Inhibit Input-Output Interrupt Indicator		-		2	-	-	-	62	PIO
Reset Inhibit Input/Output Interrupt Indicator		-		2	-	-	-	61	AIO
COMPARISON INSTRUCTIONS (CF 15000) (SET HIGH, EQUAL OR LOW INDICATOR)									
Compare algebraic	(ARi) > (m') set high indicator (ARi) = (m') set equal indicator (ARi) < (m') set low indicator	x		2	3	4	5	54	C
Compare absolute (disregard sign)	(ARi) > (m') set high indicator (ARi) = (m') set equal indicator (ARi) < (m') set low indicator	x		2	3	4	5	55	CA
Compare for selected 1's	(ARi ones) = (m' ones) set equal indicator	x		2	3	4	5	57	CONE
Compare for selected 0's	(ARi ones) = (m' zeros) set equal indicator	x		2	3	4	5	56	CZRO
CONSOLE TYPEWRITER INSTRUCTIONS (CF 19500)									
Write Typewriter Character	(m') → Typewriter AR field specifies a character position	NOT APPLICABLE		2				02	WT
Read Typewriter Character	(Type Buffer) → ARi, position 1 - 6			2				01	RT
Display Memory	(m') → Display			2				03	DIS
Activate Keyboard				2				66	ACT

11900 INSTRUCTION EXECUTION TIMING CHART

INSTRUCTION	DIAGRAM	FIELD SELECTION	MACHINE CYCLES REQUIRED PER NUMBER OF WORDS IN OPERAND 1	MACHINE CYCLES REQUIRED PER NUMBER OF WORDS IN OPERAND 2		OPERATION CODE OCTAL	OPERATION CODE MNEMONIC
SHIFT INSTRUCTIONS (CF 16000)							
Shift decimal right	Two words maximum, not restricted to adjacent registers	FIELD SELECTION NOT ALLOWED	4	7		40	SR
Shift decimal left	Two words maximum, not restricted to adjacent registers		3	6		41	SL
If a two word operand is shifted 7 to 12 decimal digit positions, it is done in the time required for a one word shift.							
Shift binary right circular	Sign is shifted also		0 to 7 bits need 4 cycles, 8 to 16 bits need 5 cycles, 17 to 25 bits need 6 cycles			44	SBC
Alphanumeric shift right	Two words maximum, not restricted to adjacent registers		4	9		42	SAR
Alphanumeric shift left	Two words maximum, not restricted to adjacent registers		3	8		43	SAL
If a two word operand is shifted 5 to 8 alphanumeric character positions, it is done in the time required for a one word shift.							
TRANSFER CONTROL INSTRUCTIONS (CF 17000)							
Unconditional transfer	m' → CC		1			06	TUN
Test Processor indicators***	If set, m' → CC, (1 cycle)		1 or 2	NOT APPLICABLE	Indicator Tested is Addressed in AR Bits	60	THI
Test Sense indicators	If reset, (CC) + 1 → CC, (2 cycles)						TLO TEQ TPOS
Test Inhibit Interrupt indicator							TSI
Test I/O Interrupt indicators	If set, (CC) + 1 → CC If reset, (CC) + 2 → CC		2				TIOP
Test I/O Interlock indicators	These instructions test indicators specified by bits in positions 1-10 for the synchronizer specified in positions 11-14.		2				TIO
Test I/O Error indicators			2			64	
Test Contingency indicators			2				TCI
Test Processor Error indicators			2				TPE

***The Inhibit Input-Output Interrupt Indicator is one of the Processor Indicators.

11900 INSTRUCTIONS EXECUTION TIMING CHART

INSTRUCTIONS	DIAGRAM	FIELD SELECTION	MACHINE CYCLES REQUIRED PER NUMBER OF WORDS IN OPERAND 1	2	3	4	OPERATION CODE OCTAL	OPERATION CODE MNEMONIC
DATA EDITING INSTRUCTIONS (CF 18000)								
Compress	(m') → ARi				8		72	ATD
Expand	(ARi) → m'				8		71	DTA
Zero Suppress	(m') → ARi		2	3	4	5	73	ZUP
@INPUT-OUTPUT INSTRUCTIONS (CF 19000) (2-WORD)								
Initiate Input-Output			3				70	IOF
INDEX REGISTER INSTRUCTIONS (CF 20000)								
Load index register	(m') → IR'		3				51	LX
Increment index register and compare	IR Modifier + (IR') → IR' (IR Modifier in bit positions 1-9 with sign in position 25) (IR') LS 15 Bits : (m') 10-24; Set indicator (>, = ,<)		4				53	ICX
Increment index register	(m') + (IR') → IR'		3				52	IX
Unload index register	(IR') → m' 1-16		3				50	STX
MISCELLANEOUS INSTRUCTIONS (CF 21000)								
No operation			2				00	NOP
Stop and Transfer			2				77	WAI
Write contents of MAC to memory & transfer	(MAC) + 1 → m' 1-16 & m' + 1 → CC		3				07	TR
Write (MAC) to Memory	(MAC) → m' 1-16		3				04	STM
Write contents of Uniservo III Synchronizer Tape Control Word Register to memory.	(TC WR) → m'		3				05	STC

FIELD SELECTION NOT ALLOWED

@Initiate Input-Output instruction can indirectly address the input-output words; the latter cannot specify indirect addressing. The initiate input-output instruction does not apply to the Console Typewriter. The Input-Output Instruction Word Function Specifications are listed on the following pages according to the unit (Paragraph 11901).

11900 INSTRUCTION EXECUTION TIMING CHART

INSTRUCTION	DIAGRAM	FIELD SELECTION		MACHINE CYCLES REQUIRED PER NUMBER OF WORDS IN OPERAND 1	2	3	4	OPERATION CODE OCTAL	OPERATION CODE MNEMONIC
ARITHMETIC INSTRUCTIONS*									
Add decimal	(m')+(ARi)→ARi	x		2	3	4	5	20	A
Subtract decimal	-(m')+(ARi)→ARi	x		2	3	4	5	21	S
Add decimal, next register	(m')+(ARi)→ARj	x		2				22	AH
	(m')+(AR1,AR2)→AR3,AR4	x			3				
Subtract decimal, next reg.	-(m')+(ARi)→ARj	x		2				23	SH
	-(m')+(AR1,AR2)→AR3,AR4	x			3				
Add binary	(m')+(ARi)→ARi	x		2	3	4	5	24	BA
Subtract binary	-(m')+(ARi)→ARi	x		2	3	4	5	25	BS
Add binary, next register	(m')+(ARi)→ARj	x		2				26	BAH
	(m')+(AR1,AR2)→AR3,AR4	x			3				
Subtract binary, next reg.	-(m')+(ARi)→ARj	x		2				27	BSH
	-(m')+(AR1,AR2)→AR3,AR4	x			3				
Decimal multiply	(AR1)x(m')→AR2,AR3	-		19 to 31, depending upon multiplier digits				30	M
Decimal divide	(AR1,AR2)/(m')→ARI(Remainder) & AR2(Quotient)	-		17 to 36, depending upon quotient digits				31	D
MEMORY-REGISTER WORD TRANSFER INSTRUCTIONS									
Clear and fetch	(m')→ARi	x		2	3	4	5	12	L
Clear and fetch negative**	-(m')→ARi	x		2	3	4	5	13	LCS
Extract into register	(m')→ARi	x	F.S.	3	4	5	6	14	EXT
Store	(ARi)→m'	-		2	3	4	5	10	ST
Store negative**	-(ARi)→m'	-		2	3	4	5	11	STCS

*ARITHMETIC INSTRUCTIONS:
Divide and multiply use only the designated registers. If recomplementing is required, add 4 microseconds for each word of the operand.

**"Negative" in instruction title means "reverse sign".

F.S. Extract includes Field Select Time.
Multiword shifts need not occur in adjacent registers. Field selection requires an additional 4 microseconds for accessing and analyzing the F/S control word. Indirect addressing requires an additional 4 microseconds for each indirect address accessed.

11901 INPUT-OUTPUT INSTRUCTION WORD FUNCTION SPECIFICATIONS

One word time is required for transferring the function specification from its Standby Location in Memory to the Synchronizer Registers. In addition, whenever the synchronizer transfers a word between itself and memory, it requests memory from the Central Processor. If the Central Processor is using memory, it will be delayed one word time while the synchronizer is making the transfer.

INSTRUCTION WORD FUNCTION SPECIFICATION	INSTRUCTION SPECIFICATION OPERATION CODE BIT POSITIONS					OPERATION CODE MNEMONIC
	20	19	18	17	16*	
UNISERVO III						
Read Tape Forward with Control Word	0	0	0	0	1	FSR
Read Tape Forward without Control Word	0	1	0	0	1	FBR
Forward Contingency Scatter Read	1	0	0	0	1	FCSR
Forward Contingency Block Read	1	1	0	0	1	FCBR
Read Backward with Control Word	0	0	1	0	1	BSR
Read Backward without Control Word	0	1	1	0	1	BBR
Backward Contingency Scatter Read	1	0	1	0	1	BCSR
Backward Contingency Block Read	1	1	1	0	1	BCBR
Write Tape	0	0	0	1	1	GWT
Write Bad Spot Pattern and then Data	0	1	0	1	1	OWT
Rewind	0	0	1	1	1	RW
Rewind and Interlock	0	1	1	1	1	RWI
UNISERVO II						
Forward Read One Block Normal Gain	0	0	0	0	1	CFRN
Forward Read One Block High Gain	1	0	0	0	1	CFRH
Forward Read One Block Low Gain	0	1	0	0	1	CFRL
Backward Read One Block Normal Gain	0	0	1	0	1	CBRN
Backward Read One Block High Gain	1	0	1	0	1	CBRH
Backward Read One Block Low Gain	0	1	1	0	1	CBRL
Compatible Write	0	0	0	1	1	CWRT
Compatible Write Subdivided	0	1	0	1	1	CWSD
Rewind	0	0	1	1	1	CRW
Rewind with Interlock	1	0	1	1	1	CRWI
HIGH SPEED PRINTER						
Advance Paper and Print Line			1	#	1	PRT
Advance Paper Only			0	#	1	PAD
HIGH SPEED READER						
Card Image Transferred to Memory Only	0	0	0	0	1	CAD
Feed Card	0	0	0	1	1	FC
Translate	0	0	1	0	1	CT
Feed Card and Translate	0	0	1	1	1	FCT
Select Stacker 1	0	1	0	0	1	CS1
Feed Card and Select Stacker 1	0	1	0	1	1	FCS1
Translate and Select Stacker 1	0	1	1	0	1	CTS1
Feed Card, Translate and Select Stacker 1	0	1	1	1	1	FCTS1
Select Stacker 2	1	0	0	0	1	CS2
Feed Card and Select Stacker 2	1	0	0	1	1	FCS2
Translate and Select Stacker 2	1	0	1	0	1	CTS2
Feed Card, Translate and Select Stacker 2	1	0	1	1	1	FCTS2

*A bit here specifies Programmed Interrupt.
#Unassigned.

11901 INPUT-OUTPUT INSTRUCTION WORD FUNCTION SPECIFICATIONS (Continued)

INSTRUCTION WORD FUNCTION SPECIFICATION	INSTRUCTION SPECIFICATION OPERATION CODE BIT POSITIONS					OPERATION CODE MNEMONIC
	20	19	18	17	16	
CARD PUNCH (CF 19300)	UNASSIGNED				COMPLETION INTERRUPT	
Clutch Feed, Move, Punch Untranslated Card		0	0	1		PC
Clutch Feed, Move, Punch Translated Card		0	1	1		PCT
Select Stacker 1, Punch Untranslated Card		1	0	1		PCS
Select Stacker 1, Punch Translated Card		1	1	1		PCTS
Select Stacker 1 for Card after Check Read		1	0	0		CCS
PAPER TAPE (CF 53000)						
Paper Tape Read (specified number of words, 1 to 126, or 256)				0		PTR
Paper Tape Backspace (the number 127 in count field specifies a 1 character backspace)				0		PTB
Paper Tape Punch (specified number of words, 1 to 126, or 256)				1		PTP

11902 ADDRESS SPECIFICATIONS FOR THE CENTRAL PROCESSOR, UNISERVO SYNCHRONIZERS, GENERAL PURPOSE CHANNEL SYNCHRONIZERS, REGISTERS AND INDICATORS

Index Register addresses are specified in binary notation (0000-1111) and appear in instructions as specified in paragraphs 11500 and 20000. Arithmetic Registers are addressed as specified in paragraph 11400. Synchronizer Standby Locations, Memory Address Counters and Tape Control Word Registers, the Control Counter and the Memory Address Register are specified by bit positions 11-14 of the appropriate instructions. Processor Indicators are also specified by bit positions 11-14. The groups of Processor Error, Contingency and Synchronizer Indicators are specified by bit positions 11-14. The individual indicators associated with each group are specified by bit positions 1-10 of the appropriate instructions.

A. The Group, Processor Error Indicators, is specified by 0001 in bit positions 11-14 of the instruction; the individual indicators comprising this group are addressed by bit positions 1-10 as listed below:

INDICATOR ADDRESS BIT POSITIONS 10 9 8 7 6 5 4 3 2 1	PROCESSOR ERROR CONDITION
0 0 0 0 0 0 0 0 0 1	Memory Address Error on Instruction Read
0 0 0 0 0 0 0 0 1 0	Memory Address Error on Operand Write
0 0 0 0 0 0 0 0 1 1	Memory Address Error on Uniservo III Write Sync. Write to Memory Operation
0 0 0 0 0 0 0 1 0 0	Memory Address Error on Uniservo III Read Sync. Write to Memory Operation
0 0 0 0 0 0 0 1 0 1	Memory Address Error on GP Ch 1 Write to Memory Operation
0 0 0 0 0 0 0 1 1 0	Memory Address Error on GP Ch 2 Write to Memory Operation
0 0 0 0 0 0 0 1 1 1	Memory Address Error on GP Ch 3 Write to Memory Operation
0 0 0 0 0 0 1 0 0 0	Memory Address Error on GP Ch 4 Write to Memory Operation
0 0 0 0 0 0 1 0 0 1	Memory Address Error on GP Ch 5 Write to Memory Operation
0 0 0 0 0 0 1 0 1 0	Memory Address Error on GP Ch 6 Write to Memory Operation
0 0 0 0 0 0 1 0 1 1	Memory Address Error on GP Ch 7 Write to Memory Operation
0 0 0 0 0 0 1 1 0 0	Memory Address Error on GP Ch 8 Write to Memory Operation
0 0 0 0 0 0 1 1 0 1	Memory Address Error on Uniservo II Sync. Write to Memory Operation
0 0 0 0 0 0 1 1 1 0	Memory Address Error on Additional Uniservo III Write Sync. Write to Memory Operation
0 0 0 0 0 0 1 1 1 1	Memory Address Error on Additional Uniservo III Read Sync. Write to Memory Operation
0 0 0 0 0 1 0 0 0 0	Mod 3 Error on Instruction Read from Memory Operation
0 0 0 0 1 0 0 0 0 0	Mod 3 Error on Operand Read From or Write to Memory Operation
0 0 0 1 0 0 0 0 0 0	Mod 3 Error on Adder Output (see 11330, 5)
0 0 1 0 0 1 0 0 0 0	Mod 3 Error during the reading of one of the following Transfer of Control instructions from memory: 06, 07, 60 or 77.
0 1 0 0 0 0 0 0 0 0	Memory Address Error on an Operand Read from Memory Operation

11902 ADDRESS SPECIFICATIONS FOR THE CENTRAL PROCESSOR, UNISERVO SYNCHRONIZERS, GENERAL PURPOSE CHANNEL SYNCHRONIZERS, REGISTERS AND INDICATORS (Continued)

B. The Group, Contingency Indicators, is specified by 0010 in bit positions 11-14 of the instruction; the individual indicators comprising this group are addressed by bit positions 1-10 as listed below:

INDICATOR ADDRESS BIT POSITIONS 10 9 8 7 6 5 4 3 2 1	CONTINGENCIES
0 0 0 0 0 0 0 0 0 1	Overflow as the result of an Arithmetic operation or Power to Addressable Clock dropped.
0 0 0 0 0 0 0 0 1 0	Operation code not part of repertoire.
0 0 0 0 0 0 0 1 0 0	Console Typewriter Interrupt on input or output of a character.
0 0 0 0 0 0 1 0 0 0	Keyboard Request (operator request for use of Typewriter)
0 0 0 0 0 1 0 0 0 0	Keyboard Release (operator has completed typed-in message)
0 0 0 0 1 0 0 0 0 0	Contingency Stop (operator signals program to bring Central Processor and Synchronizers to an orderly halt)

C. The Group, Synchronizer Indicators, is specified by designating which Synchronizer's Indicators are to be addressed in bit positions 11-14 (see paragraphs D, F and G following) and the specific indicator in bit positions 1-10. The various indicators and their general meanings are listed below:

INDICATOR ADDRESS BIT POSITIONS 10 9 8 7 6 5 4 3 2 1	INDICATOR MEANINGS (For Detailed Description See Paragraph 11353)
0 0 0 0 0 0 0 0 0 1	Standby Location Interlock Indicator
0 0 0 0 0 0 0 0 1 0	Program Interrupt, for: 1. Uniservo III, Uniservo II (see paragraph 11353, B. II), High Speed Printer and Punched Paper Tape, indicates successful completion of instruction execution, when set. 2. Card Reader and Punch, indicates that the instruction has been transferred to the synchronizer.
0 0 0 0 0 0 0 1 0 0 (Bit 3)	For Uniservo III only, indicates an error detected during writing, or if reading, indicates a Bad Spot Pattern was detected or may be set in combination with Fault Indicator (Bit 7). In any case the instruction should be re-issued.
0 0 0 0 0 0 1 0 0 0 (Bit 4)	For Uniservo III only, indicates the Uniservo specified by the instruction in the Standby Location is busy rewinding or is under control of another synchronizer. When set in combination with Bit 1 and 5, indicates an error on instruction call.

11902 ADDRESS SPECIFICATIONS FOR THE CENTRAL PROCESSOR, UNISERVO SYNCHRONIZERS, GENERAL PURPOSE CHANNEL SYNCHRONIZERS, REGISTERS AND INDICATORS (Continued)

C. (Continued)

INDICATOR ADDRESS BIT POSITIONS 10 9 8 7 6 5 4 3 2 1	INDICATOR MEANINGS (For Detailed Description See Paragraph 11353)
0 0 0 0 0 1 0 0 0 0	In general an error - specifically, for: 1. UNISERVO III tape unit, indicates an error detected while reading tape or if set in combination with Bit 1 and 4 indicates an error on instruction call. 2. UNISERVO IIA tape unit, indicates a data transfer error. When set in combination with Bits 1 and 7 indicates an error on instruction call. When set in combination with Bit 6 indicates a > 720 error and an error on data transfer. 3. For High Speed Printer, Card Reader, Card Punch and Punched Paper Tape, indicates an error on data transfers. 4. For High Speed Printer, when set in combination with Standby Location Indicator (Bit 1), indicates an error on instruction call.
0 0 0 0 1 0 0 0 0 0 (Bit 6)	For: 1. UNISERVO III tape unit, indicates End of Tape Warning. 2. UNISERVO IIA tape unit, indicates a > 720 Error. 3. Card Reader and Card Punch, indicates an Operator Contingency. 4. High Speed Printer, indicates out of paper warning condition. 5. Punched Paper Tape, indicates a wired-in stop character has been encountered by the Reader or Punch. If set in combination with Program Interrupt Indicator (Bit 2), indicates the Punch is low on tape.
0 0 0 1 0 0 0 0 0 0 (Bit 7)	In general a fault - specifically, for: 1. UNISERVO III tape unit, indicates the Addressed UNISERVO tape unit is unavailable. If set in combination with the Error A Indicator (Bit 3) indicates a Fault condition has occurred during the attempted execution of an instruction. 2. UNISERVO IIA tape unit, indicates a Fault condition. When set in combination with Bit 5 and Bit 1, indicates error on instruction call. 3. Card Reader, Card Punch, High Speed Printer and Punched Paper Tape, indicates Fault condition.

11902 ADDRESS SPECIFICATIONS FOR THE CENTRAL PROCESSOR, UNISERVO SYNCHRONIZERS, GENERAL PURPOSE CHANNEL SYNCHRONIZERS, REGISTERS AND INDICATORS (Continued)

D. The following table shows the AR bits used to designate the various Uniservo III synchronizers. One Tape Control Word Register (see paragraph 21450) is associated with each such synchronizer.

	UNISERVO III SYNCHRONIZER	TAPE CONTROL WORD REGISTER
Basic Read	0100	0100
Basic Write	0011	1000
Additional Read	1111	0001
Additional Write	1110	0010

E. The testing and resetting of all indicators in bit positions 1 through 10 for Processor Errors or Contingencies or Input/Output Indicators are explained in sections 14450, 14500, 14600 and 17300. The handling of Memory Address Counters are covered in 21300 and 21400. The appropriate AR bits are shown in sections A, B, C, D, F and G.

F. The read-write synchronizer for the compatible tape Uniservo II channel is addressed in the AR bit positions of the instructions specified in paragraph "D" above, as 1101.

G. There is a maximum of eight general purpose channel synchronizers (see paragraph 01000) which may be used for adding peripheral input-output equipment such as High Speed Printers, Paper Tape Readers and Punches, High Speed Card Readers and Card Punches. The synchronizers provided for these units will be addressed according to which general purpose channel is assigned to the particular unit, and the AR bit addresses in the instructions specified in paragraph "D" above are:

GP Ch 1	0101	GP Ch 5	1001
GP Ch 2	0110	GP Ch 6	1010
GP Ch 3	0111	GP Ch 7	1011
GP Ch 4	1000	GP CH 8	1100

11902 ADDRESS SPECIFICATIONS FOR CENTRAL PROCESSOR, UNISERVO SYNCHRONIZERS, GENERAL PURPOSE CHANNEL SYNCHRONIZERS, REGISTERS AND INDICATORS (Continued)

H. Processor Indicators are addressed in the AR bit positions of the instructions, rather than the m'-Address bit positions. These include High, Equal and Low((which are set as a result of comparisons between words in Arithmetic Registers and words in Memory (see paragraphs 15100, 15200, 15300, 15400, 17200 and 14400), or are set as a result of comparisons between the incremented contents of an Index Register and the comparison field in an Index Register Increment and Compare Word (see paragraphs 20110 and 14400), or are changed as the result of any Add or Subtract Instruction (see paragraph 12000)). Other indicators addressed in this manner are: Sign Indicators, Inhibit Input-Output Interrupt Indicator, and program settable and resettable Sense Indicators (in addition to the paragraphs mentioned above in this paragraph, see also paragraphs 14550 and 14300). The meaning of the AR bit addresses within these instructions are:

AR Bit Address	Indicator Specified
0000	Inhibit I/O Interrupt
0001	Sign of AR1 (Set if Plus)
0010	Sign of AR2 (Set if Plus)
0011	Sign of AR3 (Set if Plus)
0100	Sign of AR4 (Set if Plus)
0101	LOW Indicator
0110	EQUAL Indicator
0111	HIGH Indicator
1000	Sense Indicator #1
1001	Sense Indicator #2
1010	Sense Indicator #3
1011	Sense Indicator #4
1100	Sense Indicator #5
1101	Sense Indicator #6
1110	Sense Indicator #7
1111	Sense Indicator #8

11903 CHART CONSOLIDATING ADDRESS SPECIFICATIONS SET FORTH IN PARAGRAPH 11902

AR Bits Designating Computer Error Interrupts 0001	m' Bits Designating Types of Interrupts	AR Bits Designating Processor Contingency Interrupts 0010
Mem Addr Err (Addressed Synchronizer, CC or Instruction Register in Low 4 Bit Pos)	000000xxxx	0000000001 Overflow in Arithmetic Operation. This indicator also set when power to the Addressable Clock is dropped.
		0000000010 Operation Code Not Part of Repertoire
Mem Stall on Instruction (Simultaneous Read-Write)	0000010000	0000000100 Console Typewriter Interrupt
Parity Error in Instruction	0000100000	0000001000 Keyboard Request
Mem Stall on Operand (Read-Write)	0001000000	0000010000 Keyboard Release
Parity Error in Operand	0010000000	0000100000 Contingency Stop
Arithmetic Error on Add, Subtract, Load, Compare	0100000000	0001000000 Not Assigned

AR Bits Designating Synchronizer Addresses

Uniservo III Basic Read 0011 (1000*)	1111 (0001*) Uniservo III Additional Read
Uniservo III Basic Write 0100 (0100*)	1110 (0010*) Uniservo III Additional Write
General Purpose #1 = 0101	1101 Uniservo II Compatible Read-Write
General Purpose #2 = 0110	1010 = General Purpose #6
General Purpose #3 = 0111	1011 = General Purpose #7
General Purpose #4 = 1000	1100 = General Purpose #8
General Purpose #5 = 1001	

m'-Address Bits Designating Indicators for Uniservo & G.P. Channel Synchronizers

0000000001	Standby Location Indicator
0000000010	Completion Interrupt
0000000100	Error A (Uniservos Only)
0000001000	Busy (Uniservos Only)
0000010000	Error B (G.P. Sync "Error"; "End of File" for Univac II Tape)
0000100000	Univac III "End of Tape"; Printer "Out of Paper"; Paper Tape, "Wired Stop Character"
0001000000	Fault Indicator
0001010000	Printer "Bad Line"
0000100010	Paper Tape "Low on Paper"

*Denotes Associated Tape Control Word Register.

AR Bit Designated Indicators (See 11902H):

0000	Inhibit I/O Interrupt	1000	Sense #1
0001	AR #1 Plus	1001	Sense #2
0010	AR #2 Plus	1010	Sense #3
0011	AR #3 Plus	1011	Sense #4
0100	AR #4 Plus	1100	Sense #5
0101	Low	1101	Sense #6
0110	Equal	1110	Sense #7
0111	High	1111	Sense #8

11910 TIMING OF MULTIPLICATION

Terminology: The Multiplier is the factor in Arithmetic Register 1. Each digit is a number from zero thru nine, represented as "n". Each digit has a position within the Multiplier, from one thru six, represented as a subscript "i" to the number "n." The value of the number varies according to the value of the digit on its right, except for the number in position one, and this digit on the right is represented by the subscript "i-1." The final value of the number for timing of multiplication purposes is represented by "n'." The following formulae state the method of computing "n'," and the following table gives the number of 4μ cycles required for multiplication according to the value of "n'."

For $i=1$, $n'_i = n_1$.

For $i > 1$, $n'_i = n_i$ if $n'_{i-1} < 5$.

For $i > 1$, $n'_i = n_{i+1}$ if $n'_{i-1} \geq 5$; but if $n_i+1=10$, $n_i=0$, and $n'_{i+1}=n'_{i+1}+1$.

n_7 is a constructive digit position created to allow for the "right-hand" value of n'_6.

$$n'_7 = 0 \text{ if } n'_6 < 5$$

$$n'_7 = 1 \text{ if } n'_6 \geq 5$$

Execution time in 4μcycles = $5 + \sum_{i=1}^{7} T_i$, where T_i is found in the following table.

n'i	T
0	1
1,2	2
3,4	3
5	4
6,7	3
8,9	2

Thus, for example, if the Multiplier is 945270, the execution time is determined as follows:

i	n_i	n'_i	T
1	0	0	1
2	7	7	3
3	2	3	3
4	5	5	4
5	4	5	4
6	9	0	1
7	0	1	2
		Σ 'Ti =	18

Multiplication time = 5 + 18 = 23 cycles.

11911 TIMING OF DIVISION

Terminology: Timing of Division is computed in a fashion analogous to timing of Multiplication as described in Paragraph 11910. Each digit is a number from zero through nine, represented as "n"; but the time for execution of division depends entirely upon the digits of the quotient. Each digit has a position within the quotient, from one through six, represented as a subscript "i" to the number "n"; but the value of the number varies according to the value of the digit on its left, except for the number in position six. The digit on the left is represented by the subscript "i+1". The final value of the number for timing of division purposes is represented by "n'". The following formulae state the method of computing "n'", and the following table gives the number of 4 μ cycles required for division according to the value of "n'".

For $i = 6$, $n'_i = n_6$.
For $i < 6$, $n'_i = n_i$ IF n'_{i+1} is ODD.
For $i < 6$, $n'_i = 9-n_i$ IF n'_{i+1} is EVEN.

Execution time in 4 μ cycles = $5 + \sum_{i=1}^{6} T_i$, where T_i is found in the following table:

n'_i	T
0,1	2
2,3	3
4,5	4
6,7,8,9	5

Thus for example, if the quotient is 806491, the execution time is determined as follows:

i	n_i	n'_i	T
6	8	8	5
5	0	9	5
4	6	6	5
3	4	5	4
2	9	9	5
1	1	1	2
		$\sum T_i$ =	26

Division Time = 5 + 26 = 31 cycles

ARITHMETIC SIGNS IN UNIVAC III

21 March 1961

The logic of Univac III is designed to handle signs as described below for the indicated instructions. Product Planning Specification paragraph numbers are indicated.

15100 Compare Algebraic (Mnemonic C, Octal Operation Code 54)

If the operation is multiword, the signs of all words except the least significant word are ignored. The HI FF is set if (ARi) is algebraically greater than (m'). The LO FF is set if (ARi) is algebraically less than (m'). The EQ FF is set if (ARi) and (m') are algebraically equal. Plus binary zero is greater than minus binary zero. Only one of the three FF's can be set at one time.

15200 Compare Absolute (CA, 55)

All of the signs of all words of multiword as well as single word operands are ignored.

15300 Compare for Selected Zeroes (CZRO, 56)

All words of multiword operands as wella as single word operands are treated as 25 bit operands.

15400 Compare for Selected Ones (CONE, 57)

Same as 15300.

12000 Arithmetic Instruction - Add and Subtract

A, 20 S, 21 AH, 22 SH, 23 BA, 24 BS, 25 BAH, 26 BSH, 27
If the operand is multiword, the signs of all words of the two operands except the least significant words are ignored. All signs in the result are made identical with the sign of the least significant word, which is made algebraically correct. The EQ FF is used to indicate whether the operation has resulted in zero during the execution of the instruction. If the instruction must subtract (m') from (ARi), then the sign of the result will always be made positive if the EQ FF is set. In other words, a minus zero result is impossible and the EQ FF is affected by add and subtract instructions. These instructions can be used to test for equallity. The HI and LO FF's are not affected by addition or subtraction. Whenever the result is not zero, the EQ FF is reset. It is now possible for HI and EQ FF's or LO and EQ FF's to be set at the same time.

MORE ON SIGNS IN UNIVAC III 23 March 1961

12300, 12400 DecimalMultiply and Divide (M, 30 D, 31)

If the signs of the operands are unlike, the result will be negative. If the signs are alike, the result will be positive. No special provision is made for zero results. In Divide, the sign of the remainder is made the same as the sign of the dividend.

14100, 14200 Superimpose and Erase (SUP, 15 ERS, 16)

All signs are included in the operands.

13130 Extract into Registers (EXT, 14)

The signs of the AR's are not changed.

16100-16500 Shift Instructions

SR, 40 SL, 41 SAR, 42 SAL, 43 SBC, 44

Decimal and alphanumeric shifts do not affect the signs of the AR(s). Right binary circular shift includes the sign.

20110, 20120 Index Register Increment and Increment and Compare (IX, 52 ICX, 53)

If the sign of the control word is negative, the increment is subtracted from the contents of the index register.

18210 Zero Suppress (ZUP, 73)

The sign(s) of the operand(s) become the sign (s) of the result(with no alteration(s).

18110 Compress (ATD, 72)

All signs of the result (in ARi)will be made identical to the sign of the least significant word of the operand (from m').

18120 Expand (DTA, 71)

All signs of the result (in m' will be made identical to the sign of the least significant word of the operand (from ARi).

12000 ARITHMETIC INSTRUCTIONS

All decimal arithmetic instructions operate only on Numerical Words composed of 4-bit excess 3 characters. The zero characters in both operands of decimal addition and subtraction operations may be expressed as 0000 or 0011. The zero characters in the results of all decimal arithmetic operations are expressed as 0011. In decimal add and subtract instructions, binary zeros (0000) of the operand being transferred from the AR(s) to the adder are changed to decimal zeros (0011), and binary zeros (0000), binary ones (0001) and binary twos (0010) of the memory operand being transferred to the adder are changed to decimal zeros (0011). Care must be exercised in using these undigits in arithmetic operations, as they may cause results with Mod 3 errors. The definitions listed for decimal arithmetic instructions also apply for analogous binary arithmetic instructions. After all arithmetic operations except divide, the signs of all words of the result, if more than one register contains the result, are made to agree with the correct sign of the result, as it appears in the least significant word of the result. For division, the sign of the Remainder remains the sign of the Dividend, regardless of the sign of the Quotient.

In Binary and Decimal addition and subtraction instructions (including next register instructions), zero value results are always positive and set the EQUAL indicator. If the result is non-zero, the EQUAL indicator is reset. The HIGH and LOW indicators are not affected.

NOTE: It is therefore possible for the EQUAL indicator to be set in combination with the HIGH or LOW indicator.

Execution times quoted for instructions do not include indirect addressing, field selection or recomplementation. When these are used, the following amounts should be added to the execution times of each instruction:

1. 4 us for each stage of indirect addressing.
2. 4 us for field selection.
3. 4 us per word of the operand if recomplementation is required.

12100 ADD DECIMAL

OPERATION CODES: Octal 20, Mnemonic A

Create the algebraic sum of an operand from memory and the contents of the designated arithmetic registers.

1. The operands may be multi-word.
2. $(r_i) + (m') \longrightarrow r_i$.
3. m' is field selectable and indirectly addressable.

12110 SUBTRACT DECIMAL

OPERATION CODES: Octal 21, Mnemonic S

Perform the algebraic subtraction of an operand in memory from the contents of the designated arithmetic registers.

1. $(r_i) - (m') \longrightarrow r_i$
2. The operands may be multi-word.
3. m' is field selectable and indirectly addressable.

12120 ADD DECIMAL, NEXT REGISTER

OPERATION CODES: Octal 22, Mnemonic AH

Create the algebraic sum of an operand from memory and the contents of the designated arithmetic register(s) and store the sum into the following arithmetic register(s).

1. $(r_i) + (m') \longrightarrow r_j$, or $(r_1, r_2) + (m' - 1, m') \longrightarrow r3, r4$.
   If, for single word operands, i is 1, j may be 2, 3, or 4.
   If i is 2, j may be 3 or 4.
   If i is 3, j may be 4.
2. Operands may be single or double word.
3. m' is field selectable and indirectly addressable.
4. A single word operand may be in register 1, 2 or 3, but <u>not</u> in register 4.
5. Multi-word operands are limited to arithmetic registers 1 and 2.
   Multi-word results always occur in registers 3 and 4.
6. The execution of this instruction does not change the contents of the arithmetic register(s) containing the operand.
7. For single-word operands, the contents of AR in the instruction (see the instruction word format) must indicate both r_i and r_j. Double-word operands require that the AR field of the instruction be all 1's.

12130 SUBTRACT DECIMAL, NEXT REGISTER

OPERATION CODES: Octal 23, Mnemonic SH

Perform the algebraic subtraction of an operand in memory from the contents of the designated arithmetic register(s) and store the sum into the following register(s).

1. $(r_i) - (m') \rightarrow r_j$, or $(r_1, r_2) - (m'-1, m') - r_3, r_4$
2. May have one or two word operands.
3. m' is field selectable and indirect addressable.
4. A single word operand may be in register 1, 2 or 3, but not in register 4.
5. Multi-word operands are limited to arithmetic registers 1 and 2.
6. The execution of this instruction does not change the contents of the arithmetic register(s) containing the operand.
7. For single word operands, the contents of AR in the instruction must indicate both r_i and r_j; r_j must be a register of lower order than r_i. (i.e., r_j is to the right of r_i)

   For double word operands, the AR field must be all 1's.

12200 ADD BINARY

OPERATION CODES: Octal 24, Mnemonic BA

Create the algebraic binary sum of an operand from memory and the contents of the designated arithmetic registers, and place the result in the arithmetic registers.

12210 SUBTRACT BINARY

OPERATION CODES: Octal 25, Mnemonic BS

Perform the algebraic binary subtraction of an operand in memory from the contents of the designated arithmetic registers, and place the result in the arithmetic registers.

12220 ADD BINARY, NEXT REGISTER

OPERATION CODES: Octal 26, Mnemonic BAH

Create the binary sum of an operand from memory and the contents of the designated register(s) and store the sum in the following register(s).

See comments in paragraph 12120.

12230 SUBTRACT BINARY, NEXT REGISTER

OPERATION CODES: Octal 27, Mnemonic BSH

Perform the algebraic binary subtraction of an operand in memory from the contents of the designated register(s) and store the sum in the following register(s).

See comments in paragraph 12130.

12300 DECIMAL MULTIPLY

OPERATION CODES: Octal 30, Mnemonic M

$(r_1) \times (m') \rightarrow r_2, r_3$

Two one-word operands are multiplied algebraically to form a 12 digit product. The most significant six digits of the product appear in r_2, the least significant six digits in r_3.

1. Bits 11-14 of the instruction word must designate r_1, r_2, r_3.
2. (r_1) not destroyed by this instruction.
3. m' is not field selectable but may be indirectly addressed.
4. All zeros in the multiplier and multiplicand must be decimal.

12410 DECIMAL DIVIDE

OPERATION CODES: Octal 31, Mnemonic D

$(r_1, r_2) \div m' \rightarrow r_1, r_2$

One two word operand is divided algebraically by one word operand from memory for a six-digit quotient in r_2 and six-digit remainder in r_1.

1. Bits 11-14 of the instruction must designate r_1 and r_2.
2. m' is not field selectable but is indirect addressable.
3. The contents of r_1 must be less in magnitude than the divisor in m'.
4. All zeros in the divisor and dividend must be decimal.

13000 WORD TRANSFER INSTRUCTIONS

This class of instruction transfers words from memory to the accumulating registers, or the converse. One reference must be to an accumulating register; the other is to a core storage location. For each stage of indirect addressing or for field selection an additional machine cycle must be added to the instruction time.

13100 MEMORY-TO-REGISTER WORD TRANSFER INSTRUCTIONS

In these instructions, one or more of the four arithmetic registers may be designated. The registers need not be adjacent if more than one is designated, but the memory locations must be adjacent.

13110 CLEAR AND FETCH

OPERATION CODES: Octal 10, Mnemonic L

$(m') \rightarrow r_i$

The contents of an operand from memory replace those of r_i, after r_i is first cleared to binary zero.

1. (m') is field selectable and indirectly addressable.
2. Operands may be multi-word.

13120 CLEAR AND FETCH NEGATIVE

OPERATION CODES: Octal 13, Mnemonic LCS

$-(m') \rightarrow r_i$

The contents of an operand from memory, with the sign changed, replace those of r_i after r_i is first cleared to binary zero.

1. (m') is field selectable and indirectly addressable.
2. Operands may be multi-word.

13130 EXTRACT INTO REGISTERS

OPERATION CODES: Octal 14, Mnemonic EXT

(m') extracted into r_i

Bits within the designated field of m' replace the corresponding bits in r_i; Bits in r_i outside the designated field remain unchanged. Without field selection, this instruction operates to write (m') over (r_i) except for the sign of (r_i), which is unchanged.

1. m' is indirectly addressable and field selectable.
2. Operands may be multi-word.

13200 REGISTER-TO-MEMORY WORD TRANSFER INSTRUCTIONS

In these, one or more of the four arithmetic registers may be designated. If more than one register is designated, they need not be adjacent, but the words will be transferred to consecutive locations in memory.

13210 STORE

OPERATION CODES: Octal 10, Mnemonic ST

$(r_i) \rightarrow m'$

The contents of r_i replace those of m'.

1. m' is indirectly addressable but not field selectable.
2. Operands may be multi-word.
3. (r_i) not changed.

13220 STORE NEGATIVE

OPERATION CODES: Octal 11, Mnemonic STCS

$-(r_i) \rightarrow m'$

The contents of r_i, with sign changed, replace those of m'.

1. m' is indirectly addressable but not field selectable.
2. Operands may be multi-word.
3. (r_i) not changed.

14000 LOGICAL INSTRUCTIONS

This class of instruction performs logical and bit manipulation functions. The operation chart provided shows:

	r_i before execution
m' before execution	r_i after execution

14100 SUPERIMPOSE

OPERATION CODES: Octal 15, Mnemonic SUP

A "1" in a bit position of (m') results in a "1" in the corresponding bit position of (r_1). All other bit positions of r_i remain unchanged. $(r_i) \cup (m') \rightarrow r_i$, where $\cup$ is the logical "or" operation, for which the truth table is:

m' \ r_i	0	1
0	0	1
1	1	1

1. m' is field selectable and indirectly addressable. If field selection is used, bits outside the field in memory, bits outside the corresponding field of the register(s) and all sign bits are ignored.
2. Operands may be multi-word.
3. The operation affects all bits in each word, including the sign bit.

14200 ERASE

OPERATION CODES: Octal 16, Mnemonic ERS

A zero in a bit position of (m') results in a zero in the corresponding bit position of (r_i). All other bit positions of r_i remain unchanged.

$(r_i) \cap (m') \rightarrow r$, where $\cap$ is the logical "and" operation for which the truth table is:

m' \ r_i	0	1
0	0	0
1	0	1

1. m' is field selectable and indirectly addressable. If field selection is used, bits outside the field in memory, bits outside the corresponding field of the register(s) and all sign bits are ignored.
2. Operands may be multi-word.
3. The operation affects all bits in each word, including the sign bit.

14300 SET SENSE INDICATOR

OPERATION CODES: Octal 62, Mnemonic SSI

This instruction, like the RSI (14400), refers to a group of sense indicators located within the central processor. These indicators are available to the programmer for changing instruction sequences, or for program alterations. There are eight sense indicators, numbered 0 (zero) through 7.

Set the sense indicator specified by the binary number in bits 11-14 of the instruction.

1. Indirect addressing is possible, though meaningless, as the address field is not examined; field selection is not permitted.
2. Bit positions 1 through 10 of the instruction are not used.

14350 SET INHIBIT INPUT/OUTPUT INTERRUPT INDICATOR

OPERATION CODES: Octal 62, Mnemonic PIO.

Sets the Inhibit Input/Output Interrupt Indicator, addressed in bits 11-14 of the instruction, by the bit pattern 0000.

1. Indirect addressing is possible, though meaningless, as the address field is not examined; field selection is not permitted.

14400 RESET SENSE INDICATOR

OPERATION CODES: Octal 61, Mnemonic RSI.

Reset the sense indicator specified by the binary number in bits 11-14 of the instruction.

1. Indirect addressing is possible, though meaningless, as the address field is not examined; field selection is not permitted.
2. Bit positions 1 through 10 of the instruction are not used.
3. This instruction prevents interrupt until AFTER execution of the next instruction, in order to avoid ambiguity in the event that an interrupt condition is incipient at the time of execution of the original instruction.

14450 RESET PROCESSOR ERROR INDICATORS

OPERATION CODES: Octal 65, Mnemonic RPE, (AR bits 0001).

Reset the processor error indicator specified by bit positions 1-10 of the instruction.

1. The indicators affected are listed in Paragraph 11902A.
2. The instruction may reset any number of processor error indicators. Each indicator is specified by a unique bit position in the field consisting of positions 1-10, and inclusion of several such "1" bits will cause resetting of the several associated indicators. An attempt to reset an undefined indicator will not cause an error condition.
3. The instruction may employ indirect addressing but not field selection.
4. This instruction prevents interrupt until AFTER execution of the next instruction, in order to avoid ambiguity in the event that an interrupt condition is incipient at the time of execution of the original instruction.

14500 RESET CONTINGENCY INDICATORS

OPERATION CODES: Octal 65, Mnemonic RCI, (AR bits 0010).

Reset the contingency indicator specified by bit positions 1-10 of the instruction.

1. The indicators affected include the following:
   a. Overflow
   b. Instruction Code not part of machine repertoire.
   c. Control Console Signal
   d. Keyboard Request
   e. End of Message
   f. Console Contingency Interrupt
2. The instruction may reset any number of contingency indicators. Each indicator is specified by a unique bit position in the field consisting of positions 1-10, and inclusion of several such "1" bits will cause resetting of the several associated indicators. An attempt to reset an undefined indicator will not cause an error condition.
3. The instruction may employ indirect addressing but not field selection.
4. This instruction prevents interrupt until AFTER execution of the next instruction, in order to avoid ambiguity in the event that an interrupt condition is incipient at the time of execution of the original instruction.

14550 RESET INHIBIT INPUT/OUTPUT INTERRUPT INDICATOR

OPERATION CODES: Octal 61, Mnemonic AIO.

Resets the Inhibit Input/Output Interrupt Indicator addressed in bits 11-14 of the instruction.

1. Indirect addressing is possible, though meaningless, as the address field is not examined; field selection is not permitted.
2. This instruction prevents interrupt until AFTER execution of the next instruction, in order to avoid ambiguity in the event that an interrupt condition is incipient at the time of execution of the original instruction.

14600 RESET INPUT/OUTPUT INTERRUPT AND ERROR INDICATORS AND ASSOCIATED STANDBY LOCATION INDICATOR

OPERATION CODES: Octal 65, Mnemonic RIO

Reset the I/O Interrupt or Error Indicators specified by bits 1-10 of the instruction, for the synchronizer specified by bits 11-14.

1. The indicators affected include the following:
   a. Interrupt Indicators associated with I/O channels 1 through 13.
   b. I/O Error Indicators.
2. For any given synchronizer, the instruction may reset any number of available indicators. Each indicator is specified by a unique bit position in the field consisting of positions 1-10, and inclusion of several such "1" bits will cause resetting of the several associated indicators. An attempt to reset an undefined indicator for a given synchronizer will not cause an error condition.
3. The instruction may employ indirect addressing, but field selection is not permitted.
4. The standby location indicator associated with the specified synchronizer may also be reset by this instruction.
5. This instruction prevents interrupt until AFTER execution of the next instruction, in order to avoid ambiguity in the event that an interrupt condition is incipient at the time of execution of the original instruction.

15000 COMPARISON INSTRUCTIONS

The following instructions perform comparisons of a field in memory with a word in the arithmetic registers. The result of a comparison is reflected in the Equal, High or Low Indicators and is based on the relationship of the register to the memory field. Comparison is based upon the binary value of the operand. See 12000 for the effect of + and - operations on the EQUAL indicator.

15100 COMPARE ALGEBRAIC

OPERATION CODES: Octal 54, Mnemonic C

(r_i) is compared algebraically to (m').

1. The contents of r_i and m' are unchanged.
2. m' is field selectable and indirectly addressable.
3. Operands may be multi-word.
4. If $(r_i) < (m')$ the Low Indicator is set.
   If $(r_i) = (m')$ the Equal Indicator is set.
   If $(r_i) > (m')$ the High Indicator is set.
5. While comparison for multi-word operands considers algebraically the sign of the least significant word, signs of more significant words are completely ignored.
6. The sign in the least significant word is considered as a true sign. Any negative quantity is less than any positive quantity; if both operands are negative, the number with the greater absolute binary value is considered to be the smaller of the two operands, i.e.,"-000003" is less than "-000002".
7. Addition and subtraction will force a zero answer (decimal or binary) to be positive. However, there will be some single words consisting of six decimal zeros with a minus sign. Such a word would not be equal in this Algebraic Comparison to the word "+00000" (plus decimal zeros).

15100 COMPARE ALGEBRAIC (Continued)

8. When field selection is employed, the comparison is made only on the field selected portion of the operand from memory and the corresponding bit positions of the operand in the AR(s). In this case the sign of the operand from memory is always considered to be positive while the sign of the operand in the AR(s) is the sign of the least significant AR involved.

15200 COMPARE ABSOLUTE

OPERATION CODES: Octal 55, Mnemonic CA

(r_i) is compared absolutely with (m') and the appropriate indicator is set. (Signs are ignored).

1. The contents of r_i and m' are unchanged.
2. m' is field selectable and indirectly addressable.
3. Operands may be multi-word.

15300 COMPARE FOR SELECTED 1's

OPERATION CODES: Octal 57, Mnemonic CONE

For each bit position in the designated AR that contains a "1", the corresponding bit position of (m') is compared for a "1". If all comparisons result in equality the Equal Indicator is set. If not, the High Indicator is set. If the AR contains all zeros, the Equal Indicator is set regardless of (m'). (Bits 25 are included in the comparison unless Field Selection is specified).

1. The contents of r_i and m' are unchanged.
2. m' is field selectable and indirectly addressable. If field selection is used, bits outside the field in memory, bits outside the corresponding field in the register(s) and bits 25 are ignored.
3. Operands may be multi-word.

15400 COMPARE FOR SELECTED 0's

OPERATION CODES: Octal 56, Mnemonic CZRO

For each bit position in the designated AR that contains a "1", the corresponding bit position of (m') is compared for a "0". If all comparisons result in equality, the Equal Indicator is set. If the AR contains all zeros, the Equal Indicator is set regardless of (m'). (Bits 25 are included in the comparison unless Field Selection is specified).

1. The contents of r_i and m' are unchanged.
2. m' is field selectable and indirectly addressable. If field selection is used, bits outside the field in memory, bits outside the corresponding field in the register(s) and bits 25 are ignored.
3. Operands may be multi-word.

16000 SHIFT INSTRUCTIONS

This section covers the Shift Instructions within the Arithmetic Registers. In all cases the registers involved are designated by the AR field (bit positions 11-14). The Shift Count Field (bit positions 1-10) specifies the number of positions (Binary Bit, Decimal Digit or Alphanumeric Character) the operand is to be shifted. The count is expressed in binary notation. A shift count of zero causes a shift of zero positions. A shift count that exceeds the maximum allowable positions will result in the destruction of the operands in the AR(s) or their being shifted an incorrect number of positions. For the Decimal Shift Instructions, the following codes are converted as shown when shifted:

0000 to 0011	1101 to 0011	These cases produce carry to next higher digit.
0001 to 0011	1110 to 0100	
0010 to 0011	1111 to 0101	

16100 SHIFT DECIMAL RIGHT

OPERATION CODES: Octal 40, Mnemonic SR

(r_i) is shifted right the number of 4-bit decimal-digit positions specified by m' in the instruction.

1. The sign is not shifted.
2. Decimal zeros are inserted in the most significant portion of the registers affected. Low order digits are lost when shifted.
3. The shift may occur in one or two registers. In the latter case the registers need not be adjacent, but a shift cannot take place from one register into another with lower numerical designation.
4. The operation is indirectly addressable, but not field selectable.

16200 SHIFT DECIMAL LEFT 41

(r_i) is shifted left the number of 4-bit decimal digit positions specified by m', in the instruction.

1. The sign is not shifted.
2. Decimal zeros are inserted in the least significant portion of the word. Digits shifted past the high order position of the operand are lost.
3. The shift may occur in one or in two registers. In the latter case, the registers need not be adjacent, but a shift cannot take place from one register into another with higher numerical designation.
4. The operation is indirectly addressable but not field selectable.

16300 SHIFT BINARY RIGHT CIRCULAR 44

(r_i) is circularly shifted right the number of binary positions specified by the instruction.

1. The operation is limited to one 25-bit word.
2. The operation is indirectly addressable but not field selectable.
3. The sign is shifted.
4. Bits shifted past the least significant position enter the high-order positions. For example, for a shift of one position, the low-order bit enters the sign position, the sign bit enters position 24, etc.

16400 ALPHANUMERIC SHIFT RIGHT 42

(r_i) is shifted right the number of 6-bit alphanumeric-character positions specified by m'.

1. The sign is not shifted.
2. Binary zeros are inserted in the most significant portion of the word.
3. The shift may occur in one or two registers. In the latter case the registers need not be adjacent, but a shift cannot take place from one register into another with lower numerical designation.
4. The operation is indirectly addressable but not field selectable.

16500 ALPHANUMERIC SHIFT LEFT 43

(r_i) is shifted left the number of 6-bit alphanumeric character positions specified by the instruction.

1. The sign is not shifted.
2. Binary zeros are inserted in the least significant portion of the word.
3. The shift may occur in one or two registers. In the latter case the registers need not be adjacent, but a shift cannot take place from one register into another with higher numerical designation.
4. The operation is indirectly addressable but not field selectable.

17000 TRANSFER OF CONTROL INSTRUCTIONS

17100 UNCONDITIONAL TRANSFER OF CONTROL

OPERATION CODES: OCTAL, 06; MNEMONIC, TUN.

$m' \rightarrow CC$

The contents of the Control Counter are replaced by bits 1-15 of m'.

1. m' is indirectly addressable but not field selectable.

17200 TEST PROCESSOR INDICATOR

OPERATION CODES: OCTAL, 60; MNEMONICS, THI, TLO, TEQ, TPOS, TSI and TIOP.

Is indicator set?
- Yes: $m' \rightarrow CC$
- No: $(CC) + 1 \rightarrow CC$

The indicator specified by bits 11-14 of the instruction is tested. If the indicator is set, the contents of the control counter are replaced by the indexed m-address.

1. Only one indicator may be tested at one time.
2. m' is indirectly addressable, but not field selectable.
3. The Inhibit Input-Output Interrupt Indicator may be set, reset and tested by instructions. This is also true of Sense Indicators. The other processor indicators can only be tested.
4. The sign indicator for r_i will be set if the sign of r_i is plus.

17300 TEST INPUT/OUTPUT ERROR, INTERLOCK AND INTERRUPT INDICATORS

OPERATION CODES: OCTAL, 64; MNEMONICS, TPE, TCI and TIO.

Is indicator set?
- Yes: $(CC) + 1 \rightarrow CC$
- No: $(CC) + 2 \rightarrow CC$

The indicator specified by a bit in the field comprising bit positions 1-10, for the synchronizer specified in bit positions 11-14, is tested. If it is set, the next instruction in sequence will take place. (This instruction will usually be an unconditional transfer). If the indicator is not set, the next instruction will be skipped.

1. The instruction may test several indicators for one synchronizer at one time. If any one of them is set, the next instruction in sequence will take place. If none is set, the next instruction will be skipped. (As each indicator is designated by a unique bit position, specification of several is accomplished by placing "1's" in the appropriate positions).
2. The indicators are not reset when tested, but are reset by an instruction, which may reset the several indicators for a synchronizer separately or in combination.
3. m' may be indirectly addressed but is not field selectable.
4. An attempt to test an undefined indicator for a synchronizer will result in the same condition as a test of a defined indicator which is NOT set.
5. Indicators for the Computer Error interrupts are tested when 0001 is the address placed in the AR bit positions of the instruction; while indicators for Contingency Interrupts are tested when 0010 is placed in the AR bit positions (See Paragraph 11902 A and B).

18000 DATA EDITING AND CONVERSION INSTRUCTIONS

This section provides for the editing of data words for input/output data handling.

18100 CHARACTER CODE EXPANSION AND COMPRESSION INSTRUCTIONS

These instructions are used for converting 6-bit character codes to 4-bit codes and vice versa. Decimal arithmetic will produce correct results only if performed on numeric operands consisting of 4-bit numeric characters.

18110 COMPRESS

OPERATION CODES: Octal 72, Mnemonic ATD

$(m'-2, m'-1, m') \rightarrow$ MS AR, LS AR

Three alphanumeric words from memory are compressed into two numeric words and placed into two accumulating registers.

1. (m') may be indirectly addressed but not field selected.
2. The signs of the two-word result are the same as that of the least significant word of the three-word operand.
3. The two AR's involved need not be adjacent.

18120 EXPAND

OPERATION CODES: Octal 71, Mnemonic DTA

(MS AR, LS AR) $\rightarrow m'-2, m'-1, m'$

Two numeric words from two accumulating registers are expanded to three alphanumeric words, by the addition of two zero zone bits, and placed into three memory locations.

1. (m') may be indirectly addressed but not field selected.
2. The signs of the three-word result are the same as that of the least significant word of the 2-word operand.
3. The two AR's involved need not be adjacent.

18210 ZERO SUPPRESS

OPERATION CODES: Octal 73, Mnemonic ZUP

$(m') \rightarrow r_i$

This instruction operates only upon 6-bit alphanumeric character codes. The following non-significant codes are replaced with 000000 (SPACE): 000000 SPACE, 000001 ; (COBOL-FORTRAN) or) (UNIVAC III - USS), 000010 MINUS, 000011 ZERO and 110010 COMMA. Any other 6 bit combination will stop the edit.

1. (m') may be indirectly addressed but not field selected.
2. May be multi-word.
3. The sign is preserved.
4. The address, m', must refer to the position in memory in which the high-order word is found, when multi-word suppression is employed. The words of multi-word operand must be in consecutive positions of memory, but the suppressed result may be developed in non-adjacent registers.

18300 90 COLUMN TRANSLATE INSTRUCTIONS

These instructions exist only in systems utilizing 90 Column Card Equipment.

18310 TRANSLATE 90 COLUMN CARD CODE TO MACHINE CODE

OPERATION CODES: OCTAL 74; MNEMONIC, NITA.

$(m') \rightarrow r_i$

The contents of m' are translated into four 6-bit alphanumeric characters and the result placed in the AR specified by bit positions 11-14 of the instruction.

1. (m') may be indirectly addressed but not field selected.
2. Bit position 25 of the result in AR_i is zero.
3. Operands may be multiword.

18320 TRANSLATE MACHINE CODE TO 90 COLUMN CARD CODE

OPERATION CODES: OCTAL 75; MNEMONIC, ATNI.

$(m') \rightarrow r_i$

The contents of m' are translated into four 6-bit 90 column card code characters and the result placed in the AR specified by bit positions 11-14 of the instruction.

1. (m') may be indirectly addressed but not field selected.
2. Bit position 25 of the result in AR_i is zero.
3. Operands may be multiword.

19000 INPUT-OUTPUT INSTRUCTIONS

OPERATION CODES: Octal 70; Mnemonic IOF

Input-Output operations, except those pertaining to the typewriter, are executed by means of a pair of instructions.

The first is the Initiate Input-Output Operation instruction which has the following format:

IA	IR	OPR	SYNC.	m-ADDRESS
25	24 21	20 15	14 11	10 1

This instruction specifies the synchronizer and the location of the I/O instruction. The execution of this instruction causes (m') to be loaded into the unique standby memory location associated with the specified synchronizer. The synchronizer standby location enables continuous tape motion when executing I/O operations on the same servo, and overlap of tape start-stop time when using different servos. The standby locations are in core memory and are addressable. They occupy positions 03 through 15, and are addressed in memory at the same binary address as the AR bit address of their associated synchronizers (See Paragraph 11902).

The second word is the Input-Output instruction which serves to indicate the precise I/O operation to be performed, the unit involved, and for reading and writing on Uniservo III with control words, the absolute m-address of the first Tape Control Word. For other I/O units, the absolute address is that of the first word of the sequence to be transferred to the synchronizer. These are further explained in sections 19100, 19200, 19400 and 19600.

The I/O Instruction Words have the following format:

0	UNIT (or Line Count)	OPR	m-ADDRESS
25	24 21	20 16	15 1

Bit position 25 must be zero.

Operation of the I/O instruction pair is as follows:

1. An Initiate I/O instruction places an I/O instruction into a synchronizer standby location and sets its standby location interlock indicator.
2. When the synchronizer becomes available, the standby location interlock indicator is tested. If it is set, the synchronizer will take the I/O instruction word from the standby location for execution and for card equipment will reset the standby location interlock indicator. For Uniservos, the High Speed Printer and the Paper Tape Reader-Punch, the instruction must be successfully accessed from memory and must be executable by the synchronizer before the Standby Location Interlock Indicator is reset.

19000 INPUT-OUTPUT INSTRUCTIONS (Continued)

3. If the standby location interlock indicator is not set, the synchronizer does nothing until the standby location interlock indicator is set.
4. If the standby location interlock indicator is set, and an initiate I/O instruction is given, the associated I/O instruction will replace the one held by the standby location. In normal use, the standby location interlock indicator should be tested and found reset before an initiate I/O instruction is given. If it is found set, and an instruction is given, there is no guarantee that the instruction previously in the standby location will not be executed while the new one is being entered.
5. A switch is provided on the Univac III Servos, to allow the operator to select Univac III Compatible mode. When ON, this switch causes the Servo to transmit 3 A/N Characters plus a parity bit for each, for every memory word. When OFF, the regular 4 character word is transmitted (or 6 decimal digit word). In normal Univac III mode data on tape is word organized. See the Flow-of-Data Chart at the end of Paragraph 31000.
6. Successful Completion Interrupts are handled in a special way for the Uniservo synchronizers. See subparagraph 8 at the end of Paragraph 11320.

19050 UNISERVO III/IIIA TAPE UNIT SYNCHRONIZER INSTRUCTIONS

The information in sections 19051 through 19199 applies to both the UNISERVO III and UNISERVO IIIA Tape Units unless otherwise noted.

19051 OPERATION CODES FOR UNISERVO III TAPE UNIT INPUT/OUTPUT INSTRUCTION WORDS

The following operation codes are meaningful for the UNISERVO III/IIIA Tape Units:

Bit Position 17	18	19	20	Operation	Mnemonic Code
0	0	0	0	Read Tape Forward with Control Word	FSR
0	0	1	0	Read Tape Forward without Control Word	FBR
0	0	0	1	Forward Contingency Scatter Read	FCSR
0	0	1	1	Forward Contingency Block Read	FCBR
0	1	0	0	Read Backward with Control Word	BSR
0	1	1	0	Read Backward without Control Word	BBR
0	1	0	1	Backward Contingency Scatter Read	BCSR
0	1	1	1	Backward Contingency Block Read	BCBR
1	0	0	0	Write Tape	GWT
1	0	1	0	Write Bad Spot Pattern and then Write Data (Contingency Write)	OWT
1	1	0	0	Rewind	RW
1	1	1	0	Rewind and Interlock	RWI
1	1	1	1	Load Point Test	LPT

See Section 19150 for explanation of Forward and Backward Contingency Scatter Reads.

Whenever the position of the Load Point window is changed and prior to initial use, the tape must be bulk erased to insure reliable operation during the initial block.

To start writing on a tape which has just been previously read forward, it is necessary to use the Contingency Write Operation, so that erased tape can be advanced from the erase head to the write head of the tape unit. The Contingency Write Operation cannot be used after a Backward Read operation but may be used after a Gather-Write.
IMPORTANT - PROGRAMMING CONVENTION: The block to be overwritten must be a minimum of 150 words in length in order to make certain that a short block of data does not remain between the last block read and the first block overwritten.

Rewinds can be executed by either the Read or the Write Synchronizer.

If a Read order is issued to a Write Synchronizer (without the Read option) or vice versa, the instruction is not performed, and the fault indicator for the synchronizer is set.

19100 TAPE INSTRUCTIONS

19110 GATHER-WRITE

OPERATION CODE: Mnemonic GWT

All writing of data on tape must be done by Gather-Write instructions. The address contained in the I/O word will indicate the absolute memory location of the first word of a list of control words for writing data on tape. This list must be in consecutive memory locations. The first word of the control word list must not be a stop control word as this case will cause tape runaway.

The format of a Read-Write tape control word is as follows:

	COUNT	ADDRESS
25	24 16	15 1

When bit position 25 contains a one (1), the control word is a "STOP" control word and ends reading or writing. Other bits in a stop control word have no significance to the tape synchronizer; however, the value in bit positions 1-15 must not exceed the highest memory address available in the system concerned. If bit position 25 is a zero, bits 1 to 15 indicate the memory location of the first word of a given segment to be written on tape. Bits 16 to 24 indicate the number of words in the segment to be written up to a normal maximum of 511. All zeros in this field call for writing of 4096 words. Writing is terminated by accessing a control word containing a 1 in bit 25. A stop control word causes the recording of a reverse start sentinel on tape.

For example, a write instruction that references memory location 1000_8 is to be performed and the calling sequence in 1000_8 contains the following:

1000	XX 0	001100000 (= Dec. 96)	000011000111110 (= Oct. 3076)
1001	XX 0	000101010 (= Dec. 42)	000011010000100 (= Oct. 3204)
1002	XX 1	000000000	000000000000000

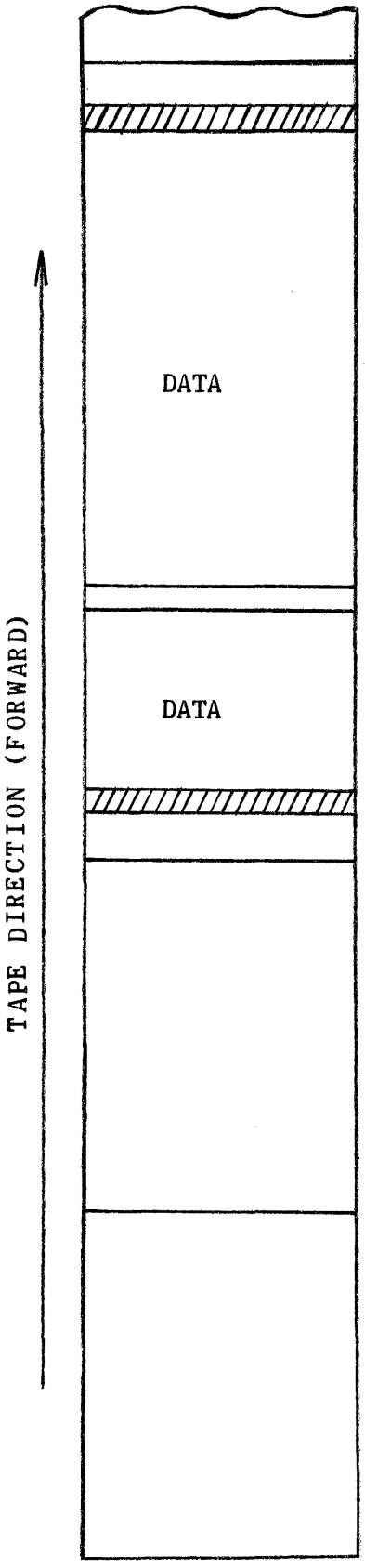
The following will occur: 96 words will be written starting with location 3076_8 in core. The second control word will cause 42 words to be written out starting with location 3204_8 in core. Accessing the third control word terminates writing because of the 1 in bit 25.

Between each group of data words on tape, is a segment separator which provides the synchronizer with a means of control when the tape is later read in the scatter mode.

A Forward Start sentinel is automatically written on tape preceding the first data word. The following diagram describes the array of this data on tape.

19110 GATHER-WRITE (Continued)

LAYOUT OF BLOCK ON TAPE



	NUMBER OF FRAMES
← ERASED TAPE GAP (Varying Distance)	
← FORWARD START PATTERN	20 - 30
← FORWARD START SENTINEL	3
← 10 DATA WORDS	30
← (SEGMENT SEPARATOR)	3
← 5 DATA WORDS	15
← REVERSE START SENTINEL	3
← REVERSE START PATTERN	20 - 30
← PATTERN IN ODD CHANNELS ONLY FOR APPROXIMATELY ONE QUARTER INCH	227
← ERASED TAPE GAP (Varying Distance)	

19120 SCATTER FORWARD READ

OPERATION CODE: Mnemonic FSR

Scatter Forward Read is performed in a manner similar to gather-write. The address in the read instruction gives the location of a sequence of control words in memory to control scatter reading. The control word for reading has the same format as a gather-write control word. An example will best describe how scatter reading is performed:

A control word specifies that 30 words are to be read into memory starting at location 1500. The specified tape is moved forward, reading 30 data words from tape into memory beginning with locations 1500 and ending in location 1529.

As each data word is read into memory, a one is subtracted from the count specified by the control word, in this case 30. When the count reaches zero, tape is moved until a segment separator on tape is detected. This is the next word on tape if the control word in memory has exactly the same count as the number of words in the segment of data written on tape. When the segment separator on tape is detected, the next control word in sequence in memory is accessed, and reading continues into the location specified by that control word, without transferring the segment separator to memory.

If a segment separator is detected while reading and the current control word count has not reached zero, then the count is cleared to zero and the next control word in sequence is accessed. In no case are segment separators on tape transferred to memory.

All reads are terminated by encountering the reverse start sentinel or a stop control word in memory, whichever occurs first. This will terminate the current read without further transference of data to memory. The synchronizer becomes available when the inter-block gap is sensed. When a Scatter Forward Read instruction references a stop control word as its first control word, no words are transferred to memory and the tape is moved forward to the next interblock gap.

19130 SCATTER BACKWARD READ

OPERATION CODE: Mnemonic BSR

Same as Scatter Forward Read except that memory locations specified by the control words in memory will be the LAST WORD address of a given segment. For example, if a segment would normally be read into 1500 through 1523 in a forward direction then 1500 would be specified as the first word address and a count of 24 would be specified. However, when reading backward, 1523 would be specified as the address of the first word to be read into memory. Subsequent words will be read in by decrementing the given address, until the segment count reaches zero or a segment separator on tape is encountered. Thus, the sequence of data from a block of tape, as it appears in memory, remains the same whether read backward or forward. The sequence of the control words in memory is also reversed; so that accesses of control words will be made by decrementing from the first control word address as specified in the Initiate I/O Order. When a Scatter Backward Read instruction references a stop control word as its first control word, no words are transferred to memory and the tape is moved backward to the next interblock gap.

19140 READ WITHOUT CONTROL WORD

OPERATION CODE: Mnemonic FBR

Read Without Control Word will read into consecutive memory locations starting with the initial memory location specified until an inter-block gap is sensed.

19145 BACKWARD READ WITHOUT CONTROL WORD

OPERATION CODE: Mnemonic BBR

Backward Read without Control Word will transmit data into consecutive memory locations beginning at the initial high order memory location and ending when an inter-block gap on tape is sensed.

19150 FORWARD CONTINGENCY SCATTER READ
OPERATION CODE: Mnemonic FCSR
FORWARD CONTINGENCY BLOCK READ
OPERATION CODE: Mnemonic FCBR
BACKWARD CONTINGENCY SCATTER READ
OPERATION CODE: Mnemonic BCSR
BACKWARD CONTINGENCY BLOCK READ
OPERATION CODE: Mnemonic BCBR

See paragraph 11353 A, III, g.

For proper Uniservo III Tape Operation, Contingency Read commands should be used as follows:

Backward Contingency Read (BCSR or BCBR) is to be issued only following an Error B (block written without error but read with error) on forward read, to position the tape in the gap preceding the block in which the error was found.

Forward Contingency Read (FCSR or FCBR) must only be issued after a backward read. It then causes skipping of the block just read and the reading of the subsequent block.

19155 LOAD POINT TEST

OPERATION CODE: Mnemonic LPT

The execution of this instruction reflects in the resultant setting of indicators whether or not the tape on the specified Uniservo is positioned at load point (first block condition). If positioned at load point, the Successful Completion Indicator will be set and interrupt will occur if specified. If not positioned at load point the Error B and Fault Indicators will be set. If the Uniservo is busy when tested, only the Busy Indicator will be set or if an abnormal condition exists in the Uniservo, only the Fault Indicator will be set. If the End of Tape Warning flip-flop in the specified Uniservo is set, the End of Tape Warning Indicator is set in combination with the indication of a "Not at Load Point", Busy or Fault Condition. Program Interrupt (a "1" in bit position 16) should always be specified.

19200 HIGH SPEED CARD READER INSTRUCTIONS

The information in this section applies to 80 and 90 column Card Readers unless otherwise stated.

19210 EXECUTION OF INITIATE I/O INSTRUCTION

Bits 1-10, modified by (IR) specified by bits 21-24, indicate the memory location of an I/O Instruction Word. Bits 11-14 specify a fixed synchronizer into whose standby location the I/O Instruction Word is to be placed. The contents of m' (the I/O Instruction Word) are transferred to the synchronizer standby location and the associated Standby Location Interlock Indicator is set. When the synchronizer becomes available, the I/O Instruction Word is taken from the standby location to the synchronizer for execution and the Standby Location Interlock Indicator is reset, whether or not the instruction transfer was successful. At this point, an I/O Interrupt occurs with the Interrupt Indicator unconditionally set, if bit position 16 is a "1". If an instruction error is detected, the Equipment Fault Indicator will also be set.

19220 I/O INSTRUCTION WORD CHARACTERISTICS

1. Bit positions 21-25 must contain zeros.
2. The contents of bit positions 1-15 enter the Memory Address Counter (MAC) when the I/O Instruction Word is transferred from the standby location to the synchronizer, thus establishing the memory address for the transfer of the first data word of the card at Read Station 2.
3. A bit in position 16 specifies interrupt upon transfer of the instruction to the synchronizer.
4. A bit in position 17 causes card feeding.
5. A bit in position 18 causes translation of 80-column or 90-column card code to Univac III code.
6. A bit in position 19 causes selection of Stacker 1.
7. A bit in position 20 causes selection of Stacker 2. If neither Stacker 1 nor 2 is selected, Stacker "0" is automatically selected. If both Stacker 1 and 2 are specified, the card will be selected into Stacker 2.
8. For correct transfer to or from card equipments all card images must have their first word in a location whose address ends in 000000.
9. The following operation codes are acceptable to the High Speed Card Reader (with or without Program Interrupt specified in bit position 16):

MNEMONIC CODE	BIT POSITIONS 20	19	18	17	
CAD	0	0	0	0	No operations specified (However, if a card is at the selected Read Station its image is transferred to memory).
FC	0	0	0	1	Feed Card.
CT	0	0	1	0	Translate.
FCT	0	0	1	1	Feed Card and Translate.
CS1	0	1	0	0	Select Stacker 1.
FCS1	0	1	0	1	Feed Card and Select Stacker 1.
CTS1	0	1	1	0	Translate and Select Stacker 1.
FCTS1	0	1	1	1	Feed Card, Translate and Select Stacker 1.
CS2	1	0	0	0	Select Stacker 2.
FCS2	1	0	0	1	Feed Card and Select Stacker 2.
CTS2	1	0	1	0	Translate and Select Stacker 2.
FCTS2	1	0	1	1	Feed Card, Translate and Select Stacker 2.
CS2	1	1	0	0	Select Stacker 2.
FCS2	1	1	0	1	Feed Card and Select Stacker 2.
CTS2	1	1	1	0	Translate and Select Stacker 2.
FCTS2	1	1	1	1	Feed Card, Translate and Select Stacker 2.

19230 EXECUTION OF I/O INSTRUCTION WORD

The Operation Code, Bits 16-20, is transferred to the specified synchronizer and the m-Address, Bits 1-15, is transferred to the synchronizer MAC. If instructions are not given for subsequent cards, their images will be transmitted to the same area of memory in the same mode as specified by bit position 18 of the last instruction executed. The Stacker Bits, 19 and 20, select the stacker to receive the card moving from card station 4 to the stacker section. The Translation Bit, 18, if a "1", causes the card passing through Read Station 2 to be translated from 80 or 90 column card code to machine code. If Bit 18 is "0", the card is transferred as stated in paragraph 19250 or 19252.

19240 AUTOMATIC CARD TRANSLATION

Normally, 80-column cards read in the Hollerith code and 90-column cards read in Remington Rand 90-column code are automatically translated into Univac III machine language code, while being transmitted by the synchronizer from the card reader to memory. The data from a card occupy 20 (for the 80-column Reader) or 24 (for the 90-column Reader) consecutive words of memory. Transfer of the data from the 80-column Reader to the memory requires 1.92 milliseconds of memory time (480 memory cycles). Transfer of data from the 90-column Reader to the memory requires 1.15 ms. (288 memory cycles) of memory time.

19250 CARD IMAGE

It is also possible to read cards directly into memory without translation in the manner indicated by the following diagrams:

80-Column Card Image:

Bit Positions
Of Corresponding
Card Image Words

	1	4 5	8 9 10 11 12	73	76 77	80
12			19 13 7 1			
11	Goes		20 14 8 2			
0	to		21 15 9 3	m+4		
1	Word m	m+2	22 16 10 4	m+36	m+38	
2	In Memory		23 17 11 5			
3			24 18 12 6			
4			19 13 7 1			
5			20 14 8 2			
6			21 15 9 3	m+5		
7	m+1	m+3	22 16 10 4	m+37	m+39	
8			23 17 11 5			
9			24 18 12 6			

Position 25
(not shown)
is zero.

Digit Positions

m+4	0	24-19	18-13	12-7	6-1
m+5	0	24-19	18-13	12-7	6-1

Locations m+4 and m+5 in memory

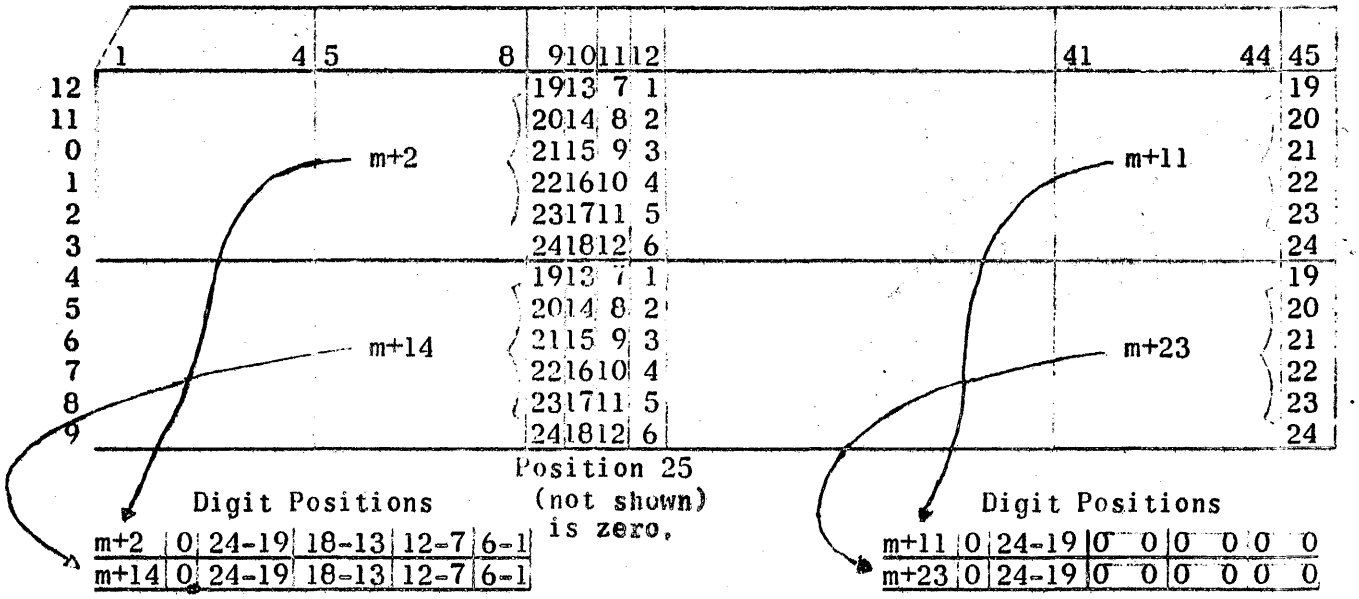
m' contains a bit for each hole either sensed while reading or to be punched in a card.
Column 1, rows 12-3, is represented by the most significant character of the contents of m.
Column 2, rows 12-3, is represented by the next most significant character of the contents of m.
Column 1, rows 4-9, is represented by the most significant character of the contents of m + 1.
The whole card image is thus represented by 160 characters (i.e., 40 words) with two characters representing one column.

19252 90-COLUMN CARD IMAGE

This image is similar to the 80-column card image except that a whole card is represented by 90 characters (i.e., 24 words) with one 6-bit character representing each of the columns 1-90.

However, the first forty-five columns of a ninety column card (the upper half of the card) will be transferred into the first twelve memory words allotted for the card image (with the three least significant characters of the twelfth word filled in with binary zeros) and columns 46 through 90 -- the lower half of the card -- will be transferred into the second twelve memory words allotted for the card image (with the three least significant character positions of word 24 filled in with binary zeros).

Bit Positions
Of Corresponding
Card Image Words



19260 90 COLUMN READ FEATURE FOR 80 COLUMN READER

19261 As an extra cost option to the customer, the Model 133 80 column card reader shall be able to read 90 column cards in the untranslated mode. This shall be accomplished by the operator replacing the 80 column brush assemblies with 90 column brush assemblies. The 90 column cards shall be oriented in the feed track, 9 edge (lower edge) first, face up.

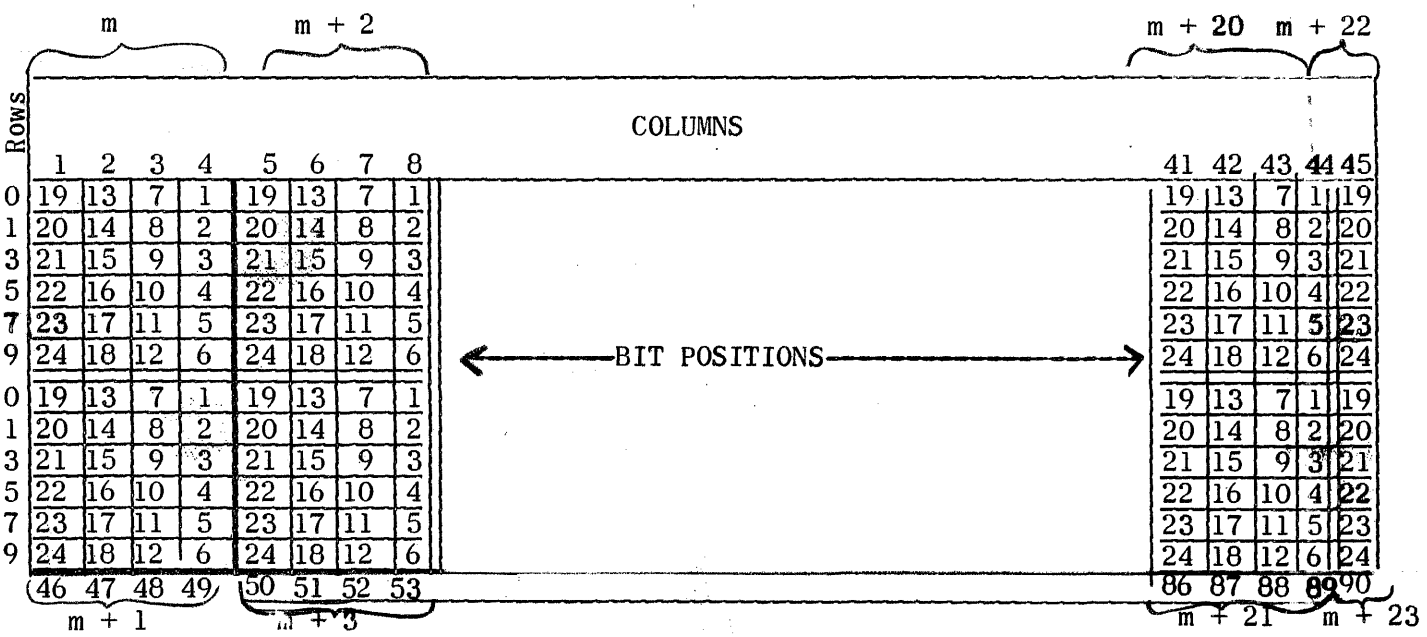
19262 The untranslated information from columns 1 through 45 of the 90 column card shall be transferred to memory, four columns per location, to locations m, m+2 and all even numbered locations through m+22. (Location m is specified by the address in the 15 least significant bit positions of the card reader function specification word.) The 18 least significant bit positions of location m+22 and all bit positions of location m+24 and all even numbered locations through m+38 shall contain binary zeros.

The untranslated information from columns 46 through 90 shall be transferred to memory, four columns per location, to locations m+1 and all odd numbered locations through m+23. The 18 least significant m+25 and all odd numbered locations through location m+39 shall contain binary zeros.

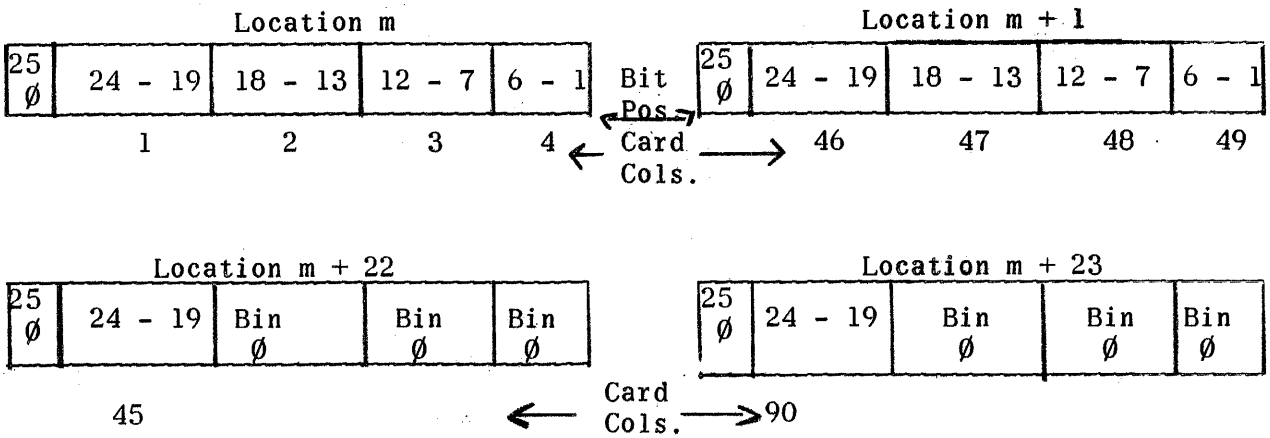
19263 All checking that takes place when the Model 133 reads 80 column cards in the untranslated mode, shall also be performed when using this option.

19264 The following chart illustrates how the 90 column card image is stored in the 40 word image in memory.

90 COLUMN CARD



CARD IMAGE AREA IN MEMORY



19270 80 COLUMN READ FEATURE FOR 90 COLUMN READER

19271 As an extra cost option to the customer, the Model 182 90 column card reader shall be able to read 80 column cards in the untranslated mode. This shall be accomplished by the operator replacing the 90 column brush assemblies with 80 column brush assemblies. The 80 column cards shall be oriented in the feed track 9 edge (lower edge) first, face down.

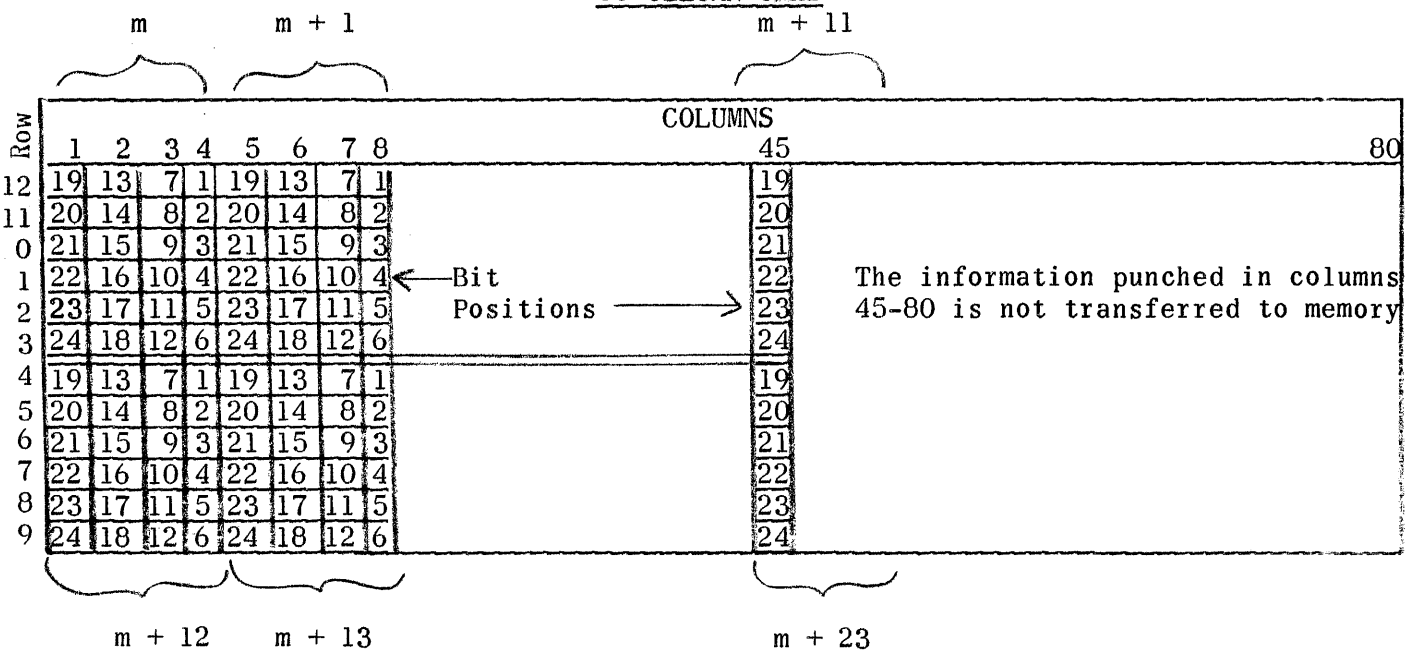
19272 The untranslated information from columns 1 through 45, rows 12 11, 0, 1, 2 and 3, shall be transferred to memory locations m through m+11. (Location m is specified by the address in the 15 least significant bit positions of the card reader function specification word.) The 18 least significant bit positions of location m+11 shall contain binary zeros. The untranslated information from columns 1 through 45, rows 4, 5, 6, 7, 8 and 9, shall be transferred to memory locations m+12 through m+23. The 18 least significant bit positions of location m+23 shall contain binary zeros.

19273 The sensing of columns 1 through 45 shall be standard. If the sensing of 45 columns other than columns 1 through 45 is required, this shall be possible at an additional one time charge to the customer.

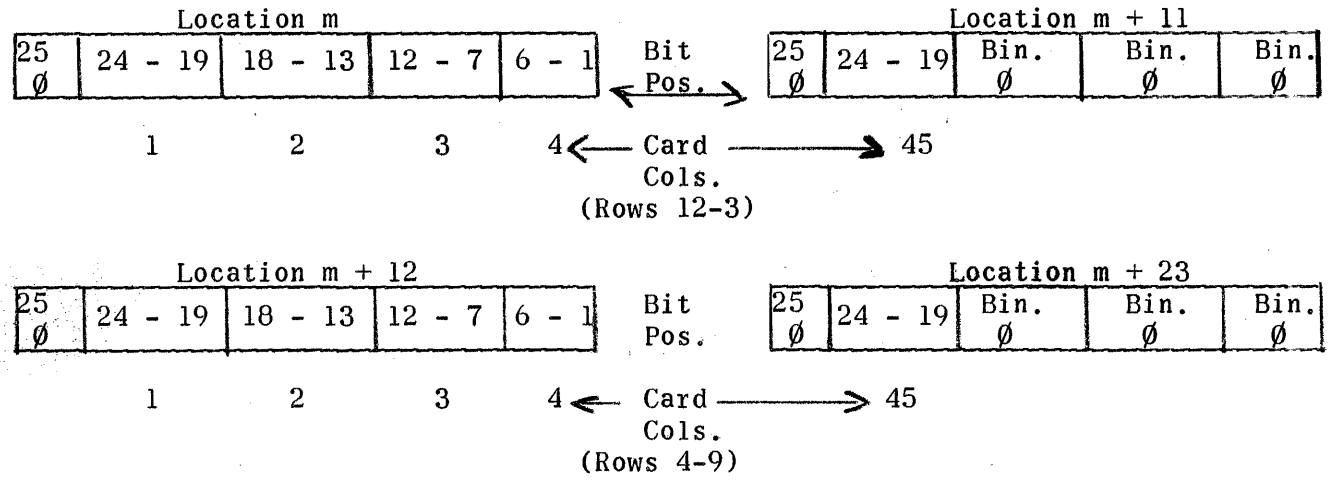
19274 All checking that takes place when the Model 182 reads 90 column cards shall also be performed when using this option, except that the hole count check shall only be made on columns 1 through 45.

19275 The following chart illustrates how the 80 column card image is stored in the 24 word image area in memory.

80 COLUMN CARD



CARD IMAGE AREA IN MEMORY



19300 CARD PUNCH UNIT INSTRUCTIONS

The information in this section applies to 80 and 90 column Card Punch units unless otherwise stated.

19310 EXECUTION OF INITIATE I/O INSTRUCTION

Bits 1-10, modified by (IR) specified by bits 21-24, specify the memory location of an I/O Instruction Word. Bits 11-14 specify the synchronizer into whose standby location the I/O Instruction Word is to be placed. The contents of m' (the I/O Instruction Word) are transferred to the synchronizer's standby location and the associated Standby Location Interlock Indicator is set. When the synchronizer becomes available, the I/O Instruction Word is transferred from its standby location to the synchronizer for execution; and the Standby Location Interlock Indicator is reset whether or not the instruction transfer was successful. At this point an I/O Interrupt takes place with the Interrupt Indicator unconditionally set, if bit position 16 is a "1". If an instruction error is detected, the Equipment Fault Indicator is also set. The synchronizer accesses an instruction at 300^{0} of the card cycle.

19320 I/O WORD CHARACTERISTICS

1. Bit positions 21-25 must contain zeros.

2. The contents of bit positions 1-15 enter the Memory Address Counter (MAC) when the I/O Instruction Word is transferred from the standby location to the synchronizer, thus establishing the memory address for the first data transfer to the card at the punch station. For correct transfer from memory to the synchronizer, all card images must have their first word in a location whose address ends in 000000.

3. A bit in position 16 specifies interrupt at the initiation of the current card cycle.

4. A bit in position 17 causes feeding of a card. It is used to activate the clutch which allows the feeding of cards and their movement from station to station (see paragraph 52000). The absence of a bit in position 17 will result in no operation of the card punch, since card feeding, punching and check-reading require card movement. However, Stacker Selection may be accomplished for a card check-read on the previous cycle.

5. A "1" in bit position 18 causes translation of Univac III machine code into 80-column card Hollerith code or into 90-column card code. A "0" causes translation and punching in card image mode, (see paragraph 19250 for 80-column and 19252 for 90-column).

6. A bit in position 19 causes selection of Stacker 1. If Stacker 1 is not selected, Stacker 0 is automatically selected.

19320 I/O WORD CHARACTERISTICS (Continued)

8. The following operation codes are acceptable to the Card Punch Unit:

BIT POSITIONS (20 19 18 17 16)		MNEMONIC
0 0 0 0 1	No operation, with Interrupt.	NOP
0 0 0 1 0	Feed card from magazine to wait station #1, move card from wait station #1 to wait station #2, move card from wait station #2 through punching dies to punch station, punching untranslated card image without interrupt; check read card punched during previous card cycle; and place card checked during previous card cycle in normal stacker numbered zero.	All Mnemonic I/O Codes require Interrupt after successful completion, or initiation.
0 0 0 1 1	Same as previous instruction, except at initiation of card cycle set the Initiation Interrupt indicator.	PC
0 1 1 0	Same as previous instruction, except that a translated card is punched without interrupt.	Interrupt required by Mnemonic Code
0 1 1 1	Punch a translated card et cetera, as in the previous instruction; but at initiation of card cycle set the initiation interrupt indicator.	PCT
1 0 0 1 0	Feed card from magazine to wait station #1, move card from wait station #1 to wait station #2, move card from wait station #2 through punching dies to punch station, punching untranslated card image without interrupt, check read card punched during previous card cycle; and place card checked during previous card cycle in selected stacker number 1.	All Mnemonic I/O Codes require Interrupt after successful completion or initiation.
1 0 0 1 1	Same as previous instruction, except at initiation of card cycle set the initiation interrupt indicator.	PCS
1 1 1 1 0	Same as previous instruction, except that a translated card is punched without interrupt.	Interrupt required by Mnemonic Code
1 1 1 1 1	Punch a translated card et cetera, as in the previous instruction; but at initiation of card cycle set the initiation interrupt indicator.	PCTS
1 0 0 0 1	**Select** Stacker 1 only (for card on continuous rollers, after check reading), and interrupt.	CCS
1 0 0 0 0	Select Stacker 1 as in previous instruction, but without interrupt.	All Mnemonic I/O codes require Interrupt after successful completion or initiation.

UNASSIGNED

19330 EXECUTION OF I/O INSTRUCTION WORD

The Operation Code, Bits 16-20, is transferred to the specified synchronizer, and the m-address, Bits 1-15, is transferred to the synchronizer's MAC. The Stacker Bit, 19, selects the stacker to receive the card check-read during the previous card cycle. The Translation Bit, 18, controls whether the card currently at the Wait Station 2 is to be punched in card image mode (see paragraph 19250 and 19252) or in 80-column card Hollerith code or 90-column card code. Detailed effect of each operation code bit is discussed in the preceding paragraph.

Since interrupt will occur by 271^{0} for a data error, 16 ms. are available after a card has been found in error for the instruction in the standby location to be amended by the interrupt program to select stacker #1 for the erroneous card. The synchronizer accesses the amended instruction from the Standby Location, if the Data Error Indicator has been reset by the program by 300^{0} of the card cycle.

19340 AUTOMATIC CARD TRANSLATION

Normally, 80-column cards punched in Hollerith code and 90-column cards punched in Remington Rand 90-column code are automatically translated into UNIVAC III machine code while being transmitted from memory to the Punch. The data to be punched occupy 20 (for 80-column) or 24 (for 90-column) consecutive memory locations. Transfer of data from memory to the Punch synchronizer requires .96 ms. (240 memory cycles) of memory time for the 80-column Punch and .58 ms. (144 memory cycles) of memory time for the 90-column Punch.

19400 HIGH SPEED PRINTER INSTRUCTIONS

19410 EXECUTION OF INITIATE I/O INSTRUCTION

Bits 1-10, modified by the (IR) specified by bits 21-24, specify the memory location of an I/O Instruction Word. Bits 11-14 specify the synchronizer into whose standby location the I/O Instruction Word is to be placed. The contents of $m^{\prime}$ (the I/O Instruction Word) are transferred to the synchronizer's standby location and the associated Standby Location Interlock Indicator is set. When the synchronizer becomes available, it takes the I/O Instruction Word from its standby location for execution; and its Standby Location Interlock Indicator is reset if the instruction is executable.

19420 I/O WORD CHARACTERISTICS

INSTRUCTION

*	No. of Lines of Paper Advance	OPR	MEMORY ADDRESS
0			
25	24 19	18 16	15 1

*Must be Zero.

When the Printer Synchronizer accesses an instruction from its standby location, it first initiates the required feeding of paper. If printing is required, a transfer from memory to the print buffer storage is initiated beginning at the address specified in the I/O Instruction Word and transferring 128 consecutive characters from the next 32 memory words. Therefore, all data editing for printout must be programmed to modify the memory area addressed, prior to programming the initiate input/output instruction.

19430 OPERATION CODES FOR THE HIGH SPEED PRINTER

The principal control of printer operation is determined by bit position 18 of the I/O Instruction Word. A zero in this position will cause the Printer to advance paper without printing. The number of lines of advance is specified by the count in the field composed of bit positions 19 through 24. The instruction may specify from zero to 63 lines of advance whether or not printing is specified. An instruction to both non-print and non-space a line is legitimate; it might be used to test the readiness of the printer.

If bit position 18 contains a "1", then a line will be printed.

Bit position 17 is unassigned and may be either 0 or 1.

Bit position 16 controls program interrupt. If a bit position 16 contains a "1", at the successful completion of the execution of an instruction, the interrupt indicator (Bit 2) will be set.

19500 CONSOLE TYPEWRITER INSTRUCTIONS

19510 The typewriter does not use the Standby Location method of instruction accessing. Therefore, one word instructions are executed to cause typewriter operations.

Contingency Interrupts occur when the printing of a character is completed or when the operator types a character into the buffer register.

19520 WRITE TYPEWRITER CHARACTER

Operation Code: Octal 02, Mnemonic WT

Instruction Format

IA	IR	OPR	CHAR. POS.	m-Address
25	24 21	20 15	14 11	10 1

Typewriter in On-Line Status } Yes: (m') → Typewriter, (CC) + 2 → CC
No: (CC) + 1 → CC

1. The specified 6 bit A/N character of (m') is transferred to the Buffer Register and an operation cycle is initiated to print the character.
2. The character position to be printed is specified by bit positions 11-14 of the instruction as follows:

Character	Bit Positions 14 13 12 11
Most significant	* * 1 1
Most significant - 1	* * 1 0
Most significant - 2	* * 0 1
Most significant - 3	* * 0 0

**These bit positions are not examined by the logic, therefore may be either "0" or "1".

3. Indirect Addressing is allowed.
4. Field Selection and Multi-word Operands are not allowed.
5. If the typewriter is in an off-line condition when the program executes this instruction, the character is not printed and an interrupt indicating the character was printed successfully does not occur.

19530 READ TYPEWRITER CHARACTER

OPERATION CODE: Octal 01, Mnemonic RT

Instruction Format

ZEROS	OPR	AR	ZEROS
25 21	20 15	14 11	10 1

(Typewriter Buffer Register) → (AR_i, Bit Positions 1-6)

1. The 6 bit alphanumeric character in the buffer register enters bit positions 1-6 of the specified AR which must contain binary zeros. The AR is specified by bit positions 11-14 of the instruction word. Positions 7-25 of the AR remain unchanged.

2. Indirect addressing, field selection and multi-word operands are not allowed.

19540 ACTIVATE KEYBOARD

OPERATION CODE: Octal 66, Mnemonic ACT

Instruction Format

ZEROS	OPR	ZEROS
25 21	20 15	14 1

1. The execution of this instruction turns on the Keyboard Active Indicator light on the console and permits the operator to type one character into the buffer register (the indicator light is turned off when the character is typed in).

2. Indirect addressing, field selection and multi-word operands are not allowed.

19550 → DISPLAY

Operation Code: Octal 03, Mnemonic DIS

(m') → Display

This instruction is primarily for the maintenance Engineer. It causes the display of the contents of m', in bit form (27 bits), on the maintenance panel. The display switch on the panel must be set to position zero.

1. Indirect addressing is allowed.

2. Field selection and multiword operands are not allowed.

19600 UNISERVO IIA TAPE UNIT SYNCHRONIZER INSTRUCTIONS

This facility is provided to allow the UNIVAC III System to communicate with the UNIVAC I, UNIVAC II and USSC-T Systems through the storage medium of magnetic tape.

19605 I/O INSTRUCTION WORD FORMAT

	SERVO NO.	OPR	m-ADDRESS
25	24 21	20 16	15 1

19610 FORWARD READ NORMAL GAIN

This instruction initiates forward reading of tape at densities from 50 PPI to 250 PPI with Normal amplifier gain. Information blocks can consist of:

1. A single 720 character block.
2. Six 120 character blockettes.

19620 FORWARD READ HIGH GAIN

This instruction operates in the same manner as 19610 except that it specifies High amplifier gain.

19630 FORWARD READ LOW GAIN

This instruction operates in the same manner as 19610 except that it specifies Low amplifier gain.

19640 BACKWARD READ NORMAL GAIN

This instruction initiates backward reading of tape at densities from 50 PPI to 250 PPI with Normal amplifier gain. Information blocks can consist of:

1. A single 720 character block.
2. Six 120 character blockettes.

19650 BACKWARD READ HIGH GAIN

This instruction operates in the same manner as 19640 except that it specifies High amplifier gain.

19660 BACKWARD READ LOW GAIN

This instruction operates in the same manner as 19640 except that it specifies Low amplifier gain.

19670 WRITE TAPE

This instruction initiates writing on tape at a density of 250 PPI. Information blocks consist of 720 characters.

19680 WRITE TAPE SUB-DIVIDED

This instruction initiates writing on tape at a density of 125 PPI with information blocks of 720 characters sub-divided into six 120-character blockettes. Subdivided tape is not written at higher densities.

19690 REWIND

This instruction initiates the rewinding of a tape reel. At the completion of the rewinding operation, the tape is positioned at the tape load point and is available for use by the program.

19695 REWIND WITH INTERLOCK

This instruction initiates the rewinding of a tape reel. At the completion of the rewinding operation, the tape is positioned at the reel change position and cannot be used by the program without operator intervention.

19697 OPERATION CODES

1. The following Operation Codes are specified for the UNISERVO IIA Tape Unit in the UNIVAC III System.

Bit Positions 17 18 19 20	
0 0 0 0	Forward Read One Block Normal Gain
0 0 0 1	Forward Read One Block High Gain
0 0 1 0	Forward Read One Block Low Gain
0 1 0 0	Backward Read One Block Normal Gain
0 1 0 1	Backward Read One Block High Gain
0 1 1 0	Backward Read One Block Low Gain
1 0 0 0	Write 250 PPI tape in Block Mode.
1 0 1 0	Write UNIVAC Tape 125 PPI sub-divided.
1 1 0 0	Rewind
1 1 0 1	Rewind with interlock.

19699 INSTRUCTION EXECUTION

1. Instruction execution takes the following steps:

   a. An Input/Output instruction is loaded into the Memory Standby Location associated with the UNISERVO IIA Tape Unit Synchronizer by the execution of an Initiate Input/Output Instruction. At the time the Standby Location is loaded, the Synchronizer Standby Location Interlock Indicator is set.
   b. When the Synchronizer successfully completes the execution of an instruction, it requests a memory access to its Standby Location if its Standby Location Interlock Indicator is set. When the Memory Priority circuits grant the Synchronizer the requested access, the contents of the Standby Location are transferred to the Synchronizer where the operation code and UNISERVO Tape Unit address are stored in static form. During the transfer, the Memory Address field is loaded into the Synchronizer MAC.

19699 INSTRUCTION EXECUTION (Continued)

c. If the Synchronizer has just completed the execution of an instruction, that instruction is compared with the new instruction in the synchronizer instruction register. If the new instruction agrees in type and direction with the previous one, it is accepted for execution by the Synchronizer without stopping the tape. If not, execution of the new instruction is delayed until the UNISERVO tape unit, currently in motion, is stopped and released from the Synchronizer. The Standby Location Interlock Indicator is reset at the time the instruction execution begins and not when it is transferred from the Standby Location to the Synchronizer.

d. If the UNISERVO Tape Unit is not available, the Synchronizer rejects the instruction, sets its associated Fault Indicator and its Standby Location Interlock Indicator remains set. Interrupt will occur simultaneously with the setting of the Fault Indicator. The Synchronizer is then effectively stalled until its Fault Indicator is reset by programming. Following the execution of the instruction resetting the Fault Indicator, the Synchronizer will call for the contents of its Standby Location. Therefore, program modification of an instruction in the Standby Location must occur before the Fault Indicator is reset.

e. If the Synchronizer accepts an instruction but fails to complete it successfully due to an error (parity or 720 error), the associated Error Indicator will be set at the time when the Synchronizer would become available due to successful completion of the instruction. The Synchronizer then effectively stalls until the Error Indicator is reset by programming.

2. The selection of a UNISERVO Tape Unit is specified by bit positions 21-24 of the Input/Output instruction word; they are numbered 0 to 5.
3. When a Backward Read instruction is given, the m-address of the instruction must specify the last word of the input area in memory rather than the first word.
4. The amplifier gain may be selected by the program each time a read instruction is given.
5. A "1" in bit position 16 of the Input/Output instruction causes an automatic Input/Output Program Interrupt at the successful completion of the execution of the instruction. See "7" below for second successful completion.
6. Reading and writing on UNIVAC tape terminates with the transfer of the 720th character.
7. If the Program has not reset the successful completion interrupt indicator set as in "5" above when a second successful completion calls for setting that indicator again, the current interrupt will not occur nor will the Synchronizer access another instruction until the previous one has been recognized and the interrupt indicator has been reset.

20000 INDEXING INSTRUCTIONS

The following instructions provide for the loading, unloading, incrementing and testing of the contents of Index Registers. The specification of a non-existent IR has the following results. Unloading Index Register 0 (a "Legitimate" Non-Existent Register) will place binary zeros in all bit positions of the word in memory. If an attempt to Increment and Compare Index Register 0 is made, incrementing does not occur and for the comparison the contents of the register are considered to be binary zeros (15 bits). Other non-existent index registers (10-15 when not included in the hardware) produce 1's in bit positions 1-16 of the word in memory when unloaded (bit positions 17-25 are cleared to binary zeros). For the Increment and Compare instruction these index registers operate in the same manner as IR 0 except their contents are considered to be 1's (15 bits) for the comparison. For loading and incrementing Index Registers 0 or 10-15 (when not included in the hardware), nothing happens since the register doesn't actually exist.

The word formats involved are the following:

Instruction Word for Manipulation of Index Registers:

IA	IR	OPR	IR'	m-ADDRESS
25	24 21	20 15	14 11	10 1

Index Register Increment and Compare Word:

S	COMPARISON AMOUNT	INCREMENT AMOUNT
25	24 10	9 1

20100 LOAD INDEX REGISTER

OPERATION CODES: Octal 51, Mnemonic LX

This instruction replaces the contents of the Index Register specified by bits 11-14 with the low-order 15 bits of the memory location indicated by m'.

1. m address + (IR) = m'
2. (m') → IR'
3. The instruction allows indirect addressing but field selection is not permitted.

20110 INDEX REGISTER INCREMENT AND COMPARE

OPERATION CODES: Octal 53, Mnemonic ICX

The instruction uses an Index Register Increment and Compare Word, which is located at the indexed m address. The contents of bits 1-9 of the Increment and Compare Word are added to the Index Register specified by IR'. The least significant 15 bits of the result in the Index Register are compared with the contents of the Comparison Field in the Increment and Compare Word, and the appropriate comparison indicator is set.

1. m + (IR) = m'
2. $(m')_{1-9}$ + (IR') → (IR')
3. (IR') LS 15 bits : $(m')_{10-24}$. If the least significant 15 bits of the contents of the Index Register are greater than that of the Comparison Field of the Increment and Compare Word, the High Indicator is set; if they are equal, the Equal Indicator is set; if the contents of the Register is less than that of the Comparison Field, the Low Indicator is set.
4. If the sign bit of the Increment and Control Word (bit position 25) is 1, the increment amount is taken as negative and the instruction actually performs a decrementation.
5. Indirect Addressing is Permissible; field selection is not.

20120 INCREMENT INDEX REGISTER

OPERATION CODES: Octal 52, Mnemonic IX

This instruction operates in the same manner as Index Register Increment and Compare, except that the comparison is not performed and indicators are not set. Thus all comments given in paragraph 20110 apply except 3., which relates to the comparison operation.

20130 UNLOAD INDEX REGISTER

OPERATION CODES: Octal 50, Mnemonic STX

Place the contents of the specified Index Register in a designated memory location. The remainder of the memory location is replaced with binary zero.

1. $(IR') \rightarrow m'_{1-16}$; binary zeros $\rightarrow m'_{17-25}$

2. The instruction allows indirect addressing, but field selection is not permitted.

21000 MISCELLANEOUS INSTRUCTIONS

21100 NO OPERATION

OPERATION CODES: Octal 00, Mnemonic NOP.

This instruction performs no action. The next instruction in sequence is performed after the "execution time" for the No-Op elapses.

21200 STOP AND TRANSFER

OPERATION CODES: Octal 77, Mnemonic WAIT

The Central Processor is stopped and the indexed m-address of the instruction is placed in the control counter. When the Start Key is depressed on the console, the program continues with the next instruction as addressed in the control counter.

1. The Central Processor ceases to call for memory. All peripheral operations in progress (those for which instructions have already been given) continue to orderly completion, $(m') \rightarrow CC$.

2. When the Start Key is depressed, the program continues, with the Control Counter as modified.

3. Indirect Addressing is permitted; field selection is not allowed.

21300 WRITE CONTENTS OF MEMORY ADDRESS COUNTER TO MEMORY AND TRANSFER

OPERATION CODES: Octal 07, Mnemonic TR

Transfer the contents of the Memory Address Counter, incremented by 1, into the low-order sixteen bit positions of m' (bit position 16 is always zero), and replace the high order bit positions (17-25) of m' with binary zeros. Then transfer control to the instruction in location m' + 1.

1. $(MAC) + 1 \rightarrow m'_{1-16}$; the other positions of m' become binary zeros.

2. $m' + 1 \rightarrow CC$.

3. The instruction allows indirect addressing but field selection is not permitted.

4. The AR bits specify the address of the synchronizer containing the specified memory address counter (See Paragraph 11902 D, F and G). The Control Counter contents plus one will be stored if 0001 is placed in the AR bit positions of this instruction or the Memory Address Register contents will be stored in m' if 0010 is specified.

21400 WRITE SYNCHRONIZER MEMORY ADDRESS COUNTER TO MEMORY

OPERATION CODES: Octal 04, Mnemonic STMC

(MAC) → m' Bit Positions 1-16

The contents of the Memory Address Counter (MAC), for the synchronizer specified in bit positions 11-14, are transferred to the low order 16 bit positions of m' (bit position 16 is always zero) and the remaining bit positions of m' are replaced by binary zeros.

1. For Uniservo III synchronizers, when reading or writing with control words, the contents of MAC is the address of the Tape Control Word currently effective in the synchronizer, and it does not reveal the location in memory to or from which data transfers are made. (See the following instruction).

2. For the Uniservo II synchronizer, General Purpose Channels and for Uniservo III reading without control words, on the other hand, the contents of MAC is the memory address from or to which the last data word transfer took place.

3. Indirect Addressing is permissible. Field Selection is not permissible.

4. Bit Positions 11-14 specify the Control Counter (0001), Memory Address Register (0010) or a Synchronizer Memory Address Counter (0011-1111).

If the MAR (0010) is specified, the address of the receiving memory location will be stored in that location since the (MAR), at the time it is stored, is actually the address of the memory location into which it is to be stored. The use of STMC in this manner is to be avoided.

21450 WRITE CONTENTS OF UNISERVO III SYNCHRONIZER TAPE CONTROL WORD REGISTER TO MEMORY

OPERATION CODES: Octal 05, Mnemonic STCR

(TCWR) → m'

The contents of the Uniservo III Synchronizer Tape Control Word Register, for the synchronizer specified in bit positions 11-14, is transferred to the location in memory specified by m'. The memory location will then contain, in positions 1-15, the address in memory of the last word transferred to or from the synchronizer, and in positions 16-24, the count contained in the Tape Control Word which effected the tape operation, decremented by one for each transfer which has taken place.

The instruction allows indirect addressing, but field selection is not permissible.

31000 UNISERVO III/IIIA TAPE UNITS

The information in Sections 31000 through 31999 applies to both the UNISERVO III and IIIA Tape Units unless otherwise noted.

The Minimal Marketable UNIVAC III System includes one UNISERVO III/IIIA Tape Unit Synchronizer pair, which can effectively employ from one to sixteen tape handling units. The Maximum System includes another UNISERVO III/IIIA Tape Unit Synchronizer pair, which can effectively employ an additional one to sixteen more tape handling units. Each power supply can effectively serve sixteen UNISERVO Tape Units. (See 01000.)

Each synchronizer pair consists of a write synchronizer which provides for recording on magnetic tape and also check-reads what it has written for the modulo 3 check, and a read synchronizer to transfer data from magnetic tape to memory. Each UNISERVO III/IIIA Tape Unit may read data from tape moving either forward or backward, write on tape moving forward, and rewind its tape. Since read and write synchronizers function independently of each other, it is normal for the write synchronizer to be recording on tape in one tape-handling mechanism, while its companion read synchronizer is simultaneously reading from tape on another tape-handling mechanism and transferring the data read to the Computer Memory. See paragraph 19000.

Each tape-handling mechanism is constructed to mount a 3,500 foot reel of MYLAR* base magnetic tape 0.5 inches wide and 1.0 mill thick. Rewind speed is 150 inches per second. Tape handling units may be redesignated from one unit number to another, without physically moving the cabinets, by changing connections on a control panel.

UNISERVO III/IIIA Tape Unit writes on this tape with a density of 1,027.5 frames of recorded data per inch. Each frame contains 9 bit positions, so that every three frames contain one UNIVAC III word of 27 bit positions, including sign and parity. (See paragraphs 11200-11220 for use of bit positions 26 and 27. See paragraph 11800 for word formats for bit positions 1 through 25.)

The 9 channel tape moves beneath a read-write head at 100 inches per second, resulting in 102,750 frames per second being transferred between the central processor and the magnetic tape. Since each UNIVAC III word of 3 frames contains four alpha-numeric characters when data is alphanumeric, this instantaneous transfer rate provides for the transfer of data between computer and tape written in this mode, of 137,000 alpha-numeric characters per second. When the words are written in decimal digit mode of 6 digits per word, 205,500 digits are transferred per second. Words are grouped in variable length blocks according to the specifications of the read-write tape control words.(see 11700 and 11813.)

The blocks are separated by inter-block gaps which allow the reel of tape to come up to transfer speed or to come to a stop from transfer speed in start/stop mode, as well as to break transferring in continuous mode. The inter-block gap size is determined in continuous mode by the distance between the read head and the write head (1/4 inches), as check reading of the previous block must be completed prior to the start of writing of the next block to provide for an error interrupt if the check reading discloses a write error, plus sufficient additional gap so that when the written tape is read again in subsequent processing, the tape mechanism can be brought up to transfer speed

(Continued on Next Page)

*MYLAR = A registered trademark of E. I. duPont deNemours Co., Inc.

31000 UNISERVO III/[redacted] (Continued)

between the end of one block and the beginning of another. In start/stop mode, the gap size is determined by the amount of tape that will pass while the tape handler is coming to a full stop, and the additional amount of tape that will pass before the Uniservo is brought up to transfer speed. Times for interrecord gaps, as well as distances, are listed in paragraph 31500.

Tape error malfunctions such as those resulting from coating defects are controlled by marking the bad spot on the tape with a bad spot pattern. See paragraphs 11353 for other error procedures.

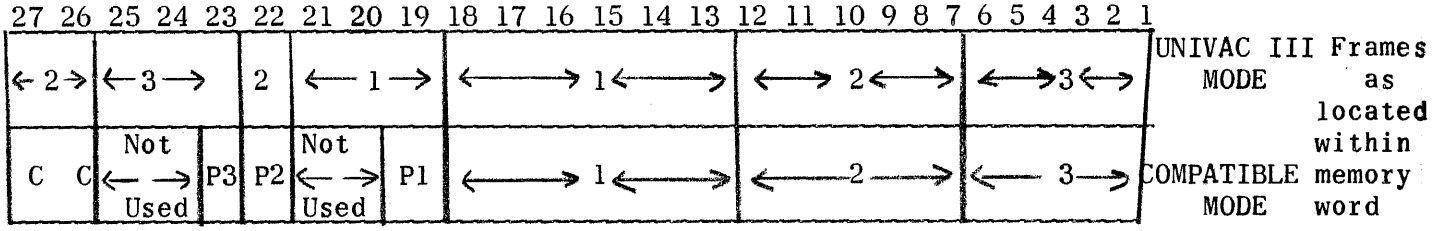
For bit positions effecting the operation code for UNISERVO III/III-A, see paragraph 19051. For the structure of the controlling instructions governing UNISERVO III/III-A see paragraphs 11812 and 11814. When an initiate input-output order is reached in the program, the designated synchronizer standby location receives the input-output instruction from the memory location addressed in the initiating order. As soon as the synchronizer becomes available, the instruction is moved from the standby location to the synchronizer itself and execution begins. The instruction gives the address of the first tape control word, and the subsequent sequential tape control words in turn govern the continued tape reading or writing, as described in paragraphs 11700-11720. In addition to the synchronizer's standby location there is provided a standby location interlock indicator which is automatically set whenever an input-output instruction is placed in its associated standby location. When the synchronizer completes the execution of the instruction in process, it interrogates this indicator. If it finds it set, it transfers the instruction from the standby location to the synchronizer for execution and resets the standby location indicator when the instruction has been successfully accessed from memory and is executable by the synchronizer. See paragraph 19000.

The synchronizer is tied up from 182 or 357 microseconds while initiating a rewind without interlock operation. After initiation, the synchronizer is free to continue operations on other Uniservos. However, if rewind with lockout is specified (requiring the operator to intervene before use of that Uniservo again after rewind is completed), the synchronizer is tied up for approximately 10 milliseconds. If the rewind instruction is accessed while both write and read synchronizers of the pair are available, both synchronizers of the pair are tied up for the specified time, regardless of which synchronizer is controlling rewind.

31000 UNISERVO III (Cont'd)

FLOW OF DATA BETWEEN CENTRAL PROCESSOR AND SYNCHRONIZER AND BETWEEN SYNCHRONIZER AND UNISERVO III TAPE

SYNCHRONIZER MEMORY



FROM AND TO TAPE FRAME DIGIT POSITIONS BELOW

TO MEMORY WORD DIGITS ABOVE

TAPE ⟷ SYNCHRONIZER

Channel -	1	2	3	4	5	6	7	8	9	
	13	15	17	21	19	20	14	16	18	FRAME 1
	7	9	11	27	22	26	8	10	12	FRAME 2
	1	3	5	25	23	24	2	4	6	FRAME 3

NOTE:

1. The End of Tape Warning window is placed about 25 feet from the end of the oxide-coated tape. This provides a sufficient amount of tape for bringing tape operations on a UNISERVO to an orderly halt before switching to another UNISERVO or mounting another another tape and continuing on the same UNISERVO.

2. Channel #1 is nearest the base plate.

3. In the compatible mode, bits #23, 22, 19 are parity bits. Channel 4 and 6 must be binary zeros. The three alphabetic characters (bits 18 - 1) are read out starting with the most significant character. In reading out in the compatible mode, bits #19 through 27 will be ignored and may be filled with hash. When reading compatible mode tape, parity bits will be transferred to memory in addition to being checked by the synchronizer. See Product Specification, P-20014, UNISERVO IIIA Compatible Mode for details.

4. A switch on the UNISERVO enables the operator to control whether the UNISERVO will make transfers in the regular UNIVAC III Mode or in the Compatible Mode, as charted above.

5. In the Compatible Mode all blocks must be written from consecutive memory locations, thus eliminating the recording of segment separators on tape. All reading must be accomplished by block read instructions; scatter reading is not permitted. By programming convention, blocks must be multiples of 40 words up to a maximum of 480 words (See Product Specification P-20014). Blocks must be written in start-stop mode, i.e., tape movement must stop and start between blocks. This is a programming convention which must be adhered to in order to permit successful reading of UNIVAC III tapes on the U1107 and U490.

31001 DETAILED DIAGRAM OF MEMORY ↔ TAPE DATA FLOW IN UNISERVO III COMPATIBLE MODE (UNIVAC III, UNIVAC 490, UNIVAC 1107) AS CONSOLIDATED ON PRECEDING 3rd PAGE OF SECTION 31000. P1, P2 and P3 are "even" parity bits for characters occupying same numbered frame.

MEMORY TO TAPE

MEMORY DIGIT POSITIONS

IGNORED	TAPE FRAME NUMBER 1	TAPE FRAME NUMBER 2	TAPE FRAME NUMBER 3
27 19	18 13	12 7	6 1

FRAME DIGIT POSITIONS

NUMBERS IN FRAME DIGIT POSITIONS STATE CORRESPONDING MEMORY WORD DIGIT POSITION										TAPE FRAMES
	13	15	17	21 0	19 P1	20 0	14	16	18	1
	7	9	11	27 0	22 P2	26 0	8	10	12	2
	1	3	5	25 0	23 P3	24 0	2	4	6	3

SUPPLIED AUTOMATICALLY BY SYNCHRONIZER

TAPE TO MEMORY

CHECKED BY SYNCHRONIZER, MUST BE PRESENT TO AVOID ERROR. TRANSFERRED TO MEMORY*

FRAME DIGIT POSITIONS

NUMBERS IN FRAME DIGIT POSITIONS STATE CORRESPONDING MEMORY WORD DIGIT POSITION										TAPE FRAMES
	13	15	17	21 0	19 P1	20 0	14	16	18	1
	7	9	11	27 0	22 P2	26 0	8	10	12	2
	1	3	5	25 0	23 P3	24 0	2	4	6	3

*X-3 Mod Parity Supplied Automatically before Arrival in Memory.

MEMORY DIGIT POSITIONS

C C	0 0	P3	P2	0 0	P1	TAPE FRAME NUMBER 1	TAPE FRAME NUMBER 2	TAPE FRAME NUMBER 3
27,26	25,24	23	22	21,20	19	18 13	12 7	6 1

31050 TAPE READ ON WRITE SYNCHRONIZER

This feature is standard at no additional cost in all UNIVAC III Systems requiring a UNISERVO III/IIIA Read-Write Synchronizer. The Write Synchronizer will accept and execute read orders in all respects as if it were a Read Synchronizer, including the execution of all UNISERVO III or IIIA Tape Unit Reader Synchronizer interrupts.

31100 UNISERVO III/IIIA TAPE UNITS - SUMMARY OF SPECIFICATIONS

Recording Density	1,027.5 frames per inch
Tape Speed	100 inches per second
Instantaneous Transfer Rates	102,750 - 9 bit frames per second 3 frames = one 27-bit word 137,000 A/N characters per second 205,500 Decimal Digits per second
Data Channels	9 (for the 9 bit frames)
Interblock gap	Nominal Nonstop Gap .4257" Nominal Start Stop Gap .6247"
Head gap	Erased Head to Write Head 1 13/16" (nominal) Write-Read Head (9 channels) Adjacent gaps are .25 inches apart
Block length	Variable in multiples of 3 frames
Check during writing	Post-write Mod 3 check
Check during reading	Residue Modulo 3 check
Bad Spot Detection	Pattern Overwrite and Program-Controlled rewrite
Load point delay	70 milliseconds
Reversal time	600 milliseconds
Rewind Speed	Tape Length / UNISERVO III / UNISERVO IIIA 625' / 50 secs. / 35 secs. 1700' / 136 secs. / 70 secs. 3500' / 280 secs. / 125 secs.
Tape	MYLAR* 0.5 inches x 625, 1700 or 3500 feet
Reel Hub	Compatible with IBM 727 and 729
Load Point Window	A clear area of tape, 1 1/8" x 1/8", located 30' from the beginning of the tape. It is used to position tape for the first block position.
End of Tape Warning Window	A clear area of tape, 1 1/8" x 1/8", located 25' from the end of the coated area of tape. It is used to signal the program that the end of tape is approaching.

NOTE: Detailed UNISERVO IIIA Tape Unit Specifications can be found in Product Specification P20008.

31200 SYSTEM CONFIGURATIONS

See paragraph 01000, Systems Configurations.
The UNISERVO III and IIIA Tape Units may be intermixed in a UNISERVO Tape Unit Lineup. They are arranged in a line as is conventional with other UNIVAC Systems. The line can have a 90^{0} bend. Wiring is channelled along the top by a trellis. As many as 16 tape handling UNISERVO tape units can be placed in one line.

Each line is associated with one UNISERVO Power Supply unit, which is connected to the trellis at one end of the UNISERVO tape unit line. It supplies power to the tape handling units only, and not to the synchronizers. The line is connected by the trellis to the Central Processor, which contains the associated read and write synchronizers and motion controls. Power requirements, heat dissipation, dimensions, and floor loading are stated in the installation section, paragraph 90000.

31300 MANUAL TAPE READ AND MANUAL REWIND

Two switches are provided on the Central Processor Operator's Console to allow manual tape read (Load button) and manual tape rewind (Rewind button). See paragraph 70220 for a description of these two buttons. The Central Processor "stop" indicator must be set for the switch to be effective. If either the Central Processor or the Synchronizer is in a "run" condition when the switches are actuated, the specified operation will be ignored. For the read instruction, the core starting address is determined by the memory address counter of the read synchronizer (MAC) prior to switch actuation. (Master Machine Clear clears MAC to binary zero). *MYLAR - A registered Trademark of E.I.DuPont deNemours Co., Inc.

31400 UNISERVO III/IIIA CONTROL PANEL

UNISERVO Tape Unit Numeral Block	Located at the left side of the UNISERVO Tape Unit Control Panel. The removable block (numbered 0-15) should be interchanged among UNISERVO Units to conform to its logical address established in the UNISERVO Tape Unit Selector Plugboard. When the power to the UNISERVO Unit is on, but the unit is not in an operating condition, the numeral is red. The numeral is white when the UNISERVO Unit is on and in an operating condition.
Air Flow	Will light when there is insufficient air flow in the blower system. Power to the UNISERVO Unit will be turned off.
Overheat	Will light when an overheat condition exists in the UNISERVO Unit. Power to the UNISERVO Unit will be turned off.
Voltage	Will light when any normal current requirement is exceeded. Power to the UNISERVO Unit will be turned off.
Forward	A button-light, will be lit when the UNISERVO Unit is set in a forward condition either manually, by depressing the button, or by Program Control. The button is used mainly for maintenance purposes.
Backward	A button-light, will be lit when the UNISERVO Unit is set in a backward condition either manually, by depressing the button, or by program control. The button is used mainly for maintenance purposes.
Rewind	A button-light, will be lit while the UNISERVO Unit is rewinding. When depressed, it will rewind the tape with interlock. For the UNISERVO III Tape Unit only, the Backward button-light must be depressed first.
Change Tape	A button-light, will be lit when the UNISERVO Unit is rewinding with interlock and remain on after it has been completed. The light is extinguished, (the interlock removed) when the button is depressed. Depression will also cause a tape that has been rewound with interlock to be positioned at its load point.
Load Point	When lit indicates that the tape is at its Load Point. It will be extinguished when the first operation on the UNISERVO Unit is initiated.
Inhibit Write	Will be lit when a reel not containing a ring is mounted on the UNISERVO Unit.
On	A button-light, will be lit when the button is depressed supplying power to the UNISERVO Unit. It will be extinguished when the Off button is depressed or power to the UNISERVO Unit is turned off.

31400 UNISERVO III CONTROL PANEL (Continued)

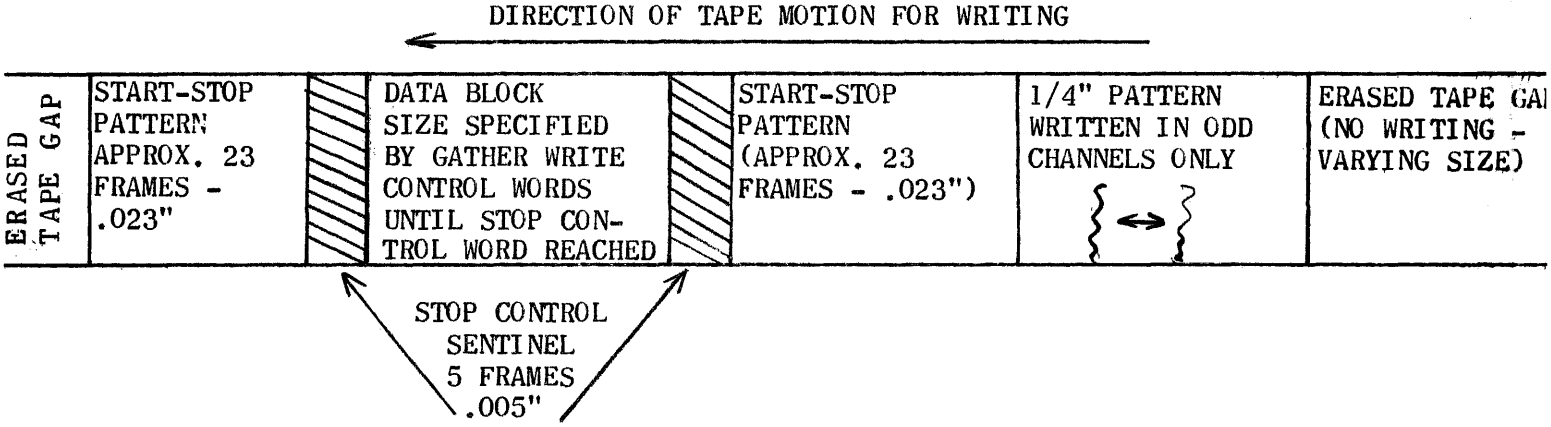
Off	A button-light, will be lit when the button is depressed removing power from the Uniservo Unit. It will be extinguished when the ON button is depressed.
Uniservo Selector Plugboard	A plugboard, located in the Intermediate Cabinet A, has been provided to allow the assignment of a logical or computer address to any physical Uniservo Unit in its bank. The removable Uniservo Numeral Block on the Uniservo Control Panel should be made to agree with the logical address assigned to it.

31412 UNISERVO III SYNCHRONIZER BAD SPOT CONTROL

The method of handling magnetically defective areas of tape for the UNIVAC III utilizes writing only in EVEN channels on tape, which is subsequently recognized on read as a bad spot pattern. The withholding of writing of data or pattern in the odd numbered channels by the write head continues for the quarter inch necessary for the read head to recognize the absence of writing in the odd channels in the presence of writing in the even numbered channels.

In the following discussion of the operation of the method for the various modes of tape writing and reading, certain conventions are used, as follows:

1. NORMAL BLOCK CONFIGURATION:



For the purpose of this paragraph the START Pattern will always mean the Pattern written BEFORE the data on a FORWARD write, regardless of whether a forward read or a BACKWARD read is being discussed. This will also be true for the START Sentinel, the STOP Sentinel, and the STOP Pattern.

2. The term "Read Head" is used whether that head is being used for reading or for checking of writing.

Methods of Operation are:

On error-free normal write the sequence is Start Pattern, Start Sentinel including Stop Control Word (for backward reading), Data Block, Stop Control Word (for forward reading) included in Stop Sentinel, Stop Pattern, FOLLOWED BY PATTERN WRITTEN IN ODD CHANNELS ONLY until the read head detects the Stop Sentinel.

When the read head detects an error, either before or after the writing of the sentinel, writing is discontinued in all EVEN channels and continued in all ODD channels as pattern for the quarter inch necessary for the condition of ODD-channels only to be detected by the read head. The ODD-only pattern is then followed by one quarter inch of non-data writing in ALL channels. The writing in ALL channels is finally followed by one quarter inch of writing in EVEN channels ONLY. When writing in EVEN channels only is detected by the read head, writing is stopped but reading continues until the erased tape gap is detected one quarter inch later. The synchronizer is then released and a write ERROR A interrupt is issued. The tape is then stopped as the ERROR A interrupt is issued. The sentinel will have been written ONLY if the entire block had been completely written prior to the write-check error detection.

31412 UNISERVO III SYNCHRONIZER BAD SPOT CONTROL (Continued)

The foregoing bad spot pattern is recognized on REVERSE READ as being at the REVERSE BEGINNING (END) of the block, causing the "SKIP" flip-flop to be set in the synchronizer. The synchronizer will continue to pass tape in the reverse direction, without transferring any data to memory, until an absence of data IN ALL CHANNELS is encountered.

The absence of data (erased tape gap) in all channels resets the "SKIP" flip-flop, allowing the next block in the reverse direction to be read without an additional command. In this manner, all blocks marked by bad spot pattern will automatically be bypassed on reverse read orders.

On forward read, the synchronizer expects to find an erased tape gap, with absence of data in all channels, at the beginning. If, instead, it finds writing in the EVEN channels ONLY, it has reached the bad spot pattern written at the end of the previous block, after the sentinel had been written. This is true because the reading of the previous block had ended, and the motion controls to stop tape travel had been initiated, upon detection of the sentinel at the end of the block. But this can only be true where the previous block was successfully read into memory, notwithstanding the fact that it failed to pass the write check when written. Since at the time of writing, the Error A interrupt resulted (by programming) in rewriting the block over again after writing the bad spot pattern (pattern in EVEN channels only), the next block on tape is a duplicate of the block which has just been successfully read. This can happen because the write check is purposefully less tolerant than reading. So if the synchronizer on forward read finds writing only in the EVEN channels, it sets the "SKIP" flip-flop. Then when the following block is recognized the synchronizer continues skipping through the block, past the sentinel, to the next interblock gap, resetting the "SKIP" flip-flop after skipping the block. Thus a number of such consecutive bad spot blocks can be skipped. Reading will commence with the block following.

During a forward block read (without Control word) if a data error occurs, the synchronizer prevents further data transfers and searches for the erased tape gap. If bad spot pattern (writing in EVEN channels only) is encountered prior to the erased tape gap, (whether reading forward with Control word or without Control word) the Error A interrupt occurs when the gap is reached and the tape is stopped. But if no bad spot pattern has been encountered by that time, Error B interrupt occurs.

See Sections 11353 A. III. g., and 19150.

31500 - UNISERVO III/IIIA INTERBLOCK GAP SIZES AND TIMES

The table below provides interblock information about the various operation combinations. The following definitions are applicable:

Gap Type - An NS (non-stop) gap is an interblock gap created by a non-stop write operation. An SS (start-stop) Gap is an interblock gap created by a start-stop write operation.

Mode of Operation - The NS (non-stop)mode of operation is where tape between two data blocks on the same UNISERVO is passed at a nominal 100 ips. The SS (start-stop) mode is where tape is stopped and then started between two operations on the same or different UNISERVOS.

Interblock Gap Size - This is the amount of tape/inches between the last data frame of one block and the first data frame of the next block.

Interblock Gap Time - This is the time to pass the tape defined as the interblock gap.

	LAST OPERATION	GAP TYPE	NEXT OPERATION	GAP TYPE	MODE OF OPERATION	NOMINAL INTERBLOCK GAP SIZE (")	NOMINAL INTERBLOCK GAP TIME (ms)
				WRITE SYNC. - SAME UNISERVO			
1.	Write	NS	Write	----	NS	.4257	4.257
2.	Write	SS	Write	----	SS	.6247	13.208
				READ OR WRITE SYNC. - SAME UNISERVO			
3.	Read	NS	Read	----	NS	.4257	4.257
4.	Read	SS	Read	----	NS	.6247	6.247
5.	Read	NS	Read	----	SS	.4257	11.257
6.	Read	SS	Read	----	SS	.6247	13.208
				WRITE SYNC. - DIFFERENT UNISERVOS			
7.	Write	SS	Write	SS	SS	.6247	6.390
8.	Read	NS/SS	Read	NS	SS	.4257	4.439
9.	Read	NS/SS	Read	SS	SS	.6247	6.390
10.	Read	NS/SS	Write	SS	SS	.6247	3.890
11.	Write	SS	Read	NS	SS	.4257	6.939
12.	Write	SS	Read	SS	SS	.6247	8.929
				READ SYNC. - DIFFERENT UNISERVOS			
13.	Read	NS/SS	Read	NS	SS	.4257	4.439
14.	Read	NS/SS	Read	SS	SS	.6247	6.390

32000 UNISERVO IIA TAPE UNIT IN THE UNIVAC III SYSTEM

32100 SYSTEM CONFIGURATIONS

1. The UNIVAC III System can include one UNISERVO IIA Synchronizer to which may be connected a maximum of six UNISERVO IIA Tape Units.

2. The UNISERVO IIA tape units can use the same power supply as a UNISERVO III and IIIA tape units. However, a power supply can only accommodate a total of 16 UNISERVO Tape Units.

32200 SUMMARY OF SPECIFICATIONS

32210 UNISERVO IIA SYNCHRONIZER

UNISERVO Tape Unit Assignment	A plugboard is provided to allow for assignment of UNISERVO tape units to the synchronizer.
Code Translation	Accomplished by programming.
Parity	The Synchronizer will convert word parity to character parity when writing and character parity to word parity when reading.
UNISERVO Tape Unit Selection	The Synchronizer can select one of six UNISERVO Tape Units for a read or write operation.
Rewinds	Any number of rewinds may proceed simultaneously once they are initiated by the Synchronizer.
Write Check	Not automatic. Checking of written tape must be programmed.
Synchronizer MAC	The MAC is incremented when the synchronizer has 4 characters (1 UNIVAC III word) to be transferred to memory. It continues to be incremented until an inter-block gap stops the tape. Incrementing does not commence until the second word is transmitted. After 720 characters are transmitted (180 words), further transmission is inhibited even though the MAC continues to be incremented. Each group of 4 characters must be accumulated before the UNIVAC III word is transferred to or from memory.

32220 UNISERVO II (UNIVAC TAPE)

Uniservo	Model 72
Method of Recording	Return to Zero
Data Channels	Univac XS-3 characters are recorded on tape in six data channels plus a seventh for an ODD parity bit. An eighth channel carries the sprocket bits.
Tape Speed	100 inches per second for reading, writing or rewinding.
Type of Tape	Mylar or Metallic - A switch is provided on the Uniservo to select the type desired.
Write Densities	Univac tape is written at densities of 125 PPI or 250 PPI as specified by the operation code of the write instruction. When information is written at 250 PPI, 720 characters are recorded in one block. When written at 125 PPI, 720 characters are recorded in six blockettes of 120 characters each.
Read Densities	Univac tape can be read at from 50 to 250 PPI.
Write Interlock	Writing on tape is prevented if the tape reel, mounted on the Uniservo, carries a protective ring.
Gap Sizes	Univac tape written at 250 PPI has a space of 1.05 inches between each block of 720 characters. When written at 125 PPI, it has a space of 1.05 inches between each blockette and 2.4 inches between each block of six blockettes.

32230 UNISERVO II (IBM 727 TAPE)

Uniservo	Modified Model 72
Method of Recording	Non Return to Zero
Data Channels	IBM 727 Tape binary-coded decimal characters are recorded on tape in six data channels, plus a seventh for an EVEN parity bit.
Tape Speed	100 inches per second for reading, writing or rewinding.
Type of Tape	Mylar on IBM type reels.
Density	IBM 727 Tape is written and read at 200 PPI.
Write Interlock	Writing on tape is prevented if the tape reel, mounted on the Uniservo, carries a protective ring.
Gap Sizes	IBM 727 tape has a space of .02 inches between the last frame of the information block and the longitudinal check frame, and one of 1.05 inches between the check frame and the beginning of the next block if the tape was written on Uniservo II. If the tape was written on an IBM 727 Tape Unit, there is a space of .02 inches between the longitudinal check frame and the last frame of the information block, and one of .75 inches between the check frame and the beginning of the next block. IBM 727 tape written on Uniservo II has a space 1.05 inches between the check character of the last block and the tape mark. If the tape were written on the IBM 727 Tape Unit, there is a space of .75 inches between the check character of the last block and the tape mark.
Reflective Spots	IBM 727 Tapes carry, on the uncoated side, reflective markers made of aluminum stripping which when sensed indicate the load point (starting point) and the physical end of the tape. When reading IBM 727 no interrupt occurs when the reflective spot that serves as the end of tape warning is detected.

32300 CHECKING FEATURES

1. All information transferred from the UNISERVO Tape Unit or the Synchronizer is checked for Odd parity. All information transferred from the synchronizer to memory and vice versa is checked for Mod 3 Errors. Also, a character count is taken to check that exactly 720 characters have been read or written.

2. On metal UNIVAC tape, defective areas are automatically skipped under the control of photo cells that detect manually-punched holes 2½ inches apart on tape. On plastic tape, coating is scraped off to indicate defective areas. The resulting transparent areas allow the photo cell detection of bad spots.

32400 UNISERVO II CONTROL PANEL

The following switches and indicators are located on the control panel at the top of the Uniservo:

FORWARD	A switch-indicator which, when depressed, places the Uniservo in a forward direction condition. The indicator is lit when the Uniservo is in this condition.
BACKWARD	A switch-indicator which, when depressed, places the Uniservo in a backward direction condition. The indicator is lit when the Uniservo is in this condition.
READ	An indicator which is lit when a read operation is in process.
WRITE	An indicator which is lit when a write operation is in process.
REWIND	A switch-indicator which, when depressed in conjunction with the BACKWARD switch-indicator, causes a rewind operation to take place. The indicator is lit when a rewind operation is in process.
CHANGE TAPE	A switch-indicator which, when depressed, causes a Uniservo to be placed in a first block condition. The indicator is lit when the tape is being or has been rewound with interlock.
INHIBIT WRITE	An indicator which is lit when the supply tape reel carries a protective ring.
METAL	An indicator which is lit when the tape select switch is in the "Metal" position.
PLASTIC	An indicator which is lit when the tape select switch is in the "Plastic" position.
AIR FLOW	An indicator which is lit when an insufficient amount of air flow is detected in the Uniservo.
OVERHEAT	An indicator which is lit when the air temperature in the Uniservo reaches 130^{0} at the thermostat.
ON	A switch-indicator which turns on power to the Uniservo when depressed. The indicator is lit when the power is on.
OFF	A switch-indicator which turns off power to the Uniservo when depressed. The indicator is lit when the power is off.
NUMERAL BLOCK	A large plastic block, with the physical number of the Uniservo scribed on it, will be illuminated by a red light if the Uniservo is turned off, or if the door is open, or if the center drive motor fuse has blown. The numeral block will be illuminated by a white light if ready and available for operation.

'32500 UNISERVO II STOP/START TIMES

No.	Operation	Mode of Operation	Gap Size	Time
1.	Write 250 PPI	Stop/Start	1.05"	15.5 ms.
2.	Write 250 PPI	Continuous	1.05"	10.5 ms.
3.	Read 250 PPI (Tape written in S/S or Continuous Mode)	Stop/Start	1.05"	15.5 ms.
4.	Read 250 PPI (Tape written in S/S or Continuous Mode)	Continuous	1.05"	10.5 ms.
5.	Write 125 PPI (Between Blockettes)	Always Continuous	1.05"	10.5 ms.
6.	Write 125 PPI (Between Blocks)	Stop/Start	2.4"	29.0 ms.
7.	Write 125 PPI (Between Blocks)	Continuous	2.4"	24.0 ms.
8.	Read 125 PPI (Between Blockettes)	Always Continuous	1.05"	10.5 ms.
9.	Read 125 PPI (Between Blocks)	Stop/Start	2.4"	29.0 ms.
10.	Read 125 PPI (Between Blocks)	Continuous	2.4"	24.0 ms.

32600 CHARACTER CODE

IBM 727 TAPE
BINARY-CODED DECIMAL
CHARACTER CODES

	00	01	10	11
0000	Accumulator & Drum Mark**	Blank	-	&
0001	1	/	J	A
0010	2	S	K	B
0011	3	T	L	C
0100	4	U	M	D
0101	5	V	N	E
0110	6	W	0	F
0111	7	X	P	G
1000	8	Y	Q	H
1001	9	Z	R	I
1010	0	(Record Mark)	$\bar{0}$	$\overset{+}{0}$
1011	#	(Comma)	$	.
1100	@	%	*	
1101				
1110				
1111	Tape Mark			Group Mark

**In the IBM 705 EDP System this character is used to mark the left-hand limit of contents of the Accumulator or Auxiliary Storage Units. It is also used to indicate the End of Record on the Auxiliary Storage Drum. The character is peculiar to these units and cannot appear in memory.

40000 UNIVAC III CODE CHART

The character at the top of each box is the printing character of the High Speed and Console Printers except for Space, Bell Ring, Carriage Return and Line Feed, Horizontal Tabulate and Form Feed which are non-printing. Where two characters are shown, the one on the left applies to the COBOL-FORTRAN set and the one on the right to the UNIVAC III-USS set. If only one character is shown, it applies to both sets. In the case of NP, the character code is non-printing on the High Speed Printer but will print the character in the parentheses on the Console Printer. The code in the middle of each box is the 80-column card code. When enclosed, the code is non-standard and applies only to the Card Punch except for enclosed codes 12-5-8, 11-3-4-6-8, 0-3-5-8 and 11-3-5-8 which also apply to the Card Reader. The code at the **bottom** is the 90-column card code.

40000 UNIVAC III CODE CHART (Continued)

	00	01	10	11
0000	SPACE BLANK BLANK	+ | & 12 0-1-3-5-7	NP (5) 11 0-1-5-7-9	NP ($) 0 0-1-7-9
0001	; |) 1-4-8 1-3-5-7	) | : 12-4-8 1-3-7-9	* 11-4-8 0-1	(| % 0-4-8 0-1-5
0010	- MINUS 11 0-3-5-7	. 12-3-8 1-3-5-9	$ 11-3-8 0-1-3-5-9	, (COMMA) 0-3-8 0-3-5-9
0011	0 0 0	CARR. RET. & LN. FD. 12-0 0-1-3	BELL RING 11-0 0-3-7-9	'APOS. | + 4-8 1-5-7-9
0100	1 1 1	A 12-1 1-5-9	J 11-1 1-3-5	/ 0-1 3-5-7-9
0101	2 2 1-9	B 12-2 1-5	K 11-2 3-5-9	S 0-2 1-5-7
0110	3 3 3	C 12-3 0-7	L 11-3 0-9	T 0-3 3-7-9
0111	4 4 3-9	D 12-4 0-3-5	M 11-4 0-5	U 0-4 0-5-7
1000	5 5 5	E 12-5 0-3	N 11-5 0-5-9	V 0-5 0-3-9
1001	6 6 5-9	F 12-6 1-7-9	O 11-6 1-3	W 0-6 0-3-7
1010	7 7 7	G 12-7 5-7	P 11-7 1-3-7	X 0-7 0-7-9
1011	8 8 7-9	H 12-8 3-7	Q 11-8 3-5-7	Y 0-8 1-3-9
1100	9 9 9	I 12-9 3-5	R 11-9 1-7	Z 0-9 5-7-9
1101	: | 'APOS 4-6-8 0-1-3-7-9	= | # 3-8 0-1-5-7	NP (2) 11-3-4-6-8 0-1-9	NP (:) or('APOS) 0-3-8 0-1-3-9
1110	< | ; 4-5-8 1-3-5-7-9	NP (-) 12-5-8 0-1-5-9	HORIZ. TAB. 11-5-8 0-1-3-7	FORM FEED 0-5-8 0-3-5-7-9
1111	> | (3-5-8 0-5-7-9	NP (ZERO) 3-5-8 0-1-3-5-7-9	NP (4) 11-3-5-8 0-1-7	NP (U) 0-3-5-8 0-1-3-5

41000 HIGH SPEED PRINTER

The UNIVAC III High Speed Printer prints 128 characters (32 words of 4 characters each) per line. When single spaced, alphanumeric printing is accomplished at the rate of 700 LPM, numeric at 922 LPM. As the spacing requirements between lines increase, the effective printing rate decreases.

One instruction word specifies both line spacing (0 to 63 lines) and the location in memory of the words making up the line of print (see paragraphs 11817 and 19420). Vertical spacing of either 6 or 8 lines per inch is operator selectable. Characters are horizontally spaced at 10 per inch.

The typedrum consists of 128 bands of 51 characters each. (For character sets and codes, see paragraph 40000 and 41100.) The placement of the characters around each band is arranged in the ascending binary sequence of the UNIVAC III internal code. The characters on alternate bands are staggered to provide a checkerboard pattern on the typedrum. This arrangement minimizes adjacent character smudging by providing spaces between neighboring characters.

The synchronizer contains buffer storage for 128 characters. Therefore only 128 μs (32 memory cycles) of memory time is required to transfer data to the buffer for printing.

Buffer storage is loaded with the previously program edited print line from 32 consecutive memory locations under control of the synchronizer and memory priority circuits. Before printing begins, a tog bit is inserted in buffer storage with each blank and non-printable character. A tog bit is also inserted with each character when it has been printed. When the 128 characters in buffer storage each have a tog bit, the printing operation for that line is complete.

41100 SUMMARY OF SPECIFICATIONS

Speed	700 Alphanumeric, 922 Numeric
Character Sets	The customer may choose one of two sets, the COBOL-FORTRAN or the UNIVAC III-USS. See paragraph 40000.
Printable Characters	51
Character print positions/line	128
Horizontal pitch	10 characters per inch.
Vertical pitch	6 or 8 lines per inch, selected by operator.
Forms	Continuous, each sheet ranging in size from 4 to 22 inches wide, up to 22 inches long.
Paper Alignment	Vertical and horizontal alignment controls are provided so the operator can make final adjustments of the print alignment on the paper form. A print position indicator (1 through 128) is included as well as a print line indicator.
Forms Thickness Adjustment	A Form Thickness Adjustment is provided for the various number of copies allowed to be printed.
Ribbon	Nylon, self-rewind.
Carbons	At least 5, for paper between 11 and 13.5 pounds in weight.
Drum Speed	922 RPM

41100 SUMMARY OF SPECIFICATIONS (Continued)

Time for Paper Advance	10 milliseconds for the first line. If continuous paper advance, 8.3 ms. for 6 lpi or 6.25 ms. for 8 lpi, for each line after the first. In addition, the synchronizer allows 10 milliseconds after paper advance for stabilization of paper before printing.
Checking	a. Buffer Mod 3 Check b. Mod 3 Check on the transmission of instruction and data from the Central Processor to the synchronizer.

41200 HIGH SPEED PRINTER CONTROL PANEL

A. CONTROL BUTTON-LIGHTS

Motor On	Depressed to turn the drive motor on or off. The light is lit when the drive motor is on.
DC On/Fault	Depressed to turn DC power to the Printer on or off. The light is lit green when all DC voltages are on. It is lit red if all DC voltages are not on. If all voltages are off, no lights are lit. The Off-Line Button should be depressed prior to turning off DC power in order to avoid interaction between the HSP synchronizer and the central processor.
Ribbon Change	Depression causes the ribbon to be wound past the automatic ribbon-reverse position on the take-up shaft and the Change Ribbon indicator to light. After the ribbon is wound completely on the take-up shaft, the Out of Ribbon indicator lights and the ribbon may then be changed.
Off-Line	Depression places the Printer in an off-line mode of operation and the light is lit. Upon completion of the execution of the current Printer instruction, no further instructions will be accessed or executed. No interrupt will occur nor will the Error or Fault Indicators be set. Depression again will place the Printer in an on-line mode and extinguish the light. Printing will commence if the standby location contains an instruction.
Abnormal Clear	When lit, this indicates that a Fault condition exists in the Printer or Synchronizer. The actual Fault condition is, in most cases, indicated by another light on the Printer Control Panel. The condition must be corrected before the button is depressed to permit the program to again use the Printer and extinguish the light.

41200 HIGH SPEED PRINTER CONTROL PANEL (Continued)

A. CONTROL BUTTON-LIGHTS (Continued)

Manual Print	The Off-Line Button must be depressed prior to depressing the Manual Print Button. Depression of the Manual Print Button causes the Manual Print indicator to be lit and the characters in the buffers to be printed continuously until the button is again depressed stopping the printing and extinguishing the light.

B. CONTROL LIGHTS

Interlock	Indicates that a door on the Printer is not properly closed. The DC power to the unit is turned off.
Printer Temp.	Indicates that the temperature of the air in the Printer Cabinet is above the maximum limit. DC power is turned off.
Synchronizer Temp.	Indicates that the temperature of the air in the Synchronizer Cabinet is above the maximum limit. DC power is turned off.
Ribbon Out	Indicates that the Printer is out of ribbon.
Forms Runaway	Indicates that the paper has advanced continuously for more than 2.5 seconds.
Forms Out	Indicates that the Printer is out of paper or that the paper has been ripped.
Carriage Out	Indicates the carriage is not in the "In" or printing position. The light is extinguished when the carriage is moved to the "In" position.

C. CONTROL SWITCHES

Carriage In/Out	A rocker switch that controls movement of the carriage to the "In" or "Out" position.
6/8 Lines	A rocker switch which selects printing of either 6 or 8 lines per inch.
Forms Advance	A rotary switch which causes paper to be advanced 1 or more lines depending on the distance of rotation. This switch is active at all times.
Print Timing	This control is used to phase the print hammer timing in respect to the type-drum location; that is, in those instances where print hammers are striking prematurely or too late. They can be adjusted to strike at the instant the type-drum is in the proper position.

41200 HIGH SPEED PRINTER CONTROL PANEL (Continued)

D. CONTROL KNOBS

Horizontal Forms Alignment	Two knobs, one for the left pair of tractors and one for the right pair of tractors, are provided for horizontal forms adjustment. If the associated rocker switch is in the "Both" position, the turning of either knob will cause both pairs of tractors to move left or right in unison. If not in the "Both" position, either pair of tractors can be moved independently by turning the appropriate knob.
Vertical Adjustment	A knob which adjusts the precise vertical position of the form in relation to the printed line.
Vertical Tension	A knob which adjusts the vertical tension on the forms between the upper and lower tractors.
Forms Thickness	A knob which adjusts the clearance between print drum and print hammers for various forms thicknesses.

41300 UNIVAC III CHARACTER CODE

	No Zone 00	12 Zone 01	11 Zone 10	0 Zone 11	CARD CODE
0000	Blank	&	-	Note 1	Blnk
0001					6-8
0010					7-8
0011	0			Note 1	0
0100	1	A	J	/	1
0101	2	B	K	S	2
0110	3	C	L	T	3
0111	4	D	M	U	4
1000	5	E	N	V	5
1001	6	F	O	W	6
1010	7	G	P	X	7
1011	8	H	Q	Y	8
1100	9	I	R	Z	9
1101	>	+	:	' (Apos.)	2-8
1110	=	.	$	, (comma)	3-8
1111	<	)	*	(	4-8

N.B. The printed digit zero must be distinguishable from the Letter O. It is suggested that the zero be somewhat squared. In addition the digit 1 must be distinguishable from the letter I. The latter distinction already exists on Univac High-Speed Printers, but the former does not.

Note 1. This bit combination not available from cards.

41400 MANUAL PRINT SWITCH, MANUAL PAPER FEED, AND MANUAL PAPER SPACE

These switches will not be effectual unless the "OFF LINE" switch on the unit is pushed first.

1. Manual Print Switch

   In addition to the "OFF LINE" switch, the "UNIT CLEAR" switch must next be pushed prior to pushing the Manual Print Switch. When the Manual Print Switch is pushed "on," a line will be printed from the characters currently loaded in the odd and even buffers. The printing of this line continues until the operator pulls the switch "off."

2. Manual Paper Feed

   As long as this switch is pushed "on," the paper will advance 913 line spaces per minute. When the switch is released, paper advance will stop.

3. Manual Paper Space

   When this switch is pushed "on" and then released paper is advanced one line. Repeating the procedure will advance the paper one line each time.

51000 HIGH SPEED CARD READER

The information in this section applies to the 80 and 90 column Card Reader unless otherwise noted.

51100 SYSTEM CONFIGURATION

Any combination of 80 or 90 column Card Readers, up to a maximum of 8, may be connected to the UNIVAC III via the General Purpose Channels.

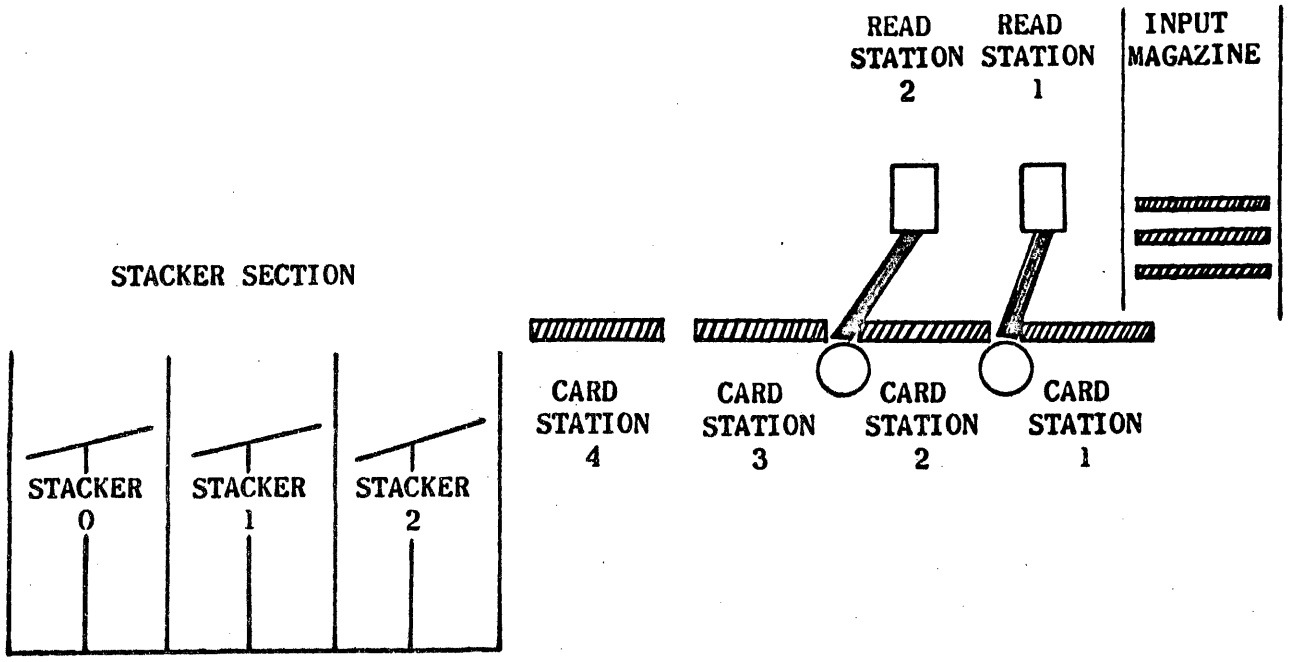
51200 SUMMARY OF SPECIFICATIONS

Card Reader (Interim)	Model 133 (80 column) Model 182 (90 column)
Card Types	80-column or 90-column
Sensing Stations	2, Read Station 1 (for check reading) and Read Station 2 (for transfers to memory)
Sensing	Holes in the card are sensed row by row by 80 brushes (for 80 column) and 45 brushes (for 90 column) at each Read Station.
Card Feed Rate	Cards pass along the feed track at a maximum rate of 700 cpm.
Card Orientation	Cards are oriented in the feed track 9 edge (lower edge) first. 80 column cards are face down and 90 column cards are face up.
Card Motion	Once the picker knife moves a card into the feed track, the card is in continuous motion until it is deposited in one of the stackers.
Input Magazine	1, with a capacity of 2000 cards.
Output Stackers	3, each with a capacity of 1000 cards.
Error and Fault Interrupts	See Paragraph 11353 D
Program Controlled Functions (See Paragraphs 19200-19240)	Feed Card Select Stacker Program Interrupt Memory Address Selection Translation
Drive Motor Shutoff	The Drive Motor is automatically turned off if no instructions have been executed by the synchronizer for a duration of several seconds. It is automatically turned on by receipt of the next reader instruction.

51200 SUMMARY OF SPECIFICATIONS (Continued)

Feed Track (As viewed from the front of the Card Reader)

The diagram below shows cards in the feed track at a point in time that is between the end of the execution of one Card Reader instruction and the beginning of another.



51300 CARD READER CONTROL PANEL

A. CONTROL BUTTON-LIGHTS

Motor On	Depression turns the drive motor on or off. The light is lit when the motor is on.
DC On	Depression turns the DC power on or off. The light is lit when DC power is on. The Off-Line Button should be depressed prior to turning off DC power in order to avoid int-action between the reader synchronizer and the central processor.
One Card	Depression of this button causes one card to be fed from the input magazine to Stacker 0 and its data to be transferred to memory in card image form (40 words). The memory location into which the data is transferred is determined by the contents of MAC at the time the button is depressed. The MAC can be cleared to zeros by depression of the CLEAR button on the Operator's Console.
Abnormal Clear	When lit indicates that a Fault condition exists in the Card Reader or Synchronizer. The actual Fault condition is, in most cases, indicated by another light on the Card Reader Control Panel. The condition must be corrected before the button is depressed to permit the program to again use the Card Reader and extinguish the light.
Off-Line	Depression places the Card Reader in an off-line mode immediately and the light is lit. When the light is lit, depression causes the Card Reader to be placed in an On-Line mode. Then, if the Standby Location Interlock Indicator is set, the instruction in the Standby Location will be accessed and executed. This button is used primarily by the customer engineer to isolate the unit from the rest of the system.
Error/Interlock	This is a two section button-light. When the upper section is lit, the detection of a data error, caused by disagreeing hole counts or by an incorrect number of memory accesses being granted to the synchronizer, is indicated. When the lower section is lit, one of the doors or covers is not in place. The Error light is extinguished by depressing the button-light.

B. CONTROL LIGHTS

Overheat	When lit, indicates the temperature inside the Card Reader is in excess of 135^{0} F.
Air Flow	When lit, indicates the blowers inside the Card Reader are not circulating a sufficient amount of air.
Misfeed	When lit, indicates that at the completion of a Feed Card instruction no card is present at Card Station 1. This is due to a misfeed or an empty input magazine.

51300 CARD READER CONTROL PANEL (Continued)

B. CONTROL LIGHTS (Continued)

Feed Jam	When lit, indicates that a Card Jam has occurred in the Feed Track.
Stacker Jam	When lit, indicates that a Card Jam has occurred in the Stacker Section of the Feed Track.
Stacker Full	When lit, indicates that one of the Card Stackers has reached its capacity.

51350 CARDS WITH CONDUCTIVE MARKS

Since there is a possibility that cards with conductive marks may produce reading errors, one of the conventions listed below should be followed.

a. Cards containing conductive marks should be fed through the Card Reader with the marks facing down.

b. If conductive marks are required on both sides of cards or on the side facing up, the marking and punching areas should not overlap.

51500 CHECKING

Brush sensing of holes in the card and the transferring of information between the synchronizer and memory are checked by the following methods:

a. As each card passes Read Station 1, a counter is increased by 1 for each hole sensed. (The counter consists of 9 bit positions and hence has a maximum capacity of 511; the arithmetic performed is modulo 512). Upon completion of sensing, the number generated in the counter is transferred to a check-counter. Then as the card passes Read Station 2, 1 is subtracted from the check-counter for each hole sensed. Also, the check-counter is decreased by 32 for each memory access granted to transfer information between the synchronizer and memory. (Again the arithmetic is modulo 512). The subtraction is an actual subtraction rather than an addition of complements. As the correct number of memory accesses to read a card is 480 (80 column) or 288 (90 column) and when multiplied by 32 equal a multiple of 512, no adjustment for the count of accesses is made to the check-counter. If the contents of the check-counter are zeros at the completion of reading the card at both stations, the card is assumed to be correctly sensed.

b. A modulo 3 check is made by the Central Processor on each word accessed from or transferred to memory. This check is also performed on each word received from the Central Processor by the synchronizer.

If any one of these checks is not satisfied, the Data Error Indicator is set and an I/O interrupt takes place.

51400 ABNORMAL CONDITIONS

1. The following abnormal conditions set the Fault Indicators in the Card Reader and CP and turn the drive motor off.

   a. Depression of the Motor Off Button on the Control panel
   b. Read Station 2 Registration Error
   c. Stacker Jam

2. The following abnormal conditions set the Fault Indicators in the Card Reader and CP and turn off DC power in the Card Reader.

   a. No Airflow
   b. Overheat
   c. Door not properly closed
   d. DC OFF
   e. Power Supply Fault

3. The following abnormal conditions set the Fault Indicators in the Card Reader and CP and inhibit the execution of Card Reader instructions as long as the Fault Indicator in the Reader is set. When a Fault Interrupt occurs, all cards remaining in the feed track are automatically selected into Stacker 2.

   a. All Motor Off conditions (No. 1 a, b and c above)
   b. All DC OFF conditions (No. 2 a, b, c, d and e above)
   c. Full Stacker
   d. Empty Input Magazine or Misfeed
   e. Logic Checks
   f. Instruction Parity Error
   g. Unit Off-Line

4. The following abnormal conditions are program testable (all are combined under the Error Indicators which they set). The card in error (the one that has just passed through Read Station 2) is automatically selected into Stacker 2.

   a. Check Read Error (hole counts do not agree)
   b. Synchronizer Underflow (unit not granted enough memory accesses to transfer card information to memory)
   c. Parity Error on a word accessed from memory or transferred to memory.

51500 CHECKING

Brush sensing of the card and transfers of information between synchronizer and memory are checked by the following method:

As each transfer between memory and synchronizer is made to set up the card image, a counter in the synchronizer is increased by 64. (The counter consists of 9 bit positions and hence has a maximum capacity of 511; the arithmetic performed in this counter is modulo 512). In addition, the counter is increased by 1 for each signal which indicates that a hole has been sensed at Read Station 1. Subsequent to the completion of reading, the number generated in the counter is transferred to a check-counter. Then, as the card passes Read Station 2, 1 is subtracted from the check-counter for each hole sensed in the card. (Again, the arithmetic is modulo 512). If the contents of the check-counter is zero at the end of the read-check, the card is assumed to be correctly sensed. (The subtraction is an actual subtraction, rather than addition of complements). As the correct number of transfers between memory and synchronizer is 480 and 480 x 64 = +0 (Mod 512), no adjustment for the count of word transfers need be made in the check counter.

Correct card alignment in the feed track is checked by a Card Registration Check at Read Station 2.

A modulo 3 Parity Check is made on each word accessed from or transferred to memory.

If any one of these checks is not satisfied, the appropriate Error or Fault Indicators are set and an I/O Error Interrupt takes place.

51600 90-COLUMN CARD READER

A 90-Column version of the Card Reader is to be developed and made available for inclusion in Univac III System some time after the first 80-Column Systems have been delivered. The 90-Column Card Reader is similar to the 80-Column Card Reader, having the same card stations in the feed track, control panel, abnormal condition indications and utilizing the same card reader instructions. Each Read Station has a set of 45 sense brushes. The transfer of information from cards to memory takes 288 memory accesses. Automatic Translation is now available. 90-Column reader and punch synchronizers and translators are packaged with their respective mechanisms in two separate cabinets of size and form comparable to (in many respects identical to) those of the 80-column equipment.

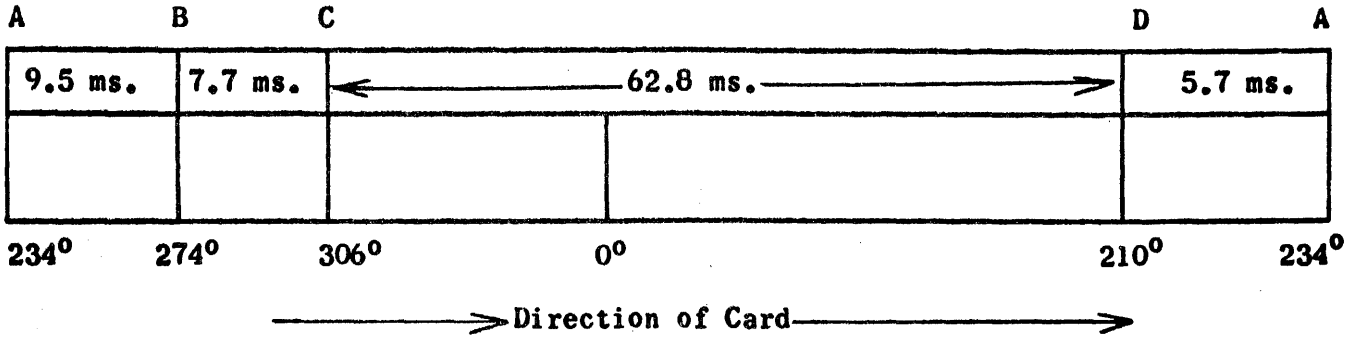
51700 90-COLUMN CARD CODE

The code chart below applies to the 90-Column Card Reader and Card Punch in the UNIVAC III System.

Zone XS-3	00	01	10	11
0000	BLANK	& 0,1,3,5,7	- 0,3,5,7	
0001				
0010				
0011	0 0			
0100	1 1	A 1,5,9	J 1,3,5	/ 3,5,7,9
0101	2 1,9	B 1,5	K 3,5,9	S 1,5,7
0110	3 3	C 0,7	L 0,9	T 3,7,9
0111	4 3,9	D 0,3,5	M 0,5	U 0,5,7
1000	5 5	E 0,3	N 0,5,9	V 0,3,9
1001	6 5,9	F 1,7,9	O 1,3	W 0,3,7
1010	7 7	G 5,7	P 1,3,7	X 0,7,9
1011	8 7,9	H 3,7	Q 3,5,7	Y 1,3,9
1100	9 9	I 3,5	R 1,7	Z 5,7,9
1101	~ 1,3,5,7,9	+ 1,5,7,9	: 1,3,7,9	' Apos. 0,1,3,7,9
1110	- 0,1,5,7	. 1,3,5,9	$ 0,1,3,5,9	, Comma 0,3,5,9
1111	< 0,1,5	) 1,3,5,7	* 0,1	(0,5,7,9

51800 CARD READER TIMING CHART

The chart below represents 1 card cycle. Point "A" is considered to be the end of one cycle and the beginning of another. A cycle equals 360° or 85.7 ms.



A. If the Standby Location Interlock Indicator is set, the synchronizer requests a memory access. When the access is granted, the instruction in the Standby Location is transferred to the synchronizer for execution. The Standby Location Interlock Indicator is reset unconditionally (regardless of whether or not the transfer was successful). At this point an interrupt will occur, if bit position 16 of the instruction is a 1 or an instruction error occurred. If bit position 16 is a 1,the Interrupt Indicator is set. If an instruction error occurred, the Equipment Fault Indicator is set. When both conditions exist, both indicators are set.

B. If the synchronizer has not found the standby location interlock indicator set by this time, one card cycle will pass until the synchronizer again attempts to access an instruction.

C. Row 9 of the card is sensed, followed by rows 8, 7 and so on until point D has been reached.

D. Row 12 is sensed. Between points D and A the synchronizer determines if a successful number of transfers of data from the card to memory has taken place and if the hole counts are equal. If so, the synchronizer is initialized for the next instruction. If not, Interrupt will take place at point A with the Data Error Indicator set, unless an Operator Contingency or Equipment Fault occurred at an earlier point in the cycle.

52000 CARD PUNCH

The information in this section applies to the 80 and 90 column Card Punch unless otherwise noted.

52100 SYSTEM CONFIGURATION

Any combination of 80 or 90 column Card Punches, up to a maximum of 8, may be connected to the UNIVAC III via the General Purpose Channels.

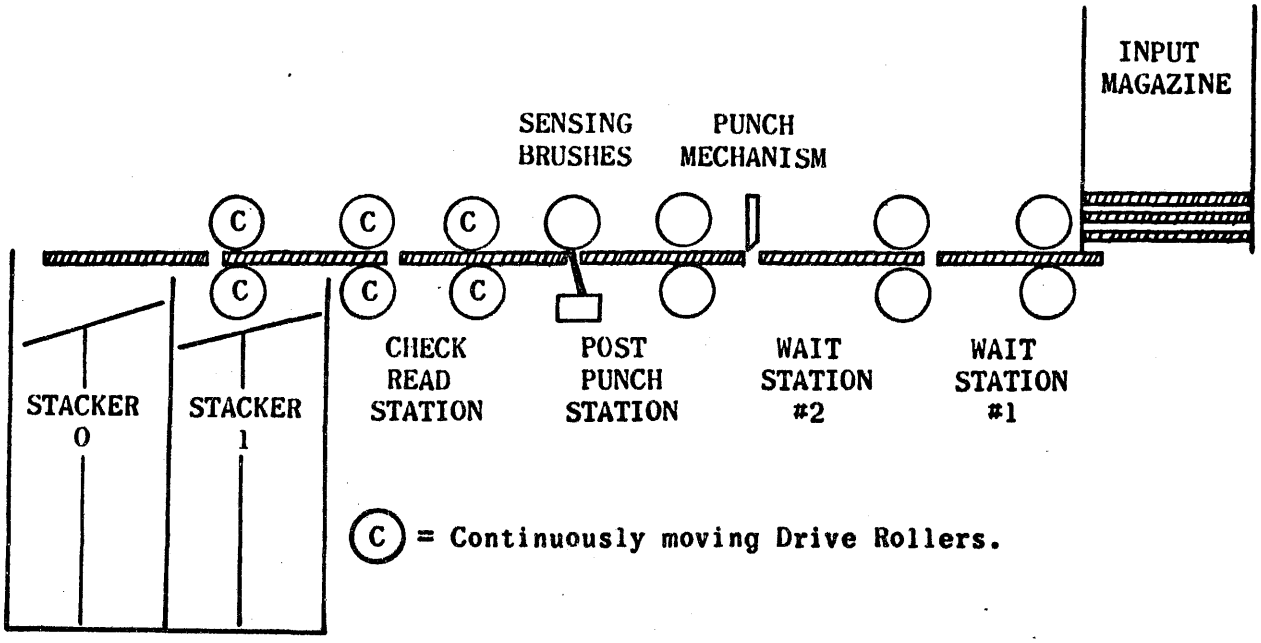
52200 SUMMARY OF SPECIFICATIONS

Card Punch	Model 127 (80 column) Model 183 (90 column)
Card Types	80 column or 90 column
Punching Method	Row-by-row
Check of Punching	Number of holes sensed at check-read station must agree with number of pulses sent to punching mechanism. (See paragraph 52400).
Card Punching Rate	Cards pass along the feed track at a maximum rate of 300 cpm.
Card Orientation	Cards are oriented in the feed track face down, 9 edge (lower edge) first. 80 column cards are face down and 90 column cards are face up.
Drive Motor Shutoff	The punch drive motor is automatically turned off if no instructions have been executed by the synchronizer for a duration of several seconds. It is automatically turned on by receipt of the next punch instruction.
Data Input from Memory	4-bit parallel, at the rate of 1 27-bit word per granted memory cycle.
Input Magazine	1, with a capacity of 1000 cards.
Output Magazine	2, each with a capacity of 1000 cards.
Program Controlled Function (See Paragraphs 19300-19340)	Feed Card Select Stacker Translation Program Interrupt Memory Address Selection
Error and Fault Interrupts	See Paragraph 11353 E.
Card Movement	Under program control, cards move in a succession of 4 card cycles along a feed path composed of an input magazine, a clutched first wait station, a clutched second wait station, a clutched post-punch station and a check read station. At the check read station, the card enters continuously moving drive rollers, and is placed in stacker #0 unless the programmer specifies stacker #1.

52200 SUMMARY OF SPECIFICATIONS (Continued)

Feed Track (As viewed from the front of the Card Punch)

The diagram below shows cards in the Feed Track at a point between card cycles (when the machine is declutched)



52300 CARD PUNCH CONTROL PANEL

A. CONTROL BUTTON-LIGHTS

Motor On	Depression turns the Drive Motor on or off. The light is lit when the motor is on.
DC On	Depression turns the DC power On or Off. The light is lit when DC power is On. The Off-Line Button should be depressed prior to turning off DC power in order to avoid interaction between the punch synchronizer and the central processor.
One Card	Depression causes all cards in the Feed Track to be moved one station forward and a card from the input magazine to be moved to Wait Station 1. To move one card from the Input Magazine to Stacker 0 requires 4 depressions: 1, Feed a card from the input magazine to Wait Station 1; 2, move it to Wait Station 2; 3, move the card through the punching mechanism to the post-punch station; 4, move the card through the Check-Read Station into Stacker 0. The button-light is only active while the Card Punch is off-line.
Abnormal Clear	When lit, indicates that an Operator Contingency or Equipment Fault condition exists in the Card Punch or synchronizer. The actual Fault condition is, in most cases, indicated by another light on the Card Punch Control Panel. The condition must be corrected before the button is depressed to permit the program to again use the Card Punch and extinguish the light.
Off-Line	Depression places the Card Punch in an off-line mode immediately and the light is lit. When the light is lit, depression causes the Card Punch to be placed in an on-line mode. Then, if the Standby Location Interlock Indicator is set, the instruction in the Standby Location will be accessed and executed. This button is used primarily by the customer engineer to isolate the unit from the rest of the system.

B. CONTROL LIGHTS

Overheat	When lit, indicates the temperature inside the Card Punch is in excess of 135^0 F.
Air Flow	When lit, indicates the blowers inside the Card Punch are not circulating a sufficient amount of air.

52300 CARD PUNCH CONTROL PANEL (Continued)

B. CONTROL LIGHTS (Continued)

Interlock	When lit, indicates one of the doors on the Card Punch is not properly closed, or the punch block is not properly positioned.
Empty Input	When lit, indicates that the input magazine is empty.
Feed Jam	When lit, indicates that a card jam has occurred between the input magazine and the Check-Read Station or a card in the input magazine was misfed.
Stacker Jam	When lit, indicates that a card jam has occurred in the stacker section of the feed track.
Stacker Full	When lit, indicates that one of the card stackers has reached its capacity.
Chip Box	When lit, indicates that the chip box is not properly positioned or requires emptying.

52400 CHECKING

The transferring of information from memory to the synchronizer and the punching of that information in the form of holes in a card are checked by the following methods:

a. As each memory access is granted to transfer information from memory to the synchronizer, a counter in the synchronizer is increased by 64. (The counter consists of 9 bit positions and hence has a maximum capacity of 511; the arithmetic performed in this counter is modulo 512). In addition, the counter is increased by 1 for each signal which indicates that a hole is to be punched. In the next cycle, the number generated in the counter is transferred to a check-counter. Then, as the card punched during the previous cycle passes the check-read station, 1 is subtracted from the check-counter for each hole sensed in the card. (The subtraction is an actual subtraction, rather than addition of complements). As the correct number of accesses to memory is 240 (80 column) or 144 (90 column) and when multiplied by 64 equal a multiple of 512, no adjustment for the count of accesses is made in the check-counter. If the contents of the check-counter are zero at the end of the check-read, the card is correctly punched.

b. A Modulo 3 check is made by the Central Processor on each word accessed from memory, and a Mod 3 check is also made on each word received from the Central Processor by the synchronizer.

If any one of these checks is not satisfied, the Data Error Indicator is set and an I/O Interrupt takes place.

53000 PAPER TAPE

Paper Tape will be read and punched by Univac III, through the use of one of the General Purpose Channels illustrated in paragraph 01000. To such a channel will be attached the Paper Tape Synchronizer, which will control the operation of both the Read and Punch units. They cannot operate simultaneously, however they are functionally independent for intermixed use. Hardware can check the validity of those tapes which have parity checks in their codes. It can supply parity bits to allow easy checking of output systems such as a leased wire network. Odd or even parity can be handled.

Both reader and punch are capable of handling paper tape in widths of 11/16", 7/8" and 1"; they can handle fully punched tape with 5, 6, 7 or 8 levels. Changing tape widths is a simple job for the operator. Tolerances, location and size of holes conform to Electronic Industries Association standard RS-227.

The following splicers have worked well in our laboratory:

Haynes Model XC
Haynes Industries Inc.
Halesite, L.I., N. Y.

53001 READER

Paper Tape will be read using the Digitronics Bi-directional Model B-3500 Reader, together with a Model 4577 Spooler. Both these equipments have been slightly modified by us. The tape may enter in anyone of three ways: It may enter in stripped form, on 8" NAB (National Association of Broadcasters) spools or on 10½" NAB spools. By operator selection, it may be run at any of three different speeds: 500 characters per second, 250 characters per second, or in a special mode of approximately 1500 to 2500 characters per second. The following table shows the possible combinations of speeds and form.

Reader Speed in Characters Per Second

Selected Mode	Non-Stop	Normal	Slow
Form of input			
8" reel (500 ft.)	1500 Approx.	500	250
10½" reel (1000 ft.)	1500 Approx.	*	250
Strip	*	500	250

*This combination is not recommended.

The reader and its spooler may be used to rewind tape under the local control of the operator. The operator can do this while the punch is operating.

The reader will handle regular, commercial paper tape. The paper may be oiled (up to 15% oil of the suitable type). Its transmissivity of light may be as high as 40%. Customers should standardize on one grade of paper tape for all the equipment which feeds the computer.

53002 NORMAL MODE

The reader and spooler together can handle 8 inch spooled paper tape at the rate of 500 characters per second and can stop "on a character". If the operator were to look at the tape, he might find it resting on the stop character, on the next character or in between, but the following operation will work correctly without loss of data.

53003 READING STRIPS OF TAPE

When the reader wishes to read strip tapes, he may do so easily by threading the tape through the reader and bypassing the spooler completely. He may run strip tape at 500 characters per second if he wishes. Some operators who have long strips of tape which they pull out of a basket may run at the slower speed of 250 characters per second. They may find that they have less trouble with tape snarls and breaks and static electricity and achieve a better operational performance.

53004 READING IN THE NON-STOP MODE

This mode is designed to satisfy the customer who has several million characters per day of paper tape to read and who is willing to give up some of the flexibility which is possible at the lower speeds. The fundamental feature of this mode is that the pinch rollers are not used and the tape is pulled through the reader by the take-up spool. When the paper tape stops in this mode, it coasts to a stop in the course of about 5 to 10 feet of paper tape. Most customers who use this mode will read a whole reel of 500 or 1000 feet of tape without stopping.

During the acceleration there is a chance that the first few characters might be repeatedly entered into memory because of jitter in the tape motion triggering the photocell several times. Therefore, there should be approximately 3 or 4 feet of leader which does not contain information at the beginning of the tape.

These tapes will often be assembled from many shorter tapes and spliced onto one reel of 500 or 1000 feet. In this case, it is convenient to splice to the end of every spool a specially colored section containing a pre-punched wired stop code. The paper tape operator may safely assume that any spool that reaches the end has been accepted by the computer. The wired stop code can be used by the program for two purposes: (1) It validates that the whole tape was read; (2) It alerts the program that the synchronizer can profitably be used to punch data for one or two minutes while the operator is changing tape on the reader.

The Non-Stop Mode requires the use of standby and alternate data areas so that the data from paper tape always has access to memory. Indeed, Reader Fault will be set in Non-Stop Mode if standby is not loaded with a new instruction or is not available by the end of the previous instruction. In order to avoid causing this fault condition, wired-stop characters should only be used as end of data characters when reading in the Non-Stop Mode.

53006 PUNCH

The Paper Tape Punch is the Teletype Model BRPE 11. It operates at 110 characters per second. A powered take-up reel is also provided. However, this reel can be ignored by the customer and the tape can be fed into a basket.

BRPE 11 can punch five channel paper tape also. The tape would be turned over in order to enter the reader for a telegraph communication network.

Nominal amounts of Mylar-based tapes can be punched for machine tool control etc. However, it causes considerable wear of the dies and excessive use is not allowed.

53010 MEMORY ADDRESS COUNTER, STANDBY LOCATION INDICATOR, COMPLETION INTERRUPT INDICATOR, FAULT AND ERROR INDICATORS

All general commands applying to input-output general purpose channel synchronizers are operative with the paper tape synchronizer. Paragraph 14600 describes the resetting of indicators, paragraph 17300 describes the testing of indicators, paragraph 21300 describes the operation "Write Contents of the Memory Address Counter to Memory and Transfer", and paragraph 21400 describes storing the contents of the memory address counter. The address of the paper tape synchronizer is specified in subparagraph "G" of paragraph 11902, and the address of its indicators is specified in subparagraph "C" of the same paragraph. The Indicator in bit position 6 is set when the wired-in stop character interrupts either the reader or the punch. If it is set in conjunction with the completion interrupt indicator (Bit #2) on a punch order, the two indicators together mean "low on paper".

53020 FORMAT IN MEMORY

In both reading and punching tape, 1-bits represent holes and 0-bits represent unpunched paper. Each character or frame on paper tape is represented by one Univac III word. The untranslated character itself is contained in the least significant positions of the word and the remaining bit positions contain binary zeros. Modulo 3 check bits for each word are handled in the standard manner by hardware.

PAPER TAPE CHARACTER - MEMORY WORD BUFFER

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	4	3	2	1	PAPER TAPE 5 Level
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	5	4	3	2	1	6 Level
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7	6	5	4	3	2	1	7 Level
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8	7	6	5	4	3	2	1	8 Level
25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	MEMORY WORD

If the synchronizer is generating parity bits for the punch, the unused bits in locations 1 to 8 of the word should be zeros.

53025 TRANSLATION BY PROGRAM

Basically all translation between the Univac III code and paper tape codes is done by programming. By use of binary addressing, field selection and multi-word features of Univac III, and with a code table in memory, the computer can translate paper tape input in approximately 50 microseconds per character. Editing Univac III words into characters for the punch requires approximately 85 microseconds per character. If the format of the data is predictable, the above figures are adequate; if the coding must look for functional codes in unpredictable locations, the times will increase significantly.

53030 SPECIAL FEATURE FOR 5 CHANNEL TAPE

In order to speed the programmed translation of this popular communications medium, special circuits are available to handle shifting without using functional characters in memory. Circuits examine bit positions 1-5 of the buffer to detect codes which can affect the implied shift status of following codes. For instance in reading, a LTRS code (holes in channels 1 2 3 4 5) is recognized by a circuit which (a) can suppress it from going into memory and decreasing the count and (b) place a ONE bit into a Shift Status flip-flop.

53030 SPECIAL FEATURE FOR 5 CHANNEL TAPE (Continued)

Similarly a FIGS code (channels 1 2 4 5) (a) does not enter memory and (b) places a ZERO bit into the Shift Status flip-flop, if desired. All the other 5 channel codes can acquire the Shift Status as a sixth bit and are placed into memory as a six-bit code. This feature can make translation simpler and faster. It also eliminates useless LTRS codes which often serve as "leaders" between messages.

A few customers have systems in which the implied shift status of the Teletype printer is affected by SPACE (00100), CARRIAGE RETURN (01000), or LINE FEED (00010). These codes are also detected by separate circuits and brought to the Format Connector (paragraph 53050) where they can be wired to jam the Shift Status Flip-Flop. (The codes would still enter memory.)

When information from Univac III is punched into 5 channel tape, normally it will be translated by program into a six bit pseudo-Teletype code (at approximately 85 seconds per 1,000,000 characters). Bits 1 to 5 will be the real Teletype code; bit 6 will be the implied shift status. This bit is compared to the Punch Shift Status flip-flop. If equal, then normal punching of one frame proceeds. However, if these bits are unequal, then the appropriate LTRS or FIGS code is punched before the data code. Again as in reading, this behavior can be suitably modified by the presence of SPACE, CR, and/or LF codes. The special circuits do not prevent the programmer from punching LTRS or FIGS codes as data. He might wish to mark the end of messages by a string of LTRS codes for a "torn-tape" communication system.

The format connector controls (cf 53050) this entire feature. There is a separate Shift Status flip-flop for the reader and the punch so that intervening use of one unit does not upset the information handled by the other when it resumes operation.

53035 READER OPERATION AT THE END OF TAPES

In some applications, the end of tape being read is marked by a Wired Stop code. (This code is defined in the Format Connector and may involve the Shift Status Flip-Flop.) When this code is read, it will stop the operation and set Indicator Bit number 6 as a signal to the program. (cf 11903.)

In other applications, it may not be convenient to place the Wired Stop Code at, and only at, the end of the tape going into the computer. Such customers will want to keep reading a tape past its physical end. This is permitted; the equipment is not harmed and the data is recoverable. When the reader runs past the physical end of the tape, the Reader Fault is set and interrupt occurs with Indicator Bit 7 on. Presumably the Executive Routine will type out on the console a short indicative message. The operator must look at the equipment. He quickly checks that the "fault" is not a malfunction, e.g. the tape has not broken or jammed, etc. Usually he would load a new tape for reading. The customer will probably have the reader restarted by a console type-in rather than using the local Reader Clear button. The need for the restart by a console type-in is the result of two features:

(1) A single synchronizer handles both the reader and the punch.
(2) A fault on reader does not block the use of the punch and vice versa.

53035 READER OPERATION AT THE END OF TAPES (Continued)

If the customer has fair volumes of both reading and punching to do, he can organize it so that the punching is done during the 60 to 90 seconds that are necessary to change spools on the reader. In this way the synchronizer is kept busy without rushing the paper tape handler.

53037 PUNCH OPERATION AT THE END OF TAPES

There is a feeler on the punch which detects a low supply of paper. This gives warning when there is at least 80 inches of tape left. This is sufficient to complete the current order and also allows end of tape messages and sentinels etc. The warning allows the current instruction to complete itself and then sets indicator Bit 6 ("Wired Stop") and also indicator Bit 2 ("Completion Interrupt"). This Low Paper indication would override Wired Stop Code condition.

53038 AUTOMATIC TURNOFF OF PUNCH

In order to save wear of the mechanical mechanism, the punch motor will be stopped after approximately a minute of idling. This feature will not concern the programmer since the motor will start automatically upon the next punch command.

53039 FAULTS AND ERRORS IN THE NON-STOP MODE

Any error recognized by hardware will stop memory transfers and any sprocket pulse which does not receive a memory access will set Reader Fault (in this Non-Stop Mode), and will bring the tape to a slow stop, skipping data. Thus some customers will prefer to detect parity errors by translation program rather than by hardware.

Normally reruns will have the operator rewind the paper tape to the beginning, and could read back the magnetic tape to the corresponding point. Alternately, the magnetic tape can remain stationary until the paper tape has been read forward till new data is encountered and normal operation resumes.

Although the Non-Stop Mode forces the computer to keep up with this "real time" peripheral for the successful reading of a whole tape, the demands on memory time and programming complexity are modest. The minimum time between characters is approximately 400 microseconds, which corresponds to a peak rate of 2500 characters per second. The entire job of reading, code translation, packing into Univac III words, even some interpretation of TAB and Carriage Return symbols, etc., and the writing of the data onto Uniservo III can be done within 110 microseconds per character.

The paper tape program may need a RUSH priority for itself and its input/output demands but it can share some 75% of the arithmetic power of Univac III with other simultaneous programs. Modest amounts of core memory should be allotted to extra output storage areas. These will allow the input to continue running even if the output tape has a bad area and needs a reissue of the same command. Conceivably an unlucky string of bad areas on magnetic tape could force a paper tape rerun because there was no more core storage left for data. We do not anticipate such troubles in normal practice and several aids are available.

53040 PAPER TAPE INSTRUCTIONS

The mode of operation of the paper tape synchronizer is essentially the same as for other input-output peripheral equipment synchronizers. Instructions are initiated by executing an Initiate I/O Instruction with the address of the general purpose channel synchronizer (see paragraph 11902G) in AR bit positions 11-14. The execution of the Initiate I/O Instruction places the addressed I/O Instruction Word (also called "Function Specification") in the synchronizer standby location at the same address in memory as the binary value of the AR bit position field of the Initiate I/O Instruction (see paragraph 19000). The synchronizer, upon becoming available, tests the standby location indicator. If it is found set, the synchronizer calls the Paper Tape Instruction Word, or Function Specification, from the standby location in memory, and executes the operation called for. The Standby Location Interlock (Indicator Bit 1) is reset when the synchronizer accepts the associated I/O Instruction Word as executable, i.e., no errors on the instruction call and the specified unit is not faulted. Normal program interrupt (if specified and if there is no error, Wired Stop, etc.) occurs at the completion of the order and after standby has supplied the next command, if any. The format of the Paper Tape Instruction Word is:

PAPER TAPE INSTRUCTION WORD

0	NUMBER OF WORDS*	OPR	m-ADDRESS
25	24 18	17 16	15 1

* Special meanings

0000000 means 256 characters to be read or punched.
1111111 tells the reader to backspace one frame; for the punch, it is not a legitimate code.

There are 3 operations available to the programmer. The operation codes appear in bit positions 16 and 17. As in other peripheral operations, bit position 16 calls for a successful completion interrupt (Indicator Bit Position 2) if a "1" is present, and this "1" is always supplied by mnemonic operation codes.

If bit position 17 is a zero, the paper tape reader is specified. If the bits in positions 18 through 24 of the Paper Tape Instruction Words are all zeros, reading of 256 characters (forward) is specified. If the binary value of this field lies between 1 and 126 then that same number of characters is read. If a value of 127 is used, the reader spaces the tape backward one character or frame; nothing is put into memory. Backspace would normally be used to reread a frame which had tripped the parity circuit.

Consecutive short reads of only one or two or three characters should be avoided in programming. Under such a condition, a character could be lost. This restriction is not burdensome considering the size of memory, the standby feature and the intended uses of this peripheral.

53040 PAPER TAPE INSTRUCTIONS (Continued)

If Bit Position 17 is a one, punching of the tape is specified. The number of characters punched is specified by binary value of the Bit Positions 18-24 of the Paper Tape Instruction Word. The value Zero has the special meaning of 256 characters. The value 127 is not defined and should not be used.

Permissible operations are:

	Bit Pos. 17	Mnemonic
Paper Tape Read, specified number of single character words	0	PTR
Paper Tape Backspace (127 in the Count Field)	0	PTB
Paper Tape Punch, specified number of single character words	1	PTP

In addition to the permissible operation codes, the synchronizer is wired to recognize stop characters specified by the customer. The reader Stop Code can be entirely different from the punch Stop Code. On both read and punch orders, the encountering of the wired-in stop character makes that stop character the last one stored or punched. The synchronizer then considers the order executed, and a "Wired Stop Character" interrupt (Indicator Bit 6) is issued. The programmer can examine the Memory Address Counter to find the last valid character.

53050 FORMAT CONNECTOR

The format connector is a removable wired panel used to supply the customer with format flexibility and the synchronizer with the information needed to automatically perform functions which differ from one paper tape system to the next. Each Punch Paper Tape Subsystem delivered to a customer shall include one format connector (for customer use), a sufficient supply of wires and a wiring tool. The connector shall be wired by the customer or local UNIVAC Sales Support personnel.

53051 SYSTEM REQUIREMENTS

Before the format connector can be wired, the following paper tape system requirements for the reader and punch must be determined:

1. Reader Requirements

a. Number of channels	Either 5, 6, 7, or 8
b. Parity	Either odd, even, or none
c. Wired-stop character	A wired-stop character may or may not be used. If it is used, its bit configuration must be established. For each bit position, three alternatives are available: the position must contain a 1-bit; it must contain a 0-bit, or it is immaterial whether it contains a 1-bit or a 0-bit. For 5-channel tape bit position 6 of the wired-stop character may contain a shift status bit if desired.
d. Memory bit position and tape channel correspondence	Any of the eight possible paper tape channel positions may be made to correspond to any of the eight bit positions of the character register which is to be transferred to memory. For 5-channel tape bit position 6 may be used to carry a status bit which eliminates the need for transferring shift codes to memory.

53051 SYSTEM REQUIREMENTS (Cont'd)

1. Reader Requirements (cont'd)

e. Jaming 0's into memory	Zeros may be jammed into any of the eight positions of the character register before the word is transferred to memory.
f. Treatment of LINE FEED, SPACE, and CARRIAGE RETURN for 5-channel applications	Each of these codes may be treated so that, when they are transferred to memory, they can effect a change to LTRS shift, or FIGS shift.

2. Punch Requirements

a. Number of channels	Either 5, 6, 7, or 8
b. Tape width*	Either 11/16 in.; 7/8 in. or 1 in.
c. Parity	Either odd, even, or none
d. Wired-stop character	A wired-stop character may or may not be used. If it is used, its bit configuration must be established. For each bit position, three alternatives are available: the position must contain a 1-bit; it must contain a 0-bit, or it is immaterial whether the position contains a 1-bit or a 0-bit. For 5-channel tape bit position 6 of the wired-stop character in memory may contain a shift status bit if desired.
e. Memory bit position and tape channel correspondence	Any of the eight possible paper tape channel positions may be made to correspond to any of the eight bit positions of the character register which contains the data that has been transferred from memory. For 5-channel tape, bit position 6 in memory may be used to carry a status bit so that shift codes can be automatically generated and punched by the synchronizer when required.

* Only tape width on the punch affects the wiring of the format connector.

53051 SYSTEMS REQUIREMENTS (Cont'd)

2. Punch Requirements (cont'd)

f. Treatment of shift codes before a LINE FEED, a SPACE, or a CARRIAGE RETURN for 5-channel applications	A shift code may be automatically punched before any or all or none of these characters, as desired.
g. Treatment of SPACE for 5-channel communications applications	If desired, the format connector may be wired so that SPACE (00100) does not change the shift status regardless of its bit position 6.

53052 WIRING THE FORMAT CONNECTOR

The format connector consists of two separate panels, A and B, of 78 hubs each (see Paragraph 53055). Hubs on paenl A are designated A1, A2, A3... A78; hubs on panel B are numbered the same but with a prefix B. Hub numbers without their prefixes are permanently marked on the panels next to each hub. Paragraph 53053 describes the wiring for reading and paragraph 53054 describes the wiring for punching.

53053 FORMAT CONNECTOR WIRING FOR THE READER

Format Used	Connector Wiring
Number of Channels	
5	The few special 5-channel wiring considerations are covered elsewhere in this table.
6	Connect B78 to B47.
7	Connect B78 to B47.
8	Connect B78 to B47.
Parity	
Odd	Connect B27 to A50.
Even	Connect B27 to A27.
None	Connect B27 to A52.
Correspondence between memory bit positions and paper tape channels	Character register entrance hubs and character register bit position correspondence are tabulated below together with the correspondence between the exit hubs from the read head and paper tape channels.

A8	A7	A6	A5	A4	A3	A2	A1
8	7	6	5	4	3	2	1

Exit hubs from read head.

Paper tape channel (Sprocket is between channels 3 and 4.)

8	7	6	5	4	3	2	1
B8	B7	B6	B5	B4	B3	B2	B1

Bit positions of the character register.*

Entrance hubs to character register.

* The character register contains the character just before it is sent to memory. 0-bits may be jammed in before it is sent to memory as described later.

53053 FORMAT CONNECTOR WIRING FOR THE READER (cont'd)

<table>
<tr><th>Format Used</th><th>Connector Wiring</th></tr>
<tr><td><u>Correspondence between memory bit positions and paper tape channels</u>

(cont'd)</td><td>Connect the entrance hubs to the character register (B1 through B8) to the exit hubs from the read head (A1 through A8) according to whatever bit position correspondence is desired.

For 5-channel tape, if bit position 6 of the character register is to be used for a status bit (without transmitting shift codes to memory), connect B6 to A26 and A49 to B78. (The status bit can be placed in bit positions other than bit position 6. In this case, A26 is connected to the desired entrance hub to the character register.) (B1 through B8)

Each of the exit hubs (A1 through A8 of any unused paper tape channels and each of the unused character register entrance hubs B1 through B8) must be connected to any of the hubs in the group: A62 through A69.</td></tr>
<tr><td><u>Wired-Stop Character</u></td><td>Each wired-stop entrance hub (B28 through B35) must be connected to one of three corresponding exit hubs; hub and bit position correspondence is shown in the table below.

<table>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>Bit positions of the character register.*</td></tr>
<tr><td>B35</td><td>B34</td><td>B33</td><td>B32</td><td>B31</td><td>B30</td><td>B29</td><td>B28</td><td>Wired-stop entrance hubs.</td></tr>
<tr><td>A25</td><td>A24</td><td>A23</td><td>A22</td><td>A21</td><td>A20</td><td>A19</td><td>A18</td><td>1-bit exit hubs.</td></tr>
<tr><td>A35</td><td>A34</td><td>A33</td><td>A32</td><td>A31</td><td>A30</td><td>A29</td><td>A28</td><td>0-bit exit hubs.</td></tr>
<tr><td></td><td colspan="6">Any B39 through B46</td><td></td><td>Exit hubs for either 0-bits or 1-bits.</td></tr>
</table>
For those bit positions where the wired-stop character contains a 1-bit, connect the wired-stop entrance hub (B28 through B35) to the corresponding 1-bit exit hub (A18 through A25).</td></tr>
</table>

* The character register contains the character just before it is sent to memory. 0-bits may be jammed in before it is sent to memory as described later.

53053 FORMAT CONNECTOR WIRING FOR THE READER (cont'd)

Format Used	Connector Wiring
Wired-Stop Character (cont'd)	For those bit positions where the wired-stop character contains a 0-bit, connect the wired-stop entrance hub (B28 through B35) to the corresponding 0-bit exit hub (A28 through A35). For those bit positions where the wired-stop character may contain either a 1-bit or a 0-bit, connect the wired-stop entrance hub (B28 through B35) to any of the exit hubs for either 0-bits or 1-bits in the group (B39 through B46). For 5-channel tape, if the wired-stop character is to have a LTRS or FIGS status denoted by the bit in position 6, then B33 must be connected either to A37 for LTRS (lower case) or to A36 for FIGS (upper case). (This status bit may be located in bit positions other than 6. The appropriate wired-stop entrance hub (B28 through B35) is connected to A37 for LTRS or to A36 for FIGS.) If a wired-stop character is not used, then any one of the wired-stop entrance hubs (B28 through B35) is connected to any of A62 to A69.
Jamming zeros into central processor bit positions	The correspondence between UNIVAC III word bit positions and the exit hubs to the central processor memory are tabulated below. To jam a zero bit into a designated bit position in the Central Processor the appropriate exit hub to the Central Processor memory (B18 through B25) is connected to any of the zero-jam hubs (A62 through A69). To let the binary digit pass on to the Central Processor, connect the exit hub (B18 through B25) to any of the hubs in the group B62 through B69.

8	7	6	5	4	3	2	1	UNIVAC III Word bit positions.
B25	B24	B23	B22	B21	B20	B19	B18	Exit hubs to central processor memory.
		Any of A62 to A69						Zero jam hubs.
		Any of B62 to B69						Hubs which permit the bit to go to memory unaltered.

53053 FORMAT CONNECTOR WIRING FOR THE READER (Cont'd)

Format Used	Connector Wiring
Treatment of LINE FEED, SPACE, and CARRIAGE RETURN for 5-channel application. (For other applications, no special wiring is required in this area.)	
Line Feed (01000)	
change to letter shift	Connect A56 to B37, B49, or B61.
change to figure shift	Connect A56 to B17, B26, or B36.
no change in shift status	Leave A56 disconnected.
Space (00100)	
change to letter shift	Connect A58 to B37, B49, or B61.
change to figure shift	Connect A58 to B17, B26, or B36.
no change in shift status	Leave A58 disconnected.
Carriage Return (00010)	
change to letter shift	Connect A60 to B37, B49, or B61.
change to figure shift	Connect A60 to B17, B26, or B36.
no change in shift status	Leave A60 disconnected.

53054 FORMAT CONNECTOR WIRING FOR THE PUNCH

Format Used	Connector Wiring
Number of Channels	
5 Communications	LTRS and FIGS codes will be automatically generated and punched as needed without any special wiring.
5 Business	Connect A53 to B50 then LTRS and FIGS codes will not be automatically generated.
6	Connect A53 to B50.
7	Connect A53 to B50.
8	Connect A53 to B50.
Parity	
Odd	Connect A38 to B38. The paper tape channel location of the parity bit is covered below.
Even	Connect A17 to B38. The paper tape channel location of the parity bit is covered below.
None	No special wiring is required.
Correspondence between memory bit positions and paper tape channels	Character register exit hub and character register bit position correspondence are tabulated below together with the correspondence between punch die entrance hubs and paper tape channels.

8	7	6	5	4	3	2	1	Bit positions of the character register.*
A77	A76	A75	A74	A73	A72	A71	A70	Exit hubs from character register.

B77	B76	B75	B74	B73	B72	B71	B70	Punch die entrance hubs.
8	7	6	5	4	3	2	1	Paper Tape Channel (Sprocket is between channels 3 and 4).

* The character register contains the data character which has been transmitted from memory.

53054 FORMAT CONNECTOR WIRING FOR THE PUNCH (Cont'd)

<table>
<tr><th>Format Used</th><th>Connector Wiring</th></tr>
<tr><td><u>Correspondence between memory bit positions and paper tape channels</u>

(cont'd)</td><td>Connect the exit hubs from the character register (A70 through A77) to the punch die entrance hubs (B70 through B77) according to the bit position correspondence desired.

If a parity bit is being punched, connect A78 to that punch die entrance hub (B70 through B77) which corresponds to the desired paper tape channel. For 7/8" paper tape B77 must be left disconnected. For 11/16" tape B75, B76, and B77 must be left disconnected.</td></tr>
<tr><td><u>Wired-Stop Character</u></td><td>Each wired-stop entrance hub (B51 through B58) must be connected to one of three corresponding exit hubs; hub and bit position correspondence is shown in the table below.

<table>
<tr><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>Bit positions of the character register.*</td></tr>
<tr><td>B58</td><td>B57</td><td>B56</td><td>B55</td><td>B54</td><td>B53</td><td>B52</td><td>B51</td><td>Wired-stop entrance hubs.</td></tr>
<tr><td>A16</td><td>A15</td><td>A14</td><td>A13</td><td>A12</td><td>A11</td><td>A10</td><td>A9</td><td>1-bit exit hubs.</td></tr>
<tr><td>A46</td><td>A45</td><td>A44</td><td>A43</td><td>A42</td><td>A41</td><td>A40</td><td>A39</td><td>0-bit exit hubs.</td></tr>
<tr><td></td><td colspan="6">Any B9 through B16</td><td></td><td>Exit hubs for either 0 bits or 1-bits.</td></tr>
</table>
For those bit positions where the wired-stop character contains a 1-bit, connect the wired-stop entrance hub (B51 through B58) to the corresponding 1-bit exit hub (A9 through A16).

For those bit positions where the wired-stop character contains a 0-bit, connect the wired-stop entrance hub (B51 through B58) to the corresponding 0-bit exit hub (A39 through A46).

For those bit positions where the wired-stop character may contain either a 1-bit or a 0-bit, connect the wired-stop entrance hub (B51 through B58) to any of the exit hubs for either 0-bits or 1-bits (B9 through B16).</td></tr>
</table>

* The character register contains the data character which has been transmitted from memory.

53054 FORMAT CONNECTOR WIRING FOR THE PUNCH (Cont'd)

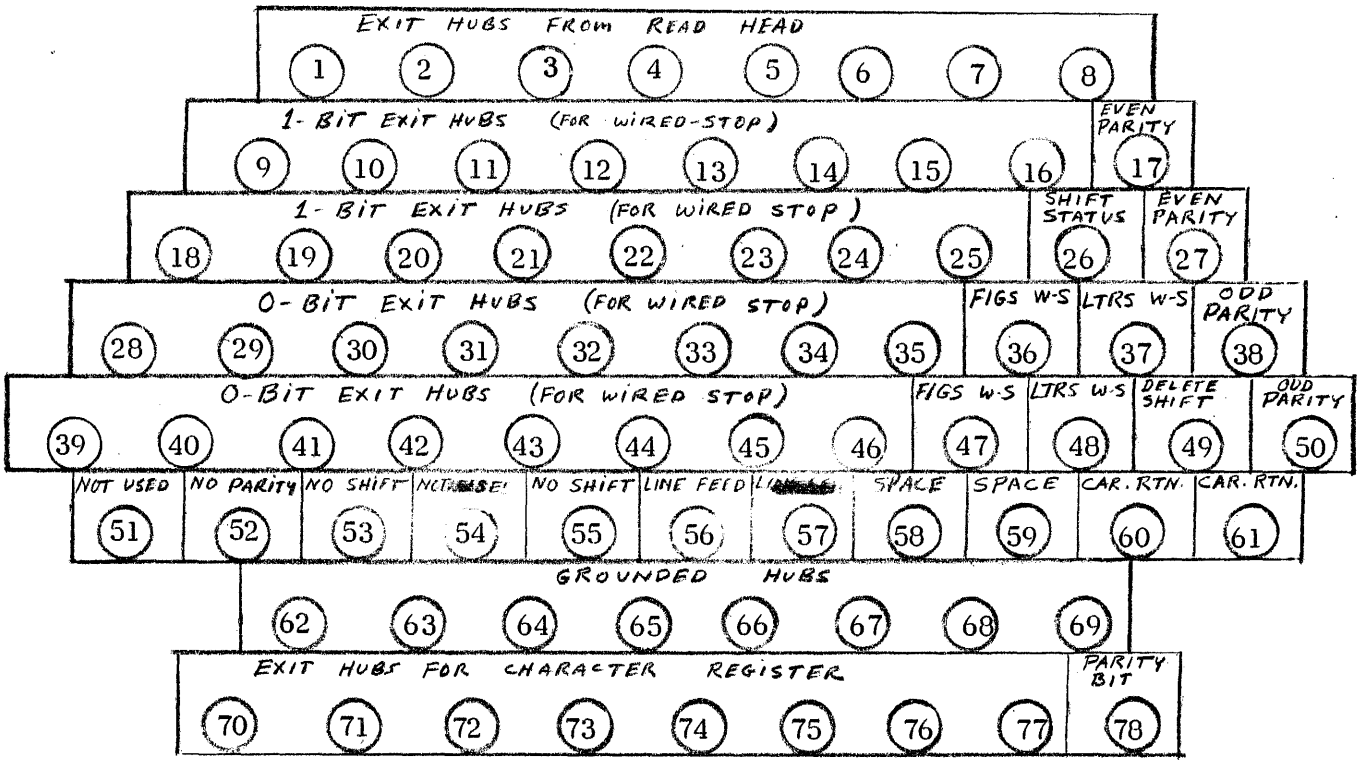
Format Used	Connector Wiring
Wired-Stop Character (cont'd)	For 5-channel tape, if the wired-stop character is to have a LTRS or FIGS status denoted by the bit in position 6, then B56 must be connected either to A48 for LTRS (lower case) or to A47 for FIGS (upper case). (This status bit may be located in bit positions other than 6.) The appropriate wired-stop entrance hub (B51 through B58) is connected to A48 for LTRS or to A47 for FIGS. If a wired-stop character is not used, then any one of the wired stop entrance hubs (B51 through B58) is connected to any of A62 - A69.
Treatment of shift codes before a LINE FEED, a SPACE, or a CARRIAGE RETURN for 5-channel applications. LINE FEED (01000) Punch a shift code before LINE FEED'S when needed. Never punch shift code before LINE FEED.	 No special wiring is required. Connect A57 to B48.

53054 FORMAT CONNECTOR WIRING FOR THE PUNCH (Cont'd)

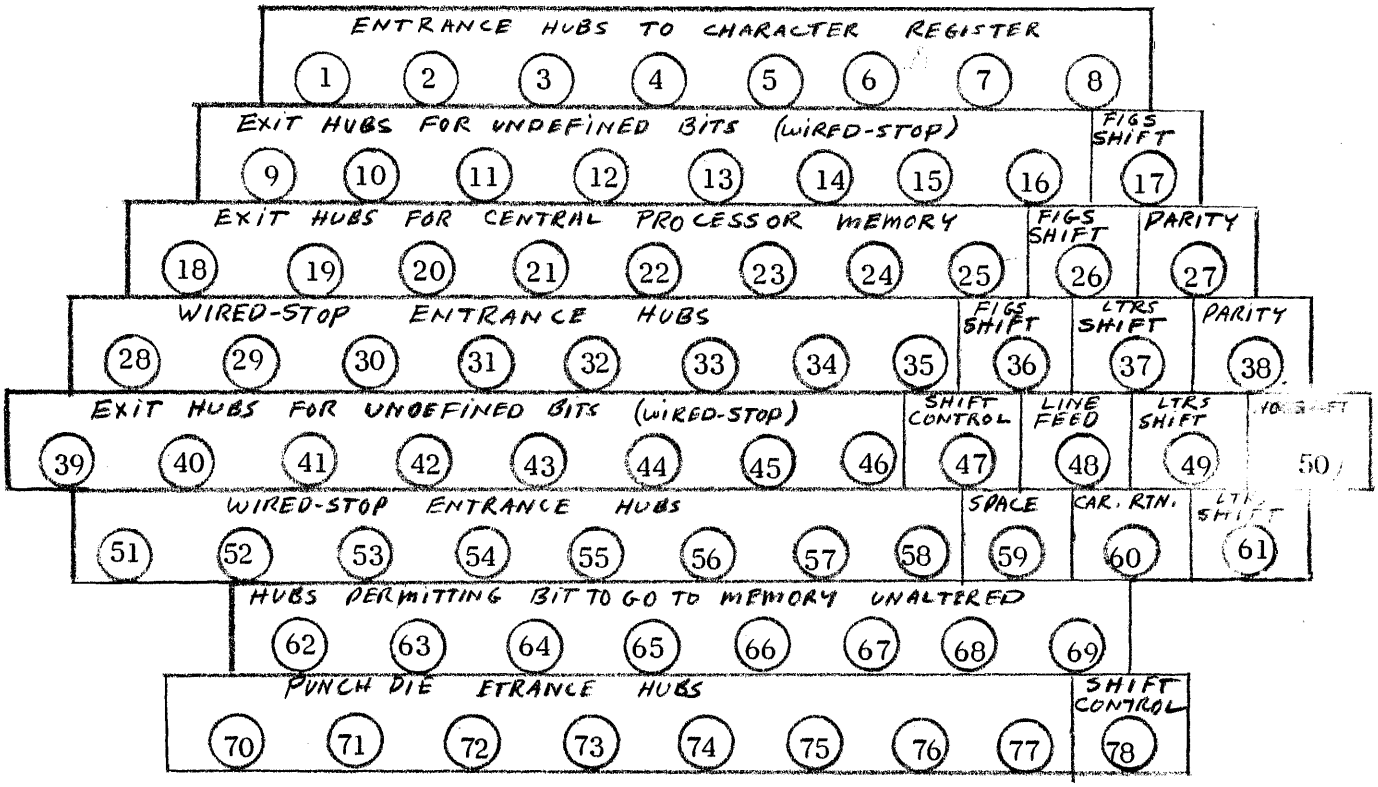
Format Used	Connector Wiring
Treatment of shift codes before a LINE FEED, a SPACE, or a CARRIAGE RETURN for 5-channel applications (cont'd) SPACE (00100) Punch shift code before SPACE when needed. Never punch shift code before SPACE CARRIAGE RETURN (00010) Punch shift code before carriage returns when needed. Never punch shift code before CARRIAGE RETURN	 No special wiring is required. Connect A59 to B59. No special wiring is required. Connect A61 to B60.
Treatment of SPACE for 5-channel communications applications	If the character, SPACE, is to have no effect on the shift status connect A59 to A55; otherwise, A55 remains disconnected.

53055 FORMAT CONNECTOR LAYOUT

PANEL A



PANEL B



53070 INSTRUCTION ERRORS

Instruction errors cause an interrupt to occur with the Data Error Indicator (bit 5) and the Standby Location Interlock Indicator (bit 1) are set. The synchronizer is inhibited from accessing memory while the Data Error Indicator is set. The following conditions are classed as instruction errors:

Memory Addressing Error	Caused when a memory addressing error occurs during the reading of an instruction from memory.
Mod 3 Error	Caused when a Mod 3 error occurs during the reading of an instruction from memory.

53071 DATA ERRORS

Data errors cause in interrupt and set the Data Error Indicator (bit 5). The Standby Location Interlock Indicator is unconditionally reset. The synchronizer is inhibited from accessing memory while the Data Error Indicator is set. If a data error is detected during reading, the indicator is set and interrupt occurs after the character in error has been transferred to memory. If a data error occurs during punching, the operation is stopped and the indicator is set, causing interrupt before the character in error is punched into the tape. The Data Error Indicator may be set in combination with the Fault Indicator. The following conditions are classed as data errors:

Memory Addressing Error	Caused when a memory addressing error occurs during the reading of a data word from memory (punching).
Mod 3 Error	Caused when a Mod 3 error occurs during the reading of a data word from memory (punching) or the writing of a data word to memory (reading).
Character Parity Error	An odd or even parity error has been detected on the character just read from tape.

53072 LOW ON PAPER - WIRED STOP CHARACTER INDICATOR

Low on paper and wired stop character conditions caused the LOW ON PAPER - WIRED STOP CHARACTER INDICATOR (bit 6) to be set, causing an input-output interrupt. The synchronizer is inhibited from accessing memory while the indicator is set. The following conditions set the indicator:

Low On Paper	The Bit 2 and Bit 6 indicators are unconditionally set when the paper supply on the punch is reduced to approximately 80 inches. In the case of a data error during the execution of an instruction which causes a Low On Paper condition, only the data error indicator **(bit 5)** is set. The Low On Paper indicator is set upon the completion of the first successful instruction following the detection of the condition.
Wired Stop Character	A wired stop character (as specified by the format connector wiring) has been detected by the reader or punch. The Bit 2 indicator is not set (even though specified in the FS) unless a Low On Paper condition for the punch is also detected.

53073 FAULTS

Faults cause interrupt with the Fault Indicator (bit 7) set upon detection of the abnormal condition. After the Fault Indicator is reset by the program, a fault for a punch will only prevent the accessing of punch unit instructions. The reader may continue with its operation. Similarly, a reader fault will only prevent the access of reader unit instructions, provided the FAULT INDICATOR is reset by the program. The synchronizer cannot access memory for data for the unit with the fault until the condition has been corrected, the appropriate Fault-Clear Button depressed and the Fault Indicator reset by the program. The Data Error Indicator may be set in combination with the Fault Indicator. The following conditions are classed as faults:

Function Specification Word Not Available	Tape is being read in the high speed non-stop mode and no FS is available in standby to control the reading of data under the read head.

53073 FAULTS (Cont'd)

Read Beyond the End of Tape	An attempt was made to read tape beyond its physical end (this is an acceptable end of tape procedure).
Broken or Jammed Tape	Tape has torn or jammed in the reader or punch.
Logic Check	A malfunction was detected as a result of one of the logic checks performed by the synchronizer on its own operation.
Unit Turned Off	The unit specified by an FS is not turned on.

53080 OPERATOR'S CONTROL PANELS

Each Punched Paper Tape Subsystem contains two control panels, one to control the reader and one to control the punch.

53081 READER CONTROL PANEL

A. Button-Lights

DC ON / DC OFF	A two sectioned button-light. The upper half lights when DC power is on. The lower half is lit when DC power is off. Depression of the button causes DC power to be removed or applied, if AC power is on.
READER ON	Lights when reader drive motor is on. Depression of button causes drive motor to be turned on or off, if DC power is on.
LOW TAPE / PF CLEAR	A two sectioned button-light. The upper half lights when less than 80 inches of tape remains on the punch supply reel. The lower half lights if a punch fault condition exists. Depressing the button after the operator has corrected a punch fault will extinguish the light and enable the punch to resume operation, provided the program has reset the FAULT INDICATOR (Bit 7) in the Central Processor.

53081 READER CONTROL PANEL (Cont'd)

A. Button-Light (cont'd)

OFF-LINE	Lights when unit is off-line. Depression places unit off-line if it has been on-line and vice-versa; however, unit does complete execution of the current function specification before going off-line.
500 CPS 250 CPS	A two sectioned button-light. Upper half lights when reader speed is set for 500 characters per second. Lower half lights when reader speed is set for 250 characters per second. Depressing the button will change the reader from one of these speeds to the other, provided the NON-STOP light is not lit.
NON-STOP	Lights when the reader is set for non-stop operation (an average of 1500 CPS). Depression causes the reader to be changed to or from Non-Stop operation.
READER FAULT CLEAR	Lights if a fault condition exists in the reader. Depression, after the operator has corrected a reader fault, causes the light to be extinguished and enables the reader to resume operation, if the program has reset the Fault Indicator (bit 7) in the Central Processor.
REWIND	Lights when the reader is rewinding. Depression causes the reader to rewind tape. This button should only be depressed when tape is motionless.

B. Buttons

HI-SPEED FORWARD	Constant depression of this button causes tape to move forward at full speed. It should not be depressed when tape is moving.
SYNCHRONIZER CLEAR	Depression initializes synchronizer so that it is ready to operate under program control.

53081 READER CONTROL PANEL (Cont'd)

C. Lights

PUNCH ON	Indicates the punch drive motor is on.
AC ON	Indicates AC power to the subsystem in on.

53082 PUNCH CONTROL PANEL

A. Button-Lights

PUNCH ON	Lights when punch dirve motor is on. Depression causes motor to be turned off or on, if DC power is on.
TAKE-UP SPOOLER ON	Lights when power to take-up spool is on. Depression turns spool on or off. The button is only operative when punch drive motor is on.
PUNCH FAULT CLEAR	Lights to indicate a punch fault condition. Depression after fault has been corrected will extinguish light and place punch unit in a ready position.

B. Buttons

SYNCHRONIZER CLEAR	Depression initializes synchronizer so that it is ready to operate under program control.

C. Lights

AC ON	Indicates AC power to the subsystem is on.
DC ON-OFF	Indicates DC power on/off status of subsystem.
LOW TAPE	Approximately 80" of tape or less remains for punching.
OFF-LINE	Indicates off/on-line status of subsystem.

70000 OPERATOR'S CONSOLE

70100 SYSTEMS CONFIGURATION

The UNIVAC III is equipped with an Operator's Console which includes an input/output typewriter, control buttons and indicators.

70200 SUMMARY OF SPECIFICATIONS

70210 INPUT/OUTPUT TYPEWRITER

Character Set and Codes	The customer may choose one of two sets, the COBOL-FORTRAN or the UNIVAC III-USS. See paragraph 40000 and 70500.
Keyboard	A standard typewriter keyboard provides the operator with the ability to enter into the typewriter buffer register, the 51 printable character codes plus certain control function. Control buttons and indicators are situated to the left and right of the character keys. Depression of a character key causes the buffer to be loaded with the 6 bit UNIVAC III code. Release of the key causes a Contingency Interrupt and sets the Typewriter Interrupt Contingency Indicator. The printing of the character must be programmed using the Write Typewriter Character Instruction. See paragraph 70500 for keyboard layout.
Character Controlled Functions	Form Feed Carriage return with line space Bell ring Horizontal tabulation Space
Speed	10 operation cycles per second. Character input or output, print box shifting between letters and figures. Carriage Return with Line Feed, Bell Ring and Space operations each require one cycle. Form Feed and Horizontal Tabulate require a variable number of cycles depending on distance.
Spacing	Horizontal spacing of 10 characters per inch and vertical spacing of 6 lines per inch. Characters are visible as soon as they are printed.

70210 INPUT/OUTPUT TYPEWRITER (Continued)

Form Feeding	Continuous forms are sprocket fed.
Copies	Up to 5 copies may be produced (using high grade paper and carbon), plus the original.
Buffer	Synchronizer contains a 6 bit buffer register (1 A/N character).

70220 CONTROL BUTTONS AND INDICATORS

Keyboard Request Button	Depression causes a Contingency Interrupt to occur and sets the program testable Keyboard Request Contingency Indicator. The button is inactive when the typewriter is off-line.
Keyboard Active Indicator	Indicator light is lit when an Activate Keyboard instruction is executed. It is extinguished when a character is typed into the buffer from the typewriter keyboard or when the Keyboard Release button is depressed. There is no associated program testable indicator.
Keyboard Release Button	Depression causes a Contingency Interrupt to occur and sets the program testable Keyboard Release Contingency Indicator. It also turns off the Keyboard Active Indicator. The button is inactive when the typewriter is off-line.
Program Run Button-Indicator	Depression causes the Central Processor to commence execution of instructions. The indicator is lit only during the execution of instructions.
Processor Error/Program Stop Indicator	This is a two section indicator. When lit, the top section indicates a Processor Error Stop (two Processor Error indicators set at one time). When lit, the bottom section indicates a Program Stop (caused by the execution of a Stop and Transfer instruction). Depression causes a Contingency Interrupt and sets the Contingency Stop Indicator.
Prevent I/O Interrupt Indicator	This indicator is lit when the program controlled Inhibit I/O Interrupt Indicator is set.

Clear Button Depression Causes the following:

a. Resets:
   1. Processor Error Indicators
   2. Contingency Indicators
   3. Input/Outout Interrupt Indicators (7 per Uniservo III synchronizer, 5 per other types of synchronizers)
   4. Sense Indicators
   5. Inhibit I/O Interrupt Indicator

b. Clears to Binary Zeros:
   1. Arithmetic Registers
   2. Index Registers
   3. Memory Address Counters
   4. Control Counter

70220 CONTROL BUTTONS AND INDICATORS (Continued)

Load Button	Depression causes logical Uniservo 0000 to read tape forward without control words. If an Error A is detected on the read operation, the light will be lit. It is extinguished by depression of the Clear Button. The button is not effective unless the Program Stop Light is lit.
Rewind Button	Depression causes the logical Uniservo 0000 to initiate a rewind without interlock instruction. The button is not effective unless the Program Stop Light is lit. If an Error B is detected during a read operation initiated by a Load Button depression, the light will be lit. The light is extinguished by depression of the Clear Button.
AC On-Off Button-Indicator	Depression causes power to the Univac III System to be turned on if in the off status and off if in the on status. The indicator has two sections, one indicates the on status when lit and the other, the off status when lit. The use of this button for turning power on can be disabled by a keylock located under the console apron.
Ready	Indicator is lit when system is ready for use.
Typewriter On/Off Line Button Indicator	If the typewriter is in an on-line status, depression causes it to be placed in an off-line status. If depressed when in an off-line status, the typewriter is placed in an on-line status. The two section indicator indicates the status.
Buzzer Button	Provides for signalling persons located at other units of the system. It is primarily a safety device. The button is located under the console apron.

70220 CONTROL BUTTONS AND INDICATORS (cont'd)

Monitor Panel	A special display panel mounted on the console top and indicating the off-line conditions for the General Purpose Channels and the abnormal (fault) conditions for the General Purpose Channels, Uniservo Power Supplies and the Central Processor. When an abnormal condition occurs, the appropriate indicator is lit and a buzzer sounds alerting the operator. The buzzer may be turned off by depressing the buzzer overide button on the monitor panel. The indicator is turned off when the abnormal condition is corrected.

70230 PHYSICAL CHARACTERISTICS

It should be high enough to allow a standing operator to use it with ease. The Operator's Console unit consists of an Input/Output Typewriter built into a table on which is mounted a panel of control buttons and indicators.

70300 TYPEWRITER OPERATION

70310 GENERAL

Input and output functions are under the control of a stored program which utilizes the Contingency Interrupt feature in conjunction with several control buttons and indicators.

70320 INPUT

Input operations may be accomplished in the following manner:

a. The operator requests the use of the typewriter by depressing the Request Button which causes a Contingency Interrupt to occur.

b. The Contingency program determines if a typewriter operation is in progress. If one is, the program makes note of this and the request is granted when the operation is completed. If an operation is not in progress, the program makes note of the request and an Activate Keyboard instruction is executed.

c. The operator types in a character causing a Contingency interrupt. The program receives the character and executes an Activate Keyboard instruction.

d. Step C is repeated until the operator has completed typing in characters.

70320 INPUT (Continued)

e. The operator then depresses the Release Button causing a Contingency Interrupt. The program determines the operation is complete and cancels the note the program made when the request was granted.

f. If the operator wishes to void the type-in at some time before releasing the keyboard, he depresses the Request Button. The program then initializes the Typein Routine because it has detected two requests not interspersed with a release.

70330 OUTPUT

Output operations are under control of the stored program and may be accomplished in the following manner:

a. The program determines that a Typewriter operation is not in progress and makes a note indicating that a typeout is in progress.

b. Program types out the message.

c. When the Typeout is completed the note the program made when the Typeout was started is cancelled.

70350 PROGRAM TESTABLE INDICATORS

The four program testable Contingency Indicators listed below are associated with the Operator's Console. They are tested by executing the Test Contingency Indicator instruction. Also see paragraph 11902 B.

a. Typewriter Interrupt - set by releasing a character key on the typewriter keyboard during input or at the completion of printing a character during output. The indicator is reset by programming.

b. Keyboard Request - set by a depression of the Request Button-Indicator on the console. Reset by programming.

c. Keyboard Release - set by a depression of the Release Button. Reset by programming.

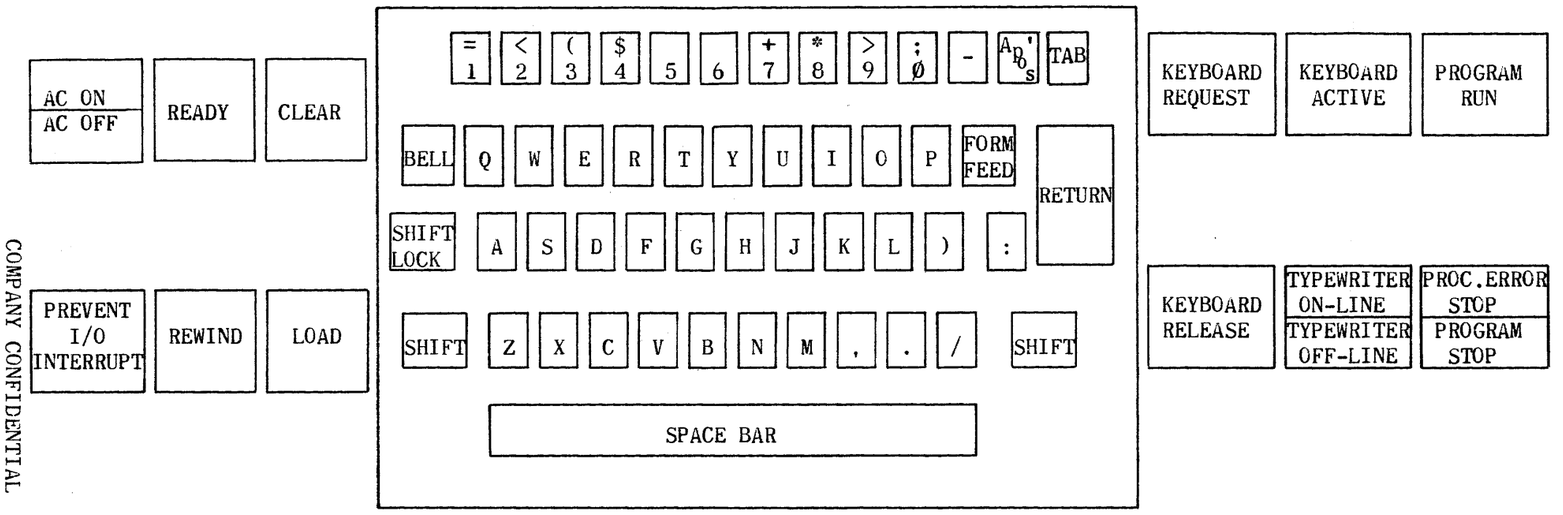
d. Contingency Stop - Set by a depression of the Contingency Stop Button. Reset by programming.

	00	01	10	11
0000	Space (Blank) Δ	12 & 0-1-3-5-7	(5)	(#)
0001	1-4-8) 1-3-5-7	12-4-8 : 1-3-7-9	11-4-8 * 0-1	0-4-8 % > 0-1-5
0010	11 - 0-3-5-7	12-3-8 . 1-3-5-9	11-3-8 $ 0-1-3-5-9	0-3-8 ; (Comma) 0-3-5-9
0011	ø 0	12-0 CARRIAGE RET. AND LINE FEED 0-1-2	11-0 BELL 0-7-9	4-8 + 1-5-7-9
0100	1	12-1 A 1-5-9	11-1 J 1-3-5	0-1 / 3-5-7-9
0101	2	B 1-5	K 3-5-9	S 1-5-7
0110	3	C 0-9	L 0-9	T 3-9
0111	4	D 0-3-5	M 0-5	U 0-5-9
1000	5	E 0-3	N 0-5-9	V 0-3-9
1001	6	F 1-7-9	O 1-3	W 0-3-5-9
1010	7	G 3-5	P 1-3-9	X 0-5-7
1011	8	H 3-9	Q 3-5-9	Y 1-3-9
1100	9	I 3-5	R 1-7	Z 5-7-9
1101	4-6-8 ; (Apos.) 0-1-3-7-9	3-8 (<) # < 0-1-5-7	(2)	( ) APOS
1110	4-5-8 (=) = 1-3-5-7-9	(-)	11-5-8 HORIZ TAB 0-1-3-9	0-5-8 FORM FEED 0-1-5-7-9
1111	3-5-8 ? 0-5-7-9	(ø)	(4)	(U)

70400 CHARACTER CODE CHART

	00	01	10	11
0000	Space Δ (blank)	&		Carriage return & line space
0001	Horizontal Tabulate		*	% (:>)
0010	Form Feed		$	Bell Ring comma ,
0011	Ø			+
0100	1	A	J	/
0101	2	B	K	S
0110	3	C	L	T
0111	4	D	M	U
1000	5	E	N	V
1001	6	F	O	W
1010	7	G	P	X
1011	8	H	Q	Y
1100	9	I	R	Z
1101				(apos.)
1110	(=) ;			(comma)
1111	(			

Bit combinations not represented by a character of function cause the typewriter to execute a no operation cycle (ignore).



NOTE: The COBOL-FORTRAN character set is shown on the key tops in the above layout. If the UNIVAC III-USS set is specified for the system, the following key top substitutions are made:

# for =	& for +	+ for ' (APOS.)
; for <	(for >	: for)
% for (	) for ;	' (APOS.) for :

71000 ADDRESSABLE CLOCK

71100 SYSTEM CONFIGURATION

The customer may specify one Addressable Clock for each UNIVAC III System. The device is optional at an additional cost.

71200 SUMMARY OF SPECIFICATIONS

Time	Modulo 24 hours
Digital Output	Hours, minutes and tenths of minutes expressed by five 4-bit XS-3 characters.
Location	The clock is located inside the Console cabinet and is not normally visible to the operator.
Time Setting	Knobs are provided on the clock housing to set the hour and minute hands.
Power Requirements	Power is supplied directly from a 115 volt A.C., 60 cycle line.
Indexing	One half second of every six seconds is required for contact settings to change. During this period, the time transferred to AR_i is invalid.

71300 OPERATION

An instruction, Load Time, is provided and accomplishes the following:

(Clock) AR_i; Time valid, (CC) + 2 → CC
Time invalid, (CC) + 1 → CC

INSTRUCTION FORMAT

OPERATION CODES: Octal 76, Mnemonic LT

ZEROS		OPR		AR		ZEROS	
25	21	20	15	14	11	10	1

71300 OPERATION (Cont'd)

INSTRUCTION FORMAT (Cont'd)

1. If the clock is not indexing, valid time is transferred to bit positions 1-20 of AR_i. The time is expressed by five 4-bit XS-3 characters. Bit positions 21-25 are set to zero. The next instruction is taken from (CC) + 2.

2. If the clock is indexing, invalid time is transferred to AR_i. The next instruction is taken from (CC) + 1.

3. If an attempt is made to execute this instruction by a UNIVAC III System that does not include an Addressable Clock, AR_i will receive binary zeros and the next instruction will be taken from (CC) + 2.

4. If more than one AR is specified in bit positions 11-14 of the instruction, the contents of the clock will be transferred to the AR addressed by the right-most bit (see paragraph 11400 for detailed discussion of register addresses).

5. Instruction execution time is 2 cycles.

6. Indirect addressing, field selection and multi-word operands are not allowed.

7. If power to the clock is dropped, a Contingency Interrupt will take place with the Overflow Indicator set at the time the Processor attempts to execute a Load Time instruction. A programmed typeout will be required to notify the operator that this contingency has occurred. The operator must then depress the Reset Button located at the clock and set the clock to the correct time. Also a check should be made to assure that the clock has power and is operating. Power to the clock is provided by a separate source.

90000 INSTALLATION DATA

91000 PHYSICAL CONSIDERATIONS

91100 PROCESSOR MODULES - OVERALL DIMENSIONS

Processor Module Type	Width (in.)	Depth (in.)	Height (in.)	Weight (lb.)	Loading(2) (lb/sq.ft.)	Floor(3) Contact
Power Supply	45	34 1/2	71	2800	280	A
Power Control	44	32 3/4	70	2000	200	A
Tape Sync. (UNISERVO II & 2nd UNISERVO III/IIIA)	44	32 3/4	70	1400	140	A
Sync. Module (UNISERVO III/IIIA & General Purpose Channels)	44	32 3/4	70	1400	140	A
Arithmetic & Control	44	32 3/4	70	1400	140	A
Memory 8,192 Words(1)	22	32 3/4	70	650	130	B
Memory 16,384 Words(1)	22	32 3/4	70	870	174	B

NOTES:

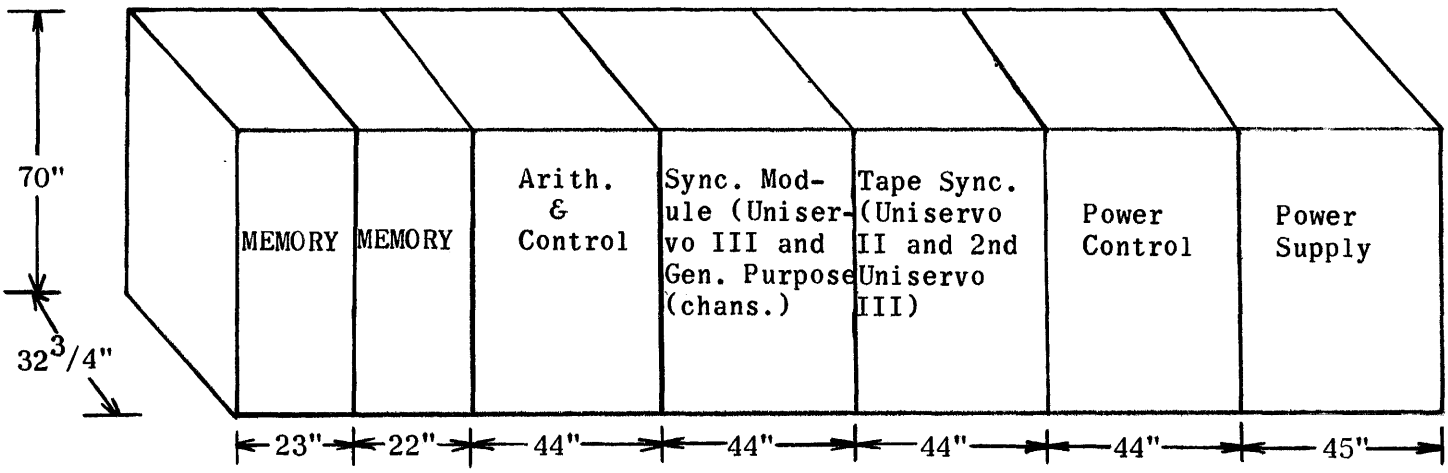
(1) The end memory module will be 23" in width, 34 1/2" in depth and 71" in height when including the end cover.

(2) Loading calculations are based on the overall dimensions of the unit.

(3) Floor contact: A = 2 leveling bars, each 4½ x 44"; B = 4 jack pads each 2" in diameter.

91100 PROCESSOR MODULES - DIMENSIONS

The sketch shows lineup of processor modules. Note that modules are placed side-by-side.



Central Processor for a Maximum System.

91200 INPUT/OUTPUT EQUIPMENT, CONSOLE-DIMENSIONS

Equipment Type	Width (in.)	Depth (in.)	Height (in.)	Weight (lb.)	Loading (lb/sq.ft.)	Floor Contact
High Speed Card Reader	28 1/2	56	52 1/2	800	75	B
Card Punch Unit	31 1/2	56	46 1/2	775	65	B
High Speed Printer (Model 152)						
Print Unit(Mod 151)	42 7/8	32	54 1/2	1700	165	B
Sync. Unit(Mod 150)	35 3/8	32	42	400	45	A
Paper Tape Reader & Punch	40	34 1/2	66	500	60	A
Operator's Console	69	33 1/2	36 1/16	500	32	B

NOTE: The Print and Synchronizer Unit of the High Speed Printer are attached together to form one unit with an overall width of 77".

91300 TAPE EQUIPMENT - DIMENSIONS

Equipment Type	Width (in.)	Depth (in.)	Height (in.)	Weight (lb.)	Loading (lb/sq.ft.)	Floor Contact
UNISERVO III/IIIA Tape Unit	30 7/8	30 7/8	63 3/8	745	113	B
UNISERVO IIA Tape Unit	30 7/8	30 5/8	69	745	113	B
UNISERVO Power Supply	45	34 1/2	71	2800	274	A
Transition Cabinet A	12	34 1/2	71	100	40	B
Transition Cabinet B	11	29 1/8	69	150	60	B
Transition Cabinet C	12	34 1/2	71	150	60	B
Adapter Cabinet	11	32 1/2	70	100	40	B
UNISERVO Corner Cabinet	30	30	63 7/8	200	24	B

NOTE: A Transition Cabinet A is required between a Tape Power Supply and a UNISERVO Tape Unit, a Transition Cabinet B between a UNISERVO III/IIIA Tape Unit and a UNISERVO IIA Tape Unit and a Transition Cabinet C with an Adapter Cabinet between a UNISERVO Power Supply and a UNISERVO IIA Tape Unit. A UNISERVO Corner Cabinet is required if a UNISERVO III/IIIA tape unit line-up makes a 90^{0} bend.

91400 OTHER MECHANICAL CONSIDERATIONS

All equipment except that covered in Section 91200 is modular in construction. Tape units are also modular. Processor modules are constructed with quick-disconnect features thus providing for field module changes. Uniservo units can be added to the end of a line by the use of an appropriate trellis sections. The use of Uniservo II units requires special trellis considerations.

Electrical connections between modules are run internally except for certain power control signals. All cables connecting Input-Output equipment and Tape Units with the Processor can enter the Processor modules at the floor level or from underneath in the case of a sub-floor. Main A.C. power enters the Processor at the Power Control module and the tape units at the Uniservo Power Supply. No other A.C. connections are required.

All units are independently air cooled with the air intake at the floor level and exhaust at the top. Replaceable filters minimize dust and dirt circulation through the equipment. The computer will signal an Early Warning when the ambient temperature of the air entering a module exceeds 83°F. The computer will continue to operate normally until the temperature reaches 85°F. At this point the machine will automatically shut down.

91500 POWER LINE SPECIFICATIONS

Power supply lines are three-phase, 60 cycles/sec. ± ½ cycle, 208/120 volts ± 5%, four-wire wye grounded neutral. A separate frame to building ground is required. Harmonic distortion is not to exceed 3%. A line voltage regulator is specified for each UNIVAC III installation and is to be supplied by the customer. See Pre-Installation Manual for details.

91600 PROCESSOR MODULES - DISSIPATION AND COOLING REQUIREMENTS

Module Type	KVA	Power Dissipated (KW) *	BTU/HR	Air Flow (CFM)	Cooling Requirements (Tons)
Power Supply	5.2	4.1	14,000	2,300	1.17
Power Control	2.3	1.8	6,200	500	.52
Tape Synch.(UNISERVO IIA & 2nd UNISERVO III/IIIA)	1.5	1.2	4,100	1,000	.34
Synch. Module (UNISERVO III/IIA & General Purpose Channels)	1.4	1.1	3,760	1,000	.31
Arithmetic & Control	1.6	1.3	4,440	1,000	.37
Memory (8,192 words)	3.0	2.5	8,530	1,400	.71
Memory (16,384 words)	3.0	2.5	8,530	1,400	.71
Memory (32,768 words)	6.0	5.0	17,060	2,800	1.42

91700 INPUT/OUTPUT EQUIPMENT - DISSIPATION AND COOLING

Equipment Type	KVA	Power Dissipated (KW) *	BTU/HR	Air Flow (CFM)	Air Conditioning Requirements (Tons)
High Speed Card Reader	1.4	1.1	3,760	250	.31
Card Punch Unit	1.8	1.4	4,780	250	.40
High Speed Printer	4.4	3.5	11,950	900	1.00
Paper Tape Reader & Punch	2.5	2.0	6,850	550	.57

91800 TAPE EQUIPMENT - DISSIPATION AND COOLING REQUIREMENTS

Equipment Type	KVA	Power Dissipated (KW) *	BTU/HR	Air Flow (CFM)	Air Conditioning Requirements (Tons)
UNISERVO III/IIIA Tape Unit	2.75	2.2	7,480	350	.62
UNISERVO IIA Tape Unit	2.62	2.1	7,140	300	.60
UNISERVO Power Supply	3.8	3.0	10,340	2,300	.86
Transition Cabinet B	.25	.2	680	150	.057
Transition Cabinet C	.25	.2	680	150	.057

*KW calculated by a power factor of 0.8.

91900 GENERAL INSTALLATION INFORMATION

1. Primarily out of consideration of paper stock and Mylar tape handling, a relative humidity of 40-60% is required.

2. Position and air volume capabilities of inlet and exhaust vents of the air conditioning system should take into account the air rates and dissipation of the various units. Ceiling exhaust vents should be located near exhaust vents at top of equipment. The air conditioning requirements specified in Sections 91600, 91700 and 91800 are based on 12000 BTU/HR requiring 1 ton of air conditioning. The specified requirements do not include cooling for room space but only for the system. It is recommended that a more detailed study be made of the particular building and exposure using the dissipation figures shown in the tables. Expansion plans are best incorporated in initial installation planning.

3. It is recommended that units stationed along walls have a clearance of at least 3½ feet. A maintenance area of 200 square feet or more should be located within the proximity of the main installation.

4. Card stock and card files should be located near the card reader and punch units.

5. The operator's console should be located such that all Uniservos are in view.

6. Primary (main) A.C. power control breakers should be located within sight of the operating area.

7. A false floor is specified for all Univac III installations. The expense is to be absorbed by the customer. It provides the following advantages:

   a. Provides an inlet air plenum for an air conditioning system.
   b. Eliminates surface cable raceways which are unsightly and dangerous to operating personnel.
   c. In some cases may help solve a weight distribution problem.
   d. Provides flexibility and ease in changing the system layout either for the purpose of improving efficiency or adding equipment to the existing system. Of course maximum cable length requirements must not be violated when changes are made.

8. Complete details concerning the planning of an installation are covered in the Pre-Installation Manual published by the Customer Services Department.

95000 COMPUTER SYSTEM OPERATIONS

95010 SYSTEM INTERRUPTIONS

In order to provide customers with Univac III's abilities and fast operating speeds at an attractive yet profitable rental price, Remington Rand Univac is designing and manufacturing the Univac III for "on-call" maintenance in most cases. Customers are assured by written contract of at least 176 hours per month of useful time for each shift on rental. We will maintain the system in a manner appropriate to the customer's special situation and our mutual best interests. Much of the minor work at the installation, currently being done by Remington Rand Univac personnel, will need to be done by the customers' operators. Three such classes of interruptions can be distinguished.

Program Recoverable

This is the least bothersome category. Magnetic tape write or read errors, and card punching errors can be corrected by the computer program without operator intervention. Assuming that correction routines do not require excessive amounts of memory, the number of such errors must only be small enough to keep the production of good output near its nominal speed. A record of bad spot areas and re-readable errors should be maintained so that inefficient reels of magnetic tape can be removed from use.

Handled By The Operator

The operator is expected to perform the following functions once per shift:

a. Turn on power to the system and run test routines for 10 to 15 minutes. Subtle types of warm-up may make the system more prone to errors at this time.
b. Turn power off.
c. Empty the Card Punch chip box.
d. Clean the read-record head and inspect the tape path and photocells and replace tape wiper if dirty for each Uniservo.
e. Perform light cleaning in the feed track area of various units.
f. The maintenance of casework appearance is the concern of the customer.

The operator is expected to perform the following functions when required:

a. Load, thread and align paper in the High Speed and Console Printers.
b. Take cards which were misread and rejected in the Card Reader and re-feed them again. For some problems the Card Reader will halt until the erroneous card is re-read. For other problems all the rejected cards can be handled at one time.

In order to reduce the number of unnecessary emergency maintenance calls, the following functions are expected to be performed by the operator. Equipment design should be such that, excluding operator caused malfunctions or changing ribbons, these actions should not need to be performed more than 6 times per 8 hour shift.

a. Change ribbons in High Speed and Console Printer.
b. Remove card jams (without the use of tools).
c. Thread leader through tape path and repair a broken tape mounted on a Uniservo.
d. Start diagnostic test routines without maintenance technician's presence. This action can overlap the technician's travel time in case of an emergency maintenance call.

95010 SYSTEM INTERRUPTIONS (Continued)

Handled By The Operator (Continued)

e. Change Uniservo designations using the plugboard in the tape synchronizer.
f. Where possible, programs should be designed so that an operator is able to modify the program to use fewer peripherals. (Presumably these changes would only be effected at rerun points).
g. Reverse memory stacks by operating a switch. (This will necessitate reloading the entire memory, e.g. from a rerun point's memory dump).

A training course in Basic Programming and Computer Operation, lasting several weeks, will be given by Remington Rand Univac. An Operator's Manual will also be published. Tape handlers as distinguished from operators, will need much less training. The economic success of on-call maintenance will strongly depend on the attitude and training of the customers' operators.

Faults Needing Emergency Maintenance

These faults are costly to both Remington Rand Univac and the customer. In order to reduce this expense, we want two qualities--reliability and maintainability--which are explained in paragraphs 95020 and 95100.

95020 RELIABILITY GOAL

The following reliability goal has been established for the Univac III: The number of system failures requiring emergency maintenance by a maintenance technician should not average more than 8.8 for every 176 hours of productive time.

This performance requirement should be met for a system configuration of:

1 Central Processor 32K memory, 15 index registers.
1 Tape Synchronizer with a Power Supply and 16 Uniservo III's.
1 Card Reader
1 Card Punch
2 High Speed Printers (Model 152)
1 Operator's Console with Addressable Clock.

By definition, reliability cannot be proven until several systems have been in operation at customer installations for some months. Therefore it cannot be determined precisely when this goal will be achieved.

95030 EQUIPMENT USAGE

It is expected that the Card Reader will read 2,000,000 cards per month; the two printers will output 20,000,000 lines per month. It is also expected that a typical installation will punch 800,000 cards per month. This is not quite 45 hours of continuous punching, but it is quite likely that customers will have the punch available all the time in order to punch a record of exceptions, machine malfunctions, etc. Unused capacity of peripherals decreases the penalty paid for their down time. In the past, customers have even rented a standby unit to obtain effective reliability. Three shift operation of a single computer is rare; the third shift is usually kept available for emergencies caused by hardware or data problems.

95040 RERUN POINTS

The customer shall provide rerun points every 15 minutes (approximately). Software should make this function an easy one. Hardware faults and errors may therefore cause a maximum loss of 15 minutes of production by the equipment involved. The reimbursement of lost time for equipment faults should therefore be limited to 15 minutes for the rerunning of calculations. Similar rerun points for the peripheral conversion routines are advisable. The operator should be able (using the console) to reprint the last page, last several pages, or the last batch. Similarly for the punch and reader. There is no real requirement for peripheral rerun points to coincide with those of the main program.

95050 HANDICAPPED OPERATION

The customer can expect to obtain some benefit from running in a handicapped mode. Perhaps only 20% of the faults will force immediate shutdown of the entire system because of failure in the power units, memory, arithmetic and control, tape synchronizer or tape trellis. Therefore, handicapped operation is possible during many failures. For example, if the card reader requires emergency maintenance, there will usually be an hour's backlog of printing, punching and calculations that can be done. It is expected that in a large majority of the time the peripherals will be treated as off-line equipment, i.e. they will communicate with Uniservo III with hardly any computation. The complicated computation **runs** will use only tape units for input and output.

The customer shall have no runs which require all his Uniservos to be operable, although he may use his spare one for "Servo Swapping" or setting up tapes for the following run. The failure of a single Uniservo III may not be corrected until scheduled (preventive) maintenance periods. However, the failure of a second tape unit would result in an emergency call. There are several ways to reduce the number of Uniservos on rental:

(a) Curtail the peripheral operations and use their Uniservo for the runs which use the maximum number.
(b) **Reduce** to one, the number of printer tapes for a run. A later sort will gather all the lines for each report into proper sequence for printing.

95060 EQUIPMENT MALFUNCTIONS

The customer's main troubles in the production of correct results will usually lie in the **keypunching** of input data. In so far as equipment malfunctions are **concerned**, the customer has the following defenses in his favor:

(a) Perhaps 75% or more of the malfunctions will give an **obvious** indication to the operator. They will trip the error circuitry or stall the program or equipment.
(b) A 15 minute test run will be executed each shift. Also the operator can schedule a short test run occasionally. This will require a few seconds to complete and several **hundred** memory locations and will detect almost all solid faults. It would be easy to incorporate this at the beginning or end of a program. In the case of runs requiring several hours to complete, it **could** be inserted at a rerun point.
(c) Solid state circuitry will fail less often **than** vacuum tubes and the failures will tend to be solid rather than intermittent.
(d) The accounting controls that were basically set up to detect input errors or fraud can be extended to find errors generated by equipment malfunctions.
(e) In exceptional cases involving hours of calculations, the customer may check some of his answers by programming, e.g. reversing factors in a few multiplications, and testing some of the results of Field Select operations.

95100 MAINTAINABILITY

Equipment design should be such that the operator's duties may be accomplished without difficulty. Interlocks should be provided to protect the operator and equipment from harming each other. Customers should follow conventions regarding documentation of programs so that maintenance engineer can quickly find "duty-cycle" errors, coding errors, etc. Logging of equipment malfunctions, including summaries of program recoverable types, is a necessary part of Univac III software.

Most emergency maintenance troubles should be repaired by experienced technicians within thirty (30) minutes after the arrival at the installation. A trouble that cannot be repaired in a four hour time period should not occur more than once a year. Operator assistance cannot be depended on.

Preventive maintenance will consist of 2 six-hour periods for a 40 hour week, 3 periods for an 80 hour one, and 4 periods for 120 hours of productive or available time. Components that will need replacement oftener than once per year should be of such weight and size that they can be removed and installed by one maintenance technician. Facilities should be provided so that the single maintenance technician can operate the various units from a position where he may not have access to the operator's control panel on the unit. This may be a start-stop switch located inside the unit's casework or a portable plug-in switch attached to a cable.

Many Uniservo faults can be corrected without the use of the Uniservo Synchronizer. The maintenance man shall be able to disconnect the faulty unit from the synchronizer (and information busses etc.) in 5 minutes. Still using the Uniservo Power Supply, he should be able to test out the mechanical operations such as start, stop, (forward and backward), rewind, etc. Thus Uniservo repair time need not halt the entire system more than five or ten minutes.

95200 FIRE PROTECTION

Because fire protection standards are being developed by government agencies and the National Fire Protection Association, all reasonably economic steps will be taken in the design of the Univac III to ensure that no cabinets or cables in the system be capable of causing or sustaining fire after power and fans are shut off. For example, backboard wires are covered with "Teflon" a noncombustible material. Circuit cards are reinforced with noncombustible fiberglass. Power and signal cables are insulated with vinyl, which does not support fire. The Pre-Installation Section of Customer Engineering Department will advise the customer in protecting tape records and the computer from fires started externally.

UNIVAC

Intercommunication

TO: All Holders of UNIVAC III Specifications

FROM: S. C. Bloom

LOCATION & DATE: Whitpain - October 21, 1963

DEPARTMENT: Product Planning

SUBJECT: REVISED UNIVAC III SPECIFICATION PAGES

The accompanying pages cover revisions and additions made since March 1, 1963. Engineering has been contacted and all changes have been approved by J. B. Deysher. The revisions are described in the attached summary.

Please replace pages, as indicated, in your copy of the specifications. Also, sign your receipt and return it to Product Planning, P. O. Box 500, Blue Bell, Pa.

S. C. Bloom

SCB:al
Attach.

October 21, 1963

PARAGRAPH	SUMMARY OF REVISIONS
01000, Minimal System	Sixth general purpose channel deleted and reference to 9 index registers added to diagram.
01000, Maximum System	Reference to mass storage synchronizer deleted. Position of sixth general purpose channel and peripheral rating chart revised. Reference to 15 index registers added.
12120, 6	Revised to add clarity.
12130, 6	Revised to add clarity.
19260, 19261, 19262, 19263, 19264, 19265	90 column read feature on 80 column reader added.
19270, 19271, 19272, 19273, 19274, 19275	80 column read feature on 90 column reader added.
31000, 3 and 5	Revised to reference Product Specification P20014 and to indicate block size convention.
53082	Paper Tape Punch control panel buttons and lights described.
70210	Description of keyboard updated.

S. C. Bloom
For Product Planning

J. B. Deysher
For Engineering

UNIVAC III

TO: All Holders of UNIVAC III Specifications

FROM: K. E. Charles

CITY & DATE: Blue Bell - March 1, 1963

DEPARTMENT: Product Planning

SUBJECT: REVISED UNIVAC III SPECIFICATION PAGES

The accompanying pages cover revisions and additions made since Sept. 14, 1962. Engineering has been contacted and all changes have been approved by J. B. Deysher. The revisions are described in the attached summary.

Please replace pages, as indicated, in your copy of the Specifications. Also sign your receipt and return it to Product Planning, P. O. Box 500, Blue Bell, Pa.

S. C. Blow for
K. E. Charles

KEC:ak
Attach.

March 1, 1963

PARAGRAPH	SUMMARY OF REVISIONS
11353, A, II, g.	The End of Tape Warning Indicator (bit 6) is set 724 us. prior to the setting of the Successful Completion Indicator (bit 2).
11620, c and e	These sub-paragraphs are revised to clarify field selection operations.
12000	The handling of undigits for decimal add and subtract instructions is clarified.
31000	UNISERVO IIIA compatible tape written by UNIVAC III must be written in start-stop mode, if it is to be read by the U1107 or U490.
31050	The read option in the write synchronizer is now a standard feature on all systems.
40000	Description of 80-column non-standard codes is revised.
53004	The last sentence of the last paragraph has been added.
53050, 53051, 53052, 53053, 53054, 53055	These paragraphs replace 53050 and contain a detailed description of the format connector.
53070, 53071, 53072, 53073	These paragraphs replace 53070 which has been rewritten.
53080, 53081	These paragraphs are additions and describe the Operator Control Panels.
71300	Sub-paragraph B is changed to read "(CC) + 2" instead of "(CC) + 1".

J. B. DeSHER
Approved for Engineering

S. C. Bloom FOR K. E. CHARLES
Approved for Product Planning

UNIVAC
Intercommunication

TO: ALL HOLDERS OF UNIVAC III SPECIFICATIONS

FROM: B. Hasbrouck

DATE: Blue Bell - September 14, 1962

DEPT: Product Planning

SUBJ: UNIVAC III REVISED PAGES

The accompanying pages cover revisions made since May 1, 1962. Engineering has been contacted and all changes have been accepted by J. B. Deysher. The revisions are described in the summary attached.

Please replace pages, as indicated, in your copy of the Specifications.

B. Hasbrouck

SB/BH/aj

B. Hasbrouck

PARAGRAPH	SUMMARY OF REVISIONS
11353, D, II	The effect of depressing the Off-Line Button is revised.
11353, E, II	The effect of depressing the Off-Line Button is revised.
12000	The fourth sentence of the first paragraph is clarified. Also a timing error is corrected in 3. of last paragraph.
19000	The Paper Tape Reader-Punch is included in 2. of last paragraph.
31000	Timing information in last paragraph corrected.
31100	Interblock gap sizes updated.
31500	Interblock gap size and timing chart revised.
32100, 2.	Reference to Uniservo IIA "Synchronizer" changed to "tape units".
40000	The 80 column card codes [5-8] [3-4-6-8] and [3-8] changed to [12-5-8] [11-3-4-6-8] and [0-3-8].
41100	Timing information for 8 lpi is added.
41200, B	Forms Runaway light is lit after 2.5 seconds of paper advance.
41200, C	Forms advance switch is active at all times.
51300, A	Card Reader now goes off-line immediately upon depression of Off-Line Button.
52300, A	Card Punch now goes off-line immediately upon depression of Off-Line Button.

J B Dreyfus
Approved for Engineering

B. Harbrouck
Approved for Product Planning

UNIVAC

INTERCOMMUNICATION

TO: All Holders of Revised UNIVAC III Specifications

FROM: B. Hasbrouck

LOCATION & DATE: Whitpain - June 12, 1962

DEPARTMENT: Product Planning

SUBJECT: UNIVAC III REVISED AND ADDITIONAL PAGES

The accompanying pages cover revisions made since February 20, 1962. Engineering has been contacted and all changes to wording or hardware have been accepted by F. R. Jones. The revisions and deletions are described in the "Summary of Revisions" below. Please replace or remove, as indicated, the appropriate pages in your copy of the specifications.

If you are no longer making active use of your copy of the specifications, please return it to Product Planning as there is a waiting list of persons who have a need for it. If you have possession of a copy assigned to another person, please notify Product Planning so that the assignment can be changed to your name, thereby assuring your receipt of future revision supplements. Commencing with this issue of revisions, if a signed receipt is not returned to Product Planning, further revisions will not be forwarded to you.

B. Hasbrouck

B. Hasbrouck

SCB/BH/nd
Encl.

PARAGRAPH	SUMMARY OF REVISIONS
TABLE OF CONTENTS	Delete the old Table of Contents. Insert the new updated and more comprehensive one.
11320, 1.	This paragraph is rewritten for clarity and to include the High Speed Printer and the Paper Tape Reader-Punch.
11320, 4.	Last paragraph clarified to state that all classes of interrupt are inhibited during a 61 or 65 instruction and also the following instruction.
11320, 8.	The High Speed Printer and the Punched Paper Tape Reader and Punch have been modified to prevent a successful completion interrupt until the previous successful completion interrupt is processed.
11353, A.	Information in this section applies to both the UNISERVO III and III-A.
11353, B. (2 pages)	All references to "IBM* 727 Tape" are deleted. Also all references to "UNISERVO II" have been changed to "UNISERVO II-A" as the UNIVAC III will only employ the Model 72 of the UNISERVO II family.

*A registered trademark of International Business Machines Corp.

PARAGRAPH	SUMMARY OF REVISIONS
11353, C, III.	Out of Paper Indicator may be set in combination with the Successful Completion Interrupt Indicator.
11353, C, IV.	Three additional abnormal conditions now cause Fault interrupt.
11353, D, II.	Information on when operator contingencies occur has been included.
11353, D, II and III.	Interlock and Off-Line classed as an operator contingency. Information on when Fault interrupts occur has been included.
11353, D, III.	Interlock and Off-Line no longer classed as faults.
11353, E, I.	A maximum of 16 ms. is allowed for the program to change the stacker bit of the instruction in standby before the instruction can be accessed and executed.
11353, E, II.	Information on when operator contingencies occur is included.
11353, E, II and III.	Interlock and Off-Line are classed as operator contingencies. Information on when fault interrupts occur is included.
11353, E, III.	Off-Line deleted as a fault condition.
11900 (First Page)	Minimum multiply time is 19 cycles. Time required to recomplement is revised.
11902, C.	References to IBM* 727 tape have been deleted from the descriptions of the Bit 5 and 6 Indicators.
18110 and 18120	The two AR's involved need not be adjacent.
18210	Zero Suppress instruction revised slightly. The non-significant codes: 000000, 000001, 000010, 000011 and 110010 are replaced by 000000.
19050	The information in sections 19051 through 19199 applies to the UNISERVO III and III-A.
19330	Data errors cause interrupt at 271^{0} of the card cycle. This allows 16 ms for the program to modify the stacker bit of the instruction in the standby location before the instruction is accessed for execution.
19430	Successful Completion Interrupt Indicator set only upon successful completion of an instruction.
19600-19699 (3 pages)	All references to IBM* 727 tape are deleted.
31050	Read feature on the write synchronizer is standard for the UNISERVO III-A Synchronizer.
31000	The information in paragraph 31000 through 31999 applies to the UNISERVO III and III-A. The UNISERVO tape units can handle a reel of 1.0 mil tape containing 3500' of recordable surface.
31100	Revised rewind speeds and tape lengths are included.
31200	UNISERVO III and III-A tape units can be intermixed in a tape lineup.

*A registered trademark of International Business Machines Corp.

PARAGRAPH	SUMMARY OF REVISIONS
31400	Slight change to Rewind button-light.
32000	All references to "UNISERVO II" have been changed to "UNISERVO II-A" since the UNIVAC III will only employ Model 72 of the UNISERVO II family.
32210	All references to IBM* 727 tape are deleted.
32230	This paragraph deleted.
32300	All references to IBM* 727 tape are deleted.
32600	This paragraph deleted.
40000	Revised to reflect choice of character sets.
41000	The reference to paragraph 41300 changed to 40000 and 41100.
41100	Choice of character sets is provided.
51200	Card orientation in the feed track has been revised for the 90 column reader.
51300	Off-Line button-light revised. A new indicator, "Error", has been combined with the Interlock light.
52200	Card orientation in the feed track has been revised for the 90 column punch.
52300, A.	Off-Line button-light revised.
52300, B.	An interlock condition does not turn off DC power.
70210 and 70500	Revised to reflect choice of two character sets.
91100	Minor revisions to a number of dimensions, weights,
91200	etc.
91400	
91500	
91600	
91700 and 91800	

B. Hasbrouck
Approved For Product Planning

F R Jones
Approved for Engineering

nd

REMINGTON RAND

INTERCOMMUNICATION

TO: All Holders of Revised Univac III Specifications

FROM: B. Hasbrouck

CITY & DATE: Whitpain - February 28, 1962

DEPARTMENT: Product Planning

SUBJECT: UNIVAC III
REVISED AND ADDITIONAL PAGES

The accompanying pages cover revisions made since 11/10/61. Engineering has been contacted and all changes of wording or hardware have been accepted by G. Smoliar. The changes and additions are described in the "Summary of Revisions" below. Please replace or remove, as indicated, the appropriate pages in your copy of the specifications.

B Hasbrouck

B. Hasbrouck

SCB/BH/nd

Paragraph	SUMMARY OF REVISIONS
11320, 4, c.	The last sentence is deleted since the same information is included in 11353, 4, b.
11320, 5	The first sentence is revised to include all classes of interrupt rather than only the class of interrupt just effective and any classes of lower priority.
11330	Processor Errors 5. and 6. are clarified.
11353, A	If the Error A, Error B, Busy or Fault indicator is set, the synchronizer cannot access the standby location.
11353, A, I, c.	Reflects the recent Uniservo III, IIIA File Protection Philosophy change, i.e. the absence of a ring inhibits writing.
11353, A, II.	The first sentence is revised. The second sentence is deleted.
11353, A, II, g.	End of Tape Warning Indicator (Bit 6) is set and interrupt occurs at completion of instruction execution. When the Bit 6 indicator is set, the synchronizer is inhibited from accessing the standby location.

Paragraph	SUMMARY OF REVISIONS (Cont'd)
11353, A, II, h.	The reverse start sentinel and the reverse start pattern are not recorded when this case occurs.
11353, A, III	Data transfers to memory are now terminated immediately upon detection of Mod 3 Error during a Scatter Read operation.
11353, A, III, f.	End-of-Tape Warning indication and interrupt have been deleted from the Uniservo III, IIIA Read Synchronizer.
11353, C, III	The amount of paper available for printing after an out of paper warning may be 0" to 2.5" depending on the number of lines of paper advance specified by the last instruction executed.
11353, D, II	Depression of the Off-Line button-light is deleted as a condition that causes an Operator Contingency Interrupt for the Card Reader.
11353, D, III	Stacker selection explained for those faults not causing interrupt. Depression of the Off-Line Button-Light is added as a Fault Condition that does not set the Fault Indicator nor cause interrupt for the Card Reader.
11353, E, II	Depression of the Off-Line Button-Light is deleted as a condition that causes an Operator Contingency Interrupt for the Card Punch. Chip Box Full has been added as a condition that causes Operator Contingency for the Card Punch.
11353, E, III (Cont'd)	Stacker Selection explained for those Faults not causing interrupt. Depression of the Off-Line Button-Light is added to No Airflow, Overheat, Power Supply Fault and DC Off Button-Light depression as conditions which do not cause fault interrupts for the Card Punch.
11500	Bit Position 16 of existent index registers is always zero.
11902, A.	Adder Error and Memory Address or Mod 3 Error on access of transfer of control instruction are clarified.
11902, C, (Bit 7), 2.	An instruction call error for the Uniservo II Synchronizer is indicated by Indicator Bits 1, 5 and 7.
19110	When the first tape control word for a Gather-Write operation is a stop control word, tape runaway will occur. The value of bit positions 1-15 of a stop control word shall not exceed the highest memory address available for the system concerned.

February 28, 1962

Paragraph	SUMMARY OF REVISIONS (Cont'd)
19110 Layout of Tape Block	Changes in the number of frames in the forward and reverse start sentinels and patterns.
21300	Bit position 16 of the MAC's is always zero.
21400	Bit position 16 of the MAC's is always zero.
31100	Distance between erase head and write head is nominal 1 13/16". Descriptions of Load Point and End of Tape Warning windows have been added.
31400	The Inhibit Write Indicator will be lit when a reel not containing a ring is mounted on a Uniservo.
40000	Addition of an updated code chart.
41200, A.	The Off-Line Button-Light should be depressed prior to turning off DC power in the HSP.
41300	Delete this page.
51300, A.	The Off-Line Button-Light should be depressed prior to turning off DC power in the Card Reader. The depression of the Off-Line Button-Light does not cause an Operator Contingency Interrupt.
51700	Delete this page.
52300, A.	The Off-Line Button-Light should be depressed prior to turning off DC power in the Card Punch. The depression of the Off-Line Button-Light on the Card Punch does not cause an Operator Contingency.
70400	Delete this page.

The release of these specification changes is approved by the undersigned.

G. Smolar
For Engineering

Robert Rund
For Product Planning

REMINGTON RAND

INTERCOMMUNICATION

TO: All Holders of Revised Univac III Specifications

FROM: B. Hasbrouck

CITY & DATE: Blue Bell - 11-10-61

DEPARTMENT: Product Planning

SUBJECT: UNIVAC III SPECIFICATIONS REVISED AND ADDITIONAL PAGES

The accompanying pages cover revisions made since 9/18/61. Engineering has been contacted and all changes of wording or hardware have been accepted by G. Smoliar. The changes are described in the "Summary of Revision" below. Please replace or remove, as indicated, the appropriate pages in your copy of the specifications.

B. Hasbrouck

B. Hasbrouck

BH/nd
Encl.

Paragraph	SUMMARY OF REVISION
11353, A, II	Minor clarifications made and End of Tape Warning revised.
11353, A, III	Several additions to first paragraph, others clarified.
11353, C	This section has been updated and amplified.
11353, E, III	Door Interlock does cause interrupt, therefore it has been removed from this section.
11620	Main paragraph clarified, also subparagraphs c and e.
15100	Subparagraph 8 added.
19051	Contingency Write instruction only to be issued after a forward tape operation. Blocks to be overwritten must be a minimum of 150 words in length.
19110	Section rewritten for clarification. Diagram of tape layout updated.
19120	A means of skipping a block of tape is given in last paragraph.
19130	Clarified.
19150	Description of a new instruction, Load Point Test.
19400	Zero lines of advance when printing is not specified is now a legal function specification.
21400	Last paragraph added.
31000, 3rd page	Note 5 added.
31400	Description of control panel added.
41000-41100	Rewritten to clarify and include minor revisions.
41200	Descriptions of controls added.

Paragraph	SUMMARY OF REVISION
53000	
53002 53006	Added Non-Stop mode for the reader. Rearranged sections.
53039	Added Faults and Errors in Non-Stop mode.
70220	Descriptions of controls updated.
70340	Paragraph deleted.
70500	Operator's Console Keyboard and Control Panel Layout updated.

The release of these specification changes is approved by the undersigned.

H. Smoliar
For Engineering

Robert Russell
For Product Planning

REMINGTON RAND

INTERCOMMUNICATION

TO: All Holders of Revised Univac III Specifications

FROM: B. Hasbrouck

CITY & DATE: Blue Bell - 10-23-61

DEPARTMENT: Product Planning

SUBJECT: UNIVAC III SPECIFICATIONS REVISED PAGES DATED 9-18-61

The accompanying pages cover revisions made since July 11, 1961. Engineering has been contacted and all these changes of wording or hardware have been accepted by G. Smoliar. The changes are described in the "Summary of Revision" below. Please replace or remove, as indicated, the appropriate pages in your copy of the specifications.

B. Hasbrouck

B. Hasbrouck

BH/nd

Paragraph	SUMMARY OF REVISION
11320, 1	Clarifies the setting of the Interrupt Indicator for the Card Reader and Card Punch Synchronizers.
11320, 9	Clarifies the resetting of Standby Location Interlock Indicator for Card Reader and Card Punch Synchronizers.
11330	New list of Processor Errors.
11340	Overflow in Division clarified.
11353, B	Section rewritten, memory addressing error on write to memory eliminated (now a Processor Error).
11353, D, I, II, III	Revised to include both 80 and 90 Column Card Readers. Several changes included.
11353, D, IV	Delete this page.
11353, E	Revised to include both 80 and 90 Column Punches. Several changes included.
11815	Console Typewriter input instruction word layout added.
11817	An instruction specifying no printing and no paper advancing is now permitted.
11900	Console Typewriter instruction diagrams corrected. Shift instructions execution time brought up to date. Test Instructions resulting in m' → CC require only 1 cycle to execute. Compress and Expand instruction execution times revised. Zero Suppress instruction diagram corrected. Increment and Compare Index Register instruction diagram changed to show comparison is made on 15 bits.

Paragraph	SUMMARY OF REVISION
11900 (Cont'd)	Unload Index Register instruction diagram corrected to show 16 bits are stored. Write (MAC) to memory and Transfer instruction diagram changed to show 16 bits are stored. Write (MAC) to Memory instruction diagram changed to show 16 bits are stored.
11901	Punched Paper Tape Synchronizer instructions revised to agree with Section 53000.
11902 A	Processor Error conditions and indicator settings revised.
11902 C	Synchronizer indicator descriptions expanded. Several revisions included.
11902 D, E, F, G, H	These paragraphs rewritten.
11903	Delete this page.
12000	In all addition and subtraction instructions, zero value results are always positive.
14450	Processor Error list removed (see 11902 A for List).
15300 and 15400	Setting of Equal Indicator clarified.
16000	Addition information on the shift count provided.
19000 (First Page)	Synchronizer standby locations occupy memory locations 00003 through 00015.
19200, 19210, 19220, 19230, 19240	Rewritten to include both 80 and 90 Column Readers. Several revisions included
19300, 19310, 19320, 19330, 19340	Rewritten to include both 80 and 90 Column Punches Several revisions included.
20000	Information on the result of an instruction specifying a non-existent IR.
20110	Comparison made on 15 bits.
51000, 51100, 51200, 51300, 51500, 51800	Revised to include both 80 and 90 Column Card Readers. Several changes included. Control panel functions described.
51400	Delete this page.
51600	This paragraph deleted.
52000, 52100, 52200, 52300	Revised to include both 80 and 90 Column Card Punches. Several changes included. Control panel functions described.
52400	Section on checking added.

B. Hasbrouck

B. Hasbrouck

SCB/BH/nd

The release of these specification changes is approved by the undersigned.

Gerald Smolar
For Engineering

C. Robert Russell
For Product Planning

REMINGTON RAND UNIVAC

INTERCOMMUNICATION

To: All Holders of Revised Univac III Specifications

From: C. R. Russell

Date: Blue Bell - July 24, 1961

Department: Product Planning

Subject: REVISED AND ADDITIONAL PAGES DATED JULY 10, 1961

The accompanying pages cover revisions made since July 11, 1961. Please replace the appropriate pages of your copy of the specifications.

for B. H. Hauck
C. Robert Russell

BH/CRR/nd
Encl.

SUMMARY OF CHANGES

11800 second page	Separate the "Console Typewriter Instruction Word" into two formats.
53000 to 53070	Replace with new section.

Note regarding 53025, "Translation by Program:" The speeds quoted for translating (50 μsec per character for reading and 80 μsec/char. for punching) include code translation and also the packing or unpacking of words between the normal Univac III format (4 characters per word) and the PPT synchronizer format (one character per word). An allowance for one interrupt and its interpretation by the executive routine for each group of 256 characters is also included in these times.

REMINGTON RAND

INTERCOMMUNICATION

TO: All Holders of Revised Univac III Specifications

FROM: C R Russell

CITY & DATE: Blue Bell - July 11 1961

DEPARTMENT: Product Planning

SUBJECT: Univac III Specifications Manual Revised Pages

The accompanying pages cover revisions made since May 5, 1961. Revisions are mostly to remove ambiguities and provide clarification; however, several reflect minor changes. These revisions are described in the "Summary of Changes" below. Please replace the appropriate pages in your copy of the specifications and remove the pages headed by paragraph 31412 (2 pages).

C Robert Russell

SCB/DH/CRR/nd

SUMMARY OF CHANGES

11320, 3.	Indication added that addresses in tables are decimal.
11320 (end of sub-paragraph 4)	Interrupt Mode Indicator is automatically reset when a Reset instruction actually resets at least one indicator which was set.
11400	Final sentence to explain effect of A2 field being all zeros.
11500	Index Register 16-bit size is explained.
11600 and 11610	Zero Bits in positions 18-20 of control words indicate indirect addressing.
11800	Indirect Addressing specified by zeros in positions 18-20 of IACW's.
11806	Unloading an index register places the 16-bit contents of the IR in the addressed location in memory.
11808	An Indirect Address Control Word is indicated by zeros in bit positions 18-20. Bits in positions 16 and 17 are disregarded.
11812	I/O Instruction Words must have zero in bit position 35.
12000	In leading paragraph, behavior of binary zeros in decimal operands is explained.
12300	Zeros must be decimal in both operands in Multiplication.
12410	In Division all zeros in both operands must be decimal.
13000	Clarification of timing for indirect addressing and field selection.
14100 and 14200	Clarification of operation when field selection is called for.
14400	Sub-paragraph added to indicate that the command prevents interrupt until execution of the following instruction.
14550	Sub-paragraph 2 added to indicate that the command prevents interrupt until execution of the following instruction.
15300 and 15400	These instructions are clarified.

SUMMARY OF CHANGES (Continued)

18210	Clarification of the ZUP instruction will follow in the next collection of revision sheets.
19000	I/O Instruction Words must have zero in bit position 25. Resetting of Standby Location Interlock Indicator is clarified. Second page includes slight clarifications.
19051	In Uniservo III Instruction Words, bit position 20 is now always specified. Uniservo III Tape must be bulk erased before initial use and after each change of Load Point Window.
19110	Slight modification of last sentence concerning array of sentinels on tape.
19150	Delete full section (2 pages) and replace by this restatement of the use of Contingency Read commands.
19530	Bit positions 1-6 of the AR must be zeros prior to execution of Read Typewriter Instruction.
20130	STX Instruction unloads 16 bits of IR into memory.
21300	Same as above. Also Final clause added to last sentence.
21400	Explanation of command operation is expressed in greater detail.
31000	Correction to statement regarding resetting of Standby Interlock Indicator (end of next to last paragraph) End of Tape transmissive window now located 25 feet from physical end of tape. Other minor restatements to avoid misinterpretations.
31412	Delete the two pages.
32230	Reflective spot on IBM 727 tapes does not cause an interrupt if encountered during reading.
32300	Sub-paragraph 3 added to explain employment of protective ring for IBM 727 Tape.
53000	Disregard All of the Specification for Paper Tape. A major revision is forthcoming.

REMINGTON RAND

INTRACOMMUNICATION

TO: All Holders of Revised Univac III Specifications

FROM: C. R. Russell

CITY & DATE: Blue Bell - May 19, 1961

DEPARTMENT: Product Planning

SUBJECT: Revised and Additional Pages

A new section covering the reliability of Univac III is included in this batch. This will be a very sensitive subject to discuss with customers and you are advised to be particularly cautious in your statements about the actual achievement of these reliability goals. We quote section 95020:

> "By definition, reliability cannot be proven until several systems have been in operation at customers' installations for some months. Therefore it cannot be determined when this goal will be achieved."

Please replace the appropriate pages in your copy of the specifications and add the new pages.

B. Harbrouck
for C. Robert Russell

BH/CRR/nd
Encl.

SUMMARY OF CHANGES

Page Headed By Below Numbered Paragraph	
11200	Added mention of the checking that the address actually operated on by the memory is the same as the address specified. This revision is dated 4-19-61.
19300 19320	These two pages amended to agree with an earlier change--interruption occurs at a successful initiation instead of a completion.
95000 95010 (Cont.) 95040 95100	These four pages have been added to cover computer operation and reliability goals.

REMINGTON RAND

INTRA-COMPANY COMMUNICATION

TO: All Holders of Revised Univac III Specifications

FROM: C. R. Russell

CITY & DATE: Whitpain - 5-4-61

DEPARTMENT: Product Planning

SUBJECT: Revised and Additional Pages

The accompanying pages cover revisions and additions made since February 14, 1961. Changes include details resulting from current construction and testing of the prototype model, changes to several pages of the manual to correct inconsistencies which have arisen due to prior major changes in other portions of the manual, and changes in the operation of the addressable clock. These and other revisions and additions described opposite the pages to which they apply are listed in the "Summary of Changes" below. Please replace the appropriate pages in your copy of the specifications and add the new pages, as listed, removing the page headed by paragraph 18300.

C. Robert Russell

EWW/CRR/nd

SUMMARY OF CHANGES

Page Headed By Below Numbered Paragraph	
11325	I/O Interrupt Diagram amended to reflect change of storage location for Control Counter and location to which Control Counter is set.
11330	Paragraph 11340 amended to add addressable clock power loss to contingency interrupts.
11350	Paragraph 11351 amended to change "completion" interrupt for card reader to be an "initiation" interrupt, as previously developed for the card punch.
11353 A. II (f)	End of Tape warning procedure changed from reflective spot to procedure (including Error A Bad Spot Interrupt) required by warning window now announced by engineering.
11806	Minor changes to paragraph 11807 specifically restate IA and m' methods for this instruction.
11812	Minor changes to paragraph 11814 to specifically restate m' method for this instruction.
11900	Ninety Column Card Translation Instructions deleted.
11902	Subparagraph "B" now shows indicator for loss of power to Addressable Clock.

Page Headed By Below Numbered Paragraph	
11903	Chart amended to conform with amendment to paragraph 11902.
12000	This paragraph amended to note agreement of signs (except for the stated special case of "divide") after arithmetic operations, and the use of the equal indicator for fixing plus zero in add and subtract.
13120	Paragraph 13130 amended to show that an Extract without field selection will leave the sign of the register unchanged.
14350	Paragraphs 14450 and 14500 clarify interrupt.
14550	Paragraph 14600 clarifies interrupt. Paragraphs 15000 and 15100 amended to clarify that comparison is based upon the binary value of the operand, and that in an algebraic comparison only the sign of the least significant word in a multi-word operand is considered.
15200	Decimal zeros inserted from left on shift right in paragraph 16100.
18000	Paragraph 18210 amended to clarify that a binary zero already in the word will stop the edit.
18300	This entire page specifying 90 column translate instructions is DELETED and should be removed and destroyed.
19051	Contingency Write clarified.
19230	Paragraph 19240 amended to show increased memory access speed from 4.5 μ to 4 μ.
19330	Paragraph 19340 amended to show increased memory access speed from 4.5 μ to 4 μ and automatic translation of 90 column cards.
19500	Paragraph 19520 amended by adding Subparagraph 5 to cover case where typewriter is in off-line condition.
20000	Result of addressing non-existent index register specified.
31001	This chart added to further clarify the detailed Memory-Tape data flow in UNISERVO III compatible mode.
51500	Paragraph 51600 amended to specify automatic translation for 90 column.
71300 (Continued)	This page states the Contingency Interrupt provided for loss of power to the Addressable Clock.
90000 91100 91200 91500 91900	These five pages are the rewritten installation specifications providing for the latest changes in installation requirements.

REMINGTON RAND

INTRA-COMPANY COMMUNICATION

TO: All Holders of Revised Univac III Specifications

FROM: C. R. Russell

CITY & DATE: Phila. - 2-14-61

DEPARTMENT: Product Planning

SUBJECT: Revised and Additional Pages Dated 2-14-61

The accompanying pages cover revisions and additions made since December 9, 1960. They include the recent change in design of the UNISERVO III read/write head to eliminate the bad spot head, and the resultant changes in Bad Spot Control and Error A and Error B interrupt procedure. Four new instructions covering forward and backward contingency reads on UNISERVO III tapes, to be used as explained in connection with Error B interrupts, have been added to the order repertoire. The Card Reader specifications have been rewritten for greater clarity and to incorporate recent changes. These and other revisions and additions described opposite the pages to which they apply are listed in the "Summary of Changes" below. Please replace the appropriate pages in your copy of the specifications and add the new pages, as listed.

C. Robert Russell

EWW/CRR/nd

SUMMARY OF CHANGES

Page Headed By Below Numbered Paragraph	
11353 A. I	Minor change to accord with new Bad Spot procedure.
11353 A. III (b)	These 2 pages replace the former 1 page. Subparagraph
11353 A. III (g)(cont.)	"g" states the specification change for program recovery after Error B interrupt.
11353 B. I	Rewritten for greater clarity.
11353 B. II	Rewritten for greater clarity.
11353 D. I	These four pages replace the two pages formerly
11353 D. II	in the manual under paragraphs 11353 D. I and
11353 D. III	11353 D. II. They also replace paragraph 51400,
11353 D. IV	which is deleted and should be removed.
11901	Instruction Timing Chart changed to delete FBM and BBM and add the four new instructions: FCSR, FCBR, BCSR, and BCBR.
11910	Multiplication Timing.
11911	Division Timing.
14600	Reference to Console Typewriter interrupt indicator deleted.

Page Headed By Below Numbered Paragraph	
19051	Operation Codes for UNISERVO III changed to delete FBM and BBM and add the four new instructions: FCSR, FCBR, BCSR, and BCBR. Specification for operation of Contingency Write changed.
19110	Tape Block Layout on Tape revised.
19150	Forward Contingency Scatter and Block Read Orders, and Backward Contingency Scatter and Block Read Orders, explained in detail in these two new page additions.
19150 (cont.)	
19200	Paragraph 19210 and subparagraph 3 of paragraph 19220 added to specify when a programmed I/O interrupt occurs for the Card Reader.
19230	This and paragraph 19240 changed to delete a single instruction procedure and to add translation for 90 column cards.
19330	Card Punch instruction call time changed from 275^0 to 300^0.
19699	Subparagraph 9 added to provide conformity of UNISERVO II Compatible Tape with UNISERVO III second interrupt procedure.
31100	UNISERVO III Tape Reel Hub specification added and Bad Spot Head specification deleted.
31412	These 2 pages replace the 1 page formerly in the manual for Bad Spot procedure.
31412 (cont.)	
32000	Paragraph 32210 clarifies incrementing of Synchronizer MAC upon transfer of UNIVAC III word by UNISERVO II.
51000	An additional station added to Card Reader track feed diagram.
51300	One card feed button added to Card Reader Control Panel.
51800	Card Reader Timing Chart added to manual.
71000	Paragraph 71300 amended to allow Addressable Clock contents to be read out into ANY one Arithmetic Register.
91500	Voltage tolerances deleted.
91900	Subparagraph 9 adds false floor specification for installation.

#81

REMINGTON RAND

INTRA-COMPANY COMMUNICATION

TO: All Holders of Revised Univac III Specifications

FROM: C. R. Russell

CITY & DATE: Phila. - December 15, 1960

DEPARTMENT: Product Planning

SUBJECT: REVISED AND ADDITIONAL PAGES DATED 12-9-60

The accompanying pages cover revisions and additions made since December 1, 1960. Due to the relatively short interval possible between completion interrupts by the Uniservo synchronizers, the Univac III Product Planning Specification revisions attached provide that a second successful completion (occurring before the interrupt program has progressed to the point of resetting the completion interrupt indicator for the first completion) will not cause the second setting of the completion interrupt indicator until after the first setting of the indicator has been reset. This delay will inhibit further accessing of the synchronizer standby location until such time as the delayed setting of the completion interrupt indicator takes place. This and the other revisions and additions described opposite the pages to which they apply are listed in the "Summary of Changes" below. Please replace the appropriate pages in your copy of the specifications, and add the new pages, as listed.

C. Robert Russell

EWW/CRR/nd
Attachment

SUMMARY OF CHANGES

Page Headed By Below Numbered Paragraph	
11000	Paragraph 11130 revised to state the 4 microsecond machine cycle.
11300	Subparagraph 1 of Paragraph 11320 revised to state for Uniservos (a) the unique setting of the interrupt indicator (b) the inhibition of the second setting of the completion interrupt indicator and (c) the delayed accessing of the standby location until after such second setting of the interrupt indicator is no longer inhibited.
11320	Subparagraph 5 (Continued) Subparagraphs 8 and 9 added.

SUMMARY OF CHANGES (Continued)

Page Headed By Below Numbered Paragraph	
11350	Paragraph 11351 revised to state for Uniservos (a) the unique setting of the interrupt indicator and (b) the inhibition of the second setting of the completion interrupt indicator.
11353	Subparagraph A II f. The End-of-Tape Warning indication procedure has been completely revised to clarify exactly what happens.
11353 A III (Continued).	This page added since the preceding revision of 11353 A II f required more space than originally required when on the same page of the manual with 11353 A III.
11353 E	Subparagraph I revised to state that memory accessing is prevented until after the card punch error condition has been corrected.
11903	This chart consolidating the address specifications set forth in paragraph 11902 is added.
19000	Subparagraph 3. Subparagraph 4 revised to state more exactly when the standby location is reset. Subparagraph 6 added to describe the selection of the Uniservo III (not Uniservo II) Compatible Mode. (This is restated as a note to the Flow of Data Chart at the end of Paragraph 31000 as revised with this letter). Subparagraph 7 added to cross-reference Paragraph 11320.
19051	This paragraph is revised to further clarify the use of the Contingency Write operation.
19320	Subparagraph 8 "Select Stacker 1 Only". Operation codes clarified for both programmed interrupt and non-interrupt.
19330	This paragraph revised to specify the new feature which prevents accessing by the card punch synchronizer of its associated standby location following the setting of error or fault indicators, until after the interrupt program resets the set indicator. The timing limitation for selection of the error stacker and resetting of the error indicator in order to lift the stacker knife prior to the arrival of the check read card is also specified.
31000	The first page of this specification is amended to show the transfer rate of 205,500 decimal digits per second.
31000	Flow of Data Chart. Note 4 added to specify a switch on the servo for the operator to control whether Uniservo III transfers are made in normal Univac III mode or in Uniservo III Compatible Mode.

SUMMARY OF CHANGES (Continued)

Page Headed By Below Numbered Paragraph	
31100	Transfer rate amended to show 205,500 decimal digits per second.
70210	The page headed by the continuation of this paragraph is amended at the top to provide for 5 copies, plus the original.
71000	This page ADDED to provide the specifications for the Univac III Addressable Clock.

Copy # 85

REMINGTON RAND

INTRA-COMPANY COMMUNICATION

TO: All Holders of Revised
Univac III Specifications

FROM: C. R. Russell
Philadelphia
December 2, 1960

DEPARTMENT: Product Planning

SUBJECT: REVISED AND ADDITIONAL PAGES
DATED 12/1/60

The accompanying pages cover revisions and additions made since October 31, 1960. Please replace the appropriate pages in your copy of the specifications with these sheets, and add the new pages as specified below.

B Haslbauch for
C. Robert Russell

CRR:sm
Attachment

SUMMARY OF CHANGES

Pages, Beginning with Paragraph Number:		
11353	BIIa.	Third from last line of subparagraph "a" corrected to show calculation.
11902	D.	This paragraph corrected to emphasize the distinction between the UNISERVO III synchronizers and their associated Tape Control Word Registers.
19500)		These three pages revise the Console Typewriter instruction specifications formerly on the one page headed by 19500.
19530)		
19550)		
31000		UNISERVO III (continued). The chart showing the flow of data between Central Processor and UNSERVO III TAPE through the synchronizer has been revised to facilitate Compatible Mode transfers with other UNIVAC Computers.
70000)		
70210)		
70220 (continued))		These new Console Typewriter specifications are added.
70220 ("))		
70320)		
70400)		
70500)		

Remington Rand

INTRA-COMPANY COMMUNICATION

TO: M. Harper

PERSON OR EPARTMENT:

CARBONS: Systems Programming
Master Distribution
(85)

FROM: K. M. Gellhaus

CITY & DATE: Whitpain 9/15/61

DEPARTMENT: Technical Publications

SUBJECT: Univac III Operator's Notes

Attached is a tabulation of all Univac III controls and indicators relevant to the duties of a system operator. The information is tailored to suit your need for details on the two prototype machines at UEC Whitpain, and is not intended to be entirely factual for production units.

Technical Publications will appreciate any comments the users of this document may care to contribute. Please direct all communication on this matter to J. Frank, department 110.

K. M. Gellhaus

/dd

Att.

CONTENTS

Table 1. Operator's Console Model 124 Control Panel

Component type is abbreviated as follows:

S - Switch only,
L - Indicator (lamp) only, and
S/L - Combined switch and indicator.

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
None		Key	When locked in off position, prevents use of any system controls.
AC ON / AC OFF	Red / Green	S/L	When key switch is on, turns on or turns off system power. Red half (AC ON) lights when a-c contactors are closed; green half (AC OFF) lights when a-c contactors are open.
READY	Green	L	Indicator lights when all voltages are at operating levels.
CLEAR	White	S	De-energizes clear relay for 0.5 sec to perform general clear of processor and memory control circuits. Resets the following flip-flops (FF's):* Computer Error FF's Contingency FF's Input-Output Interrupt FF's Standby Location Interlock FF's Input-Output Error FF's Input-Output Fault FF's Inhibit Input-Output Interrupt FF's Comparison FF's Arithmetic-Register (AR) Sign FF's Sense FF's Clears to binary zeros the following registers:* Index Register (IR) Memory-Address Counters (MAC) Control Counter (CC) Memory-Address Register (MAR) Instruction Register

* Subject to change. Check with engineering staff for latest information.

Table 1. Operator's Console Model 124 Control Panel (cont)

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
LOAD	White	S/L	Switch causes logical Uniservo 0 to read forward one block. Indicator lights if information on tape was not written correctly.
REWIND	White	S/L	Indicator lights when information on tape on logical Uniservo 0 is read incorrectly during a load operation. Switch causes logical Uniservo 0 to rewind tape without interlock.
KEYBOARD ACTIVE	White	L	Keyboard may be used to type in information. Keyboard is active as a result of an ACT (66) instruction, or when typewriter is off line.
RUN	Green	S/L	Switch starts processor. Indicator is lighted while processor is running.
PREVENT I/O INTERRUPT	Blue	L	Indicator is lighted when Input-Output Interrupt Inhibit FF is set by PIO (62) instruction.
TYPEWRITER ON LINE TYPEWRITER OFF LINE	White Blue	S/L	If typewriter is off line, pressing switch places typewriter in on-line status; if typewriter is on line, pressing switch places typewriter in off-line status. Indicator shows status of typewriter.

Table 1. Operator's Console Model 124 Control Panel (cont)

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
PROC ERROR STOP PROGRAM STOP	Red	S/L	PROC ERROR STOP indicator lights when processor stops because of a processor error (second error). Pressing the switch sets the Contingency Stop FF to cause a program interrupt. The interrupt test transfers control to a routine that contains a WAIT (77) instruction. Execution of the WAIT instruction stops the processor. PROGRAM STOP indicator lights when processor executes WAIT instruction and stops.

Table 2. Uniservo III Magnetic Tape Unit Model 126 Control Panel

Component type is abbreviated as follows:

S - Switch only,
L - Indicator (lamp) only, and
S/L - Combined switch and indicator.

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
WRITE	Yellow	L	Not used.
READ	Green	L	Not used.
INHIBIT WRITE	Yellow	L	Lights when tape reel on Uniservo contains reel-safety ring.
FORWARD	Green	S/L	Pressing switch sets Uniservo for forward operation. Indicator lights when Uniservo is set for forward operation, or is running forward.
BACKWARD	Yellow	S/L	Pressing switch sets Uniservo for backward operation. Indicator lights when Uniservo is set for backward operation, or is running backward.
REWIND	Red	S/L	When servo is set for backward operation, pressing switch starts rewind operation, with interlock against further system-controlled operation. (Lights CHANGE TAPE indicator.) Indicator lights when rewind operation is in progress.

Table 2. Uniservo III Magnetic Tape Unit Model 126 Control Panel (cont)

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
CHANGE TAPE	Red	S/L	Pressing switch removes rewind interlock and, if door is closed, advances tape to load point. Indicator lights when rewind interlock is in effect; operator intervention required to return servo to system control.
LOAD POINT	Green	L	Lights when tape is in first-block position.
AIR FLOW	Red	L	Lights when airflow failure has occurred. D-c power is off.
OVERHEAT	Red	L	OVERHEAT indicator lights when cabinet temperature has exceeded 120°F. D-c power is off.
VOLTAGE	Green		VOLTAGE indicator lights when a circuit breaker in the Uniservo is open.
ON	Green	S/L	Pressing switch starts power turn-on sequence in Uniservo. Indicator lights when power turn-on sequence is complete; Uniservo is ready to operate.
OFF	Red	S/L	Pressing switch turns off d-c power in Uniservo. Indicator lights when a-c power is on and d-c power is off.

Table 3. Uniservo II Magnetic Tape Unit Model 72 Control Panel

Component type is abbreviated as follows:

S - Switch only,
L - Indicator (lamp) only, and
S/L - Combined switch and indicator.

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
WRITE	Yellow	L	Lights during write operation.
READ	Green	L	Lights during read operation.
INHIBIT WRITE	Yellow	L	Function identical with counterpart on Uniservo III Model 126. Refer to table 2.
FORWARD	Green	S/L	
BACKWARD	Yellow	S/L	

Table 3. Uniservo II Magnetic Tape Unit Model 72 Control Panel (cont)

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
REWIND	Red	S/L	Function identical with counterpart on Uniservo III Model 126. Refer to table 2.
CHANGE TAPE	Red	S/L	
METAL	Green	L	Lights when tape-selector switch is set for metal tape.
PLASTIC	White	L	Lights when tape-selector switch is set for plastic tape.
AIR FLOW	Red	L	Lights when airflow failure has occurred. Servo is off.
OVERHEAT	Red	L	Lights when temperature in servo cabinet has exceeded 120°F. Servo is off.

Table 3. Uniservo II Magnetic Tape Unit Model 72 Control Panel (cont)

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
ON	Green	S/L	Function same as counterpart on Uniservo III Model 126. Refer to table 2.
OFF	Red	S/L	

Table 4. High-Speed Card Reader Model 133 Control Panel

NOTE: On the prototype readers, the markings shown in this table as pushbutton markings appear on the reader control panel, not on the pushbuttons.

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
UNIT	Yellow	S/L	Pressing switch logically disconnects reader from system control. Indicator lights when reader is 'off line' (not under system control).
CLEAR	Red	S/L	Indicator lights when fault occurs. Pressing switch clears error FF's associated with reader.
ONE CARD	Green	S	Pressing switch causes reader to feed one card. Switch can be used to perform initial load operation from reader when memory is clear.
D. C.	Green	S/L	Pressing switch turns on or turns off d-c power.* Indicator lights when d-c power is on.
MOTOR	Green	S/L	Pressing switch turns on or turns off drive motor. (Has no effect unless d-c power is on.) Indicator is lighted when drive motor is running.

* Turning off d-c power, either manually or as the result of a fault, also turns off the drive motor.

Table 4. High-Speed Card Reader Model 133 Control Panel (cont)

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
(R) SYNCHRONIZER (Y)	Red and Yellow	L	Red half of indicator lights to show that airflow failure has occurred. D-c power is off. Yellow half of indicator lights to show that synchronizer temperature has exceeded 120°F. D-c power is off.
DOOR	Yellow	L	Lights when a door is open. D-c power is off.
(R) STACKER (Y)	Red and Yellow	L	Red half lights to indicate a card jam at stacker. Drive motor is off. Yellow half lights to show that a stacker is full. Next card feed is inhibited.
FEED	Red	L	Lights when a card-feed jam or a registration error occurs at a read station. Drive motor is off.
MAGAZINE	Red	L	Lights when feed hopper is empty or a misfeed occurs. Next card feed is inhibited and drive motor is off.

Table 5. High-Speed Printer Model 125 Control Panel

Component type is abbreviated as follows:

S - Switch only,
L - Indicator (lamp) only, and
S/L - Combined switch and indicator.

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
SPACE PAPER	White	S	Advances paper one space each time operator presses and releases switch.
OUT RUNAWAY	Red	L	OUT indicator lights when end of paper is four inches below print station (out of paper, or paper torn). RUNAWAY indicator lights when fast feed continues for more than two seconds.
FEED PAPER	White	S	Pressing switch causes paper to feed in one-line steps as long as switch is held.
IN	Green	S	Pressing switch moves carriage toward printing position. To place carriage in printing position, operator must hold switch until carriage stops.
OUT	Red	S/L	Pressing switch moves carriage away from printing position. To move carriage to servicing position, operator must hold switch until carriage stops. Indicator lights when carriage is not in printing position.

Table 5. High-Speed Printer Model 125 Control Panel (cont)

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
ABNORMAL CLEAR	Red	S/L	Indicator lights when any abnormal condition occurs. Pressing switch clears error FF's associated with printer, and clears MDL loops.
MANUAL PRINT	White	S/L	Pressing switch causes printer to print continously, in all printing positions, the character set up on test panel. Pressing switch a second time stops the manual print operation. Indicator lights during print operation. NOTE: Printer must be off line.
OFF LINE	Blue	S/L	Pressing switch logically disconnects printer from system control. Pressing switch a second time returns printer to system control. Indicator lights when printer is off line.
CHANGE	Yellow	S/L	Pressing switch once bypasses automatic ribbon-reverse circuits, sets ribbon drive to wind ribbon onto bottom roll when manual ribbon-feed switch is held in either position, lights indicator. (Carriage must be out.) Pressing switch a second time restores ribbon-control circuits to normal operation, extinguishes indicator.
OUT	White	L	Indicator lights when printer is out of ribbon, or ribbon is torn.

Table 5. High-Speed Printer Model 125 Control Panel (cont)

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
SYNC OVERHEAT	Red	L	Indicator lights when temperature in synchronizer has exceeded 135°F, or when airflow failure has occurred in synchronizer. D-c power is off.
PRINTER OVERHEAT	Red	L	Indicator lights when temperature in printer has exceeded 135°F, or when airflow failure has occurred in printer. D-c power is off.
INTERLOCK	Yellow	L	Indicator lights when a printer or synchronizer door is open. D-c power is off.
MOTOR ON	Green	S/L	Pressing switch turns on or turns off printer motors, except blowers.* Indicator lights when printer motors are on.
(R) (G) (No Marking)	Red and Green	S/L	Pressing switch turns on or turns off printer power. Red half of indicator lights when operator presses switch, remains on until d-c power comes on. Green half of indicator lights when all power is on, all operating conditions normal. Both halves of indicator light when fault occurs; red half remains on until operator presses switch, green half remains on as long as d-c power remains on.

* Blowers start when system power is turned on.

Table 6. Summary Card Punch Model 127 Control Panel

Component type is abbreviated as follows:

S - Switch only,
L - Indicator (lamp) only, and
S/L - Combined switch and indicator.

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
OVERHEAT / AIR FLOW	Red	L	OVERHEAT indicator lights when synchronizer temperature has exceeded 135°F. D-c power is off. AIRFLOW indicator lights when airflow in synchronizer has failed or is insufficient. D-c power is off.
CHIP BOX	Yellow	L	Lights when chip box is full or not in place.
STACK FULL	Yellow	L	Lights when a stacker is full.
FEED JAM / STACK JAM	Red	L	FEED JAM indicator lights when card jam occurs between input hopper and stacker. Drive motor is off. STACK JAM indicator lights when card jam occurs at either stacker. Drive motor is off.
EMPTY INPUT	Yellow	L	Lights when input hopper is empty.

Table 6. Summary Card Punch Model 127 Control Panel (cont)

Pushbutton or Indicator			Function or Indication
Marking	Color	Type	
INTERLOCK	Yellow	L	Lights when a cabinet door is open. D-c power and the drive motor are off.
D C ON	Green	S/L	Pressing switch turns on or turns off d-c power. Indicator is lighted when d-c power is on.
MOTOR ON	Green	S/L	Pressing switch once places motor-control circuits under system control and lights indicator. Pressing switch a second time disconnects motor-control circuits from system control and extinguishes indicator.
ONE CARD	White	S	Pressing switch causes punch to feed one card.
OFF-LINE	Blue	S/L	Pressing switch logically disconnects punch from system control. Pressing switch a second time returns punch to system control. Indicator lights when punch is 'off line' (not under system control).
ABNORMAL CLEAR	Red	S/L	Indicator lights when abnormal condition occurs. Pressing switch clears unit.

Table 7. Engineer's Maintenance Panel, Processor Assembly Model 134[1]

Component		Function or Indication
Marking	Number and Type	
	MEMORY INFORMATION	
1...27	27 Lamps	Display information in display registers.
28	Lamp	Displays memory address check bit.
	WRITE MEMORY INFORMATION[2]	
1 OFF 0 (1...27)	27 2-position toggle switches	Select bit to be written into the corresponding bit position (1...27) of a memory address. Requires use of MEMORY ADDRESS and MEMORY WRITE switches.
SELECT ON--OFF	2-position toggle switch	Placing switch in ON position enables WRITE MEMORY INFORMATION switches 1...27.
	MEMORY ADDRESS[2]	
1 0	2-position toggle switch	Setting switches selects a memory address. Used with WRITE MEMORY INFORMATION switches, MEMORY WRITE switch, MEMORY READ switch, or INSTRUCTION REGISTER switches. NOTE: Leftmost switch (bit 16) not used.
SELECT ON--OFF	2-position toggle switch	ON position enables 15 MEMORY ADDRESS switches.

[1] Normally mounted in cabinet of Power Control Section Model 137.

[2] PROCESSOR STATUS switch must be in TEST position.

Table 7. Engineer's Maintenance Panel, Processor Assembly Model 134[1] (cont)

Component		Function or Indication
Marking	Number and Type	
		INSTRUCTION REGISTER Display bit contents of instruction register as follows:
AR	4 Lamps	Four AR lamps show bits 11...14 (arithmetic register code).
OPR	6 Lamps	Six OPR lamps show bits 15...20 (operation code).
IR	4 Lamps	Four IR lamps show bits 21...24 (index register code).
		Setting switches jams selected bit into corresponding bit position of instruction register as follows (right to left):
AR	4 3-position toggle switch	Four AR switches control bits 11...14.
OPR	6 3-position toggle switch	Six OPR switches control bits 15...20.
IR	4 3-position toggle switch	Four IR switches control bits 21...25.
		Instruction register SELECT switch (left-hand end of INSTRUCTION REGISTER group) must be in ON position.
SELECT ON--OFF	2-position toggle switch[2]	ON position enables 14 INSTRUCTION REGISTER switches.

[1] Normally mounted in cabinet of Power Control Section Model 137.

[2] PROCESSOR STATUS switch must be in TEST position.

Table 7. Engineer's Maintenance Panel, Processor Assembly Model 134[1] (cont)

Component		Function or Indication
Marking	Number and Type	
	MEMORY[2]	
READ	Pushbutton	Pressing pushbutton causes processor to read contents of address selected by MEMORY ADDRESS switches, and display on MEMORY INFORMATION lamps.
WRITE	Pushbutton	Pressing pushbutton causes processor to write information from WRITE MEMORY INFORMATION switches into address selected by MEMORY ADDRESS switches.
	PROCESSOR STATUS	
TEST NORMAL	2-position toggle switch	TEST position logically disables control console RUN switch, lights the processor fault indicator on the console monitor board, and enables the following controls on the engineer's panel: Write-memory-information SELECT switch, Memory-address SELECT switch, Memory READ switch, Memory WRITE switch, Instruction-register SELECT switch, OPERATION group controls, and INTERRUPT CONTROL switches. NORMAL position disables controls enabled in TEST position.

[1] Normally mounted in cabinet of Power Control Section Model 137.

[2] PROCESSOR STATUS switch must be in TEST position.

Table 7. Engineer's Maintenance Panel, Processor Assembly Model 134[1] (cont)

Component		Function or Indication
Marking	Number and Type	
	OPERATION[2]	
CONTINUOUS STEP AUTOMATIC	3-position toggle switch	When switch is in CONTINUOUS position, processor executes instructions at normal program rate. When switch is in STEP position, processor executes one instruction each time operator presses RUN pushbutton. When switch is in AUTOMATIC position, processor executes instructions at a rate determined by the setting of the RATE control.
RATE	Potentiometer	When CONTINUOUS-STEP-AUTOMATIC switch is in AUTOMATIC position, RATE control enables operator to vary instruction rate continuously between ten per second and one per two seconds.
(Not used) OFF RETAIN CC	3-position toggle switch	Placing switch in RETAIN CC position causes processor to retain contents of control counter.
SKIP OFF TEST IND	3-position toggle switch	Placing switch in SKIP position causes processor to execute consecutive skip instructions. (Jams zeros into instruction register.) Placing switch in TEST IND position tests panel-lamp drivers for ability to turn off lamps. All panel lamps should turn off.

[1] Normally mounted in cabinet of Power Control Section Model 137.

[2] PROCESSOR STATUS switch must be in TEST position.

Table 7. Engineer's Maintenance Panel, Processor Assembly Model 134[1] (cont)

Component		Function or Indication
Marking	Number and Type	
	PROGRAM	
CLASS I STOP	Lamp	When lighted, indicates that processor has stopped on second machine error.
STOP	Lamp	When lighted, indicates that central processor is stopped.
RUN	Pushbutton	Pressing switch starts processor.
STOP	Pushbutton	Pressing switch stops processor.
	DISPLAY SELECTOR	
0...16	19-position rotary switch	Selects information read from memory for display on memory information indicators as follows: 0 - Program selects information. 1 - Display all instructions. 2 - Display all operands. 3 - Display servo III sync A information. 4 - Display servo III sync B information. 5 - Display G-P channel 1 information. . . . 12 - Display G-P channel 8 information. 13 - Display servo II sync information. 14 - Display servo III sync C information. 15 - Display servo III sync D information. 16 - Spare

[1] Normally mounted in cabinet of Power Control Section Model 137.

[2] PROCESSOR STATUS switch must be in TEST position.

Table 7. Engineer's Maintenance Panel, Processor Assembly Model 134[1] (cont)

Component		Function or Indication
Marking	Number and Type	
	DISPLAY SELECTOR (cont)	
SYNC INST ONLY	2-position toggle switch	When actuated, switch causes processor to display only instructions for synchronizer selected by display-selector rotary switch.
	CLEAR	
MASTER MACHINE	Pushbutton	When actuated, switch starts system-clear operation. Duplicates function of CLEAR switch on operator's console. Refer to table 1. NOTE: Details of function not final. Consult engineering staff for latest information.
CENTRAL PROCESSOR	Pushbutton	Details of function not final. Consult engineering staff for lates information.
IR-MAC I	Pushbutton	
INTERRUPT FF	Pushbutton	When actuated, switch clears interrupt FF's (all classes).
SENSE FF	Pushbutton	When actuated, switch resets all sense FF's.

[1] Normally mounted in cabinet of Power Control Section Model 137.

Table 7. Engineer's Maintenance Panel, Processor Assembly Model 134[1] (cont)

Component		Function or Indication
Marking	Number and Type	
	INTERRUPT CONTROL	
CLASS I (II, III)		
STOP	3-position toggle switches	STOP position causes processor to stop when interrupt occurs in selected class.
NORM		NORM position causes program to follow normal interrupt routine for selected class.
IGNORE		IGNORE position causes processor to ignore interrupt in selected class.
INTERRUPT INHIBIT	Lamp	Lights when Inhibit-I/O-Interrupt FF is set.
	TAPE CONTROL	
LOAD	Pushbutton	Pressing switch causes logical servo 0 to read forward one block.
REWIND	Pushbutton	Pressing switch causes logical servo 0 to rewind without interlock.
	CLOCK	
TOL	Lamp	Lights when central processor clock fails for one or more pulses, or is out of tolerance. System is stopped.

[1] Normally mounted in cabinet of Power Control Section Model 137.