Univac®

LARC PROCESSOR

MAGNETIC TAPE SYNCHRONIZER SYSTEM

Remington Rand Univac®
DIVISION OF SPERRY RAND CORPORATION
UNIVAC ENGINEERING CENTER • PHILADELPHIA

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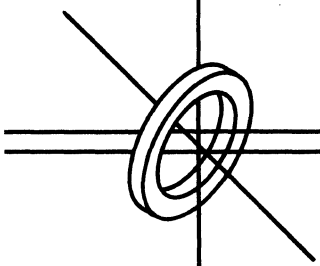

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JULY 1961

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INTRODUCTION

1-1. PURPOSE AND SCOPE OF MANUAL

This manual provides training and reference information covering the theory of operation of the logic circuits in the Processor Magnetic Tape Synchronizer System in the Univac® Larc* Computing System. It is intended to apply to a basic Larc tape system as well as to a partially or fully expanded system. The manual does not aim to describe physical characteristics of the tape system or detailed circuit operation of basic logic elements such as gates, delay flops, and pulseformers. Information on the physical characteristics of the system is found in the publication, Univac Larc System Maintenance, Introduction and Physical Description. A detailed treatment of the properties of the various logic and circuit elements used in the Tape Synchronizer System is found in the manual, Univac Larc Circuitry.

The Tape Synchronizer System controls the model 69 Uniservo* II magnetic tape unit. To understand the operation of the tape synchronizer it is necessary to have a good working knowledge of how the magnetic tape unit operates. The required background information may be obtained by reference to sections 1 and 2 of the manual, Univac Larc Uniservo Magnetic Tape Unit, Model 69 - Description and Maintenance.

In carrying out tape operations, the processor program integrates and supervises the operation of the Tape Synchronizer System. Although control by the program is described in this manual in order to supplement the description of the circuits in the Tape Synchronizer System, a more comprehensive discussion of program control, together with a list of processor instructions, is provided in the manual, Univac Larc Programming, the Processor.

Not every detail of the Tape Synchronizer System is described in this manual; however, enough background information is provided to enable the reader to track down details on the relevant engineering drawings which completely define the logic of the Tape Synchronizer System.

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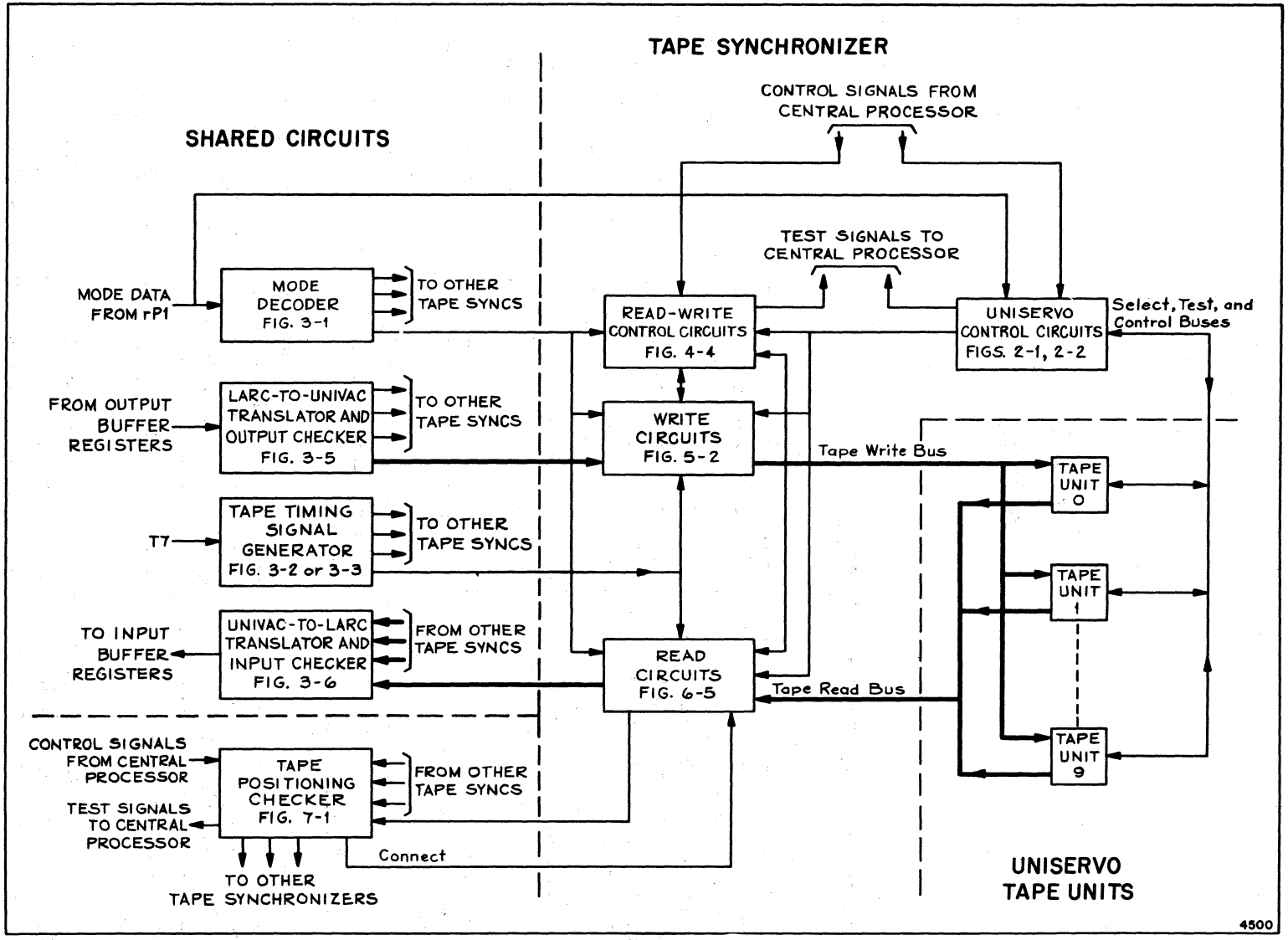


Figure 1-1. Magnetic Tape Synchronizer System, Block Diagram

1-2. ORGANIZATION OF THE TAPE SYNCHRONIZER SYSTEM

There may be as many as four synchronizers in a Larc magnetic tape system; these synchronizers are numbered 7, 8, 9, and 10. Synchronizers 7 and 8 are included in a basic Larc system. Each tape synchronizer may control up to ten Uniservo tape units. Each tape synchronizer divides functionally into four more-or-less independent sections (figure 1-1) as follows: (1) Uniservo control circuits, (2) read-write control circuits, (3) read circuits, and (4) write circuits. Synchronizer 7 differs slightly from the others in that it is associated with a group of initial-read circuits which, although used during maintenance and test periods, are not involved in the normal operation of the Tape Synchronizer System.

In addition to the tape synchronizers, the Larc processor contains a tape positioning checker (that may be connected to the read circuits of any tape synchronizer) and a number of circuits that are shared in common by all of the tape synchronizers in the system. (See figure 1-1.) The tape positioning checker and the shared circuits are included in any system, basic or expanded. The complement of equipment associated with the Tape Synchronizer System is listed in table 1-1.

Table 1-1. Complement of Equipment in Tape System

Equipment	Number
Tape Read-Write Synchronizers	2 to 4
Circuits Shared by all Tape Synchronizers	
Mode Decoder	1
Timing Signal Generator	1
Univac-to-Larc Translator and Input Checker	1
Larc-to-Univac Translator and Output Checker	1
Tape Positioning Checker (connects to any tape synchronizer)	1
Tape Buffer Registers in Dispatcher	Two input and 2 output registers per synchronizer
Uniservo Remote Control Panel	One per 2 synchronizers with one plugboard for each synchronizer
Initial-Read Circuits	One for Synchronizer 7 only
Uniservo II Tape Unit, Model 69	Two to 10 per synchronizer
Uniservo Power Supply Cabinet	One per each 10 Uniservo tape units

The organization of this manual reflects the functional organization of the Tape Synchronizer System. Sections 2 through 7 describe the major functional subdivisions of the synchronizer system. The appendix contains

a description of the initial-read circuits (associated only with Synchronizer 7) which are not involved in the normal synchronizer system operation.

The descriptions and illustrations in sections 2, 4, 5, and 6 are based on Synchronizer 7; they are, however, applicable to the other three synchronizers. except as follows:

(1) Minor differences exist between the logic circuits of Synchronizer 7 and the other three tape synchronizers. The differences are few, however, and unless noted otherwise the description of Synchronizer 7 applies to the other three synchronizers.

(2) Signals generated by Synchronizer 7 are prefixed by S7; the corresponding signals in Synchronizers 8, 9, and 10 are prefixed by S8, S9, and S10, respectively. For example, a word-end signal designated S7WEND originates in Synchronizer 7, and S8WEND in Synchronizer 8. Similarly, signals from the Uniservo tape units controlled by Synchronizer 7 are prefixed by U7, whereas the corresponding signals in Synchronizers 8, 9, and 10 are prefixed by U8, U9, and U10, respectively. Signals from the engineer's control console are prefixed with ES7 for Synchronizer 7, and ES8, ES9, and ES10 for Synchronizers 8, 9, and 10, respectively. Tape-synchronizer-select signals from the central processor are designated PST1 for Synchronizer 7, and PST2, PST3, and PST4, for Synchronizers 8, 9, and 10, respectively. Similarly, connect signals from the tape positioning checker are designated SCT1 for Synchronizer 7, and SCT2, SCT3, and SCT4 for Synchronizers 8, 9, and 10, respectively.

(3) Synchronizer 7 contains several signals not found in the other three tape synchronizers. These signals are PNTP, PNTRU, and PNTRM, generated by the initial-read circuits. Although these signals are shown on the simplified diagrams illustrating the logical operation of Synchronizer 7 they are otherwise ignored except in the discussion of the initial-read circuits in the appendix to the manual. The signals do not affect the normal operation of Synchronizer 7, discussed in the body of the manual.

1-3. TAPE COMPATIBILITY FEATURES

The Univac Larc Tape Synchronizer System can record magnetic tapes for use as input to other Univac computing systems and to off-line Univac output and output-conversion equipment. It can also read magnetic tapes prepared by other Univac computing systems and by off-line Univac input and input-conversion equipment. To achieve compatibility the following features are provided for in the Larc tape system.

1-4. PLASTIC AND METAL TAPE

Each tape synchronizer and Uniservo tape unit can read or record on either plastic or metal tapes.

1-5. CODE TRANSLATION

All data on the magnetic tapes used with the Larc system is recorded in standard seven-bit Univac code consisting of one check bit, two zone bits, and four XS-3 bits. Eight bits, consisting of the seven bits representing a character and one sprocket bit, are recorded in parallel on the tape in standard order. Characters are recorded serially. All input data read from tape into the Larc memory is automatically translated from Univac code into either Larc one-digit numeric code or Larc two-digit alphanumeric code by a built-in translator in the Tape Synchronizer System. All output data is automatically translated from Larc one-digit numeric or Larc two-digit alphanumeric code into Univac code before it is wrtten on magnetic tape.

1-6. DATA BLOCK LENGTHS

Each tape synchronizer can read or record standard 720-character Univac data blocks or blocks that are any multiple of 120 characters in length. The Univac blocks that are read may or may not be divided into 120-character "blockettes".

1-7. PULSE DENSITIES

A wide range of pulse densities, from 20 to 250 pulses per inch, can be read by the Tape Synchronizer System. The Larc System, Serial 1 Tape Synchronizer System can write either 104 or 208 pulses per inch; the Larc System, Serial 2 Tape Synchronizer System can write either 125 or 250 pulses per inch.

1-8. SPACE BETWEEN BLOCKS

The Tape Synchronizer System can read or record tapes with either a 1.0-inch or 2.4-inch space between blocks.

1-9. BASIC OPERATIONS

The Tape Synchronizer System, under supervision of the processor program, controls five basic operations; these are read, check-read, write, rewind, and rewind-with-interlock. A read or check-read operation can be performed in either a forward or backward direction. There are variations of the read, check-read, and write operations depending upon the pulse density, size of space between blocks, translation mode, etc., specified by the program. (Refer to table 1-2.)

1-10. READ OPERATION

During a tape-read operation, data is read (a character at a time) from tape and is sent to consecutive memory locations (a word at a time) by way of the dispatcher. As the characters are processed, they are translated from Univac to Larc code, and parity, count, and other checks are

Table 1-2. Tape System Characteristics

Tape Read/Write Speed	100 inches per second
Tape Rewind Speed	100 inches per second
Recording Density	
Larc System, Serial 1	104 or 208 characters per inch
Larc System, Serial 2	125 or 250 characters per inch
Reading Density	20 to 250 characters per inch
Recording Rate	
Larc System, Serial 1	10,400 or 20,800 characters per second
Larc System, Serial 2	12,500 or 25,000 characters per second
Reading Rate	2000 to 25,000 characters per second
Tape Stop or Tape Start Time	5 milliseconds (maximum)
Tape Reversal Delay	800 milliseconds
Read Start Delay from Rewound State	1 second
Write Start Delay from Rewound State	1.6 seconds
Tape Recording Method	Return-to-zero, bit parallel, character serial
Number of Tape Tracks	8
Tape Base	Metal or plastic
Tape Reel Sizes	
Metal	6 or 8 inches
Plastic	6, 8, or 10-1/2 inches
Usable Tape on an 8-inch Reel	
Metal	1500 feet (minimum)
Plastic	2400 feet (minimum)
Tape Width	0.5 inch
Block Length	Any multiple of 120 characters
Space Between Blocks	1.0 inch or 2.4 inches
Direction of Read	Forward or backward
Direction of Write	Forward only

performed. When 120 (Univac) characters have been read and processed, the tape synchronizer alerts the processor program by setting a ten-word flip-flop. The processor program initiates the read operation and exercises over-all control of the operation by monitoring the ten-word flip-flop by way of the master input-output priority tests.

1-11. CHECK-READ OPERATION

A check-read operation is similar to a read operation except that the data read from tape is not sent to the memory. A check-read operation is performed to ensure that data recorded on tape is readable and error-free, to position the tape in preparation for reading or recording a particular block of data, or to simultaneously check the data and position the tape. The processor program keeps track of the tape position by monitoring the ten-word flip-flop.

1-12. WRITE OPERATION

During a write operation, data is transferred from the memory a word at a time by way of the dispatcher and is recorded on tape a character at a time. In the process, the data is translated from Larc to Univac code. As with the read operation, the program exercises over-all control of the write operation by monitoring the ten-word flip-flop by way of the master input-output priority test.

1-13. REWIND OPERATIONS

A rewind operation differs from other operations in that once it is started on the Uniservo tape unit, it continues to completion independent of control by the program or the tape synchronizer. Consequently, the tape synchronizer circuits that select and control the Uniservo tape unit, are then free to begin an operation on another tape unit. A tape can be rewound either with or without interlock. A Uniservo tape unit that performs a rewind with interlock is unavailable until the operator releases the tape unit, normally when the tape reel is changed.

1-14. SIMULTANEOUS OPERATIONS

Only one read, check-read, or write operation at a time can be controlled by a single tape synchronizer, with one exception. The exception is that in which the tape positioning checker is connected to the read circuits of a tape synchronizer to control a check-read operation simultaneously with a write operation being controlled by the same synchronizer. If the check-read operation is performed by a tape synchronizer without the aid of the tape positioning checker, the synchronizer cannot simultaneously perform a write (or read) operation. While a read or write operation is being performed by a tape synchronizer on one Uniservo tape unit, a rewind operation can proceed simultaneously on any one or all of the remaining tape units controlled by the same synchronizer. The tape synchronizers are essentially independent of one another and one can always perform its operations simultaneously with another.

1-15. TAPE SYNCHRONIZER

Each tape synchronizer (figure 1-1) divides functionally into the following more-or-less independent sections: Uniservo control circuits, read-write control circuits, read circuits, and write circuits.

1-16. UNISERVO CONTROL CIRCUITS

The Uniservo control circuits are a relatively self-contained group of circuits used by the processor program at the beginning of a tape operation to select a Uniservo tape unit, test its condition, prepare it for the operation, and start the tape moving. Once the tape is in motion on the selected Uniservo tape unit, the Uniservo control circuits are available for use in selecting and preparing another Uniservo tape unit for an operation. If the operation initiated through the Uniservo control circuits is a rewind or rewind-with-interlock operation, no further control by the synchronizer or program is required. If the operation initiated is a read, check-read, or write operation, responsibility for controlling the operation and processing the data is shifted to other sections of the tape synchronizer system.

1-17. READ-WRITE CONTROL CIRCUITS

The read-write control circuits are active during a write operation, a read operation, or a check-read operation that is performed without using the tape positioning checker. Only one read or write operation at a time can be controlled by the circuits, never both. The essential functions of these circuits are to count characters and words as they are read or written, to request the dispatcher to transfer data words to or from the memory, and to communicate with the processor program on the status of the read or write operation. When the tape positioning checker is used for a check-read operation it takes over the functions of counting data and communicating with the program, thereby leaving the read-write control circuits available to the program for controlling a write operation.

1-18. READ CIRCUITS

The read circuits are active only during a read or check-read operation. During a read operation they always function in conjunction with the read-write control circuits. During a check-read operation they function in conjunction with either the read-write control circuits or the tape positioning checker. The read circuits receive and synchronize input data read from tape and perform other functions associated with a read operation.

1-19. WRITE CIRCUITS

The write circuits are active only during a write operation. They always function in conjunction with the read-write control circuits. The write circuits drive the read-write heads in a Uniservo tape unit at the proper frequency for the specified pulse density, insert the specified spaces between blocks, and perform other functions associated with a write operation.

1-20. TAPE POSITIONING CHECKER

The tape positioning checker consists of a group of circuits that may be connected to the read circuits of any one of the tape synchronizers to perform a check-read operation for the purpose of positioning a tape and checking the data recorded on the tape. The tape positioning checker, however, cannot be used to check-read tapes prepared on the Univac I computing system; such tapes must be read using the read-write control circuits. When connected to a synchronizer, the tape positioning checker does not tie up the synchronizer read-write control circuits but leaves them available for performing a write operation. The tape positioning checker contains circuits for making connections to any tape synchronizer, for counting the data as it is read, and for communicating with the program on the status of the check-read operation.

1-21. SHARED CIRCUITS

The shared circuits perform functions or provide control for all of the four possible tape synchronizers in a system. The circuits consist of a timing signal generator, a Univac-to-Larc translator and input checker, a Larc-to-Univac translator and output checker, and a mode decoder.

1-22. TIMING SIGNAL GENERATOR

The timing signal generator generates special timing signals for controlling and coordinating the digit-read and digit-write cycles of the tape synchronizers to ensure proper time sharing among the synchronizers of the Univac-to-Larc and Larc-to-Univac translators. It also provides timing control for clearing the output buffer registers of a tape synchronizer at the beginning of a write operation and generates sprocket pulses that control the tape writing density. There are two versions of the tape timing signal generator; one is designed for the Larc System, Serial 1, which has tape writing densities of 104 and 208 pulses per inch, and the other is designed for the Larc System, Serial 2, which has tape writing densities of 125 and 250 pulses per inch. Both versions of the timing signal generator are described in section 3 of this manual.

1-23. UNIVAC-TO-LARC TRANSLATOR AND INPUT CHECKER

The Univac-to-Larc translator is time-shared to translate input data, read from tape, for all of the tape synchronizers in the system. All data recorded on tape is in the form of Univac seven-bit, XS-3 code. The translator translates the data into either Larc one-digit numeric code or two-digit alphanumeric code. An input checker associated with the translator checks the input data for parity errors during a read or check-read operation. When the input data is being translated into Larc one-digit numeric code the checker also checks for untranslatable Univac code combinations. The parity checker functions during a check-read operation whether the operation is controlled by the read-write control circuits of a synchronizer or by the tape positioning checker.

1-24. LARC-TO-UNIVAC TRANSLATOR AND OUTPUT CHECKER

The Larc-to-Univac translator is time-shared to translate output data, recorded on tape, for all of the tape synchronizers in the system. The data is translated from Larc one-digit numeric code or two-digit alphanumeric code into Univac seven-bit code. The output of the translator is checked by an associated parity checker.

1-25. MODE DECODER

The mode decoder merely consists of a number of gates that decode, for all of the tape synchronizers, mode data that is preloaded into rP1 by the processor program. The decoded mode data is gated to a particular synchronizer by processor instruction 66.

1-26. PROGRAM CONTROL

Control of tape operations is divided between the processor program and the Tape Synchronizer System. In general, routine functions repetitive in nature or limited in scope such as decoding, reading, writing, synchronizing, translating, and counting are built into the Tape Synchronizer System. Supervisory functions that must be carried out with flexibility are assigned to the program. Functions performed by the program usually involve specifying a choice among several possibilities such as the type of operation to be performed, Uniservo tape unit to be selected, memory area to be used, whether to start or delay an operation, and whether to continue or end an operation.

The processor program bases its actions on information supplied to it (usually by a computing unit program in the form of summary orders) and on tests that it performs to determine the condition of tape operations or the state of the equipment or circuits in the tape system. The tape synchronizers and the tape positioning checker base their actions chiefly on information and control supplied by the processor program.

The focal point of any processor program is the master input-output priority test; that is, a 99 instruction of the form 99 xx0xx MMMMM. All routines within the processor program are designed to transfer control to the master input-output priority test instruction within a limited period of time after the test was last performed. This is done so that the program may properly monitor and maintain real-time control over the various synchronizers and input-output devices operating in parallel. If a synchronizer or input-output device completes a task that was previously ordered or triggered by the program, it sets a flip-flop that causes the master input-output priority test to transfer control. The program is then directed through a series of tests of diminishing priority to a routine which attends to any requirements for further instruction by the synchronizer or input-output device.

The Uniservo control circuits in each of the synchronizers contain a Uniservo selection-completed flip-flop with which to alert the program, by way of the master input-output priority tests, when a previously ordered task has been completed. The read-write control circuits in each tape synchronizer, and the tape positioning checker, each contain a ten-word

flip-flop with which they alert the program through the master tests when a previously ordered task has been completed. In addition to the Uniservo selection-completed and ten-word flip-flops, the program may test other flip-flops to determine if an error has been detected, or to determine the operating condition of a particular Uniservo tape unit or circuit.

Before the program can proceed with an operation, the Uniservo tape unit and the tape circuits that are to carry it out must be available; that is, they must not be interlocked or be performing another operation. The program can test for availability the Uniservo control circuits, a selected Uniservo tape unit, the read-write control circuits, the tape positioning checker, and the read circuits. The write circuits need not be tested for availability since they can only operate in conjunction with the read-write control circuits when those circuits are available.

The program routine that initiates and controls a tape operation is performed in several steps. During each step, a tape synchronizer or the tape positioning checker is instructed to perform a part of the over-all operation. After each step, the program exits from the tape routine and performs other functions. Meanwhile, the tape synchronizer or tape positioning checker carries on unattended and alerts the program by way of the master input-output priority test when it requires additional instructions. The program then reenters the tape routine and the same sequence is repeated until the operation is complete.

As an example of how a program might control a tape operation, the sequence of program steps for initiating and controlling a tape write operation are listed below. (It should be understood that the example is a general one and any tape control routine is subject to change by the programmer within limits imposed by the operating characteristics of the Tape Synchronizer System.)

(1) Test the availability of the Uniservo control circuits. If they are available, instruct the circuits to select a specified Uniservo tape unit. (The Uniservo control circuits will alert the program, when the tape unit is selected, by setting the Uniservo selection-completed flip-flop.)

(2) Test the availability of the selected Uniservo tape unit. If it is available, transfer the starting address to the synchronizer address register. Instruct the Uniservo control circuits to energize the forward and write relays in the selected tape unit and instruct the read-write control and write circuits to prepare to operate in the specified modes. (The circuits will alert the program when the relays have pulled in by setting the Uniservo selection-completed flip-flop.)

(3) After waiting for any necessary tape reversal instruct the Uniservo control circuits to begin moving tape on the Uniservo tape unit prepared for the write operation.

(4) After waiting for the tape leader to pass the read-write head (if the tape unit is in the rewound state) instruct the read-write control circuits to begin writing data on tape. (The circuits will alert the program as soon as writing begins by setting the

ten-word flip-flop and will thereafter alert the program by setting the same flip-flop whenever writing begins on a new group of ten words.)

(5) When alerted by the ten-word flip-flop, instruct the read-write control circuits to either continue writing ten more words, or leave a space between blocks and continue writing ten more words (when the current ten words are completed) until the one or more data blocks of the required length are recorded on tape.

The delay (0.8 second) due to tape reversal referred to in step 3 and the first-block delay (1.6 seconds) referred to in step 4 are timed by the program using the 8.3-millisecond real-time clock test and the central processor adder-comparator. Shorter delays required to prevent writing while the tape accelerates, decelerates, etc., are timed automatically by the tape synchronizer.

1-27. ILLUSTRATION CONVENTIONS

There are three kinds of illustrations used in this manual: block diagrams, timing diagrams, and simplified logic diagrams.

1-28. BLOCK DIAGRAMS

The block diagram is a general representation of a circuit in which major functional subdivisions are shown as blocks. Its purpose in the manual is to introduce the reader to the over-all organization of a circuit and the main paths of communication between subdivisions. It is of limited use, however, in understanding the actual operations performed by the circuit.

1-29. TIMING DIAGRAMS

The timing diagram is a graphical representation of the timing of a circuit or operation. The significant state (the "on" state) of a signal, flip-flop, circuit, or operation is represented on the timing diagrams in this manual by a shaded or solid bar. The state of a signal, flip-flop, circuit, or operation that is not significant (the "off" state) is represented by the absence of a bar. The term "significant" is used here for convenience in presentation only and does not imply that the opposite state is not at any time significant. To simplify understanding, transitions from one state to the other are shown on the timing diagram as occurring at the beginning or end of a standard 0.5-μsec time period although the actual transitions may occur sometime in the middle of the 0.5-μsec period.

1-30. SIMPLIFIED LOGIC DIAGRAMS

The simplified logic diagram is a more detailed representation of a circuit in which logic symbols and blocks illustrate the actual operation of a circuit. Extraneous circuit details are avoided in order to facilitate understanding of the over-all theory of operation. The following

techniques and conventions are used on the simplified logic diagrams.

1-31. BLOCKS. Logic circuits that are relatively standard, such as decoders, counters, and registers, are often represented as blocks.

1-32. DUPLICATE CIRCUITS. Several duplicate or nearly identical circuits are often represented by a single circuit.

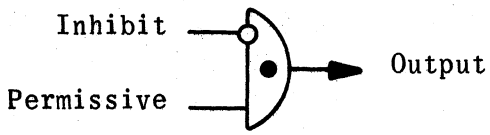
1-33. SIGNAL PATHS. Information signal paths are represented by heavy lines; control signal paths by lighter lines. Often a single line is used to represent several signal paths; in this case the number of paths is indicated by a circled number on the line.

1-34. POLARITIES. Signal polarities are ignored and the gates and buffers are assumed not to invert the polarity of signals.

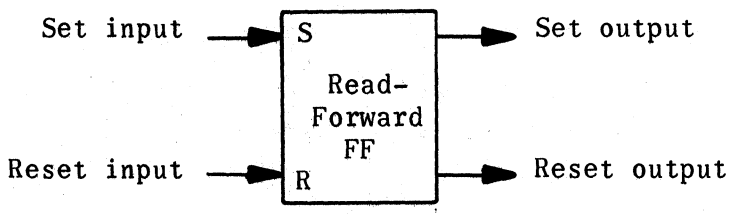
1-35. CIRCUIT RESTRICTIONS. Circuit restrictions on the number of logical stages between pulseformers, delays between pulseformers, units of drive, the number of inputs to a gate or buffer, etc., are disregarded. An operation is sometimes represented as being performed in a simplified manner when in the actual circuits it is performed in a more roundabout or complex manner because of circuit restrictions. In any case, the over-all effect of the operation is the same.

1-36. DRAWING NUMBERS. Some diagrams are divided by broken lines signifying that several detailed drawings are represented; the numbers of the detailed drawings of the circuits so represented are placed within the divisions. The drawing numbers for Synchronizer 7 only are given in the tape synchronizer diagrams; however, the equivalent drawing numbers for Synchronizers 8, 9, and 10 may be obtained by adding 20, 40, and 60, respectively, to the given number.

1-37. INHIBIT. A signal that inhibits a gate is indicated by a small circle at the input to the gate. All other signals are permissive. For example:

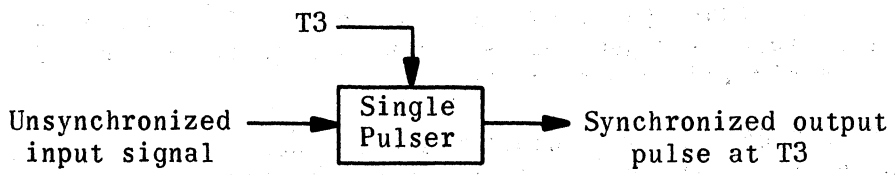


1-38. FLIP-FLOPS. A flip-flop is represented on the diagrams, as follows:



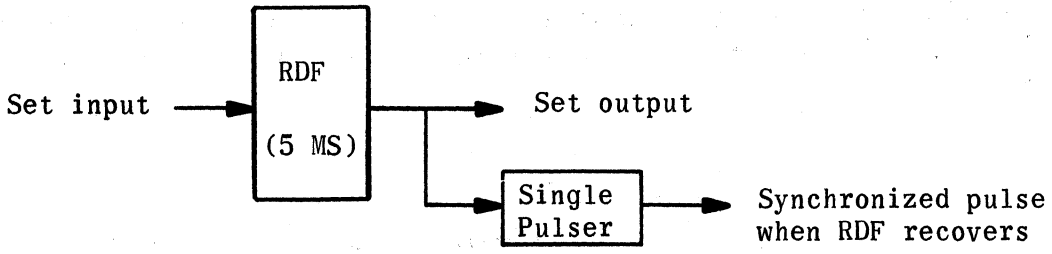
When the flip-flop is set, the set output is considered to be significant. Likewise, when the flip-flop is reset, the reset output is significant. The set and reset outputs are never significant at the same time, since one is always the logical inverse of the other. A setting pulse always overrides a resetting pulse. The flip-flop is assumed to change state 0.5 μsec after it is set or reset.

1-39. SINGLE PULSER. A single pulser is represented as follows:



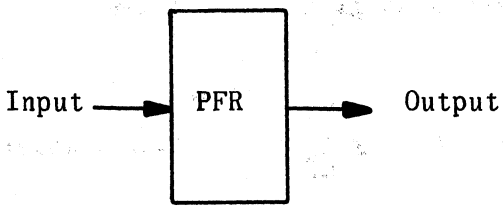
A single pulser is always followed by a pulseformer (PFR). This pulseformer, although not shown on the simplified logic diagrams, is assumed to be present when a single pulser is represented. A timing signal, if present, represents the time at which the synchronized output pulse appears at the output of the pulseformer which follows the single pulser.

1-40. RETRIGGERABLE DELAY FLOP. A retriggerable delay flop (RDF) is a device which, once set, recovers after a fixed delay period during which it is sensitive to further input signals. Each new setting signal initiates a full delay period, which is indicated in the RDF block. An RDF is always followed by a Schmitt trigger circuit (type ST-C or ST-B). The Schmitt trigger circuit, although not shown on the simplified logic diagrams is assumed to be present whenever an RDF is represented. The set output signal of the RDF shown below is present from the time the RDF is first set until it recovers 5 milliseconds after the last setting.



A single pulser following an RDF produces a synchronized output pulse when the RDF recovers.

1-41. PULSEFORMERS. A pulseformer is represented on a diagram as follows:



A delay of 0.5 μsec exists between the input of the pulseformer and the output.

1-42. OTHER LOGIC CIRCUIT ELEMENTS. Logic circuit elements other than the flip-flop, single pulser, RDF, and pulseformer are represented on diagrams by the same symbols as used on the detailed engineering logic drawings.

1-43. RELAYS AND SWITCHES. Relay contacts are shown with the relay coil windings deenergized. Switches are shown in normal unactivated positions.

SECTION 2

UNISERVO CONTROL CIRCUITS

2-1. GENERAL ORGANIZATION AND FUNCTION OF CONTROL CIRCUITS

The Uniservo control circuits are a relatively self-contained group of circuits in the tape synchronizer through which the processor program tests and exerts control over the Uniservo tape units. The four basic functions of the circuits are (1) to select a Uniservo tape unit, (2) to sample and record the status or condition of the selected tape unit, (3) to fire thyratrons in the selected tape unit to prepare it for a read or write operation or to start a rewind operation, and (4) to control the centerdrive of a tape unit during a read or write operation.

The four basic functions of the Uniservo control circuits are reflected in the functional organization of the circuits which divide into the following four sections: select control circuits, status control circuits, thyratron control circuits, and centerdrive control circuits. (See figure 2-1.)

The processor program exercises over-all control of the operations performed by the Uniservo control circuits by (1) testing various status flip-flops in the circuits to determine if an operation can take place and if an error has occurred, (2) executing instructions that specify and trigger the operations performed by the circuits, and (3) monitoring the circuits by way of the master input-output priority tests to determine when operations performed by the circuits are completed.

Once a rewind or rewind-interlock operation is started, the Uniservo control circuits are released and the operation continues to completion entirely independent of further control by the tape synchronizer. Once the Uniservo tape unit is prepared to begin a read, check-read, or write operation, the Uniservo control circuits are released and responsibility for controlling the operation is shifted either to the read-write control circuits operating in conjunction with the read or write circuits, or to the tape positioning checker operating in conjunction with the read circuits. After the Uniservo control circuits are released they may be used by the program to select another Uniservo tape unit and start a rewind or rewind interlock operation, or to select another Uniservo tape unit and prepare it for a read, check-read, or write operation provided the selected tape unit and the circuits that are to carry on the operation are available (that is, they are not interlocked or performing a previously ordered operation).

2-2. OVER-ALL OPERATION

The following general description of the operation of the Uniservo control circuits is based on the block diagram of figure 2-1. The circuits are represented in more detailed form in the simplified logic diagram of figure 2-2 and are described in more detail under headings 2-9 through 2-23. Because the Uniservo control circuits represent a two-way communication and control link between the Uniservo tape units and the central processor, the signal lines and circuits in both diagrams are, in general, so oriented that the operation flow from the Uniservo tape units to the central processor is from left to right and the flow from the central processor to the Uniservo tape units is from right to left. Subdivisions of the circuits are shown in approximately the same relative positions in both diagrams.

The last two digits of each three-digit function signal, shown encircled in figures 2-1 and 2-2, signify an instruction that generates the signal. For example, function signal 863 (FS863) is generated by instruction 63. Only one instruction generates each function signal except for FS877 which is generated by instructions 63, 65, and 68 as well as instruction 77. Signals sent to or received from the Uniservo tape units are described in tables 2-1 and 2-2, respectively.

2-3. UNISERVO TAPE UNIT SELECTION

Before a tape operation can be initiated, the program must first execute a 60 instruction to determine if the Uniservo control circuits are available. The 60 instruction, in addition to testing the circuits for availability, enters a Uniservo number (contained within the instruction) into the tape/drum number register in the central processor. If the circuits are available, the program selects the Uniservo tape unit by executing a 63 instruction. The 63 instruction first generates a presetting signal that sets or resets flip-flops in all four sections of the circuits to prepare them for the beginning of an operation, and then gates the Uniservo number to the select control circuits.

The select control circuits decode the Uniservo number to select one of the ten possible Uniservo tape units connected to the tape synchronizer. As a result, the NEP, MIR, BIR, FIR, and RIR signals are returned from the selected tape unit. After sufficient time has elapsed for the Uniservo select line to turn on and return the signals, the MIR, BIR, and FIR signals are sampled by the status control circuits to determine whether or not the Uniservo tape unit is available, is interlocked or is in the first block state, and whether the tape unit is set for a forward or backward operation. In addition, the NEP signal is sampled by the centerdrive control circuits to determine if a master tape reel is mounted on the tape unit. When the return signals are sampled, the status control circuits alert the program by way of the selection-completed and master input-output priority tests that selection is completed; that is, the tape unit is being selected and is returning the NEP and interlock-release signals.

Table 2-1. Signal Lines from Tape Synchronizer to Uniservo Tape Unit

Signal Line	Signal Name	Description or Function
		Uniservo-Select Lines
XT0...9	Uniservo Select	One line per tape unit. Selects particular tape unit by: (1) Alerting backward, forward, read, write, rewind, and rewind-interlock thyratron gates. (2) Testing the relay contact through which the MIR signal is generated. (3) Testing the select-signal gate. If neither the read nor write thyratrons are fired, the select-signal gate produces an output which tests the no-erase switch contact through which the NEP signal is generated and the network of relay contacts through which the FIR, BIR, and RIR signals are generated.
		Pickup Lines
FP	Forward Pickup	Fires the forward thyratron of the tape unit alerted by its Uniservo-select line.
BP	Backward Pickup	Fires the backward thyratron of the tape unit alerted by its Uniservo-select line.
RP	Read Pickup	Fires the read thyratron of the tape unit alerted by its Uniservo-select line.
WP	Write Pickup	Fires the write thyratron of the tape unit alerted by its Uniservo-select line.
RWP	Rewind Pickup	Fires the rewind thyratron of the tape unit alerted by its Uniservo-select line.
RVP	Rewind Interlock Pickup	Fires the rewind interlock thyratron of the tape unit alerted by its Uniservo-select line.
		Centerdrive Control Lines
RCDC	Read Centerdrive Control	Fires the centerdrive-clutch thyratron if the read thyratron is fired.
WCDC	Write Centerdrive Control	Fires the centerdrive-clutch thyratron if the write thyratron is fired.
		Clear Lines
RC	Read clear	Simultaneously extinguishes the read thyratron, if fired, of all tape units in the group.
WC	Write clear	Simultaneously extinguishes the write thyratron, if fired, of all tape units in the group.
		Write Bus Lines
WB1...8	Write Bus	Eight lines over which the seven information signals and the one sprocket signal of a digit are transmitted to the read-write heads of the tape unit whose write thyratron is fired.

Table 2-2. Signal Lines from Uniservo Tape Unit to Tape Synchronizer

Signal Line	Signal Name	Description or Function
		Signals Directly Dependent on Uniservo Tape Unit Selection
MIR*	Main-Interlock Release	Indicates that the tape unit being selected is available to the tape synchronizer; that is, (1) the main-interlock thyratron is fired, (2) the rewind-interlock thyratron is not fired, and (3) the door interlock switch is closed.
FIR**	Forward-Interlock Release	Indicates that the tape unit being selected is available and set for forward operation; that is, (1) the main-interlock thyratron is fired; (2) the rewind-interlock, rewind, read, write, and backward thyratrons are not fired; and (3) the door interlock switch is closed.
BIR**	Backward-Interlock Release	Indicates that the tape unit being selected is available and set for a backward operation; that is, (1) the main-interlock thyratron is fired; (2) the rewind-interlock, rewind, read, write, and forward thyratrons are not fired; and (3) the door interlock switch is closed.
RIR	Rewind-Interlock Release	Indicates that the tape unit being selected is being (or has been) rewound with interlock; that is, the main-interlock and rewind-interlock thyratrons are fired and the door interlock switches are closed.
NEP	No-Erase Probe	Indicates that the no-erase switch on the tape unit being selected is activated, signifying that a master tape reel is mounted on the Uniservo tape unit.
		Signals Not Directly Dependent on Uniservo Tape Unit Selection
WTB	Write Test Bus	Indicates that none of the write thyratrons in the tape units are fired.
WCT	Write Clutch Test	Indicates that the centerdrive clutch is engaged in the tape unit whose write thyratron is fired.
RFW	Read Forward	Indicates that the centerdrive motor is operating forward in the tape unit whose read thyratron is fired.
RB	Read Backward	Indicates that the centerdrive motor is operating backward in the tape unit whose read thyratron is fired.
WF	Write Forward	Indicates that the centerdrive motor is operating forward in the tape unit whose write thyratron is fired.
RPA	Read Photocell Alert	Indicates that defective tape is approaching the read-write head during a read operation.

* The absence of the MIR signal indicates to the synchronizer that operator intervention is required to make the tape unit being selected available to the tape synchronizer. Operator intervention normally consists of depressing the OFF pushbutton (to extinguish the rewind-interlock and main-interlock thyratrons), changing the tape reel, and then depressing the ON pushbutton to refire the main-interlock thyratron.

** The joint occurrence of the FIR and BIR signals indicates to the synchronizer that the tape unit being selected is in the initial or first-block condition and is ready to accept pickup signals for forward operation. Such a condition would normally exist after a rewind-without-interlock operation or after the operator had depressed the OFF pushbutton, changed the tape reel, and depressed the ON pushbutton.

The absence of both the FIR and BIR signals indicates to the synchronizer that the tape unit being selected is unavailable to perform an intended operation either because it is already performing an operation, or because it requires operator intervention to make it available.

Table 2-2. Signal Lines from Uniservo Tape Unit to Tape Synchronizer (cont)

Signal Line	Signal Name	Description or Function
		Signals Not Directly Dependent on Uniservo Tape Unit Selection (cont)
WPA	Write Photo-cell Alert	Indicates that defective tape is approaching the read-write head during a write operation.
PT	Plastic Tape	Signifies that a reel of plastic tape is mounted on a tape unit whose read thyratron is fired. Signal is generated when the PLASTIC/METAL tape switch is in the PLASTIC position on the tape unit whose read thyratron is fired.
RB1...8	Read Bus	The eight lines over which the seven information signals and the sprocket signal from the read-write heads are transmitted to the tape synchronizer from a tape unit whose read thyratron is fired.

2-4. UNISERVO TAPE UNIT AVAILABILITY

After reentering the tape routine by executing the 64 instruction, the program executes a 72 instruction to determine if the selected Uniservo tape unit is available; that is, if it is not interlocked or is not already performing an operation. If the tape unit is not available, the program executes a 76 instruction to determine if it is interlocked; that is, if power is off in the tape unit or it is in the rewound-with-interlock state. Either of these conditions requires operator intervention; the program normally informs the operator of their existence by means of a printout.

When the unavailable Uniservo tape unit is encountered the program has two choices: (1) it may cancel for the time being the operation intended for the unavailable tape unit and clear the Uniservo control circuits so that a new operation may be started on another tape unit, or (2) it may delay starting any new operations on other tape units until after the unavailable tape unit becomes available and is started in operation.

If the first choice is made, the program executes a 78 instruction. This instruction causes the thyratron control circuits to terminate selection and generate a pickup-completed signal. The pickup-completed signal makes the Uniservo control circuits available and alerts the program by way of the selection-completed test to the fact that the Uniservo control circuits have been cleared and are available for selecting another tape unit.

If the second choice is made, the synchronizer continues to select the same tape unit and the status control circuits continue to sample the FIR and BIR signals. When either or both of these signals turn on (as a result of the operator removing an interlock on the tape unit or as a result of the tape unit completing an operation) the status control circuits alert the program by way of the selection-completed test to the fact that the tape unit is now available.

When the program has established that the selected tape unit is available, a rewind or rewind-interlock operation is started on the tape unit (heading 2-5 below) or the tape unit is prepared for a read or write operation (heading 2-6).

2-5. REWIND AND REWIND-INTERLOCK OPERATIONS

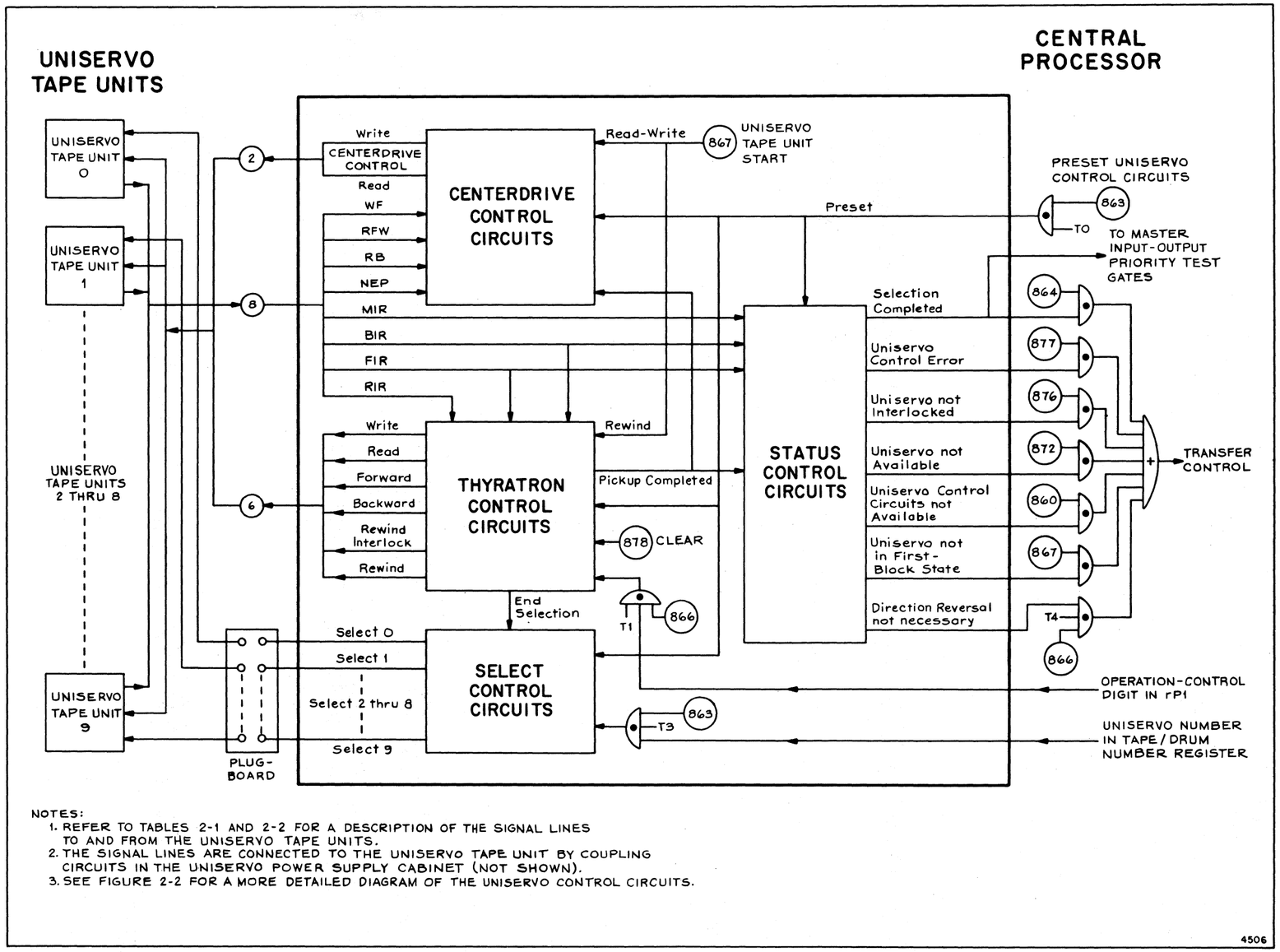
The program begins a rewind or rewind-interlock sequence by executing a 66 instruction. The 66 instruction gates an operation-control digit (preloaded in register P1 by the program) to the thyratron control circuits. The operation-control digit specifies the type of operation. It is decoded by the thyratron control circuits to generate a backward-pickup signal provided the Uniservo tape unit is not in the first-block condition. The backward-pickup signal fires the backward thyratron if it is not already fired. The combination of thyratrons that are fired for each type of tape unit operation is shown in table 2-3.

Table 2-3. Thyratrons Fired for Each Type of Uniservo Tape Unit Operation

Operation	Thyratrons						
	Main Interlock	Backward	Forward	Rewind	Rewind-Interlock	Read	Write
Rewind	X	X		X			
Rewind-with-Interlock	X	X		X	X		
Read Forward	X		X			X	
Read Backward	X	X				X	
Write	X		X				X

The 66 instruction also performs a test to determine if a tape direction reversal will take place on the tape unit as a result of the backward-pickup signal being generated. If a tape direction reversal is not indicated, the program immediately executes a 67 instruction. If a tape direction reversal is indicated, the program delays execution of the 67 instruction for 0.6 second until the loop balance position of the tape unit has shifted.

A rewind-pickup signal is generated by the 67 instruction provided that (1) a rewind or rewind-interlock operation is specified by the operation-control digit, (2) the selected Uniservo tape unit is available, (3) the tape unit is set for a backward operation, and (4) the tape unit is not in the first-block condition. A rewind-interlock pickup signal is generated by the 67 instruction provided that (1) a rewind-interlock operation is specified, (2) the selected tape unit is available, and (3) the tape unit is set for a backward operation or is in the first-block condition. After the necessary thyratrons have been fired by the pickup signals, the thyratron control circuits terminate tape-unit selection by generating a pickup-completed signal. This signal makes the Uniservo control circuits available, alerting the program by way of the selection-completed test to the fact that



NOTES:
1. REFER TO TABLES 2-1 AND 2-2 FOR A DESCRIPTION OF THE SIGNAL LINES TO AND FROM THE UNISERVO TAPE UNITS.
2. THE SIGNAL LINES ARE CONNECTED TO THE UNISERVO TAPE UNIT BY COUPLING CIRCUITS IN THE UNISERVO POWER SUPPLY CABINET (NOT SHOWN).
3. SEE FIGURE 2-2 FOR A MORE DETAILED DIAGRAM OF THE UNISERVO CONTROL CIRCUITS.

Figure 2-1. Uniservo Control Circuits, Block Diagram

the rewind or rewind-interlock operation has been initiated or the tape unit was already rewound or rewound with interlock. The thyratron control circuits detect the firing of the rewind thyratron by sampling the FIR and BIR signals, both of which should be off after the thyratron is fired. The firing of the rewind-interlock thyratron is detected by sampling the RIR signal which should be on after the thyratron is fired.

2-6. READ, CHECK-READ, AND WRITE OPERATIONS

Before a Uniservo tape unit can be prepared for a read, check-read, or write operation, the processor program must establish that the circuits required to complete the intended operation are available (instructions 66, 62, and 56). Also, if a read-to-memory or write operation is intended, a starting address must be loaded into the synchronizer address register (instruction 74). The program then executes a 66 instruction which transfers an operation-control digit to the thyratron control circuits. The operation-control digit is decoded to generate a read or write pickup signal and a forward or backward pickup signal (table 2-3). When the read or write thyratron has fired the thyratron control circuits terminate selection and 10 milliseconds later generate a pickup-completed signal. The pickup-completed signal makes the Uniservo control circuits available, removes an interlock on the read or write center-drive control circuits, and alerts the program (by way of the selection-completed test) to the fact that the tape unit is ready to begin moving tape provided a direction reversal is not taking place. The pickup-completed signal is delayed for 10 milliseconds to allow time for the relays energized by the read or write thyratrons to pull in before tape motion starts.

If the tape-direction test, performed by the 66 instruction, indicates that a tape direction reversal is not required, the program executes a 67 instruction immediately after it is alerted by the pickup-completed signal. If a tape direction reversal is required, the program delays execution of the 67 instruction until 0.8 second after the 66 instruction is executed. When the 67 instruction is executed a read or a write centerdrive signal is produced by the centerdrive control circuits, thereby starting tape motion on the particular tape unit which had a read or write thyratron fire. The read or write centerdrive signal will not be generated, however, if a tape direction signal (WF, RFW, or RB) or the NEP signal from the tape unit indicates that it is not prepared to begin the specified operation. The 67 instruction also performs a test to determine whether or not the tape unit is in the first-block state. If it is in the first-block state, the program delays reading or writing until the tape leader has passed the read-write head.

The read or the write centerdrive signal remains on until the end of the operation, at which time it is turned off by an ending signal from the read or write circuits in the synchronizer. The same circuits then generate a (read or write) clear signal to extinguish the read or write thyratron that fired.

2-7. ERROR CONTROL

The operations performed by the Uniservo control circuits and the program are checked throughout for programming and machine error conditions.

If an error is detected, a Uniservo-control-error flip-flop in the status control circuits and one of a number of error-diagnostic flip-flops in the central processor are set. (Refer to heading 2-17 and table 2-4.) By testing the Uniservo-control-error flip-flop, the program determines whether an error has occurred. By testing the error-diagnostic flip-flops, the program determines the type of error that occurred.

2-8. PRESETTING SIGNAL

When a 63 instruction is executed, at the beginning of a tape operation, FS863 is gated with the tape-synchronizer-select signal (PST1) to produce the presetting signal, S7FRS. (See figure 2-2.) The S7FRS signal functions as a type of initial-clear signal which clears control flip-flops and registers throughout the Uniservo control circuits to prepare for the selection, test, and control of a Uniservo tape unit. In order that the condition of the Uniservo control circuits at the beginning of an operation may be better understood, the effect of the presetting signal, S7FRS, on the circuits is described below before the circuits themselves are described.

The S7FRS signal, generated at T0, clears the Uniservo-select register before a Uniservo number is gated into the register at T3 by FS863. The S7FRS signal also sets the Uniservo-select flip-flop and the read and write centerdrive-interlock flip-flops, clears the tape operation-control register, and resets the following flip-flops:

(1) Ring-in tape

(2) Start tape

(3) Uniservo interlock

(4) Uniservo selection-completed

(5) Uniservo available

(6) Uniservo-control-circuits available

(7) First-block

At T3, 1.5 μsec later, FS863 tests the buffed outputs of the pickup, FIR, and BIR flip-flops and all of the flip-flops that are set or reset by the S7FRS signal (excepting the Uniservo-select flip-flop and the flip-flops in the Uniservo-select register). If any one of these flip-flops is not in the proper state for beginning an operation, the preset error-diagnostic flip-flop in the central processor and the Uniservo-control-error flip-flop in the status control circuits are set. The pickup flip-flop should be reset from a previous operation and the FIR and BIR flip-flops are reset by an RDF that is triggered when the Uniservo-control-circuits-available flip-flop is reset by the S7FRS signal. FS877, generated by the 63 instruction at T4,5, tests the Uniservo-control-error flip-flop. If the flip-flop is set as the result of a preset error, the test will transfer control and reset the flip-flop.

2-9. SELECT CONTROL CIRCUITS

The select control circuits consist of a one-digit select register and decoder that stores and decodes the number of the Uniservo tape unit being selected; a Uniservo-select flip-flop which turns the select decoder on or off; an amplifier for each select line which amplifies the select signal for transmission to the Uniservo tape unit; and a select checker and associated dummy-select flip-flop which check to ensure that one and only one select line is active during selection. (See figure 2-2.)

After the presetting signal, S7FRS, at T0 clears the select register and turns on the select decoder by setting the Uniservo-select flip-flop, the Uniservo number is gated at T3 from the LSD position of the tape/drum number register into the Uniservo-select register by FS863. The number gated into the select register is decoded by the select decoder whose outputs are amplified to drive the Uniservo-select lines. Only one of the Uniservo-select lines should be energized when the number is being decoded.

All of the Uniservo-select lines, together with the amplified output of the dummy-select flip-flop, are sampled by the select checker. The select checker is a special gating circuit having the characteristic of producing a low output if none or one of its inputs is energized (positive) and a high output if more than one input is energized.

Two hundred microseconds after selection is started by the 63 instruction, the status control circuits generate an S7SEL signal which simultaneously tests the output of the select checker and sets the dummy-select flip-flop. In the normal case, at the instant the checker output is tested by the S7SEL signal one of the Uniservo-select lines should be completely energized and the dummy-select flip-flop should be reset. The checker should therefore produce a low output. (The dummy-select flip-flop does not change state - set - until after the checker output is tested.) If more than one Uniservo-select lines are energized or if the dummy-select line as well as a Uniservo-select line is energized, the checker will produce a high output resulting in an S7SELE error signal. This error signal, in turn, will set the Uniservo control-error flip-flop in the status control circuits and the improper-connection diagnostic flip-flop in the central processor.

Later in the selection period, the select checker is tested a second time by an S7PCKD signal generated by the thyratron control circuits. The S7PCKD signal is normally generated after pickup signal lines have been energized to fire the proper combination of read, write, forward, and backward thyratrons in the selected Uniservo tape unit. The S7PCKD signal may also be generated by a 78 instruction. In either case, both the dummy-select line and one of the Uniservo-select lines should be energized when the checker is tested the second time, producing a high output from the checker. If none of the Uniservo-select lines is energized or if the dummy-select line is not energized, the checker will produce a low output which, when tested by the S7PCKD signal, will generate an S7SALE error signal. This error signal sets the Uniservo control-error flip-flop and the improper-connection flip-flop. The S7PCKD signal also resets the dummy-select flip-flop to prepare it for the first-selection error test after another tape unit is selected. After the thyratron control circuits have fired all the thyratrons required to be fired in the selected tape unit, an S7SELF signal is generated to clear the Uniservo-select register and reset the Uniservo-select flip-flop, thereby ending selection. The S7SELF signal is also

generated when a 78 instruction is executed. When the Uniservo-select flip-flop is reset it inhibits the FIR and BIR flip-flops in the status control circuits from being set (heading 2-12).

The combination of the two tests of the selector checker constitutes a check to ensure that one and only one Uniservo tape unit is selected at a time. The first test, while selection is taking place and the dummy-select line is not energized, ensures that not more than one tape unit is being selected; the second test, while selection is taking place and the dummy-select line is energized, ensures that at least one tape unit is being selected. The checking is designed in such a way that a fault in the checking circuits themselves will be detected by the tests.

2-10. STATUS CONTROL CIRCUITS

The status control circuits provide the means by which the Uniservo control circuits communicate with the processor program. They keep track of the following conditions for the program:

(1) The availability of the Uniservo control circuits.

(2) The state or condition of the selected Uniservo tape unit.

(3) The completion of an operation specified by the program.

(4) The error conditions detected by the Uniservo control circuits.

The functions of the status control circuits are carried out by a number of flip-flops and their associated circuits (figure 2-2) each of which is described below under headings 2-11 through 2-17.

2-11. UNISERVO-CONTROL-CIRCUITS-AVAILABLE FLIP-FLOP

This flip-flop records whether or not the Uniservo control circuits are available to the program for use in selecting a Uniservo tape unit and preparing it for an operation. The flip-flop is reset to the unavailable state at the beginning of a Uniservo control sequence by the presetting signal, S7FRS, generated by a 63 instruction. It is set to the available state by the S7ST6 pickup-completed signal generated by the thyratron control circuits. The S7ST6 signal is generated following the firing of thyratrons on the selected tape unit or following execution of a 78 instruction.

When the Uniservo-control-circuits-available flip-flop is first reset by the S7FRS presetting signal, it triggers a 200- and a 150-μsec RDF. The function of these RDF's is described in the next paragraph.

2-12. FIR AND BIR FLIP-FLOPS

The FIR and BIR flip-flops sample and store the U7FIR and U7BIR interlock-release signals if and when they are returned by the selected Uniservo tape unit. When selection first starts both flip-flops are jammed

to the reset state for 150 μsec by an RDF that is triggered when the Uniservo-control-circuits-available flip-flop is reset by the presetting signal. This prevents the FIR and BIR flip-flops from being incorrectly set by any stray transient pulses that might appear on the U7FIR and U7BIR lines when the Uniservo-select line turns on and tests the tape unit circuits that generate the interlock-release signals.

When the Uniservo-control-circuits-available flip-flop is reset by the presetting signal, the 200-μsec RDF, as well as the 150-μsec RDF, is triggered. The 200-μsec RDF, like the 150-μsec RDF, provides a delay while signals from the tape unit turn on at the beginning of the selection period. When the 200-μsec RDF recovers, it generates the S7SEL signal through a single pulser. The S7SEL signal tests the select checker, sets the dummy-select flip-flop, and sets the Uniservo selection-completed flip-flop. The S7SEL signal also sets the Uniservo interlock flip-flop if the U7MIR signal is not returned by the selected tape unit and sets the ring-in-tape flip-flop if the U7NEP signal is returned.

When the 200-μsec RDF recovers it also tests and continues to monitor the buffed outputs of the FIR and BIR flip-flops. If either or both of these flip-flops is set, signifying that the selected tape unit is available, an S7FISP signal is produced. The S7FISP signal sets the Uniservo-available flip-flop, resets the Uniservo interlock flip-flop and sets the Uniservo selection-completed flip-flop. The difference in recovery time between the 200-μsec RDF and the 150-μsec RDF is accounted for by the fact that the 200-μsec RDF tests the FIR and BIR flip-flops whose setting, in turn, is dependent upon recovery of the 150-μsec RDF.

If the Uniservo tape unit is available when selection begins, the S7SEL and the S7FISP signals are both generated and concurrently set the Uniservo selection-completed flip-flop to alert the processor program that selection has begun. If, however, the tape unit is not available when selection begins, only the S7SEL signal is generated to set the Uniservo selection-completed flip-flop. If, at a later time, the U7FIR or U7BIR signal, or both, turn on and set their respective flip-flops, the S7FISP signal is generated and sets the Uniservo selection-completed flip-flop a second time to alert the program to the fact that the previously unavailable tape unit has become available. When the Uniservo-select flip-flop is reset, it inhibits both the FIR and BIR flip-flops from being set. This prevents the S7FISP signal from being generated and erroneously setting the Uniservo selection-completed flip-flop in the event the tape unit should become available while selection is ending as a result of a 78 instruction being executed.

The FIR and BIR flip-flops are tested by FS866. If both the FIR and BIR flip-flops are set, this test will set the first-block flip-flop (heading 2-13). The outputs of the FIR and BIR flip-flops are also gated with the check-bit of the digit in the tape-operation control register to determine if a reversal of tape direction on the tape unit is required. The tape-operation control register stores the operation-control-digit I specified by the program (instruction 66). Since the operation-control-digit I is an even number for all backward tape operations and an odd number for all forward tape operations, the check-bit of this digit functions as a tape-direction indicator. The check-bit, together with the S7FIR and S7BIR signals, determines if a tape reversal on the tape unit is required. For example, if the check-bit is odd, indicating that a forward tape operation

is called for, and the BIR flip-flop only is set (indicating that the tape unit is prepared for a backward operation), then tape reversal is required. The gates that determine if a direction reversal is required are tested by FS866. In figure 2-2 the opposite states of the check-bit are represented by the decoded outputs S7F and S7B of the operation-control register.

2-13. FIRST-BLOCK FLIP-FLOP

The first-block flip-flop provides the processor program and the thyratron control circuits with an indication of whether or not the selected Uniservo tape unit is in the initial, or first-block, condition. Such a condition would normally exist at the tape unit after a rewind-without-interlock operation or after the operator has changed a tape reel on the tape unit and depressed the Uniservo ON pushbutton. The first-block flip-flop is reset (cleared) by the presetting signal S7FRS. It is set, by FS866, if both the FIR and the BIR flip-flops are set, indicating that the selected Uniservo tape unit is in the first-block condition.

2-14. UNISERVO-AVAILABLE FLIP-FLOP

The Uniservo-available flip-flop provides the processor program, the thyratron control circuits, and the centerdrive control circuits with an indication of whether or not the selected Uniservo tape unit is available. It is reset (cleared) to the unavailable state by the presetting signal. It is set by S7FISP at least 200 μsec after the 63 instruction is executed, provided either the FIR or BIR signal, or both, are returned by the tape unit as indicated by the state of the FIR and BIR flip-flops.

2-15. UNISERVO SELECTION-COMPLETED FLIP-FLOP

The Uniservo selection-completed flip-flop provides the means by which the processor program monitors the Uniservo control circuits. When set, it alerts the program through the master input-output priority tests to the fact that a specified operation has been completed or that a selected Uniservo tape unit has become available.

The Uniservo selection-completed flip-flop is tested by FS864. The flip-flop is reset (cleared) at the beginning of the selection period by the presetting signal, S7FRS, and is thereafter reset whenever it is tested by a 64 instruction.

The flip-flop is set, 200 μsec after a select instruction, by the S7SEL signal regardless of whether or not the tape unit is available at that time. Setting the flip-flop alerts the program to the fact that selection has begun. Consequently, a test by the program to determine if the tape unit is available would be valid at this time. If the tape unit is not available at the time the Uniservo selection-completed flip-flop is set the first time, it may be set subsequently by the S7FISP signal, if and when the Uniservo becomes available; that is, if and when the U7FIR or U7BIR signal, or both, turn on. This setting alerts the program to the fact that the tape unit has become available since the first time it was tested after selection. The flip-flop would be set by the S7FISP signal if and when the

selected tape unit completes a read, write, or rewind operation or if and when the operator manually releases the tape unit from a rewind-interlock or other interlock condition, provided, of course, that the Uniservo control circuits were not cleared in the meantime by a 78 instruction.

The Uniservo selection-completed flip-flop is also set, by the S7ST6 signal, 10 milliseconds after the proper thyratrons have been fired in the selected tape unit or 10 milliseconds after a clear-Uniservo-control-circuits instruction (78) is executed. This setting would indicate one of the following to the processor program:

(1) The Uniservo control circuits are available after the execution of a clear-Uniservo-control-circuits instruction (78).

(2) The Uniservo control circuits are available after a rewind or rewind-with-interlock operation has been initiated.

(3) If a tape direction reversal is not taking place, the tape unit is ready to begin moving tape in preparation for a specified read or write operation.

2-16. UNISERVO INTERLOCK FLIP-FLOP

The Uniservo interlock flip-flop provides the processor program and the operator with an indication of whether or not the selected Uniservo tape unit is rewound with interlock or power is off in the tape unit. The flip-flop is reset (cleared) at the beginning of the selection period by the presetting signal. It is set by the S7SEL signal 200 μsec after the 63 instruction is executed, provided the MIR test-return signal from the tape unit is not turned on, indicating that the main interlock thyratron is extinguished (Uniservo power is off), a door interlock switch is open, or the rewind-interlock thyratron is fired. The flip-flop may be subsequently reset by the S7FISP signal if and when the selected tape unit becomes available; that is, if and when the U7FIR or U7BIR signal, or both, turn on. When set, the flip-flop lights a tape-interlock indicator light on the operator's control console panel.

2-17. UNISERVO CONTROL-ERROR FLIP-FLOP

The Uniservo control-error flip-flop indicates to the program whether or not an error condition has been detected by the Uniservo control circuits while selecting a Uniservo tape unit and attempting to generate pick-up and centerdrive signals. The flip-flop is tested by FS877 (generated by instructions 63, 65, 68, and 77) and is always reset upon testing. Error signals that set the flip-flop also set appropriate error-diagnostic flip-flops in the central processor to alert the processor program to the type of error that occurred. Each of the error signals that sets the flip-flop is listed and described in table 2-4. The number of the error-diagnostic flip-flop that is set when an error signal is generated is also listed. The first two digits of the number in the third column of the table identify the number of the instruction that tests the diagnostic flip-flop; the third digit is the selector digit. For example, diagnostic flip-flop 47-9 is tested by a 47 instruction having a selector digit of 9.

Table 2-4. Uniservo Control-Error Signals

Error Signal	Signal Name	Diagnostic Flip-Flop Set	Condition Causing Error
S7PRSE and S7PRF	Preset Error	46-9	The pickup flip-flop, the FIR flip-flop, the BIR flip-flop or one of the flip-flops (excepting the Uniservo-select and the Uniservo-select-register flip-flops) that are normally preset (set or reset) by the S7FRS signal is not in the proper state after a 63 instruction is executed.
S7SELE	Select Error	46-7	More than one tape unit is selected following a Uniservo-select instruction (63) or the select checker is not operating properly.
S7SALE	Select Error	46-7	No tape unit was selected following a Uniservo-select instruction (63) or the select checker is not operating properly.
S7UE	Unavailable Error	47-6	A 66 instruction is executed when the selected tape unit is unavailable.
S7WTE*	Write Test Error	47-6	A write operation is specified by the processor program (instruction 66) and either a master tape reel is mounted on the selected tape unit or a tape unit is already writing (that is, a write thyratron is fired).
S7RCHE*	Ring Check Error	46-8	A write operation is specified by the processor program and a master tape reel is mounted on the selected tape unit.
S7MOE1	Mode Error 1	47-9	(1) A write operation is specified by the program (instruction 66) and a legitimate translation control digit (K) or SBB-length control digit (L) is not specified, or (2) a read operation (tape-to-memory) is specified by the program and a legitimate translation control digit (K) or a legitimate tape-identification digit (L) is not specified.
S7MOE2	Mode Error 2	47-9	A read operation is specified by the program (instruction 66) and a legitimate gain-control digit (G) is not specified.
S7DIRE	Direction Error	47-7	The program attempts to start tape motion (instruction 67) after specifying a read forward, read backward, or write operation and the direction the tape unit centerdrive motor is set for does not agree with the specified operation.

* The S7WTE signal can be generated either because a write operation is specified and a tape unit is already writing or because a write operation is specified and a master tape reel is mounted on the selected tape unit. The latter condition also generates an S7RCHE signal. The S7WTE signal and the S7RCHE signal set, respectively, the 47-6 and 46-8 diagnostic flip-flops. By testing these flip-flops the processor program can determine which of the two possible error conditions generated an S7WTE signal.

2-18. THYRATRON CONTROL CIRCUITS

The main function of the thyratron control circuits is to generate pickup signals which fire a combination of thyratrons in the selected Uniservo tape unit. The fired thyratrons prepare the tape unit for a read or write operation, or initiate a rewind operation. The processor program specifies the operation by executing a 66 instruction after it has been established that the selected tape unit and the processor tape circuits needed to perform the operation are available. The 66 instruction transfers an operation-control digit (I), preloaded into rP1, to the thyratron control circuits where it is stored and decoded to generate pickup signals that fire the proper combination of thyratrons in the tape unit being selected. The read, write, backward, and forward pickup signals are generated as a result of executing a 66 instruction. However, if a rewind or rewind-with-interlock operation is specified, pickup signals are not generated until a Uniservo-start instruction (67) is executed. The rewind pickup signals are generated separately because the firing of the rewind thyratron automatically starts tape motion on the tape unit which could interfere with a tape direction reversal. In the event a tape direction reversal is indicated by a test performed by the 66 instruction, the program must delay executing the 67 instruction for 0.8 second to allow time for the loop balance position of the tape unit to shift. The thyratrons that must be fired to prepare a tape unit for each type of operation are listed in table 2-3. Each of the thyratrons listed, except the main interlock thyratron, is fired by a combination of the Uniservo-select signal and a pickup signal.

After the necessary thyratrons have been fired, the pickup signals are turned off and Uniservo selection is terminated. After a 10-millisecond delay to allow circuits in the tape unit to be activated by the fired thyratrons, the centerdrive control circuits are alerted in the event a read or write operation is to be performed, the Uniservo-control-circuits-available flip-flop is set to "available," and the Uniservo selection-completed flip-flop is set in order to alert the program to the fact that the pickup sequence has ended.

The thyratron control circuits (figure 2-2) consist of the following main parts:

(1) A one-digit register and decoder that stores and decodes the operation-control digit specified by the program.

(2) A pickup flip-flop and associated pickup RDF which gate outputs of the operation control decoder to drive the proper write, read, forward and backward pickup bus amplifiers for the time duration required to fire the thyratrons.

(3) A rewind pickup flip-flop which gates outputs of the decoder to drive the proper rewind and rewind-interlock pickup bus amplifiers until the associated thyratrons have fired.

(4) A number of pickup-ending gates that detect the ending of the pickup sequence, and a pickup-ending RDF which times the interval required for relays to be activated by the fired thyratrons.

2-19. OPERATION CONTROL

The tape operation-control register is cleared by the presetting signal S7FRS. The operation-control digit is gated into the register from register P1 at T1 by FS866. There, the digit is decoded to generate read, write, forward, backward, rewind, and rewind-interlock signals which are used to generate the proper combination of pickup signals and to control gates in both the centerdrive and thyratron control circuits.

Outputs of the operation-control register and decoder are gated by FS866 at T4 with outputs of the mode decoder to set a combination of mode flip-flops in the read and write circuits. The mode decoder, which decodes mode digits in register P1 for all of the tape synchronizers, is described in section 3. A check is performed by FS866 at T4 to ensure that the mode-control data decoded from rP1 is consistent with the data in the operation-control register. If the data is not consistent, a mode error 1 or mode error 2 signal is generated. The conditions that cause the mode error signals are described in table 2-4.

2-20. WRITE, READ, FORWARD, AND BACKWARD PICKUP

The pickup flip-flop generates the write, read, forward, and backward pickup signals by gating signals from the operation-control register and decoder to drive the proper pickup signal amplifiers. If the selected Uniservo tape unit is in the first-block condition, the backward pickup signal is inhibited by the S7FB signal. The pickup flip-flop is set by FS866 at T1 provided that neither a write-test error (S7WTE) nor an unavailable error (S7UE) is detected. The conditions that cause these errors are described in table 2-4. When the pickup flip-flop is set, a pickup RDF is triggered which generates an S7PCKD signal upon recovery, 440 μsec later. By that time, any pickup signals that were generated should have fired their respective thyratrons. The S7PCKD signal therefore resets the pickup flip-flop to turn off the pickup signals. The S7PCKD signal also tests the select checker, resets the dummy-select flip-flop, and, if a read or write operation is specified, generates signals that terminate the pickup sequence (heading 2-22). A 78 instruction clears the Uniservo control circuits by artificially generating the S7PCKD signal. When the S7PCKD signal is generated by FS878, however, the signals that normally terminate the pickup sequence are generated regardless of the operation specified.

2-21. REWIND AND REWIND-INTERLOCK PICKUP

The rewind pickup flip-flop generates the rewind-pickup signal and alerts the gate (in the operation control decoder) that produces the rewind-interlock pickup signal. The rewind-pickup flip-flop is set by FS867 when a rewind operation is specified, provided the Uniservo-available and BIR flip-flops are set, indicating that the Uniservo tape unit is available and set for backward operation or possibly is already rewound. If the selected tape unit is already rewound, the rewind-pickup signal is inhibited by the S7FB signal from the first-block flip-flop. The rewind-interlock pickup signal may be generated, however, even though the tape unit is in the first-block condition.

When the rewind pickup flip-flop is set, it samples gates which detect the ending of the pickup sequence; that is, they detect the firing of the proper thyratrons or the fact that the selected tape unit is already rewound or rewound with interlock. When one of these conditions is detected the rewind pickup flip-flop is reset.

2-22. PICKUP ENDING

After the proper thyratrons have fired or after an attempt is made to rewind or rewind with interlock a Uniservo tape unit that is already rewound or rewound with interlock, the thyratron control circuits generate an S7SELF signal. The S7SELF signal resets the rewind pickup flip-flop (if it is set), clears the Uniservo-select register, and resets the Uniservo-select flip-flop to terminate selection. The S7SELF signal also triggers a 10-millisecond pickup-ending RDF which, when it recovers, produces the pickup-completed signal, S7ST6. The 10-millisecond pickup-ending delay is only important for a read or write operation. It ensures that sufficient time has elapsed for the contacts of the mercury read or write relays in the tape unit to pull in or drop out before the program is alerted to begin moving tape. The S7ST6 signal sets the Uniservo-control-circuits-available flip-flop to "available" and sets the Uniservo selection-completed flip-flop. When a write operation is specified, the S7ST6 signal also resets the write centerdrive interlock flip-flop in the centerdrive control circuits and generates a write-preset signal provided the write-centerdrive and ring-in-tape flip-flops are not set. When a read operation is specified, the signal resets the read centerdrive interlock flip-flop and generates a read preset signal provided the read centerdrive flip-flop is not set.

The termination of a pickup sequence is detected by four gates whose outputs are buffed together to produce the S7SELF signal which, in turn, triggers the RDF that produces the pickup-completed signal, S7ST6. The conditions detected by each gate and the way in which they are detected are described individually, as follows:

Condition 1: Read or write thyratron fired or Uniservo control circuits cleared. This condition is detected by sampling the S7PCKD signal when a rewind operation is not specified. If the S7PCKD signal is artificially generated by FS878 to clear the circuits, the S7RW signal is inhibited and does not inhibit the S7PCKD signal.

Condition 2: Rewind thyratron fired (rewind interlock thyratron not fired). This condition is detected by sampling the U7FIR and U7BIR signals from the Uniservo tape unit when a rewind operation is attempted. When the rewind thyratron is fired neither the U7FIR nor the U7BIR signal is returned to the tape synchronizer.

Condition 3: Rewind-interlock thyratron fired or Uniservo already rewound with interlock. This condition is detected by sampling the U7RIR signal from the tape unit when a rewind or rewind-interlock operation is attempted. When the rewind-interlock thyratron is fired, the tape unit returns the U7RIR signal.

Condition 4: Uniservo already rewound. This condition is detected by sampling the first-block flip-flop when a rewind operation is attempted. If the tape unit were already rewound, the first-block flip-flop would be set.

2-23. CENTERDRIVE CONTROL CIRCUITS

The main function of the centerdrive control circuits is to transmit read and write centerdrive signals to the Uniservo tape units for controlling tape movement during a read or write operation. Since a check-read operation using the tape positioning checker and a write operation can occur simultaneously on the same tape synchronizer, the read and the write centerdrive signals are generated individually. The read centerdrive signal energizes the clutch coil and deenergizes the brake coil in the centerdrive of the tape unit whose read thyratron is fired. The write centerdrive signal does the same on a tape unit whose write thyratron is fired. The centerdrive control circuits are interlocked against generating either signal until the proper combination of thyratrons in the tape unit have been fired and have had time to energize their respective relays.

The centerdrive control circuits contain the following flip-flops:

(1) A read centerdrive flip-flop and a write centerdrive flip-flop, which are set to generate the read and write centerdrive signals, respectively, that control tape motion of the tape unit.

(2) A read centerdrive-interlock flip-flop and a write centerdrive-interlock flip-flop which inhibit the respective read and write centerdrive flip-flops from being set until the program has been alerted to the fact that the tape unit thyratrons have fired and have activated the read (or write) relays.

(3) A ring-in-tape flip-flop which prevents the write centerdrive-interlock flip-flop from being reset (and consequently a write centerdrive signal from being generated) if U7NEP signal was returned by the selected tape unit.

(4) A start-tape flip-flop which is set by a 67 instruction, and, depending of which centerdrive-interlock flip-flop is reset, sets the read or the write centerdrive flip-flop, provided in either case that the centerdrive motor in the tape unit is set to operate in the proper direction. If the tape unit is not set to operate in the proper direction, the start-tape flip-flop will generate, instead, a direction error when it is set.

The read and the write centerdrive-interlock flip-flops are both set by the presetting signal when the tape unit is first selected by a 63 instruction. Ten milliseconds after a read or write thyratron is fired, the S7ST6 signal is generated by the thyratron control circuits. If a read operation is specified by the I digit in the operation-control register, and the read centerdrive signal is not being generated, the S7ST6 signal produces a read preset signal, S7RPR. The S7RPR signal clears various flip-flops in the read circuits (section 6) of the synchronizer preparatory to reading and resets the read centerdrive-interlock flip-flop. The read centerdrive-interlock flip-flop then alerts the gates that set the read

centerdrive flip-flop and the gates that detect a direction error for a read operation.

If a write operation is specified, the write centerdrive signal is not already being generated, and the ring-in-tape flip-flop is not set, then the S7ST6 signal generates a write-preset signal, S7WPR. The S7WPR signal alerts the write circuits to clear the output buffer register, clears various flip-flops in the write circuits of the synchronizer preparatory to writing, and resets the write centerdrive-interlock flip-flop. The write centerdrive-interlock flip-flop then alerts the gate that sets the write centerdrive flip-flop and the gate that detects a direction error for a write operation.

The write-preset signal, S7WPR, together with a similar read preset signal generates an S7RS signal (not shown in figure 2-2) which is used to clear various flip-flops and counters in the read-write control circuits of the synchronizer preparatory to a read or write operation. The derivation and function of the S7RS signal is described fully in section 4.

After the processor program is alerted by the Uniservo selection-completed flip-flop to the fact that the tape unit thyratrons have fired, it initiates tape motion on the tape unit by executing a 67 instruction. If a tape direction reversal, as indicated by a previously executed 66 instruction, is necessary to perform the specified read or write operation, the program will delay executing the 67 instruction for 0.8 second until the loop balance position in the tape unit has shifted. When the program executes a 67 instruction, FS867 is generated which sets the start-tape flip-flop if the Uniservo-available flip-flop is set to "available". If the Uniservo tape unit is set to move tape in the correct direction, the start-tape flip-flop will then generate an S7RSTU or an S7WSTU signal depending on whether the read or the write centerdrive-interlock flip-flop is reset. If the tape unit is not set to move tape in the correct direction, a direction-error signal (S7DIRE) is generated which sets the direction-error diagnostic flip-flop (in the central processor) and the Uniservo control-error flip-flop. Whether or not a tape unit is set to operate in the correct direction is determined for a read operation by matching the read-forward and read-backward signals from the tape units against the outputs from the read-direction flip-flops in the read circuits of the tape synchronizer. For a write operation (which can only take place in a forward direction) it is determined by testing the write-forward signal from the tape units.

The remaining description of the centerdrive control circuits is similar for a read and a write operation. To avoid repetition, it is written to apply to a read operation, with substitute words in parentheses applicable to a write operation.

The S7RSTU (S7WSTU) signal sets the read (write) centerdrive flip-flops, resets the start-tape flip-flop, and alerts the read (write) circuits to the fact that tape motion has started. The read (write) centerdrive flip-flop acts as a single pulser in generating the S7RSTU (S7WSTU) signal since its output is recirculated through its set gate to turn off the S7RSTU (S7WSTU) signal 0.5 μsec after it is generated. The read (write) centerdrive flip-flop remains set throughout the read (write) operation, energizing the clutch coil in the tape unit. It is reset at the end of the

operation by a read (write) ending signal from the read (write) circuits of the synchronizer. The same read (write) ending signal triggers an RDF that energizes a read-clear (write-clear) relay (in the Uniservo power supply cabinet) which extinguishes any fired read (write) thyratrons in the group of tape units. Normally, only one thyratron would be extinguished since only one read (write) operation at a time can be performed by the tape synchronizer.

After tape motion has started, the actual reading or writing is controlled, respectively, by the write circuits operating in conjunction with the read-write control circuits or by the read circuits operating in conjunction with the read-write control circuits or the tape positioning checker.

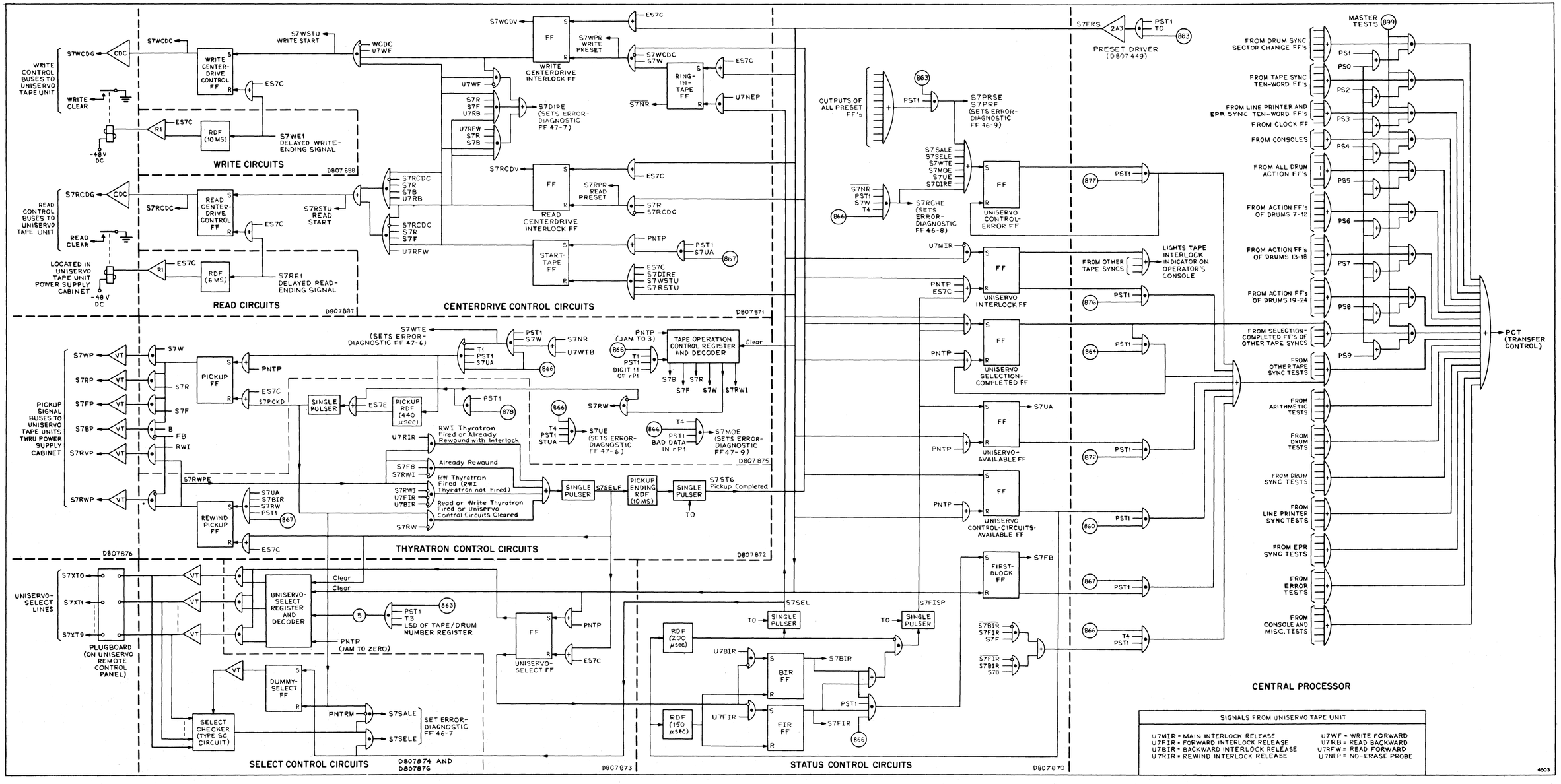


Figure 2-2. Uniservo Control Circuits, Simplified Logic Diagram

SECTION 3
SHARED CIRCUITS

3-1. GENERAL

The circuits shared by all of the four possible tape synchronizers consist of a mode decoder, tape timing signal generator, Larc-to-Univac translator and output checker, and Univac-to-Larc translator and input checker. Each circuit is described in this section to provide an understanding of how it operates individually. The description also provides a background for understanding the role each circuit plays in performing the write, read, and check-read operations described in succeeding sections.

There are two versions of the tape timing signal generator; one is for a tape synchronizer that records at a density of either 104 or 208 pulses per inch (PPI) and the other for a system that records at 125 or 250 PPI. The 104 and 208 PPI generator is used in the Larc System, Serial 1. The 125 and 250 PPI generator, a similar but modified version of the 104 and 208 PPI generator, is used in the Larc System, Serial 2. The generator used in the Larc System, Serial 1 is described in detail under heading 3-3 followed, under heading 3-7, by a description of the differences between it and the generator used in the Larc System, Serial 2. Differences in operation between the Larc System, Serial 1 and Larc System, Serial 2 tape synchronizer systems are confined almost exclusively to their respective timing signal generators.

3-2. MODE DECODER

The mode decoder decodes, for all of the tape synchronizers, mode data that is loaded into rP1 prior to the execution of a 66 instruction. The 66 instruction gates the operation-control digit I (digit 11) in rP1 into the operation-control register in the Uniservo control circuits of the specified synchronizer. Here, the operation-control digit is decoded to generate pick-up signals (heading 2-18) that are sent to a selected Uniservo tape unit. The mode decoder decodes the G, L, K, and I digits in digit positions 8, 9, 10, and 11 of rP1. Outputs of the mode decoder, together with outputs of the operation-control register and decoder, are tested by the 66 instruction to set the appropriate combination of mode flip-flops in the specified synchronizer and to detect error conditions. (See figure 3-1.) The actual decoding of the mode digits is not shown in figure 3-1 but is represented

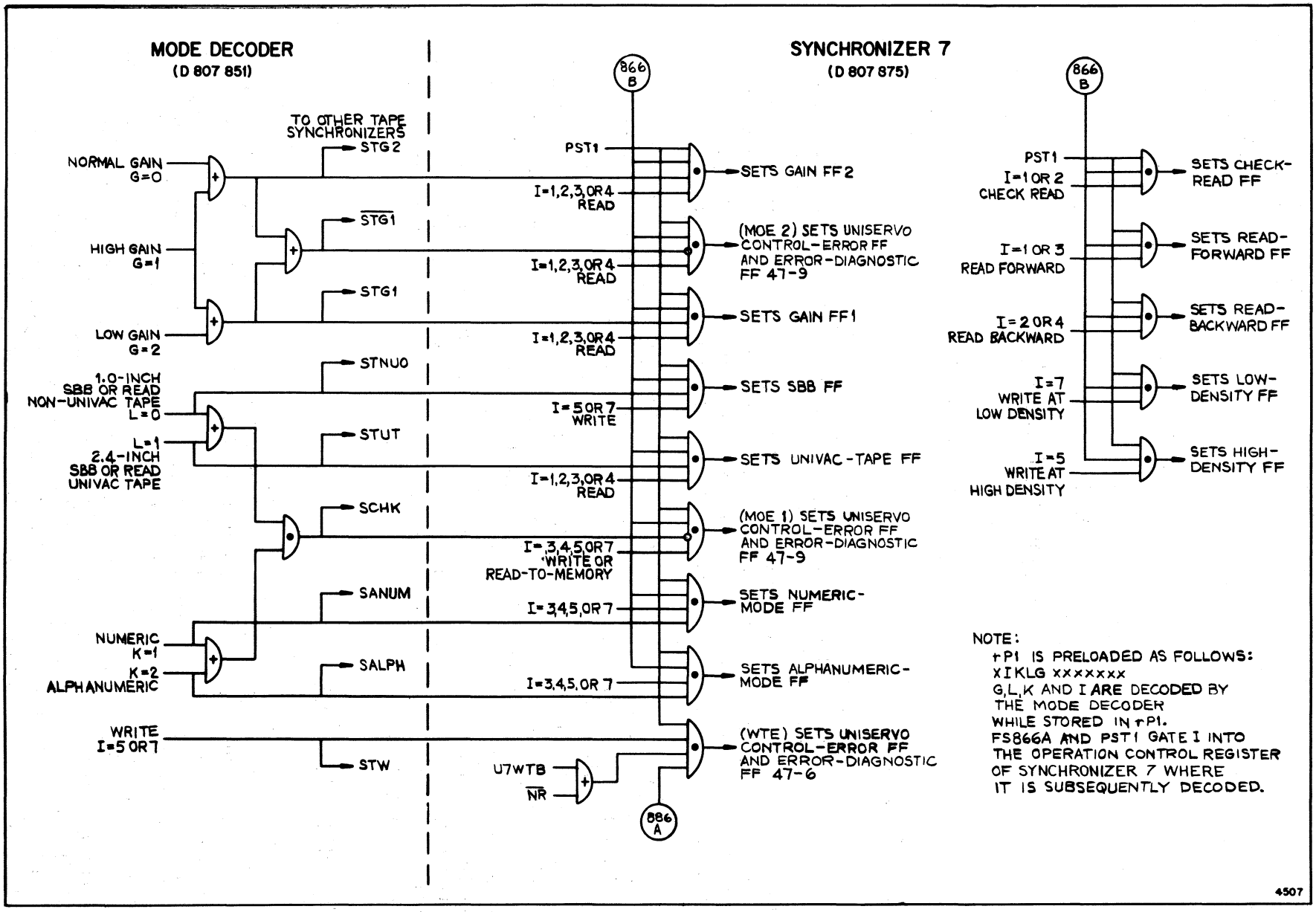


Figure 3-1. Mode Decoder, Simplified Diagram

by the mode designator and its number. For example, K = 2 represents the decoding of a K digit of 2 stored in register P1. The digits G, L, K, and I, shown in the mode decoder portion of figure 3-1, are stored in and decoded from register P1; the digit I, shown in the Synchronizer 7 portion of figure 3-1, is stored in and decoded from the operation-control register in the Uniservo control circuits of Synchronizer 7.

The mode flip-flops control write, read, and check-read operations in accordance with the modes specified by the program. Functionally, the numeric and alphanumeric mode flip-flops are part of the synchronizer read-write control circuits (section 4); the SBB, low-density, and high-density mode flip-flops are part of the write circuits (section 5); and the gain, read-direction, check-read, and Univac-read mode flip-flops are part of the read circuits (section 6).

3-3. TAPE TIMING SIGNAL GENERATOR IN THE LARC SYSTEM, SERIAL 1

The tape timing signal generator produces timing signals that perform the following functions:

(1) Define unique time intervals for each tape synchronizer during which character-read cycles can begin, thereby ensuring proper time-sharing of the Univac-to-Larc translator and input checker.

(2) Define unique time intervals for each tape synchronizer for beginning character-write cycles, thereby ensuring proper time-sharing of the Larc-to-Univac translator and output checker.

(3) Define, in accordance with the pulse density specified by the processor program, the length of and distance between successive pulses written on tape.

(4) Step the clearing of the tape output buffer registers and define the time at the beginning of a write operation when the output buffer registers of a tape synchronizer may be cleared without interfering with a write operation on another tape synchronizer.

In addition to producing timing signals for the preceding functions, the tape timing signal generator produces a number of signals derived from standard timing signals generated by the main cycling unit in the central processor. Since these timing signals are standard and are merely buffed together, passed through a pulseformer, or amplified to build up sufficient driving power for the needs of the tape synchronizer system, they are not described further.

3-4. TAPE CYCLING UNIT

The main section of the tape timing signal generator consists of six flip-flops connected as a ring counter. (See figure 3-2.) At any one time only one of these flip-flops should be set. Every 4 μsec the ring of flip-flops is stepped by a standard T7 timing signal which clears (attempts to reset) all six flip-flops and simultaneously gates the output of each flip-flop to the next one in line. A pulse gated into one of the flip-flops is

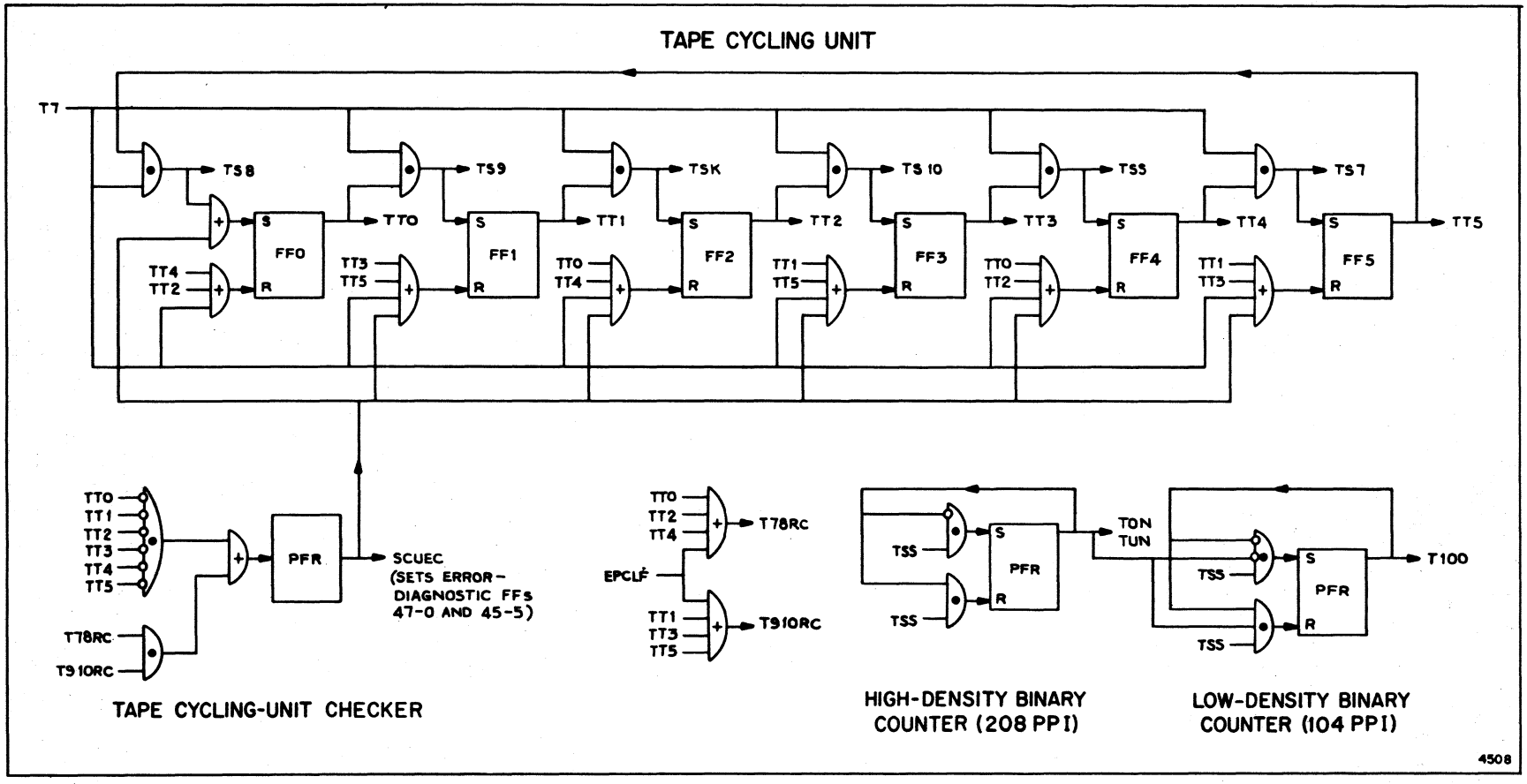


Figure 3-2. Tape Timing Signal Generator in Larc System, Serial 1 (D807 850)

transferred to the next in line 4 μsec later, eventually traveling completely around the ring and into the first flip-flop 24 μsec after it was last introduced. As long as the main cycling unit in the central processor is operating, this cycle continues indefinitely.

The outputs of the six flip-flops (FF0 through FF5) are designated TT0 through TT5. (See upper portion of figure 3-4.) Each occurs (is low) once every 24 μsec beginning at T0, and lasts for 4 μsec. The even-numbered outputs, TT0, TT2, and TT4 are buffed together to generate the timing signal T78RC and the odd-numbered outputs are buffed together to generate T910RC. The T78RC and T910RC signals change state every 4 μsec and are opposite in phase.

The 0.5 μsec pulses that set flip-flops FF0 through FF5 are designated TS8, TS9, TSK, TS10, TSS, and TS7, respectively. Each TS pulse occurs once every 24 μsec, at T7. They are separated from one another by 4 μsec intervals.

3-5. BINARY COUNTERS

A binary counter, made up of standard pulseformer and gating elements, is stepped every 24 μsec by the TSS signal. The outputs of the binary counter are designated T0N and TUN. They change state every 24 μsec and correspond to the 208-PPI tape-writing density. The output of the high-density binary counter is gated with the TSS signal to step a second binary counter, the output of which, designated T100, changes state once every 48 μsec and corresponds to the 104-PPI tape-writing density.

3-6. TAPE CYCLING UNIT ERROR CHECKING

The tape cycling unit is checked continuously to ensure that only one pulse is present in the ring of flip-flops. If no pulse is present or if more than one pulse is present, an error signal is generated which sets appropriate error flip-flops and automatically clears and restarts the tape cycling unit.

The absence of a pulse is detected by gating together outputs of all six flip-flops. If none of the flip-flops is set, an SCUEC error signal is generated. The SCUEC error signal is also produced when the T78RC and the T910RC timing signals are present (low) simultaneously. This indicates that two or more cycling unit flip-flops are set simultaneously, one of which is an even-numbered flip-flop that generates the T78RC signal and another an odd-numbered flip-flop that generates the T910RC signal. The error signal is generated indirectly when two or more even-numbered flip-flops or two or more odd-numbered flip-flops are set simultaneously. Each even-numbered flip-flop, when set, always resets the remaining two even-numbered flip-flops. Similarly, each odd-numbered flip-flop, when set, always resets the remaining two odd-numbered flip-flops. If more than one even-numbered flip-flop or more than one odd-numbered flip-flop were set, they would, therefore, reset one another and clear the cyling unit. The error signal would then be generated by the gate that detects the absence of a pulse in the cycling unit.

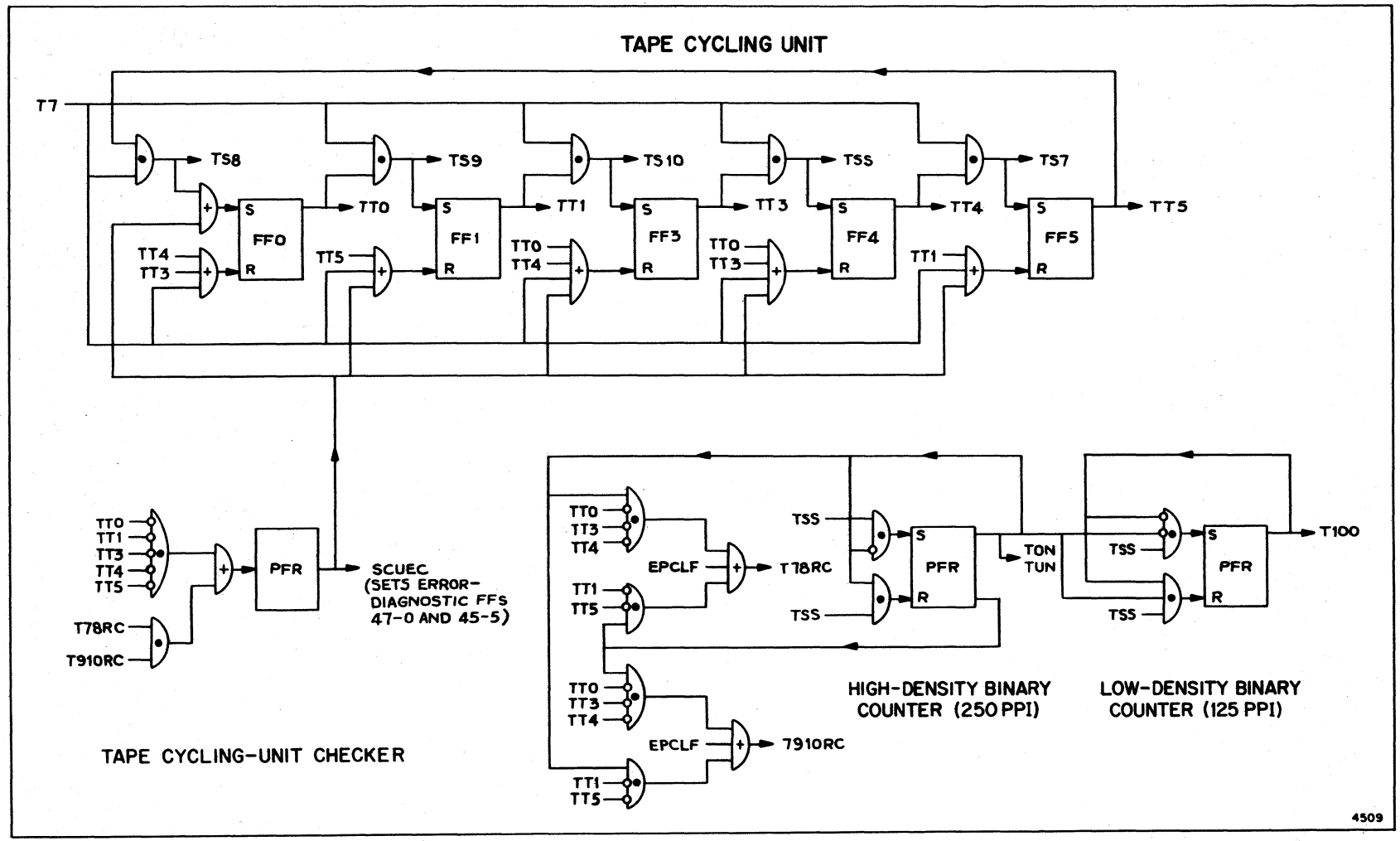


Figure 3-3. Tape Timing Signal Generator in Larc System, Serial 2 (D807 950)

The SCUEC error signal clears (resets) all six flip-flops in the cycling unit and sets FF0, thereby automatically restarting the cycle. A tape cycling unit error, depending on the operating state of the synchronizer when the timing error occurs, may or may not produce reading or writing error conditions in any one or all of the tape synchronizers. Since any one of the tape synchronizers may be affected by an error in the tape cycling unit, the SCUEC error signal alerts the program by setting the main cycling unit error flip-flop which causes an automatic transfer (RU) of the program to the error routine. To aid the program in classifying the error, the SCUEC signal also sets the tape-sprocket-generator error diagnostic flip-flop.

When the main cycling unit in the central processor is cleared and started by the cycling-unit-clear switch on the engineer's console the EPCLF signal artificially generates the SCUEC signal by simultaneously jamming the T78RC and T910RC signals to their low state. The SCUEC signal, in turn, clears and restarts the tape cycling unit.

3-7. TAPE TIMING SIGNAL GENERATOR IN THE LARC SYSTEM, SERIAL 2

This paragraph presupposes a knowledge of the function of the tape timing signal generator used in the Larc System, Serial 1; if such is not the case, it is necessary to read paragraph 3-3 in its entirety before continuing further.

The tape timing signal generator used in the Larc System, Serial 1 was modified for use in the Larc System, Serial 2. The modifications have the effect of increasing the writing densities from 104 and 208 PPI to 125 and 250 PPI, respectively. The differences in the two generators are covered in the following paragraphs, headings 3-8 through 3-11. (See figures 3-2 and 3-3.)

3-8. TAPE CYCLING UNIT

FF2 present in the tape cycling unit of the generator in the Larc System, Serial 1, is omitted from the tape cycling unit of the generator in the Larc System, Serial 2. Consequently, signals TT2 and TSK are not generated (figure 3-4) and the timing cycle is reduced from 24 to 20 μsec.

3-9. BINARY COUNTERS

Since the timing cycle is reduced to 20 μsec, the high-density binary counter is stepped once every 20 μsec. Its outputs (TON and TUN) change state every 20 μsec and correspond to the 250-PPI tape writing density. Similarly, the low-density binary counter is stepped once every 40 μsec; its output (T100) changes state once every 40 μsec and corresponds to the 125-PPI tape writing density.

3-10. GENERATION OF TIMING SIGNALS T78RC and T910RC

To perform their function properly the timing signals T78RC and T910RC must change state each 4 μsec and be opposite in phase. Since the Larc

System, Serial 2 tape cycling unit contains an odd number of flip-flops, these signals cannot be generated directly from the TT outputs of the flip-flops as they are in the Larc System, Serial 1. Instead, T78RC and T910RC are generated alternately by gating outputs of the high-density binary counter with the TT timing pulses. When the binary counter is in one state, TON and TUN low, the T78RC signal is generated at TT1 and TT5 and the T910RC signal is generated at TT0, TT3, and TT4. When the binary counter is in the opposite state, TON and TUN high, the T910RC signal is generated at TT1 and TT5 and the T78RC signal is generated at TT0, TT3, and TT4. Consequently, the T78RC and T910RC signals, like the equivalent signals in the Larc System, Serial 1 change state every 4 μsec and are opposite in phase.

3-11. CYCLING UNIT ERROR CHECKING

Because of the differences in the timing signal generator the cycling unit error-checking in the Larc System, Serial 2 differs somewhat from that in the Larc System, Serial 1. The tape cycling unit is continuously and directly checked to ensure that a pulse is always present in the ring of flip-flops and is indirectly checked to ensure that not more than one pulse is present in the ring. If no pulse or more than one pulse is present, an SCUEC error signal is generated which sets appropriate error flip-flops and automatically clears and restarts the tape cycling unit.

The absence of a pulse is detected by gating together outputs of all five flip-flops. If none of the flip-flops are set, an SCUEC error signal is generated immediately. As in the Larc System, Serial 1 the T78RC and T910RC signals are gated together to generate SCUEC when both are low simultaneously. However, because of the way in which T78RC and T910RC are generated, this does not necessarily indicate, as it does in the Larc System, Serial 1, that two or more cycling unit flip-flops are set simultaneously. In the case where two, and in some cases more than two, flip-flops are set simultaneously, SCUEC is generated as follows: When FF0, FF3, or FF4 is set, it resets the remaining two flip-flops in the group; similarly, when FF1 is set, it resets FF5, and when FF5 is set, it resets FF1. If more than one of the flip-flops, FF0, FF3, and FF4 were set or if both FF1 and FF5 were set, they would immediately reset one another and the SCUEC error signal would be generated by the gate that detects the absence of a pulse in the cycling unit. If one of the flip-flops, FF0, FF3, and FF4 and either FF1 or FF5 were set simultaneously, the cycling unit would clear itself after being stepped once or twice and would thus generate the SCUEC error signal.

3-12. FUNCTION OF TIMING SIGNAL GENERATOR OUTPUTS

The description under this heading is applicable to both Larc Systems, Serials 1 and 2. Its purpose is not only to provide information concerning the function of the timing signals, but also to provide background information for understanding the time-sharing of the Larc-to-Univac and Univac-to-Larc translators.

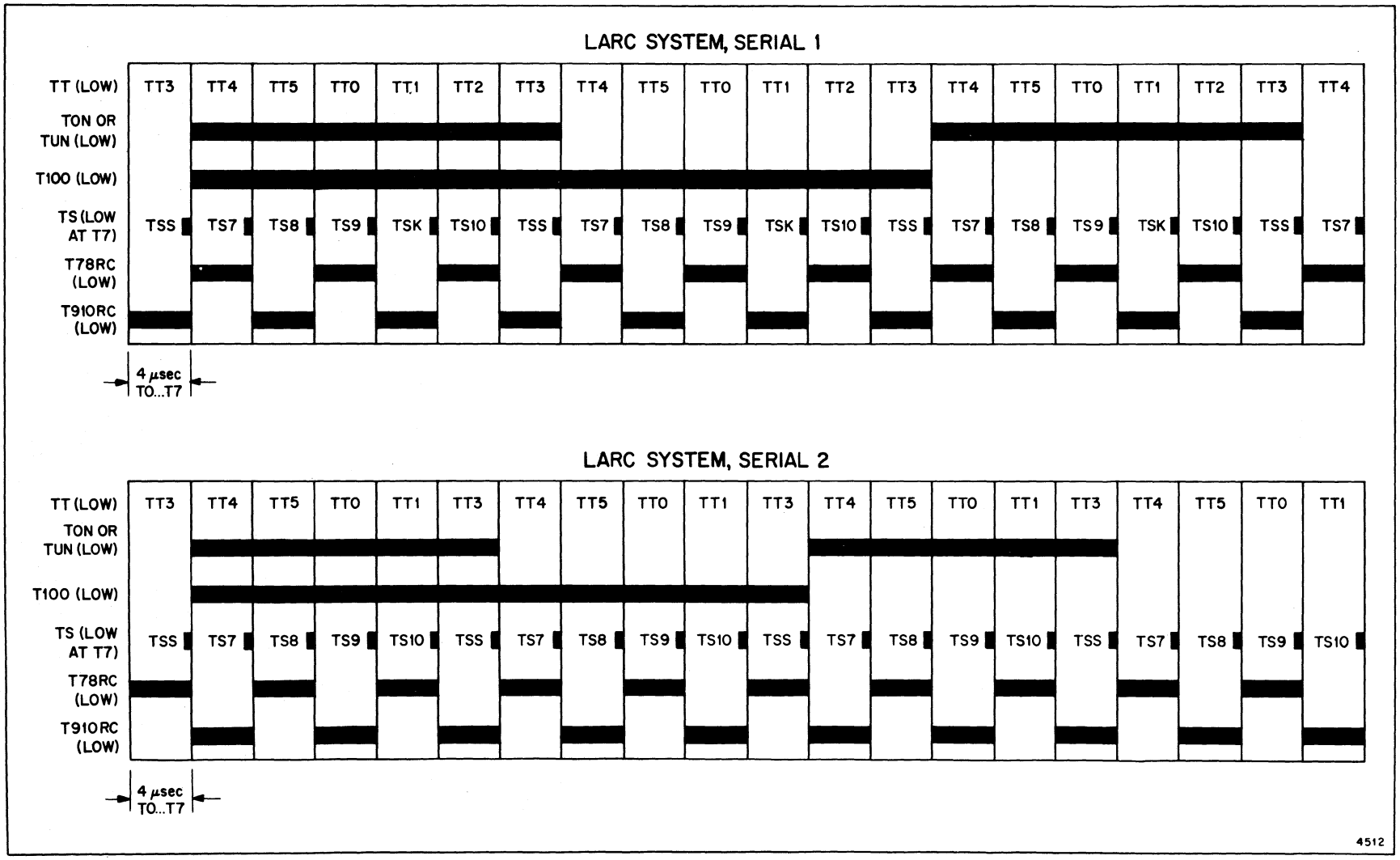


Figure 3-4. Tape Timing Signal Generator Outputs (Larc System, Serials 1 and 2)

3-13. TAPE READ CYCLE TIMING

The T78RC and T910RC signal outputs of the timing signal generator (figure 3-4) time the setting of tape-read-cycle flip-flops in the read circuits of the synchronizers. Each synchronizer has a tape-read-cycle flip-flop that is set after the arrival of a Univac character over the tape-read bus from the Uniservo tape unit. When set, the tape-read-cycle flip-flop controls the gating of the character through the Univac-to-Larc translator, the stepping of the digit counter, and the writing of the translated character into an input buffer register. To ensure proper time-sharing of the translator among the four synchronizers, the tape-read-cycle flip-flops are timed so that more than one cannot be in the set state at the same time. The tape-read-cycle flip-flop of Synchronizer 7 can be set only at T1 of T78RC and is reset at the following T5. The tape-read-cycle flip-flop of Synchronizer 8 can be set only at T5 of T78RC and is reset at the following T1. Similarly, the tape-read-cycle flip-flops of Synchronizers 9 and 10 can be set only at T1 and T5, respectively, of T910RC and are reset 2 μsec after being set. Consequently, the read cycles of the four synchronizers never coincide. This fact is illustrated in figure 6-2 which shows the timing of four successive read cycles, each for a different tape synchronizer. The time between settings of a particular tape-read-cycle flip-flop depends on the frequency at which digits are received from the Uniservo tape unit. This, in turn, depends on the pulse density of the tape being read.

3-14. TAPE WRITE CYCLE TIMING

The TS signal together with the TON (or TUN) and T100 signals time the setting of tape-write-cycle flip-flops in the write circuits of the synchronizers. Each synchronizer has a tape-write-cycle flip-flop that is set for 4 μsec when it is time to transmit a character over the tape-write bus to the Uniservo tape unit. When set, the tape-write-cycle flip-flop controls the stepping of the digit counter, the reading of a digit (or digit pair) out of an output buffer register, the translation of the digit through the Larc-to-Univac translator, and the gating of the digit into the output flip-flops that drive the tape-write-bus amplifiers.

The tape-write-cycle flip-flop in each synchronizer is set during the low half-cycle of the TON signal by the TS signal whose number corresponds to the number of the synchronizer; that is, TS7, TS8, TS9, and TS10 set the tape-write-cycle flip-flops in Synchronizers 7, 8, 9, and 10, respectively. Since the TS signals are at least 4 μsec apart and each flip-flop is reset after 4 μsec, only one tape write cycle at a time will be in the set state, thus ensuring proper time-sharing of the Larc-to-Univac translator and output checker.

During a high-density write operation, a tape-write-cycle flip-flop is alerted only during the low half-cycle of the TON signal. It is therefore set by its associated TS signal once every 48 μsec in Larc System, Serial 1 and once every 40 μsec in Larc System, Serial 2. This corresponds to the time required to record a pulse and leave a space between pulses when writing at high density. During a low-density write operation, T100 as well as TON must be low before the tape-write-cycle flip-flop is set by its associated TS signal; therefore, the flip-flop will set once every 96 μsec for Larc System, Serial 1 and once every 80 μsec for Larc System, Serial 2,

which is the time required to record a pulse and leave a space between pulses when writing at low density.

The TS signals are also used to control the pulse time duration of a character being written. (Refer to heading 5-10.)

3-15. CLEAR CYCLE TIMING

The fact that only one tape-write-cycle flip-flop at a time is set ensures proper time-sharing among the synchronizers of the Larc-to-Univac translator and output checker during simultaneous write operations. However, a digit that is read from any of the tape-output buffer registers feeds directly into the translator and therefore means must be provided to ensure that the clearing of an output buffer register by one synchronizer does not interfere with the translation of a digit during a write cycle on another synchronizer. The output buffer registers of a tape synchronizer are always cleared at the beginning of a write operation to ensure that no extraneous data remains in the registers from a previous operation. The clearing of the output buffer registers is controlled by an output-buffer-clear flip-flop in the write circuits of the tape synchronizer. Before the synchronizer begins writing on tape, its buffer-register-clear flip-flop is set at time TSS of TON and is reset by the following TS signal. Thus, a clear cycle never overlaps a tape write cycle. During the clear cycle, the timing signals TT4, TT5, TT0, TT1, and TT3 control the clearing of digits from the output buffer registers. To avoid possible simultaneous clearing of several registers, the output-buffer-clear flip-flops are interlocked so that not more than one is set at a time. This reduces the drive requirements on the TT timing pulses which control the clearing of the registers.

3-16. LARC-TO-UNIVAC TRANSLATOR AND OUTPUT CHECKER

All information read from or recorded on magnetic tape by the Larc System is in the Univac seven-bit code, consisting of four XS-3 bits, two zone bits, and a check bit. The numbers 0 through 9 and the non-numeric characters plus (+), minus (-), space (∧), period (.), and ignore (/) are represented in the Larc System by a one-digit (five-bit) code combination. Alphanumeric information is represented in the Larc System by a two-digit (ten-bit) combination composed of two consecutive one-digit numeric combinations. For every character represented in the Univac XS-3 code there is a Larc two-digit code equivalent. For Univac code combinations representing the numbers 0 through 9 and the non-numeric characters plus, minus, space, period and ignore, there is a one-digit as well as a two-digit Larc code equivalent.

The Larc one- and two-digit codes are shown in decimal form in table 3-1 arranged in columns and rows according to the equivalent Univac zone and XS-3 combinations. The shaded areas of the table denote the Larc code combinations that have a 1 check bit when represented in the Univac code. For ease of reference, both the standard and memory Larc codes are listed in the last three columns of the table. All inputs to the Larc-to-Univac translator are in the Larc standard code.

The Larc-to-Univac translator is time-shared to translate output data for all of the four possible tape synchronizers in the system. The

translator receives Larc one- or two-digit code combinations directly from the tape synchronizer output buffer registers and translates them into Univac code combinations that are transmitted to the Uniservo tape unit and written on tape. A Larc code combination is read from an output buffer register only during a tape write cycle or an output-buffer-clear cycle in one of the tape synchronizers. Since the tape write cycles and output-buffer-clear cycles of the four synchronizers never occur simultaneously, only one Larc code one-digit or two-digit combination at a time is received at the input to the translator.

During each tape write cycle outputs of the translator are checked for errors. If an error is detected, error signals are generated which set appropriate error flip-flops and the Univac code combination 1111111 is written on tape in place of the erroneously translated combination.

The translator (figure 3-5) consists of the following circuits:

(1) Five most-significiant-digit (MSD) flip-flops and five least-significant-digit (LSD) pulseformers that receive one- or two-digit combinations from the tape output buffer registers and provide inputs to the translator. The flip-flops and pulseformers together delay the LSD of a two-digit combination (which is received first) until the MSD is received, thereby providing simultaneous inputs to the translator.

(2) A one-digit-translate flip-flop which is set during a tape write cycle of a tape synchronizer operating in the numeric (one-digit) mode. The flip-flop alerts gates within the translator that are required to be active only during a one-digit translation.

(3) A set of LSD decoding gates that decode a one-digit combination or the LSD of a two-digit combination.

(4) A set of non-numeric decoding gates that are active only during a one-digit translation to decode the non-numeric combinations (ignore, space, minus, period, and plus) of the Larc one-digit code.

(5) A set of MSD decoding gates which decode the MSD of a two-digit combination.

(6) A set of buffers, represented in matrix form in figure 3-5, which encode outputs of the decoders to generate the first six bits of the Univac code as well as check-bit signals that are gated in the synchronizer to produce the seventh bit.

(7) A tape output odd-even checker which checks outputs of the translator against their independently generated logical inverse.

3-17. TRANSLATOR INPUTS

During a tape write cycle of a tape synchronizer operating in the one-digit numeric mode, a digit is read out of the output buffer register at T4. During a tape write cycle of a tape synchronizer operating in the two-digit alphanumeric mode, the LSD is read out of the buffer register at T4

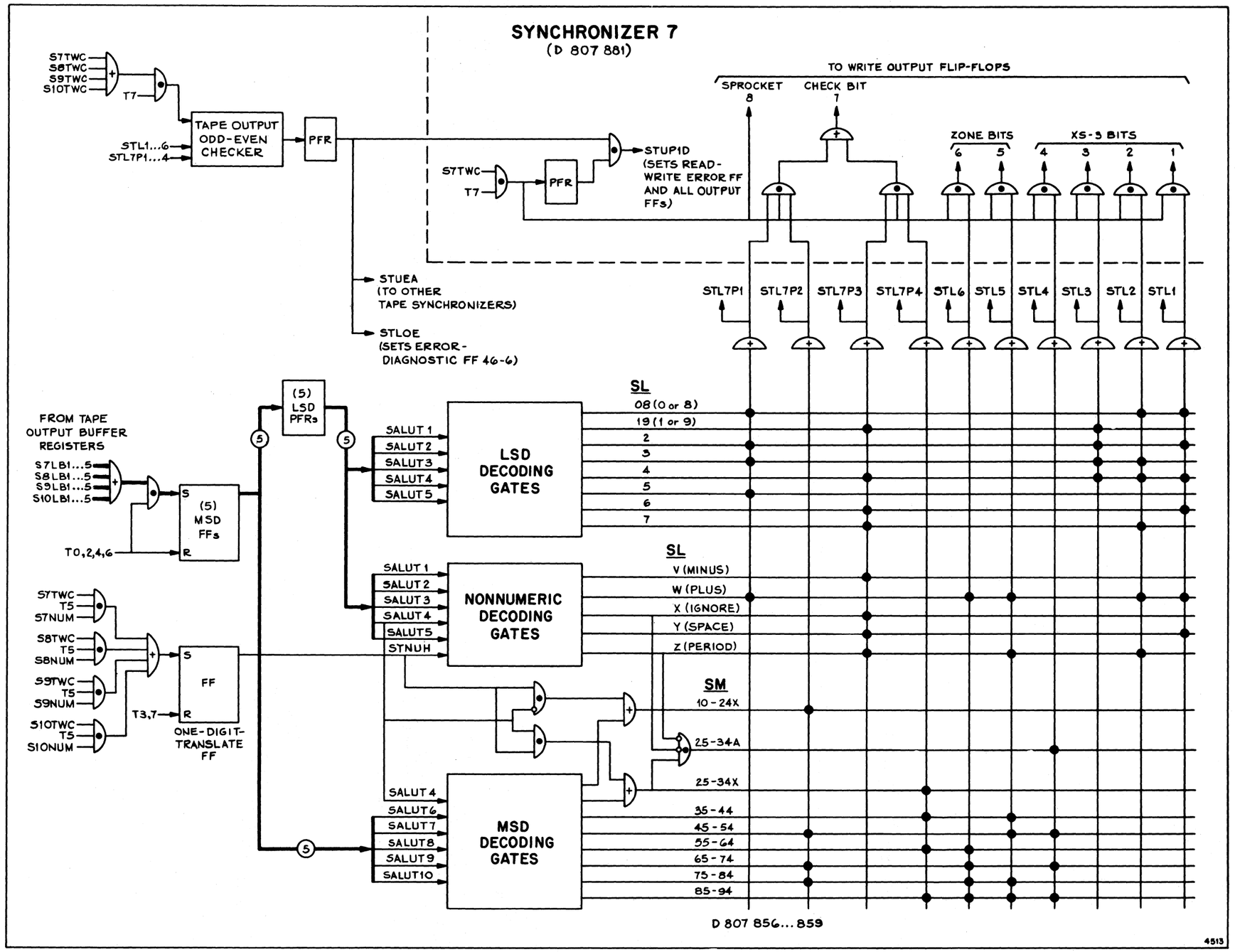


Figure 3-5. Larc-to-Univac Translator and Output Checker

and the MSD is read out 1 μsec later, at T6. Since both digits of a two-digit combination must be translated simultaneously, the LSD must be delayed to await the arrival of the MSD before being translated.

The outputs of both halves of the output buffer registers of all four tape synchronizers are buffed together at the input to the five MSD flip-flops. Since only one digit at a time is read from either half of the eight tape output buffer registers, only one digit at a time will appear at the input of the MSD flip-flops. The flip-flops are timed to gate a digit in, and to clear, at T0, T2, T4, or T6.

A one-digit combination or the LSD of a two-digit combination is received and gated into the MSD flip-flops at T4 and cleared at T6; therefore, the digit is present at the output of the flip-flops at T5 and T6. Since the five MSD flip-flops feed directly into the five LSD pulseformers, the same digit is present at the output of the pulseformers at T6 and T7.

The actual translation, whether one-digit or two-digit, takes place at T7. During a one-digit translation, the digit is present at the output of the LSD pulseformers at T7 and the MSD flip-flops are cleared. During a two-digit alphanumeric translation, the LSD is followed by the MSD which is gated into the MSD flip-flops when they are cleared at T6. The MSD therefore, is present at the output of the MSD flip-flops at T7, concurrently with the LSD at the output of the LSD pulseformers.

3-18. ONE-DIGIT-TRANSLATE FLIP-FLOP

The one-digit-translate flip-flop is set at T5 during a tape write cycle of a tape synchronizer operating in the numeric (one-digit) mode and is reset at T7. The flip-flop differentiates between a one- and two-digit translation by alerting a number of gates in the translator so that they are operative only during a one-digit translation.

3-19. DECODING GATES

A one-digit combination, other than a non-numeric combination, or the LSD of a two-digit combination, is decoded from the LSD pulseformers to generate one of the SL signals, 08, 19, 2, 3, 4, 5, 6, or 7. The number of the SL signal signifies the digit which generates it; for example, SL08 is generated by a 0 or 8 in Larc code, SL2 is generated by a 2, and so on.

A non-numeric combination of the Larc one-digit code is decoded to generate one of the SL signals, V, W, X, Y, or Z. The name of the non-numeric digit generating each signal is shown in parentheses in figure 3-5. The gates that decode the non-numeric combinations are inhibited by the one-digit-translate flip-flop and therefore do not generate an output when a two-digit combination is being translated.

The MSD of a two-digit combination and the fourth (binary) bit of the LSD are decoded to generate an SM signal. The number of the SM signal indicates the two-digit combinations that generate it; for example, SM3544A is generated by all two-digit combinations between 35 and 44, inclusive.

During a one-digit translation, the MSD flip-flops are cleared; consequently, no outputs are generated by the MSD decoding gates. However, one of the signals, SM1024X, SM1024A, SM2534X, and SM2534A may be generated during a one-digit as well as a two-digit translation. SM1024X is produced during a one-digit translation by all combinations containing a binary 0 in the fourth bit position. SM1024A is produced by the same combinations with the exception of the non-numeric combination, plus. SM2534X is produced by all one-digit combinations containing a binary 1 in the fourth bit position. SM2534A is produced by the same combinations with the exception of the non-numeric combinations ignore and period. SM1024A is not shown in figure 3-5 since it is used only for the purpose of generating the inverse of translator outputs for checking purposes.

3-20. ENCODING BUFFERS

The SL and SM signals are encoded into Univac code combinations by a set of buffers, represented in matrix form in figure 3-5. The outputs STL1 through STL6 of the matrix represent binary 1's in bit positions 1 through 6 of the Univac code. The STL7P1 output gated with STL7P2, and STL7P3 gated with STL7P4 represent a 1 check bit in bit position 7 of the Univac code. The gating together of the STL7P signals takes place in the individual synchronizer performing a tape write cycle. For purposes of error detection, circuits in the translator also generate the logical inverse of the signals STL1 through STL6. These circuits and signals are essentially redundant and therefore are not shown in figure 3-5. It may be noted that STL7P1 is the logical inverse of STL7P3 and STL7P2 is the logical inverse of STL7P4. Thus, the inverse of all of the outputs are generated.

The first three bits of the Univac code, represented by the signals STL1, STL2, and STL3, are encoded by buffing the SL signals generated by the LSD and non-numeric decoding gates. STL1, for example, is generated by buffing all of the SL signals decoded from either the one- or two-digit combinations that produce a binary 1 in bit 1 position of the Univac code.

The fourth bit of the Univac code (STL4) is encoded by buffing together the SM signals 2534, 4554, 6574, and 8594. One of these signals is produced by any of the one- or two-digit combinations shown in rows 9 through 16 of table 3-1, all of which produce a binary 1 in bit position 4 of the Univac XS-3 code.

The zone bits (STL5 and STL6) of the Univac code are encoded from the SM signals and from the SL signals generated by the non-numeric decoding gates. STL5 is produced by SLW, SLZ, SM3544, SM4554, SM7584, and SM8594 which, in turn, are produced by the one- or two-digit combinations shown in the zone 01 and zone 11 columns of table 3-1. STL6 is produced by SLW, SM5564, SM6574, SM7584, and SM8594 which, in turn, are produced by the combination shown in the zone 10 and zone 11 columns of table 3-1.

During a two-digit translation STL7P2 is produced by any combination in the ranges 10-24, 45-54, 65-74, and 75-84; STL7P1 is produced by combinations in these ranges that would result in a 1 check bit when translated to Univac code; that is, combinations with an LSD of 0, 8, 2, 3, or 5. Consequently, a 1 check-bit signal is produced by gating together the STL7P2 and STL7P1 signals. Combinations generating both signals are denoted in table 3-1 by the shaded areas in rows 1 through 8 of the zone 00 and 11

columns and in rows 9 through 16 of the zone 01 and 10 columns. Similarly, STL7P4 is generated by any two-digit combination in the ranges 25-34, 35-44, 55-64, and 85-94 and STL7P3 is generated by combinations in these ranges (with an LSD of 1, 9, 4, 6, or 7) that result in a 1 check bit in Univac code. Both signals are generated by the combinations which are denoted in table 3-1 by shaded areas in rows 9 through 16 of the zone 00 and 11 columns and rows 1 through 8 of the zone 01 and 10 columns.

During a one-digit translation, the STL7P2 signal is generated by a combination containing a binary 0 in the fourth bit position and STL7P1 is generated by 0, 8, 2, 3, 5, or plus. Both signals are produced by 0, 2, 3, or plus, all of which result in a 1 check bit when translated into Univac code. The STL7P4 signal is generated by a one-digit combination containing a binary 1 in the fourth bit position and STL7P3 by a 1, 9, 4, 6, 7, minus, ignore, space, and period. Both signals are generated by 6, 7, 9, ignore, and period, all of which result in a 1 check bit in Univac code.

Outputs from the translator go to all of the synchronizers but are only gated at T7 into the write-output flip-flops of the specified tape synchronizer performing a tape write cycle. In the process, STL7P1 is gated with STL7P2 and STL7P3 is gated with STL7P4.

3-21. TAPE OUTPUT ODD-EVEN CHECKER

The tape output odd-even checker is alerted at T7 during a synchronizer tape write cycle. The checker simply compares the outputs of the translator with their independently generated logical inverse. If the two sets of outputs do not agree, error signals STLOE and STUEA are produced at T0. The STLOE signal sets the output odd-even diagnostic flip-flop in the central processor and the STUEA signal generates an STUPnD* signal in the synchronizer performing the tape write cycle. The STUPnD signal sets the synchronizer master error flip-flop and jams all the write-output flip-flops to the set state, thereby causing the code combination of all 1's (1111111) to be written on tape in place of the combination just translated.

3-22. UNIVAC-TO-LARC TRANSLATOR AND INPUT CHECKER

All information read from or recorded on magnetic tape by the Larc System is in the Univac seven-bit code consisting of four XS-3 bits, two zone bits, and a check bit. The numbers 0 through 9 and the non-numeric characters plus (+), minus (-), space (∧), period (.) and ignore (/) are represented in the Larc System by a one-digit (five-bit) code combination. Alphanumeric information is represented in the Larc code by a two-digit (ten-bit) combination composed of two consecutive one-digit numeric combinations. For every character represented in Univac code there is a two-digit code equivalent. For Univac code combinations representing the numbers 0 through 9 and the non-numeric characters plus, minus, space, period, and ignore, there is a one-digit as well as a two-digit Larc code equivalent.

* Letter n represents a tape synchronizer number 1, 2, 3, or 4 which corresponds to synchronizer number 7, 8, 9, and 10, respectively.

The Larc one- and two-digit codes are shown in decimal form in table 3-1 arranged in columns and rows according to the equivalent Univac zone and XS-3 combinations. The shaded areas of the table denote the Larc code combinations that have a 1 check bit when represented in the Univac code. For ease of reference both the Larc standard and Larc memory codes are listed in the last three columns of the table. The Univac-to-Larc translator translates from Univac code to Larc memory code. Whenever reference is made to the Larc code in the remainder of this section, the Larc memory code is intended.

The Univac-to-Larc translator is time-shared to translate input data for all of the four possible tape synchronizers in the system. The translator receives Univac code combinations read from tape and translates them into Larc one- or two-digit memory-code combinations that are written into the tape synchronizer input buffer registers. A Univac character is gated into the translator only during a tape read cycle of a synchronizer which can occur only after the character and its accompanying sprocket pulse is received from the Uniservo tape unit. Since the tape read cycles of the tape synchronizers never occur simultaneously, only one Univac character at a time is received at the input to the translator.

During each tape read cycle, an odd-even check is performed on the Univac character read from tape. The odd-even checker is operative during a read and check-read operation regardless of whether the check-read operation is controlled by a tape synchronizer or by the tape positioning checker. During a one-digit translation each Univac character read from tape is additionally checked to ensure that it is a translatable combination; that is, that it has an equivalent Larc one-digit code combination. The translatability check is not operative during a check-read operation. If an untranslatable Univac character is detected, the Larc one-digit code combination for a plus is jammed into the tape input buffer register in place of the translated combination.

The Univac-to-Larc translator and input checker (figure 3-6) consists of the following circuits:

(1) Seven input pulseformers that receive a Univac code combination from the skew flip-flops of a tape synchronizer at the beginning of a tape read cycle and provide inputs to the translator and the checkers associated with the translator.

(2) An auxiliary decoding matrix that partially decodes the Univac character and provides inputs to both the MSD and LSD translation matrixes.

(3) An MSD translation matrix that translates signals from the translator input pulseformers and the auxiliary decoding matrix to generate the MSD of the Larc two-digit code.

(4) Five MSD flip-flops that store the translated MSD of the Larc two-digit code until the input buffer register in ready to accept the MSD by way of the buffer register input pulseformers.

(5) An LSD translation matrix that translates signals from the translator input pulseformers and the auxiliary decoding matrix to generate the least significant digit of the Larc two-digit code.

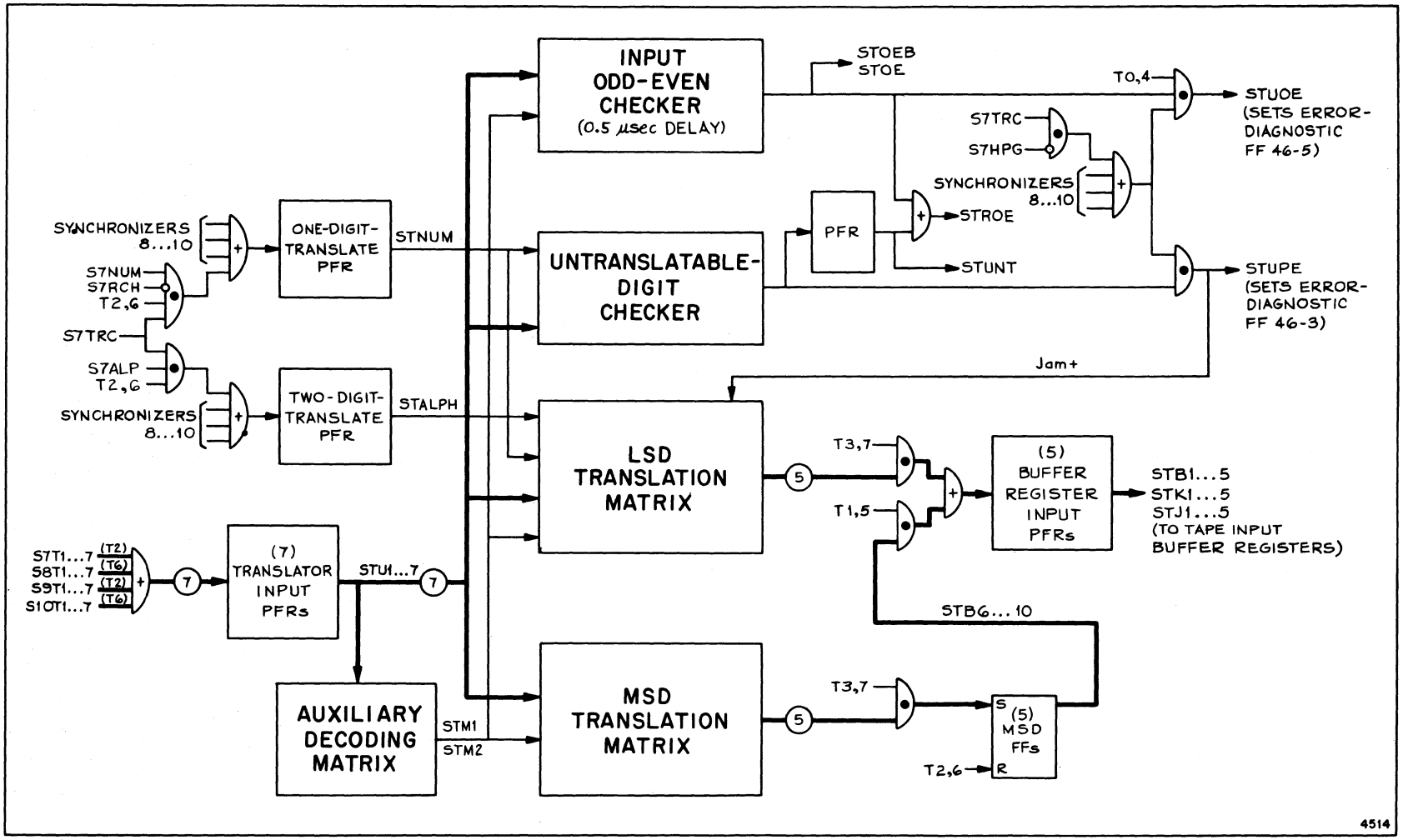


Figure 3-6. Univac-to-Larc Translator and Input Checker (D 807 853...855)

(6) A set of five buffer register input pulseformers which, depending on the translation mode, receives either a Larc one-digit combination or the LSD of a Larc two-digit combination followed by the MSD, and drives the input amplifiers of the tape input buffer registers.

(7) One-digit- and two-digit-translate pulseformers. The one-digit-translate pulseformer alerts gates in the LSD translation matrix that are required to be active only during a one-digit translation and alerts a gate in the checking circuits that detects untranslatable one-digit combinations. The pulseformer alerts these gates during a tape read cycle of a tape synchronizer performing a numeric-read operation; it is inhibited during a tape read cycle of a synchronizer performing a check-read operation.

The two-digit-translate pulseformer alerts gates in the LSD translation matrix that are required to be active only during a two-digit translation. It alerts these gates during a tape read cycle of a tape synchronizer operating in the alphanumeric mode.

(8) A time-shared, odd-even checker that performs a parity check of each Univac character read from tape as well as a check on the auxiliary decoder.

(9) An unstranslatable-digit checker that performs a check during a one-digit translation to detect if the Univac-code digit being translated is translatable into a Larc one-digit combination.

3-23. TIMING

The translation timing for four read cycles in succession is shown in figure 6-2. A translation for Synchronizer 7 is always separated by an increment of 4 μsec from a translation for Synchronizer 9; likewise, a translation for Synchronizer 8 is separated by 4 μsec from a translation for Synchronizer 10. Otherwise, the translation timing for Synchronizer 7 is the same as that for 9 and the timing for Synchronizer 8 is the same as that for 10.

A Univac character is transferred to the translator input pulseformers from the skew flip-flops of Synchronizer 7 or 9 at T2 or from the skew flip-flops of Synchronizer 8 or 10 at T6. The actual translation in both the LSD and MSD translation matrixes occurs at T3 for Synchronizer 7 or 9 or at T7 for Synchronizer 8 or 10. A translated one-digit code combination or the LSD of a two-digit combination is immediately gated into the buffer register input pulseformers and is then written into an input buffer register at T4 for Synchronizer 7 or 9 or at T0 for Synchronizer 8 or 10. The translated MSD of a two-digit combination is temporarily stored in the MSD flip-flops before being gated into the buffer register input pulseformers at T5 for Synchronizer 7 or 9 or at T1 for Synchronizer 8 or 10. The MSD is then written into the input buffer register 1 μsec after the LSD at T6 for Synchronizer 7 or 9 or at T2 for Synchronizer 8 or 10.

3-24. AUXILIARY DECODING

The four bits of the Univac XS-3 code (STU1 through STU4) are decoded by the auxiliary decoding matrix to generate one of the signals, STM1 or STM2. The STM1 signal is generated by the Univac XS-3 code combinations shown in rows 4 through 13 of table 3-1. Each of these combinations is the equivalent of either a Larc two-digit combination having an even MSD or one of the Larc one-digit combinations for 0 through 9, or plus. The STM2 signal is generated by the Univac XS-3 code combinations shown in rows 1 through 3 and rows 14 through 16 of table 3-1. Each of these combinations is the equivalent of either a Larc two-digit combination having an odd MSD or one of the Larc one-digit combinations for a non-numeric other than plus. The STM1 and STM2 signals are mutually exclusive; their function in the LSD and MSD translation matrixes is to distinguish between the two sets of combinations that generate them.

3-25. MSD TRANSLATION

The MSD of a Larc two-digit combination is translated from the zone-bit signals (STU5 and STU6), the fourth bit signal (STU4) of the XS-3 code, and the STM signals. These signals are converted into the MSD of the two-digit code by the gates which form the MSD translation matrix. These gates detect, for each bit position of the MSD, any combination of the signals (STU4, STU5, STU6, STM1, and STM2) that would result in binary 1. For example, a binary 1 is generated for the first bit position of the MSD (STB6) if any of the following conditions are present:

(1) The fifth and sixth bits (zone bits) of the Univac code are both 0 ($\overline{STU5}$ and $\overline{STU6}$) indicating that the translation will result in one of the two-digit combinations 15, 16, 17; 20 through 29; or 32, 33, 34.

(2) The fourth bit of the Univac code is 0 ($\overline{STU4}$), the fifth bit is a 1 (STU5) and the STM2 signal is generated indicating that the translation will result in one of the two-digit combinations 35, 36, 37 or 75, 76, 77.

(3) The sixth bit of the Univac code is a 1 (STU6) and an STM1 signal is generated indicating that the translation will result in one of the two-digit combinations 60 through 69 or 80 through 89.

(4) The fourth bit of the Univac code is a 1 (STU4), the fifth bit is 0 ($\overline{STU5}$), and STM2 is generated indicating the translation will result in one of the two-digit combinations 32, 33, 34 or 72, 73, 74.

Each of the conditions listed above result in a Larc two-digit combination having an MSD of 1, 2, 3, 6, 7, or 8, all of which have a 1 in the first bit position. Univac combinations that result in a binary 1 are detected in a similar manner for each of the other four bit positions. At T3 or T7, the MSD is translated and gated into the MSD flip-flops where it is stored until the translated LSD has been written into the input buffer register. The MSD is gated into the buffer register input pulseformers at T5 or T1 after which the MSD flip-flops are reset at T6 or T2. Although the MSD translator operates during a one-digit translation and produces

an erroneous MSD, the MSD that is translated is not written into an input buffer register.

3-26. ONE-DIGIT AND LSD TRANSLATION

A one-digit combination or the LSD of a two-digit combination is translated from the Univac code bit signals STU1 through STU7 and the STM signals by a number of gates in the LSD translation matrix. In addition to these gates the matrix contains a set of five gates that gate the outputs of the MSD flip-flops (STB6 through STB10) into the buffer register input pulseformers at T1 or T5. The translation gates in the matrix that are operative only during a one-digit translation are alerted by the STNUM signal from the one-digit-translate pulseformer. Gates operative only during a two-digit translation are alerted by the STALPH signal from the two-digit-translate pulseformer. Gates operative during either a one- or two-digit translation, have neither the STNUM nor STALPH signals as inputs.

If, during a one-digit translation an untranslatable error is detected by the checking circuits, an STUPE signal is generated. The STUPE signal jams binary 1's into the first three bit positions (STB1, STB2, STB3) of the buffer register input pulseformers and inhibits each of the gates in the matrix that could produce a binary 1 in bit positions 4 and 5. In this way, the combination for a plus (00111) is entered into the input buffer register in place of the possible non-legitimate combination that would have resulted from the untranslatable Univac digit.

The translation gates detect, for each bit position, the combination of input signals that would result in a binary 1. For example, a binary 1 is detected for the fourth bit position (STB4) if any of the following conditions are present:

(1) The fourth bit of the Univac code is a 1 (STU4), the STM2 signal is not generated ($\overline{\text{STM2}}$)* and an untranslatable one-digit combination is not detected ($\overline{\text{STUPE}}$) indicating that the translation will result in either one of the two-digit combinations 25 through 29, 45 through 49, 65 through 69, 85 through 89, or one of the one-digit combinations 5 through 9.

(2) The fourth bit of the Univac code is a zero ($\overline{\text{STU4}}$), the STM2 signal is generated, and a two-digit translation is taking place (STALPH) indicating that the translation will result in one of the two-digit combinations 15, 16, 17; 35, 36, 37; 55, 56, 57; or 75, 76, 77.

(3) The sixth bit of the Univac code is a 0 ($\overline{\text{STU6}}$), the seventh bit is a 1 (STU7), the STM2 signal is generated, a one-digit translation is taking place (STNUM), and an untranslatable one-digit combination is not detected ($\overline{\text{STUPE}}$) indicating that the translation will result in a period or ignore one-digit combination.

* Since STM1 and STM2 are mutually exclusive, $\overline{\text{STM2}}$ is logically the same as STM1.

Table 3-1. Univac ⟷ Larc Code Comparison

Row No.	Univac XS-3 Code	Univac Zones								Decimal Digit	Larc Standard Code	Larc Memory Code
		00		01		10		11			Bit Positions	Bit Positions
		Larc 2-Digit Code	Larc 1-Digit Code	Larc 2-Digit Code	Larc 1-Digit Code	Larc 2-Digit Code		Larc 2-Digit Code	Larc 1-Digit Code		54321	54321
1	0000	15	ignore	35		55		75		minus	00010	10000
2	0001	16	space	36		56		76		space	00100	10110
3	0010	17	minus	37	period	57		77		plus	10101	00111
4	0011	20	0	40		60		80	plus	0	10000	00010
5	0100	21	1	41		61		81		1	00001	10011
6	0101	22	2	42		62		82		2	10011	00001
7	0110	23	3	43		63		83		3	00111	10101
8	0111	24	4	44		64		84		4	10110	00100
9	1000	25	5	45		65		85		5	01000	11010
10	1001	26	6	46		66		86		6	11001	01011
11	1010	27	7	47		67		87		7	01011	11001
12	1011	28	8	48		68		88		8	11111	01101
13	1100	29	9	49		69		89		9	01110	11100
14	1101	32		52		72		92		period	11010	01000
15	1110	33		53		73		93		ignore	11100	01110
16	1111	34		54		74		94				

Univac Code Bit Positions = Check Bit Zone Bits XS-3 Bits
7 65 4321

Each of the listed conditions result in either a Larc two-digit combination with an LSD of 5, 6, 7, 8, or 9, or a one-digit combination of 5, 6, 7, 8, 9, period, or ignore, all of which have a 1 in the fourth bit position. Univac combinations that result in a binary 1 are detected in a similar manner for each of the other four bit positions. A one-digit combination is translated and gated into the buffer register input pulseformers at T3 or T7. After a two-digit translation the LSD is followed by the MSD which is gated into the pulseformers at T5 or T1.

3-27. ERROR CHECKING

Inputs to the Univac-to-Larc translator are checked by the input odd-even checker during any read or check-read, numeric or alphanumeric tape read cycle. Each Univac seven-bit code combination should contain an odd number of 1 bits. The checker examines all Univac combinations and produces error signals whenever a combination with an even number of 1 bits is detected. The same error signals are also produced if the STM1 and STM2 signals are in the same state, indicating an error in the auxiliary decoder. During a tape read cycle for a numeric (one-digit) read operation, the translator inputs are also checked by the untranslatable-digit checker to ensure that they constitute a combination that can be translated into Larc one-digit code. If such a combination is not detected, error signals are generated. The input odd-even and untranslatable-digit checkers are described below followed by an explanation of how the error signals produced by the checkers are distributed.

3-28. INPUT ODD-EVEN CHECKER. Univac code bits 1, 2, 3 (STU1, STU2, STU3) are decoded in the checker to produce a SNUF signal if they contain an even number of 1 bits or a SNUG signal if they contain an odd number of 1 bits. Similarly, bits 4, 5, 6 (STU4, STU5, STU6) are decoded to produce a SNUK signal if they contain an even number of 1 bits or a SNUP signal if they contain an odd number of 1 bits. The SNU signals thus produced are gated with the Univac check bit (STU7) to detect all combinations with an odd number of 1 bits. If a combination with an odd number of 1 bits is detected, then the odd-even error signal (STOE) is inhibited; otherwise the signal is generated. A legitimate combination is detected by the conditions indicated in the following table:

BIT POSITIONS		
7	6 5 4	3 2 1
1 (STU7)	Even number of 1 bits (SNUK, $\overline{\text{SNUP}}$)	Even number of 1 bits (SNUF, $\overline{\text{SNUG}}$)
1 (STU7)	Odd number of 1 bits ($\overline{\text{SNUK}}$, SNUP)	Odd number of 1 bits ($\overline{\text{SNUF}}$, SNUG)
0 ($\overline{\text{STU7}}$)	Even number of 1 bits ($\overline{\text{SNUK}}$, SNUP)	Odd number of 1 bits (SNUF, $\overline{\text{SNUG}}$)
0 ($\overline{\text{STU7}}$)	Odd number of 1 bits (SNUK, $\overline{\text{SNUP}}$)	Even number of 1 bits ($\overline{\text{SNUF}}$, SNUG)

The auxiliary decoder is checked by gating together the STM1 and STM2 signals. If these signals are both low, an $\overline{\text{STEM1}}$ signal is generated. If the inverse of these signals are both low, an $\overline{\text{STEM2}}$ signal is generated. Either condition represents an error because the state of signal STM1 should always be the opposite of STM2. An $\overline{\text{STEM1}}$ or $\overline{\text{STEM2}}$ signal forces an error signal to be generated by the odd-even checker by jamming to the same state a pair of SNU signals that should normally be in opposite states.

3-29. UNTRANSLATABLE-DIGIT CHECKER. The untranslatable-digit checker consists of a number of gates that detect combinations of the Univac code (STU1 through STU7) that are capable of being translated into the Larc one-digit code. If a Univac code combination is detected which is the equivalent of a 0 through 9, minus, space, plus, period, or ignore in Larc one-digit code, then a gate that produces the STUNT error signal is inhibited. Otherwise, the STUNT error signal is generated. The gate that produces the error signal is alerted by the one-digit-translate pulseformer and is therefore active only during a numeric (one-digit) read-to-memory operation.

3-30. DISTRIBUTION OF ERROR SIGNALS. To properly understand the distribution of the input odd-even and untranslatable-error signals, it is first necessary to understand something about the reading of pulses from tape during a hash-pulse period (HPP). The HPP is the name given to a period that occurs while the tape leader or a space between blocks of data on the tape is passing the read-write head. During this period any pulses on tape that are sensed by the read circuits of a synchronizer and gated into the translator may be either legitimate information pulses or extraneous hash pulses (usually erroneous pulses written on tape when the read-write head is disconnected). Input odd-even or untranslatable-error signals generated by pulses read from tape during the HPP are temporarily stored in an HPP odd-even error flip-flop or an HPP untranslatable-error flip-flop in the read circuits of the synchronizer. They are stored there until the pulses are classified by the synchronizer as belonging in either the information or hash-pulse category. If the pulses later prove to fall within the information category, then any error signal stored in an HPP error flip-flop is used to set the tape synchronizer or tape positioning checker error flip-flop and the proper error-diagnostic flip-flop. If the pulses fall within the hash-pulse category, then the HPP error flip-flops are cleared and the hash pulses are cleared out of the input buffer register. A more complete explanation of hash-pulse detection and control is given under heading 6-10.

The distribution of the input odd-even and untranslatable-error signals is as follows:

(1) STOEB sets the positioning-checker error flip-flop if the positioning checker is connected to the synchronizer performing the tape read cycle, provided the cycle does not occur during an HPP.

(2) STOE sets the HPP odd-even error flip-flop in the synchronizer performing the tape read cycle provided the cycle occurs during an HPP.

(3) STUNT sets the HPP untranslatable-error flip-flop in the synchronizer performing the tape read cycle provided the cycle occurs during an HPP.

(4) STROE sets the read-write error flip-flop in the tape synchronizer performing the tape read cycle provided the cycle does not occur during an HPP and the positioning checker is not connected to the synchronizer.

(5) STUOE sets the input odd-even error-diagnostic flip-flop in the central processor. The STUOE signal and the STUPE signal (item 6) are not produced during a tape read cycle occurring during an HPP. These signals are inhibited by an SnHPG* signal (figure 3-6) generated during an HPP by the read circuits of a synchronizer.

(6) STUPE sets the untranslatable-error diagnostic flip-flop in the central processor. The STUPE signal also jams the Larc one-digit code combination for a plus (00111) into the translator in place of the translated combination. An untranslatable check is not performed during a check-read operation.

* n = synchronizer number 7, 8, 9, or 10.

SECTION 4
READ-WRITE CONTROL CIRCUITS

4-1. GENERAL

The tape synchronizer read-write control circuits operate in conjunction with either the write circuits (section 5) in controlling a write operation, or the read circuits (section 6) in controlling a read or check-read operation. The read-write control circuits divide functionally into five subdivisions (figure 4-4); these subdivisions and their major functions are as follows:

(1) Read-Write Mode Controls. The read-write mode controls control the translation mode of the read or write operation as specified by the processor program.

(2) Digit-Count Controls. The digit-count controls count the digits of each Larc word as they are transferred to or from a buffer register during a read or write operation and count the Univac characters as they are read during a check-read operation. The controls supply digit-count and word-end control signals to the read and write circuits.

(3) Buffer Register Controls. The buffer register controls alternate the roles of the odd and even buffer registers and alert the dispatcher to transfer data words to or from the memory during read or write operations.

(4) Word-Count Controls. The word-count controls count the Larc data words transferred to or from the memory during a read or write operation and the Univac words read from tape during a check-read operation. During an alphanumeric operation, the word-count control circuits generate a signal which is used to compensate for the fact that the count is in terms of Larc words, whereas control is usually exercised in terms of the Univac words read from, or written on, tape.

(5) Read-Write Status Controls. The read-write status controls communicate to the program the status of an operation being carried out by the read or write circuits and communicate the requirements of the program to the read or write circuits.

The subdivisions are described individually in the following paragraphs; the circuits are illustrated by the simplified logic diagram, figure 4-4.

4-2. READ-WRITE MODE CONTROLS

There are two flip-flops in the read-write mode control circuits (figure 4-4), the numeric flip-flop and the alphanumeric flip-flop. At the beginning of a read or write operation (I = 3, 4, 5, or 7), a 66 instruction sets one flip-flop or the other depending upon the K digit specified in rP1. If K = 1, the numeric flip-flop is set; if K = 2, the alphanumeric flip-flop is set.

The output (S7NUM) of the numeric flip-flop modifies the operation of the translators and the synchronizer proper by alerting gates that function only during one-digit (numeric) translate operations. Conversely, the output (S7ALP) of the alphanumeric flip-flop alerts gates that function only during two-digit (alphanumeric) translate operations.

At the beginning of a check-read operation on the synchronizer, the numeric flip-flop is set by a 68 instruction provided the write circuits are available. Although the information read during a check-read operation may be either numeric or alphanumeric, the numeric flip-flop must be set to provide proper control for stepping and clearing the digit counter. The digit counter is cleared and stepped identically for a check-read operation and a numeric read or write operation. The signal (S7L1Z) that sets the numeric flip-flop for a check-read operation generates an S7RS signal which clears the digit counter and other control circuits in preparation for beginning the operation.

The numeric or alphanumeric flip-flop is reset at the end of an operation by a read-ending (S7RE1) or write-ending (S7WE1) signal, respectively.

4-3. DIGIT-COUNT CONTROLS

The digit-count control circuits (figure 4-4) consist of a 12-count closed counter which counts the digits of a word as they are written into or read out of a buffer register, clearing and stepping controls which clear and step the counter during each read or write cycle in accordance with the current operating mode, and word-end detection gates which generate a word-end signal every 12th step of the counter.

Because the internal operation of the digit counter is not pertinent to an understanding of the operation of the synchronizer as a whole, the counter is represented as a block in figure 4-4; however, the contents of this block are illustrated in figure 4-1.

The main output of the digit-count control circuits are 12 digit-count signals (S7DC1 through S7DC12), a word-end signal (S7WEND), and a count-digit signal (S7CD) that is generated each time the counter is stepped. The digit-count outputs control the digit-by-digit stepping of the input buffer register write drivers during tape-read operations or the output buffer register read drivers during tape-write operations. The word-end and count-digit signals perform control functions throughout the tape

synchronizer. The main functions of the word-end signal are (1) to initiate word transfer requests to the dispatcher during read or write operations, and (2) to step the word counter during check-read operations.

The digit counter is stepped once each tape-read or tape-write cycle when the synchronizer is operating in the one-digit (numeric) translate mode and twice each cycle when the synchronizer is operating in the two-digit (alphanumeric) translate mode. The count therefore reflects the number of Larc digits transferred to or from a buffer register, rather than the number of Univac digits read from or written on tape. During a check-read operation the counter is stepped as it is during a numeric read or write operation. Since information read from tape during a check-read operation is not translated or written into an input buffer register, it is necessary to step the counter only once each tape-read cycle regardless of whether the information read is numeric or alphanumeric.

The counter may be stepped in either an ascending or descending order. If the synchronizer is performing a forward-read operation, the over-all digit count is in descending order; if it is performing a backward read operation, the over-all count is in ascending order. As a consequence, the digits of a word are arranged in an input buffer register in the same order whether they are read from tape in a forward or a backward direction.

4-4. OPERATING SEQUENCES

At the beginning of an operation the digit counter is cleared to a particular count depending on the mode of operation. (See table 4-1.) Stepping of the counter always coincides with the writing of a digit into an input buffer register (figure 6-2) or the reading of a digit out of an output buffer register (figure 5-1). While one digit is written in or read out, the counter is stepped to alert the buffer register driver controls for writing or reading the next digit. On the 12th step a word-end signal is generated and the same stepping sequence is repeated for the next word. The counting sequence is repeated when the counter is stepped beyond its capacity.

4-5. FORWARD NUMERIC. In performing a forward numeric or forward check-read operation the counter is first cleared to 12 and a -1 step is performed during each tape read or write cycle. The 12th -1 step steps the counter from 1 to 12 and generates a word-end signal. The digits of a word are, therefore, transferred to or from a buffer register during a forward numeric write or read operation beginning with the MSD.

4-6. BACKWARD NUMERIC. In performing a backward numeric-read or check-read operation, the sequence is reversed by initially clearing the counter to 1 and performing a +1 step during each tape-read cycle. The 12th +1 step steps the counter from 12 to 1 and generates a word-end signal.

4-7. FORWARD ALPHANUMERIC. For a forward alphanumeric write or read operation one would expect the counter to be initially cleared to 12 and a -1 step to be performed for each Larc digit transferred to or from a buffer register; however, a different pattern of clearing and stepping is required to accommodate the design of the translators. The Larc-to-Univac translator is designed to receive, from a buffer register, the LSD of an alphanumeric digit pair first; the Univac-to-Larc translator is designed to transfer to

a buffer register the LSD of an alphanumeric digit pair first. Each digit pair, however, is arranged in the buffer register MSD first. Consequently, the counter is initially cleared to 11 and a +1 step is performed as each LSD of a digit pair is read out or written into a buffer register. Each of these steps is followed by a -3 step as the MSD is read out or written in. The count, therefore, proceeds in the following sequence:

11,12 9,10 7,8 5,6 3,4 1,2

The sixth -3 step steps the counter from 2 to 11 and generates a word-end signal.

Table 4-1. Digit Counter Operation

Operation	Counter Initially Cleared To	Any TWC or Sync 7 or 9 TRC Produces	Sync 8 or 10 TRC Produces	Word-End (WEND) Detected When Stepping From
Forward Operation				
Numeric-Read Numeric-Write Check-Read	12	-1 step at T3	-1 step at T7	1 to 12
Alphanumeric Write or Read	11	+1 step at T3 -3 step at T5	+1 step at T7 -3 step at T1	2 to 11*
Backward Operation				
Numeric-Read Check-Read	1	+1 step at T3	+1 step at T7	12 to 1
Alphanumeric	1	+1 step at T3 +1 step at T5	+1 step at T7 +1 step at T1	12 to 1*

* Occurs on every 6th tape read or write cycle.

4-8. BACKWARD ALPHANUMERIC. In performing a backward alphanumeric-read operation, the counter is initially cleared to 1 and a +1 step is performed as each digit is written into a buffer register. Since the LSD of an alphanumeric digit pair is received first from the translator, the digits of a word enter the buffer register in sequence beginning with the LSD of the least-significant digit-pair. The 12th +1 step steps the counter from 12 to 1 and generates a word-end signal.

4-9. DIGIT COUNTER CODE

A seven-bit, tri-quaternary code is used in the digit counter. There are 12 possible combinations of the code corresponding to the 12 digit counts of a word. The combinations and the digit counts they represent are shown in table 4-2. Bits B1, B2, B3, and B4, referred to as the quaternary part of the code, have numerical weights of 1, 2, 3, and 4, respectively. Bits Q1, Q2, and Q3, referred to as the trinary part of the code, have weights of 0, 4, and 8, respectively. An important characteristic of the code is the fact that it has a single 1 bit in both the quaternary part and the trinary part.

Table 4-2. Digit Counter Tri-Quaternary Code

Digit Count	Trinary Bits Q3	Q2	Q1	Quaternary Bits B4	B3	B2	B1
	Bit Weights 8	4	0	4	3	2	1
1	0	0	1	0	0	0	1
2	0	0	1	0	0	1	0
3	0	0	1	0	1	0	0
4	0	0	1	1	0	0	0
5	0	1	0	0	0	0	1
6	0	1	0	0	0	1	0
7	0	1	0	0	1	0	0
8	0	1	0	1	0	0	0
9	1	0	0	0	0	0	1
10	1	0	0	0	0	1	0
11	1	0	0	0	1	0	0
12	1	0	0	1	0	0	0

The seven bits of the code are stored in seven flip-flops (figure 4-1). The outputs of the flip-flops are decoded to generate one of the signals S7DC1 through S7DC12 which, for a read or write operation, represent the count of the next Larc digit to be transferred to or from a buffer register. Every time the counter is stepped or cleared to a particular count, the seven flip-flops are reset and a new combination is simultaneously gated in, thereby changing the digit-count output.

4-10. MODE CONTROL

The clearing, stepping, and word-end detection of the digit counter differ depending upon the direction of tape operation (forward or backward), the translation mode (numeric or alphanumeric), and the type of operation (read or write). A tape-direction indication is supplied by the tape-forward signal (S7XTF). This signal is derived from the buffed outputs of the high-density, low-density, and read-forward mode flip-flops, one of which is set during a forward operation. The translation mode is indicated by the numeric (S7NUM) and alphanumeric (S7ALP) signals from the read-write mode flip-flops. The type of operation is indicated by the tape-read cycle and tape-write cycle signals (S7TRC and S7TWC, respectively) which, along with the timing signals, actually trigger the stepping of the counter. (The derivation of S7TRC and S7TWC is described under headings 3-13 and 3-14, respectively.)

4-11. CLEARING

Before a write, read, or check-read operation is begun on the tape synchronizer, or after extraneous (hash) pulses are detected during a read or check-read operation, the digit counter must be cleared to a particular count depending on the mode of operation. (See table 4-1.) The counter is cleared by an S7RS signal (figure 4-1 and 4-4). This signal resets the seven digit-counter flip-flops and tests the numeric (S7NUM), alphanumeric (S7ALP), and tape-forward (S7XTF) mode signals to generate one of the clear signals, S7CL12, S7CL11, or S7CL1. The clear signal then jams the proper digit-code combination into the counter flip-flops. For example, a clear-to-12 signal (S7CL12) sets flip-flops B4 and Q3, thereby entering the code combination for a 12.

The S7RS signal is generated some 6 milliseconds after the proper combination of thyratrons in the Uniservo tape unit has been fired, but before tape motion has started. This signal is generated at the beginning of a write operation only if the Uniservo tape unit does not mount a master tape reel and a write operation is not already in progress. It is generated at the beginning of a read or check-read operation only if the read-write control circuits are not controlling another operation. When the S7RS signal is first generated at the beginning of a check-read operation on the tape synchronizer, the numeric mode flip-flop, which provides control for clearing the counter, will not be set, since it is not set until the check-read operation is started by a 68 instruction. The first clearing of the counter for a check-read operation is therefore erroneous. The S7RS signal is, however, generated again by the S7L1Z signal, the same signal that sets the numeric mode flip-flop for a check-read operation.

The S7RS signal may also be generated by the S7HP signal if a hash pulse is detected at the beginning of a read operation or during reading of an SBB. Since a hash pulse may trigger a tape-read cycle and thereby cause the digit counter to step, the counter must be cleared to prepare for processing legitimate data read from tape.

4-12. STEPPING

The digit counter is stepped once during each tape-read or tape-write cycle when the synchronizer is operating in the numeric mode, and twice during each cycle when operating in the alphanumeric mode. The tape read- and write-cycle signals (S7TRC and S7TWC) are gated with timing and mode signals to step the counter as indicated in table 4-1. Depending on the time and mode of operation, a -3 step, a +1 step, or a -1 step signal (S7CM3, S7CP1, and S7CM1, respectively) is generated along with an S7CD signal. The S7CD signal clears flip-flops B1, B2, B3, and B4 and tests gates which detect the end of a word during a backward or numeric forward operation. Since the digit-counter code (table 4-2) is such that the same combination of quaternary bits recurs every fourth count, adding 1 or subtracting 3 from the quaternary part produces the same result. Therefore, the S7CM3 and S7CP1 step signals are buffed together to generate a single signal (S7CMP31) which is gated with the outputs of the quaternary flip-flops to add 1 or subtract 3 from the quaternary part of the code. Similarly, the -1 step signal (S7CM1) is gated with the outputs of flip-flops B1 through B4 to subtract 1 from the quaternary part of the code.

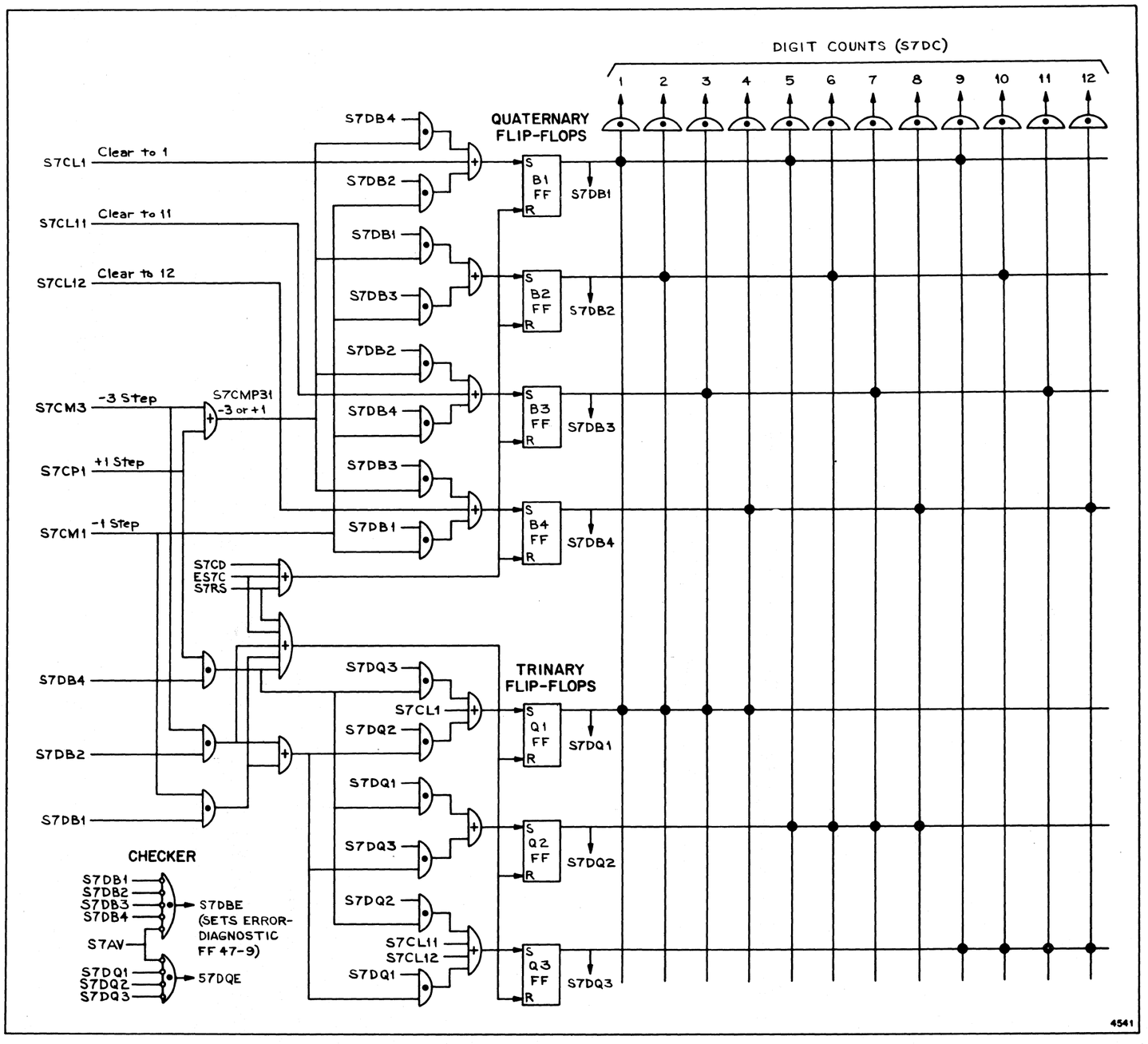


Figure 4-1. Digit Counter
(D 807 885)

The trinary part of the digit-counter code changes every fourth count. When the counter is stepped, any change in the trinary part of the code depends on the original state of the quaternary as well as the trinary part. If a +1 step is performed and FF B4 contains a 1 bit, an S7QD signal is generated which is gated with the output of trinary flip-flops to add 1 to the trinary part. If a -3 step is performed and FF B2 contains a 1 bit, or if a -1 step is performed and FF B1 contains a 1 bit, an S7QS signal is generated which subtracts 1 from the trinary part of the code. When either the S7QD or S7QS signal is generated, an S7QA signal is generated to clear the old combination from the trinary flip-flops.

4-13. WORD-END DETECTION

A word-end signal (S7WEND) is generated each 12th step of the digit counter. The end of a word for the numeric forward, backward, or alphanumeric forward operations is detected by three separate gates. The gate which detects the end of a word during a numeric-forward operation has as inputs the digit-count-1 signal (S7DC1) of the counter and the S7NUM and S7XTF mode signals. Every time the counter is stepped, the gate is tested by the S7CD signal. If the counter reads 1, indicating the current step is from 1 to 12, an S7WEND signal is generated.

The word-end detection gate for a backward operation has as inputs the inverse of the S7XTF signal and the digit-count-12 signal (S7DC12). The gate is tested by the S7CD signal every time the counter is stepped. If the counter reads 12 when stepped, an S7WEND signal is generated.

The detection gate for an alphanumeric forward operation has as inputs the S7XTF signal and the digit-count-2 signal (S7DC2). The gate is tested by the S7CM3 signal each time a -3 step is executed. If the counter reads 2 when a -3 step is executed, indicating that the step is from 2 to 11, the S7WEND signal is generated. Because the -3 step is executed only during an alphanumeric operation the gate is not tested during a numeric operation.

4-14. CHECKING

The digit-counter code should always contain a single 1 bit in the trinary part and a single 1 bit in the quaternary part. The counter (figure 4-1) is therefore checked to ensure that one and only one quaternary flip-flop is set and one and only one trinary flip-flop is set when the counter is operating. The absence of a 1 bit is detected by two gates, one of which gates together the reset (barred signal) outputs of the quaternary flip-flops, and the other the reset outputs of the trinary flip-flops. When a write, read, or check-read operation is not in progress both gates are inhibited by a signal from the read-write-circuits-available flip-flop. If none of the quaternary flip-flops are set, an S7DBE error signal is generated. If none of the trinary flip-flops are set, an S7DQE error signal is generated. Both error signals set the tape read-write error flip-flop and an error-diagnostic flip-flop.

Although not shown in figure 4-1, these same error signals are generated indirectly in the case where more than one quaternary flip-flop or more than one trinary flip-flop is set. For ease in understanding the normal operation of the counter, the gates that set the digit-counter flip-flops are represented in simplified form in figure 4-1. For example, one of the set gates of FF B4 is shown as being alerted by the set output of FF B3 (S7DB3), although in the actual circuit this gate is instead inhibited by the reset (barred signal) outputs of flip-flops B1, B2, and B4. Since, in normal operation, only one of the quaternary flip-flops is set at any one time, the general logical effect is the same in either case. However, in the event an error occurs that causes more than one quaternary flip-flop to be set, the method of setting the flip-flops actually used will cause the flip-flops to inhibit one another from being set on the next step of the counter. As a result, the four quaternary flip-flops will be reset on the next step by the S7CD clearing signal and an S7DBE error signal will be generated by the gate that detects the absence of a 1 bit in the quaternary part of the code. An S7DQE error signal is generated by a similar method in the event more than one of the trinary flip-flops are set simultaneously.

4-15. BUFFER REGISTER CONTROLS

There are two one-word input and two one-word output buffer registers for each tape synchronizer. While a word is being read from tape and entered into one input buffer register, a word in the other register is transferred to the memory. By the time the one register is full, the word in the other will have been sent to the memory. Then, the roles of the registers are reversed. Similarly, the two output buffer registers reverse roles after each word is recorded on tape. While one register is waiting to receive a word from memory, data in the other is being recorded on tape. One of the input and one of the output buffer registers are distinguished by the term "even", the other two by the term "odd". The buffer register controls consist of two flip-flops, a memory-request flip-flop which alerts the dispatcher to transfer a word between a buffer register and the memory, and a word-driver flip-flop which defines the current role of the even and odd registers. (See figure 4-4.)

4-16. MEMORY-REQUEST FLIP-FLOP

The memory-request flip-flop is set (normally by the word-end signal) whenever a data word is required from or ready to be sent to the memory. When it is set, the flip-flop alerts the priority circuits in the dispatcher to initiate the memory reference. When access to the memory is ensured, the dispatcher generates a signal (S7RFR) that resets the flip-flop.

The flip-flop has two set gates, one of which is alerted during a write operation by the write-circuits-in-use signal (S7WBG), and the other during a read operation by the read-circuits-in-use signal (S7RBG). Since data read during a check-read operation is not sent to the memory, the read gate is inhibited by S7RCH from the check-read mode flip-flop. Normally, the memory-request flip-flop is set by the word-end signal (S7WEND) when the last digit of an input word is written from tape into an input buffer register or when the last digit of an output word is read from an output buffer register. However, before the first S7WEND signal is generated during a tape-write operation, both output buffer registers must be loaded from

the memory. Therefore, the memory-request flip-flop is set twice at the beginning of a write operation by signals from the write-start controls; it is set first by S7WERD to load the first word, and then, after access to the memory has been obtained, by S7RSWD. At the end of the write operation the reverse situation exists. The last two word-end signals must be prevented from setting the flip-flop after the data for the tenth word of the last ten-word group has been transferred from the memory. This is accomplished by a gate which has as inputs $\overline{\text{SCT}}$ from the continue flip-flop (which, when it is low, indicates that writing is to end when the current ten-word group has been written) and S7CAL and S7WX10 from the word-count controls which indicate that the data for the tenth word of a ten-word group has been transferred from the memory. Whenever the memory-request flip-flop is set at the end of a word, the dispatcher should complete the requested transfer and reset the flip-flop before the end of the next word. To check this, each word-end signal tests the flip-flop, and if it is set, generates S7FLE which sets the synchronizer overflow error-diagnostic flip-flop. During a read operation this would indicate that the synchronizer failed to have the contents of an input buffer register transferred to the memory before it was ready to load the same register with another word from tape. During a write operation it would indicate that the synchronizer failed to have a buffer register loaded with a word obtained from the memory by the time the synchronizer was ready to write the word on tape.

4-17. WORD-DRIVER FLIP-FLOP

The word-driver flip-flop causes the odd and even buffer registers to switch roles at the end of each word. It is connected as a binary counter, and, except at the beginning of a write operation, it functions as such. Each time a word-end signal is generated, the flip-flop changes from one state to the other.

When it is set during a tape-write operation, the flip-flop alerts the controls (in the dispatcher) that energize the magnetic-amplifier write drivers of the odd output buffer, and the controls in the write circuits (in the synchronizer) that energize the read drivers of the even output buffer register. Thus, the word requested from the memory is loaded into the odd register by the dispatcher and the word in the even register is written on tape by the synchronizer. When the flip-flop is stepped to the opposite state by the next word-end signal, it alerts the write-driver controls of the even register and the read-driver controls of the odd register, thereby switching the roles of the odd and even registers.

When the first two words are loaded into the output buffer registers at the beginning of a write operation, the flip-flop is controlled by the write-start controls. It is first reset by S7WERD to direct the first word from memory into the even register and then it is set by S7RSWD to direct the second word from memory into the odd register.

When the word-driver flip-flop is set during a read operation, it alerts the controls in the dispatcher that energize the read drivers of the odd input buffer register, and the controls in the read circuits of the synchronizer that energize the write drivers of the even input bufffer register. Thus, the word in the odd register will be sent to the memory by the dispatcher and the word from tape will be loaded into the even register. When

the flip-flop is stepped to the opposite state by the next word-end signal, it alerts the read-driver controls of the even register and the write-driver controls of the odd register, thereby switching the roles of the registers.

Initially, the word-driver flip-flop is set by S7RS. Thus, the first word read from tape during a read operation is loaded into the even buffer register.

4-18. WORD-COUNT CONTROLS

The word-count controls (figure 4-4) consist of the following:

(1) A ten-count closed counter, which counts the Larc words transferred to or from the memory during a read or write operation, respectively, or counts the Univac words read from tape during a check-read operation.

(2) An alphanumeric-compensate flip-flop which modifies the operation of the synchronizer during an alphanumeric operation to compensate for the fact that the word count is in terms of Larc words, whereas the Univac words that are read from or written on tape are the equivalent of two Larc alphanumeric words.

Because the internal operation of the word counter is not essential to an understanding of the operation of the synchronizer as a whole, the counter is represented as a block in figure 4-4. The contents of this block are illustrated in figure 4-2.

4-19. WORD COUNTER

During a read or write operation the word counter (figure 4-2) is stepped by S7BA from the dispatcher. This signal is generated at the same time as a word from the memory is written into an output buffer register or at the time a word is read out of an input buffer register and sent to the memory.

During a write operation, the first two words to be written are transferred from the memory to an output buffer register before writing begins. Consequently, the word counter will be stepped twice (first from 10 to 1, then from 1 to 2) by S7BA before the first word is written. Subsequently, memory references are initiated by the word-end signal and the counter will normally be stepped by S7BA several milliseconds after the word-end signal occurs. The exact time S7BA is generated cannot be predicted since its generation depends on the dispatcher gaining access to the memory for the synchronizer which, in turn, depends on the outstanding memory requests of other synchronizers. However, it is normally generated long before the next word-end signal. Where word-count control is required in the synchronizer, a specific counter output is sampled by the word-end signal. The relationship of the word counts (at S7WEND) to the actual words being written (A, figure 4-3) differs depending upon whether a numeric or alphanumeric write operation is being performed. The last two word-end signals of a tape-write operation are inhibited from initiating a memory transfer. Consequently, the word count will stop at 10.

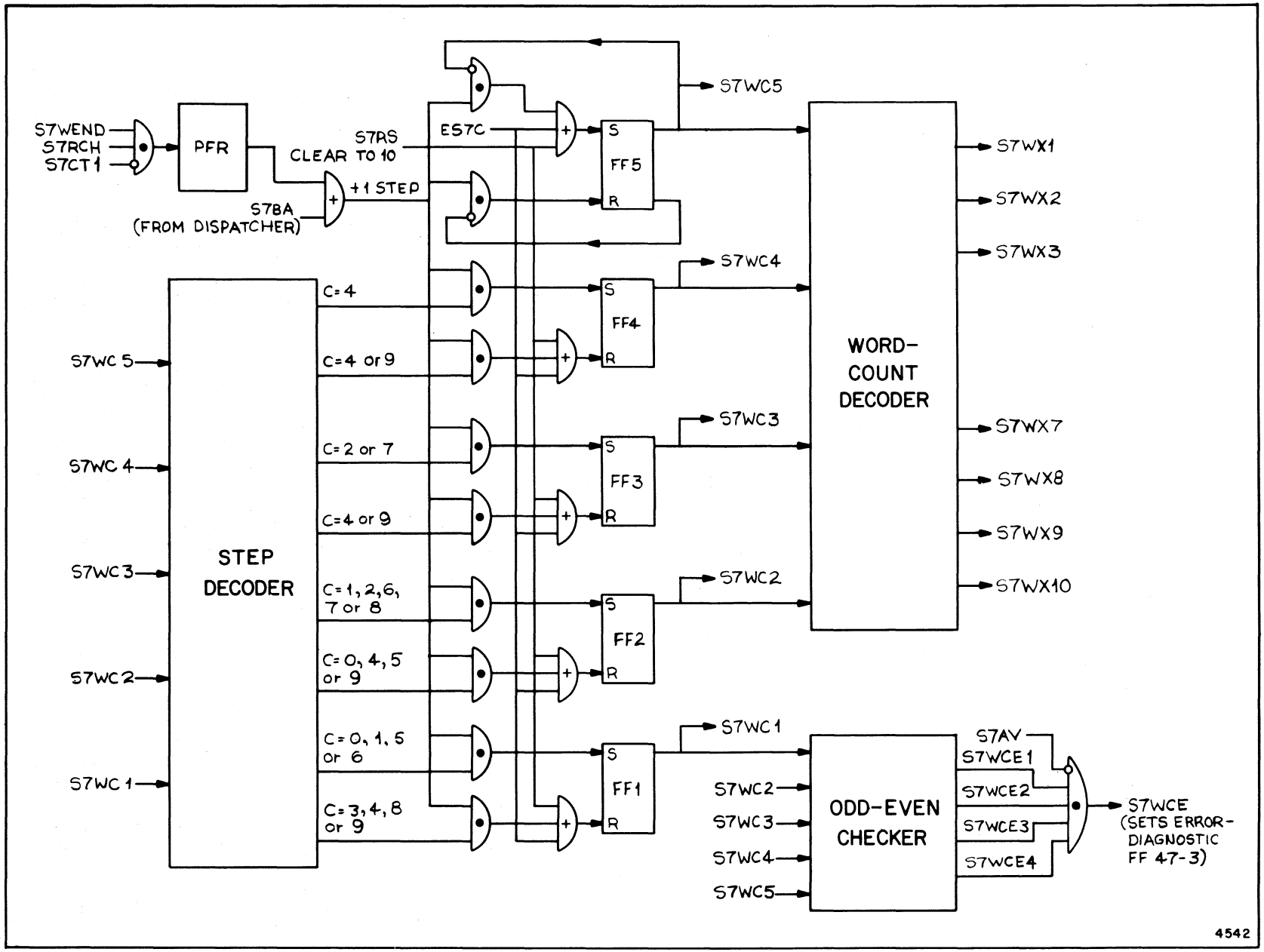


Figure 4-2. Word Counter (D 807 886)

During a tape-read operation, a memory reference is always initiated by the word-end signal. As with the write operation, the relationship of the word counts at S7WEND to the words being read (B, figure 4-3) differs for numeric and alphanumeric operations. At the end of a read operation the word counter is stepped to 10 as the tenth word of the last ten-word group is transferred to the memory.

During a check-read operation, the data read from tape is not sent to the memory; therefore, the counter is stepped by the word-end signal which causes the count to change, 1 μsec after the word-end signal occurs.

The word counter uses standard Larc five-bit code combinations which are stored in five flip-flops and decoded by a word-count decoder to produce the word-count signals S7WX1, S7WX2, S7WX3, and S7WX7 through S7WX10. Word-count signals for counts 4, 5, and 6 are not generated because they are not required for control purposes, although the counter is stepped through these counts. The code combination for zero is decoded to produce the word-count-10 signal, S7WX10. At the beginning of a read or write operation, the flip-flops are cleared to zero, which is equal to a count of ten. The count then proceeds from 10 to 1 and thereafter in ascending order. After the tenth step the sequence repeats unless the operation ends.

The outputs of the five flip-flops are also decoded by a step decoder. Each time a step signal is generated the step decoder sets or resets the proper combination of flip-flops (FF1 through FF4) to advance the count by 1. The check-bit flip-flop (FF5) is connected as a binary counter and changes state whenever the step signal is generated. A decoded code combination that changes the state of a flip-flop is indicated in figure 4-2 by the letter C followed by the decimal equivalent of the combination.

The outputs of flip-flops FF1 through FF4 are compared, in the odd-even (parity) checker, with the output of the check-bit flip-flop. If an even combination of 1 bits is detected, S7WCE is generated which sets the word counter error-diagnostic flip-flop. The odd-even checker is turned off by S7AV from the read-write-circuits-available flip-flop when the word counter is not operating.

4-20. ALPHANUMERIC-COMPENSATE FLIP-FLOP

During a read or write operation, the word counter counts the Larc words transferred to or from the memory. When the synchronizer is operating in the numeric mode, this is equivalent to counting the Univac words that are read from or written on tape because of the one-to-one relationship between Larc and Univac numeric words. During a check-read operation, the digit counter operates in the numeric mode and the word-end signal steps the word counter; therefore, the word count during a check-read operation is also in terms of the Univac words read from tape. During an alphanumeric read or write operation, however, the count is not in terms of Univac words since each 12-digit Univac alphanumeric word is equal to two Larc 12-digit words. To compensate for this, the alphanumeric-compensate flip-flop is alternately set and reset at intervals of ten word counts during an alphanumeric operation and is set throughout a numeric or check-read operation. (See figure 4-3.)

When the alphanumeric-compensate flip-flop is set it alerts gates (in the synchronizer) that sample the word-counter outputs and inhibits the same gates when it is reset. Thus, a gate that samples a particular word-count signal will be permissive at intervals of 20 word counts during an alphanumeric operation and at intervals of ten word counts during a numeric or check-read operation. In this way the SBB, bad-spot, and ending controls in the read and write circuits and the read-write status controls are made to operate identically for an alphanumeric, a numeric, and a check-read operation.

During an alphanumeric operation, the alphanumeric-compensate flip-flop operates as a binary counter. It changes state at the end of every second word, the equivalent of a word count of three for a write operation or a word count of one for a read operation. The flip-flop changes state at the end of the second, rather than the tenth, word in order to provide proper control for the bad-spot controls. S7BSG1 and S7BSG2, which reset the flip-flop during an alphanumeric operation, each sets a bad-spot-gating flip-flop in the write and read circuits, respectively.

4-21. READ-WRITE STATUS CONTROLS

The read-write status controls (figure 4-4) provide the means by which the processor program exercises over-all control of a read, check-read, or write operation performed on the tape synchronizer. The program exercises control in the following ways:

(1) By testing to determine if the read-write circuits are available (instruction 61).

(2) By alerting the synchronizer to start the operation (instruction 68).

(3) By monitoring the progress of an operation by way of the master input-output priority, ten-word, and SBB tests (instructions 99, 69, and 73, respectively).

(4) By issuing continue or continue-beyond-SBB instructions, as required, to complete the operation (instructions 70 and 71).

(5) By testing to determine if an error has been detected during the operation (instruction 48).

Each of these functions and the circuits in the read-write status controls that enable the program to carry them out are described under headings 4-22 through 4-29, following.

4-22. AVAILABILITY CONTROL

The program determines the availability of the read-write control circuits by testing the read-write-circuits-available flip-flop which is reset at the beginning of an operation and set at the end. When a 68 instruction is executed, to begin a read, check-read, or write operation, the flip-flop is reset to the unavailable state by S7RST. For a write operation it is

also reset, prior to clearing the output buffer registers, by S7WDR from the start controls of the write circuits. During an initial-read operation (covered in the appendix) it is reset by S7WFS from the start controls of the read circuits. At the end of an operation, the flip-flop is reset by a signal from the read- or write-ending controls.

4-23. READ-WRITE START CONTROL

The program orders the synchronizer to begin a read, check-read, or write operation by setting the read-write start flip-flop with a 68 instruction. The flip-flop then alerts the start controls in the read or write circuits to begin the operation. If a check-read operation is to be controlled by the tape positioning checker, the read-write start flip-flop is set by a 65 instruction. This flip-flop is the only part of the read-write control circuits which is employed for a check-read operation controlled by the positioning checker. However, the flip-flop merely triggers a check-read operation and is immediately reset by S7RRS from the start controls in the read circuits. Consequently, the read-write controls are not tied up by a positioning checker check-read operation.

When a read-to-memory operation is started by the read circuits, the read-write start flip-flop is reset (by S7RRS) only after the even input buffer register has been cleared. When a write operation is started in the write circuits, the flip-flop is reset by S7SUCR from the write-start controls after the output buffer registers have been cleared and the tape has accelerated and travelled the proper distance for beginning the operation.

4-24. TEN-WORD AND SBB CONTROL

The processor program monitors an operation by testing the ten-word flip-flop. When it is set, this flip-flop causes the master input-output priority test (99 xx0xx MMMMM), master ten-word test (99 xx2xx MMMMM), and ten-word test (instruction 69) instructions to transfer control. The flip-flop is set at the following times:

(1) As the first digit of each ten-word group is read from or written on tape.

(2) At the beginning of an SBB.

(3) When reading or writing has ended.

The set gate of the ten-word flip-flop is alerted by the ten-word-alert flip-flop. This flip-flop is set by S7RST at the start of a read, check-read, or write operation and at the end of each ten-word group by one or the other of two gates. One gate is alerted during a write operation by the write-operation signal (S7WOP) and the other during a read or check-read operation by the read-operation signal (S7ROP). The flip-flop is simultaneously reset and tested by the count-digit signal (S7CD) which occurs on every digit count. If the flip-flop is set when tested, indicating that the first word of a ten-word group is being counted, the ten-word flip-flop is set.

The ten-word flip-flop is also set by the following signals:

(1) S7RE at the end of a read or check-read operation.

(2) S7C10B when an SBB is encountered during a read or check-read operation.

(3) S7VWF at the end of a write operation or when the write circuits begin to insert an SBB.

In the event one of the setting signals (S7RE, S7C10B, or S7VWF) is generated at T4, it is inhibited from setting the ten-word flip-flop immediately. Instead, it is delayed by a pulseformer and sets the flip-flop at T5. The reason for this follows. When the flip-flop is tested by a 69 instruction and is found to be reset, the test gate generates a conditional-transfer signal and resets the flip-flop at T4. However, to check the resetting, the gate is tested for two pulse times (T4,5) and the conditional-transfer signal is, in effect, sampled during the last pulse time to ensure that the flip-flop was actually reset at T4. If the flip-flop was not reset, a conditional-transfer error is generated. Therefore, a set pulse arriving at T4 while a 69 instruction is being executed will override the reset pulse at T4 and cause an erroneous conditional-transfer error to be generated. To avoid this, a set pulse arriving at T4 is prevented from setting the flip-flop until T5.

Although not actually part of the read-write controls there are two additional flip-flops which the program tests to monitor and control reading or writing; these flip-flops are the read-SBB and write-SBB flip-flops in the read and write circuits, respectively. The read-SBB flip-flop is set for 5 milliseconds whenever an SBB passes the read-write head during a read or check-read operation, and at the end of the operation. The write-SBB flip-flop is set for 10 milliseconds when a 1.0-inch SBB is being inserted during a write operation and for 24 milliseconds when a 2.4-inch SBB is being inserted. The write SBB flip-flop is also set for 10 milliseconds when the write operation has ended. By testing these flip-flops with a 73 instruction, the program can determine whether the ten-word flip-flop was set as a result of an SBB or as a result of a new ten-word group being started. The test also provides a convenient means for the program to keep track of the number of blocks that are read or written.

4-25. CONTINUE CONTROL

Whether or not an operation is to continue is controlled by the state of the continue, continue-beyond-SBB, continue-check (figure 6-5), and read-write-error flip-flops.

The continue flip-flop is set by either a 70 or 71 instruction and is reset at the same time the ten-word flip-flop is set; that is, as the first digit of each ten-word group is read or written. (See timing diagram, figure 4-3.)

The continue-beyond-SBB flip-flop is set by the 71 instruction only. During a Univac read or check-read operation, the continue-beyond-SBB flip-flop can only be set when an S7BL6 signal from a "blockette" counter in the read circuits indicates that the last ten words of a 720-character Univac block are being read. The flip-flop is reset, during a write operation, by S7VWF whenever the write circuits begin inserting an SBB, and, during a read or check-read operation, by S7C10D whenever the read circuits detect the beginning of an SBB other than the terminal SBB.

The effect of the continue and continue-beyond-SBB flip-flops, as well as the continue-check and read-write-error flip-flops, on the read, check-read, and write operations is covered in the following paragraphs.

4-26. READ OPERATION. When the program is alerted by the ten-word and SBB tests to the fact that reading of a new ten-word group has begun, it determines whether or not the operation is to continue.

If the read operation is to terminate after the current ten-word group is read, the program witholds execution of both the 70 and 71 instructions, thereby leaving the continue flip-flop reset. When the continue flip-flop is reset, it alerts a gate in the read circuits (which detect the end of the ten-word group) and sets the check-read flip-flop. With the check-read flip-flop set, the remaining data in the block, if any, is check read only; that is, it is not transferred to the memory. The same signal (S7ZEN) that sets the check-read flip-flop also sets the continue-check flip-flop which, in turn, resets the continue-beyond-SBB flip-flop in the event it had been set previously by a 71 instruction. When the continue-beyond-SBB flip-flop is reset, it alerts the ending controls in the read circuits and all reading ends at the end of the current block. Both the 70 and 71 instructions test the continue-check flip-flop. If it is set, indicating that the read operation cannot continue because it has already terminated, a read-check error signal is generated.

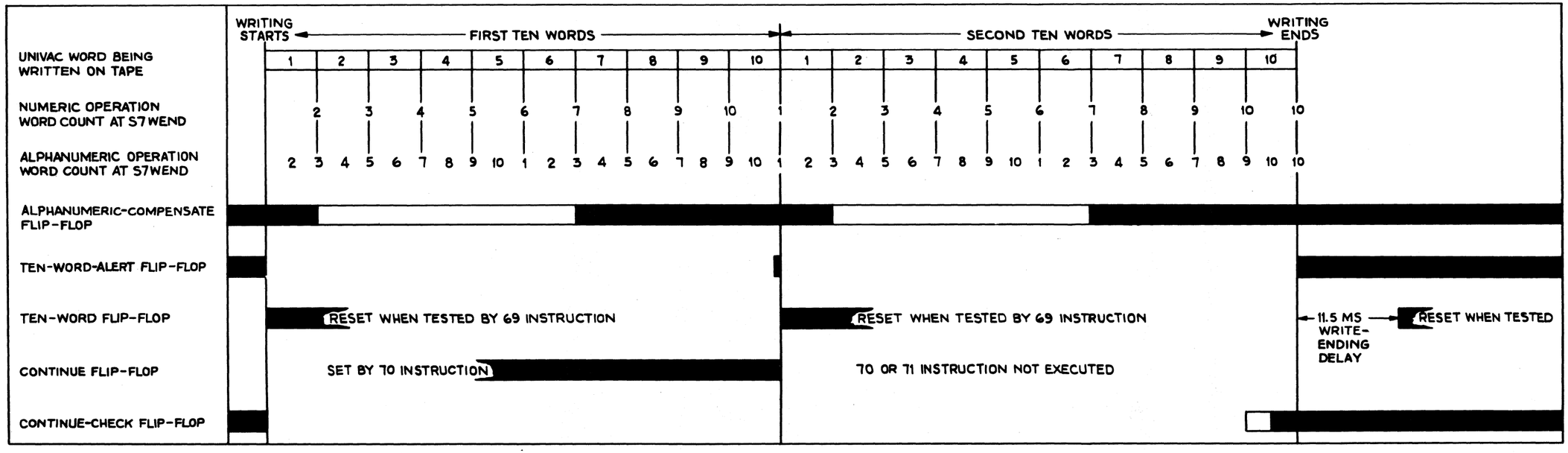
If an SBB follows the current ten-word group, the program may continue the read operation by executing a 71 instruction, thereby setting both the continue and continue-beyond-SBB flip-flops. The latter flip-flop inhibits the ending controls in the read circuits, thus enabling reading to continue through the SBB and into the next block. The continue flip-flop inhibits the gate that sets the check-read and continue-check flip-flops, thus preventing them from being set at the end of the ten-word group and consequently interfering with the read operation.

If an SBB does not follow the current ten-word group, the program may continue the read operation by executing either the 70 or 71 instruction. Either instruction sets the continue flip-flop which, in turn, prevents the check-read and continue-check flip-flops from being set at the end of the ten-word group. The state of the continue-beyond-SBB flip-flop is not significant in this case because the read operation cannot terminate at the end of a ten-word group unless it is followed by an SBB.

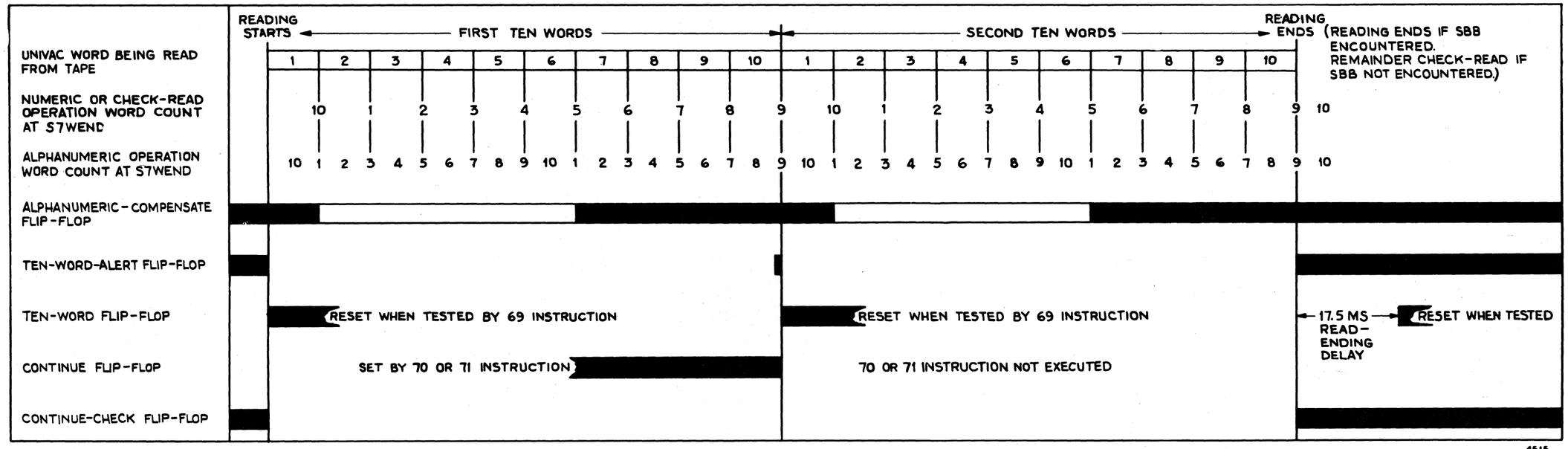
The program can actually control the continuation of a read operation using only the 71 instruction. This may be done by executing the 71 instruction while each ten-word group except the last one is being read.

When an error is detected during a read operation, the read-write error flip-flop resets the continue and continue-beyond-SBB flip-flops. As

A. WRITE OPERATION (20-WORD BLOCK)



B. READ OPERATION (20-WORD BLOCK)



= NUMERIC ONLY

= NUMERIC AND ALPHANUMERIC

NOTES:
1. IF CONTINUE-CHECK FLIP-FLOP IS SET WHEN A 70 OR 71 INSTRUCTION IS EXECUTED, A READ-CHECK ERROR IS GENERATED.
2. FIRST WORD IS WRITTEN INTO OR READ FROM THE EVEN BUFFER REGISTER.

Figure 4-3. Read and Write Word Timing

a result, reading terminates in the same way as it does when neither the 70 nor 71 instruction is executed; that is, the check-read and continue-check flip-flops are set at the end of the current ten-word group, the remainder of the block, if any, is check read, and the check-reading stops at the end of the block.

4-27. CHECK-READ OPERATION. Once check-reading of a block begins, it continues to the end of the block whether or not a 70 or 71 instruction is executed. If check-reading is to continue into the next block, a 71 instruction should be executed while the last ten-word group in the current block is being read. When a non-Univac tape is being check read it is possible to execute the 71 instruction while any one ten-word group is being read in order to continue the operation into the next block. However, with either Univac or non-Univac tape it is usually more convenient to design the program so that a 71 instruction is executed while each ten-word group in every block except the last two blocks is being read and then withold execution of the 71 instruction while the last two blocks are being read.

When an error is detected during a check-read operation, the continue and continue-beyond-SBB flip-flops are reset. As a result, the operation concludes at the end of the current block.

4-28. WRITE OPERATION. When the program is alerted by the ten-word and SBB tests that writing of a new ten-word group has begun, it determines whether the operation is to continue or not. If writing is to end after the current ten-word group has been written, the program witholds execution of both the 70 and 71 instruction, thereby leaving the continue flip-flop reset. When it is reset, the continue flip-flop alerts a gate which sets the continue-check flip-flop after nine numeric or nine and one-half alphanumeric words of the current ten-word group have been written.

The continue-check flip-flop alerts the ending controls in the write circuits and writing ends after the tenth word in the group has been written. The continue flip-flop, when it is reset, also alerts a gate in the buffer register controls which prevents the memory-request flip-flop from being set after the data for the tenth word has been transferred from the memory.

The program may continue the write operation beyond the current ten-word group by using a 70 or 71 instruction to set the continue flip-flop. The output of the continue flip-flop inhibits the setting of the continue-check flip-flop, thereby preventing a write-ending sequence from being triggered at the end of the tenth word. It also inhibits the gate in the buffer register control that prevents the memory-request flip-flop from being set. This gate must be inhibited by the continue flip-flop before the end of nine numeric words or nine and one-half alphanumeric words of the current ten-word group to enable data for the first word of the next ten-word group to be requested from the memory. Therefore, a 70 or 71 instruction must be executed before the end of nine numeric or nine and one-half alphanumeric words if the operation is to continue for ten more words. If it is not executed by then, the continue-check flip-flop is set and writing ends after the tenth word in the currrent group has been written. If a 70 or 71 instruction is executed after the continue-check flip-flop is set, a continue-check error is generated.

If a 71 instruction is executed while the first nine numeric words or nine and one-half alphanumeric words of a ten-word group are being written,

the continue-beyond-SBB flip-flop is set which then alerts the SBB controls in the write circuits. After the tenth word has been written the SBB controls interrupt the write operation to insert an SBB. At the end of the SBB writing continues for ten more words.

When an error is detected during a write operation, both the continue and continue-beyond-SBB flip-flops are reset. If the error occurs while the first nine numeric or nine and one-half alphanumeric words of a ten-word group are being written, the write operation will terminate at the end of the ten-word group. If the error occurs while the tenth numeric word or the last half of the tenth alphanumeric word is being written, the write operation will not terminate until the end of the next ten-word group.

4-29. ERROR CONTROL

Whenever an error is detected by the read-write control circuits, by the write circuits, or by the read circuits when the tape positioning checker is not connected, a read-write error flip-flop is set as well as an appropriate error-diagnostic flip-flop in the central processor. The error signals that set the read-write error flip-flop are listed and described in table 4-3. The number of the error-diagnostic flip-flop that is set when an error signal is generated is also listed. The first two digits of the number in the third column of the table identify the number of the instruction that tests the diagnostic flip-flop; the third digit is the selector digit. For example, diagnostic flip-flop 47-5 is tested by a 47 instruction that has a selector digit of 5.

Table 4-3. Read and Write Error Signals

Error Signal	Signal Name	Diagnostic Flip-Flop Set	Condition Causing Error
		Read/Write Errors	
S7CHE	Continue Check	47-5	Instruction 70 or 71 executed at the wrong time; that is, (1) after the ninth word of a ten-word group has been written, or (2) after a read-to-memory operation has ended, or (3) while the synchronizer is not performing a read, check-read, or write operation.
S7WCE	Word Counter	47-3	An odd-even error in the code combination stored in the word counter.
S7DQE or S7DBE	Digit Counter	47-9	A non-legal code combination in the digit counter.
S7FLE	Overflow	46-4	Memory request sent to dispatcher but word not transferred to or from the buffer register before next request is made.
S7MSE	Memory Select	46-2	Odd-even error in address sent to the address decoder by the dispatcher; or, the address is greater than 97499.
S7E1	HSB	46-1	Odd-even error in data transferred to or from the memory.

Table 4-3. Read and Write Error Signals (cont)

Error Signal	Signal Name	Diagnostic Flip-Flop Set	Condition Causing Error
		Write Errors	
S7WCTE	Write Clutch Test	46-9	A write-clutch-test signal not being returned by the Uniservo tape unit when tested at the end of the ninth word of a ten-word group indicating that the tape unit centerdrive clutch is not engaged. This error condition stops the write operation at the end of the tenth word.
S7SLE2	Sprocket Lost Error	47-4	Write sprocket signal (S7TWC) not generated or not generated in time.
STUP1D	Output Odd-Even	46-6	An odd-even error is detected in a translated output character combination. When this error is detected, the combination 1111111 is written on tape in place of the translated combination.
		Read Errors	
S7OSS	Overskew	47-8	New sprocket signal is detected by the synchronizer before preceding sprocket signal has gated its associated character into the skew flip-flops.
S7BCE	Bad Count	47-7	The number of characters in a block differs by 12 or less from the number actually read. This error initiates a read-ending sequence.
S7VBCE	Very Bad Count	47-2	The number of characters in a block differs by more than 12 from the number actually read. This error initiates a read-ending sequence.
S7RUN	Tape Runaway	46-0	Tape travels 17½ inches without data being detected by synchronizer. This error signal initiates a read-ending sequence.
S7HDE	Hash-Pulse-Period Odd-Even	46-5	Input odd-even error detected during hash-pulse period.
S7HUNT	Hash-Pulse-Period Untranslatable	46-3	An untranslatable error* detected during a hash-pulse period.
STROE**	-	46-5 If odd-even error; 46-3 if untranslatable error	An input odd-even error or an untranslatable error* detected during a period other than a hash-pulse period. If an untranslatable error is detected, the code combination for a plus (00111) is written into the input buffer register in place of the untranslatable combination.

* An untranslatable error is produced during a numeric read-to-memory operation if the Univac code digit being translated does not have a Larc one-digit-code equivalent.

** STROE is gated with S7HPG, S7TRC, $\overline{\text{SCT1}}$, and T0,4 to set the tape read-write error flip-flop.

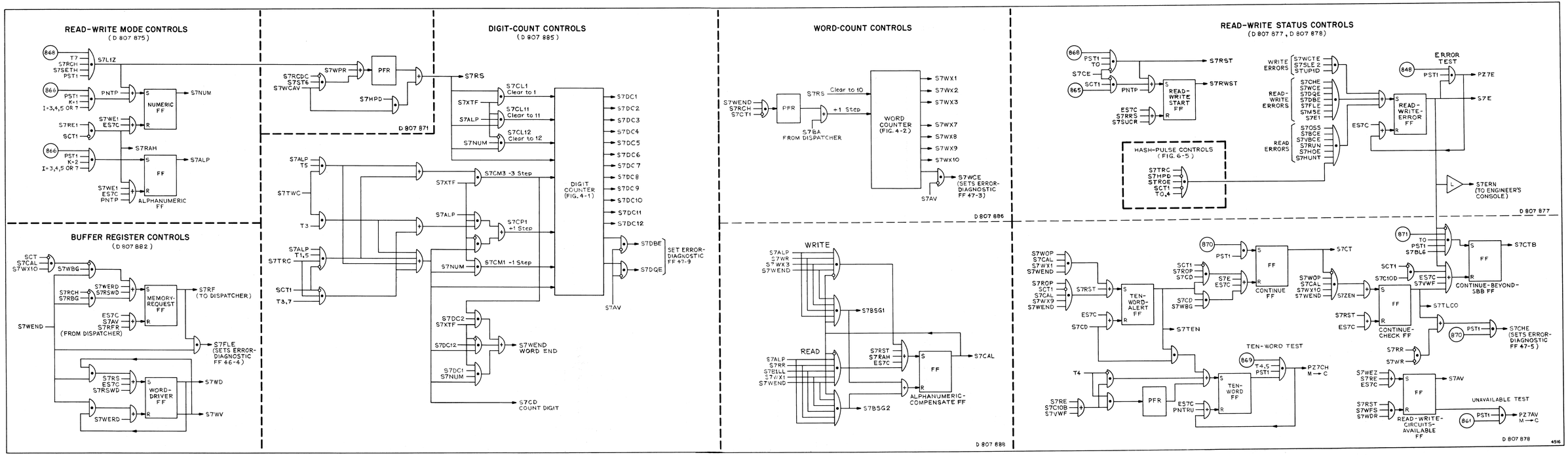


Figure 4-4. Read-Write Control Circuits

SECTION 5
WRITE CIRCUITS

5-1. GENERAL

The write circuits in the magnetic tape synchronizer operate in close conjunction with the read-write control circuits and the time-shared Larc-to-Univac translator and output checker in performing a write operation. Timing signals, for clearing the output buffer registers and for controlling tape writing density, are supplied to the write circuits by the tape timing signal generator. The write circuits (figure 5-2) divide functionally into seven subdivisions, as follows:

(1) Write Mode Controls. The write mode controls control, as specified by the program, the length of the space between data blocks and the writing density.

(2) Write-Start Controls. The write-start controls control initial clearing and loading of the output buffer registers and starting and interrupting of the tape-write operations.

(3) Output Buffer Read-Driver Controls. The output buffer read-driver controls control the magnetic-amplifier drivers that clear or read data out of the tape-synchronizer output buffer registers in the dispatcher.

(4) Write Output Circuits. The write output circuits receive character combinations from the Larc-to-Univac translator and record them on tape in accordance with the specified pulse density.

(5) Write SBB Controls. The write SBB controls interrupt the write operation to insert spaces of the specified length between blocks of data on tape.

(6) Write Bad-Spot Controls. The write bad-spot controls interrupt the write operation while sections of tape, unsuitable for recording purposes, pass the read-write head.

(7) Write-Ending Controls. The write-ending controls stop the write operation at the end of the last block, clear the write circuits, stop tape travel, and disconnect the write bus from the Uniservo tape unit.

The seven subdivisions are individually discussed in the following paragraphs. Although they are not considered part of the write circuits of a tape synchronizer, the output buffer registers and the Larc-to-Univac translator and output checker are included in figure 5-2 to achieve continuity in tracing a write operation through the diagram. Since the write circuits and the read-write control circuits operate together as a unit, it will be necessary in this section to frequently refer to the diagrams in figures 4-3 and 4-4 illustrating the read-write control circuits and the timing relationships.

5-2. WRITE MODE CONTROLS

There are three mode flip-flops in the write mode controls (figure 5-2); they are the high-pulse-density, the low-pulse-density, and the SBB flip-flops.

5-3. PULSE-DENSITY FLIP-FLOPS

The state of the low-pulse-density and high-pulse-density flip-flops determines the tape writing density. One or the other of the two flip-flops is set during a write operation. When the low-pulse-density flip-flop is set and the high-pulse-density flip-flop is reset, the write output circuits are alerted to write on tape at a density of 104 PPI (in the Larc System, Serial 1) or 125 PPI (in the Larc System, Serial 2). When the high-pulse-density flip-flop is set and the low-pulse-density flip-flop reset, the write output circuits are alerted to write on tape at a density of 208 PPI (in the Larc System, Serial 1) or 250 PPI (in the Larc System, Serial 2).

The 66 instruction sets the low-pulse-density flip-flop if the I digit of the control-data word in register P1 specifies a low-density write operation (I = 7); the high-pulse-density flip-flop is set if the I digit specifies a high-density write operation (I = 5). Both flip-flops are reset at the end of the write operation by the write-ending signal, S7WE2.

Because one or the other of the density flip-flops is set throughout a write operation, signals are generated by these flip-flops which indicate that a forward operation is being performed (signal S7XTF) and that the write circuits are available (signals S7WCAV, S7SETH, and S7B1LL) or in use (signal S7WBG). S7XTF is also generated during a forward-read operation.

5-4. SBB FLIP-FLOP

The state of the SBB flip-flop determines the length of the spaces left between blocks of data during a write operation. When the SBB flip-flop is set, the SBB and write-start controls are alerted to leave a 1.0-inch space between blocks (SBB). When the flip-flop is reset the write-start controls are alerted to leave a 2.4-inch SBB. A 66 instruction sets the flip-flop if the I digit of the control-data word in register P1 specifies a write operation (I = 5 or 7) and the L digit specifies a 1.0-inch SBB (L = 0). The flip-flop is always reset at the end of a write operation by the write-ending signal, S7WE1. When a 2.4-inch SBB is specified by the L digit (L = 1), the 66 instruction does not reset the flip-flop; however, it should already be reset from the end of a previous write operation.

5-5. WRITE-START CONTROLS

Before a tape synchronizer can begin recording data on tape the following three conditions must be satisfied:

(1) Both output buffer registers must be cleared and the first data word loaded into the even buffer register.

(2) The tape must accelerate and travel a distance equal to approximately one-half the specified SBB.

(3) The read-write start flip-flop in the read-write circuits must be set by a 68 instruction.

An additional factor must be considered when the Uniservo tape unit is starting from the first-block state; that is, a bad area may exist at the beginning of the tape. Because of this possibility, the write start must be delayed to allow a bad area of tape to pass the read-write head if a write photocell signal is generated near the end of the first-block delay period.

The three basic functions of the write-start controls (figure 5-2) are as follows:

(1) Control the clearing and the initial loading of the output buffer registers.

(2) Delay the start of the write operation until the tape has accelerated and traveled the proper distance for the specified SBB.

(3) Start the write operation when all conditions for beginning the operation have been satisfied, provide the means for interrupting the write operation while an SBB is being inserted or a bad spot is passing the read-write head, and provide the means for stopping the operation.

To simplify the description of the write-start controls, they are divided into three sections, reflecting the three basic functions listed above. The three sections are the output buffer ready controls, tape ready controls, and write operate controls.

5-6. OUTPUT BUFFER READY CONTROLS

Before a tape synchronizer can begin a write operation both output buffer registers must be cleared to ensure that no extraneous data remains from the last write operation. Normally, the registers will conclude an operation cleared of all data; however, if the last write operation was not completed because of an error condition or machine failure, there may be extraneous data remaining. After both registers have been cleared, the dispatcher is alerted to transfer the first output data word from storage to the even output buffer register. When the first word is loaded in the register, the dispatcher is alerted to load the second word in the odd output buffer register. Simultaneously, an output-buffer-ready flip-flop is set which alerts the write-operate controls to the fact that the registers are prepared for the start of the write operation.

The clearing of the output buffer registers is triggered by the write-preset signal (S7WPR) from the Uniservo control circuits. This signal is generated after the Uniservo tape unit has been prepared for a write operation but before tape motion has started. It sets the write-preset flip-flop which, in turn, alerts the set gate of the output-buffer-clear flip-flop. The output-buffer-clear flip-flop then sets at TSS of signal TON (figure 3-4) and resets at the following TSS. While it is set, the output-buffer-clear flip-flop alerts the output buffer read drivers to clear both output buffer registers. During the clear cycle, the read drivers are stepped by the TT timing signals from the tape timing signal generator.

In order to reduce drive requirements on the TT timing signals, which are applied to output buffer read gates of all four synchronizers, the output-buffer-clear flip-flops in Synchronizers 8, 9, and 10 are interlocked to ensure that only one synchronizer at a time will clear its buffer registers. The interlocking is controlled by the write-preset flip-flops. When the write-preset flip-flop in one synchronizer is set, it inhibits the setting of the output-buffer-clear flip-flop in a higher-numbered synchronizer. Thus, Synchronizer 7 is given first priority in clearing, followed in order by Synchronizers 8, 9, and 10. The timing signals (TSS and TON) that begin and end the clear cycles ensure that a clear cycle never coincides with a tape-write cycle. Since the digits cleared from the tape-output buffer registers feed directly into the Larc-to-Univac translator, this ensures that the clearing of an output buffer register by one tape synchronizer does not interfere with the translation of a digit during a write cycle in another tape synchronizer.

At the end of the clear cycle, S7WERD signals the buffer register controls to alert the dispatcher to transfer the first output data word from storage and load it into the even output buffer register. S7WERD also sets the first-word-requested flip-flop which then tests the S7PGR return signal from the dispatcher. When S7PGR is returned, indicating that the first word has been loaded, S7RSWD is generated. S7RSWD signals the buffer register controls to initiate the transfer of the second data word into the odd output buffer register; it also sets the output-buffer-ready flip-flop to indicate that the buffer registers are ready for a write operation.

5-7. TAPE READY CONTROLS

When a write operation starts with the read-write head positioned over an SBB, it is necessary to delay the actual writing until the tape has accelerated and has traveled a distance equal to approximately one-half the SBB specified by the program. The delay allows time for the centerdrive circuits in the Uniservo tape unit to operate and the tape to accelerate and travel a distance which, when added to the distance between the end of the previous block and the starting point, will provide an SBB of a nominal 1.0 or 2.4 inches. For a 1.0-inch SBB this delay is 8.7 milliseconds; for a 2.4-inch SBB it is 22.7 milliseconds. Because of tape speed and acceleration tolerances in the Uniservo tape unit and tolerances in the delay device itself, the length of the SBB will vary somewhat. However, the minimum length will allow enough time during a read operation for the tape to stop at the end of a block of data and then to start and accelerate to full speed before the beginning of the next block reaches the read-write head.

The delay is triggered by signal S7WSTU (which is generated by the Uniservo control circuits) when the Uniservo centerdrive signal is turned on to start tape motion. S7WSTU tests the outputs of the SBB mode flip-flops (S7SBB0 and S7SBB1) and triggers one of two RDF's. If S7SBB0 is present (indicating that a 1.0-inch SBB was specified by the program) an 8.7-millisecond RDF is triggered. If S7SBB1 is present (indicating a 2.4-inch SBB was specified) a 22.7-millisecond RDF is triggered. When the triggered RDF recovers, a tape-ready flip-flop is set indicating that the tape is in position to begin writing; provided, however, that the write operation is not starting from a first-block condition.

5-8. WRITE OPERATE CONTROLS

After the output-buffer-ready, tape-ready, and read-write start flip-flops are all set, the write-ready flip-flop is set which then generates an S7WOP signal. S7WOP is a key signal which starts the synchronizer recording output data stored in the buffer registers.

After tape motion has started, the read-write start flip-flop in the read-write control circuits is set by a 68 instruction. The time at which the 68 instruction is executed determines whether or not a first-block delay will occur. If the write operation is starting from an SBB, the program will execute the 68 instruction immediately. If the operation is starting from the first-block condition, the execution of the instruction will be delayed by the program for 1.6 seconds until the tape leader has passed the read-write head. In the latter case, the read-write start flip-flop will be set after the tape-ready flip-flop and override the 8.7- or 22.7-millisecond delay.

In the event a bad spot is detected near the end of a first-block delay, it is necessary to delay the beginning of the write operation until the bad spot has passed the read-write head. In such a case the write operation is delayed by a gate which has as inputs S7FB from the first-block flip-flop in the Uniservo control circuits and S7WBSF from the write bad-spot controls. A complete explanation of bad-spot control is found under heading 5-14.

When all conditions for beginning the write operation have been satisfied, S7SUCR sets the write-ready flip-flop, thereby generating S7WR and S7WOP. S7WR alerts various gates in the synchronizer that are involved in the write operation, and S7WOP begins the operation. S7SUCR also clears (resets) the read-write start, output-buffer-ready, tape-ready, and inhibit-write flip-flops. In generating S7SUCR, the write-ready flip-flops acts as a single pulser, since its output is recirculated through the set gate to turn off the signal 0.5 μsec after it is generated.

After the write operation starts, it is interrupted or terminated setting the inhibit-write flip-flop which inhibits S7WOP. When it is necessary to interrupt writing to insert an SBB, the inhibit-write flip-flop is set and reset by S7VWF and S7VWR, respectively, from the SBB controls. When writing is interrupted to allow a bad spot to pass the read-write head, the flip-flop is set and reset by S7VRW and S7RSWB, respectively, from the write bad-spot controls. At the completion of a write operation the inhibit-write flip-flop is set and the write-ready flip-flop is reset by S7WHF and S7WE1, respectively, from the write-ending controls.

5-9. OUTPUT BUFFER READ-DRIVER CONTROLS

The output buffer read-driver control circuits (figure 5-2), generate signals which energize magnetic-amplifier drivers that clear or read the cores of the two output buffer registers of the tape synchronizer. Each register has 12 read drivers, each of which drives the five cores of a digit location. Each driver is triggered by a 1-μsec signal produced by either of two gates, a clear gate or a read gate. The signals produced by these gates are designated S7RD1 through S7RD12 for the odd register and S7RV1 through S7RV12 for the even register.

The 24 clearing gates of the combined odd and even registers are alerted at the start of a tape-write operation by signal S7WST from the output-buffer-clear flip-flop in the write-start controls. S7WST remains on for 24 μsec in the Larc System, Serial 1 and for 20 μsec in the Larc System, Serial 2. During this on period the clear gates are systematically stepped by combinations of 4-μsec signals from the tape timing signal generator and 1-μsec signals derived from the main cycling unit. Thus, both registers are cleared of any extraneous data remaining from a previous tape-write operation.

The 12 read gates for each buffer register are alerted by the 12 outputs (S7DC1 through S7DC12) of the digit counter (figure 4-1). Consequently, the order in which digits are read from a register during a tape-write operation is controlled by the way in which the digit counter is stepped. The time at which a digit is read out of a register is controlled by two read-control gates associated with each register. While digits are being read out of one register, a signal from the word-driver flip-flop in the read-write circuits inhibits the read-control gates of the other register. After a complete word has been read out of one register, the word-driver flip-flop changes state, thereby reversing the roles of the two registers. One of the two read-control gates of a register is alerted by S7ALP and is therefore permissive only during an alphanumeric (two-digit) tape-write operation. The other gate is permissive during both a numeric and an alphanumeric write operation. During a tape-write cycle the read gates of a register are sampled at T2,3 to energize the one read driver corresponding to the digit count. If an alphanumeric operation is being performed, the read gates are sampled again at T4,5 of the same tape-write cycle. Between readouts the digit counter is stepped so that a different driver is energized each time. The two digits of an alphanumeric pair appear at the output of the register cores at T4 and T6, respectively (figure 5-1) and enter directly into the Larc-to-Univac translator and output checker. For a numeric operation, the digit counter is stepped to read the digits of a word out of a register in a straight sequence (12 through 1) beginning with the MSD. For an alphanumeric operation, a pair of digits are read out of a register during each tape-write cycle and the digit counter is stepped to read the digits in the following sequence:

11,12 9,10 7,8 5,6 3,4 1,2

5-10. WRITE OUTPUT CIRCUITS

The write output circuits (figure 5-2) in only the Larc System, Serial 1 are covered in detail in the following paragraphs; however, the description also applies to the Larc System, Serial 2 except for the differences in the timing of the circuits which are treated separately under heading 5-12.

5-11. LARC SYSTEM, SERIAL 1

The write output circuits, under the influence of timing signals (figure 3-4) from the tape timing signal generator, control the character-by-character recording of data on tape. The circuits are made up of the following:

(1) A tape-write-cycle flip-flop which is set at regularly recurring intervals during a write operation to generate signals that control the tape writing density.

(2) A write-sprocket flip-flop and seven write-output flip-flops which receive a sprocket pulse and the seven bits of a character during each tape-write cycle and store them while they are recorded on tape.

(3) Eight write amplifiers which amplify the contents of the sprocket and write-output flip-flops for transmission over the write bus to the Uniservo tape unit.

(4) A pulse-length-control flip-flop which is set each tape-write cycle during a low-density write operation to double the recording time of a character.

(5) A sprocket checker which checks to ensure that the tape-write-cycle flip-flop is set periodically during a write operation.

In the Larc System, Serial 1 the tape writing density is either 208 or 104 pulses per inch (PPI). The 208 PPI writing density is the equivalent of a character rate of one character each 48 μsec. Each character is recorded on the basis of a 50-50 duty cycle. During the first 24-μsec period, the read-write heads are energized to record in parallel on tape a sprocket bit and the seven bits of a character. During the second 24-μsec period, the read-write heads are not energized resulting in a space between characters being left on the tape. Similarly, the 104 PPI writing density is the equivalent of a duty cycle of 96 μsec, which divides into two 48 μsec periods for recording a character and leaving a space.

The writing of a character on tape is controlled by the tape-write-cycle flip-flop. During a write operation, this flip-flop is periodically set by signals from the tape timing signal generator. It is set once each 48 μsec by TON and TS7 when the synchronizer is writing at a density of 208 PPI, and once each 96 μsec by TON, T100, and TS7 when writing

at 104 PPI. The tape-write-cycle flip-flop remains set for 4 μsec; during this time it does the following:

(1) Alerts the output buffer read-driver controls to read a digit or digit pair from an output buffer register into the Larc-to-Univac translator.

(2) Alerts the digit counter to step to the next count as each digit is read from a buffer register.

(3) Sets the one-digit-translate flip-flop in the translator if the numeric mode flip-flop is set.

(4) Sets the write-sprocket flip-flop and gates the 1 bits of the translated character into the seven write-output flip-flops where they are amplified and transmitted over the tape-write bus.

(5) Sets the pulse-length-control flip-flop if the low-pulse-density mode flip-flop is set.

(6) Samples the output odd-even checker and sets all seven of the write-output flip-flops to the 1 state if an odd-even error is detected.

In Synchronizer 7 the setting of the tape-write-cycle flip-flop is triggered by timing signal TS7. The corresponding flip-flops in Synchronizers 8, 9, and 10 are set by timing signals TS8, TS9, and TS10, respectively. Consequently, the tape-write cycles in the four synchronizers never overlap which ensures proper time-sharing of the translator.

Write timing is shown in figure 5-1 for the four tape synchronizers operating simultaneously. Synchronizers 7 and 10 are represented performing low-density write operations (the pulse-length-control flip-flop is set each cycle and the write pulse duration is 48 μsec followed by a 48-μsec space between pulses). Synchronizers 8 and 9 are represented performing high-density write operations (the pulse-length-control flip-flop is not set and the write pulse duration is 24 μsec followed by a 24-μsec space between pulses).

The tape-write-cycle flip-flop remains set for 4 μsec. At the end of this period (at T7) a character from the translator is gated into the write-output flip-flops and the write-sprocket flip-flop is set. At the same time, the pulse-length-control flip-flop is set if a low-density operation is signified by the presence of S7P100. In Synchronizer 7, the write-output, write-sprocket, and pulse-length-control flip-flops are all reset by the TS8 timing pulse. If a high-density operation is being performed, the write-output and write-sprocket flip-flops are cleared after 24 μsec by the first TS8 pulse. However, if a low-density operation is being performed, the first TS8 pulse is inhibited by the pulse-length-control flip-flop and the write-output and write-sprocket flip-flops are cleared, after 48 μsec have elapsed, by the next TS8 pulse. In Synchronizers 8, 9, and 10, the write-output, write-sprocket and pulse-length-control flip-flops are cleared by TS9, TSK, and TSS, respectively.

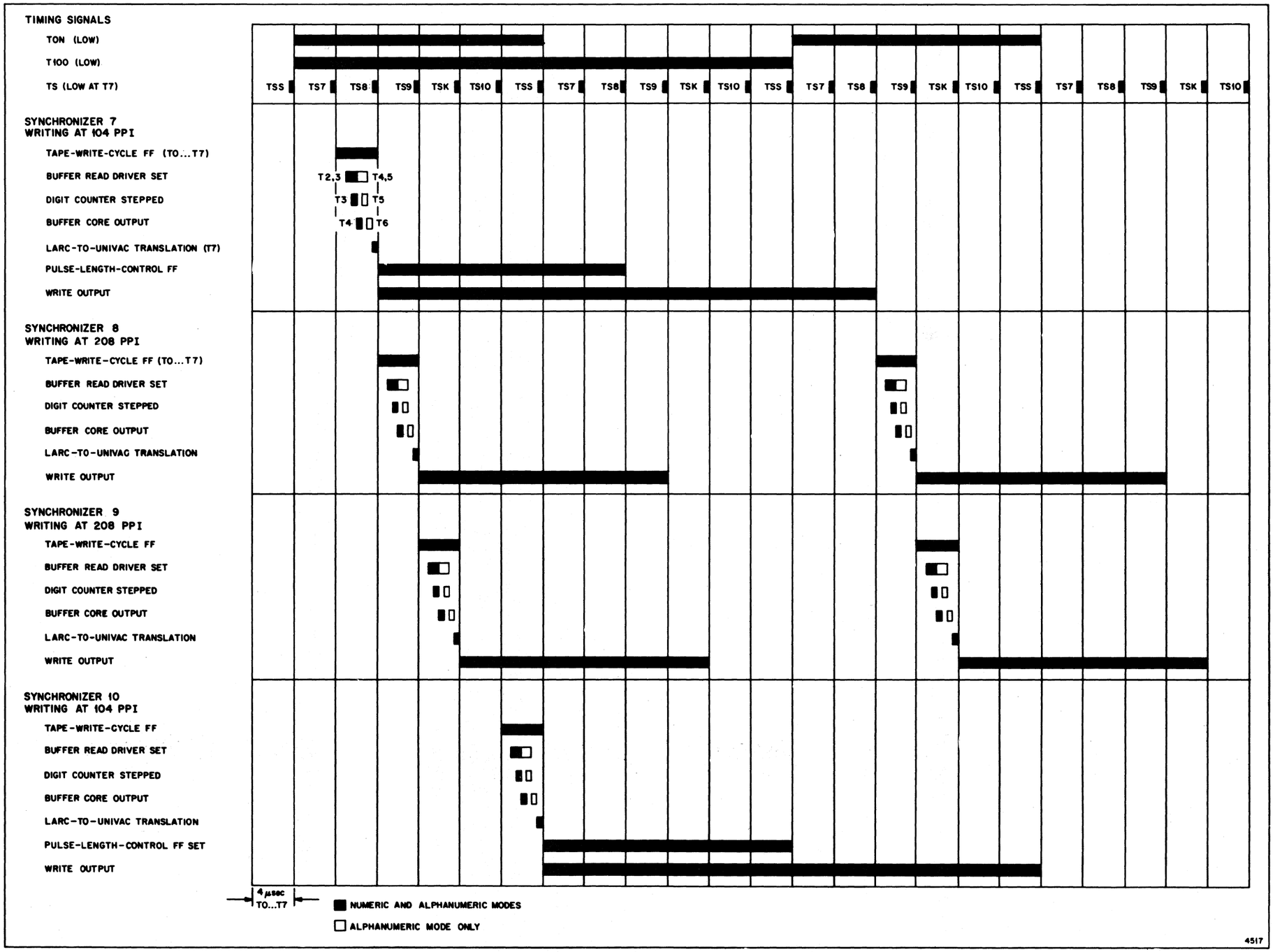


Figure 5-1. Write Cycle Timing, Larc System, Serial 1

The signal that sets the write-sprocket flip-flop is delayed for 0.5 μsec and tests STUEA from the output odd-even checker. If an error was detected in the translated combination, all seven of the write-output flip-flops are set, thereby replacing the translated combination with a combination consisting of all 1's.

Each time the tape-write-cycle flip-flop is set it triggers either a 120-μsec or 60-μsec RDF depending on whether a low- or high-density operation, respectively, is being performed. If the RDF recovers while the synchronizer is writing, S7SLEZ is generated and sets the tape read-write error flip-flop and the sprocket-check diagnostic flip-flop. During a low-density write operation the tape-write-cycle flip-flop normally is set each 96 μsec. Therefore, the 120-μsec RDF should not recover unless the tape-write-cycle flip-flop fails to set in time. Similarly, during a high-density write operation the tape-write-cycle flip-flop normally is set each 48 μsec and the 60-μsec RDF should not recover.

5-12. LARC SYSTEM, SERIAL 2

This paragraph discusses the differences between the write output circuits in the Larc System, Serial 1 and Larc System, Serial 2. It presupposes a knowledge of the write output circuits in the Larc System, Serial 1; if such is not the case, it is necessary to read the paragraphs under heading 5-11 before continuing.

In the Larc System, Serial 2 the writing densities are 125 and 250 PPI, the equivalent of write pulse times of 40 and 20 μsec, respectively. The increased writing density in the Larc System, Serial 2 is achieved by eliminating one of the flip-flops (FF2) present in the cycling unit of the tape timing signal generator used in the Larc System, Serial 1. The effect of this may be seen by referring to figure 3-4. Since FF2 in the cycling unit is eliminated, timing signal TT2 is not generated. Also, TSK is not generated and TON and T100 are shortened to 20 and 40 μsec, respectively. The effect of this on the write output circuits is to increase the writing density from 104 to 125 PPI or from 208 to 250 PPI. Other than this, there is only one other significant difference between the write output circuits in the two systems: because TSK is not present in the Larc System, Serial 2, TS10 is used in Synchronizer 9 to reset the pulse-length-control, write-output, and write-sprocket flip-flops.

5-13. WRITE SBB CONTROLS

The write SBB controls (figure 5-2) detect the conditions necessary for inserting an SBB during a write operation; they also interrupt writing until a 1.0 or 2.4-inch length of tape, depending on the SBB specified by the program, has passed the read-write head. The controls also provide an indication to the program that an SBB is being inserted.

An SBB will be inserted after writing a ten-word group if the continue-past-SBB flip-flop in the read-write status controls is set by a 71 instruction while the ten words are being written. The set output of the continue-past-SBB flip-flop alerts two gates which detect the end of a ten-word group

by sampling S7WX1, S7CAL, and S7WEND. One gate is alerted by the 1.0-inch SBB mode signal (S7SBB0) and the other by the 2.4-inch SBB mode signal (S7SBB1). Depending on which SBB mode was specified by the program, either a 10 or a 24-millisecond RDF is triggered. At the same time, S7VWF is generated which sets the inhibit-write, ten-word, and write-SBB flip-flops and resets (clears) the continue-past-SBB flip-flop. After the RDF recovers, S7VWR is generated to reset the inhibit-write and write-SBB flip-flops. Since the tape travels at 100 inches per second the 10 or 24 milliseconds during which writing is interrupted will result in an SBB of 1.0 or 2.4 inches, respectively.

The signal from the set output of the write-SBB flip-flop, together with a similar signal from the read circuits, is tested by the 73 instruction. This test provides the program with a means for keeeping track of the blocks written. After the tape has stopped at the end of a write operation, S7WE2 from the write-ending controls triggers the 10-millisecond RDF and generates S7VWF which, by setting the write-SBB and ten-word flip-flops, alerts the program to the completion of the operation. After the 10-millisecond RDF recovers, S7VWR resets the write-SBB flip-flops.

5-14. WRITE BAD-SPOT CONTROLS

Sections of tape possessing poor magnetic properties and sections containing splices are designated bad spots. (Figure 6-4, although not intended to support this paragraph, is nevertheless useful in illustrating some of the subjects of this discussion.) These bad spots are identified by at least two holes punched through the tape. The spacing between holes is nominally 2.5 inches but may vary somewhat due to bad-spot holes that are hand-punched over splices made in the field. The first hole of a series of holes precedes the actual bad spot and the last hole follows it. Thus, the bad area is marked to allow for both forward and backward tape movement.

Photocells mounted on the tape panel of the Uniservo tape unit detect the bad-spot holes during tape motion. When a hole is detected a signal is generated to alert the synchronizer to the approach of a bad spot. During a write operation the holes are detected by two forward photocells connected in parallel. The two forward photocells are located 5 and 4-1/4 inches from the read-write head.

If a forward photocell detects a hole during a write operation, signal S7WPA is sent to the synchronizer. (See figure 5-2.) The trailing edge of this signal triggers a 100-millisecond RDF and interrupts the write operation after the current word has been written.

Although the tape continues to move past the photocells, the write operation continues interrupted until the RDF recovers. Since the holes are 2.5 inches apart and the tape travels at 100 inches per second, a new S7WPA signal will be generated by each of the two forward photocells each 25 milliseconds until the end of the bad area. Thus, the second and succeeding holes will retrigger the 100-millisecond RDF before it recovers and writing will be suspended until 100 milliseconds elapse after the last hole is detected by the forward photocell nearest the read-write head. Since 100 milliseconds of tape motion is the equivalent of 10 inches of tape

travel, and since the nearest photocell is 4-1/4 inches from the read-write head, writing will not resume until the last hole is about 5-3/4 inches past the head.

Several special conditions arise to complicate the write bad-spot controls. When writing on tape the SBB must be held to the standard 1.0 or 2.4 inches in order that proper timing of a read or write operation may be maintained. Therefore, the tape area between data blocks must not be cut by a bad area. Furthermore, the last word of a ten-word group must not be cut by a bad area because the read circuits are alerted to detect an SBB during the whole time the last word is being read. If the last word should be cut by a bad area, the bad area would appear to the read circuits as an SBB and a bad-count error would result. Since the first word of a ten-word group becomes the last word during a backward read operation, the same situation arises. In view of these conditions, the write bad-spot controls must be inhibited from interrupting the write operation from the beginning of each tenth word, through the SBB (if an SBB is inserted), and through the first word of the following ten-word group. However, due to certain peculiarities of the bad-spot controls, the interruption of writing is actually inhibited through the first two words during a numeric-write operation and through the first one and one-half words during an alphanumeric-write operation.

The write operation is interrupted for a bad spot by signal S7VRW which sets the inhibit-write flip-flop in the write-start controls. The gate that generates S7VRW is alerted by the write-operate signal (S7WOP) and by the write bad-spot-detector and write bad-spot-gating flip-flops. The write-bad-spot detector flip-flop is set by the trailing edge of the write-photocell signal and remains set until the 100-millisecond RDF, triggered by the same signal, recovers. The write bad-spot-gating flip-flop is set after the first word of a ten-word group has been written, and is reset before the ninth word is written. The gate that generates S7VRW is sampled at the end of each word by S7WEND. Since the gate is not alerted by the write bad-spot-gating flip-flop until after the end of the first word, S7VRW cannot be generated (by S7WEND) during a numeric-write operation until the end of the second word, and during an alphanumeric-write operation until the end of one and one-half words. When the 100-millisecond RDF finally recovers, S7RSWB resets the write bad-spot-detector flip-flop and resets the inhibit-write flip-flop, thus turning on the S7WOP signal that enables writing to begin again.

Another case must be considered in connection with the write bad-spot controls; that is, a bad area may exist at the beginning of the tape. The start of the write operation must therefore be delayed in the event a bad spot occurs near the beginning of the first block. The delay is accomplished by gating S7WBSF from the write bad-spot-detector flip-flop with the first-block signal (S7FB) from the first-block flip-flop in the Uniservo control circuits. If both of these flip-flops are set the write-ready flip-flop in the write-start controls is prevented from setting, thereby delaying the start of the write operation. Thus, if holes are detected just before the writing of the first block is to start, the start is delayed until 100 milliseconds after the last hole is detected by which time the bad spot will have passed the read-write head.

Normally, only one forward photocell would be required on the Uniservo tape unit for bad-spot control; however, to accommodate certain extreme

operating conditions two forward photocells are used. For example, if the tape synchronizer detected a hole while writing the last word of a block, then terminated the operation and stopped the tape after the block was written, the S7WPA signal would trigger the 100-millisecond RDF. However, writing would not be interrupted because interruption is inhibited during the last word by the write bad-spot-gating flip-flop. Furthermore, the RDF would recover while the tape was stopped and no indication would remain that a bad spot was detected. Normally, such a situation would not be a problem because the next hole in a series would be detected after the next operation started and would interrupt writing before the bad tape area reached the read-write head. However, if only one photocell were used, it would be possible under certain conditions to lose the indication of the second hole. This could happen if the synchronizer were writing at high density with a 1.0-inch SBB. If, after losing the indication of the first hole, the synchronizer wrote a single ten-word block and then stopped the tape, it would be possible for the second hole to be detected and the indication of it to be lost in the same way as the first. When the tape started and writing began again, the writing would occur over the bad area. The provision of the second photocell ensures that a bad tape area, missed by the first photocell under the conditions described, will be detected by the second photocell and writing will be inhibited before the bad area reaches the read-write head.

5-15. WRITE-ENDING CONTROLS

Normally, a write-ending sequence is begun after writing a ten-word group if a 70 or 71 instruction is not executed while the first nine (numeric) or nine and one-half (alphanumeric) words are being written. This condition is detected by testing S7TLC0 from the continue-check flip-flop with the word-end signal (S7WEND). (See figure 5-2.) The continue-check flip-flop is set at the end of nine numeric or nine and one-half alphanumeric words if the continue flip-flop is not set as a result of a 70 or 71 instruction being executed. When the continue-check flip-flop is tested at the end of the tenth word (by S7WEND) and is found to be set, a 1.5-millisecond RDF is triggered and the write-ending sequence begins.

The write-ending sequence is also initiated in the event the center-drive clutch in the Uniservo tape unit is found to be disengaged. This condition is detected by testing the write clutch-test signal from the tape unit at the beginning of each ten-word group. If the clutch is disengaged, indicating that tape motion has stopped, signal WCTE is generated which sets the preset error-diagnostic flip-flop and triggers the 1.5-millisecond RDF that begins the write-ending sequence.

When the 1.5-millisecond RDF is triggered it sets the inhibit-write flip-flop, thereby ending writing as soon as the current character is written. When the RDF recovers, S7WE1 is generated. S7WE1 triggers a 10-millisecond RDF, clears the write and read-write mode flip-flops, resets the write-ready flip-flop, and resets the write-centerdrive flip-flop in the Uniservo control circuits, thus stopping tape motion. Resetting of the write-centerdrive flip-flop is delayed for 1.5 milliseconds in order to keep the distance the tape travels before stopping at the end of a write operation approximately equal to the distance the tape travels before stopping at the end of a read operation. A read-ending sequence is not begun until 1.5 milliseconds after the last sprocket pulse in a block is

read. This delay ensures that a sprocket pulse preceding a missing or skipped sprocket pulse will not be erroneously detected as the last sprocket pulse in a block. If the stopping delay were not the same for reading and writing, a data block that was alternately and repeatedly read and written would gradually creep toward an adjacent data block and finally overlap it.

When the 10-millisecond RDF is triggered by S7WE1, it energizes a write-clear relay in the Uniservo power supply cabinet. The energized write-clear relay extinguishes the Uniservo write thyratrons, thus disconnecting the Uniservo read-write head from the write bus. A hash-pulse pattern is written on tape when the read-write head is disconnected. Since the tape has stopped by this time, the hash-pulse pattern occurs at the approximate center of the SBB.

When the 10-millisecond RDF recovers, S7WE2 is generated. Signal S7WE2 does three things:

(1) It sets the ten-word flip-flop to alert the program to the completion of the write operation.

(2) It sets the write-SBB flip-flop. This flip-flop remains set for 10 milliseconds to indicate to the program that an SBB has been inserted.

(3) It sets the read-write-circuits availability flip-flop to indicate to the program that the write and read-write circuits are available for another operation.

The 10-millisecond RDF serves two purposes; first, it provides a signal of sufficient time duration to energize the write-clear relay, and second, it delays making the read-write circuits available until the Uniservo tape unit has been disconnected from the write bus.

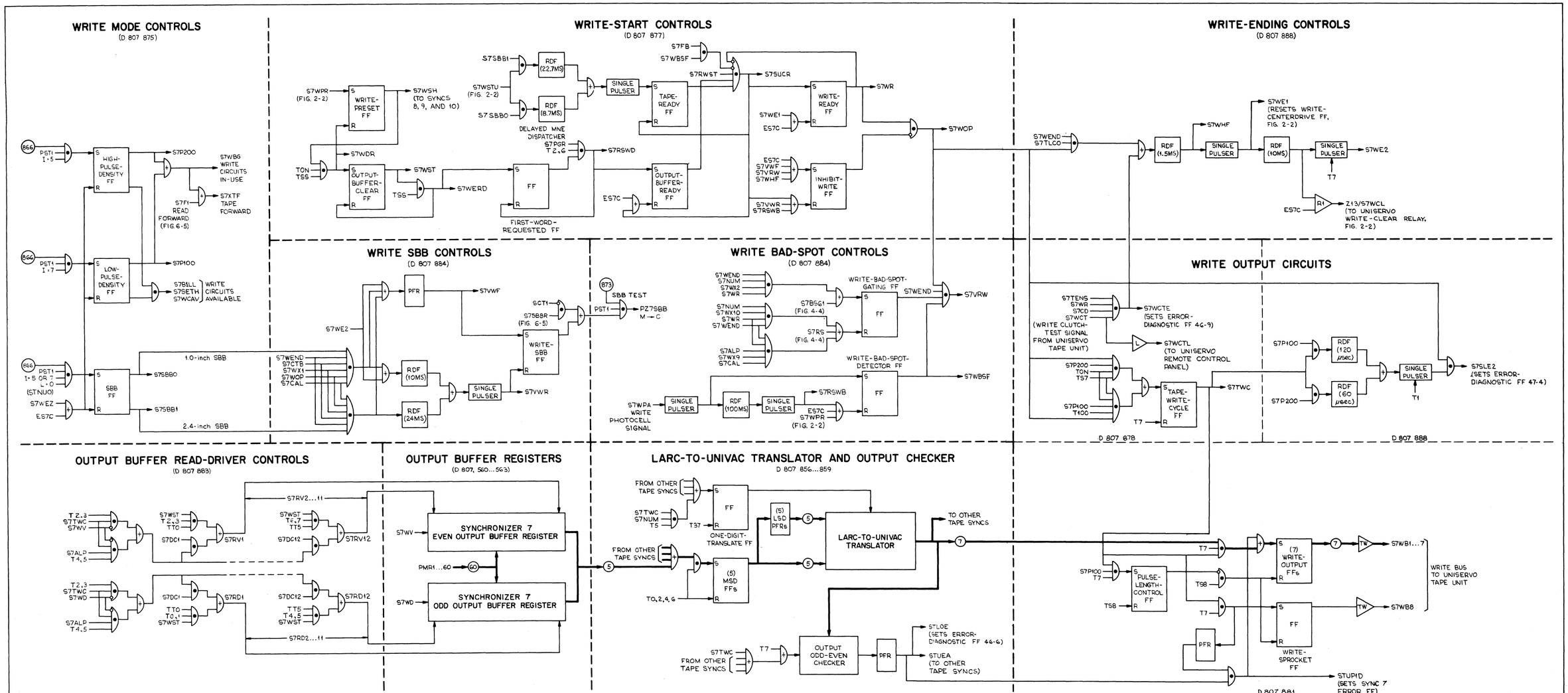


Figure 5-2. Write Circuits, Simplified Logic Diagram

SECTION 6
READ CIRCUITS

6-1. GENERAL

The read circuits operate in close conjunction with the read-write control circuits and the time-shared Univac-to-Larc translator and input checker in performing a read or check-read operation. Or, they function with the tape positioning checker in performing a check-read operation only. The read circuits (figure 6-5) divide functionally into eight subdivisions, as follows:

(1) Read Mode Controls. As specified by the program, these controls control the gain of the read amplifiers and adjust the operation of the synchronizer to read or check-read in a forward or backward direction in either the Univac or Larc mode.

(2) Read-Start Controls. The read-start controls control the clearing of the even input buffer register prior to the start of reading or after a hash pulse has been detected. They also control the start and interruption of reading.

(3) Read Input Circuits. The read input circuits receive, amplify, and synchronize the Univac characters read from tape and generate tape-read-cycle signals which control the processing of each character through the translator and into the input buffer register.

(4) Input Buffer Write-Driver Controls. The input buffer write-driver controls control the magnetic-amplifier drivers that write data into the tape synchronizer input buffer registers in the dispatcher.

(5) Hash-Pulse Controls. The hash-pulse controls detect extraneous hash pulses, picked up at the beginning of a tape or in an SBB, and clear the synchronizer to prevent the extraneous pulses from affecting the reading of legitimate data.

(6) Univac Blockette Counter. This unit counts the ten-word "blockettes" in each data block when a Univac I tape is being read and modifies the operation of the read circuits to enable them to properly control the reading of the Univac blocks.

(7) Read Bad-Spot Controls. The read bad-spot controls interrupt reading while sections of tape unsuitable for recording purposes pass the read-write head.

(8) Read-SBB and Ending Controls. The read-SBB and ending controls detect spaces between blocks and initiate either an SBB or read-ending sequence. They also check for bad count and tape-runaway error conditions and initiate a read-ending sequence if such conditions are detected.

These subdivisions are discussed in the following paragraphs and illustrated by the read circuits simplified logic diagram in figure 6-5. Although they are not considered part of the read circuits, the input buffer registers and the Univac-to-Larc translator and input checker are included in figure 6-5 to achieve continuity in tracing a read operation through the diagram. Because the read circuits operate as a unit with either the read-write control circuits or the tape positioning checker, frequent reference will be required to the diagrams for the read-write control circuits in figures 4-3 and 4-4 and the diagram of the tape positioning checker in figure 7-1.

6-2. READ MODE CONTROLS

The read mode controls (figure 6-5) consist of the gain, Univac-read, read direction (forward and backward) and check-read flip-flops. As pointed out under heading 3-2, these flip-flops are set at the beginning of an operation by a 66 instruction, depending upon the modes specified by the program. In general, their function is to adjust or modify the operating characteristics of the read circuits in accordance with the specified modes by alerting or inhibiting the proper combination of gates. When a read operation is completed the flip-flops are reset by signals (S7RE1, S7RE2, and S7RE3) from the read-ending controls.

6-3. GAIN FLIP-FLOPS

Gain flip-flops 1 and 2 generate bias voltages through GN-type gain networks which control the gain of the tape read amplifiers. If both gain flip-flops are set (G = 1), the amplifiers are adjusted for high gain. If flip-flop 2 is set and flip-flop 1 reset (G = 0), the amplifiers provide normal gain. If flip-flop 1 is set and flip-flop 2 reset (G = 2), the amplifiers provide low gain. The reasons for changing the gain of the read amplifiers are discussed under heading 6-8.

6-4. UNIVAC-READ FLIP-FLOP

The Univac-read flip-flop functions to differentiate between (1) a tape prepared by the Univac I computer or Univac auxiliary devices in which data blocks are 60 words (720 characters) long with bad spots located anywhere between the first and last words of a block, and (2) tapes prepared by the Larc or Univac II computers in which the data blocks are multiples of ten words in length with bad spots located only between the first and last word of a ten-word group.

The essential function of the Univac-read flip-flop is to alert the clearing and stepping gates of a six-count-capacity, ten-word-group counter which, in turn, modifies the operation of the bad-spot, SBB, and read-ending controls in order to compensate for the difference in bad-spot locations on Univac I tapes.

6-5. READ DIRECTION FLIP-FLOPS

In addition to providing control for the read circuits, the read-forward and read-backward flip-flops provide tape direction indications to (1) the address modifier in the dispatcher to indicate whether a 1 shall be subtracted or added to the memory address each time a word is transferred to the memory, and (2) to the tape motion controls in the Uniservo control circuits to determine if the Uniservo tape unit is prepared to begin moving tape in the specified direction. Because either one or the other of the two read direction flip-flops is set during a read operation, they are used to generate signals that signify whether the read circuits are available (S7AVB) or in use (S7RBG).

6-6. CHECK-READ FLIP-FLOP

The essential function of the check-read flip-flop is to inhibit the input buffer write-driver controls, thereby preventing the data that is read from tape from being written into an input buffer register and sent to storage. Other than this, and the fact that the word counter (figure 4-2) is stepped by the word-end signal during a check-read, there is little difference between a read-to-memory and a check-read operation.

If, during a read-to-memory operation, the continue flip-flop in the read-write control circuits is not set by a 70 or 71 instruction while a ten-word group is being read, the check-read flip-flop is set (by S7ZEN) after the last word in the ten-word group has been read. Consequently, the remaining data, if any, in the block is check read only. S7ZEN also sets the continue-check flip-flop which, when set, will generate a continue-check error signal if a 70 or 71 instruction is executed while the remainder of the block is being check read. Whether or not a 70 or 71 instruction is executed, the operation terminates when the data block is completed.

6-7. READ-START CONTROLS

The read-start controls (figure 6-5) consist of the input-buffer-clear, read-ready, and inhibit-read flip-flops.

The input-buffer-clear flip-flop is set at the beginning of a read operation by S7RPR from the Uniservo control circuits and when a hash pulse is detected by S7HPD from the hash-pulse controls. When set, it alerts a gate in the buffer register controls of the dispatcher which clears the even input buffer register. To prevent a tape synchronizer and an instruction from clearing two or more input buffer registers simultaneously, the instructions (53, 55, and 68) that clear the input buffer registers generate FS814 which temporarily inhibits the clear gate, in the dispatcher, that is alerted by the input-buffer-clear flip-flop. Normally, the input-buffer-clear flip-flop is reset after 2 μsec at T4; however, FS815 delays its

resetting for an additional 4 μsec. Consequently, the even input buffer register is cleared by S7HC immediately after the instruction that generates the function signal has been executed. To prevent two or more input buffer registers from being simultaneously cleared by different tape synchronizers, the input-buffer-clear flip-flop in one tape synchronizer inhibits clearing by the corresponding flip-flops in any lower priority tape synchronizers. For example, S7HC from the input-buffer-clear flip-flop in Synchronizer 7 inhibits the clearing gates in the dispatcher for the even input buffer registers of Synchronizers 8, 9, and 10. (Synchronizer 7 has first priority, followed in order by 8, 9, and 10.) During a check-read operation it is not necessary to clear the input buffer register; consequently, the input-buffer-clear flip-flop is reset by the read-check flip-flop immediately after it is set.

When the input-buffer-clear flip-flop is reset it alerts the gate which sets the read-ready flip-flop. The same gate is also alerted by S7RCDC and S7RCDV from the Uniservo control circuits which indicate that tape motion has begun. The read-ready flip-flop is not set until the read-write start flip-flop in the read-write control circuits is set by a 68 or 65 instruction. When the read-write start flip-flop is set, S7TRSE is generated which clears the read input circuits and, in turn, generates S7RRS if the read-ready flip-flop is not already set. S7RRS sets the read-ready flip-flop and resets the read-write start and read-SBB flip-flops. When the read-ready flip-flop is set the read-operate signal (S7ROP) is generated. This is a key signal which begins the actual read operation. When a bad spot is detected during a read operation, reading is temporarily interrupted by the inhibit-read flip-flop. This flip-flop is initially reset by the tape-start signal S7RSTU from the Uniservo control circuits. When a bad spot is detected the flip-flop is set by S7BSR (from the read bad-spot controls) and inhibits S7ROP. The flip-flop is reset by S7SRN after the bad spot has passed the read-write head.

6-8. READ INPUT CIRCUITS

The return-to-zero recording method is used in the Larc Uniservo tape unit. With this method, the read-write head writes a binary 0, or erase polarity, on a tape in the absence of a binary 1. To record a 1 bit, a reverse current pulse is applied to the head coil. It reverses the direction of polarization of the magnetic tape and then returns it to zero polarity before the time for recording the next bit.

A recorded channel on tape can be visualized as a line of bar magnets oriented in the direction of tape motion, with the normal north-south direction of magnetization interrupted by a south-north magnetized region for each 1 bit written along the channel. When the tape is read a maximum voltage is induced in the head coil of the channel as a north-north or south-south boundary passes the head, and essentially no voltage is induced between boundary regions on the tape. A binary 1 is therefore read out as a series of two pulses of opposite polarity. (See figure 6-1.)

The low-voltage signals from the read-write head are amplified from 600 to 3200 times by variable gain amplifiers in the synchronizer. (See figure 6-5.) The gain is controlled through type-GN gain-control networks by the plastic-tape signal (U7PT) from the Uniservo tape unit and by signals from the gain mode flip-flops. When the PLASTIC-METAL switch on the

Uniservo tape panel is in the PLASTIC position, the plastic-tape signal increases the gain of the read amplifiers to accommodate low-amplitude signals received from the plastic tape during a high-density read operation. In addition, the gain can be set low, normal, or high for both metal and plastic tape, depending on the state of S7H and S7N from the gain mode flip-flops. Recorded data that cannot be read at one gain setting can often be salvaged by reading at a different setting. At normal gain setting, the read amplifier safely passes all normal signals and blocks out noise pulses of average amplitude. At low gain, normal signals are passed but above-average noise pulses are blocked. The high gain setting enables the amplifiers to pass low-level signals but still discriminate against average noise pulses.

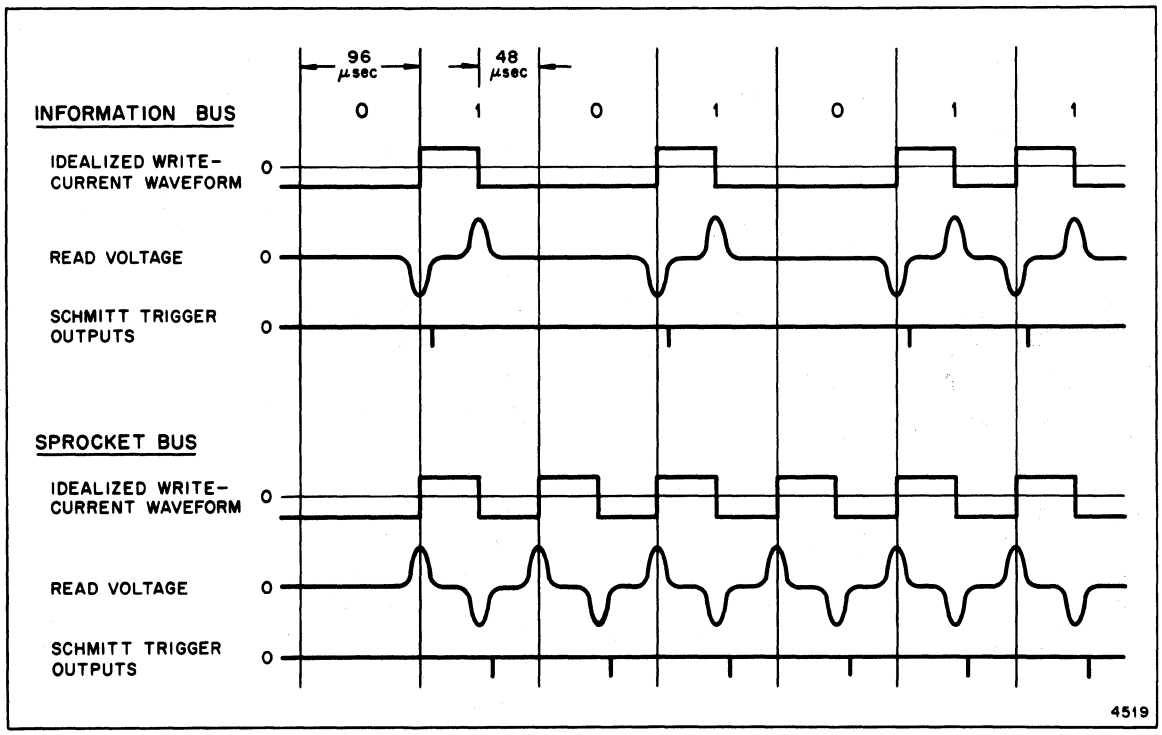


Figure 6-1. Read and Write Waveforms at 104 PPI

The sine-wave output of the read amplifier is converted into an 0.8-μsec negative pulse by an STE-type Schmitt trigger circuit. The Schmitt trigger detects a positive-going, near-zero (about -0.2 V) crossing of the input signal waveform for a binary 1. A binary 1 is represented on the sprocket channel by a high-voltage pulse followed by a low-voltage pulse. The inverse is true for the information channels; that is, a binary 1 is represented by a low-voltage pulse, followed by a high-voltage pulse. Since the Schmitt trigger, which is identical for information and sprocket channels, detects positive-going, slightly below zero crossing of the waveform, the 1 bits on the information channels are detected first, followed by detection of the sprocket bit. (See figure 6-1.) When a binary 1 is detected in an information channel, the low output of the Schmitt trigger is inverted and sets an asynchronous-type flip-flop. When the sprocket pulse arrives later, the low output of the sprocket-channel Schmitt trigger is synchronized by a single pulser to set a pulseformer-type sprocket flip-flop.

The time between detection of the information pulses of a character and detection of the associated sprocket pulse differs depending upon the pulse density of the tape being read. The time difference ranges from a nominal 20 μsec for a tape with a density of 250 PPI to 250 μsec for a tape with a density of 20 PPI. The time between the detection of the last information pulse of a character and the detection of the sprocket pulse may be less than the nominal value because of skewing of the eight parallel bits of a character on tape relative to the read-write head channels. If the eight bits of a character do not arrive at the read-write head channels simultaneously due to misalignment of the tape, the read-write head, or the data recorded on tape, the individual bits of the character are read at different times. If the skewing is bad enough, it is possible for the bits of one character to be identified as belonging with the bits of a character immediately preceding or following.

To avoid the possibility of the bits of one character being confused with those of another, the 1 bits of a character stored in the tape-input flip-flops are gated into seven skew flip-flops, and simultaneously, the sprocket skew flip-flop is set; all this occurs as soon as possible after the sprocket pulse is detected and stored in the sprocket flip-flop. First, however, S7SS from the sprocket flip-flop tests the skew flip-flops to determine if they are all reset, which would indicate that the preceding character read from tape had been vacated and transferred to the Univac-to-Larc translator. If all the skew flip-flops are found to be reset when tested by S7SS, signal S7GTB is generated. S7GTB sets the sprocket skew flip-flop and transfers the seven information bits from the tape-input flip-flops into the skew flip-flops. During the same pulse time, S7GTB generates S7GTBD which simultaneously clears the sprocket flip-flop, the skew flip-flops, and the sprocket skew flip-flop. The clearing of the skew and sprocket skew flip-flops at this time is not significant since they are already cleared and the signals which set them override the resetting signal. However, S7GTBD is generated by a number of other signals which must clear the input circuits. S7GTBD passes through a type-DB delay circuit and clears the tape-input flip-flops. The clearing of the tape-input flip-flops is delayed because they are of the asynchronous type. The delay avoids the possibility of resetting the flip-flops before the character stored in them has been gated into the skew flip-flops.

Once the sprocket skew flip-flop is set, it alerts the tape-read-cycle flip-flop. This flip-flop is timed to set only at increments of 8 μsec, with each setting dependent upon the arrival of the sprocket pulse. The flip-flop remains set for a 2-μsec period (T2 through T5) during which it transfers the character in the skew flip-flops to the Univac-to-Larc translator and controls the translation of the character, the stepping of the digit counter, and the writing of the character into an input buffer register. To ensure proper time-sharing of the translator, the tape-read-cycle flip-flop in only one of the synchronizers is set at any one time. This fact is illustrated in figure 6-2 which shows the timing of four consecutive read cycles, each in a different synchronizer. Although S7TRC gates the output of the skew flip-flops into the translator during the entire 2 μsec tape-read cycle, the flip-flops are cleared during the first pulse time (T2) of the cycle by S7TRC gated with T2,6. Consequently, the S7T1 through S7T7 inputs to the translator only have significance at T2.

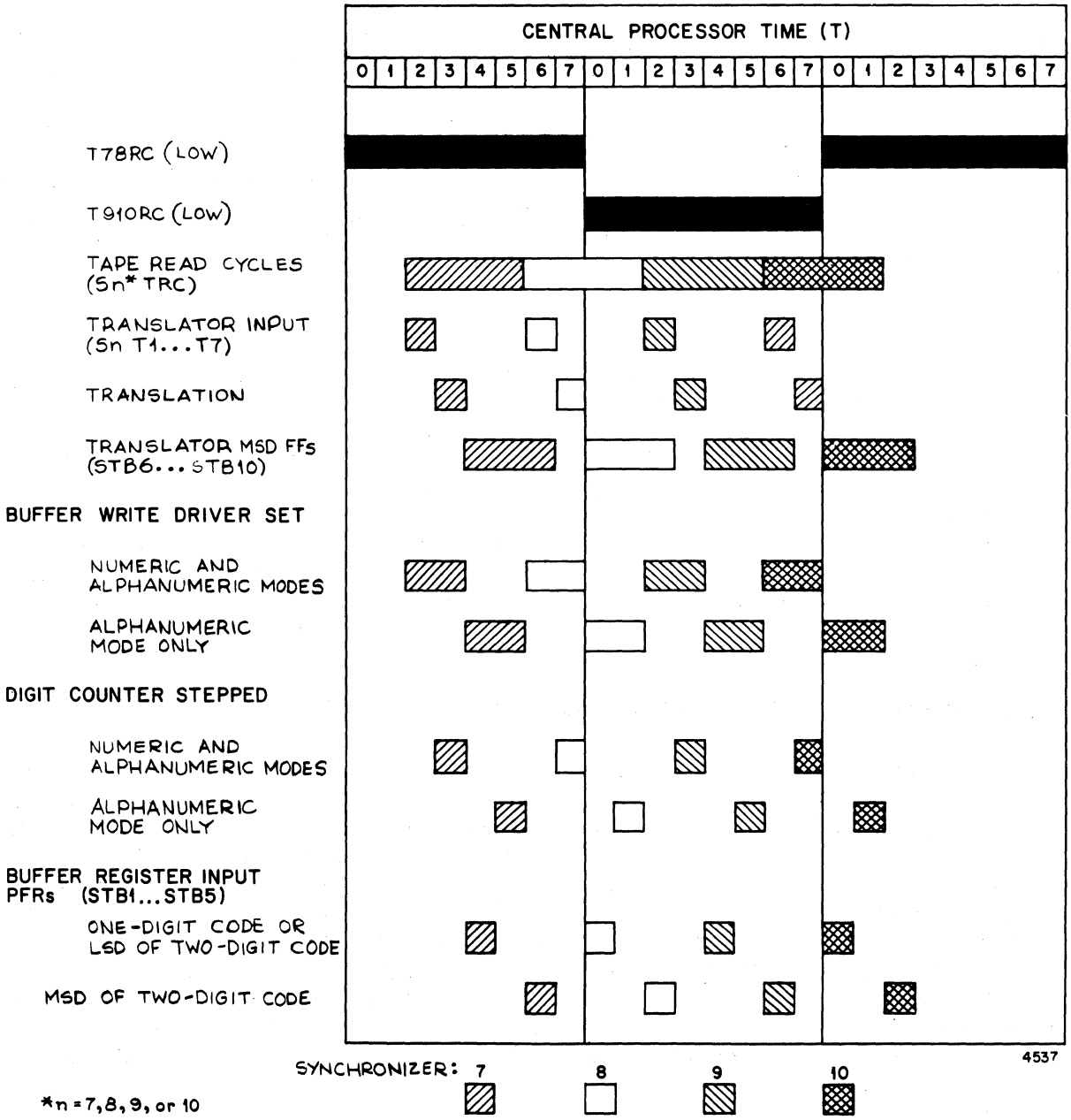


Figure 6-2. Input Timing for Four Consecutive Read Cycles on Different Synchronizers

In the event a new sprocket pulse is detected by the synchronizer before the preceding sprocket pulse has gated its associated character into the skew flip-flops, overskew error signals are generated which set the overskew (error) diagnostic flip-flop and the tape synchronizer or tape positioning checker error flip-flop (figure 7-1). This condition is detected by gating the output of the sprocket single pulser with the output of the sprocket flip-flop. To avoid possible erroneous generation of an overskew error during a hash-pulse period, the gate is inhibited by S7HPG from the hash-pulse-gating flip-flop.

The read input circuits are cleared by several signals other than S7GTB. These signals, which clear any extraneous pulses from the circuits, are the following:

(1) ES7C1 from the tape synchronizer CLEAR switch on the engineer's console.

(2) S7HP which is generated when a hash pulse has been detected.

(3) S7SR1D which is generated 5 milliseconds after an SBB has been detected.

(4) S7TRSE which is generated when the read-ready flip-flop is set at the beginning of the read operation.

To avoid possible detection of extraneous hash pulses on the read bus while the synchronizer is not reading, or when reading is interrupted to allow a bad spot to pass the read-write head, a blocking signal is generated by S7VR from the inhibit-read flip-flop. This signal blocks all eight of the STE-type Schmitt trigger circuits, thereby preventing the input flip-flops from being set. The same blocking signal is generated by S7HPD to block the Schmitt triggers while a hash pulse is being deleted.

6-9. INPUT BUFFER WRITE-DRIVER CONTROLS

The input buffer write-driver controls (figure 6-5), generate signals that energize magnetic-amplifier drivers that write the translated digits into the two input buffer registers of the tape synchronizer. Each register has 12 write drivers, each of which drives the five cores of a digit location. The roles of the registers are controlled by the word-driver flip-flop (in the read-write control circuits) which at any one time alerts the write-driver controls of only one of the registers. When the word driver is set (resulting in S7WD), only the write-driver signals S7WV1 through S7WV12 can be generated; when it is reset (resulting in S7WV), only the signals S7WD1 through S7WD12 can be generated. The controls of both registers are inhibited during a check-read operation and while the tape positioning checker is connected.

The 12 write gates of each register are alerted by the 12 outputs (S7DC1 through S7DC12) of the digit counter. Consequently, the order in which digits are written into a register during a tape-read operation is controlled by the way in which the digit counter is stepped. During a tape-read cycle (SnTRC, figure 6-2) the write gates are sampled at T2,3 (for Synchronizers 7 and 9) or T6,7 (for Synchronizers 8 and 10) to energize the one digit driver corresponding to the digit count. If an alphanumeric operation is being performed the write gates are sampled again at T4,5 (for Synchronizers 7 and 9) or T0,1 (for Synchronizers 8 and 10) of the same tape-read cycle. Between the time that one driver and another is energized the digit counter is stepped so that a different driver is energized each time. The two digits of an alphanumeric pair are actually written into the register at T4 and T6 (for Synchronizers 7 and 9) or T0 and T2 (for Synchronizers 8 and 10). For a backward-read operation, the digit counter is stepped to write the digits of a word into a register in a straight sequence beginning with the LSD. For a forward-numeric-read operation, the digit

counter is stepped to write the digits of a word into a register in a straight sequence beginning with the MSD. However, during a forward-alphanumeric-read operation the LSD of a digit pair is received first from the translator and the digit counter is stepped to write digits into the register in the following sequence:

11,12 9,10 7,8 5,6 3,4 1,2

6-10. HASH-PULSE CONTROLS

When the tape leader or an SBB passes the read-write head during a read operation, it is possible for extraneous pulses, not representing legitimate recorded information, to be picked up on the read bus. These pulses are referred to as hash pulses. Hash pulses may result from such things as noise induced in the read bus cabling, unerased data on tape, or a pulse pattern of all 1's recorded on tape when the write bus is disconnected at the end of a write operation. These hash pulses may be picked up by the tape synchronizer read amplifiers and stored in the tape-input flip-flops. If a hash pulse is picked up on the sprocket channel, a tape-read cycle could result which would step the digit counter and pass the hash-pulse pattern through the translator and into the even input buffer register. The function of the hash-pulse controls (figure 6-5) is to detect hash pulses and clear them from the tape synchronizer and from the tape positioning checker, if it is connected, so that they do not interfere with the reading and processing of legitimate information.

The synchronizer may monitor the read bus while an SBB or the tape leader is passing the read-write head since any hash pulses detected during this time are automatically cleared from the synchronizer by the hash-pulse controls. Although a 1.0-second delay may be programmed between a start-tape instruction (67) and a start-read instruction (68) when a read operation is starting with the tape in the rewound state, such a delay is not absolutely necessary as evidenced by the fact that it is not included in an initial-read operation.

6-11. HASH-PULSE PERIOD

The hash-pulse period (HPP) is the time period during which the synchronizer discriminates against hash pulses. It is defined by the set state of the hash-pulse-gating flip-flop. This flip-flop is set by S7RSTV when tape motion begins for a read operation, and by S7C10 when an SBB is detected. When the tape positioning checker is not connected, the flip-flop is reset by the first word-end signal (S7WEND) following either the SBB or the start of the read operation. Therefore, the flip-flop is reset after the first 12 characters of a data block are read during a numeric-read or check-read operation and after the first six characters of a block are read during an alphanumeric operation. If the tape positioning checker is connected, the hash-pulse-gating flip-flop is reset when a digit counter in the tape positioning checker steps from 11 to 12, indicating that the first 12 characters in a block have been read.

During the HPP any pulses detected on the read bus are suspect; they may or may not turn out to be hash pulses. Therefore, any input odd-even or untranslatable error signals generated during this period are inhibited from setting a diagnostic-error flip-flop and the tape read-write or positioning checker error flip-flops. These error signals are instead stored in HPP error flip-flops until it is determined if the errors were generated by hash pulses or legitimate information pulses. If it is later determined that the error signals were generated by hash pulses, then the HPP error flip-flops are cleared. If, on the other hand it is determined that the error signals were generated by legitimate information, then the signals are used to set the tape read-write or positioning checker error flip-flops and the appropriate error-diagnostic flip-flop. Also during the HPP, the overskew check gate in the read input circuits is inhibited in the event an overskew error is generated by a hash pulse in the sprocket channel.

6-12. HASH-PULSE DETECTION

Hash pulses are detected by a 1.2-millisecond RDF that samples signals from the sprocket channel and each of the information channels. If a 1 bit is detected in any one of these channels the RDF is triggered. If the RDF is triggered by an information pulse, it should not recover during the HPP because each information pulse should be followed by another in time to re-trigger the RDF before it recovers. For example, when a low-density tape of 20 PPI is read, the information pulses arrive at nominal 0.5-millisecond intervals. Furthermore, the sprocket pulses lag the information pulses and, if all eight channels are considered, the RDF should be triggered at nominal 0.25-millisecond intervals. If the 1.2-millisecond RDF is triggered by a pulse and then recovers during an HPP of a read operation, it is assummed that a hash pulse was picked up. When the RDF recovers, a pulse is generated which generates a hash-pulse-delete signal provided that the hash-pulse-gating flip-flop is set and the read-operate signal is present. This method of detecting hash pulses is based on two assumptions: first, it assumes that a hash pulse is separated from an information pulse by more than 1.2 milliseconds (if the hash pulse were not separated thus, the RDF would be retriggered by an information pulse before it recovered from a trigger by the hash pulse); second, it assumes that not more than five hash pulses occur in the sprocket channel in succession during an alphanumeric-read operation and not more than 11 in succession during a numeric-read or check-read operation. If more than that number occurred in succession, the RDF would not recover until after the hash-pulse-gating flip-flop was reset as a result of the hash pulses triggering tape-read cycles.

6-13. HASH-PULSE DELETION

When a hash pulse is detected, the hash-pulse-delete signal (S7HP or S7HPD) resets the HPP error flip-flops, clears the read input circuits, and sets the input-buffer-clear flip-flop to clear the even input buffer register. Thus, the effect of any hash pulses or errors generated by hash pulses is removed from the read circuits. When the read-write control circuits are

used to control a read or check-read operation, the hash-pulse-delete signal generates S7RS to clear the digit counter in the event it was stepped as a result of a hash pulse that triggered a tape-read cycle. Although the word counter is also cleared, it should not have been stepped during the HPP. When the tape positioning checker is connected, the hash-pulse-delete signal clears the 120 counter in the positioning checker.

At the end of an HPP, any input odd-even or untranslatable errors resulting from hash pulses should be cleared from the HPP error flip-flops. Therefore, if an error signal is stored in the HPP error flip-flops at the end of the period, it is assumed that it represents a legitimate error and the tape read-write or positioning checker error flip-flop and the appropriate error-diagnostic flip-flop are set.

6-14. UNIVAC BLOCKETTE COUNTER

The Univac blockette counter (figure 6-5) is included in the read circuits solely for the purpose of reading Univac I tapes. Such tapes differ from those prepared by the Larc computing system in the following respects:

(1) Each data block on a Univac I tape is always 60 words (720 characters) long. On a Larc tape the blocks may be any multiple of ten words in length.

(2) Bad-spot areas may be located anywhere between the first and last word of a 60-word block on a Univac I tape. On a Larc tape they are located only between the first and last word of a ten-word group.

(3) A block on a Univac I tape may be subdivided into six ten-word "blockettes" with spaces between the blockettes. The data in each block on a Larc tape is continuous.

Because of these differences, a Univac tape must be read with the read circuits operating in a special mode controlled by the "blockette counter". The blockette counter is stepped only when the Univac-mode flip-flop is set. The counter counts the six blockettes (ten-word groups) of each block on a Univac tape and generates a signal (S7BL6) which is high while the first five blockettes are being read and low while the sixth blockette is being read. This signal, which is the only output of the counter, has the following two main functions:

(1) It prevents the read-SBB and ending controls from detecting an SBB except after reading of the last blockette has begun. It thus suppresses detection of any spaces between blockettes.

(2) It enables the read bad-spot controls to detect bad spots between the first word and last word of the 60-word block rather than between the first and last word of each ten-word blockette.

The blockette counter (figure 6-3) consists of three flip-flops, outputs of which are gated with a stepping signal to step the count. To simplify the diagram in figure 6-3, the outputs of the three flip-flops are labeled B1, B2, and B3, although they are not so labeled on the detailed engineering drawing. The count is in terms of the three-bit code shown in the table included in figure 6-3. When the count is six, S7BL6 is generated; for all other counts it is not. When a 66 instruction is executed, the counter is set to the six count by setting all three flip-flops. If the Univac-read flip-flop is not set, the counter remains in this state throughout the operation. However, if the Univac-read flip-flop is set, the counter is subsequently cleared to zero by the 68 instruction and is then stepped in ascending order as the first character of each blockette is read. Therefore, the counter will read 1 while the first blockette is read, 2 while the second is read, and so on. On the sixth step, the S7BL6 output of the counter changes state and alerts a gate in the bad-spot controls that detects the end of a bad-spot alert period, and gates in the SBB and ending controls that detect an SBB. If reading continues into the next block, the 0 count is bypassed and the counter will step from 6 to 1 as the first character of a new block is read, and then in ascending order as each new blockette is reached.

It may be noted that the blockette counter is not designed to operate in conjunction with the tape positioning checker. Because of this, the positioning checker cannot be used to control check-reading of a Univac tape.

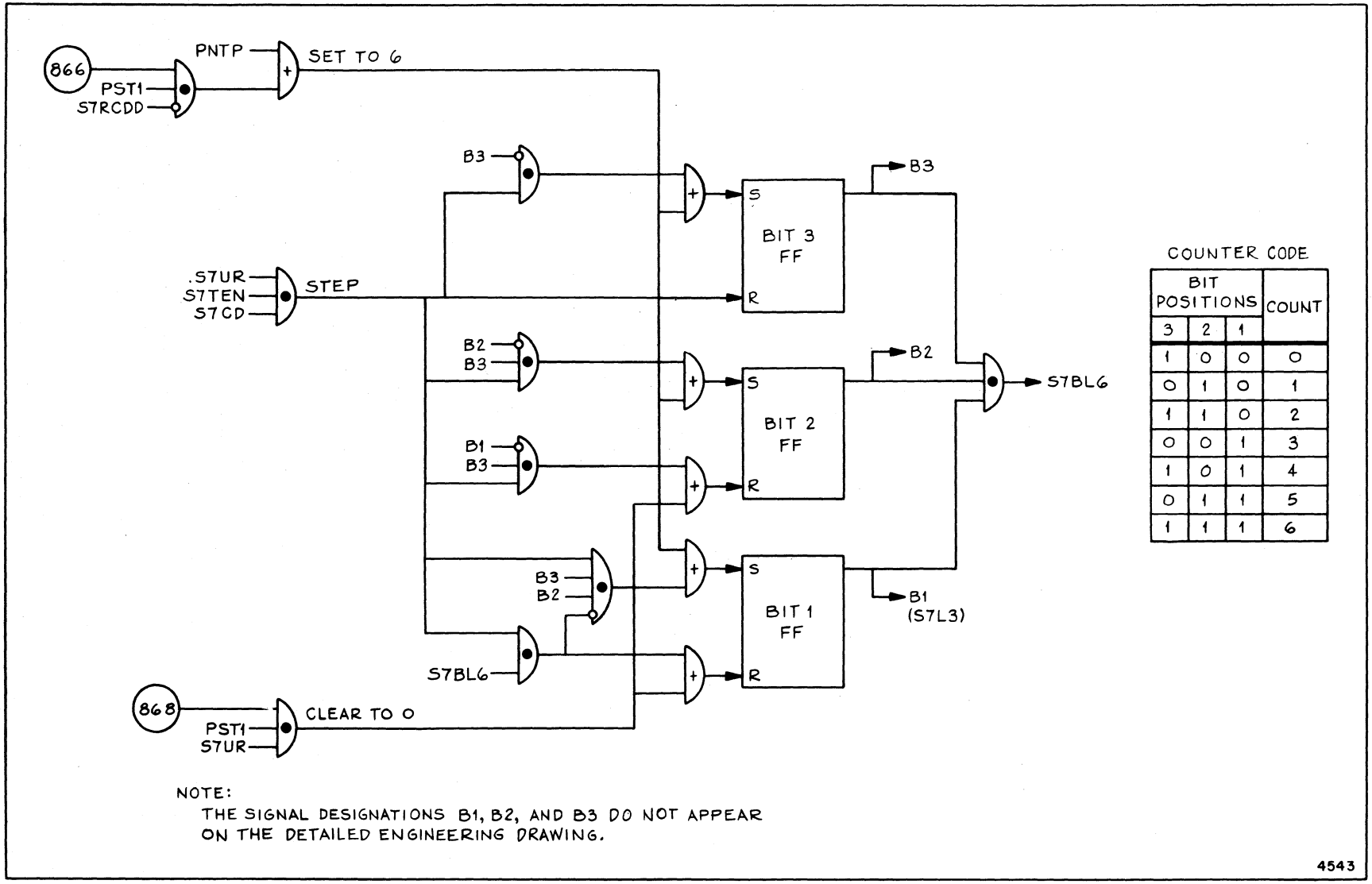
6-15. READ BAD-SPOT CONTROLS

Sections of tape possessing poor magnetic properties or spliced sections are designated bad spots. These bad spots are identified by at least two holes punched through the tape. (See figure 6-4.) The spacing between holes is about 2-1/2 inches. The first hole of a series of holes precedes the actual bad spot and the last hole follows it. Thus, the bad area is marked for both forward and backward tape movement.

Photocells mounted on the tape panel of the Uniservo tape unit detect the bad-spot holes when the tape is in motion. If a hole is detected, an S7RPA signal is generated to alert the synchronizer to the approach of a bad tape area. During a forward read operation, the S7RPA signal is generated by two forward photocells connected in parallel. One forward photocell is located 5 inches from the read-write head and the other 4-1/4 inches from the head. During a backward read operation, the S7RPA signal is generated by a backward photocell located 2-1/2 inches from the read-write head on the opposite side from the forward photocells.

The write bad-spot controls (heading 5-14) operate in such a way that recording is interrupted for bad-spot areas only between the first and last word of a ten-word group. A bad-spot area on a Univac-prepared tape, however, may occur anywhere between the first and last word of a 60-word block. Moreover, the blocks on a Univac tape may be subdivided into 10-word blockettes and a bad-spot area may be located in the space between blockettes.

To distinguish a bad-spot area from an SBB, the read bad-spot controls (figure 6-5) are alerted to detect a bad-spot area only from the end of the first word to the beginning of the last word of each ten-word group on a



COUNTER CODE

BIT POSITIONS			COUNT
3	2	1	
1	0	0	0
0	1	0	1
1	1	0	2
0	0	1	3
1	0	1	4
0	1	1	5
1	1	1	6

Figure 6-3. Univac Blockette Counter (D 807 888)

Larc tape or between the first and last word of each 60-word block on a Univac tape. This alert period is defined by the read bad-spot-gating flip-flop which is set at the end of the first word of each ten-word group and reset by S7TRC if the end-of-bad-spot-alert flip-flop is set. The latter flip-flop is set at the end of the ninth word of each ten-word group when a Larc tape is being read, and at the end of the 59th word of a data block when a Univac tape is being read.

A break in the data recorded on tape may be either an SBB, a bad-spot area or, in the case of a Univac tape, a space between blockettes. Such a break is detected by a 1.5-millisecond RDF which samples the sprocket signal from the read bus. While data is read without interruption the RDF will not recover since the sprocket pulses at the lowest reading density (20 PPI) are nominally 0.5 millisecond apart. However, when a break occurs in the recorded data, the RDF will recover 1.5 milliseconds after the last sprocket is received and signal S7SPR will be generated indicating that a bad-spot area, an SBB, or a space between blockettes has been reached. The delay is long enough to ensure that the S7SPR signal will not be generated as a result of a single sprocket pulse being skipped or missed. During a hash-pulse period the signal is inhibited to prevent it from being erroneously generated after the RDF is triggered by a hash sprocket pulse.

If an S7SPR signal is generated while the read bad-spot flip-flop is set, it sets the last-sprocket flip-flop. If a Larc tape were being read this would indicate that a bad-spot area has reached the read-write head. If a Univac tape were being read it would indicate that either a bad-spot area or a space between blockettes, or a combination of both, has been reached. In either case, reading is not interrupted until after a read photocell signal is received from the Uniservo tape unit. The timing of the interruption depends upon the direction of the read operation.

6-16. FORWARD READ

During a forward-read operation the first hole is detected by the forward photocell furthest from the read-write head. (See figure 6-4.) The S7RPA signal thus generated will set a 16-millisecond and a 55-millisecond RDF. With the tape moving at the normal 100 inches per second, the same hole will be detected by the second photocell, about 7.5 milliseconds later, and retrigger the 16-millisecond RDF before it recovers. Therefore, about 23.5 milliseconds (16 + 7.5) after the first hole is detected, the 16-millisecond RDF will recover and the read bad-spot flip-flop will be set. When this flip-flop is set, S7BSR is generated and interrupts all reading by setting the inhibit-read flip-flop. The interruption of reading is delayed for 23.5 milliseconds to ensure that an actual bad-spot area has been detected by the last-sprocket flip-flop and not a space between blockettes preceding the bad spot area. At 100 inches per second the tape travels about 2-1/3 inches during the 23.5-millisecond delay before reading stops. Thus, the last of the recorded data should be safely past the read-write head.

Every hole after the first hole in a series will retrigger the 55-millisecond RDF before it recovers. Fifty-five milliseconds after the last hole in the series has passed the forward photocell nearest the read-write head, the 55-millisecond RDF will recover and reset the read bad-spot flip-flop. When this flip-flop is reset, S7SRN will be generated to reset the

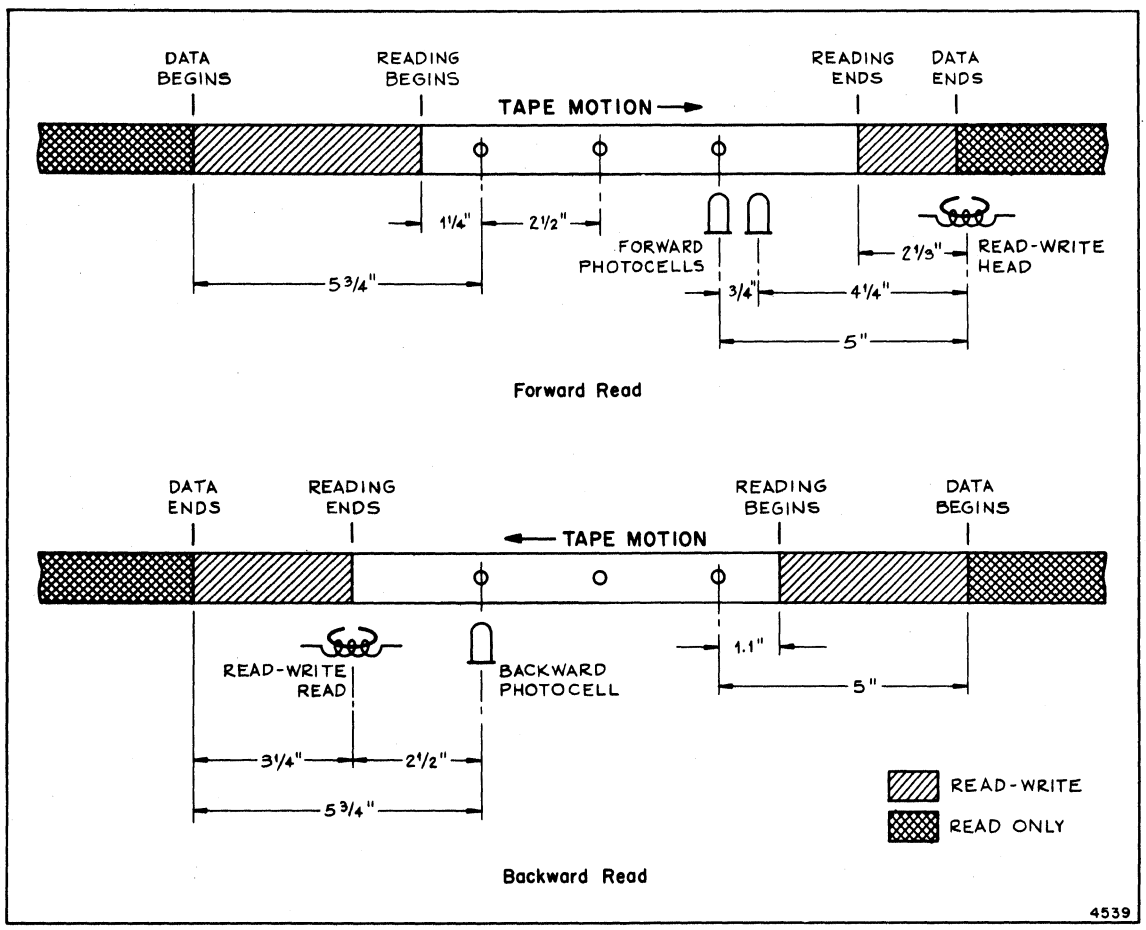


Figure 6-4. Tape Bad Spots

inhibit-read flip-flop and allow reading to resume. Since 55 milliseconds of tape motion corresponds to 5-1/2 inches of tape length and since the nearest photocell is 4-1/4 inches from the read-write head, reading will resume when the last hole is about 1-1/4 inches past the head. When bad spots are detected during a write operation recording resumes when the last hole is about 5-3/4 inches past the read-write head. Thus, reading will resume long before the recorded data reaches the read-write head.

6-17. BACKWARD READ

When the first hole of a series is detected by the backward photocell (figure 6-4) during a backward read operation, a 36-millisecond RDF is triggered as well as the 16-millisecond RDF which is used in the forward read operation. Although the 16-millisecond RDF is triggered, it will not be effective because the photocell signal bypasses the RDF and sets the read bad-spot flip-flop to stop reading immediately. The interruption of reading need not be delayed during a backward read operation because the last of the recorded data will be about 3-1/4 inches past the read-write head when the first hole is detected.

Each succeeding hole in the series of holes will retrigger the 36-millisecond RDF. When the RDF finally recovers, 36 milliseconds after the last hole passes the backward photocell, the read bad-spot flip-flop is reset and reading resumes. Since 36 milliseconds of tape motion corresponds to 3.6 inches of tape length and because the backward photocell is 2-1/2 inches from the read-write head, reading will resume when the last hole is about 1.1 inches past the head. Because the beginning of the recorded data is 5 inches (or slightly less) from the last hole, it will not reach the read-write head until several milliseconds after reading resumes.

6-18. READ-SBB AND ENDING CONTROLS

When the continuous sequence of reading characters from tape is broken, the last-sprocket signal, S7SPR (figure 6-5) is generated 1.5 milliseconds after the character preceding the break has been read. If the break occurs after a multiple of 120 characters have been read from a Larc tape, or after 720 characters have been read from a Univac tape, then an SBB is detected by the read-SBB and ending controls. When an SBB is detected, reading either continues into the next block or the read operation is ended. Which alternative occurs depends upon the state of the continue-past-SBB flip-flop in the read-write control circuits or, when the tape positioning checker is connected, upon the state of the continue flip-flop in the positioning checker.

If a break in the flow of characters from tape occurs at a place other than at the end of a block and the break is not caused by a bad-spot area or a space between blockettes, then one of three error conditions are detected, all of which cause the read operation to end. The three error conditions are the following:

(1) Bad-Count Error. A bad-count error is detected if the break in the flow of data occurs when counters in the synchronizer or tape positioning checker indicate that the first or last word of a ten-word group on a Larc tape, or the first or last word of a 60-word block on a Univac tape, is being read. It therefore indicates that the number of digits in a block differs from the number actually read by 12 or less.

(2) Very-Bad-Count Error. A very-bad-count error is detected if the break in the flow of data occurs when the counters indicate that the read operation is somewhere between the first and last word of a ten-word group on a Larc tape or the first and last word of a 60-word block on Univac tape. It therefore indicates that the number of characters in a block differs from the number actually read by more than 12.

(3) Tape-Runaway Error. A tape-runaway error is detected when a break occurs in the flow of data and the tape travels 17-1/2 inches without any additional data being read.

There are several key signals that are sampled by the last-sprocket signal to detect an SBB or an error condition; they are the following:

(1) S7BL6 from the blockette counter which indicates that either a Larc tape is being read or the last blockette of a Univac block is

being read. This signal causes the detection of spaces between blockettes to be suppressed when a Univac tape is being read.

(2) S7G108, which indicates that the first or last word of a ten-word group on a Larc tape is being read or the first or last word of a 60-word block on Univac tape is being read. This signal comes from the last-word flip-flop which is set by the same signal that resets the read bad-spot-gating flip-flop and is reset by the same signals that set the bad-spot-gating flip-flop. However, when an SBB is detected the last-word flip-flop is reset by S7C10.

(3) S7D120 is produced by digit and word-count signals from the read-write control circuits after the last character of a ten-word group or blockette has been read.

(4) SC120 is produced by a digit counter in the tape positioning checker after the last character of a ten-word group has been read.

(5) S7BSGR is generated by the read bad-spot-gating flip-flop between the first and last words of a ten-word group on Larc tape or between the first and last words of a 60-word block on Univac tape.

6-19. SBB DETECTION

When the tape positioning checker is connected, an SBB is detected by using the last-sprocket signal to test the signals S7BL6, SG108, and S7D120. If the continue-past-SBB flip-flop is reset when an SBB is detected, a read-ending sequence is initiated. If the continue-past-SBB flip-flop is set, an SBB sequence is initiated and S7C10B is generated to set the ten-word flip-flop in the read-write control circuits. When the tape positioning checker is connected, an SBB is detected by testing signal SC120 with the last-sprocket signal. If SC120 is present a read-ending or SBB-sequence is initiated, depending upon the state of the continue flip-flop in the positioning checker.

6-20. READ-ENDING SEQUENCE

When a read-ending sequence is initiated, signal S7RE1 is generated. This signal resets the read-ready flip-flop and sets the inhibit-read flip-flop to end reading; it resets the read-centerdrive flip-flop in the Uniservo control circuits (figure 2-2) to stop tape motion; it resets the Univac-read flip-flop if it is set; it resets the numeric and alphanumeric mode flip-flops if the tape positioning checker is not connected and it triggers a 6-millisecond RDF which energizes a read-clear relay in the Uniservo power supply cabinet. The read-clear relay extinguishes the read thyratron in the Uniservo tape unit and thus disconnects the tape unit from the read bus. When the 6-millisecond RDF recovers, S7RE2 is generated which resets the gain flip-flops and triggers a 10-millisecond RDF. When this RDF recovers, S7RE3 is generated. This signal resets the read direction flip-flops (read-forward and read-backward), thereby making the read circuits available; it also initiates an SBB sequence. The 10-millisecond delay ensures that the Uniservo tape unit is disconnected before the read circuits and (if the tape positioning checker is not connected) the read-write control circuits are made available to the program.

6-21. SBB SEQUENCE

An SBB sequence is initiated at the end of a read operation (by S7RE3) or when an SBB is detected while the continue-past-SBB flip-flop is set. When the sequence is initiated at the end of a read operation and the tape positioning checker is not connected then signal S7RE will be generated to set the ten-word and read-write-circuits-available flip-flops in the read-write control circuits. This signal will be inhibited by the read-circuits-available signal (S7AVB) when reading past an SBB. However, at the end of a read operation, S7RE3 resets the read flip-flops thereby making the read circuits available. Consequently, S7RE will be generated if the positioning checker is not connected.

When an SBB sequence begins, the signals S7C10, S7C10C, and S7C10D are always generated. S7C10 resets the last-word flip-flop. It also sets the read-SBB flip-flop and triggers a 5-millisecond RDF to alert the program for 5 milliseconds that an SBB has been reached. S7C10C sets the hash-pulse-gating flip-flop to begin the hash-pulse period. S7C10D resets the continue-past-SBB flip-flop provided the tape positioning checker is not connected. When the 5-millisecond RDF recovers, S7R1D and S7R1B are generated. S7R1D clears the read input circuits and S7R1B disconnects the positioning checker if its continue flip-flop is not set.

6-22. BAD-COUNT ERROR

When the tape positioning checker is not connected, a bad-count error is detected by using the last-sprocket signal to test signals S7BL6, S7G108, and S7D120. If signals S7BL6 and S7G108 are present and S7D120 is not present, indicating that the last-sprocket pulse occurred while reading the last or first word but not after reading the last character of a block, then signal S7BCE is generated. This signal initiates a read-ending sequence and sets the read-write error flip-flop. When the positioning checker is connected, a bad-count error is similarly detected by testing S7G108 and SC120, using the last-sprocket signal. If S7G108 is present and SC120 is not then signal SCBCE1 is generated. This signal initiates a read-ending sequence and sets the tape-positioning-checker-error flip-flop.

6-23. VERY BAD COUNT AND RUNAWAY ERROR DETECTION

If a very bad count occurs, the last-sprocket signal will be generated while the read bad-spot-gating flip-flop is set; however, the same condition will exist if the last-sprocket signal resulted from a bad-spot area or a space between blockettes on Univac tape. Therefore, if a last-sprocket signal occurs while the read bad-spot-gating flip-flop is set, the very-bad-count-detection flip-flop will be set to record the fact that a possible very bad count has occurred, although the actual error will not be detected unless and until it is finally determined that the last-sprocket signal did not result from a bad-spot area or a space between blockettes. When the very-bad-count detection flip-flop is set a 75-millisecond RDF is triggered which tests the flip-flop when it recovers. If a bad-spot area or a space between blockettes is detected during the 75-millisecond delay time of the RDF, the flip-flop is reset. However, if the flip-flop is still set at the end of 75 milliseconds, it is assumed that a very bad count has occurred and the very-bad-count flip-flop is set.

When a Univac tape is being read, a space between blockettes is detected by testing S7D120 during a tape-read cycle. Since S7D120 should be present during a space between blockettes, the very-bad-count-detection flip-flop will be reset as the first character following a space between blockettes is read.

When a bad spot is detected the very-bad-count-detection flip-flop will be reset by S7RUMP which is generated by the read photocell signal from the Uniservo tape unit. In the event this signal is generated slightly before a last-sprocket signal during a forward read operation, the very-bad-count-detection flip-flop is also reset by S7RBSF from the read bad-spot flip-flop. In either case, the very-bad-count-detection flip-flop should be reset before the 75-millisecond RDF recovers if a bad spot is detected. The longest delay between the setting of the flip-flop by the last-sprocket signal and the arrival of a photocell signal to reset it would occur during a backward-read operation. However, considering all the tolerances involved in detecting bad spots, the flip-flop will be reset well before the 75-millisecond RDF recovers.

After a very bad count is detected, an error signal is not generated unless and until a last-sprocket signal arrives. If a last-sprocket signal is generated while the very-bad-count flip-flop is set, a very-bad-count error is generated and a read-ending sequence is initiated. This would indicate that additional data was read by the synchronizer following detection of a very bad count. However, if no additional data is read for a period of 100 milliseconds following detection of a very bad count, a tape-runaway error, rather than a very-bad-count error, results. Such a condition might result from a variety of causes; for example, when a very bad count is detected because of a permanent failure in the sprocket-detection circuits.

A tape-runaway error is detected by a tape-runaway-detection flip-flop which is set when a very bad count is detected and is reset by a tape-read cycle, if and when any data is read from tape. When the tape-runaway-detection flip-flop is set a 100-millisecond RDF is triggered which tests the flip-flop when it recovers. If the flip-flop is still set 100 milliseconds later, indicating that no sprocket signals were generated after the very-bad-count-detection flip-flop was set, a tape-runaway error is generated which sets the appropriate error flip-flops and initiates a read-ending sequence to stop the tape.

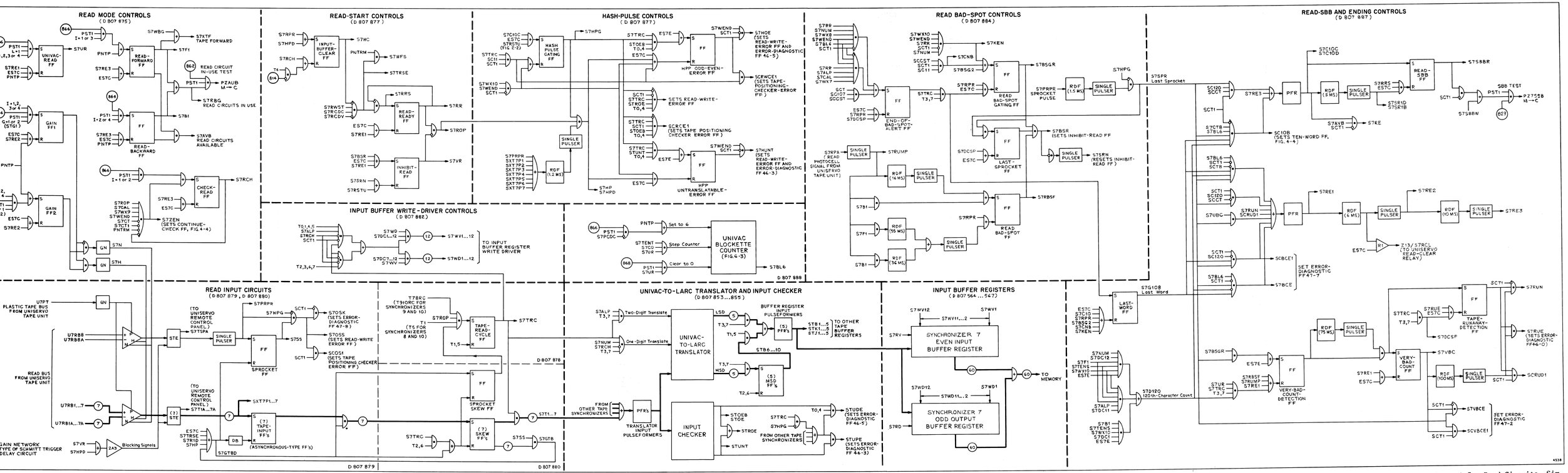


Figure 6-5. Read Circuits, Simplified Block Diagram

SECTION 7
TAPE POSITIONING CHECKER

7-1. GENERAL

The tape positioning checker (figure 7-1) may be connected to any one of the tape synchronizers to control a check-read operation. It cannot, however, be used to check-read a Univac I tape. When the tape positioning checker is connected to a synchronizer, the read circuits of the synchronizer are disconnected from the read-write control circuits (figure 4-4) and connected to the tape positioning checker. The read circuits and the tape positioning checker together perform the check-read operation. This does not in any way interfere with the read-write control and write circuits which may perform a write operation simultaneously with the check read.

Because the data read during a check-read operation is not sent to storage, the tape positioning checker need not contain circuits for controlling the buffer registers or the translation mode. Although the data read from tape is supplied to the Univac-to-Larc translator and input checker, the output of the translator is not written into an input buffer register. However, an odd-even check of the data is performed by the input checker associated with the translator.

The main functions of the tape positioning checker are the following:

(1) Disconnect the read circuits of a selected tape synchronizer from the read-write control circuits and connect them to the tape positioning checker.

(2) Count the characters read from tape.

(3) Communicate with the program on the status of an operation.

These three functions are performed by the connect flip-flops, the count controls, and the status controls, each of which will be discussed individually.

7-2. CONNECT FLIP-FLOPS

The tape positioning checker (figure 7-1) may contain as many as four connect flip-flops, one for each of the tape synchronizers in the system. The tape positioning checker is connected to a particular synchronizer by use of a 65 instruction to set the appropriate connect flip-flop. The 65 instruction also initiates reading in the synchronizer read circuits. When reading ends, the connect flip-flop that was set is reset by Sn*R1B from the read-ending circuits in the synchronizer provided a continue flip-flop in the tape positioning checker is not set.

7-3. COUNT CONTROLS

When the tape positioning checker is connected to a tape synchronizer, the 120 characters of each ten-word group read from tape are counted by a 120 counter. The 120 counter is a seven-stage binary counter that counts in straight binary code. The count, in binary code, is stored in seven flip-flops. Outputs of the seven flip-flops are decoded to generate digit-count signals that control bad-spot, SBB and read-ending controls in the read circuits of the connected synchronizer, and also alert the status controls in the tape positioning checker to the completion of a ten-word group.

At the beginning of a check-read operation, or whenever a hash pulse is detected by the connected synchronizer, the 120 counter is cleared to zero by resetting all seven flip-flops. The counter is stepped in ascending order during each tape-read cycle of the connected synchronizer. Each time the counter is stepped the lowest order count flip-flop changes state (from 1 to 0 or from 0 to 1); each of the other counter flip-flops changes state when the counter is stepped if all the lower order flip-flops contain a 1 bit. On the 120th step, when the counter reads 119 (1110111), all seven flip-flops in the counter are reset to zero so that the sequence can be repeated for the next ten-word group. Simultaneously with the 120th step, the stepping signal samples the 119-character-count signal (SC119) to set the ten-word-alert flip-flop in the status controls. The output (SC120) of this flip-flop then indicates that the last character of the ten-word group has been read. (SC120 is the equivalent of the zero count of the counter.) Apart from SC119 there are only two other character-count signals decoded by the counter; they are SC11 and SC107, which are gated with the stepping signal, SCCST, to define the beginning and end of the bad-spot alert period in the read bad-spot controls of the connected synchronizer.

7-4. STATUS CONTROLS

The status controls provide the means by which the processor program exercises control of a check-read operation performed with the aid of the tape positioning checker. They perform functions similar to those performed by the read-write status controls in the tape synchronizer. The program exercises control by the following means:

* n = 7, 8, 9, or 10.

(1) Performing a test (instruction 56) to determine if the tape positioning checker is in use, that is, connected to a synchronizer.

(2) Connecting the tape positioning checker to a particular synchronizer and alerting the synchronizer to begin reading (instruction 65).

(3) Monitoring the progress of the check-read operation by way of the master input-output priority, ten-word, and SBB tests (instructions 99, 69, and 73, respectively).

(4) Controlling the progress of the operation by issuing continue instructions (instruction 70 or 71) as required to complete the operation.

(5) Testing (instruction 48) to determine if an error has been detected during the operation.

The status controls consist essentially of four flip-flops as follows: a ten-word-alert flip-flop, a ten-word flip-flop, a continue flip-flop, and an error flip-flop. Each of these flip-flops is discussed individually.

7-5. TEN-WORD-ALERT FLIP-FLOP

The ten-word-alert flip-flop is set by FS865 at the beginning of the check-read operation and at the end of each ten-word group thereafter. When it is set, the flip-flop alerts the SBB-and-ending controls in the read circuits (figure 6-5) of the synchronizer. If a last-sprocket signal is detected while the ten-word-alert flip-flop is set either an SBB or read-ending sequence will be initiated depending upon the state of the continue flip-flop. If the check-read operation continues, the ten-word-alert flip-flop will be reset by SCCST as the first character of the new ten-word group is counted; simultaneously, SCCST will test the ten-word-alert flip-flop and, finding it still set, will reset the continue flip-flop and set the ten-word flip-flop to indicate that a new ten-word group has been started.

7-6. TEN-WORD FLIP-FLOP

The processor program monitors the check-read operation by testing the ten-word flip-flop. When it is set, the flip-flop causes the master input-output priority test (99 xx0xx MMMMM), master ten-word test (99 xx2xx MMMMM), and ten-word test (69 xxx9x MMMMM) instructions to transfer control.

The ten-word flip-flop is set as the first character of each new ten-word group is read and whenever the read-SBB flip-flop in the read circuits of the connected synchronizer is set. The program can test the read-SBB flip-flop with a 73 instruction to determine whether the ten-word flip-flop was set as a result of an SBB being detected or as a result of a new ten-word group being started.

7-7. CONTINUE FLIP-FLOP

Once check-reading of a block of data has begun, the operation continues to the end of the block. The program may continue the operation into the next block by executing either a 70 or 71 instruction while the last ten-words of the block are being read. However, to simplify programming a 70 or 71 instruction is normally executed during each ten-word group if the operation is to continue into the next block. Both the 70 and 71 instruction set the continue flip-flop. When the flip-flop is set it alerts the read-SBB controls in the synchronizer. If the flip-flop is set when an SBB is detected, reading will continue through the SBB and into the next block. When the flip-flop is reset it alerts the read-ending controls in the synchronizer. If the flip-flop is reset when an SBB is detected, the check-read operation will end and the tape positioning checker will be disconnected from the synchronizer. Normally, the continue flip-flop will be reset at the beginning of each ten-word group; therefore, it must be set while the last ten-word group of a block is being read if the operation is to continue into the next block. If an error is detected during the check-read operation, the error flip-flop will jam the continue flip-flop to the reset state and thereby terminate the operation when the next SBB is detected by the synchronizer.

7-8. ERROR FLIP-FLOP

Whenever an error is detected by the read circuits of the tape synchronizer connected to the tape positioning checker, the error flip-flop in the positioning checker is set as well as an appropriate error-diagnostic flip-flop.

The error flip-flop and an error-diagnostic flip-flop are also set if a 65 instruction is executed while the ten-word flip-flop, the continue flip-flop, or one of the connect flip-flops is set. This situation would indicate that an attempt was made to connect the tape positioning checker while it was already connected or that the continue flip-flop, the ten-word flip-flop, or one of the connect flip-flops was not properly cleared.

The error signals that set the tape positioning checker error flip-flop are listed and described in table 7-1. The number of the error-diagnostic flip-flop that is set when the error signal is generated is also listed. The first two digits of the number in the third column of the table identify the number of the instruction that tests the diagnostic flip-flop; the third digit is the selector digit. For example, diagnostic flip-flop 46-7 is tested by a 46 selector that has a selector digit of 7.

Table 7-1. Tape Positioning Checker Error Signals

Error Signal	Signal Name	Diagnostic Flip-Flop Set	Condition Causing Error
SCALE	Connected Already	46-7	A 65 instruction is executed while the continue flip-flop, the ten-word flip-flop, or one of the connect flip-flops is set, indicating that the tape positioning checker is already connected or improperly cleared.
SCOS1...4	Overskew	47-8	New sprocket pulse is detected by the synchronizer before preceding sprocket pulse has gated its associated character into the skew flip-flops.
SCBCE1...4	Bad Count	47-7	The number of characters in a block differs by 12 or less from the number actually read. This error initiates a read-ending sequence.
SCVBCE1...4	Very Bad Count	47-2	The number of characters in a block differs by more than 12 from the number actually read. This error initiates a read-ending sequence.
SCRUD1...4	Tape Runaway	46-0	Tape travels 17½ inches without data being detected by synchronizer. This error signal initiates a read-ending sequence.
SCRCE1...4	-	46-5	An input odd-even error detected at a time other than during a hash-pulse period.
SCRWCE1...4	-	None	An input odd-even error detected during a hash-pulse period.

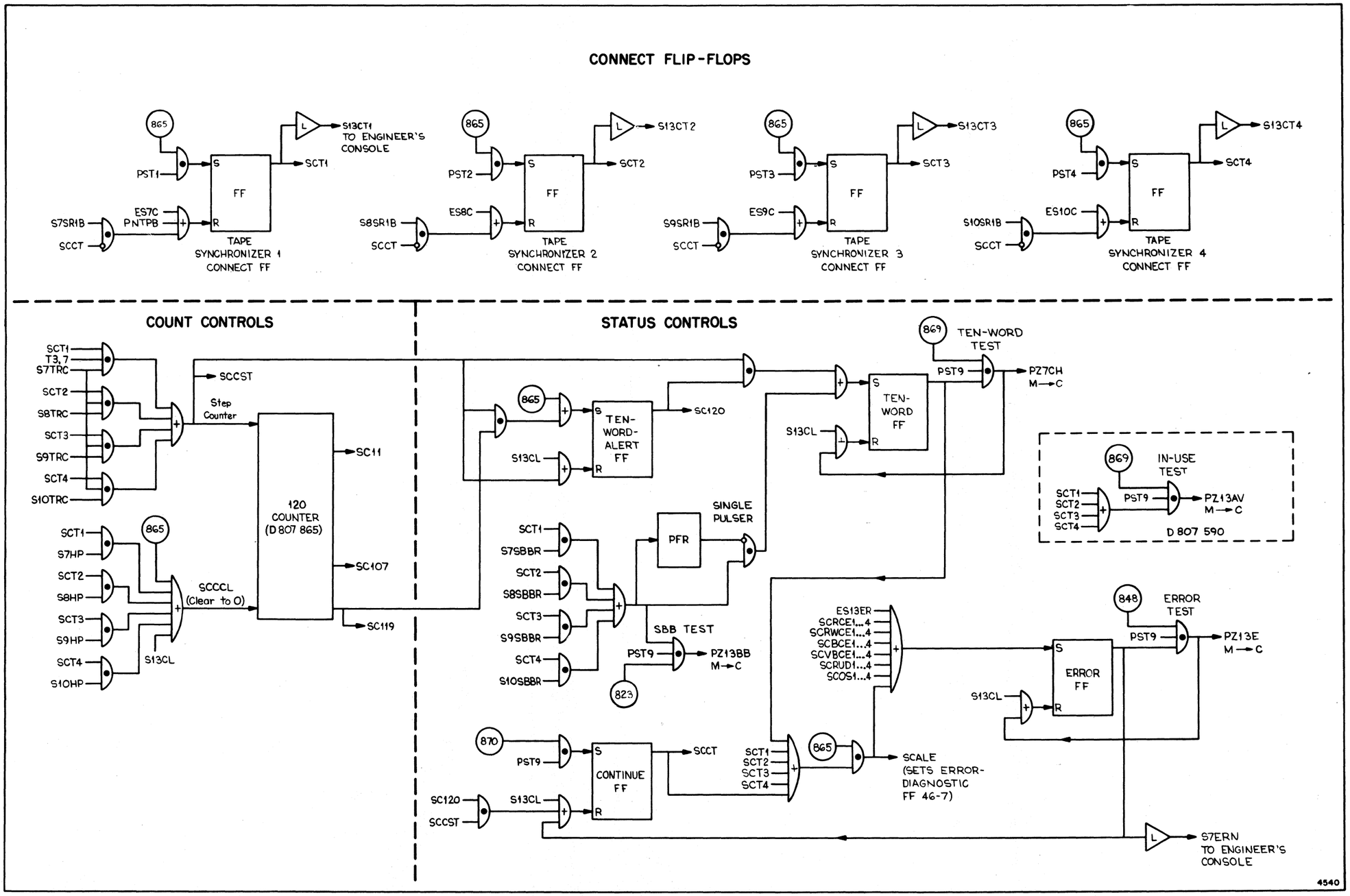


Figure 7-1. Tape Positioning Checker (D 807 865 and D 807 866)

APPENDIX
INITIAL-READ CIRCUITS

A-1. GENERAL

The initial-read circuits (figure A-1) are associated only with Synchronizer 7. They provide a means by which the maintenance engineer can manually initiate the transfer of a block of data from a tape mounted on Uniservo tape unit 10 to storage. Normally, initial data is read into the cleared Larc Computing System by way of the paper tape reader mounted on the console printer and controlled by the INITIAL LOAD pushbutton on the operator's control console. However, the data read in in this way is transferred to storage by way of the display registers in the computing unit. The initial-read circuits in the processor provide a fast means of reading, under manual control, a limited amount of data into storage when the computing unit is shut down. Normally, the initial read-in of data is performed when the processor is being tested during a maintenance period.

Initial reading is controlled by the INITIAL READ and START switches on the processor panel of the engineer's control console. The initial-read switch is connected in series with the continuous (CON) mode switch, which, in turn, is mechanically interlocked with the other mode switches. For the initial-read switch to be effective, a mode switch other than continuous (CON) must be activated.

The procedure for starting initial reading is as follows:

(1) Make certain the MASTER CHECK OPTION pushbutton N (normal) and the mode pushbutton 1 INS (one instruction) are depressed.

(2) Depress the CLEAR pushbutton GEN (general clear).

(3) While holding down the INITIAL READ pushbutton, depress the START pushbutton once.

When the START pushbutton is depressed, the INITIAL READ pushbutton lights and one block of data is read from the tape on Uniservo tape unit 10 into storage, beginning at location 00000. The data is read in the numeric mode at normal gain with the Univac-read flip-flop reset. When the end of the block is reached the tape stops, the light behind the INITIAL READ pushbutton goes out, and the automatic RU circuits in the central processor cause a 14 00000 00001 instruction to be executed. The processor ends up

with the contents of memory location 00001 in IR1 and 00002 in IR2. The control counter will read 00003.

A-2. INITIAL-READ-START FLIP-FLOP

As the INITIAL READ pushbutton is depressed (step 3, above) it alerts the initial-read-start flip-flop; the flip-flop is then set at T2 and reset at T0. The output of the flip-flop (PNTPK) clears the Synchronizer 7 input buffer registers in the dispatcher. When the START pushbutton is depressed, signals PNTPA and PNTPB will be generated at T5. These signals set the insert-initial-address flip-flop, set the time-out flip-flop in the central processor, and go to Synchronizer 7 where they set up and start the read-in operation. The PNTPA and PNTPB signals perform the following functions in Synchronizer 7:

(1) Reset the Uniservo selection-completed flip-flop, the Uniservo interlock flip-flop, the Uniservo-available flip-flop, and the Uniservo control-circuits-available flip-flop (figure 2-2).

(2) Jam the Uniservo-select register to 0 and set the Uniservo-select flip-flop (figure 2-2), thus selecting Uniservo tape unit 0.

(3) Jam the operation control register to 3 and set the thyratron-pickup flip-flop (figure 2-2) thus firing the read and forward thyratrons in the selected Uniservo tape unit.

(4) Reset the alphanumeric flip-flop (figure 4-4), the gain FF1, the read backward flip-flop, and the Univac-read flip-flop (figure 6-5).

(5) Set the numeric flip-flop (figure 4-4), the gain FF2, and the read forward flip-flop (figure 6-5).

(6) Set the start-tape flip-flop (figure 2-2), thus starting tape motion after the thyratrons have fired.

(7) Set the read-write-start flip-flop (figure 4-4), thus starting reading after tape motion begins.

(8) Set the Univac blockette counter to 6 (figure 6-5).

(9) Reset the tape positioning checker tape-synchronizer-1-connect flip-flop (figure 7-1).

A-3. INSERT-INITIAL-ADDRESS FLIP-FLOP

The insert-initial-address flip-flop is set at T5 and reset at T1. While it is in the set state, output PNLTP clears the Synchronizer 7 address register in the dispatcher and generates function signals 819 and $\overline{820}$. FS819 blocks regeneration of the cleared address and $\overline{820}$ blocks the priority circuits. At T1, PNLTPA and PNLTPB are generated. These signals jam decimal zeros into the synchronizer address register pulseformers to replace the cleared address.

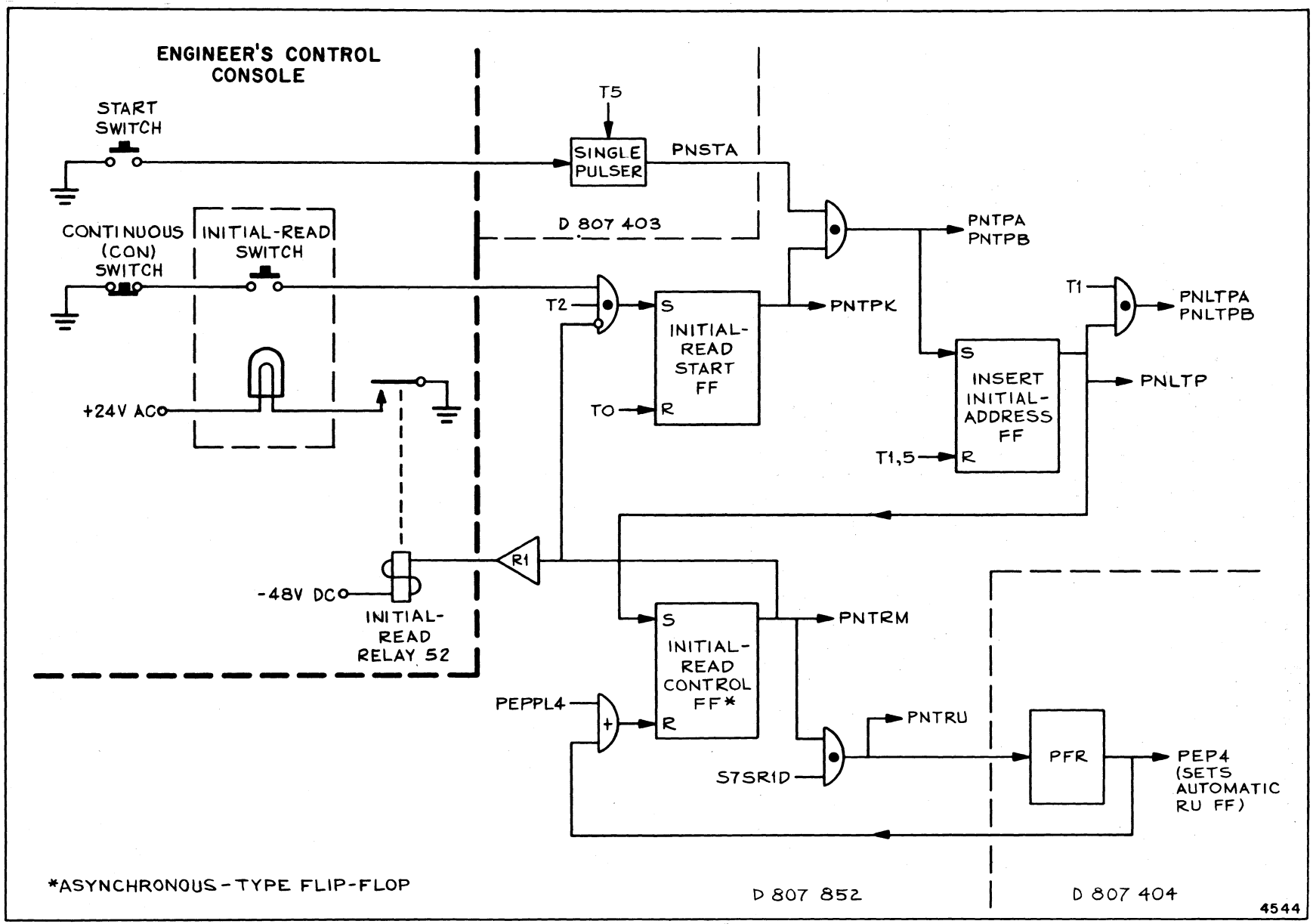


Figure A-1. Initial-Read Circuits (D 807 852)

A-4. INITIAL-READ-CONTROL FLIP-FLOP

The insert-initial-address flip-flop, when it is set, sets the initial-read-control flip-flop. This is an asynchronous-type flip-flop which remains set until the end of the initial-read operation. While it is set, it energizes the initial-read relay in the engineer's control console which causes the INITIAL READ pushbutton to light. The flip-flop also generates PNTRM which performs the following functions:

(1) Inhibits generation of the Uniservo-select error signal (S7SALE, figure 2-2).

(2) Inhibits the check-read flip-flop from being set (figure 6-5).

(3) Alerts a gate in the read-start controls (figure 6-5) which generates signal S7WFS. This signal resets the read-write-circuits-available flip-flop to "unavailable".

After a block of data has been read into storage, S7R1D from the read-ending controls samples the initial-read-control flip-flop to generate PNTRU. This signal resets the ten-word flip-flop (figure 4-4) and generates PEP4. The PEP4 signal sets the automatic RU flip-flop in the central processor and resets the initial-read-control flip-flop.