UNIVAC®

9200/9300 SYSTEMS

DATA COMMUNICATIONS SUBSYSTEM

SUPPLEMENTARY REFERENCE

UP-7614

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1. INTRODUCTION

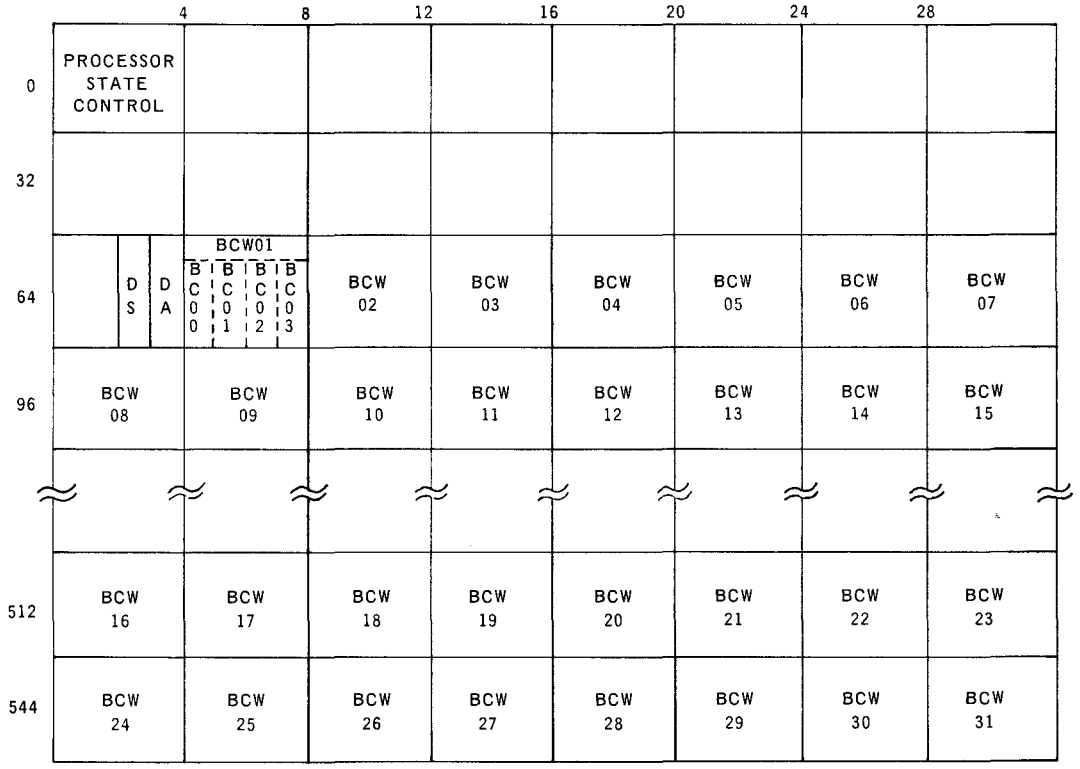
This supplement provides the basic programming information required to utilize the Data Communications Subsystem (DCS) with the UNIVAC 9200 and 9300 Series Central Processors From the point of view of the DCS, both central processors, equipped with a multiplexer channel , operate identically and the information given in this supplement is applicable to both central processors.

2. DEVICE ADDRESSING

2.1. GENERAL

The multiplexer channel (channel) recognizes two device address formats; one format is for *shared* subchannels and the other is for *nonshared* subchannels. Basically, when two or more devices share one Buffer Control Word (BCW), the subchannel is said to be a shared subchannel. An example of this is a tape controller for several tape units. The tape units (device) all share one BCW and they cannot operate concurrently. On the other hand, a subchannel is defined as nonshared when each device is assigned its own BCW. The DCS operates in a nonshared subchannel environment. The input and the output logic of each line terminal (device) are independently addressable and have their own BCW. Since each addressable device has one BCW assigned to it, which it does not share with any other device, concurrent operation of two or more devices is possible.

Figure 2-1 is a map of the main memory area utilized by systems incorporating one or more DCS's. Only those areas pertinent to control of the DCS are shown.



NOTES: Addresses are decimal.

DS – Device Status
DA – Device Address

Figure 2-1. Memory Map

2.2. ADDRESS FORMAT

The binary device address format for devices operating on nonshared subchannels is as indicated below:

00xxssss
↓

The bit indicated by the small arrow is used to indicate whether the BCW is located in the lower bank of BCW's (starting at address 68_{10}) or the upper bank of BCW's (starting at address 512_{10}). If this bit is a 0, the BCW is located in the lower bank; if it is a 1, the BCW is located in the upper bank. The location of the most significant byte (BC00) of subchannel N is memory location 64_{10} + 4N (or 512_N + 4N) where N = ssss (in binary).

For DCS's, the convention has been adopted that the devices associated with the DCS controller will use the upper bank of BCW's. The device addresses range from 40_{16} to $4F_{16}$ (needed to accommodate two DCS-4's).

For example, the device address for input logic of a line terminal to which BCW19 has been assigned is as follows:

```
00xxssss  ← DEVICE ADDRESS FORMAT
01000011  ← BINARY DEVICE ADDRESS
  4   3   ← HEXADECIMAL DEVICE ADDRESS
```

3. INPUT/OUTPUT CONTROL

3.1. GENERAL

Input/output (I/O) control requires the following software steps:

(1) Load the proper BCW with the necessary information required for data transfer and control.

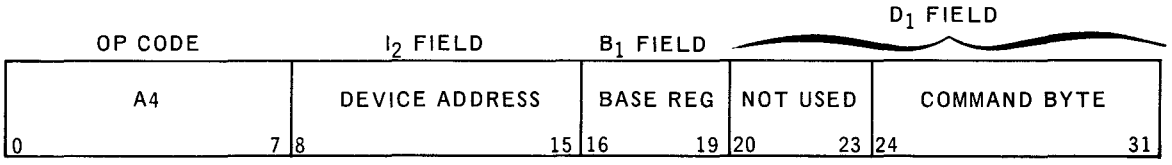
(2) Issue an I/O instruction which specifies the device address and the function to be performed.

(3) Test the Condition Code setting to determine if the instruction was accepted.

(4) Test the status of the device when the operation is completed (generally indicated by an interrupt from the device) to determine if the operation was successfully completed.

The I/O instructions all use the SI instruction format with modifications. Refer to 'UNIVAC 9200/9300 Central Processor and Peripherals, Programmers Reference Manual,' UP-7546 (current version) for basic format.

3.2. EXECUTE I/O (XIOF) INSTRUCTION



This instruction is used to initiate a function on the device specified by the I_2 field. The BCW and the buffer area (output) should have been loaded with the appropriate data prior to the execution of this instruction. The execution of XIOF instruction sets the Condition Codes (see 3.4) in the processor state control area of memory (byte 00). The possible Condition Codes (CC) in response to an XIOF instruction and their meaning are as follows:

CC = 00 Command accepted

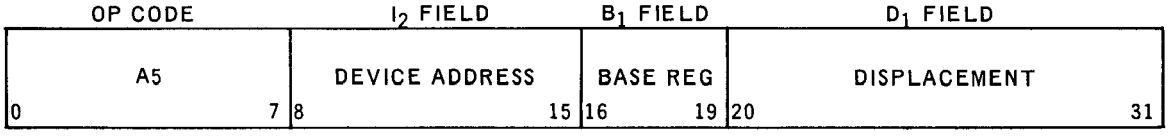
CC = 10 Command rejected

CC = 11 Command rejected - invalid device address or device is offline

When an interrupt is granted, the status of the addressed device is stored in memory

location 66_{10} and the device number is stored in memory location 67_{10} (DS and DA respectively in Figure 2-1).

3.3. TEST I/O STATUS (TIO) INSTRUCTION



The TIO instruction tests the status of the device specified in the I_2 field. The status of the device is stored at the memory address specified by the $B_1 - D_1$ fields. If the tested device is not operating, the status in the device is cleared; if the device is operating, device status is not reset. The execution of a TIO instruction sets the Condition Codes (see 3.4) in the processor state control area of memory (byte 00). The possible Condition Codes (CC) in response to a TIO instruction and their meaning are as follows:

CC = 00 Zero status - device available

CC = 01 Valid status - interrupt was pending - device now available

CC = 10 Busy status - device not available

CC = 11 Zero status - invalid device number

3.4. CONDITION CODES

When an Execute I/O or Test I/O instruction is issued by way of the channel, the results of the operation are summarized in the Condition Code (CC) and placed in the processor state control area of memory. Table 3-1 summarizes the Condition Codes and their meaning.

CC CODE	EXECUTE I/O INSTRUCTION	TEST I/O INSTRUCTION
0 0	Command accepted. No channel error. Status byte all 0's except for CHANNEL and DEVICE END bits.	Device available. No channel error.
0 1	Command rejected. No channel error. Status other than BUSY or CHANNEL and DEVICE END pending.	Nonzero status stored and cleared. No channel error. Status other than BUSY.
1 0	Command rejected. No channel error. Device BUSY. Status, if any, is BUSY.	Device BUSY. No channel error.
1 1	Nonoperational device. Probe return or channel error.	Nonoperational device. Probe return or channel error.

Table 3-1. Condition Codes

4. BUFFER CONTROL WORDS (BCW)

4.1. GENERAL

Each subchannel (addressed device) requires a four-byte BCW in main memory. The BCW's contain initial and working data counts, data addresses, and control bits. The program must load the proper BCW with the correct initial conditions before issuing an Execute I/O order. Refer to Figure 2-1. BCW's 01 through 04 are reserved for use by card readers and punches, and for printers (if any). Generally speaking, BCW's 5 through 31 are reserved for the DCS. Univac has adopted the convention that DCS devices will utilize BCW's 16 through 31.

4.2. BCW FORMAT

An alternate BCW Format (LT BCW format) is provided for the DCS. This format differs from the standard BCW format for the UNIVAC 9200/9300 Central Processor in that it has provision for fixed-length, wraparound buffer addressing which may be considered a limited form of data chaining. This operation is defined by *program* and not by any device characteristic. The LT BCW format is specified when the W and M bits of byte BCOO are both 1's (would specify 'write backwards' in normal format). Figure 4-1 illustrates the LT BCW format.

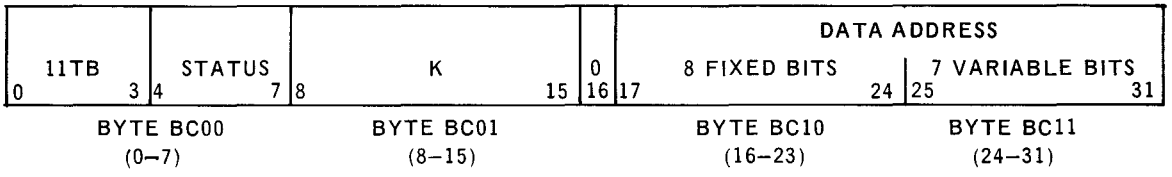


Figure 4-1. LT BCW Format

T (Terminate) Bit - Whenever T = 1, no data is transferred, the data address is not modified, and the channel gives the terminate response to data requests. The channel will set T = 1 when wraparound error occurs (see B bit below). The channel will not erase a T bit.

B (Buffer End) Bit - When the data address modification generates a carry out of the data address bit position (bit 26), the channel sets B = 1 and generates an LT summary interrupt request. The setting of the B bit alerts the program that a 64-byte buffer segment has ended. The program must reset the B bit when the buffer is again ready for use. If the channel finds a set B bit remaining in the BCW when the end of buffer action occurs again, the channel sets T = 1 thereby terminating

transfers so as to prevent data overlay (wraparound error condition). The channel will not erase the B bit.

STATUS Field – When a device initiates a present status sequence, bits 4 through 7 of the status byte are merged (OR'ed) into this field. If the central processor allows the interrupt, the entire status byte is also placed in the interrupt entry area and the LT summary interrupt request is reset. If the interrupt is not allowed, the LT summary interrupt request is set. The STATUS field must be cleared by program when data transfer is completed.

K Field - If a device attempts to present status while bits 4 and 5 of the BCW STATUS field were both previously 0, the eight least significant bits of the DATA ADDRESS field are transferred to the K field. If either bit 4 or 5 of the STATUS field was previously a 1, the transfer does not take place.

DATA ADDRESS Field - This field contains the address of the next data byte to be transferred. Address modification is always A + 1 → A (Mod 128). This sequence, in conjunction with the B bit, gives the effect of alternating the use of two adjacent 64-byte buffer areas.

4.3. DATA DIRECTION CONTROL

The LT BCW format does not provide control bits for indicating data direction. When using a DCS, odd-numbered devices are assumed to be input devices and even-numbered devices are assumed to be output devices. Thus, the least significant bit of the device address indicates data direction.

4.4. LT SUMMARY INTERRUPT

Certain device addresses are recognized and/or generated by the channel. One of these 'dummy' device addresses is the LT summary interrupt (device address 88_{16}) . This address is generated whenever a device reaches buffer end or a request to present status is rejected. At this point, the LT summary interrupt request flip-flop is set and when the interrupt is allowed, 88_{16} is placed in the device address (DA) main memory area (memory location 67_{10}) and $0C_{16}$ is placed in the device status (DS) area (memory location 66_{10}). Channel clear or master clear will set the inhibit flip-flop to the inhibit state which suppresses LT summary interrupts. This interrupt can be cleared with a Test I/O instruction. Further information concerning the LT summary interrupt can be found in Section 5.

5. COMMUNICATIONS CONTROL ROUTINES

5.1. GENERAL

The function of the Communications Control Routine (CCR) is to provide control information to the Supervisor program. Univac will provide CCR's for using the UNIVAC 9200/9300 Series Central Processors and the Data Communications Subsystem to communicate with other Univac hardware units such as another 9200/9300 Central Processor, DCT 2000, etc. However, if the device being communicated with is not manufactured by Univac, the user must write his own CCR. This section describes the linkage needed between the user's CCR and the Supervisor. This discussion covers three major areas:

- Communications interrupts
- Issuance of input/output request
- Clocking

5.2. COMMUNICATIONS INTERRUPTS

When operating with communication devices, two types of interrupts can occur: the normal end of function interrupt and the LT summary interrupt. The normal interrupt occurs when the DCS completes a transmit or receives function to or from a given device. When this interrupt occurs, the channel logs the interrupting device address in storage location 67_{10} and presents a device status in storage location 66_{10}. An LT summary interrupt can be generated when 64 characters of the message buffer are filled or when a communications function is completed but, because interrupts are inhibited for some reason, normal device address and status cannot be presented. LT summary interrupts provide no device address and store status in the BCW associated with the interrupting device.

Although LT summary interrupts are not mandatory for communications, the nature of the operation suggests their use for most efficient operation. In order to provide the LT summary interrupt capability, the LT BCW format is used for all communications lines. When the LT BCW format is used, a normal interrupt causes status to be stored in the BCW as well as in location 66_{10}.

5.2.1. Interrupt Processing

It is the responsibility of the user's CCR to provide a routine to process these interrupts when they occur and to place the address of the processing routine(s) into the Supervisor interrupt table. The Supervisor interrupt table has an entry location for each subchannel (device). The CCR interrupt processing routine address must be placed in the interrupt table location which corresponds to the device address of the interrupting line terminal. Following a normal communications interrupt, the Supervisor branches to the CCR

interrupt processing routine through the interrupt table entry for the interrupting line terminal.

To determine the proper interrupt table entry location, which should receive the CCR interrupt processing routine address for a given line terminal, the subchannel number (identical to BCW number) multiplied by 2 should be added to the base address of the table which is stored in memory locations 270_{10} and 271_{10}.

The primary function of the CCR interrupt processing routine is to check the status byte presented by the line terminal when an interrupt occurs. For communications, this status byte is the one found in the BCW associated with the interrupting line terminal rather than the status located in 66_{10}. The extended Supervisor arbitrarily assumes that the BCW's located from 512_{10} to 575_{10} are sequentially associated with subchannel addresses 16 through 31. It is necessary for the CCR to reset all BCW status and buffer bits when necessary.

5.2.2. Buffer Scan

Since the LT summary interrupt does not generate a device address when it occurs, the Supervisor must be prepared to determine which line terminal caused the LT summary interrupt. This is done by scanning the BCW's to determine which are active. A buffer scan table is provided in the Supervisor which must be loaded with the address of any BCW associated with a line from which an LT summary interrupt is expected. Each scan table entry consists of four bytes in the following format:

Bytes 0 and 1 - BCW address

Bytes 2 and 3 - Interrupt routine address

The interrupt routine address supplied in the scan table is the same as the one supplied in the Supervisor interrupt table.

The following instructions are used to load the buffer scan table:

```
LH 15,LABEL

SRC 0,30
```

LABEL is a label which points to an address constant containing the address of the BCW. This must be immediately followed in memory by the interrupt processing routine address constant. The interrupt caused by the SRC will result in the entry pointed to by register 15 being placed in the scan table. This coding would most likely appear in the user's 'OPEN' subroutine of the CCR.

A scan priority can be set up by the sequence in which the BCW addresses are placed in the scan table.

To remove a BCW from the scan table, the following instructions are required:

```
LH 15,LABEL

SRC 0,32
```

LABEL is the label which points to the BCW address constant. The Supervisor responds to the interrupt by finding a match for the BCW address pointed to by register 15 and clearing it to binary zero.

When a BCW is found to be active during the scan, the Supervisor branches unconditionally to the interrupt routine. The Supervisor also controls re-entry so that a complete scan of all BCW's is done before exiting from the original LT summary interrupt.

5.3. ISSUANCE OF INPUT/OUTPUT REQUESTS

Input/output (I/O) requests are normally executed in I/O mode. When a routine is in processor mode, and must switch to I/O mode to execute an I/O request, the following instructions are required:

```
LH 15,LABEL

SRC 0,34
```

LABEL is the label of an address constant which points to the routine to be entered in I/O mode. The Supervisor responds to the resulting interrupt by executing an unconditional jump, in I/O mode, to the address in processor register 15. The routine at the address specified in register 15 would contain the I/O instruction (XIOF) to be executed. When the request is executed, the subroutine should return control to the Supervisor's re-entry routine, the address of which is in locations 274_{10} and 275_{10} of the Supervisor.

The instructions shown above may also be used by any program that has need to switch to I/O mode to inhibit interrupts.

5.4. CLOCKING

The Supervisor maintains a 1-second counter for clocking purposes. This facility is available to any routine desiring interrupts each second. The user can then maintain within his program a clock value of any desired setting for checking time limits, polling, etc.

The Supervisor maintains a clocking table made up of two-byte entries. The CCR should enter the address of an interrupt handling routine in the table for any program desiring notification at 1-second intervals. This would most likely be done during the 'OPEN' portion of the CCR. The following instructions are required to place an address in the clocking table:

```
LH 15,LABEL

SRC 0,36
```

LABEL is the label of the address constant containing the address of the routine to be executed as a result of the 1-second interrupt. The interrupt resulting from the SRC would cause the address in register 15 to be stored in the clocking table by the Supervisor.

The Supervisor, when recognizing a 1-second interrupt, resets the clock, and executes a BAL, through I/O register 15, to each address in the clocking table. When an individual

user routine, which was branched to because of the interrupt, completes its task, control must be returned to the Supervisor through I/O register 15. This means that the 1-second interrupt routine must be executed in I/O mode.

To remove an address from the clocking table, the following instructions are required:

```
LH 15,LABEL

SRC 0,38
```

LABEL is the label of the address constant containing the address to which control was to have been transferred in the case of a 1-second interrupt.

The Supervisor responds to the SRC interrupt by finding a match in the clocking table and clearing the entry to binary zero.

The clocking table entries are checked by Job Control following end-of-job indication (EOJ), a cancellation, or a Kill keyin to eliminate the entry from the table for the cancelled program or symbiont.

The Supervisor assumes the obligation, when loaded, of initiating the 1-second clock and of permitting LT summary interrupts.

When a job is cancelled, the Non-Concurrent Operating System (NCOS) and Concurrent Operating System (COS) Supervisor will clean up the interrupt table, scan table, and clocking table. The Minimum Operating System (MOS) Supervisor must be reloaded after a cancellation.

The inclusion of the communications portion of the Supervisor, as well as the size of the buffer scan table and clocking table, is optional and is specified by the user at the time the Supervisor is generated. During buffer scan and clock interrupts, during which time the user's CCR has control, I/O register 8 must be preserved if it is used by the interrupt processing.

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