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CORE MEMORY
Type 9150-10

Maintenance Manual

Field Engineering Department
Ilion, New York

UNIVAC
DIVISION OF SPERRY RAND CORPORATION

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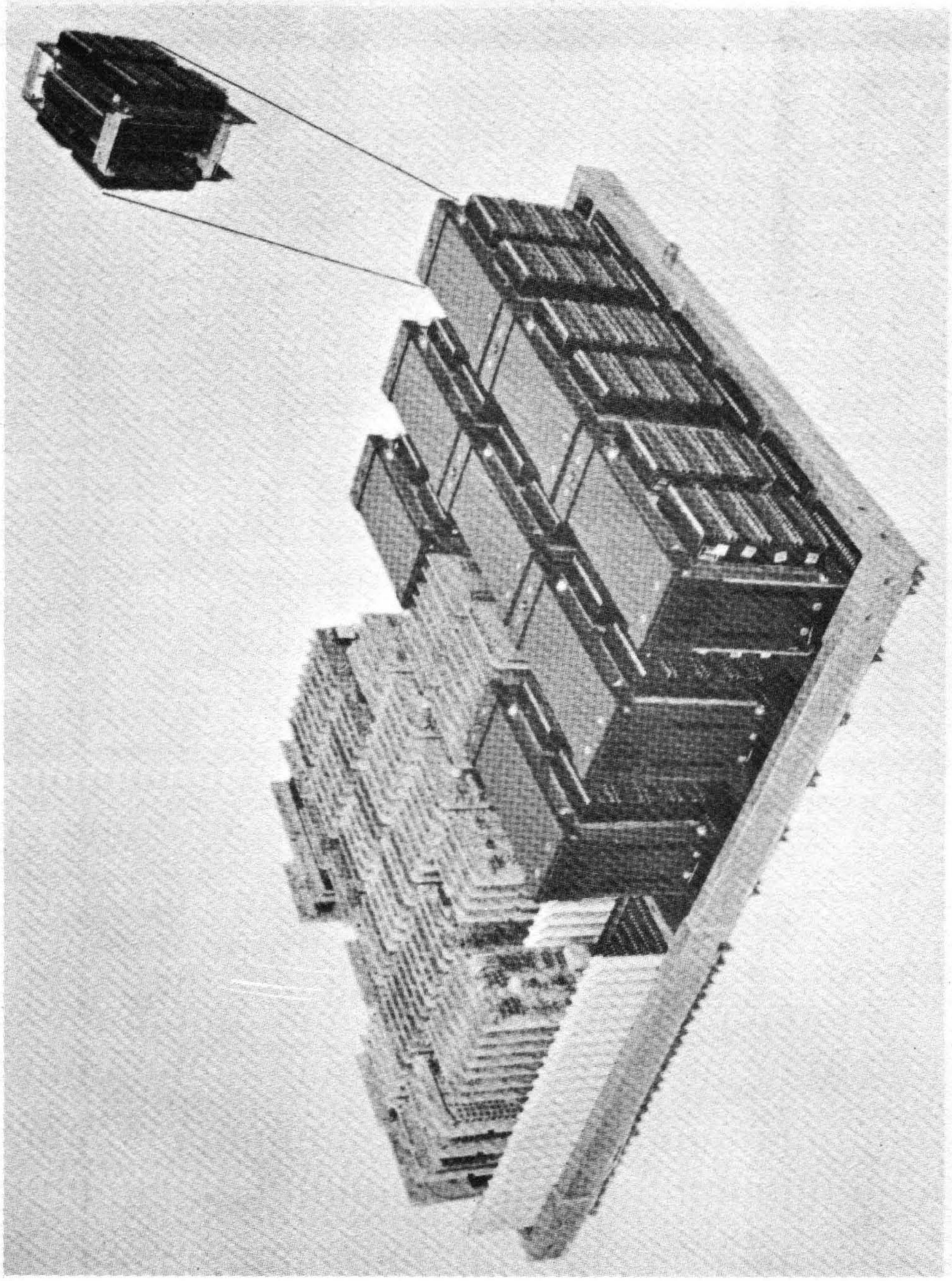


Figure 1-1. Model M2-32 Core Memory From UNIVAC 1050

SECTION 1

INTRODUCTION

1-1. GENERAL DESCRIPTION

The Type 9150-10 memory is a random-access, bit-organized, coincident-current core storage unit which can be readdressed every four and one-half microseconds. The memory together with the address and data registers of the processor provides data storage for the processor. The memory operates in either of two cycles, the clear/write cycle and the read/write cycle, which are controlled by signals received from the processor. During a clear phase of a clear/write cycle, the information stored in the memory at the selected address is read out and destroyed. New information from the processor is stored in the memory during the write phase. During a read phase of a read/write cycle, the information stored in the memory at the selected storage location is read out and transferred to the processor. Information from the processor is then restored in the original storage location during the write phase.

The memory is packaged on one UNIVAC® standard 6 by 6 connector frame and is mounted in the processor cabinet. The electrical power and air cooling are provided by the processor power and cooling systems. The storage capacity of the type 9150-10 memory is variable in groups of 4096 characters from a minimum of 4096 seven-bit characters to a maximum of 32,768 seven-bit characters. The capacity is increased by plugging in the proper additional printed-circuit boards and unit stacks. The connector frame, connectors, and the backboard wiring for a maximum storage capacity memory are included in the minimum unit.

1-2. FUNCTIONAL CHARACTERISTICS

Character bit length:		7 bits
Storage Capacity:	9150-3	4,096 seven-bit characters
	-4	8,192 seven-bit characters
	-5	12,288 seven-bit characters
	-6	16,384 seven-bit characters
	-7	20,480 seven-bit characters
	-8	24,576 seven-bit characters
	-9	28,672 seven-bit characters
	-10	32,768 seven-bit characters
Cycle Time:		4.5 microseconds

1-3. PHYSICAL CHARACTERISTICS

Dimensions:

Width	26 1/2 inches
Height	19 1/2 inches
Depth	6 inches

Weight:

Minimum	45 pounds
Maximum	60 pounds

Power Requirements:

AC Voltage	None	
DC Voltage	Minimum Current	Maximum Current
+20 volts	8.0 amps	9.8 amps
ground		
-8 volts	2.0 amps	5.2 amps
-30 volts	2.5 amps	2.5 amps

Cooling Requirements:

200 cfm

1-4. INTERFACE CHARACTERISTICS

The processor-memory interface signals and the function performed by each are listed in table 1-1. The polarity shown is when the signal is utilized.

TABLE 1-1. INTERFACE SIGNALS AND FUNCTIONS

SIGNAL	LINE DESIGNATION	POLARITY	FUNCTION
Input Signals Unit Stack Select	$\overline{\text{PARU1}}$ through $\overline{\text{PARU8}}$	+	Selects corresponding stack by selecting the associated read/write diverters and inhibit drivers.
Timing Pulse	PTP2M	-	Initiates internal memory timing
Unit Enable	PBUEA	+	Enable read/write current generators
Read Enable	$\overline{\text{PREAD}}$	+	Enable the strobe gate.
Address Information	$\overline{\text{PARY0}}$ through $\overline{\text{PARY7}}$	+	Provides Y-axis line selection
	$\overline{\text{PARX0}}$ through $\overline{\text{PARX7}}$	+	Provides X-axis line selection
	PARY00 PARY10 PARY20 PARY30 PARY40 PARY50 PARY60 PARY70	+	Provides X-axis bus selection
	$\overline{\text{PARX00}}$ through $\overline{\text{PARX07}}$	+	Provides X-axis bus selection
Write Data	$\overline{\text{PMZ1}}$ through $\overline{\text{PMZ7}}$	+ for 0	Data to be stored in memory
Output Signals Output Data	MOZ01 through MOZ07	+ for 0	Data read from memory and transferred to the processor
Marginal Check Voltage Lines			
Marginal Check Low	OZMCM2	-	Controls the output from the Read/Write and inhibit drivers by controlling the voltage regulator output.
Marginal Check High	OZMCM1	-	

SECTION 2

FUNCTIONAL DESCRIPTION

2-1. SCOPE

This section describes the functional operation of the logical sections of the memory. A detailed logic description is presented in Section 3.

2-2. GENERAL

The type 9150-10 memory provides data storage for the processor. When utilizing the memory, the processor may either store data in the memory or retrieve data from the memory, depending on the requirements of the given processor operation. When data is to be stored in memory, the memory performs a clear/write cycle of operation and, when data is to be retrieved from the memory, a read/write cycle of operation is performed. When performing either cycle of operation, the memory is dependent upon the processor for control information pulses.

2-3. CYCLES OF OPERATION

The operation of the memory cycles must coincide with the processor timing sequence. Thus the processor initiates the memory action and also provides the memory with the input data at the proper time. Since the processor is the controlling agent, the cycle in which the memory operates is determined by the processor. Also the storage location and the core stack to be utilized are selected by signals from the processor. The transfer of information from the memory to the processor and the step-by-step timing of a memory cycle are controlled by the memory timing circuits.

During memory operation the initiating pulses (PTP2M and PBUEA), the address information (PARX-, PARX--, PARY-, and PARY--), one of eight unit stack select signals ($\overline{\text{PARU1}}$ through $\overline{\text{PARU8}}$), and the read enable ($\overline{\text{PREAD}}$) which controls the cycle of memory operation are sent to memory by the processor. (When the read enable is sent to the memory, a read/write cycle is initiated. When the read enable is not sent to the memory, a clear/write cycle is initiated.) At this point the timing and control section of the memory assumes control,

and utilizing the signals received from the processor, a unit stack and the storage location within the stack are selected. Then either a clear/write cycle or a read/write cycle is performed.

a. CLEAR/WRITE CYCLE. - During the clear phase of the clear/write cycle the data stored at the selected storage location is read from the cores. Because the read enable is not received from the processor during this phase, the strobe pulse is not developed and the data read from the cores is not transferred to the processor, but is destroyed.

During the write phase, the processor sends new data to the memory. This new data is stored or written in the same storage location from which the old data was read out and destroyed.

b. READ/WRITE CYCLE. - During the read phase of the read/write cycle, the data stored at the selected storage location is read from the cores. The read enable pulse and a timing pulse from the memory timing circuits provide a strobe pulse which transfers the amplified version of the data read from the cores to the processor.

During the write phase, the processor sends data to the memory. This data is then stored in the same storage location from which the original data was read.

2-4. MEMORY LOGICAL SECTIONS

The following paragraphs describe the functional operation of the logical sections of the memory. Figure 2-1 is a block diagram of a 4K memory showing the interrelations among the timing and control section, the address section, the core stack, and the data section.

a. TIMING AND CONTROL SECTION. - This section contains the internal timing circuits and the control circuits operated from the timing circuits. The timing circuits receive the PTP2M pulse from the processor which initiates the timing action of the memory. The timing pulses from the timing circuits are used in conjunction with the unit enable and read enable signals from the processor to operate the control circuits. The control circuits provide the necessary pulses for internal timing and control of the memory.

b. ADDRESS SECTION. - This section contains the selector switches, the X and Y selection systems and the X and Y read/write current generators. The selector switches are operated by the address information from the processor and control the X and Y selection systems. The selection systems select one X drive line and one Y drive line in each stack and provide a path to supply the driving currents to the selected drive lines. The read/write current generators supply the current necessary to switch the selected cores.

c. UNIT STACK. - A unit stack consists of seven core planes. One storage location (a core in each plane) is selected when one X drive line and one Y drive line are selected by the selection system. Information received from the processor is stored in the core stack.

One of the eight unit stacks is selected by the unit stack select pulse which enables the associated read/write diverters and inhibit drivers.

d. DATA SECTION. - This section contains the preamplifiers, the sense amplifiers, and the inhibit drivers. The preamplifiers receive the signals read from the core stack, amplify them, and reduce the noise pulses to a level below the saturation level of the sense amplifiers. Each sense amplifier receives the outputs from a maximum of eight preamplifiers, only one of which is active during a given cycle, and amplifies the signal; when strobed, the amplifier outputs are transferred to the processor. The inhibit drivers are selected by the unit stack signals and are timed by the inhibit driver enable timing pulse from the timing and control section; when 0 data bits are received from the processor, the drivers supply the inhibit current to the core stack. The inhibit current counteracts the effect of the Y write current during a write phase and prevents writing a 1 in that plane.

SECTION 3

LOGIC DESCRIPTION

3-1. GENERAL

This section explains the logical operation of the memory. Paragraphs 3-2 through 3-4 describe the operation of logic sections outlined in Section 2. The interactions of the logic sections are demonstrated in descriptions of the clear/write cycle and the read/write cycle under paragraphs 3-6 and 3-7.

The logic of the memory is presented on drawings 4026120 through 4026123, 4026125, 4026126, 4026142, 4026144, 4026146 and 4026147. Figure 3-1 is a block diagram of a 32,768-character memory. The circuits represented by the blocks enclosed within the dashed lines must be added to increase the memory capacity from 4096 characters. All other circuits represented are common to all capacity options.

3-2. TIMING AND CONTROL SECTION

This section contains a 4.0-microsecond delay line, the delay line drivers, and the control circuits operated from the delay line. The timing and control section receives the PTP2M pulse, the unit enable (PBUEA) and the read enable ($\overline{\text{PREAD}}$) signals from the processor and develops the internal timing and control pulses for the memory. The timing and control pulses developed are the read driver enable (RDRVRE), the read diverter enable (RDVTRE), the strobe pulse, the write driver enable (WDRVRE), the write diverter enable (WDVTRE) and the inhibit driver enables 1 through 4 (IDE 1).

Drawing 4026120 is the logic diagram of the timing and control section. The delay line has taps available at 50-nanosecond increments. A pulse is applied to the input of the delay line; as it traverses the delay line, it is tapped off at the required time to control the timing of the memory. Figure 3-2 is a timing diagram of the pulse tapped from the delay line. Drawing 4026154 is a timing diagram of key memory signals. The times shown on the diagram are typical and may vary from one memory to the next. The use of these pulses may best be understood by referring to figures 3-3 and 3-4. These figures show the timing sequence for a clear/write cycle and a read/write cycle.

The pulse applied to the delay line is developed from timing pulse, PTP2M, received from the processor. PTP2M sets the single-shot multivibrator. The inverter in the 1 output line from the SS sends a negative going pulse to the 0.4-microsecond time delay circuit. Since the time delay circuit is an open ended delay line, the input pulse is reflected back. The time required for the pulse to traverse the delay circuit and to be reflected back is 0.8 microsecond. Thus, a 0.8-microsecond negative pulse is developed and applied to the 4.0-microsecond delay line circuit which supplies the internal timing of the memory. The first timing pulse from the 4.0-microsecond delay line clears the single-shot multivibrator. The SS stays in the clear state until the PTP2M pulse is received at the beginning of the next cycle.

3-3. STORAGE LOCATION SELECTION

This section is composed of the selector switches, the X and Y transformer diode matrices, and the X and Y read/write current generators. The selector switches receive the address information from the processor and control the X and Y transformer diode matrices. The matrices each select one drive line and provide a path to supply the driving currents to the cores. The read/write current generators supply the driving current necessary to switch the selected cores.

The logic diagrams of the selection section are 4026121, 4026126, 4026142 and 4026144. Address information is received from the processor in octal code. Thirty-two bits, divided into four groups of eight bits each, are required for the X and Y selection. Address bits $\overline{\text{PARX0}}$ through $\overline{\text{PARX7}}$ operate the X line switches, bits $\overline{\text{PARX00}}$ through $\overline{\text{PARX07}}$ operate the X bus switches, bits $\overline{\text{PARY0}}$ through $\overline{\text{PARY7}}$ operate the Y line switches, and bits $\overline{\text{PARY00}}$, $\overline{\text{PARY10}}$, $\overline{\text{PARY20}}$, $\overline{\text{PARY30}}$, $\overline{\text{PARY40}}$, $\overline{\text{PARY50}}$, $\overline{\text{PARY60}}$ and $\overline{\text{PARY70}}$ operate the Y bus switches. These switches operate the X and Y selection matrices. The X and Y selection matrices are each composed of 64 line transformers and 8 bus transformers. Each bus transformer drives eight line transformers. The line and bus transformers are represented by AND gates on logic diagrams 4026142 and 4026144. On drawing 4026142 the gates numbered 164 through 179 are bus transformers; all other gates represent the line transformers.

The selection of one line switch and one bus switch by the address information provides a path for the application of the driving current to the core stack drive line. The actual selection of a drive line is not completed

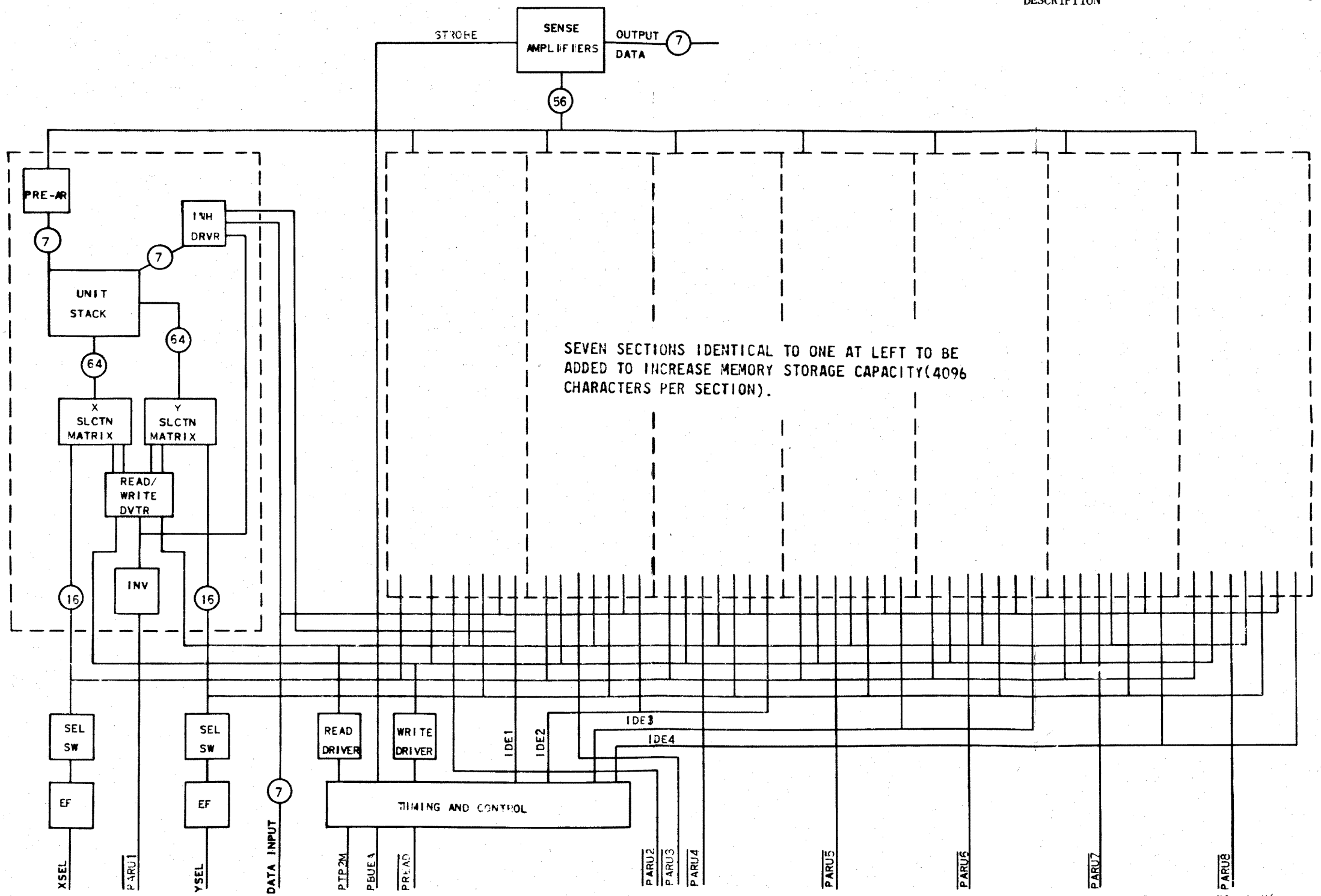


Figure 3-1. 32K Memory Block Diagram

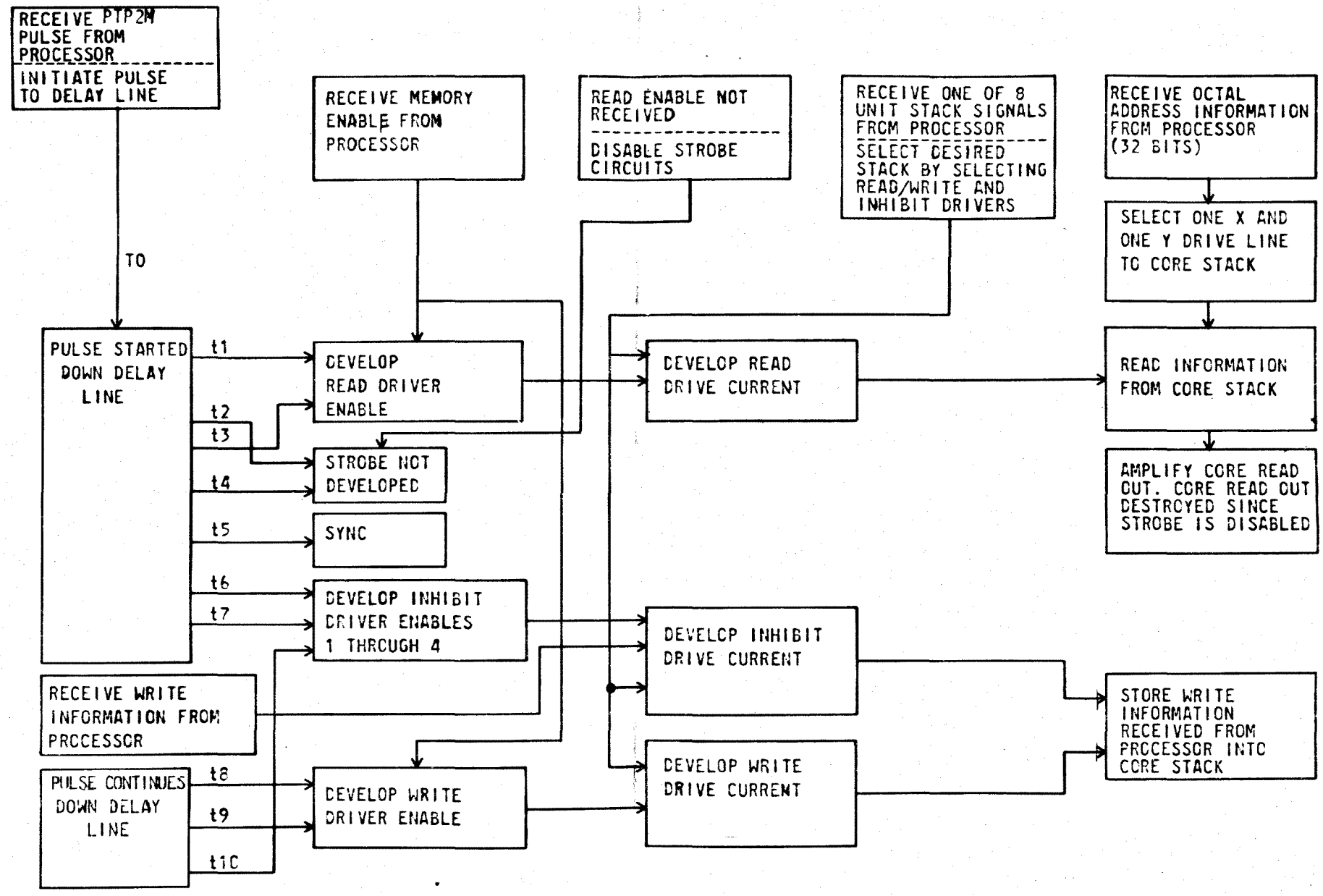


Figure 3-3. Timing Sequence of Clear/Write Cycle

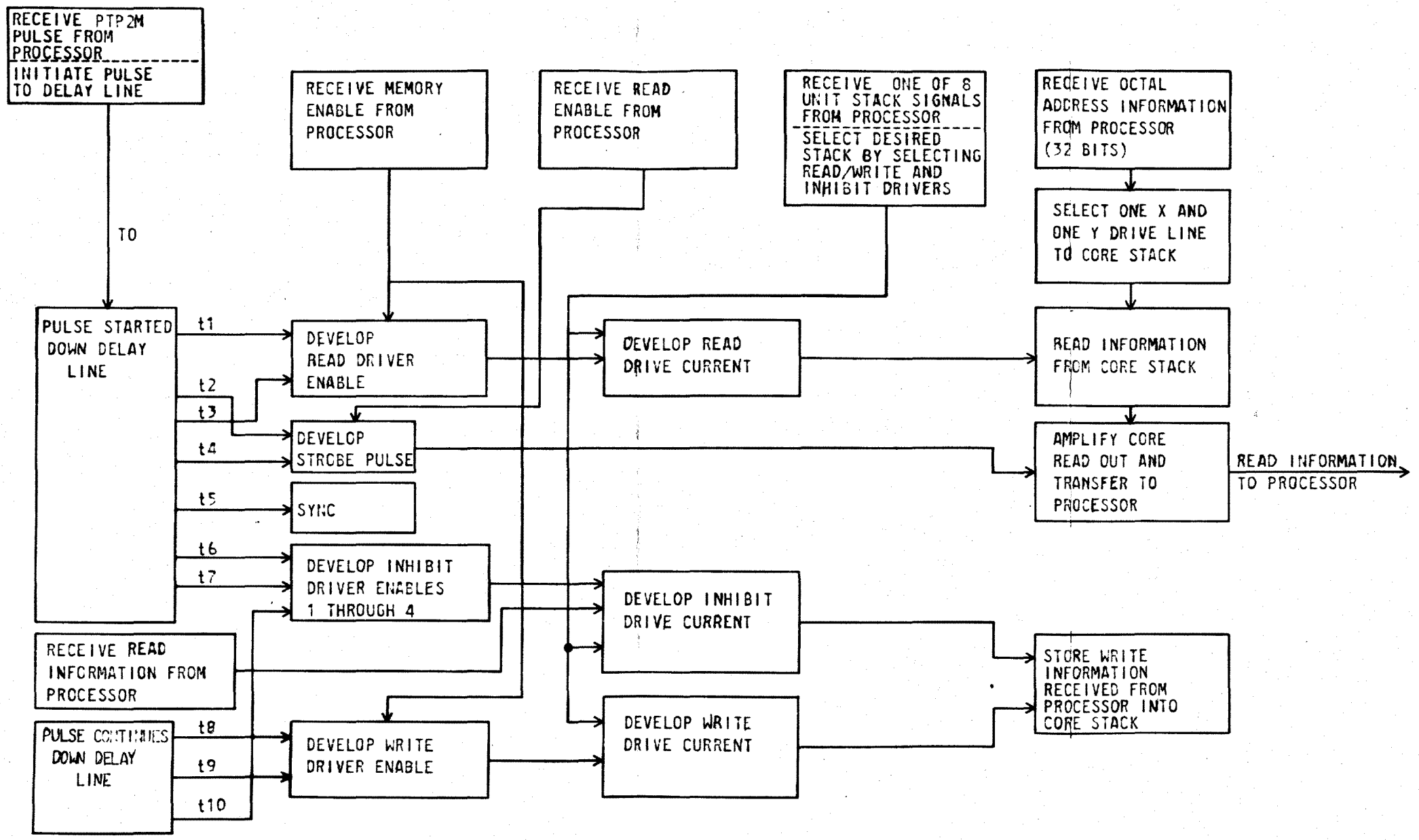


Figure 3-4. Timing Sequence of Read/Restore Cycle

until the read or write drive current is supplied to the selection system bus transformers. The read current generator for the addressed stack is selected by the unit stack select pulses USS1 through USS8, and when the read driver enable is received from the timing section of the memory, the generator is operated and supplies driving current to the selection system bus transformer. The read drive current is transformer coupled to the selected core stack drive line by the selected line transformer. The selection of one output from the selection system and the flow of read current is shown by heavy lines on figure 3-5. The flow of write current is identical to that of the read current utilizing the opposite half of the bus and line transformers. The write drive current is supplied by the write current generator which is selected by the unit stack pulse and timed by the write driver enables from the timing section of the memory.

3-4. DATA SECTION

This section is composed of 56 preamplifiers, 7 sense amplifiers, and 56 inhibit drivers for a full capacity memory. A full capacity memory is the type 9150-10 consisting of eight unit stacks of seven planes each and the associated electronic circuits. The sense output from each plane is connected to a preamplifier, thus the requirement for the 56 preamplifiers. The outputs from the preamplifiers associated with the same plane in each of the eight unit stacks are OR gated together and supply the input to one sense amplifier. Thus only seven sense amplifiers are required. This OR function is possible since only one of the eight preamplifiers is active during any one cycle. The interconnection of eight preamplifiers to one sense amplifier is shown on logic diagram 4026125.

The preamplifier receives the core readout from the sense line, amplifies the signal, and transfers it to the sense amplifier. The sense amplifier amplifies both the 1 and the 0 signals read from a core; however, the level of the 0 signal is small compared to that of the 1. Thus, by strobing the output from the sense amplifier at a level above the 0 signal and timed for the 1 signal a distinction is made between the two signals. The presence of a signal on the output data lines indicates that a 1 was read from the core, and the absence of a signal on the output data lines indicates that a 0 was read from the cores.

The above explanation is true only for the read phase of the read/write cycle. During the clear phase of a clear/write cycle the data stored in the core stack is read out and goes through the preamplifiers and sense amplifiers; however, the output from the sense amplifier is not strobed to the processor. Thus the readout from the unit stack is destroyed during the clear phase.

The inhibit drivers receive the input data from the processor during a write phase and develop inhibit current in the selected stack (logic drawings 4026122 and 4026123). The input to the drivers is a three-input AND gate. Thus the unit stack select signal, the inhibit driver enable, and a 0 input pulse is required to operate the individual driver. The $\overline{\text{PARU}}$ pulse is received from the processor and enables the inhibit drivers associated with only one stack during any one cycle. The inhibit driver enable is received from the memory timing and control section and enables all inhibit drivers in the memory. The input data is received from the processor by all inhibit drivers; however, the only drivers that operate are those that receive the USS signal.

The logic diagrams of the data section are 4026122, 4026123, and 4026125. To increase the capacity of the memory, unit stacks, preamplifiers, inhibit drivers, and stack select circuits are added. The sense amplifiers are capable of handling up to eight preamplifier outputs each. Thus only seven sense amplifiers are required for any capacity option. When less than eight stacks are used, load impedance is added to the input of the sense amplifiers to maintain the impedance match between the sense amplifiers and the preamplifiers.

During a read phase the information stored in the core stack is read out and transferred to the preamplifiers. The preamplifiers amplify the readout, eliminate the common mode noise pulses, and limit the bipolar noise pulses. The output from the preamplifiers is transferred to the sense amplifiers, which amplify the signal and transfer it to the processor during strobing. During a clear phase, the data stored in the core stack is read out and goes through the preamplifiers and sense amplifiers, but it is not strobed to the processor. Thus, the readout from the core stack is destroyed during the clear pulse.

During a write phase, data is received from the processor by the inhibit drivers. The input data from the processor along with the inhibit driver

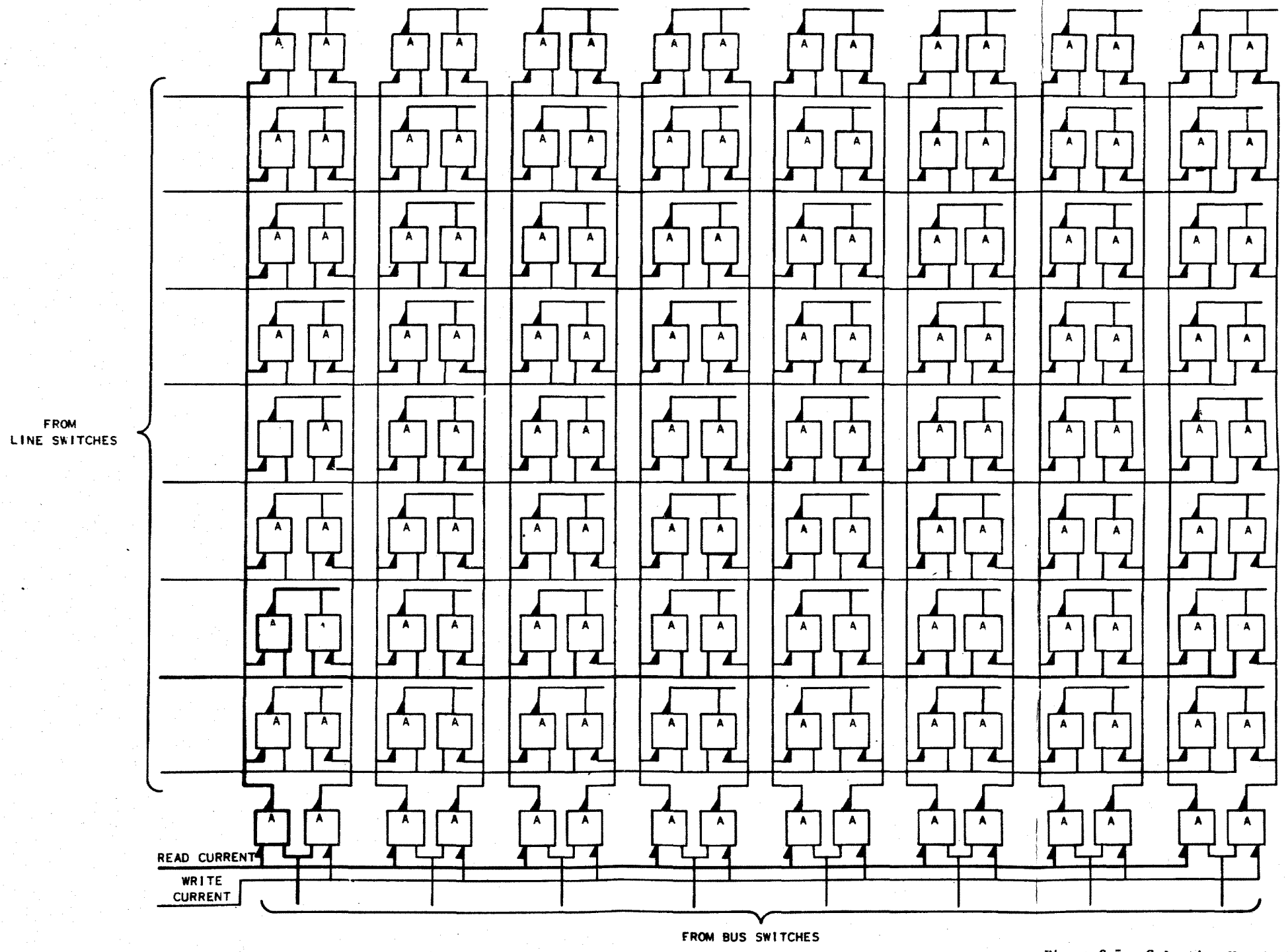


Figure 3-5. Selection Matrix Logical Representation

enable and the unit stack signal operate the inhibit drivers. The inhibit drivers that receive 1's from the processor are disabled while the drivers that receive 0's from the processor are operated. The cores in the stack that receive both the write current and the inhibit current store 0's. The cores in the stack that receive only the write current store 1's.

3-5. CYCLES OF OPERATION

The memory will perform either a clear/write cycle or a read/write cycle, depending upon the signal received from the processor. The PTP2M pulse starts the timing action of the memory. The unit enable (PBUEA) signal enables the read/write current generators. If the read enable ($\overline{\text{PREAD}}$) signal which enables the strobe circuit is received from the processor, a read/write cycle is initiated. If the read enable signal is not received from the processor, the strobe circuits are disabled, and a clear/write cycle is initiated.

a. CLEAR/WRITE CYCLE. - When the memory receives the PTP2M pulse and the PBUEA signals from the processor, a clear/write cycle is initiated. From the PTP2M pulse, the memory develops the timing pulse and applies it to the delay line. The timing pulse is tapped from the delay line at times t1 throug t13 and controls the timing of the memory circuits.

The PBUEA is received from the processor. It is AND gated with timing pulses t2 and t4 to develop the read drive enable pulse and the read diverter enable pulse. However, the latter pulse enables all read diverters in the memory. The only diverter that operates is the one selected by the unit stack signal from the processor. If information is to be stored in unit stack 1, the unit stack 1 signal is received from the processor. The read driver enable pulse operates the read driver. The octal address information is received and the storage location is selected by the selector switches operating the X and Y selection matrices of all stacks. Since only one read diverter is operated by the unit stack signal, only the information stored in that stack is read out and applied to the preamplifiers associated with that stack. The output from the preamplifiers is applied to the sense amplifiers where the readout from the core stack is amplified and rectified. Since the strobe pulse is not developed during a clear/write cycle, the information read from the cores is destroyed.

Timing pulses t8, t9, and t13 are OR gated together and develop the inhibit driver enable (IDE) pulses 1 through 4. IDE 1 enables the inhibit drivers for stacks 1 and 2. IDE 2 enables the inhibit drivers for stacks 3 and 4. IDE 3 enables the inhibit drivers for stacks 5 and 6 while IDE 4 enables the drivers for stacks 7 and 8. As in the case of the read diverters, only the inhibit drivers that receive the unit stack signal from the processor are alerted. The write data is received from the processor and applied to the inhibit drivers. The inhibit drivers associated with the selected stack operate; i.e., the inhibit drivers that receive 0 information from the processor provide inhibiting current to the selected plane, but the inhibit drivers that receive 1 information from the processor do not supply inhibit current.

Timing pulses t10 and t12 are AND gated with the memory enable signal to start the write drivers, which supply drive current to the diverters selected by the unit stack signal. This supplies the write driving current to the selected core stack. The selected cores within the stack that receives both the inhibit current and the write current store 0's. The cores that receive only the write current store 1's. Timing pulse t13 keeps the inhibit drivers on until after the write drivers have been turned off. This prevents writing 1's in all the selected cores.

b. READ/WRITE CYCLE. - The read/write cycle is similar in operation to the clear/write cycle. The only differences are that the read enable is received from the processor and the strobe pulse is developed. The strobe pulse enables the transfer of the data read from the core stack to the processor. The remainder of the cycle is identical to the clear/write cycle.

SECTION 4

CIRCUIT DESCRIPTION

4-1. GENERAL

This section presents the theory of operation of the electronic circuits used within the Type 9150-10 memory. The circuits are divided into six categories according to their functional use within the memory (refer to table 4-1). In some cases an electronic circuit is packaged on more than one printed circuit board because of the physical limitations of the board. In these cases, a composite schematic of the circuit is presented in this section. The schematics for the circuits packaged on one printed circuit board, may be found in the machine documentation manual. With the exception of the transformer-diode module, all schematics are on the assembly drawings. The assembly drawing numbers are listed in table 4-1.

TABLE 4-1. PRINTED CIRCUIT BOARDS

TYPE NO.	TITLE	ASSEMBLY DWG. NO.	ABBR.
	GENERAL CIRCUITS		
A103	Inverter and AND Gate	4026309	N, A
A122	High Power Inverter	4026362	HGN
A123	Low Power Inverter	4026365	HGN
	TIMING AND CONTROL CIRCUITS		
A105	Pulse Shaper-Delay Line Driver	4026315	SS, N. TD4
A100	Delay Line	4026300	DL
A120	Delay Line	4026360	DL
A121	Delay Line	4026361	DL
A127	Emitter Follower; AND Gate	4026377	EF, A
	ADDRESS SELECTION CIRCUITS		
A101	Selector Switch	4026303	AR
A102	Selector Switch Load	4026306	XBL, YBL, XLL, YLL
A118-A119	Transformer-diode Modules	4026354	A
	DRIVER CIRCUITS		
A113	Read/Write Driver	4026339	RDRVR, WDRVR
A114	Read/Write Diverter	4026342	RDVTR, WDVTR
A115	Power Resistor	4026345	DRVRL1, DRVRL2
A107	Inhibit Driver	4026321	N,ID

TABLE 4-1. PRINTED CIRCUIT BOARDS (Cont.)

TYPE NO.	TITLE	ASSEMBLY DWG. NO.	ABBR.
	AMPLIFIER CIRCUITS		
A151	Preamplifier	4026437	PAR
A154	Sense Amplifier	4026204	SAR
A133	Sense Load Card	4026399	SARL
	VOLTAGE REGULATION CIRCUITS		
A116	Voltage Regulator	4026348	VR
A117	Voltage Regulator Heat Sink	4026351	VRHS
A140	Temperature Control	4026420	R
A153	Sense Bias Regulator	4026442	VR

4-2. COMPONENT IDENTIFICATION

The grid system of component placement is used on all printed circuit boards. (Refer to drawing 4026300.) Therefore, all components on the schematic diagram are identified by the grid location where the topmost or leftmost component lead connects to the board. The standard symbol such as R for resistor is not included on the schematic. For ease in identifying the components when referred to in the text, the standard symbols listed in table 4-2 are used along with the grid reference of the component connections. Thus the text reference for a resistor that has its topmost or leftmost lead wire connected to the board at L3 would appear as follows:

R(L3)

When referencing a transistor, only the collector lead connection is identified.

TABLE 4-2. COMPONENT SYMBOLS

Symbol	Component
C	Capacitor
CR	Diode
L	Inductor
Q	Transistor
R	Resistor
S	Switch
T	Transformer

4-3. GENERAL CIRCUITS

a. INVERTER and AND GATE (TYPE A 103), ASSEMBLY DWG. NO. 4026309

Circuits per Board: 6

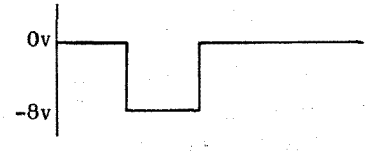
Circuit	Major Component
Low Power Inverter	Q(Q6)
Low Power Inverter	Q(L7)
High Power Inverter	Q(G7)
High Power Inverter	Q(C7)
AND Gate	CR(T1) and CR(U2)
AND Gate	CR(T5) and CR(T12)

Current Ratings:

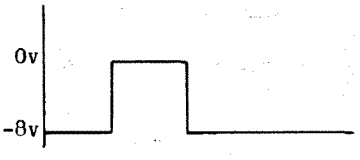
	Low Power Inverter	High Power Inverter
Input Current:	6.42 ma	20.6 ma
Output Current:	20.6 ma -0.275 volt	100.0 ma -0.285 volt

Waveshapes:

Input Waveshape:



Output Waveshape:



(1) CIRCUIT FUNCTION. - The inverters provide inversion and current gain for the timing control of the memory and for the interface signals. The inverters used in the timing control section supply the current necessary to operate the read/write drivers, the inhibit drivers, and the strobe circuit. The interface inverters drive the stack selection circuits and provide inversion for the read enable signal. Each inverter has a diode input and one direct input, only one of which may be used in a given instance. The diode input is used when isolation between the signal source and the inverter is required.

The AND gates consist of two diodes with separate inputs and a common output. The input and output pins which are available at the backboard are used throughout the system where AND gate logic is required.

(2) CIRCUIT OPERATION. - The operation of both the high and the low power inverters is identical. For the following explanation refer to circuit 1 transistor Q(Q6) of the schematic diagram listed at the heading of this section. When a high signal (0 volt) is presented to either input of the inverter, the base of the inverter transistor is driven positive from the +20 volt source due to the voltage divider action of resistor R(10) and diode CR(R10). This positive potential reverse-biases the emitter-base junction of the transistor and prevents conduction. In this state the output from the transistor is low (-8 volts). When a low signal is presented to either input of the inverter, the base of the inverter transistor is driven negative from the +20 volt and -30 volt sources by the voltage divider action of resistors R(S3), R(S7), and R(Q10). The negative potential, at the base of the transistor, forward-biases the emitter-base junction and the transistor conducts. In this state the transistor output is high (0 volt) and a low impedance path to ground through the collector-emitter of the transistor is presented to the output circuit.

The switching time of the transistor and thus the rise and fall time of the output signal is decreased by capacitor C(R1) in the base circuit. During turn-on of the transistor, the capacitor provides a path for the transient currents to enter the base circuit, and forward-bias the emitter-base junction. During turn-off the capacitor discharges through the emitter-base junction applying a reverse-bias potential to the transistor.

The AND gates shown on the assembly drawing consist of diodes and interconnecting printed circuitry. The voltage and current sources necessary for operation must be supplied by the circuits connected to the inputs and output. Figure 4-1 is a schematic of the AND gate and typical input output circuits. If either input to the AND gate is at 0 volt, the associated diode conducts and the output from the gate is nearly 0 volt which reverse biases the second diode, preventing its conduction.

When both inputs to the AND gate go negative, as shown in figure 4-1, the voltage divider network consisting of R3, R4, and R5 applies approximately -6 volts to the AND gate output. Since this potential is more positive than the

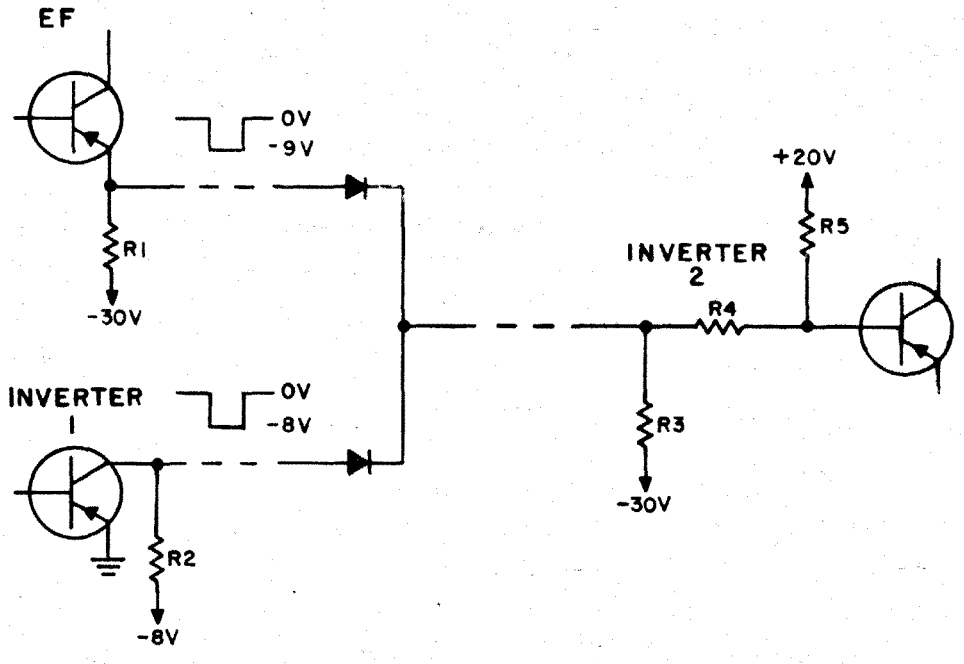


Figure 4-1. Typical "AND" Gate Connection

input potential to the AND gate, the diodes are reverse biased and do not conduct. In effect, no output exists from the AND gate and the inverter transistor is free to conduct.

b. HIGH POWER INVERTER (TYPE A122) ASSEMBLY DWG. NO. 4026362

Circuits per board: 4 identical

Current Ratings:

Input Current: 20.6 ma
Output Current 100 ma -0.285 $\pm$ 0.135 volts

(1) CIRCUIT FUNCTION. - The inverters on this board are used in conjunction with those on board type A103; see paragraph 4-4.

(2) CIRCUIT OPERATION. - The operation of the inverters on this board is explained under Circuit Operation, paragraph 4-4.

c. LOW POWER INVERTER (TYPE A123) ASSEMBLY DWG. NO. 4026365

Circuits per board: 4 identical

Current Rating:

Input Current: 6.42 ma
Output Current: 20.6 ma -0.275 $\pm$ 0.125 volts

(1) CIRCUIT FUNCTION. - The inverters on this board are used in conjunction with those on board type A103 (paragraph 4-4). In addition they provide inversion for the write enable signal.

(2) CIRCUIT OPERATION. - The operation of the inverters on this board is explained under Circuit Operation, paragraph 4-4.

4-4. TIMING AND CONTROL CIRCUITS

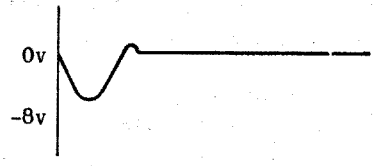
a. PULSE SHAPER-DELAY LINE DRIVER (TYPE A105) ASSEMBLY DWG. NO. 4026315

Circuits per Board: 5

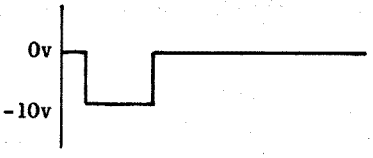
Circuit	Major Component
Single Shot	Q(G7), Q(P6)
Inverter	Q(C7)
Delay Line	
Emitter Follower	Q(S8)

Waveshapes:

Input Waveshape:



Output Waveshape:



(1) CIRCUIT FUNCTION. - The delay line driver is triggered by the leading edge of the clock pulse (PTP2M) received from the processor. The driver generates a -10 volt, 800 nanosecond pulse which is applied to the 4 microsecond memory timing delay line.

(2) CIRCUIT OPERATION. - This printed circuit board contains the pulse shaper delay line driver circuits which consist of a single shot multivibrator (SS), a driver-inverter, and an emitter follower. During standby, the single shot is in the clear 0 state. In the 0 state, transistors Q(G7), Q(P6) (NPN, and Q(C7) are nonconducting. Note that the output from the driver transistor, Q(C7), which is applied to the 0.4 microsecond delay line, is at +20 volts.

The PTP2M pulse received from the processor sets the SS. The 1 output from the SS is positive and is direct coupled to the driver transistor. The driver transistor Q(C7) conducts and the driver output goes to near ground potential. Since the 0.4 microsecond delay line is ac coupled to the +20 volt supply and is referenced at ground, a negative 20 volt wave front is presented to the 0.4 microsecond delay line. Since the 0.4 microsecond delay line is open ended, the -20 volt wavefront travels down the delay line and is reflected back. The time required for the wavefront to travel down the delay line and

back again is 0.8 microsecond which determines the width of the output pulse from the pulse shaper circuit. The amplitude of the output pulse is established at -10 volts since the 0.4 microsecond delay line and the 4 microsecond memory timing delay line have the same characteristic impedance and are connected in series. Thus, a -10 volt, 0.8 microsecond pulse is applied to the memory timing delay line.

During the 0.8 microsecond time interval, the SS remains in the set condition. At approximately 0.9 microsecond after the pulse is applied to the memory timing delay line (not shown on the schematic), a timing pulse is coupled from the memory timing delay line to the SS clear side by the emitter follower circuit, Q(S8). The output pulse from the emitter follower clears the SS, and the pulse shaper-driver circuit returns to the standby condition.

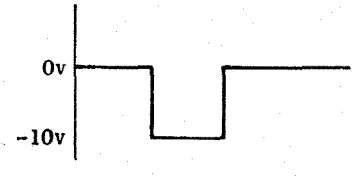
b. DELAY LINE BOARDS (TYPES A100, A120 and A121)
ASSEMBLY DWG. NO'S. 4026300, 4026360 and 4026361

Circuits per board:	Total delay
A100- 32, 50 nanosecond LC networks	1.6 microseconds
A120- 32, 50 nanosecond LC networks	1.6 microseconds
A121- 16, 50 nanosecond LC networks	0.8 microseconds

Current Rating:

Input Current:	100 ma	-10 volts
Output Current	1 ma	-10 volts per tap

Waveshape:



(1) CIRCUIT FUNCTION. - This circuit provides the internal timing and control of the memory, by providing a pulse available at 50 nanosecond intervals from 0 to 4 microseconds.

(2) CIRCUIT OPERATION. - The three delay line sections are connected in series to form one delay line with a total delay of 4.0 microseconds. Taps are available at each 50 nanosecond section. The taps are connected to the

output pins on the board by jumper wires. A preset pattern of jumper wires is connected on each board; this pattern is for nominal times which may require adjustment after the card has been inserted into the memory.

A -10 volt, 800 nanosecond pulse is applied to the delay line input at the beginning of each new memory cycle. As the pulse traverses the delay line, it is delayed by each LC network and is available at the output taps. When utilizing the pulse from the delay line, an emitter follower circuit must be used to couple the pulse to the timing control circuits. The emitter follower prevents excessive loading of the delay line by matching the impedance between the delay line and the timing control circuits.

c. EMITTER FOLLOWER and AND GATE (TYPE A127) ASSEMBLY DWG. NO. 4026377

Circuits per Board: 6

Circuit	Major Component
AND Gate	CR(R9) and CR(S9)
OR Emitter Follower	Q(C7)
Emitter Follower	Q(Q6)
AND Emitter Follower	Q(L7)
OR Emitter Follower	Q(E6)
OR Emitter Follower	Q(J6)

Current Ratings:

Input Current

1) OR input, 1 ma 0.3 volts; 0.54 ma -9 volts
2) AND input, 2 ma 0.3 volts; 0.67 ma -9 volts

Output Current

Diode leakage current only at -9 volts
6.5 ma -0.35 ± 0.65 volts

(1) CIRCUIT FUNCTION. - The emitter followers provide impedance matching between the delay line and the low power inverters used in the timing control of the memory. Three of the emitter followers have OR circuits on the inputs to obtain a timing pulse width greater than 0.8 microsecond. One emitter follower has an AND gate on the input to obtain a timing pulse width less than 0.8 microsecond.

The AND gate on this board is a two diode gate with its inputs and output available at the backboard. This circuit is used in the memory wherever negative AND gate logic is required.

(2) CIRCUIT OPERATION. - The emitter follower has a high input impedance, a low output impedance and a voltage gain of less than 1. The emitter follower transistor is biased for continuous conduction. When a negative pulse is applied to the base, the emitter goes negative. When a positive pulse is applied to the base, the emitter goes positive. Thus the emitter follows the base input.

4-5. ADDRESS SECTION CIRCUITS

a. SELECTOR SWITCH (TYPE A101) ASSEMBLY DWG. NO. 4026303
SELECTOR SWITCH LOAD (TYPE A102) ASSEMBLY DWG. NO. 4026306

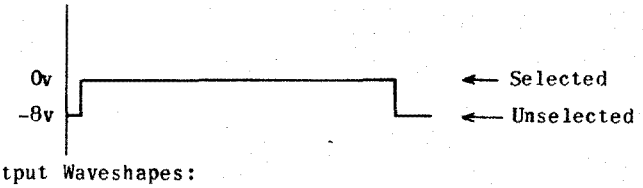
Circuits per Board: A101-3 identical; A102-16 load resistors

Current Ratings:

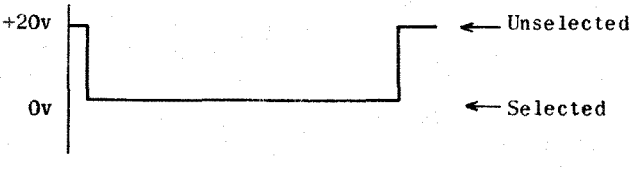
Input current (max):	19 ma	-0.15 to -1.5 volts
Output current (max):	385 ma	-0.15 to -0.75 volts

Waveshapes:

Input Waveshapes:



Output Waveshapes:



(1) CIRCUIT FUNCTION. - The selector switches are controlled by the address information received from the computer. They select one bus transformer and a group of eight line transformers in the selection system for both the X and Y axis. There are 32 selector switches, in four groups of eight switches, used in the memory. One switch from each group is selected at one

time. When address information is received, the selector switch operates the associated selection system transformer by providing a low impedance path to ground for the read/write drive current. In the unselected state the collector supply of the selector switch transistor provides reverse-bias potential to the diodes of the selection system.

When the storage capacity of the memory is increased, selector switch load cards must be added. The load resistors on the load board are paralleled with the collector load resistors of the selector switches; two load resistor cards are required for each core stack utilized. The resistors on the load card, when paralleled with the collector resistors, maintain a constant RC product of the resistors, and the backboard wiring and selection system capacitance. The backboard wiring and selection system capacitance increases as the storage capacity is increased.

(2) CIRCUIT OPERATION. - The selector switch consists of two transistors. The first transistor, Q(S7), is an emitter follower biased such that saturation of the transistor occurs when a negative signal is received at the input. The transistor is reverse-biased when a positive signal is received at the input. When the transistor is conducting, unselected, the output from the emitter is negative. When the transistor is nonconducting, selected, the output from the emitter is positive. The second stage of the switch is an NPN amplifier-switch. When the output from the first stage is negative, the second stage is reverse-biased, nonconducting, and the output from the switch is at +20 volts. The diode in the base circuit of Q(Q6) clamps the base potential at -0.4 volts, the diode drop. When the output from the first stage is positive, the second stage is forward biased and conducts. In this state, the selected state, transistor Q(Q6) presents a low impedance path to ground for the read/write current applied to the selection system.

When in the unselected condition, the collector supply of the switch Q(Q6) must supply charging current for the capacitance in the backboard wiring and in the selection system, plus a sufficient potential to reverse-bias the diodes in the unselected transformer circuits. When one stack is used, the collector supply and one load source is sufficient to supply this charging current. However, when more than one stack is used, the collector supply and one load source are not sufficient to charge the capacitance in the required time. Thus an additional current source is necessary. For each stack added, one selector switch load circuit is paralleled with each collector supply.

The load resistors maintain a constant R.C. product consisting of the load resistors, and the backboard and selection system capacitance.

b. TRANSFORMER-DIODE MODULE (TYPE A118 and A119) ASSEMBLY DWG. NO. 4026354 AND 4026357 SCHEMATIC DWG. NO. 4026404

Module components: 1 bus transformer; 8 line transformers

Component:

T1	Bus Transformers
T2-T9	Line Transformers

(1) CIRCUIT FUNCTION. - The transformer-diode modules are used to select the X and Y drive lines of the core stack, and to provide a path for the read/write drive current. Eight modules are used to select the X drive lines and eight are used to select the Y drive lines.

(2) CIRCUIT OPERATION. - Eight transformer-diode modules are mounted on one printed circuit board. One such printed circuit board (type 118) provides the X selection and a second such board (type A119) provides the Y selection. The inputs to the primary of the bus transformers of all eight modules are connected in parallel; i.e., pin P01 of all modules is connected by printed wiring and is available at one of the jack pins of the board; the same is true of P02. Pin P04 on each module has a separate connection. The centertap connection on the line transformers are connected in parallel with the corresponding transformer in each module; e.g., pin P06 of all line transformers is connected in parallel by the printed circuit wiring and is available at a jack pin. One side of the secondary from each line transformer has a separate drive line connection. The other side of the secondary from all line transformers is connected to ground.

The read drive current is applied to pin P01 of all X bus transformers simultaneously, at the proper time, and the write drive current is applied to pin P02 of all X but transformers simultaneously, at the proper time. The return path for either the read or write currents is through pin P04 which is connected to a selector switch circuit. One output from a line transformer is obtained when the selector switch associated with the transformer centertap is operated. The operation of the selector switch applies a low impedance path to ground for the transformer. The read current and write current connections to the Y selection board are the reverse of that for the X selection board.

When read drive current is presented at pin P01, diode CR1 is forward biased and conducts. The drive current is presented to one half the primary of the bus transformer. The output from the secondary of the bus transformer

is diode coupled to all line transformers associated with the bus transformer. If ground is applied to one line transformer centertap, the read current causes conduction of the coupling diode and the current flows through the primary of that transformer. The output from the line transformer is applied to the associated drive winding of the core stack.

The input diodes to the bus transformer and line transformer primaries serve as isolation diodes. The diodes in the line transformer inputs are reverse biased when the selector switch is unselected. The diodes in the primary of the bus transformer prevent the read current from feeding into the write driver and vice-versa.

4-6. DRIVER CIRCUITS

a. READ/WRITE CURRENT PULSE (GENERATOR). - This circuit is packaged on three card types; for a composite schematic refer to figure 4-2.

READ/WRITE DRIVER (TYPE A113) ASSEMBLY DWG. NO. 4026339
READ/WRITE DIVERTER (TYPE A114) ASSEMBLY DWG. NO. 4026342
POWER RESISTOR (TYPE A115) ASSEMBLY DWG. NO. 4026345

Circuits per Board: 2

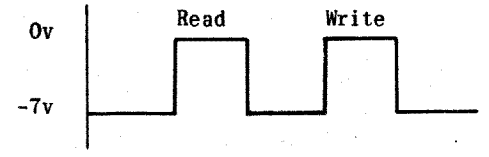
A113 Circuit	Major Component
Read Driver	Q(G7) and Q(L7)
Write Driver	Q(E6) and Q(S7)
A114	
Read Diverter	Q(C7) and Q(Q6)
Write Diverter	Q(G7(and Q(L7)
A115	
Circuit	Major Component
Read Driver Power Resistor network	L(L3) and L(M8)
Write Driver Power Resistor network	L(H6) and L(H11)

Current Rating, composite circuit:

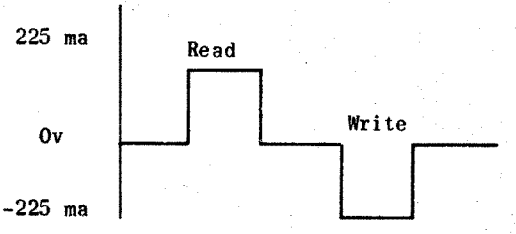
Input Current: 19.85 ma +0 to -0.6 volts
Output Current: 290 ma nominal vary from 260 ma to 320 ma

Waveshapes:

Input Waveshapes:



Output Waveshapes:



(1) CIRCUIT FUNCTION. - The current generator supplies the read and the write driving currents necessary to operate or switch the selected cores of the core stack. Each generator supplies both the X and the Y driving currents to one seven-plane core stack.

(2) CIRCUIT OPERATION. - Figure 4-2 is a schematic diagram of the read current pulse generator. When in the standby condition (no current supplied to the core stack), transistors Q1, Q3 and Q4 are nonconducting and Q2 is conducting. With Q2 conducting, the current through L2 and L3 is at maximum.

When a positive pulse is received at the input to Q1, the base-emitter junction is forward-biased and the transistor conducts. The conduction of Q1 applies a negative going pulse from +V regulated to ground to the base of Q2, reverse-biasing the base-emitter junction and the transistor is cut off. The potential across L3 reverses, applying a negative potential to the emitter of Q4. At the same time, the read diverter enable and US signals go positive and forward-bias the base-emitter junction of Q3. Q3 conducts and the base-emitter junction of Q4 is forward-biased and the transistor conducts. The conduction of Q4 diverts the current flowing through L2, to the primary of the output transformers. At the instant of conduction of Q4, the current

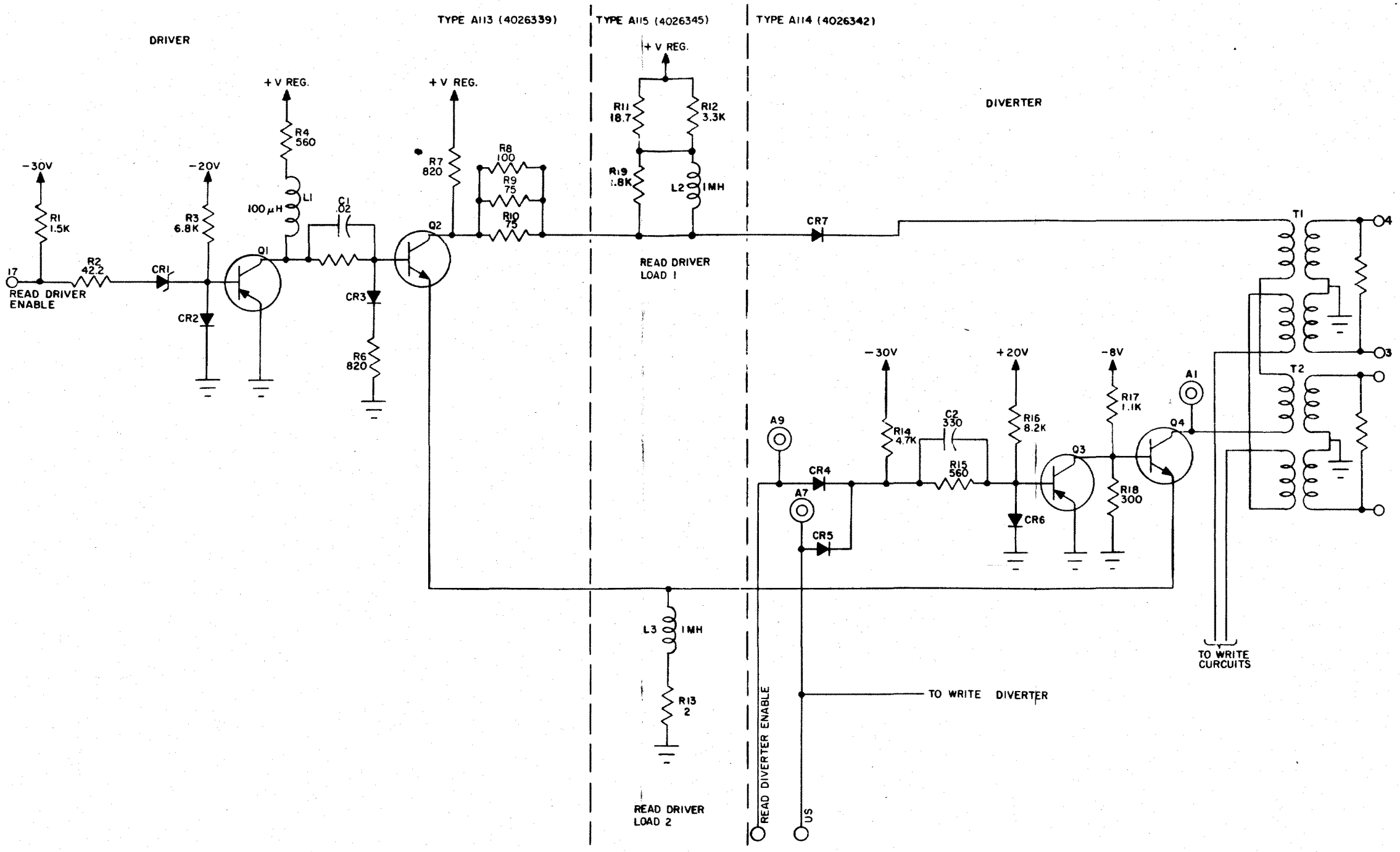


Figure 4-2. Read Current Pulse Generator

buildup in L2 provides a positive voltage spike to the primary of the output transformers which serves to bring the current level within the primary winding to maximum, decreasing the rise time of the output current pulse.

The output from the generator stays at a relatively constant level until a negative level is received at the input to Q1. When the input to Q1 goes negative, the base-emitter junction is reverse-biased and the transistor is cut off. The potential across L1 aids in forward-biasing the base-emitter circuit of Q2. Q2 conducts; inductor L2 applies a negative voltage spike to the primary of the output transformers and brings the current level to standby level, decreasing the fall time of the output current pulse. The current flow through L3 due to conduction of Q2 is sufficient to apply a positive potential to the emitter of Q4. The read diverter enable and US signals subsides cutting Q4 off, and the generator returns to the standby condition.

The operation of the write current generator is identical to that of the read current generator.

The current output from the generators varies with the(+ V Reg) voltage regulator output which is temperature controlled. Figure 4-3 shows the voltage regulator output vs temperature and current output vs + V Reg.

b. INHIBIT DRIVER (TYPE A107) ASSEMBLY DWG. NO. 4026321

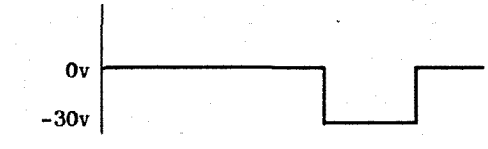
Circuits per board: 2 identical

Current Rating:

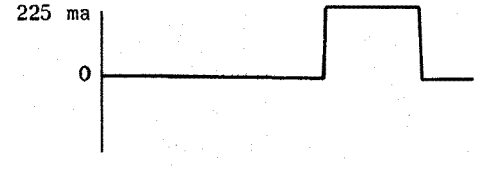
Output Current: 225 ma

Waveshapes:

Input Waveshapes:



Output Waveshapes:



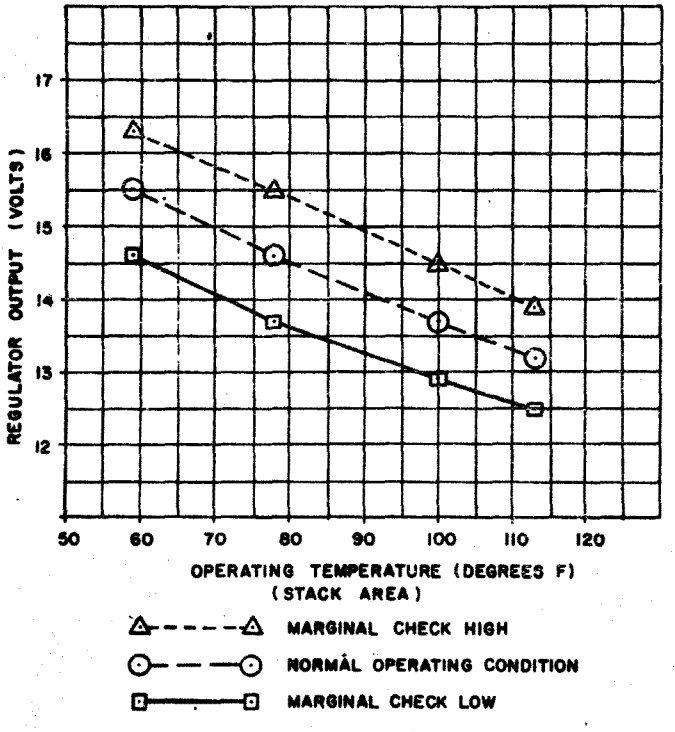


Figure 4-3a. Voltage Regulator Output vs Temperature

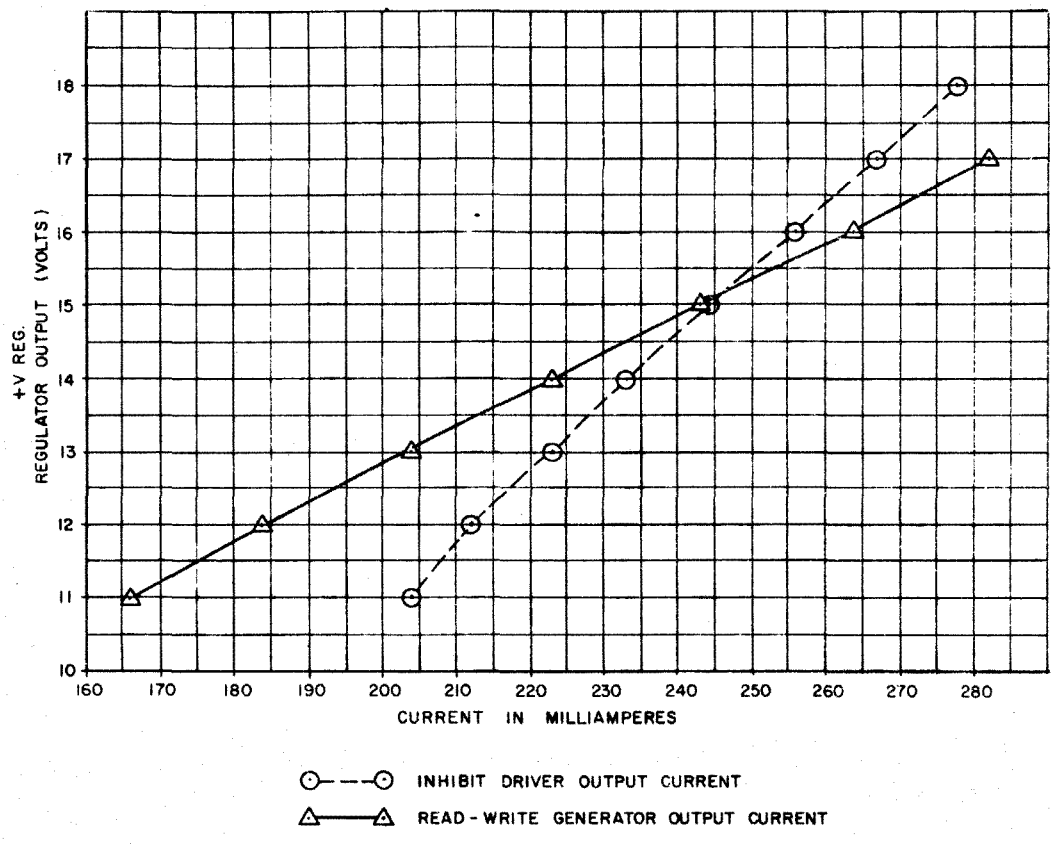


Figure 4-3b. Read/Write and Inhibit Current vs +V Reg

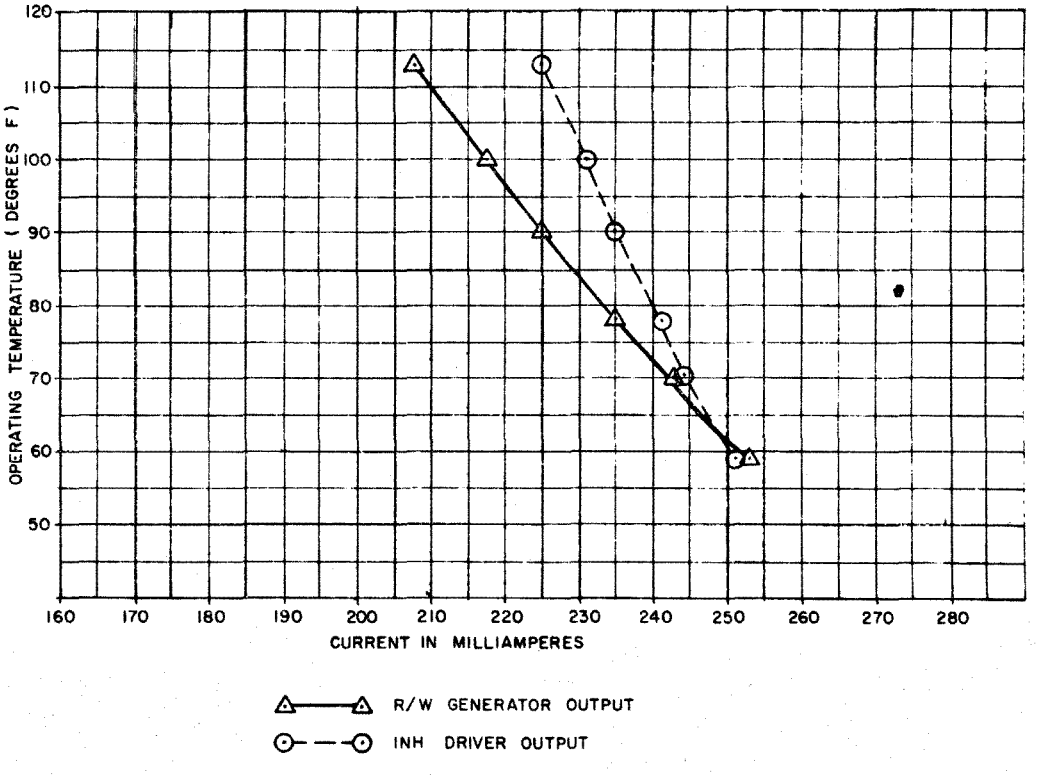


Figure 4-3c. Read/Write and Inhibit Current vs Temperature

(1) CIRCUIT FUNCTION. - The inhibit driver supplies the current necessary to cancel the effect of the Y write drive current at the core in which a 0 is to be stored. The driver output is connected to the inhibit line of one core plane within a stack.

(2) CIRCUIT OPERATION. - When the inhibit enable is received on pin 15, the input information pulse is received on pin 14 and the stack select pulse is received on pin 13 of the input AND gate to the inhibit driver; the base of Q(H7) is forward-biased and the transistor conducts. The condition of Q(H7) supplies a forward-biasing current to the base-emitter junction of Q(D7) and this transistor conducts. When Q(D7) conducts, conventional current flows from the +V regulated source through the parallel resistors and capacitor, through the primary of the transformer, through the inhibit winding of the core plane, through the secondary of the transformer, and through the collector-emitter of transistor Q(D7) to the -8 volt source. The primary and secondary of the transformer are connected in series with the inhibit winding. The transformer prevents noise pulses from entering the inhibit line. If a noise pulse is applied to one winding of the transformer it is induced into the second winding, in phase, and the resulting current flow through the inhibit winding due to the noise pulse is reduced to 0.

When any one or all the signals at the input AND circuit go positive, transistor Q(H7) is cut off, and supplies a reverse-biasing potential to the base of Q(D7). Q(D7) is cut off and the inhibit drive current is stopped.

4-7. AMPLIFIER CIRCUITS

a. PREAMPLIFIER (TYPE A151) DWG. NO. 4026437

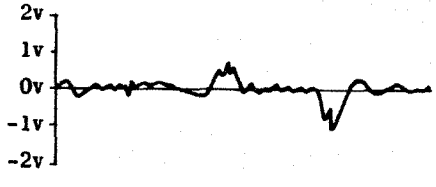
Circuits per board: 4

Circuits:

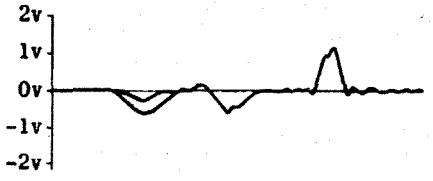
Preamplifier; Class A	Q(L7)
Preamplifier; Class A	Q(N6)
Preamplifier; Class A	Q(S7)
Preamplifier; Class A	Q(Q6)

Waveshapes:

Input Waveshape:



Output Waveshape:



(1) CIRCUIT FUNCTION. - The preamplifier acts as a buffer stage between one sense winding and the associated sense amplifier. The outputs from a maximum of eight preamplifiers, two groups of four preamplifiers, one connected to a core plane from each core stack, can by bussed together and applied to the input to one sense amplifier. Small data signals are amplified, and large noise signals are attenuated by the preamplifier. The common mode noise signals from the sense winding, because of the interwire capacitance between the sense winding and the inhibit winding, are cancelled by the input transformer to the preamplifier.

(2) CIRCUIT OPERATION. - The preamplifier operates as a class A amplifier for the data signals received from the sense winding and is biased to clip the bipolar noise signals. When a positive going noise pulse is received at the input to transistor Q(L7), the emitter follows the base positive. The emitter continues to go positive until it reaches the unloaded ac voltage value of the emitter biasing network (approximately 0.7 volt positive). If the input noise continues positive above this value, the transistor is reverse-biased and is cut off. Thus, the output from the preamplifier goes from approximately -7 volts during class A standby to approximately -9 volts with a large positive noise signal applied to the input.

When a negative noise pulse is received at the input of the preamplifier transistor, the emitter goes negative. As the emitter goes negative, a negative pulse is RC coupled to and reverse biases diode CR(L2) in the emitter biasing circuit. When the diode is reverse biased to cut off, the emitter current for Q(L7) must be supplied through R(F2) and R(H2) in parallel. Since the parallel resistance of the two resistors is much larger than that of R(J2) and CR(L2) in series, the amplification of the preamplifier transistor is reduced from 1.42 to 0.04. The output from the preamplifier is thus limited when a large negative noise pulse is applied to the input.

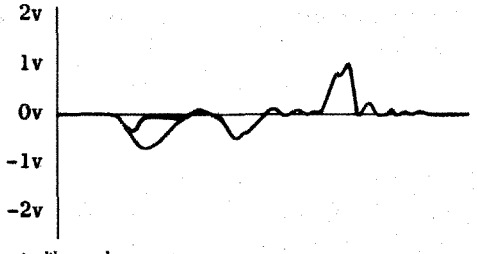
b. SENSE AMPLIFIER (TYPE A154) ASSEMBLY DWG. NO. 4026338
SENSE AMPLIFIER LOAD (TYPE A133) ASSEMBLY DWG. NO. 4026399

Circuits per Board: A112 a1

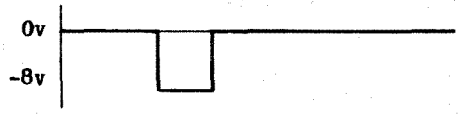
Class A Amplifier	Q(S7) and Q(Q6)
Phase Inverter	Q(L8)
Class C Amplifier	Q(D6)
Class C Amplifier	Q(C7)

Waveshapes:

Input Waveshapes:



Output Waveshapes:



(1) CIRCUIT FUNCTION. - The sense amplifier receives the amplified core outputs from one to eight preamplifiers, amplifies the signal, distinguishes between 0's and 1's, stretches the signal to provide for strobing and transfers the information to the processor.

(2) CIRCUIT OPERATION. - The class A amplifier, transistor Q(TU7,8) amplifies the bipolar pulses received from the preamplifier. The output from Q(TU7,8) is transformer coupled to the input of the differential amplifier, Q(F7) and Q(QR7,8). When the input to the class A amplifier goes negative, the transistor conducts more, thereby increasing the voltage drop across the primary of transformer T(R3). This increase in voltage is coupled to the secondary of the transformer appearing positive at pin 3 and negative at pin 6 of the secondary. The positive potential at pin 3 is applied to the base of transistor Q(F7) decreasing the conduction of the transistor. This decrease in conduction decreases the voltage drop across resistor R(C7) and a negative pulse is capacitor coupled C(D4), to the junction of diodes CR(F10) and CR(G10).

The negative pulse forward biases diode CR(G10) and is bypassed to ground by the diode.

The negative potential at pin 6 of transformer T(R3) is applied to the base of transistor Q(QR7,8). The transistor conducts more increasing the voltage drop across R(B10) and a positive pulse is capacitor coupled, C(D9), to the junction of diodes CR(J13) and CR(L13). The positive pulse forward biases diode CR(J13) and is applied to the base of transistor Q(H8) reverse biasing the transistor to cutoff. When the negative strobe pulse is received from the timing and control section on pin 17, the AND gate consisting of CR(Q13) and CR(L9) is satisfied and a negative pulse is available at the output, pin 15.

The output at pin 15, in addition to being available to the processor, is also diode coupled by CR(P6), to the base circuit of feedback amplifier, Q(M8). The negative pulse forward biases the transistor; the transistor conducts and a positive going pulse (from -8 volts to ground) is capacitor coupled to the base circuit of Q(H8). The effect of this feedback pulse is to stretch the output pulse to allow for strobing of the seven sense amplifier outputs. This is necessary due to the variation in circuit parameters.

The input circuit of the class A amplifier is designed to operate with an input load impedance obtained when eight preamplifiers are connected at the input. When only four preamplifiers are used, a load resistor (type A133) must be connected to input pin 1 of the sense amplifier.

4-8. VOLTAGE REGULATION CIRCUITS

a. VOLTAGE REGULATOR (TYPE A116) ASSEMBLY DWG. NO. 4026348
VOLTAGE REGULATOR HEAT SINK (TYPE A117) ASSEMBLY DWG. NO. 4026351
TEMPERATURE CONTROL (TYPE A140) ASSEMBLY DWG. NO. 4026420

Circuits per Board: 1

Voltage Ratings:

Input Voltage: +20 volts unregulated

Output Voltage: Regulated output variable from 13.6 volts to +15.4 volts. See figure 4-3a.

(1) CIRCUIT FUNCTION. - The voltage regulator supplies a temperature compensated voltage to the read/write current pulse generators and to the inhibit drivers. The variable voltage is derived from the +20 volt unregulated dc supply. The output from the circuit is regulated to ±1 percent.

(2) CIRCUIT OPERATION. - The output from the voltage regulator varies inversely with the temperature of the core stack area. This characteristic is obtained by using a temperature sensitive resistor (Sensistor*) in the feedback circuit of the voltage regulator. As the temperature in the core stack area increases, the resistance of the Sensistor increases and controls the voltage regulator such that the output from the regulator decreases. The Sensistor is physically located on a printed circuit board in the center of the core stack area.

The voltage regulator is a series type voltage regulator utilizing a tetrode transistor, (Q(Pin 17), as the control transistor. A fixed reverse-bias is developed from the unregulated 20 volt source by inductor L(P4) and is applied to base 2 of Q(Pin 17). The reverse-bias supplies the leakage current for conduction of Q(J5). Since Q(Pin 17) is a tetrode, this leakage current is not amplified by Q(Pin 17). Transistors Q(J5) and Q(C7) are DC amplifiers which supply the regulating feedback to base 1 of Q(Pin 17). Since the transistors are biased for conduction at all times, the level of conduction of Q(Pin 17) determines the output from the circuit, while the level of conduction of Q(J5) and Q(C7) determines the level of conduction of Q(Pin 17). Zener diode CR(C3) supplies the reference voltage for dc amplifier Q(C7). The level of conduction of Q(C7) determined by the voltage divider network of the Sensistor, and resistors R(B,C2), R(B3) and R(B10), compared with the reference voltage. The level of conduction of Q(J5) is determined by the voltage divider network consisting of R(M2), R(E3), and the collector-emitter voltage drop of Q(C7), and resistor R(C10). The level of conduction of Q(J5) determines the potential applied to base 1 of Q(Pin 17). Switches S1 and S2 control the high, normal, or low output from the regulator. High voltage output is obtained when both switches are open; normal output is obtained when S1 is open and S2 is closed; low output is obtained when both switches are closed.

*A trademark of Texas Instrument Inc.

Resistor R(V6) provides increased regulation under full load conditions by increasing the base-emitter potential of Q(C7) above what it is for low load. Capacitor C(V8) provides filtering of the output. Capacitor C(S7) and resistor R(Q10) provide a path for base current during turn-on of Q(pin 17).

b. SENSE BIAS VOLTAGE REGULATOR (TYPE A153) DWG. NO. 4026442

Circuits per Board: 1

Voltage Ratings:

Input Voltage: -30 volts

Output Voltage: Regulated output variable from -23.5 volts to -24.5 volts.

(1) CIRCUIT FUNCTION. - The sense bias voltage regulator supplies the regulated -24 volts necessary for proper biasing of the sense amplifiers.

(2) CIRCUIT OPERATION. - The operation of the sense bias regulator is similar to the temperature compensated voltage regulator described under paragraph 4-8,a. However since the temperature compensating requirements are not needed, the Sensistor is replaced by a common fixed resistor. The regulator is a series type voltage regulator with transistor Q(M10) as the regulating transistor. Only one feedback control amplifier, Q(D7) is required compared to two amplifiers in type A116. Zener diode CR V10 supplies a constant emitter-bias reference for transistor Q(D7). The feedback control voltage is developed from the voltage divider network formed by R(V2), R(B,C2,3) and R(T1). The voltage divider controls the base-bias to Q(D7). The level of conduction of Q(D7) controls the level of conduction of Q(M10) which controls the output from the circuit. The output from the regulator circuit may be adjusted by potentiometer R(B,C2,3). The regulator is adjusted to produce -24 volts at the output when the memory leaves the factory. No further adjustment is required.

SECTION 5

MAINTENANCE PROCEDURES

5-1. GENERAL

This section of the manual describes the preventive maintenance, routine checks, and troubleshooting procedures.

5-2. PREVENTIVE MAINTENANCE

Preventive maintenance of the core memory is accomplished by running diagnostic or maintenance routines on the computer. The results of these programs indicate developing weak points within the memory. Refer to the processor manual for information on the diagnostic or maintenance routine programs.

5-3. ROUTINE CHECKS

Because of the simplicity of the memory unit and the fact that the memory is mounted in the processor cabinet, the only routine checks necessary are the periodic checks of the voltages received from the processor and of the output from the voltage regulator. Table 5-1 lists the voltage check points and the voltage values.

TABLE 5-1. VOLTAGE CHECKS

VOLTAGE	TERMINAL OR TEST POINT
+20 ground -8 -30	Refer to figure 5-1
+V Reg (14.6 Volts @ 78°F)	A6 (B49)

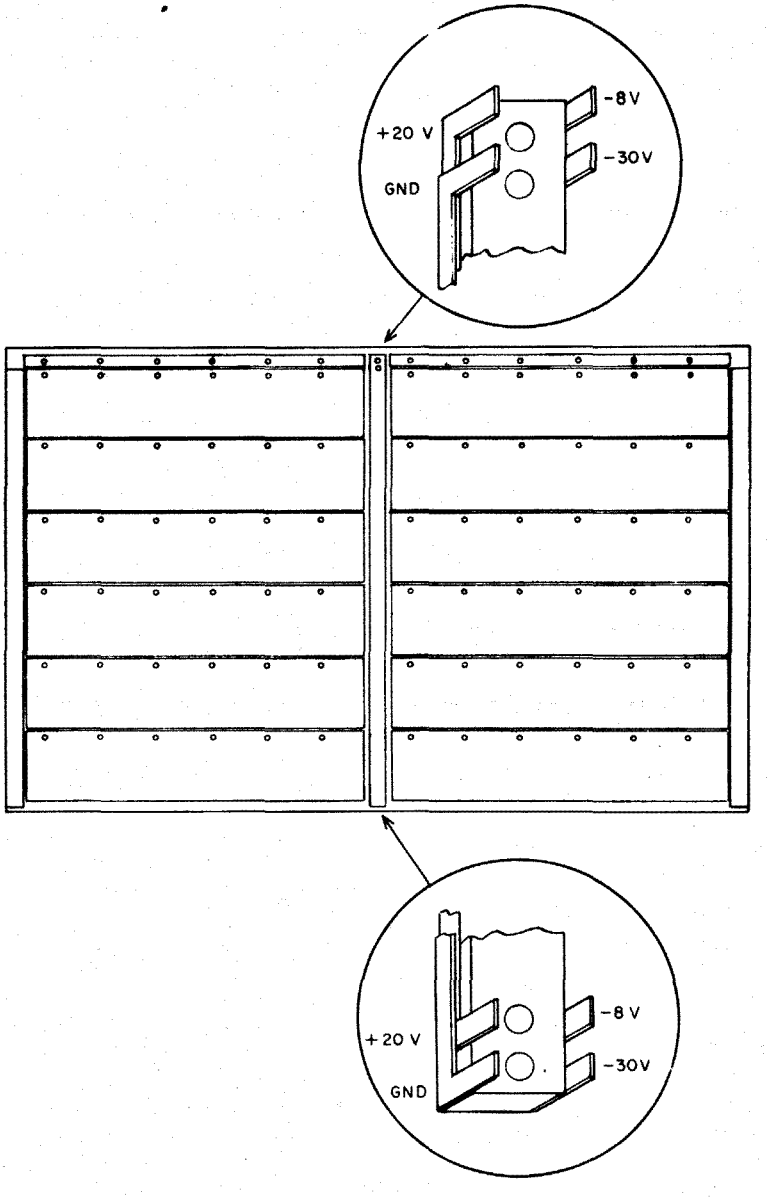


Figure 5-1. Rear View of Memory (Showing Voltage Terminals)

5-4. TROUBLESHOOTING PROCEDURE

In most cases a trouble area within the memory may be located by running a diagnostic routine on the processor and observing the bit(s) failure on the processor indicator panel. When the bit location and the addressed stack have been established, the easiest method of determining which individual circuit has failed is to observe, with the oscilloscope, the outputs from the circuits associated with the failing bit(s). In this manner the trouble may be traced to the circuit or circuits that have failed.

5-5. ADJUSTMENT PROCEDURE

The only adjustment made internal to the memory is the adjustment of the potentiometer on the +V Reg voltage regulator board. The potentiometer is used to control the output from the voltage regulator by varying the fixed bias applied to the feedback network transistor. To adjust the output from the voltage regulator to the value given in table 5-1, vary the adjustable potentiometer on the voltage regulator board (figure 5-2). There are two switches on the processor test panel which also control the output from the voltage regulator. For normal operation switch S1 is open and switch S2 is closed. For marginal testing purposes the switches may be operated to obtain high or low voltage output from the regulator as described under paragraph 5-6. .

5-6. MARGINAL-CHECKING

Marginal checking of the memory circuits is provided for in the memory. The operation of switches S1 and S2 located on the processor test panel controls the output voltage from the voltage regulator (+V Reg). The regulator output controls the current output from the read/write current generators and the inhibit drivers. Table 5-2 presents the circuits checked under high and low marginal testing conditions. The information in the symptom and probable cause column is based on the assumption that the memory operates properly under normal conditions. Refer to figure 4-3 for actual voltage values of the voltage regulator output for high, normal, and low conditions.

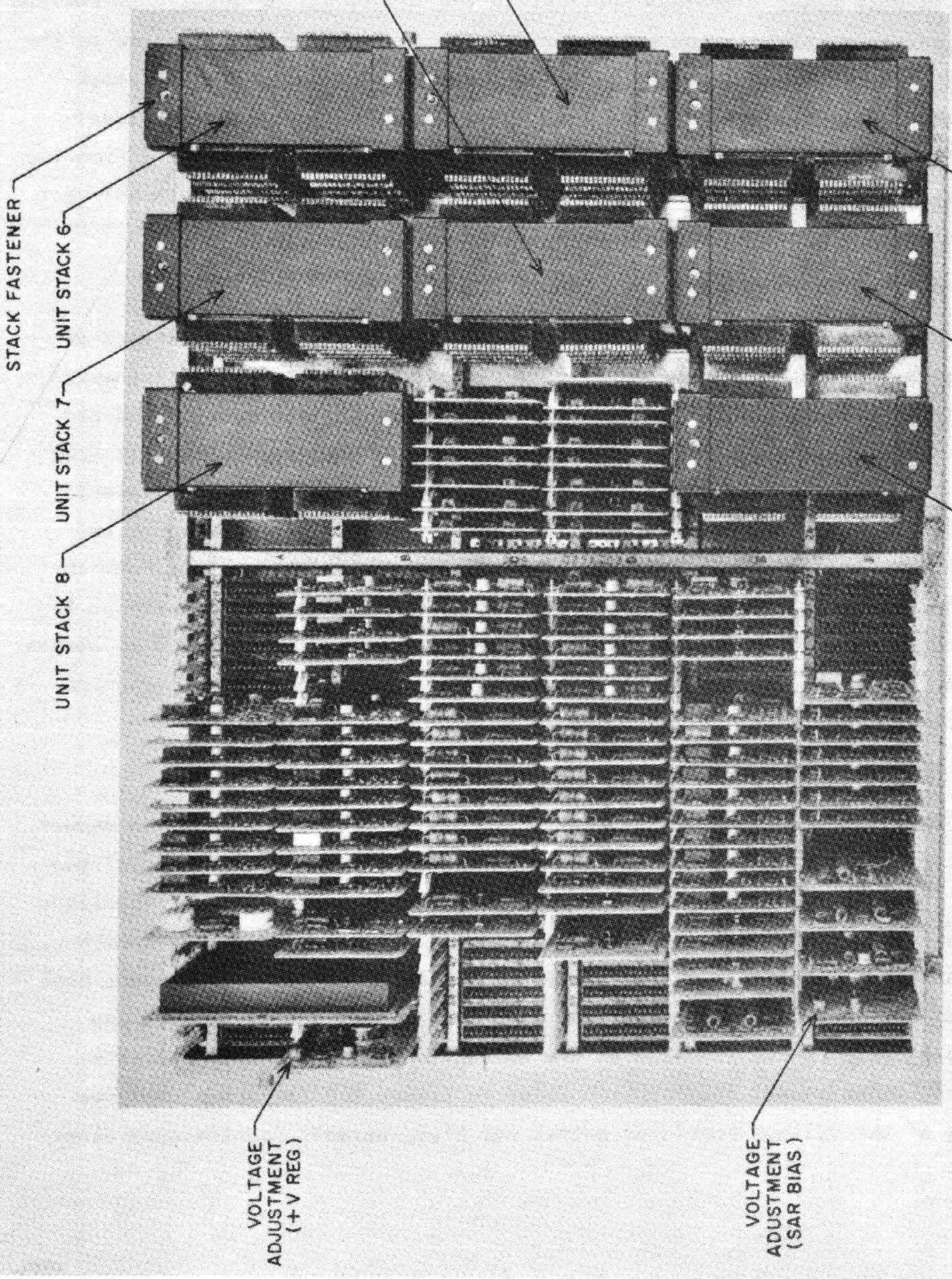


Figure 5-2. M2-32 Core Memory

TABLE 5-2. MARGINAL TESTING PROCEDURES

Switch Position S1	Switch Position S2	Regulator Output	Current Driver Output	Symptom	Probable Cause
Open	Open	High	High	Pick Up 1's on Read	1a. Preamplifier clipping circuit inoperative allowing saturation of Sense amplifiers by noise pulses. b. Strobe timing fast.
				Drop 1's on Read or Write	2. Selector Switch not saturated presenting high impedance to Read/Write drive current.
Closed	Closed	Low	Low	Drop 1's on Read	1a. Read/Write current generator output too low. b. Weak Preamplifier c. Weak Sense Amplifier d. Strobe timing slow.
				Pick Up 1's on Read	2. Strobe timing is fast allowing noise pulses to be strobed out.
				On Write	3a. Inhibit driver current output low. b. Inhibit timing slow or write timing fast.
Open	Closed	Normal	Normal	None	None

SECTION 6

REMOVAL AND REPLACEMENT PROCEDURE

The core stacks in the memory are plug-in units which can be removed and replaced with another core stack. To remove the core stack, loosen stack fastener on top of stack (figure 5-1); grasp both ends of the stack frame, and pull in a direction perpendicular to the cast frame. Extreme care must be exercised to ensure that equal force is applied to both selection boards or the printed circuit board may crack.

Replacement procedure of the core stack is the reverse of the removal procedure; however, be certain that the plugs on the selection boards are properly inserted into the connectors. Also, equal pressure must be applied to both selection boards when pushing the plugs into the connectors. Secure stack to the frame by tightening the stack fastener.

SECTION 7

PARTS LIST

7-1. GENERAL

This parts list illustrates and identifies units,, assemblies, and detail parts of Types 9150-03 through 9150-10 Memory Units, manufactured by UNIVAC, Division of Sperry Rand Corporation, UNIVAC Park, St. Paul 16, Minnesota.

The parts list should not be used for disassembly or assembly procedures. Maintenance, overhaul, or repair should be performed by authorized personnel using the applicable maintenance, service, or overhaul instructions.

The Table of Contents lists the units and assemblies covered and the page number where the breakdown for each may be found.

The parts breakdown consists of illustrations, where necessary, and listings of units, assemblies, and parts.

7-2. FIGURE AND INDEX NUMBER COLUMN

This column reflects a figure number assigned to a particular unit or assembly, and index numbers which reference illustrated parts or subassemblies to the corresponding descriptions in the table. The term figure in this column heading implies a pictorial presentation of the unit or assembly only when deemed necessary for clarification.

7-3. REFERENCE DESIGNATION COLUMN

This column lists the reference designations assigned to parts and assemblies. All reference designations are marked on the actual equipment.

7-4. UNIVAC PART NUMBER COLUMN

This column lists UNIVAC part numbers exclusively. A "No Number" entry in this column is used to indicate a grouping of parts, which are electrically and/or mechanically related, but which cannot be purchased as such.

The parts of subject groups can only be procured by their individual part numbers. Part numbers preceded by an asterisk (*) are physically

related to their next higher assembly, as indicated; however, these parts are not included in the next higher assembly for the purpose of procurement and must be purchased by their individual part numbers.

7-5. DESCRIPTION COLUMN

This column lists the basic item name followed by descriptions which will assist in identifying a unit, assembly, or part. Indenture levels, indicated by numerals 1 through 7 establish a distinct parts relationship. All parts can be purchased independently or by next higher assemblies, as indicated by indenture level, with the exception of parts preceded by an asterisk (*) in the UNIVAC Part Number column (paragraph 7-4).

7-6. UNITS PER ASSEMBLY COLUMN

This column indicates the quantity of parts in a particular unit or assembly. If the equipment contains two or more identical assemblies, this column will indicate the quantity of parts for one assembly only. The entry "AR" (as required) indicates that a part must be procured by part number and specifics, such as length and bulk quantities. A "Ref" entry in this column indicates that subject assembly has previously been identified.

7-7. USABLE ON CODE COLUMN

This column has not been employed in the parts list for subject equipment.

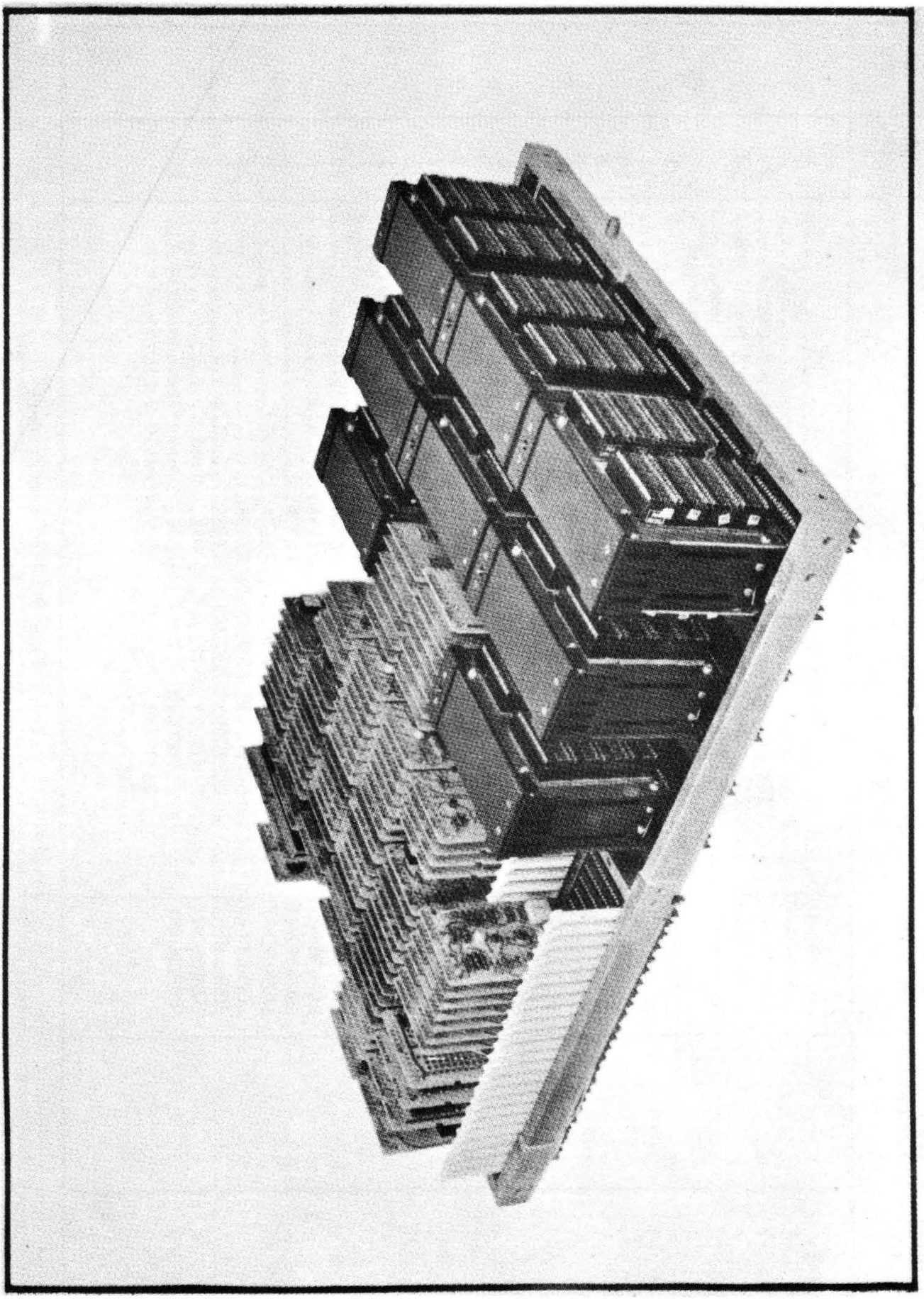


Figure 7-1. M2-32 X-Line MEMORY Unit

FIG. AND INDEX NO.	REFERENCE DESIGNATION	UNIVAC PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY.	USABLE ON CODE
7-1-		4026000-10	MEMORY UNIT (TYPE 9150-10).....	1	
-1		4026097-00	. FRAME ASSY, Wired.....	1	
-2		4026086-00	. GUIDE, Electronic circuit plug-in unit, 8 positions..	23	
		4026086-01	. GUIDE, Electronic circuit plug-in unit, 2 positions..	2	
-3		No Number	. COMPLEMENT, Electronic circuit plug-in unit(see..... System Diagram Manual for detail breakdown)		
		4026300-00	. . COMPONENT ASSEMBLY, A100A.....	1	
		4026303-00	. . COMPONENT ASSEMBLY, A101B.....	11	
		4026306-00	. . COMPONENT ASSEMBLY, A102A.....	16	
		4026309-00	. . COMPONENT ASSEMBLY, A103A.....	2	
		4026315-00	. . COMPONENT ASSEMBLY, A105A.....	1	
		4026321-00	. . INHIBIT DRIVER, A107B.....	28	
		4026338-00	. . SENSE AMPLIFIER, A154A.....	7	
		4026339-00	. . COMPONENT ASSEMBLY, A113B.....	1	
		4026342-00	. . COMPONENT ASSEMBLY, A114C.....	8	
		4026345-00	. . COMPONENT ASSEMBLY, A115B.....	1	
		4026348-00	. . COMPONENT ASSEMBLY, A116B.....	1	
		4026351-00	. . V. R. POWER TRANSISTOR AND HEAT SINK, A117A.....	1	
		4026360-00	. . COMPONENT ASSEMBLY, A120A.....	1	
		4026361-00	. . COMPONENT ASSEMBLY, A121A.....	1	
		4026362-00	. . COMPONENT ASSEMBLY, A122A.....	5	
		4026365-00	. . COMPONENT ASSEMBLY, A123A.....	3	
		4026377-00	. . COMPONENT ASSEMBLY, A127A.....	1	
		4026420-00	. . COMPONENT ASSEMBLY, A140A.....	1	
		4026437-00	. . COMPONENT ASSEMBLY, A151A.....	14	
		4026442-00	. . COMPONENT ASSEMBLY, A153A.....	1	
-4		4026050-00	. CORE MEMORY UNIT, 4K, 7 bit, wired.....	8	
-5		907804-00	. SEMICONDUCTOR DEVICE, Diode, Sperry Semiconductor.... Division, Type 2681 or Fairchild Semiconductor. Corp., Type FD 377	AR	

Figure 7-1(Cont.). Type 9150-10 Memory Unit

FIG. AND INDEX NO.	REFERENCE DESIGNATION	UNIVAC PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY.	USABLE ON CODE
7-2		4026000-09	MEMORY UNIT (TYPE 9150-9)..... Type 9150-9 Memory Unit is the same as Type 9150-10 (Figure 7-1) with the following exceptions: 1. 4026050-00 4K Core Memory Unit, qty 7 used instead of 8 2. 4026306-00 COMPONENT ASSEMBLY, qty 14 used instead of 16 3. 4026321-00 INHIBIT DRIVER, qty 25 used instead of 28 4. 4026342-00 COMPONENT ASSEMBLY, qty 7 used instead of 8	1	

Figure 7-2. Type 9150-9 Memory Unit

FIG. AND INDEX NO.	REFERENCE DESIGNATION	UNIVAC PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY.	USABLE ON CODE
7-3		4026000-08	MEMORY UNIT (TYPE 9150-8)..... Type 9150-8 Memory Unit is the same as Type 9150-10 (Figure 7-1) with the following exceptions: 1. 4026050-00 4K Core Memory Unit, qty 6 used instead of 8 2. 4026306-00 COMPONENT ASSEMBLY, qty 12 used instead of 16 3. 4026321-00 INHIBIT DRIVER, qty 21 used instead of 28 4. 4026342-00 COMPONENT ASSEMBLY, qty 6 used instead of 8 5. 4026362-00 COMPONENT ASSEMBLY, qty 4 used instead of 5	1	

Figure 7-3. Type 9150-8 Memory Unit

FIG. AND INDEX NO.	REFERENCE DESIGNATION	UNIVAC PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY.	USABLE ON CODE
7-4		4026000-07	MEMORY UNIT (TYPE 9150-7)..... Type 9150-7 Memory Unit is the same as Type 9150-10 (Figure 7-1) with the following exceptions: 1. 4026050-00 4K Core Memory Unit, qty 5 used instead of 8 2. 4026306-00 COMPONENT ASSEMBLY, qty 10 used instead of 16 3. 4026321-00 INHIBIT DRIVER, qty 18 used instead of 28 4. 4026342-00 COMPONENT ASSEMBLY, qty 5 used instead of 8 5. 4026362-00 COMPONENT ASSEMBLY, qty 4 used instead of 5	1	

Figure 7-4. Type 9150-7 Memory Unit

FIG. AND INDEX NO.	REFERENCE DESIGNATION	UNIVAC PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY.	USABLE ON CODE
7-5		4026000-06	MEMORY UNIT (TYPE 9150-6)..... Type 9150-6 Memory Unit is the same as Type 9150-10 (Figure 7-1) with the following exceptions: 1. 4026050-00 4K Core Memory Unit, qty 4 used instead of 8 2. 4026306-00 COMPONENT ASSEMBLY, qty 8 used instead of 16 3. 4026321-00 INHIBIT DRIVER, qty 14 used instead of 28 4. 4026342-00 COMPONENT ASSEMBLY, qty 4 used instead of 8 5. 4026362-00 COMPONENT ASSEMBLY, qty 4 used instead of 5 6. Add 4026399-00 COMPONENT ASSEMBLY, A133B1, qty 1 used 7. 4026437-00 COMPONENT ASSEMBLY, qty 7 used instead of 14	1	

Figure 7-5. Type 9150-6 Memory Unit

FIG. AND INDEX NO.	REFERENCE DESIGNATION	UNIVAC PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY.	USABLE ON CODE
7-6		4026000-05	MEMORY UNIT (TYPE 9150-5)..... Type 9150-5 Memory Unit is the same as Type 9150-10 (Figure 7-1) with the following exceptions: 1. 4026050-00 4K Core Memory Unit, qty 3 used instead of 8 2. 4026306-00 COMPONENT ASSEMBLY, qty 6 used instead of 16 3. 4026321-00 INHIBIT DRIVER, qty 11 used instead of 28 4. 4026342-00 COMPONENT ASSEMBLY, qty 3 used instead of 8 5. 4026362-00 COMPONENT ASSEMBLY, qty 3 used instead of 5 6. Add 4026399-00 COMPONENT ASSEMBLY, A133B1, qty 1 used 7. 4026437-00 COMPONENT ASSEMBLY, qty 7 used instead of 14	1	

Figure 7-6. Type 9150-5 Memory Unit

FIG. AND INDEX NO.	REFERENCE DESIGNATION	UNIVAC PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY.	USABLE ON CODE
7-7		4026000-04	MEMORY UNIT (TYPE 9150-4).....	1	
			Type 9150-4 Memory Unit is the same as Type 9150-10 (Figure 7-1) with the following exceptions: 1. 4026050-00 4K Core Memory Unit, qty 2 used instead of 8 2. 4026306-00 COMPONENT ASSEMBLY, qty 4 used instead of 16 3. 4026321-00 INHIBIT DRIVER, qty 7 used instead of 28 4. 4026342-00 COMPONENT ASSEMBLY, qty 2 used instead of 8 5. 4026362-00 COMPONENT ASSEMBLY, qty 3 used instead of 5 6. Add 4026399-00 COMPONENT ASSEMBLY, A133B1, qty 1 used 7. 4026437-00 COMPONENT ASSEMBLY, qty 7 used instead of 14		

Figure 7-7. Type 9150-4 Memory Unit

FIG. AND INDEX NO.	REFERENCE DESIGNATION	UNIVAC PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY.	USABLE ON CODE
7-8		4026000-03	MEMORY UNIT (TYPE 9150-3)..... Type 9150-3 Memory Unit is the same as Type 9150-10 (Figure 7-1) with the following exceptions: 1. 4026050-00 4K Core Memory Unit, qty 1 used instead of 8 2. 4026306-00 COMPONENT ASSEMBLY, qty 2 used instead of 16 3. 4026321-00 INHIBIT DRIVER, qty 4 used instead of 28 4. 4026342-00 COMPONENT ASSEMBLY, qty 1 used instead of 8 5. 4026362-00 COMPONENT ASSEMBLY, qty 3 used instead of 5 6. Add 4026399-00 COMPONENT ASSEMBLY, A133B1, qty 1 used 7. 4026437-00 COMPONENT ASSEMBLY, qty 7 used instead of 14	1	

Figure 7-8. Type 9150-3 Memory Unit