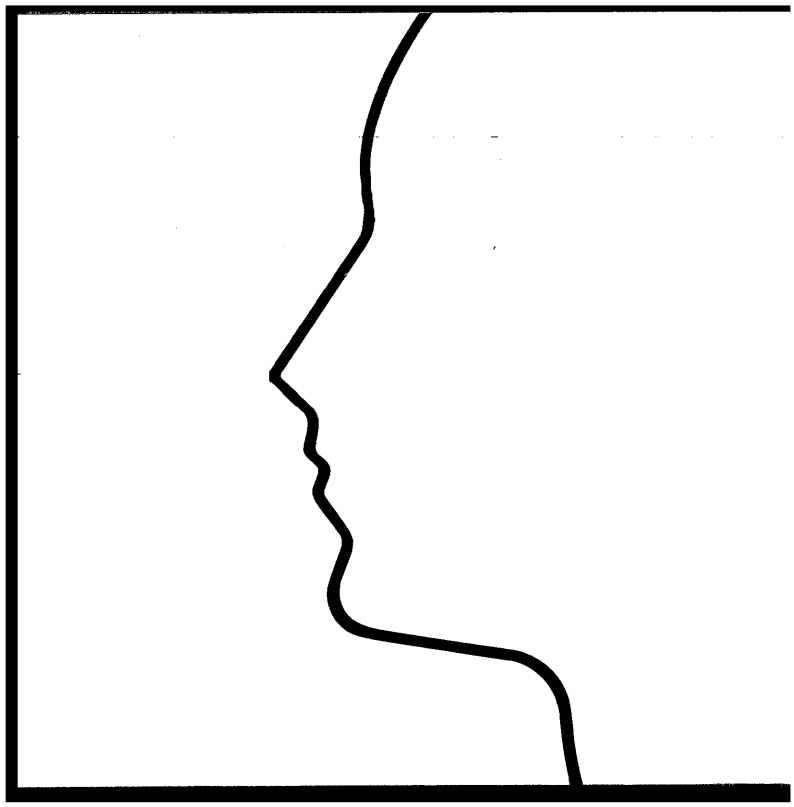
TEXAS INSTRUMENTS

EXPLORER™

7-SLOT SYSTEM ENCLOSURE

GENERAL DESCRIPTION



EXPLORER™ 7-SLOT SYSTEM ENCLOSURE GENERAL DESCRIPTION

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, can cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computer device pursuant to Subpart J of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference; in which case, the user at the user's own expense will be required to take whatever measures necessary to correct the interference.

WARNING: Lethal high voltages are present inside the chassis of this equipment. Only qualified service personnel who are familiar with the dangers of high voltages are permitted to open the chassis of this equipment to the service access position.

WARNING: The 68020-based processor board and the system interface board both contain lithium batteries. Lithium batteries can explode if the positive and negative terminals are shorted together. DO NOT place either of these boards on a conductive surface. The outside surfaces of all antistatic shipping bags are conductive; do not place either of these boards on an antistatic shipping bag, as this can cause the batteries to discharge.

CAUTION: Do not stack more than two mass storage units on top of the Explorer 7-slot enclosure. When more than two units are stacked on top of the 7-slot enclosure, there is a danger that the stacked units will become top heavy and possibly tip over the 7-slot enclosure.

MANUAL REVISION HISTORY

Explorer 7-Slot System Enclosure General Description (2243143-0001)

Original Issue ..... November 1984

Revision E ..... June 1987

Texas Instruments Incorporated
ATTN: Data Systems Group, M/S 2151
P.O. Box 2909
Austin, Texas 78769-2909

THE EXPLORER™ SYSTEM HARDWARE MANUALS

System Level Publications

Explorer 7-Slot System Installation 2243140-0001
Explorer System Field Maintenance 2243141-0001
Explorer System Field Maintenance Documentation Kit 2243222-0001
Explorer System Field Maintenance Supplement 2537183-0001
Explorer System Field Maintenance Supplement Documentation Kit 2549278-0001
Explorer NuBus™ System Architecture General Description 2537171-0001

System Enclosure Equipment Publications

Explorer 7-Slot System Enclosure General Description 2243143-0001
Explorer Memory General Description (8-megabytes) 2533592-0001
Explorer 32-Megabyte Memory General Description 2537185-0001
Explorer Processor General Description 2243144-0001
68020-Based Processor General Description 2537240-0001
Explorer II Processor and Auxiliary Processor Options General Description 2537187-0001
Explorer System Interface General Description 2243145-0001
Explorer NuBus Peripheral Interface General Description (NUPI board) 2243146-0001

Display Terminal Publications

Explorer Display Unit General Description 2243151-0001
CRT Data Display Service Manual, Panasonic code number FTD85055057C 2537139-0001
Model 924 Video Display Terminal User's Guide 2544365-0001

143-Megabyte Disk/Tape Enclosure Publications

Explorer Mass Storage Enclosure General Description 2243148-0001
Explorer Winchester Disk Formatter (ADAPTEC) Supplement to Explorer Mass Storage Enclosure General Description 2243149-0001
Explorer Winchester Disk Drive (Maxtor) Supplement to Explorer Mass Storage Enclosure General Description 2243150-0001
Explorer Cartridge Tape Drive (Cipher) Supplement to Explorer Mass Storage Enclosure General Description 2243166-0001
Explorer Cable Interconnect Board (2236120-0001) Supplement to Explorer Mass Storage Enclosure General Description 2243177-0001

143-Megabyte Disk Drive Vendor Publications

XT-1000 Service Manual, 5 1/4-inch Fixed Disk Drive, Maxtor Corporation, part number 20005 (5 1/4-inch Winchester disk drive, 112 megabytes) 2249999-0001
ACB-5500 Winchester Disk Controller User's Manual, Adaptec, Inc., (formatter for the 5 1/4-inch Winchester disk drive) 2249933-0001

1/4-Inch Tape Drive Vendor Publications	Series 540 Cartridge Tape Drive Product Description, Cipher Data Products, Inc., Bulletin Number 01–311–0284–1K (1/4-inch tape drive) ..... 2249997-0001 MT01 Tape Controller Technical Manual, Emulex Corporation, part number MT0151001 (formatter for the 1/4-inch tape drive) 2243182-0001
182-Megabyte Disk/Tape Enclosure MSU II Publications	Mass Storage Unit (MSU II) General Description 2537197-0001
182-Megabyte Disk Drive Vendor Publications	Control Data® WREN™ III Disk Drive OEM Manual, part number 77738216, Magnetic Peripherals, Inc., a Control Data Company 2546867-0001
515-Megabyte Mass Storage Subsystem Publications	SMD/515-Megabyte Mass Storage Subsystem General Description (includes SMD/SCSI controller and 515-megabyte disk drive enclosure) 2537244-0001
515-Megabyte Disk Drive Vendor Publications	515-Megabyte Disk Drive Documentation Master Kit (Volumes 1, 2, and 3), Control Data Corporation ..... 2246129-0002 Volume 1, General Description, Operation, Installation and Checkout, and Part Data ..... 2246125-0004 Volume 2, Theory, General Maintenance, Trouble Analysis, Electrical Checks, and Repair Information ..... 2246125-0005 Volume 3, Diagrams 2246125-0006
1/2-Inch Tape Drive Publications	MT3201 1/2-Inch Tape Drive General Description 2537246-0001
1/2-Inch Tape Drive Vendor Publications	Cipher CacheTape® Documentation Manual Kit (Volumes 1 and 2 With SCSI Addendum and, Logic Diagram), Cipher Data products ..... 2246130-0001 1/2-Inch Tape Drive Operation and Maintenance (Volume 1), Cipher Data Products ..... 2246126-0001 1/2-Inch Tape Drive Theory of Operation (Volume 2), Cipher Data Products ..... 2246126-0002 SCSI Addendum With Logic Diagram, Cipher Data Products 2246126-0003

Printer Publications

Model 810 Printer Installation and Operation Manual	2311356-9701
Omni 800™ Electronic Data Terminals Maintenance Manual for Model 810 Printers	0994386-9701
Model 850 RO Printer User's Manual	2219890-0001
Model 850 RO Printer Maintenance Manual	2219896-0001
Model 850 XL Printer User's Manual	2243250-0001
Model 850 XL Printer Quick Reference Guide	2243249-0001
Model 855 Printer Operator's Manual	2225911-0001
Model 855 Printer Technical Reference Manual	2232822-0001
Model 855 Printer Maintenance Manual	2225914-0001
Model 860 XL Printer User's Manual	2239401-0001
Model 860 XL Printer Maintenance Manual	2239427-0001
Model 860 Xl Printer Quick Reference Guide	2239402-0001
Model 860/859 Printer Technical Reference Manual	2239407-0001
Model 865 Printer Operator's Manual	2239405-0001
Model 865 Printer Maintenance Manual	2239428-0001
Model 880 Printer User's Manual	2222627-0001
Model 880 Printer Maintenance Manual	2222628-0001
OmniLaser™ 2015 Page Printer Operator's Manual	2539178-0001
OmniLaser 2015 Page Printer Technical Reference	2539179-0001
OmniLaser 2015 Page Printer Maintenance Manual	2539180-0001
OmniLaser 2108 Page Printer Operator's Manual	2539348-0001
OmniLaser 2108 Page Printer Technical Reference	2539349-0001
OmniLaser 2108 Page Printer Maintenance Manual	2539350-0001
OmniLaser 2115 Page Printer Operator's Manual	2539344-0001
OmniLaser 2115 Page Printer Technical Reference	2539345-0001
OmniLaser 2115 Page Printer Maintenance Manual	2539356-0001

Communications Publications

990 Family Communications Systems Field Reference	2276579-9701
EI990 Ethernet® Interface Installation and Operation	2234392-9701
Explorer NuBus Ethernet Controller General Description	2243161-0001
Communications Carrier Board and Options General Description	2537242-0001

THE EXPLORER™ SYSTEM SOFTWARE MANUALS

Mastering the Explorer Environment	Explorer Technical Summary	2243189-0001
	Introduction to the Explorer System	2243190-0001
	Explorer Zmacs Editor Tutorial	2243191-0001
	Explorer Glossary	2243134-0001
	Explorer Networking Reference	2243206-0001
	Explorer Diagnostics	2533554-0001
	Explorer Master Index to Software Manuals	2243198-0001
	Explorer System Software Installation Guide	2243205-0001
Programming With the Explorer	Explorer Programming Concepts	2549830-0001
	Explorer Lisp Reference	2243201-0001
	Explorer Input/Output Reference	2549281-0001
	Explorer Zmacs Editor Reference	2243192-0001
	Explorer Tools and Utilities	2549831-0001
	Explorer Window System Reference	2243200-0001
Explorer Options	Explorer Natural Language Menu System User's Guide	2243202-0001
	Explorer Relational Table Management System User's Guide	2243203-0001
	Explorer Grasper User's Guide	2243135-0001
	Explorer Prolog User's Guide	2537248-0001
	Programming in Prolog, by Clocksin and Mellish	2537157-0001
	Explorer Color Graphics User's Guide	2537157-0001
	Explorer TCP/IP User's Guide	2537150-0001
	Explorer LX™ User's Guide	2537225-0001
	Explorer LX System Installation	2537227-0001
	Explorer NFS™ User's Guide	2546890-0001
	Explorer DECnet™ User's Guide	2537223-0001
	Personal Consultant™ Plus Explorer	2537259-0001
System Software Internals	Explorer System Software Design Notes	2243208-0001
	Release Information, Explorer System Software	2549844-0001

CONTENTS

Index

ABOUT THIS MANUAL

Purpose

This manual describes the Texas Instruments Explorer 7-slot system enclosure. The information in this manual is intended for system designers, value-added resellers (VARs), maintenance personnel, operators, and system users.

Contents

This manual consists of three sections and an appendix, as follows:

Section 1: General Information — Briefly describes the features, configurations, and specifications of the Explorer 7-slot system enclosure.

Section 2: Installation, Operation, and PM — Provides information for installing, connecting, operating, and servicing the system enclosure.

Section 3: Equipment Description — Describes the 7-slot system enclosure, the power distribution, the power supplies, and backplanes associated with the different system enclosures.

Appendix A: NuBus Summary — Contains a summary of the NuBus used in the Explorer systems.

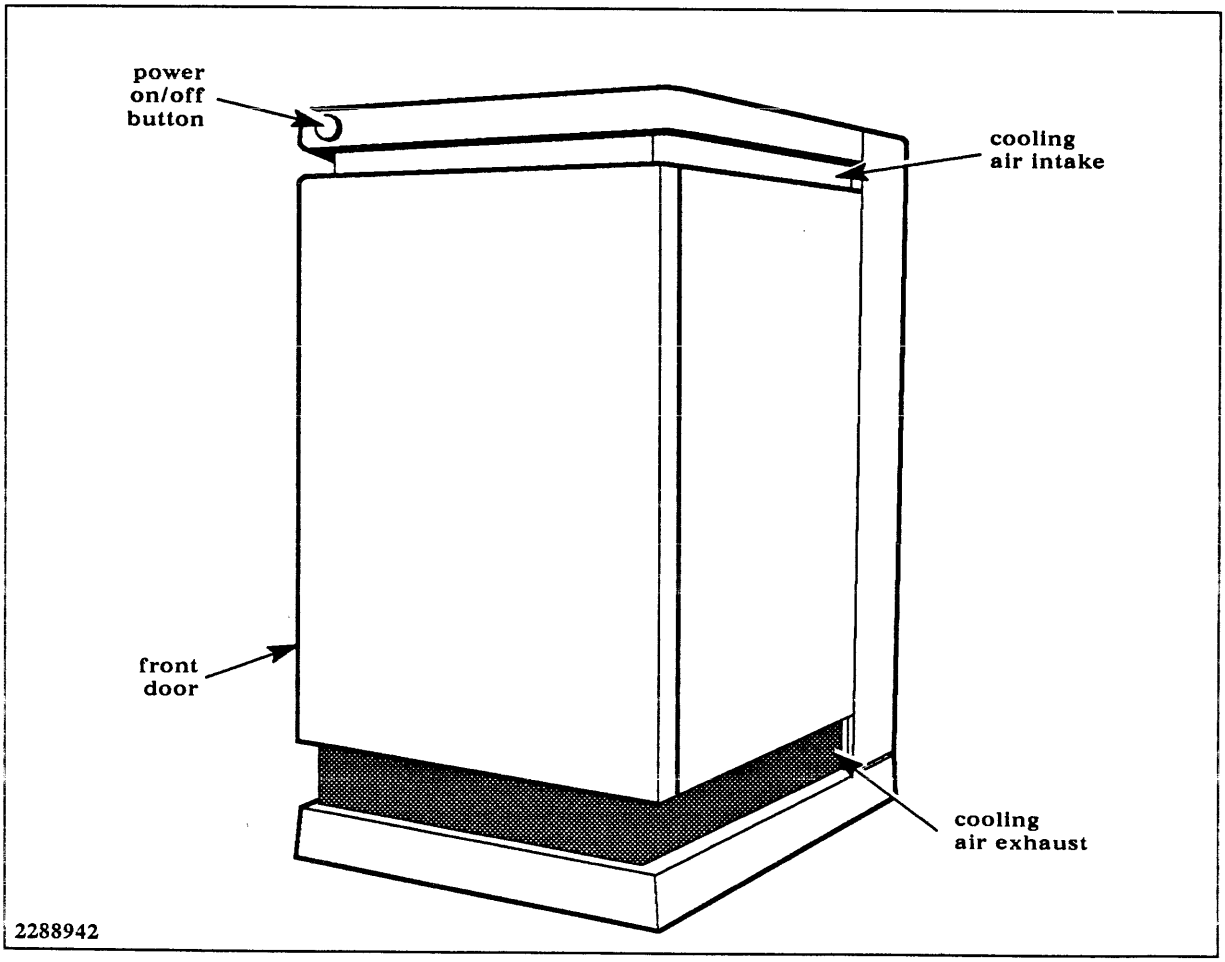
1 GENERAL INFORMATION

Introduction

1.1 This section provides a general overview of the Explorer 7-slot system enclosure (Figure 1-1). This section contains information on the following topics:

- Features
- Configurations
- Specifications
- Physical description
- Reference information

Figure 1-1 Explorer 7-Slot System Enclosure



Features

1.2 The Texas Instruments Explorer 7-slot system enclosure (Figure 1-1) is a low-profile, free-standing unit that provides cooling air, operating voltage, signal connections from external units, and mounting slots for the boards. The enclosure is mounted on casters for optimum mobility. Enclosure features include:

- Mounting slots for up to seven system boards.
- Unique airflow design for maximum reliability.
- On early models of the enclosure with an 80-ampere power supply, two auxiliary ac power receptacles that can connect to peripherals. The power to these receptacles is controlled by the enclosure ac power on/off button.
- An ac power input circuit breaker used with the 110-ampere power supply.
- Explorer backplane with the NuBus and the local bus, or the NuBus-only backplane without the local bus.
- Low-voltage and high-voltage power settings that span the standard ac line voltages/frequencies of most countries.
- Extensive shielding and filtering to prevent electromagnetic interference (EMI) radio frequency radiation and power line conduction emissions.
- Circuit board fault indicator light-emitting diodes (LEDs) to indicate faults within circuit boards.
- A flat top surface for stacking a maximum of two mass storage units.
- User maintainability.
- Built-in self-test capabilities to provide a high confidence level.

Configurations

1.3 The primary configuration for the 7-slot enclosure is the standalone work station for advanced applications. The enclosure also has the capability for multiprocessor configurations. To provide ample dc power for the variety of optional circuit boards, the 7-slot enclosure can have the following configurations:

- Enclosure with a local bus backplane and an 80-ampere power supply or a 110-ampere power supply
- Enclosure with a NuBus-only backplane with a 110-ampere power supply

The enclosures can also be configured for low-voltage (120 Vac) or high-voltage (220/240 Vac) input power requirements.

Backplane Configurations

1.3.1 The original 7-slot enclosure has the local bus backplane. The local bus is required with the Explorer I processor. The local bus consists of connectors P23 through P26 (slots 3 through 6) on row 2 of the backplane. The local bus slots are dedicated in most cases to certain types of circuit boards.

The NuBus-only backplane does not have a local bus. All slots (slots 0 through 6) on the NuBus-only backplane are available for any type of circuit board. The NuBus-only backplane is also designed to handle higher currents on most of the dc voltages distributed over the backplane.

Low-Voltage and High-Voltage Inputs

1.3.2 Standard ac line voltages throughout the world range from 120 volts to 240 volts nominal. A low-voltage configuration operates over an input range of 102 to 132 volts, and a high-voltage configuration operates over an input range of 187 to 264 volts. The voltage range is selected by the voltage select switch on the motor power supply, located behind the motor power supply cover for 80-ampere power supply versions. On 110-ampere power supply versions, the voltage range selector is accessible through the power interface assembly cover.

Specifications

1.4 Table 1-1 summarizes the specifications of the 7-slot enclosure for the standalone, single-processor work station with an 80-ampere power supply or a 110-ampere power supply.

Table 1-1 Enclosure Specifications

Category	Specifications	
Dimensions:		
Height	635.0 mm (25 in)	
Width	330.2 mm (13 in)	
Depth	457.2 mm (18 in)	
Weights:		
Enclosure (without boards)	26.30 kg (58 lb)	
Enclosure (with boards)	38.90 kg (85 lb)	
Mounting requirements	Free standing	
80-A power supply output requirements	+5 main (+5.1 Vdc ± 3%)	80 A (5 A minimum)
	+12 main (+12 Vdc ± 5%)	1 A
	−5 main (−5 Vdc ± 5%)	0.1 A
	−12 main (−12 Vdc ± 5%)	1 A
110-A power supply output requirements	+5 main (+5.1 Vdc ±3%)	110 A (10 A minimum)
	+12 main (+12 Vdc ± 5%)	1.5 A
	−5 main (−5 Vdc ± 5%)	4.0 A
	−12 main (−12 Vdc ± 5%)	1 A
Power supply efficiency	65%	
Air conditioning load for fully loaded enclosure	80-A power supply	610 W (2100 Btu/h)
	110-A power supply	920 W (3139 Btu/h)
Acoustic noise	50 dBA	
EMI conduction/radiation	Meets limits specified by FCC docket 20780 (Class A), VDE 0871 (Level A)	

Table 1-1 Enclosure Specifications (Continued)

Category	Specifications	
80-A power input requirements:		
Input voltage range (low)	102 to 132 Vac, 3-wire service (line, neutral, ground), 120 Vac nominal 7.5 A	
Input voltage range (high)	187 to 264 Vac, 3-wire service (line, neutral, ground), 220 Vac nominal 4.8 A, 240 Vac nominal 4.5 A	
Input frequency	47 to 63 Hz	
Input power	Mass storage unit	181 W
	Display monitor	60 W
	7-slot enclosure	610 W
	Maximum total VA using auxiliary receptacles	850 W
110-A power input requirements:		
Input voltage range (low)	102 to 132 Vac, 3-wire service (line, neutral, ground), 120 Vac nominal 12.0 A	
Input voltage range (high)	187 to 264 Vac, 3-wire service (line, neutral, ground), 220 Vac nominal 6.0 A, 240 Vac nominal 6.0 A	
Input frequency	47 to 63 Hz	
Input power	920 W	

Physical Description

1.5 The paragraphs that follow provide a physical description of the 7-slot enclosure. Figures 1-2 through 1-5 show the locations of various parts of the enclosure.

The exterior cover, made of high-strength plastic, completely encloses the system chassis assembly. The exterior cover consists of right and left sides, front and rear doors, and a backplane cover. The exterior covers are attached to the system chassis assembly with thread-forming screws.

The system chassis (Figure 1-2) is a zinc-plated, sheet-steel assembly. This assembly provides shielding and mounting for the circuit boards and other enclosure parts. The system chassis has a metal door for access to the circuit boards. The following parts make up the system chassis assembly:

- System power supply
- Motor power supply with the 80-ampere power supply
- Power interface assembly with the 110-ampere power supply
- Adapter guide assembly

- Intake assembly
- Card cage assembly
- Backplane with local bus
- Backplane without local bus
- Chassis base assembly

Figure 1-2 7-Slot Enclosure With 80-Ampere Power Supply — Front Interior View

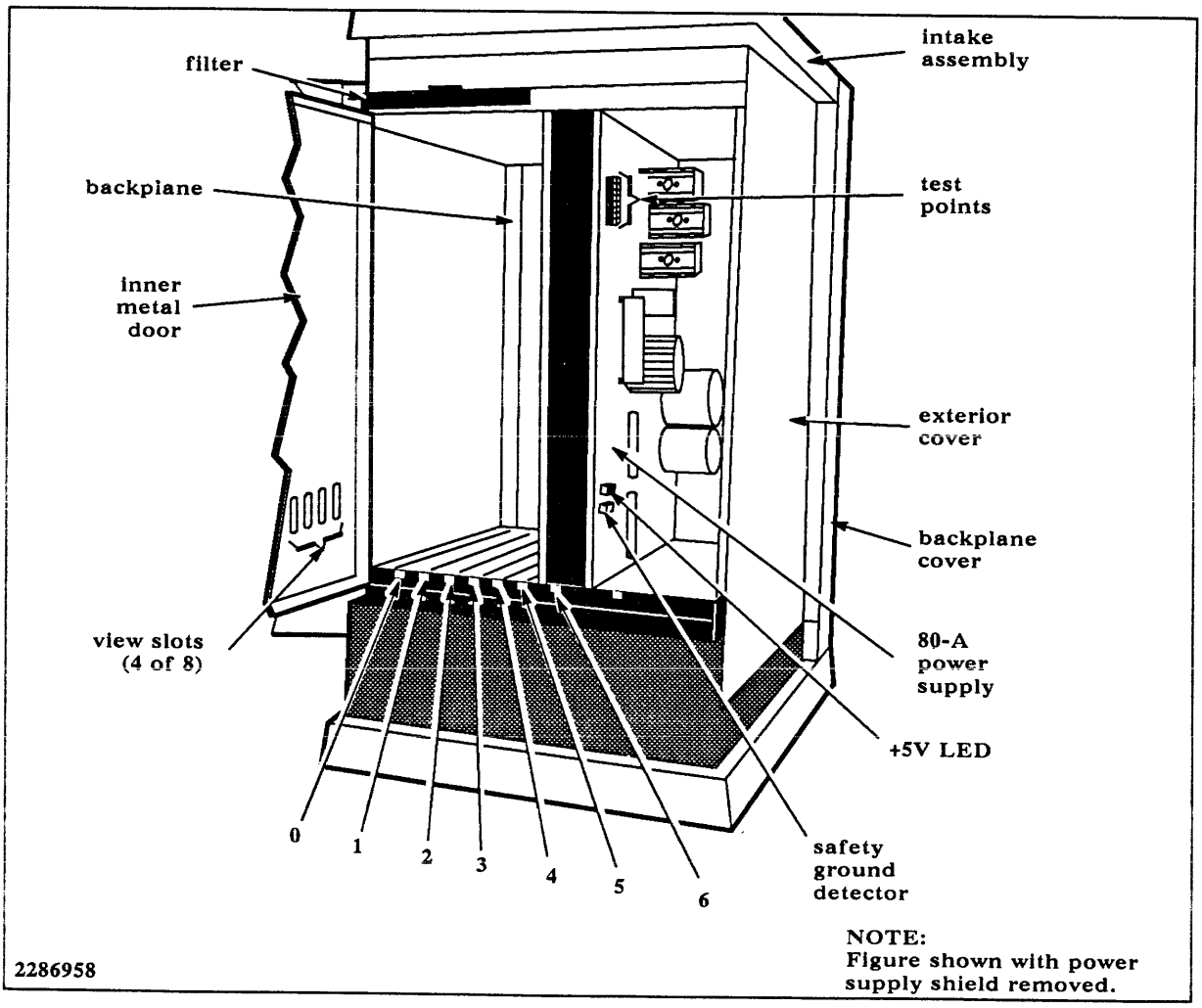
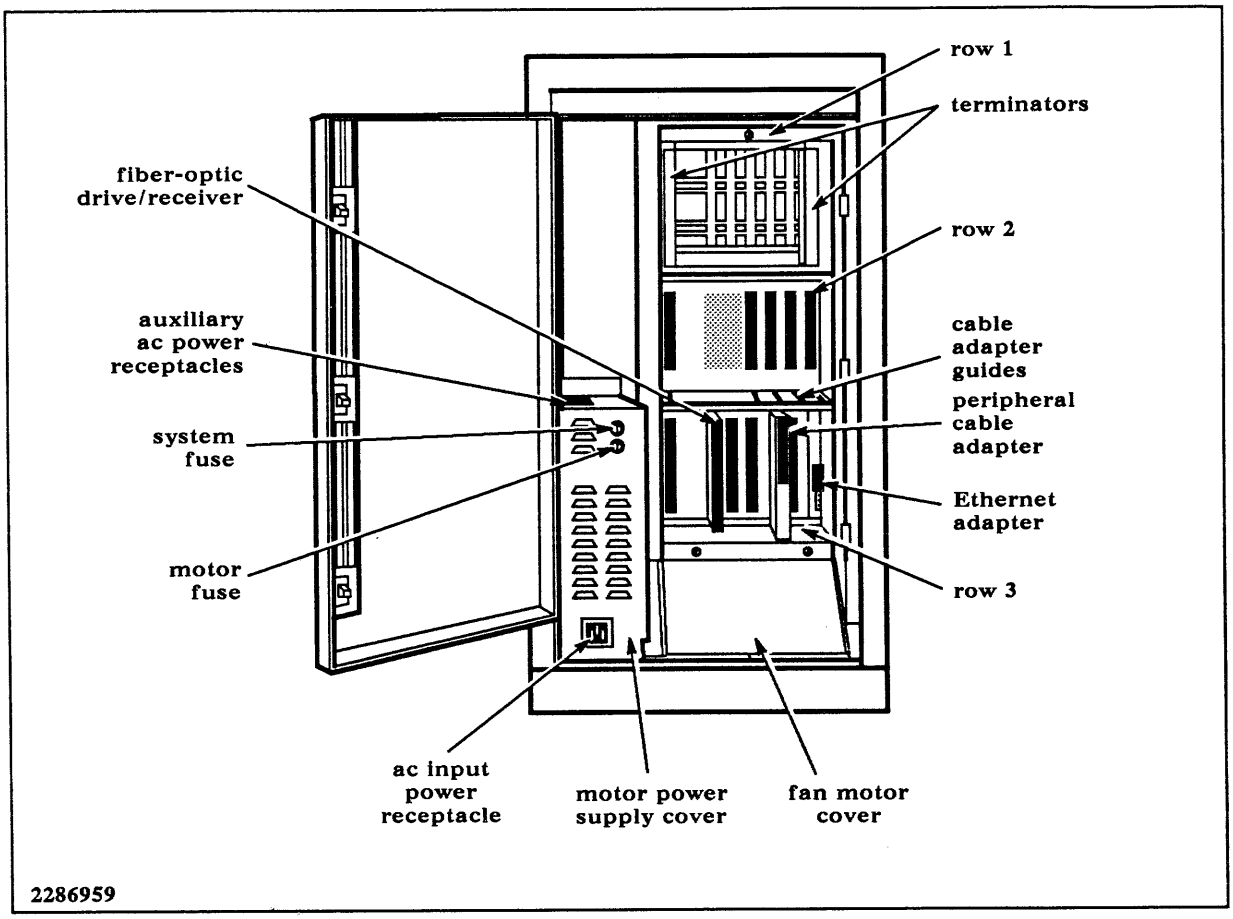


Figure 1-3 7-Slot Enclosure With 80-Ampere Power Supply — Rear Interior View



The enclosure base assembly contains the impeller, casters, motor, and transformer assemblies. The 110-ampere version does not have a transformer in the base assembly.

A disposable air filter is located in a slot at the top of the system chassis assembly. The filter fits flush against the slotted metal grill of the board slot assembly. You can access the filter by opening the front enclosure door. Refer to Section 2 for information on filter service.

An on/off push-button control switch is located on the left front edge of the top cover. With an 80-ampere power supply, the two auxiliary ac power receptacles (see Figure 1-3) for the display monitor and mass storage unit (MSU) are located on top of the motor power supply cover. The system fuse and the motor fuse are accessible through the motor power supply cover.

NOTE: The two auxiliary ac power receptacles are present only on early models of the enclosure that have the 80-ampere power supply.

The fuses and auxiliary ac power receptacles are not provided with a 110-ampere power supply. A circuit breaker located on the power interface assembly cover (see Figure 1-5) replaces the fuses used with the 80-ampere power supply.

Figure 1-4 7-Slot Enclosure With 110-Ampere Power Supply — Front Interior View

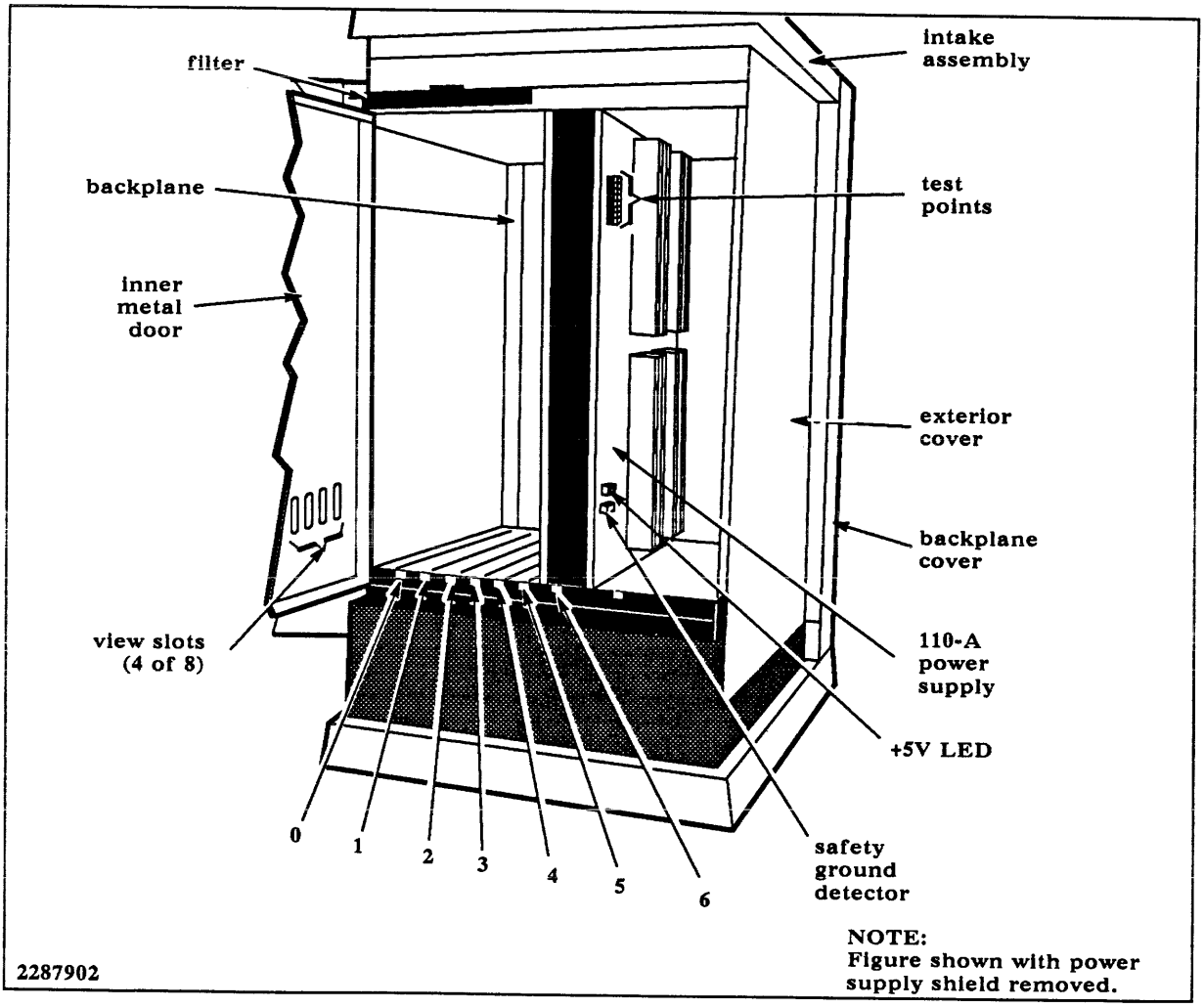
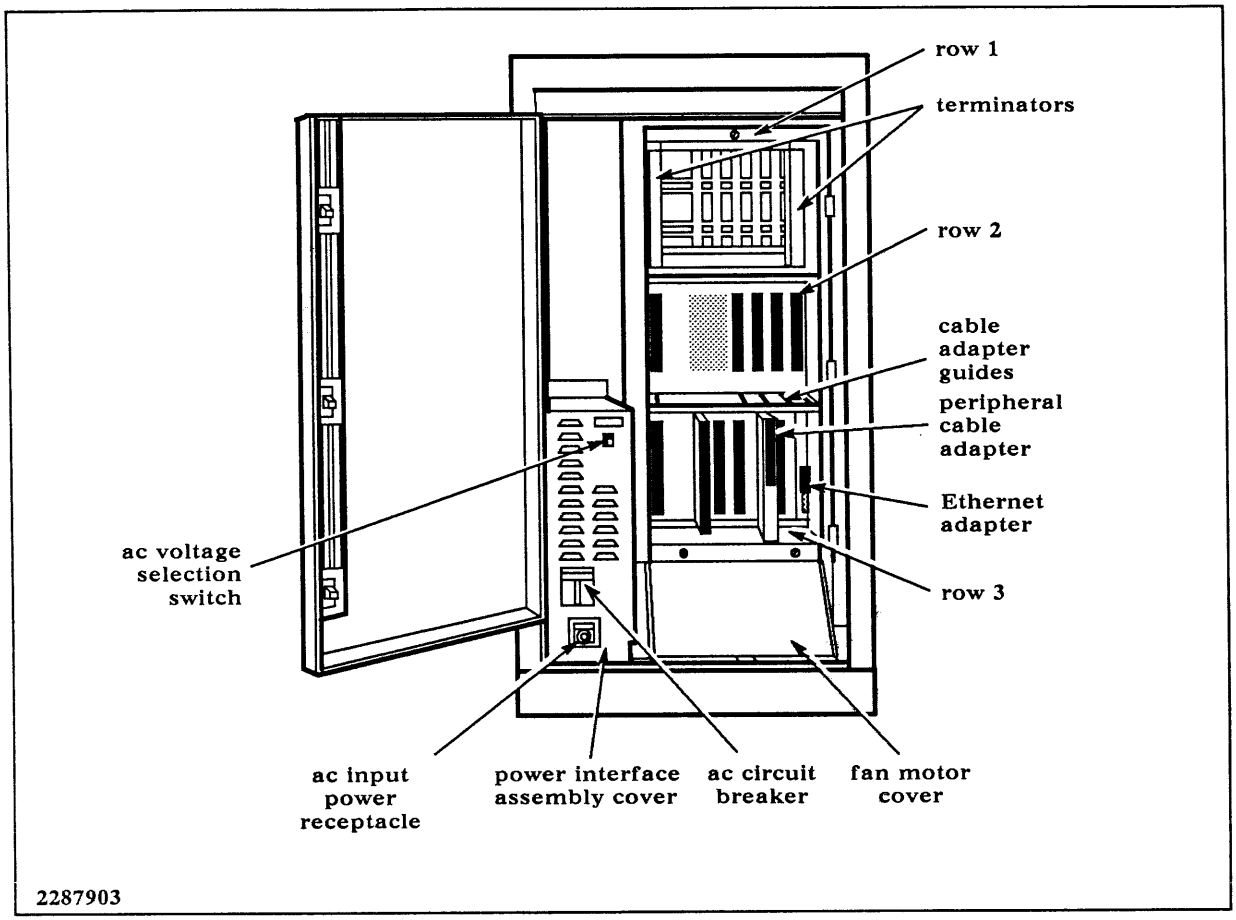


Figure 1-5 7-Slot Enclosure With 110-Ampere Power Supply — Rear Interior View



Eurocard Circuit Board Slots

1.5.1 The system chassis assembly has seven vertical slots for mounting the processor and other Eurocard circuit boards plus a slot for the power supply board. The inner metal door contains view slots for observing the fault indicator LEDs located on the edge of each circuit board. Access to the boards is gained by opening the front enclosure door and then unlocking the two latches on the inner metal door and opening it. Safety interlock switches are provided to shut off power to the enclosure when either the inner metal door or rear enclosure door is opened. Refer to Section 2 for removal and installation procedures for circuit boards.

WARNING: Ensure that power to the enclosure is off prior to accessing the circuit boards. Lethal voltage exists on the power supply board.

Each board slot has three connectors mounted to the enclosure backplane. (Refer to Section 3 for pin number assignments.) The system circuit board slots are numbered 0 through 6, reading from left to right when facing the front of the enclosure. The power supply board occupies an unnumbered slot

position that can be called slot 7. Due to airflow design, the Explorer I processor must be installed in slot 6. The system interface board must be installed in slot 5. The slots are designed to hold three-high Eurocards.

Backplane Information

1.5.2 The backplane (see Figure 1-2) consists of three rows of eight connectors each. Refer to Section 3 for pin number assignments. The slot numbers read from right to left on the backplane when facing the rear of the system enclosure.

The top row of connectors for slots 0 through 6 are reserved for the NuBus for data, control, power, and address lines. The bus line connects across all seven signal connectors so that each slot has access to the NuBus. The NuBus is a flexible bus structure based on a master/slave concept. For each interaction, a device takes control of the NuBus, thus becoming a master, and addresses another device, which becomes the slave for that interaction.

On enclosures with the local bus backplane, the second row of connectors connect to the local bus and input/output (I/O) ports. Local bus lines interconnect on slots 3 through 6 to provide a local bus. The local bus is a high-speed, 32-bit private bus for exclusive use by the Explorer I processor. The local bus provides a high processor-to-memory bandwidth and leaves the NuBus available for system-wide operations. Slots 0 through 2 can be used for additional I/O ports.

On enclosures with the NuBus-only backplane, the second row of connectors in slots 0 through 6 connect to I/O ports that are defined by the type of board in the slot.

The third row of connectors in slots 0 through 6 are reserved for the I/O connections that are defined by the type of board in the slot.

NuBus Terminator Information

1.5.3 The NuBus terminators associated with the local bus backplane and the NuBus-only backplane are listed in the following chart. The NuBus clock is available from the system interface board (SIB) or terminator, TI part number 2249565-0001. When both clock sources are available in the same chassis, the SIB clock is disabled.

Backplane Usage	Terminator Part Number	Description
Local bus backplane	2243885-0001	Clock termination
	2243885-0002	Regular NuBus termination
NuBus-only backplane	2249565-0001	NuBus clock logic
	2249565-0002	Regular NuBus termination

Fuse Data

1.5.4 Power enters the enclosure through connector J1 attached to the motor power supply cover assembly or connector J1 attached to the power interface board on the rear of the enclosure. With the 80-ampere power supply, two fuse holders are located on the motor power supply and are accessible by opening the rear door of the enclosure. With the 110-ampere power supply, these fuses are replaced by an ac circuit breaker. Refer to Section 2 for more information on fuse location and replacement.

WARNING: Ensure that power to the enclosure is off prior to accessing the fuses. A safety interlock switch is provided to disconnect power from the enclosure when the rear door is opened.

Each of the fuses can be either a UL/CSA-approved GLH type or 5-by-20-millimeter SPT type. The type of fuse needed depends on whether a U.S. or international fusecap is installed. Table 1-2 lists the fuse data for the 7-slot enclosure with an 80-ampere power supply.

Table 1-2 Fuse Data With 80-Ampere Power Supply

Power Setting	Fuse Type	Fuse Protection	Current Rating	Source	Part Number
Low power setting	GLH	System	10.0 A	TI Bussman Mfg.	0416434-0005 GLH10
	GLH	Motor	3.0 A	TI	0416434-0303
High power setting	SPT	System	5.0 A	TI H.Schurter	2220531-0008 034.3124
	SPT	Motor	1.6 A	TI	2220531-0003

Reference Information

1.6 Table 1-3 lists reference information that can be referred to when additional technical information is needed.

Table 1-3 Additional Reference Documents

Item Identification	Part Number
Explorer Enclosure Family Tree	2235534-0001
Explorer Enclosure Assembly	2235540-0001
Explorer Enclosure Backplane Assembly (with NuBus and local bus)	2235535-0001
Explorer Enclosure Backplane Logic Diagram	2235537-0001
Explorer Enclosure Backplane Specification	2235539-0001
Explorer Enclosure Backplane Assembly (with NuBus only)	2535855-0001
Explorer Enclosure Backplane Logic Diagram	2535857-0001
Explorer Enclosure Backplane Specification	2535859-0001
80-Ampere Power Supply Assembly	2235505-0001
80-Ampere Power Supply Logic Diagram	2235507-0001
80-Ampere Power Supply Specification	2235509-0001
Motor Power Supply Assembly (80-A power supply)	2235600-0001
Motor Power Supply Logic Diagram	2235602-0001
Motor Power Supply Specification	2235604-0001
Power Supply Upgrade Procedure (80-A power supply chassis to 110-A power supply chassis)	2537300-0001
110-Ampere Power Supply Assembly	2542005-0001
110-Ampere Power Supply Logic Diagram	2542007-0001
110-Ampere Power Supply Specification	2542009-0001
Power Interface Board Assembly	2542010-0001
Power Interface Board Logic Diagram	2542012-0001
Power Interface Board Specification	2542014-0001
NuBus Terminator Assembly (local bus backplane with clock termination)	2243885-0001
NuBus Terminator Assembly (local bus backplane)	2243885-0002
NuBus Terminator Logic Diagram	2243887-0001
NuBus Terminator Assembly (NuBus-only backplane with NuBus clock)	2249565-0001
NuBus Terminator Assembly (NuBus-only backplane)	2249565-0002
NuBus Terminator Logic Diagram	2249567-0001
NuBus Terminator Specification	2249569-0001

2 INSTALLATION, OPERATION, AND PM

Introduction

2.1 This section provides installation, operation, and preventive maintenance information for a basic Explorer 7-slot system enclosure. This section is arranged under the following major topics:

- 7-slot enclosure installation
- Eurocard circuit board removal and installation
- Installation of option boards and adapters
- Cable routing
- Operation
- Preventive maintenance

7-Slot Enclosure Installation

2.2 A computer site must provide the electrical power, a controlled environment, and adequate space for proper operation. The following paragraphs provide installation information for the 7-slot enclosure:

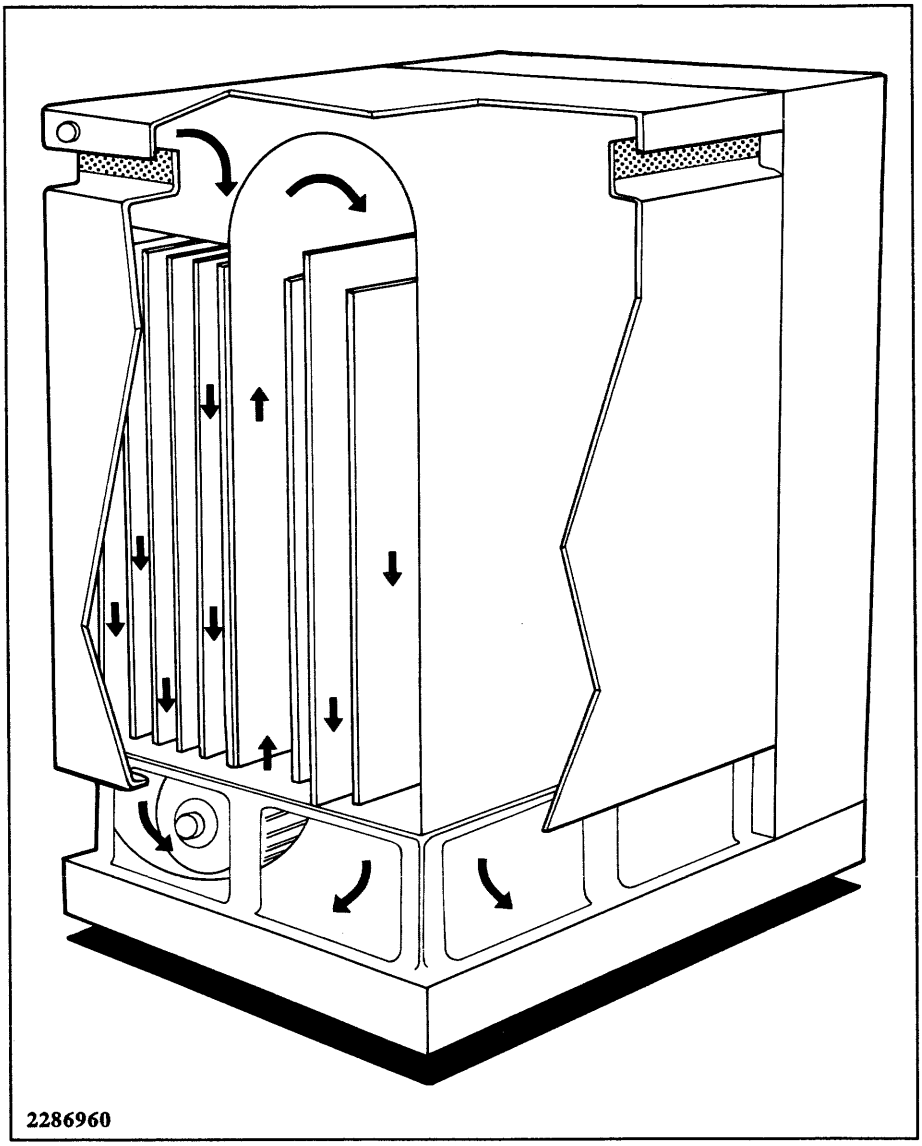
- Airflow requirements
- Power distribution and grounding
- Space requirements
- Environmental requirements
- Electrical power connectors and cords

Refer to the *Explorer 7-Slot System Installation* manual, TI part number 2243140-0001, for additional information on site preparation, power distribution, and equipment installation.

Airflow Requirements

2.2.1 Figure 2-1 shows the enclosure airflow. Air is drawn in through a filter at the top of the enclosure and down over slots 0 through 5 to the fan. The fan forces the air up through slot 6 and then down through slot 7 to exit at the bottom of the enclosure. This airflow scheme directs maximum cooling to the processor in slot 6 and to the power supply in slot 7.

Figure 2-1 **Enclosure Airflow**



Power Distribution and Grounding

2.2.2 Voltage irregularities and noise on ac power lines can cause errors in computer operation. To minimize line noise, it is recommended that you provide a dedicated ac power circuit for your 7-slot enclosure. Route the power circuit away from large switching devices, motors, welders, and other sources of induction fields. Copiers, electric typewriters, and other office machines can also generate electrical noise. All power circuits must meet the safety and good practice standards of the regulatory agencies having jurisdiction at your site.

Space Requirements

2.2.3 The 7-slot enclosure is compact enough to fit under most desks and tables. To ensure maximum air cooling, at least three sides of the enclosure should be unobstructed at all times. For example, do not place the enclosure flush between two filing cabinets.

The enclosure opens from both the front and the rear for access to the boards and the cables. The placement of the enclosure for access requirements is unrestricted because the enclosure is free-standing and movable.

Environmental Requirements

2.2.4 The 7-slot enclosure is rated for a wide range of operating temperatures and humidities. These ranges coincide with the comfort range settings of most office air-conditioning systems. Table 2-1 lists the environmental requirements for the 7-slot enclosure.

Table 2-1 **Environmental Requirements**

Requirements	Range/Limit
Operating temperature	10° to 35° C (50° to 95° F)
Operating humidity	20% to 80% noncondensing
Storage temperature	−40° to 65° C (−40° to 149° F)
Storage humidity	5% to 95% noncondensing
Operating shock	15 g for 11 ms (half sine wave)
Storage shock	25 g for 11 ms (half sine wave)
Operating vibration	0.5 g (sine wave)
Storage vibration	1.0 g (sine wave)
Operating altitude	−300 to 2000 m (−1000 to 6500 ft)
Storage altitude	−300 to 3000 m (−1000 to 10,000 ft)
Electrostatic discharge	20 kV (operator recoverable)

Electrical Power Connectors and Cords

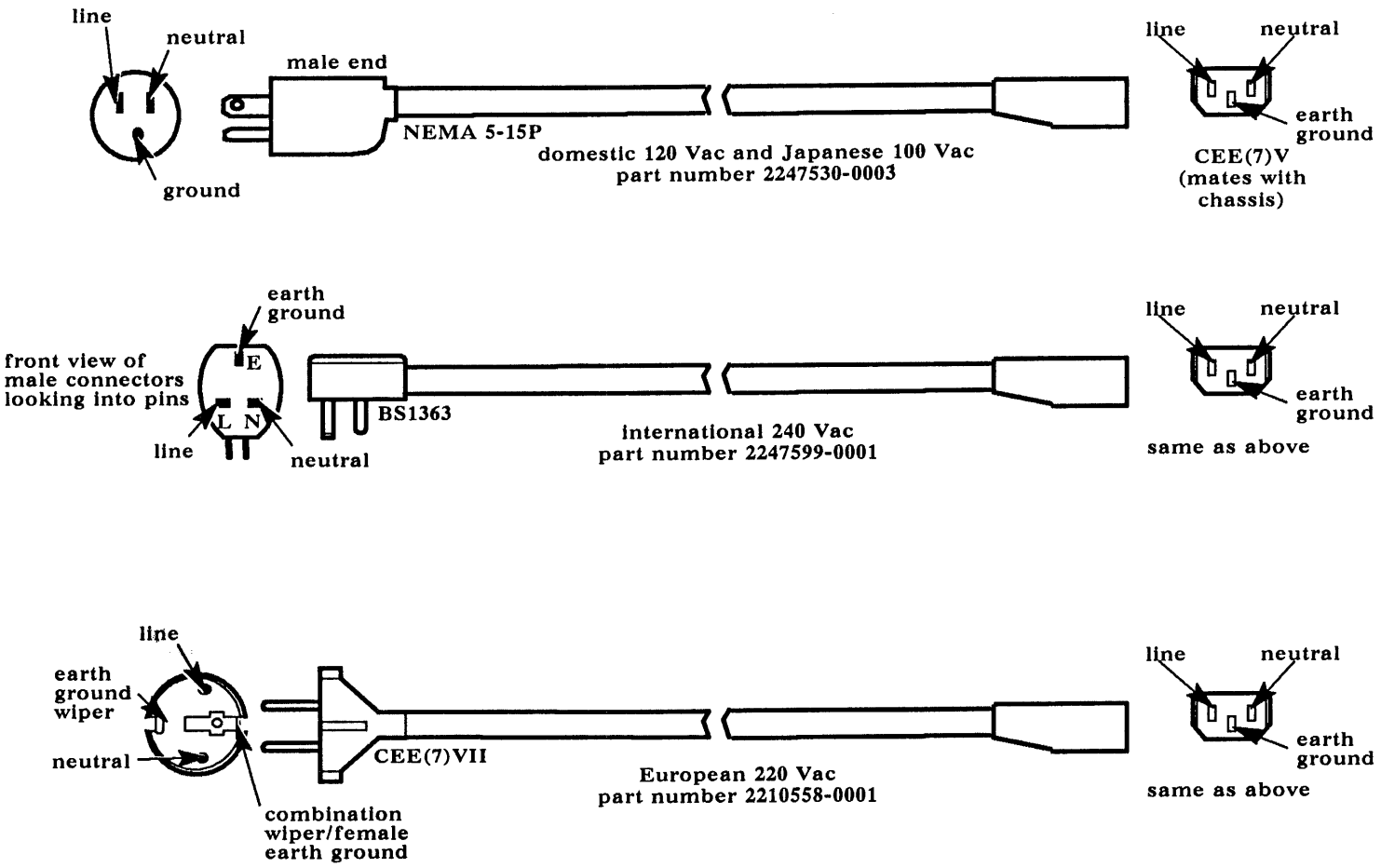
2.2.5 The low-voltage setting of the 7-slot enclosure can operate on any ac voltage ranging from 102 to 132 volts at 47 to 63 hertz. The high-voltage setting can operate on any ac voltage ranging from 187 to 264 volts at 47 to 63 hertz. The enclosure comes with the voltage set for your requirements.

These wide input-voltage ranges allow the 7-slot enclosure to operate in most countries. With an 80-ampere power supply, the enclosure is designed to accept a CEE(7)V plug no matter what range is selected. With a 110-ampere power supply, the enclosure is designed to accept a IEC C20 plug no matter what range is selected. A three-wire line cord with separate line, neutral, and ground conductors connects the enclosure to the wall socket.

Figures 2-2 and 2-3 show the prewired cord sets that are available in the U.S. and other countries for Explorer systems with an 80-ampere or 110-ampere power supply, respectively. Details of the line plug are shown at the left side of the figure. The NEMA 5-15P line plug is supplied in the U.S., Canada, and Japan. Standard line voltage is 120 volts in the U.S. and Canada, and 100 volts in Japan. Great Britain has a 240-volt power system, and the line cord has a BS 1363A plug. This plug contains an internal 5-ampere BS 1362 fuse as shown in Figure 2-4. Refer to Section 1 for fuse part numbers.

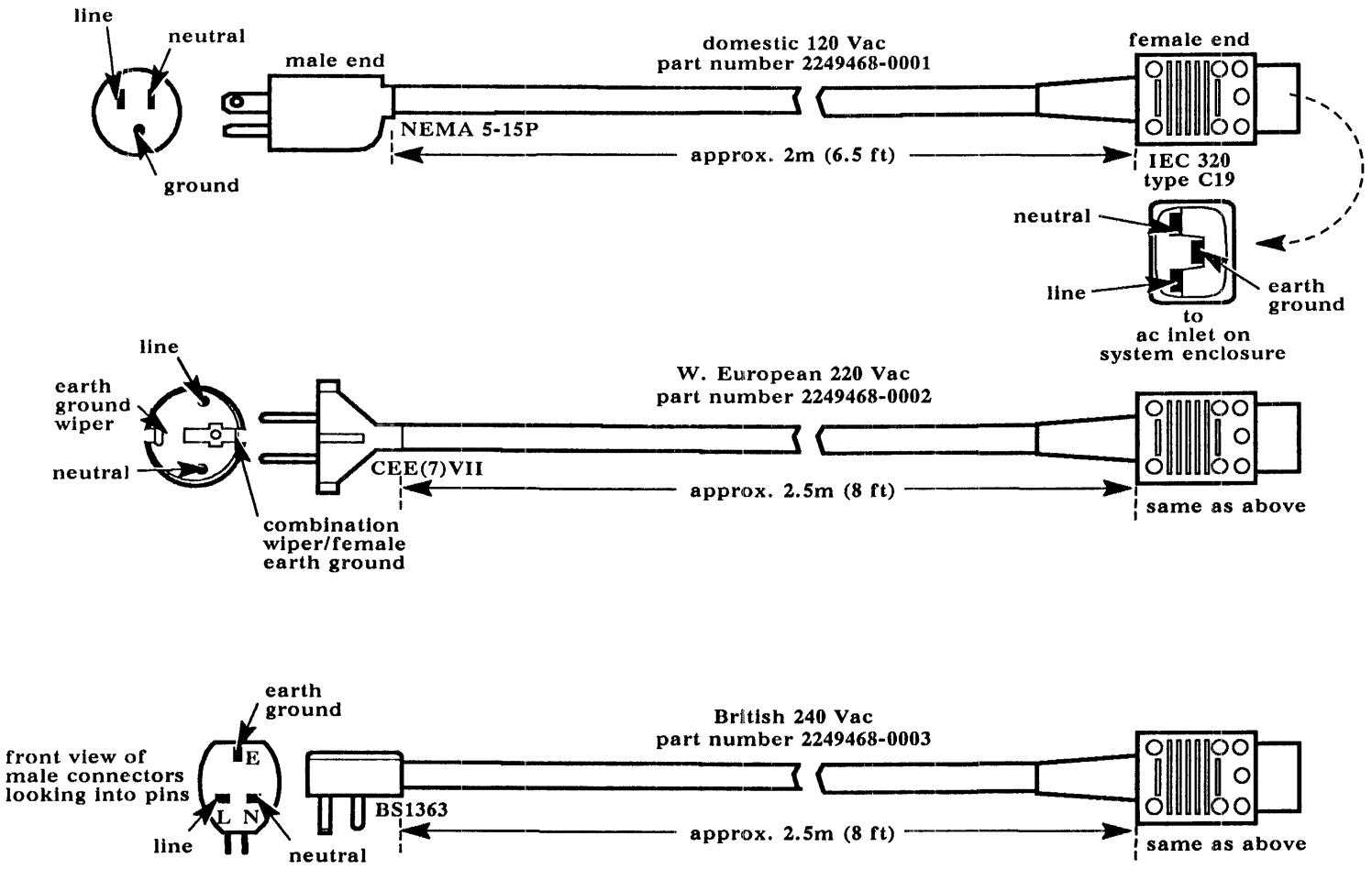
Western European countries (except Switzerland and Denmark) commonly use the CEE(7)VII line plug supplied for Germany, France, Belgium, Austria, Norway, Sweden, the Netherlands, and Finland. The nominal line voltage is 220 volts in these countries.

Figure 2-2 Power Cord Set and Connectors, 80-Ampere Power Supply (Early Enclosure Models Only)



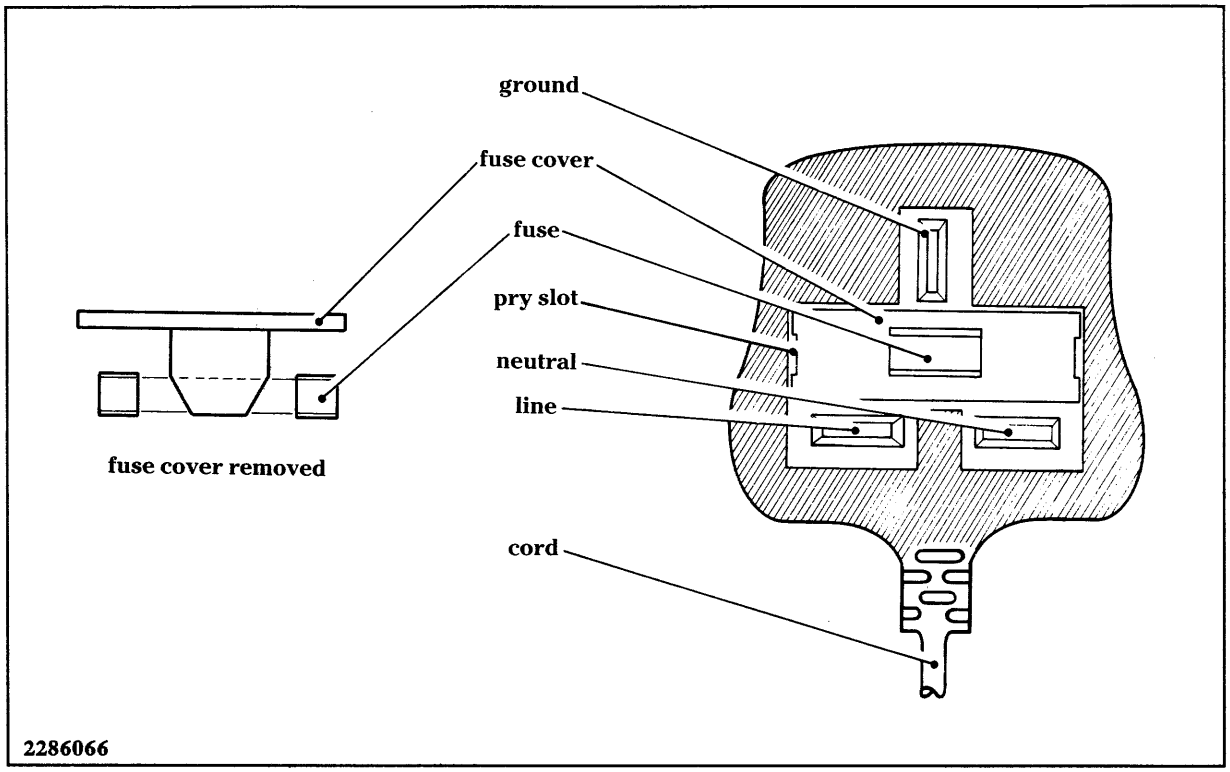
2288943

Figure 2-3 Power Cord Set and Connectors, 110-Ampere Power Supply



2287919

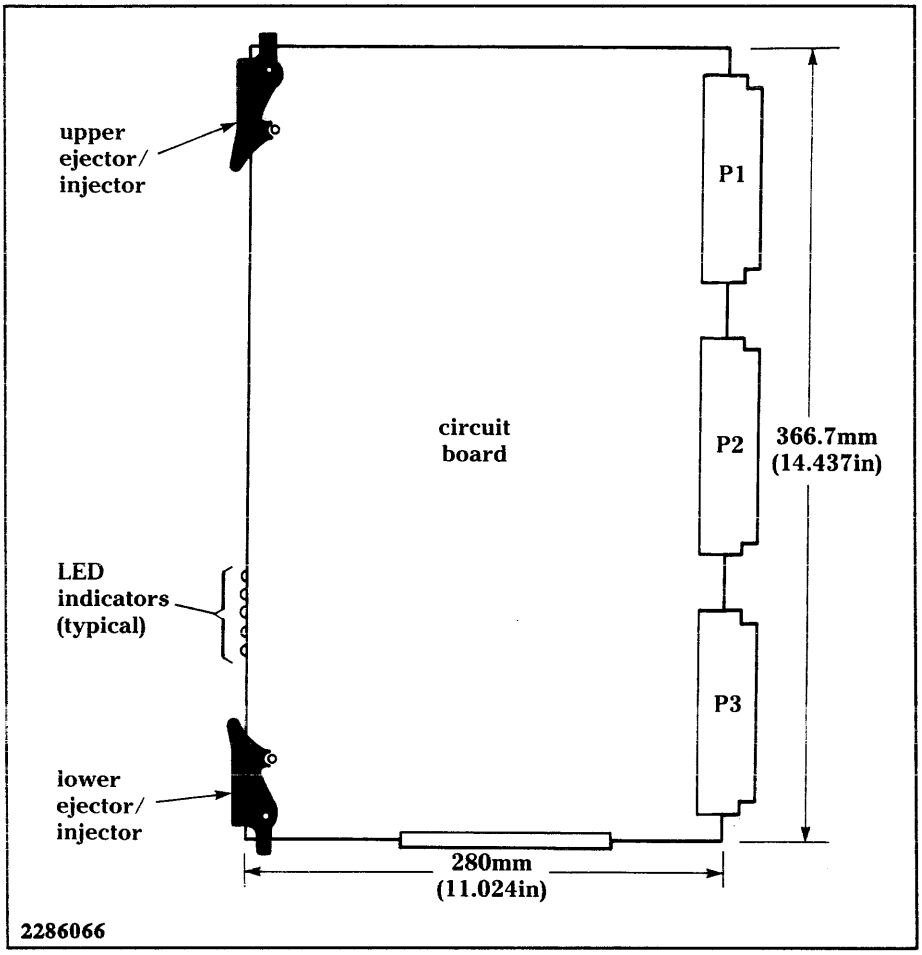
Figure 2-4 BS 1363A Fused Power Connector for Great Britain



Eurocard Circuit Board Information

2.3 The boards are three-high International Electrotechnical Commission (IEC) boards called *Eurocards*. Each of the boards includes three 603-2-IEC-C096-M connectors. These connectors are referred to as P1, P2, and P3. P1 is the top connector and P3 is the bottom connector. Ejector/injector tabs are located on the front edge of each board, at the top and bottom. These ejector/injector tabs are used for engaging or disengaging the board with the backplane connectors. The boards also have fault indicator LEDs on the front edge for self-test indication. Figure 2-5 shows a typical Eurocard configuration.

Figure 2-5 **Typical Eurocard Configuration**



Eurocard Circuit Board Removal

2.3.1 Use the procedure that follows to remove Eurocard circuit boards from the enclosure.

WARNING: Before removing the power supply board, allow a five-minute bleedoff time after power has been removed from the enclosure. Connector J37 pins — ACHI, ACLO, and CT — have lethal potential after power is disconnected.

1. Ensure that power to the enclosure is off.
2. Open the front enclosure door by holding the right outer edge and pulling outward.
3. Press left on the two latches located on the inner metal door and swing open to the left. See Figure 2-6 for latch locations.

4. If the power supply board is to be replaced, complete steps 5 and 6; if not, proceed to step 7.

5. Remove the two screws located at the top and bottom of the power supply shield (see Figure 2-7) and retain for installation.

6. Pull the power supply shield back at the top, and lift up to remove.

7. Using both hands, hold the part of the top and bottom ejector tabs that is toward the center edge of the board and pull away from the board. This step unseats the board connector from the backplane connector.

8. Pull the board straight out of the enclosure.

9. If you are going to replace a board, refer to the installation procedure.

Figure 2-6 **Chassis Door Latch**

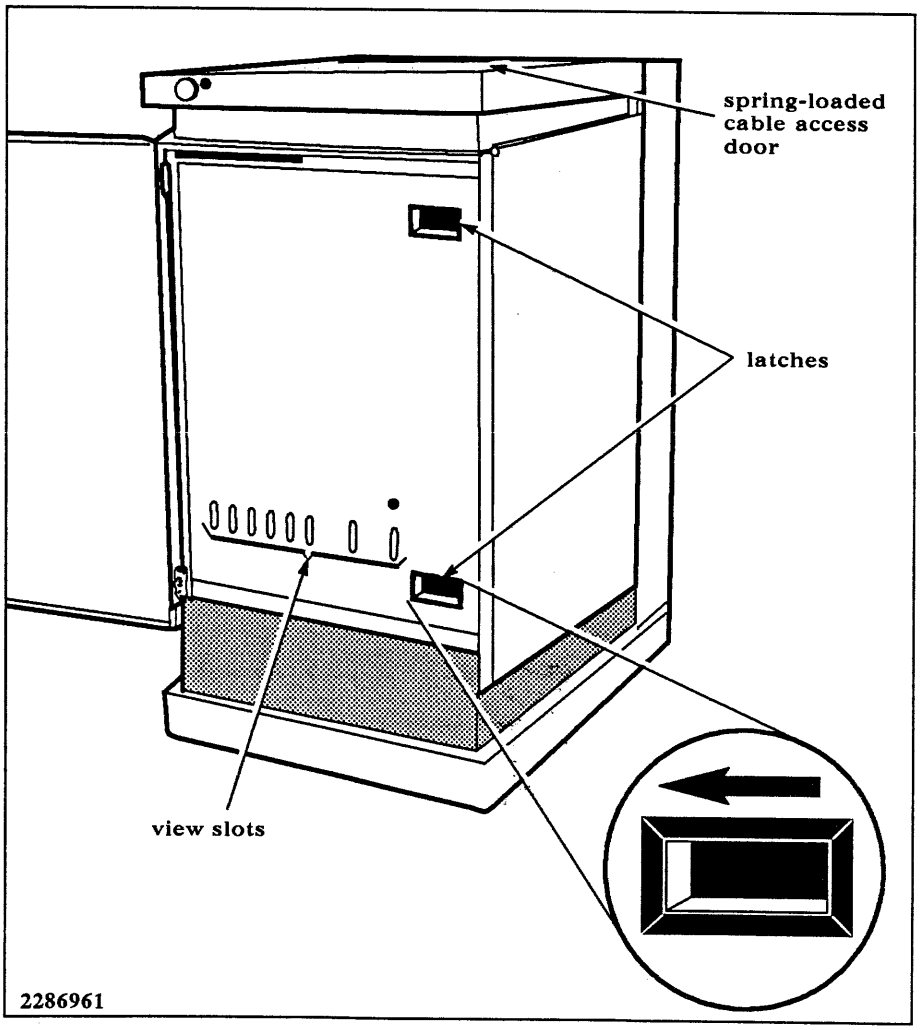
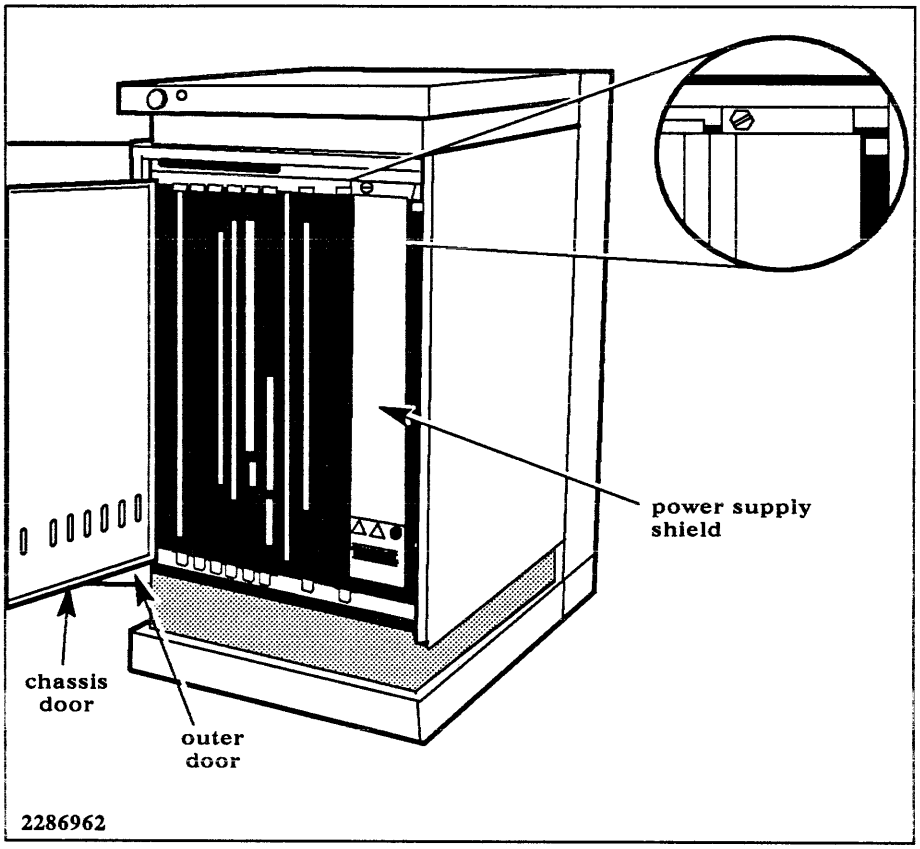


Figure 2-7 Power Supply Shield



Eurocard Circuit Board Installation

2.3.2 Use the procedure that follows to install the Eurocard circuit boards in the 7-slot enclosure.

NOTE: The power on/off switch is a spring-loaded push-button switch that is turned on or off by pressing and releasing the button. If the switch is in the off (0) position, pressing and releasing the switch places it in the on (1) position; if it is in the on position, pressing and releasing it places it in the off position.

WARNING: Ensure that power to the enclosure is off prior to installing Eurocard circuit boards.

1. Open the front enclosure door by holding the right outer edge and pulling outward. The door swings open to the left.

2. Press left on the two latches located on the inner metal door and swing open to the left. See Figure 2-6 for latch locations.

3. Determine the slot in which the board is to be installed. See Section 4 for slot selection.

4. Place the board on the guide track with connector P1 at the top, and slide the board back to the backplane connectors.

NOTE: The boards can be inserted in only one way (component side to the right when installed) to mate properly with the backplane connectors.

---

5. Using one hand on each injector tab, press down on the top injector and up on the bottom injector until they are flush with the front edge of the board. This step properly seats the board into the backplane connector.

6. Close the inner metal door by pushing the door inward until the two latches snap closed. (Press firmly near each latch to ensure complete closure of the door.)

NOTE: The inner metal door must be fully closed to ensure EMI integrity and to activate the interlock switches so that power can be applied.

---

7. Close the outer enclosure door.

NOTE: If the installed Eurocard circuit board requires a cable adapter, refer to paragraph 2.4, Installation of Option Boards and Adapters.

---

8. Set the enclosure power on/off switch to the on (in) position.

Installation of Option Boards and Adapters

2.4 A variety of option boards and adapters are used with the Explorer 7-slot system enclosure. Table 2-2 lists four classifications of the option boards and adapters.

The installation information for the option boards and the adapters that appear in this manual are typical examples only. Table 2-3 lists the option boards and adapters with their associated installation reference documents. Refer to these reference documents if you need to remove or install any of the option boards and/or adapters.

Table 2-2 Classifications of Option Boards and Adapters

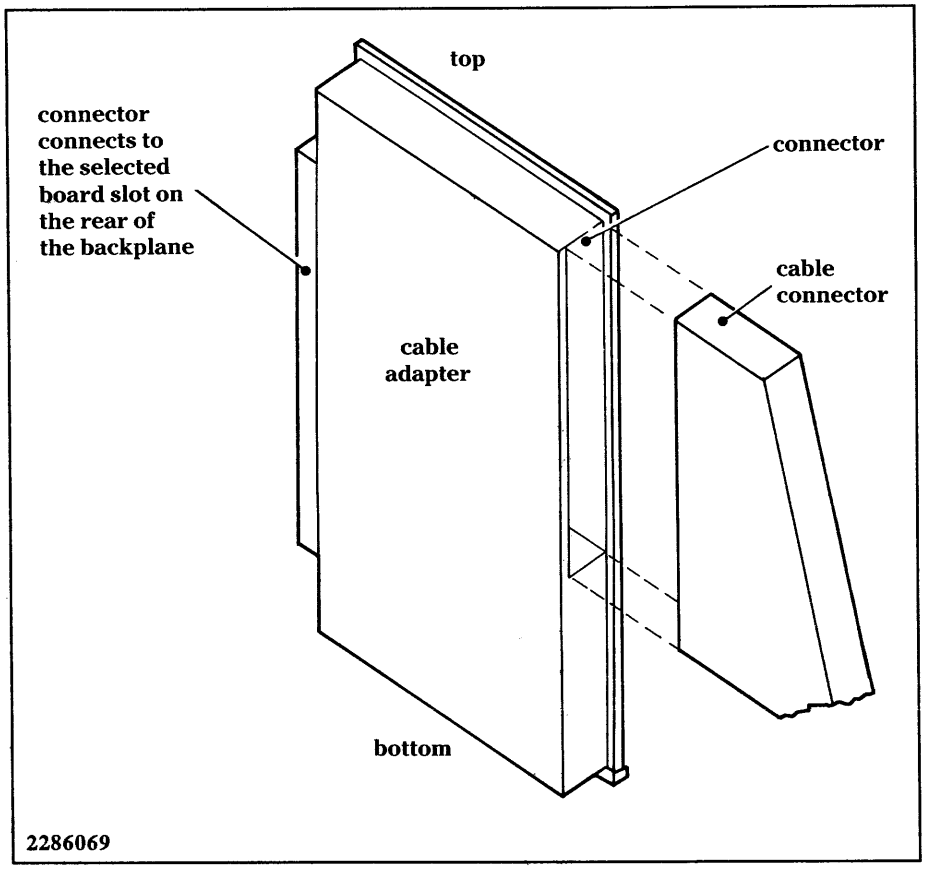
Classification	Description
Piggyback option boards	These are option boards that plug into the Eurocards in a piggyback manner.
Backplane option boards	These are option boards that plug into the rear of the backplane without any cables attached.
Backplane adapters	These are adapters that plug into the rear of the backplane without any cables attached.
Backplane cable adapters	These are adapters that plug into the rear of the backplane and connect to interface cables.

Table 2-3 Installation Reference Information for Option Boards and Adapters

General Categories	Types of Option Boards and Adapters	Installation Reference Documents
Piggyback option boards	68020-based processor, 2-megabyte option board	68020-Based Processor General Description
	Communications carrier board option boards	Communications Carrier Board and Options General Description
Backplane option boards	Explorer II processor auxiliary processor options	Explorer II Processor and Auxiliary Processor Options General Description
Backplane adapters	68020-based processor software protection adapter	68020-Based Processor General Description
Backplane cable adapters	Communications carrier board cable adapters	Communications Carrier Board and Options General Description
	Peripheral cable adapter (PCA)	Explorer NuBus Peripheral Interface (NUPI) General Description
	SMD/SCSI cable adapter	SMD/515-Megabyte Mass Storage General Description
	SMD cable adapter	SMD/515-Megabyte Mass Storage General Description
	Ethernet cable adapter	Explorer NuBus Ethernet Controller General Description
	Fiber-optic cable adapter	Explorer System Interface General Description

A typical cable adapter (Figure 2-8) consists of a PWB with a connector that plugs into the shrouded long pins on the rear side of the backplane. After the cable adapter is connected to the backplane, the interface cable from the interface is connected. Each cable adapter is configured for the type of Eurocard circuit board installed in the enclosure.

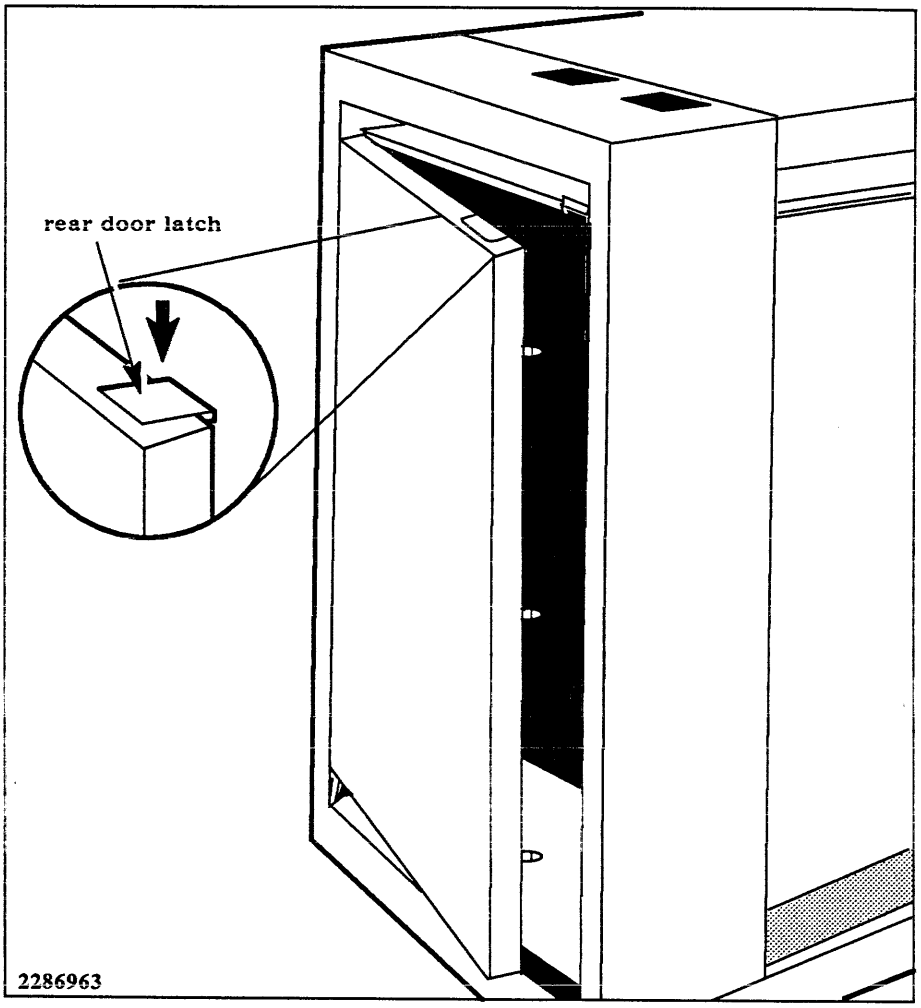
Figure 2-8 **Typical Cable Adapter**



WARNING: Before accessing the backplane, ensure that the power is turned off.

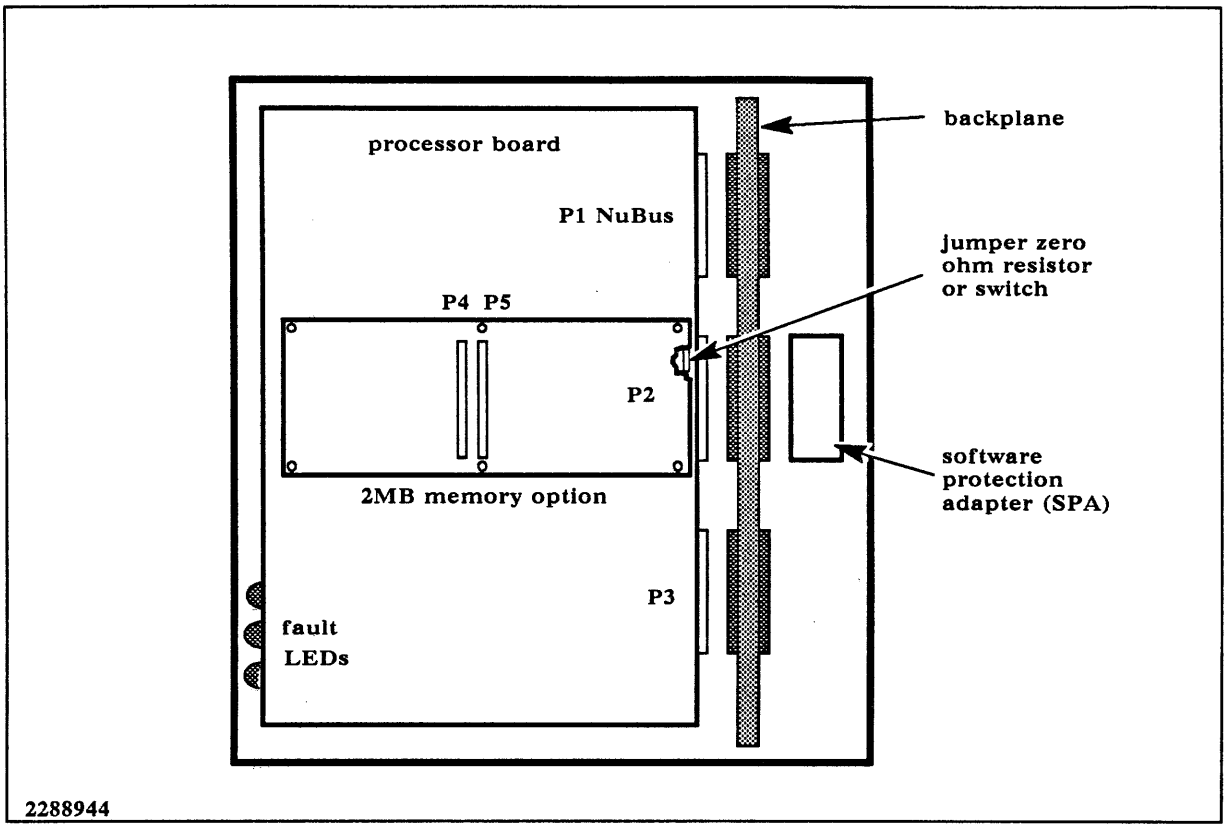
To access the rear side of the backplane, open the rear door by pressing down on the latch (Figure 2-9) located on the right top edge of the door and pulling outward. Two safety interlock switches are installed to shut off the power to the enclosure when the rear door is opened.

Figure 2-9 **Rear Door Latch**



When optional equipment is used with the Explorer, additional adapters, cable adapters, and option boards can be installed in rows 2 and 3, slots 0 through 5, on the rear of the backplane. A typical example of this optional equipment is the installation of the 2-megabyte memory option board and the software protection adapter shown installed in Figure 2-10.

Figure 2-10 68020-Based Processor Option Board and Adapter Installation



Cable Routing

2.5 The enclosure is designed for cables to be routed either through the top of the enclosure or through the bottom. The spring-loaded cable access panel on the rear side of the top cover can be pushed back to route the power cords from the display monitor and mass storage unit (MSU) to the auxiliary receptacles located on the motor power supply cover. Other cables can also be routed through this spring-loaded cable access panel, or they can be routed through the cable security tie-wrap system at the bottom of the rear door, where they can be securely tied in place. Figures 2-11 and 2-12 show the typical routing of system cables.

NOTE: The two auxiliary ac power receptacles are present only on early models of the enclosures that have the 80-ampere power supply.

Figure 2-11 Cable Routing With 80-Ampere Power Supply and Two MSUs

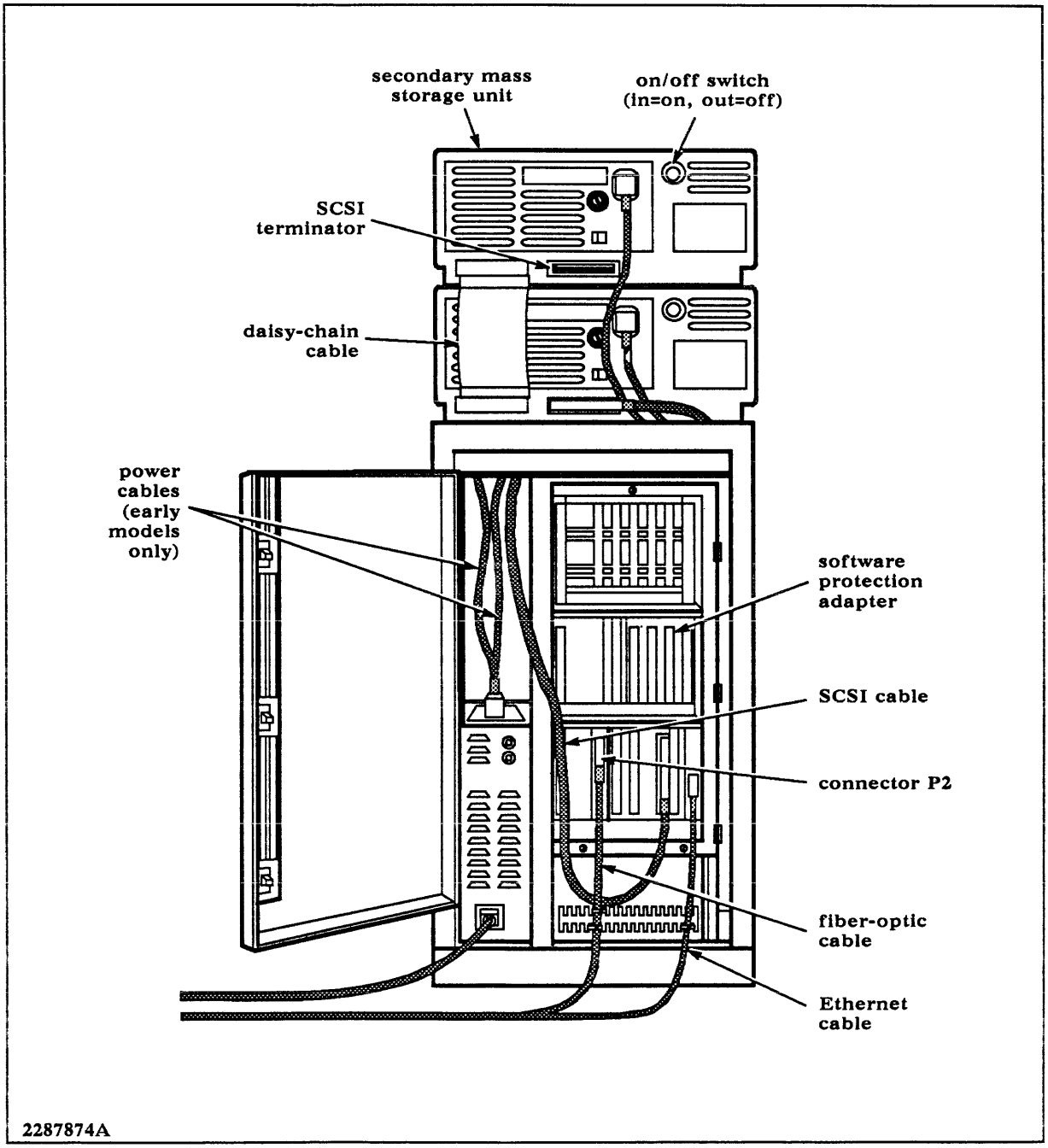
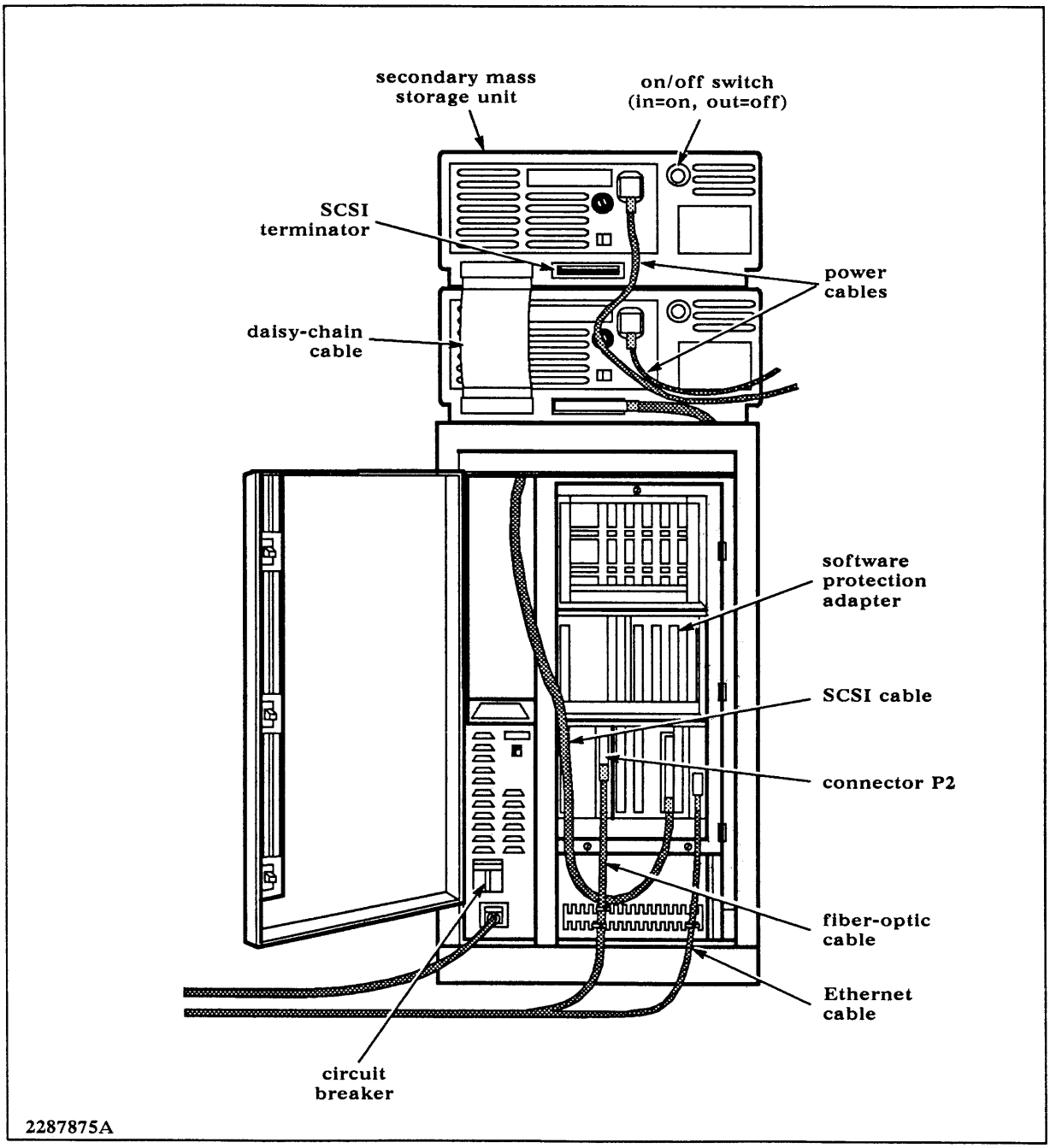


Figure 2-12 Cable Routing With 110-Ampere Power Supply and Two MSUs



Operation

2.6 Early models of the 7-slot enclosure with the 80-ampere power supply have the capability of performing a complete system shutdown. If the display monitor and the MSU are plugged into the auxiliary ac power receptacles located on the motor power supply cover, the single on/off switch (Figure 2-13) on the enclosure controls power to the entire system.

In a system with the 110-ampere power supply, there are no auxiliary ac power receptacles on the power interface board cover; therefore, ac power must be controlled at each component in the system.

This section provides information on the following topics:

- Power-up procedures
- Power-down procedures
- Fault indicators

Power-Up Procedure

2.6.1 The power-up procedure for the 7-slot enclosure consists of the following steps:

1. Ensure that the power cable is plugged into the correct power outlet.

NOTE: If the display monitor and the MSU are plugged into the 7-slot enclosure auxiliary receptacles provided with the 80-A power supply, ensure that their power switches are set to the on position. If these units are connected to other receptacles, ensure that the units are powered up prior to applying power to the enclosure.

---

2. Ensure that the power to the enclosure is on.

NOTE: During power-up, the system performs a diagnostic test and displays the results on the video display. As each board passes self-test, the red LED located on the board goes out.

---

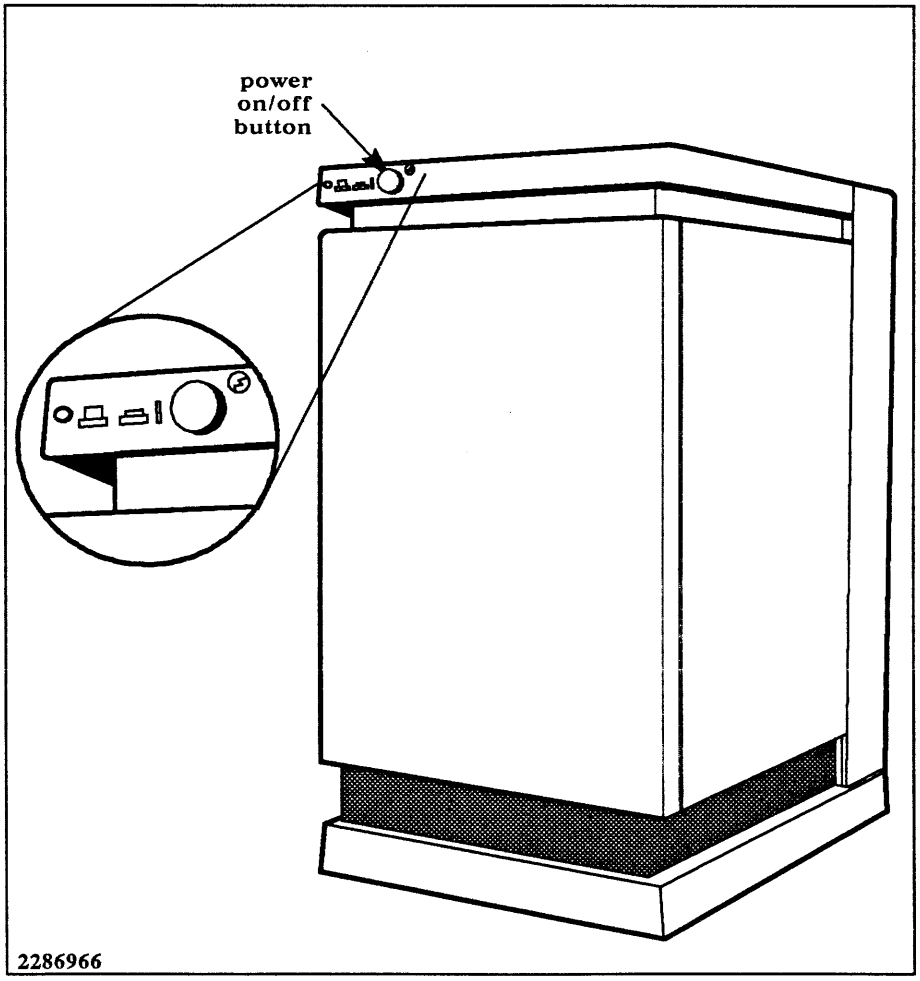
3. Verify that the fan is operating. If the fan fails to start, make sure that ac power is available to the enclosure.

CAUTION: Do not operate the enclosure if the fan is not working. A faulty fan can cause overheating and damage to the enclosure electronics.

Power-Down Procedure

2.6.2 To initiate the power-down procedure, place the enclosure on/off switch in the off (out) position. If the display monitor and MSU are plugged into the auxiliary receptacles on the enclosure, power is removed from these units when the enclosure power is removed. If the auxiliary receptacles are not used, power must be removed at each peripheral device.

Figure 2-13 **On/Off Switch**



Fault Indicators

2.6.3 Fault indicator LEDs are located on the front edges of the circuit board. At power-up, the LEDs are lighted; then, as each board passes self-test, the LED goes out. If a red fault LED remains on, that board has failed self-test. The other indicators on the boards are used by technical personnel for failure information. Even though a board fails self-test, the system may still operate at a reduced capability. If the processor fails in single processor systems, the system does not operate.

Preventive Maintenance

2.7 For efficient operation, cooling air must be supplied to the circuit boards and the power supply. If the filter clogs with dust, airflow is restricted and the electronic components can then overheat. If the filter loses its filtering ability, dust can enter the enclosure, thereby decreasing cooling efficiency.

The following preventive maintenance procedures, which are discussed in the next paragraphs, are recommended for an office environment:

- Clean the enclosure as needed.
- Clean the air filter after six months.
- Replace the air filter once a year.

CAUTION: Carefully monitor the condition of the air filter. Set up a schedule for more frequent cleanings and filter replacements if the filter collects excess dust between scheduled cleanings and/or replacements. Dust buildup can lead to overheating, accelerated aging, and reduced reliability.

Enclosure Cleaning

2.7.1 Keep the enclosure clean and dust-free by wiping the exterior with a damp (not wet) cloth and mild detergent.

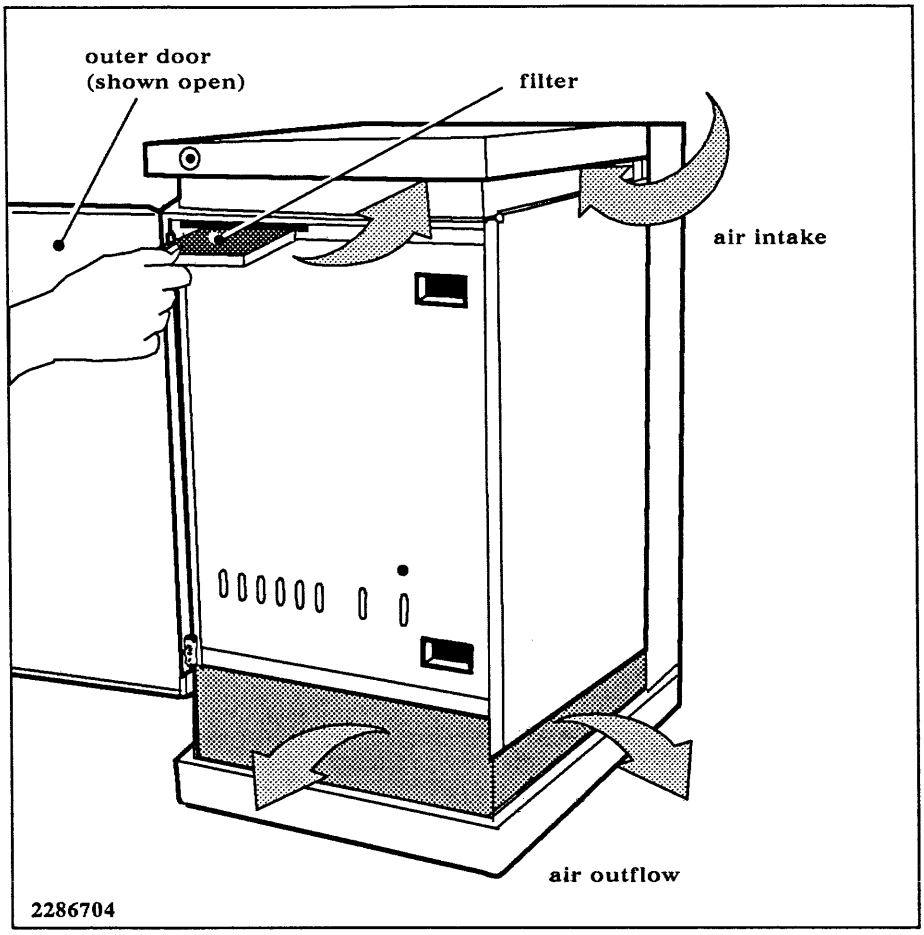
CAUTION: Do not use strong detergents, cleaners, or solvents to clean the enclosure.

Air Filter Service

2.7.2 Refer to Figure 2-14 for the air filter location. To replace the air filter, perform the following steps:

1. Turn off the power to the enclosure.
2. Open the front door to the enclosure. The filter is located in the slot at the upper left corner above the chassis assembly.
3. Hold the tab on the air filter and pull straight away from the slot.
4. Insert the new filter in the slot with the tab out, and push straight inward.
5. Close the enclosure door.
6 Turn the power back on.

Figure 2-14 **Air Filter Replacement**



3 EQUIPMENT DESCRIPTION

Introduction

3.1 This section contains information on the following topics:

- Enclosure slot configurations
- Backplane configurations
- 80-ampere power supply subsystem
- 110-ampere power supply subsystem

Enclosure Slot Configurations

3.2 Typical enclosure slot configurations for the Explorer 7-slot enclosure are shown in Figures 3-1 through 3-4. The following general guidelines apply to enclosure slot configurations:

- The term *local bus backplane* refers to a backplane with a NuBus, a local bus, and I/O connectors.
- The term *NuBus-only backplane* refers to a backplane with only a NuBus and I/O connectors.
- Explorer systems with a local bus backplane can use either an 80-ampere or a 110-ampere power supply. Explorer systems with a NuBus-only backplane normally have the 110-ampere power supply. Normally, all Explorer LX systems use the 110-ampere power supply.
- *Explorer I processor* refers to the original two-board processor assembly. This processor must be in slot 6 in an enclosure with the local bus backplane. An 8-megabyte (2243910) memory board must be in slot 4 when the Explorer I processor is used. Additional 8-megabyte or 32-megabyte (2540835) memory boards can be installed in any slot.
- *Explorer II processor* refers to the single-board processor that uses the Explorer Lisp microprocessor chip. This processor will operate in any slot, but should be placed in slot 6 due to board cooling requirements. The Explorer II processor does not use the local bus; however, it will operate in slots with an active local bus without interference.
- The system interface board is normally in slot 5 in systems with the local bus backplane. It will operate in any slot in systems with the NuBus-only backplane.
- The NuBus Ethernet controller and the 32-megabyte memory board will operate in any slot in the system.
- All other circuit boards that use connector P2 for I/O operations must be in a slot without the local bus.

Figure 3-1 Typical Explorer System With Local Bus Backplane

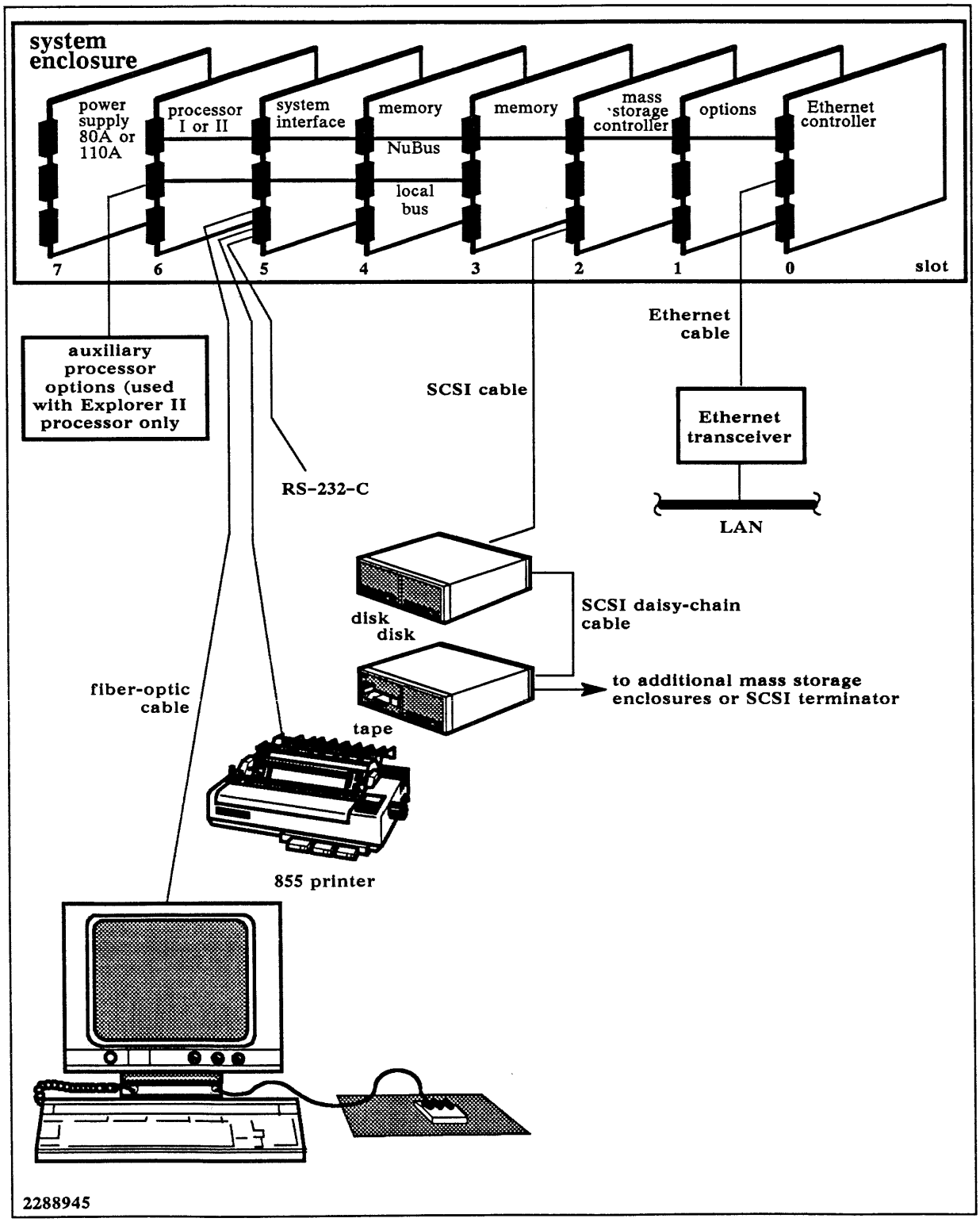


Figure 3-2 Typical Explorer LX System With Local Bus Backplane

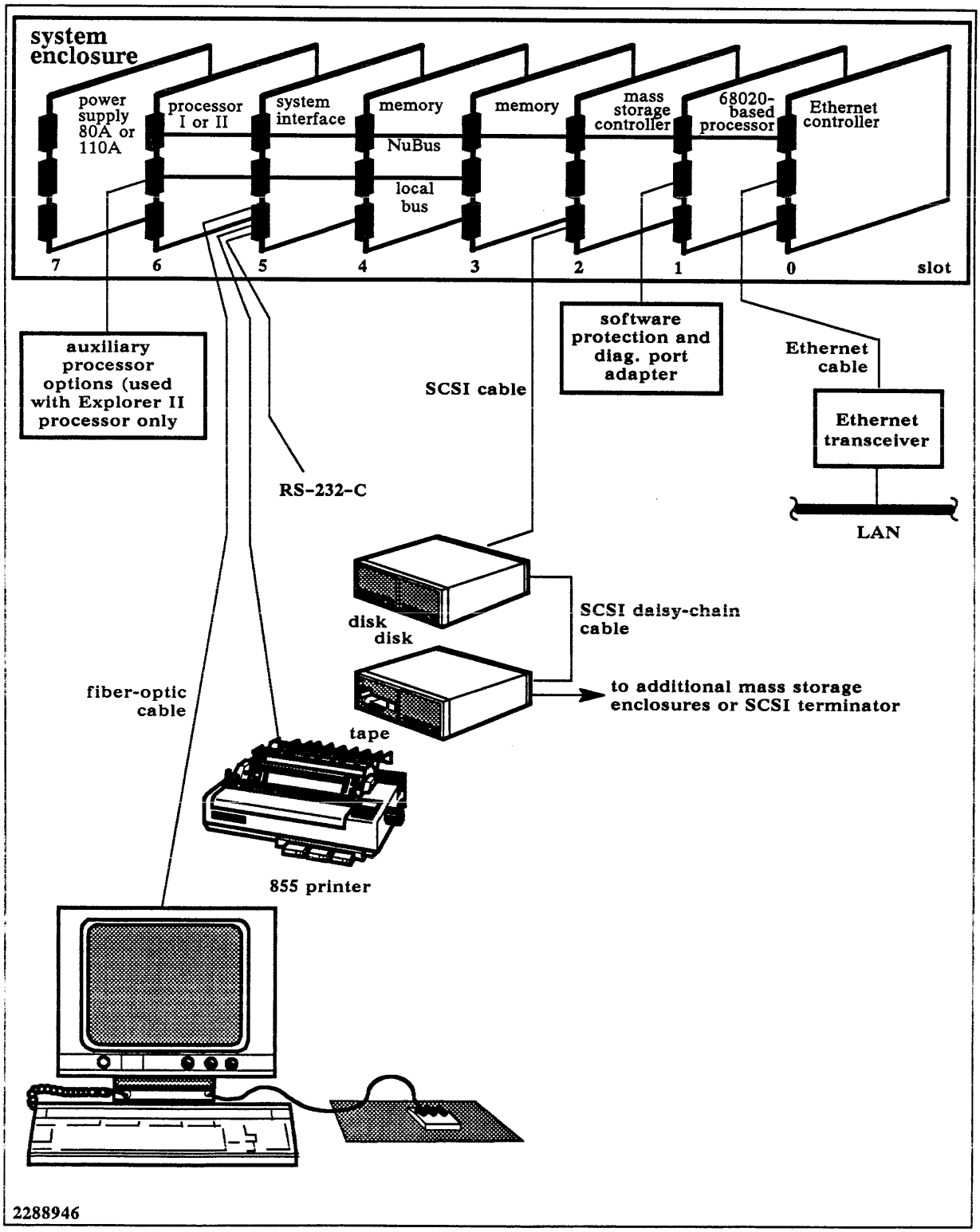


Figure 3-3 Typical Explorer II System With NuBus-Only Backplane

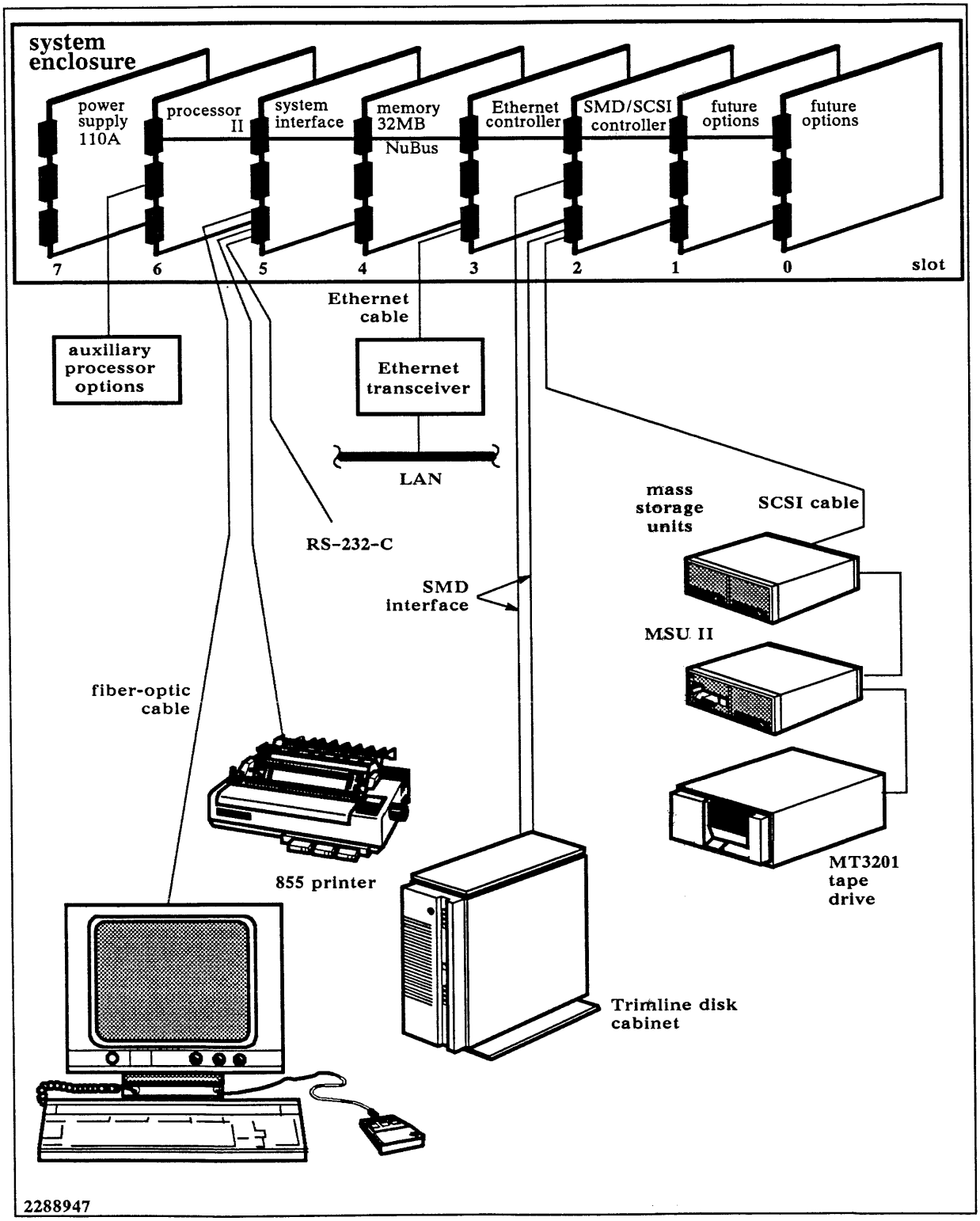
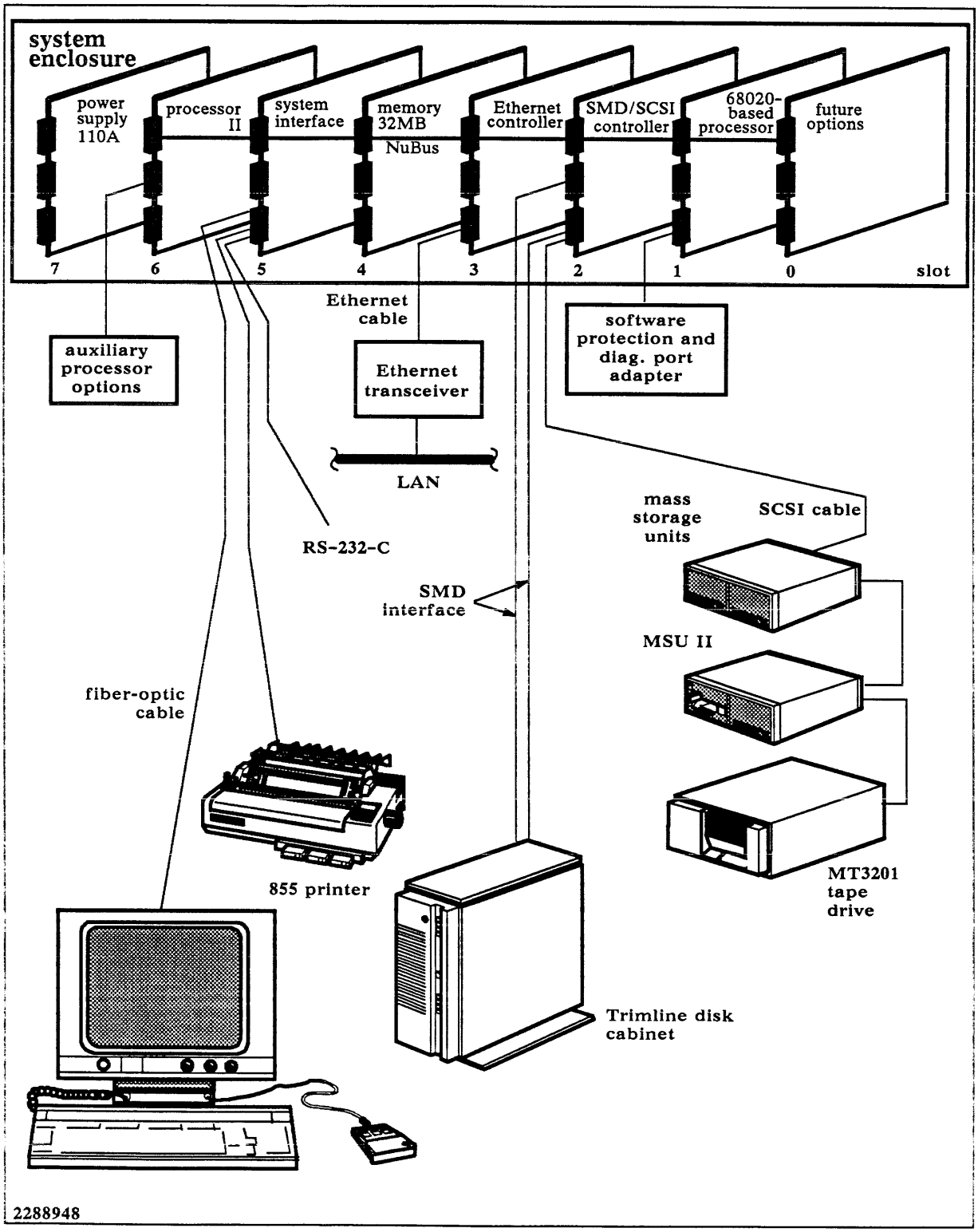


Figure 3-4 Typical Explorer II LX System With NuBus-Only Backplane



Backplane Configurations

3.3 The backplane is a printed wiring board (PWB) that provides power planes, signal lines, and signal ground planes. The local bus backplane and the NuBus-only backplane are shown in Figures 3-5 and 3-6. Both backplanes contain eight columns and three rows of DIN 41612 96-pin female connectors. Seven columns (slots 0 through 6) are provided for system circuit boards. An eighth column is provided for the power supply board.

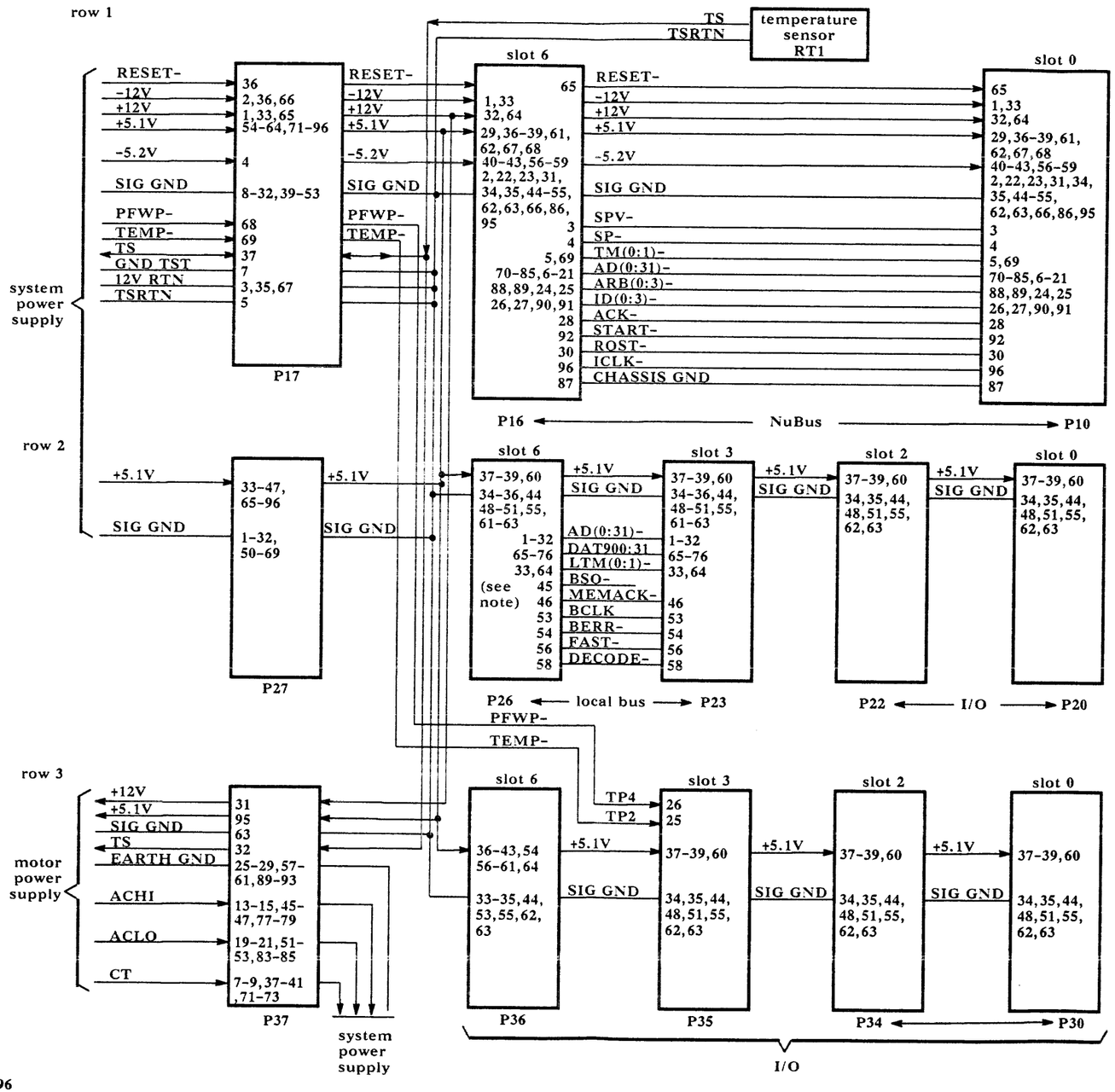
Slots 0 through 6 in row 1 are reserved for the NuBus on both backplanes. The local bus occupies slots 3 through 6 in row 2. Slots 0 through 2 in row 2 are reserved for I/O ports. Slots 0 through 6 in row 3 are reserved for I/O ports in both backplanes. The motor power supply is inserted in the connector in row 3 of the eighth column on the rear side of both backplanes.

The 96-pin DIN connectors use an alphanumeric pin numbering scheme. The pin numbers are stamped on the body of the connector. The numbers 1 through 32 identify rows; the letters A, B, and C identify the three columns. Software requires a simple, sequential, numeric, pin-numbering system in the input/data files. Table 3-1 lists the conversion from alphanumeric to sequential numeric. Columns 1A through 32A become 1 through 32; columns 1B through 32B become 33 through 64; and columns 1C through 32C become 65 through 96.

The NuBus terminators associated with the local bus backplane and the NuBus-only backplane are listed in the following chart. The NuBus clock is available from the system interface board (SIB) or terminator, TI part number 2249565-0001. When both clock sources are available in the same chassis, the SIB clock is disabled.

Backplane Usage	NuBus Terminator Part Numbers	Description
Local bus backplane	2243885-0001	Clock termination
	2243885-0002	NuBus termination only
NuBus-only backplane	2249565-0001	NuBus clock logic
	2249565-0002	NuBus termination only

Figure 3-5 Backplane Configuration With NuBus and Local Bus



2287096

NOTE:
Signal BSO- connects to pin 45 in slots 4, 5, and 6 only.

Table 3-1

Pin Number Conversion

Row	Columns A	B	C
1	1	33	65
2	2	34	66
3	3	35	67
4	4	36	68
5	5	37	69
6	6	38	70
7	7	39	71
8	8	40	72
9	9	41	73
10	10	42	74
11	11	43	75
12	12	44	76
13	13	45	77
14	14	46	78
15	15	47	79
16	16	48	80
17	17	49	81
18	18	50	82
19	19	51	83
20	20	52	84
21	21	53	85
22	22	54	86
23	23	55	87
24	24	56	88
25	25	57	89
26	26	58	90
27	27	59	91
28	28	60	92
29	29	61	93
30	30	62	94
31	31	63	95
32	32	64	96

NOTES:

This conversion does not apply to the motor power supply or cable adapters that plug into the rear side of the backplane.

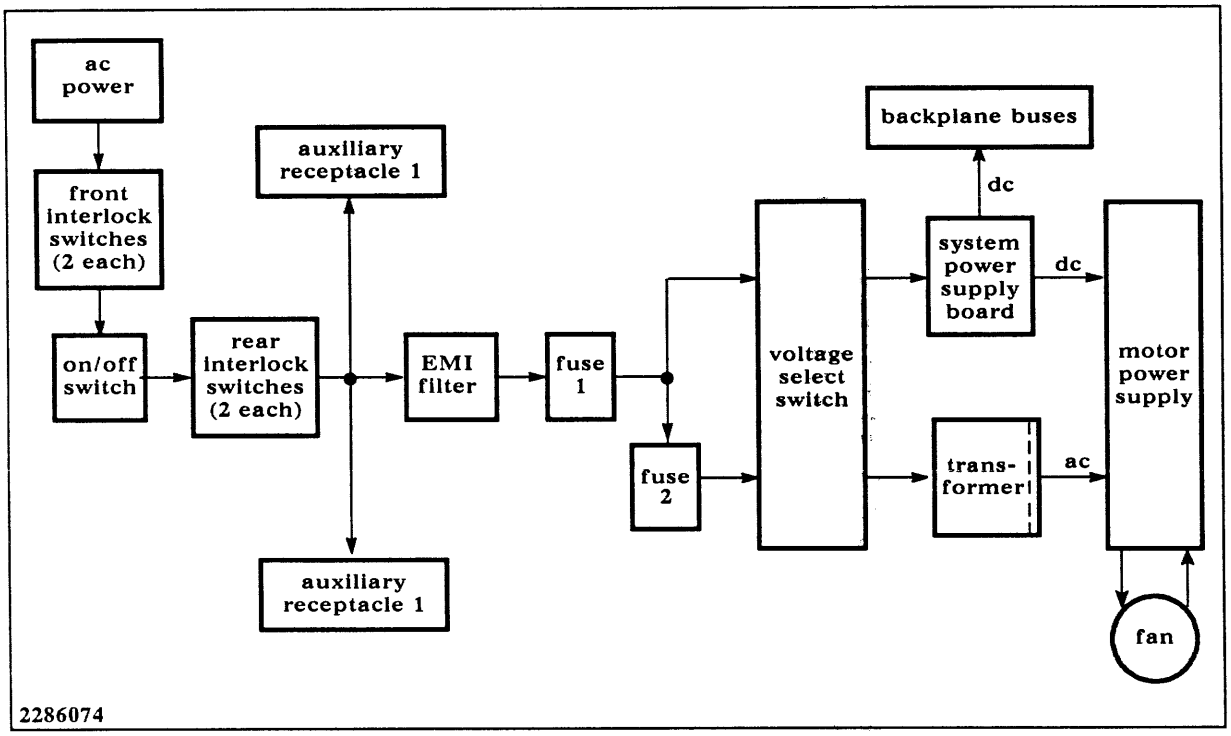
The actual lettering on the backplane in each column is numbers 1 through 32.

80-Ampere Power Supply Subsystem

3.4 Figure 3-7 shows a block diagram of the 80-ampere power supply subsystem. The ac power enters the enclosure at the motor power supply ac connector. From there it passes through four interlock switches to the on/off switch. On early models of the enclosure, two auxiliary receptacles tap off the ac power line at this point.

Power continues through an EMI filter on the motor power supply and two fuses to the voltage select switch. The ac voltage is then routed to the system power supply and the transformer. The system power supply then routes dc power to the backplane and the motor power supply. The secondary winding on the transformer supplies ac power to the motor power supply. The system power supply also has an EMI filter circuit.

Figure 3-7 80-Ampere Power Supply Subsystem Block Diagram

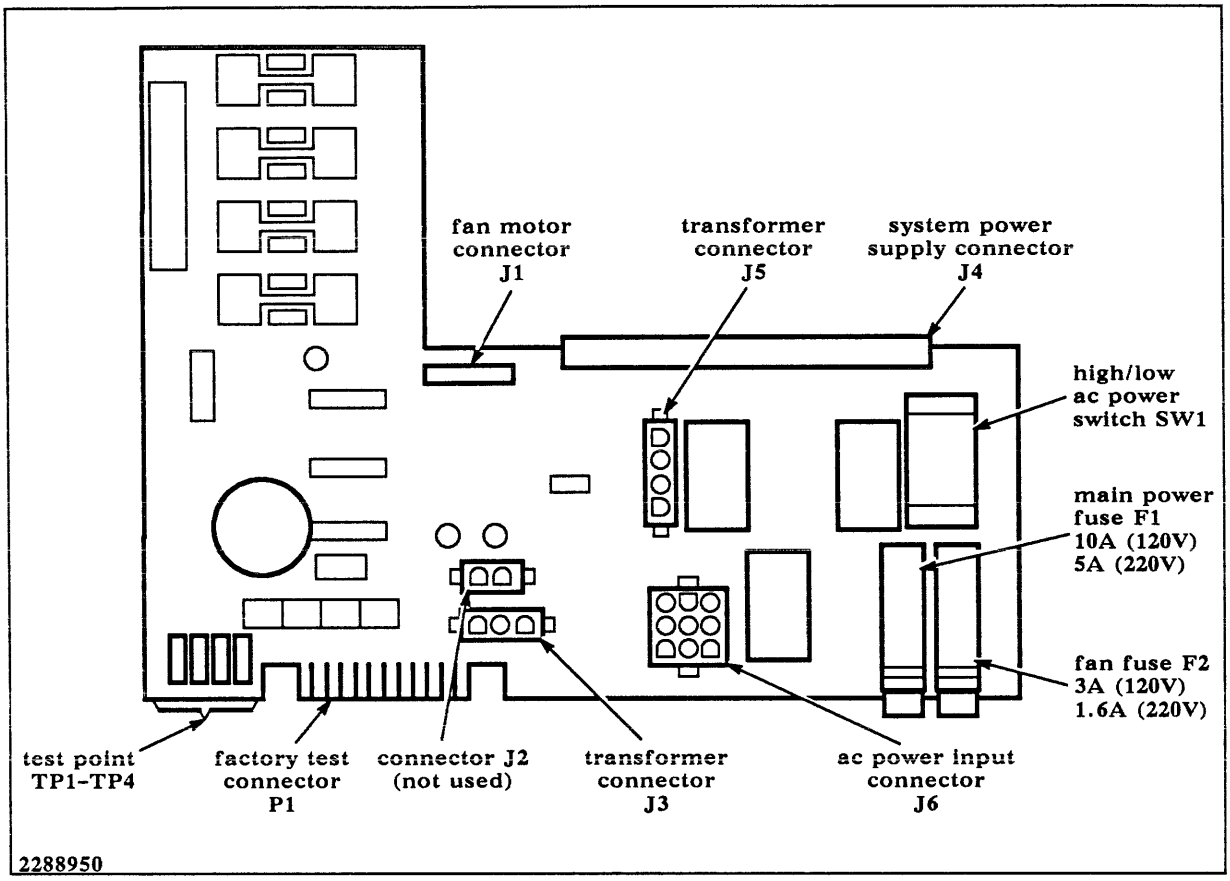


Motor Power Supply Board

3.4.1 The motor power supply (Figure 3-8), which is mounted behind the motor power supply cover (Figure 3-9), plugs into J37 on the backplane. The six connectors on the motor power supply are for the fan, transformer, auxiliary receptacles (when present), ac input, and system power supply. The test points on the motor power supply are as follows:.

Test Point	Location	Test
TP1	Top	Ground
TP2	Second from top	Current limit
TP3	Third from top	Fan motor dc/rpm
TP4	Bottom	Transformer output

Figure 3-8 Motor Power Supply



Fuse Replacement

3.4.1.1 The motor power supply has two fuses (see Figures 3-8 and 3-9) that protect the fan and the system. For fuse replacement, open the enclosure rear door, remove the fuse caps located on the motor power supply cover, and replace the blown fuse. For information on types of fuses to use, refer to Table 1-2 in Section 1.

Block Diagram

3.4.1.2 Figure 3-10 is a block diagram of the motor power supply. GND, TEMP, 5.1V, and 12V enter the variable speed circuitry and from there the signals are routed to the motor drive circuit. The signals for phases A, B, and C are routed to the fan motor. The fan motor sends S1, S2, and S3 signals to the logic circuitry, which in turn sends signals to the motor drive circuit.

Figure 3-9 **Motor Power Supply Location in the 7-Slot Enclosure**

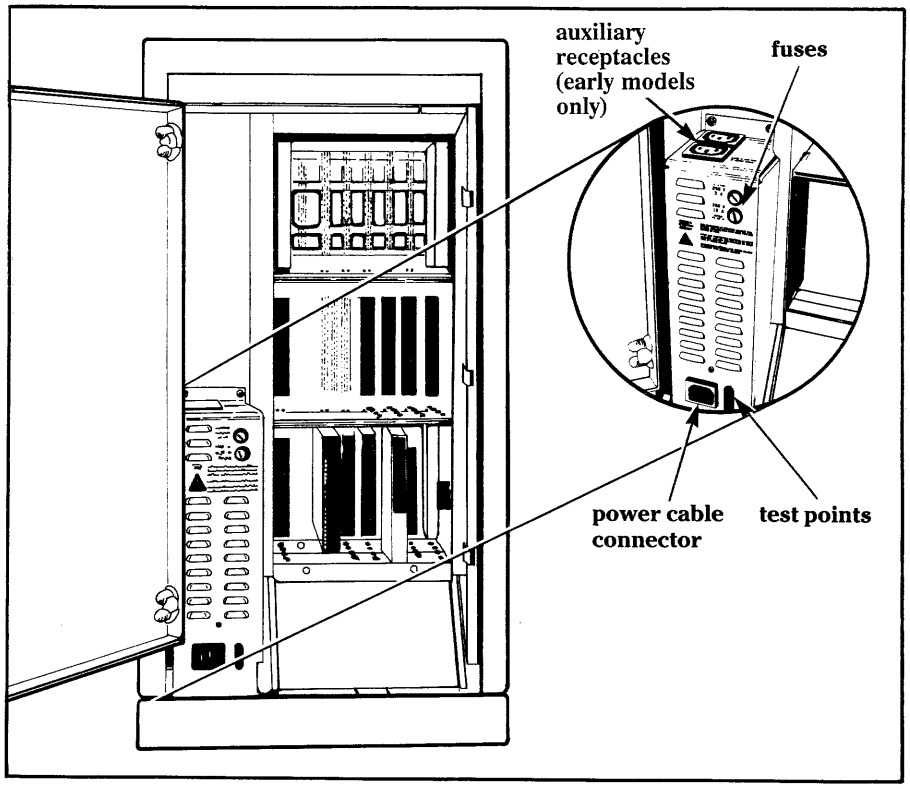
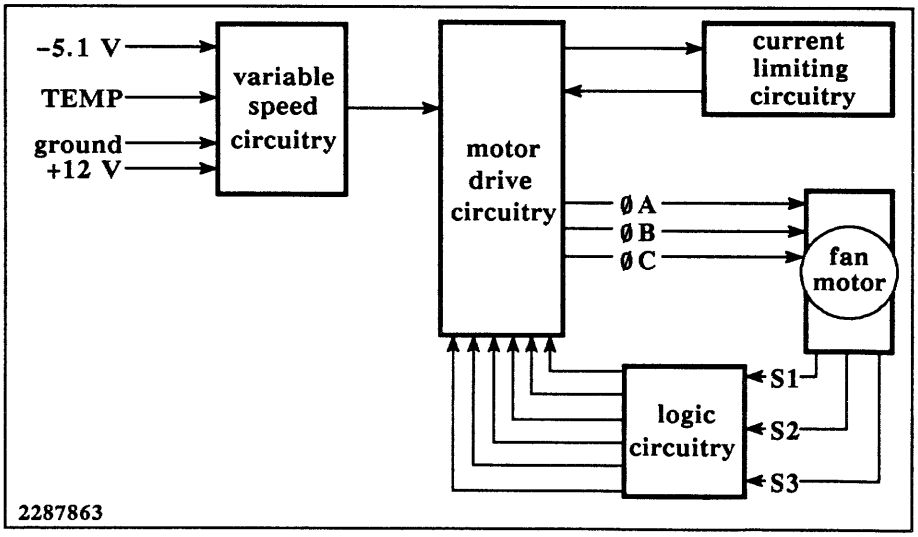


Figure 3-10 **Motor Power Supply Block Diagram**



80-Ampere Power Supply Board

3.4.2 The 80-ampere power supply board (Figure 3-11) is constructed on a standard three-high Eurocard. The input and output voltages and test point information for the 110-ampere power supply are as follows:

Item	Description
Input voltages	102 to 132 Vac, 47 to 63 Hz, at 12 A 187 to 264 Vac, 47 to 63 Hz, at 6.4 A
Output voltages	+5.1 Vdc (+/–3%) at 80 A (10 A minimum) +12 Vdc (+/–5%) at 1.0 A –12 Vdc (+/–5%) at 1.0 A –5 Vdc (+/–3% at 0.1 A
Test points on edge of board	TP8 — +12 Vdc TP7 — –12 Vdc TP6 — –5 Vdc TP5 — PFWP– TP4 — RESET– TP3 — TEMP– TP2 — +5 Vdc TP1 — GND

WARNING: Lethal voltages exist on the power supply board. Do not touch or handle the power supply until power has been disconnected for a minimum of one minute.

A block diagram of the 80-ampere power supply is shown in Figure 3-12. Figure 3-13 shows the complete power distribution for an Explorer system with an 80-ampere power supply subsystem.

Three control signals, RESET–, PFWP– (power failure warning pulse), and TEMP– (temperature), are generated by the power supply board. RESET– is active low until all supplies are stable for a minimum of 100 milliseconds; then it goes to active high. PFWP– is active low when a power shutdown is imminent. The power supply board is protected from short-circuit and overload conditions. TEMP– goes active low when the ambient temperature approaches a limit that will cause thermal shutdown. These signals provide protection for the enclosure whenever excessive temperature or excessive voltage is detected.

Thermal Protection

3.4.2.1 The power supply board monitors the airflow within the enclosure. A temperature sensor, which is mounted on the backplane, controls the amount of air flowing through the chassis by regulating the speed of the fan motor. An ambient temperature sensor is mounted on the power supply. When the temperature of this sensor approaches the critical operating temperature, a warning appears on the video display. If you do not turn the system off at this time and the temperature continues to increase, an automatic shutdown occurs.

WARNING: Do not use the neon lamp DS1, on the system power supply, as an indication of a satisfactory safety earth ground connection to the 7-slot system enclosure. Neon lamp DS1 indicates only that an unqualified earth ground path exists. Special instruments are required to determine if the earth ground connection is a qualified safety ground.

Safety Ground Detector

3.4.2.2 The safety ground detector is a neon light (see Figures 1-2 and 3-11) located on the power supply board. This light can be seen by looking through a view slot on the inner metal door. When power is turned on and a ground is present, the light is on. When power is on and a ground connection is missing, the light is off.

Overvoltage Protection

3.4.2.3 The voltage monitor circuit is set to cut off power for voltage inputs above 140 Vac (low range) or 280 Vac (high range). The -5 and -12 volts use a zener diode type of protection circuit so that when the voltage falls below -5.6 or -13, the zener protection circuit clamps and creates a short that blows the fuse. The +12 volts also uses a zener protection circuit. If the +5-volt circuit rises above +6.4 volts, the zener protection circuit cuts off power to the system.

Figure 3-11 80-Ampere Power Supply

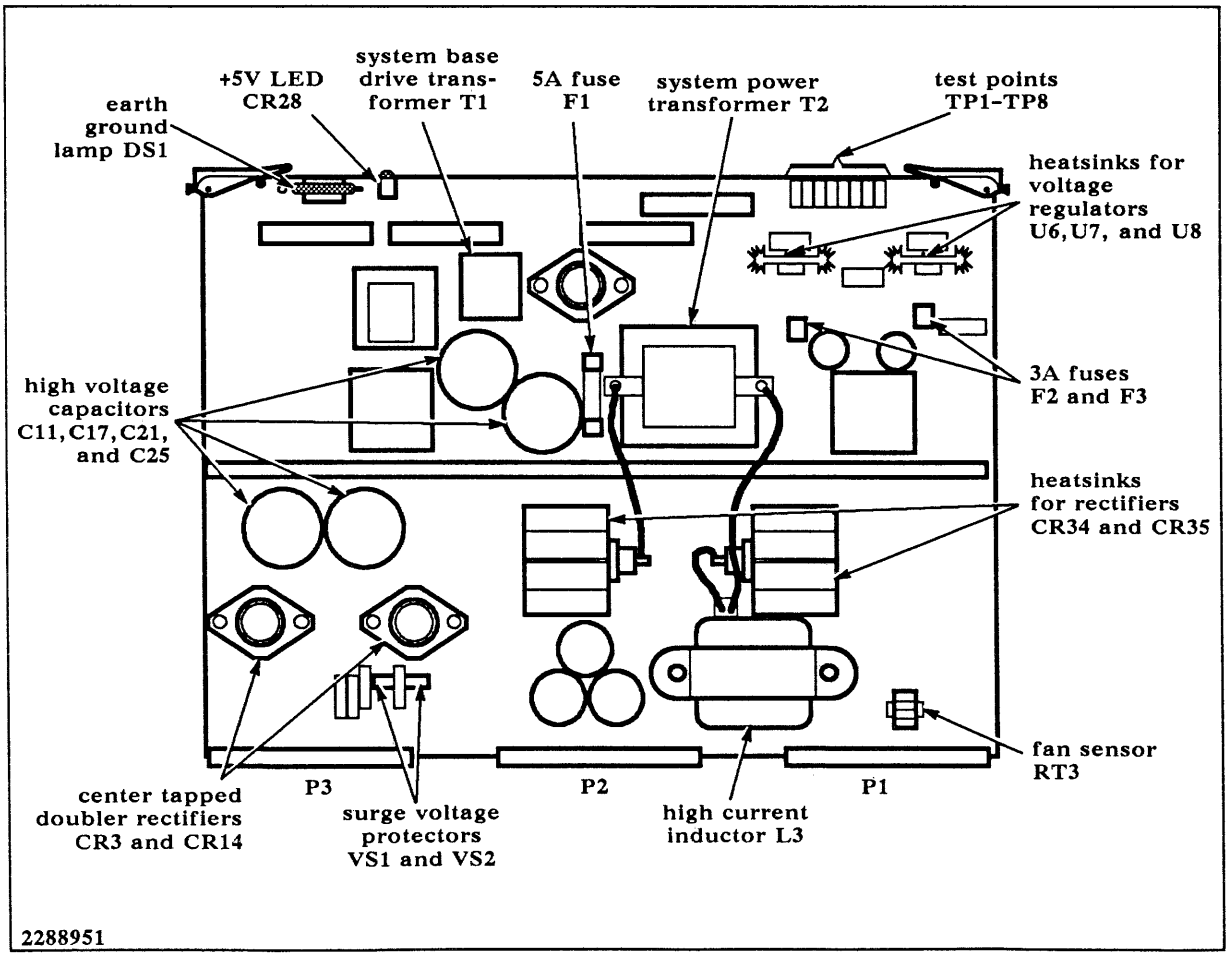
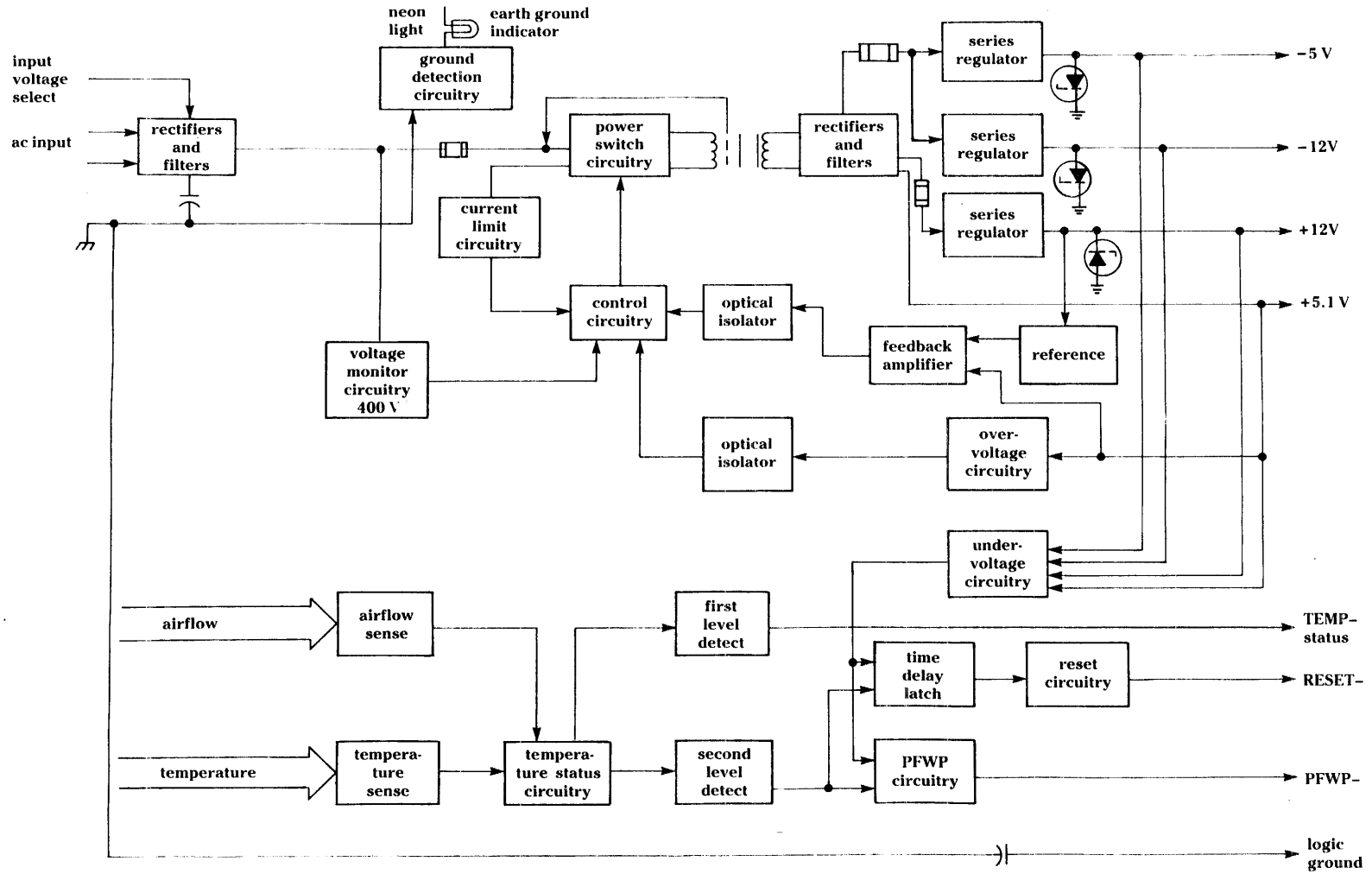
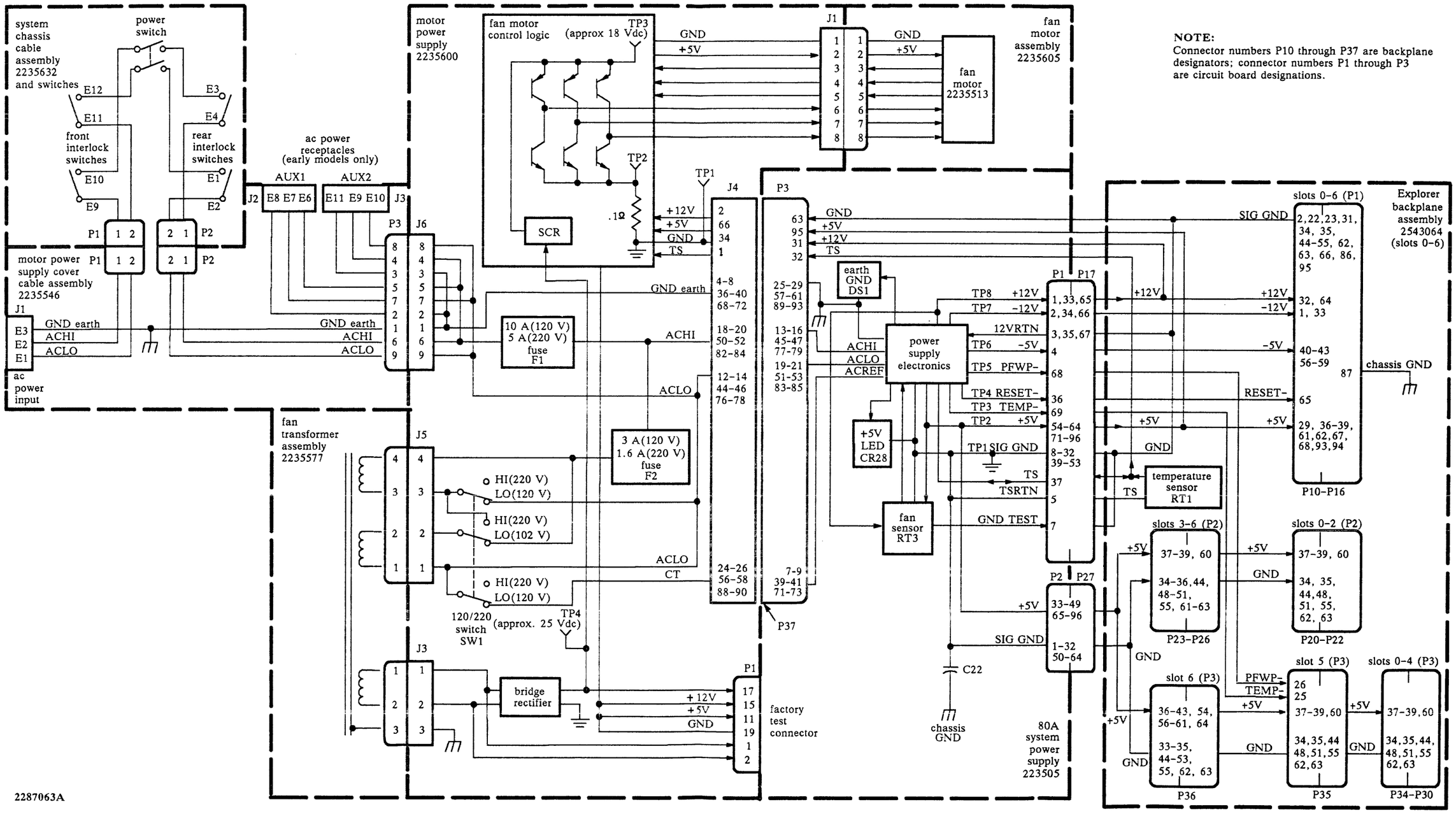


Figure 3-12 80-Ampere Power Supply Block Diagram



2287918

Figure 3-13 80-Ampere Power Supply/Local Bus Backplane Power Distribution



NOTE:
Connector numbers P10 through P37 are backplane designators; connector numbers P1 through P3 are circuit board designations.

Figure 3-15 Power Interface Board

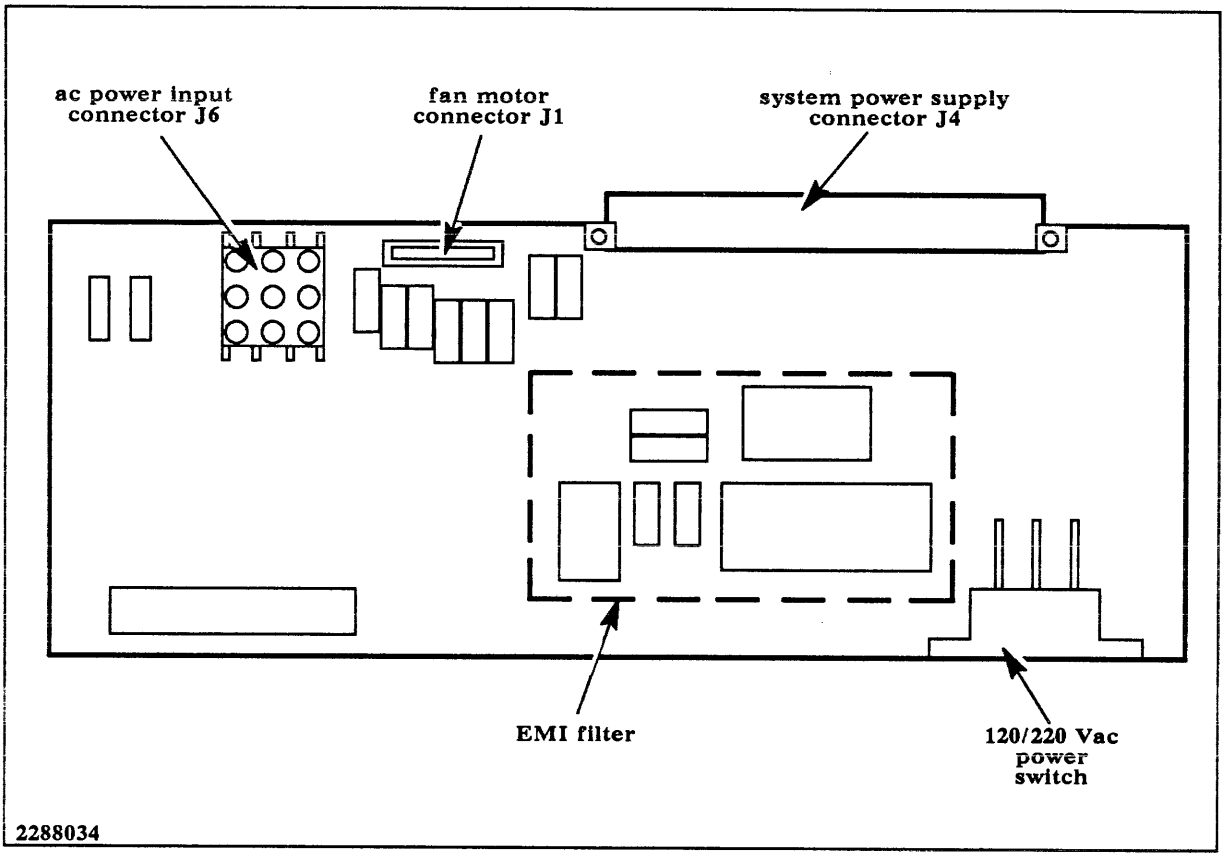
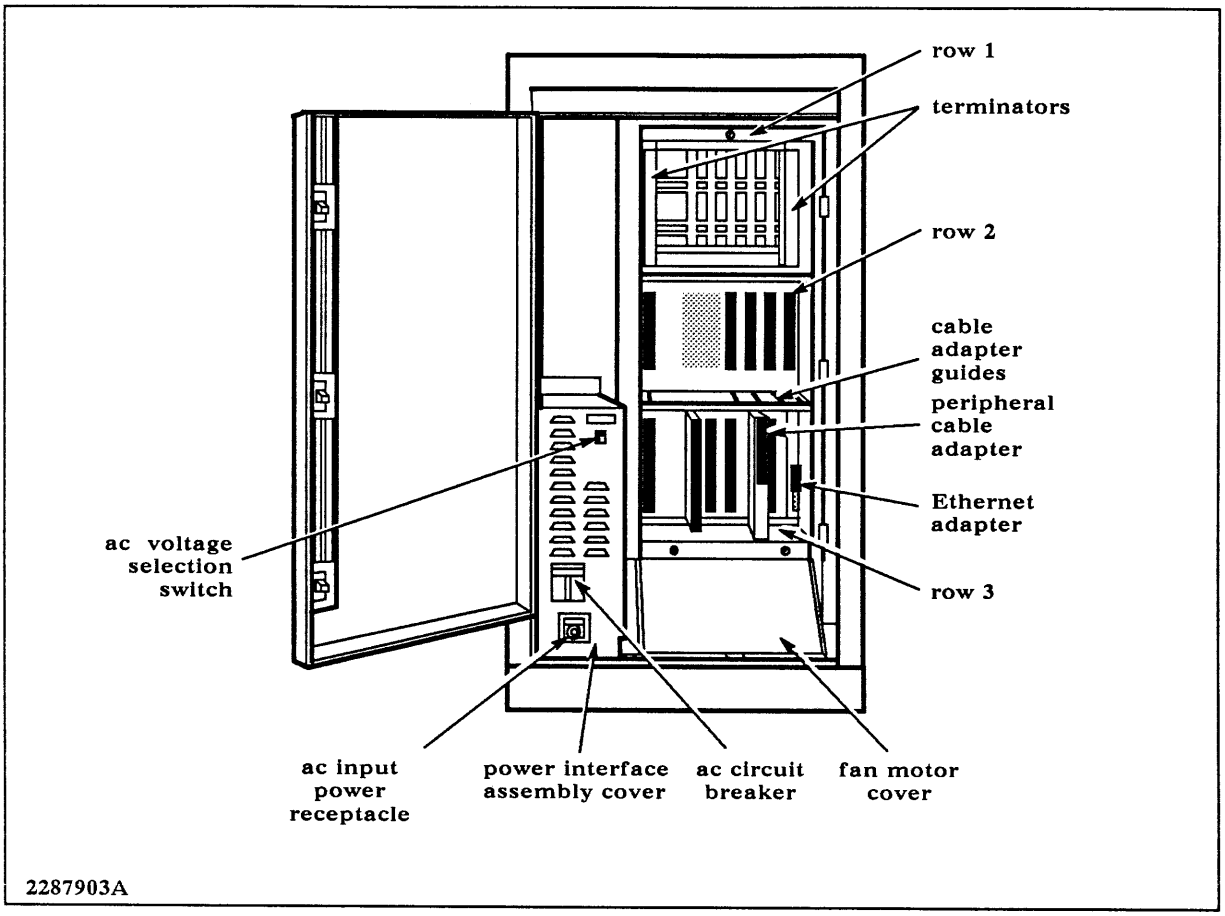


Figure 3-16 Power Interface Board Location

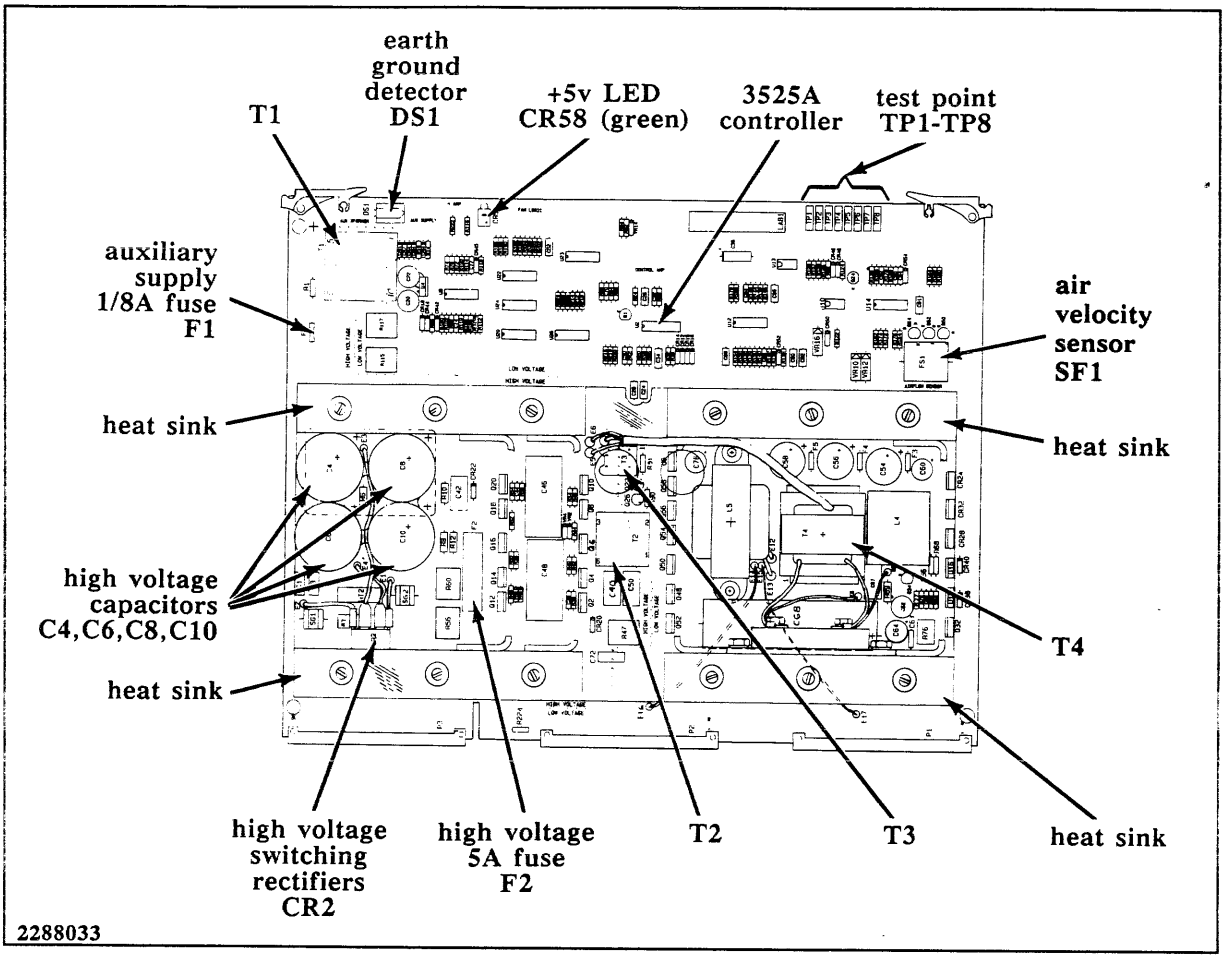


110-Ampere Power Supply Board

3.5.2 The 110-ampere power supply board (Figure 3-17) is constructed on a standard three-high Eurocard. The input and output voltages and test point information for the 110-ampere power supply are as follows:

Item	Description
Input voltages	102 to 132 Vac, 47 to 63 Hz, at 12 A 187 to 264 Vac, 47 to 63 Hz, at 6.4 A
Output voltages	+5.1 Vdc (+/–3%) at 110 A (10 A minimum) +12 Vdc (+/–5%) at 1.5 A –12 Vdc (+/–5%) at 1 A –5.2 Vdc (+/–3% at 4 A
Test points on edge of board	TP8 — +12 Vdc TP7 — –12 Vdc TP6 — –5 Vdc TP5 — PFWP– TP4 — RESET– TP3 — TEMP– TP2 — +5 Vdc TP1 — GND

Figure 3-17 110-Ampere Power Supply



A block diagram of the 110-ampere power supply is shown in Figure 3-18. Figure 3-19 shows the complete power distribution for an Explorer system with a 110-ampere power supply subsystem and a local bus backplane. Figure 3-20 shows the complete power distribution for an Explorer system with a 110-ampere power supply subsystem and a NuBus-only backplane.

Three control signals, RESET–, PFWP– (power failure warning pulse), and TEMP– (temperature), are generated by the power supply board. RESET– is active low until all supplies are stable for a minimum of 100 milliseconds; then it goes to active high. PFWP– is active low when a power shutdown is imminent. The power supply board is protected from short-circuit and overload conditions. TEMP– goes active low when the ambient temperature approaches a limit that will cause thermal shutdown. These signals provide protection for the enclosure whenever excessive temperature or excessive voltage is detected.

WARNING: Lethal voltages exist on the power supply board. Do not touch or handle the power supply until power has been disconnected for a minimum of one minute.

Thermal Protection

3.5.2.1 The 110-ampere power supply board monitors the airflow within the enclosure. A temperature sensor, which is mounted on the backplane, controls the amount of air flowing through the chassis by regulating the speed of the fan motor. An ambient temperature sensor is mounted on the power supply. When the temperature of this sensor approaches the critical operating temperature, a warning appears on the video display. If you do not turn the system off at this time and the temperature continues to increase, an automatic shutdown occurs.

WARNING: Do not use the neon lamp DS1, on the 110-ampere power supply, as an indication of a satisfactory safety earth ground connection to the 7-slot system enclosure. Neon lamp DS1 indicates only that an unqualified earth ground path exists. Special instruments are required to determine if the earth ground connection is a qualified safety ground.

Safety Ground Detector

3.5.2.2 The safety ground detector is a neon light (see Figure 3-17) located on the power supply board. This light can be seen by looking through a view slot on the inner metal door. When power is turned on and a ground is present, the light is on. When power is on and a ground connection is missing, the light is off.

Overvoltage Protection

3.5.2.3 The overvoltage circuit is set to cut off power for voltage inputs above 140 Vac (low range) or 280 Vac (high range). The −5 and −12 volts use a zener diode type of protection circuit so that when the voltage falls below −5.6 or −13, the zener protection circuit clamps and creates a short that blows the fuse. The +12 volts also uses a zener protection circuit. If the +5-volt circuit rises above +6.4 volts, the zener protection circuit cuts off power to the system.

Figure 3-18 110-Ampere Power Supply Block Diagram

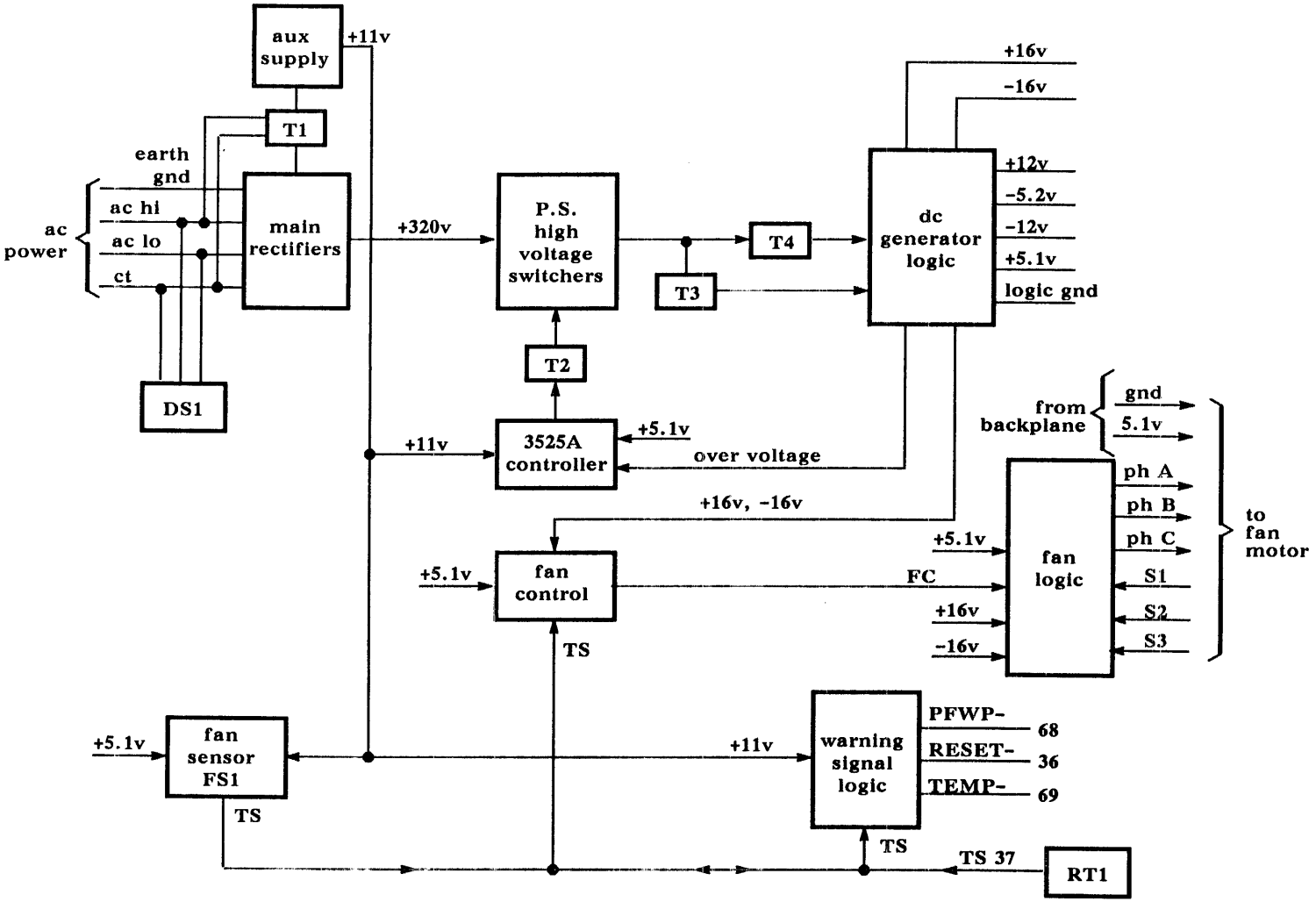
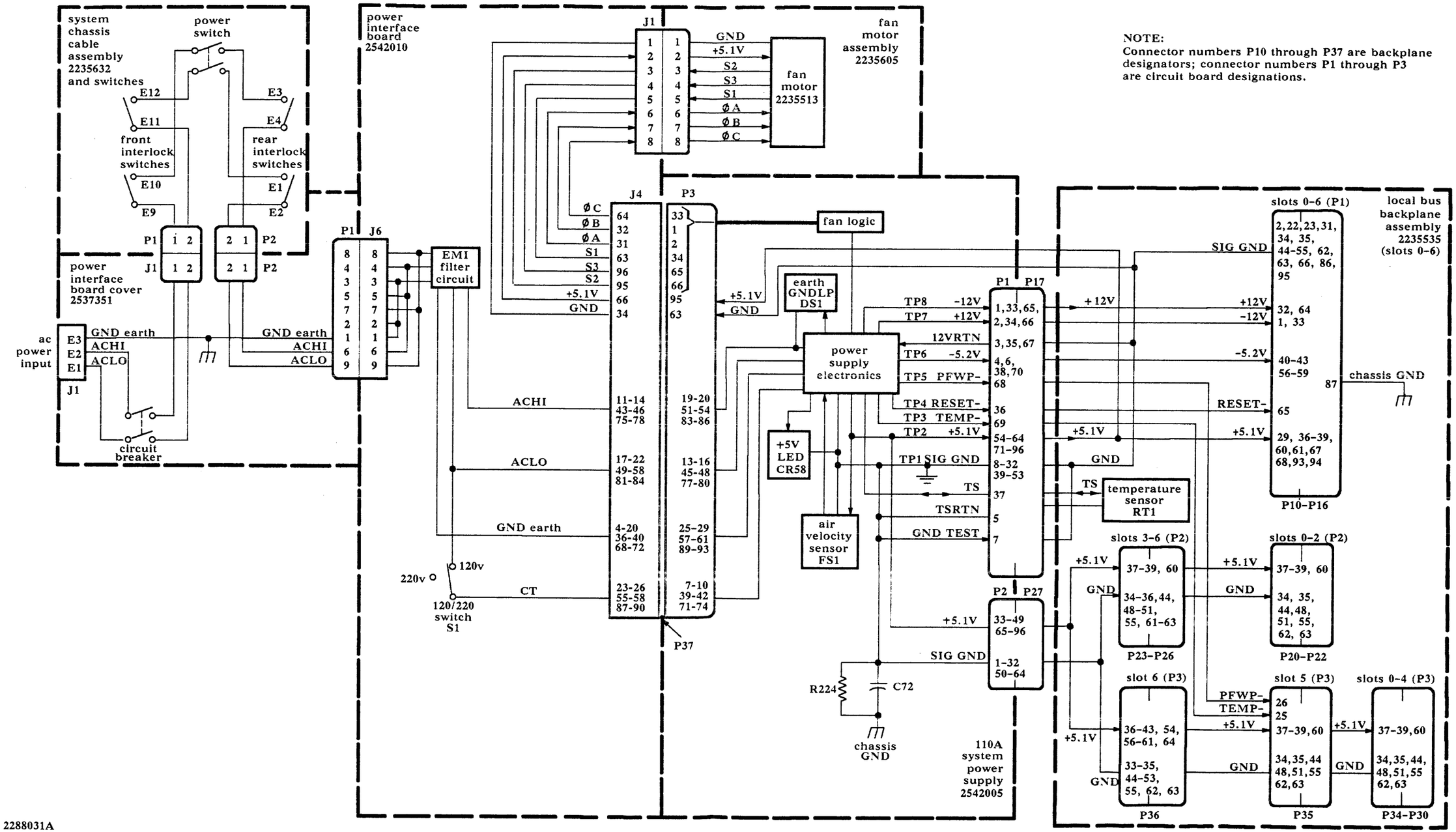


Figure 3-19 Power Distribution Diagram With 110-Ampere Power Supply and Local Bus Backplane



NOTE:
Connector numbers P10 through P37 are backplane designators; connector numbers P1 through P3 are circuit board designations.

2288031A

NUBUS SUMMARY

Overview of NuBus Elements

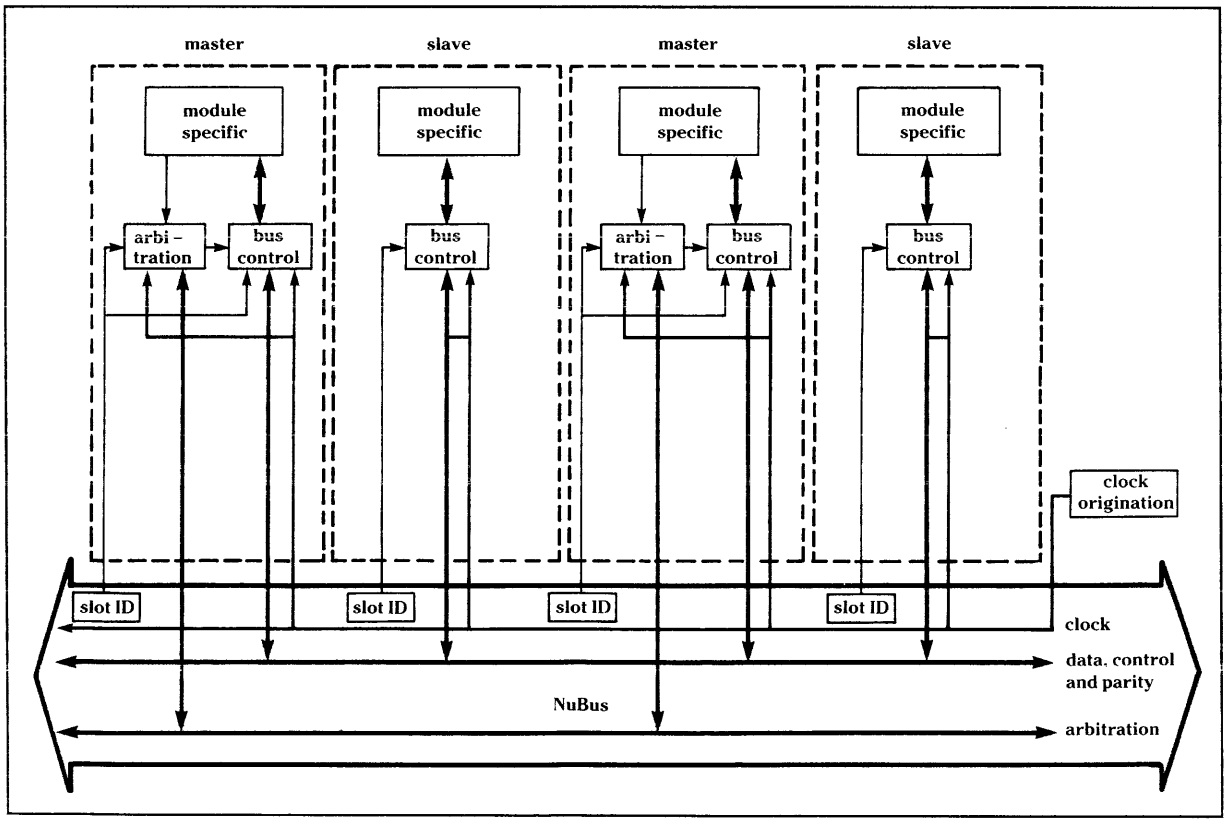
A.1 Appendix A contains information for those who intend to evaluate or design products that are compatible with the NuBus.

The NuBus is a synchronous bus that has many features of an asynchronous bus. Although all transactions and signal samplings are synchronized to a central system clock, they can vary in length (number of clock cycles). Thus the NuBus has the adaptability of an asynchronous bus with the design of a synchronous bus.

Figure A-1 shows the major elements of a typical NuBus system. The NuBus supports multiprocessing and other sophisticated system architectures with a few simple mechanisms.

For additional details on NuBus operation, refer to *NuBus — a Simple 32-Bit Backplane Bus, P1196 Specification, Draft 2.0*, a draft specification of the P1196 working group of the Microprocessor Standards Committee of the Institute of Electrical and Electronic Engineers, Inc., copyright (c) 1986.

Figure A-1 Simplified NuBus Diagram



Only read and write operations in a single address space are supported; I/O and interrupts are accomplished with these operations. All NuBus modules are equal; no board or slot position is the default master or special slot. The clock (CLK–) signal can originate at one of the NuBus modules or at one of the NuBus terminators. Each slot has an ID code hard-wired into the backplane; this code allows boards to be identified without the use of jumpers or switches.

The NuBus system is made complete with the addition of only eight more lines. The ID, clock, address/data, and ARB (arbitrate) lines are supplemented with reset, parity, and data transfer control lines.

NuBus Signal Classifications

A.2 Table A-1 shows the types of NuBus signals. The signals are grouped according to the functions they perform.

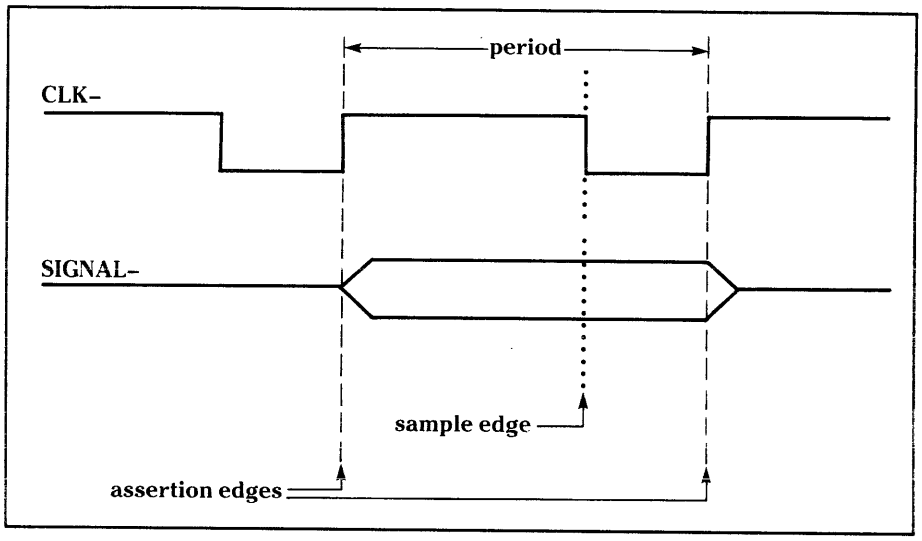
Table A-1 **List of NuBus Signals**

Classification	Signal	No. of Pins
Utility	RESET–	1
	CLK–	1
Control	START–	1
	ACK–	1
	TM0–	1
	TM1–	1
Address/data	AD<31 to 0>–	32
Arbitration	ARB<3 to 0>–	4
	RQST–	1
Parity	SP–	1
	SPV–	1
Slot ID	ID<3 to 0>–	4
Power/ground	+5V	11
	–5V	8
	+12V	2
	–12V	2
	GND	23
Reserved	RSVD–	1
	Total pin count:	96

Basic NuBus Timing

A.3 The NuBus system clock has a 100-nanosecond period with 75 nanoseconds inactive and 25 nanoseconds active. Figure A-2 shows the basic timing for NuBus signals. The low-to-high transition of the clock is used to activate and deactivate signals on the bus. Signals are sampled on the high-to-low transition of the clock. The asymmetric duty cycle of the clock provides 75 nanoseconds for propagation and setup time, with 25 nanoseconds between the sample and activation edges.

Figure A-2 **Basic NuBus Signal Timing**



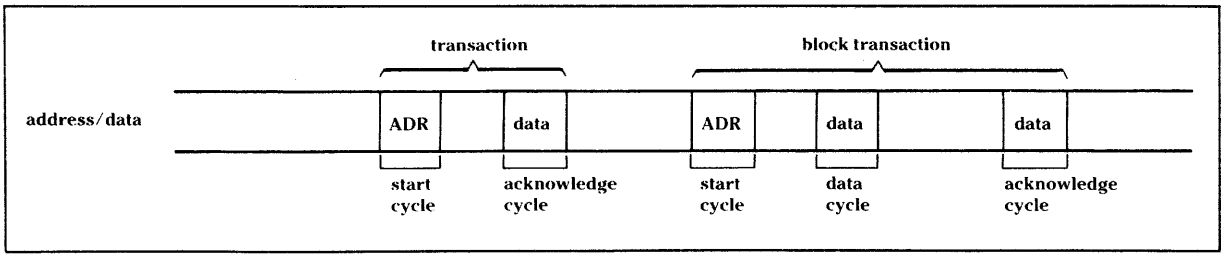
Basic Definitions

A.4 All NuBus signals are active when low, as indicated by a bar (–) after the signal name. Figures A-2 and A-3 show the relationships between some of the terms used throughout the NuBus specification. These terms are defined as follows:

- Acknowledge cycle — The last clock period of a transaction during which the ACK– signal is activated.
- Address cycle — The first clock period of a transaction during which the START– signal is activated. This term is synonymous with start cycle.
- Activated — In an active state. This term is synonymous with low and true.
- Activation edge — The rising edge of the central system clock.
- Cycle — A phase of a NuBus transaction. An address cycle is one clock period long and conveys address and command information. A data cycle is also one clock period long; it conveys data and acknowledge information.
- Attention cycle — A cycle in which both START– and ACK– are asserted at the same time. The TM1– and TM0– lines encode four possible types of attention cycles, two of which are reserved for future use. The other two cycles are used as broadcast messages to lock and unlock resources.

- Bus busy — The bus is busy during the time between a start cycle and its corresponding acknowledge cycle.
- Bus idle — The bus is idle during the time between an acknowledge cycle and the next start cycle.
- Data cycle — Any period in which data is known to be valid and acknowledged. It includes acknowledge cycles as well as intermediate data cycles within a block transfer.
- High — This term is synonymous with inactive.
- Inactive — In a dormant state. This term is synonymous with high.
- Low — This term is synonymous with active.
- Period — The 100-nanosecond clock period of the CLK– signal consisting of a 75-nanosecond inactive state and a 25-nanosecond active state.
- Sample edge — The falling edge of the central system clock.
- Slot ID — The hexadecimal number (0 through 15) corresponding to each board slot. Each slot ID is established by the backplane and communicated to the board through the ID lines.
- Slot space — The upper 1/16 of the total address space. The addresses are in the form *FSXXXXXX* where *F*, *S*, and *X* are hexadecimal digits of four bits each. (The letter *S* denotes slot ID.) This address space is geographically divided among the NuBus boards according to slot ID numbers.
- Start cycle — This term is synonymous with address cycle.
- Tenure — Bus tenure is a time period of unbroken control of the bus by a single master. A master can lock the bus and perform several transactions during one tenure.
- Transaction — A transaction is a complete NuBus operation such as read, write, block read, or block write. It is made up of one address cycle and one or more data cycles.
- Deactivated — This term is synonymous with high.

Figure A-3 Cycle and Transaction Relationships



Utility Signals

A.5 The following paragraphs identify the signal lines that serve utility functions for the NuBus.

Clock Signal

A.5.1 The clock (CLK–) signal is driven from a single source and synchronizes bus arbitration and data transfers between system modules. CLK– has an asymmetrical period of 25 nanoseconds active and 75 nanoseconds inactive and a constant nominal frequency of 10 megahertz. In general, signals are changed at the rising edge of CLK– and are sampled at the falling edge.

Reset Signal

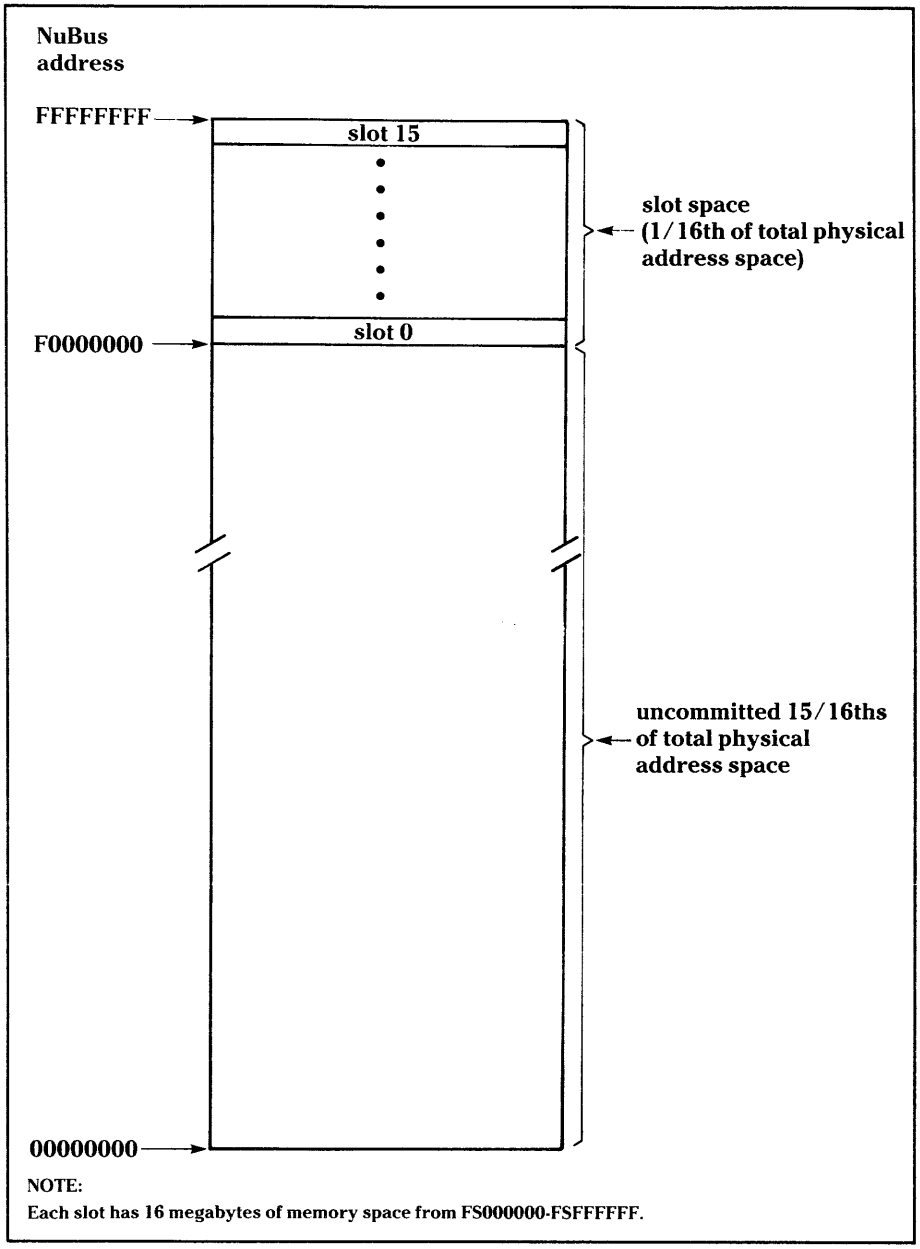
A.5.2 The reset (RESET–) signal is an open-collector line that returns all boards to the initial power-up state (system reset). If it is active for more than one clock period, it must be active for a minimum of one millisecond.

Board Slot ID Signals

A.5.3 Identification signals 0 through 3 (ID0– through ID3–) are binary coded to specify the physical location of each module. These signals are hard-wired on the backplane and identify the location of each circuit board.

ID signals are used to allocate a small portion of the total address space to each board. The upper 1/16 (256 megabytes) of the entire 4-gigabyte NuBus address space is called slot space. As shown in Figure A-4, this area is further divided into sixteen 16-megabyte areas that are mapped to the 16 possible NuBus board slots (or ID codes). Addresses of the form *FSXXXXXX* belong to a board's slot space. This fixed address allocation based on slot location allows the boards to be free of jumpers and switches. The remaining 15/16 of the 32-bit physical address space is available for allocation as required. Any allocation of that space is board- and system-dependent but is normally programmable by way of registers in the slot space.

Figure A-4 NuBus Address Space



Bus Data Transfer Signals

A.5.4 The bus data transfer signals, including control, address/data, and bus parity, are all three-state signals.

Control Signals

A.5.4.1 Descriptions of primary functions of the four NuBus control signals are as follows:

- The transfer start (START–) signal is driven for only one clock period by the current bus master at the beginning of a transaction. START– indicates that the address/data signals are carrying a valid address.
- The transfer acknowledge (ACK–) signal is driven for only one clock period by the addressed slave device and indicates the completion of the transaction.
- The transfer mode (TM0– and TM1–) signals are driven by the current bus master during the transfer start cycles to indicate the type of bus operation being initiated. They are also driven by bus slaves during the transfer acknowledge cycles to denote the type of acknowledgment. Table A-2 shows TM0– and TM1– encoding.

Address/Data Signals

A.5.4.2 Address/data signals 0 through 31 (AD0– through AD31–) are multiplexed to carry a 32-bit byte address at the beginning of each transaction and up to 32 bits of data later in the transaction. Note that the AD0– and AD1– signals carry address information during the start cycle of a byte transaction and control information during the start cycle of a nonbyte transaction. AD0– and AD1– encoding is shown in Table A-2.

Table A-2 **Transfer Mode Summary**

TM1–	TM0–	AD1–	AD0–	Type of Cycle
L	L	L	L	Write byte 3
L	L	L	H	Write byte 2
L	L	H	L	Write byte 1
L	L	H	H	Write byte 0
L	H	L	L	Write halfword 1
L	H	L	H	Write block
L	H	H	L	Write halfword 0
L	H	H	H	Write word
H	L	L	L	Read byte 3
H	L	L	H	Read byte 2
H	L	H	L	Read byte 1
H	L	L	H	Read byte 0
H	H	L	L	Read halfword 1
H	H	L	H	Read block
H	H	H	L	Read halfword 0
H	H	H	H	Read word

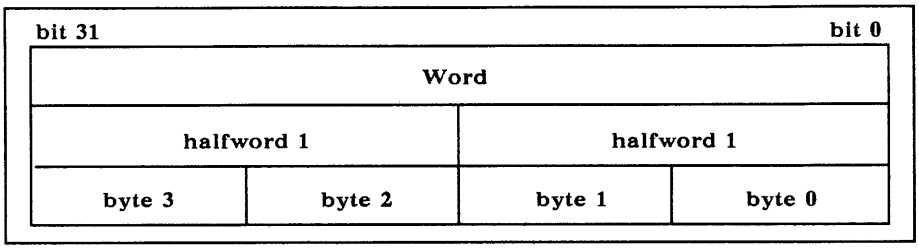
Bus Parity Signals

A.5.4.3 The system parity (SP–) signal transmits parity information between the NuBus boards that implement NuBus parity checking.

Data Transfer Operation

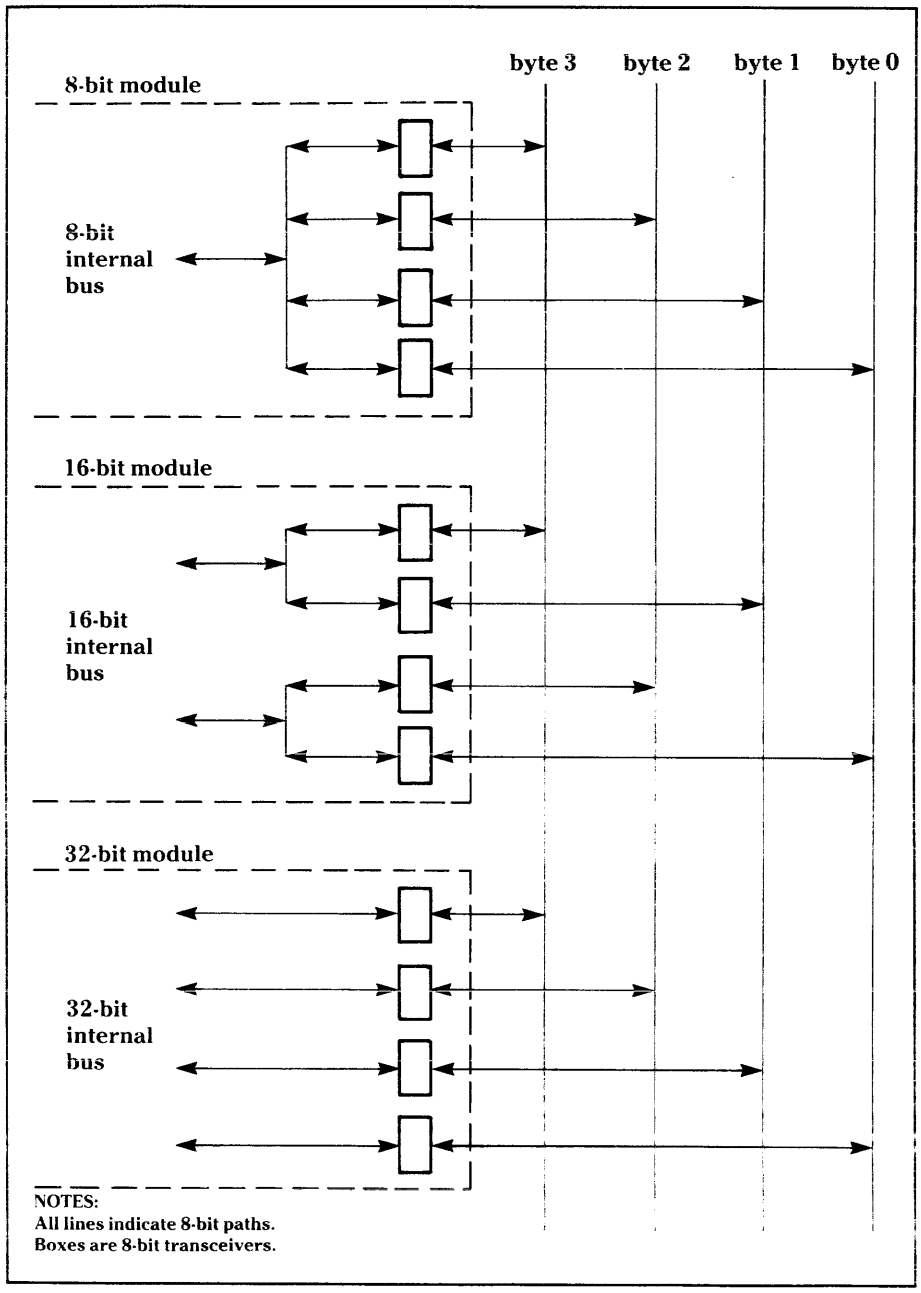
A.6 The NuBus supports read and write operations of several different data sizes. Although optimized for transactions of words and blocks of words, the NuBus also supports byte and halfword transactions. Figure A-5 shows the relationship between words, halfwords, and bytes.

Figure A-5 **Layout of Words, Halfwords, and Bytes**



All NuBus data transfers take place without byte position justification, as shown in Figure A-6. A byte of data is conveyed on the same signal lines regardless of the transfer mode used to access the data. This system simplifies the connection of 8-bit, 16-bit, and 32-bit devices.

Figure A-6 **Data Paths for 8-Bit, 16-Bit, and 32-Bit Devices**



Single Data Cycle Transactions

A.6.1 The simplest transactions on the NuBus convey one data item and consist of a start cycle and a subsequent acknowledge cycle. These transactions are read or write operations of either bytes, halfwords, or words.

All transactions are initiated when a bus master activates START– while driving TM0–, TM1, AD0–, and AD1– to define the cycle type. The remaining AD– signals are also driven to convey the address. The transaction is completed when the responding slave activates ACK– while driving status information on the TM0– and TM1– lines.

For write transactions, the master must switch the AD– signals from address to data information in the second clock period and hold that data until acknowledged. In read cycles, the slave drives the data simultaneously with the acknowledge cycle in the last period.

Read Transactions

A.6.1.1 Figure A-7 shows the timing for read bus transactions other than block transfers. Read operations with data widths of 8, 16, and 32 bits are selected by the transfer mode (TM0– and TM1–) signals and the low order address (AD0– and AD1–) signals. The slave must put the requested data on either 8, 16, or all 32 of the address/data (AD0– to AD31–) signal lines. Any bits other than the requested data can be driven either high or low by the slave. Once the bus master has acquired control of the bus, a read transaction involves the following steps:

1. On the first rising edge of CLK–, the bus master generates START– and the appropriate levels on TM0–, TM1–, AD0–, and AD1– to initiate the transfer operation. It also places the appropriate address on the bus.

2. On the first falling edge of CLK–, the slave devices sample the address and mode signals.

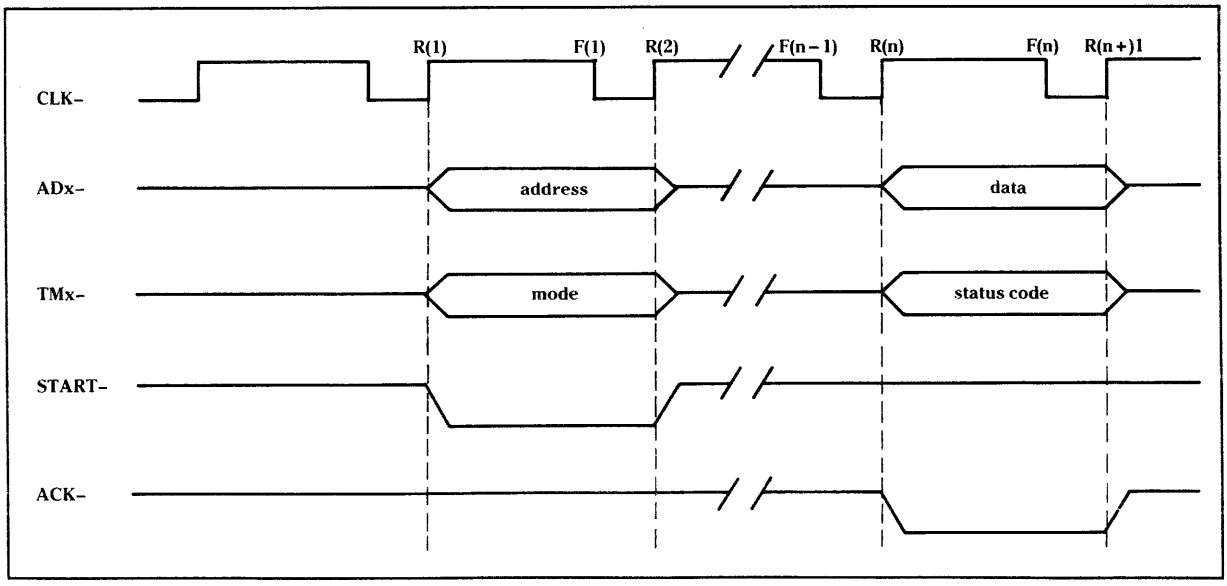
3. On the next rising edge of CLK–, the bus master releases all bus signals and waits for an ACK– signal.

4. On the next rising edge of CLK–, the bus slave places the requested data on the bus and activates the status code and ACK–.

5. On the next falling edge of CLK–, the bus master samples the data and status lines to receive the requested data and to detect any error condition.

6. On the next rising edge of CLK–, the bus slave deactivates all bus lines. This could be the first rising edge on the next transaction.

Figure A-7 NuBus Read Operation



Write Transactions

A.6.1.2 Figure A-8 shows the timing for write operations other than block transfers. Write operations with data widths of 8, 16, and 32 bits are selected by the transfer mode signals and the 2 low-order bits of the address bus. The bus master has the responsibility for aligning data on the appropriate address lines for halfword and byte write operations. For example, a write byte 3 operation requires that data be placed on AD24– through AD31–. All other address lines are undefined, and their states are irrelevant. Once the bus master acquires control of the bus, a write transaction involves the following steps:

1. On the first rising edge of CLK–, the bus master activates the START– signal and the appropriate mode signals, and then places an address on the bus.

2. On the next falling edge of CLK–, the bus slave devices sample the address and the mode signals.

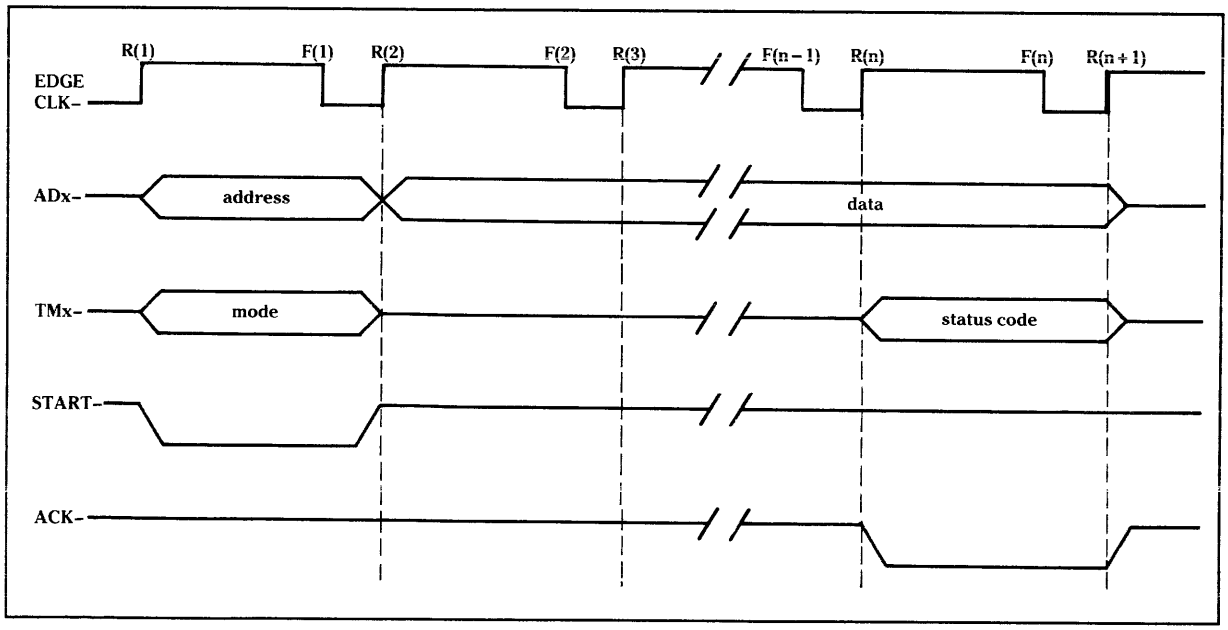
3. On the next rising edge of CLK–, the bus master places the data to be written on the bus, deactivates the START– and the mode signals, and waits for an ACK– signal.

4. On a later rising edge of CLK–, the bus slave activates ACK– and generates the appropriate status code.

5. On the next falling edge of CLK–, the bus slave samples the address lines to capture the data. This action can occur before or during the ACK– signal; that is, it can occur on any falling edge between F2 and F*n*.

6. On the next rising edge of CLK–, the bus master deactivates the data lines, and the bus slave deactivates the ACK– signal and the bus status lines.

Figure A-8 NuBus Write Operation



Attention Cycle Operation

A.6.1.3 An attention cycle is defined as the activation of START– and ACK– during the same period. The TM1– and TM0– lines are also driven and define one of four types of attention cycles as shown in Table A-3. The address lines are ignored by all bus devices and no data can be transferred.

The attention-null cycle is used to reinitiate bus arbitration. If the bus is requested and acquired but is not used (or required), an attention cycle must be inserted by the bus master to initiate a new contest among any contenders that are holding the request (RQST–) signal active. If RQST– is inactive, an attention cycle is not needed (but can be inserted). The arbitration period can now be timed from the activation of RQST–.

Table A-3 **Attention Cycle Summary**

TM1–	TM0–	Type of Attention Cycle
L	L	Attention null
L	H	Reserved
H	L	Attention-resource-lock
H	H	Reserved

Acknowledge Cycle

A.6.1.4 During acknowledge cycles, the addressed slave drives the status lines while it drives ACK–. These lines provide status information to the current bus master as follows:

- Bus transfer complete — A bus transaction has completed normally.
- Error — An error condition has occurred, such as an uncorrectable memory read error or a bus parity error. The transaction terminates in a normal manner, and the bus master has responsibility for handling the error condition.
- Bus time-out — The system-defined time-out period has elapsed while the bus is busy, and no transfer acknowledge cycle has occurred. Bus time-out can occur if an unimplemented address location is summoned.

  Bus time-out also occurs if a contender requests the bus and does not generate a start cycle. In this case, the bus time-out logic generates an idle cycle to reinitiate bus arbitration.
- Try again later — An addressed slave cannot respond to a master's transfer request at the time of the request. The master should re-arbitrate for the bus later. This message is not an error indication.

Table A-4 summarizes the status codes.

Table A-4 **Status Code Summary**

TM1–	TM0–	Type of Acknowledgment
L	L	Bus transfer complete
L	H	Error
H	L	Bus time-out error
H	H	Try again later

Block Transfers

A.6.2 Block transfers consist of a start cycle, multiple data cycles from or to sequential address locations, and an acknowledge cycle. The number of data cycles is controlled by the master and communicated during the start cycle. Allowed lengths of block transfers are 2, 4, 8, and 16 words. (Only word transfers are supported in the block transfer mode; that is, all data transfer lengths must be specified in 4-byte multiples.)

Table A-2 shows the mode encoding for block transfers. The block's starting address must correspond to its size and is encoded by the AD2– through AD5– lines as shown in Table A-5.

During block transfers, each data cycle is acknowledged by the responding slave. The slave holds TM0– active and TM1– and ACK– inactive for intermediate acknowledge data cycles. For intermediate acknowledgments, TM0– has the same significance and timing as the ACK– signal for nonblock transfers. The final word transfer acknowledgment is a standard acknowledge cycle.

Table A-5 **Block Size and Starting Address Summary**

AD5–	AD4–	AD3–	AD2–	Block Size (Words)	Block Starting Address
X	X	X	H	2	(AD31–AD3)000
X	X	H	L	4	(AD31–AD4)0000
X	H	L	L	8	(AD31–AD5)00000
H	L	L	L	16	(AD31–AD6)000000

Block Read Operation

A.6.2.1 Figure A-9 shows the timing for a NuBus block read operation. The AD2– through AD5– lines determine the size and starting address of the transaction. The responding slave drives data onto the bus, and the initiating bus master accepts the data on each intermediate or final acknowledge cycle. Once the bus master acquires control of the bus, a block read consists of the following steps:

1. On the first rising edge of CLK–, the bus master activates START– and the appropriate address and mode lines.
2. On the next falling edge of CLK–, the bus slave device samples the address and mode lines.
3. On the next rising edge of CLK–, the bus master deactivates START– and the address lines and waits for an intermediate acknowledge cycle (TM0– active).
4. On a later rising edge of CLK–, the bus slave places the first word of the requested data on the bus and asserts TM0–.
5. On the next falling edge of CLK–, the bus master samples the bus lines and TM0– to capture the data.

6. On the next rising edge of CLK–, the bus slave removes the data word from the bus, and if the next word is not ready to be placed on the bus, the slave drives TM0– inactive until the word is ready.

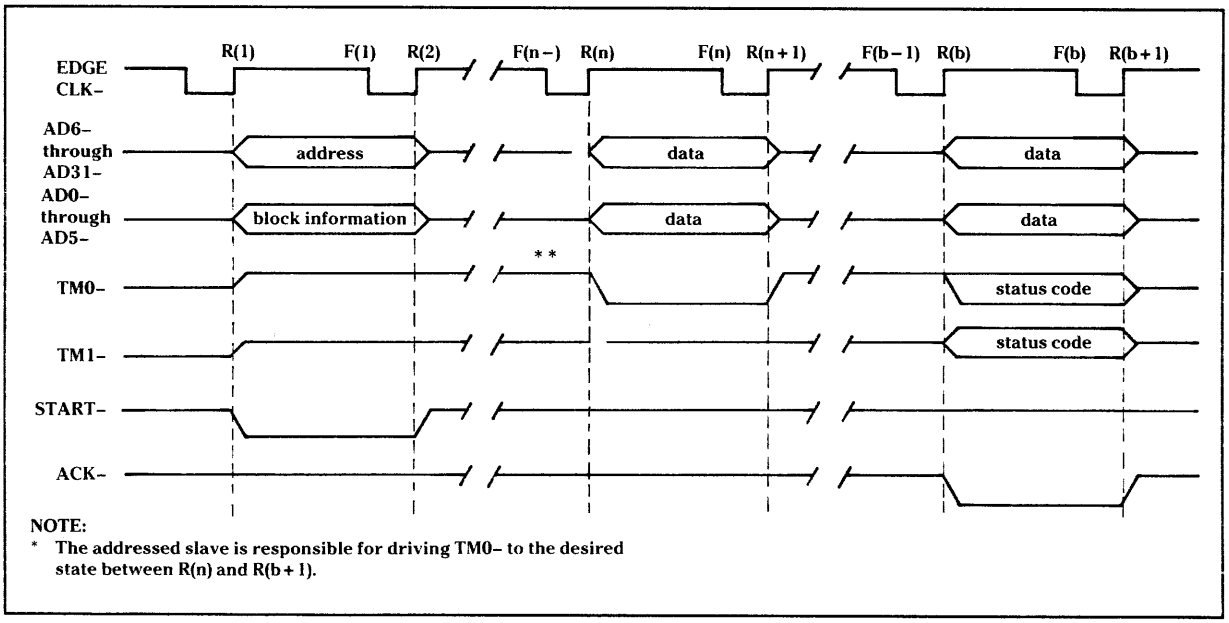
NOTE: Steps 4 through 6 are repeated for ascending addresses until all words of the block, except the final word, have been transferred.

7. On some later rising edge of CLK–, the bus slave device places the final word of the requested data on the bus and activates ACK– and the appropriate status code on TM0– and TM1–.

8. On the next falling edge of CLK–, the bus master samples the bus and the status lines to receive the data and status information.

9. On the next rising edge of CLK–, the bus slave device deactivates all signals.

Figure A-9 NuBus Block Read Operation



Block Write Operation

A.6.2.2 Figure A-10 is a timing diagram for a NuBus block write operation. Block write operations are similar to block read operations, except that the bus master drives the data bus while the slave accepts data. The format for describing block size and starting address is the same as for block read operations. Once the master has acquired control of the bus, a block write operation consists of the following steps:

1. On the first rising edge of CLK–, the bus master activates START– and the appropriate address and mode lines to initiate the transfer.

2. On the next falling edge of CLK–, the bus slave device samples the address and mode lines.

3. On the next rising edge of CLK–, the bus master places the data to be written on the bus, then releases START– and the mode lines, and waits for an intermediate acknowledge cycle (TM0– active).

4. On the next rising edge of CLK–, the bus slave activates TM0– to acknowledge that bus data is valid.

5. On the next falling edge of CLK–, the bus slave samples the address lines to capture the data being written. This action can occur on any falling edge of CLK–, either before or during the time in which TM0– is active.

6. On the next rising edge of CLK–, the bus master places the next consecutive word of data on the bus.

NOTE: Steps 4 through 6 are repeated for ascending addresses until all words of the block, except the final word, have been transferred.

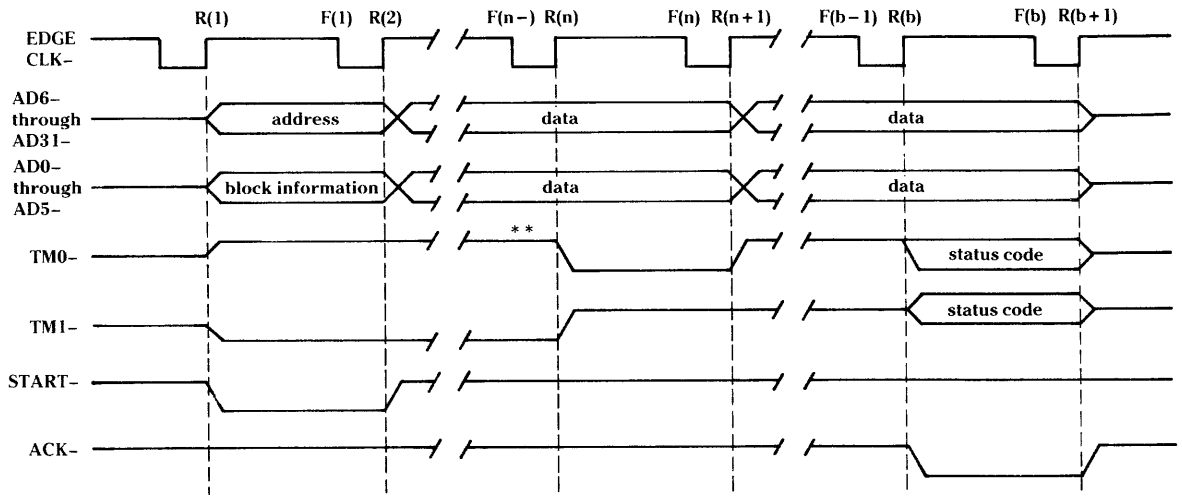
---

7. On the next rising edge of CLK–, after the final data word has been placed on the bus, the bus slave device activates ACK– and the appropriate status code.

8. On the next falling edge of CLK–, the bus slave device samples the address lines to capture the data. This action can occur on any falling edge of CLK–, either before or during the time in which TM0– is active.

9. On the next rising edge of CLK–, the bus master deactivates the bus lines while the bus slave deactivates ACK– and the status lines.

Figure A-10 NuBus Block Write Operation



NOTE:
** The addressed slave is responsible for driving TM0− to the desired state between R(n) and R(b+1).

Block Transfer Early Termination

A.6.2.3 An addressed slave that is incapable of performing any block transfer shall issue an acknowledge cycle without any intermediate data transfer cycles (TM0− asserted, TM1− and ACK− unasserted) with a bus transfer complete transaction response status. The single word transferred shall be ignored by the master during read and shall be ignored by the address slave during write. This is a normal response of a module incapable of supporting block transfers and is not an error condition.

If the addressed slave detects an error during a block transaction, the transaction can be terminated by the addressed slave by issuing an acknowledge cycle with the appropriate transaction response status. Any data transferred during a block transfer that is ended with an error condition is not guaranteed to be meaningful.

The slave is not required to signal the error as soon as it is detected. Thus, the error could have occurred at any time during the active block transfer, which makes all transferred data suspect.

Interrupt Operations

A.6.3 Interrupts on the NuBus are implemented as write transactions and require no unique signals or protocols. Any module on the NuBus can interrupt a processor by performing a write operation into an area of memory that is monitored by the processor. Any address range on the processor module can be defined as an interrupt space. This interrupt method allows interrupts to be posted to individual processors and allows interrupt priority to be software-specified by memory mapping the priority level. This method of interrupt handling is called *event generation*.

Bus Parity

A.7 Parity protects the integrity of all address and data transfers. Parity generation is optional on a cycle-by-cycle basis. Parity is useful only if the module driving the bus lines generates parity, and the module capturing the address or data information checks it.

Signal parity (SP–) and signal parity valid (SPV–) are used to communicate parity and parity valid, respectively. Activation of SPV– (with the same timing as the bus lines) generates parity. SP– carries even parity, meaning that if an even number of lines within AD0– through AD3– are active, SP– is inactive. Otherwise it is active.

Parity checking is optional. Modules that cannot check parity normally ignore the SPV– and SP– signals. Although byte and halfword transfers are supported, parity is always calculated over the complete 32 bits of the bus lines. This system simplifies interface design. Parity error detection results in one of the following conditions:

- If the detection occurs during an address cycle, the slave device ignores the address, and the transaction usually times out.
- If the detection occurs during a data read cycle, the master device ignores the received data.
- If the detection occurs during a data write cycle, the slave device acknowledges with the error status code.

Compliance Categories

A.8 Some NuBus devices do not support all NuBus features. Masters and slaves do not need to support all transfer types. Any combination of 8-bit, 16-bit, and 32-bit single data transfers, either master or slave, is allowable.

Bus Arbitration

A.9 The following paragraphs describe the arbitration signals for the NuBus.

Arbitrate Signals

A.9.1 Arbitrate 0 through 3 (ARB0– through ARB3–) are open-collector binary-coded lines driven by contenders for the bus. They are used by the distributed arbitration logic to determine bus mastership.

Request Signal

A.9.2 Bus request (RQST–) is an open-collector line driven low by the contenders for the bus.

Arbitration Operation

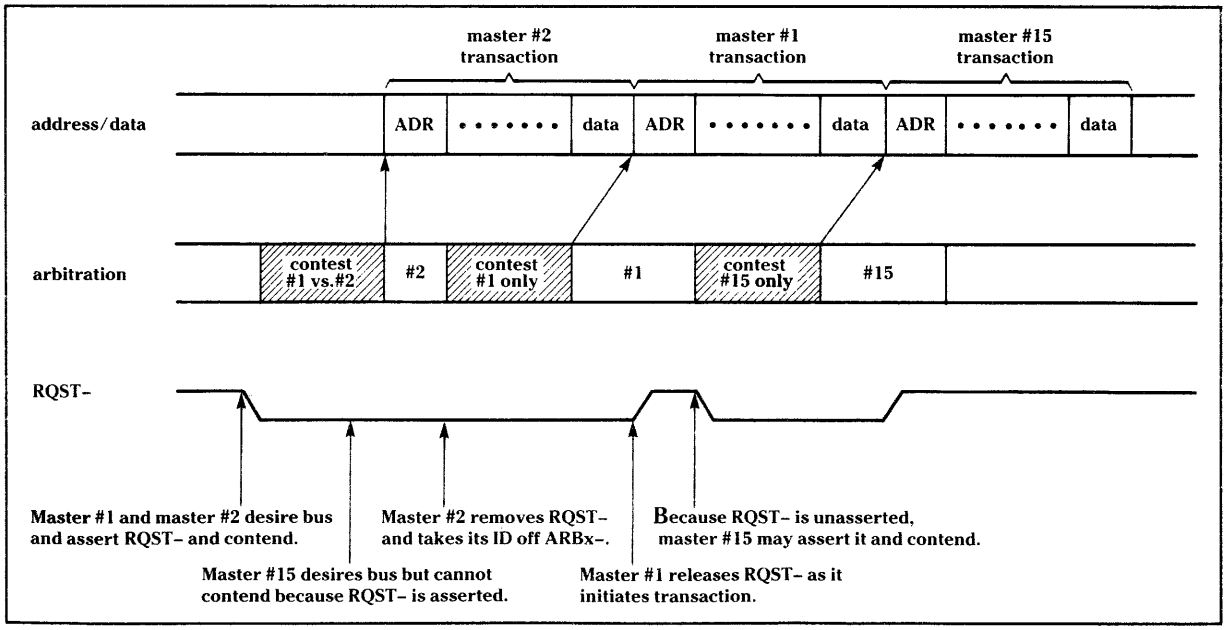
A.9.3 NuBus arbitration differs from strict priority arbitration in that it prevents boards from waiting too long for bus use and also distributes the bus bandwidth evenly.

During arbitration, one or more modules contend for control of the NuBus. Modules must first activate RQST–, which can be activated only while it is in an inactive state. All modules activating RQST– place their ID codes on the arbitrate lines and contend for the bus. The arbitration logic distributed among the modules determines which module gains control of the NuBus in two clock periods. The contender with the highest ID code has its code on the arbitrate lines, gains control of the bus, and then can initiate a transaction.

Presuming the winner does not desire to lock the bus, the winning module removes its RQST– at the same time that START– is activated and removes its arbitrate signals after the start cycle of its first transaction. Deactivation of START– initiates another contest between any modules that originally requested the bus but have not yet won. These modules are granted ownership in turn from the highest to the lowest ID number. The rule that RQST– must be inactive before it can be asserted by a module keeps other modules from participating in contests until all original requesters have been served.

Figure A-11 shows modules with codes 1 and 2 requesting the bus during the same clock period. Module 2 wins the first arbitration contest and then removes its request following its start cycle. Module 15 desires the bus as well but cannot request it because RQST– is already active. Since no other module has requested bus use, module 1 wins the next contest and gains control of the bus. When module 1 releases RQST–, module 15 requests, arbitrates, and wins. Note that module 1 can control the bus only after it wins a contest and the transaction in progress ends.

Figure A-11 Sample Arbitration Contest



Arbitration Logic Mechanism

A.9.4 When a bus contest occurs, each module drives the arbitrate lines with its unique ID code and then deactivates the lines if it detects higher ID codes than its own on the lines. Figure A-12 shows an implementation of this logic. Note that the ARB– lines are bused common to all boards, while the ID lines present a unique binary code to each board slot.

ARB and GRANT are module signals. ARB indicates whether the module is contending for the bus, and GRANT indicates whether the arbitrate lines currently match this module's ID lines. The following logic equations describe how the arbitration logic works on any given module:

- ARB3 = ID3 * ARB
- ARB3 = ID2 * ARB * (ID3 + ARB3–)
- ARB1 = ID1 * ARB * (ID3 + ARB3–) * (ID2 + ARB2–)
- ARB0 = ID0 * ARB * (ID3 + ARB3–) * (ID2 + ARB2–) * (ID1 + ARB1–)

General Arbitration Timing

A.9.5 Arbitration events generally occur on rising and falling edges, synchronous to the system clock, with the same timing as the basic address/data, control signals, and utility signals. For example, RQST– can be activated on a particular rising edge only if it is inactive on the previous falling edge. However, the arbitrate lines differ from all other NuBus signals in that their activation time is specified from the falling edge of the bus clock.

On the second falling edge after a contest starts, all contenders sample their internal grant mode signal. The highest priority contender finds its grant mode signal active. The winner can now take control of the bus and activate START– on the next rising edge of CLK– if the bus is not in use. If the bus is in use, the winner activates START– on the rising edge of CLK– following the falling edge that occurs during the current transaction's ACK– period. The new winner continues to hold its ID code active on the arbitrate lines throughout the start cycle of its first transaction, allowing for bus-lock detection and bus diagnostics.

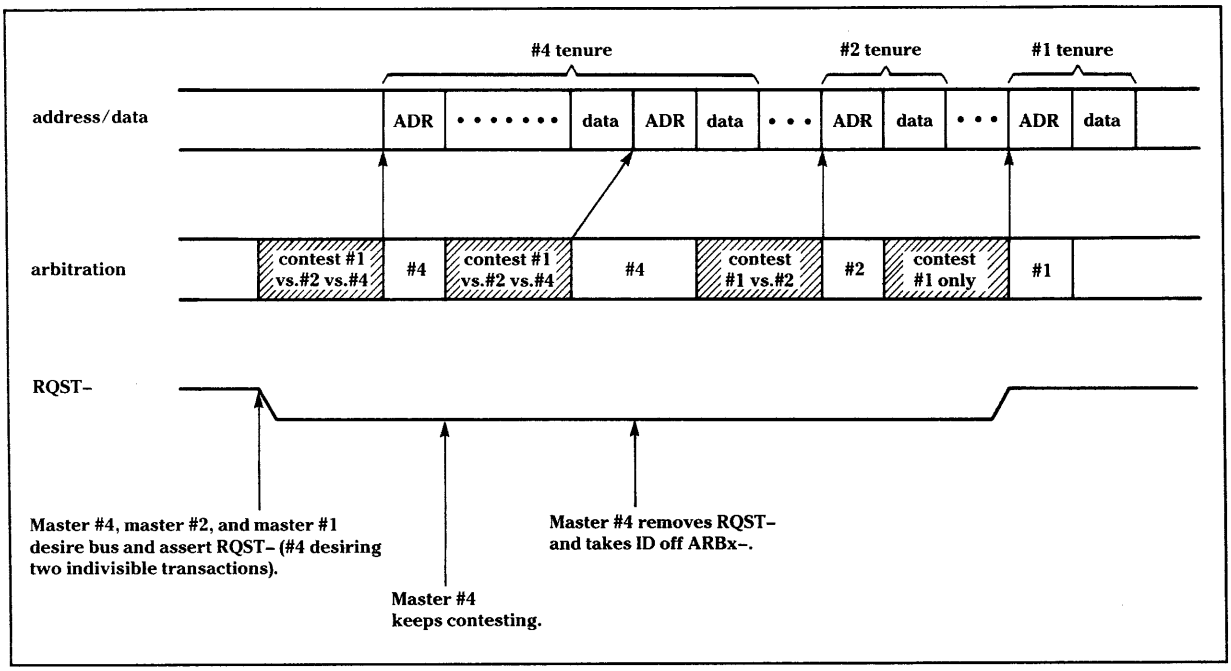
Bus Locking

A.9.6 Although modules generally use the bus for short periods, sometimes a module must lock the bus. An example of a module that must lock the bus is an indivisible test-and-set operation performed in a multiprocessor environment.

Bus locking is accomplished with no added mechanism. To lock the bus, a master simply continues to request and contend. Since it has the highest ID code of those modules present, it wins subsequent contests. Figure A-12 shows an example in which module 4 locks the bus for two transactions.

A bus owner that intends to perform an indivisible bus operation should always lock resources on addressed slaves in addition to locking the bus. Resource locking is accomplished by issuing an attention-bus-lock cycle as the first transaction of the locked bus tenure to alert all modules that a locked operation is occurring. A bus owner that issues an attention-bus-lock cycle shall issue an attention-null cycle as the last cycle of its locked bus tenure to indicate to all modules that the locked operation is completed. All bus modules with resources that can be locked shall monitor the NuBus for attention-bus-lock cycles.

Figure A-12 Sample Bus Lock



Bus Parking

A.9.7 In a NuBus system with few modules, a bus master that has deactivated RQST– stays on the bus and can use it at any time until another module activates RQST–. After RQST– is activated, the master that is on the bus finishes its current transaction and relinquishes the bus to the new winner. This type of operation reduces the average time required to gain control of the bus in systems with a small number of contenders.

INDEX

Numbers

A

B

C

D

Data Systems Group – Austin
Documentation Questionnaire

Explorer 7-Slot System Enclosure General Description

Do you use other TI manuals? If so, which one(s)?

_____ _____

_____ _____

_____ _____

How would you rate the quality of our manuals?

	Excellent	Good	Fair	Poor
Accuracy	_____	_____	_____	_____
Organization	_____	_____	_____	_____
Clarity	_____	_____	_____	_____
Completeness	_____	_____	_____	_____
Overall design	_____	_____	_____	_____
Size	_____	_____	_____	_____
Illustrations	_____	_____	_____	_____
Examples	_____	_____	_____	_____
Index	_____	_____	_____	_____
Binding method	_____	_____	_____	_____

Was the quality of documentation a criterion in your selection of hardware or software?

☐ Yes ☐ No

How do you find the technical level of our manuals?

☐ Written for a more experienced user than yourself

☐ Written for a user with the same experience

☐ Written for a less experienced user than yourself

What is your experience using computers?

☐ Less than 1 year ☐ 1-5 years ☐ 5-10 years ☐ Over 10 years

We appreciate your taking the time to complete this questionnaire. If you have additional comments about the quality of our manuals, please write them in the space below. Please be specific.

_____

_____

_____

_____

_____

Name _____ Title/Occupation _____

Company Name _____

Address _____ City/State/Zip _____

Telephone _____ Date _____

Manual Part No. 2243143-0001 *E

TAPE EDGE TO SEAL

FOLD

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

BUSINESS REPLY MAIL

FIRST-CLASS PERMIT NO. 7284 DALLAS, TX

POSTAGE WILL BE PAID BY ADDRESSEE

TEXAS INSTRUMENTS INCORPORATED
DATA SYSTEMS GROUP
ATTN: PUBLISHING CENTER
P.O. Box 2909 M/S 2146
Austin, Texas 78769-9990

FOLD