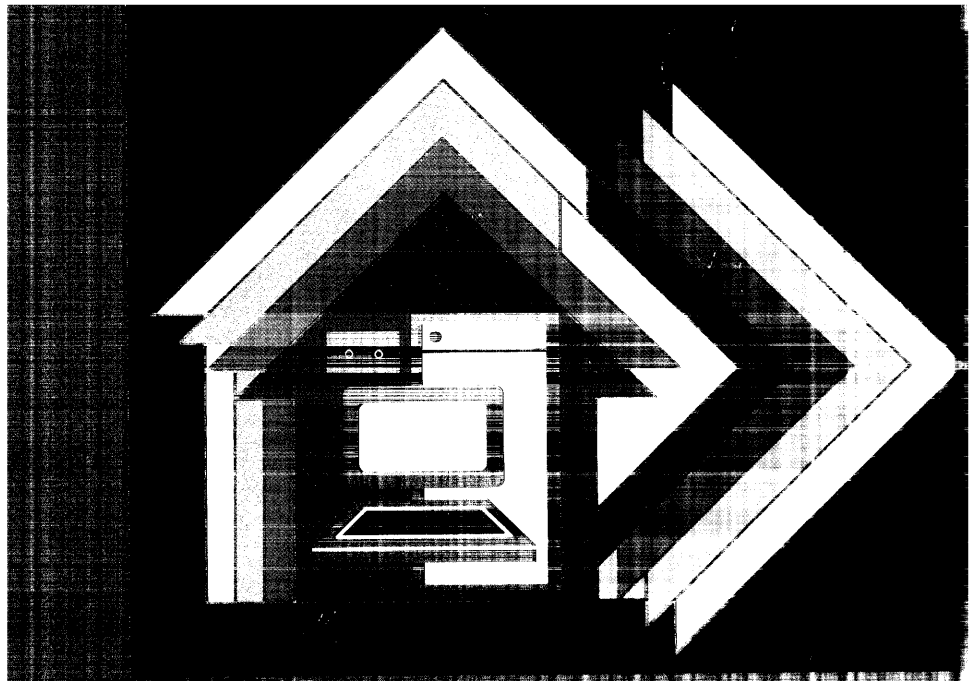# 990/SCSI MASS STORAGE

SUBSYSTEM

GENERAL DESCRIPTION

TEXAS
INSTRUMENTS

990/SCSI MASS STORAGE SUBSYSTEM
GENERAL DESCRIPTION

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, can cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computer device pursuant to Subpart J of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference; in which case, the user at the user's own expense will be required to take whatever measures necessary to correct the interference.

WARNING: There are no serviceable, installable, or replaceable parts inside the 990A13 chassis. The card cage area of the model 990A13 chassis contains hazardous live electrical components involving risk of electric shock and energy hazard-high current levels. Installation instructions provided in this manual are to be used by trained personnel familiar with electrical hazards, and with a knowledge of basic hand tools and cabling techniques. A detailed knowledge of computer hardware or software is not required.

CAUTION: Do not stack more than two MSUs on top of each other. When more than two units are stacked on top of each other, there is a danger of the stacked units becoming top heavy and possibly tipping over.

Do not place the MSU in a closed compartment with limited air circulation. Heat buildup within such an environment can result in damage to one or more components of the MSU.

To avoid possible damage to the MSU power supply, ensure that the voltage range select switch is in the proper position prior to connecting the ac line cord or applying power.

MANUAL REVISION HISTORY

990/SCSI Mass Storage Subsystem General Description (2540219-0001)

Original Issue .... December 1987

Revision A .... September 1988

HARDWARE MANUALS

OmniLaser is a trademark of Texas Instruments Incorporated.

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Paragraph	Title	Page

3 **Functional Description**

Paragraph	Title	Page

Paragraph	Title	Page

4   MSU Functional Description

Acronym List

Index

Figure	Title	Page

ABOUT THIS MANUAL

Purpose

This document provides a general description of the Texas Instruments (TI) 990/SCSI mass storage subsystem. The information in this document is intended to be used by system designers, value added resellers (VARs) and maintenance personnel.

Contents of This Manual

Section 1: General Description — Provides general information on the 990/SCSI controller and mass storage unit (MSU) interface and its usage in 990 computer systems.

Section 2: Installation, Operation, and PM — Provides installation and operation information for the 990/SCSI and MSU. The installation instructions include site requirements, equipment placement, cables, and line voltage selection. The operation instructions provide general operational information.

Section 3: Functional Description — Provides technical information on the 990/SCSI controller hardware, plus programming and self-test information.

Section 4: MSU Functional Description — Provides a brief overview of the MSU and references for detailed theory of operation and other details on the internal components of the MSU. Information on formatted capacity and synchronous operation are also provided in this section.

Acronym List: Lists the meanings of acronyms used throughout this book.

Related Documents

The following documents supply additional information related to the 990/SCSI controller and its operation.

■ Board Outline, 990 Full Size, EMI/RFI Chassis (TI drawing 2308627)

■ ESDI/SCSI Formatter Specification (TI drawing 2238064)

■ Cartridge Tape with SCSI Formatter Specification (TI drawing 2238108)

■ American National Standard ANSI X3.131-1986, Small Computer System Interface (SCSI)

■ Common Command Set (CCS), Small Computer System Interface (SCSI), ANSI X3T9 draft proposal, revision 2, October 21, 1985
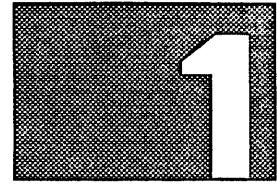
GENERAL DESCRIPTION

Introduction

1.1 The 990/SCSI controller provides a TILINE™ interface to mass storage unit(s) (MSU) through the American National Standard Institute (ANSI) small computer system interface (SCSI). This 990/SCSI controller, when combined with MSU(s), a host 990 computer, and optional mounting hardware, forms the 990/SCSI mass storage subsystem. This mass storage subsystem will be illustrated and described in greater detail in the following paragraphs:

■ Purpose

■ Features

■ Major Components

NOTE: Except where noted, the MSU II and MSU IIA are synonymous in this document.

Purpose

1.2 The 990/SCSI controller provides mass storage support for TILINE-based products, such as the Business System 600/800 series computers. The controller is implemented on a multi-layer, full-sized 990 board assembly. Two separate AMPMODU™ type connectors provide the SCSI port interconnect and an EIA port connection.

The 990/SCSI controller supports both magnetic disks and tapes, mounted in MSUs, via the SCSI port. Only tape units with fixed block sizes are supported. The controller supports QIC-24 tape devices with block sizes of 512 bytes.

The EIA port is intended for factory debug purposes and depot repair facilities only. The port allows an external monitor, such as a TIPC or a 931 terminal, to be connected to the board and gain access to an internal ROM-resident firmware monitor.

Features

1.3 The 990/SCSI controller key features are as follows:

■ Simple cost-effective architecture

   ■ Moderate data throughput

   ■ Minimal command processing overhead

TILINE is a trademark of Texas Instruments Incorporated.
AMPMODU is a trademark of AMP Inc.

- 10-MHz 68010 microprocessor

- Full functionality firmware contained in 64K bytes of onboard ROMs

- 68901 multi-function integrated circuit (IC) for interrupts and timers

■ TILINE interface

- CSD2051 TILINE IC

- Asynchronous bus

- 16-bit data bus

- 20-bit address bus

■ SCSI interface

- Reliable WD33C93 IC features internal line drivers/receivers

- SCSI data throughput rates up to 1.5 MB/s

- Asynchronous protocols

- Single-ended SCSI bus drivers/receivers

■ ROM-resident self-test diagnostics

■ EIA port for factory debug capability

■ Controller level defect data gathering

- Controller dynamically logs blocks for which the operating system receives read or write errors for future reallocation.

Major Components

1.4 The major components of the 990/SCSI mass storage subsystem consist of the following:

■ 990/SCSI Controller

■ MSU

■ I/O Cable (AMPMODU to CHAMP®)

■ Mounting Enclosure

990 SCSI Controller

1.4.1 The 990/SCSI controller converts operating system commands to SCSI operations that are then issued to the appropriate mass storage device. TILINE and SCSI interface protocols are handled in order to transfer data, commands, and status between the mass storage peripherals and TILINE memory. A board outline of the 990/SCSI controller board is shown in Figure 1-1.

CHAMP is a registered trademark of AMP, Inc.

Connectors P1 and P2 are standard 80-pin edge card connectors which meet the requirements of the TILINE. Connector P3 is dedicated to the SCSI port, while connector P4 provides an EIA interface for an external monitor intended for debug environments only.

Figure 1-1   990/SCSI Controller Board Outline
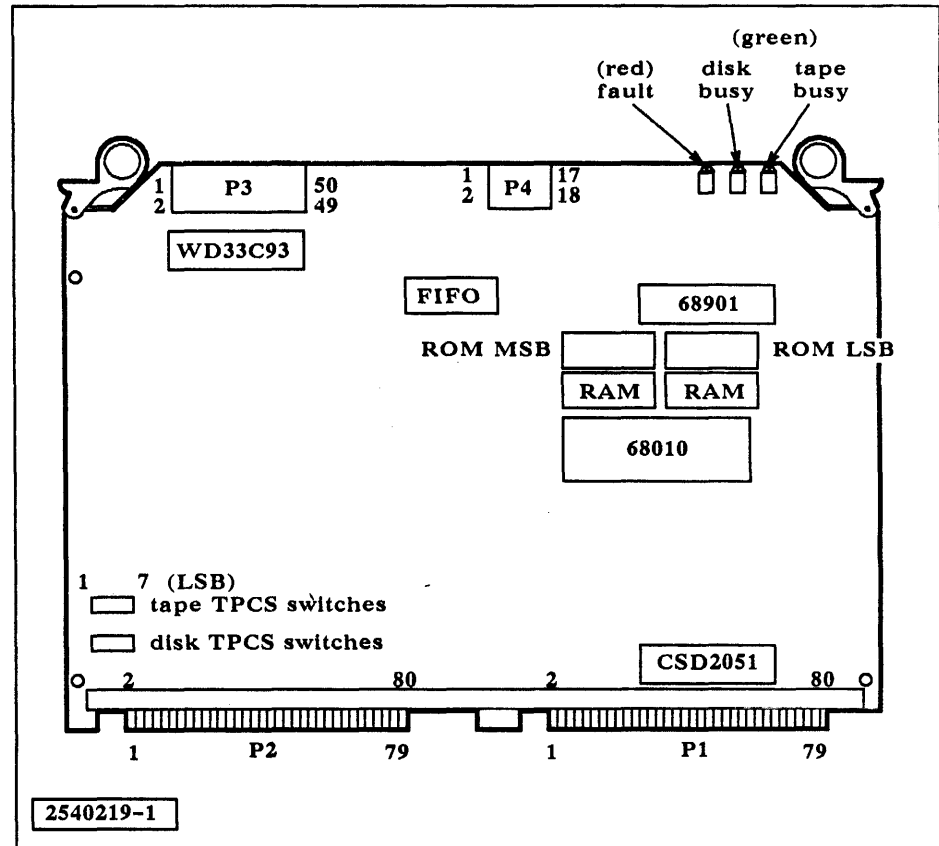
SCSI interface signals are terminated on the 990/SCSI controller. The SCSI termination follows the ANSI SCSI interface specification and is a split termination with 220-ohm pull-ups and 330-ohm pull-downs for the single-ended interface.

MSU II   1.4.2 The MSU II, when combined with the 990/SCSI controller board and the SCSI cable, provides a mass storage subsystem for use with host TILINE-based products, such as the Business System 600/800 series computers. Key features of the MSU II, compared to earlier versions of MSUs are: ANSI enhanced small device interface (ESDI) disk drive formatters and Champ I/O connectors. The difference between an AMPMODU connector and a CHAMP connector is shown in Figure 2-10 entitled SCSI Bus Cables.

MSU IIA   **1.4.3**   The MSU IIA differs from the MSU II in that the former uses an embedded SCSI disk drive, which eliminates the need for the ESDI drive formatter.

Communication between the MSU and the host computer is through the 990/SCSI controller board via the SCSI cable. The 990/SCSI controller board is located in the host computer chassis. The SCSI cable attaches to the SCSI port (P3) on one end and to the MSU on the other.

The MSU subsystem uses a distributed intelligence scheme. The 990/SCSI controller board interprets requests from the host processor and coordinates the transfer of data commands and status signals between the host memory and the formatters in the MSU. The use of the SCSI provides maximum flexibility for selection of mass storage devices. SCSI circuitry is located on the 990/SCSI controller board at the computer end, and on the formatter board(s) at the MSU end. Figure 1-2 shows typical configurations for two MSUs with a cartridge tape drive and two ESDI Winchester disk drives. Figure 1-3 is a line drawing of the MSU subsystems, showing interconnections between a host computer and three table top MSUs.

Figure 1-2   Two Table Top MSUs

2540219-19
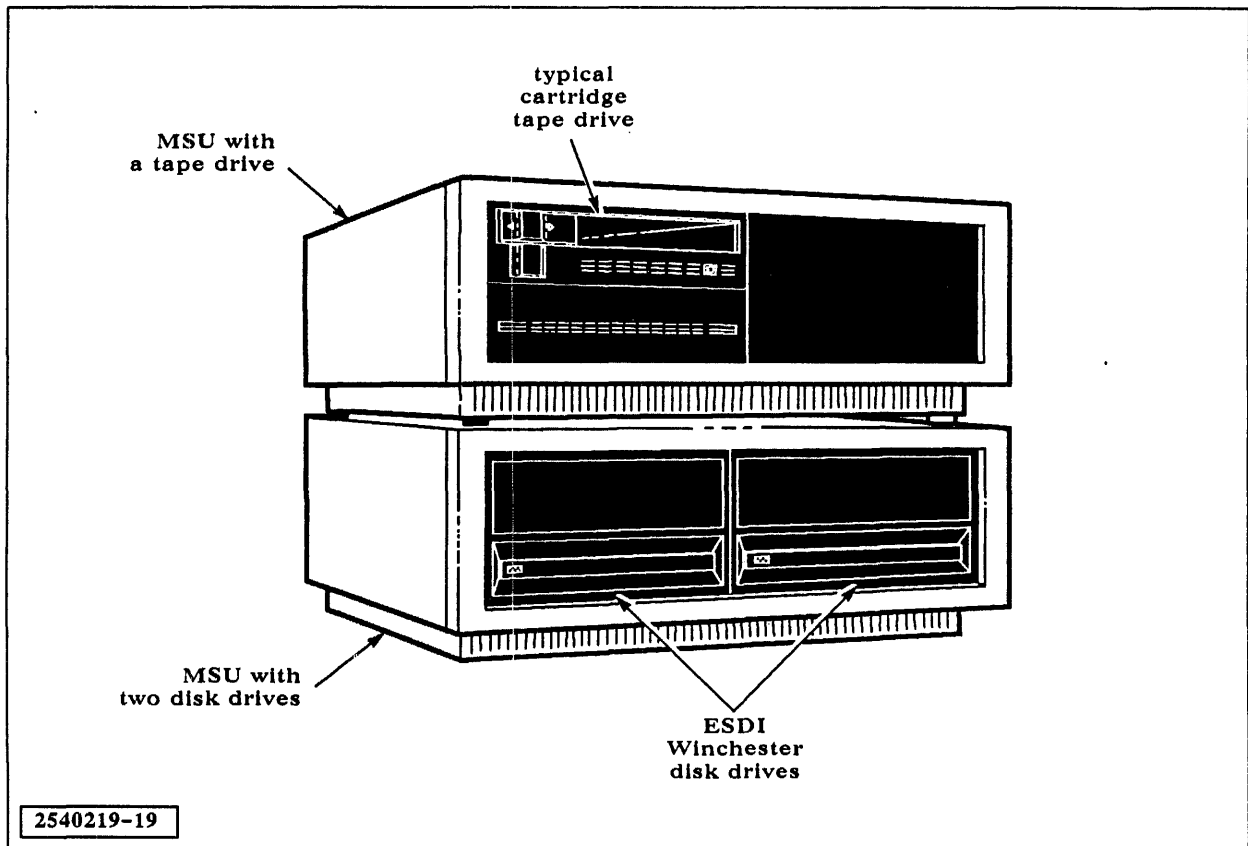
Figure 1-3 Multiple MSU Connections (Table Top Kits Only)
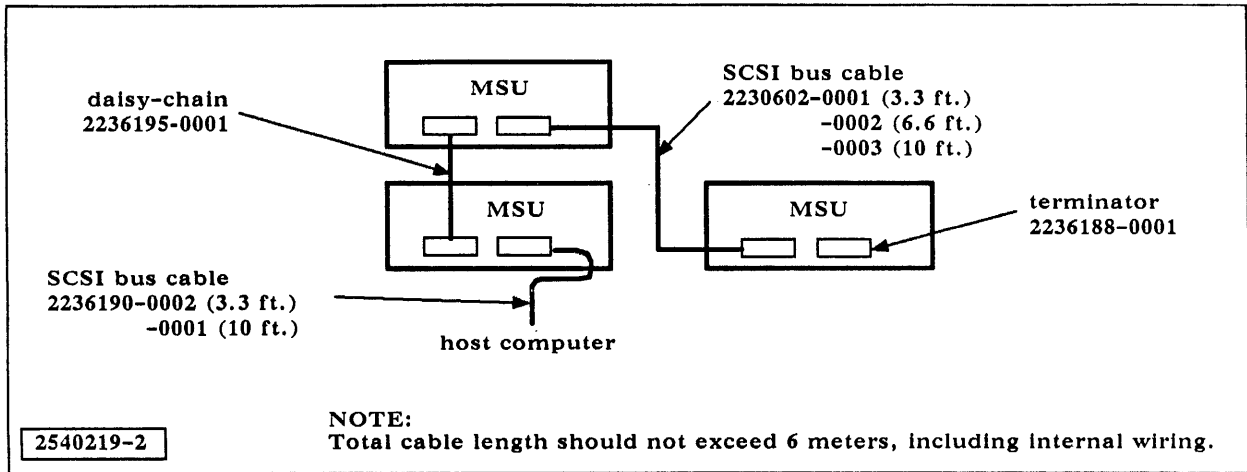
Rack Mounting Enclosure

1.4.4 The mounting enclosure for the 990/SCSI mass storage subsystem consists of a tray assembly and trim panel. A secondary tray assembly is available for mounting two MSUs in a single 32-inch enclosure. This secondary tray assembly has a power junction box that provides primary power distribution for the secondary MSU. Figure 1-4 shows the mounting arrangements for the 990 computer chassis and the primary and secondary MSU.

Figure 1-4 Rack Mounting Configurations for Business Systems 677/877
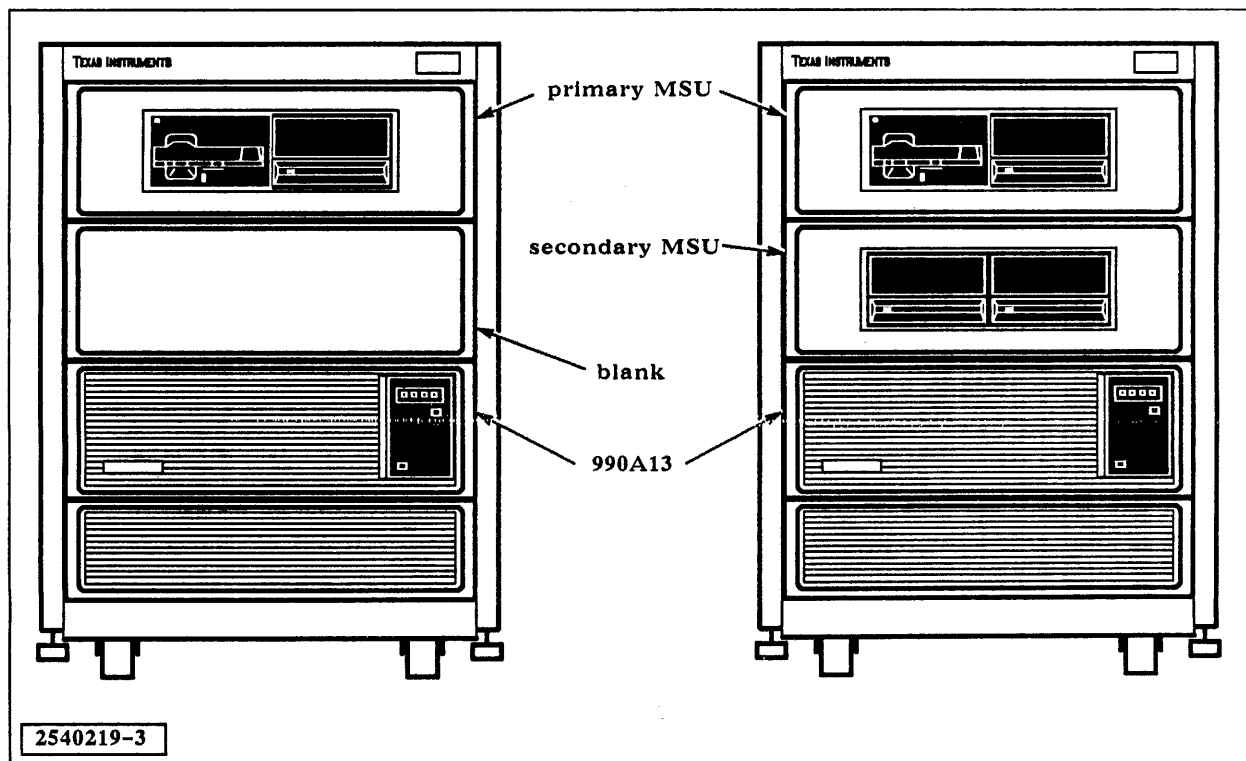
Kits and Part Numbers

1.5 Kit components are provided for mounting the 990/SCSI mass storage subsystem into the 32-inch cabinet. Primary and secondary kits are provided for mounting MSUs as primary and secondary units in the system. The following is a list of the major assemblies of the primary kit. Note that a primary kit will always contain an MSU with one disk and one tape.

■ 990/SCSI controller

■ SCSI interface (I/F) cable

■ MSU kit, including disk and tape, terminator, and power supply

■ Tray sub-assembly (primary rackmount kit)

■ MSU trim kit

The following is a list of the major assemblies of the secondary kit.

■ SCSI interface (I/F) cable

■ MSU kit, including disk and/or tape, terminator, and power supply

■ Secondary rackmount kit

The following is a list of major system component part numbers.

990/SCSI controller	2549505-0001
Table top MSU II kits	2552452-xxxx*
Rackmount MSU II kit	2552456-xxxx*
Tape cartridge media (450 ft), 310 oe	2270391-0001
Tape cartridge media (600 ft), 310 oe	2270391-0002

* Dash numbers indicate voltage/frequency and disk/tape configuration. xxxx varies depending on configuration.

INSTALLATION, OPERATION, AND PM

2
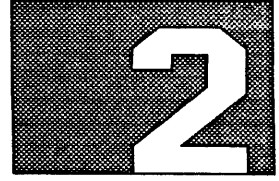
Introduction

2.1 This section contains 990/SCSI mass storage subsystem information on the following topics:

■ Installation

■ Operation

■ Preventive maintenance (PM)

Installation

2.2 When the 990/SCSI controller is shipped as part of a 990 computer system, the controller and primary MSU are installed at the factory. Secondary MSUs and tape drives are shipped in boxes and are available as factory or field installed options.

The instructions for installing the 990/SCSI controller and secondary or add-on MSUs are presented in the following paragraphs.

Unpacking

2.2.1 The 990/SCSI controller is shipped packaged within an MSU pack along with an MSU, an SCSI bus cable, and a package of documents (Refer to Figure 2-1). Inspect packaging immediately upon receipt for evidence of abuse.

CAUTION: The 990/SCSI controller contains static-sensitive electronic components. To avoid damage to these components, ensure that you discharge any accumulated static before removing or handling the printed circuit boards. This can be done by touching a grounded object before unpacking the board. Then, as a further precaution, place the board on a grounded work surface after removing it from the assembly or its protective package. Before storing or transporting the board, return it to its protective package or the assembly.

NOTE: Save the shipping cartons and packing materials for reshipment of any parts, if required.

CAUTION: To avoid equipment damage, use tools carefully during unpacking.

Figure 2-1   MSU Shipping Container

folder

990/SCSI
controller

MSU
cushion

MSU

MSU box

tape

2540219-4
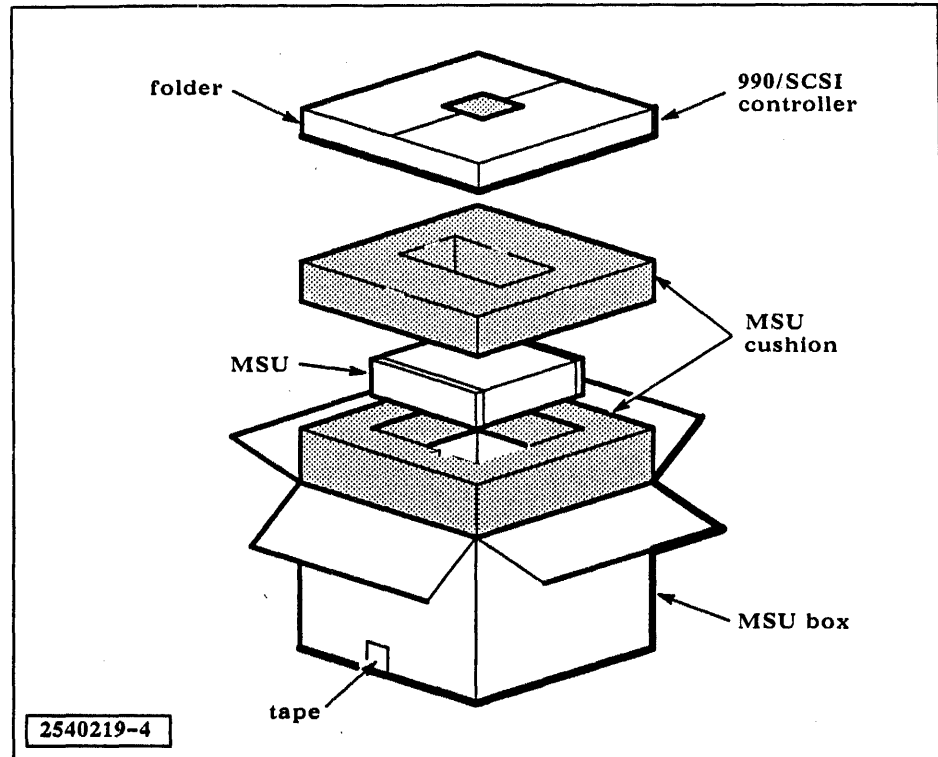
Inspect the 990/SCSI controller for shipping damage. Contact carrier imme-
diately upon discovery of shipping damage.

Switch Setting **2.2.2** The central processing unit (CPU) incorporates the 990/SCSI control-
ler into addressable memory space for access via the TILINE. Switches on
the 990/SCSI controller board determine the TILINE base memory
addresses and must be correctly set prior to use. If the 990/SCSI controller is
shipped as part of a 990 computer system, computer chassis preparation is
done at the factory. The controller is assigned a slot location, the interrupt
jumpers are installed, and the TILINE access-granted (TLAG) jumpers are
correctly set. They should be verified only if they are changed from standard
factory settings.

After the controller switch settings are verified, the hardware is compatible
with the supplied software. If you are installing the 990/SCSI controller,
proceed by selecting the chassis slot.

**CAUTION: Do not connect or disconnect any plug or circuit board when
power is applied to the system since voltage transients may damage elec-
tronic parts.**

Table 2-1 lists the CPU byte addresses and corresponding switch positions for each of these addresses. The standard main 990 computer chassis slot assignment for a system disk controller is slot 7 for the 13-slot chassis. The CPU byte address for the system disk controller is >F800 (all switches in the off position). The CPU byte address for the system tape controller is >F880 (all switches in the off position except switch number four).

If these switches need setting, determine the proper TILINE address according to the operating system software and set the switches accordingly (Table 2-1). For proper operation, the settings of the two switches must not be equal.

Table 2-1 990/SCSI Controller TPCS Switch Addressing

CPU Address	Switch Location AH004 (DISK TPCS) Switch Location BK004 (TAPE TPCS)						
	1	2	3	4	5	6	7
F800	OFF	OFF	OFF	OFF	OFF	OFF	OFF
F810	OFF	OFF	OFF	OFF	OFF	OFF	ON
F820	OFF	OFF	OFF	OFF	OFF	ON	OFF
F830	OFF	OFF	OFF	OFF	OFF	ON	ON
F840	OFF	OFF	OFF	OFF	ON	OFF	OFF
F850	OFF	OFF	OFF	OFF	ON	OFF	ON
F860	OFF	OFF	OFF	OFF	ON	ON	OFF
F870	OFF	OFF	OFF	OFF	ON	ON	ON
F880	OFF	OFF	OFF	ON	OFF	OFF	OFF
• F890	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
FBB0	OFF	ON	ON	ON	OFF	ON	ON
FBC0	OFF	ON	ON	ON	ON	OFF	OFF
FBD0	OFF	ON	ON	ON	ON	OFF	ON
FBE0	OFF	ON	ON	ON	ON	ON	OFF

NOTES:
AH004 switch 1 allows for different SCSI ID mapping of disk 2. Refer to Table 3-2.
BK004 switch 1 is reserved and should be off.

Selecting Chassis Slot

2.2.3 Chassis slot selection is based upon interrupt level and TILINE priority considerations. Each of the 990 packaged systems already incorporates a planned growth path that specifies preferred slot locations, interrupt levels, and TILINE base addresses for standard peripheral controllers.

NOTE: If the next lower-numbered slot contains a board that is equipped with a shield-stiffener, the plastic insulator must be removed from the shield-stiffener of the 990/SCSI controller board. If the next lower-numbered slot contains a board that is not equipped with a shield-stiffener, the plastic insulator must be on the shield-stiffener of the 990/SCSI controller board.

Coordinate interrupt assignments and TILINE address switch settings with the operating system software by system generation (sysgen) procedures. Refer to sysgen instructions in the operating system documentation upon completion of hardware installation.

The TILINE is a common data path that connects to all slot positions in the 990 chassis. Users of this bus fall into two major device types: masters and slaves. Master devices address slave devices and command them to accept or transmit data. Some TILINE peripherals, including the 990/SCSI controller, have both master and slave logic.

To resolve conflicts between multiple masters contending for TILINE control, a positional priority scheme is used. The TLAG signal that establishes positional priority among masters is wired along the P2 side of the computer chassis. The TILINE master installed in the highest numbered slot has the highest priority, with priority decreasing with each slot toward the central processor location (slot 1).

The TLAG signal from a higher priority master enters each master on P2, pin 6. The signal leaves the master on P2, pin 5. Logic on the master allows it to block the output to lower priority masters. Jumpers are installed on the back-panel to assure line continuity across slots not occupied by masters. Additional masters can be inserted at slot positions of higher or lower priority by opening the jumper between P2, pin 5 and P2, pin 6 (TLAG) for the selected slot location. Installing a board with TILINE master logic, such as the 990/SCSI controller, requires the following:

■ The TLAG jumper (P2, pin 5 to P2, pin 6) must be opened for the chosen slot. Opening a TLAG jumper consists of physically pulling out a jumper (13-slot chassis).

■ Continuity of the TLAG lines between the highest priority master and the central processor board must be preserved. This means that if an intermediate slot is assigned to a TILINE master, that master must be installed to preserve continuity and to allow the priority system to function. This also means that the jumpers must be in place (or jumper switches on) for all slots not occupied by TILINE couplers or TILINE device controllers.

Preparing Chassis Slot

2.2.4 Current production units (13-slot) have the TLAG jumpers accessible from the connector side of the motherboard, as shown in Figure 2-2. For these units, perform the following steps:

1. Turn off power and unplug the ac line cord.

2 . Remove any circuit boards that are necessary for access by rocking the plastic ejector tabs firmly. Note the locations and orientation of the boards to reinstall them properly.

3 . Remove the access-granted jumper plug for the selected location.

4. To change interrupt levels, refer to the paragraph entitled Interrupts.

5. Reinstall the circuit boards in the proper locations. Check the configuration label on the chassis to ensure that the boards are installed in the correct slots.

6. Record the new slot assignment on the configuration chart affixed to the chassis.

Figure 2-2 TLAG Jumper Locations for 13-Slot Chassis

assembly 945015-0001 rev (R)

NOTE:
Jumper may be either a removable jumper
plug or a wire that must be cut. Only right half
(P2) of chassis contains tlag jumpers.

2277302
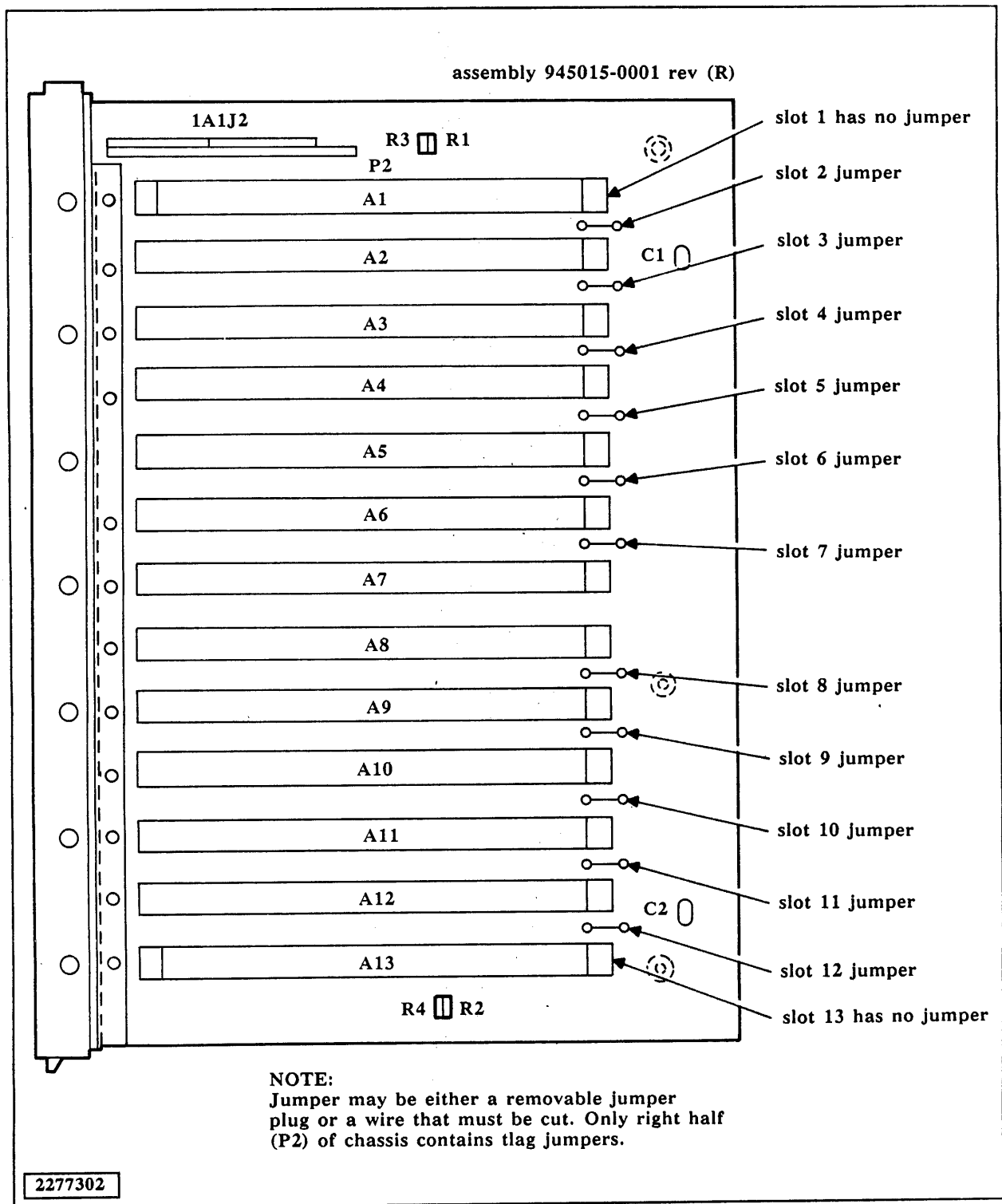
Interrupts   **2.2.5** Interrupt connections to interface peripheral equipment with the 990 processor are usually made before the system is delivered to the customer. The planned growth path for the 990 system avoids the necessity for the customer to modify interrupt levels. Preassigned slot assignments do not require modification of the factory prewired interrupt levels. Note, however, that adding a controller to a previously existing installation requires a sysgen operation to coordinate hardware and software operation.

The information in the following paragraphs is for users who must modify existing interrupt assignments.

NOTE: Refer to the *Model 990A13 Chassis General Description*, TI part number 2308774-9701, or the *Business Systems 600/800 Field Engineering Reference Handbook*, TI part number 2311344-9701, for interrupt information regarding the 990A13 chassis

---

The 990 processor has 16 interrupt levels, numbered 0 through 15. Interrupt level 0, which is internal to the processor, has the highest priority. Interrupt levels 3, 4, and 6 through 15 are external inputs that are available for assignment to peripheral controllers installed in the chassis. The interrupt input lines are wired from chassis slot 1 to an interrupt header adjacent to slot 1.

Each of the remaining chassis slots (numbered 2 and above) has two interrupt output lines wired to the same interrupt header. Interrupt level to device assignments are made by jumper connections at the interrupt header.

Figure 2-3 shows the recommended standard interrupt level assignments and command register unit (CRU) addresses with the type 13-1 interrupt board.

Figure 2-3 Interrupt Assignments — Type 13-1 Interrupt Board

slot number	P1 (chassis front) fixed CRU base address	circuit board	inter-rupt level	P2 (chassis rear) fixed CRU base address	circuit board	inter-rupt level
1	N/A		N/A	N/A		N/A
2	02E0		6	02C0		15
3	02A0		10	0280		8
4	0260		11	0240		12
5	0220		7	0200		3
6	01E0		11	01C0		11
7	01A0		9	0180		13
8	0160		8	0140		9 or 14
9	0120		8	0100		10
10	00E0		12	00C0		11
11	00A0		3	0080		7
12	0060		14	0040		4
13	0020		15	0000		6

13-slot chassis
with interrupt module
type 13-1 board

2540219-20

Notice that the interrupt level for slot 8, P2 side may be either interrupt 9 or interrupt 14. A jumper on the type 13-1 board (Figure 2-4) allows you to select between these interrupts.

White lines painted on the board show the two jumper positions. With the jumper parallel to the interrupt connector, interrupt 14 is selected (8P2 to INT14). With the jumper perpendicular to the connector, interrupt 9 is selected (8P2 to INT9). If the jumper is removed entirely, interrupts generated at the P2 side of slot 8 cannot be recognized. The jumper should always be installed.

Figure 2-4 Interrupt Jumper — Type 13-1 Interrupt Board

Jumper shown in
interrupt level
14 position

INT9

INT14 ─ 8P2

(tape)   (disk)

INTERRUPT
MODULE
TYPE 13-1

SLOT	INTERRUPT	
	P1	P2
1	X	X
2	6	15
3	10	8
4	11	12
5	7	3
6	11	11
7	9	13
8	8	9 OR 14
9	8	10
10	12	11
11	3	7
12	14	4
13	15	6

SCHEMATIC NO.
2310382-9901

ASSY NO.
2310380-1

PWB NO.
2310381-1

SERIAL NO.
(   )

MADE IN U.S.A.

2540219-5
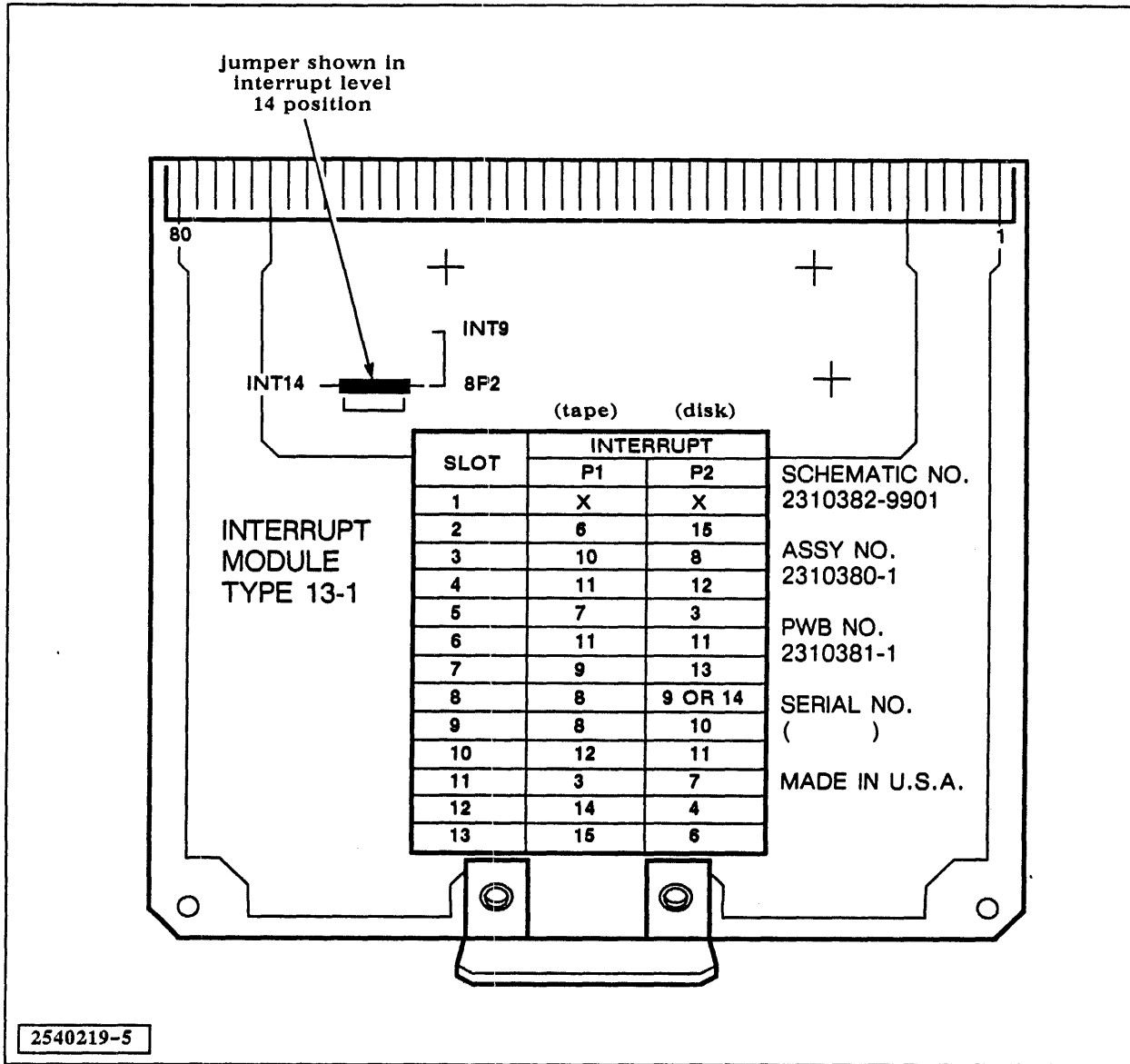
Interrupt 9 is available for use at slot 8 only if it is not used at slot 7, P1 side. Many of the full-size 990 logic boards do not generate interrupts at the P1 connector, making interrupt 9 available for use at slot 8. Refer to the installation manual for the logic board installed at slot 7 for this information.

Interrupt 14 is available for use at slot 8 without such restrictions.

**Installing
Interrupt Board**

2.2.6 Interrupt connections in the 990A13 chassis are made by a small printed circuit board (Figure 2-4) installed directly above slot 1. The interrupt connector is a standard 80-pin connector located at 0P2 (slot 0, P2 side).

NOTE: The following procedure requires complete removal of power, including standby power. Any data in the computer memory will be lost. Save any critical memory data to disk or tape before turning off the power.

To install an interrupt board:

1. Set the rear panel ON-1/OFF-0 switch to the OFF-O position.

2. Disconnect the ac line cord from the rear of the chassis.

3. If standby power supply is installed, ensure that standby power is off.

4. Extend the chassis on its slides, or otherwise gain access to the right side as viewed from the front. Remove any logic boards in slots 1 through 6 for ease of access.

5. A white nylon latch knob is suspended from the chassis top cover by a metal bracket. Turn the knob so the grooved front part is horizontal and parallel to the chassis top cover.

6. Orient the interrupt board with the latch bracket on top and the connector end pointed toward the chassis backpanel.

   Insert the board into the chassis with the board connector just touching the chassis connector. Do not press home.

7. Align the interrupt board so the grooved part of the nylon latch passes through the slot in the latch bracket. Adjust the board position so the connector and latch bracket are both aligned in their mating position.

   Gently press the interrupt board home in the chassis connector. Do not use excess force. If the connectors do not mate on the first try, realign the board and try again. A gentle side-to-side rocking motion helps.

8. Turn the nylon latch knob 90 degrees either way to hold the interrupt board in place.

9. Reinstall any logic boards that you removed.

10. Replace the line cord.

11. Turn on standby power.

Installing
Controller Board

2.2.7 Now that you have completed chassis slot selection and preparation, and have selected the interrupts and installed the interrupt board, you are ready to install the 990/SCSI controller board into the chosen slot of the 13-slot chassis, by performing the following procedure:

CAUTION: Always turn off power to the chassis before attempting logic board installation or removal. Failure to observe this precaution can result in damage to the board since connector pins may be temporarily misaligned during board removal and installation.

---

1. With system power off, insert the 990/SCSI controller board (component side up) into the assigned slot in the 990 chassis. Make sure the circuit board edge connectors mate firmly with the backpanel connectors.

2. Connect the SCSI cable to connector P3 on the 990/SCSI controller board.

CAUTION: Insert the connector carefully to avoid bending pins. Bent pins may cause erratic operation.

Planning

2.2.8 Power and environmental requirements for the 990/SCSI controller are listed in Tables 2-2 and 2-3. For more comprehensive information on system power requirements, refer to the *Business Systems 600/800 Site Preparation,* TI part number 2311340-9701.

■ Ensure that power and environmental conditions meet the requirements specified in Tables 2-2 and 2-3.

■ If there is a conflict between the requirements of Tables 2-2 and 2-3 and the site requirements of your computer system, the requirements in Tables 2-2 and 2-3 should be followed.

Table 2-2

990/SCSI Controller Power Requirements

	+5 Vdc	+12 Vdc	-12 Vdc
Typical Amps (statistically calculated)	5.7	0.010	0.008
Typical Amps (calculated)	5.0	0.010	0.008
Maximum Amps (calculated)	7.9	0.022	0.020
Measured Amps	5.3	0.069	0.060

NOTES:
All voltages +/-5 percent
+/- 12 Vdc calculated current based on SN75150 data sheet
+/- 12 Vdc calculated current required for P4 line drivers/receivers only.

Table 2-3 990/SCSI Controller Specifications

Item	Specifications
Temperature:	
Operating:	0 to 50 degrees C, 32 to 120 degrees F
Non-operating:	−40 to 65 degrees C, −40 to 149 degrees F

NOTE: Operating temperature is derated 2 degrees Celsius for every 762 meters of elevation.

Relative Humidity:	
Operating:	20% to 90% (non-condensing)
Non-operating:	5% to 95% (non-condensing)
Shock:	
Operating:	3 g for 11 ms
Non-operating, unpacked:	30 g for 11 ms
Non-operating, packed:	60 g for 18 ms

NOTE: Non-operating, packed specification is tested by applying shock directly to packed unit.

Vibration:	
Operating:	0.15 mm, 10 to 60 Hz.
Non-operating, unpacked:	2.0 g, 10 to 200 Hz.
Non-operating, packed:	5.1 mm 5 to 10 Hz.
	2.0 g, 10 to 50 Hz.
	3.5 g, 50 to 500 Hz.

NOTE: Non-operating, packed vibration is tested by applying vibration directly to packed unit.

Altitude:	
Operating:	−1000 to 6,500 feet
Non-operating:	−1000 to 10,000 feet

**Installing Primary
Rackmount Adapter**

2.2.9 The rackmount adapter containing the primary MSU for Business Systems 67x/87x is installed at the factory. The SCSI bus cable is installed from the 990/SCSI controller to the MSU, and the terminator is installed on the MSU. The power cord is part of the cabinet. The front panel is shipped with the system but is not installed. Figure 2-5 shows primary and secondary MSUs in rackmount adapters installed in a 32-inch cabinet with the side panel removed. The 990 computer is shown mounted in the lower portion of the cabinet, with the cabling from the computer to the MSU visible. Figure 2-6 shows the side view of a 32-inch cabinet with the side panel removed. The rackmount adapter containing an MSU is shown installed in the top of the cabinet.

Figure 2-5 32-Inch Enclosure Front and Side View

2540219-6
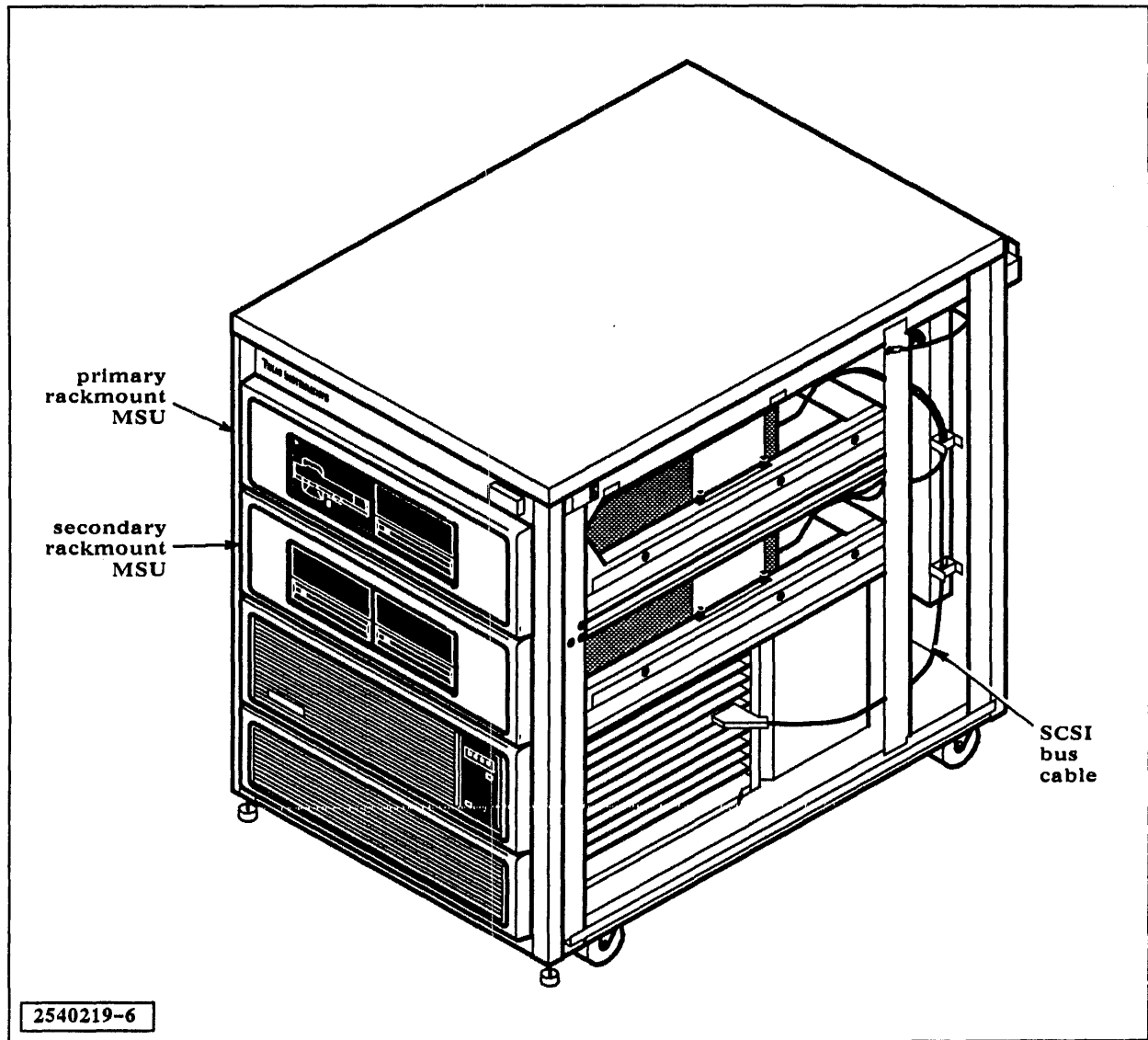
Figure 2-6   32-Inch Enclosure Side View, Side Panel Removed

2540219-22
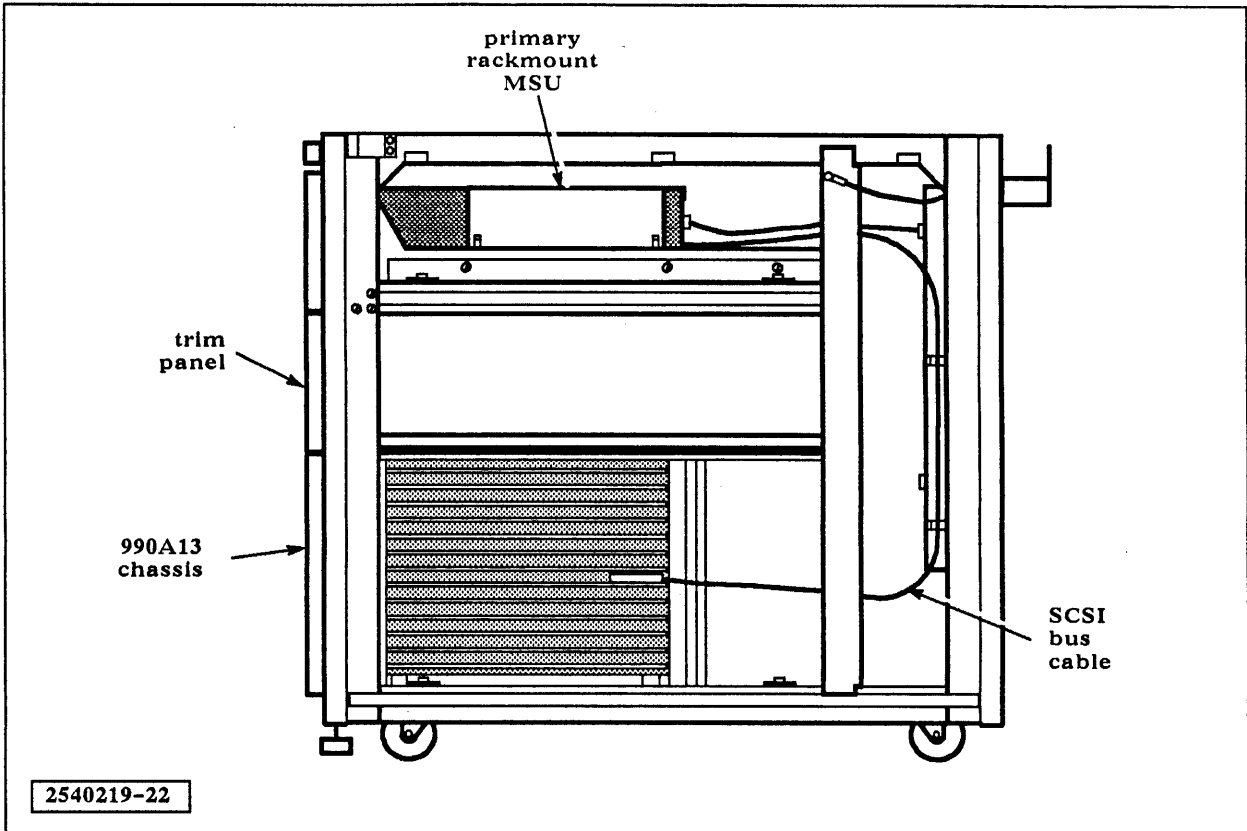
Installing Secondary Rackmount Adapter

2.2.10 The rackmount adapter for a secondary MSU in Business Systems 67x/87x is installed at the factory when ordered as factory installed kits. Otherwise the front panel for the MSU is taped to the tray. Secondary MSUs and connecting cables are shipped in a kit box and installed at the customer's site.

Secondary rackmount adapters include a power spreader to increase the allowable number of plug-ins to three. In systems with one or more secondary MSUs, the terminator is installed on the last secondary MSU.

Detailed instructions are included in the rackmount adapter kit. Refer to these instructions for information regarding actual installation of the tray assembly and MSU.

32-Inch Cabinet Tray Assembly

2.2.11 Figure 2-7 shows details of a rackmount kit for 32-inch cabinets. Figures 2-7 and 2-8 identify the components of the tray sub-assembly and rackmount adapter and illustrate installation and removal of the MSU from the tray.

Figure 2-7   32-Inch Enclosure Rackmount Kit

daisy chain cable

tray

controller to MSU cable

trim panel

2540219-26
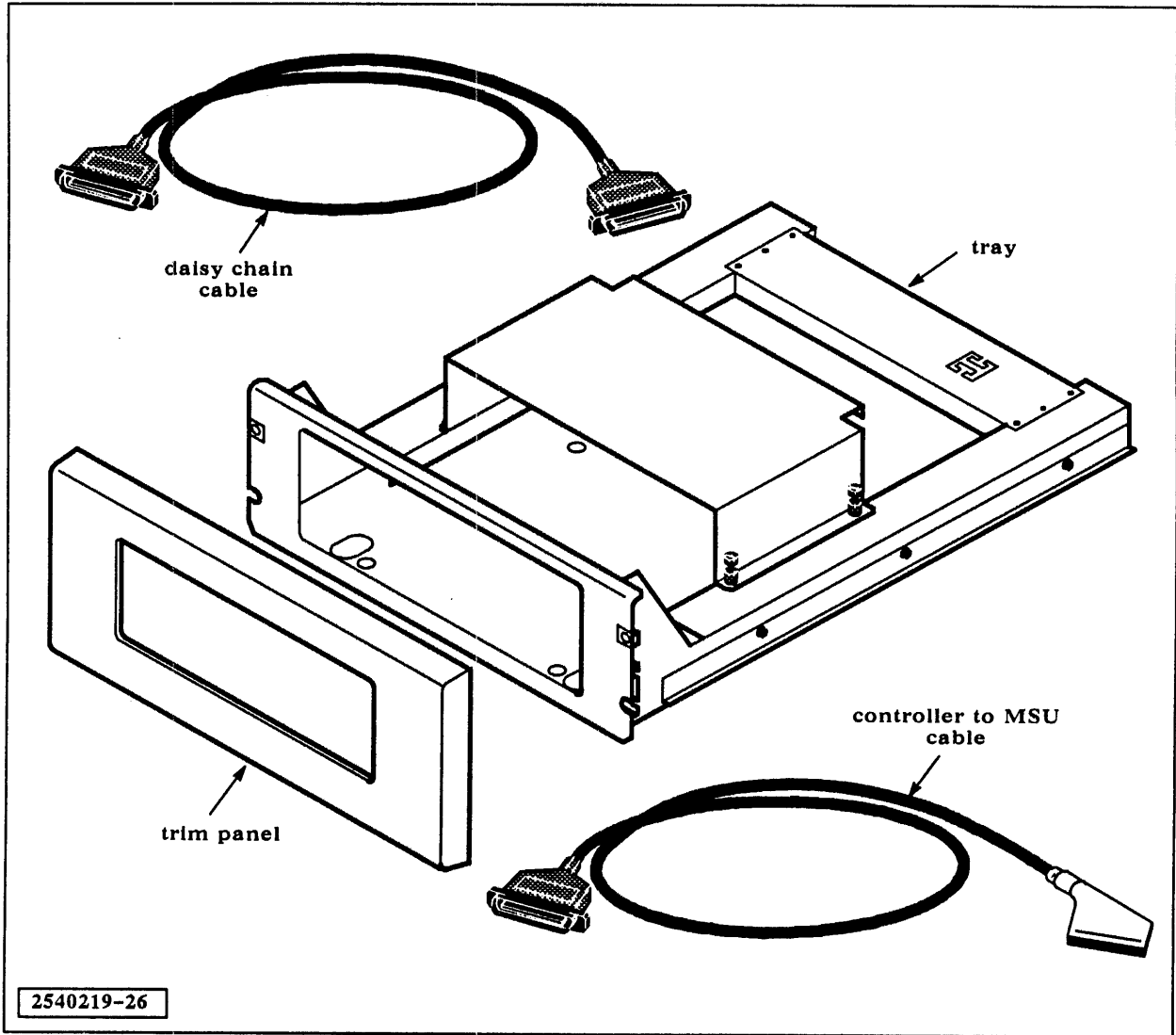
Figure 2-8   MSU Installation and Removal From Tray

2540219-23
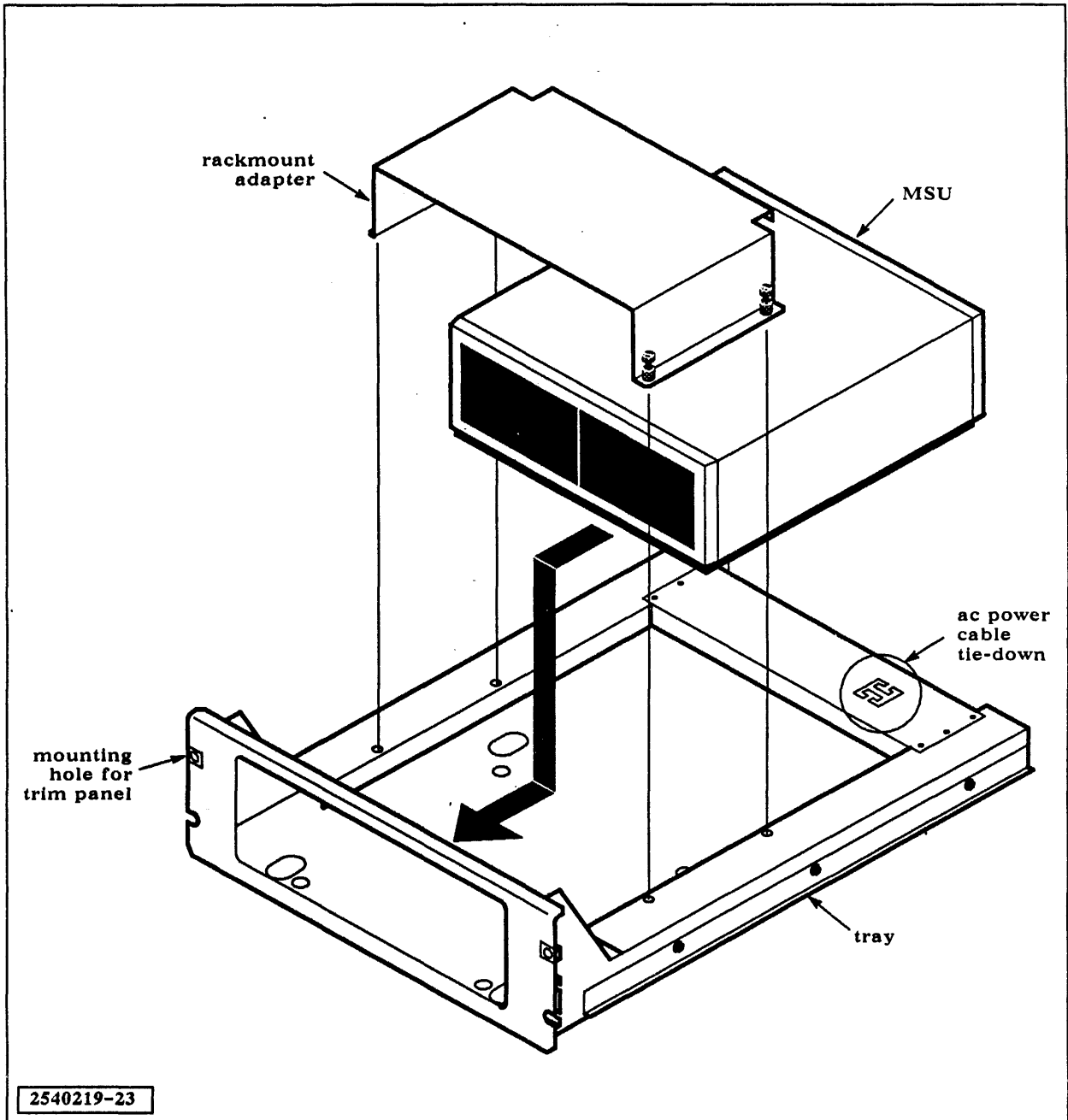
32-Inch Cabinet and Table Top Mounting

2.2.12 Figure 2-9 shows a system with primary and secondary MSUs installed in a 32-inch cabinet, and an additional MSU mounted on a nearby table top. The figure shows a typical cable routing for this type of system. Figure 2-10 shows the SCSI bus cables.

Figure 2-9 Cable Routing Including Table Top on 67x/87x

2540219-25
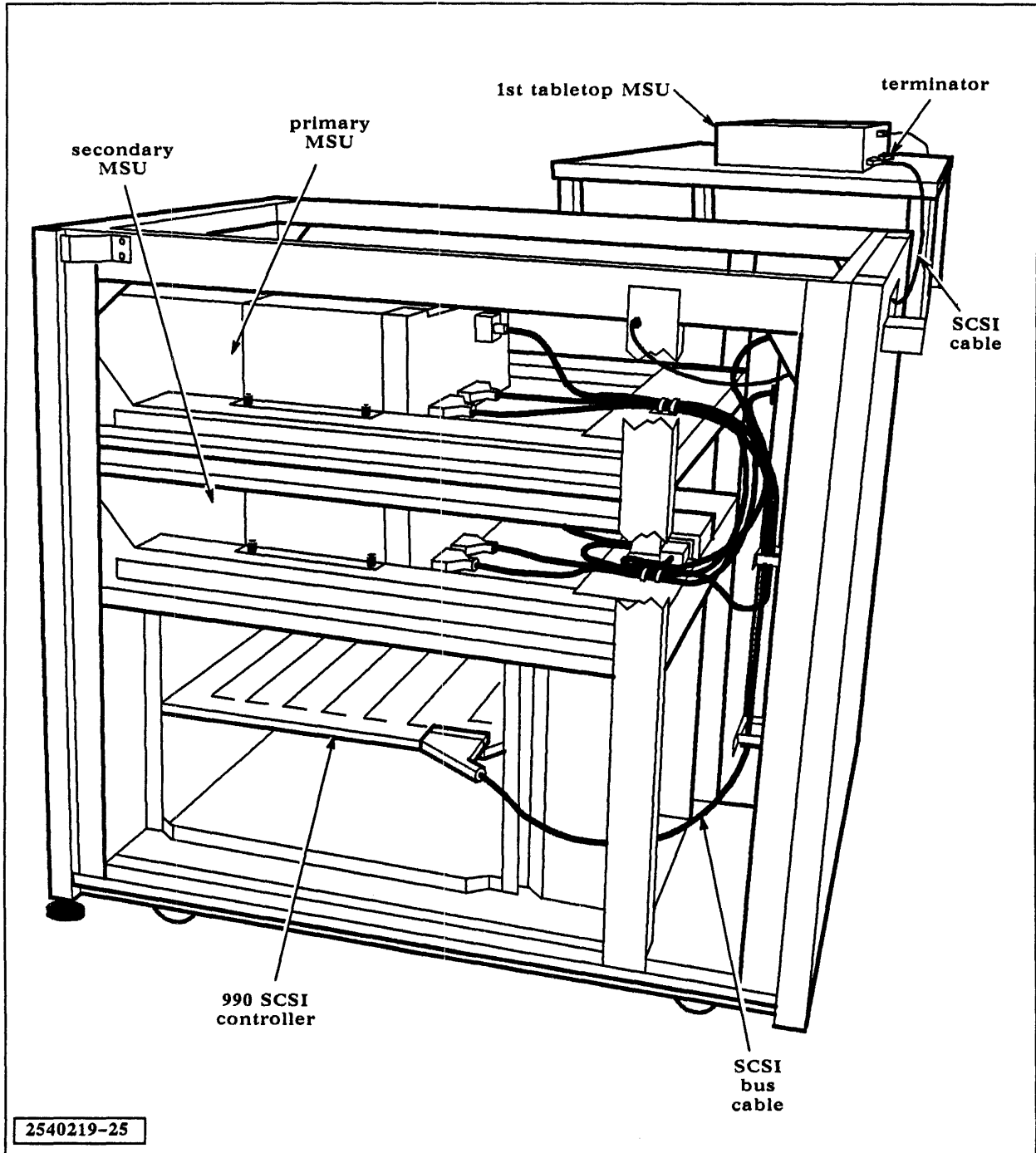
Figure 2-10   SCSI Bus Cables

CHAMP
connector

AMPMODU
connector

CHAMP
connectors

2287751
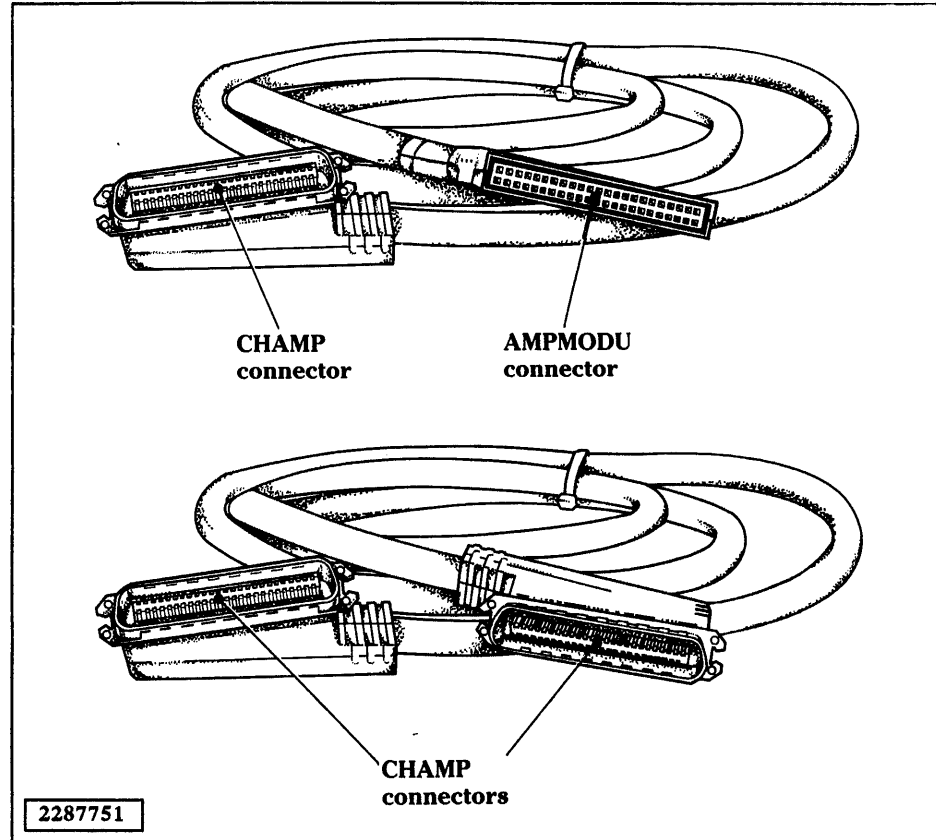
NOTE: For reliable operation, you must use shielded cables.

Unpacking/Installing
Additional MSUs

2.2.13 Figure 2-11 shows the SCSI daisy-chain cable used for interconnecting table top MSUs. For MSU owners who install additional table top MSUs, perform the following steps to unpack and install the MSU:

1. Locate the MSU General Description manual packed in the top carton of the MSU pack. Unpack and inspect as described in the MSU manual.

2. Insure that formatter ID switches are properly set as shown in Table 3-2 and Figure 3-1 of this manual (990/SCSI). Refer to the appropriate MSU manual if changes are needed.

3. Route cables as described in paragraph 2.2.16 entitled Cable Routing.

4. Refer to the appropriate software manual for making any software changes.

Figure 2-11   **SCSI Daisy-Chain Cable**

2287711
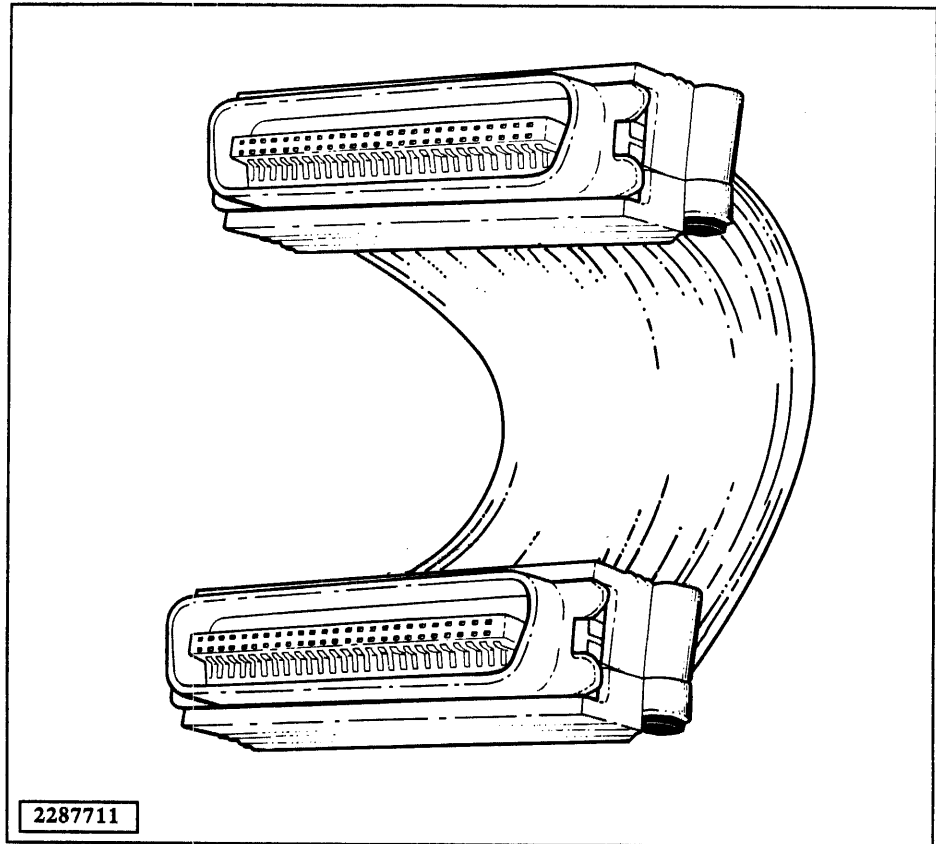
Placement of Equipment

2.2.14 In a Business System 67x/87x, the MSU primary and secondary kits are installed within the 32-inch cabinet. In extended systems, MSUs can be placed on top of the 32-inch cabinet or on a tabletop or desk.

CAUTION: Do not stack more than two MSUs on top of each other. When more than two units are stacked on top of each other, there is a danger of the stacked units becoming top heavy and possibly tipping over.

Do not place the MSU in a closed compartment with limited air circulation. Heat buildup within such an environment can result in damage to one or more components of the MSU.

To avoid possible damage to the MSU power supply, ensure that the voltage range select switch is in the proper position prior to connecting the ac line cord or applying power.

It is important to keep the air cooling intake and exhaust vents of the MSU free of any obstructions. Position the enclosure so that air is free to enter and exit all air intake and exhaust vents. Also, avoid any accumulation of articles, such as books, in front of the MSU where they can hinder the airflow.

Air is drawn in at several points on the front of the MSU, as shown in Figure 2-12. Intake slots are located across the front bottom of the unit and on the front panel of most disk drives. The disk and/or tape drives are recessed slightly behind the front frame of the unit to allow air to enter around the edge of the panels. For a tape drive, the cartridge compartment serves as the front air intake.

Figure 2-13 shows the airflow paths within the MSU. Air enters at point A around the edge of the disk or tape drive panel and flows over the top of the drive and down into the exhaust fan. The front panel air intake slots on most disk drives allow air to enter at point B. The air then flows beneath the drive to cool the components on the drive's printed wiring board (PWB) then up into the fan. The air that enters at point C splits into two paths to provide cooling for both sides of the SCSI/ESDI disk drive formatter board.

The fan draws the air from the front of the MSU, blows it over the power supply area to the back of the unit, and out the top and bottom edges of the access cover.

If the intake or exhaust airflow is blocked, the temperature inside the MSU II can rise to unacceptable levels. A sensor on the power supply board monitors the internal temperature and provides two overtemperature thresholds. At the first threshold, the power supply issues a warning to the host system via the host interface. At the second threshold, the power supply issues a reset signal and shuts down to prevent component damage.

The MSU IIA does not support this overtemperature sensing.

Figure 2-12   Front View of Two MSUs Showing Air Intake

air intake

tape drive

disk drive

disk drive

disk drive

2287713
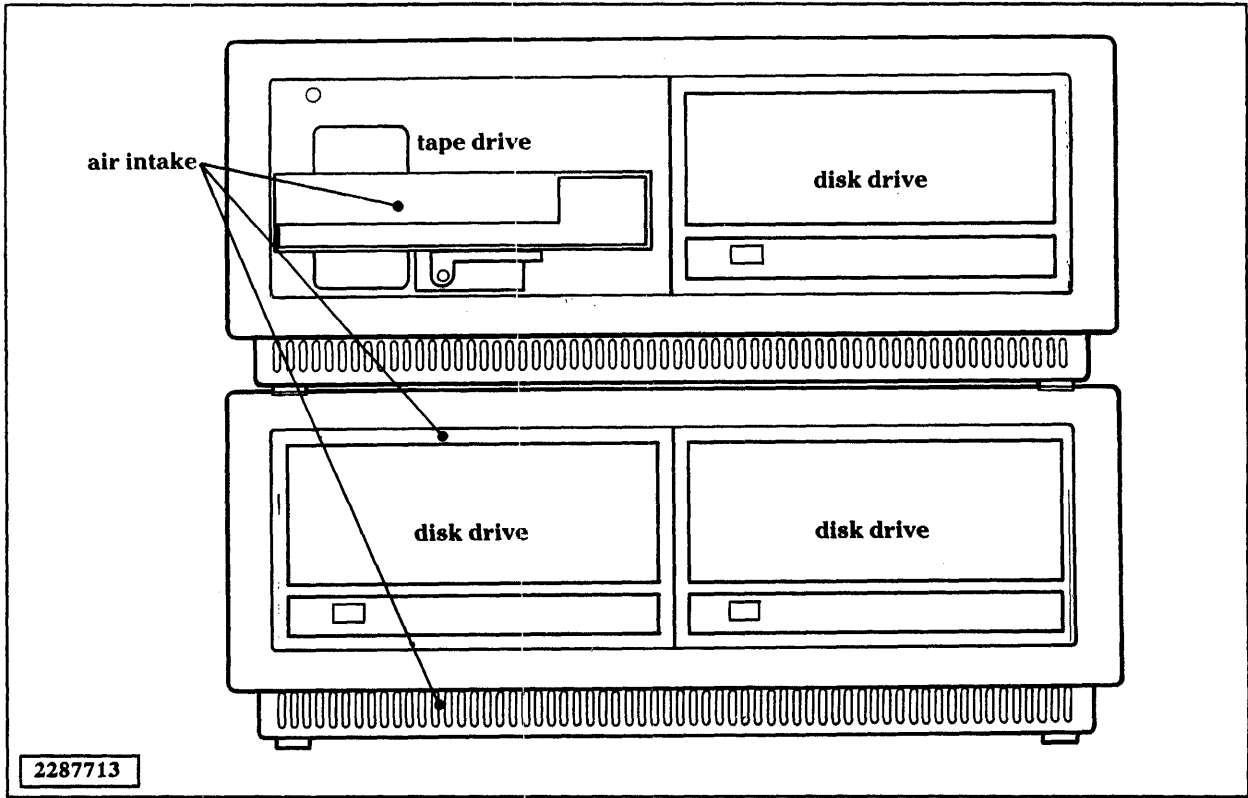
Figure 2-13   Airflow Through the MSU

disk/tape drive

fan   power supply

A

access cover

B

C

PWBs (MSU II only)

chassis

2286314
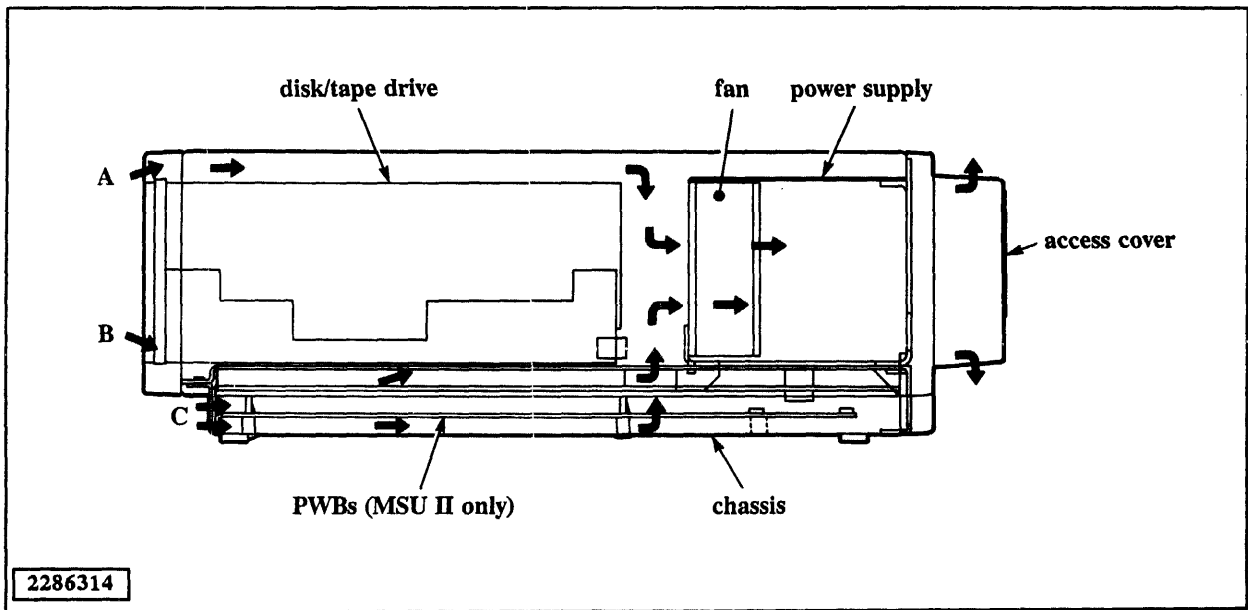
MSU Controls   **2.2.15** All operator accessible controls for the MSU are on the enclosure rear panel (Figure 2-14). The power on/off switch is a two-position, push-button switch labeled 0 (off) and 1 (on). As the label indicates, position 0 is with the switch all the way out (disengaged); position 1 is with the switch all the way in (engaged). The lightning-bolt symbol near the switch indicates that this is an ac power control.

The power transformer for the MSU power supply has a split primary winding. The voltage range select switch (labeled 115 V and 220 V) connects the two primary windings in parallel for a line voltage range of 100 to 132 volts, or in series for a line voltage range of 180 to 264 volts. The switch labels are arranged to show only the selected range (115 V or 220 V).

A label above the fuse holder lists the proper fuse values for the two ac line voltage ranges. The correct fuse values are as follows:

■   115 volt range — 5 amperes, 250 volts ac, slow blow (TI part number 0416434-0503)

■   220 volt range — 2 amperes, 250 volts ac, IEC 127-III (TI part number 2248068-0023)

Figure 2-14   **Rear View of the MSU**

2287714
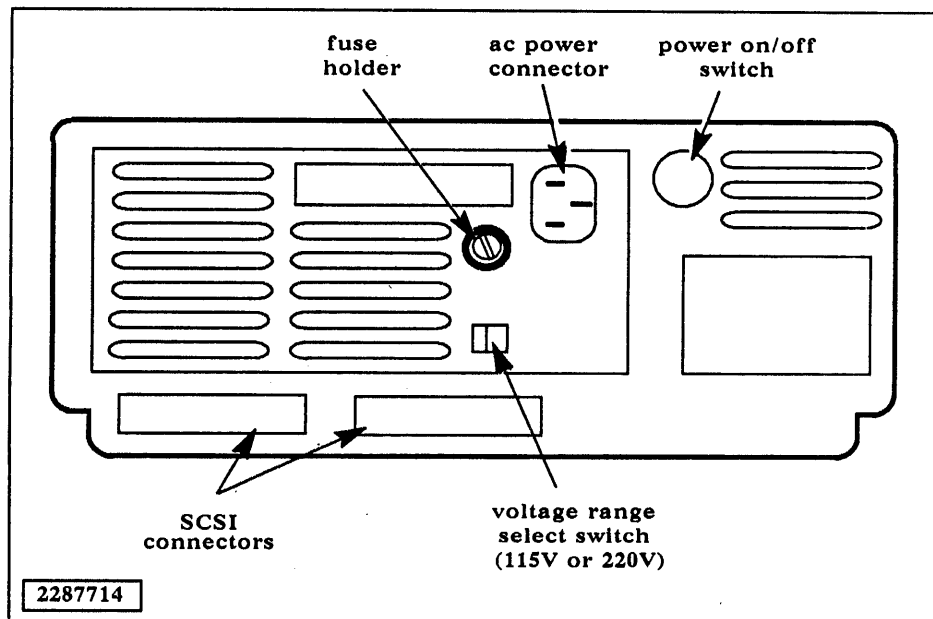
NOTE: The MSU connected directly to the host computer is called the primary enclosure (not to be confused with primary storage, which is generally considered to be the main memory of a system). The additional second, third, and fourth MSUs are known as secondary enclosures. Each computer system must have one (and only one) primary enclosure.

Cable Routing   2.2.16 Signal cable and power cord routing between the MSU and the host computer depends on the placement of the MSU in relation to the host computer.

CAUTION: Be very careful that you do not bend or break any connector pins when you connect and disconnect the SCSI cables, adapters, or terminators. Push or pull on both ends of the connectors at the same time whenever you connect and disconnect cables, adapters, or terminators. Always inspect connectors for bent pins and proper connector alignment before you install any cables, adapters, or terminators.

Figures 1-3 and 3-1 show examples of multiple MSU tabletop connections. The terminator is always installed at the end of a daisy-chain SCSI bus.

The maximum allowable total length of the SCSI bus, including the daisy-chain cables, is 6 meters (19.68 feet). Optional 1-, 2-, and 3-meter (3.28-foot to 9.84-foot) SCSI bus cables are available to keep this length within tolerance. Figure 2-15 shows a typical arrangement for a 990/SCSI mass storage subsystem.

Figure 2-15   **990/SCSI Mass Storage Subsystem With Two MSUs**

2540219-24
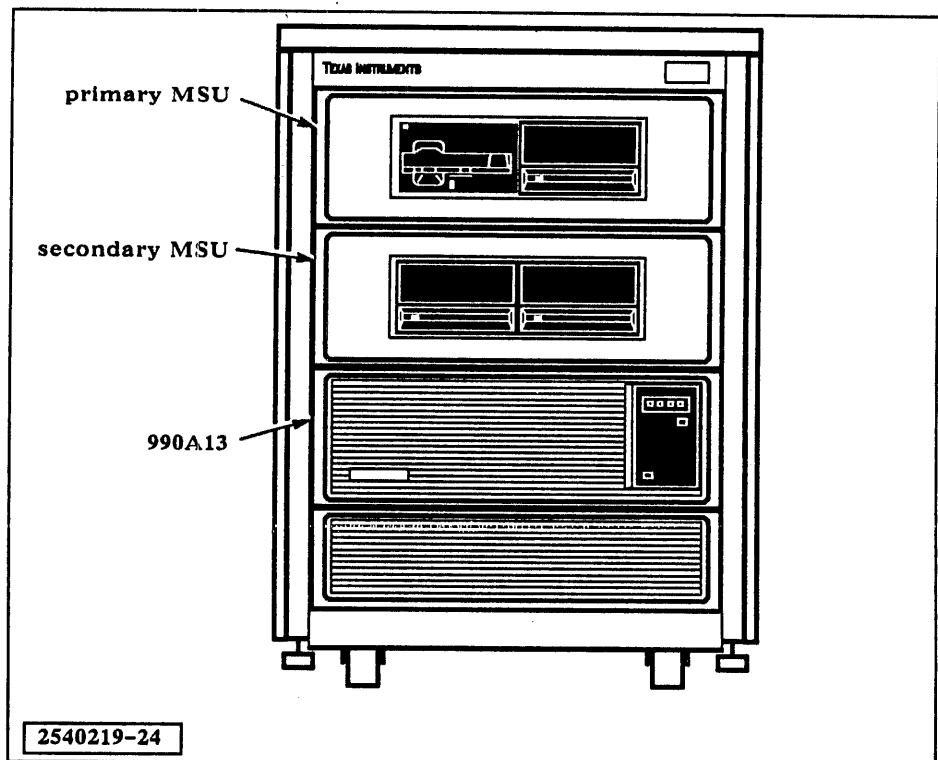
**Configuring
Add-On MSUs**

2.2.17 When a mass storage subsystem includes more than one MSU, the SCSI bus address (SCSI ID) switch on additional MSUs may need to be reconfigured. The convention for SCSI IDs is to use even numbers for disk drives (for example: 0, 2, 4, 6), and odd numbers for tape drives (for example: 3, 1, 7). Refer to Table 3-2 entitled TPCS Unit to SCSI Formatter Mapping and Figure 3-1 entitled System Level Block Diagram and to the appropriate *Mass Storage Unit (MSU)* manual to ensure that proper formatter SCSI IDs are set up.

NOTE: A SELECT switch on the 990/SCSI controller may also need to be set to accomplish the desired configuration. (Refer to Table 3-2 on formatter mapping.)

**System
Grounding**

2.2.18 MSU IIs have a switch on the disk formatter board or the cable interconnect board that connects chassis and logic ground (MSU IIA enclosures have the connection on the cable interface board). This switch is closed (making the connection) on MSUs shipped from TI.

Refer to the appropriate *Mass Storage Unit (MSU)* manual for information on locating and altering this switch, along with other MSU switches.

Controller
Operation

2.3 Once the controller has been installed, and the power to the chassis is applied, the controller will execute a self test to ensure the board functions before operation begins. The LEDs on the board should be observed to verify that the controller self test has passed.

Three LEDS are provided to indicate self-test fault and disk/tape active status. These LED indicators are located on the outer edge of the board (Figure 1-1), adjacent to the right ejector-injector tab. Table 2-4 defines the functions of the indicators. The red LED is located closest to the middle of the board.

Table 2-4

LED Definitions

Indicator	Color	Function
Fault	Red	Self-test and board summary fault indicator. Turns on (lit) at the beginning of self-test and turns off to indicate successful completion. When blinking, indicates a controller hardware error has occurred which may be recoverable by cycling power or resetting the controller.
Disk TPCS Active	Green	When on (lit), indicates that a disk operation has been requested and is not yet complete.
Tape TPCS Active	Green	When on (lit), indicates that a tape operation has been requested and is not yet complete.

All indicators are controlled by MC68010 control firmware routines rather than by dedicated fault detection hardware. Therefore, the indicator definitions may vary with firmware releases. Indications may be misleading in the event of a firmware error or a fault related to the microprocessor and its input/output (I/O) data transfer. Self-test error codes will be passed to the user via the TILINE peripheral control space (TPCS) registers. Refer to the paragraph entitled Maintenance/Diagnostic Commands in Section 3 of this manual for additional information.

MSU Operation

2.4 The MSU operation instructions are arranged under the following topics:

- Start-up

- Self-tests

- Tape cartridge operating precautions

- Tape cartridge insertion and removal

Earlier MSU IIs may contain Cipher drives; Archive drives, which differ from Cipher drives, are in current MSU configurations. Refer to the *MSU General Description* manual for details on how to physically distinguish these two drives.

Start-Up

2.4.1 The following paragraphs provide start-up information for the mass storage enclosure.

CAUTION: Before applying power to the MSU, make sure that the voltage range select switch on the back of the unit is in the proper position. The proper position depends on whether you are using a low line voltage (approximately 120 volts ac) or a high line voltage (approximately 240 volts ac). The location of this switch is shown in Figure 2-14.

MSUs are normally plugged directly into receptacles within the 32-inch cabinet that must be switched on to provide ac input power.

Self-Tests

2.4.2 Almost immediately after the power is applied, the following occurs if the MSU is running properly:

■ You hear the disk drive spindle motor start.

■ The LEDs on the front panel come on.

■ The MSU performs self-tests while the LEDs remain on.

During the self-tests, the disk formatter reads certain information from the disk to verify reliable operation, while the tape formatter proceeds through tests of its various buffers and internal circuits.

■ At the conclusion of the self-tests, the panel LEDs on the disk drive go out. The LED on the Cipher tape drive lights when a tape cartridge is installed and ready for use. The LED on the Archive tape drive lights only when the tape is (or has been) in active motion. The Archive LED goes out when a completed rewind or unload command is terminated, while the Cipher LED turns off when the cartridge is removed or an unload command completes.

■ If a drive or formatter fails the self-test, the panel LEDs on the disk drive continue to flash.

After a self-test is complete, the sequence of events varies with the system configuration. Normally, an initial program load proceeds with appropriate messages visible on the system monitor. If you suspect that something is wrong, check the fault LEDs on the 990/SCSI controller and the LED on the disk drive.

Tape Cartridge Operating Precautions

2.4.3 To prevent the loss of data and extend the life of your equipment, observe the following precautions when using the tape cartridge.

■ Make sure the tape drive is not in use before you remove the tape cartridge.

■ Use your unload software command, Unload Logic Unit Number (Unload LUNO), to prepare the tape cartridge for removal from the tape

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drive. The Unload LUNO command performs a retension and places blank leader tape under the access door instead of recording tape, helping to prevent contamination of the recording media. Refer to your applicable computer application software to execute a tape unload.

■ Store your tape cartridge in a dust-free location with temperatures in the range of 5 to 45 degrees Celsius (41 to 113 degrees Fahrenheit) and humidity in the range of 10 to 80 percent. Note that the operating humidity is limited to a range of 20 to 80 percent, and operating temperature is 10 to 35 degrees Celsius (50 to 95 degrees Fahrenheit).

■ Keep your tape cartridge away from magnets and machines that produce magnetic fields, such as fans, typewriters, X-ray machines, and other power machines.

■ Do not expose your tape cartridge to heat, direct sunlight, or moisture.

■ Keep your tape cartridge away from sticky, oily, or abrasive substances.

■ If a tape cartridge is stored at a temperature significantly different from that of the tape drive, let the tape cartridge reach room temperature before using it.

■ If you suspect a tape cartridge has been exposed to an extreme temperature, re-tension the tape before you read from or write to the tape. Refer to your applicable computer application software to re-tension the tape (Unload LUNO command).

■ For longest head life, media with a coercivity of 310 oersteds is recommended.

Tape Cartridge Insertion/Removal

2.4.4 The insertion and removal of the tape cartridge in the Cipher and Archive tape drives is explained in the following paragraphs.

Before you insert a tape cartridge, check that the protect mechanism is set properly. To write on the tape, set the file protect mechanism so that the arrow points away from the word Safe. When the arrow points to the word Safe, the tape is write protected.

When the tape cartridge is inserted, the Cipher drive automatically verifies that the cartridge is inserted correctly and then, before executing a write or read command, it rewinds the tape to the beginning of tape (BOT) holes in the tape. For Archive units (or drives), this sequence is executed upon receipt of the first command.

Cipher Tape Drive Cartridge Insertion and Removal

2.4.4.1 The Cipher tape drive has a sliding tray that holds the tape cartridge in the drive. A lever in front of the tray rotates 90 degrees to lock the tray in the drive. You must pull out the tray before you insert a tape cartridge into the drive. Position the tape cartridge so that its clear plastic side is up, with the tape access door to the right, before you place it in the tray. If a tape cartridge is not inserted into the tray, lock the empty tray in the drive as a safety precaution.

Archive Tape Drive
Cartridge Insertion
and Removal

2.4.4.2 The Archive tape drive allows the cartridge tape to be loaded in only one orientation. The cartridge is loaded by pushing it through the loading aperture until it reaches a hard stop. As the cartridge is inserted, it encounters slight resistance from the ejector assembly. This resistance cushions the loading action. Just before the cartridge reaches the stop point, the cartridge protective door is opened to expose the tape. The stop point is reached when the cartridge metal base drops behind the lip of the front bezel aperture. Move the head loading lever as far as it will move toward the cartridge. This action secures the cartridge and loads the head assembly into operating position.

The cartridge is ejected by sliding the loading lever away from the cartridge. The head assembly retracts, and the cartridge ejection system pushes the cartridge up and out of the drive.

Preventive Maintenance

2.5 Preventive maintenance (PM) for the MSU consists of cleaning the enclosure as needed and cleaning the read/write heads on the tape drive. This maintenance is normally done by the user and not by TI.

Keep the enclosure clean and dust free by wiping the exterior with a damp (not wet) cloth and mild detergent as needed.

CAUTION: Do not use strong detergents, cleaners, or solvents to clean the enclosure.

The read/write heads of the tape drive can accumulate metal oxides and dust. Figure 2-16 shows how particles of dust and smoke, and fingerprints can block the gap between the heads and the tape substrate and cause errors during read/write operations. A large accumulation of material on the read/write heads also can cause poor performance. To ensure good performance from the tape drive, clean the read/write heads after every eight hours of drive use. If you are using a new tape, you should clean the heads after the initial pass of the new tape cartridge to remove the accumulation of metal oxides.

Clean the read and write heads as follows:

1. Set the ac power on/off button on the rear of the MSU to the off (out) position.

2. Remove the tape cartridge (if installed) from the tape drive.

3. Position the heads to the forward position as follows:

   a. In a Cipher drive (Figure 2-17), rotate the lever on the front of the tape drive counterclockwise to its vertical position to position the heads forward. The heads are located in the drive along the right side of the opening where the tape cartridge is inserted. The heads are part of the brass-colored rectangular piece that measures about 13 millimeters (1/2-inch) by 19 millimeters (3/4-inch).

b. In an Archive drive (Figure 2-18), slide the cartridge loading lever toward the cartridge insertion opening until the heads are extended into the cartridge cavity. The heads are located in the drive along the left side of the opening where the tape cartridge is inserted. The heads are part of the brass-colored rectangular piece that measures about 13 millimeters (1/2-inch) by 19 millimeters (3/4-inch).

4. Visually inspect the interior of the drives. If contamination is visible in the sensor holes or within the cartridge cavity of the drive, carefully blow out visible dust or debris from these areas with low pressure air from an aerosol can.

5. Moisten the spade end of a swab with head-cleaning solution until it is saturated but not dripping. It is best to pour the solution on the swab rather than to dip the swab into the bottle. The following head-cleaning materials are available:

   a. CDC head-cleaning solvent number 82365800 (TI part number 0943849-1513). This is a Freon™ solution mixed with a small amount of alcohol.

   b. Archive streaming head-cleaning fluid, Archive part number 14917-001.

   c. Six-inch long swabs made from lintless cotton or equivalent non-abrasive material, or any industry acceptable head-cleaning swabs.

6. Carefully wipe the swab across the heads in the direction that the tape moves. Do not wipe the heads in the direction perpendicular to the tape movement as residue can collect in minute crevices of the head. Do not use a scrubbing, circular motion.

7. Discard the first swab, then moisten a second swab and repeat the wiping motion until all residue has been removed from the head surface.

8. Discard the second swab. With a clean, dry swab, wipe the head using the same motions described in step 6, until the head is clean and dry.

Freon is a trademark of E.I. du Pont de Nemours & Company, Inc.

Figure 2-16 Relative Contamination Particle Sizes

human hair
3×10^{-3} inch
(diameter)

read head gap
50×10^{-6} inch

dust particle
300×10^{-6} inch

finger print
150×10^{-6} inch

smoke particles
40×10^{-6} inch

tape substrate

recording media

2287037
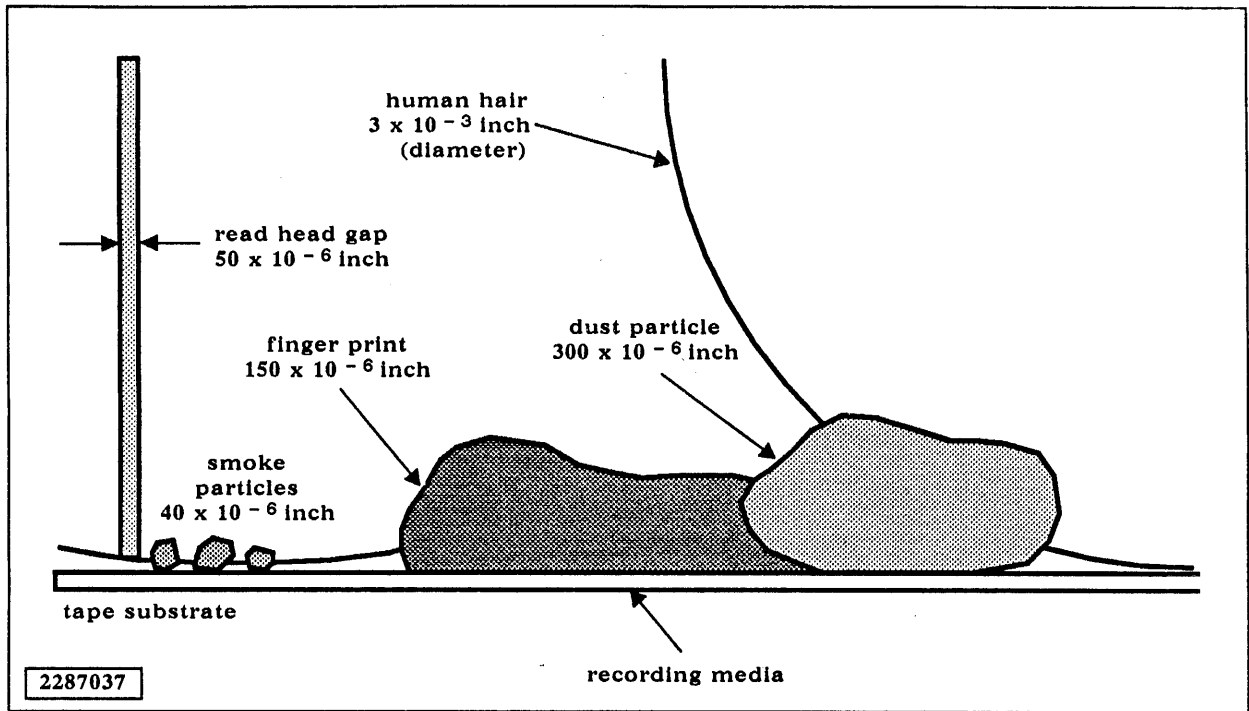
Figure 2-17   **Cipher Tape Drive Read/Write Head Location**

lever   tape drive   read/write heads   tray

2287717
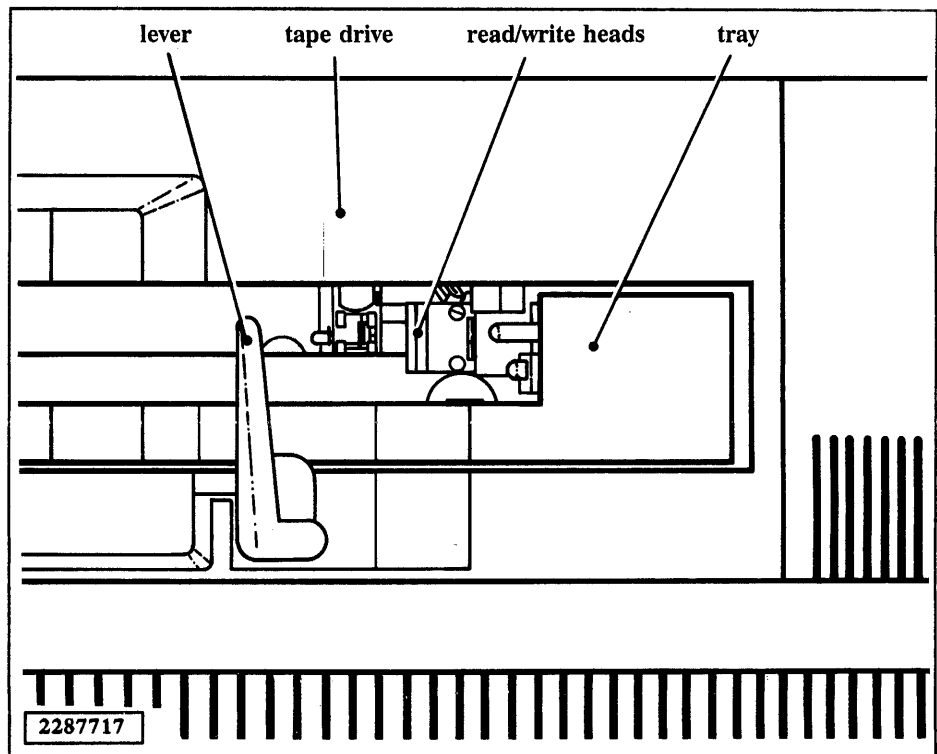
Figure 2-18 Archive Tape Drive Read/Write Head Location

head loading lever

tape drive

Note: This illustration is drawn at an angle to show details of the read/write head mechanism. The read/write head is actually on the left side of the drive.

read/write heads

2288145
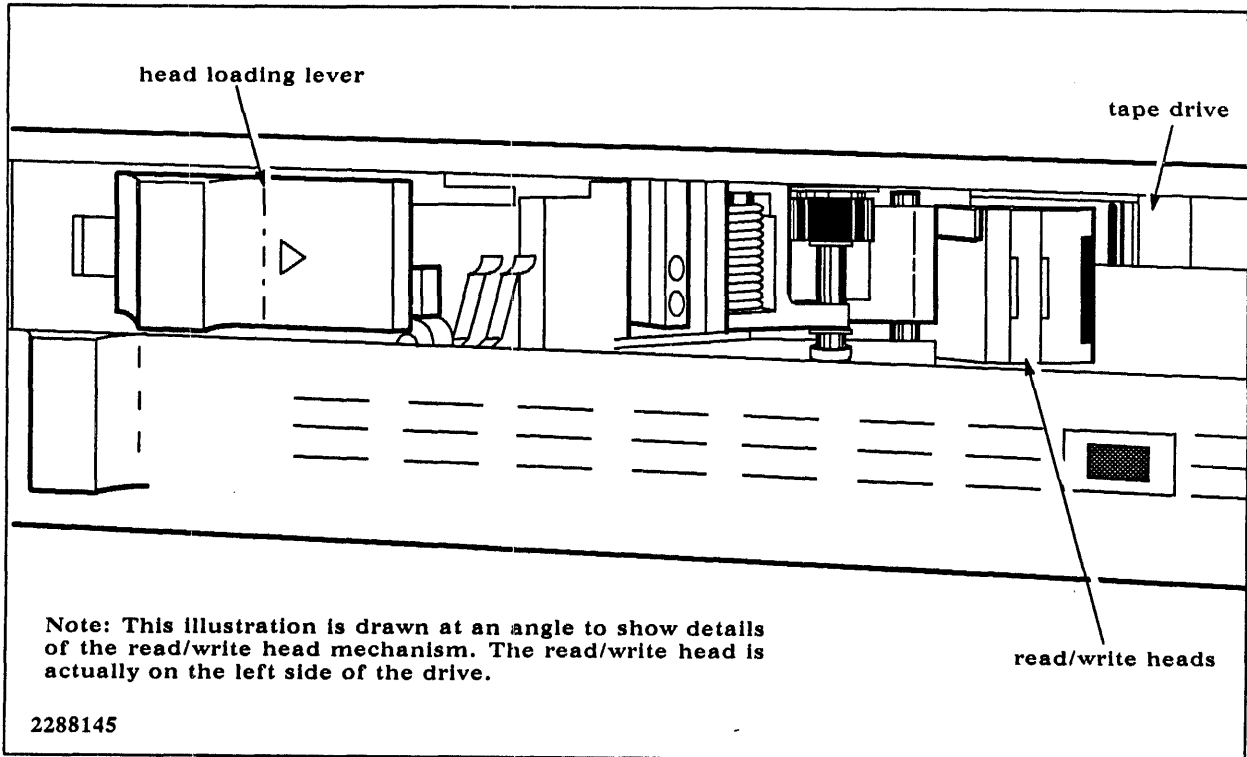
No preventive maintenance on the 990/SCSI controller is required. Refer to the *Chassis General Description* manual (TI part number 2308774-9701) for 13-slot chassis preventive maintenance.

FUNCTIONAL DESCRIPTION

3
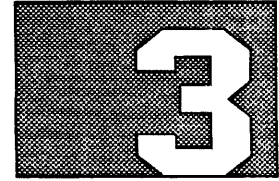
Introduction	**3.1** This section describes the following system level functions of the 990/SCSI Mass Storage Subsystem.
	■ Overview
	■ Hardware
	■ Programming
	■ Self-test
	■ System-Level Information
Overview	**3.2** The 990/SCSI mass storage subsystem consists of the host 990 system, the 990/SCSI controller, one or more MSUs, and optional mounting hardware. Refer to Figure 3-1 for a system level pictorial. This pictorial illustrates proper formatter IDs (and 990 unit numbers) for a maximum configuration using MSU IIs. Figure 3-1A is a maximum system using MSU IIAs. Note the difference in formatter ID mapping due to the use of embedded SCSI drives on the MSU IIA. The host system issues commands to and receives status from the 990/SCSI controller, using the TILINE for address and data transfer. The 990/SCSI controller translates commands reserved for itself and issues all other commands to the appropriate MSU. Formatters contained within the MSU are responsible for controlling the actual storage device. Refer to the appropriate *Mass Storage Unit* manual for details on internal MSU cabling and components.
Hardware	**3.3** Figure 3-2 is a block diagram that details the major components of the 990/SCSI controller. Refer to this block diagram while reading the following. The major blocks are:
	■ TILINE interface
	■ Microprocessor
	■ Autonomous data transfer control
	■ Pack/Unpack data buffer
	■ SCSI data transfer first-in first-out (FIFO)
	■ SCSI bus controller subsystem
	■ System level considerations
	These blocks are discussed in the following paragraphs.

Figure 3-1 System Level Block Diagram — MSU II-Based

CPU

TILINE

memory

990/SCSI
controller
2549505

P2

P3   2550865-0001

P4   2550864-0001

P1

fault
disk busy
tape busy

2550864-0001

2236187-0001

2236187-0001

terminator
2236188-0001

1st rackmount MSU II
tape form ID = 3 (990 T0)
disk form ID = 0 (990 D0)

2nd rackmount MSU II
disk form ID = 2
(990 D1) (990 D2)

1st tabletop MSU II
tape form ID = 6 (990 T3)
disk form ID = 4 (990 D3)

2nd tabletop MSU II
tape form ID = 1 (990 T1)

3rd tabletop MSU II
tape form ID = 7 (990 T2)

2540219-7

form=formatter

Figure 3-1A System Level Block Diagram — MSU IIA-Based
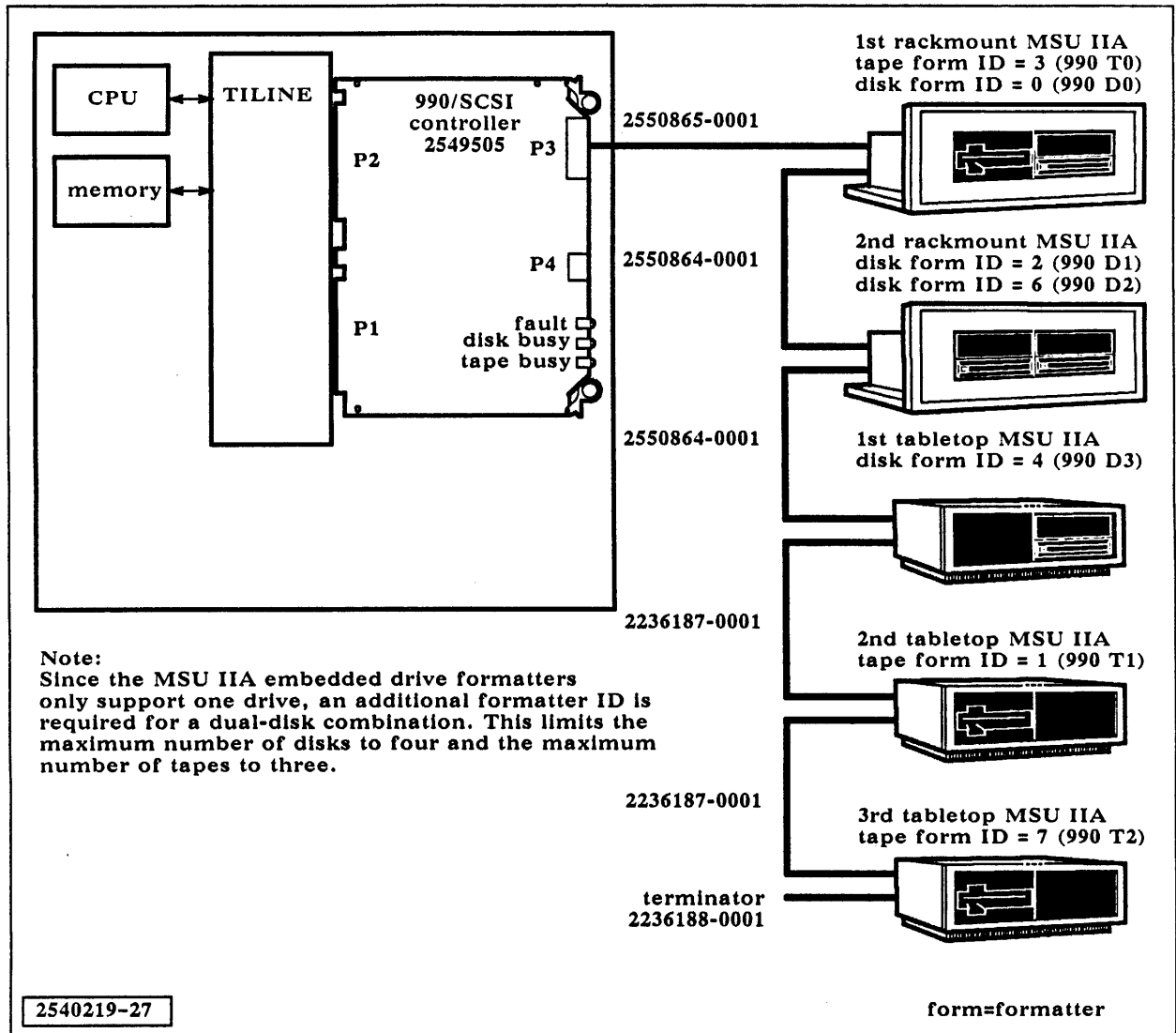
TILINE Interface   3.4   The TILINE is a 16-bit data transfer bus and associated control lines which serve to transfer data between all high-speed system elements. The TILINE is asynchronous, and therefore the speed of data transfers over the TILINE is determined by distance and the speed of the devices connected to it.

The TILINE interface connects at P1 and P2. Refer to Table 3-1 for pinout assignments and signal descriptions.

Looking at the assembly from the component side, with the 80 pin edge connectors toward the bottom, P1 is on the right and P2 is on the left. The even numbered pins are on the component side, with pin 2 leftmost and pin 80 rightmost. The odd numbered pins are on the conductor side of the printed wiring board. Refer to the board outline drawing (Figure 1-1).

The pinout for the SCSI connector, P3, is shown in Figure 3-3.

There are two classes of controllers which interface to the TILINE: TILINE master controllers, which control data transfers, and TILINE slave devices, which generate or accept data in response to some master. Data transfers in either direction always occur between one master and one slave. The system is configured so that at any given instant, only one master has control of the TILINE and only one slave recognizes any particular address. The 990/SCSI controller features both a master and a slave controller.

Commands are initiated by the operating system software writing to the appropriate 8-word TILINE peripheral control space (TPCS). One TPCS is provided for the disk channel and one for the tape channel. Once the idle bit of TPCS is cleared (word 7 write), the 990/SCSI controller begins execution. The TPCS words are numbered 0 through 7.

TILINE Data Path   3.4.1   The TD data bus and the BD register provide a TILINE data path for either the 68010 or the autonomous control. The BA register and the TA bus provide the address path.

TILINE Transfer Control   3.4.2   Control logic is implemented to control the TILINE slave or the TILINE Master data transfers. The major control elements are:

■ TILINE Master Cycle Control (TMX0Q, TMX1Q)

■ TILINE Master Control Chip (CSD2051)

■ Arbitration for TD (0-15) Bus Control (LOCKQ)

■ TILINE Slave Address Decode (ADROKD, ADROKT)

■ Slave Access To TPCS Control (TSC0Q, TSC1Q)

■ TILINE Interrupts (TLINTD, TLINTT)

CSD2051 TILINE Master Control Chip   3.4.3   The CSD2051 controls the TILINE Master cycle. It arbitrates for the TILINE busses, issues the TILINE go signal (TLGO), generates enables for data movement, and waits for a slave to respond with a termination signal (TLTM).

Figure 3-2 990//SCSI Controller Block Diagram

BD (0-15)

TILINE

TD<00-15>—

XCVR
LS640

TD<00-15>

ALS652
Q Q

SPD<0-15>
BDSPDEN

XFR
count
(4 X ALS569)

Aut.
XFR
control

BUFFULLQ
PBFULLQ
AONQ

TDTDEN-
TDTOTON-

BDTDEN-

CNT0-

SCSQ-

SWE-

SRE-

SCSI
33C93

SCSI I/F
P3

file

special

FOE-
LS240

SPDTOD

SPDTOD-

TPCSW0
TPCSW3

TPSC file
16 X 16
D   Q

FQ<0-15>-

(2 X ALS645)

SPDDEN-

16

8

D<0-7>

TSC0
TSC1

slave
control

TILINE
address
decode
ALS520

(switches)
TPCS
ADDR
SEL

D<0-15>

MC68010
10 MHZ

RWB-

ALS645

RWB

PTOSEN

ALS652
PKPEN

PPKCK

pack   unpack
Q
Q

SD<0-7>

F521

BA<00-19>
(5 X ALS561)

A<X,Y,Z>

A<0-19>

TD<00-19>—

XCVR
LS640

TA<00-19>

Q

PKFEEN
FPKECK

PKFOEN,FPKOCK,
PKWE-,PKRE-,
PBFODQ,PBFULLQ

TATAEN-
TATOTAN-

BATAEN-

A<5-19>

eprom
(27256)
A 64KB D

16

D<0-15>

monitor I/F
P4

RXD

DSR-

75189

RXDEIA

DSR

8

PD<0-7>

8

ALS574
PKFWC

8

ALS574
SDWDCK

5

LS244

ATOTA-
(tpcs file only)

A<7-19>

ram
(HM6264)
A 16KB D

16

D<0-15>

FIFO hold
PFI (0-7)

FIFO hold
SFI (0-7)

COMTX

75150

TXD

DTR

MEMER-,
TLGO-,
TLTM-,
TLWAIT,
TLREAD,
TLAGIN,
TLAGOUT

ARB

TLTO, TLMER,
ABE-, MDTR,
TIC-, SLGO,
SLRD

LOCKQ

DIRQ

DIRQ-

ALS574
DIRQ-

FDI<0-7>

ALS574
FSOC

PKWE-

PKRE-

SWE-

SRE-

R/W sync
and
source
mux

RE-

WE-

SCWEQ-

SCREQ-

TILINE
master
control
2051

DARCKQ-

buf/dtack
cntl

A<15-19>

MC68901
A   D

8

D<8-15>

RXD

FIFO hold
PFO (0-7)

FPKRC

8

FIFO hold
SFO (0-7)

FPKRC

FDO<0-7>

8

RE-,WE-
FE-
SCREQ-
SCWEQ-
FRQ-
RRDYQ
WRDYQ

FIFO
control
and
almost
counter

FRE-,FWE-
DEC,INC
FC<0-9>- (NC)
ALMOST,HALF
FEMTY,FFULL

TMXO
TMX1
BUFFLQ

CS901-

DSQ-

SSYNCQ

COMTX

clocks

20 MHZ
10 MHZ
5 MHZ
(SYNCQ)

local
decodes
F138

(5 MHZ)

FIFO
D   Q

FRQ-

RS-

FWE-

W-   FF-

(NC)

FRE-

R-   FE-

FE-

TILINE
ints.

TLINTD-
TLINTT-

STREO-
STRE1-
STRE2-

status
bits
ALS574, LS244

16

D<0-15>

LS390
clear (100ms)
min.

control
bits
ALS874

8

D<0-7>
CTWCK

D<0-7>
CTRE

2540219-8

Table 3-1 P1 and P2 Connector Pin Assignments

P1				P2			
01	GND	41	−12	01	GND	41	
02	GND	42	−12	02	GND	42	
03	+5	43		03	+5	43	TD06−
04	+5	44		04	+5	44	TA01−
05		45		05	TLAG(OUT)	45	TD07−
06		46		06	TLAG(IN)	46	
07		47		07	GND	47	TA06−
08		48		08	TA14−	48	
09		49		09	TA15−	49	TA07−
10		50		10	TA10−	50	
11	TLREAD	51		11	TA12−	51	TA02−
12	GND	52		12	TA11−	52	
13	TLPRES−	53		13		53	TA03−
14	TLIORES−	54		14		54	
15	GND	55	TLMER−	15	TA13−	55	TA00−
16	TLPFWP−	56		16		56	
17	GND	57		17	TA08−	57	TA04−
18		58	TLAV	18		58	
19	GND	59		19	TA09−	59	TA05−
20	TLTM−	60		20	TD11−	60	
21	GND	61		21	TD08−	61	TD04−
22		62		22		62	
23		63	TLWAIT−	23	TD10−	63	TD05−
24	GND	64		24		64	
25	TLGO−	65		25	TA18−	65	
26	GND	66	TLINTT−	26		66	TLINTD−
27	TD12−	67		27	TA17−	67	TD00−
28	TD13−	68		28		68	
29		69		29	TA16−	69	TD01−
30	TD14−	70		30		70	
31	TD15−	71	TLAK−	31	TA19−	71	
32		72	GND	32		72	
33		73		33	TD09−	73	
34		74	GND	34		74	
35		75		35	TD02−	75	
36		76		36		76	
37		77	+5	37	TD03−	77	+5
38		78	+5	38		78	+5
39	+12	79	GND	39		79	GND
40	+12	80	GND	40		80	GND

TILINE Interrupts 3.4.4 Separate disk and tape interrupts are implemented to signal the 990 host processor when the controller completes a requested operation.

Microprocessor

3.5 The 990/SCSI Controller processor features a 10 MHz 68010 microprocessor, 16K bytes of RAM, 64K bytes of EPROM, and a 5 Mhz 68901 multi-function peripheral chip (MFP).

Bus Structure 3.5.1 The MC68010 micro-processor features a 16-bit data bus and a 24-bit address bus. The microprocessor bus is an MC68010-type bus with separate address and data lines. Address lines A(X,Y,Z) & (00–19), combined with upper and lower data strobes, give an effective 24-bit address range. The address bus is driven by the the MC68010 address outputs whenever the MC68010 initiates a bus cycle.

A synchronous two-clock-wide DTACK is implemented. RAM, EPROM, control register, status reads, and autonomous register transfers run with zero wait states. Transfers to and from Pack/Unpack, the SCSI SD bus, the TILINE or the TPCS file cause the addressed control to generate a DTACK when the requested cycle is complete. Transfers to and from the 68901 are considered asynchronous. The 68901 generates its own DTACK for these transfers.

The data lines D(00–15) are driven by MC68010 when writing data, or by the selected read-data source when the 68010 reads data. Possible sources for read data are the following: MC68901, RAM, EPROM, the TILINE buffer, the SCSI pack buffer, the autonomous count register, the 33C93 data bus, the board status buffers, or feedback from the control register.

64K Byte EPROM 3.5.1.1 The EPROM is word wide (16 bits), 32K words deep, and features 150ns access times.

16K Byte RAM 3.5.1.2 The static RAM is word wide (16 bits) and 8K words deep. The RAM is byte addressable.

MC68901 MFP 3.5.1.3 The 68901 MFP connects to the 68010 via an asynchronous bus structure. The 68901 provides eight programmable I/O pins with interrupt capability, four timers, and 16-source interrupts with individual source enabling and masking. The 68901 also contains an asynchronous channel that connects a debug monitor (that resides in EPROM) to an external EIA terminal.

Autonomous Control 3.6 Autonomous control is provided to improve the SCSI/TILINE data transfer latency on the controller board. The time between the end of a TILINE transfer and the request for the next TILINE transfer can be one clock interval with the autonomous on and will be a minimum of one 68010 four-clock memory cycle when the 68010 is moving TILINE data.

The autonomous transfer uses hardware common to the 68010/pack buffer and the 68010/TILINE data transfer paths. Additional hardware to implement the autonomous transfer includes:

■ AONQ — Autonomous-on control bit

■ SPD — (0–15) data bus

■ BUFFLQ — The TILINE buffer is full flag

■ CNT0 — Autonomous count register and count equal zero decode

Pack/Unpack Buffer Register	**3.7** The purpose of the pack/unpack buffer is to translate the 16-bit TILINE, or 68010 data bus words, to the 8-bit (byte wide) SCSI controller (33C93) data bus width. The left byte (byte 0) is the first byte to or from the FIFO (storage medium).

Automatic Transfer Control times the 68010 transfer to or from the pack/ unpack buffer (PPD1Q), indicates when there is valid data in the buffer (PBFULLQ), and automatically unpacks or packs the buffer on the FIFO side (PBFODQ). The direction bit (DIRQ) in the control register is monitored to determine the direction of the data movement.

SCSI Data Transfer FIFO

3.8 A FIFO is implemented between the pack/unpack buffer and the 33C93 data bus. The purpose of the FIFO is to smooth the data flow since neither the TILINE nor SCSI data rate is likely to be constant. Eight bits of a nine-bit-wide communications FIFO implement a byte-wide FIFO.

Data movement into and out of the FIFO on the pack/unpack buffer side is automatic. Data movement is controlled by a buffer-full flag (PBFULLQ), the odd byte control (PBFODQ), the direction bit (DIRQ), and the full or empty (FFULL, FEMTY) status of the FIFO.

Data movement into and out of the FIFO on WD33C93 side is controlled by the 33C93 chip. The WD mode of the chip is used, and it issues read (SRE) or write (SWE) strobes as required to accomplish the SCSI data transfer.

SCSI Bus Controller

3.9 The SCSI bus controller subsystem is discussed under the following topics:

■ SCSI bus introduction

■ SCSI controller

■ System level considerations

SCSI Bus Introduction

3.9.1 The small computer system interface (SCSI) bus is a system-level data bus for communication between host computers and a variety of peripheral devices. SCSI is defined by American National Standards Institute (ANSI) standard X3.131-1986 which includes:

■ Electrical definition

■ Signal assignments (name, function)

■ Signal sequences, timing, and handshake requirements

■ Signal levels and drive current

■ Cable length, characteristics, and pin assignments

■ Communication protocol

    ■ Bus arbitration/deselect/reconnect

    ■ Initiator/target functions

    ■ Standard communication "phases"

■ Command set

    ■ Command definitions

    ■ Logical addressing

    ■ Fields for vendor-specific functions

The ANSI XT39.2 definition of SCSI is approximately 200 pages in length (single-spaced). System integrators and peripheral manufacturers are also working on a common command set (CCS) definition, which is a more practical subset of the SCSI commands. This definition is approximately 50 pages long. Thus, a complete SCSI description is beyond the scope of this document. Refer to the SCSI and CCS documents for additional detailed information.

The SCSI bus includes eight bidirectional, active-low data lines, a parity line, and nine control lines. The bus is connected as a daisy chain, with maximum allowable length of six meters for single-ended 48-mA drivers as provided by the 990/SCSI. The bus is terminated at both ends by 220/330-ohm split terminators from +5-volt Vcc to logic ground. A removable terminator connects to the far end of the bus. The 990/SCSI controller provides a fuse-protected and diode-isolated terminator power connection for both terminators.

CAUTION: Power cycling on any device attached to the SCSI bus may cause a SCSI bus reset, which aborts any I/O in progress on the bus.

Up to eight logical units may reside on an SCSI bus, each with its own ID. Although the SCSI definition allows a mix of independent host units and peripheral devices (seven peripheral devices for MSU IIA), 67x/87x mass storage is limited to a single host and one to eight peripherals. Each peripheral unit must include an SCSI port embedded in an intelligent formatter that makes conversions between the device-level signal interface and the SCSI bus.

Data transfers are byte wide with odd parity, and follow a request/acknowledge handshake protocol. In asynchronous operation, the handshake sequence accompanies each byte, and no other byte can be transmitted until the sequence is completed. This limits asynchronous speed to a maximum burst transfer rate of 1.5 megabytes per second (MB/s). This speed is dependent on bus propagation time between the sending and receiving units.

Synchronous operation and protocols are not supported by the 990/SCSI Controller.

SCSI Controller **3.9.2** The SCSI controller is built around the WD33C93 SCSI-bus interface controller (SBIC). This device incorporates all of the SCSI data and control signals (except SCSI bus reset) and includes 48-ma line drivers for the output signals. Discrete devices in the SCSI interface logic provide a separate driver for the SCSI bus reset line.

The SBIC is programmable via an 8-bit I/O bus that also serves as a data path to and from the SCSI FIFO. There are 28 SBIC internal registers that the MC68010 microprocessor may load with commands, operating parameters, and option control bits.

Upon completing the operation, the SBIC issues the SCSI microprocessor interrupt, SINTRQ. The MC68010 can then read any desired status or data from the SBIC internal registers.

The SBIC direct buffer access (DBA) mode is used for data read and write operations. In this mode, the SBIC serves as bus master for the SBIC I/O bus and controls data transfers between the SBIC and the read or write FIFO buffer.

In this case, the microprocessor is not involved except at the initiation and the completion of the data transfer. On the 990/SCSI Controller, the FIFO serves as the data transfer interface to the 68010 or the autonomous data transfer.

The third SBIC I/O mode, DMA mode, is not used by the 990/SCSI. DMA mode involves direct control of the SBIC by an external DMA Controller.

The SBIC offers asynchronous operation at a speed approximately 1.5 megabytes per second (sustained data rate). This rate is closely matched to the maximum TILINE transfer rate for the 990/SCSI controller.

Refer to Figure 3-3 for P3 connector pin out assignments. Note that the minus sign next to the signal indicates an active low signal. Refer to the board outline drawing (Figure 1-1) for additional information.

Figure 3-3   **P3 Connector Pinout**

looking into PWB male connector

conponent side ———→   ←——— conductor side

gnd	1	2	SDB0-
gnd	3	4	SDB1-
gnd	5	6	SDB2-
gnd	7	8	SDB3-
gnd	9	10	SDB4-
gnd	11	12	SDB5-
gnd	13	14	SDB6-
gnd	15	16	SDB7-
gnd	17	18	SCSIDBP-
gnd	19	20	gnd
gnd	21	22	gnd
gnd	23	24	gnd
	25	26	TERMPWR (+5V fused)
gnd	27	28	gnd
gnd	29	30	gnd
gnd	31	32	SATN-
gnd	33	34	gnd
gnd	35	36	SBSY-
gnd	37	38	SACK-
gnd	39	40	SCSIRST- (driven but not receivd)
gnd	41	42	SMSG
gnd	43	44	SSEL-
gnd	45	46	SCD-
gnd	47	48	SREQ-
gnd	49	50	SIO-

metal
shield

PWB

2540219-9

System Level Considerations

3.10 System level considerations of the SCSI bus controller subsystem are discussed in the following paragraphs:

■ SCSI formatter to TPCS unit number mapping

■ Booting considerations

■ Defect handling

■ Tape media transportability

■ Unload command

■ Overtemperature polling of disk formatters

■ End-of-tape considerations

■ Appending tape data

SCSI Formatter to TPCS Unit Number Mapping

3.10.1 Disk and tape control spaces provide addressing for up to 4 discrete devices or units in each space. This provides four disk units called D0, D1, D2, and D3 and four tape units called T0, T1, T2, and T3.

By SCSI conventions, SCSI logical units (LUNOS) are associated with specific formatter SCSI IDs. Up to eight SCSI IDs are available for SCSI bus addressing, with one being allocated for the host controller. Typically there will be one SCSI ID per formatter and one or more logical units associated with that formatter.

Table 3-2 describes the assumed TPCS unit to SCSI formatter unit mapping that will be supported by the 990/SCSI controller. Note that MSU II disk formatters can support one or two drives, while tape formatters and MSU IIA disk formatters support only one drive. MSU IIA disks are embedded SCSI drives and support only one disk per SCSI ID.

Formatter IDs for the disks and tapes must be assigned as indicated in Table 3-2 for proper operation.

TPCS mapping supports primary configurations of one disk drive and one tape drive or two disk drives. Secondary configuration options include additional tape and disk drives. Due to the enclosed mechanical locator plate, a disk-only MSU II can have a second disk added, but not a tape. A tape-only MSU II has a locator plate that allows a disk to be added, but not another tape.

MSU IIA locator plates support any disks/tapes combination.

Table 3-2

TPCS Unit to SCSI Formatter Mapping

SCSI ID (Formatter)	Formatter Unit to TPCS Unit DRIVE SEL 1 SCSI LUNO 0	DRIVE SEL 2 SCSI LUNO 1	Comments
0	DISK D0	N/A	Primary Disk Unit
1	TAPE T1	N/A	
2	DISK D1	DISK D2	SELECT Switch = off
2	DISK D1	N/A	SELECT Switch = on
3	TAPE T0	N/A	Primary Tape Unit
4	DISK D3	N/A	
5	N/A	N/A	990/SCSI Controller
6	TAPE T3	N/A	SELECT Switch = off
6	DISK D2	N/A	SELECT Switch = on
7	TAPE T2	N/A	

Comments:

1. SELECT SWITCH resides on 990/SCSI controller at location AH004, SW1. Default =on.
2. The 990 software maps TPCS units (0-3) to 990 logical units (1-4), etc.
3. For MSU IIA, disk D2 must be at ID 6.
4. For MSU IIA, SCSI LUNO 1 column is not applicable.
5. For MSU IIA, tape T3 not available.

Booting Considerations

3.10.2 The user should be aware that booting from devices on the 990/SCSI controller may take slightly longer than on previous 990 disk subsystems. This is because the controller must wait approximately 30 seconds for the devices to come on-line before accepting any commands.

Defect Handling

3.10.3 Since logical block addresses are used in SCSI peripherals, and the 990 host has used physical addressing for disks, the two philosophies had to be specially mated.

Defect mapping is one such area. The objective of the mass storage subsystem (controller plus MSU) is to provide the appearance of an error-free disk to the 990 host. This allows DX10/DNOS utilities such as DCOPY to be supported. To do this, the controller reserves certain areas on the disk (within a diagnostic cylinder) to keep a list of defective block addresses. Whenever a read or write error related to data or ID occurs, the controller updates this list with the logical block address. An entry in the list tracking the number of failure occurrences of the block is incremented. The list also contains header information needed for integrity information. This list will be referred to as the FMT map. The format of this list is defined in the disk software section explaining the >44 command.

Whenever a Format Disk command (>44) is received (with head=0 and cylinder=0), the controller will obtain the vendor defect map, the grown defect map (if applicable), and the FMT (format) map. For the FMT map, all blocks which have count values exceeding a predefined threshold level will be combined with the vendor and grown lists. The combined list of block addresses will be re-allocated (mapped out) by the target formatter. An "error-free" disk will result. During this operation, no other disks on the controller will be available for use.

One advantage to this approach is that for the initialize disk surface (IDS) utility, the user does not need to input a list of head/cylinder defects; the controller already has the list contained in the FMT list. If the user inputs a list, it will be ignored since the controller does not support the relocate command (>41), which is what the DNOS/DX10 device service routine (DSR) uses to map out the defects.

Users should consult the diagnostic documentation for information regarding utilities which allow modifications to the FMT list.

Tape Media Transportability

3.10.4 Data cannot be interchanged between cartridge tapes on 990/SCSI and WD800A or System 1000 tape units. However, System 1000 units may read 990/SCSI tapes, but programs must compensate for the header information contained within the data block.

A 990 OS level utility called TOTAR has been developed which executes on the 990. This utility uses the Write Physical Block command to write data on the 990/SCSI tape, without header information. This tape can then be read by standard System 1000 software.

Although the MSU will work with 550-oersted media (310-OE recommended), the WD800A will not perform reliably with 550-oersted media.

Unload Command

3.10.5 The DX10/DNOS Unload LUNO procedure will issue a unload command to the controller. This will retension the tape and position it at BOT. A media exchange is then necessary to use the retensioned tape.

Overtemperature Polling

3.10.6 The MSU II contains temperature monitoring circuitry designed to allow host systems to detect overtemperature conditions and warn the user.

In a 990 environment, this warning is handled in the following manner: The 990/SCSI controller will periodically poll each on-line MSU for an overtemperature indication. Polling will occur every 30 seconds to sequential disk formatters. (Tape formatters and MSU IIA do not support overtemperature sensing.) Therefore, if four on-line disks are present, each disk formatter will be polled once every two minutes.

If a disk formatter reports an overtemperature condition, then one of the following cases should apply:

If the system is not issuing commands to that particular MSU, then no message will be passed to the user. Unless a command is issued to the disk, the controller cannot send back an appropriate warning code in the TPCS command block.

If a command for the overheated disk formatter is completed without error, the 990/SCSI controller will set the retry bit and place an error code (D0, D1, D2, or D3) in word 2, and a SCSI sense key of 9 in word 3. By setting the retry bit, the TPCS register contents will then be placed into the system log.

If a command for the overheated disk formatter results in an error condition (such as ID error, block not found, etc.) then that error is reported. The overtemp warning is not reported until a command to the formatter is completed without error.

After warnings are returned to the system log, operations will continue normally. However, the user should locate the cause of the overheating and correct the situation before the thermal shutdown point is reached. If the temperature continues rising to the thermal shutdown point (approximately 44 degrees C) then the disk formatter will power itself down as described in the appropriate *MSU General Description* manual.

End-of-Tape Considerations

3.10.7 The current definition of the SCSI Standard for tape handling (particularly, in the implementations for streamers) contains an anomaly in the reporting of EOT status. Past 990 tape handling hardware was able to report EOT (early warning) on both reads and writes. On the SCSI side, this early warning only occurs on writes. Therefore, application software should perform proper EOF and/or trailer record writes before physical EOT is reached. This will allow a predictable scenario on future reads of this tape.

Archive and Cipher units differ slightly in their implementation details, as noted below:

Archive tape — Returns EW (early warning) on write operations (not reads) and once past EW, the unit will return EW on each and every write operation.

Cipher tape — Returns EW only on the first write operation; subsequent writes past EW will not report this warning.

It should also be noted that EW is mapped to EOT in Tape TPCS register 0. Once physical EOT is reached, OFFLINE and EOT status will be reported. See paragraph 3.17 for more details.

Appending Tape Data

3.10.8 Tape streamers can only append write data when heads are positioned over blank tape. In terms of the 990/SCSI tape, the following rules should be followed:

1. Read or Forward Space tape until COMMAND TIMEOUT status is received in Tape TPCS REG 0 bit 7.

2. Write tape — if normal completion then write is successful
   — if EOT and ONLINE then write is successful
   — if EOT and OFFLINE then write was unsuccessful

Remember that SCSI tape units (erase heads) will erase the tape when writes on track 0 are performed. Appended errors are reported by the 990/SCSI tape if a write command is issued with tape not at BOT, and not at a blank portion of tape. These appended errors should not be confused with reads of blank tape, although both errors are mapped to COMMAND TIMEOUT.

990/SCSI Programming

3.11 This paragraph contains information for programming assembly language routines that use the 990/SCSI controller. The programmer must be familiar with assembly language as described in the *Model 990 Computer 99/10 and 990/12 Assembly Language Reference Manual*.

Most users prefer Texas Instruments standard operating system software, including device service routines (DSRs). This software features standardized file manipulation schemes that are essentially independent of I/O device type. Users wanting this standard software can refer to the applicable operating system reference manual. Users wanting to perform direct disk I/O operations without using a standard operating system DSR can initiate disk commands and receive disk status as described in this section.

Additional information regarding the programming interface is discussed under the following paragraphs.

TILINE
Communication

3.11.1 The TILINE links the 990 processor, memory boards, and high-speed controllers, such as the 990/SCSI controller. The 990/SCSI controller is assigned two blocks of eight TILINE addresses. The 990 processor communicates with the 990/SCSI controller by writing 16-bit command words into one set of these eight TILINE address blocks. After a command completes, the 990/SCSI controller replaces the control words with status words that the 990 processor reads to determine command completion and device status. The 990/SCSI controller operations are initiated when control words containing command parameters are written into the TILINE addresses (slave registers) assigned to the 990/SCSI controller. After initialization, the 990/SCSI controller acts independently of the 990 processor and transfers data between specified TILINE memory locations and the formatter, as required. Any computer instruction that reads or modifies general memory can be used to communicate with the 990/SCSI controller slave registers. However, bit-oriented instructions should be used to control the interrupt mask in word 0.

TPCS
Addressing

3.11.2 The TILINE address range from >FFC00 to >FFDFF is reserved for the command and status communication blocks of TILINE peripheral controllers, such as the 990/SCSI controller. This range of addresses is called the TPCS and it is accessed by any TILINE master device that can generate addresses in this range. Model 990 computer logical byte addresses >F800 to >FBFE are mapped by the processor hardware to TILINE addresses in the range >FFC00 to >FFDFF, if the 990 processor is operating either unmapped or in map file 0. The TPCS is also addressed through alternate map files if the mapping bias value is chosen to yield a TPCS TILINE address. This programmable mapping feature is standard on some 990 CPUs and optional on others.

The physical TILINE bus includes 20 address lines; however, the CPU byte address consists of 16 bits. When a CPU map 0 byte address falls within the TPCS, all ones are loaded automatically into the upper five bits of the TILINE address, and the least significant bit (LSB) is dropped. (This LSB is a byte selector used only within the CPU.) The remaining 15 bits form the lower 15 bits of the TILINE address. Figure 3-4 shows the conversion of a 16-bit CPU byte address to a 20-bit TILINE word address. One way to visualize this conversion is to think of a 21-bit TILINE *byte* address of >1FF800 that loses its LSB (byte selector) to become TILINE *word* address >FFC00. The 1F comes from the five ones and the >F800 comes from the original CPU byte address. The only part of this map 0 address accessible to the programmer is the CPU byte address >F800.

Each of the two address blocks assigned to the 990/SCSI controller range from an independently switch-selectable base address to the base address plus seven word addresses. The consecutive words of each block starting from the base address are designated W0 through W7 in this document.

Each base address is selected by a dual in-line package (DIP) switch on the 990/SCSI controller board. Base address selection is coordinated with the operating system software during system hardware configuration and software system generation. Refer to paragraph 2.2.2 entitled Switch Setting for setting TPCS address switches.

The 990/SCSI controller is capable of communicating with TILINE memory in any range of the TILINE address space.

Figure 3-4 Relationship Between TILINE Address and CPU Byte Address

2540219-21
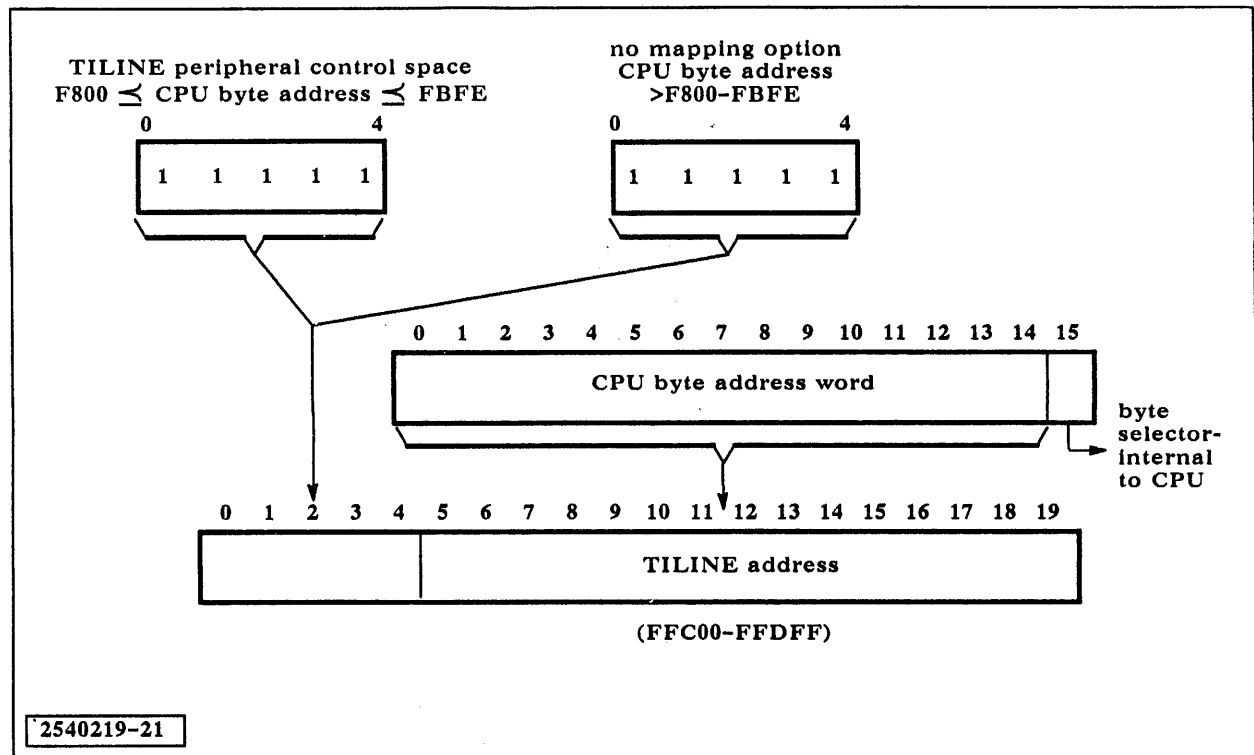
Command and Status

3.11.3 There are two independent sets of eight control and status words that the host CPU uses to communicate with the 990/SCSI controller for system operation. To initiate a system operation, the program loads control words into one of the two sets of control and status word registers assigned to the 990/SCSI controller. The order in which control words are loaded is not important except that word W7 must be last. Operation initiates immediately when bit 0 of W7 is set to zero.

Transmitting a new set of control words to the 990/SCSI controller erases the status words from the previous operation, except for the unit status fields of word W0 (bits 0 through 11) that the formatter or the 990/SCSI controller sets and that the host CPU cannot overwrite. If overwriting is attempted, the 990/SCSI controller ignores bits placed in the 990/SCSI controller registers.

If the host attempts to send a control word to a 990/SCSI controller slave set that is busy executing a command to the TILINE, the attempt appears to complete normally, but the contents of the addressed word do not change.

Disk TPCS Register Definitions

3.12 The control words shown in Figure 3-5 are implemented as TILINE peripheral space slave words and are used to control the TILINE/SCSI disk transfers. Bits and fields in these words specify the disk operation to the 990/SCSI controller and report command termination status to the host. These words will also be updated at command termination to reflect the final disk and TILINE transfer address and the final transfer counts. The bits and fields of the words are described in the following paragraphs.

Figure 3-5 Disk TPCS Registers

MSB															LSB
bit: 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
reg. 0 off line	not rdy	wrt prt	un- saf	end cyl	sk inc	ofs act	pak cng	attn 0	1	lines 2	3	attn 0	1	mask 2	3
1 extended com- mands	stb ear	stb lat	tfr inh	command				off set	off fwd	head address					
2 sectors/record								sector address							
SCSI error code															
selftest error code								completed/failed test #							
selftest: internal byte address															
cylinder								address							
3 SCSI sense key			EXT		cylinder address (LSBs)										
lp	con	selftest number						reserved							
4 data or record word count (data/format)															0
5 TILINE (men)								address (LSBs)							0
6 reserved 0s			unit 0	1	select 2	3		reserved 0s			TILINE (men) addr. (MSBs)				
7 idle	op cmp	err	int en	lo "0"	re try	ecc 'd	abn cmp	mem err	dat err	tl to	ld err	rte err	cmd to	sch err	unt err
bit: 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

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Control Word 0,
Disk Status

3.12.1 Bit 0 through 7 of word 0 contain individual status indicators from the selected disk drive (see word 6). Bits 8 – 11 correspond to the attention status of all the connected disk drives. Bits 12 – 15 enable a TILINE interrupt when a corrresponding attention bit (8 – 11) transitions on.

Bits 0 – 11 are set according to status, sense, and mode information returned from the formatter and may not be valid until after commands have been issued to the formatter. These bits are read-only to the host.

Bits 0 – 7 cause command abort when the command can not be executed because of the reported condition. Aborted commands cause word 7, bits 2 and 15 to set.

Bits 12 – 15 are controlled by the host.

Bit 0, Offline

3.12.1.1 When bit 0 is set, it indicates that the selected disk drive is not powered up, is not up to proper speed, or that an unsafe condition exists. This bit is also set after power on or after any reset.

Bit 1,
Not Ready

3.12.1.2 When bit 1 is set, it indicates that the selected disk drive is in the process of performing a seek, restore, or format operation, or the heads are not loaded, and the selected unit is not ready to read or write. This bit is also set after power on or after any reset.

The not ready to ready transition of this bit causes the attention bit in word 0 that corresponds to the selected drive to set.

Bit 2,
Write Protect

3.12.1.3 When this bit is set, it indicates that the selected drive is write protected.

Bit 3,
Unsafe

3.12.1.4 When bit 3 is set, it indicates that a fault exists that may destroy disk data if a disk write is allowed. A restore command will reset this bit if the unsafe condition no longer exists.

Bit 4, End
of Cylinder

3.12.1.5 When bit 4 is set, it indicates that the requested track number exceeds the tracks per cylinder parameter reported in the store registers command. This limit is derived from mode sense information previously reported by the formatter.

Bit 5, Seek
Incomplete

3.12.1.6 When bit 5 is set, it indicates that the selected disk drive did not complete a seek operation or a transfer beyond the last user cylinder that was requested. A restore command should be issued prior to issuing any following commands.

Bit 6,
Offset Active

3.12.1.7 When bit 6 is set, it indicates that the selected disk drive has its read/write heads offset from track center and write can not be allowed. This bit is effective during maintenance commands only.

Bit 7,
Pack Change

3.12.1.8 When bit 7 is set, it indicates that the selected disk drive may contain new media (power up, spin up, recabled, etc.).

A restore command will reset this bit.

Bits 8 – 11,
Attention Bits

3.12.1.9 When one or more of these bits (8 – 11) are set, it indicates that the corresponding disk drive(s) (0 – 3) are not seeking or restoring the heads to a new cylinder. When these bits transition on and the corresponding mask bit (12 – 15) is a one an interrupt will be sent to the TILINE if the 990/SCSI 990/SCSI Controller is (or becomes) idle.

These bits are set after power on or after any reset and are reset while the corresponding disk is executing either a seek or a restore command.

Bits 12 – 15,
Attention Mask

3.12.1.10 When one or more of these bits (12 – 15) are set, it indicates an interrupt will be sent to the TILINE when a corresponding attention bit sets (or is already set) indicating completion of a head movement operation. The interrupt will be active only while the 990/SCSI controller is idle and not actively executing a subsequent command.

The interrupt will be negated when the host writes a zero to the corresponding mask bit. Also initiating a read or write data command to disk, which causes the controller to go not idle, will negate the interrupt until the controller is again idle.

These bits are cleared after power on or after any reset.

Control Word 1, Command

3.12.2 Control word 1 contains fields that specify the command and the disk surface to the 990/SCSI controller. It also contains bits that can be used to enhance read error recovery or diagnostic effectiveness.

Bits 0, 1, and 5 – 7 of control word 1 specify the command to be executed by the 990/SCSI controller. Refer to paragraph 3.13 for additional information.

Bits 2, 3, 8, and 9 can be used to modify read commands to the formatter in an attempt to recover marginal read data. Bit 2 will cause the disk data to be sampled early. Bit 3 will cause the disk data to be sampled late. Bit 8 will cause the disk heads to be offset toward the spindle if bit 9 is set or away from the spindle if bit 9 is not set. These bits will be effective only for diagnostic commands. During normal operation, the formatter automatically uses these techniques if disk-read data errors occur.

Bit 4 is effective for read commands. When this bit is set, data will be read from the disk, but it will not be transferred to the TILINE address. Disk status can be checked to verify data integrity.

Bits 10 – 15 specify the head (disk surface) that will be used during command execution. If the specified surface is not valid, an end of cylinder status will be reported. The formatter remaps sectors to avoid media defects. There will be cases where the data will be mapped to a surface other than the one specified.

Control Word 2, Sector Address

3.12.3 Control word 2 contains fields that specify the number of sectors per data record and the starting sector address for the command to the 990/SCSI controller.

Bits 0 – 7 specify the number of sectors per data record. This parameter will be fixed at >01 for this 990/SCSI controller. If the specified word count (word 4) does not fill the last sector to be transferred, the 990/SCSI controller will dummy in the remaining words to or from the sector to enable storage or reading of the disk data and the associated check characters.

Bits 8 – 15 specify the starting sector address for a data-transfer command. If the specified sector is larger than the maximum sector address, a command timeout will be reported.

Control Word 2, SCSI Error Code

3.12.4 If the SCSI error code is all zeros, then no SCSI error information was obtained. If non-zero, it will represent the SCSI error code, extended or non-extended, depending upon the state of the EXT bit in word 3.

Control Word 2, Selftest Error Code, Internal Address Test Number

3.12.5 Refer to the section on maintenance commands for a description of these fields.

Control Word 3, Cylinder Address	**3.12.6** Control word 3 contains a field that specifies the starting cylinder address for the command to the 990/SCSI controller. Bits 0 – 15 specify the starting cylinder address. If the address is larger than the maximum cylinder, seek-incomplete status will be reported in control word 0, and command execution will be aborted.
Control Word 3, LP Bit, CON Bit, and Selftest Number	**3.12.7** Refer to the section on maintenance commands for a description of these fields.
Control Word 3, SCSI Sense Key, EXT, and Cylinder Address	**3.12.8** This field contains the cylinder address when the command is issued. In the case of an error, the EXT bit will be zero if the sense key (word 3) is invalid. In addition, the SCSI error code reported in word 2 will be the non-extended SCSI status. If the EXT bit is set to a one, the sense key (word 3) is valid, and the SCSI error code reported in word 2 will be the extended SCSI status.
Control Word 4, Word Count	**3.12.9** Control word 4 contains a field that specifies the number of 16-bit data words that will be transferred between the disk and host memory. Bits 0 – 14 specify the number of words that will be transferred during command execution. The format command will not use this field as ID (header) word 3 as it had in the past. For format commands, the disk formatter will select a value of 512 for sector size by default.
Control Word 5, Memory Address LSB	**3.12.10** Control word 5 contains one of two fields that specify the starting TILINE (host) memory address to be used during command execution. Bits 0 – 14 specify the least significant portion of the TILINE word address. The most significant portion is specified in word 6. If the initial address or an incremented address encountered during command execution is not available in the system, TILINE timeout will be reported (also see Word 6 description).
Control Word 6, Drive Select	**3.12.11** Control word 6 contains fields that specify the unit to be used and a portion of the TILINE word address to be used during command execution. Bits 4 – 7 specify the logical unit to be used during command execution. Only one unit 0 – 3 can be selected at any particular time. If more than one unit is selected, offline will be reported (also see word 0 description). Up to two logical units are supported by each disk formatter. This field will be cleared during power up processing. Bits 11 – 15 specify the most significant portion of the 20-bit TILINE word address. See word 5 for further details.
Control Word 7, Status and Control	**3.12.12** Word 7 contains control bits assigned to the 990/SCSI to the host, or to both. It also contains status bits used by the 990/SCSI controller to report command completion status to the host.

Word 7 is the last control word written by the host when a command is being initialized. Writing a 0 to bit 0 causes command execution to commence. The host may set bit 3 of word 7 at the same time to enable a command-complete interrupt, but all other bits must be cleared to 0 when bit 0 is cleared. The 990/SCSI Controller will set bit 0 and the appropriate status bits when command execution completes.

The content of word 7 should be checked for command completion status after each command terminates. Bit 3 is the only bit that can not contain 990/SCSI Controller-generated status at the end of a command execution.

The host may clear bit 3 or may start execution of another command to clear the command-complete interrupt. The attention interrupt generated by word 0 status is separate from the word 7 execution-complete interrupt. Command-completion status should be cleared however, before checking or clearing the attention interrupt.

When bit 0 is a 0, writing to any disk-control register is inhibited; for reads, all register data will be indeterminate except for bit 0 of word 7. Incorrect use of the control registers will not generate error status. The host must ensure serial (one command at a time) use of the control registers.

Bit 0, Idle   3.12.12.1 When bit 0 is set by the 990/SCSI controller, it indicates that the 990/SCSI controller has completed command execution. In some cases, such as if the previous command was a seek command, the drive may still be executing the command.

This bit is cleared to a 0 by the host to start execution of the operation defined by the control registers.

Interrupts to the host will be issued only while this bit is a one. If not cleared, the interrupt will again be issued when the controller returns to idle.

The 990/SCSI controller will be busy (bit 0 equal 0) after power on and after reset until self test and initialization are complete.

Bit 1, Operation Complete   3.12.12.2 When bit 1 is set by the 990/SCSI controller, it indicates that the previous command completed without errors. The host should reset this bit (during interrupt service) to indicate it has read 990/SCSI controller status.

Bit 2, 990/SCSI Controller or Device Error   3.12.12.3 When bit 2 is set by the 990/SCSI controller, it indicates that the previous command terminated with error indicators set. The host may read bits 5 – 15 in word 7 and bits 0 – 7 in word 0 to determine the reason for the error. Word 7, bits 5 – 15 may not be valid if bit 2 is not set. The host should reset this bit after it reads the 990/SCSI controller status.

Bit 3, Interrupt Enable   3.12.12.4 When bit 3 is set by the host, a command-complete interrupt will be sent to the host when command execution terminates. Clearing this bit will clear the command-complete interrupt. This bit is cleared after power on or any reset.

Bit 4, Old Lockout Bit   3.12.12.5 This bit was originally defined to control access to the peripheral space control words. This bit is no longer supported and should be cleared to 0 by the host.

Bit 5, Retry   3.12.12.6 When bit 5 is set by the 990/SCSI controller, it indicates that retries were used by the formatter during execution of the command.

Bit 6, ECC Used   **3.12.12.7** When bit 6 is set by the 990/SCSI controller, it indicates that an error-correcting process was used to recover data from the disk.

Conditions that cause the following bits to set will also cause bit 2 to set.

Bit 7, Abnormal   **3.12.12.8** When bit 7 is set by the 990/SCSI controller, it indicates that a
Completion   command was terminated due to a TILINE I/O reset or a power failure early warning pulse.

Bit 8, TILINE   **3.12.12.9** When bit 8 is set by the 990/SCSI controller, it indicates that a
Memory Error   TILINE memory data error was detected during a TILINE memory read operation. The TILINE data transfer will terminate, and the 990/SCSI controller will dummy in any remaining disk transfer so that disk ECC characters will be properly checked or generated for the data blocks.

Bit 9, Data Error   **3.12.12.10** When bit 9 is set by the 990/SCSI controller, it indicates that either a data record or a record header (ID) contains parity errors on the disk and cannot be recovered. The formatter will normally have retried the operation. Error correction will normally have been attempted on read errors. Bit 11 will also be reported for ID errors.

Bit 10, TILINE   **3.12.12.11** When bit 10 is set by the 990/SCSI controller, it indicates that
Timeout   the TILINE did not respond to the asserted address. The TILINE data transfer will terminate, and the 990/SCSI controller will dummy in the remaining disk transfer so that disk ECC characters will be properly checked or generated for the data blocks.

Bit 11, ID Error   **3.12.12.12** When bit 11 is set by the 990/SCSI controller, it indicates that the ID words for the requested sector could not be found. Either the track is not properly formatted, or an error exists in the header for the requested sector. If bit 9 is also set, it indicates that the ID was found but the check characters indicate an error present.

Bit 12, Rate Error   **3.12.12.13** When bit 12 is set by the 990/SCSI controller, it indicates that the TILINE transfer ran below the required disk rate.

Bit 13, Command   **3.12.12.14** When bit 13 is set by the 990/SCSI controller, it indicates that
Timeout   the formatter did not report completion status within an alloted time interval, or that illegal command parameters were sent to the formatters.

Bit 14,   **3.12.12.15** When bit 14 is set by the 990/SCSI controller, it indicates that
Search Error   a data sync character was not found in the data space on the sector after the desired sector was found.

Bit 15, Unit   **3.12.12.16** When bit 15 is set by the 990/SCSI controller, it indicates that
Error-Device   a drive error prevented the completion of the requested operation. Word 0 error status should be checked.

Disk Commands   **3.13** This paragraph contains information necessary for accessing the 990/SCSI controller and issuing commands to it. Disk-command codes are transmitted to the 990/SCSI controller via control TPCS register 1 associated with the disk space. Command encoding resides in five bits of this register, bits 0 & 1 form an extended field while bits 5 – 7 form the command field. Mapping of the extended bits provides command groupings of >0x, >4x, >8x, and >Cx; where x=0 – 7.

An overview of the disk related commands is shown in Table 3-3. For command opcodes not listed, the 990/SCSI controller will return command-complete status with the following status:

TPCS REG 0:   Bits 00–07 are set to 0.

TPCS REG 7:   Set to 1 — IDLE, ERROR, CMD TIMEOUT
Set to 0 — all remaining except for INT ENABLE
Unchanged — INT ENABLE

Table 3-3 Disk Command Summary Description

Code	990/SCSI Disk Command	Functional Description
>00	STORE REGISTERS	Returns Drive Related Parameters
>01	WRITE TRACK	Write specified pattern to Track
>02	READ DATA	Reads #Bytes @ Hd,Cyl,Sector
>03	WRITE DATA	Writes #Bytes @ Hd,Cyl,Sector
>04	READ ID	Returns Head and Cylinder Address
>05	WRITE DATA	Writes #Bytes @ Hd,Cyl,Sector
>06	SEEK	Seeks to specified Cylinder
>07	RESTORE	Resets to Head=0 & Cylinder=0
>40		
>41		
>42		
>43		
>44	FORMAT DISK	If Hd=0 & Cyl=0 then Formats Disk
>45		
>46		
>47		
>80	EXTRACT INTERLACE	Returns Disk Interlace Factor
>81	WRITE TRACK	Write Specified Pattern to Track
>82	READ DATA	Reads #Bytes @ Hd,Cyl,Sector
>83	WRITE DATA	Writes #Bytes @ Hd,Cyl,Sector
>84		
>85		
>86		
>87	MAINTENANCE/DIAGNOSTIC	Refer to Note 2
>C0		
>C1		
>C2		
>C3		
>C4		
>C5		
>C6		
>C7		

NOTES:

1. Commands left blank are unimplemented and will generate a "command timeout" error condition.

2. All commands except >87 with Reg 3, bit 1 set, will be inhibited following unsuccessful selftest. Refer to the section on Maintenance and Diagnostic Commands for more information.

Store Registers —
>00

3.13.1 The Store-registers command will accept as input the unit select field of register 6 and the TILINE buffer address in registers 5 & 6. It will obtain specific drive-related parameters for the specified unit and return them to the host memory at the specified address.

Upon receiving a Store-registers command, the 990/SCSI controller will return three words of data as defined in Figure 3-6. The returned data will apply only to the unit selected by the Store-registers command. The data returned are specified in Figure 3-7.

Figure 3-6   **Disk Store Registers Format**

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
words per track															
sectors per track								overhead per record							
track per cylinder					cylinders per drive										

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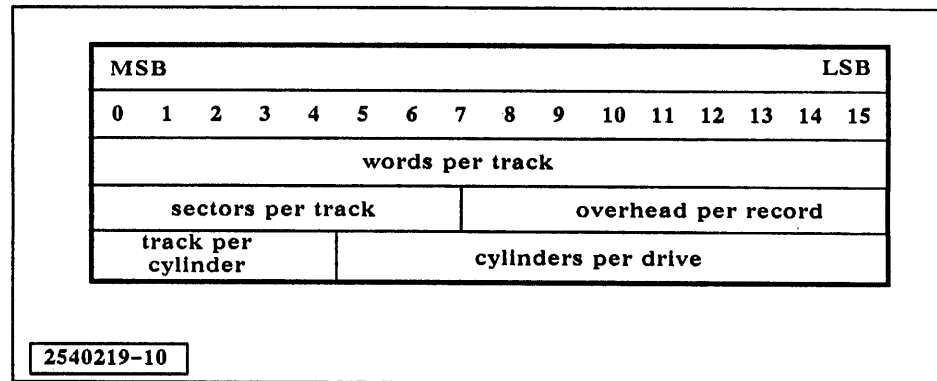
Figure 3-7   **Disk Store Registers Values**

peripheral	word	hex	dec	meaning
MSU II	0	>2400	9216	(36*512=18432 bytes/track)
	1	>2400	36,00	36 sectors/track, 0 overhead
	2	>4BBD	9,957	9 track/cyl, 957 cyl/drive
MSU IIA	0	>2400	9216	(36*512=18432 bytes/track)
	1	>2400	36,00	36 sectors/track, 0 overhead
	2	>7CB4	15,1204	15 track/cyl, 1204 cyl/drive

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Write Track —
>01 or >81

3.13.2 This command performs a write data operation to all bytes of all sectors on a specified disk track. The data pattern used is supplied from a TILINE memory location that is pointed to by the TILINE address in registers 5 and 6. The pattern written to disk is always a word (2 bytes).

The required inputs to this command are the unit select field of register 6, the head address field of register 1, the cylinder address field of register 3, and the TILINE address in registers 5 and 6. The sector address field of register 2 will be ignored on input.

Upon any error conditions, the sector address field of register 2 will reflect the failed sector, and the head/cylinder addresses will be unchanged. This command will be terminated on the first occurrence of any error.

Read Data —
>02 or >82

3.13.3   This command performs a seek, read data from disk, and data transfer to TILINE memory.

Required inputs to this command are head address of register 1, cylinder address of register 3, sector address of register 2, transfer count of register 4, unit select field of register 6, and TILINE address in register 5 and 6.

Execution of this command forces a seek to the specified cylinder and the selection of a head or surface, followed by a reading of data at the specified sector. The appropriate number of sectors are read and transferred to meet the required length specified in the transfer count. Automatic switching of head and cylinder location is handled by the hardware for sectors accessed across these boundaries. Data is transferred to TILINE memory starting at the location specified.

Upon completion, this command updates status and reflects the current head, cylinder, and sector address (last sector read). If an error occurs, then these fields reflect the failed disk sector, and the transfer count contains the number of remaining bytes not transferred to memory. In either case, the TILINE address reflects the incremented address of the byte transferred.

Write Data —
>03, >05, or >83

3.13.4   This command performs a seek and write data to disk from TILINE memory.

Required inputs to this command are head address of register 1, cylinder address of register 3, sector address of register 2, transfer count of register 4, unit-select field of register 6, and TILINE address in register 5 and 6.

Execution of this command forces a seek to the specified cylinder and the selection of a head or surface which is followed by writing of data at the specified sector. The appropriate number of sectors are written to satisfy the required length specified in the transfer count. Automatic switching of head and cylinder location is handled by the hardware for sectors accessed across these boundaries. Any residual bytes in a sector are zero filled. Data is transferred from TILINE memory starting at the location specified.

Upon completion, this command updates status and reflects the current head, cylinder, and sector address (last sector written). If an error occurs, the transfer count contains the number of remaining bytes not transferred to disk. In either case, the TILINE address reflects the incremented address of the last byte transferred.

Read ID
— >04

3.13.5   This command returns information to TILINE memory that reflects the current head and cylinder position of the selected disk unit.

The Read ID command will accept as input the unit-select field of register 6 and the TILINE buffer address in registers 5 and 6. It will obtain specific drive-related parameters at the specified unit and return them to the host memory at the specified address.

Returned parameters will be defined as follows:

WORD 0	BITS 00–04:	HEAD #
	BITS 05–15:	CYLINDER #
WORD 1	BITS 00–07:	# sectors per record (always = 1)
	BITS 08–15:	SECTOR #
WORD 2	BITS 00–15:	data words/record (either 128 or 256 words)

Seek
— >06

3.13.6 This command forces the specified disk unit to position its heads over a particular cylinder.

Required inputs to this command are the cylinder address of register 3 and the unit-select field of register 6.

Command completion status is immediately returned upon execution of this command so overlapped operations to other units can occur. The attention bit for a particular unit is reset while seeking, and the not-ready bit of register 0 is set. Upon completion of the seek, and if the controller is idle, a disk interrupt is generated while the attention-mask bit is set. The not-ready bit will be reset, and the attention bit will be set upon successful completion. Errors while seeking will generally reflect an incomplete or invalid seek condition.

Restore
— >07

3.13.7 This command forces the specified disk unit to position its heads over cylinder #0 and select head #0.

Required input to the command is the unit-select field of register 6.

Command completion status is immediately returned upon execution of this command so overlapped operations to other units can occur. The attention bit for a particular unit is reset while seeking, and the not-ready bit of register 0 is set. Upon completion of the restore, if controller is idle, a disk interrupt is generated while the attention-mask bit is set. The not-ready bit will be reset, and the attention bit will be set upon successful completion. Errors while restoring will generally reflect an incomplete or invalid restore condition.

Format Disk
— >44

3.13.8 This command allows the host to initiate a disk format-and-verify operation. The disk will appear to be defect free after the command successfully completes. The format operation takes place only when the head and cylinder addresses are equal to 0. All non-zero head and cylinder addresses will force an immediate return of command completion status.

The required inputs to this command are the unit-select field of register 6, the head address field of register 1, and the cylinder address field of register 3. The TILINE address in registers 5 and 6 point to a buffer used during the format-disk command. The byte count in register 4 contains the size of this TILINE buffer area. The definition of this buffer area is shown in Figure 3-8.

The sector address field of register 2 will be ignored on input.

Figure 3-8 Disk Format Command TILINE Buffer Definition

	MSB															LSB
bit:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
word 0	error threshold/fatal error code															
word 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SA	X
word 2	S.A. pattern															
word 3	progress code (output)															
word 4	words 4 thru X will be initialized to 0000 by format command															

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WORD 0 — The Error Threshold specifies the minimum number of times a
block must fail before it is considered a hard failure and is re-allocated. This
threshold applies to bad blocks logged prior to the format command as well as
those encountered during the format verification. An entry of 0000 will
default to a threshold of 2. If a fatal error occurs during the format, this word
will contain an error code indicating the problem in more detail. The codes
are defined in Table 3-4.

Table 3-4

Disk Format Command Extended Error Codes

Code	Definition
FF11	Unable to write defect backup map
FF12	Fatal SCSI format command completion status
FF13	Fatal SCSI status during verification
FF14	Defect list parameter error
FF15	Fatal SCSI error status during mode select
FF16	Mode select data parameter error
FF17	Format iteration count expired
FF18	Translate operation failure

WORD 1 — If bit 14 of word 1 is set, then the format command will write the
entire disk with the pattern specified in word 2 after a format-and-verify pass.
The disk will then be verified after the write operation. If any read errors or
retries are reported during the verify, the failure occurrence count is incre-
mented. The controller will then re-allocate the block. Up to 16 errors will be
re-allocated, after which a new format-disk operation will begin. Each verify-
reallocate/reformat sequence is referred to as a pass. Up to six passes will be
attempted to yield an "error-free" disk. If an error is experienced during the
sixth pass, an error code of FF17 will be returned in word 0.

If bit 14 is reset (0), then the disk will be verified using the formatter's default format pattern. No additional writing or reading will be done.

Bits 00 through 13 of word 1 are ignored by the controller.

WORD 2 — Word 2 contains the data pattern to be used in writing the disk, if Word 1, bit 14 is set.

WORD 3 — The progression code indicates what the format command is doing. It will be initialized to a 0000 upon format-command initiation and after the format command completes. It will be non-zero during the format command as defined in Table 3-5.

Table 3-5

Disk Format Command Progression Codes

Code	Definition
1	Reading defective blocks record
2	Reading vendor map
3	Converting block address
4	Formatting drive
5	Verifying disk
6	Writing surface analysis pattern

The disk slave registers will remain BUSY during the entire format and verify operation. Any tape operations will be allowed and will continue without interruption.

The 990/SCSI controller manages a list of defective blocks located on a diagnostic track. The track is located two cylinders past the last cylinder defined by the store-registers data, head 0. The list is 512 bytes long and begins on sector 0. It is replicated sequentially two times for a total of three identical lists. When a data related error or retry occurs during read and write operations, the 990/SCSI controller will log the block address of the defective block in this list along with the number of failure occurrences. The format command will read this record and re-allocate those defective blocks logged with a failure occurrence greater than or equal to the threshold specified in the TILINE buffer. The data format of this record is defined in Figure 3-9. The data in this list will be invalid after a format command until a new defect is logged, since the Format-disk command will reformat the diagnostic cylinders.

Figure 3-9   Defective Block Logging Record Data Format

```
                 byte
                 0-7  ┌─────────────────────────────────────┐
                      │        header "NEW_BLKS"             │
                 8    ├─────────────────────────────────────┤
                      │        defect list size MSB          │
                 9    ├─────────────────────────────────────┤
                      │        defect list size LSB          │
                 .    ├─────────────────────────────────────┤
                      │      defect 1 block address MSB      │
                 .    ├─────────────────────────────────────┤
                      │       defect 1 block address         │
                 .    ├─────────────────────────────────────┤
                      │       defect 1 block address         │
                 .    ├─────────────────────────────────────┤
                      │      defect 1 block address LSB      │
                 .    ├─────────────────────────────────────┤
                      │                00                    │
                 .    ├─────────────────────────────────────┤
                      │                00                    │
                 .    ├─────────────────────────────────────┤
                      │    defect 1 failure occurence MSB    │
                 .    ├─────────────────────────────────────┤
                      │    defect 1 failure occurence LSB    │
                 .    ├─────────────────────────────────────┤
                      │      defect 2 block address MSB      │
                 .    ├─────────────────────────────────────┤
                      │               ect...                 │
                 .    ├─────────────────────────────────────┤
                      │        Nth defect (62 max)           │
                 .    ├─────────────────────────────────────┤
                      │             list CRC                 │
                      └─────────────────────────────────────┘

       2540219-13
```
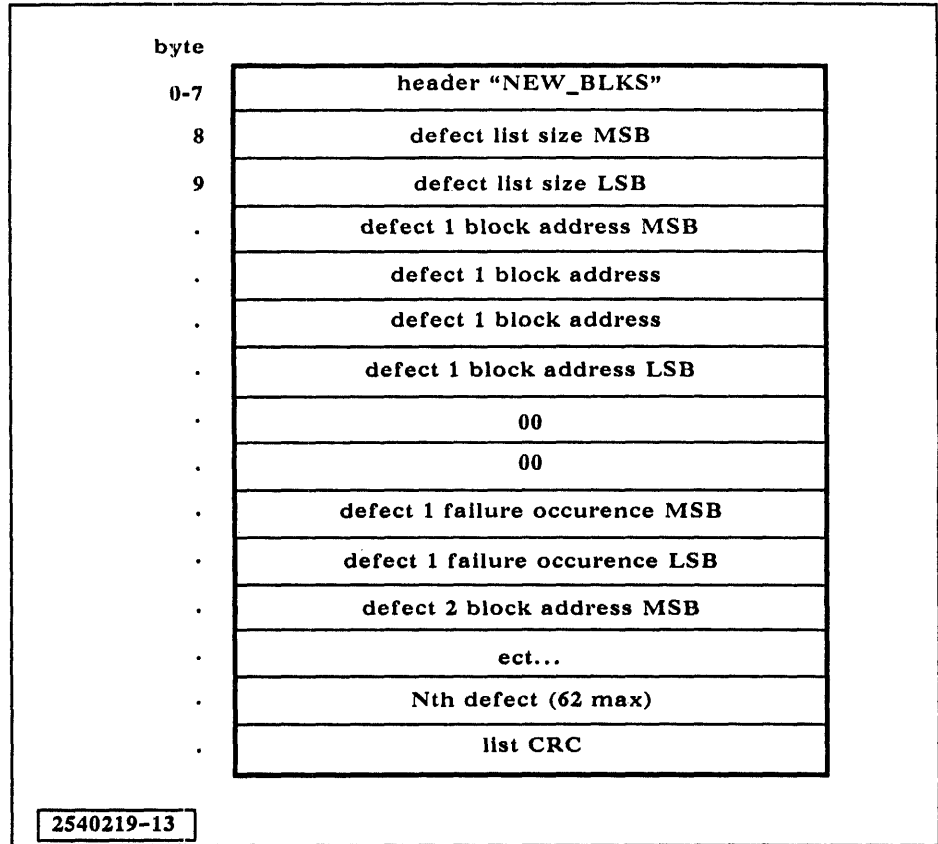
Bytes 8 and 9 are the defect list size. This size value does not include bytes 0 through 7 (the header), bytes 8-9 (the size), or the cyclic redundacy check (CRC) byte.

The CRC value is calculated by starting with a 16-bit word of all 1s. Each word of the list is xor'ed to the previous CRC value then rotated left one position. The calculated value is then appended after the last entry in the list.

Extract Interlace — >80   3.13.9 This command returns the disk interlace factor for the specified unit to TILINE memory. The data returned will always be one word in length.

Required input to the command is the unit-select field of register 6 and the TILINE address registers 5 and 6.

Maintenance/ Diagnostic Commands — >87   3.13.10 This operation allows execution of specific self-test routines as well as special device unique commands. Refer to the section on Disk Maintenance Commands for further details.

Tape TPCS Register Definitions

3.14 The control words shown in Figure 3-10 are implemented as TILINE peripheral space slave words and are used to control the TILINE/SCSI data transfers. Bits and fields in these words specify the tape operation to the controller and report command termination status to the host. These words will also be updated at command termination to reflect the final tape and TILINE count, address, and status to the host. The bits and fields of the words are described in the following paragraphs.

Figure 3-10 Tape TPCS Registers

bit:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
reg. 0	off line	bot	eor	eof	eot	wrt pro	rw	cmd to	rewind bits 0	1	2	3	rewind mask 0	1	2	3
1	read overflow status count (lsb's)															
2	SCSI error code								SCSI sense key				EXT			
	selftest error code								selftest: test # performed							
	selftest: internal byte address															
	read offset															
3	lp	con	maintenance command						reserved							
4	character count/record count															
5	TILINE address (lsb's)															0
6	unit 0	1	select 2	3	command				0	0	0	TILINE address (msb's)			
7	idle	op cmp	err	int en	lo "0"	ST REG	tap fmt	abn cmp	raw err	cor err	dat err	mem err	tim err	TL to	fmt err	tap err
bit:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

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Control Word 0, Tape Status

3.14.1 Bit 0 through 7 of word 0 report individual status indicators from the selected tape drive (see word 6). Bits 8 – 11 correspond to the rewind status of all the connected tape drives. Bits 12 – 15 enable a TILINE interrupt when a corresponding rewind bit (8 – 11) transitions off.

Bits 0 – 11 are set according to status, sense, and mode information returned from the formatter and may not be valid until after commands have been issued to the formatter. These bits are read only to the host.

Bits 0 – 7 are reported for each command and also cause command-abort status to be reported if the condition prevented the command from being executed. Bits 0 or 6 also cause the command Read Transport Status to report abort status.

Commands aborted because of conditions that set these bits cause word 7, bits 2 and 15 to set.

Bits 12 – 15 are controlled by the host.

Bit 0, Offline 3.14.1.1 When bit 0 is set, it indicates that the selected tape drive is not ready, and a rewind is not in progress. This bit is set after power on or any reset.

Bit 1, Beginning of Tape 3.14.1.2 When bit 1 is set, it indicates that the media in the selected tape drive is loaded to the beginning of the first track.

Bit 2, End of Record 3.14.1.3 When bit 2 is set, it indicates that a Read command requested a data record, and either erased media was found, or the logical end of data was sensed before the transfer count reached zero.

Bit 3, End of File 3.14.1.4 When bit 3 is set, it indicates that a Read command or a Record skip command encountered an end of file mark. Abort status will be reported.

Bit 4, End of Tape 4.14.1.5 When bit 4 is set, it indicates that the early end of media mark was detected during a write command. In the case of a write, the data transfer will complete, and the cache buffer will be flushed to tape. If a command continues to the physical end-of-tape mark, abort status will be reported. Physical end of tape detected during a Record-skip-forward command causes abort status to be reported.

Bit 5, Write Protected 3.14.1.6 When bit 5 is set, it indicates that a Write command or an Erase command detected media write-protected status. Write protect error causes abort status to be reported.

Bit 6, Rewinding 3.14.1.7 When bit 6 is set, it indicates that a command was issued while the media was rewinding. Abort status will be reported.

Bit 7, Command Timeout 3.14.1.8 When bit 7 is set, it indicates that the selected tape drive failed to respond within a 990/SCSI controller selected time out period. Abort status will be reported.

Bit 8 – 11, Rewind Bits 3.14.1.9 When one or more of bits 8 – 11 are set, it indicates that the corresponding tape drive is rewinding. This is not an error condition. When a bit transitions off, and the corresponding mask bit (12 – 15) is a one, an interrupt will be sent to the TILINE if the 990/SCSI controller is idle (or becomes idle). These bits are set after any reset.

Bit 12 – 15, Rewind Mask Bits 3.14.1.10 When one or more of these bits (12 – 15) are set, it indicates that an interrupt will sent to the TILINE when a corresponding rewind bit resets (or is already reset) indicating the completion of a rewind operation. The interrupt will only be active while the 990/SCSI controller is idle and not actively executing a subsequent command.

The interrupt will be cleared when the host writes a zero to the corresponding mask bit. Also, initiating a read or write data command to tape, which causes the controller to go not idle, will negate the interrupt until the controller is again idle.

These bits are cleared after power on or after any reset.

Control Word 1, Read Overflow Count

3.14.2 Control word 1 contains one field used by the 990/SCSI controller to report completion status.

Bits 0 – 15 are set at command completion to indicate the number of characters in the record beyond the last character sent to TILINE memory.

Control Word 2, Read Overflow Count

3.14.3 Word 2 contains a field that could be used by the 990/SCSI controller to report read-completion status.

Bits 0 – 7 have in the past been used to report the most significant bits of a 24-bit read overflow count (see word 1). These bits will not be supported since a maximum-length character count will be $((2*16)-1)$, or decimal 65535.

Control Word 2, Self-test Status and Internal Address

3.14.4 Refer to the section on maintenance commands for a description of the self-test status and internal address fields.

Control Word 2, SCSI Error Code, Sense Key, and EXT Bit

3.14.5 This field is valid when word 7, bit 2 is set to a one, or when SCSI status has been mapped to a non-fatal status such as a retry. In some cases, a tape error may not result in a valid SCSI error code. For these cases, the SCSI error code and sense key will be all zeros.

The EXT bit (bit 12) is set to 1 whenever an extended SCSI error code is to be reported with a valid sense key. If EXT=0, then an invalid sense key is reported in word 2. However, the error code will be a valid, non-extended SCSI error code.

Control Word 3, Read Offset

3.14.6 Word 3 contains a field that specifies a read offset character count to the 990/SCSI controller.

Bits 0 – 15 specify the number of characters to read from the record (skip) before starting to transfer characters (words) to TILINE memory. The complete record will be read so that CRC characters can be verified.

Control Word 3, Self-test Number, LP, and Con Bits

3.14.7 Refer to the section on maintenance commands for a description of the LP bit, self-test number, and CON bits.

Control Word 4, Character/Record Count

3.14.8 Word 4 contains a field that specifies the number of characters to transfer to or from tape or the number of tape records to skip.

Bits 0 – 15 specify the number of characters to transfer to or from tape for write or read data commands. If the combination of offset and character count would result in an odd number of bytes transferred to the TILINE, either the next sequential byte from tape, if present, or an all zeros byte will be used to fill (right byte) the TILINE word. If the command is a Record-skip command, bits 0 – 15 specify the number of records to skip.

Word 4 has in the past supplied a record skip reverse count or an erase length character count to the Skip-reverse or Erase commands respectively. Skip reverse and variable length erase are not supported by the 990/SCSI controller. This word may be used for a file count for the File-skip command.

Control Word 5,
TILINE
Address LSB

3.14.9 Control word 5 contains one of two fields that specify the starting TILINE (host) memory address to be used during command execution.

Bits 0 – 14 specify the least significant portion of the TILINE word address. The most significant portion is specified in word 6. If the initial address or an incremented address encountered during command execution is not available in the system, TILINE timeout will be reported (also see word 6 description).

Control Word 6,
Unit/Command/
Address

3.14.10 Control word 6 contains a field that specifies the command to be used. Word 6 also specifies the logical unit and a portion of the TILINE word address to be used during command execution.

Bits 0 – 3 specify the logical unit to be used during command execution. Only one unit, 0 – 3, can be selected at any particular time. If more than one unit is selected, the leftmost unit-select bit will be honored. One logical unit is supported by each tape formatter. This field will be cleared during power-up processing.

Bits 11 – 15 specify the most significant portion of the 20-bit TILINE word address. See word 5 for further detail.

Bits 4 – 7 specify the command to be executed by the 990/SCSI controller. See Table 3–6, entitled Tape Command Summary, for a list of supported commands.

Control Word 7,
Status and Control

3.14.11 Word 7 contains control bits assigned to the host, to the 990/SCSI controller or to both. It also contains status bits used by the controller to report command-completion status to the host.

Word 7 is the last control word written by the host when a command is being initialized. Writing a 0 to bit 0 causes command execution to commence. The host may set bit 3 of word 7 to enable a command-complete interrupt, but all other bits must be cleared to zero when bit 0 is cleared. The 990/SCSI controller will set bit 0 and the appropriate status bits when command execution completes.

The contents of word 7 should be checked for command-completion status after each command terminates. Bit 3 is the only bit that cannot contain 990/SCSI controller-generated status at the end of a command execution.

The host may clear bit 3 or may start execution of another command to clear the command-complete interrupt. The attention interrupt generated by word 0 status is separate from the word 7 execution-complete interrupt. Command-completion status should be cleared, however, before checking or clearing the attention interrupt.

When bit 0 is a zero, writing to any tape-control register is inhibited. For reads, all register data will be indeterminate except for bit 0 of word 7. Incorrect use of the control registers will not generate error status. The host must ensure serial (one at a time) use of the control registers.

Bit 0, Idle   3.14.11.1 When bit 0 is set by the 990/SCSI controller it indicates that the controller has completed command execution. In some cases, such as if the previous command was a rewind command, the drive may still be executing the command.

This bit is cleared to a zero by the host to start execution of the operation defined by the eight control registers.

Interrupts to the host will be issued only while this bit is a 1. If not cleared, the interrupt will again be issued when the controller returns to idle.

The 990/SCSI controller will be busy (bit 0 equals 0) after power on and after reset until self test and initialization are complete.

Bit 1, Complete   3.14.11.2 When bit 1 is set by the 990/SCSI controller, it indicates that the previous command completed without errors. This host should reset this bit (during interrupt service) to indicate it has read 990/SCSI controller status.

Bit 2, Error   3.14.11.3 When bit 2 is set by the 990/SCSI controller, it indicates that the previous command completed with error indicates set. The host may read bits 7–15 in words 7 and bits 0–7 in word 0 to determine the reason for the error. Bits 7–15 of word 7 may not be valid if bit 2 is not set. The host should reset this bit after it reads 990/SCSI controller status.

Bit 3,   3.14.11.4 When bit 3 is set by the host, a command complete interrupt will
Interrupt Enable   be sent to the host when command execution terminates. Clearing this bit will clear the command-complete interrupt. This bit is cleared after power on or any reset.

Bit 4, Lock Out   3.14.11.5 This bit was originally defined to control access to the peripheral space control words. This bit is no longer supported and should be cleared to 0 by the host.

Bit 5, Store   3.14.11.6 Bit 5 should be set to 0 by the host when initiating a command.
Register Support   When set to 1 by the controller, this bit indicates that the tape Store Registers command (a maintenance command) is supported.

Bit 6, Tape Type   3.14.11.7 Bit 6 is set by the 990/SCSI controller to indicate that the transport is either a cartridge or a phase-encoded type transport. This bit will be set by the 990/SCSI controller after power on, after any reset, or at command completion time.

Conditions that cause the following bits to set will also cause bit 2 to set.

Bit 7, Abnormal   3.14.11.8 When bit 7 is set by the 990/SCSI controller it indicates that a
Completion   command was terminated due to a TILINE I/O reset or a power failure early warning pulse.

Bit 8, Read After Write Error

3.14.11.9 When bit 8 is set by the 990/SCSI controller it indicates that the maximum number of retries was used during a Write command. The data on the tape is likely not correct.

Bit 9, Correctable Error

3.14.11.10 When bit 9 is set by the 990/SCSI controller, it indicates that retries were used to affect a successful tape operation.

Bit 10, Data Error

3.14.11.11 When bit 10 is set by the 990/SCSI controller, it indicates that a Read-data or Write-file-mark command detected bad data on the tape. Retries were not successful.

Bit 11, TILINE Memory Error

3.14.11.12 When bit 11 is set by the 990/SCSI controller it indicates that a TILINE memory data error was detected during the TILINE read operation. The TILINE data transfer will terminate and the 990/SCSI controller will dummy in the remaining tape transfer so that tape position is maintained.

Bit 12, Rate Error

3.14.11.13 When bit 12 is set by the 990/SCSI controller, it indicates that the TILINE transfers underran the required tape transfer rate.

Bit 13, TILINE Timeout Error

3.14.11.14 When bit 13 is set by the 990/SCSI controller, it indicates that the TILINE did not respond to the asserted address. The TILINE data transfer will terminate and the 990/SCSI controller will dummy in the remaining tape transfer so that tape position is maintained.

Bit 14, Format Error

3.14.11.15 When bit 14 is set by the 990/SCSI controller, it indicates that a block of data was not found on the tape during a read or a tape positioning operation. This bit may also indicate that the media was not positioned properly to honor the requested command.

Bit 15, Tape Error

3.14.11.16 When bit 15 is set by the 990/SCSI controller, it indicates that word 0 should be checked for error status, since a transport error has occured.

Tape Commands

3.15 Tape command codes are transmitted to the 990/SCSI controller via control-space register 6 associated with the tape TPCS. Command encoding resides in bits 4 through 7 of this register, giving opcodes of >0 through >F.

An overview of the tape-related commands is shown in Table 3-6. For commands opcodes listed as NOP, the 990/SCSI controller will return command-complete status with the following status (except for the rewind/offline condition noted as follows):

TPCS REG 0: Bits 00–07 updated to reflect current status

TPCS REG 7: SET to 1 — IDLE, OP COMPLETE
SET to 0 — all remaining except for INT ENABLE
UNCHANGED — INT ENABLE

However, if the tape is offline or rewinding when either a NOP or Read-transport-status command is received (>00,>03,>08,>09), then the tape-error bit (word 7, bit 15) will be set, and either the offline (word 0,bit 0) or rewind bit (word 0, bit 6) will be set.

Table 3-6 Tape Command Summary

Code	990/SCSI Disk Command	Functional Description
>00	NOP	Performs NOP
>01	(SYNC)	Performs NOP
>02	WRITE END-OF-FILE	Writes 1 Block of File Marks on Tape
>03	(RECORD SKIP REVERSE)	Performs non-overlapped Rewind
>04	READ LOGICAL RECORD	Reads Logical Record in Fwd Direction
>05	RECORD SKIP FORWARD	Skips Specified # of Records on Tape
>06	WRITE LOGICAL RECORD	Write Logical Record in Fwd Direction
>07	(ERASE)	If BOT, Erase Entire Media; Else NOP
>08	READ TRANSPORT STATUS	Allows Status Update For Selected Unit
>09	READ TRANSPORT STATUS	Allows Status Update For Selected Unit
>0A	REWIND	Forces Tape to BOT
>0B	UNLOAD	Performs Retension, Leaves Tape at BOT
>0C	(WRITE PHYSICAL BLOCKS)	Writes one or More Blocks to Tape
>0D	(READ PHYSICAL BLOCKS)	Reads one or More Blocks From Tape
>0E	(FILE/RECORD POSITION)	Performs NOP
>0F	MAINTENANCE COMMAND	Perform Specified MAINT/DIAG Command

NOTES:

1. Commands in ( ) represent new or redefined commands that are specific to 990/SCSI tape functions.

2. All commands except >0F with Reg 3, bit 1 set, will be inhibited following unsuccessful self test. Refer to the section on Maintenance and Diagnostic Commands for more information.

NOP — >00 or >01

3.15.1 The NOP command does not execute any tape operations, but it does update status information about the selected unit.

Required input to this command is the unit-select field of register 6. Returned status will reside in control-space registers 0 and 7.

Write End-of-File — >02

3.15.2 This command allows the host to write a file mark indication to tape. EOF indications will consist of 1 physical block (512 bytes) of file mark patterns. Execution of this command also implies a flush of the internal cache buffer on tape formatters.

Required input to this command is the unit-select field of register 6. Returned status will reside in control-space registers 0 and 7.

Read Logical Record — >04

3.15.3 This command allows one logical record to be read from tape and transferred to TILINE memory at the specified address. Logical records may be up to 65,535 bytes long.

Required inputs to this command are the unit-select field of register 6, the transfer count in register 4, the read-offset count in register 3, and the TILINE destination address in registers 5 and 6.

Execution of this command forces a tape-block read at the current position to obtain header information. The logical record length for this record is extracted from the header and is used in conjunction with the read-offset count to compute where the actual data for the transfer resides in the record. Data is then transferred to TILINE memory at the specified address until either an EOR is encountered or the transfer count is exhausted. The remaining number of data bytes in the record is reflected in the returned read-overflow count of register 1.

Completion of this command leaves the tape positioned at the next logical record. The transfer count will reflect how many bytes remain to be transferred. The TILINE address will contain the incremented value of the last byte sent. On a read of short records, where requested bytes are greater than the logical record length, the read terminates at the next logical record boundary.

Error conditions from this read operation are:

■   If header verification fails, the command will be aborted with a format error and the tape will be left positioned at the next physical tape block (which may not be on a logical boundary).

■   If blank media is encountered, the command reports command timeout.

■   If the transfer count does not reach zero when the logical EOR is encountered, the operation reports EOR status. Or if an EOF mark is detected, EOF status is reported. Tape error is also set.

■   If the tape runs out, the operation reports EOT status and tape error.

Record Skip Forward — >05

3.15.4   This command allows the host to skip forward a specified number of logical records.

Required inputs to this command are the unit-select field of register 6 and the record-skip count in register 4. The record-skip count is an unsigned integer, with a value of 0 meaning 65,535.

Execution of this command continues until either the skip count is exhausted or some condition such as EOF, EOT, or EOM is detected. In the case of EOF detection, the tape will be left positioned at the first logical record (1st physical block) past the EOF mark.

As a special case, if the skip count is zero, the controller will position the tape at the first EOF it encounters. This permits faster file skipping.

Write Logical Record — >06

3.15.5   This command allows one logical record to be transferred from TILINE memory at the specified address and written to tape. Logical records may be up to 65,535 bytes long.

Required inputs to this command are the unit-select field of register 6, the transfer count in register 4, and the TILINE source address in registers 5 and 6. The transfer count will be used as the logical record length in the header information.

Execution of this command forces a tape write of one or more physical blocks that make up the logical record. Header information is compiled and placed in the first physical block, and the bytes transferred from TILINE memory make up the data portion of the record. Residual portions of the last physical block will be zero filled.

Upon command completion, the transfer count will reflect the number of remaining bytes to transfer, and the TILINE address will be the incremented byte address of the last byte sent. Error status will be reported in registers 0 and 7 of the control space.

Overwriting of records, even though the logical record length is the same, cannot be used for tape record modification since downstream records/blocks will be corrupted by tape streaming characteristics.

Erase Tape — >07

3.15.6 This command forces an erase of the entire tape media if it was positioned at BOT, otherwise it returns completed status. After an erasure, the tape will be at the load point or BOT. Required input to this command is the unit-select field of register 6.

Read Transport Status — >08 or >09

3.15.7 This command allows status update for the selected unit. Status information about the unit will be returned in TPCS register 0. Other than returning status, this command does not affect the addressed unit.

Rewind — >0A

3.15.8 This command forces the tape to be positioned at BOT or load point.

Execution of this command will immediately return Command Complete so overlapped rewind operations to other units can occur. The rewind bit of register 0 will be set to reflect a rewind in progress, and the rewind-attention bit (8,9,10, or 11) will be set. Upon completion of the rewind operation, and if the controller is idle, a tape interrupt will be asserted when the attention-mask bit (12,13,14, or 15) is set, and the rewind attention goes to a 0. At this point, the rewind-in-progress bit will also be reset.

Unload — >0B

3.15.9 This command forces a tape-retension pass to be performed on the tape media before completing the unload. The tape is left positioned at BOT. Required input to this command is the unit-select field of register 6.

Execution of this command forces rewind status to be reported in register 0. Upon completion, rewind status is cleared, and offline status is set. The not-safe LED is also turned off at command completion.

Until the media is changed, tape operations to that drive will report offline status and tape error (EMULEX/Cipher only). However, the read-transport status/NOP will still report the drive formatter to be online.

Write Physical Block — >0C

3.15.10 This command forces tape writes to occur that deal in physical tape blocks only. No header information is supplied by the controller. Physical tape blocks contain a fixed length of 512 bytes.

Required inputs to this command are the unit-select field of register 6, the transfer count in register 4, and the TILINE source address in registers 5 and 6. The transfer count will be used as the required data-byte transfer length.

An integral number of physical blocks will always be written, and any residual data will be padded with zeros.

If header compatibility is to be maintained, it is the responsibility of the user to handle it properly. Therefore, if future file and record skipping and normal reads & writes of logical records are required, the user must adhere to the proper protocol. These compatibility considerations also include proper EOF blocks that separate sequential files.

Error and status reporting will be as in normal write data.

Read Physical Block — >0D

3.15.11 This command forces tape reads to occur that deal in physical tape blocks. Physical tape blocks contain a fixed length of 512 bytes. This command is the inverse of the Write-physical-block command.

Required inputs to this command are the unit-select field of register 6, the transfer count in register 4, and the TILINE destination address in registers 5 and 6. The transfer count will be used as the required data-byte transfer length.

The execution of this command will force an integral number of blocks to read from the tape, and then transfer count bytes will be written to TILINE memory. Residual portions of the last physical block will be discarded.

The read-offset and read-overflow registers are not used in the execution of this command. Transfer-count and TILINE-address registers will reflect proper status as in normal reads.

Maintenance/ Diagnostic Commands — >0F

3.15.12 This operation allows execution of specific self-test routines as well as special device-unique commands. See the section on Tape Maintenance Commands for further details.

Tape Data Format Characteristics

3.16 Since the 990 understands variable-length data records, and the SCSI formatter understands fixed-length blocks, additional steps were taken to mate the two philosophies. The following paragraphs describe these steps:

Physical Record Format

3.16.1 The tape will be formatted into physical records made up of consecutive fixed blocks. Each fixed block has 512 bytes of data.

Data Block Format

3.16.2 Tape format must comply to QIC-24 standard for 1/4-inch streaming tape.

	Preamble	— flux reversals: 120 min/300 max
	Data Block Marker	— 1 byte
*	Data	— 512 bytes
	Block Address	— 4 bytes
	CRC	— 2 bytes
	Postamble	— flux reversals: 5 min/20 max

* Data area is the only interface accessible entity.

Logical Record Format

3.16.3 Logical records will consist of one or more consecutive physical records with header information occupying the first physical data block. This header information specifies necessary information about record lengths, file numbers, and record numbers. These identifiers facilitate record skipping and file skipping as well as handling variable logical record lengths.
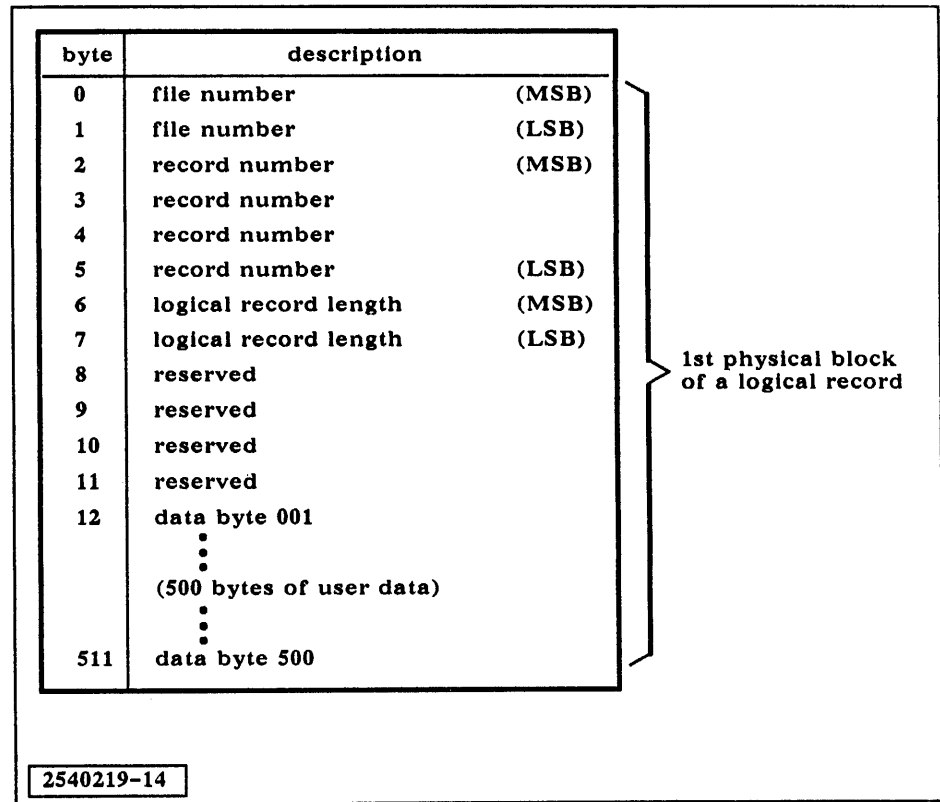
Essentially, the record length will be the specified transfer-byte count used when the record was originally written. On writes, data will be filled into the remaining bytes of the first block and any number of the successive 512 byte blocks to satisfy the remaining bytes. Fractional parts of the last block will be zero filled. EOF indications will be denoted by one file-mark block on the tape.

The maximum logical record length will be limited to 65,535 bytes and the minimum length to 1 byte.

The tape header information is detailed in Figure 3-11.

Figure 3-11

Tape Header Information Block

byte	description	
0	file number	(MSB)
1	file number	(LSB)
2	record number	(MSB)
3	record number	
4	record number	
5	record number	(LSB)
6	logical record length	(MSB)
7	logical record length	(LSB)
8	reserved	
9	reserved	
10	reserved	
11	reserved	
12	data byte 001	
	•	
	(500 bytes of user data)	
	•	
511	data byte 500	

1st physical block of a logical record

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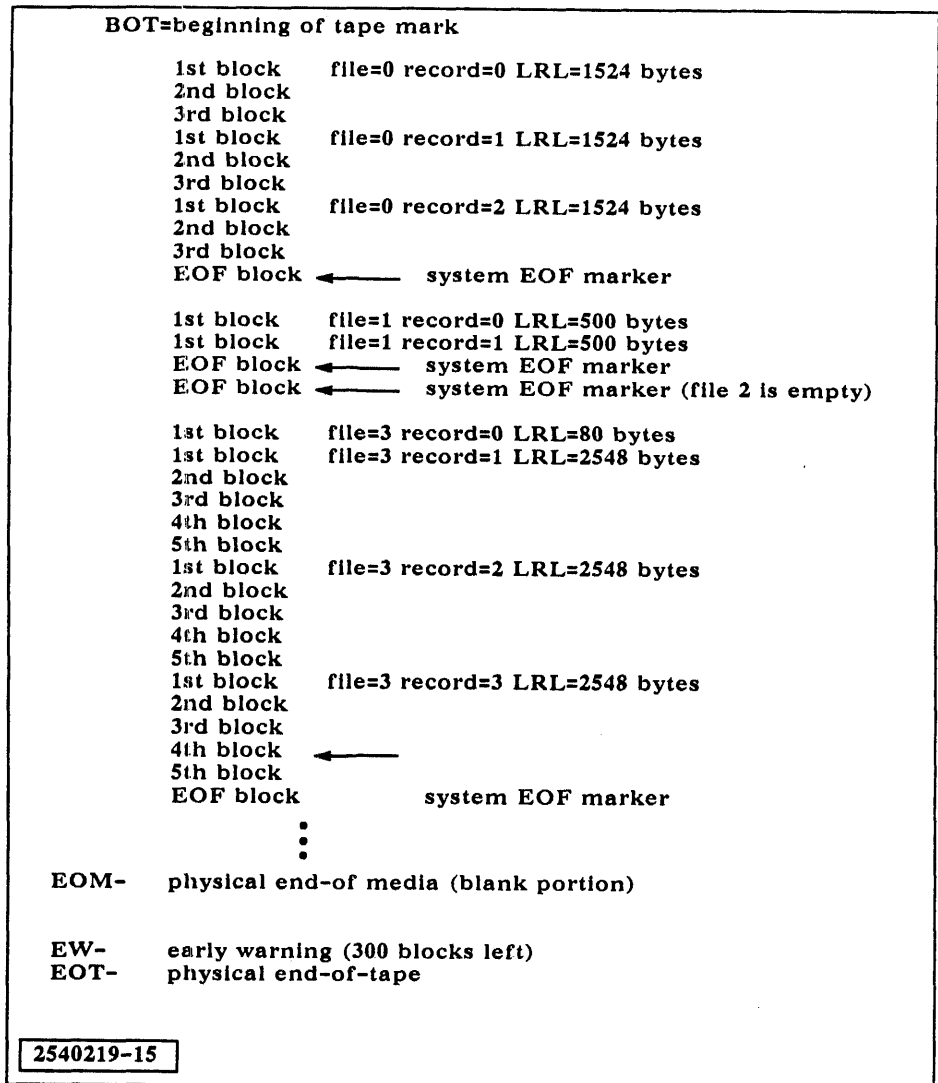
The following illustration, Figure 3-12, demonstrates several files of varying record lengths stored on a tape.

Figure 3-12

Tape File Structure Example

```
BOT=beginning of tape mark

         1st block      file=0 record=0 LRL=1524 bytes
         2nd block
         3rd block
         1st block      file=0 record=1 LRL=1524 bytes
         2nd block
         3rd block
         1st block      file=0 record=2 LRL=1524 bytes
         2nd block
         3rd block
         EOF block  ◄──────  system EOF marker

         1st block      file=1 record=0 LRL=500 bytes
         1st block      file=1 record=1 LRL=500 bytes
         EOF block  ◄──────  system EOF marker
         EOF block  ◄──────  system EOF marker (file 2 is empty)

         1st block      file=3 record=0 LRL=80 bytes
         1st block      file=3 record=1 LRL=2548 bytes
         2nd block
         3rd block
         4th block
         5th block
         1st block      file=3 record=2 LRL=2548 bytes
         2nd block
         3rd block
         4th block
         5th block
         1st block      file=3 record=3 LRL=2548 bytes
         2nd block
         3rd block
         4th block   ◄──────
         5th block
         EOF block              system EOF marker
                      •
                      •
                      •
EOM-    physical end-of media (blank portion)


EW-     early warning (300 blocks left)
EOT-    physical end-of-tape
```

2540219-15

End-of-Tape Handling

3.17 The physical description of the cartridge tape format is shown in Figure 3-13.

Figure 3-13 Physical Tape Description
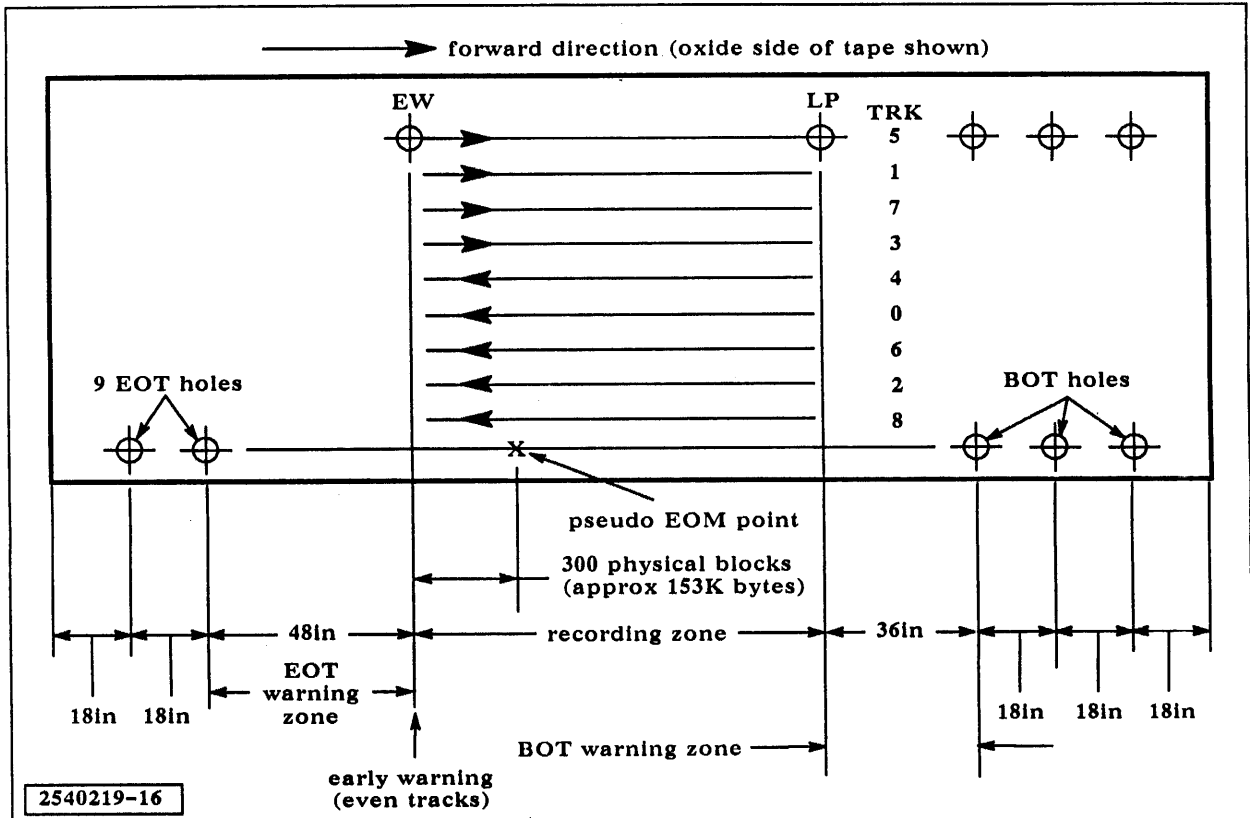
Status Reporting on End-of-Tape Situations

3.18 While writing data to tape using tracks 0 through 7, either the EW hole or LP hole are used to sense when a track switch and tape direction reversal should occur. In the case of track 8, the pseudo EOM point is sensed by formatter hardware, and SCSI write EOM status is returned to the controller. At this point, there are approximately 300 physical blocks (153K bytes) of data left on tape that can be written. Maximum number of blocks left in cache at this time will be about 27 or about 13.8K bytes.

Assuming maximum logical record size of 64K bytes, this leaves about 90K bytes remaining for error recovery in that record and any additional trailer records needed for system operation.

The 990/SCSI controller will flush the remaining portion of the record to tape and then report EOT status to the host. Additional writes can occur until physical EOT is received by the controller, whereby the host write is aborted and errored off. Physical EOT status will force Offline and EOT to be reported. This offline condition can only be cleared by executing an Unload command and removing or inserting a tape.

Maintenance/ Diagnostic Commands

3.19 Maintenance and diagnostic commands allow program control of on-board self-test routines as well as gaining access to 990/SCSI controller parameters. These commands are intended for diagnostic purposes, but it does not preclude others from using them. In particular, SCSI Pass-thru commands will extend program control over devices and formatters that reside on the SCSI bus.

Maintenance and diagnostic commands are accessed via disk TPCS command >87 and tape TPCS command >F. Upon acceptance of maintenance command, TPCS register 3 will contain the maintenance and diagnostic command code in bits 2–7. This maps into >00–>3F as the possible command codes. Bit 0 of register 3 will control the loop on the test feature of the self-test commands, and bit 1 maps commands into the controller-only mode.

Upon completion of self-test commands, register 7 will reflect failed status by setting bits 8–15 to all ones. At this point, register 2 will contain the self-test error code in bits 0–7 and the self-test number in bits 8–15.

Each individual command function will be discussed in the sections to follow. There are 64 maintenance commands available for each TPCS, as well as 64 commands for the 990/SCSI controller. All unused self-test commands are defaulted to execute all self test. All unused special commands perform no operation and return normal completion status.

990/SCSI Controller Maintenance Commands

3.19.1 Controller maintenance commands can be accessed via either disk or tape control space. These commands are control-space and unit-select independent, but their execution does force both TPCSs into the busy state until execution is completed. Selection of controller-only commands is addressed by opcodes >40 – >7F of register 3.

Table 3-7 Controller Maintenance Command Summary

Code	Maintenance Command	Functional Description
>40	EXECUTE ALL SELFTESTS	Performs All Tests
>41	ROM TEST	ROM CRC
>42	PROCESSOR TEST	68010 Test
>43	RAM TEST	Static Ram test
>44	MULTIFUNCTION CHIP	68901
>45	SCSI CHIP TEST	WD33C93 Controller
>46	FIFO TEST	FIFO Controller & FIFO Memory
>47	TPCS TEST	TILINE Registers & Control
>48	EXECUTE ALL SELFTESTS	Default Test #08 (Reserved)
>49	•	Default Test #09 (Reserved)
•	•	•
•	•	•
•	•	•
>5F	EXECUTE ALL SELFTESTS	Default Test #31 (Reserved)
>60	SCSI bus reset command	Resets SCSI Bus
>61	NO OPERATION	Reserved
>76	NO OPERATION	Reserved
>77	NO OPERATION	Reserved
>78	NO OPERATION	Reserved
>79	NO OPERATION	Reserved
>7A	NO OPERATION	Reserved
>7B	NO OPERATION	Reserved
>7C	READ PARAMETER BLOCK	Returns 990/SCSI Control/Info Block
>7D	EXECUTE MEMORY	Execute Code at PARM Block PC
>7E	WRITE MEMORY	Write Data to 990/SCSI Controller
>7F	READ MEMORY	Read Data from 990/SCSI Controller

Execute All Self-test — >40 and >48 Through >5F

3.19.1.1 This command forces the on-board self-test to execute all available tests. Error reporting for self-test failures is returned via the standard protocol of register 2 in the TPCS. Error codes will reside in the MSB. of the word and the self-test number will reside in the LSB. In the event of a self-test failure, the Fault LED will be lit, and all subsequent disk or tape operations (non-maintenance commands) will be prohibited from execution. This inhibit can be overridden by writing a 0 to the command-inhibit override location in the controller RAM. (Refer to the parameter block definitions.)

ROM Test — >41

3.19.1.2 This test will verify 990/SCSI controller ROMs for proper CRC-16 checksum. CRC is performed upon the entire ROM address space and should always be equal to the ROM revision level. This test is also run at power-up self test, but not from TILINE I/O reset.

Processor Test — >42

3.19.1.3 This test will perform a basic 68010 processor test for the on-board microprocessor. Basic commands and addressing modes will be verified. The test is run upon power-up self-test and upon TILINE I/O reset.

RAM Test — >43   **3.19.1.4** This test will perform an address and data pattern check for the onboard static RAM storage. When run from TILINE I/O reset, the original contents are saved, and a minimal pattern test is performed on each RAM location. When run from power-up self test, a more extensive address and pattern test is performed.

Multifunction Chip Test — >44   **3.19.1.5** This test will verify the MC68901 peripheral chip operation. Its internal registers will be verified for R/W capability and functional operation. Internal timers will be tested for accuracy and fundamental operation. Interrupt operation will also be checked. UART operation will be verified as a function of the resident monitor. This test is run upon power-up self test and upon TILINE I/O reset.

SCSI Chip Test — >45   **3.19.1.6** This test will verify operation and functioning of the WD33C93 SCSI controller chip. Internal register access and operation will be verified without forcing a SCSI bus reset to the formatters. This test is run upon power-up self test and upon TILINE I/O reset.

FIFO Test — >46   **3.19.1.7** This test will verify the on-board FIFO controller and its associated data path. Basic operation of R/W to the FIFO will be checked by both direct access as well as by pack/unpack buffer access. All status flags, control lines, and interrupt conditions will be verified. Also, a basic pattern test will be applied to the FIFO storage. This test is run upon power-up self-test and upon TILINE I/O reset.

TPCS Test — >47   **3.19.1.8** This test will verify local processor accesses to both TPCS registers and check appropriate data paths. Address uniqueness will also be verified. At this point, off-board master cycles will not be generated during self-test. This test is run upon power-up selftest and upon TILINE I/O reset.

SCSI Bus Reset Command — >60   **3.19.1.9** This command performs a hardware reset to the SCSI controller chip and the associated SCSI bus-reset line in the interface cable. Thus, all attached formatters will experience a reset and take appropriate action. Caution should be exercised before executing this command since subsequent disk and tape operations may be affected. This command is executed during power-up self test, so formatters are in a known state. TILINE I/O reset will only reset the SCSI bus when an outstanding command is active and not completed.

Read Parameter Block — >7C   **3.19.1.10** This command will transfer the 990/SCSI parameter block from controller memory to TILINE memory. A summary of this block is given in Table 3-8. Note that this block is read only, while parameters with address pointers are readable and variable. All pointer addresses are given MSB first.

Table 3-8

990/SCSI Controller Parameter Block Definitions

Parameter Definition	RO or R/W	Byte (DEC)	Comments
Board assy number	RO	00	ASCII characters 02549505
ROM firmware rev	RO	08	ASCII characters REVxxx$y
Address pointer to CMD inhibit	R/W	16	Address of command inhibit override (Write >0000)
Address pointer to program counter	R/W	18	Used by execute memory maintenance command
Address pointer to RAM low	RO	20	Lower bound of scratch RAM area
Address pointer to RAM high	RO	22	Upper bound of scratch RAM area

Execute Memory — >3D, >7D 3.19.1.11 This command forces program execution of 990/SCSI native code at the address pointed to by the program counter variable.

Write Memory — >3E, >7E 3.19.1.12 This command transfers the number of bytes specified in TPCS register 4 from TILINE memory to 990/SCSI controller memory. TILINE source address is specified in TPCS registers 5 and 6, while 990/SCSI destination address is specified in TPCS register 2. All addresses must be on a word boundary.

Read RAM Memory — >3F, >7F 3.19.1.13 This command transfers the number of bytes specified in TPCS register 4 from 990/SCSI to TILINE memory. TILINE destination address is specified in TPCS registers 5 and 6, while the 990/SCSI source address is specified in TPCS register 2. Note that only RAM memory is addressed by this command. All addresses must be on the word boundary.

Disk TPCS
Maintenance
Commands

3.19.2 TPCS disk maintenance commands are accessed via the Disk command >87. Maintenance opcodes >00 - >3F are defined in Table 3-9.

Table 3-9 Disk Maintenance Command Summary

Code	Maintenance Command	Functional Description
>00	EXECUTE ALL DISK TESTS	Performs all disk tests
>01	NO OPERATION	Default Test #01 (Reserved)
•	•	•
•	•	•
•	•	•
>1F	NO OPERATION	Default Test #31 (Reserved)
>20	NO OPERATION	Disk Special Command #00 (Reserved)
•	•	•
•	•	•
•	•	•
>38	NO OPERATION	DISK Special Command #24 (Reserved)
>39	SCSI DISK PASS-THRU READ	CPU issues SCSI cmd to Disk unit
>3A	SCSI DISK PASS-THRU WRITE	CPU issues SCSI cmd to Disk unit
>3B	NO OPERATION	Reserved
>3C	READ PARAMETER BLOCK	(Reserved for future expansion)
>3D	EXECUTE MEMORY	Execute code at PARM Block PC
>3E	WRITE MEMORY	Write data to 990/SCSI
>3F	READ MEMORY	Read data from 990/SCSI

Execute All Disk Tests — >00

3.19.2.1 This test will perform all defined disk tests as described in >01 through >1F. Error reporting will be via the standard test number- and error-code protocol as described in TPCS register 2.

Disk Tests — >01 Through >1F

3.19.2.2 These tests are reserved for future expansion. Presently they execute a maintenance NOP.

SCSI Pass Through Read — >39

3.19.2.3 This command allows the host to completely control the operation of a particular formatter with explicit SCSI commands. The formatter and logical unit addressed are derived from the TPCS used in issuing the command and the unit-select fields of the appropriate TPCS register. The host CPU is responsible for handling proper SCSI command setup.

This command allows data to be transferred from a device to TILINE memory. Due to hardware and firmware implementation, the 990/SCSI controller cannot transfer more than 64K bytes in one operation.

Required input to this command is a pointer to a parameter list in TILINE memory. This pointer is supplied in the TILINE address of registers 5 and 6. The parameter block is always nine words in length. For pass-through structure, refer to Figure 3-14, entitled SCSI Pass-Through Command Structure.

Figure 3-14 SCSI Pass-Through Command Structure

2540219-28
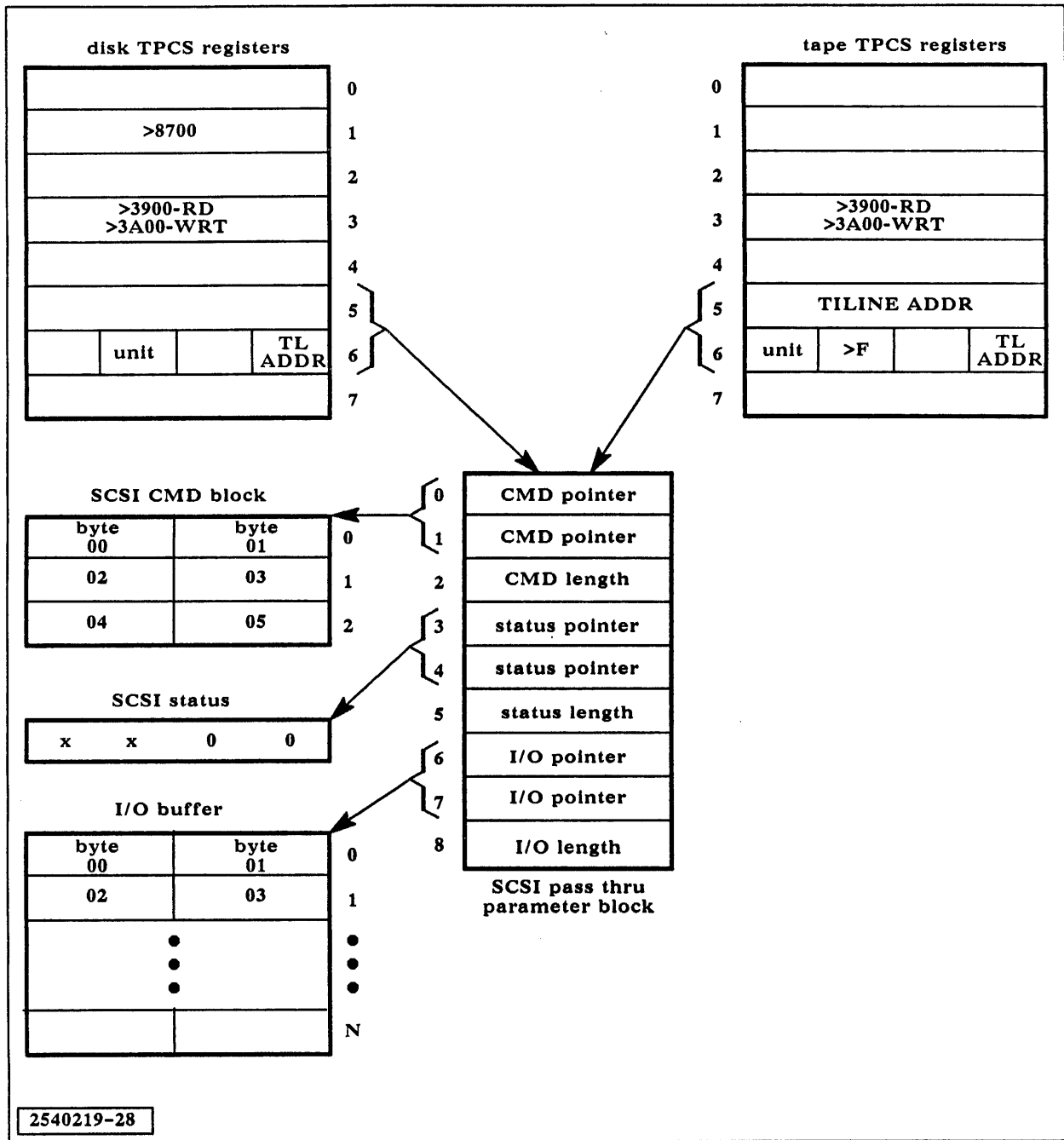
This parameter block contains the following information (Table 3-10):

Table 3-10

Word	Definition
SCSI Pass-Through Parameter Block
0	SCSI command pointer (MSW)
1	SCSI command pointer (LSW)
2	SCSI command length in bytes
3	Status buffer pointer (MSW)
4	Status buffer pointer (LSW)
5	Status buffer length in bytes
6	I/O data buffer pointer (MSW)
7	I/O data buffer pointer (LSW)
8	I/O data buffer length in bytes

Upon command completion, normal TPCS status will be returned with the affected bits being idle, op complete, and error (Reg 7, Bits 0 – 2). The only error conditions that will be flagged are command timeout, TILINE timeout, TILINE memory error, and abnormal completion. Unit error (Reg 7, Bit 15) will always be cleared. The user will be responsible for extracting device status with the SCSI pass-thru protocol. TPCS status in register 0 will reflect the state (except command timeout for tape) of the last normal TPCS command.

CAUTION: SCSI Pass-thru commands are intended for an "expert user" situation and should not be attempted without prior knowledge of SCSI command protocol and status reporting.

SCSI Pass Through Write — >3A

3.19.2.4 This command is identical to the SCSI pass-thru read, except it allows data to be transferred from TILINE memory to a device.

Tape TPCS Maintenance Commands

3.19.3 TPCS tape-maintenance commands are accessed via the Tape command >0F. Maintenance opcodes >00 – >3F are defined in Table 3-11.

Table 3-11 Tape Maintenance Command Summary

Code	Maintenance Command	Functional Description
>00	EXECUTE ALL TAPE TESTS	Performs All Tape Tests
>01	NO OPERATION	Default Test #01 (Reserved)
•	•	•
•	•	•
•	•	•
>1F	NO OPERATION	Default Test #31 (Reserved)
>20	TAPE STORE REGISTERS	Return Execution Dependent Info
>21	NO OPERATION	Tape Special Command #01(Reserved)
•	•	•
•	•	•
•	•	•
>38	NO OPERATION	Tape Special Command #24 (Reserved)
>39	SCSI TAPE PASS-THRU READ	CPU Issues SCSI Cmd to Tape unit
>3A	SCSI TAPE PASS-THRU WRITE	CPU Issues SCSI Cmd to Tape unit
>3B	NO OPERATION	Reserved
>3C	READ PARAMETER BLOCK	(Reserved for Future Expansion)
>3D	EXECUTE MEMORY	Execute Code at PARM Block PC
>3E	WRITE MEMORY	Write Data to 990/SCSI
>3F	READ MEMORY	Read Data from 990/SCSI

Execute All Tape Tests — >00
3.19.3.1 This test will perform all defined tape tests as described in >01 through >1F. Error reporting will be via the standard test number- and error-code protocol as described in TPCS register 2.

Tape Tests — >01 Through >1F
3.19.3.2 These tests are reserved for future expansion. Presently they execute a maintenance NOP.

Tape Store Registers — >20
3.19.3.3 This command will return specific tape-related parameters that will allow customization of DSR routines. In particular, this command will return a three-word block to TILINE memory as specified in TPCS registers 5 and 6. The unit-select field of register 6 will be used for selecting the desired tape unit.

The words-returned parameters are defined as follows:

WORD 0 BITS 00–15: TAPE COMMANDS SUPPORTED —
    >00 THRU >0F
    1 = Command supported
    0 = Command not supported

WORD 1 BIT 00: RETRY INHIBIT BIT
    1 = System S/W should not attempt retries
    0 = Tape controller does no retries
    BITS 01–02: TAPE MEDIA TYPE — returns 00
    (Cartridge Streamer)
    BITS 03–15: RESERVED — returns all 0's

WORD 2 BITS 00–15: RESERVED — returns all 0's

Each bit of word zero is assigned to one of 16 commands. When the bit is set to a 1, it indicates to the software that the associated tape command is supported by the 990/SCSI controller. Table 3-12 details the bit assignments. Unsupported commands (bit state = 0) execute the same as a NOP command or result in definitive error codes.

Table 3-12

Supported Commands for Tape

Command Code	990 Command	Bit Position in Word 0	Bit State
0	NOP (Reserved)	0	1
1	Buffer Sync (write sync)	1	0
2	Write End of File (EOF)	2	1
3	Record Skip Reverse	3	0
4	Read Forward	4	1
5	Record Skip Forward	5	1
6	Write Forward	6	1
7	Erase	7	1
8	Read Transport Status	8	1
9	Read Transport Status	9	1
A	Rewind	10	1
B	Unload (rewind and offline)	11	1
C	Write Unformatted	12	1
D	Read Unformatted	13	1
E	NOP (Reserved)	14	1
F	Extended Control/Status	15	1

990/SCSI Controller Error Codes

3.20   The 990/SCSI controller error codes are described in the following paragraphs.

Maintenance/ Diagnostic Error Codes

3.20.1   Diagnostic commands, particularly self-test routines, will return error codes in Bits 00-07 of TPCS register 2. These codes will reflect the failure that occurred.

Other commands will use the normal error-reporting mechanisms of TPCS registers 0 and 7. Also, certain error conditions may prompt further investigation into SCSI error codes reported in TPCS register 2 for tape and TPCS registers 2 and 3 for disk. Refer to the appropriate section of this specification for more details.

Controller Hardware/ Firmware Errors

3.20.1.1   Hardware failures detected during any self-test situation will illuminate the Fault LED and prohibit any further disk or tape commands from executing. The failed self-test number and error code will be reported as termination status for each subsequent command to the disk or tape. Overt actions must be taken to override this error condition.

When situations of hardware or firmware failures occur that are unrecoverable as to TPCS command completion, all attempts of normal error conventions will be used. In the event of hard failures, the Fault LED will be illuminated and normal self-test reporting will be initiated. In the event of soft failures, the Fault LED will be continuously in a blinking mode of operation. This will visually alert the user that system integrity may be threatened.

Some situations, such as SCSI formatter failures, will be presented to the user only as offline devices

SCSI Error Code Mapping for Disks

3.21 For the MSU II disk formatter, which does support extended status, the error class is set to >7, and the error code is set to >00. Neither of them is mapped into the TPCS for MSU II. Rather, the additional error byte is mapped into the TPCS word 2, bits 0-7; the sense key is mapped to TPCS word 3, bits 0-3; and the EXT bit is set to 1.

Any SCSI error code which is not listed in Table 3-13 is mapped to a status of offline, unit error, and error (bits 15, 2 of word 7; and bit 7 of word 0). In addition, the SCSI sense key and error code is reported in words 2 and 3.

Paragraph 3.21 (this section) illustrates the mapping from sense code to 990 disk TPCS words and bits. Paragraph 3.22 illustrates the mapping from SCSI sense code to 990 tape TPCS words and bits.

Formatter status is obtained by the firmware via the Request-sense SCSI command. Per ANSI specifications for SCSI (and CCS), the sense key refers to byte 0, bits 0-3; the error class refers to byte 0, bits 4-6, the error code refers to byte 0, bits 0-3; and the additional error byte refers to byte 0C, bits 0-7.

Table 3-13 SCSI to Disk TPCS Error Code Mapping

SCSI Sense Key	SCSI Error Code		Description	990 TPCS Status Reg 0 (Bits 0–7)	990 TPCS Status Reg 7 (Bits 0–15)
No Sense					
00	00		No Sense	$00 – none	$0000 – no error
Recovered Error					
01	02		No seek cmplt	$00 – none	$0400 – RETRY
01	03		Write fault	$00 – none	$0400 – RETRY
01	04		Drive not ready	$00 – none	$0400 – RETRY
01	08		LUN comm failure	$00 – none	$0400 – RETRY
01	09		Track follow err	$00 – none	$0400 – RETRY
01	10	*	ID CRC error	$00 – none	$0400 – RETRY
01	12	*	No ID adr mark	$00 – none	$0400 – RETRY
01	13	*	No data adr mark	$00 – none	$0400 – RETRY
01	14	*	Block not found	$00 – none	$0400 – RETRY
01	15		Seek error	$00 – none	$0400 – RETRY
01	17	*	RD err w/retry	$00 – none	$0400 – RETRY
01	18	*	RD err w/ECC	$00 – none	$0600 – RETRY,ECC
01	19		Defect list error	$00 – none	$0400 – RETRY
01	1C		Primary list lost	$00 – none	$0400 – RETRY
01	44		SCSI h/w error	$00 – none	$0400 – RETRY
01	81	*	ID CRC (shock)	$00 – none	$0400 – RETRY
01	82		Parity err ESDI status	$00 – none	$0400 – RETRY
01	83		RCVD data — R/SK/Low	$00 – none	$0400 – RETRY
01	84		RCVD data — R/SK/High	$00 – none	$0400 – RETRY
01	85		CMD abort timeout	$00 – none	$0400 – RETRY
01	86		Unspecified RD err	$00 – none	$0400 – RETRY
01	87		Unspecified WRT err	$00 – none	$0400 – RETRY
01	89		ESDI Status 0	$00 – none	$0400 – RETRY

Table 3-13 SCSI to Disk TPCS Error Code Mapping (Continued)

SCSI Sense Key	SCSI Error Code		Description	990 TPCS Status Reg 0 (Bits 0–7)	990 TPCS Status Reg 7 (Bits 0–15)
Not Ready					
02	04		Drive notrdy	$80 – Offline	$2001 – ERR,UERR
02	05		Drive not seltd	$80 – Offline	$2001 – ERR,UERR
02	22		Illegal function dev	$00 – none	$2004 – ERR,CMDTO
02	44		SCSI h/w error	$00 – none	$2004 – ERR,CMDTO
Medium Error					
03	10	*	ID CRC error	$00 – none	$2010 – ERR,ID
03	11	*	Uncorr data err	$00 – none	$2040 – ERR,DATA
03	12	*	No ID adr mark	$00 – none	$2010 – ERR,ID
03	13	*	No data adr mark	$00 – none	$2002 – ERR,SCH
03	14	*	Block not found	$00 – none	$2010 – ERR,ID
03	15		Seek error	$04 – SEEK INC	$2001 – ERR,UERR
03	19		Defect list err	$10 – UNSAFE	$2001 – ERR,UERR
03	1C		Prim defect lst n/f	$10 – UNSAFE	$2001 – ERR,UERR
03	31		Format corrupt	$10 – UNSAFE	$2001 – ERR,UERR
03	32		No spare avail	$10 – UNSAFE	$2001 – ERR,UERR
03	80		Error on drive r/w	$10 – UNSAFE	$2001 – ERR,UERR
03	81	*	ID CRC (shock)	$00 – none	$2010 – ERR,ID
03	86		Unspecified RD err	$10 – UNSAFE	$2001 – ERR,UERR
03	87		Unspecified wrt err	$10 – UNSAFE	$2001 – ERR,UERR
Hardware Error					
04	01		Index/sector	$10 – UNSAFE	$2001 – ERR,UERR
04	02		No seek cmplt	$04 – SEEK INC	$2001 – ERR,UERR
04	03		Write fault	$10 – UNSAFE	$2001 – ERR,UERR
04	04		Drive notrdy	$80 – OFFLINE	$2001 – ERR,UERR
04	05		Drive not seltd	$80 – OFFLINE	$2001 – ERR,UERR
04	06		No track 0	$10 – UNSAFE	$2001 – ERR,UERR
04	08		LUN comm failure	$10 – UNSAFE	$2001 – ERR,UERR
04	09		Track following err	$10 – UNSAFE	$2001 – ERR,UERR
04	10	*	ID CRC error	$00 – none	$2010 – ERR,ID
04	12	*	No ID adr mark	$00 – none	$2010 – ERR,ID
04	15		Seek error	$04 – SEEK INC	$2001 – ERR,UERR
04	40		RAM failure	$10 – UNSAFE	$2001 – ERR,UERR
04	43		SCSI message reject	$00 – none	S2004 – ERR,CMDTO
04	44		SCSI h/w err	$00 – none	$2004 – ERR,CMDTO
04	45		Sel/Rslt err	$00 – none	$2004 – ERR,CMDTO
04	47		Parity error	$00 – none	$2004 – ERR,CMDTO
04	82		Parity err ESDI status	$00 – none	$2004 – ERR,CMDTO
04	89		ESDI status 0	$10 – UNSAFE	$2001 – ERR,UERR
Illegal Request					
05	1A		Parameter overrun	$00 – none	$2004 – ERR,CMDTO
05	1C		Primary list lost	$10 – UNSAFE	$2001 – ERR,UERR
05	20		Invalid Cmd op code	$00 – none	$2004 – ERR,CMDTO
05	21		Bad block adr	$04 – SEEK INC	$2001 – ERR,UERR
05	22		Illegal funct device	$00 – none	$2004 – ERR,CMDTO
05	24		Bad fld in CDB	$00 – none	$2004 – ERR,CMDTO
05	25		Invalid LUN	$00 – none	$2004 – ERR,CMDTO
05	26		Bad parm list	$00 – none	$2004 – ERR,CMDTO

Table 3-13 SCSI to Disk TPCS Error Code Mapping (Continued)

SCSI Sense Key	SCSI Error Code	Description	990 TPCS Status Reg 0 (Bits 0–7)	990 TPCS Status Reg 7 (Bits 0–15)
UNIT Attention				
06	28	Media change	$80 – OFFLINE	$2001 – ERR,UERR
06	29	Pwrup/Reset	$00 – none	$2100 – ERR,ABN
06	2A	Mode sel chng	$10 – UNSAFE	$2001 – ERR,UERR
Data Protect				
07	27	Wrt protected	$20 – WP	$2001 – ERR,UERR
990/SCSI Controller Specific				
09	50	SCSI bus hung	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	51	Excess data; incmplt xfr	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	63	Sync/SCSI parity error	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	66	Invalid disconnect	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	67	Unexpected disconnect	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	68	Invld mode on status phase	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	69	Invld mode on command phase	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	71	Invld mode on MSG in phase	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	72	Status received twice	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	75	Invalid reconnect	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	76	Cmd cmplt MSG not recvd	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	77	Illegal message recvd	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	78	Reconnect w/invld ID error	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	79	Invalid mode on message out	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	7A	Invalid mode on data phase	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	7B	Invld mode — illegal reject	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	7C	Cmd cmplt MSG before status	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	7D	Non-disc after cmd cmplt	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	7E	Illegal phase	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	81	Timeout & cmd abort error	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	8A	Formatter did not connect	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	A1	Illegal interrupt	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	A2	Paused w/ack int w/o cause	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	A3	DBR timeout	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	AD	LCI error	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	AE	CIP timeout error	$80 – OFFLINE	$2005 – ERR,CMDTO,UERR
09	D0	Disk 0 fmtr overtemp	$00 – none	$0400 – RETRY
09	D1	Disk 1 fmtr overtemp	$00 – none	$0400 – RETRY
09	D2	Disk 2 fmtr overtemp	$00 – none	$0400 – RETRY

Table 3-13 SCSI to Disk TPCS Error Code Mapping (Continued)

SCSI Sense Key	SCSI Error Code	Description	990 TPCS Status Reg 0 (Bits 0–7)	990 TPCS Status Reg 7 (Bits 0–15)
Aborted Command				
0B	43	SCSI MSG RJT	$00 – none	$2004 – ERR,CMDTO
0B	45	Sel/Resel error	$00 – none	$2004 – ERR,CMDTO
0B	47	Parity error	$00 – none	$2004 – ERR,CMDTO
0B	48	Init detect	$00 – none	$2004 – ERR,CMDTO
0B	49	Illegal MSG	$00 – none	$2004 – ERR,CMDTO
0B	85	CMD abort timeout	$00 – none	$2004 – ERR,CMDTO
Non-Extended Codes				
––	00	No error	$00 – none	$0000 – none
––	01	No index sector	$10 – UNSAFE	$2001 – ERR,UERR
––	02	No seek complete	$04 – SEEK INC	$2001 – ERR,UERR
––	03	Write fault	$10 – UNSAFE	$2001 – ERR,UERR
––	04	No drive ready	$80 – OFFLINE	$2001 – ERR,UERR
––	10 *	ID CRC error	$00 – none	$2010 – ERR,ID
––	11 *	Data error	$00 – none	$2040 – ERR,DATA
––	12 *	No ID adr mark	$00 – none	$2010 – ERR,ID
––	14 *	No ID compare	$00 – none	$2010 – ERR,ID
––	15 *	Seek error	$00 – none	$2010 – ERR,ID
––	18	Data check	$00 – none	$0600 – RETRY,ECC
––	19	Data ECC Err-verify	$00 – none	$2240 – ERR,ECC,DATA
––	1C	Format error	$10 – UNSAFE	$2001 – ERR,UERR
––	20	Invalid command	$00 – none	$2004 – ERR,CMDTO
––	21	Illegal block	$04 – SEEK INC	$2001 – ERR,UERR
––	23	Volume overflow	$04 – SEEK INC	$2001 – ERR,UERR
––	24	Illegal argument	$00 – none	$2004 – ERR,CMDTO
––	25	Illegal LUNO	$00 – none	$2004 – ERR,CMDTO
––	27	Write protect	$02 – WP	$2001 – ERR,UERR
––	28	Media change	$80 – OFFLINE	$2001 – ERR,UERR
––	29	Parameters changed	$10 – UNSAFE	$2001 – ERR,UERR
––	2B	Limit violation	$10 – UNSAFE	$2001 – ERR,UERR
––	2C	Err count overflow	$10 – UNSAFE	$2001 – ERR,UERR
––	2D	Initiator detected err	$10 – UNSAFE	$2001 – ERR,UERR
––	2E	SCSI parity error	$00 – none	$2004 – ERR,CMDTO
––	2F	Fmt internal parity err	$10 – UNSAFE	$2001 – ERR,UERR
Unknown Sense Key & Error Code				
??	??	Not in this table	$80 – OFFLINE	$2001 – ERR,UERR

NOTE:

Errors marked with * will force an FMT table entry.

SCSI Error Code Mapping for Tapes

3.22 This paragraph describes how SCSI sense keys and error codes are mapped to 990 TPCS words. Table 3-14 illustrates how the 990 TPCS error bits map into SCSI sense keys and error codes. The sense key is from byte 02, bits 0-3. The error code is from byte 08, bits 0-3.

Table 3-14   SCSI to Tape TPCS Error Code Mapping

SCSI Sense Key	SCSI Error Code	Description	990 TPCS Status Reg 0 (Bits 0-7)	990 TPCS Status Reg 7 (Bits 0-15)
Archive Tape (Extended Sense)				
00	00	No sense	$00 – none	$0000 – no error
00	1C *	File mark found	$10 – EOF	$2001 – ERR,UERR
00	34 *	End-of-media (early warn)	$08 – EOT	$2001 – ERR,UERR
01	00	Recovered error	$00 – none	$2040 – ERR,CORR
02	00	Not ready/no medium	$80 – OFFLINE	$2001 – ERR,UERR
03	00	Medium error	$00 – none	$2020 – ERR,DATA
04	00	H/w error	$80 – OFFLINE	$2001 – ERR,UERR
05	00	Illegal request	$01 – Cmdto	$2001 – ERR,UERR
06	00	Unit attention	$C0 – OFFLINE, BOT	$2001 – ERR,UERR
07	00	Write protect	$04 – WP	$2001 – ERR,UERR
08	00	Blank check	$01 – CMDTO	$2001 – ERR,UERR
0B	00	Aborted command	$80 – OFFLINE	$2001 – ERR,UERR
0D	00	Volume overflow	$88 – OFFLINE, EOT	$2001 – ERR,UERR
Cipher Tape (Extended Sense)				
00	00	No sense	$00 – none	$0000 – no error
00	0A	Insufficient capacity	$08 – EOT	$2001 – ERR,UERR
00	1C	File mark found	$10 – EOF	$2001 – ERR,UERR
00	34	End-of-media (early warn)	$08 – EOT	$2001 – ERR,UERR
01	18	Correctable data check	$00 – none	$2040 – ERR,CORR
02	09	Media not loaded	$80 – OFFLINE	$2001 – ERR,UERR
02	31	Command timeout	$01 – CMDTO	$2001 – ERR,UERR
03	11	Uncorrectable data error	$00 – none	$2020 – ERR,DATA
03	31	Command timeout	$01 – CMDTO	$2001 – ERR,UERR
04	04	Drive not ready	$80 – OFFLINE	$2001 – ERR,UERR
05	20	Invalid command	$01 – CMDTO	$2001 – ERR,UERR
05	33	Append error on write	$01 – CMDTO	$2001 – ERR,UERR
05	34	Read past end-of-media	$01 – CMDTO	$2001 – ERR,UERR
06	30	Unit attention	$C0 – OFFLINE, BOT	$2001 – ERR,UERR
07	17	Write protect	$04 – WP	$2001 – ERR,UERR
08	34	Read past end-of-media	$01 – CMDTO	$2001 – ERR,UERR
0B	09	Media not loaded	$80 – OFFLINE	$2001 – ERR,UERR
0D	0A	Insufficient capacity	$88 – OFFLINE, EOT	$2001 – ERR,UERR
0E	1D	Compare error on verify	$01 – CMDTO	$2001 – ERR,UERR

Table 3-14 SCSI to Tape TPCS Error Code Mapping (Continued)

SCSI Sense Key	SCSI Error Code	Description	990 TPCS Status Reg 0 (Bits 0-7)	990 TPCS Status Reg 7 (Bits 0-15)
Cipher Tape (Non-Extended Sense)				
--	0B	Drive timeout	$01 - CMDTO	$2001 - ERR,UERR
--	14	Block not found	$00 - none	$2002 - ERR,FMT
--	16	DMA timeout	$00 - none	$2008 - ERR,TIM
--	19	Bad block found	$00 - none	$2020 - ERR,DATA
--	1D	Compare error on verify	$01 - CMDTO	$2001 - ERR,UERR
990/SCSI Controller Specific				
09	3E	EOR status detected	$20 - EOR	$2001 - ERR,DATA
09	3F	Bad header detected	$00 - none	$2002 - ERR,FMT
09	50	SCSI bus hung	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	51	Excess data; incmplt xfr	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	63	Sync/SCSI parity error	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	66	Invalid disconnect	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	67	Unexpected disconnect	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	68	Invld mode on status phase	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	69	Invld mode on command phase	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	71	Invld mode on msg in phase	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	72	Status received twice	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	75	Invalid reconnect	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	76	Cmd cmplt msg not recvd	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	77	Illegal message recvd	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	78	Reconnect w/invld ID error	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	79	Invalid mode on message out	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	7A	Invalid mode on data phase	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	7B	Invld mode — illegal reject	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	7C	Cmd cmplt msg before status	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	7D	Non-disc after cmd cmplt	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	7E	Illegal phase	$81 - OFFLN, CMDTO	$2001 - ERR,UERR
09	81	Timeout and cmd abort	$81 - OFFLN, CMDTO	$2001 - ERR,UERR

Table 3-14 SCSI to Tape TPCS Error Code Mapping (Continued)

SCSI Sense Key	SCSI Error Code	Description	990 TPCS Status Reg 0 (Bits 0–7)	990 TPCS Status Reg 7 (Bits 0–15)
09	8A	Formatter did not connect	$81 – OFFLN CMDTO	$2001 – ERR,UERR
09	A1	Illegal interrupt	$81 – OFFLN CMDTO	$2001 – ERR,UERR
09	A2	Paused w/ack int w/o cause	$81 – OFFLN CMDTO	$2001 – ERR,UERR
09	A3	DBR timeout	$81 – OFFLN CMDTO	$2001 – ERR,UERR
09	AD	LCI error	$81 – OFFLN CMDTO	$2001 – ERR,UERR
09	AE	CIP timeout error	$81 – OFFLN CMDTO	$2001 – ERR,UERR
Unknown Sense Key & Error Code				
??	??	Not in this table	$80 – OFFLINE	$2001 – ERR,UERR

NOTE:

Errors marked with * will force an FMT table entry.

Overview

4.1 The mass storage unit (MSU) provides high performance and large capacity with small form-factor (5 1/4-inch) Winchester disk drives and cartridge tape drives. The MSU provides data/program storage as well as backup and transportable media.

Each MSU contains a power supply with a fan. The MSU II also contains a disk drive formatter when Winchester disk drives are present. The formatter for the cartridge tape drive is mounted on the tape drive. MSU IIA disks and tapes have their individual formatters (drive mounted). The MSU can have the following combinations of Winchester disk drives and cartridge tapes:

■ Two Winchester disk drives

■ One Winchester disk and one cartridge tape

■ One Winchester disk drive

■ One cartridge tape drive

A variety of combinations of disks and tapes, up to a total of four disks and four tapes, are available by connecting MSU IIs with one or more daisy-chain cables. Figure 1-2 shows two MSUs; the top one contains a cartridge tape drive; the lower one has two Winchester disk drives.

MSU IIAs feature embedded SCSI drives that require one formatter per drive. Therefore, seven devices can be supported (four disks and three tapes).

For additional information regarding the internal components of the MSU, refer to the appropriate *Mass Storage Unit General Description* manual.

The remainder of this section details changes from the *MSU II General Description* manual. These include:

■ Formatted capacity — MSU II and MSU IIA

■ Synchronous operation

Formatted Capacity	**4.2** To determine the formatted capacity in a 990 environment, spare sectors and reserved cylinders need to be considered. The following paragraphs detail how the formatted capacity values are determined, taking into account these reserved areas and spare sectors for the MSU II and the MSU IIA.

For the MSU II, the calculations are as follows:

Total formatted capacity, (not including spares)
= (36 sect/trk)(512 bytes/sector)(9 heads)(969 cylinders)
= 160,745,472 bytes

Reserved cylinders = 3 for vendor map, grown map, & format information.
+ 7 which represents total amount of spare sectors.
+ 2 for 990 diagnostics use.
─────
= 12 cylinders total, reserved.

Unreserved cylinders = total − Reserved = 969−12=957

Total 990 user capacity (accounting for spares and reserved areas)
= (36 sect/trk)(512 bytes/sector)(9 heads)(957 cylinders)
= 158,754,816 bytes

The seven cylinders which represent the total amount of spare sectors is derived as follows:

Total spare sectors = (2 sectors)(966 cyl.) + 34 (last track remainder)
= 1966 sectors

Number of cylinders = ((1966 sectors)/(36 sect/track)) / (9 heads)
= 6.0679 cylinders
= 7 (rounded up)

Thus the 990 user has 486,400 fewer bytes of formatted capacity than the MSU II manual indicates. This loss is attributed to the following items:

■ Diagnostic cylinders (331,776 bytes)

■ Additional spares (154,624 bytes)

For the MSU IIA, the calculations are as follows:

Total formatted capacity, (not including spares)
= (36 sect/trk)(512 bytes/sector)(15 heads)(1224 cylinders)
= 338,411,520 bytes

Reserved cylinders = 6 for vendor map, grown map, & format information.
+ 12 which represents total amount of spare sectors.
+ 2 for 990 diagnostics use.
_____

= 20 cylinders total, reserved.

Unreserved cylinders = total − Reserved = 1224−20=1204

Total 990 user capacity (accounting for spares and reserved areas)
= (36 sect/trk)(512 bytes/sector)(15 heads)(1224 cylinders)
= 338,411,520 bytes

The 12 cylinders which represent the total amount of spare sectors are derived as follows:

Total spare sectors   = (5 sect/cyl)(1224 cyl−6 reserved cyl)
= 6090 sectors

Number of cylinders = ((6090 sect)/(36 sect/trk)) / (15 heads)
= 11.277 cylinders
= 12 (rounded up)

Thus, the 990 user has 752,640 fewer bytes of formatted capacity than the MSU IIA manual indicates. This loss is attributed to the following items:

■ Diagnostic cylinders (552,960 bytes)

■ Additional spares (199,680 bytes)

**Synchronous
Operation**

4.3 Synchronous operation and protocols are not supported by the 990/SCSI controller.

ACRONYM LIST

a

ANSI	American National Standard Institute
ASCII	American Standard Code for Information Interchange

b

BOT	Beginning of Tape

c

CCS	Common Command Set
CMD	Command

d

DMA	Direct Memory Access

e

EOM	End of Medium
EOT	End of Tape
ESDI	Enhanced Small Disk Interface

f

FCC	Federal Communications Commission
FIFO	First-in, First-out Memory
FM	File Mark

h

HEX or >	Hexidecimal
HW	Hardware

i

ID	Identification
ILI	Incorrect Length Indicated
I/O	Input/Output

k

KB	Kilobyte

l

LED	Light-Emitting Diode
LSB	Least Significant Bit

m

MB	Megabyte
Mb	Megabit
MSG	Message
MSW	Most Significant Word
MP	Microprocessor
MTBF	Mean Time Between Failure
MTTR	Mean Time To Repair
MSB	Most Significant Bit.
MSU	Mass Storage Unit

n

n/c	No Connection
NOP	No-operation

p

PLO	Phase-locked Oscillator

r

RAM	Random Access Memory
ROM	Read Only Memory

s

SCSI	Small Computer System Interface
S-T	Self-Test
SW	Software

v

VSE	Verband Deutscher Electrotechniker

symbols

>nnnn	Hexidecimal (hex) number

INDEX

DB380, CT2000,
AND WD1200 FIRMWARE SUPPORT

Introduction

Congratulations on the purchase of your new Texas Instruments peripheral. TI peripherals (DB380, CT2000, and WD1200) have important features that require appropriate supporting firmware on the host controller.

Firmware Check

If your peripheral is shipped as part of a system, the host controllers in the system will contain the necessary firmware to fully support the devices. If the peripheral is to be configured as an add-on to an existing system, then you should verify that the host controller(s) on the existing system contains operational firmware that is designed to support the peripheral.

You should refer to Table 1 and Table 2 of this document to perform this firmware check. Table 1 identifies each host controller along with its corresponding firmware EPROMs and their locations on the board.

Table 1 EPROM Identification

Assembly Board	Assembly Part Number	EPROM Part Number	EPROM Location
MSC	2537780	2537809	EH091
		2537810	FF096
NUPI	2238040	2238056	FA059
		2238057	EC059
990/SCSI	2549505	2549515	GA105
		2549516	GA086
S1200/1300 SCSI Host Option Controller	2535695	2552552	BA056

Table 2 on the next page identifies the host controller firmware revision that supports the applicable peripheral devices. The firmware revision listed is the minimum acceptable revision for that peripheral. Later revisions are also acceptable unless otherwise noted. Note also that not all peripheral devices are supported by all host controllers.

To obtain EPROM dash numbers, inspect the board assembly. A label on the EPROM(s) indicates the base number and dash number of the firmware. Assembly revision levels are marked on the printed wiring board, usually located along the top edge of the board. On NuBus™ systems you can also determine the MSC and NUPI board assembly numbers and revision levels by typing an E when the load prompt appears.

NuBus is a trademark of Texas Instruments Incorporated.

Table 2 Firmware Requirements for Peripherals

Board	Parameter	DB380	CT2000	WD1200
MSC	Firmware code revision	*E	*F	*D
	EPROM dash number	-0007	-0008	-0006
	Firmware update tape	2.1.0	2.2.0	2.0.0
	Assembly revision	BJ	BL	BF
NUPI	Firmware code revision	*M	See note.	See note.
	EPROM dash number	-0013		
	Assembly revision	AH		
990/SCSI	Firmware code revision	*E	See note.	See note.
	EPROM dash number	-0006		
	Assembly revision	J		
S1200/1300 SCSI Host Option Controller	Firmware code revision	1.1	See note.	See note.
	EPROM dash number	-0002		
	Assembly revision	N		

Note:
This peripheral is not supported by this host controller.

Data Systems Group – Austin
Documentation Questionnaire

990/SCSI Mass Storage Subsystem General Description

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_____   _____

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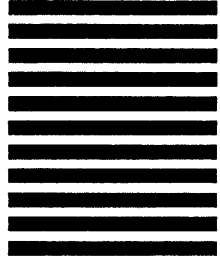
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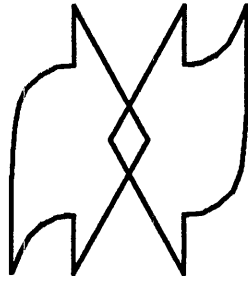☐ I wish to join now and include my credit card information below.

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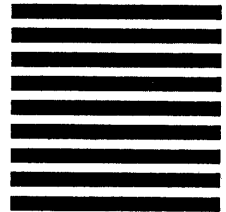IN THE
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