INSTALLATION AND OPERATION

Four-Channel Asynchronous Communications Interfaces (CI403 and CI404)

Part No. 2263897-9701 *B
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The computers offered in this agreement, as well as the programs that TI has created to use with them, are tools that can help people better manage the information used in their business; but tools—including TI computers—cannot replace sound judgment nor make the manager's business decision.

Consequently, TI cannot warrant that its systems are suitable for any specific customer application. The manager must rely on personal judgment of what is best for his or her business.

Preface

This manual contains the information necessary to install, program, and operate the Texas Instruments Models CI403 and CI404 Four-Channel Asynchronous Communications Interfaces in any Business Systems computer that has a TILINE* data bus. The information in this manual is organized into three major sections:

Section

1 General Description — Provides an overview of the purpose, features, and major components of the CI403 and CI404. It also contains information on cables, signals, and connector pin assignments.

2 Installation — Provides instructions for installing the CI403 or CI404 in TI computer chassis.

3 Programming — Provides the information necessary for an assembly language programmer to write programs to control operation of the CI403 or CI404.

The following documents contain helpful information related to the installation, troubleshooting, and repair of the CI403 and CI404:

Title	Part Number
9900 Family Systems Design and Data Book, Microprocessor Series, First Edition	97049-118-NI
Model 990/10 Computer System Hardware Reference Manual	945417-9701
Model 990/10A Computer Maintenance Manual, General Description	2302633-9701
Model 990/12 Computer Maintenance Manual, General Description	2268239-9701
Model 990/12 Computer Hardware User's Manual	2264446-9701
Model 990A13 Chassis Maintenance Manual, General Description	2308774-9701
Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide	943441-9701

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Title	Part Number
Model 990 Computer Unit Diagnostics Handbook, Volumes 1 Through 6	945400-9701 through 945400-9706
990 Family Communication Systems Field Reference Manual	2276579-9701
990 CRU/TILINE Expansion Installation and Operation Manual	2272075-9701
Model 990/12 Computer Assembly Language Programmer's Guide	2250077-9701
CI403 Family Tree Drawing	2230355-9901
CI404 Family Tree Drawing	2230358-9901
Four-Channel Asynchronous Communications Interfaces (CI403 and CI404) Maintenance Manual	2263898-9701
Technical Aspects of Data Communication by John E. McNamara, Digital Equipment Corporation	

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1

General Description

1.1 GENERAL

The Texas Instruments Four-Channel Asynchronous Communications Interfaces (CI403 and CI404) are TILINE slave devices that plug into a TI computer or expansion chassis backplane. The CI403 provides serial, half- or full-duplex, buffered, asynchronous data communications between the computer and as many as four external asynchronous devices. The CI403 allows TI computers with a TILINE bus to communicate with asynchronous modems, terminals, or other asynchronous devices compatible with the Electronic Industries Association (EIA) standard RS-232-C or the Consultative Committee on International Telephone and Telegraph (CCITT) recommendation V.24. The CI403 supports half- or full-duplex communications at speeds from 75 baud through 19.2 kilobaud (k baud) on each channel.

The CI404 is similar to the CI403 and provides the same capabilities as the CI403 with the exception that the interface between the CI404 and the external devices is a fiber-optic link and the CI404 does not support modems. The CI404 supports full-duplex (only) communications at speeds from 75 baud through 19.2 k baud on each channel.

The CI404 supports communications between TI computers with a TILINE bus and terminals with fiber-optic interfaces. It can also support terminals with EIA RS-232-C or CCITT V.24 compatible interfaces through use of an optical-to-EIA converter. The part number of the optical-to-EIA converter is included in Table 1-4 with the CI404 cables. Instructions for connecting the converter are included in Section 2.

NOTE

All references to the CI403 in this manual apply equally to both the CI403 and CI404 except where specifically indicated otherwise.

Figure 1-1 is a photograph of the CI403. Figure 1-2 is a photograph of the CI404.

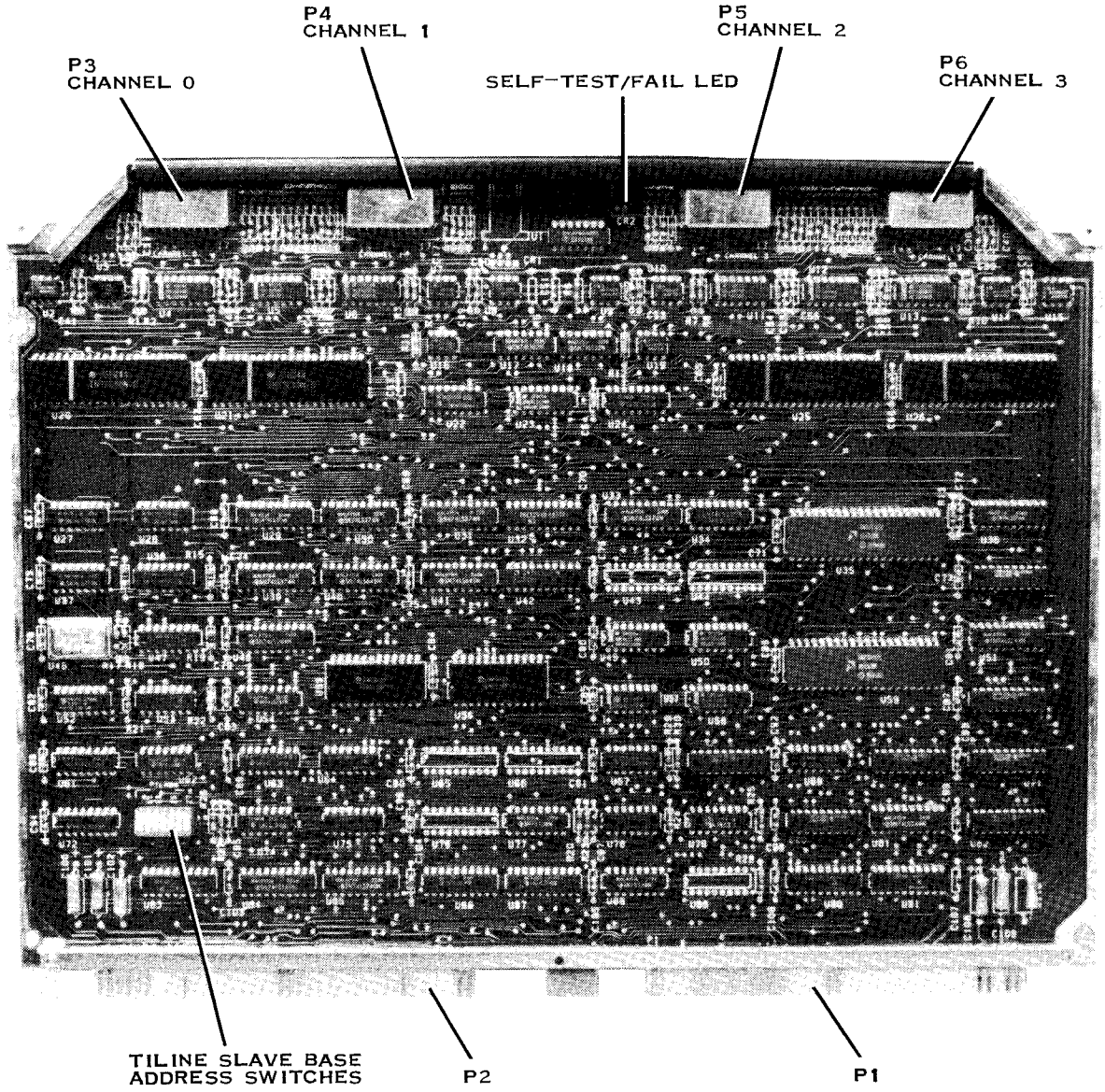


Figure 1-1. CI403 Four-Channel Asynchronous Communications Interface

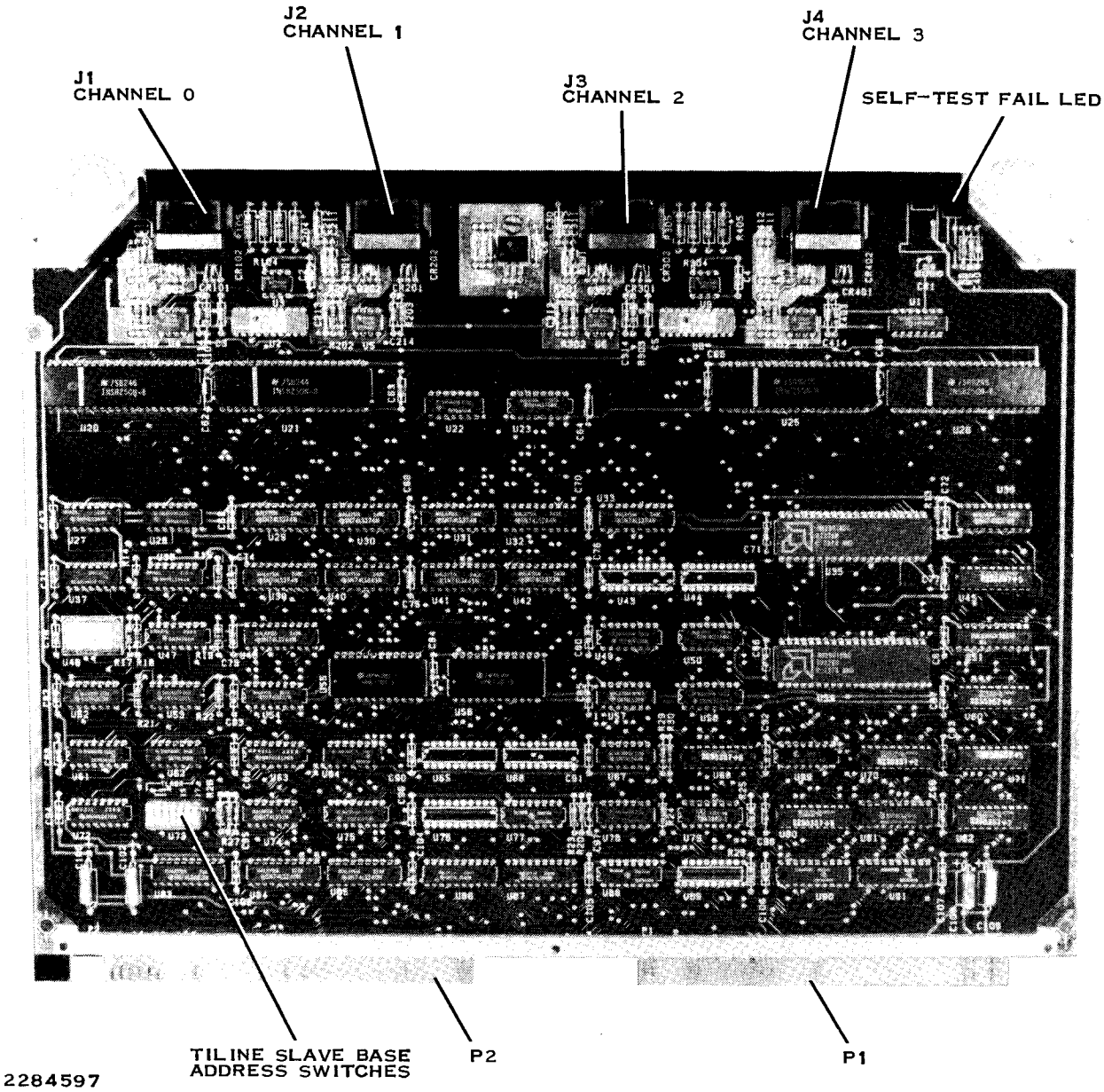


Figure 1-2. CI404 Four-Channel Asynchronous Communications Interface

CI403 features include:

- Single-board construction
- Four independent data communications channels
- Half- or full-duplex, asynchronous data transmission and reception (full-duplex only on the CI404)
- Fully buffered data transmission and reception
- All standard baud rates up to 19.2k baud
- Fully programmable serial interface characteristics:
  - — 5-, 6-, 7-, or 8-bit characters
  - — Even, odd, constant mark, constant space, or no parity bit generation
  - — 1, 1 1/2, or 2 stop bit generation
- Loopback test and self-test capability
- Full modem control and status signals (CI403 only)
- On-board self-test
- TILINE interface to host computer

The CI403 also has extensive electromagnetic interference (EMI) reduction features, including:

- Large power and ground buses in the power distribution matrix
- Extensive bypass capacitors
- Extensive decoupling of grounds
- A metal shield along the top edge of the printed wiring board (PWB)
- Shielded connectors (CI403 only)

1.2 KITS AND CABLES

Table 1-1 lists the components of the CI403 kit, TI part number 2230356-0001. Table 1-2 lists the components of the CI404 kit, TI part number 2230358-0001.

Table 1-1. CI403 Kit

Component Part Number	Item
2230350-0001	CI403 Four-Channel Asynchronous Communications Interface
2263897-9701	*Four-Channel Asynchronous Communications Interfaces (CI403 and CI404) Installation and Operation* manual
2303114-9901	CI403 System Test Procedure
2230355-9901	CI403 Family Tree

Table 1-2. CI404 Kit

Component Part Number	Item
2230360-0001	CI404 Four-Channel Asynchronous Communications Interface
2263897-9701	*Four-Channel Asynchronous Communications Interfaces (CI403 and CI404) Installation and Operation* manual
2230365-9901	CI404 System Test Procedure
2230358-9901	CI404 Family Tree

Table 1-3 lists the cables available for use with the CI403. Table 1-4 lists the cables available for use with the CI404. Table 1-4 also includes the part number of the optic-to-EIA converter kit that is required if you use the CI404 to interface EIA terminals.

Table 1-3. CI403 Cables

Part Number	Description
2303070-0002	CI403 to external modem, 9.1 m (30 ft)
2303070-0003	CI403 to external modem, 3.0 m (10 ft)
2303071-0002	EIA extension cable, 15 m (49.2 ft)
2303071-0004	EIA extension cable, 60 m (196.8 ft)
2303077-0001*	CI403 to EIA terminal, 9.1 m (30 ft)
2303080-0001	CI403 to 810, 850, 855, and 880 printers, 9.1 m (30 ft)
2308661-0001	CI403 to letter quality printer, 9.1 m (30 ft)

Note:

*This cable mates with terminals and printers that have a 25-pin D-type EIA connector, including models 780, 820, 840, and 940.

Table 1-4. CI404 Cables

Part Number	Description
2233200-0001	Standard duplex fiber-optic cable, 15 m (49.2 ft)
2233201-0002	Fiber-optic extension cable, 60 m (196.8 ft)
2233201-0003	Fiber-optic extension cable, 150 m (492.1 ft)
2233201-0004	Fiber-optic extension cable, 300 m (984.2 ft)
2233210-0001	Converter module kit, includes: • Converter • Power module • Power cord, 2.4 m (8 ft)

Notes:

Each fiber optic extension cable includes a connector that can be used to connect two fiber-optic cables.

The maximum recommended length of fiber-optic cable between the CI404 and a terminal is 1000 m (3281 ft) with no more than one splice.

Contractual maintenance and installation of all cables in excess of 15 meters (49.2 feet) is the responsibility of the customer. TI will replace these cables if they become defective during the warranty period but it is the responsibility of the user to install them.

1.3 PHYSICAL DESCRIPTION

The CI403 is implemented on a full-size 990 PWB, which occupies one full slot in the computer mainframe or in an expansion chassis. The CI403 PWB is 362 mm (14.25 in) wide and 274.3 mm (10.8 in) high. Bottom edge connectors P1 and P2 are both 80-pin connectors that provide the interface between the CI403 and the host computer TILINE bus. The CI403 has four 18-pin (AMP 102792-2) connectors (P3 through P6) on the top of the board that provide RS-232-C compatible interfaces to external devices. The CI404 has four fiber-optic connectors (P3 through P6) on the top of the board that provide fiber-optic interfaces to external devices.

1.4 HARDWARE FUNCTIONAL DESCRIPTION

The host computer TILINE bus connects the CI403 to the central processing unit (CPU) of the host computer. As shown in Figure 1-3, the CI403 interfaces directly between the TILINE bus and external RS-232-C devices (CI403) and fiber-optic devices (CI404). The TILINE bus is a high-speed, asynchronous, 16-bit parallel data bus that transfers data between high-speed system elements such as main memory, the CPU, and mass data storage systems. Using the TILINE, the CPU handles all control, select, status, and data communications between the host computer and the CI403.

Four TILINE memory locations are assigned to the CI403. The CPU communicates with the CI403 by writing words to and reading words from these four memory locations.

1.4.1 Typical Operation

The CPU initiates operation by writing control information into the TILINE memory locations reserved for the CI403. The control information directs the CI403 to operate in a particular configuration and to transmit and receive data on specified channels. The control information includes parameters such as the channel number, the baud rate, the number of stop bits, and parity characteristics. Once the control parameters are established, the CPU transmits and receives data by writing words to and reading words from the four memory locations reserved for the CI403. Transmit data words contain the channel number and data; received data words contain the channel number, data, and status. All four channels of the CI403 can operate simultaneously by intermixing data transmissions and receptions, since each data word includes the channel number.

1.4.2 CI403 Functional Components

As shown in Figure 1-4, the CI403 functionally consists of:

- A 256-word TILINE transmit first-in, first-out (FIFO) buffer common to all four channels
- A 256-word receive FIFO buffer common to all four channels
- One 128-byte transmit FIFO buffer for each channel
- One asynchronous communications element (ACE) for each channel
- One set of RS-232-C drivers/receivers for each channel on the CI403
- One set of fiber-optic drivers/receivers for each channel on the CI404
- A microprocessor with on-board permanent programs

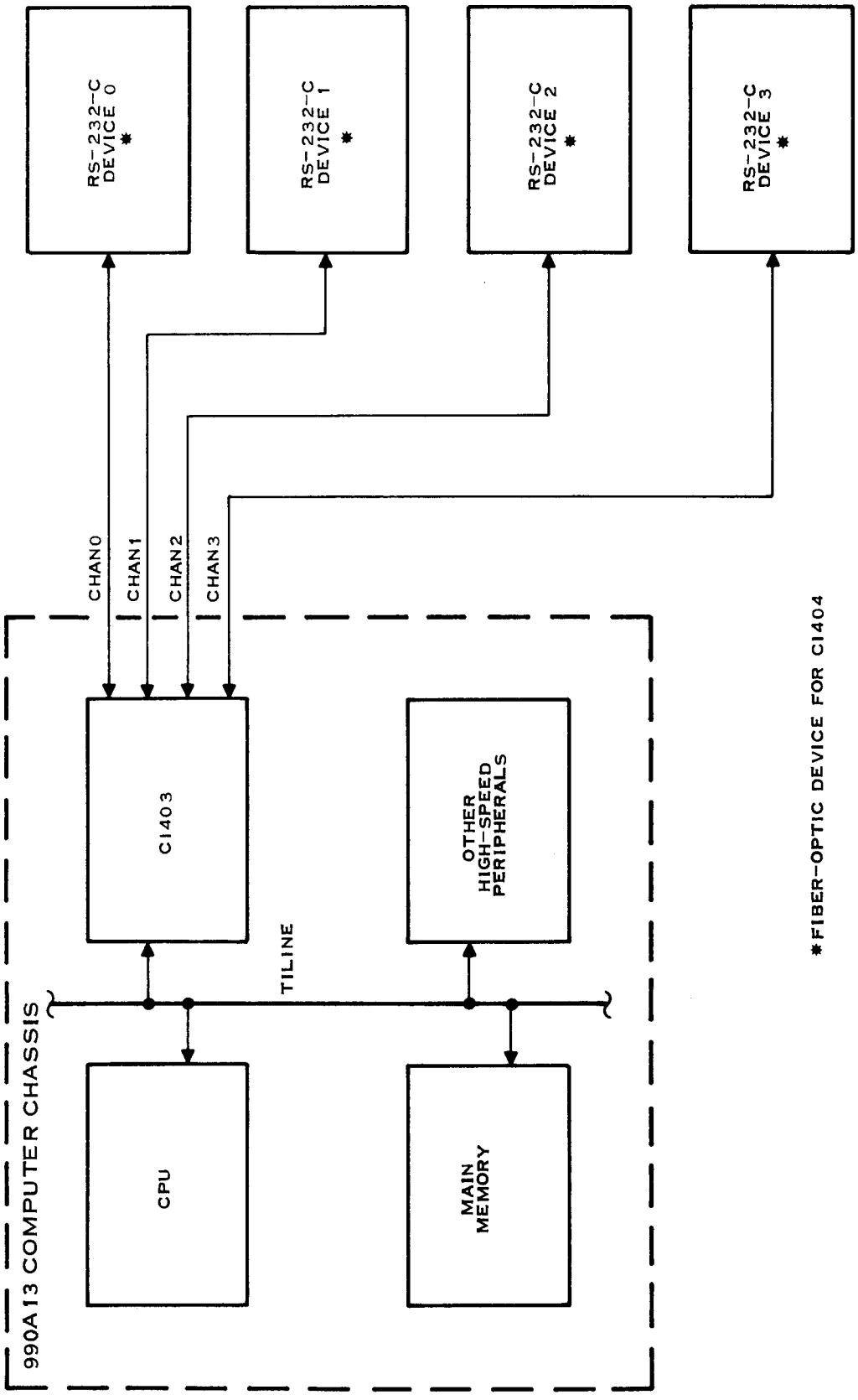


Figure 1-3. CI403 System Block Diagram

The following paragraphs describe these elements.

1.4.2.1 First-In, First-Out (FIFO) Buffers. The CI403 buffers all data transmissions and receptions with on-board FIFOs that allow transfers between the TILINE bus and the external devices to occur at different data rates. Buffering is necessary since it is impossible to predict either the rate that characters are transferred over the TILINE bus or the rate that characters are transmitted and received through the external communications devices.

A FIFO is a block of memory locations with an input and an output. Words are written into and fetched from the FIFO, one at a time. When the first word is entered into an empty FIFO, it immediately appears at the output. Additional words entered into the FIFO are stacked at the output in the order of entry. Once a word is read from the FIFO, the next word in sequence appears at the output. Thus, writing data into the FIFO and reading data from it are two independent operations and can take place at different rates. The writing and reading operations can continue as long as the FIFO does not overflow, which occurs only when the input rate exceeds the output rate for an extended period.

As shown in Figure 1-4, a 256-word TILINE transmit FIFO and a 256-word receive FIFO are common to all four channels on the board. Additionally, each channel has a separate 128-byte transmit FIFO. The CPU routes data words over the TILINE bus to the CI403 for transmission and places them in the 256-word TILINE transmit FIFO. Each transmit data word consists of one byte that identifies the transmit channel and one byte of transmit data. The control logic on the CI403 examines each transmit word to determine the proper transmit channel, and then transfers the 8-bit data character portion of the word (from the 256-word TILINE transmit FIFO) into the 128-byte transmit FIFO associated with the appropriate transmit channel. The control logic discards the channel identifier portion of the word after it determines in which channel transmit FIFO to place the data. Transmit data words from the CPU can be intermixed since the CI403 examines each word and routes the data portion to the proper channel for transmission.

The CI403 control logic notifies the host when the 256-word TILINE transmit FIFO is more than 75 percent full; however, this condition should not occur in normal operation. The host software must be designed to prevent overflow of the 128-byte channel transmit FIFOs, since the CI403 control logic does not notify the host of impending overflow of these FIFOs.

The CI403 control logic adds a byte containing channel identification and status information to each received data character and then places the word in the 256-word TILINE receive FIFO. The received data remains in the 256-word TILINE receive FIFO until it is read by the host over the TILINE bus. The host software determines which channel the received data came from by examining the portion of the word that contains the channel identifier.

1.4.2.2 Asynchronous Communications Elements (ACEs). Each ACE is a self-contained, single-chip integrated circuit that can be programmed for a wide variety of transmit and receive configurations. It performs serial-to-parallel conversions on data characters received from external terminals or modems, and parallel-to-serial conversions on outgoing data characters before they are transmitted to external terminals or modems. The ACE generates all handshaking signals necessary to perform data transfers with external modems and terminals. The CI403 control logic reads ACE status, which includes the type and condition of the transfer operations performed by the ACE and any error conditions that arise. Each ACE contains an internal baud rate generator that provides common timing signals for the transmitter and receiver logic. The ACEs also contain complete modem control logic for controlling external modems.

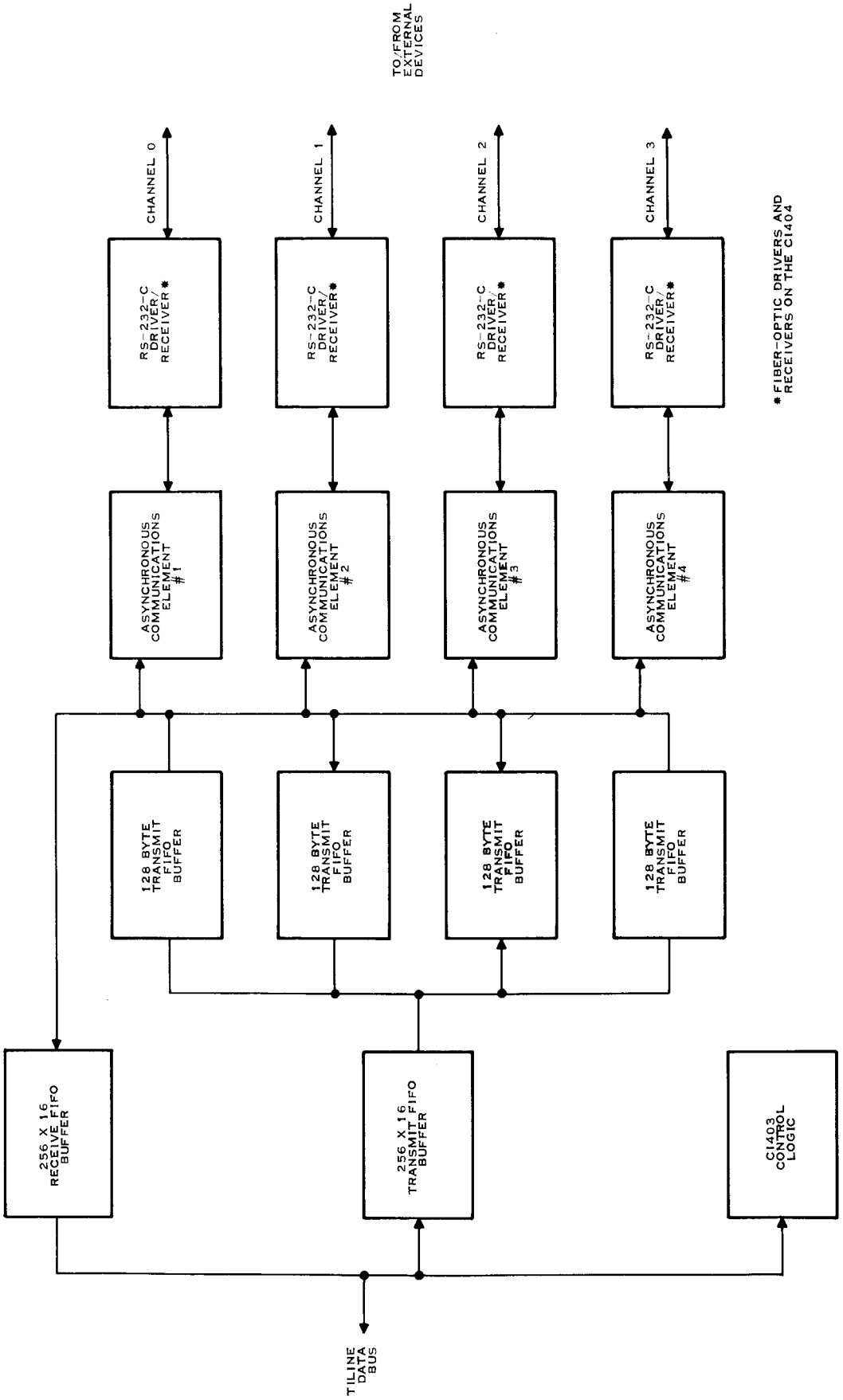


Figure 1-4. CI403 Simplified Functional Block Diagram

1.4.2.3 CI403 Control Logic. The CI403 control logic consists of an internal bus that connects an 8-bit microprocessor, a 2048-word by 16-bit random-access memory (RAM), and a 256-word by 56-bit programmable read-only memory (PROM). The PROM contains a firmware program that controls all aspects of CI403 operation. The following paragraphs describe each of these major components of the CI403 control logic.

Microprocessor. Due to pin number restrictions and other construction constraints, it is sometimes desirable to build microprocessors in several packages, where each package contains a section of a complete microprocessor. The packages can be wired together to form a large microprocessor, called a bit-slice processor, since each package processes a limited number of bits of information. The CI403 uses two processor packages wired to form an eight-bit microprocessor.

The microprocessor contains its own internal registers, arithmetic logic unit (ALU), input buffers, output buffers, and shift registers. It can add, subtract, complement, shift, store, mask, test conditions, and perform all logical operations required by the firmware.

Programmable Read-Only Memory (PROM). The 256-word by 56-bit PROM contains the program routines and subroutines that control all internal operations of the CI403. The program is permanently programmed into the ROM integrated circuits, and is called a microprogram or microcode. A microassembler helps generate the microprogram.

Random-Access Memory (RAM). The RAM stores control words received from the CPU and stores intermediate values during processor calculations. The processor manipulates the RAM to create the FIFOs that store transmit and receive characters. Although FIFOs are sometimes specially built for this purpose, the RAM performs the same function when under microprocessor control.

1.4.2.4 CI403 RS-232-C Drivers/Receivers. This paragraph applies only to the CI403. The RS-232-C driver and receiver circuits on the CI403 perform the conversion between transistor-transistor logic (TTL) levels used internally on the CI403, and the RS-232-C voltages required at interface connectors P3 through P6. The conversion process includes incoming and outgoing data and the control signals required for control of external modems or terminals.

1.4.2.5 CI404 Fiber-Optic Drivers/Receivers. This paragraph applies only to the CI404. The driver circuits on the CI404 convert outgoing data from TTL levels to optical signals (light flashes). The receiver circuits convert incoming optical signals to TTL logic levels. The conversion process includes only incoming and outgoing data signals; the CI404 does not provide external modem or terminal control signals.

1.5 CI403 INTERFACES

The left side of Figure 1-5 shows the signals that comprise the interface between the host computer TILINE bus and the CI403. The CI403 and CI404 are identical at this interface. The right side of Figure 1-5 shows the interface signals between the CI403 and supported modems or other devices compatible with EIA standard RS-232-C or CCITT recommendation V.24. The CI404 interface to external fiber-optic terminals consists of only the optical transmit and receive data signals for each of the four channels; no control signals are involved. The following paragraphs provide details of these interfaces and define the use of the signals.

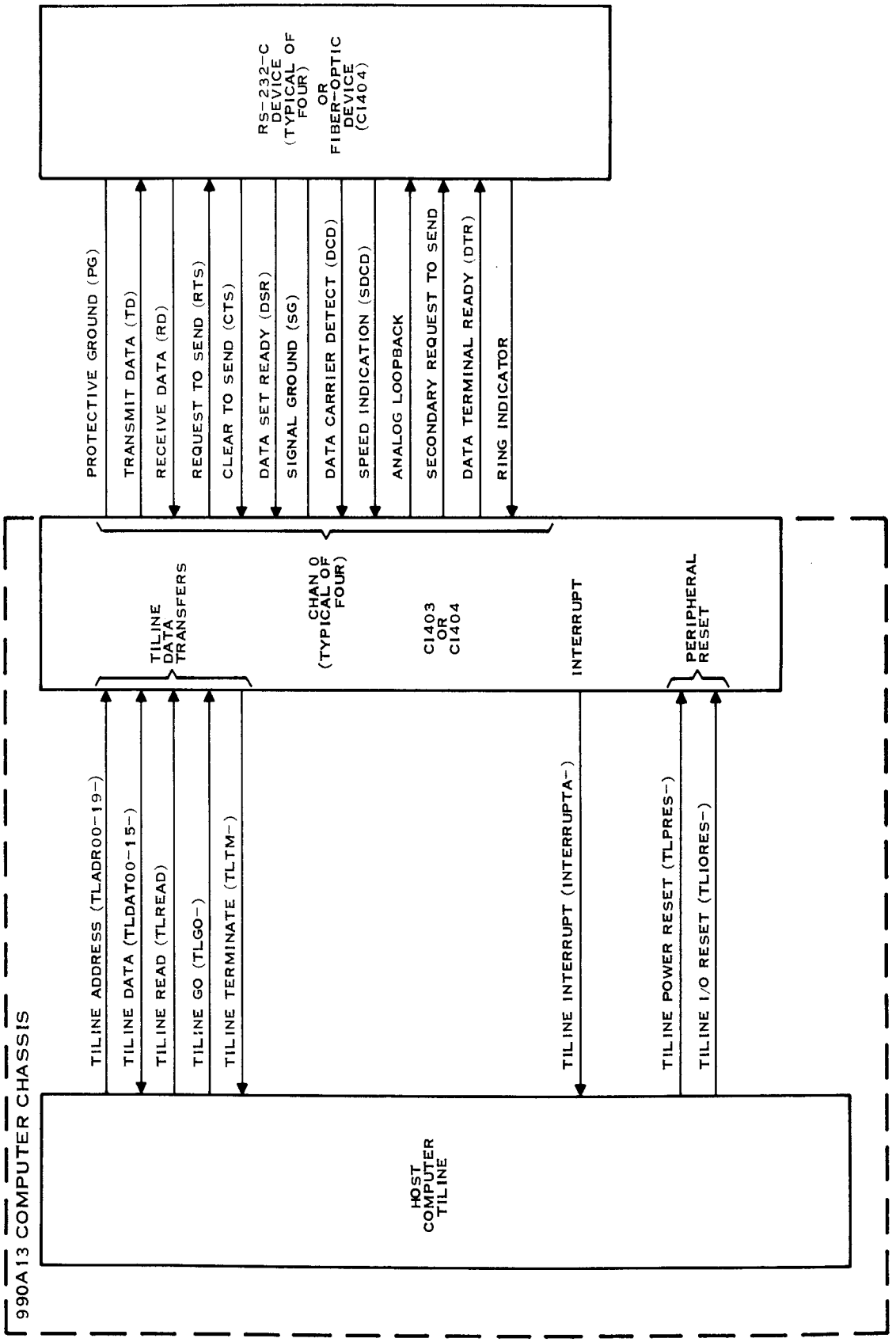


Figure 1-5. CI403 Interface Signals

1.5.1 CI403 to Host Computer TILINE Interface

When the CI403 is installed in the host computer chassis, it obtains power and shares access to the host computer TILINE bus with other TILINE-controlled devices. Section 2 includes instructions for installing the CI403 in the computer chassis and configuring the interrupts and address switches. Table 1-5 lists the connector pin assignments for TILINE connector P1; Table 1-6 lists the connector pin assignments for TILINE connector P2. Table 1-7 lists the functions of each of the TILINE interface signals used by the CI403. Several of the TILINE interface signals in connectors P1 and P2 are used only by TILINE master devices and are not included in Table 1-7.

Table 1-5. TILINE Connector P1 Pin Assignments

Pin	Function	Pin	Function
1,2	Ground	43-45	Open
3,4	+ 5 V main power	46	MODSELB –
5,6	+ 12 V memory power	47	Open
7,8	+ 5 V memory power	48	MODSELA –
9,10	– 5 V memory power	49	Open
11	TLREAD	50	CRUBIT7
12	Ground	51	Open
13	TLPRES –	52	CRUBIT6
14	TLIORES –	53	Open
15	Ground	54	CRUBIT5
16	TLPFWP –	55	TLMER –
17	Ground	56	CRUBIT4
18	CRUBITOUT	57	Ground
19	Ground	58	TLAV
20	TLTM –	59	Ground
21	Ground	60	CRUBITIN
22	STORECLK –	61	Open
23	Open	62	CRUBIT8
24	Ground	63	TLWAIT –
25	TLGO –	64	CRUBIT9
26	Ground	65	Open
27	TLDAT12 –	66	INTP1A –
28	TLDAT13 –	67	Open
29	120HZ	68	CRUBIT10
30	TLDAT14 –	69	Open
31	TLDAT15 –	70	CRUBIT11
32	CRUBIT13	71	TLAK –
33	Open	72	Ground
34	CRUBIT15	73	Open
35	Open	74	Ground
36	CRUBIT12	75	Open
37	Open	76	Open
38	CRUBIT14	77,78	+ 5 V main power
39,40	+ 12 V main power	79,80	Ground
41,42	– 12 V main power		

Table 1-6. TILINE Connector P2 Pin Assignments

Pin	Function	Pin	Function
1,2	Ground	43	TLDAT06 –
3,4	+ 5 V main power	44	TLADR01 –
5	TLAG(Out)	45	TLDAT07 –
6	TLAG(In)	46	MODSELB –
7	Ground	47	TLADR06 –
8	TLADR14 –	48	MODSELA –
9	TLADR15 –	49	TLADR07 –
10	TLADR10 –	50	Open
11	TLADR12 –	51	TLADR02 –
12	TLADR11 –	52	Open
13	TLPRES –	53	TLADR03 –
14	TLIORES –	54	Open
15	TLADR13 –	55	TLADR00 –
16	TLPFWP –	56	Open
17	TLADR08 –	57	TLADR04 –
18	CRUBITOUT	58	Ground
19	TLADR09 –	59	TLADR05 –
20	TLDAT11 –	60	CRUBITIN
21	TLDAT08 –	61	TLDAT04 –
22	STORECLK –	62	Open
23	TLDAT10 –	63	TLDAT05 –
24	Ground	64	Open
25	TLADR18 –	65	Open
26	TLHOLD –	66	INTP2A –
27	TLADR17 –	67	TLDAT00 –
28	Open	68	Open
29	TLADR16 –	69	TLDAT01 –
30	Ground	70	Open
31	TLADR19 –	71,72	– 5 V memory power
32	CRUBIT13	73,74	+ 5 V memory power
33	TLDAT09 –	75,76	+ 1 V memory power
34	CRUBIT15	77,78	+ 5 V main power
35	TLDAT02 –	79,80	Ground
36	CRUBIT12		
37	TLDAT03 –		
38	CRUBIT14		
39,40	+ 12 V main power		
41,42	– 12 V main power		

Note:

Pins 5 and 6 in P2 are connected together on the CI403 to allow the TILINE access-granted signal (TLAG) to pass uninterrupted to other TILINE controllers.

Table 1-7. TILINE Interface Signal Definitions

Designation	Pin No.	Definition
TLGO –	P1-25	TILINE Go. This signal initiates all data transfers when the transition from high (> 3.0 V) to low (< 1.0 V) occurs.
TLREAD	P1-11	TILINE Read. When this signal is high (> 3.0 V), it designates a read from slave operation; when it is low (< 1.0 V), it designates a write to slave operation.
TLADR00 –	P2-55	TILINE Address. This signal defines the location of data during a fetch or store operation. When it is high (> 2.0 V), the corresponding address bit is 0; when it is low (< 0.8 V), the corresponding address bit is 1.
TLADR01 –	P2-44	
TLADR02 –	P2-51	
TLADR03 –	P2-53	
TLADR04 –	P2-57	
TLADR05 –	P2-59	
TLADR06 –	P2-47	
TLADR07 –	P2-49	
TLADR08 –	P2-17	
TLADR09 –	P2-19	
TLADR10 –	P2-10	
TLADR11 –	P2-12	
TLADR12 –	P2-11	
TLADR13 –	P2-15	
TLADR14 –	P2-8	
TLADR15 –	P2-9	
TLADR16 –	P2-29	
TLADR17 –	P2-27	
TLADR18 –	P2-25	
TLADR19 –	P2-31	
TLDAT00 –	P2-67	TILINE Data. This bidirectional signal defines data on the TILINE. When it is high (> 2.0 V), the corresponding data bit is 0; when it is low (< 0.8 V), the corresponding data bit is 1.
TLDAT01 –	P2-69	
TLDAT02 –	P2-35	
TLDAT03 –	P2-37	
TLDAT04 –	P2-61	
TLDAT05 –	P2-63	
TLDAT06 –	P2-43	
TLDAT07 –	P2-45	
TLDAT08 –	P2-21	
TLDAT09 –	P2-33	
TLDAT10 –	P2-23	
TLDAT11 –	P2-20	
TLDAT12 –	P1-27	
TLDAT13 –	P1-28	
TLDAT14 –	P1-30	
TLDAT15 –	P1-31	
TLTM –	P1-20	TILINE Terminate. When this signal is low (< 1.0 V), it indicates that a slave device has completed the requested operation.

Table 1-7. TILINE Interface Signal Definitions (Continued)

Designation	Pin No.	Definition
TLIORES –	P1-14	TILINE I/O Reset. A normally high (> 2.0 V) signal that, when low (< 1.0 V), halts and resets all TILINE I/O devices. This signal is a 100- to 500-nanosecond pulse generated by the reset switch on the control console or by the execution of a CPU reset instruction.
TLPRES –	P1-13	TILINE Power Reset. A normally high (> 2.0 V) signal that goes low (< 1.0 V) at least 10 microseconds before dc voltages begin to fail during power-down, and remains low until dc voltages stabilize during power-up.
INTP2A –	P2-66	External Interrupt. Interrupt from the CI403 to the host computer.

1.5.2 CI403 to Communications Device Interface

This paragraph and Tables 1-8 and 1-9 apply only to the CI403. The interface signals at connectors P3 through P6 conform to the requirements of EIA standard RS-232-C and CCITT recommendation V.24. Important characteristics of the EIA standard include the following:

- The receiver circuit can withstand ± 25 volts.
- The drivers are limited to ± 6 volts.
- A positive voltage greater than + 3 volts equals binary zero, signal space, or control on.
- A voltage more negative than – 3 volts equals binary one, signal mark, or control off.

Table 1-8 lists the connector pin assignments and the signal functions for CI403 connectors P3 through P6. It includes pin assignments for data circuit terminating equipment (DCE), such as a modem, that conforms to EIA standard RS-232-C or CCITT recommendation V.24. Table 1-8 also lists EIA and CCITT designations for equivalent circuit functions where they exist.

Table 1-8. EIA Interface Connector (P3 Through P6) Pin Assignments

P3 Through P6 Pin Number	Modem Pin Number	CCITT	EIA	Function
Backshell	1	101	AA	Protective ground
1	2	103	BA	Transmit data
2	3	104	BB	Receive data
3	4	104	BB	Request to send
4	5	106	CB	Clear to send
5	6	107	CC	Data set ready
16	7	102	AB	Signal ground
6	8	109	CF	Data carrier detect
N/C	9			Reserved
N/C	10			Reserved
N/C	11			Reserved
8	12	122	CI	Speed indication
15	13			Analog loopback
9	14			Reserved
10	15			Reserved
N/C	16			Reserved
11	17			Reserved
N/C	18			Reserved
7	19	120	SCA	Secondary request to send
12	20	108.2	CD	Data terminal ready
N/C	21			Reserved
13	22	125	CE	Ring indicator
18	23			Spare
14	24			Reserved
N/C	25			Reserved
17	N/C			RS-232-C key

Note:

N/C means this pin is not connected.

Table 1-9 presents detailed descriptions of the interface signals at CI403 connectors P3 through P6 and indicates the direction of information flow where it is applicable. The data terminal equipment (DTE) includes the host computer and the CI403; the DCE is the modem or, if no modem is involved, the peripheral device with which the host computer communicates.

Table 1-9. EIA Interface Signal Descriptions

Signal Name	P3 Through P6 Pin Number	Function
Protective Ground	Backshell	Connects to the connector backshell on systems that require a protective ground.
Transmit Data C1403 to DCE	1	The CI403 generates the signals on this circuit and transfers them to the DCE for transmission to the remote data terminal. This circuit is held in the marking condition during intervals between characters and when no data is being transmitted. The CI403 requires only CTS in the on condition to transmit data; however, the modem requires the following four signals to be on before data is transmitted: • Request to send (CA) • Clear to send (CB) • Data set ready (CC) • Data terminal ready (CD)
Receive Data DCE to CI403	2	The DCE generates the signals on this circuit in response to data signals received from the remote terminal. This circuit is held in the marking condition when the signal data carrier detect (CF) is off. On a half-duplex channel, the controller holds this circuit in the marking condition when circuit request to send (CA) is on and for a brief interval following the on-to-off transition of request to send (CA).
Request to Send CI403 to DCE	3	This circuit conditions the DCE for data transmission. On a half-duplex circuit, it controls the direction of data transmission. An off-to-on transition instructs the DCE to enter the transmit mode. The DCE responds by turning on the transmitter and transmitting a mark condition for a preset interval. Then, it turns on clear to send (CB), indicating that data can be transferred to the DCE on the transmit data (BA) circuit. The on-to-off transition of this circuit instructs the DCE to complete transmission and turn the transmitter off. An asynchronous modem with soft-carrier turnoff selected transmits an out-of-band tone (900 Hz for a 202 modem) for a preset time interval and then turns the transmitter off.

Table 1-9. EIA Interface Signal Descriptions (Continued)

Signal Name	P3 Through P6 Pin Number	Function
Clear to Send DCE to CI403	4	The on condition of this circuit indicates that the DCE is ready to transmit data received on circuit transmit data (BA). The on-to-off and off-to-on transitions of this circuit are in response to transitions on circuit request to send (CA).
Data Set Ready DCE to CI403	5	The on condition of this circuit informs the CI403 that the DCE is connected to a data channel and all control circuits are valid. The on condition of this circuit indicates the following conditions exist: • The local modem is connected to a data channel (off-hook in switched service). • The local modem is not in talk or dial mode. • The local modem has completed any timing functions required by the switched system to complete call establishment. This circuit is in the off condition at all other times, indicating to the CI403 that all signals other than ring indicator (CE) should be disregarded.
Data Carrier Detect DCE to CI403	6	The on condition of this circuit indicates that the DCE is receiving a signal that meets its suitability criteria and that receive data (BB) is valid. The off condition indicates that the DCE is not receiving a signal from the remote terminal or the received signal is not suitable for demodulation. On half-duplex channels, this signal is held in the off condition whenever request to send (CA) is on and for a brief interval after the on-to-off transition of request to send. In the CI404, the on condition of DCD indicates that the FSK modem has detected an optical carrier signal.
Secondary Request to Send CI403 TO DCE	7	The on condition of this signal requests the modem to transmit a tone on the secondary channel (also called the reverse channel, supervisory channel, or backward channel). This signal can be used as a general purpose input for special applications.

Table 1-9. EIA Interface Signal Descriptions (Continued)

Signal Name	P3 Through P6 Pin Number	Function
Speed Mode Indication DCE to CI403	8	Dual-speed modems use this signal to indicate which speed is active. The on condition indicates that the modem is in the high-speed mode. This signal can be used as a general purpose input for special applications.
Data Terminal Ready CI403 to DCE	12	Signals on this circuit control switching the DCE to the communication channel. The on condition prepares the DCE to be connected to the communication channel and maintains the connection established by external means, such as manual call origination, manual answering, or automatic call origination. TI internal modems and most external modems automatically answer an incoming call if circuit data terminal ready (CD) is on and a ringing signal is detected. The off condition of circuit data terminal ready (CD) causes the DCE to be disconnected from the communication channel. In switched network applications, after circuit data terminal ready (CD) is turned off, it is not turned on again until circuit data set ready (CC) is turned off by the DCE. In the CI404, the on condition of DTR turns on the fiber-optic carrier.
Ring Indicator DCE to CI403	13	The on condition of this circuit indicates reception of a ringing signal on the communication channel. The on condition is approximately coincident with the on segment of the ringing signal.

Table 1-9. EIA Interface Signal Descriptions (Continued)

Signal Name	P3 Through P6 Pin Number	Function
Analog Loopback CI403 to DCE	15	The on condition of this circuit instructs compatible modems to disconnect from the telephone network and connect the transmitter output to the receiver input. On TI internal modems, all interface circuits except data set ready (CC) operate as in normal full-duplex mode. Data set ready is forced off while the modem is in analog loopback. This circuit allows the host computer to exercise the CI403 and the local modem in a local test mode. The off condition of this circuit returns the modem to normal operation. This signal can be used as a general purpose output for special applications.
Signal Ground	16	This signal establishes the signal common reference potential for unbalanced signals between the CI403 and the DCE.
Keying Pin	17	This pin keys an RS-232-C cable to CI403 connectors P3 through P6.
Spare	18	Pin 18 is a spare.

1.5.3 CI404 to Communications Device Interface

This paragraph and Table 1-10 apply only to the CI404. The CI404 interfaces directly to compatible TI fiber-optic devices through four connectors (TI part number 2221056-0001) mounted at the top of the board. Devices equipped with TI fiber-optic interfaces can be connected directly by using either TI Duplex Fiber-Optic cable, part number 2233200, or TI Duplex Fiber-Optic extension cable, part number 2233201.

The interface between the CI404 and the external device consists of only the optical transmit and receive data signals for the four channels on the CI404. Table 1-10 lists the pin assignments in CI404 connectors J1 through J4 for these signals.

Standard EIA RS-232-C terminals can connect to the CI404 with the Fiber-Optic to EIA Converter Assembly, provided the terminals do not use modem control signals other than DCD (received line signal detect (RLSD)) and DTR. DCD (RLSD) indicates that the remote device is ready to receive data, and DTR indicates that the CI404 is ready to receive data and/or is transmitting data. Modem control lines other than DCD (RLSD) and DTR are not included in the interface, thus standard communications line interface modems cannot be remotely supported.

Table 1-10. CI404 Interface Connector (J1 Through J4) Pin Assignments

J1 Through J4 Pin Number	Signal Function
1	Optical Transmit Data
2	Optical Receive Data

2

Installation

2.1 GENERAL

This section describes how to unpack, install, and perform initial checkout of the CI403. It also includes power and environmental requirements of the board to aid in planning the installation.

NOTE

All references to the CI403 in this section apply to both the CI403 and the CI404 except where specific differences are pointed out.

This section also includes illustrations and descriptions of the CI403 in typical applications, including the part numbers of the cables required for each configuration. The last part of this section describes the recommended method of checking the CI403 for proper operation after you complete the installation.

2.2 UNPACKING AND INSPECTION

The CI403 is shipped either as a kit (TI part number 2230356-0001 for the CI403, TI part number 2230359-0001 for the CI404) or as a part of a system where it is already installed in a Business System Series 600 or 800 computer. If the CI403 is already installed in a computer, use the unpacking and inspection instructions in the *Model 990A13 Chassis Maintenance Manual, General Description*, TI part number 2308774-9701.

The CI403 and CI404 kits are shipped in cardboard containers. The circuit boards are placed in a conductive bag, wrapped in bubble-pack, and sealed to a piece of rigid cardboard. Unpack the kit and inspect it as follows:

CAUTION

The CI403 and CI404 are susceptible to damage from electrostatic discharge once they are removed from their protective packaging. Ensure that you are well grounded before removing the circuit boards from their protective packaging. The recommended grounding method is to use a wrist strap, in contact with the skin, connected to ground. If you do not have a wrist strap available, touch a grounded object to discharge any accumulated static charge before unpacking the board. Unpack the board on a grounded work surface. Place the board back in the protective bag to transport or store it.

1. Before unpacking the cardboard container, inspect it for evidence of damage, such as crumpled corners, tears, water stains, and so forth.

2. Open the cardboard container and remove the circuit board container.

3. Ensure that you are grounded or have touched a ground, then remove the board from its protective package. Verify that the part number matches the number listed in Table 1-1 (CI403) or Table 1-2 (CI404).

4. Inspect the board for any cracks, loose or damaged components, or loose material lodged between components that could cause a short circuit.

5. If you ordered any optional cables or parts, verify that their part numbers match those on the shipping list and inspect them carefully for damage.

2.3 PLANNING

The CI403 board requires one full-slot location in the computer chassis. The power requirements for the board are as follows:

Power	CI403	CI404
+5 ± 0.25 Vdc	3.0 amperes	3.0 amperes
+12 ± 0.60 Vdc	0.3 amperes	0.1 amperes
−12 ± 0.72 Vdc	0.3 amperes	N/A

Table 2-1 lists the environmental requirements of the CI403. Verify that the characteristics of the board are compatible with the planned environment.

Table 2-1. CI403 Environmental Requirements

Parameter	Range
Operating temperature	0° C to 65° C (32° F to 149° F)
Shipping temperature	−40° C to 70° C (−40° F to 158° F)
Humidity (operating)	5% to 95% noncondensing
Humidity (nonoperating)	0% to 95%
Altitude	0 m to +3049 m (0 to 10,000 ft)
Shock (operating)	1 g
Shock (shipping)	15 g to shipping container
Vibration (operating)	1 g, 5 to 80 Hz; 0.3 g, 80 to 500 Hz

2.4 INSTALLATION

The following instructions for installing the CI403 apply when the board is packaged and shipped separately from the host computer.

Before installing the CI403 in the host computer, you must do the following:

- Select a suitable chassis slot.
- Ensure that the interrupt level jumpers or switches in the computer chassis are configured to allow proper interrupt processing between the software in the host computer and the CI403.
- Set the CI403 TILINE base address switches.
- Inform the system software of the TILINE base address and interrupt level assigned to the CI403. This is usually done by regenerating the system. You can perform this step after you install the board in the chassis.

The following paragraphs explain how to accomplish these tasks.

CAUTION

Always turn off power to the computer when installing or removing any circuit board from the chassis to prevent damage to the computer or to the board.

2.4.1 Selecting a Chassis Slot for the CI403

You can install the CI403 in any available location in the host computer chassis or in a TILINE expansion chassis.

2.4.2 Interrupt Connections

Interrupt connections required to interface peripheral equipment to a Business System Series computer usually are made before the system is delivered to the customer. These interrupt assignments are coordinated with the software supplied with the system so that the software can communicate with and control the peripheral device. If you purchase the CI403 as a kit, you must modify the interrupt connections as part of the board installation.

The method of modifying interrupts varies with the chassis in which you install the CI403. You can install the CI403 in a 6-slot, 13-slot, or 17-slot chassis used with earlier Texas Instruments computer systems or in the 13-slot 990A13 chassis introduced in mid-1982 for the Business System 600 and 800 series computers. TI ships a manual describing how to modify interrupts for installation of boards with each of the different chassis. The following describes which manual you should use:

- If you are installing the CI403 in a 6-slot or 13-slot chassis, refer to the *Model 990/10 Computer System Hardware Reference Manual.*
- If you are installing the CI403 in a 17-slot chassis, refer to the *Model 990/12 Computer Hardware User's Manual.*
- If you are installing the CI403 in a 990A13 chassis, refer to the *Model 990A13 Chassis Maintenance Manual, General Description.*

You can find the part numbers of the referenced manuals in the Preface.

NOTE

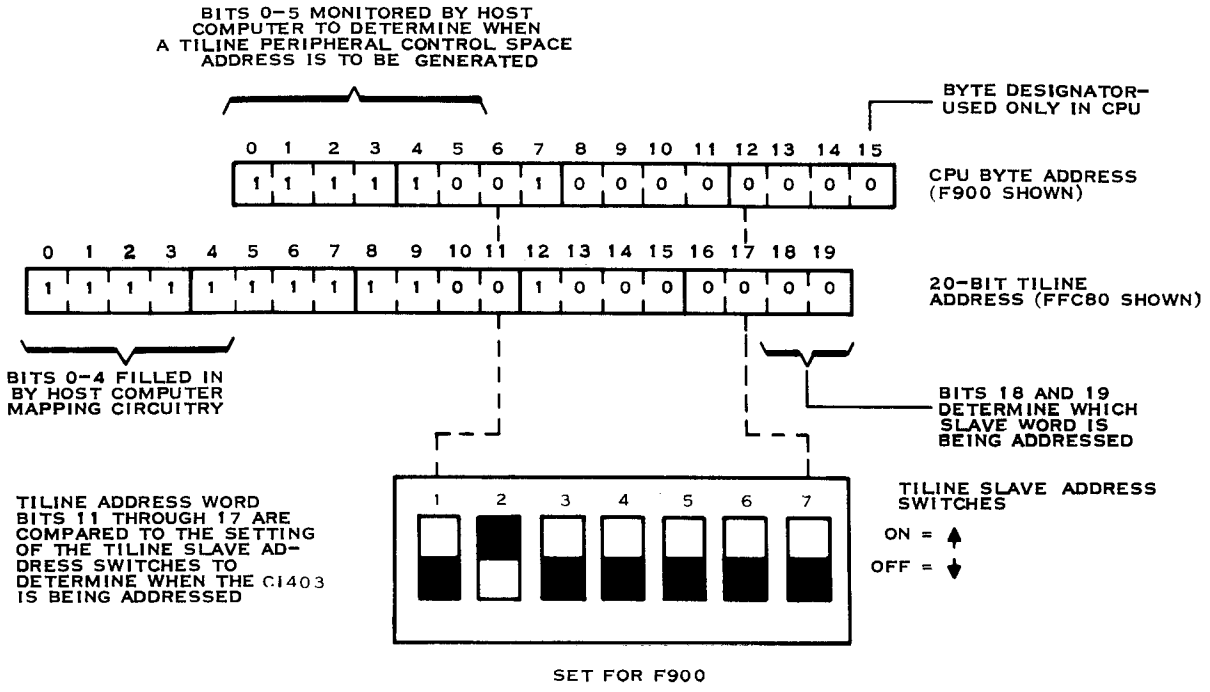
When you install the CI403 in a TILINE expansion chassis, in a system that uses the DX10 or DNOS operating system, you must use the TILINE interrupt (not the CRU interrupts) in the chassis. If you install several CI403s in one TILINE expansion chassis, they must share a TILINE interrupt. You will need the custom interrupt PC board to connect several TILINE controllers to one interrupt. Refer to the *990 CRU/TILINE Expansion Installation and Operation Manual.* The necessity for sharing a common interrupt is dictated by the DX10 and DNOS operating systems. If your system uses a different operating system, this restriction may not apply.

2.4.3 CI403 TILINE Base Address Switches

NOTE

Numbers or letters preceded by a greater-than symbol (>) are hexadecimal values.

The TILINE base address switches are located in the lower left corner of the component side of the CI403. Pencil switches 1 through 7 are compared to bits 11 through 17 of the 20-bit TILINE address from the host computer (as shown in Figure 2-1) to determine when the host is addressing the CI403. Figure 2-1 contains a table that lists TILINE addresses within the legal range of >FFC00 to >FFDFC. The table also lists the CPU byte address that maps to each 20-bit TILINE address to aid programmers. You can assign the CI403 any address within this range that is compatible with the system software. You must inform the system software of the TILINE address selected and the interrupt level of the slot where you install the CI403.



HEXADECIMAL ADDRESS		TILINE ADDRESS SWITCHES
CPU BYTE	TILINE	1 2 3 4 5 6 7
F800	FFC00	0 0 0 0 0 0 0
F808	FFC04	0 0 0 0 0 0 X
F810	FFC08	0 0 0 0 0 X 0
F818	FFC0C	0 0 0 0 0 X X
F820	FFC10	0 0 0 0 X 0 0
F828	FFC14	0 0 0 0 X 0 X
F830	FFC18	0 0 0 0 X X 0
F838	FFC1C	0 0 0 0 X X X
F840	FFC20	0 0 0 X 0 0 0
INCREMENTS OF 8_{16}	INCREMENTS OF 4_{16}	STRAIGHT BINARY SEQUENCE
F8E8	FFC74	0 0 X X X 0 X
F8F0	FFC78	0 0 X X X X 0
F8F8	FFC7C	0 0 X X X X X
F900	FFC80	0 X 0 0 0 0 0
F908	FFC84	0 X 0 0 0 0 X
F910	FFC88	0 X 0 0 0 X 0
F980	FFCC0	0 X X 0 0 0 0
FBE0	FFDF0	X X X X X 0 0
FBE8	FFDF4	X X X X X 0 X
FBF0	FFDF8	X X X X X X 0
FBF8	FFDFC	X X X X X X X

X = ON
0 = OFF

2284554

Figure 2-1. CI403 TILINE Base Address Switches

CAUTION

If you install the CI403 in a system with multiple processors using TILINE bus couplers, you must take care to position the coupler switches to inhibit TPCS addresses from propagating in the direction of the coupler priority vector. Refer to the *990 CRU/TILINE Expansion Installation and Operation Manual* for detailed information.

2.4.4 Installing the CI403

After you select a chassis slot, modify the interrupts, and set the TILINE base address switches, you can install the CI403 in the selected slot.

CI403 boards and other shielded boards are shipped from the factory with an insulator sleeve installed on the upper lip of the shield-stiffener. If you install the CI403 in a chassis with conventional (unshielded) boards, leave the insulator in place to protect the board above the CI403 from shorting to the metal shield. When you install the CI403 with other shielded boards, remove the insulator from the upper lip of the shield by sliding it off as shown in Figure 2-2.

CI403 boards equipped with ejectors of the type shown in Figure 2-3 do not seat properly in some chassis. If you encounter difficulty seating the board, clip the tabs off the ejectors as indicated in Figure 2-3.

2.4.5 Software Considerations

You must inform the system software of the TILINE base address and TILINE interrupt level assigned to the CI403. This requires that you regenerate the system in most cases. Refer to the software manuals shipped with the system software for information on reconfiguring the system to recognize and communicate with the CI403.

2.4.6 Cable Connections

The cable connections for the CI403 and CI404 are discussed separately in the following paragraphs.

Figure 2-4 shows the CI403 in an application where two of the channels support dial-up communications using asynchronous modems. The other two channels support local devices. This is one of many ways that you can use the CI403; it is not limited to the configuration shown. The CI403 can support dial-up communications on all four channels or any mix of dial-up and local devices that you require.

Figure 2-5 shows the CI404 with one channel connected to a terminal with a fiber-optic interface and another channel connected to a terminal with a conventional EIA RS-232-C interface. Notice that you must use the fiber-optic-to-EIA converter kit, TI part number 2233210-0001, to connect the CI404 to a terminal with an RS-232-C interface. The CI404 is not limited to the application shown.

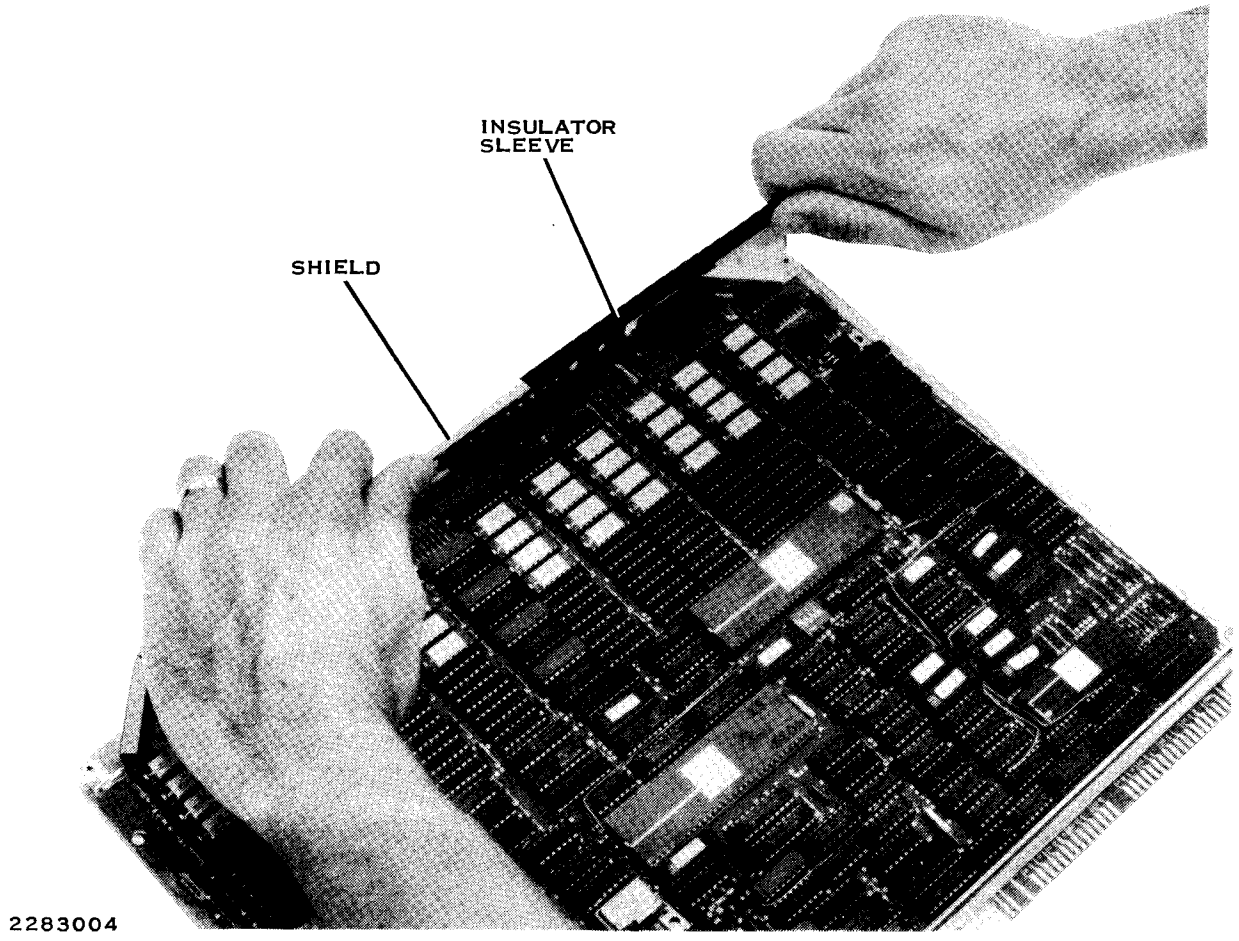


Figure 2-2. Removing the Insulator From the CI403

You must observe a few precautions when you install and handle the fiber-optic cables used with the CI404. Some of the more important considerations follow:

1. Avoid sharp bends in the cable.

2. Place the cables where people will not walk on them.

3. Avoid using excess force when pulling the cables. When pulling cables through a conduit or raceway, do not pull on the connector. Two recommended ways to pull fiber-optic cables follow and are illustrated in Figure 2-6.

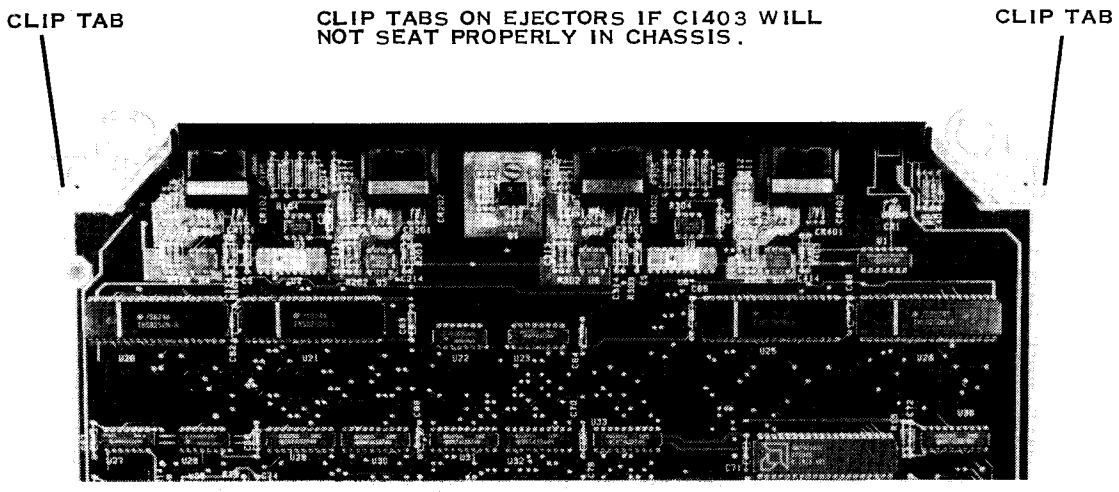


Figure 2-3. Special Installation Problems

a. Tape a rope or steel cable to the fiber-optic cable. Place padding between the pulling rope or cable and the fiber-optic connector, then extend the tape over the connector to protect it.

b. Use a braided stainless-steel pulling grip with padding between the connector and the pulling grip.

4. Keep the protective caps over the ends of the exposed fiber in the connectors until you are ready to connect the cable to the terminal or CI404. The optical fiber loses its light transmitting quality when it becomes dirty.

5. Installing connectors on fiber-optic cables in the field is not recommended.

6. Customers who fabricate their own fiber-optic cables should limit the length to 1000 meters and should use no more than one connector or splice in the cable (in addition to the connectors that mate with the CI404 and the terminal).

2.4.7 Compatible Modems

This paragraph applies only to the CI403; the CI404 does not support modems. The CI403 supports use of the TI Model 451 and Bell 103, 113, 202, and 212A modems. The CI403 also supports most other manufacturer's asynchronous modems that comply with EIA standard RS-232-C.

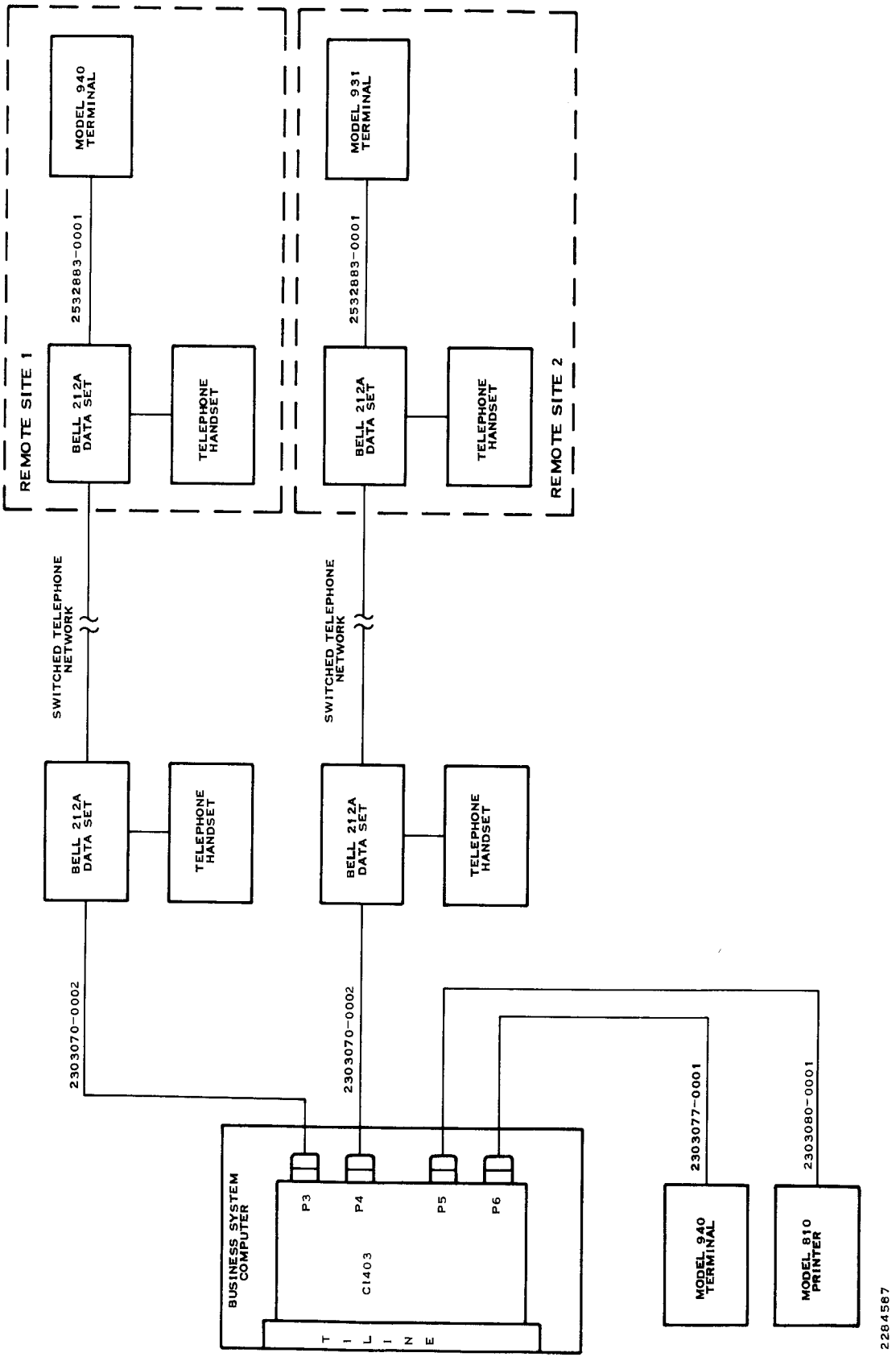


Figure 2-4. Typical Application of the CI403

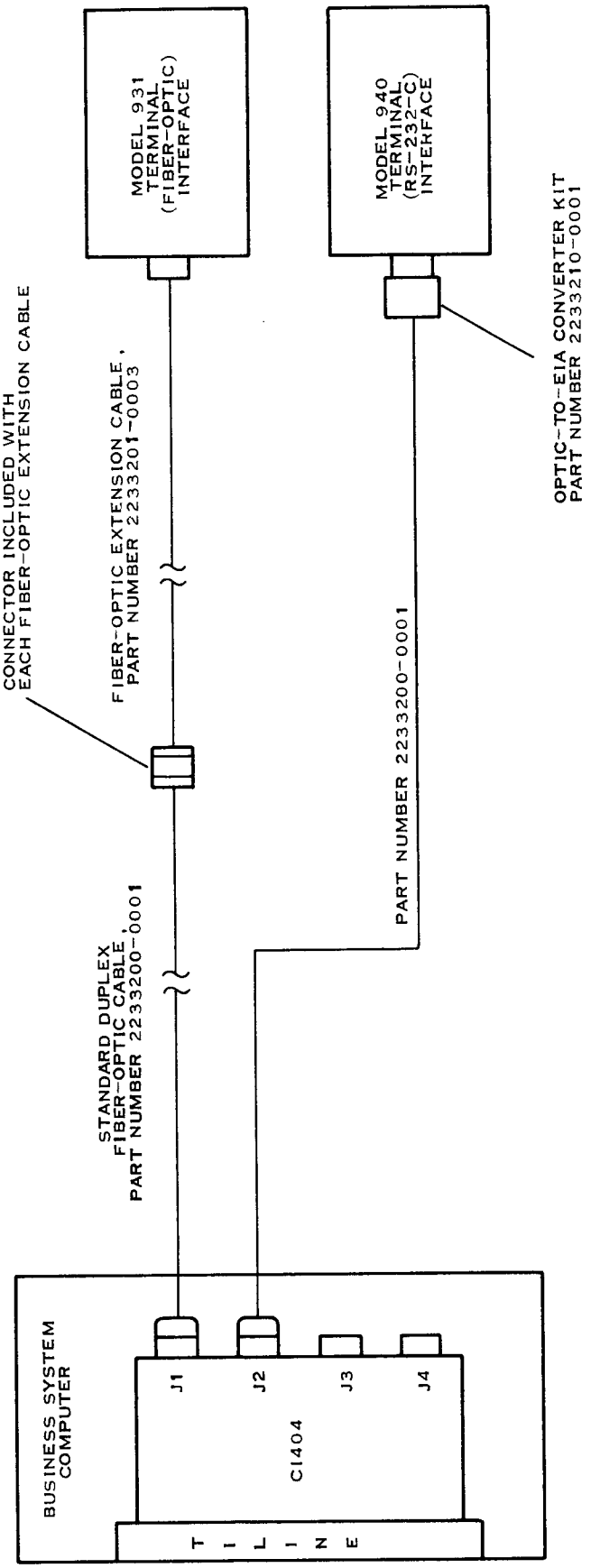


Figure 2-5. Typical Application of the CI404

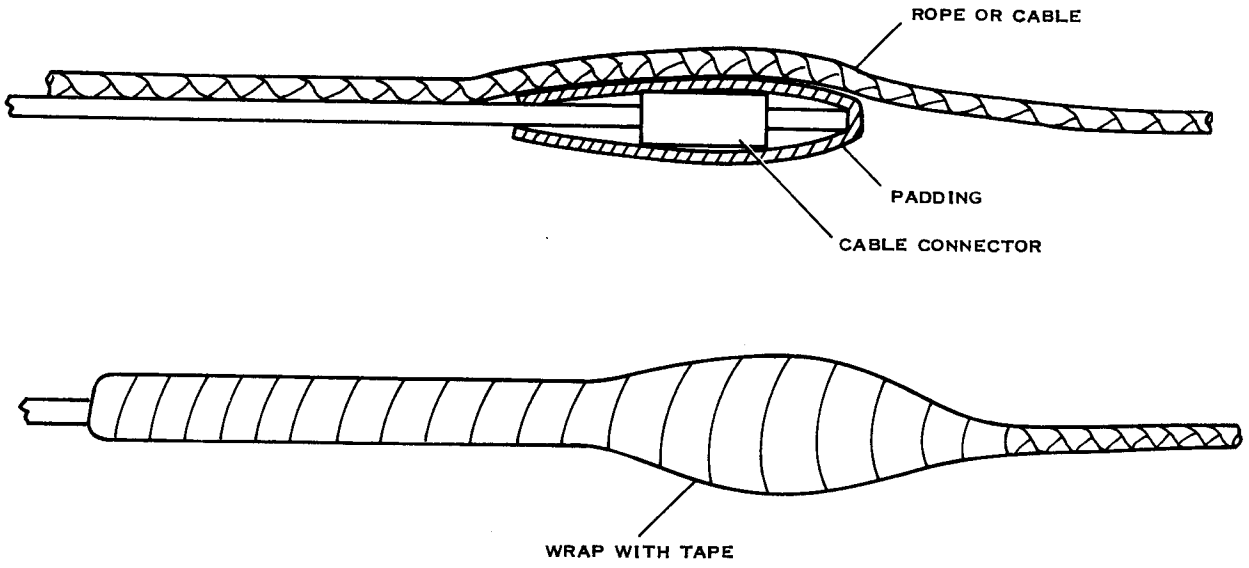


Figure 2-6. Fiber-Optic Cable Pulling Techniques

2.5 CHECKOUT

After you install the CI403 in the host computer as described in this section, check it for proper operation by powering up the computer and observing the self-test/fault light-emitting diode (LED). The LED should light while the on-board self-test routines execute and can remain on until after the first reset is issued to the board. There is a problem with the CI403 board if the self-test/fault LED remains lighted for more than 10 seconds after reset. In case of a failure, ensure that you have set the TILINE base address switches and interrupt level jumpers or switches correctly. Also ensure that the system has been regenerated to recognize the TILINE base address and interrupt level you assigned the CI403.

The next phase of checking operation of the CI403 consists of loading and executing the CI403 diagnostic MUXTST. You can find the instructions for loading the diagnostic in the *Model 990 Computer Unit Diagnostics Handbook, Volume 1*, TI part number 945400-9701. Volume 6 of the diagnostics handbook, TI part number 945400-9706, contains a program description of MUXTST and explains how to use the tests included in the diagnostic.

The diagnostic consists of a series of tests that thoroughly test the hardware on the CI403, starting with the TILINE interface logic and working through the logic for the four communication channels. You can also use the loopback tests in the diagnostic to verify proper operation of the interconnecting cables and some parts of the communication system, depending upon how the system is configured.

After you load and initialize the diagnostic, messages displayed on the CRT guide you through the tests. The CRT displays error messages whenever the tests encounter problems on the board or in the system. The error messages usually indicate the area of the problem or the failing component.

To properly check the communications interfaces at connectors P3 through P6 on the CI403, you need to install a loopback assembly or connector on the channel you are testing. The diagnostic asks you if the connector is installed and includes the interface circuits in the test if you answer yes. The loopback assembly for the CI403, TI part number 2303065-0001, is a miniature PWB with two connectors on it. The connectors are keyed to allow only the correct connector to mate with P3 through P6 on the CI403. There is also a 25-pin loopback connector, TI part number 2265197-0001, that mates with the connector on the external modem cable and includes the cable in the loopback test (if you wish to check the cable).

The loopback connector for the CI404 is a fiber-optic connector, TI part number 2233202-0001. You can install it on CI404 connectors J1 through J4 or on the end of the fiber-optic cable if you wish to include the cable in the test. You must use the cable-to-cable connector included with the loopback connector to connect it to a fiber-optic cable. If the fiber-optic cable is over 300 meters long or has splices in it, you will need to install the optic-to-EIA converter on the end of the cable and place the EIA loopback connector (TI part number 2265197-0001) on the EIA connector of the converter to boost the signal strength. If a fiber-optic cable fails the loopback test, install the converter and EIA loopback connector and try it again before assuming that the cable is faulty.

Figure 2-7 shows some examples of how you can use the loopback assembly and loopback connectors to verify proper operation of the boards and cables.

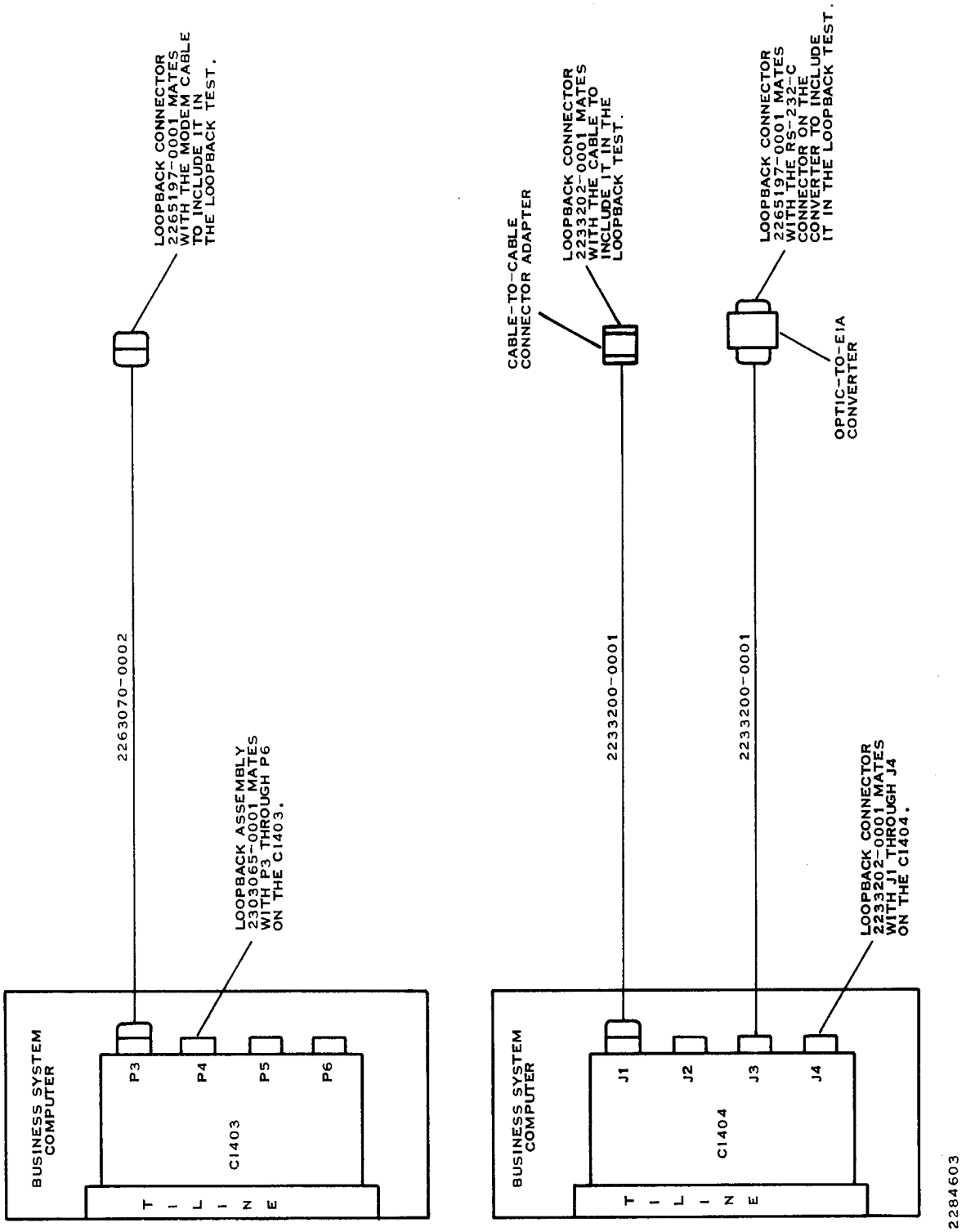


Figure 2-7. Checkout With the Loopback Assembly and Connector

3

Programming

3.1 GENERAL

This section contains information necessary for an assembly language programmer to write software routines that communicate with external modems or terminals through the Model CI403 Four-Channel Asynchronous Communications Controller. The programmer must be familiar with assembly language described in the *Model 990/12 Computer Assembly Language Programmer's Guide.*

NOTE

All references to CI403 in this section apply to both the CI403 and CI404 unless specifically indicated otherwise.

Most users prefer Texas Instruments standard operating system software that includes these communications routines. These users should refer to the applicable operating system reference manual. Users who wish to perform direct communications without using standard operating system software routines can initiate communications and receive status as described in this section.

This section provides detailed discussions of the following:

- Communication between the CI403 and the CPU using the TILINE bus
- Basic programming of the CI403, including initialization, character transmission and reception, and status recovery
- Control, status, and data word formats and descriptions

3.2 TILINE COMMUNICATION

The following paragraphs discuss communications between the host computer and the CI403 using the TILINE bus.

3.2.1 TILINE Description

The TILINE is a high-speed, asynchronous, 16-bit parallel data bus that transfers data between high-speed system elements such as main memory, the CPU, and mass data storage systems. The CI403 is assigned a block of four TILINE memory addresses. These memory locations are physically located on the CI403 board, but are addressed by the host CPU as if they were in main memory. The host CPU communicates with the CI403 by writing to and reading from these four TILINE addresses. During operation, the CPU transmits characters to any one or all of the four external modems by writing to one of these four addresses. The CPU receives data by reading one of these four addresses. The CPU also initializes the CI403 and reads its status by accessing these same four addresses.

The words written into TILINE memory at the addresses designated for CI403 communications are called slave words, and are designated slave word 0 (SW0) through slave word 3 (SW3). The CI403 is a TILINE slave and cannot control TILINE transfers; it can only respond to TILINE master devices that are capable of controlling TILINE transfers. The host CPU is a TILINE master device. Any computer instruction that reads or modifies general memory can be used to communicate with the CI403.

3.2.2 TILINE Addresses

Standard conventions built into the computer hardware and software reserve CPU byte addresses >F800 to >FBF8 for control and status communication with TILINE peripheral controllers, such as the CI403. This range is called the TILINE peripheral control space (TPCS). The processor hardware can map addresses within this range to 20-bit TILINE addresses in the range >FFC00 to >FFDFC.

The physical TILINE bus includes 20 address lines; however, a CPU byte address consists of only 16 bits. When a CPU byte address falls within the TPCS, the processor hardware automatically adds five ones to the most significant byte of the CPU byte address, making a 21-bit address. Then, the least significant bit (LSB) is dropped (this bit is a byte selector that is used only within the CPU) leaving the 20-bit TILINE address. Figure 3-1 shows the conversion of a 16-bit CPU byte address to a 20-bit TILINE word address. One way to visualize this conversion is to think of a 21-bit TILINE *byte* address of >1FF800 that loses its LSB (byte selector) to become TILINE *word* address >FFC00. The >1F comes from the five ones; the >F800 comes from the original CPU byte address. The only part of this address accessible to the programmer is the CPU byte address >F800.

The four addresses assigned to the CI403 range from the base word address to the base word address +3 word addresses. The base address is dedicated to SW0, base address +1 is dedicated to SW1, base address +2 is dedicated to SW2, and base address +3 is dedicated to SW3.

A seven-section TILINE base address switch selects the base address of the CI403. Selecting the base address of TILINE peripherals, such as the CI403, allows you to use multiple TILINE devices in one system. The base address selected must be coordinated with the operating system software. Refer to Section 2 of this manual for instructions on setting the base address switches.

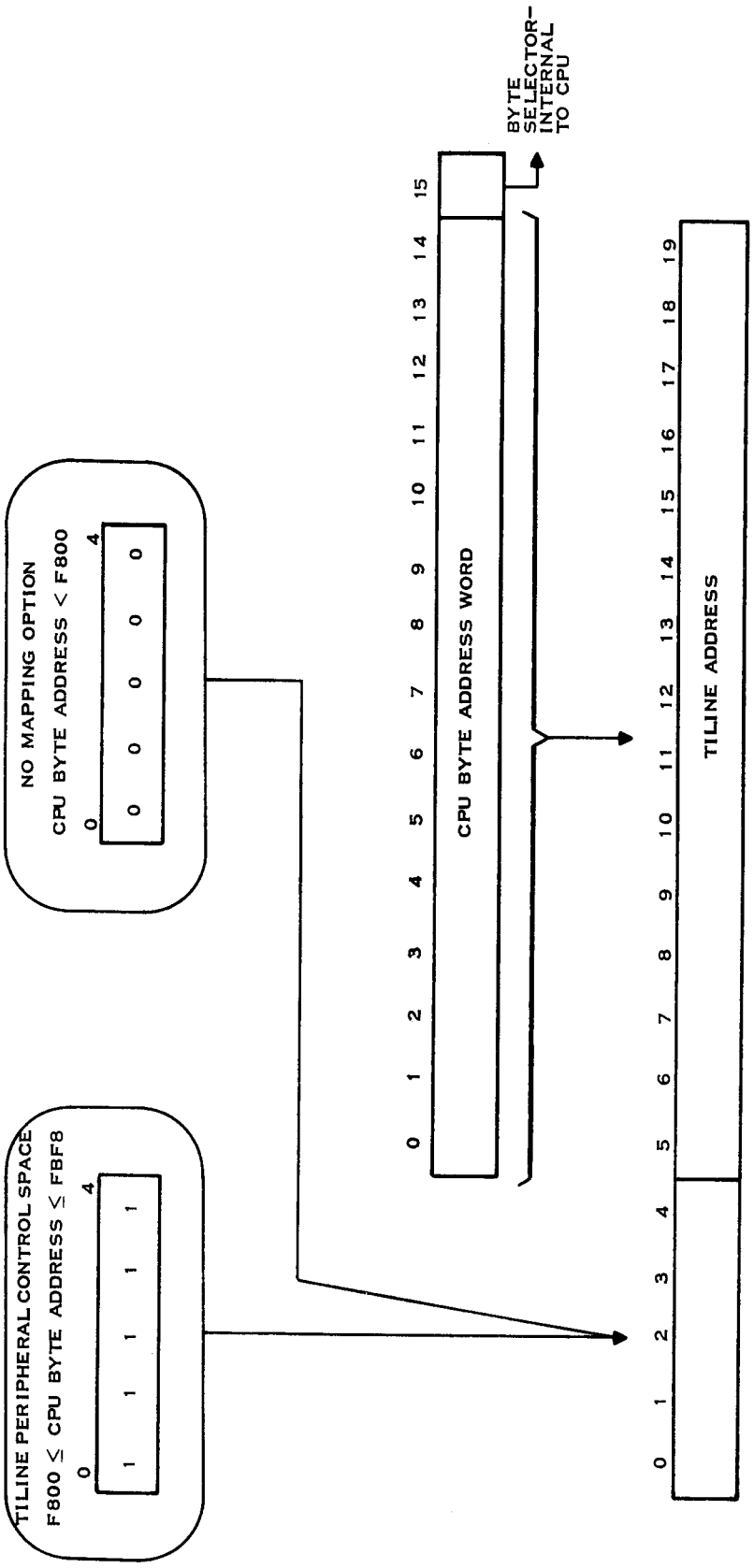


Figure 3-1. Relationship Between TILINE Address and CPU Byte Address

3.3 SLAVE WORDS

Figure 3-2 shows the format of each of the slave words used to communicate with the CI403. The purpose of each word is as follows:

- Slave word 0 — The CPU generally reads or writes this word to determine overall board status, to set interrupt conditions, and to test and set other board functions. This word also returns a unique identification number that identifies the board as a CI403 or a CI404.

- Slave word 1 — The CPU programs the ACEs for specific channel transmission and reception characteristics by writing control codes into this word location. The CPU can also read this word to determine how the ACE has been programmed and to determine ACE status. The CPU can program each channel ACE individually.

- Slave word 2 — Transmit data for all four channels is written into this word location. Each word includes a channel number as well as the data so that input data for different channels can be intermixed.

- Slave word 3 — The CPU acquires receive data from all four channels by reading this word location. Each word includes a channel number, data, and status information concerning the information transfer. Also, additional status information and error codes are returned to the CPU via SW3.

To program a channel of the board for operation, you must first initialize transmit and receive parameters such as baud rate, number of stop bits, and parity. You must also set the proper modem signals and ensure that the channel is out of the loopback mode. After initializing the channel, the CPU loads transmit data into the CI403 by successively writing to slave word 2. The CPU acquires receive data by successively reading slave word 3. The CPU and acquire status at any time by reading the remaining two slave words. The board can be programmed to interrupt the host CPU when it has valid words for the CPU to read or it can be used in a polled environment, where the CPU interrogates the board periodically to determine whether it needs service.

The following paragraphs describe the functions of each of these words and their constituent bits.

NOTE

In order to avoid confusion between signals that are active in either the high or low state, the following text uses the terms assert (or asserted) and negate (or negated) to describe active and inactive signals, respectively, regardless of their actual logic level.

In programming the CI403, however, it is important to note that positive logic is used throughout. Therefore, when the discussion indicates that a signal should be asserted, set the particular bit under discussion to logic level 1 (high); if the signal should be negated, set the bit to logic level 0 (low). Logic level 1 is read in bits that are asserted; logic level 0 is read in bits that are negated.

SLAVE WORD	FUNCTION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SW0	BOARD STATUS	IP	IE	IS	IR	MR	TE	FA	TST	UNUSED		BOARD IDENTIFICATION					

IP – INTERRUPT PENDING
IE – INTERRUPT ENABLE
IS – INTERRUPT SELECT
IR – INPUT READY

MR – MASTER RESET
TE – TIMER ENABLE
FA – FAILED CHANNEL TEST
TST – TEST MODE SELECT

BOARD ID: CI403 = 000011
CI404 = 000100

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SW1	ACE CONTROL	ACE R/W	ACE REGISTER NUMBER			NOT USED	CHANNEL NUMBER			ACE DIRECT READ/WRITE DATA							

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SW2	TRANSMIT DATA	NOT USED					CHANNEL NUMBER			TRANSMIT FIFO WRITE DATA							

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SW3	RECEIVE DATA AND STATUS	DA INV	STATUS CODE			CH CHG	CHANNEL NUMBER			RECEIVE FIFO DATA AND STATUS							

DA INV – DATA INVALID

CH CHG – CHANNEL NUMBER AND/OR STATUS IS DIFFERENT THAN IT WAS ON THE LAST VALID READ OF RECEIVED DATA

STATUS CODE:

0 – RECEIVE DATA PRESENT
1 – TRANSMIT FIFO EMPTY
2 – TRANSMIT SHIFT REGISTER EMPTY
3 – INVALID ACE INTERRUPT
4 – INTERFACE STATUS

DATA	EVENT CODE
>00	– TIMER TICK
>01	– STOP SENDING XMIT DATA TO TILINE FIFO
>02	– RESUME SENDING XMIT DATA

5 – LINE STATUS
6 – MODEM STATUS
7 – RESERVED

2284604

Figure 3-2. CI403 Slave Word Formats

3.3.1 Slave Word 0 (SW0) — Board Status

SW0 (Figure 3-3) reports the status of the CI403 to the CPU during a slave read operation and establishes board-wide parameters, such as interrupt configurations, during slave write operations. All SW0 write operations must use a read-modify-write type of instruction except when first initializing the board. At the time of power-up initialization, the CPU software should execute a master reset sequence as defined in paragraph 3.3.1.5.

CAUTION

The software should not allow any SW2 or SW3 activity for three microseconds after an SW0 write command is executed.

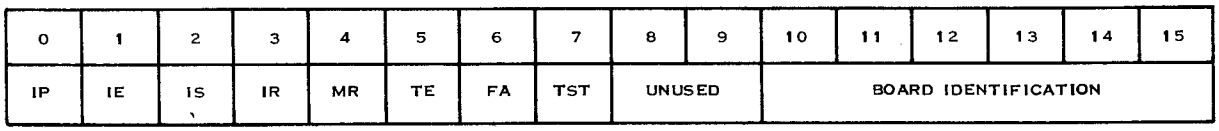
3.3.1.1 Interrupt Pending — SW0, Bit 0. The CI403 asserts this bit to indicate that receive data is available to be read from the receive FIFO via SW3. Assertion of this bit generates a TILINE interrupt only if the interrupt enable bit (SW0, bit 1) is asserted. If the host does not assert SW0, bit 1, the host software must poll SW0, bit 3 to determine if the CI403 receive FIFO data is available. When the CPU software reads SW3, the interrupt is cleared and the CI403 negates this bit. No other CPU action is required to clear a CI403 interrupt or this bit. Note that this is the only CPU interrupt.

3.3.1.2 Interrupt Enable — SW0, Bit 1. The interrupt enable bit controls whether the CI403 generates a TILINE interrupt when receive data is available. When the CPU asserts this bit during a write operation, a TILINE interrupt is generated when the CI403 asserts SW0, bit 0. If the CPU negates this bit, no TILINE interrupt is generated.

3.3.1.3 Interrupt Select — SW0, Bit 2. External interrupts are not currently supported. This bit must always be set to zero to select the backplane TILINE interrupt.

3.3.1.4 Input Ready — SW0, Bit 3. The CI403 asserts this bit to indicate that receive FIFO data is available. The CPU can poll this bit if the TILINE interrupt is not used. The CI403 negates this bit after the CPU has read the last valid data word from the receive FIFO.

3.3.1.5 Master Reset — SW0, Bit 4. The CPU sets the master reset bit to initiate master reset processing by the CI403. The CI403 negates this bit when master reset processing completes successfully. Master reset processing is in progress as long as this bit remains asserted. If this bit remains asserted longer than one second, it indicates significant hardware problems in the CI403. In this case, the board should be replaced. The normal time required for completion of reset processing is approximately 50 milliseconds, if all channels are functional.



0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IP	IE	IS	IR	MR	TE	FA	TST	UNUSED		BOARD IDENTIFICATION					

IP – INTERRUPT PENDING
IE – INTERRUPT ENABLE
IS – INTERRUPT SELECT
IR – INPUT READY

MR – MASTER RESET
TE – TIMER ENABLE
FA – FAILED CHANNEL TEST
TST – TEST MODE SELECT

BOARD ID: CI403 = 000011
CI404 = 000100

2284605

Figure 3-3. Slave Word 0, Bit Format

During master reset processing, the CI403 performs a read and write test of all FIFO memory, resets all channels, and does an internal loopback test of all channels. When a master reset completes successfully, SW0 and the ACE registers are set as follows:

- SW0, bits 0 through 5 and bit 7 are reset; bit 6 indicates whether a channel failure has occurred.
- ACE register 0 contains irrelevant data.
- ACE register 1 contains > 0D.
- ACE register 2 contains > 01.
- ACE register 3 contains > 1A.
- ACE register 4 contains > 10.
- ACE registers 5 and 6 contain > 00.
- The ACE baud rate select registers are set for a baud rate of 1200.

If any channel fails the loopback test, SW0, bit 6 is asserted and ACE register 7, bit 2 is asserted for the failing channel. Table 3-1 shows the status of the various bits associated with the self-test error reporting following a master reset operation.

Table 3-1. Master Reset Error Reporting

Master Reset Final Status	SW0 Bit 4	SW0 Bit 6	ACE Reg 7, Bit 2 Ch 0	Ch 1	Ch 2	Ch 3
Global board failure (software time-out required to detect)	1	X	X	X	X	X
Channel #0 failure	0	1	1	X	X	X
Channel #1 failure	0	1	X	1	X	X
Channel #2 failure	0	1	X	X	1	X
Channel #3 failure	0	1	X	X	X	1
No failure detected	0	0	0	0	0	0

Note:

The X's in the table refer to bits that may or may not be asserted, depending upon the error condition.

The host software is responsible for performing the following steps in its master reset routine:

1. Read SW0 and test bit 4 for status. If it is not asserted, proceed with step 2. If it is asserted, a master reset has been initiated by a previous power-up reset or an I/O reset has not completed. In this case, go to step 5.

2. If SW0, bit 4 was not asserted when tested in step 1, delay for 20 milliseconds, then reread SW0 and test bit 4 again. If it is still not asserted and the board ID reads 03 or 04, there was no previous reset in progress. In this case, proceed to step 3. If bit 4 is asserted, go to step 5.

3. Set SW0, bit 4 by writing to SW0 to initiate a master reset.

4. Read SW0 to verify that bit 4 is asserted.

5. Monitor the state of SWO, bit 4. If it is not negated within one second, the board has failed self-test. If it is asserted within one second, proceed with step 6.

6. Read SW0 and test bit 6. If it is not asserted, the self-test has completed without detecting any bad channels. If it is asserted, proceed to step 7.

7. Read ACE register 7 for each channel. Each channel that has ACE register 7, bit 2 asserted has failed self-test.

3.3.1.6 Timer Enable — SW0, Bit 5. Asserting the timer enable bit enables the 213-millisecond timer. When enabled, the CI403 returns timer attention status via SW3. See paragraph 3.3.4.2 for more information. Negating this bit disables the timer.

3.3.1.7 Failed Channel Test — SW0, Bit 6. The CI403 asserts this bit when any channel self-test fails during master reset processing. If the CI403 asserts this bit immediately after a master reset, the CPU software must read ACE register 7 for each channel to determine which channel(s) has failed. See the discussion of ACE register 7 for more information.

3.3.1.8 Test Mode Select — SW0, Bit 7. Asserting the test mode select bit places the CI403 in the test mode. In this mode, the CI403 neither transmits nor receives data via the ACEs. However, ACE direct commands and FIFO input and output are still functional. Negating this bit returns the CI403 to normal operation.

3.3.1.9 Not Used — SW0, Bits 8 and 9. These bits are not used by the CI403 and should remain zero.

3.3.1.10 Board Identification — SW0, Bits 10 Through 15. These bits can be read to determine board identification. They are permanently set to 000011 (> 03) for the CI403 and 000100 (> 04) for the CI404.

3.3.2 Slave Word 1 (SW1)

SW1 (Figure 3-4) allows direct programming and reading of status of the ACE registers. Each ACE performs serial-to-parallel data conversion on received data characters and parallel-to-serial conversion on transmit characters. The ACE has fully programmable serial interface characteristics and complete status reporting capabilities.

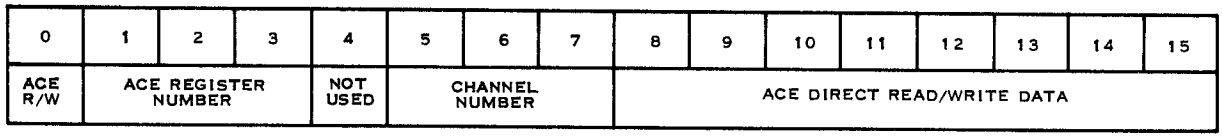


Figure 3-4. Slave Word 1, Bit Format

The CPU programs the ACE configuration by writing to SW1 and can determine ACE status at any time by reading SW1. Reading status during normal data transmission is not necessary since the CI403 reports any error conditions that occur on any channel in use.

3.3.2.1 Read/Write Control — SW1, Bit 0. A write to SW1 with the read/write control bit asserted informs the CI403 that the CPU wants to read the designated ACE register on a particular channel. SW1, bits 1 through 3 designate the register number; SW1, bits 5 through 7 designate the channel number. When the CI403 determines that a read operation is desired, it transfers the appropriate ACE register information to SW1, bits 8 through 15, and negates SW1, bit 0. The CPU can poll SW1, bit 0 until it is negated, to ensure that the register data is valid.

CAUTION

The software should allow no other ACE direct commands from the time that an ACE read is requested until it completes. A read should take no longer than 50 microseconds to complete.

A SW1 write with the read/write control bit negated indicates to the CI403 that the CPU is writing ACE control information to a specific ACE register. SW1, bits 1 through 3 contain the ACE register number; SW1, bits 5 through 7 contain the ACE channel number. SW1, bits 8 through 15 contain the desired ACE control information, as described in the following paragraphs.

CAUTION

The software must ensure that ACE direct commands (SW1 writes) are separated in time by at least 50 microseconds.

3.3.2.2 ACE Register Number — SW1, Bits 1 Through 3. Each CI403 channel has 9 ACE registers, plus a hardware register that is addressed like an ACE register, accessible to the CPU. Note that two of the ACE register addresses are multiplexed to provide 9 registers from 7 addresses. These registers control ACE operations and transmit and receive data. The following paragraphs describe each of these registers.

Register 0 — Data/Baud Rate Selection. ACE register 0 is either a data register or a baud rate selection register, depending upon the state of the baud rate generator access bit. The baud rate generator access bit is located in ACE register 3. When the baud rate generator access bit is negated, ACE register 0 is a data register. When the CPU software initiates a read of register 0 in this mode, the receiver buffer contents are returned in SW1, bits 8 through 15. When the CPU software initiates a write to register 0 in this mode, the data in SW1, bits 8 through 15 is written to the ACE transmitter holding register.

When the baud rate generator access bit is asserted, ACE register 0, SW1, bits 8 through 15 correspond to the least significant byte of the baud rate word when the CPU software programs the ACE baud rate. Refer to Table 3-4 for baud rates.

Register 1 — Interrupt Enable/Baud Rate Selection. ACE register 1 is either the ACE interrupt enable register or a baud rate selection register, depending upon the state of the baud rate generator access bit. The baud rate generator access bit is located in ACE register 3.

When the baud rate generator access bit is negated, ACE register 1 is the interrupt enable register that allows ACE interrupts to be selectively enabled. In this case, SW1, bits 12 through 15 correspond to specific ACE interrupt enable bits when read by the CPU software. Table 3-2 describes the ACE interrupt enable bits.

NOTE

ACE interrupts are enabled for internal use by the CI403 hardware only and do not enable interrupts to the CPU. They are described here for testing purposes only and must not be altered during normal operation.

Table 3-2. Interrupt Enable Bit Definitions

SW1, Bit	Definition
15	Receive data interrupt enable
14	Transmitter holding register empty interrupt enable
13	Receiver line status interrupt enable
12	Modem status interrupt enable
8-11	Zero

When the baud rate generator access bit is asserted, ACE register 1, SW1, bits 8 through 15 correspond to the most significant byte of the baud rate word when the CPU software programs the ACE baud rate. See the description of ACE register 3 and Table 3-4.

Register 2 — Interrupt Identification. ACE register 2 is the interrupt identification register. A zero in bit 15 indicates whether an ACE interrupt is pending, bits 13 and 14 identify the ACE interrupt condition that is pending, and bits 8 through 12 are always zero. The following paragraphs describe the ACE interrupt that is designated by the conditions of SW1, bits 13 and 14.

NOTE

Register 2 identifies the ACE interrupt rather than a CPU interrupt.

- Bit 13 = 1, bit 14 = 1, receiver line status. When enabled, the ACE generates a receiver line status interrupt to the CI403 hardware when an overrun error, parity error, framing error, or break interrupt occurs. When the line status register is read, the ACE clears the interrupt.

- Bit 13 = 1, bit 14 = 0, receive data available. When enabled, the ACE generates an interrupt to the CI403 hardware when receive data is input to the ACE receive buffer register. When the receive data register is read, the ACE clears the interrupt.

- Bit 13 = 0, bit 14 = 1, transmitter holding register empty. When enabled, the ACE generates an interrupt to the CI403 hardware when the transmitter holding register is empty. When the identification register is read, the ACE clears the interrupt. This interrupt is normally not enabled by the CI403 microcode.

- Bit 13 = 0, bit 14 = 0, modem status. When enabled, the ACE generates an interrupt to the CI403 hardware when a change in status occurs with CTS, DSR, RI, or RLSD (DCD). When the modem status register is read, the ACE clears the interrupt.

Register 3 — Line Control. ACE register 3 is the line control register, a read/write register that specifies the asynchronous data format. SW1, bits 8 through 15 are written to configure the ACE for specific data transfers. The CPU can read register 3 to determine this configuration. SW1, bits 8 through 15 are used as described in the following paragraphs. Bits 14 and 15 specify the word length (excluding the parity bit) as shown in Table 3-3.

Table 3-3. Word Length Codes

SW1,14	SW1,15	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- SW1, bit 13, number of stop bits. When bit 13 is negated, one stop bit is generated during transmission or checked during reception. When bit 13 is asserted, one and one-half stop bits are generated or checked when using 5-bit data; two stop bits are generated or checked when using 6-, 7-, or 8-bit data.

- SW1, bit 12, parity enable. When bit 12 is asserted, parity is generated on transmission or checked during reception. When bit 12 is negated, parity is neither generated nor checked.

- SW1, bit 11, even parity select. When parity is enabled (SW1, bit 12 is asserted) and bit 11 is asserted, even parity is generated or checked. When parity is enabled and bit 11 is negated, odd parity is generated or checked.

- SW1, bit 10, stick parity. When parity is enabled and bit 10 is asserted, parity is transmitted and received in a fixed state (always asserted or negated), opposite the state of SW1, bit 11. For example, when bit 11 is asserted, the parity bit is always zero.

- SW1, bit 9, break control. When bit 9 is asserted, the output of the ACE transmitter is forced to the spacing state (logic 0) and remains there regardless of transmitter activity. When bit 9 is negated, normal transmission can occur.

- SW1, bit 8, baud rate generator access bit. When bit 8 is asserted, channel speed can be programmed by writing to ACE registers 0 and 1. Once channel speed has been programmed, bit 8 must be negated to allow receiver buffer and transmitter holding register access. Table 3-4 lists the hexadecimal value for each baud rate.

NOTE

The value in the baud rate generator register determines both transmit and receive baud rates.

Table 3-4. Encoded Baud Rates

Baud Rate	Hex Rate	Percent Error
50.0	0C00	0.0
75.0	0800	0.0
110.0	0574	0.0
134.5	0476	0.0
150.0	0400	0.0
200.0	0300	0.0
300.0	0200	0.0
600.0	0100	0.0
1,200.0	0080	0.0
1,800.0	0055	0.4
2,400.0	0040	0.0
3,600.0	002B	0.8
4,800.0	0020	0.0
7,200.0	0015	1.6
9,600.0	0010	0.0
19,200.0	0008	0.0

Note:

Do not use the 7200 baud rate unless absolutely necessary due to the large percentage of error inherent in this rate.

Program the desired baud rate by performing the following procedure:

1. Construct a 16-bit binary word with bit 0 = 0. (This becomes the SW1 read/write bit.) Set bits 1 through 3 to 011 (to program register 3). Set bit 4 to zero, set bits 5 through 7 to the desired channel number, and set bit 8 to one (the baud rate generator access bit). Each of the remaining bits can be set, as desired, for the particular conditions listed in the register 3 discussion (later in this section). After you have constructed the word, write it to SW1.

2. Construct a word with bit 0 = 0, bits 1 through 3 = 000 (ACE register 0), and bits 4 through 7 set to the desired channel number. Set bits 8 through 15 to the least significant byte of the baud rate word from Table 3-4. This byte is the last two digits in the Hex Value column. After you construct the word, write it to SW1.

3. Construct a word with bit 0 = 0, bits 1 through 3 = 001 (ACE register 1), and bits 4 through 7 set to the desired channel number. Set bits 8 through 15 to the most significant byte of the baud rate word from Table 3-4. This byte is the first two digits in the Hex Value column. After you construct the word, write it to SW1.

4. Repeat step 1 with bit 8 set to zero to disable the baud rate generator access bit.

NOTE

Consecutive ACE direct commands must be at least 50 microseconds apart in accessing SW1.

Register 4 — Modem Control. ACE register 4 is a read/write register that controls the modem interface. SW1, bits 8 through 15 manipulate the state of the modem control output signals. ACE register 4 is read to determine the status of the modem control signals. SW1 bit definitions are described as follows:

- SW1, bit 15, data terminal ready (DTR). Asserting this bit asserts the DTR modem output signal. Negating this bit negates the DTR modem output signal. For example, when a one is written to bit 15, the DTR modem output signal goes to the EIA control on state (+3 V).

- SW1, bit 14, request to send (RTS). Asserting this bit asserts the RTS modem output signal. Negating this bit negates the RTS modem output signal. For example, when a one is written to bit 15, the RTS modem output signal goes to the EIA control on state (+3 V).

- SW1, bit 13, secondary request to send (SRTS). Asserting this bit asserts the SRTS modem output signal. Negating this bit negates the SRTS modem output signal. For example, when a one is written to bit 15, the SRTS modem output signal goes to the EIA control on state (+3 V).

- SW1, bit 12, external analog loopback (AL). This bit corresponds to RS-232-C, pin 15. Asserting this bit places the external modem in an analog loopback condition if the modem is so equipped. Negating this bit terminates the external loopback mode. Asserting this bit forces pin 15 to the EIA control on state (+ 3 V).

- SW1, bit 11, internal loopback. Asserting this bit causes transmit data to the ACE to be connected directly to the receive data inputs. Modem interface signals are connected as follows:

  — DTR to DSR

  — RTS to CTS

  — SRTS to RI

  — AL to RLSD (DCD)

NOTE

The modem output leads are still active when you select the internal loopback mode.

- Bits 8 through 10 are not used and must remain zero.

Register 5 — Line Status. ACE register 5 can be read to determine data transfers status. Reading this register negates bits 11 through 14. SW1, bits 8 through 15 are described as follows:

- SW1, bit 15, data ready indicator. The ACE asserts this bit when it has received a complete character and transferred it into the ACE receive buffer register. The ACE negates this bit when the ACE receive buffer register is read. This bit can also be negated by writing directly to this register.

- SW1, bit 14, overrun error indicator. The ACE asserts this bit if the data in the ACE receive buffer register is not read before the next input character is transferred to the ACE receive buffer register. The ACE negates this bit when the line status register is read.

- SW1, bit 13, parity error indicator. The ACE asserts this bit if the received data character does not have the correct parity, as selected by the parity select bits (ACE register 3, SW1, bits 10 through 12). The ACE negates this bit when the line status register is read.

- SW1, bit 12, framing error indicator. The ACE asserts this bit if the received character did not have a valid stop bit. The ACE negates this bit when the line status register is read.

- SW1, bit 11, receive break indicator. The ACE asserts this bit if the line is held in the spacing state longer than a full word transmission time. The ACE negates this bit when the line status register is read.

- SW1, bit 10, transmitter holding register empty indicator. The ACE asserts this bit when a character is transferred from the transmitter holding register to the transmitter shift register. The ACE negates this bit when the transmitter holding register is loaded. If the CI403 hardware asserts the transmitter holding register empty interrupt enable bit, the CI403 hardware is interrupted when this indicator bit is asserted.

- SW1, bit 9, transmitter shift register empty indicator. The ACE asserts this bit when the transmitter shift register is idle. The ACE negates this bit when a character is transferred from the transmitter holding register to the transmitter shift register. The CI403 hardware determines this condition by reading the line status register. When the transmitter shift register interrupt is enabled, (ACE register 7, SW1, bit 9), the CI403 places the transmitter shift register empty status condition into the receive FIFO if this bit is asserted.

- SW1, bit 8, not used. This bit is not used and is always zero.

Register 6 — Modem Status. Register 6 can be read to determine current modem status. Reading this register clears bits 11 through 15. Bit definitions of SW1, bits 8 through 15 follow:

- SW1, bit 15, delta clear to send. The ACE asserts this bit if the state of CTS has changed since the last time the modem status register was read. The ACE negates this bit when the modem status register is read.

- SW1, bit 14, delta data set ready. The ACE asserts this bit if the state of DSR has changed since the last time the modem status register was read. The ACE negates this bit when the modem status register is read.

- SW1, bit 13, trailing edge of ring indicator. The ACE asserts this bit if the RI signal changes from an asserted condition to a negated condition. The ACE negates this bit when the modem status register is read.

- SW1, bit 12, delta received line signal detector. The ACE asserts this bit if RLSD (DCD) has changed state since the last time the modem status register was read. The ACE negates this bit when the modem status register is read.

- SW1, bit 11, clear to send (CTS) input. This bit is asserted when the CTS input signal to the modem is asserted (in the EIA on state). It is negated when the CTS input is negated. Transfer of data from the channel transmit data FIFO to the ACE is inhibited if CTS is false.

- SW1, bit 10, data set ready (DSR) input. This bit is asserted when the DSR input signal to the modem is asserted. It is negated when the DSR input is negated.

- SW1, bit 9, ring indicator (RI) input. This bit is asserted when the RI input signal to the modem is asserted. It is negated when the RI input is negated.

- SW1, bit 8, received line signal detect (RLSD(DCD)) input. This bit is asserted when the input signal to the modem is asserted. It is negated when the RLSD (DCD) input is negated. Any received data characters or line status errors received while this bit is negated are discarded and not reported to the host.

Register 7 — Channel Control. Register 7 can be read to acquire certain channel status information; it can be written to set channel dependent control states. A successful master reset and channel loopback test negates all bits in this register. An unsuccessful channel loopback test negates all register 7 bits except the channel disable bit. Bits 8 through 15 are used as follows:

- SW1, bit 8, transmit FIFO empty interrupt enable. If this bit is asserted and the channel transmit FIFO becomes empty, channel transmit FIFO empty status is written to the receive FIFO. This bit is negated when the interrupt occurs and must then be reasserted to cause additional interrupt notification. The CPU reads this bit to determine whether this interrupt is enabled.

- SW1, bit 9, transmit shift register empty enable. If this bit is asserted and the channel transmit shift register becomes empty, channel transmit shift register empty status is written to the receive FIFO. This bit is negated when the interrupt occurs and must then be reasserted to cause additional interrupt notification. The CPU can read this bit to determine whether this interrupt is enabled.

- SW1, bit 10, channel disable. When this bit is asserted, the CI403 stops polling the specified channel ACE for information so that transmission and reception is disabled. ACE programming, however, is not changed. Since the state of the ACE is not changed, ACE direct commands can be used to transmit and receive data over the communications line. The channel remains disabled until this bit is negated. The CPU can read register 7 to determine whether the channel is disabled. A channel-related failure detected during master reset channel loopback tests also causes this bit to be asserted. This allows the host software to poll each channel to isolate the source of the failure when SW0, bit 6 is asserted after a master reset.

NOTE

This method of transmitting and receiving must only be used during testing and not during normal data handling.

- SW1, bit 11, channel reset. Asserting this bit resets the specified channel ACE. The reset procedure lasts approximately 23 microseconds; however, there may be several hundred microseconds of delay after the request before the reset is initiated. The CI403 negates this bit after the channel reset completes. After a channel reset, the ACE registers contain the following: ACE register 1 contains >0D, ACE register 2 contains >01, ACE register 3 contains >1A, ACE register 4 contains >10, ACE register 5 contains >00, ACE register 6 contains >00, and the baud rate is set to 1200.

- SW1, bit 12, disable ACE output. Asserting this bit disables the specified channel transmit FIFO output. The channel output remains disabled until this bit is negated. The CPU can read this bit to determine if the channel FIFO output is disabled. Note that the channel receive remains active regardless of the setting of this bit.

- SW1, bit 13, speed indicator/modem status inhibit. The CPU reads this bit to determine the state of the modem speed indicator bit input. Speed indication is supported with the Bell 212A and Vadic 3400 (or equivalent) modems. When the host writes to the CI403 and sets this bit, all modem status interrupts to the host via the receive FIFO are inhibited.

- SW1, bit 14, receiver squelch (half duplex). Asserting this bit disables the receiver during transmissions (when RTS is asserted). Negating this bit enables the receiver during transmission.

- SW1, bit 15, clear transmit FIFO. Asserting this bit aborts transmission of all data in the FIFO. However, it does not affect transmission of any data already transferred to the ACE (up to two data bytes). Asserting this command clears all bits of ACE register 7 except the channel disable bit (SW1, bit 0).

3.3.3 Slave Word 2 (SW2)

The host loads data into the TILINE transmit FIFO via SW2 (Figure 3-5). The CI403 inspects the word to determine the channel number and then transfers the data byte of this word to the appropriate channel transmit FIFO. Note that SW2, bits 0 through 4 are not used and should remain zero. SW2, bits 5 through 7 specify the channel number.

The CPU software routine uses SW2 to fill the appropriate channel transmit FIFO independent of other CI403 functions. Full-word instructions should always be used. If the CI403 becomes overrun with transmit data, it places a data word in the receive FIFO with a status code of 4, channel number of F, and a data byte of >01, informing the host to stop the flow of transmit data. When the CI403 is ready to accept transmit data again, it places a data word in the receive FIFO with a status code of 4, a channel number of F, and a data byte of >02. Refer to the discussion of the status code bits, SW3, bits 1 through 3 later in this section. The CI403 can accept at least 64 word transfers after it issues a request to halt the transfers. An overrun condition should never occur in normal operation.

3.3.4 Slave Word 3 (SW3)

The CPU reads data and status from the receive FIFO via SW3 (Figure 3-6). If interrupts are enabled (SW0, bit 1), the CI403 interrupts the CPU when SW3 contains valid information for the host. If interrupts are not enabled the CPU must poll the input ready bit (SW0, bit 3) to determine when SW3 is valid. When the CPU software reads all data stored in the receive FIFO, the CI403 clears the interrupt. The CPU software should never perform a write instruction to SW3.

The following paragraphs describe the functions of the bits in SW3.

3.3.4.1 Invalid Receive Data — SW3, Bit 0. The CI403 asserts this bit to indicate that data in SW3, bits 8 through 15 is invalid. SW3 can be successively read to acquire receive data until this bit is asserted, which indicates that the receive FIFO is empty and that data in SW3, bits 8 through 15 should be ignored.

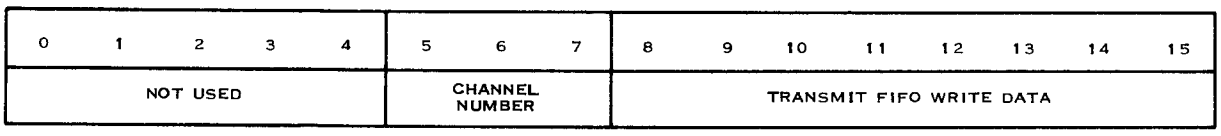


Figure 3-5. Slave Word 2, Bit Format

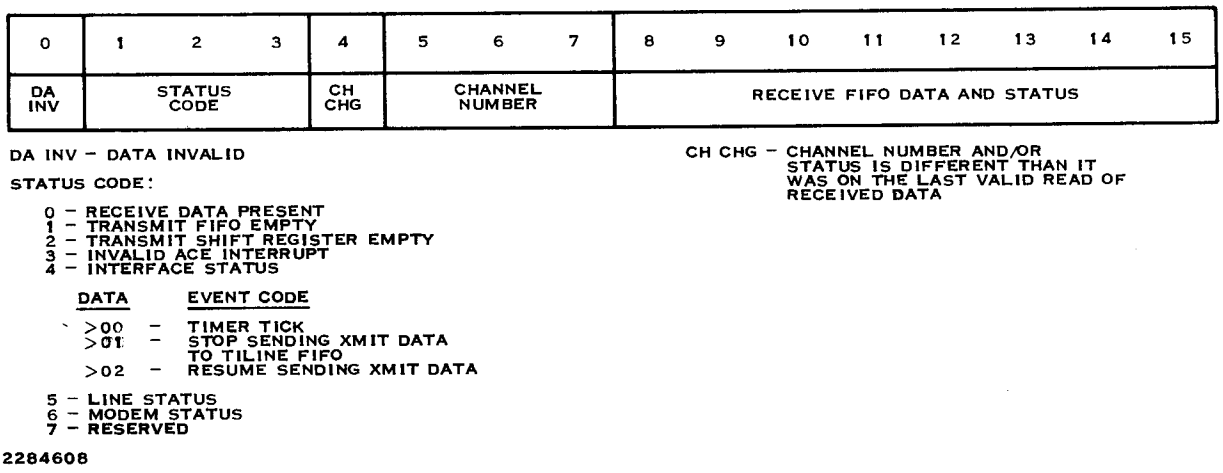


Figure 3-6. Slave Word 3, Bit Format

3.3.4.2 Status Code — SW3, Bits 1 Through 3. When SW3, bit 0 is negated (data is valid in SW3, bits 8 through 15), bits 1 through 3 contain an interrupt status code that indicates the cause of the CPU interrupt. The following paragraphs explain status codes 0 through 7. The CI403 writes status codes 1, 2, and 6 only if the appropriate interrupt is enabled in ACE register 7.

Status Code 0 — Receive Data. A status code of 0 (SW3, bits 1 through 3 = 000) indicates that receive data is present in bits 8 through 15 for the channel specified in bits 5 through 7.

Status Code 1 — Transmit FIFO Empty. A status code of 1 (SW3, bits 1 through 3 = 001) indicates that the transmit FIFO for the channel specified in bits 5 through 7 is empty.

Status Code 2 — Transmit Shift Register Empty. A status code of 2 (SW3, bits 1 through 3 = 010) indicates that the transmit shift register for the channel specified in bits 5 through 7 is empty.

Status Code 3 — Invalid ACE Interrupt. A status code of 3 (SW3, bits 1 through 3 = 011) indicates that the CI403 hardware received an invalid interrupt from the ACE channel specified in bits 5 through 7. This occurs when there is a hardware problem.

Status Code 4 — Interface Status. A status code of 4 (SW3, bits 1 through 3 = 100) indicates that an event has occurred on the CI403 that affects all channels. When this status code is returned, SW3, bits 4 through 7 are all asserted (> F). The specific event is identified in the data byte (SW3, bits 8 through 15). In this case, the value in the data byte is called an event code. The following paragraphs describe each of these event codes:

- Timer Tick (> 00). An event code of > 00 is returned when the CI403 timer interval has expired and the host has enabled the timer by asserting SW0, bit 5. The time interval is approximately 213 milliseconds.

- Halt Transfer (> 01). An event code of > 01 is returned if the TILINE FIFO is becoming full. When this status code is returned, at least 64 word spaces remain in the TILINE FIFO before an overflow occurs. The CI403 returns a resume transfer event code (> 02) when it is prepared to accept more transmit data. The halt and resume conditions pertain to data transferred to the CI403 via SW2 only. Other slave words can be used independently of these halt or resume commands. The halt condition is a rare occurrence, possible only under certain worst-case conditions.

- Resume Transfer (> 02). The CI403 returns event code > 02 when the TILINE FIFO contains enough space to allow the host to resume sending transmit data via SW2. This event code is returned only after the CI403 has previously issued a halt event code.

Status Code 5 — Line Status. A status code of 5 (SW3, bits 1 through 3 = 101) indicates that the line status register interrupt producing inputs have changed for the channel specified in bits 5 through 7. The ACE line status register contents are stored in bits 8 through 15. The next entry in the receive FIFO is always the data that caused the line status change.

Status Code 6 — Modem Status. A status code of 6 (SW3, bits 1 through 3 = 110) indicates that the modem status register contents have changed for the channel specified in bits 5 through 7. The ACE modem status register contents are stored in bits 8 through 15. If ACE register 7, bit 13 is asserted, modem status reporting is inhibited.

Status Code 7 — Reserved. This status code is presently unused and is reserved for future definition.

3.3.4.3 Channel Change Flag — SW3, Bit 4. If SW3, bit 0 is negated (receive data is valid), this bit is negated to indicate that the channel number and status code in this word are the same as for the previous valid SW3 word. If this bit is asserted, either the status code or the channel number (or both) are different from the last valid SW3 read cycle.

3.3.4.4 Channel Number — SW3, Bits 5 Through 7. Bits 5 through 7 specify the channel number associated with the receive FIFO data or status contained in SW3 bits 8 through 15.

3.3.4.5 Receive Data — SW3, Bits 8 Through 15. Depending on the status code specified, bits 8 through 15 either contain eight bits of valid receive data, the contents of one of the ACE status registers (ACE register 5 or 6), the interface event code byte, or meaningless data.

Alphabetical Index

Introduction

HOW TO USE INDEX

The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables.

INDEX ENTRIES

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections — Reference to Sections of the manual appear as "Sections x" with the symbol x representing any numeric quantity.

- Appendixes — Reference to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.

- Paragraphs — Reference to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph may be found.

- Tables — References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number.

  Tx-yy

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CUT ALONG LINE

USER'S RESPONSE SHEET

Manual Title: Four-Channel Asynchronous Communications Interfaces (CI403 and CI404) Installation and Operation (2263897-9701)

Manual Date: 11 November 1983 **Date of This Letter:** _____

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