Hardware Concepts Session

The 990/10A: Squeezing Five and A Half Boards Down To One

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Abstract

The 990/10A provides the user with a giant stride forward in price/performance. This paper discusses how five and a half boards of the 990/10 were reduced to a single board, and in the process provided a 30-70% improvement in processor speed. What this new design, and its companion, the 990A13 chassis means to the user in regards to price, performance and maintenance is covered, as well as why they are possible.

Introduction

The purpose of this paper is to focus on the heart of the Business System 600 Series of minicomputers, the 990/10A processor and its chassis, the 990A13. The 990/10A gives more performance at a lower price, while consuming considerably less board space and power. These factors give the 990/10A a considerable advantage over the 990/10 which it replaces. The single board 990/10A contains the complete processor, up to 512 K-bytes of error correcting memory, an RS-232 interface, and is designed to comply with the Federal Communications Commission (FCC) regulations on ElectroMagnetic Interference (EMI). This single board functionally replaces five and a half boards of the 990/10 minicomputer. The 990A13 chassis retains the same footprint of the old 13-slot chassis, while providing a greater cooling capability, a larger amperage power supply, and is designed to comply with the FCC regulations on EMI.

A discussion of how these products evolved, and how their improved functionality was achieved follows. These products will also be compared with the ones that they replace on the price/performance

curve. The two sections that follow will discuss the details of each of these products along the lines outlined above, and will be followed with some closing observations.

990/10A Processor

Background The 990/10A is an evolutionary step in the 990 family of minicomputers. It is completely compatible with the CRU and TILINE buses that the other members of the family utilize to interface to peripherals. It also maintains the same board form factor, and is upwards software compatible with the 990/4, 990/5 and 990/10 computers.[1,2]

The 990/10A is implemented on a single full-sized 990 board and includes the processor, TILINE and CRU interfaces, an RS-232 port, and either 256K or 512K bytes of Dynamic Random Access Memory (DRAM). This is achieved through the use of the TMS 99000 microprocessor, several custom Integrated Circuits (ICs), and 64K bit DRAM memory devices.

The design of the 990/10A was undertaken to fulfill three needs. First, it boosted the performance of the 990/10 class machine. Second, it reduced the cost of the 990/10 class machine. And third, it was designed to comply with the FCC EMI regulations.

The TMS 99000 microprocessor retains the memory-to-memory architecture introduced in 1975 with the 990/10 minicomputer and TMS 9900 microprocessor. This architecture was a deviation from conventional architecture. Processors originally had but a single accumulator to handle the logic and arithmetic functions. As time passed and implementation costs fell, processors were designed with multiple accumulators to simplify coding. Finally, with the advances of Medium Scale Integration (MSI) and Large Scale Integration (LSI), machines could be cost effectively designed with general purpose registers. These machines could do the logical and arithmetic operations as had the previous accumulator

implementations, and in addition, could be used for operand address generation and index addressing.

Since the function of registers and memory were basically the same, and because the speed of memory devices was rapidly approaching that of on board registers, the designers of the TMS 9900 and TI 990 chose to take a different approach to their new design. They implemented a memory oriented architecture instead of a register oriented architecture. This implementation was made by creating a pseudo "register file" in main memory, pointed to by a single hardware register in the processor. The primary benefit of this approach was to drastically reduce the work required to perform a context switch. This meant that only three registers (the Work Space Pointer, Status, and Program Counter) in the 990/9900 processor had to be saved and loaded to give the user a clean set of 16 registers. With the register architecture, each of the 16 registers would have had to have been saved and loaded separately. Thus the memory architecture provides a significant time savings during context switching, which is extremely important for interrupt processing and subroutine calls.

Speed of function execution is also an advantage of the 990/9900. Though individual instructions may be slower because of the memory architecture, fewer instructions are usually needed than with a register oriented architecture, and therefore function execution time is faster. For instance, with the 990/9900 to move a word in memory only requires the execution of the MOVE instruction. With the register architecture, the word would have to LOADed into a register, and then SAVEed into the new memory location. This also provides a much easier to program machine, giving a 3:1 typical instruction reduction.[3-5]

Hardware Description The 990/10A processor is implemented with the TMS 99000 microprocessor and a custom Large Scale Integration (LSI) device that handles the memory mapping algorithm. Memory is implemented with 64K by 1 Dynamic Random Access Memory (DRAM)

devices to provide the user with either 256K or 512K bytes of on board memory. Much of the other logic that consumed considerable board space on the 990/10 in Small Scale Integration (SSI) and medium Scale Integration (MSI) devices, have now been reduced to three custom LSI devices on the 990/10A. These ICs are the TILINE control chip, Correction Control chip (CCC), and Communications Register Unit (CRU) chip. Logic array devices have also been used to perform some of the functions previously performed by SSI and MSI devices. A TMS 9902 chip is also incorporated in order to provide an on board RS-232 interface.

Figure 1 gives a block diagram of the 990/10A. Several buses are implemented on the 990/10A board, but the ones of primary interest to the user are the internal memory bus and the TILINE bus. The TILINE bus allows the 990/10A to interface to all 990 TILINE devices, as well as to off board expansion memory. The internal memory bus is an internal, high speed, synchronous bus that allows access from the TMS 99000, TILINE interface, on board memory devices, memory error log register, and multiprocessor interface. Since this internal bus is limited to just the devices mentioned, it has been optimized with regard to on board memory access. Thus, though off board memory can be added, performance with off board memory will always be below that of the on board memory. The various devices that make up the 990/10A will be examined in more detail, and their functions more fully described in the following paragraphs.

TMS 99000. The processing element in the 990/10A is the TMS 99000 microprocessor. This is a Very Large Scale Integration (VLSI) device implemented in Scaled Metal Oxide Semiconductor (SMOS) technology, and is the third generation of the 16 bit 9900 family of microprocessor. It is fully assembly language compatible with the earlier members of the family, the TMS 9900 and TMS 9995, plus it has five new instructions of its own (see the section on functions for details). Use of the TMS 99000 allowed the replacement of 51 devices with the single TMS 99000.[6]

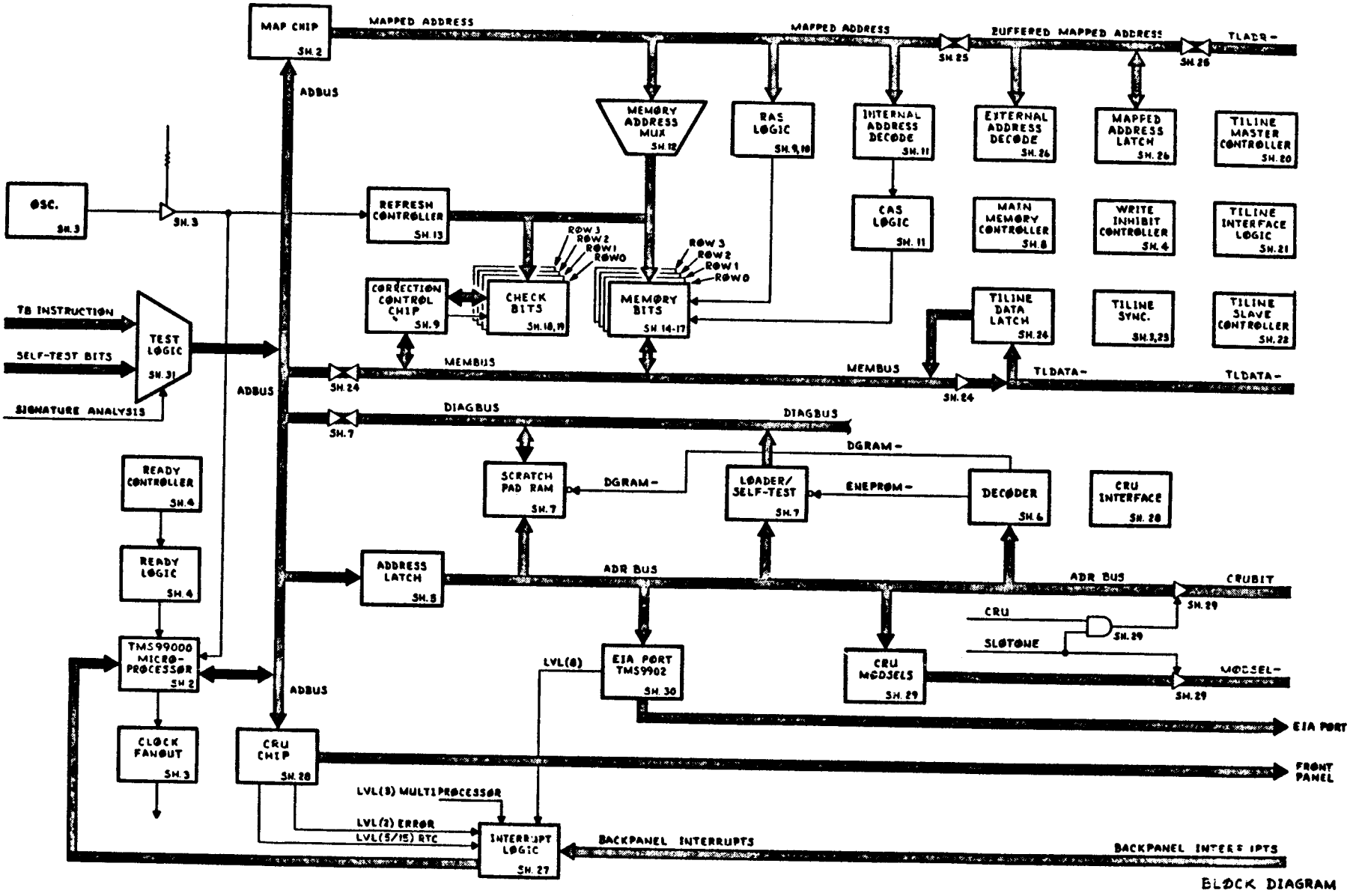

Figure 1 990/10A Block Diagram

MEMORY. The memory devices used on the 990/10A are 64K x 1 bit devices. A typical memory chip used is the TMS 4164. These devices require only a single +5 volt supply, draw the same power, and are more reliable than a single 16K chip, yet provide four times the storage capacity.

MAP CHIP. The MAP chip uses the standard TI Data Systems Group (DSG) algorithm to convert a 15 bit word level logical address from the TMS 99000, into a 20 bit physical address in the 2M byte address space. The physical address is then used to access either on board or external TILINE memory. This also is used to detect attempts to access memory above the largest limit register. In addition, the MAP chip also detects accesses to the TILINE Peripheral Control Space (TPCS) and maps these into high order addresses when operating under the map 0 mapping registers. This custom LSI device contains some 3500 gates, and was able to replace 56 MSI and SSI devices previously providing the mapping function, and reduce the pin count from 934 to just 64.

CORRECTION CONTROL CHIP. This custom LSI device contains the memory error detection and correction logic. The CCC detects and corrects single bit memory errors, and detects double bit errors via six Hamming code bits stored with each word in memory. Logic is also contained on this device to facilitate memory testing. Status information about memory tests, memory size, memory address, and which chip is in error is contained in the memory error log contained on this chip. By going to custom LSI the number of devices to perform this function was reduced from 50 to one, and the pin count reduced to 64 from 828.

CRU CHIP. The CRU chip is the custom LSI device that implements the Communications Register Unit (CRU) interface. It controls the interface to 4,096 inputs and 4,096 outputs that are used for a variety of device interfaces. In addition it also controls access to various functions on the 990/10A board that lie outside the normal 4,096 input/output address range. By going to this LSI

device the chip count was reduced from 61 to 1, and the pin count from 854 to 64.

TILINE CONTROL CHIP. This custom device contains the common logic used by the on board TILINE master and slave device controllers. By integrating this function into a LSI device, 16 MSI and SSI devices were eliminated, and the pin count reduced from 234 to just 40.

LOGIC ARRAYS. Logic arrays have been used on the 990/10A for a number of functions, and provide a large reduction in components. Functions incorporated into the logic arrays include: portions of the memory controller; row decode logic; write inhibit controller; bus status code decoder; memory address and CRU decoder; memory refresh controller; TILINE master controller; and TILINE slave controller.

TMS 9902. The on board RS-232 port of the 990/10A is implemented using the TMS 9902 asynchronous controller chip. This provides an asynchronous interface with many user programmable features, including: five to eight bit character lengths; programmable data rate generation; interval timer with 64 to 16,320 microsecond resolution; even, odd or no parity; and one, one and a half, or two stop bits. The TMS 99000 processor accesses the TMS 9902 via the CRU bus, thus providing an interface to a printer or terminal.

LOADER/SELF-TEST ROM. This Read Only Memory (ROM) contains 1K bytes of loader code, and 7K bytes of self-test code separated into eight 1K byte pages. Upon power up, or initiation of the LOAD cycle, the self-test code is executed. Two Light Emitting Diodes (LEDs) are provided at the edge of the 990/10A board to indicate self-test results. One indicates a failure in the data path kernel, while the other indicates failures in components outside the kernel. The kernel consists of the TMS 99000, address latch, loader/self-test ROMs, the scratchpad RAM, the ready controller and logic, and oscillator (see figure 1). Once the self-test has successfully passed on the data path kernel, on

board memory, TILINE and CRU logic, the EIA port, and multiprocessor logic is tested. If a failure is found, and it is not a catastrophic error, an indication is displayed upon the 990A13 operators panel to indicate the segment of self-test that failed. The loader operation is described in a later paragraph on the operation of the operator panel hardware on the 990A13 chassis.

Functionality The 990/10A provides three functions above and beyond those that were provided by the 990/10. These are the on board RS-232 port, the multiprocessor interface, and five new instructions.

The RS-232 port is a general purpose asynchronous port that allows the 990/10A to interface to the model 810 or 840 printers, or model 940 terminal. This port is accessed as a CRU device via the on board TMS 9902 asynchronous controller. Both DX10 and DNOS support devices from this terminal.

A multiprocessor interface is provided to facilitate interprocessor communications in multiprocessor environments. This interface consists of a scheme of attention and acknowledge interrupts. With this scheme, an auxiliary processor can interrupt the host processor via a backplane interrupt, and the host can interrupt the auxiliary via its level three interrupt. Interrupts are set and cleared by writing to words in the TPCS.

The five new instructions on the 990/10A are new for the 990/10 class machine, but are compatible with instructions existing on the 990/12. These new instruction are BIND (branch indirect), DIVS (signed divide), MPYS (signed multiply), LST (load status register), and LWP (load workspace pointer). Further details on these instructions can be found in the assembly language manual.[5]

Packaging A major attribute of the 990/10A is that is contained on a single board. This was made possible through the use of the

custom LSI circuits and logic arrays described earlier, the new 64K DRAM memory devices, and the use of a fine line printed circuit board. A fine line printed circuit board means that interconnecting lines are so small that two can be run between component pads. Standard printed circuit boards allow only a single line to be run between component pads, thus the printed circuit board can be made with fewer layers, and therefore are less costly. The 64K DRAM devices offer a four fold improvement in memory density for the same size device. The use of custom LSI circuits and logic arrays, enable 888 devices on the 990/10 to be replaced with 229 devices on the 990/10A, thereby shrinking the board space required from 846 square inches on five and a half boards to 154 square inches on just one board. It is this same use of custom LSI devices, though packaged a different way, that allows roughly the equivalent of a 990/10A to be contained in a 940 terminal enclosure (the Business System 300).[7]

Another factor incorporated into the 990/10A packaging is compliance with the FCC EMI regulations. Two principal changes were made to the normal 990 board layout to meet the FCC EMI specifications. First, a metal shield was added to the exposed edge of the 990/10A board. This, in conjunction with the shields on other boards and the 990A13 chassis, forms a barrier around the various boards generating EMI in the chassis. The second change was the addition of a ground plane around the edge of the board. More details of the FCC and their EMI requirements are presented in a companion paper.[8]

Performance The performance of the 990/10A is superior to the 990/10 regardless of how they are compared. In slot space, the 990/10A takes but a single slot, where the equivalent 990/10 function takes five and a half slots. This provides the user with four and a half slots that can be filled with expansion boards, without going to an expansion chassis. Looking at this in terms of savings, the 990/10A user has four and a half more slots of usable space before he has to purchase an expansion chassis. An expansion chassis would be an expenditure of $4,000, or a prorated

cost of $308 per slot. In power dissipation the 990/10A uses only 30 watts, where the equivalent 990/10 configuration uses 82 watts.

In throughput, the 990/10A provides 30-70% improvement over the 990/10, depending upon the instruction mix (highest performance improvements are for CPU intensive tasks, and lowest for I/O intensive tasks). The CPU and memory cycle and access times for the 990/10A are listed in table 1 below.

Table 1
CPU and Memory Cycle and Access times

Memory Cycle Time	350ns.
Memory Access Time	200ns.
CPU Cycle Time	600ns.
CPU Access Time	600ns.

Since execution time of individual instructions are determined by a mix of clock cycles, wait states and memory access for each instruction, determining the execution time for a specific instruction is difficult. To further complicate calculation of instruction execution times, accesses to TILINE (off board) memory requires more clock cycles due to overhead and synchronization required. Other factors that complicate instruction speed calculation are the introduction of TILINE slave cycles, and wait states introduced because of refreshing of the dynamic RAM chips. As a result, the best way to determine average execution time of an instruction or string of instructions is through the use of loop and repetitive execution of the instructions in question. It was by this means that the 30-70% improvement figure in throughput was arrived at.

990A13 Chassis

Chassis Evolution With the 990/10 three different chassis were offered, the six slot, 13-slot and 17-slot. However, these had several drawbacks. First, they did not comply with FCC EMI regulations. Second, only the 17-slot chassis allowed a simple upgrade path to the 990/12. Third, Available power limits were

being approached because of the more complicated, smarter boards being introduced. And lastly, heat dissipation limits were being approached by those same complicated, intelligent boards. To solve all of these needs the 990A13 chassis was developed.

Hardware Description The 990A13 chassis is a 13 slot chassis designed to accomodate both the 990/10A and 990/12 LR processors, and, in addition, will accomodate all existing 990 style boards. The power supply has been improved to provide higher currents on the available buses. Table 2 lists the current capacities of the 990A13. The capacities listed are shown in amperes, both with and without the optional standby power supply.

Table 2
990A13 Chassis Power Capacities

	Standby Power Supply	
	Without	With
+5 Main	65	59
+12 Main	4	2
-12 Main	2	2
- 5 Mem	0.1	0.1
+12 Mem	0	2
+ 5 Mem	0	6

A major change in the 990A13 chassis over the old chassis is the new operators panel. The new operators panel consists of four hexadecimal displays, and four switches. The display provides all the information that the old programmers panel displayed, is more compact, and easier for the user to read. The switches provide the functions of HALT, RUN, LOAD and ALTERNATE LOAD to the user. The loader ROMs on both the 990/10A and 990/12 LR cause the LOAD switch to be reset, and a load attempted from unit 0 at TILINE address 0F800. The ALTERNATE LOAD switch causes the system to attempt to boot from the following devices in the order indicated:

* Maintenance Diagnostic Unit
* Online magnetic tape unit at 0F880, units 0-3
* Online, unprotected disk unit at 0F800, units 0-3, at 0F810, units 0-3, and at 0F820, units 0-3.
* First online, protected disk unit at 0F800, units 0-3, at 0F810, units 0-3, and at 0F820, units 0-3.

If no device is found ready, then the loader firmware continues searching, by starting back at the magnetic tape unit at 0F880. The search will continue until a ready device is found, or the processor is halted.

Also available for use with the 990A13 chassis is a programmer/test panel. This is a device that allows the user full access to the Program Counter (PC), Workspace Pointer (WP), and status register. This unit is designed for table top operation, and is easily installed via a connector behind the plastic grille at the front of the chassis. Because it is so easy to attached, a single unit may be used to service a number of systems.

Functionality Three major functional improvements are found in the 990A13 chassis over the old chassis. First, power supply capacity has been boosted. Second, airflow design was changed to provide higher heat dissipation. And last, the chassis was designed to meet FCC level A regulations for EMI.

Packaging As far as packaging goes, the 990A13 has the same dimensions as the old 13-slot chassis, and may be used to replace a 13-slot chassis. The 990A13 has taken on a new look. It has a gray plastic front panel that is consistent with the rectilinear look of the Business System series of computer systems. Cooling air flow has been changed to draw the cooling air from the front, and hence from the cooler air outside of the cabinet. This also facilitates easy change of the air filters by office personnel, as they are located just behind the plastic front panel.

Performance Heat dissipation in the 990A13 chassis is superior to that in the old 13-slot chassis. Not only is more air moved across the boards, but a more uniform air flow is achieved throughout the 13 slots in the 990A13. To further enhance the cooling ability of the 990A13, the cooling air is pulled from the front of the chassis, and hence from the ambient air in the office where the system is installed. This air is much cooler than the air drawn from inside the cabinet, as with the 13-slot chassis.

The capacity of the power supply was increased to provide 65A of +5 main, as compared with 40A in the old 13-slot chassis. Shielding was provided so that when TI circuit boards designed to comply with FCC regulations are used with this chassis, radiated EMI will be below the level A limits. The new operators panel provides much of the same information as the old programmers panel, yet is much simpler to operate for the less sophisticated user.

Summary

The performance of the 990/10A and 990A13 chassis are superior to the 990/10 and 13-slot chassis regardless of how they are compared. The 990/10A gives a 60% improvement in available chassis slots, 30-70% improvement in throughput, and a 82% decrease in power consumption over the comparable 990/10 configuration. The 990A13 chassis provides a 62% improvement in power capacity. Both are designed to meet FCC level A EMI regulations, And all of this is available at a price 36% less than the equivalent 990/10 package.

Another aspect of the 990/10A and 990A13 chassis is their greatly improved reliability and serviceability. A good indication of the improved reliability may be obtained by comparing service rates. A 990/10A with 512KB in a 990A13 chassis costs $71 a month for service, while a 990/10 with 512KB in the 13-slot chassis costs $227 per month. This is a 69% decrease in monthly service costs for the 990/10A package over the comparable 990/10 configuration.

Comparing the five year cost of ownership for a comparable 512K-byte 990/10A with 990A13 chassis, and a 990/10 with 13-slot chassis, gives a good indication of the savings associated with the newer hardware. To evaluate these two alternatives, the initial costs of the respective packages are taken, along with the costs of maintaining them for five years. Calculating the present value of these cash flows at an annual interest rate of 15%, we find that the 990/10A gives a present value of $19,987, while the

990/10 has a present value of $35,707. Thus the 990/10A and 990A13 chassis will cost the user 44% less than the comparable 990/10 configuration over a five year period.[9] An in depth examination of how to evaluate computer systems and estimate their lifetime costs is discussed elsewhere.[10-14]

About the Author

John Purvis is a Product Manager of Business System computers with the Data Systems Group of Texas Instruments in Austin, Texas. He has a Bachelor of Science degree in Electrical Engineering from the University of Houston (1973), and a Masters of Science in Electrical Engineering from the University of Texas (1982). He is a register Professional Engineer in Texas, a member of both the Institute of Electrical and Electronics Engineers (IEEE) and the Instrument Society of America (ISA), and has been working in the computer field for 10 years. Other papers authored or coauthored with Ivan Erickson, cover the areas of computer systems, data communications, and computer system cost analysis. These papers have been presented at TI-MIX, ISA and ISMM conferences. Articles have appeared in publications such as **InTech**, and **Systems & Software.**

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