TeleVideo® TS 816 Maintenance Manual

TeleVideo® Systems, Inc.

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TeleVideo Systems, Inc. 1170 Morse Avenue Sunnyvale, California 94086 408/745-7760

PREFACE

Any comments and suggestions on this manual are welcome. Please address them to:

TeleVideo Systems, Inc.
c/o Customer Service Computers
1170 Morse Ave.
Sunnyvale, CA 94086

TeleVideo Systems, Inc. reserves the right to make improvements to products without incurring any obligations to incorporate such improvements in products previously sold. Specifications and information herein are subject to change without notice.

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STATEMENT OF LIMITED WARRANTY

TeleVideo Systems, Inc. ("TeleVideo") warrants to Buyer that products, except software, manufactured by TeleVideo will be free from defects in material and workmanship. TeleVideo's obligations under this warranty will be limited to repairing or replacing, at TeleVideo's option, the part or parts of the products which prove defective in material or workmanship within 90 days after shipment by TeleVideo, provided that Buyer gives TeleVideo prompt notice of any defect and satisfactory proof thereof. Products may be returned by Buyer only after a Return Material Authorization number ("RMA") has been obtained from TeleVideo by telephone or in writing. Buyer will prepay all freight charges to return any products to the repair facility designated by TeleVideo and include the RMA number on the shipping container. TeleVideo will deliver replacements for defective products or parts on an exchange basis to Buyer, freight prepaid to the Buyer or the Customer. Products returned to TeleVideo under this warranty will become the property of TeleVideo. With respect to any product or part thereof not manufactured by TeleVideo, only the warranty, if any, given by the manufacturer thereof, will apply.

EXCLUSIONS

This limited warranty does not cover losses or damage which occurs in shipment to or from Buyer, or is due to, (1) improper installation or maintenance, misuse, neglect or any cause other than ordinary commercial or industrial application, or (2) adjustment, repair or modifications by other than by TeleVideo-authorized personnel, or (3) improper environment, excessive or inadequate heating or air conditioning and electrical power failures, surges or other irregularities or (4) any statements made about TeleVideo's products by salesmen, dealers, distributors or agents, unless confirmed in writing by a TeleVideo officer.

THE FOREGOING TELEVIDEO LIMITED WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, WHETHER ORAL, WRITTEN, EXPRESS, IMPLIED OR STATUTORY. IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE WILL NOT APPLY. TELEVIDEO'S WARRANTY OBLIGATIONS AND BUYER'S REMEDIES HEREUNDER ARE SOLELY AND EXCLUSIVELY AS STATED HEREIN. TELEVIDEO MAKES NO WARRANTY WHATSOEVER CONCERNING ANY SOFTWARE PRODUCTS, WHICH ARE SOLD "AS IS" AND "WITH ALL FAULTS."

TELEVIDEO'S LIABILITY, WHETHER BASED ON CONTRACT, TORT, WARRANTY, STRICT LIABILITY OR ANY OTHER THEORY, SHALL NOT EXCEED THE PRICE OF THE INDIVIDUAL UNIT WHOSE DEFECT OR DAMAGE IS THE BASIS OF THE CLAIM. IN NO EVENT SHALL TELEVIDEO BE LIABLE FOR ANY LOSS OF PROFITS, LOSS OF USE OF FACILITIES OR EQUIPMENT, OR OTHER INDIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES.

SPARE PARTS AND REPAIR PRICE LISTS

This section contains the Repair Price List for Computers and the Systems Spare Parts Price List in effect at the printing date of this manual. Use these lists for estimating repairs: prices are subject to change without prior notice.

Repairs Price List for Computers

July 1, 1982

REPAIR	Price
Basic Repair Charge	$ 70.00
INDIVIDUAL REPAIR CHARGES	
Logic Board TS800 (B900005-001)	$135.00
Logic Board TS800A, TS802, TS802H (B900019-001)	150.00
Logic Board TS801 (B900006-001)	175.00
Logic Board TS806 (B900007-001)	250.00
Logic Board TS816 (B900008-001)	350.00
Floppy Controller TS802, TS802H (B900017-001)	50.00
Winchester Disk Controller TS806 (B900010-001)	175.00
Interface Board TS816 (B900009-001)	50.00
Keyboard Repair TS800, TS800A, TS802, TS802H (K030331-001)	50.00
Power Supply Module TS800 (P100005-001) and TS800A (BC-01642)	50.00
Video Module TS800, TS800A, TS802, TS802H (BC-01643)	50.00
5" Floppy Drive (M210001-001)	160.00
Tape Controller TS806C (B900018-001)	95.00
Logic Board Cartridge Tape Drive	300.00
Head Module Cartridge Tape Drive	400.00
Motor Cartridge Tape Drive	250.00
5" Winchester Drive (M210002-002)	160.00
8" Winchester—Head Disk Assembly	700.00
8" Winchester—Disk Controller	600.00
8" Winchester—Power Amplifier	253.00
Computer Power Supply	110.00
Picture Tube Broken TS800, TS800A, TS802, TS802H (T300002-002)	214.00
Picture Tube and Top Case TS800, TS800A, TS802, TS802H	270.00
Top Case Broken TS800, TS800A, TS802, TS802H	80.00
Bottom Case Broken TS800, TS800A, TS802, TS802H	100.00
Top/Bottom Case Broken Computer	80.00
Front/Rear Panel Broken Computer	60.00

Out of Warranty

Customer to return defective replaceable module freight prepaid to the factory, 1170 Morse Avenue, Sunnyvale, CA 94086. TeleVideo will send replacement repaired module, billing per above price schedule plus return freight.

Prices subject to change without notice.

TeleVideo Systems, Inc.

1170 Morse Avenue • Sunnyvale, CA 94086

Eastern Regional—(212) 308-0705 • Northeast Region—(617) 369-9370 • Midwest Region—(312) 969-0112
South Central Region—(214) 258-6776 • Southwest Region—(714) 752-9488 • Northwest Region—(408) 745-7760
Southeast Region—(404) 447-1231 • European Sales—(31) 075-28-7461 TLX: 844-19122 (TLVDO NL)

Systems Spare Parts Price List

TeleVideo Systems, Inc.

TELEVIDEO COMPUTER SYSTEMS
PARTS LIST

10-27-82

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
			LITERATURE/MANUALS [class A]
B300017-001	2004200	20.00	Guide, Installation & User's TS 800A
B300014-001	2003700	20.00	Guide, Installation & User's TS 802
B300015-001	2003900	20.00	Guide, Installation & User's TS 802H
B300039-001	2134000	20.00	Guide, Installation & User's TS 802G
B300008-001	2003000	10.00	Guide, Installation & User's TS 806
B300022-001	2004700	10.00	Guide, Installation & User's TS 806C
B300034-001	2133400	10.00	Guide, Installation & User's TS 806H
B300009-001	2003100	10.00	Guide, Installation & User's TS 816
	2150300	50.00	Guide, User's TELEPLAN
B300010-001	2003200	25.00	Manual, Mmmost
B300012-001	2003400	50.00	Manual, CP/M
050054	2150400	40.00	Manual, TELEVIDEO - COBOL
B300007-002	2131200	50.00	Manual, Maintenance TS 801
B300038-001	2133900	50.00	Manual, Maintenance TS 800A, 802, 802H
	2162200	50.00	Manual, Maintenance TS 806 & TS 806C
B300009-002	2131400	50.00	Manual, Maintenance TS 816
			KITS [class B] Contents at end of List
A300001-002	2000100	134.28	Kit, Spare Parts, Pwr Sply - Video Module
A300001-008	2000700	300.12	Kit, Spare Parts, Logic Board - Systems
	2202800	90.88	Kit, Spare Parts, Mech - TS 802/800A
	2202900	244.80	Kit, Spare Parts, Logic Board WDC
	2203000	199.59	Kit, Spare Parts, Logic Board FDC
	2228400	306.78	Kit, Spare Parts, System Data Cables
			MAJOR ASSEMBLIES/PRINTED CIRCUIT BOARDS [class B]
B900005-001	2011000	1,195.00	PCB Asy Logic Board TS 800 (Obs)
B900019-001	2018000	1,199.67	PCB Asy Logic Board TS 800A/802
B900019-002	2018001	1,199.67	PCB Asy Logic Board TS 802H
B900022-001	2019500	1,361.22	PCB Asy Logic Board TS 802G
B900006-001	2011500	1,465.74	PCB Asy Logic Board TS 801 (Obs)
B950001-001	2198900	1,474.14	PCB Asy Mod 8" Flpy TS 801
B900007-001	2012000	1,251.12	PCB Asy Logic Board TS 806
B900018-002	2017501	658.32	PCB Asy Logic Board TS 806C
B900008-001	2012500	1,765.83	PCB Asy Logic Board TS 816
B900009-001	2013000	360.00	PCB Asy Logic Board TS 816U
BC-01643	2195800	93.00	Video Module
B900010-001	2013500	866.19	PCB Asy Winchester Disk Controller
B900017-001	2017000	210.75	PCB Asy Floppy Disk Cont TS 802 (Dau Bd)
B900021-001	2019000	656.87	PCB Asy Graphics
P100001-001	2109100	561.00	Pwr Sply SW 130W (Obs) See 2109200
P100002-001	2109200	654.00	Pwr Sply SW 100W TS 801/806
P100002-002	2109201	827.34	Pwr Sply SW 150W TS 802/802H

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
P100002-003	2109202	954.00	Pwr Sply SW 200W TS 816/806C
P100005-001	2191500	103.00	Pwr Sply 3A/5V TS 800A/800
			STORAGE DEVICES [class C]
M210001-001	2099200	591.00	Flpy 48 TPI D/S 5 1/4" .5 MB
M210002-002	2099301	2,025.00	Disk Dr Winch 5 1/4" 9.57 MB
M210003-001	2099400	4,140.00	Disk Dr Winch 8" 23.40 MB
M210004-001	2099500	2,100.00	Cartridge Mag Tape Drive W/Codec Bd
			MISC. MAJOR PARTS [class D]
T300002-002	2049300	179.00	Tube CRT Black/Green 12"
K030331-001	2090200	175.00	PCB Asy Kybd TS 800A/802
M210006-001	2174800	111.90	Cartridge, Tape
I830001-001	2221400	228.00	Disk DS/DD 40 Trk/Side 5 1/4" (20 ea)
I830001-002	2223900	255.00	Disk DS/DD 40 Trk/Side 5 1/4" Formatted 20
M400005-001	2099800	70.20	Case Bottom TS 801 & 806
M400006-001	2099900	70.20	Case Top TS 801 & 806
M400015-001	2100600	110.00	Case Top TS 802
M400016-001	2100700	85.00	Case Bottom TS 802
M400017-001	2100800	40.00	Bezel TS 802
M400021-001	2141700	70.20	Case Bottom TS 800A
M400022-001	2141800	97.80	Case Top TS 800A
M400023-001	2141900	20.00	Bezel TS 800/800A
M410014-001	2103100	70.00	Case Top TS 816
M410015-001	2103200	180.00	Case Bottom TS 816
M470009-001	2204200	25.00	Case Top Kybd TS 800A/802'S
CRT-04002	2198000	35.00	Case Bottom Kybd TS 800A/802'S
M470010-001	2170700	10.00	Bezel Kybd TS 800A/802'S
			SOFTWARE/FIRMWARE
I800000-001	8000001	18.90	IC 2332 Term Portion TS 800 (F000)
I800000-007	8000007	18.90	IC 2332 Term Portion TS 800 (E000)
I800000-002	8000002	16.92	IC 2332 Char Gen Upper Char Cell
I800000-003	8000003	16.92	IC 2332 Char Gen Lower Char Cell
I800000-009	8000009	23.28	IC Prog ROM Kybd TS 800A/802
I800000-018	8000018	34.50	IC 2716 Sys Prog EP Kybd TS 800A/802
I800000-023	8000023	55.50	IC 2532 Sys Prog EP 450ns TS 800/801
I800000-024	8000024	55.80	IC 2532 Sys Prog EP 450ns TS 806
I800000-045	8000045	37.50	IC Sys Prog EP Z80 Portion TS 800A/802
I800000-046	8000046	37.50	IC Sys Prog EP Lower Term Firmware
I800000-047	8000047	37.50	IC Sys Prog EP Higher Term Firmware
I800000-050	8000050	37.50	IC Sys Prog EP Z80 Portion TS 802H
I800000-053	8000053	30.90	IC 2532 Sys Prog EP 450ns TS 816 /W Code
I800000-054	8000054	30.90	IC Sys Prog EP TS 806C Firmware
I810000-023	8100023	100.00	Listing Sys Prog TS 800/801 *
I810000-024	8100024	100.00	Listing Sys Prog TS 806 *
I810000-045	8100045	100.00	Listing 800A, 802, [Z80 Portion] *
I810000-046	8100046	500.00	Listing 800A, 802, 802H [6502 Portion] *
I810000-050	8100050	100.00	Listing TS 802H [Z80 Portion] *

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
I810000-053	8100053	100.00	Listing Sys Prog EP TS 816 W/Code *
I810000-054	8100054	100.00	Listing Firmware EP TS 806C *

* Require non-disclosure agreements and letter of intended use.

I800000-025	8000025	55.80	IC Diagnostic EP TS 801
I800000-026	8000026	55.80	IC Diagnostic EP TS 800
I800000-027	8000027	55.80	IC Diagnostic EP TS 806
I800000-052	8000052	55.80	IC Diagnostic EP TS 806C
I800000-035	8000035	23.70	IC L2-7 Sys Prog ROM WDC
I800000-036	8000036	23.70	IC MX-7 Sys Prog ROM WDC
I800000-037	8000037	23.70	IC FX-7 Sys Prog ROM WDC

CABLES/CONNECTORS/WIRE

B510000-001	2005700	25.44	Cbl Asy, Kybd TS 800A/802
B510006-014	2006201	54.60	Cbl Asy, 14" Lgc To Tape, Lgc To TS 816U
B510007-010	2128500	19.32	Cbl Asy, 20 Pin 10" TS 806H Outside
B510009-010	2006300	23.40	Cbl Asy, 34 Pin 10" TS 806H Outside
B510010-016	2006400	46.20	Cbl Asy, 50 Pin 16" Logic To Winch TS 816
B510011-003	2006500	32.70	Cbl Asy, 16 Pin 3" TS 806C RS 422 Internal
B510011-008	2006501	16.02	Cbl Asy, 16 Pin 8" TS 806 RS 422 To Lgc
B510012-007	2006600	36.00	Cbl Asy, 34 Pin 7" TS 801/806 PRINTER
B510013-001	2006700	29.64	Cbl Asy, 34 Pin 12" TS 801 Logic To Flpy
B510014-012	2006800	14.22	Cbl Asy, 20 Pin 12" TS 802H/GH WDC To Winch
B510014-015	2006801	14.52	Cbl Asy, 20 Pin 15" TS 806 WDC To Winch
B510015-015	2006900	18.60	Cbl Asy, 34 15" TS 802H Dau Bd/Flpy WDC/Winch
B510015-018	2006901	18.96	Cbl Asy, 34 Lgc To Flpy/WDC To Winch TS 806
B510017-013	2007000	20.28	Cbl Asy, 40 Pin 13" TS 806 Lgc To WDC
B510017-016	2007001	32.28	Cbl Asy, 40 Pin 16" TS 802H/GH Dau Bd To WDC
B510018-001	2007100	51.00	Cbl Asy, 50 Pin 3" TS 806C Logic To Tape
B510018-012	2007101	42.00	Cbl Asy, 20 Pin 12" TS 806 Internal (For 806H)
B510023-001	2007300	29.16	Cbl Asy, 34 Pin 14" TS 802/G Dau Bd To Flpy
B510031-006	2007600	42.60	Cbl Asy, 20 Pin 12" TS 806H Internal
B510032-005	2007700	54.00	Cbl Asy, 34 Pin 10" TS 806H Internal
B510033-009	2007800	73.08	Cbl Asy, 34 Pin 16" TS 806 Internal (For 806H)
B520002-005	2007900	28.00	Harness Asy, Power Cabel 16" TS 801/806
B520003-012	2136500	28.00	Harness Asy, Power Cabel 12" TS 801/806
B520004-024	2008000	12.84	Harness Asy, Power Cabel 24" TS 816
B520005-001	2008101	69.60	Harness Asy, Tape Cassette Pwr-1
B520006-001	2008201	28.08	Harness Asy, Tape Cassette Pwr-2
B520010-014	2008400	10.20	Harness Asy, 1.00 Reset Switch 3 Pin 14"
B520010-015	2008401	20.40	Harness Asy, 1.00 Reset Switch 3 Pin 15"
B520013-001	2176200	50.00	Harness Asy, Power TS 816
B520014-001	2008600	28.00	Harness Asy, Power TS 802H
B520015-014	2008700	30.36	Harness Asy, Power Floppy General 14"
B520016-001	2008800	28.00	Harness Asy, Winchester/Serv. Board TS 816
B520017-001	2008900	28.00	Harness Asy, Tape Cassette Pwr 1 & 2
B520018-001	2135800	28.00	Harness Asy, Power TS 802G
M200201-001	2097800	10.62	Connector 25 Pin D-SUB FEM-PCB Mount
M200202-001	2097900	2.22	Connector RJ11 FEM-PCB Mount (AMP)
M200207-001	2098000	9.60	Connector 15 Pin D-SUB FEM-PCB Mount RS422

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
M200208-003	2174401	8.10	Connector 50 Pin Header - Angle
M200209-002	2098103	3.06	Connector 16 Pin Header - Straight
M200209-003	2098108	7.56	Connector 50 Pin Header - Straight
M200209-004	2098107	4.68	Connector 40 Pin Header - Straight
M200209-005	2098106	4.56	Connector 34 Pin Header - Straight
M200209-006	2098104	2.76	Connector 20 Pin Header - Straight
M200209-007	2098100	.72	Connector 3 Pin Header - Straight
M200215-001	2098300	1.80	Connector 2 Position Jumper
M200601-006	2098703	1.74	Connector 2 Pin Right Angle Molex
M200603-002	2098800	.72	Connector 2 Pin Straight Wafer
M200603-003	2098801	3.72	Connector 3 Pin Straight Wafer
M200603-005	2098802	.72	Connector 5 Pin Straight Wafer
M600008-001	2109000	19.87	Pwr Cord 3 Conductor/3 Prong 6 FT
			CAPACITORS
C600100-004	2024700	.72	Cap Mica 100pf 50V 5%
C600100-005	2024900	.72	Cap Mica 47pf 50V 5%
C600100-006	2025100	.72	Cap Mica 150pf 500V 1%
C600100-007	2025300	.95	Cap Mica 330pf 500V 5%
C600100-008	2025500	1.07	Cap Mica 390pf 500V 5%
C700100-001	2025700	.72	Cap Electrolytic 22uf 15V
C700100-002	2025900	1.74	Cap Tantalum .68uf 50V
C700100-003	2026100	.72	Cap Electrolytic 22uf 50V
C700100-005	2026300	2.40	Cap Tantalum 3.3uf 50V 10%
C700100-009	2027100	1.98	Cap Tantalum 10uf 25V 10%
C700100-010	2027300	.72	Cap Electrolytic 10uf 16V 20%
C700100-011	2027500	.96	Cap Tantalum 4.7uf 16V 10%
C700100-014	2028100	2.16	Cap Mylar .0068uf 100V 5%
C700100-015	2028300	.72	Cap Electrolytic 2.2uf 63V
C700100-017	2137700	.72	Cap Electrolytic 100uf 2V
C900100-001	2028700	.72	Cap Ceramic .01uf 16V 20%
C900100-002	2028900	.72	Cap Monolythic .01uf 50V 10%
C900100-003	2029100	.72	Cap Ceramic 330pf 50V 20%
C900100-004	2029300	.72	Cap Monolythic 330pf 100V 20%
C900100-006	2029700	.72	Cap Monolythic 22pf 1KV 20%
C900100-007	2029900	.72	Cap Monolythic 68pf 1KV 20%
C900100-008	2030100	.72	Cap Ceramic 0.1uf 50V 10%
C900100-011	2030700	1.08	Cap Monolythic 100pf 100V 5% (Radial Lead)
C900100-012	2030900	2.04	Cap Ceramic 1.0pf 1KV Spark Gap
C900100-013	2031100	1.44	Cap Monolythic 82pf 50V 5%
C900100-014	2031300	.72	Cap Ceramic 0.1uf 16V +80% -20%
C900100-015	2137800	.72	Cap Ceramic Monolythic 0.33uf
CC-50221SL	2195900	.72	Cap Ceramic 220PF 50V
CE-10107S	2196000	.72	Cap Electrolytic 100uf 50V
CE-10226SH	2196100	.72	Cap Electrolytic 22uf 100V
CE-10228S	2196200	2.28	Cap Electrolytic 2.2kuf 10V
CE-16107SH	2196300	6.60	Cap Electrolytic 100uf 160V
CE-16226SH	2196400	1.27	Cap Electrolytic 22uf 160V
CE-16227S	2199300	.72	Cap Electrolytic 220uf 16V
CE-35338S	2196500	6.91	Cap Electrolytic 3.3kuf 35V

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION	
CE-35478S	2196600	6.56	Cap Electrolytic	4.7kuf 16V
CM-16475S	2196700	.72	Cap Electrolytic	4.7uf 16V
CM-20682H	2196800	.72	Cap Mylar	.0068uf 200V
CM-50102	2196900	.72	Cap Mylar	.001uf 50V
CM-50103	2197000	.72	Cap Mylar	.01uf 50V
CM-50473	2197100	.72	Cap Mylar	.047uf 50V
CM-50474	2197200	1.44	Cap Mylar	.47uf 50V
CM-60104H	2197300	1.35	Cap Mylar	.1uf 600V
CN-15206S	2197400	4.63	Cap	.22uf 50V
CO-40473H	2197500	1.86	Cap Mylar	.047uf 400V
CT-35334	2198100	1.20	Cap Tantalum	.33uf 35V
CT-35338S	2198200	1.68	Cap Electrolytic	470uf 35V

INTERGRATED CIRCUITS

I740010-000	2024000	2.20	IC 74S00	
I740010-001	2024200	1.72	IC 74LS00	
I740010-003	2024600	2.41	IC 74S04	
I740010-004	2024800	1.80	IC 74LS04	
I740010-006	2025200	1.80	IC 74LS08	
I740010-007	2025400	1.80	IC 74LS10	
I740010-009	2025800	1.86	IC 74LS32	
I740010-010	2026000	2.55	IC 74LS42	
I740010-011	2026200	1.80	IC 74LS51	
I740010-012	2026400	3.58	IC 74S74	(TI, SIG, NAT, AMD)
I740010-013	2026600	1.80	IC 74LS74	(TI, SIG)
I740010-014	2026800	2.07	IC 74LS86	
I740010-015	2027000	2.00	IC 74LS109	
I740010-016	2027200	3.18	IC 74LS139	(TI, SIG, NAT, FAIR, AMD)
I740010-017	2027400	2.76	IC 74LS157	
I740010-018	2027600	4.56	IC 74LS163	(TI)
I740010-019	2027800	5.04	IC 74LS166	
I740010-020	2028000	4.14	IC 74LS173	
I740010-021	2028200	3.18	IC 74LS174	
I740010-023	2028600	2.76	IC 74LS367	
I740010-024	2028800	3.48	IC 74LS373	
I740010-025	2029000	3.48	IC 74LS374	
I740010-026	2029200	4.14	IC 75188N	
I740010-027	2029400	4.14	IC 75189AN	
I740010-031	2030200	2.58	IC NE555	
I740010-054	2034800	2.05	IC 7406	(TI, NAT)
I740010-057	2035400	1.92	IC 7414	(NAT, TI)
I740010-059	2035800	9.75	IC 2114-ICB Static RAM	(GTE, TI, NEC, FUJ)
I740010-061	2036200	5.76	IC N8T245N	(SIG, TI)
I740010-063	2036600	2.70	IC 74LS191	(TI, NAT)
I740010-067	2037400	1.56	IC 74LS365	(TI, SIG, AMD, NAT, MOT)
I740010-068	2037600	3.48	IC 74LS273	(TI, SIG, AMD, NAT, MOT)
I740010-069	2037800	8.82	IC 74S240	(TI, SIG, AMD, NAT, MOT)
I740010-070	2038000	1.74	IC 74LS175	(TI, SIG, AMD, NAT)
I740010-071	2038200	2.52	IC 74S157	(TI, SIG, AMD, NAT)
I740010-072	2038400	1.50	IC 74S133	(TI, SIG, AMD, NAT)

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION	
I740010-073	2038600	9.54	IC 74S124	(TI)
I740010-074	2038800	1.80	IC 74S32/629	(TI, SIG, AMD, NAT)
I740010-075	2039000	1.26	IC 7416	(TI, SIG, AMD, NAT)
I740010-076	2040000	1.14	IC 74LS11	(AMD, TI, SIG)
I740010-077	2040200	26.70	IC WD2143-01	(WES DIG)
I740010-078	2040400	35.70	IC WD1691	(WES DIG)
I740010-079	2040600	113.70	IC FD1793-02	(WES DIG)
I740010-080	2040800	6.60	IC 93S16	(FAIR, AMD)
I740010-081	2041000	1.68	IC 74LS138	(TI, SIG, NAT, FAIR, AMD)
I740010-082	2041200	1.08	IC 74LS27	(TI, SIG, NAT, FAIR, AMD)
I740010-083	2041400	1.44	IC 74S10	(TI, SIG, NAT, FAIR, AMD)
I740010-084	2041600	1.14	IC 74LS02	(TI, SIG, NAT, FAIR, AMD)
I740010-085	2041800	1.44	IC 74S02	(TI, SIG, NAT, FAIR, AMD)
I740010-086	2042000	3.54	IC 74LS241	(TI, SIG, NAT, AMD)
I740010-088	2042400	7.92	IC AM26LS31	(AMD, NAT, TI)
I740010-089	2042600	7.92	IC AM26LS32	(AMD, NAT,TI)
I740010-091	2043000	2.16	IC 74LS161A	(TI, SIG, NAT, FAIR)
I740010-092	2043200	7.50	IC 8212	(INTEL, AMD)
I740010-094	2043600	1.32	IC 7438	(TI, SIG, NAT)
I740010-095	2043800	2.22	IC 74LS123	(TI, SIG, NAT)
I740010-096	2044000	3.54	IC 74LS240	(TI, SIG, NAT)
I740010-097	2044200	5.52	IC 74LS244	(TI, SIG, NAT)
I740010-098	2044400	2.10	IC 74193	(TI, SIG, NAT)
I740010-099	2044600	3.96	IC 74S174	(TI, SIG, NAT)
I740010-100	2044800	2.64	IC 74S138	(TI, SIG, NAT)
I740010-101	2045000	1.80	IC 74S86	(TI, SIG, NAT)
I740010-102	2045200	1.50	IC 74S64	(TI, SIG, NAT)
I740010-103	2045400	1.08	IC 74LS54	(TI, SIG, NAT)
I740010-104	2045600	1.44	IC 74S51	(TI, SIG, NAT)
I740010-105	2045800	1.44	IC 74LS14	(TI, SIG, NAT)
I740010-107	2046200	22.20	IC Digital Delay Module	(AMD)
I740010-108	2046400	2.16	IC 74LS193	(TI, SIG)
I740010-109	2046600	21.90	IC 74S472 512 X 8	(NAT, TI)
I740010-110	2046800	5.76	IC 96S02	(FAIR)
I740010-111	2047000	1.44	IC 74S11	(TI, SIG)
I740010-112	2047200	20.52	IC 74S225	(TI)
I740010-123	2138100	13.14	IC 74LS299 Universal Shift Reg	
I740010-125	2138300	1.50	IC 7407 O.C. Buffer	
I740011-000	2049200	40.00	IC 6116 RAM (150ns)	(HIT, OKI, TOS, MIT, MOS)
I740011-002	2049600	28.94	IC 6502A MicroProcessor	(SYN, MOS T)
I740011-003	2049800	66.24	IC 6545 CRT Controller	(SYN, ROCK)
I740011-004	2155700	28.80	IC 6551 UART (1MHz)	(SYN, ROCK)
I740011-005	2050200	27.21	IC 6522A	(SYN, MOS T)
I740011-006	2050400	18.00	IC Z80A-PIO	(ZIL, MOS, SGS, SHA)
I740011-007	2050600	58.00	IC Z80A-SIO/2	(ZIL, MOS, SGS, SHA)
I740011-008	2050800	16.80	IC Z80A-CTC	(ZIL, MOS, SGS, SHA)
I740011-009	2051000	21.18	IC Z80A-CPU	(ZIL, MOS, SGS, SHA)
I740011-010	2051200	57.48	IC Z80A-DMA	(ZIL, MOS, SGS, SGA)
I740011-011	2051400	10.32	IC HM4716A-2 RAM (150ns)	(HIT, FUJ, TDS)
I740011-012	2051600	83.76	IC Dyn RAM 64K (200ns)	(FUJ, HIT, OKI, MIS)
I740011-015	2052200	184.50	IC 8 x 300 MicroControl	(SIG)

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
I740011-016	2052400	19.50	IC 8-Bit Bidir I/O Port (SIG)
I740011-022	2053600	33.00	IC 2149H/HL
I740011-037	2139200	7.20	IC Dynamic RAM 4116 16K x 1 (120ns)
I740012-001	2056200	39.60	IC Par Ser/Conv WD1100V-01 (WES DIG)
I740012-002	2056400	39.60	IC MFM Gen WD1100V-12 (WES DIG)
I740012-003	2056600	39.60	IC AM Detector WD1100V-03 (WES DIG)
I740012-004	2056800	39.60	IC CRC Gen/Checker WD1100V-04 (WES DIG)
I740012-005	2057000	39.60	IC Par/Ser Conv WD1100V-05 (WES DIG)
I740012-006	2057200	18.00	IC Delay Line SIP (60ns) (PCA)
I740012-010	2139400	1.86	IC 74LS114A Dual J.U.F.F.
I740012-011	2139500	2.40	IC 74S260 Dual NOR Shottky
I740012-012	2139600	8.40	IC 74S374 Octal D.F.F. Shottky
I740012-013	2139700	4.02	IC 74S175 Quad D.F.F. Shottky
I740012-014	2139800	330.00	IC 7220 Graphic Display Controller
	2168700	8.88	IC 74LS629

KEYBOARD PARTS

K030305-001	2222100	13.50	Keycap Dark Gray 1X1 Blank (25 ea)
K030305-XXX	20XXXXX	.72	Keycap Dark Gray 1X1
K030306-001	2222200	33.00	Keycap Dark Gray 1X1 1/2 Blank (25 ea)
K030306-XXX	2072XXX	1.50	Keycap Dark Gray 1X1 1/2
K030307-001	2222300	33.00	Keycap Light Gray 1X1 1/2 Blank (25 ea)
K030307-XXX	2072XXX	1.50	Keycap Light Gray 1X1 1/2
K030308-001	2222400	15.00	Keycap Light Gray 1X1 Blank (25 ea)
K030308-XXX	207XXXX	.72	Keycap Light Gray 1X1
K030309-001	2222500	13.50	Keycap Light Gray 1X1 LP Blank (25 ea)
K030309-XXX	207XXXX	.72	Keycap Light Gray 1X1 Low Profile
K030310-001	2077100	1.86	Keycap Light Gray "L" RETURN
K030311-001	2222600	31.50	Keycap Light Gray 1X1 1/4 Blank (25 ea)
K030311-002	2077300	1.52	Keycap Light Gray 1X1 1/4 CLEAR SPACE
K030312-001	2077400	1.98	Keycap Dark Gray 1X8 Space Bar
K030315-001	2222700	22.50	Keycap Mat Dark Gray 1X1 Blank (25 ea)
K030315-XXX	20XXXXX	.72	Keycap Mat Dark Gray 1X1
K030316-001	2222800	33.00	Keycap Mat Dark Gray 1X1 1/2 Blank (25 ea)
K030316-XXX	2084XXX	2.56	Keycap Mat Dark Gray 1X1 1/2
K030317-001	2222900	33.00	Keycap Mat Light Gray 1X1 1/2 Blank (25 ea)
K030317-XXX	2084XXX	2.56	Keycap Mat Light Gray 1X1 1/2
K030318-001	2223000	22.50	Keycap Mat Light Gray 1X1 Blank (25 ea)
K030318-XXX	208XXXX	.72	Keycap Mat Light Gray 1X1
K030319-001	2223100	22.50	Keycap Mat LG 1X1 Low Profile Blank (25 ea)
K030319-XXX	2089XXX	.72	Keycap Mat Light Gray 1X1 Low Profile
K030320-001	2089400	2.76	Keycap Mat Light Gray "L" RETURN
K030321-001	2223200	28.50	Keycap Mat Light Gray 1X1 1/4 Blank (25 ea)
K030321-002	2089600	2.44	Keycap Mat Light Gray 1X1 1/4 CLEAR SPACE
K030322-001	2089700	3.00	Keycap Mat Dark Gray 1X8 Space Bar
K030600-XXX	214XXXX	1.32	Keycap 1X1 Graphic Keys
K030402-001	2090900	79.29	Keycap Set Gray Shiny Stepped
K030402-002	2091000	59.10	Keycap Set Gray Matted Sculpured
K030500-001	2091200	1.80	Keyguide For Equalizer Asy-Space Bar
K030500-002	2096200	.90	Guide Stem For Equalizer Asy-Space Bar

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
K030500-003	2096300	.72	Damper For Equalizer Asy-Space Bar
K030500-004	2096400	3.00	Keyguide Arm For Equalizer Asy-Space Bar
K030500-005	2096500	13.44	Keyswitch Mounting Plate
KS123456	2199400	3.60	Keyswitch
KS123457	2199500	5.40	Keyswitch Alpha Lock
KS123458	2223800	45.00	Keystopper (25 ea)
			SWITCHES/SOCKETS/FUSES
M200100-003	2096600	6.30	Switch 4 Position DIP 8 Pin SPST
M200100-006	2096700	3.90	Switch 8 Position DIP 16 Pin Top Adjust
M200101-003	2096800	5.70	Switch 10 Position DIP 20 Pin Right Angle
M200107-001	2097300	7.89	Switch Rocker Pwr ON-OFF (SPDT)
M200108-001	2097400	6.92	Switch Slide Power Select (DPDT)
M200111-001	2097500	12.90	Switch Pushbutton (SPDT) -MOME 15" (Reset Sw)
FC12503A	2223700	11.85	Fuse 125V 3 AMP (25 ea)
M200104-001	2223300	11.85	Fuse 3AG 250V 1 AMP (25 ea)
M200104-007	2223400	11.85	Fuse 3AG 250V 4 AMP (25 ea)
M200104-008	2223500	11.85	Fuse 3AG 250V .5 AMP (25 ea)
M200106-001	2097200	21.00	Holder Fuse - Term
4301512	2180400	1.87	Clip Fuse Holder Pwr Sply Module TS 800A
M200100-002	2180800	.72	Transistor Pads (Large) 3005-A
M200301-001	2098400	.83	Socket IC 18 Pin
M200301-002	2098401	1.10	Socket IC 24 Pin
M200301-003	2098402	1.80	Socket IC 40 Pin
M200301-004	2098403	.78	Socket IC 14 Pin
M200301-005	2098404	1.32	Socket IC 28 Pin
M200301-007	2098405	.72	Socket IC 16 Pin
M200301-008	2098406	.72	Socket IC 20 Pin
M200302-001	2174500	15.00	Socket IC 50 Pin
M200303-002	2174600	4.11	Socket IC 14 Pin Low Profile
M200304-002	2098500	3.00	Plug Adapter IC 14 Pin (.10 Spacing)
M200304-003	2098501	5.52	Plug Adapter IC 16 Pin (.10 Spacing)
			CRYSTALS
I740010-056	2035200	37.08	Crystal 23.814 MHz K1114A(MOT, CTS)
M200401-004	2098603	4.80	Crystal 8.0000 MHz
M200401-005	2098604	4.50	Crystal 20.000 MHz
I740010-090	2042800	27.00	Crystal 16 MHz (MOT, CTS, HYT)
M220000-001	2099700	1.02	Insulator Mounting Pad For Crystal
			FANS
M200701-001	2099000	35.28	Fan 115V/230V AC 36-47 CFM (AIR OVER)
M200704-001	2141500	52.50	Fan Box 230V AC TS 802/802H
			BEZEL'S/CASE ASSEMBLIES
M400007-001	2100000	40.00	Panel Front TS 801
M400024-001	2142000	40.00	Panel Front TS 806

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
M400025-001	2142100	40.00	Panel Front TS 806C
M400026-001	2142200	40.00	Panel Front TS 806H
M470002-002	2105401	40.00	Panel Back TS 801/806
M470003-001	2105500	40.00	Panel Back TS 816
M470004-001	2105600	40.00	Panel Front TS 816
M400008-003	2100101	10.00	Shroud Connector TS 800
M400008-004	2100102	10.00	Shroud Connector TS 800A
M400014-001	2100500	10.00	Shroud Connector TS 802
M400018-001	2219800	5.00	Card Guide TS 802
M400012-001	2100300	15.00	Cover Fan TS 816
M400019-001	2101300	10.00	Cover Connector Cut-out Header TS 801
M400020-005	2101400	10.00	Cover Connector Cut-out D/SUB TS 801
M410009-001	2170100	32.40	Panel Flpy Cover TS 802H (Plastic)
M440001-001	2172000	16.68	Housing Contact 16 Position
M440002-001	2172100	.72	Housing Socket 4 Pin
M440003-001	2172200	1.58	Housing Socket 6 Pin
M440003-002	2172201	15.60	Housing Socket 6 Pin
M440006-001	2172300	1.07	Housing Term 5 Circuit
M440006-002	2172301	1.07	Housing Term 3 Circuit
M440009-001	2172400	1.07	Housing Socket 3 Pin
			MISC. ASSEMBLIES
M410001-001	2101600	64.80	Chassis Mounting TS 801/806
M410008-001	2101900	5.88	Panel Cover Hard Disk TS 806
M410018-001	2103500	19.98	Cover Top Pwr Sply TS 802
			LABELS/LOGO'S
M450004-001	2105000	1.50	Label Logo Plastic TELEVIDEO
M450006-010	2105103	1.80	Label Kybd TS 800
M450006-011	2105104	.72	Label Kybd TS 800A
M450006-012	2105105	.72	Label Kybd TS 802
M450006-013	2105106	.72	Label Kybd TS 802H
M450006-014	2105107	1.80	Label Kybd TS 802G
M450006-015	2105108	1.80	Label Kybd TS 802GH
M450011-001	2105300	.96	Label Back Panel RS 232 TS 801/806
M450011-002	2105301	.96	Label Back Panel Term TS 801/806
M450012-003	2154402	1.50	Label TS 800A Back of Unit
M450014-002	2142900	.90	Label S1 TS 800A
M450014-003	2142901	.90	Label S2 TS 800A
			SCREWS/FASTNERS
M490004-001	2158500	.72	Clip Fastner 950/800A
M490005-001	2106000	.88	Term Ring 22-16 AWG Size 6 31881
M490009-001	2106200	1.14	Standoff PCB Screw Mounting 3/8"
M490008-006	2106101	.72	Standoff Flex Support Hinge 3/8"
M490027-005	2107100	.96	Fastner PCM Locking Mounting Support
M490028-003	2107200	.72	Fastner Dual Locking Board Spacers
M490028-006	2107201	.72	Fastner Dual Locking Board Spacers

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
M490019-001	2175200	.72	Nut Hex D/C UNC .112
M490042-001	2108000	.72	Nut Hex D/C #3 Metric
M490042-002	2108001	.72	Nut Hex D/C #4 Metric
M490020-001	2106700	.72	Nut #4 Hex Steel/Zinc
M490023-002	2106800	.72	Screw Mach Flat Hd Phl 4-40 X 1/4"
M490024-002	2106900	.72	Screw Mach Flat Hd Phl 6-32 X 1/4"
M490025-004	2107000	.72	Screw Mach Flat Hd Phl 8-32 X 3/8"
M490010-006	2106300	.72	Screw Mach Pan Hd Phl 6-32 X 1/2"
M490011-004	2106400	.72	Screw Mach Pan Hd Phl 8-32 X 3/8"
M490011-006	2106401	.72	Screw Mach Pan Hd Phl 8-32 X 1/2"
M490011-008	2106402	.72	Screw Mach Pan Hd Phl 8-32 X 5/8"
M490013-002	2106500	.72	Screw Mach Pan Hd Phl 4-40 X 1/4"
M490013-003	2106501	.72	Screw Mach Pan Hd Phl 4-40 X 5/16"
M490013-005	2106503	.72	Screw Mach Pan Hd Phl 4-40 X 7/16"
M490032-002	2107300	.72	Screw Tap Mach Pan Hd Phl 8-32 X 5/16"
M490043-003	2108103	.72	Screw Mach Pan Hd Phl #4 10MM
M490043-006	2108100	.72	Screw Mach Pan Hd Phl #4 16MM
M490034-001	2107400	.72	Screw Tap Mach Pan Hd Cres Steel #3 6MM
M490034-002	2107401	.72	Screw Tap Mach Pan Hd Cres Steel #3 8MM
M490034-006	2107403	.72	Screw Tap Mach Pan Hd Cres Steel #3 16MM
M490020-002	2106701	.72	Washer Lock Steel/Zinc #6
M490020-003	2106702	.72	Washer Lock Steel/Zinc #8
M490040-001	2107800	.72	Washer Flat Steel/Zinc #3 Metric
M490017-002	2106601	.72	Washer Flat #6
M490017-003	2106602	.72	Washer Flat #8
M490040-002	2107801	.72	Washer Flat Steel/Zinc #4 Metric
M490040-003	2107802	.72	Washer Flat Steel/Zinc #5 Metric
M490041-001	2107900	.72	Washer Locking Steel/Zinc #3 Metric
M490041-002	2107901	.72	Washer Locking Steel/Zinc #4 Metric
			BOXES/PACKING MATERIAL
	2208800	25.00	Carton Shipping TS 802
M620000-001	2143600	31.98	Carton Outer Shipping TS 802
M620000-002	2143700	20.52	Carton Shipping TS 806
	2208900	31.98	Carton Outer Shipping TS 806
M620000-003	2143800	26.22	Carton Shipping TS 816
M620001-003	2209000	31.98	Carton Outer Shipping TS 816
M630000-001	2185700	3.18	Corner Blocks Shipping Carton
			RESISTORS
R514000-001	2051100	.72	Resistor Carbon Film 68 Ohm 1/4W 5%
R514000-002	2051300	.72	Resistor Carbon Film 270 Ohm 1/4W 5%
R514000-003	2051500	.72	Resistor Carbon Film 330 Ohm 1/4W 5%
R514000-006	2052100	.72	Resistor Carbon Film 1.0K Ohm 1/4W 5%
R514000-009	2052700	.72	Resistor Carbon Film 3.3K Ohm 1/4W 5%
R514000-011	2053100	.72	Resistor Carbon Film 4.7K Ohm 1/4W 5%
R514000-014	2031500	.72	Resistor Carbon Film 1M Ohm 1/4W 5%
R514000-015	2031700	.72	Resistor Carbon Film 750 Ohm 1/4W 5%
R514000-017	2032100	.72	Resistor Carbon Film 100K Ohm 1/4W 5%

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
R514000-018	2032300	.72	Resistor Carbon Film 51K Ohm 1/4W 5%
R514000-024	2033500	.72	Resistor Carbon Film 22 Ohm 1/4W 5%
R514000-025	2033700	.72	Resistor Carbon Film 47K Ohm 1/4W 5%
R514000-026	2033900	.72	Resistor Carbon Film 150 Ohm 1/4W 5%
R514000-027	2034100	.72	Resistor Carbon Film 10K Ohm 1/4W 5%
R514000-028	2034300	.72	Resistor Carbon Film 200 Ohm 1/4W 5%
R514000-029	2034500	.72	Resistor Carbon Film 33 Ohm 1/4W 5%
R514000-030	2034700	.72	Resistor Carbon Film 20 Ohm 1/4W 5%
R514000-031	2034900	.72	Resistor Carbon Film 100 Ohm 1/4W 1%
R514000-032	2035100	.72	Resistor Carbon Film 1.5K Ohm 1/4W 1%
R514000-033	2035300	.72	Resistor Carbon Film 3.92K Ohm 1/4W 1%
R514000-034	2035500	.72	Resistor Carbon Film 511 Ohm 1/4W 1%
R514000-035	2035700	.72	Resistor Carbon Film 8.25K Ohm 1/4W 1%
R514000-036	2035900	.72	Resistor Carbon Film 1.30K Ohm 1/4W 1%
R514000-037	2036100	.72	Resistor Carbon Film 51 Ohm 1/4W 5%
R514000-039	2036500	.72	Resistor Carbon Film 240 Ohm 1/4W 5%
R514000-041	2036900	.72	Resistor Carbon Film 2K Ohm 1/4W 5%
R514000-042	2037100	.72	Resistor Carbon Film 680 Ohm 1/4W 5%
R514000-043	2037300	.72	Resistor Carbon Film 27K Ohm 1/4W 5%
R514000-044	2037500	.72	Resistor Carbon Film 560 Ohm 1/4W 5%
R514000-045	2037700	.72	Resistor Carbon Film 47 Ohm 1/4W 5%
R514000-046	2037900	.72	Resistor Carbon Film 56 Ohm 1/4W 5%
R514000-047	2038100	.72	Resistor Carbon Film 4.7 Ohm 1/4W 5%
R514000-048	2038300	.72	Resistor Carbon Film 2.7K Ohm 1/4W 5%
R514000-056	2039900	.72	Resistor Carbon Film 6.8 Ohm 1/4W 5%
R514000-057	2040100	2.70	Resistor Metal Film 6.8K Ohm 1/4W 1%
R514000-058	2040300	.72	Resistor Carbon Film 220 Ohm 1/4W 5%
R514003-002	2186100	.72	Resistor Carbon Film 390 Ohm 1/2W 5%
R514003-003	2186200	.72	Resistor Carbon Film 820 Ohm 1/2W 5%
R514003-004	2186300	.72	Resistor Carbon Film 1.5K Ohm 1/2W 5%
R514003-005	2186400	.72	Resistor Carbon Film 10K Ohm 1/2W 5%
R514003-006	2186500	.72	Resistor Carbon Film 2.2M Ohm 1/2W 5%
R514000-100	2040500	1.58	Resistor Pack 1K Ohm 10%
R514000-103	2041100	2.04	Resistor 8 Pin DIP 10K Ohm
R514000-104	2041300	1.20	Resistor 10 Pin DIP 4.7K Ohm
R514000-105	2041500	2.34	Resistor 16 Pin DIP 68 Ohm
R514000-106	2041700	2.64	Resistor 16 Pin DIP 33 Ohm
R514000-107	2041900	.96	Resistor 10 Pin SIP 220 Ohm
R514000-108	2042100	1.53	Resistor 10 Pin SIP 330 Ohm
R514000-109	2042300	4.20	Resistor 8 Pin SIP 220/330 Ohm
R514000-110	2042500	1.08	Resistor 8 Pin SIP 150 Ohm
R514000-111	2042700	3.00	Resistor 8 Pin Pack SIP 1K Ohm
R514000-112	2042900	1.08	Resistor 8 Pin Pack SIP 4.7K Ohm
R514000-113	2043100	2.00	Resistor 16 Pin Pack DIP 1K Ohm
R514001-001	2043900	6.24	Pot 50K Ohm
R514001-003	2044300	6.24	Pot 200K Ohm
R514001-004	2044500	6.24	Pot 2K Ohm
R514001-005	2044700	6.24	Pot 10K Ohm
RF-07104B	2177700	1.06	Pot Brightness & Vertical Height
RF-07202B	2177800	1.06	Pot Vertical Linearity
RF-07473B	2177900	1.06	Pot Video B+ Adjust

OLD PART NUMBER	NEW PART NUMBER	PRICE	DESCRIPTION
RV-24205B	2180100	3.86	Pot Focus
RV-24501B	2180200	2.77	Pot Contrast
			TRANSISTORS/REGULATORS/DIODES
R600000-001	2126100	3.96	Voltage Regulator 78 MO5
R600000-002	2126200	2.40	Voltage Regulator 79LO5AC
R600004-001	2126600	16.50	Voltage Regulator LAS L1405 3A/5V
R600005-001	2126900	18.60	Voltage Regulator LAS 16CB 2A/13.8V
S350100-000	2045300	3.60	Transistor 2N2219A
S350100-001	2045500	2.02	Transistor 2N4401 NPN/Silicon
S350100-003	2045900	.97	Transistor 2N2907A
S350100-004	2046100	8.52	Transistor ARRAY 2 NPN/ 2 PNP TRQ-6700
S350100-005	2046300	3.90	Transistor Pwr 2N5320
S350100-006	2046500	4.50	Transistor 2N3904 NPN/Silicon
S350100-007	2046700	2.07	Transistor KTC1627A/MPSA06
S350100-009	2047100	2.59	Transistor 2N5551
S350100-010	2047300	22.80	Transistor MJE 13006
ST-01353	2199700	4.00	Transistor 2SC1173/2N6121
ST-01354	2199800	3.72	Transistor 2SA473/2N6123
ST-01361	2200000	4.38	Transistor 2SC1166/2N4401
ST-10351	2199900	.79	Transistor 2SA495/2N3906
S360100-003	2048100	3.00	LED (Red) Low Current (5MA) MV55
S360100-000	2047500	.72	Diode 1N914
S360100-001	2047700	.72	Diode 1N4001
S360100-002	2047900	4.20	Diode Voltage Suppressor P6KE15A
S360100-004	2048300	29.70	Diode Tuning MV1404 TS 806/WDC
S360100-005	2048500	.72	Diode Switch 1N4148
S360100-006	2151400	.72	Diode 1N4004 (SD-01257)
S360100-007	2048900	.72	Diode 1N5391 (SD-01251)
SD-01252	2201400	.72	Diode DS18/1DS135D
SD-01253	2201500	1.94	Diode DSA17C/MR500
SD-01254	2201600	1.82	Diode Zener RD12EB/IN759A
SD-01255	2201700	6.29	Diode DS113A/MRI-1000
SD-01258	2201800	.90	Diode KDS8513A/IN920
			INDUCTORS/COILS/TRANSFORMERS
R700001-001	2127100	1.38	Inductor 3.30uh
R700001-002	2127200	1.08	Inductor 4.70uh
3312453	2180300	1.44	Thermister SDT-100
IC-01462	2200900	5.24	Linearity Coil (LC-36) 5.40uh
IC-01464	2201000	1.20	Inductor 27uh .3PIE
IC-01465	2201100	129.24	Transformer Pwr W/Connector CRT858
IC-01466	2201200	4.08	Transformer Horizontal Drive HDT-19
IC-01467	2201300	55.48	Transformer Flyback KFS-00093
IS-01461	2200800	31.63	Yoke Deflection W/Connector KYS-00060

****

RECOMMENDED SPARES STOCKING

****

P/N	Spare Part	Recommended Quantity
2099400	8" Winchester Drive TS 816's	1 per 20
2099301	5" Winchester Drive TS 802H,806H,806	1 per 20
2099200	5" Flpy Drive TS 801,802	1 per 40
	TS 802H,806	1 per 20
2099500	Tape Drive TS 806C,816	1 per 20
2090200	Keyboard TS 800,800A,802,802H	1 per 50
2195800	Video Module TS 800,800A,802,802H	1 per 25
2191500	Pwr Sply Module TS 800,800A	1 per 20
2109100	Pwr Sply TS 806,806H,801	1 per 75
2109202	Pwr Sply TS 816,806C	1 per 75
2109201	Pwr Sply TS 802,802H	1 per 75
201800X	Main Logic Board TS 800A,802,802H	1 per 25
2011000	Main Logic Board TS 800	1 per 25
2017000	Flpy Daughter Board TS 802,802H	1 per 25
2013500	Winchester Disk Controller TS 802H TS 806	1 per 25
2012000	Main Logic Board TS 806	1 per 25
2011500	Main Logic Board TS 801	1 per 25
2017501	Main Logic Board TS 806C	1 per 25
2012500	Main Logic Board TS 816	1 per 15
2013000	User Interface Board TS 816	1 per 25

When using Kits to Repair Systems on a Component Basis you should purchase one each Kit per mixture of 25 systems.

TS 800A uses 2000700 - 2202800 - 2000100

TS 802 uses 2000700 - 2202800 - 2000100 - 2203000 - 2228400

TS 802H uses 2000700 - 2202800 - 2000100 - 2203000 - 2228400 - 2202900

TS 806 uses 2000700 - - 2228400 - 2202900

TS 806C uses 2000700

TS 816 uses 2000700 - - 2228400

****

SPARE PARTS KITS

****

Kit Contents:

2000100 Kit, Spare Parts, Power - Video Module

2199900	2N3906 Vertical Amplifier
2046500	2N3904 Vertical Drive
2200000	2N4401 Horizontal Drive
2047100	2N5551 Reference Amplifier
2046700	KTC1627A 75Volt Regulator
2201400	DS135D/IN391
2047500	IN914
2200800	Yoke Deflection With Connector
2201200	Transformer Horizontal Drive
2200900	Linearity Coil 5.40uh
2201300	Transformer Flyback (High Voltage)
2201000	Inductor 27uh
2126900	Voltage Regulator LAS 16CB 2A/13.8Volts
2186200	Resistor CF 390 Ohms 1/2Watt 5%
2201600	IN759A Zener Diode
2199300	Capacitor 220uf 16Volt Electrolytic
2197300	Capacitor .1uf 600Volt Mylar
2047300	2SC2233/MJE13006

2000700 Kit, Spare Parts, Logic Bd Systems

2042600	26LS32 RS422 interface
2042400	26LS31 RS422 interface
2050600	SIO/2 serial communications chip
2050800	CTC counter timer chip
2051000	CPU Z80A central processor unit
2051200	DMA direct memory access chip
2051600	64K dynamic RAM (4 each)
2029200	75188N
2029400	75189N

2228400 Kit Spare Parts, System Data Cables

2006201	Logic to tape/Logic to 816U
2006400	Logic to winch 816
2006501	806 RS422 to Logic
2006600	801/806/816 printer to Logic
2006800	802H WDC To Winch
2006801	806 WDC To Winch
2006900	802H Dau Board To Flpy/ WDC To Winch
2006901	806 Logic To Flpy/ WDC To Winch
2007000	806 Logic To WDC
2007001	802H Dau Board To WDC
2007300	802 Dau Board To Flpy

****

SPARE PARTS KITS

****

Kit Contents:

2202800 Kit, Spare Parts, Mech TS802/800A
- 2005700 cord for keyboard
- 2223700 3 amp 125V fuse (25 each)
- 2199400 keyswitch
- 2096800 10 position side dip switch
- 2223300 1 amp 250V fuse (25 each)
- 2182100 RS232 connector
- 2097900 RJ-11 connector
- 2098000 RS422 connector
- 2100500 connector shroud

2202900 Kit, Spare Parts Logic bd WDC
- 2056200 parallel converter
- 2056400 MFM converter
- 2056600 AM detector
- 2056800 CRC generator/checker
- 2057000 parallel to serial converter
- 2057200 delay line

2203000 Kit, Spare Parts Logic bd FDC
- 2040200 WD2143-01 four phase clock logic
- 2040400 WD1691 floppy support logic
- 2040600 FD1793-02 (93816 fair amd) floppy controller

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MINIMUM ORDER $50.00

TS 816 THEORY OF OPERATION

This discusses the theory of operation of the TS 816 and the layout of the TS 816 logic boards.

TABLE OF CONTENTS

1.0 INTRODUCTION

The TS 816 is a multi-user system which supports up to 16 user stations. It is a three-board microcomputer based on the Z80A microprocessor and the Z80A family of support LSI ICs.

The system functions as a central resource manager for the user stations via RS 422 SDLC communication links. The central storage devices are an 8-inch Winchester disk drive and a 1/4-inch tape cartridge.

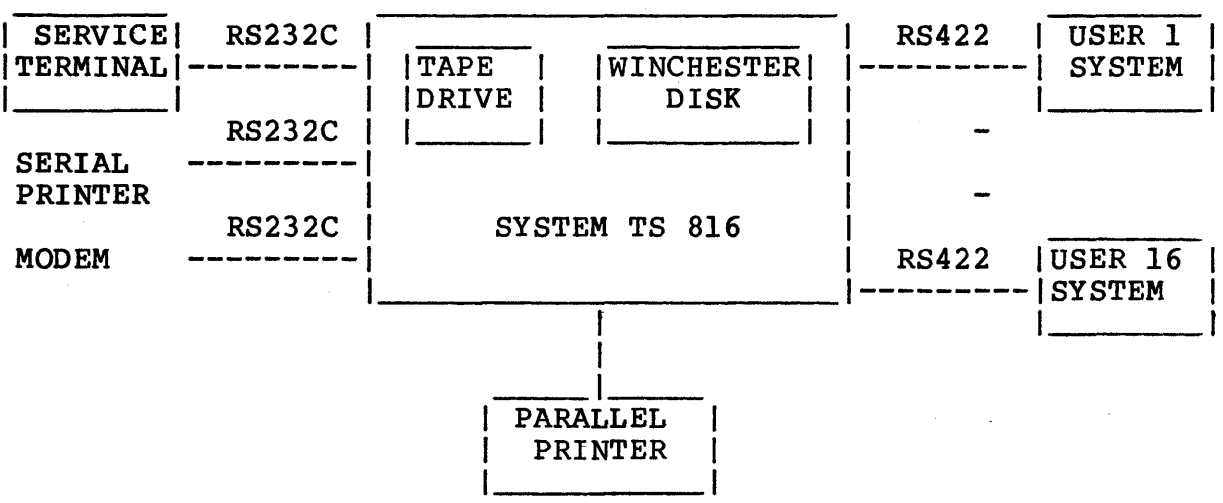


Fig. 1 System TS 816 Configuration

2.0 GENERAL DESCRIPTION

a. Z80A CPU--The main processing unit in the system (4.0MHz operation).

b. Z80A CTC--Counter/Timer IC, generating the baud rates for RS 232C serial channels and a time-of-day facility.

c. Z80A-PIO--Parallel I/O IC, providing Centronics-type printer interface.

d. Z80A SIO--Serial I/O ICs, providing RS 232C interface at a data rate up to 19.2 KB and RS 422 high speed serial interface with data at a rate of 800 Kbits/sec. The SIO also provides the serial interface to the cartridge tape drive.

e. Z80A DMA--Direct memory access controller IC used for direct transfer of data between memory and peripheral I/O, such as SIO's and Winchester (hard) disk interface.

f. MEMORY--128 Kbytes of main memory, using 64K x 1 dynamic RAM ICs. System firmware uses 4 Kbytes of PROM (during power-up or reset only).

g. HARD DISK INTERFACE--Interface for communication to a Winchester disk drive (Fujitsu M2302K, 8-inch). Refer to Fujitsu's "M2031K/2302K Microdisk Drives CE Manual" for detailed information.

h. CARTRIDGE TAPE INTERFACE--Interface for communication to a cartridge tape drive [DEI (Data Electronic Inc.) CMTD-3400S2 6400 BPI]. Refer to DEI's "Series CMTD-3400S2 6400 BPI High Density Cartridge Magnetic Tape Drive Operation and Maintenance Manual" for detailed information.

3.0 FUNCTION

There are two banks of dynamic memory of 64 Kbytes each. Only one bank at a time can be accessed by the CPU through the use of the "EN DRAM" latch and "2ND BANK" latch. Both of these latches are software programmable. See 4.3 for a detailed description.

The TS 816 contains:

128 Kbytes of main memory

Interface to communicate with Fujitsu's 8-inch Winchester drive

Interface to communicate with DEI's tape drive (used as backup to the Winchester)

Parallel port for high-speed Centronics-type printer interface

Three RS 232 channels

16 channels of RS 422 for communication interface with the user stations

Four Kbytes of PROM are used for system initialization, diagnostics, boot, and hard disk/tape drive control during the power-up or reset sequence. This PROM is not accessible to the users. After the initial program in the PROM is run, the PROM maps itself off and returns a full complement of DRAM.

The DMA in the TS 816 transfers data between memory and I/O devices, memory and memory, and I/O device and I/O device.

The CTC IC provides interrupt handling for the hard disk interface. A second CTC generates the baud rates for the RS 232 channels. It also provides the time and date facility.

One RS 232C port is reserved for a service terminal. The baud rate of this port is selected as the software reads a dipswitch (A13) and loads the appropriate value into the CTC. The baud rates of the other two RS 232C ports are set by the operating system when the system is loaded.

The interrupts are prioritized by using locations A33 and A35. The highest priority is assigned to the DMA (IEI) by having it tied high at the dip plug adaptors.

Four LED indicators are used for diagnostic purposes during power-up to help debug the logic board.

The system block diagram is shown in Figure 2; I/O port assignments are shown in Table 1; and the baud rate switch configuration is shown in Table 2.

Figure 2 System Block Diagram of the TS 816

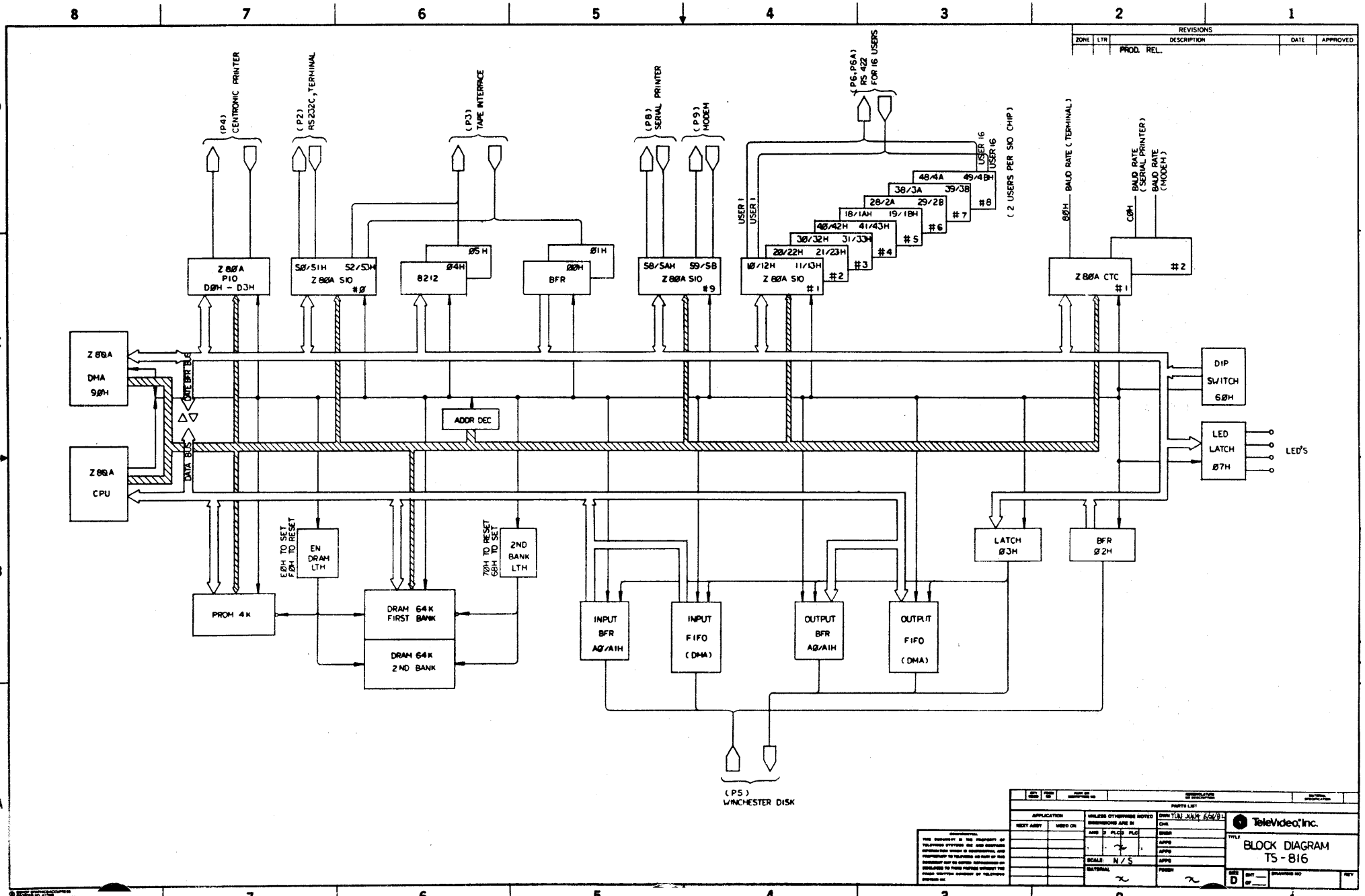


Table 1 I/O Port Assignments

ADDRESS BIT #									I/O PORT
7	6	5	4	3	2	1	0	HEX	
0	0	0	0	0	0	0	0	00H	TAPE STATUS BYTE 1
					0	0	1	01H	TAPE STATUS BYTE 2 & DIAGNOSTIC MODE
					0	1	0	02H	HARD DISK STATUS
					0	1	1	03H	HARD DISK OUPUT LATCH
					1	0	0	04H	TAPE OUTPUT LATCH BYTE 2
					1	0	1	05H	TAPE OUTPUT LATCH BYTE 1
					1	1	1	07H	INDICATOR LOAD (LED)
0	0	0	1	0	X	0	0	10H	SIO 1, CH A DATA REG.
						1	0	12H	COM/STAT REG (USER 1)
						0	1	11H	CH B DATA REG.
						1	1	13H	COM/STAT REG (USER 2)
0	0	1	0	0	X	0	0	20H	SIO 2, CH A DATA REG.
						1	0	22H	COM/STAT REG (USER 3)
						0	1	21H	CH B DATA REG.
						1	1	23H	COM/STAT REG (USER 4)
0	0	1	1	0	X	0	0	30H	SIO 3, CH A DATA REG.
						1	0	32H	COM/STAT REG (USER 5)
						0	1	31H	CH B DATA REG.
						1	1	33H	COM/STAT REG (USER 6)
0	1	0	0	0	X	0	0	40H	SIO 4, CH A DATA REG.
						1	0	42H	COM/STAT REG (USER 7)
						0	1	41H	CH B DATA REG.
						1	1	43H	COM/STAT REG (USER 8)
0	1	0	1	0	X	0	0	50H	SIO 0, CH A DATA REG.
						1	0	52H	COM/STAT REG (RS232 #1) (TERMINAL)
						0	1	51H	CH B DATA REG.
						1	1	53H	COM/STAT REG (TAPE INTERFACE)
0	1	1	0	0	X	X	X	60H	DIP-SWITCH READING
1	0	0	0	0	X	0	0	80H	CTC 1, CH 0(BAUD RATE TERMINAL)
						0	1	81H	CH 1
						1	0	82H	CH 2
						1	1	83H	CH 3
1	0	0	1	0	X	X	X	90H	DMA
1	0	1	0	0	X	X	0	A0H	WDC STATUS/COMMAND REG.
							1	A1H	DATA REG.
1	1	0	0	0	X	0	0	C0H	CTC 2, CH 0(BAUD RATE PRINTER)
						0	1	C1H	CH 1(BAUD RATE MODEM)
						1	0	C2H	CH 2
						1	1	C3H	CH 3
1	1	0	1	0	X	0	0	D0H	PIO CH A DATA REG.
						1	0	D2H	COM/STAT REG
						0	1	D1H	CH B DATA REG.
						1	1	D3H	COM/STAT REG
1	1	1	0	0	X	X	X	E0H	SET 'EN DRAM' LATCH
1	1	1	1	0	X	X	X	F0H	RESET 'EN DRAM' LATCH
0	0	0	1	1	X	0	0	18H	SIO 5, CH A DATA REG.
						1	0	1AH	COM/STAT REG (USER 9)
						0	1	19H	CH B DATA REG.
						1	1	1BH	COM/STAT REG (USER 10)

Table 1 I/O Port Assignments continued

ADDRESS BIT #									I/O PORT
0	0	1	0	1	X	0	0	28H	SIO 6, CH A DATA REG.
7	6	5	4	3	2	1	0	HEX	
						1	0	2AH	COM/STAT REG (USER 11)
						0	1	29H	CH B DATA REG.
						1	1	2BH	COM/STAT REG (USER 12)
0	0	1	1	1	X	0	0	38H	SIO 7, CH A DATA REG.
						1	0	3AH	COM/STAT REG (USER 13)
						0	1	39H	CH B DATA REG.
						1	1	3BH	COM/STAT REG (USER 14)
0	1	0	0	1	X	0	0	48H	SIO 8, CH A DATA REG.
						1	0	4AH	COM/STAT REG (USER 15)
						0	1	49H	CH B DATA REG.
						1	1	4BH	COM/STAT REG (USER 16)
0	1	0	1	1	X	0	0	58H	SIO 9, CH A DATA REG
						1	0	5AH	COM/STAT REG (RS232 PRINTER)
						0	1	59H	CH B DATA REG.
						1	1	5BH	COM/STAT REG (RS232 MODEM)
0	1	1	0	1	X	X	X	68H	SET '2ND BANK' LATCH
0	1	1	1	0	X	X	X	70H	RESET '2ND BANK' LATCH

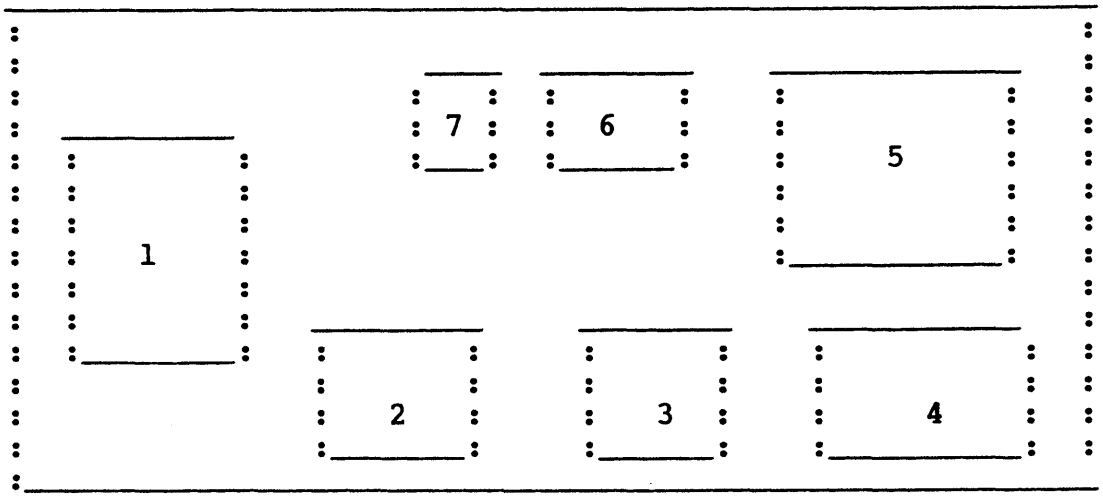
Table 2 Baud Rate Switch (A13) for RS 232C #1 (Terminal)

DIPSWITCH KEYS: 3 2 1	BAUD RATE OF RS232C # 1(Terminal)
0 0 0	19.2 KB
0 0 1	9.6 KB
0 1 0	4.8 KB
0 1 1	2.4 KB
1 0 0	1.2 KB
1 0 1	600 B
1 1 0	300 B
1 1 1	150 B

LEGEND
0 : close
1 : open

4.0 CIRCUIT DESCRIPTION

The TS 816U logic board consists of eight 26LS32 receivers (A9, A10, A11, A12, A13, A14, A15, and A16) and eight 26LS31 drivers (A1, A2, A3, A4, A5, A6, A7, and A8) for the standard RS 422. The standard RS 422 interface board is configured for 8 users.



1) 16-user Serial I/O
2) Tape Interface
3) CPU and DMA
4) Memory
5) Winchester Drive Interface
6) Parallel I/O for Centronic-type Printer
7) Clock

Figure 3 Logic Board Layout

4.1 RESET

-Reset must be active for at least three clock cycles for the CPU to properly accept it. As long as -Reset remains active, the address and data bus float and the control signal outputs are inactive. Two internal T cycles are used before the CPU returns to normal operation. -Reset clears the PC register so that the CPU restarts the program execution from address 0000 hex.

4.2 CLOCK GENERATION

A transistor (TR 2N2907) is used to generate the proper system clock level needed by the Z80 ICs. 16MHz is divided by A36 (93S16 IC) to 4MHz to be used as the system clock. The transmit clock for the SIO RS 422 interface is generated through A73 (74LS163 IC) and A72 (74LS04 IC) using the system clock (4MHz).

To get the baud rates from the CTC for the RS 232C interface, an

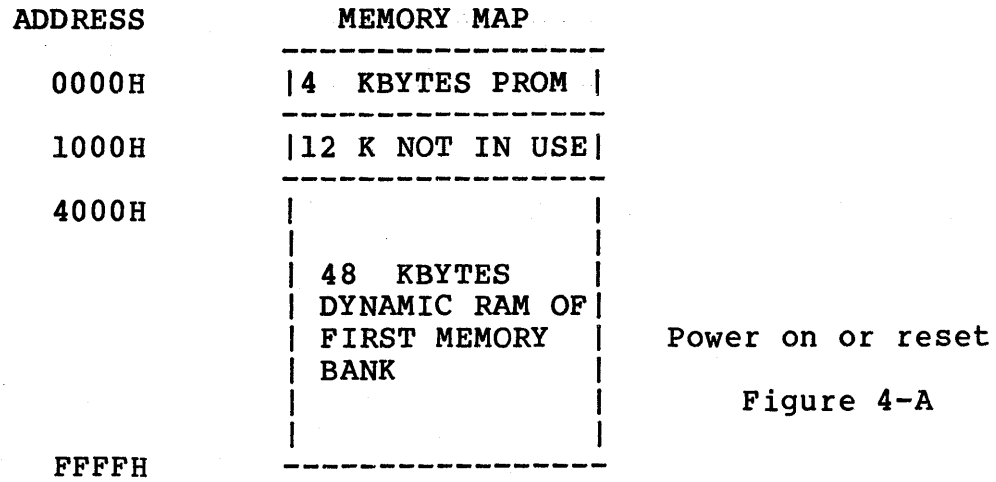
8MHz signal from the 93S16 IC is fed into A37 (74LS163 IC) to generate a frequency of 1/6.5 times the system clock. The resulting clock is then used as the CTC clock.

4.3 MEMORY

4.3.1 PROM--A 4K X 8 A96 PROM is used. PROM is automatically enabled upon power-up or reset. PROM selection circuitry consists of A84 (74LS138 IC) and other common gates. The PROM is enabled or disabled by using the Z80 I/O instruction. When the PROM is enabled, the -CAS signal for the dynamic RAM column address becomes inactive making dynamic RAM disabled and the PROM active. During PROM operation, one wait state is generated to give sufficient time for the slower PROM access speeds.

4.3.2 DYNAMIC RAM--Sixteen ICs, each with 65,536 X 1 bits, are used for main memory (A110 thru A125). These ICs are divided into two banks of 64K X 8 bits each. Two latches are involved in selecting combinations of working memory. The first latch is "EN DRAM" (A69-2) which remains in the reset state upon power on or a hardware reset. The latch is programmable by sending an I/O write instruction to port E0H. The second latch is "2ND BANK" (A69-1) which remains in the reset state during power on and is programmable by writing to port 68H (set) or 78H (reset).

The following illustrates the memory configurations:



Power on or reset

Figure 4-A

After setting the 'EN DRAM' latch (write I/O port E0H), the '2ND BANK' latch remains in the reset state:

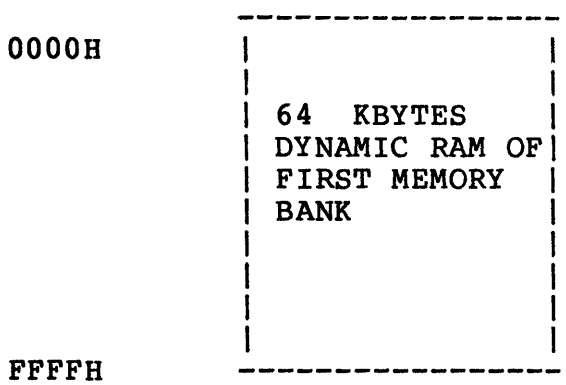


Figure 4-B

After setting both the 'EN DRAM' latch and the '2ND BANK' latch, the memory map is as follows:

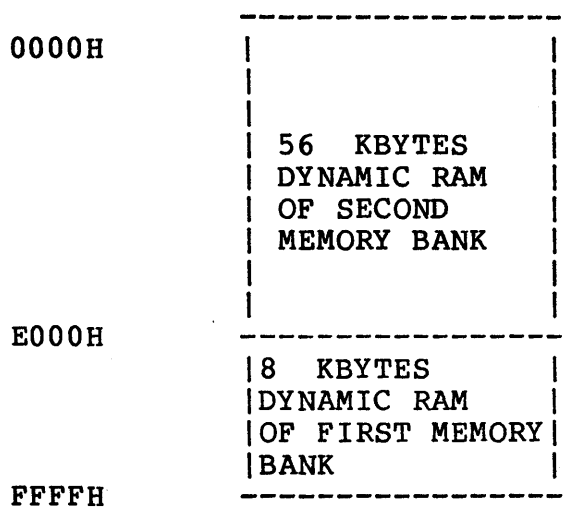


Figure 4-C

Figure 4 Memory Map

-CAS and -RAS are provided to read or write to the dynamic RAM. They specify column and row addresses giving the means to access the 64K memory space. A53, A70 (74S74 IC), and other related ICs generate -CAS and -RAS from the -M1 and -MREQ signals. "SEL CLM" chooses either addresses A0-A7 or A8-A15 as the row and column address.

When dynamic RAM is enabled, it also activates -CAS so that all RAM locations can be accessed. During refresh, -RAS is activated and a row per RAM is refreshed for each CPU cycle.

The following diagrams show the timing for the memory signals.

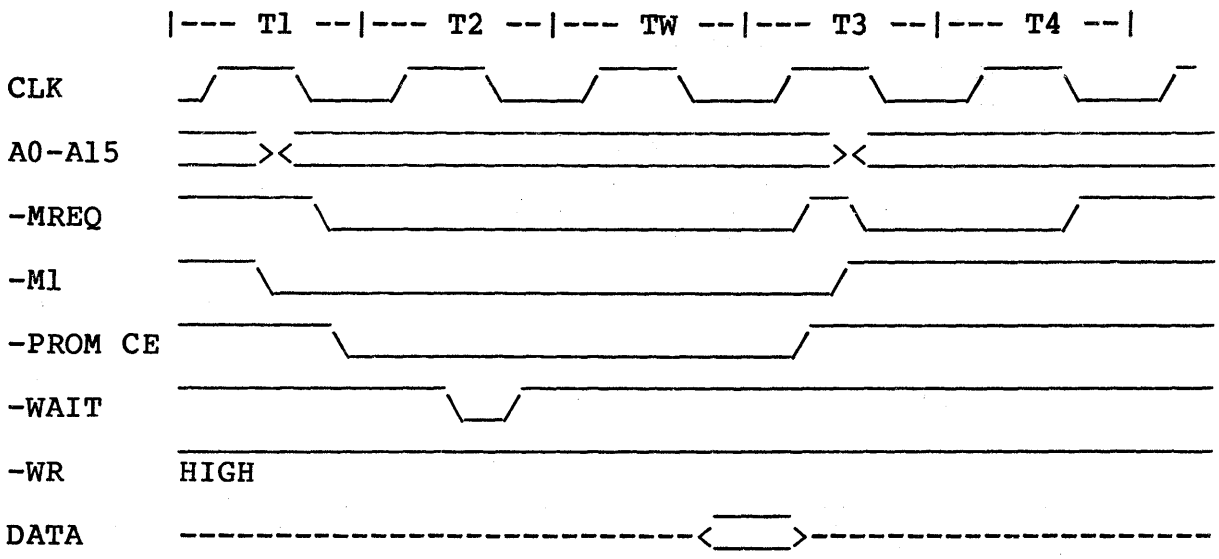


Figure 5 Instruction Fetch from PROM

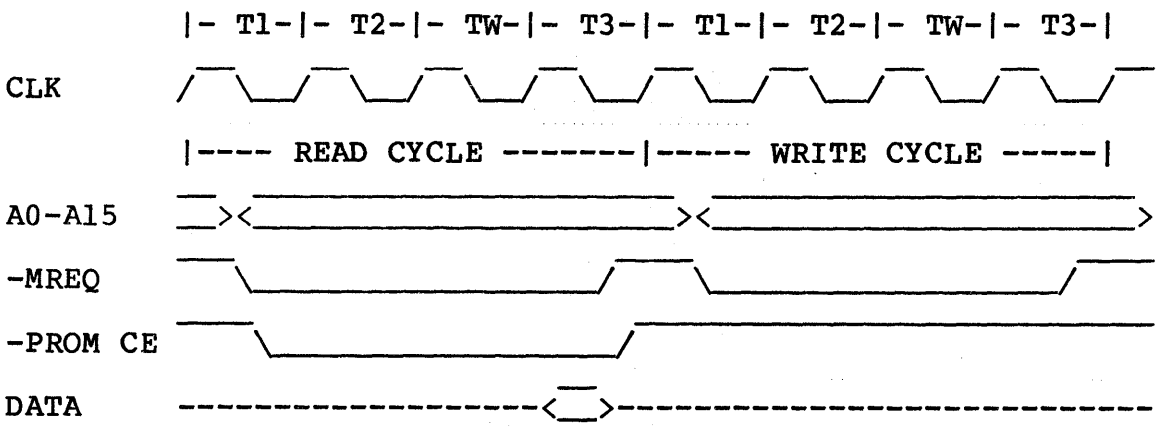


Figure 6 Read/Write to PROM

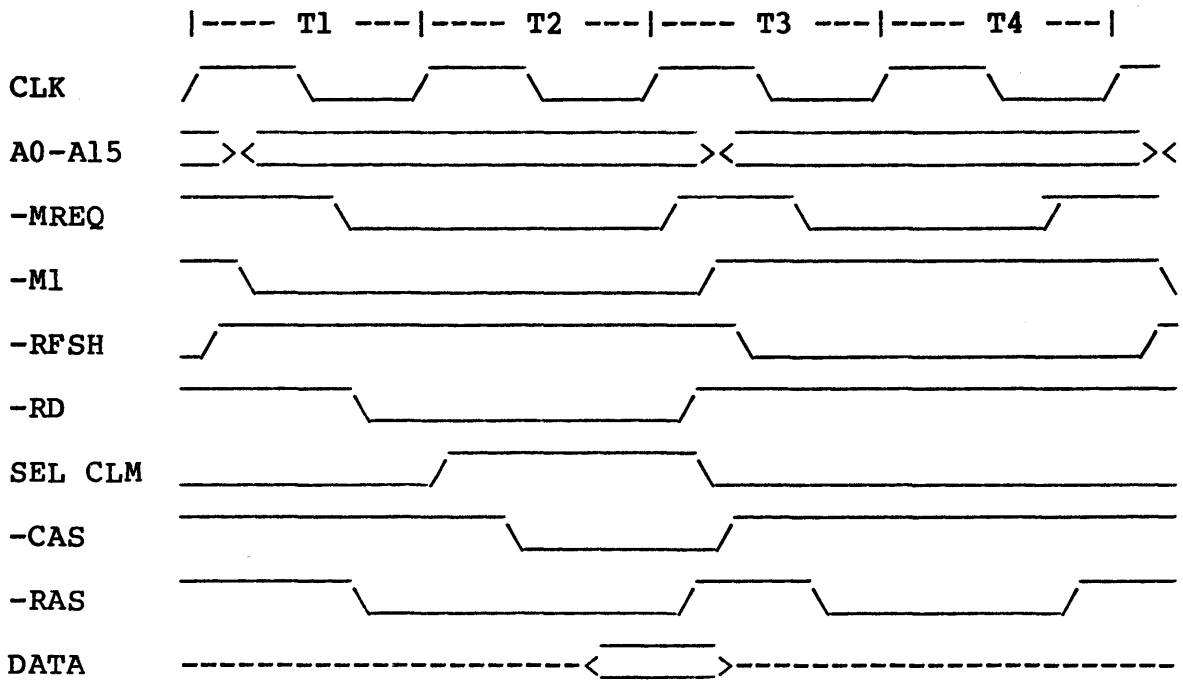


Figure 7 Instruction Fetch from DRAM

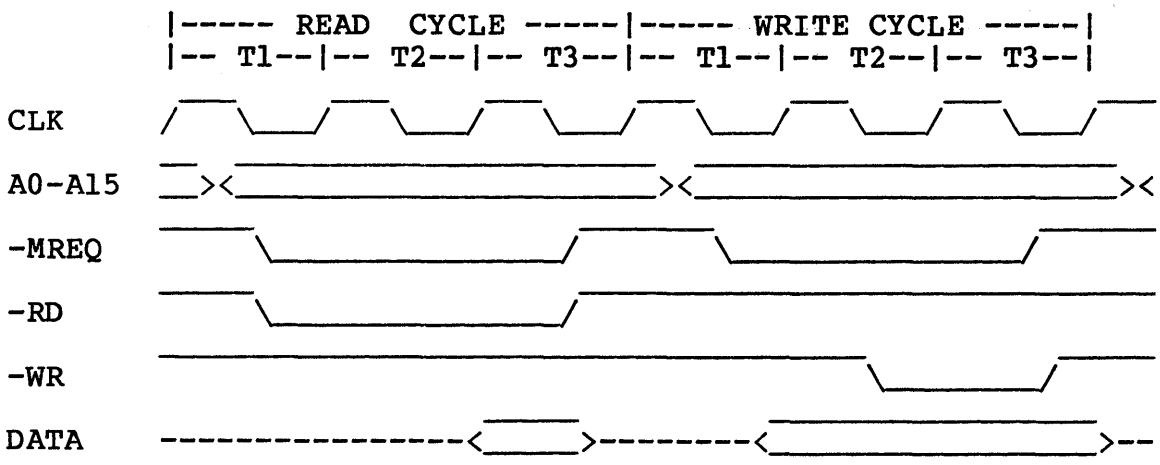


Figure 8 Read/Write from DRAM without Wait States

4.4 DMA OPERATION

The DMA "RDY" line is monitored to determine when a peripheral device is ready for a read or write operation. The RDY line indirectly controls DMA operation. -BUSREQ is used by the DMA to request control of the address, data and control buses from the CPU. When the CPU receives an active -BUSREQ, it waits until the current CPU machine cycle is terminated and then sets the buses to the high impedance state. The CPU then sends a -BUSAK signal to the DMA indicating that it has control of the buses. Figure 9 illustrates this timing.

On every rising edge of clock, the ready line is sampled by the DMA to see if it is at an active level. When the DMA detects a low -BAI for two consecutive rising edges of clock, it begins transferring data on the next rising edge of clock.

Figure 10 shows the timing of the ready line in burst mode. Figure 11 illustrates the continuous mode operation of the DMA.

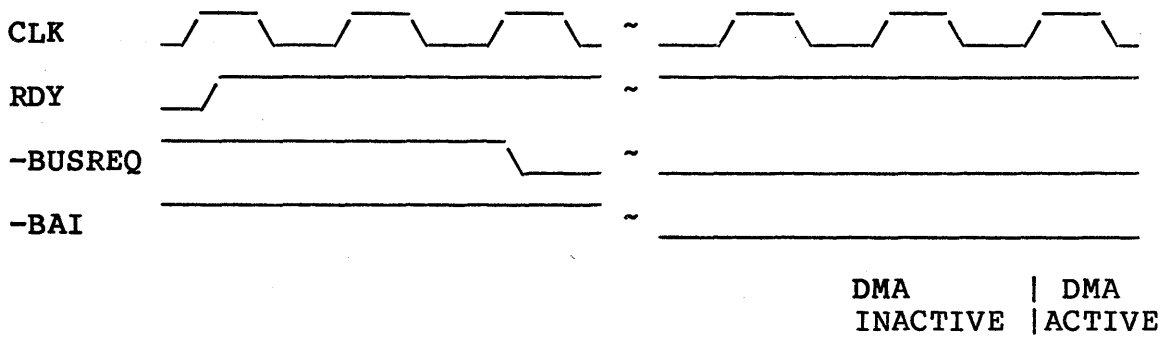


Figure 9 Bus Request and Acceptance Timing

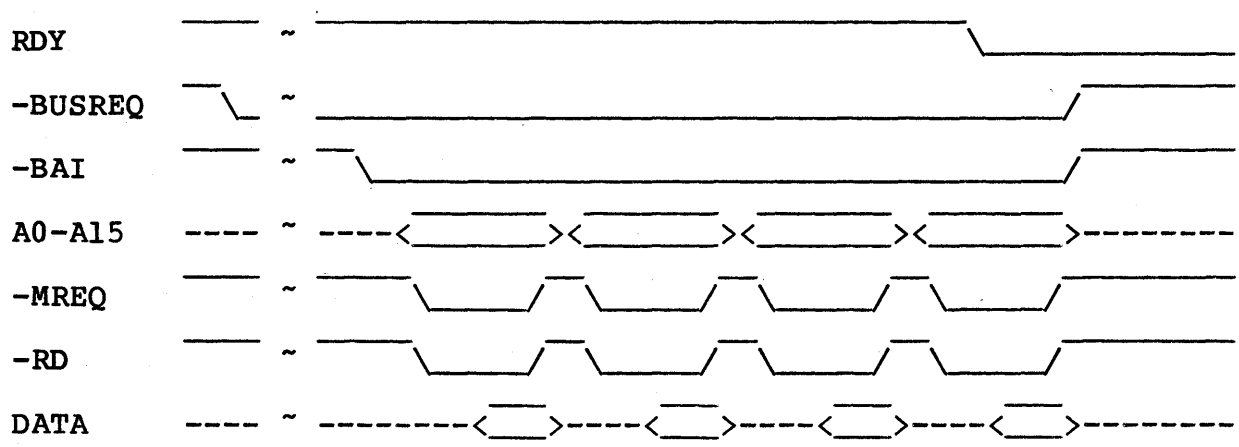


Figure 10 RDY Line in Burst Mode

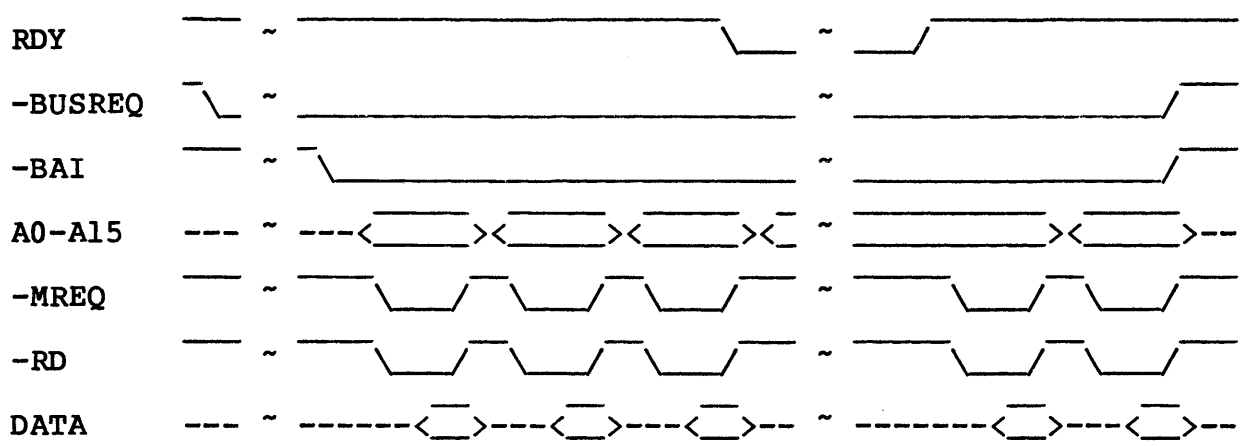


Figure 11 RDY Line in Continuous Mode

4.5 I/O OPERATIONS

The Z80A CPU can handle up to 256 I/O ports. The I/O port address decoding is done by ports A45, A46, A47, and A91 (74S138 or 74LS138 ICs). One I/O port is activated at a time. An I/O read/write IORQ signal is "nanded" with a read/write signal to produce an -IORD/-IOWR signal. During the I/O operation, the CPU automatically inserts a single wait state (TW). This extra wait state allows sufficient time for the I/O port address to be decoded.

There are 10 SIO ICs; eight of them (A2, A3, A27, A28, A55, A56, A86, and A87) are for the 16-user RS 422 interfaces. These interfaces require 16 channels of serial-to-parallel and parallel-to-serial interface.

Two channels of the SIO at A4 are for an RS 232C interface (RS 232 printer and RS 232 modem). The two channels use the standard RS 232C (75188) driver and receiver IC set (75189).

One channel of the SIO at A29 is for an RS 232C terminal interface (the diagnostic or service port). The other channel of the SIO at A29 is for the tape drive interface. This channel includes two output latches, A88 and A89 (8212), and two input status receivers, A103 and A102 (74LS240). A more detailed description of the tape interface is given in Section 4.6 and for the drive in 4.7. The timing for input/output instructions for an SIO is illustrated in Figure 12.

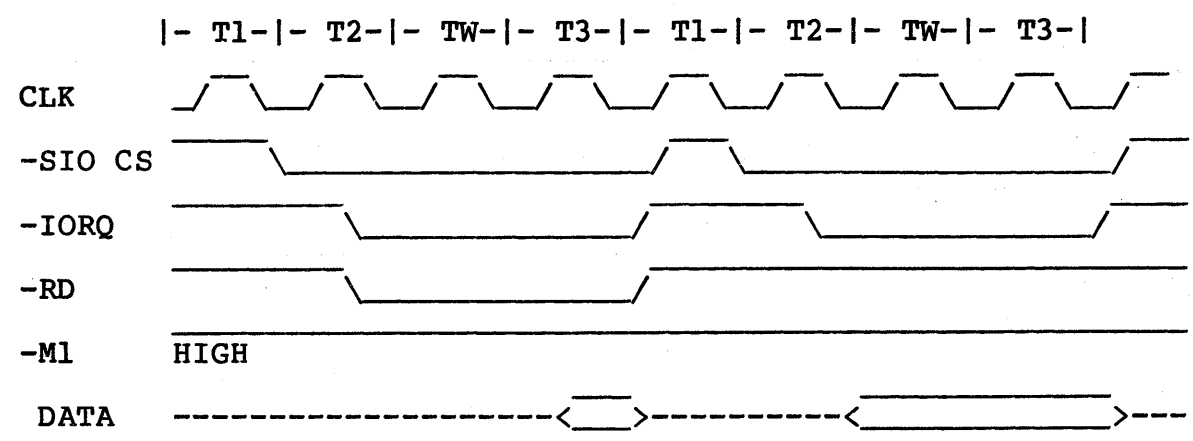


Figure 12 Timing Diagram for Read/Write of SIO

4.6 TAPE OPERATION

Tape operation involves one channel of an SIO (A29), two output latches [A88 and A89 (8212 IC)], and two input inverted buffers [A103 and A102 (74LS240 IC)]. The output latches are called "Tape output latch 1" (05H) and "Tape output latch 2" (04H). The input inverters are called "Tape input status 1" and "Tape input status 2".

Data word for "Tape output latch 2"

D7	D6	D5	D4	D3	D2	D1	D0
-TR2	-TR1	-SL4	-SL2	-SL1	X	X	X

Track select is via D7 and D6 according to the following chart with a low being true. During track selection, all heads for a given track (erase, write and read) are selected. The last track selection is stored in the tape drive even after deselection by the controller.

TRACK #	TR2	TR1
1	H	L
2	L	H
3	L	L
4	H	H

Tape drive select is via D5, D4 and D3. Together these bits determine the tape drive address (low true). The address function will process and remain active during any other drive I/O. The following chart shows the address selection.

Address Selection

DRIVE #	SL4	SL2	SL1
1	H	H	L
2	H	L	H
3	H	L	L
4	L	H	H
5	L	H	L
6	L	L	H
7	L	L	L
8	H	H	H

D2, D1 and D0 are not used and will not effect the system.

Data word for "Tape output latch 1"

SLG	X	-RWD	FB	-WEN	-HSP	-FWD	-REV
D7	D6	D5	D4	D3	D2	D1	D0

Reverse direction (-REV) is D0. Active low causes the tape to move in the reverse direction.

Forward direction (-FWD) is D1. Active low causes the tape to move in the forward direction.

High speed (-HSP) causes the tape to move at high speed in the direction selected.

Tape motion continues until command signals go false. False signals can be triggered by the end of the tape (when going forward) or by the beginning of the tape (when in reverse). The tape will also stop if both directions are given at the same time, if the ready signal goes inactive, or if a higher priority rewind command is given.

In high speed motion, the speed will drop to low speed when the upper loading point hole is sensed in the reverse direction or if the upper early warning hole is sensed in the forward direction.

Write enable (-WEN) enables writing and erasing functions for the selected track. The writing and erasing operations are allowed only when the tape cartridge is in the unprotected state. Write enable should be set prior to the tape going into motion and should not be reset until the drive has stopped. At least two milliseconds are needed between the reset of write enable and the selection of a new track. The write enable signal is reset by either reverse or high speed commands.

Feedback (FB) is for general use and can also be read through port 0CH at D4.

Rewind (-RWD) positions the tape at its beginning at a high speed. The drive must be selected to start a rewind but may be deselected after the sequence has started.

D6 is not used.

Select gate (SLG) allows selection of the track or device per the select and address codes. Select gate is used to prevent a change in the track or device until Select gate is active.

"Tape input status 1" address is 00H

RDY	LPS	EWS	FLG	FUP	WEN	BSY	SLD
D7	D6	D5	D4	D3	D2	D1	D0

Ready (RDY) is true when all of the following occur:

the tape cartridge is installed

the sensor lamp is drawing current

five volts are applied to the tape drive

Load point sensed (LPS) is set and latched when the upper load point hole (the warning for the start of the tape) is passed when the tape moves in the reverse direction. The signal is reset when the load point is passed when the tape moves in the forward direction. When this signal is true, the high speed signal is disabled in the reverse direction. At this time, reverse tape motion is allowed until the beginning of the tape hole is encountered. The drive then stops and only accepts forward commands.

Early warning sensed (EWS) is set and latched when the upper early warning hole (warning for the end of the tape) is passed when the tape moves in the forward direction. This signal is reset when the hole is passed when the tape moves in the reverse direction. When this signal is true, the high speed signal is disabled and forward motion is allowed until the end of tape hole is encountered. The tape then stops and only accepts reverse direction commands.

Flag (FLG) is set when the automatic sequence to position the tape at the beginning has been executed or a rewind command has been completed. This signal is reset by a subsequent receipt of a forward command.

File unprotected (FUP) is true when a tape cartridge is installed and it is in the unprotected state (meaning the tape can be written on).

Write enable (WEN) is true when a write enable is latched within

the tape drive.

Busy (BSY) is true when a cartridge is inserted and the drive is performing an automatic rewind sequence, a normal rewind, a forward command, or a reverse command. This signal goes true when the command is received and remains true until tape motion has stopped. The time for slow speed commands is 30 milliseconds and for high speed commands is 80 milliseconds.

Selected (SLD) is true when the tape drive has received its proper address.

"Tape input status 2" address 01H

DIAG	X	DAD	FB	X	X	X	X
D7	D6	D5	D4	D3	D2	D1	D0

Diagnostic (DIAG) is reserved for starting the diagnostic routines which can be initiated by power on or reset.

Data Detected (DAD) is true when the data has been detected during a read from the tape cartridge at either low or high speed.

Feedback (FB) is the same as bit four in "Tape output status 2".

4.6.1 DATA COMMUNICATION WITH THE TAPE DRIVE--The preamble for tape data is 39 zeros (0) followed by a one (1) at the beginning of each data block. The postamble is the reverse of this with a "one" followed by 39 "zeros" at the end of each data block. The preamble is stripped from the read data when data is being read in the forward direction. The postamble is stripped from the read data when the data is read in the reverse direction.

Example of a data block on the tape cartridge:

39 'ZEROS'| 1 'ONE'| ADDRESS | DATA | 1 'ONE' | 39 'ZEROS'|

To create preambles and postambles, -DTR must be low on the SIO for the equivalent of a five-byte transmission time before and after the data is transmitted. During data transfer, -DTR is at a high level.

4.7 OPERATION OF WINCHESTER DRIVE INTERFACE

The 8" Winchester drive interface consists of:

Four FIFO (first in-first out) memory ICs at locations A22, A23, A38 and A39 (74S225)

Four output drivers using A36, A50, A66, and A67

Buffer ICs 7438 (74LS244) using A24, A40, and A41

Inverter IC (74LS240) at location A25

Miscellaneous gates providing control signals for the FIFOs

The "Hard disk output latch" (I/O port 03H) is an eight-bit latch that is automatically reset to all zeroes at power-on or during a hardware reset. The contents of the bits are:

BIT 0 - WD SL 1	Lower bit of the drive select
BIT 1 - WD SL 2	Higher bit of the drive select (Note: The interface can communicate with up to four drives. We only have one drive in the system. It is designated as drive #0 and is selected with both bits 0 and 1 low.)
BIT 2 - WR OP	This bit should be high during a data write operation and low during a data read operation.
BIT 3 - WD SFT RST	This bit, when high, sends a reset signal to the hard disk drive.
BIT 4 - WD FIFO RST	This bit, when high, resets all of the FIFO ICs.
BIT 5 -	Unused.
BIT 6 -	Unused.
BIT 7 -	Unused.

The "Hard disk input status" (I/O port 02H) is a four-bit input buffer whose contents are:

BIT 0	WDC INT	This bit reflects the interrupt signal directly from the hard disk drive. When high, it indicates that the hard disk is in the interrupt phase.
BIT 1	WDC ATN	This bit reflects the attention signal directly from the hard disk drive.
BIT 2	WDC BSY	This bit reflects the busy signal directly from the hard disk drive.
BIT 3		Unused.

The Winchester drive requires a nominal data transfer rate of 1.68 microseconds per byte. Therefore, FIFO buffers are needed to match the data transfer rate of the DMA burst mode. The DMA burst mode is programmable from 1.5 to 1.75 microseconds or faster. When the DMA runs faster, FIFOs are still needed because occurrence of the first byte is unpredictable and some delay is needed for the DMA to freeze the system data bus. The FIFOs buffers are five bytes wide and two each are needed for read and write operations.

In the data read operation, the drive sends a data request signal

when it is ready to send a byte of data. The read enable signal is generated by the interface and sent to the drive. The data is then available at the input buffer (A25) and is clocked into the input FIFO ICs (A22, A23) where it is propagated to the last latch in the FIFOs. As soon as the input FIFOs have a byte of Data Ready to be transferred to the memory, an Output Ready (OR) is sent from the FIFO creating a "WDC RDY;" this initiates DMA operation. The DMA gets the byte out of the FIFO by giving an "IORD" to the I/O port (A0H) and a "FIFO output enable." This clocks the byte out of the last latch of FIFOs. Normal operation requires that the input FIFO ICs never be full. For this reason the DMA transfer rate must be faster than 1.68 microseconds per byte.

The status register of the drive is readable directly by the CPU through I/O port A0H. The data from the status register is passed through the input buffer (A25), bypasses the FIFOs, and goes through another buffer (A24) to the system data bus.

During the data write operation, the DMA keeps the output FIFOs (A38, A39) full by doing I/O writes to port A1H. The DMA is operating in burst mode and continues filling the FIFOs until their input enable (IR) signal goes inactive. The inactive "IR" releases "WDC RDY" and stops the DMA operation. As long as the FIFOs have data to be sent, the output ready (OR) signal generates a write enable to the drive and transfers data at the speed of the data request signal from the drive. Normal operation requires the output FIFOs never to be empty during a data transfer. The DMA data transfer rate must be 1.68 microseconds per byte.

The command register for the drive can be sent through the interface by doing an I/O write to port A0H. The data bypasses the output FIFOs and is sent to the drive via output buffers A40 and A41.

5.0 CONNECTOR DESCRIPTION OF MAIN TS 816 LOGIC BOARD

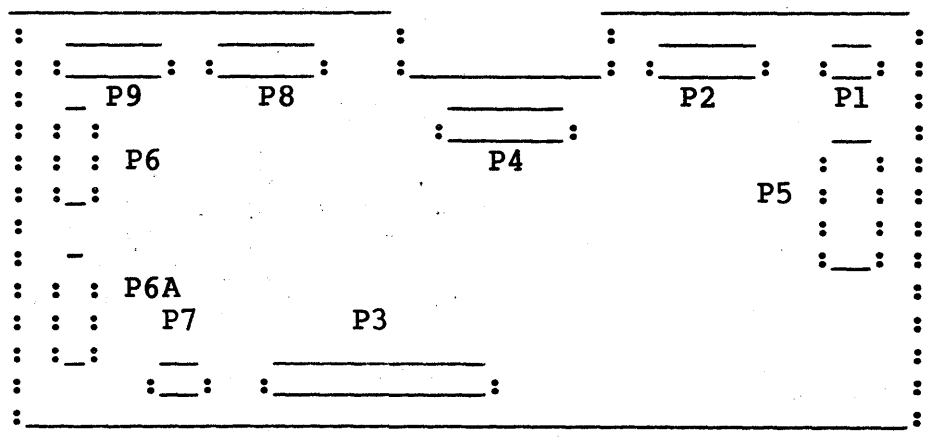


Figure 13 Connectors on the Main TS 816 Logic Board

Table 3 Connector Assignment of the Main TS 816 Logic Board

CONNECTOR #	DESCRIPTION
P1	POWER
P2	RS232C # 1 (FOR SERVICE TERMINAL)
P3	CARTRIDGE TAPE INTERFACE
P4	CENTRONIC TYPE PRINTER INTERFACE
P5	WINCHESTER DISK DRIVE INTERFACE
P6	TS 816U BOARD INTERFACE (1ST BOARD)
P6A	TS 816U BOARD INTERFACE (2ND BOARD)
P7	RESET INTERFACE
P8	RS232C # 2 (FOR SERIAL PRINTER)
P9	RS232C # 3 (FOR MODEM)

5.1 POWER CONNECTOR (P1: 5 PIN)

Table 4 Power Connector Configuration

PIN NO.	DESCRIPTION
1	-12 V
2	UNUSED
3	GND
4	+5 V
5	+12 V

5.2 RS 232C CONNECTOR (P2, P8, P9: 25 PIN)

Table 5 RS 232C Connector Configuration

PIN NO.	DESCRIPTION
1	FRAME GROUND
2	TRANSMIT DATA (RECEIVE)
3	RECEIVE DATA (TRANSMIT)
4	REQUEST TO SEND
5	CLEAR TO SEND
7	SIGNAL GROUND
8	DATA CARRIER DETECT
15	TRANSMIT CLOCK INPUT (ONLY IN P9)
17	RECEIVE CLOCK INPUT (ONLY IN P9)
20	DATA TERMINAL READY
24	TRANSMIT CLOCK OUTPUT (ONLY IN P9)
25	(IN P2,RESERVED FOR MANUFACTURER'S USE) (IN P8 & P9, NO CONNECTION)

NOTES
1. P9 is configured for the connection to a modem of asynchronous mode.
   P8 is configured for the connection to a serial printer.
   P2 is configured for the connection to a terminal.
2. Polarity of data signals : - (negative) : true

Polarity of control signals : + (positive) : true

5.3 CARTRIDGE TAPE INTERFACE CONNECTOR (P3: 50 PINS)

Table 6 Cartridge Tape Connector Configuration

PIN NO.	I/O	DESCRIPTION
2	I	-SLD, SELECTED
4	I	-RDY, READY
6	I	-WND, WRITE ENABLED
8	I	-FLG, FLAG
10	I	-LPS, LOAD POINT SENSED
12	I	-FUP, FILE UNPROTECTED
14	I	-BSY, BUSY
16	I	-EWS, EARLY WARNING SENSED
18	O	-RWD, REWIND
20	O	-REV, REVERSE
22	O	-FWD, FORWARD
24	O	-HSP, HIGH SPEED
26	O	-WEN, WRITE ENABLE
28	O	-SL1, UNIT SELECT (2 EXP 0)
30	O	-SL2, UNIT SELECT (2 EXP 1)
32	O	-SL4, UNIT SELECT (2 EXP 2)
34	O	-SLG, SELECT GATE
36	I	-RNZ, READ NRZ DATA
38	I	-RDS, READ DATA STROBE
40	I	-DAD, DATA DETECTED
42	O	-WDE, WRITE DATA ENABLE
44	O	-WNZ, WRITE NRZ DATA
46	O	-TR2, TRACK SELECT (2 EXP 1)
48	I	-WDS, WRITE DATA STROBE
50	O	-TR1, TRACK SELECT (2 EXP 0)

ALL THE ODD NUMBER PINS ARE GROUNDED

5.4 WINCHESTER HARD DISK DRIVE INTERFACE CONNECTOR (P5: 50 PIN)

Table 7 Winchester Drive Interface Connector Configuration

PIN NO.	I/O	DESCRIPTION
1	O	-DBCK, DATA BUS CHECK
3		(SPARE)
5	O	-SL2, UNIT SELECT (2 EXP 1)
7	O	-SL1, UNIT SELECT (2 EXP 0)
9	I	-ATN, ATTENTION
11	I	-BSY, BUSY
13	I	-TX, TRANSFER
15	O	-TC, TERMINATE CONTROL
17	I/O	-DB7, DATA BUS BIT 7
19	I/O	-DB6, DATA BUS BIT 6
21	I/O	-DB5, DATA BUS BIT 5
23	I/O	-DB4, DATA BUS BIT 4
25	I/O	-DB3, DATA BUS BIT 3
27	I/O	-DB2, DATA BUS BIT 2
29	I/O	-DB1, DATA BUS BIT 1
31	I/O	-DB0, DATA BUS BIT 0
33	I/O	-DBP, DATA BUS PARITY BIT
35	O	-RST, RESET
37	O	-DACK, DATA ACKNOWLEDGE
39	I	-DRQ, DATA REQUEST
41	I	-INT, INTERRUPT
43	O	-CS, CONTROLLER SELECT
45	O	-W, WRITE
47	O	-R, READ
49	O	-A, ADDRESS

ALL EVEN NUMBER PINS ARE GROUNDED

5.5 CENTRONICS-TYPE PRINTER INTERFACE CONNECTOR (P4: 40 PIN)

The Centronics printer interface connector, located on the main logic board, is a 40-pin, right-angle header. Its corresponding rear panel connector, labeled PRINTER, is a 36-pin connector. Figure 14 shows the physical comparison of the two and Table 8 gives the signal association to the pin outs.

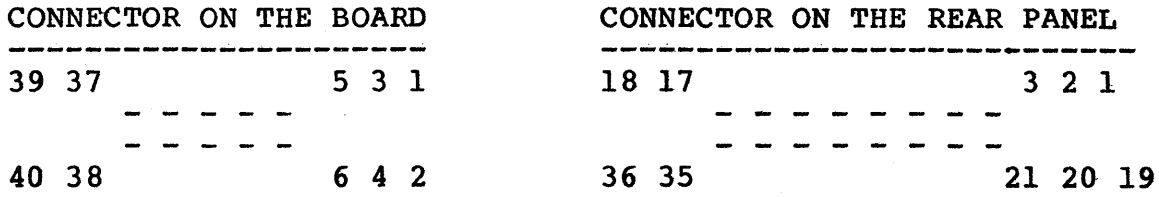


Figure 14 Comparison of Two Connectors for Printer

Table 8 Configuration of Printer Interface Connector on Board

PIN NO. ON REAR PANEL	PIN NO. ON TS 816 BOARD	DESCRIPTION	
1, 19	1, 2*	-DATA STROBE	
2, 20	3, 4*	DATA 0	
3, 21	5, 6*	DATA 1	
4, 22	7, 8*	DATA 2	
5, 23	9, 10*	DATA 3	
6, 24	11, 12*	DATA 4	
7, 25	13, 14*	DATA 5	
8, 26	15, 16*	DATA 6	
9, 27	17, 18*	DATA 7	
10, 28	19, 20*	-ACKNLG	
11, 29	21, 22*	BUSY	
12	23	PE (PAPER EMPTY)	(**5)
30	24	(NOT USED)	(**6)
13	25	SELECT	(**4)
31	26	(NOT USED)	(**8)
14	27	(NOT USED)	(**7)
32	28	-FAULT	(**3)
15	29	(NOT USED)	
33	30	LIGHT DETECT	(**2)
16	31	GND	
34	32	(NOT USED)	
17	33	GND	
35	34	(NOT USED)	
18	35	(NOT USED)	
36	36	(NOT USED)	
	37 THRU 40	(NOT USED)	

NOTES

* Second pin number indicates return
**2 Grounded (no light detect) if jumper 'W2' is connected
**3 Always high (no fault) if jumper 'W3' is connected
**4 Always high (select enabled) if jumper 'W4' is connected
**5 Grounded (no paper empty) if jumper 'W5' is connected
**6 Grounded if jumper 'W6' is connected
**7 Grounded if jumper 'W7' is connected
**8 'Input prime' is generated if jumper 'W8' is connected

5.6 TS 816U INTERFACE CONNECTOR (P6, P6A : 50 PIN)*

Table 9 TS 816U Interface Connector Configuration

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	TXD1	26	TXD8
2	-DTR1	27	-DTR8
3	TXD2	28	RXD5
4	-DTR2	29	-RXC5
5	TXD3	30	-DCD5
6	-DTR3	31	RXD6
7	TXD4	32	-RXC6
8	-DTR4	33	-DCD6
9	RXD1	34	RXD7
10	-RXC1	35	-RXC7
11	-DCD1	36	-DCD7
12	RXD2	37	RXD8
13	-RXC2	38	-RXC8
14	-DCD2	39	-DCD8
15	RXD3	40	(NOT USED)
16	-RXC3	41	GND
17	-DCD3	42	TXC1
18	RXD4	43	GND
19	-RXC4	44	TXC5
20	-DCD4	45	(NOT USED)
21	TXD5	46	(NOT USED)
22	-DTR5	47	(NOT USED)
23	TXD6	48	(NOT USED)
24	-DTR6	49	(NOT USED)
25	TXD7	50	-DIAG MODE

* P6 is connected to the first TS 816U board in the 8-user environment. In the case of a 16-user environment, a second TS 816U board is connected through the P6A connector.

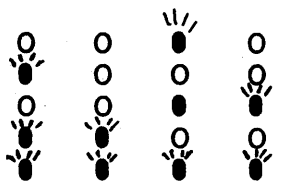
5.7 RESET CONNECTOR (P7: 3 PIN)

Table 10 Reset Connector Configuration

PIN NO.	DESCRIPTION
1	GND
2	RESET SW (NORMALLY HIGH)
3	RESET SW (NORMALLY LOW)

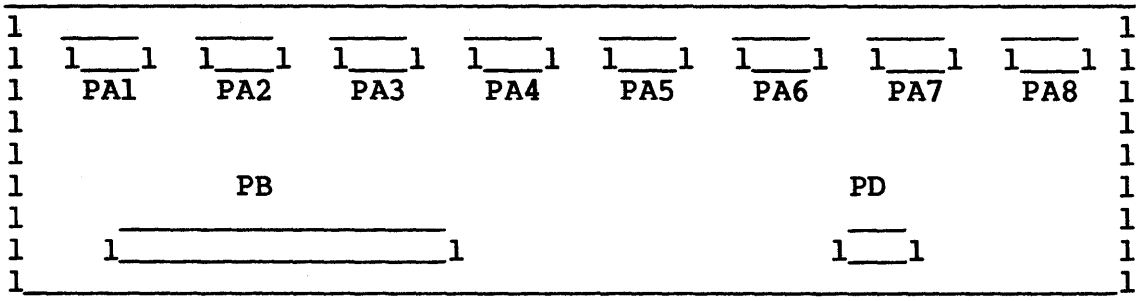
5.8 DIAGNOSTIC LEDS

CR2	CR3	CR4	CR5	TEST DESCRIPTION
O	O	O		Test Memory Bank 1; if there is a failure,



light stays on.
Test Memory Bank 2; if fail LED blinks and message.
Test hard disk; if fail light stays on.
No test performed
No test performed
Test complete

6.0 CONNECTOR CONFIGURATION OF TS 816U BOARD



PA1 ~ PA8 RS422 user interface
PB TS 816 interface
PD Power

Figure 15 Connector Configuration of TS 816U Board

6.1 CONNECTOR OF RS 422 USER INTERFACE (PA1 THRU PA8: 15 PINS)

Table 11 Connector Configuration of RS422 User Interface

PIN NO.	DESCRIPTION
1	SHIELD GROUND
2	TXD
3	RXD
4	RTS
5	CTS
6	-TXC
7	-RXC
8	SIGNAL GROUND
9	-TXD
10	-RXD
11	-RTS
12	-CTS
13	TXC
14	RXC
15	(RESERVED)**

** Pin 15 of PA1 is connected to pin 50 of PB. This is used for diagnostics purposes.

6.2 CONNECTOR CONFIGURATION OF MAIN TS 816 LOGIC INTERFACE(PB: 50 PIN) TO THE TS 816U

Table 12 Connector Configuration of Main TS 816 Logic Interface

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	TXD1	26	-DTR7
2	-DTR1	27	TXD8
3	TXD2	28	-DTR8
4	-DTR2	29	RXD5
5	TXD3	30	-RXC5
6	-DTR3	31	-DCD5
7	TXD4	32	RXD6
8	-DTR4	33	-RXC6
9	RXD1	34	-DCD6
10	-RXC1	35	RXD7
11	-DCD1	36	-RXC7
12	RXD2	37	-DCD7
13	-RXC2	38	RXD8
14	-DCD2	39	-RXC8
15	RXD3	40	-DCD8
16	-RXC3	41	GROUND
17	-DCD3	42	TXC1
18	RXD4	43	GROUND
19	-RXC4	44	TXC5
20	-DCD4	45	(UNUSED)
21	TXD5	46	(UNUSED)
22	-DTR5	47	(UNUSED)
23	TXD6	48	(UNUSED)
24	-DTR6	49	(UNUSED)
25	TXD7	50	-DIAG MODE

6.3 CONNECTOR CONFIGURATION OF POWER (PD: 5 PINS)

Table 13 Connector Configuration of Power

PIN NO.	DESCRIPTION
1	(UNUSED)
2	(UNUSED)
3	GROUND
4	+5V
5	(UNUSED)

7.0 POWER REQUIREMENTS

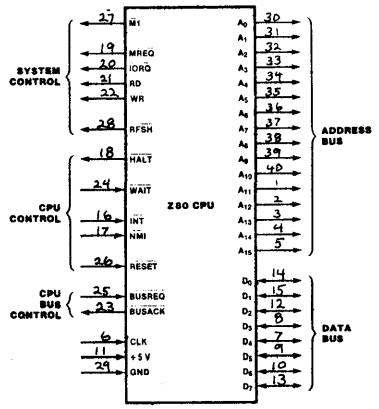
Table 14 Requirement of System III Power Supply

	TAPE	HARD DISK	TS816+2X(TS816U	TOTAL TS816 SYSTEM
+5V	1.3A TYP 2.61 MAX	5.6A TYP 7.5A MAX	4.6A TYP 8.5A MAX	11.5A TYP 18.6A MAX
+12V			0.1A TYP 0.1A MAX	0.1A TYP 0.1A MAX
-12V		0.5A TYP 0.5A MAX	0.5A TYP 0.5A MAX	1.0A TYP 1.0A MAX
+24V	1.6A TYP 3.1A MAX	1.2A TYP 1.6A MAX 6/0A SURGE		2.8A TYP 4.7A MAX 9.1A SURGE
-24V	1.8A TYP 3.5A MAX			1.8A TYP 3.5A MAX

Zilog

Z8400
Z80® CPU Central Processing Unit

Features



Pin Descriptions

A_0-A_{15}. *Address Bus* (output, active High, 3-state). A_0-A_{15} form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

$\overline{BUSACK}$. *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ have entered their high-impedance states. The external circuitry can now control these lines.

$\overline{BUSREQ}$. *Bus Request* (input, active Low). Bus Request has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle. $\overline{BUSREQ}$ forces the CPU address bus, data bus, and control signals $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ to go to a high-impedance state so that other devices can control these lines. $\overline{BUSREQ}$ is normally wire-ORed and requires an external pullup for these applications. Extended $\overline{BUSREQ}$ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

D_0-D_7. *Data Bus* (input/output, active High, 3-state). D_0-D_7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

$\overline{HALT}$. *Halt State* (output, active Low). $\overline{HALT}$ indicates that the CPU has executed a Halt instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

$\overline{INT}$. *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. $\overline{INT}$ is normally wire-ORed and requires an external pullup for these applications.

$\overline{IORQ}$. *Input/Output Request* (output, active Low, 3-state). $\overline{IORQ}$ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. $\overline{IORQ}$ is also generated concurrently with $\overline{M1}$ during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

$\overline{M1}$. *Machine Cycle One* (output, active Low). $\overline{M1}$, together with $\overline{MREQ}$, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. $\overline{M1}$, together with $\overline{IORQ}$, indicates an interrupt acknowledge cycle.

$\overline{MREQ}$. *Memory Request* (output, active Low, 3-state). $\overline{MREQ}$ indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{NMI}$. *Non-Maskable Interrupt* (input, active Low). $\overline{NMI}$ has a higher priority than $\overline{INT}$. $\overline{NMI}$ is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

$\overline{RD}$. *Memory Read* (output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{RESET}$. *Reset* (input, active Low). $\overline{RESET}$ initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that $\overline{RESET}$ must be active for a minimum of three full clock cycles before the reset operation is complete.

$\overline{RFSH}$. *Refresh* (output, active Low). $\overline{RFSH}$, together with $\overline{MREQ}$, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

$\overline{WAIT}$. *Wait* (input, active Low). $\overline{WAIT}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended $\overline{WAIT}$ periods can prevent the CPU from refreshing dynamic memory properly.

$\overline{WR}$. *Memory Write* (output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

Instruction Set

The Z80 microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the Z80 instruction set and shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. The *Z80 CPU Technical Manual* (03-0029-01) and *Assembly Language Programming Manual* (03-0002-01) contain significantly more details for programming use.

The instructions are divided into the following categories:

- ☐ 8-bit loads
- ☐ 16-bit loads
- ☐ Exchanges, block transfers, and searches
- ☐ 8-bit arithmetic and logic operations
- ☐ General-purpose arithmetic and CPU control
- ☐ 16-bit arithmetic operations
- ☐ Rotates and shifts
- ☐ Bit set, reset, and test operations
- ☐ Jumps
- ☐ Calls, returns, and restarts
- ☐ Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- ☐ Immediate
- ☐ Immediate extended
- ☐ Modified page zero
- ☐ Relative
- ☐ Extended
- ☐ Indexed
- ☐ Register
- ☐ Register indirect
- ☐ Implied
- ☐ Bit

8-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD r, r'	r ← r'	•	•	X	•	X	•	•	01 r r'		1	1	4	r, r' Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
LD r, n	r ← n	•	•	X	•	X	•	•	00 r 110		2	2	7	
									← n →					
LD r, (HL)	r ← (HL)	•	•	X	•	X	•	•	01 r 110		1	2	7	
LD r, (IX+d)	r ← (IX+d)	•	•	X	•	X	•	•	11 011 101	DD	3	5	19	
									01 r 101					
									← d →					
LD r, (IY+d)	r ← (IY+d)	•	•	X	•	X	•	•	11 111 101	FD	3	5	19	
									01 r 110					
									← d →					
LD (HL), r	(HL) ← r	•	•	X	•	X	•	•	01 110 r		1	2	7	
LD (IX+d), r	(IX+d) ← r	•	•	X	•	X	•	•	11 011 101	DD	3	5	19	
									01 110 r					
									← d →					
LD (IY+d), r	(IY+d) ← r	•	•	X	•	X	•	•	11 111 101	FD	3	5	19	
									01 110 r					
									← d →					
LD (HL), n	(HL) ← n	•	•	X	•	X	•	•	00 110 110	36	2	3	10	
									← n →					
LD (IX+d), n	(IX+d) ← n	•	•	X	•	X	•	•	11 011 101	DD	4	5	19	
									00 110 110	36				
									← d →					
									← n →					
LD (IY+d), n	(IY+d) ← n	•	•	X	•	X	•	•	11 111 101	FD	4	5	19	
									00 110 110	36				
									← d →					
									← n →					
LD A, (BC)	A ← (BC)	•	•	X	•	X	•	•	00 001 010	0A	1	2	7	
LD A, (DE)	A ← (DE)	•	•	X	•	X	•	•	00 011 010	1A	1	2	7	
LD A, (nn)	A ← (nn)	•	•	X	•	X	•	•	00 111 010	3A	3	4	13	
									← n →					
									← n →					
LD (BC), A	(BC) ← A	•	•	X	•	X	•	•	00 000 010	02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	•	X	•	•	00 010 010	12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	•	X	•	•	00 110 010	32	3	4	13	
									← n →					
									← n →					
LD A, I	A ← I	↕	↕	X	0	X	IFF	0	11 101 101	ED	2	2	9	
									01 010 111	57				
LD A, R	A ← R	↕	↕	X	0	X	IFF	0	11 101 101	ED	2	2	9	
									01 011 111	5F				
LD I, A	I ← A	•	•	X	•	X	•	•	11 101 101	ED	2	2	9	
									01 000 111	47				
LD R, A	R ← A	•	•	X	•	X	•	•	11 101 101	ED	2	2	9	
									01 001 111	4F				

NOTES: r, r' means any of the registers A, B, C, D, E, H, L.
IFF the content of the interrupt enable flip-flop, (IFF) is copied into the P/V flag.

For an explanation of flag notation and symbols for mnemonic tables, see Symbolic Notation section following tables.

16-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	•	•	X	X	•	•	00 dd0 001 ← n → ← n →	3	3	10	dd Pair 00 BC 01 DE 10 HL 11 SP
LD IX, nn	IX ← nn	•	•	X	X	•	•	11 011 101 DD 00 100 001 21 ← n → ← n →	4	4	14	
LD IY, nn	IY ← nn	•	•	X	X	•	•	11 111 101 FD 00 100 001 21 ← n → ← n →	4	4	14	
LD HL, (nn)	H ← (nn + 1) L ← (nn)	•	•	X	X	•	•	00 101 010 2A ← n → ← n →	3	5	16	
LD dd, (nn)	dd_H ← (nn + 1) dd_L ← (nn)	•	•	X	X	•	•	11 101 101 ED 01 dd1 011 ← n → ← n →	4	6	20	
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	•	•	X	X	•	•	11 011 101 DD 00 101 010 2A ← n → ← n →	4	6	20	
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	•	•	X	X	•	•	11 111 101 FD 00 101 010 2A ← n → ← n →	4	6	20	
LD (nn), HL	(nn + 1) ← H (nn) ← L	•	•	X	X	•	•	00 100 010 22 ← n → ← n →	3	5	16	
LD (nn), dd	(nn + 1) ← dd_H (nn) ← dd_L	•	•	X	X	•	•	11 101 101 ED 01 dd0 011 ← n → ← n →	4	6	20	
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	•	•	X	X	•	•	11 011 101 DD 00 100 010 22 ← n → ← n →	4	6	20	
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	•	•	X	X	•	•	11 111 101 FD 00 100 010 22 ← n → ← n →	4	6	20	
LD SP, HL	SP ← HL	•	•	X	X	•	•	11 111 001 F9	1	1	6	
LD SP, IX	SP ← IX	•	•	X	X	•	•	11 011 101 DD 11 111 001 F9	2	2	10	
LD SP, IY	SP ← IY	•	•	X	X	•	•	11 111 101 FD 11 111 001 F9	2	2	10	
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H SP ← SP − 2	•	•	X	X	•	•	11 qq0 101	1	3	11	qq Pair 00 BC 01 DE 10 HL 11 AF
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H SP ← SP − 2	•	•	X	X	•	•	11 011 101 DD 11 100 101 E5	2	4	15	
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H SP ← SP − 2	•	•	X	X	•	•	11 111 101 FD 11 100 101 E5	2	4	15	
POP qq	qq_H ← (SP + 1) qq_L ← (SP) SP ← SP + 2	•	•	X	X	•	•	11 qq0 001	1	3	10	
POP IX	IX_H ← (SP + 1) IX_L ← (SP) SP ← SP + 2	•	•	X	X	•	•	11 011 101 DD 11 100 001 E1	2	4	14	
POP IY	IY_H ← (SP + 1) IY_L ← (SP) SP ← SP + 2	•	•	X	X	•	•	11 111 101 FD 11 100 001 E1	2	4	14	

NOTES: dd is any of the register pairs BC, DE, HL, SP.
qq is any of the register pairs AF, BC, DE, HL.
$(PAIR)_H$ $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively.
e.g., BC_L = C, AF_H = A.

Exchange, Block Transfer, Block Search Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	DE ↔ HL	•	•	X	•	X	•	•	•	11 101 011 EB	1	1	4	
EX AF, AF'	AF ↔ AF'	•	•	X	•	X	•	•	•	00 001 000 08	1	1	4	
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	•	•	X	•	X	•	•	•	11 011 001 D9	1	1	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	•	•	X	•	X	•	•	•	11 100 011 E3	1	5	19	
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	•	•	X	•	X	•	•	•	11 011 101 DD 11 100 011 E3	2	6	23	
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	•	•	X	•	X	•	•	•	11 111 101 FD 11 100 011 E3	2	6	23	
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	•	•	X	①	X	0	↕	0	•	11 101 101 ED 10 100 000 A0	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	0	0	•	11 101 101 ED 10 110 000 B0	2 2	5 4	21 16	If BC ≠ 0 If BC = 0

NOTE: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1.

Exchange, Block Transfer, Block Search Groups (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	•	•	X	① 0	X	↕	0	•	11 101 101 ED 10 101 000 A8	2	4	16	
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	① 0	X	0	0	•	11 101 101 ED 10 111 000 B8	2 2	5 4	21 16	If BC ≠ 0 If BC = 0
CPI	A − (HL) HL ← HL + 1 BC ← BC − 1	↕	↕	X	↕	X	↕	1	•	11 101 101 ED 10 100 001 A1	2	4	16	
CPIR	A − (HL) HL ← HL + 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	↕	X	↕	X	↕	1	•	11 101 101 ED 10 110 001 B1	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	↕	↕	X	↕	X	↕	1	•	11 101 101 ED 10 101 001 A9	2	4	16	
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	↕	X	↕	X	↕	1	•	11 101 101 ED 10 111 001 B9	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)

NOTES: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1.
② Z flag is 1 if A = (HL), otherwise Z = 0.

8-Bit Arithmetic and Logical Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A, r	A ← A + r	↕	↕	X	↕	X	V	0	↕	10 000 r	1	1	4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
ADD A, n	A ← A + n	↕	↕	X	↕	X	V	0	↕	11 000 110 ← n →	2	2	7	
ADD A, (HL)	A ← A + (HL)	↕	↕	X	↕	X	V	0	↕	10 000 110	1	2	7	
ADD A, (IX + d)	A ← A + (IX + d)	↕	↕	X	↕	X	V	0	↕	11 011 101 DD 10 000 110 ← d →	3	5	19	
ADD A, (IY + d)	A ← A + (IY + d)	↕	↕	X	↕	X	V	0	↕	11 111 101 FD 10 000 110 ← d →	3	5	19	
ADC A, s	A ← A + s + CY	↕	↕	X	↕	X	V	0	↕	001				s is any of r, n, (HL), (IX + d), (IY + d) as shown for ADD instruction. The indicated bits replace the 000 in the ADD set above.
SUB s	A ← A − s	↕	↕	X	↕	X	V	1	↕	010				
SBC A, s	A ← A − s − CY	↕	↕	X	↕	X	V	1	↕	011				
AND s	A ← A ∧ s	↕	↕	X	1	X	P	0	0	100				
OR s	A ← A ∨ s	↕	↕	X	0	X	P	0	0	110				
XOR s	A ← A ⊕ s	↕	↕	X	0	X	P	0	0	101				
CP s	A − s	↕	↕	X	↕	X	V	1	↕	111				
INC r	r ← r + 1	↕	↕	X	↕	X	V	0	•	00 r 100	1	1	4	
INC (HL)	(HL) ← (HL) + 1	↕	↕	X	↕	X	V	0	•	00 110 100	1	3	11	
INC (IX + d)	(IX + d) ← (IX + d) + 1	↕	↕	X	↕	X	V	0	•	11 011 101 DD 00 110 100 ← d →	3	6	23	
INC (IY + d)	(IY + d) ← (IY + d) + 1	↕	↕	X	↕	X	V	0	•	11 111 101 FD 00 110 100 ← d →	3	6	23	
DEC m	m ← m − 1	↕	↕	X	↕	X	V	1	•	101				m is any of r, (HL), (IX + d), (IY + d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

General-Purpose Arithmetic and CPU Control Groups

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	Converts acc. content into packed BCD following add or subtract with packed BCD operands.	↕	↕	X	↕	X	P	•	↕	00 100 111 27	1	1	4	Decimal adjust accumulator.
CPL	$A \leftarrow \overline{A}$	•	•	X	1	X	•	1	•	00 101 111 2F	1	1	4	Complement accumulator (one's complement).
NEG	$A \leftarrow 0 - A$	↕	↕	X	↕	X	V	1	↕	11 101 101 ED 01 000 100 44	2	2	8	Negate acc. (two's complement).
CCF	$CY \leftarrow \overline{CY}$	•	•	X	X	X	•	0	↕	00 111 111 3F	1	1	4	Complement carry flag.
SCF	CY ← 1	•	•	X	0	X	•	0	1	00 110 111 37	1	1	4	Set carry flag.
NOP	No operation	•	•	X	•	X	•	•	•	00 000 000 00	1	1	4	
HALT	CPU halted	•	•	X	•	X	•	•	•	01 110 110 76	1	1	4	
DI *	IFF ← 0	•	•	X	•	X	•	•	•	11 110 011 F3	1	1	4	
EI *	IFF ← 1	•	•	X	•	X	•	•	•	11 111 011 FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	•	•	•	11 101 101 ED 01 000 110 46	2	2	8	
IM 1	Set interrupt mode 1	•	•	X	•	X	•	•	•	11 101 101 ED 01 010 110 56	2	2	8	
IM 2	Set interrupt mode 2	•	•	X	•	X	•	•	•	11 101 101 ED 01 011 110 5E	2	2	8	

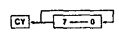
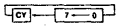
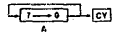
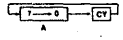
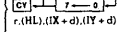
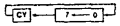
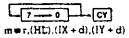
NOTES: IFF indicates the interrupt enable flip-flop.
CY indicates the carry flip-flop.
* indicates interrupts are not sampled at the end of EI or DI.

16-Bit Arithmetic Group

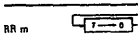
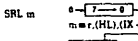
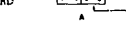
Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD HL, ss	HL ← HL + ss	•	•	X	X	X	•	0	↕	00 ss1 001	1	3	11	ss Reg. 00 BC 01 DE 10 HL 11 SP
ADC HL, ss	HL ← HL + ss + CY	↕	↕	X	X	X	V	0	↕	11 101 101 ED 01 ss1 010	2	4	15	
SBC HL, ss	HL ← HL − ss − CY	↕	↕	X	X	X	V	1	↕	11 101 101 ED 01 ss0 010	2	4	15	
ADD IX, pp	IX ← IX + pp	•	•	X	X	X	•	0	↕	11 011 101 DD 01 pp1 001	2	4	15	pp Reg. 00 BC 01 DE 10 IX 11 SP
ADD IY, rr	IY ← IY + rr	•	•	X	X	X	•	0	↕	11 111 101 FD 00 rr1 001	2	4	15	rr Reg. 00 BC 01 DE 10 IY 11 SP
INC ss	ss ← ss + 1	•	•	X	•	X	•	•	•	00 ss0 011	1	1	6	
INC IX	IX ← IX + 1	•	•	X	•	X	•	•	•	11 011 101 DD 00 100 011 23	2	2	10	
INC IY	IY ← IY + 1	•	•	X	•	X	•	•	•	11 111 101 FD 00 100 011 23	2	2	10	
DEC ss	ss ← ss − 1	•	•	X	•	X	•	•	•	00 ss1 011	1	1	6	
DEC IX	IX ← IX − 1	•	•	X	•	X	•	•	•	11 011 101 DD 00 101 011 2B	2	2	10	
DEC IY	IY ← IY − 1	•	•	X	•	X	•	•	•	11 111 101 FD 00 101 011 2B	2	2	10	

NOTES: ss is any of the register pairs BC, DE, HL, SP.
pp is any of the register pairs BC, DE, IX, SP.
rr is any of the register pairs BC, DE, IY, SP.

Rotate and Shift Group

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA		•	•	X	0	X	•	0	↕	00 000 111 07	1	1	4	Rotate left circular accumulator.
RLA		•	•	X	0	X	•	0	↕	00 010 111 17	1	1	4	Rotate left accumulator.
RRCA		•	•	X	0	X	•	0	↕	00 001 111 0F	1	1	4	Rotate right circular accumulator.
RRA		•	•	X	0	X	•	0	↕	00 011 111 1F	1	1	4	Rotate right accumulator.
RLC r		↕	↕	X	0	X	P	0	↕	11 001 011 CB 00 000 r	2	2	8	Rotate left circular register r.
RLC (HL)		↕	↕	X	0	X	P	0	↕	11 001 011 CB 00 000 110	2	4	15	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLC (IX + d)	 r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	11 011 101 DD 11 001 011 CB — d — 00 000 110	4	6	23	
RLC (IY + d)		↕	↕	X	0	X	P	0	↕	11 111 101 FD 11 001 011 CB — d — 00 000 110	4	6	23	
RL m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	010				Instruction format and states are as shown for RLC's. To form new opcode replace 000 of RLC's with shown code.
RRC m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	001				

Rotate and Shift Group (Continued)

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RR m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	011				
SLA m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	100				
SRA m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	101				
SRL m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	111				
RLD		↕	↕	X	0	X	P	0	•	11 101 101 ED 01 101 111 6F	2	5	18	Rotate digit left and right between the accumulator and location (HL).
RRD		↕	↕	X	0	X	P	0	•	11 101 101 ED 01 100 111 67	2	5	18	The content of the upper half of the accumulator is unaffected.

Bit Set, Reset and Test Group

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
BIT b, r	$Z \leftarrow \overline{r_b}$	X	↕	X	1	X	X	0	•	11 001 011 CB 01 b r	2	2	8	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
BIT b, (HL)	$Z \leftarrow \overline{(HL)_b}$	X	↕	X	1	X	X	0	•	11 001 011 CB 01 b 110	2	3	12	
BIT b, (IX + d)$_b$	$Z \leftarrow \overline{(IX+d)_b}$	X	↕	X	1	X	X	0	•	11 011 101 DD 11 001 011 CB — d — 01 b 110	4	5	20	b Bit Tested 000 0 001 1 010 2 011 3 100 4 101 5 110 6 111 7
BIT b, (IY + d)$_b$	$Z \leftarrow \overline{(IY+d)_b}$	X	↕	X	1	X	X	0	•	11 111 101 FD 11 001 011 CB — d — 01 b 110	4	5	20	
SET b, r	$r_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 001 011 CB 11 b r	2	2	8	
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 001 011 CB 11 b 110	2	4	15	
SET b, (IX + d)	$(IX+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 011 101 DD 11 001 011 CB — d — 11 b 110	4	6	23	
SET b, (IY + d)	$(IY+d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 111 101 FD 11 001 011 CB — d — 11 b 110	4	6	23	
RES b, m	$m_b \leftarrow 0$ m ≡ r, (HL), (IX + d), (IY + d)	•	•	X	•	X	•	•	•	10				To form new opcode replace 11 of SET b, s with 10. Flags and time states for SET instruction.

NOTES: The notation m_b indicates bit b (0 to 7) of location m.

Jump Group

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP nn	PC ← nn	•	•	X	•	X	•	•	•	11 000 011 C3 — n — — n —	3	3	10	
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	•	•	X	•	X	•	•	•	11 cc 010 — n — — n —	3	3	10	cc Condition 000 NZ non-zero 001 Z zero 010 NC non-carry 011 C carry 100 PO parity odd 101 PE parity even 110 P sign positive 111 M sign negative
JR e	PC ← PC + e	•	•	X	•	X	•	•	•	00 011 000 18 — e − 2 —	2	3	12	
JR C, e	If C = 0, continue If C = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00 111 000 38 — e − 2 —	2 2	2 3	7 12	If condition not met. If condition is met.
JR NC, e	If C = 1, continue If C = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 110 000 30 — e − 2 —	2 2	2 3	7 12	If condition not met. If condition is met.
JP Z, e	If Z = 0 continue If Z = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00 101 000 28 — e − 2 —	2 2	2 3	7 12	If condition not met. If condition is met.
JR NZ, e	If Z = 1, continue If Z = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 100 000 20 — e − 2 —	2 2	2 3	7 12	If condition not met. If condition is met.
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	11 101 001 E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	11 011 101 DD 11 101 001 E9	2	2	8	

Jump Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11 111 101 FD 11 101 001 E9	2	2	8	
DJNZ, e	B ← B − 1 If B = 0, continue	•	•	X	•	X	•	•	•	00 010 000 10 — e − 2 —	2	2	8	If B = 0.
	If B ≠ 0, PC ← PC + e										2	3	13	If B ≠ 0.

NOTES: e represents the extension in the relative addressing mode.
e is a signed two's complement number in the range < −126, 129 >.
e − 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e.

Call and Return Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	•	•	X	•	X	•	•	•	11 001 101 CD — n — — n —	3	5	17	
CALL cc, nn	If condition cc is false continue, otherwise same as CALL nn	•	•	X	•	X	•	•	•	11 cc 100 — n — — n —	3	3	10	If cc is false.
											3	5	17	If cc is true.
RET	PC_L ← (SP) PC_H ← (SP + 1)	•	•	X	•	X	•	•	•	11 001 001 C9	1	3	10	
RET cc	If condition cc is false continue, otherwise same as RET	•	•	X	•	X	•	•	•	11 cc 000	1	1	5	If cc is false.
											1	3	11	If cc is true.
RETI	Return from interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 001 101 4D	2	4	14	
RETN[1]	Return from non-maskable interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 000 101 45	2	4	14	
RST p	(SP − 1) ← PC_H (SP − 2) ← PC_L PC_H ← 0 PC_L ← p	•	•	X	•	X	•	•	•	11 t 111	1	3	11	

cc	Condition
000	NZ non-zero
001	Z zero
010	NC non-carry
011	C carry
100	PO parity odd
101	PE parity even
110	P sign positive
111	M sign negative

t	p
000	00H
001	08H
010	10H
011	18H
100	20H
101	28H
110	30H
111	38H

NOTE: [1]RETN loads IFF_2 → IFF_1

Input and Output Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
IN A, (n)	A ← (n)	•	•	X	•	X	•	•	•	11 011 011 DB — n —	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
IN r, (C)	r ← (C) If r = 110 only the flags will be affected	↕	↕	X	↕	X	P	0	•	11 101 101 ED 01 r 000	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INI	(HL) ← (C) B ← B − 1 HL ← HL + 1	X	↕ ①	X	X	X	1	•		11 101 101 ED 10 100 010 A2	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INIR	(HL) ← (C) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	1 ①	X	X	X	1	•		11 101 101 ED 10 110 010 B2	2	5 (If B ≠ 0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B = 0)	16	
IND	(HL) ← (C) B ← B − 1 HL ← HL − 1	X	↕ ①	X	X	X	1	•		11 101 101 ED 10 101 010 AA	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INDR	(HL) ← (C) B ← B − 1 HL ← HL − 1 Repeat until B = 0	X	1 ①	X	X	X	1	•		11 101 101 ED 10 111 010 BA	2	5 (If B ≠ 0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B = 0)	16	
OUT (n), A	(n) ← A	•	•	X	•	X	•	•	•	11 010 011 D3 — n —	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
OUT (C), r	(C) ← r	•	•	X	•	X	•	•	•	11 101 101 ED 01 r 001	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	X	↕ ①	X	X	X	1	•		11 101 101 ED 10 100 011 A3	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	1 ①	X	X	X	1	•		11 101 101 ED 10 110 011 B3	2	5 (If B ≠ 0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B = 0)	16	
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	X	↕ ①	X	X	X	1	•		11 101 101 ED 10 101 011 AB	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}

NOTE: ① If the result of B − 1 is zero the Z flag is set, otherwise it is reset.

Input and Output Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 Repeat until B = 0	X	1	X	X	X	1	•		11 101 101 ED 10 111 011	2	5 (If B ≠ 0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B = 0)	16	

Summary of Flag Operation

Instruction	D_7 S	Z		H		P/V	N	D_0 C	Comments
ADD A, s; ADC A, s	↕	↕	X	↕	X	V	0	↕	8-bit add or add with carry.
SUB s; SBC A, s; CP s; NEG	↕	↕	X	↕	X	V	1	↕	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	↕	↕	X	1	X	P	0	0	Logical operations.
OR s, XOR s	↕	↕	X	0	X	P	0	0	
INC s	↕	↕	X	↕	X	V	0	•	8-bit increment.
DEC s	↕	↕	X	↕	X	V	1	•	8-bit decrement.
ADD DD, ss	•	•	X	X	X	•	0	↕	16-bit add.
ADC HL, ss	↕	↕	X	X	X	V	0	↕	16-bit add with carry.
SBC HL, ss	↕	↕	X	X	X	V	1	↕	16-bit subtract with carry.
RLA, RLCA, RRA; RRCA	•	•	X	0	X	•	0	↕	Rotate accumulator.
RL m; RLC m; RR m; RRC m; SLA m; SRA m; SRL m	↕	↕	X	0	X	P	0	↕	Rotate and shift locations.
RLD; RRD	↕	↕	X	0	X	P	0	•	Rotate digit left and right.
DAA	↕	↕	X	↕	X	P	•	↕	Decimal adjust accumulator.
CPL	•	•	X	1	X	•	1	•	Complement accumulator.
SCF	•	•	X	0	X	•	0	1	Set carry.
CCF	•	•	X	X	X	•	0	↕	Complement carry.
IN r (C)	↕	↕	X	0	X	P	0	•	Input register indirect.
INI, IND, OUTI; OUTD	X	↕	X	X	X	X	1	•	Block input and output. Z = 0 if B ≠ 0 otherwise Z = 0.
INIR; INDR; OTIR; OTDR	X	1	X	X	X	X	1	•	
LDI; LDD	X	X	X	0	X	↕	0	•	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDIR; LDDR	X	X	X	0	X	0	0	•	
CPI; CPIR; CPD; CPDR	X	↕	X	X	X	↕	1	•	Block search instructions. Z = 1 if A = (HL), otherwise Z = 0. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LD A, I, LD A, R	↕	↕	X	0	X	IFF	0	•	The content of the interrupt enable flip-flop (IFF) is copied into the P/V flag.
BIT b, s	X	↕	X	1	X	X	0	•	The state of bit b of location s is copied into the Z flag.

Symbolic Notation

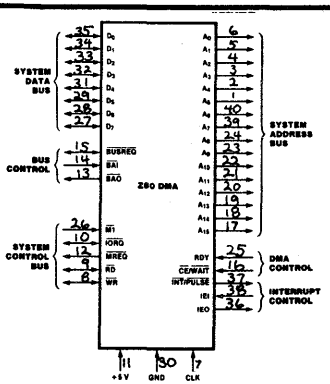
Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.
Z	Zero flag. Z = 1 if the result of the operation is 0.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V = 1 if the result of the operation is even, P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow.
H	Half-carry flag. H = 1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N = 1 if the previous operation was a subtract.
H & N	H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
C	Carry/Link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.

Symbol	Operation
↕	The flag is affected according to the result of the operation.
•	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care."
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range < 0, 255 >.
nn	16-bit value in range < 0, 65535 >.

Zilog

Z8410
Z80® DMA Direct Memory Access Controller

Features



Pin Description

A_0-A_{15}. *System Address Bus* (output, 3-state). Addresses generated by the DMA are sent to both source and destination ports (main memory or I/O peripherals) on these lines.

$\overline{BAI}$. *Bus Acknowledge In* (input, active Low). Signals that the system buses have been released for DMA control. In multiple-DMA configurations, the $\overline{BAI}$ pin of the highest priority DMA is normally connected to the Bus Acknowledge pin of the CPU. Lower-priority DMAs have their $\overline{BAI}$ connected to the $\overline{BAO}$ of a higher-priority DMA.

$\overline{BAO}$. *Bus Acknowledge Out* (output, active Low). In a multiple-DMA configuration, this pin signals that no other higher-priority DMA has requested the system buses. $\overline{BAI}$ and $\overline{BAO}$ form a daisy chain for multiple-DMA priority resolution over bus control.

$\overline{BUSREQ}$. *Bus Request* (bidirectional, active Low, open drain). As an output, it sends requests for control of the system address bus, data bus and control bus to the CPU. As an input, when multiple DMAs are strung together in a priority daisy chain via $\overline{BAI}$ and $\overline{BAO}$, it senses when another DMA has requested the buses and causes this DMA to refrain from bus requesting until the other DMA is finished. Because it is a bidirectional pin, there cannot be any buffers between this DMA and any other DMA. It can, however, have a buffer between it and the CPU because it is unidirectional into the CPU. A pull-up resistor is connected to this pin.

$\overline{CE}$/$\overline{WAIT}$. *Chip Enable and Wait* (input, active Low). Normally this functions only as a $\overline{CE}$ line, but it can also be programmed to serve a $\overline{WAIT}$ function. As a $\overline{CE}$ line from the CPU, it becomes active when $\overline{WR}$ and $\overline{IORQ}$ are active and the I/O port address on the system address bus is the DMA's address, thereby allowing a transfer of control or command bytes from the CPU to the DMA. As a $\overline{WAIT}$ line from memory or I/O devices, after the DMA has received a bus-request acknowledge from the CPU, it causes wait states to be inserted in the DMA's operation cycles thereby slowing the DMA to a speed that matches the memory or I/O device.

CLK. *System Clock* (input). Standard Z-80 single-phase clock at 2.5 MHz (Z-80 DMA) or 4.0 MHz (Z-80A DMA). For slower system clocks, a TTL gate with a pullup resistor may be adequate to meet the timing and voltage level specification. For higher-speed systems, use a clock driver with an active pullup to meet the V_{IH} specification and risetime requirements. In all cases there should be a resistive pullup to the power supply of 10K ohms (max) to ensure proper power when the DMA is reset.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). Commands from the CPU, DMA status, and data from memory or I/O peripherals are transferred on these lines.

IEI. *Interrupt Enable In* (input, active High). This is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this DMA. Thus, this signal blocks lower-priority devices from interrupting while a higher-priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$/PULSE. *Interrupt Request* (output, active Low, open drain). This requests a CPU interrupt. The CPU acknowledges the interrupt by pulling its $\overline{IORQ}$ output Low during an $\overline{M1}$ cycle. It is typically connected to the $\overline{INT}$ pin of the CPU with a pullup resistor and tied to all other $\overline{INT}$ pins in the system. This pin can also be used to generate periodic pulses to an external device. It can be used this way only when the DMA is bus master (i.e., the CPU's $\overline{BUSREQ}$ and $\overline{BUSACK}$ lines are both Low and the CPU cannot see interrupts).

$\overline{IORQ}$. *Input/Output Request* (bidirectional, active Low, 3-state). As an input, this indicates that the lower half of the address bus holds a valid I/O port address for transfer of control or status bytes from or to the CPU, respectively; this DMA is the addressed port if its $\overline{CE}$ pin and its $\overline{WR}$ or $\overline{RD}$ pins are simultaneously active. As an output, after the DMA has taken control of the system buses, it indicates that the 8-bit or 16-bit address bus holds a valid port address for another I/O device involved in a DMA transfer of data. When $\overline{IORQ}$ and $\overline{M1}$ are both active simultaneously, an interrupt acknowledge is indicated.

$\overline{M1}$. *Machine Cycle One* (input, active Low). Indicates that the current CPU machine cycle is an instruction fetch. It is used by the DMA to decode the return-from-interrupt instruction (RETI) (ED-4D) sent by the CPU. During two-byte instruction fetches, $\overline{M1}$ is active as each opcode byte is fetched. An interrupt acknowledge is indicated when both $\overline{M1}$ and $\overline{IORQ}$ are active.

$\overline{MREQ}$. *Memory Request* (output, active Low, 3-state). This indicates that the address bus holds a valid address for a memory read or write operation. After the DMA has taken control of the system buses, it indicates a DMA transfer request from or to memory.

$\overline{RD}$. *Read* (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to read status bytes from the DMA's read registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled read from a memory or I/O port address.

RDY. *Ready* (input, programmable active Low or High). This is monitored by the DMA to determine when a peripheral device associated with a DMA port is ready for a read or write operation. Depending on the mode of DMA operation (Byte, Burst or Continuous), the RDY line indirectly controls DMA activity by causing the $\overline{BUSREQ}$ line to go Low or High.

$\overline{WR}$. *Write* (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to write control or command bytes to the DMA write registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled write to a memory or I/O port address.

Programming

The Z-80 DMA has two programmable fundamental states: (1) an enabled state, in which it can gain control of the system buses and direct the transfer of data between ports, and (2) a disabled state, in which it can initiate neither bus requests nor data transfers. When the DMA is powered up or reset by any means, it is automatically placed into the disabled state. Program commands can be written to it by the CPU in either state, but this automatically puts the DMA in the disabled state, which is maintained until an enable command is issued by the CPU. The CPU must program the DMA in advance of any data search or transfer by addressing it as an I/O port and sending a sequence of control bytes using an Output instruction (such as OTIR for the Z-80 CPU).

Writing. Control or command bytes are written into one or more of the Write Register groups (WR0-WR6) by first writing to the base register byte in that group. All groups have base registers and most groups have additional associated registers. The associated registers in a group are sequentially accessed by first writing a byte to the base register containing register-group identification and pointer bits (1's) to one or more of that base register's associated registers.

This is illustrated in Figure 8b. In this figure, the sequence in which associated registers within a group can be written to is shown by the vertical position of the associated registers. For example, if a byte written to the DMA contains the bits that identify WR0 (bits D0, D1 and D7), and also contains 1's in the bit positions that point to the associated "Port A Starting Address (low byte)" and "Port A Starting Address (high byte)," then the next two bytes written to the DMA will be stored in these two registers, in that order.

Reading. The Read Registers (RR0-RR6) are read by the CPU by addressing the DMA as an I/O port using an Input instruction (such as INIR for the Z-80 CPU). The readable bytes contain DMA status, byte-counter values, and port addresses since the last DMA reset. The registers are always read in a fixed sequence beginning with RR0 and ending with RR6. However, the register read in this sequence is determined by programming the Read Mask in WR6. The sequence of reading is initialized by writing an Initiate Read Sequence or Set Read Status command to WR6. After a Reset DMA, the sequence must be initialized with the Initiate Read Sequence command or a Read Status command. The sequence of reading all registers that are not excluded by the Read Mask register must be completed before a new Initiate Read Sequence or Read Status command.

Fixed-Address Programming. A special circumstance arises when programming a destination port to have a fixed address. The load command in WR6 only loads a fixed address to a port selected as the source, not to a port selected as the destination. Therefore, a fixed destination address must be loaded by temporarily declaring it a fixed-source address and subsequently declaring the true source as such, thereby implicitly making the other a destination.

The following example illustrates the steps in this procedure, assuming that transfers are to occur from a variable-address source (Port A) to a fixed-address destination (Port B):

1. Temporarily declare Port B as source in WR0.
2. Load Port B address in WR6.
3. Declare Port A as source in WR0.

Programming (Continued)

4. Load Port A address in WR6.
5. Enable DMA in WR6.

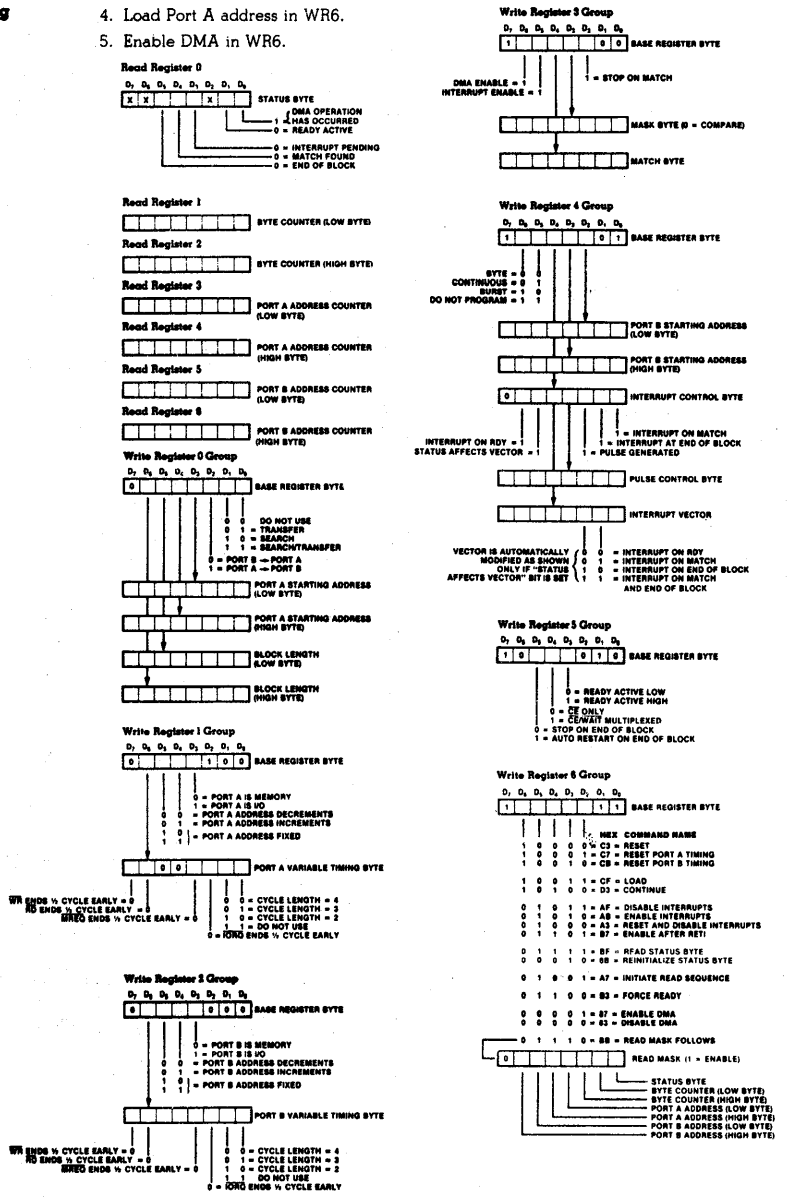


Figure 8b. Write Registers

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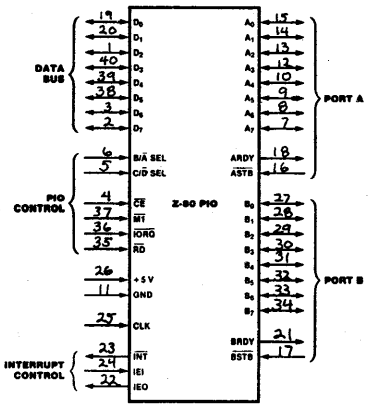
Z8420
Z80® PIO Parallel Input/Output Controller

Features



Pin Description

A_0-A_7. *Port A Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port A of the PIO and a peripheral device. A_0 is the least significant bit of the Port A data bus.

ARDY. *Register A Ready* (output, active High). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. This signal goes active to indicate that the Port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device.

Input Mode. This signal is active when the Port A input register is empty and ready to accept data from the peripheral device.

Bidirectional Mode. This signal is active when data is available in the Port A output register for transfer to the peripheral device. In this mode, data is not placed on the Port A data bus, unless $\overline{ASTB}$ is active.

Control Mode. This signal is disabled and forced to a Low state.

$\overline{ASTB}$. *Port A Strobe Pulse From Peripheral Device* (input, active Low). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the PIO.

Input Mode. The strobe is issued by the peripheral to load data from the peripheral into the Port A input register. Data is loaded into the PIO when this signal is active.

Bidirectional Mode. When this signal is active, data from the Port A output register is gated onto the Port A bidirectional data bus. The positive edge of the strobe acknowledges the receipt of the data.

Control Mode. The strobe is inhibited internally.

B_0-B_7. *Port B Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port B and a peripheral device. The Port B data bus can supply 1.5 mA at 1.5 V to drive Darlington transistors. B_0 is the least significant bit of the bus.

B/$\overline{A}$. *Port B Or A Select* (input, High = B). This pin defines which port is accessed during a data transfer between the CPU and the PIO. A Low on this pin selects Port A; a High selects Port B. Often address bit A_0 from the CPU is used for this selection function.

BRDY. *Register B Ready* (output, active High). This signal is similar to ARDY, except that in the Port A bidirectional mode this signal is High when the Port A input register is empty and ready to accept data from the peripheral device.

$\overline{BSTB}$. *Port B Strobe Pulse From Peripheral Device* (input, active Low). This signal is similar to $\overline{ASTB}$, except that in the Port A bidirectional mode this signal strobes data from the peripheral device into the Port A input register.

C/$\overline{D}$. *Control Or Data Select* (input, High = C). This pin defines the type of data transfer to be performed between the CPU and the PIO. A High on this pin during a CPU write to the PIO causes the Z-80 data bus to be interpreted as a *command* for the port selected by the B/$\overline{A}$ Select line. A Low on this pin means that the Z-80 data bus is being used to transfer data between the CPU and the PIO. Often address bit A_1 from the CPU is used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle. This signal is generally decoded from four I/O port numbers for Ports A and B, data, and control.

CLK. *System Clock* (input). The Z-80 PIO uses the standard single-phase Z-80 system clock.

D_0-D_7. *Z-80 CPU Data Bus* (bidirectional, 3-state). This bus is used to transfer all data and commands between the Z-80 CPU and the Z-80 PIO. D_0 is the least significant bit.

IEI. *Interrupt Enable In* (input, active High). This signal is used to form a priority-interrupt daisy chain when more than one interrupt-driven device is being used. A High level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

Pin Description (Continued)

IEO. *Interrupt Enable Out* (output, active High). The IEO signal is the other signal required to form a daisy chain priority scheme. It is High only if IEI is High and the CPU is not servicing an interrupt from this PIO. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When $\overline{INT}$ is active the Z-80 PIO is requesting an interrupt from the Z-80 CPU.

$\overline{IORQ}$. *Input/Output Request* (input from Z-80 CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{RD}$ to transfer commands and data between the Z-80 CPU and the Z-80 PIO. When $\overline{CE}$, $\overline{RD}$, and $\overline{IORQ}$ are active, the port addressed by B/$\overline{A}$ transfers data to the CPU (a read operation). Conversely, when $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is not, the port addressed by B/$\overline{A}$ is written into from the CPU with either data or control information, as specified by C/$\overline{D}$. Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt; the interrupting port automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{M1}$. *Machine Cycle* (input from CPU, active Low). This signal is used as a sync pulse to control several internal PIO operations. When both the $\overline{M1}$ and $\overline{RD}$ signals are active, the Z-80 CPU is fetching an instruction from memory. Conversely, when both $\overline{M1}$ and $\overline{IORQ}$ are active, the CPU is acknowledging an interrupt. In addition, $\overline{M1}$ has two other functions within the Z-80 PIO: it synchronizes the PIO interrupt logic; when $\overline{M1}$ occurs without an active $\overline{RD}$ or $\overline{IORQ}$ signal, the PIO is reset.

$\overline{RD}$. *Read Cycle Status* (input from Z-80 CPU, active Low). If $\overline{RD}$ is active, or an I/O operation is in progress, $\overline{RD}$ is used with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{IORQ}$ to transfer data from the Z-80 PIO to the Z-80 CPU.

Programming

Mode 0, 1, or 2. *(Byte Input, Output, or Bidirectional).* Programming a port for Mode 0, 1, or 2 requires two words per port. These words are:

A Mode Control Word. Selects the port operating mode (Figure 6). This word may be written any time.

An Interrupt Vector. The Z-80 PIO is designed for use with the Z-80 CPU in interrupt Mode 2 (Figure 7). When interrupts are enabled, the PIO must provide an interrupt vector.

Mode 3. *(Bit Input/Output).* Programming a port for Mode 3 operation requires a control word, a vector (if interrupts are enabled), and three additional words, described as follows:

I/O Register Control. When Mode 3 is selected, the mode control word must be followed by another control word that sets the I/O control register, which in turn defines which port lines are inputs and which are outputs (Figure 8).

Interrupt Control Word. In Mode 3, handshake is not used. Interrupts are generated as a logic function of the input signal levels. The interrupt control word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), and OR (if any one of the input bits changes to the active level, an interrupt is triggered). Bit D_6 sets the logic function, as shown in Figure 9. The active level of the input bits can be set either High or Low. The active level is controlled by Bit D_5.

Mask Control Word. This word sets the mask control register, allowing any unused bits to be masked off. If any bits are to be masked, then D_4 must be set. When D_4 is set, the next word written to the port must be a mask control word (Figure 10).

Interrupt Disable. There is one other control word which can be used to enable or disable a port interrupt. It can be used without changing the rest of the interrupt control word (Figure 11).

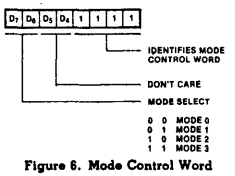


Figure 6. Mode Control Word

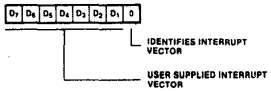


Figure 7. Interrupt Vector Word

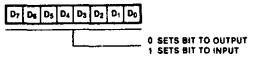


Figure 8. I/O Register Control Word

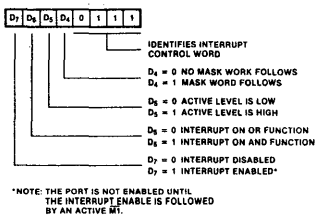


Figure 9. Interrupt Control Word

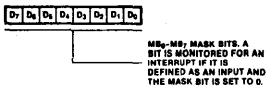


Figure 10. Mask Control Word

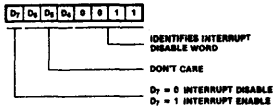
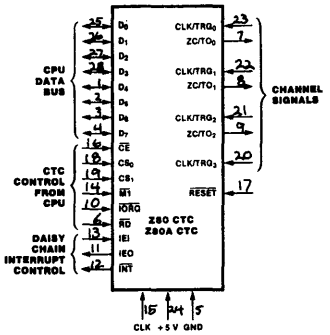


Figure 11. Interrupt Disable Word

Zilog

Z8430
Z80® CTC Counter/ Timer Circuit

Features



Pin Description

$\overline{CE}$. *Chip Enable* (input, active Low). When enabled the CTC accepts control words, interrupt vectors, or time constant data words from the data bus during an I/O write cycle; or transmits the contents of the down-counter to the CPU during an I/O read cycle. In most applications this signal is decoded from the eight least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter-timer channels.

CLK. *System Clock* (input). Standard single-phase Z-80 system clock.

CLK/TRG0-CLK/TRG3. *External Clock/Timer Trigger* (input, user-selectable active High or Low). Four pins corresponding to the four Z-80 CTC channels. In counter mode, every active edge on this pin decrements the down-counter. In timer mode, an active edge starts the timer.

CS_0-CS_1. *Channel Select* (inputs active High). Two-bit binary address code selects one of the four CTC channels for an I/O write or read (usually connected to A_0 and A_1).

D_0-D_7. *System Data Bus* (bidirectional, 3-state). Transfers all data and commands between the Z-80 CPU and the Z-80 CTC.

IEI. *Interrupt Enable In* (input, active High). A High indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the Z-80 CPU.

IEO. *Interrupt Enable Out* (output, active High). High only if IEI is High and the Z-80 CPU is not servicing an interrupt from any Z-80 CTC channel. IEO blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). Low when any Z-80 CTC channel that has been programmed to enable interrupts has a zero-count condition in its down-counter

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). Used with $\overline{CE}$ and $\overline{RD}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC. During a write cycle, $\overline{IORQ}$ and $\overline{CE}$ are active and $\overline{RD}$ inactive. The Z-80 CTC does not receive a specific write signal; rather, it internally generates its own from the inverse of an active $\overline{RD}$ signal. In a read cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ are active; the contents of the down-counter are read by the Z-80 CPU. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest priority interrupting channel places its interrupt vector on the Z-80 data bus.

$\overline{M1}$. *Machine Cycle One* (input from CPU, active Low). When $\overline{M1}$ and $\overline{IORQ}$ are active, the Z-80 CPU is acknowledging an interrupt. The Z-80 CTC then places an interrupt vector on the data bus if it has highest priority, and if a channel has requested an interrupt ($\overline{INT}$).

$\overline{RD}$. *Read Cycle Status* (input, active Low). Used in conjunction with $\overline{IORQ}$ and $\overline{CE}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC.

$\overline{RESET}$. *Reset* (input active Low). Terminates all down-counts and disables all interrupts by resetting the interrupt bits in all control registers; the ZC/TO and the Interrupt outputs go inactive; IEO reflects IEI; D_0-D_7 go to the high-impedance state.

ZC/TO_0-ZC/TO_2. *Zero Count/Timeout* (output, active High). Three ZC/TO pins corresponding to Z-80 CTC channels 2 through 0 (Channel 3 has no ZC/TO pin). In both counter and timer modes the output is an active High pulse when the down-counter decrements to zero.

Programming

Each Z-80 CTC channel must be programmed prior to operation. Programming consists of writing two words to the I/O port that corresponds to the desired channel. The first word is a control word that selects the operating mode and other parameters; the second word is a time constant, which is a binary data word with a value from 1 to 256. A time constant word must be preceded by a channel control word.

After initialization, channels may be reprogrammed at any time. If updated control and time constant words are written to a channel during the count operation, the count continues to zero before the new time constant is loaded into the counter.

If the interrupt on any Z-80 CTC channel is enabled, the programming procedure should also include an interrupt vector. Only one vector is required for all four channels, because the interrupt logic automatically modifies the vector for the channel requesting service.

A control word is identified by a 1 in bit 0. A 0 in bit 2 indicates a time constant word is to follow. Interrupt vectors are always addressed to Channel 0, and identified by a 0 in bit 0.

Addressing. During programming, channels are addressed with the channel select pins CS_1 and CS_2. A 2-bit binary code selects the appropriate channel as shown in the following table.

Channel	CS_1	CS_0
0	0	0
1	0	1
2	1	0
3	1	1

Reset. The CTC has both hardware and software resets. The hardware reset terminates all down-counts and disables all CTC interrupts by resetting the interrupt bits in the control registers. In addition, the ZC/TO and Interrupt outputs go inactive, IEO reflects IEI, and D_0–D_7 go to the high-impedance state. All channels must be completely reprogrammed after a hardware reset.

The software reset is controlled by bit 1 in the channel control word. When a channel receives a software reset, it stops counting. When a software reset is used, the other bits in the control word also change the contents of the channel control register. After a software reset a new time constant word must be written to the same channel.

If the channel control word has both bits D_1 and D_2 set to 1, the addressed channel stops operating, pending a new time constant word. The channel is ready to resume after the new constant is programmed. In timer mode, if D_3 = 0, operation is triggered automatically when the time constant word is loaded.

Channel Control Word Programming. The channel control word is shown in Figure 5. It sets the modes and parameters described below.

Interrupt Enable. D_7 enables the interrupt, so that an interrupt output ($\overline{INT}$) is generated at zero count. Interrupts may be programmed in either mode and may be enabled or disabled at any time.

Operating Mode. D_6 selects either timer or counter mode.

Prescaler Factor. (Timer Mode Only). D_5 selects factor—either 16 or 256.

Trigger Slope. D_4 selects the active edge or slope of the CLK/TRG input pulses. Note that reprogramming the CLK/TRG slope during operation is equivalent to issuing an active edge. If the trigger slope is changed by a control word update while a channel is pending operation in timer mode, the result is the same as a CLK/TRG pulse and the timer starts. Similarly, if the channel is in counter mode, the counter decrements.

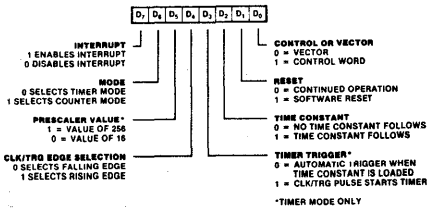


Figure 5. Channel Control Word

Programming (Continued)

Trigger Mode (Timer Mode Only). D_3 selects the trigger mode for timer operation. When D_3 is reset to 0, the timer is triggered automatically. The time constant word is programmed during an I/O write operation, which takes one machine cycle. At the end of the write operation there is a setup delay of one clock period. The timer starts automatically (decrements) on the rising edge of the second clock pulse (T_2) of the machine cycle following the write operation. Once started, the timer runs continuously. At zero count the timer reloads automatically and continues counting without interruption or delay, until stopped by a reset.

When D_3 is set to 1, the timer is triggered externally through the CLK/TRG input. The time constant word is programmed during an I/O write operation, which takes one machine cycle. The timer is ready for operation on the rising edge of the second clock pulse (T_2) of the following machine cycle. Note that the first timer decrement follows the active edge of the CLK/TRG pulse by a delay time of one clock cycle if a minimum setup time to the rising edge of clock is met. If this minimum is not met, the delay is extended by another clock period. Consequently, for immediate triggering, the CLK/TRG input must precede T_2 by one clock cycle plus its minimum setup time. If the minimum time is not met, the timer will start on the third clock cycle (T_3).

Once started the timer operates continuously, without interruption or delay, until stopped by a reset.

Time Constant to Follow. A 1 in D_2 indicates that the next word addressed to the selected channel is a time constant data word for the time constant register. The time constant word may be written at any time.

A 0 in D_2 indicates no time constant word is to follow. This is ordinarily used when the channel is already in operation and the new channel control word is an update. A channel will not operate without a time constant value. The only way to write a time constant value is to write a control word with D_2 set.

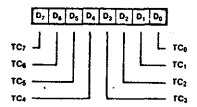


Figure 6. Time Constant Word

Software Reset. Setting D_1 to 1 causes a software reset, which is described in the **Reset** section.

Control Word. Setting D_0 to 1 identifies the word as a control word.

Time Constant Programming. Before a channel can start counting it must receive a time constant word from the CPU. During programming or reprogramming, a channel control word in which bit 2 is set must precede the time constant word to indicate that the next word is a time constant. The time constant word can be any value from 1 to 256 (Figure 6). Note that 00_{16} is interpreted as 256.

In timer mode, the time interval is controlled by three factors:

- The system clock period (ϕ)
- The prescaler factor (P), which multiplies the interval by either 16 or 256
- The time constant (T), which is programmed into the time constant register

Consequently, the time interval is the product of $\phi \times P \times T$. The minimum timer resolution is $16 \times \phi$ (4 μs with a 4 MHz clock). The maximum timer interval is $256 \times \phi \times 256$ (16.4 ms with a 4 MHz clock). For longer intervals timers may be cascaded.

Interrupt Vector Programming. If the Z-80 CTC has one or more interrupts enabled, it can supply interrupt vectors to the Z-80 CPU. To do so, the Z-80 CTC must be pre-programmed with the most-significant five bits of the interrupt vector. Programming consists of writing a vector word to the I/O port corresponding to the Z-80 CTC Channel 0. Note that D_0 of the vector word is always zero, to distinguish the vector from a channel control word. D_1 and D_2 are not used in programming the vector word. These bits are supplied by the interrupt logic to identify the channel requesting interrupt service with a unique interrupt vector (Figure 7). Channel 0 has the highest priority.

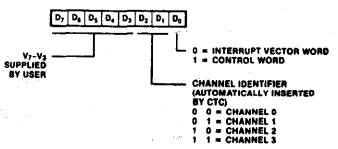
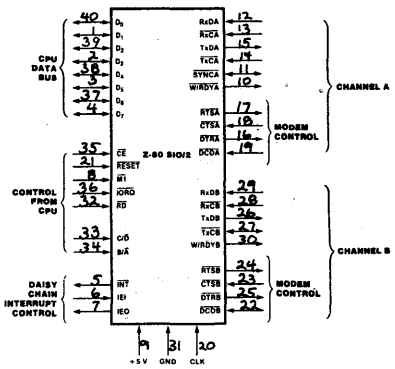


Figure 7. Interrupt Vector Word

Zilog

Z8440
Z80® SIO Serial Input/Output Controller

Features



Pin Description

Figures 1 through 6 illustrate the three pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together in the three bonding options offered:

- Z-80 SIO/2 lacks $\overline{SYNCB}$
- Z-80 SIO/1 lacks $\overline{DTRB}$
- Z-80 SIO/0 has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together

The first bonding option above (SIO/2) is the preferred version for most applications. The pin descriptions are as follows:

B/$\overline{A}$. *Channel A Or B Select* (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A_0 from the CPU is often used for the selection function.

C/$\overline{D}$. *Control Or Data Select* (input, High selects Control). This input defines the type of information transfer performed between the CPU and the SIO. A High at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A Low at C/$\overline{D}$ means that the information on the data bus is data. Address bit A_1 is often used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low level at this input enables the SIO to accept command or data input from the CPU during a write cycle or to transmit data to the CPU during a read cycle.

CLK. *System Clock* (input). The SIO uses the standard Z-80 System Clock to synchronize internal signals. This is a single-phase clock.

$\overline{CTSA}$, $\overline{CTSB}$. *Clear To Send* (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). The system data bus transfers data and commands between the CPU and the Z-80 SIO. D_0 is the least significant bit.

$\overline{DCDA}$, $\overline{DCDB}$. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if the SIO is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffering does not guarantee a specific noise-level margin.

$\overline{DTRA}$, $\overline{DTRB}$. *Data Terminal Ready* (outputs, active Low). These outputs follow the state programmed into Z-80 SIO. They can also be programmed as general-purpose outputs.

In the Z-80 SIO/1 bonding option, $\overline{DTRB}$ is omitted.

IEI. *Interrupt Enable In* (input, active High). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When the SIO is requesting an interrupt, it pulls $\overline{INT}$ Low.

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). $\overline{IORQ}$ is used in conjunction with

Pin Description (Continued)

B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$ and $\overline{RD}$ to transfer commands and data between the CPU and the SIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are all active, the channel selected by B/$\overline{A}$ transfers data to the CPU (a read operation). When $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is inactive, the channel selected by B/$\overline{A}$ is written to by the CPU with either data or control information as specified by C/$\overline{D}$. If $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{M1}$. *Machine Cycle* (input from Z-80 CPU, active Low). When $\overline{M1}$ is active and $\overline{RD}$ is also active, the Z-80 CPU is fetching an instruction from memory; when $\overline{M1}$ is active while $\overline{IORQ}$ is active, the SIO accepts $\overline{M1}$ and $\overline{IORQ}$ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the Z-80 CPU.

$\overline{RxCA}$, $\overline{RxCB}$. *Receiver Clocks* (inputs). Receive data is sampled on the rising edge of $\overline{RxC}$. The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. These clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).

In the Z-80 SIO/0 bonding option, $\overline{RxCB}$ is bonded together with $\overline{TxCB}$.

$\overline{RD}$. *Read Cycle Status* (input from CPU, active Low). If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with B/$\overline{A}$, $\overline{CE}$ and $\overline{IORQ}$ to transfer data from the SIO to the CPU.

RxDA, RxDB. *Receive Data* (inputs, active High). Serial data at TTL levels.

$\overline{RESET}$. *Reset* (input, active Low). A Low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High and disables all interrupts. The control registers must be rewritten after the SIO is reset and before data is transmitted or received.

$\overline{RTSA}$, $\overline{RTSB}$. *Request To Send* (outputs, active Low). When the RTS bit in Write Register 5 (Figure 14) is set, the $\overline{RTS}$ output goes Low. When the RTS bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{SYNCA}$, $\overline{SYNCB}$. *Synchronization* (inputs/outputs, active Low). These pins can act either as inputs or outputs. In the asynchronous receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0 (Figure 13), but have no other function. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven Low on the second rising edge of $\overline{RxC}$ after that rising edge of $\overline{RxC}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced Low, it should be kept Low until the CPU informs the external synchronization detect logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode.

In the internal synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.

In the Z-80 SIO/2 bonding option, $\overline{SYNCB}$ is omitted.

$\overline{TxCA}$, $\overline{TxCB}$. *Transmitter Clocks* (inputs). In asynchronous modes, the Transmitter Clocks may be 1, 16, 32 or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified). Transmitter Clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation.

In the Z-80 SIO/0 bonding option, $\overline{TxCB}$ is bonded together with $\overline{RxCB}$.

TxDA, TxDB. *Transmit Data* (outputs, active High). Serial data at TTL levels. TxD changes from the falling edge of $\overline{TxC}$.

$\overline{W/RDYA}$, $\overline{W/RDYB}$. *Wait/Ready A, Wait/Ready B* (outputs, open drain when programmed for Wait function, driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

Programming

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first; then the interrupt mode; and finally, receiver or transmitter enable.

Both channels contain registers that must be programmed via the system program prior to operation. The channel-select input (B/$\overline{A}$) and the control/data input (C/$\overline{D}$) are the command-structure addressing controls, and are normally controlled by the CPU address bus. Figures 15 and 16 illustrate the timing relationships for programming the write registers and transferring data and status.

Read Registers. The SIO contains three read registers for Channel B and two read registers for Channel A (RR0-RR2 in Figure 13) that can be read to obtain the status information; RR2 contains the internally-modifiable interrupt vector and is only in the Channel B register set. The status information includes error conditions, interrupt vector and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing a read instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occurred, all the appropriate error bits can be read from a single register (RR1).

Write Registers. The SIO contains eight write registers for Channel B and seven write registers for Channel A (WR0-WR7 in Figure 14) that are programmed separately to configure the functional personality of the channels; WR2 contains the interrupt vector for both channels and is only in the Channel B register set. With the exception of WR0, programming the write registers requires two bytes. The first byte is to WR0 and contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the SIO.

WR0 is a special case in that all of the basic commands can be written to it with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This implies that a channel reset must not be combined with the pointing to any register.

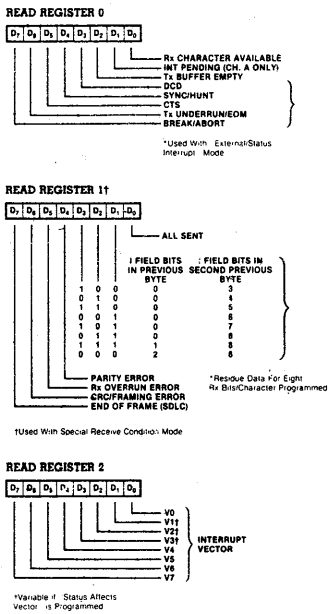


Figure 13. Read Register Bit Functions

Programming (Continued)

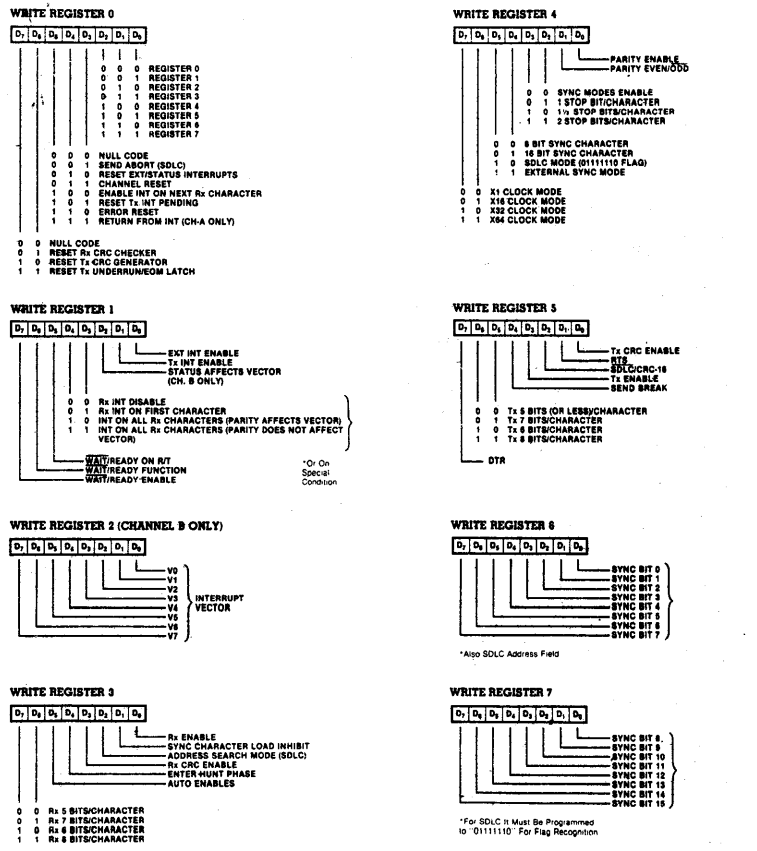


Figure 14. Write Register Bit Functions

B900008-001

PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A3
2024700	CAP., 100 pf 50V 5%	C18,19
2029300	CAP., 330 pf 50V 10%	C3-6,8-11, 13-17
2026100	CAP., 22 uf 50V ELECT	C22,CA,CB,CC
2028700	CAP., .01 uf 16V +80%-20%	C1,20,25,26,27
2031300	CAP., 0.1 uf 16V +80%-20%	UNMARKED,& C2, 7,12
2050600	IC Z80A-SIO/2	A2-4,27-29,55, 56,86,87
2036200	IC 74LS245	A78
2038000	IC 74LS175	A32
2027600	IC 74LS163	A37,73
2024600	IC 74S04	A21,58,72,79
2050400	IC Z80-A PIO	A7
2047000	IC 74S11	A34,60
2040800	IC 93S16	A36
2042800	OSC 16 MHZ	A20
2050800	IC Z80A CTC	A10,11
2029400	IC 75189	A5,18,30
2029200	IC 75188	A6,19,31
2026600	IC 74LS74	A62,63,66,68, 69,97
2025800	IC 74LS32	A64,74,76,80, 81,98
2025200	IC 74LS08	A49,50,51,61, 65,77,82,83
2026400	IC 74S74	A53,70

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PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A3
2038800	IC 74S32	A99
2024000	IC 74S00	A100
2024800	IC 74LS04	A48,59,67
2043600	IC 7438	A14-17
2041000	IC 74LS138	A45-47,84
2041400	IC 74S10	A101
2038400	IC 74S133	A71
2024200	IC 74LS00	A92
2044000	IC 74LS240	A25,102,103
2047200	IC 74S225	A22,23,38,39
2039000	IC 7416	A44
2035400	IC 7414	A75
2037600	IC 74LS273	A90
2051000	IC Z80A CPU	A95
2051200	IC Z80A DMA	A94
2037400	IC 74LS365	A93,107,108
2038200	IC 74S157	A106,109
8100053	IC SYS PROG EPROM 2352	A96
2043200	IC 8212	A88,89
2051600	IC MB8264E,200NS	A110-125
2044800	IC 74S138	A91
2040000	IC 74LS11	A43,57
2044200	IC 74LS244	A1,8,9,12,24 26,40,41,54,85
2037800	IC 74S240	A105

B900008-001

PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A3
2045900	TRANSISTOR, 2N2907	Q1,2
2048100	DIODE, LED	CR2-5
2047500	DIODE, 1N914	CR1
2051500	RES. 330 ohm 5% 1/4W	R1-4,29,30,50, 51
2052100	RES. 1K ohm 5% 1/4W	R5,6,15,17,21, 25,31-35,38-41, 44,69
2034300	RES. 200 ohm 5% 1/4W	R13,14
2051100	RES. 68 ohm 5% 1/4W	R16,18,64-67
2034700	RES. 20 ohm 5% 1/4W	R19,20
2034500	RES. 33 ohm 5% 1/4W	R26,36,37,43, 52,56-63
2053100	RES. 4.7K OHM 5% 1/4	R10-12,22-24,42 46,53-55,68
2041300	RES. PACK 4.7K 10pin SIP	RP1,6-8,11
2042100	RES. PACK 330 10pin SIP	RP3,5,10
2041900	RES. PACK 220 10pin SIP	RP2,4,9
2042900	RES. PACK 4.7K 8 PIN SIP	RP12
2041700	RES. PACK 33 ohm 16pin DIP	A104
2040300	RES. 220 ohm 5% 1/4W	R27,28,48,49
2096700	DIP-SWITCH 16 PIN	A13
2098501	DIP-ADAPTOR PLUG 16 PIN	A33,35
2098402	SOCKET, 40 PIN	A2-4,7,27-29, 55,56,86,87, 94,95
2098404	SOCKET, 28 PIN	A10,11
2098401	SOCKET, 24 PIN	A96

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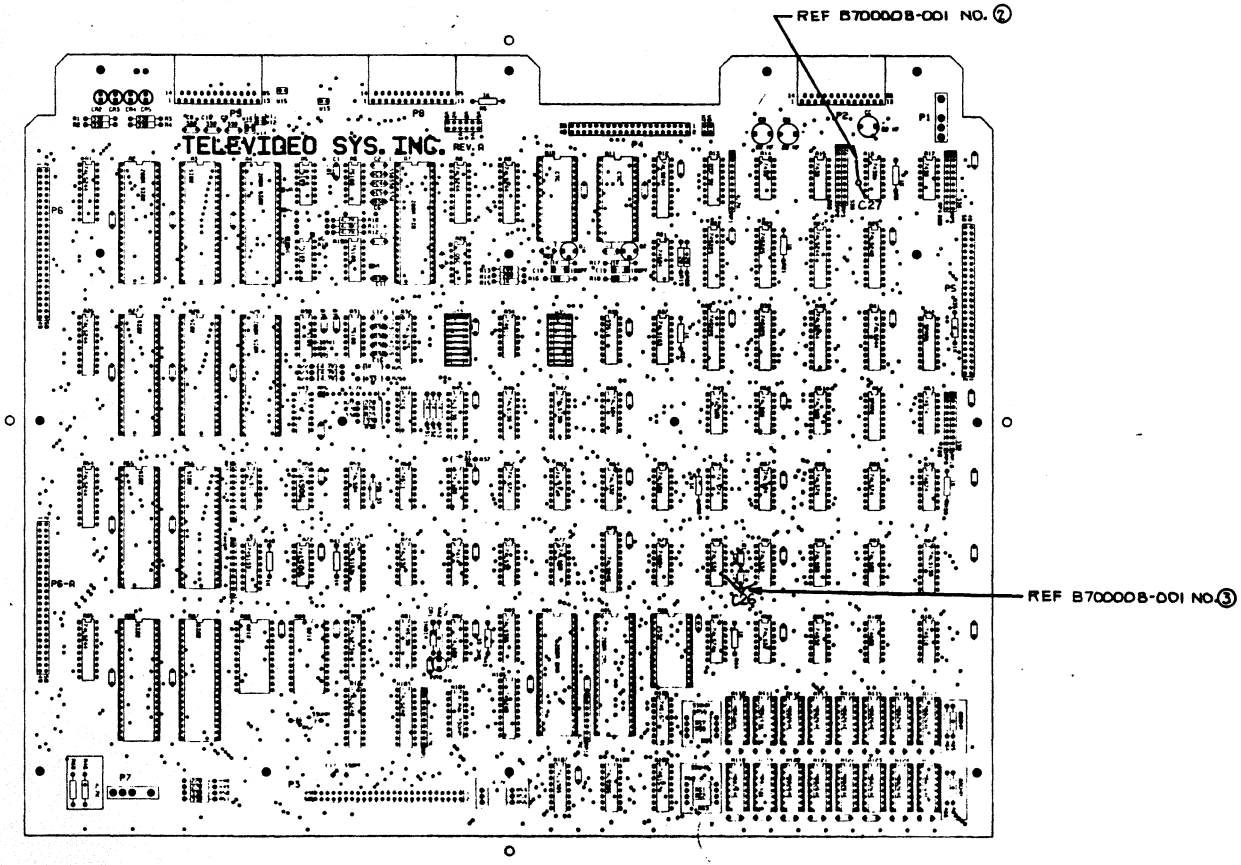
PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A3
2098405	SOCKET, 16 PIN	A110-125
2097800	CONN.25PIN,D-SUB,FEM-PCB	P2,8,9
2098107	CONN.40 PIN HEADER,STRAIGHT	P4
2098108	CONN.50 PIN HEADER,STRAIGHT	P3,P5,P6,P6A
2098700	CONN. 5 PIN WAFER, R/A	P1,7

		DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 174	1-20-82	wchan
	A1	PROD REL PER ECO 212, 224	3/2/82	wchan
	A2	PROD REL PER ECO 225	3/12/82	wchan
	A3	PROD REL PER ECO 255, 276	9/2/82	VS WILLEY
	A4	PROD REL PER ECO 381	6/29/83	wchan



NOTE: UNLESS OTHERWISE SPECIFIED

1. REFER TO SEPARATE PARTS LIST FOR COMPLETE IDENTIFICATION OF PEFERENCE DESIGNATION.
2. MADE FROM B800008-001 FAB REV A.
3. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
4. RUBER STAMP REV. LETTER APPROXIMATELY WHERE SHOWN.

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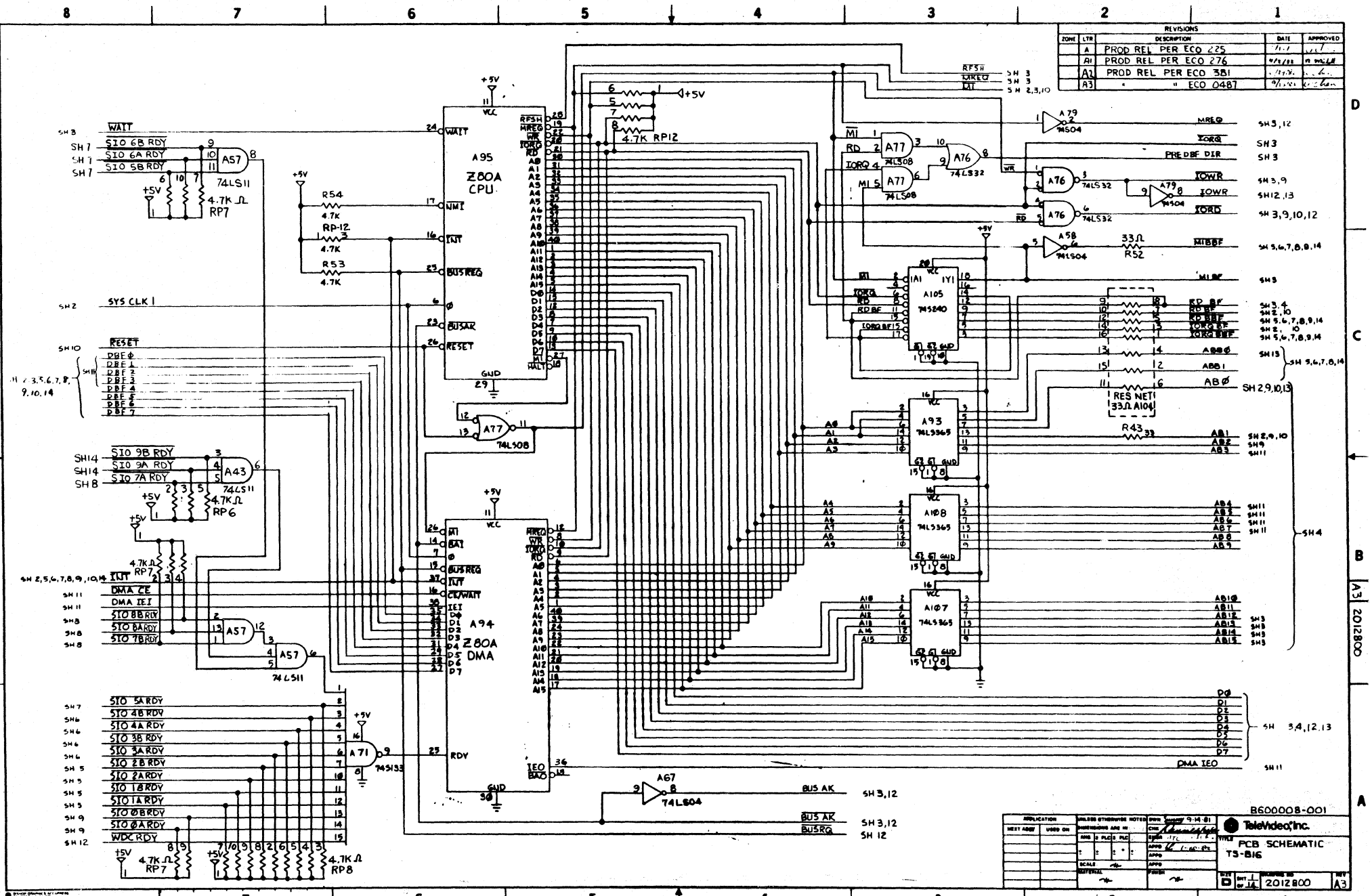
SIZE D | SHT 1 OF 1 | DRAWING NO 20129-00 | REV A4

20129-00


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | PROD REL PER ECO 225
A1 | PROD REL PER ECO 276
A2 | PROD REL PER ECO 381
A3 | " " ECO 0487
A95 Z80A CPU
A94 Z80A DMA
A105 74S240
A93 74LS365
A106 74LS365
A107 74LS365
A77 74LS08
A76 74LS32
A79 74S04
A58 74LS04
A67 74LS04
A71 74S133
A57 74LS11
A43 74LS11
R54 4.7K
RP-12 4.7K
R53 4.7K
4.7K RP12
33Ω R52
RES NET 33Ω A104
R43 33
4.7K RP7
4.7K RP6
4.7K RP8
WAIT
SYS CLK I
RESET
DBF 0
DBF 1
DBF 2
DBF 3
DBF 4
DBF 5
DBF 6
DBF 7
SIO 9B RDY
SIO 9A RDY
SIO 7A RDY
DMA CE
DMA IEI
SIO 8B RDY
SIO 8A RDY
SIO 7B RDY
SIO 5A RDY
SIO 4B RDY
SIO 4A RDY
SIO 3B RDY
SIO 3A RDY
SIO 2B RDY
SIO 2A RDY
SIO 1B RDY
SIO 1A RDY
SIO 0B RDY
SIO 0A RDY
WDC RDY
BUS AK
BUS AR
BUS RQ
MREQ
IORQ
PRE DBF DIR
IOWR
IORD
MIBBF
RD BF
RD BBF
IORQ BF
IORQ BBF
DMA IEO
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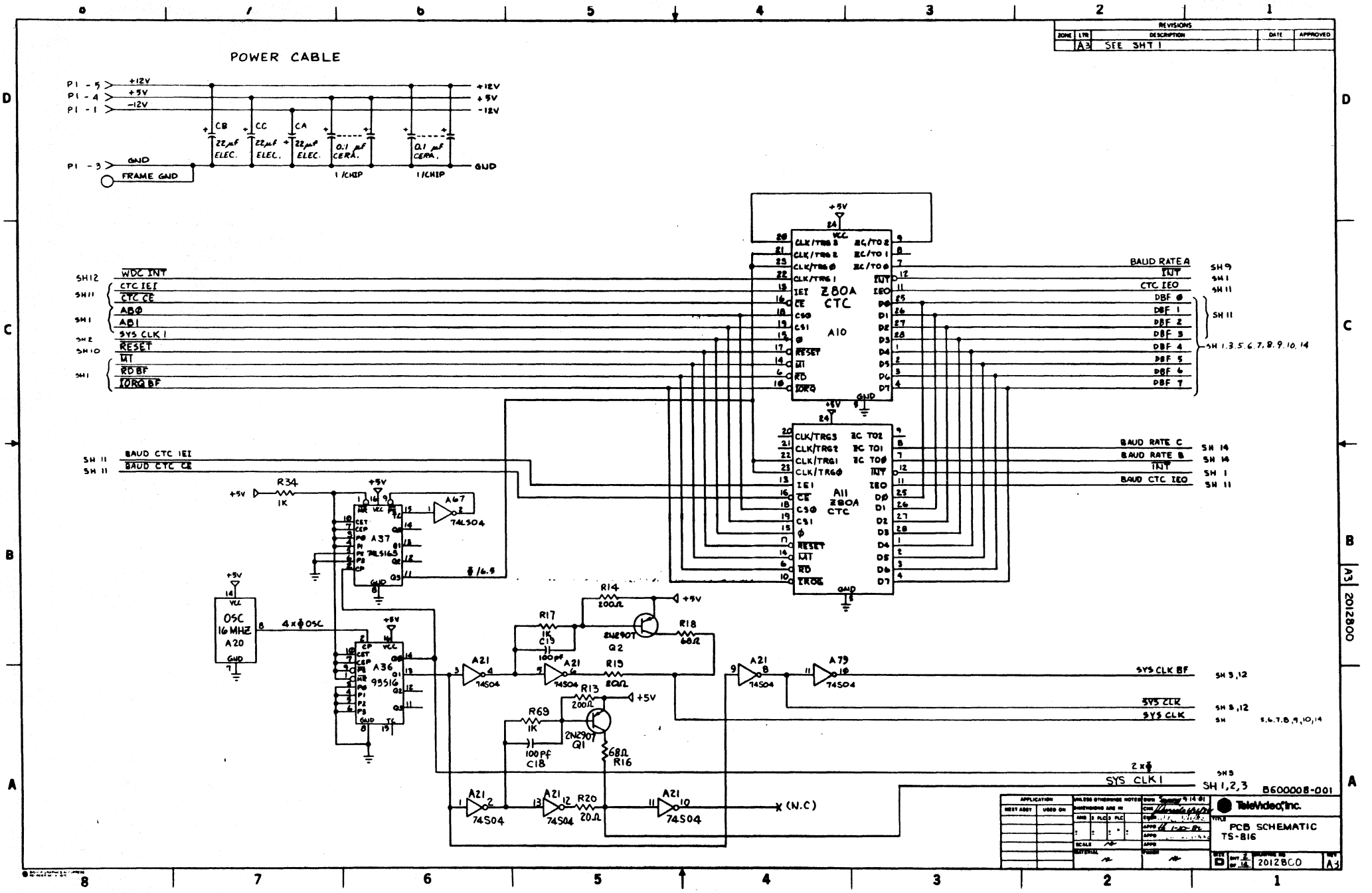
A3


POWER CABLE
P1 - 5 +12V
P1 - 4 +5V
P1 - 1 -12V
P1 - 3 GND
FRAME GND
CB 22µf ELEC.
CC 22µf ELEC.
CA 22µf ELEC.
0.1 µf CERA. 1/CHIP
0.1 µf CERA. 1/CHIP
+12V
+5V
-12V
GND
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A3 SEE SHT 1
Z80A CTC A10
Z80A CTC A11
WDC INT
CTC IEI
CTC CE
AB0
AB1
SYS CLK 1
RESET
WT
RD BF
IORQ BF
BAUD CTC IEI
BAUD CTC CE
BAUD RATE A
CTC IEO
DBF 0
DBF 1
DBF 2
DBF 3
DBF 4
DBF 5
DBF 6
DBF 7
BAUD RATE C
BAUD RATE B
INT
BAUD CTC IEO
R34 1K
A37 74LS163
A67 74LS04
÷16
OSC 16 MHZ A20
4x OSC
A36 95516
R14 200Ω
R17 1K
C19 100pf
2NE907 Q2
R18 68Ω
R15 82Ω
R13 200Ω
R69 1K
C18 100pf
2N2907 Q1
68Ω R16
R20 20Ω
A21 74S04
A79 74S04
SYS CLK BF
SYS CLK
SYS CLK 1
2x
X (N.C)
B600008-001
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2012BCO
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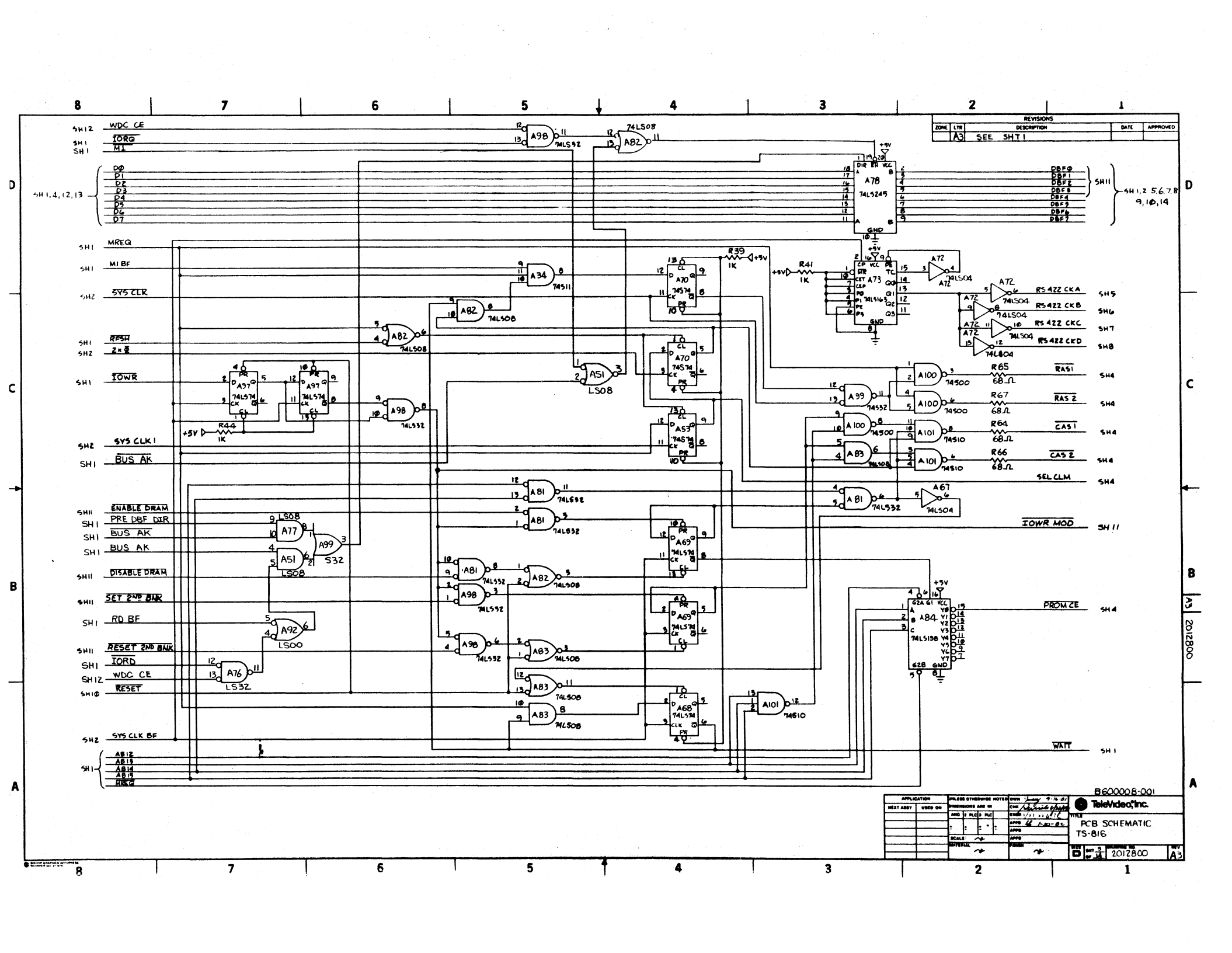
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A3 SEE SHT 1
WDC CE
IORQ
M1
D0 D1 D2 D3 D4 D5 D6 D7
MREQ
MI BF
SYS CLR
RFSH
2xB
IOWR
SYS CLK 1
BUS AK
ENABLE DRAM
PRE DBF DIR
DISABLE DRAM
SET 2ND BNK
RD BF
RESET 2ND BNK
IORD
RESET
SYS CLK BF
A0 A1 A2 A3 A4 A5 A6 A7
DBF0 DBF1 DBF2 DBF3 DBF4 DBF5 DBF6 DBF7
RS422 CKA
RS422 CKB
RS422 CKC
RS422 CKD
RAS1
RAS 2
CAS1
CAS 2
SEL CLM
IOWR MOD
PROM CE
WAIT
A78 74LS245
A73 74LS163
A84 74LS138
A34 74S11
A98 74LS32
A82 74LS08
A51 LS08
A77 LS08
A99 S32
A92 LS00
A76 LS32
A97 74LS74
A70 74S74
A53 74S74
A69 74LS74
A68 74S74
A72 74LS04
A100 74S00
A101 74S10
A83 74LS08
A81 74LS32
R39 1K
R41 1K
R44 1K
R65 68Ω
R67 68Ω
R64 68Ω
R66 68Ω
B600008-001
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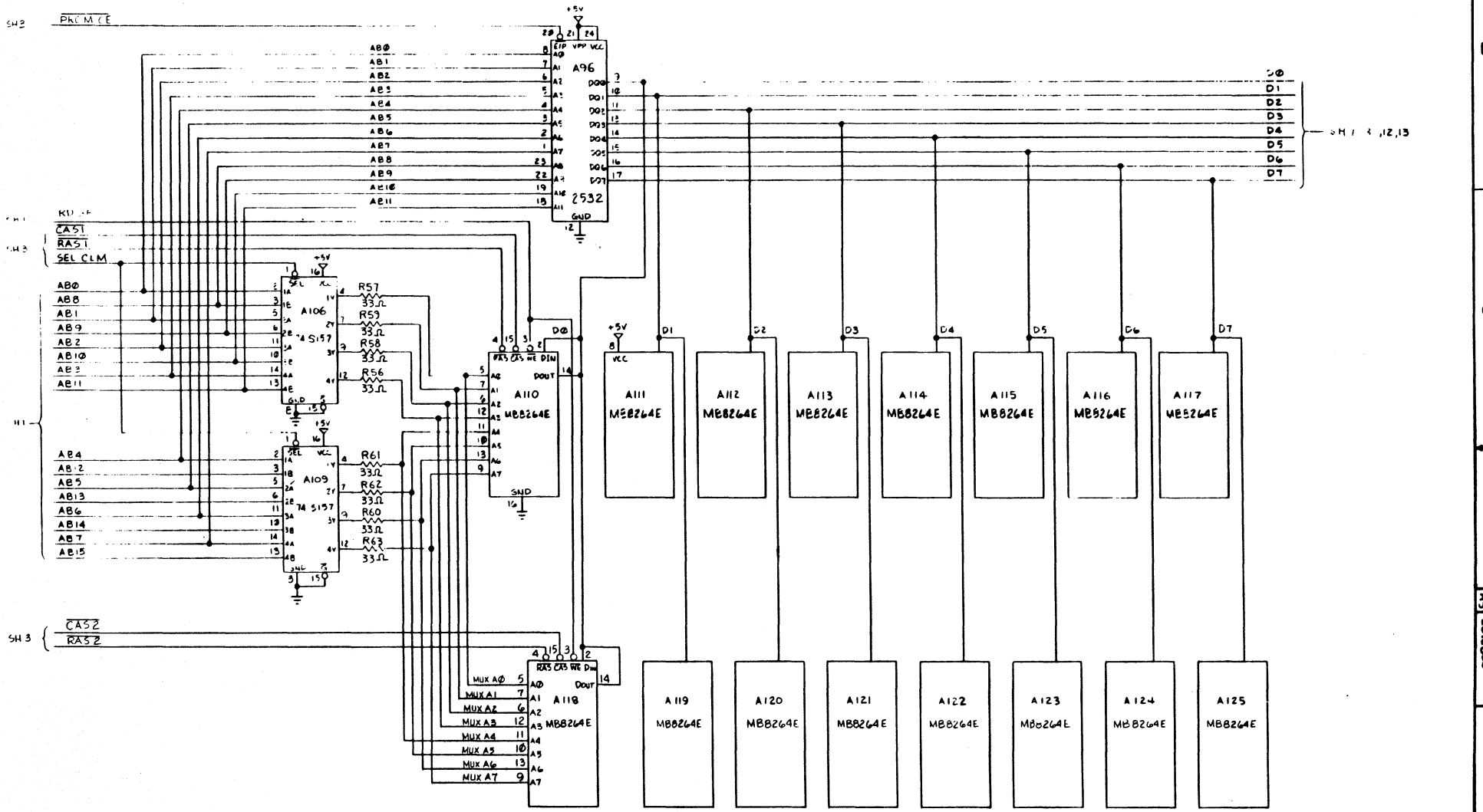
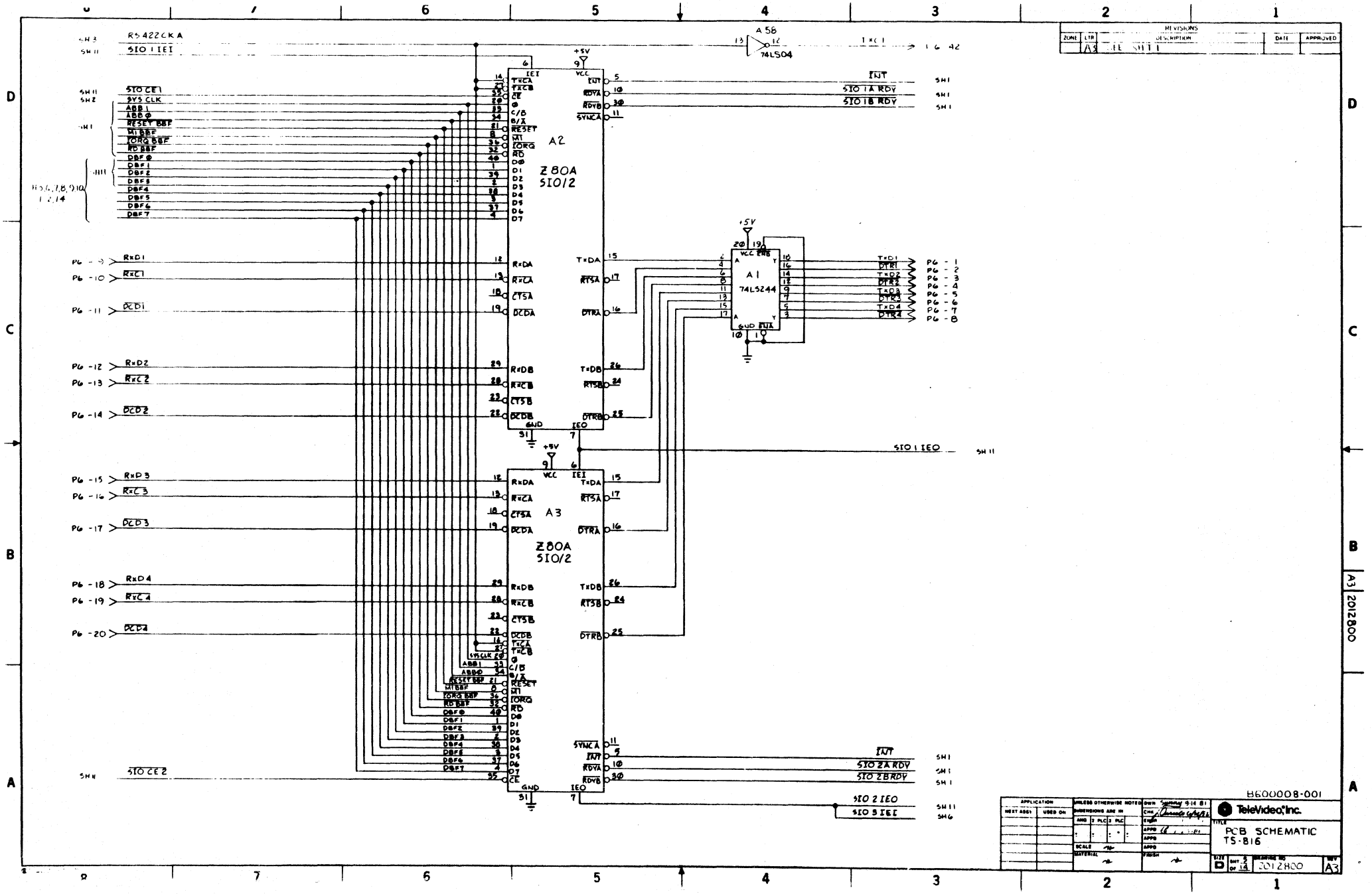


APPLICATION		UNLESS OTHERWISE NOTED	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	TITLE: PCB SCHEMATIC TS-816
		SCALE	SIZE D
			DRAWING NO 20128 00
			REV A3

B000008-001


A2
Z80A SIO/2
A3
Z80A SIO/2
A1
74LS244
74LS04
A5B
RS422CLK A
SIO 1 IEI
SIO CE1
SYS CLK
SIO CE2
SIO 1 IEO
SIO 2 IEO
SIO 2 IEI
SIO 1A RDY
SIO 1B RDY
SIO 2A RDY
SIO 2B RDY
P6 - 1
P6 - 2
P6 - 3
P6 - 4
P6 - 5
P6 - 6
P6 - 7
P6 - 8
P6 - 9
P6 - 10
P6 - 11
P6 - 12
P6 - 13
P6 - 14
P6 - 15
P6 - 16
P6 - 17
P6 - 18
P6 - 19
P6 - 20
+5V
GND
B600008-001
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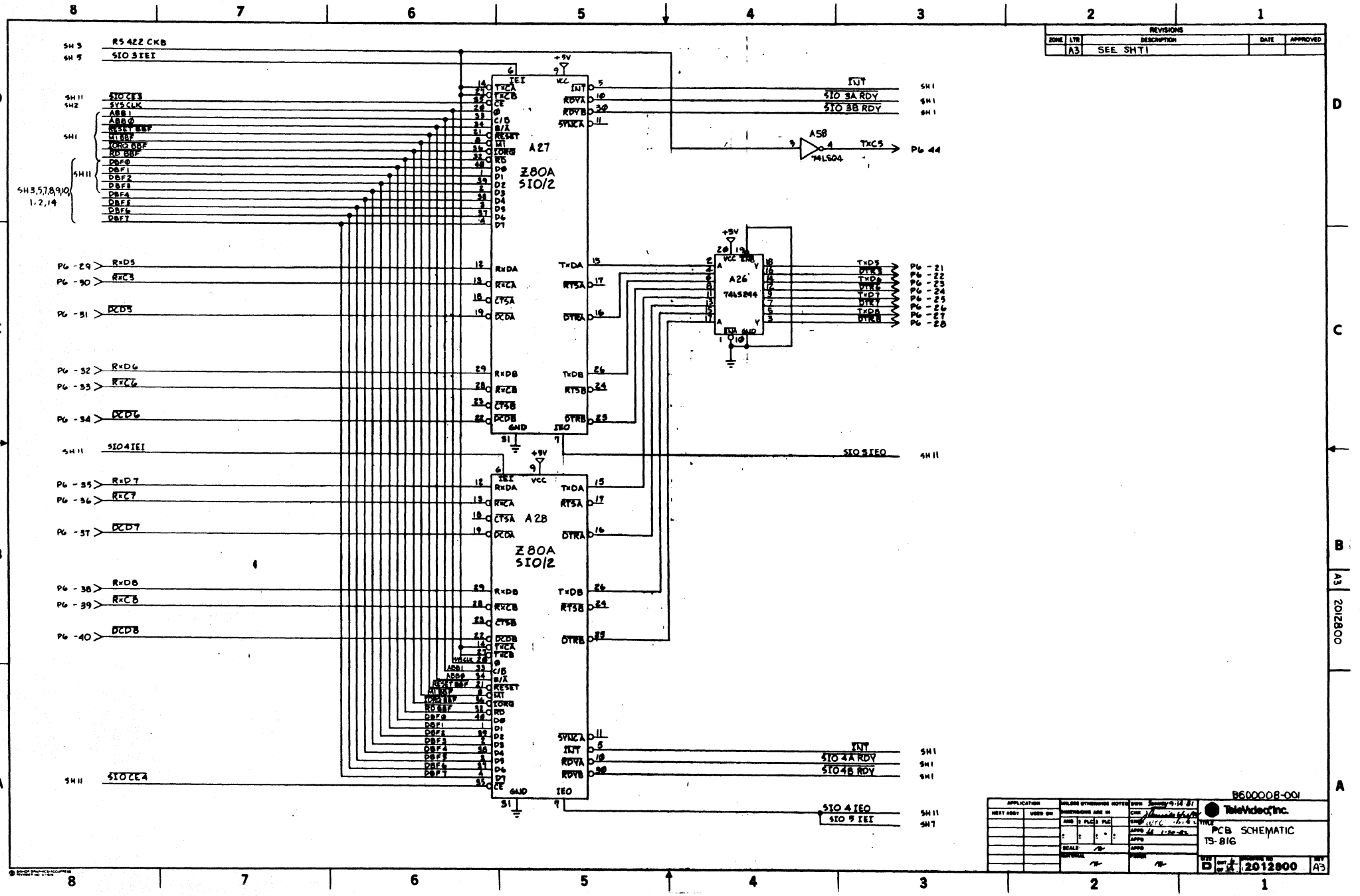
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A3 SEE SHT1
RS422 CKB
SIO 3 IEI
SIOCE3
SYSCLK
ABB1
ABB0
RESET BBF
M1 BBF
IORQ BBF
RD BBF
DBF0
DBF1
DBF2
DBF3
DBF4
DBF5
DBF6
DBF7
SH3,5,7,8,9,10, 1,2,14
A27
Z80A SIO/2
INT
SIO 3A RDY
SIO 3B RDY
A58
74LS04
TXC5
P6 44
A26
74LS244
P6 - 29 RXD5
P6 - 30 RXC5
P6 - 31 DCD5
P6 - 32 RXD6
P6 - 33 RXC6
P6 - 34 DCD6
SIO 4 IEI
SIO 3 IEO
P6 - 35 RXD7
P6 - 36 RXC7
P6 - 37 DCD7
A28
Z80A SIO/2
P6 - 38 RXD8
P6 - 39 RXC8
P6 - 40 DCD8
SIOCE4
SIO 4A RDY
SIO 4B RDY
SIO 4 IEO
SIO 5 IEI
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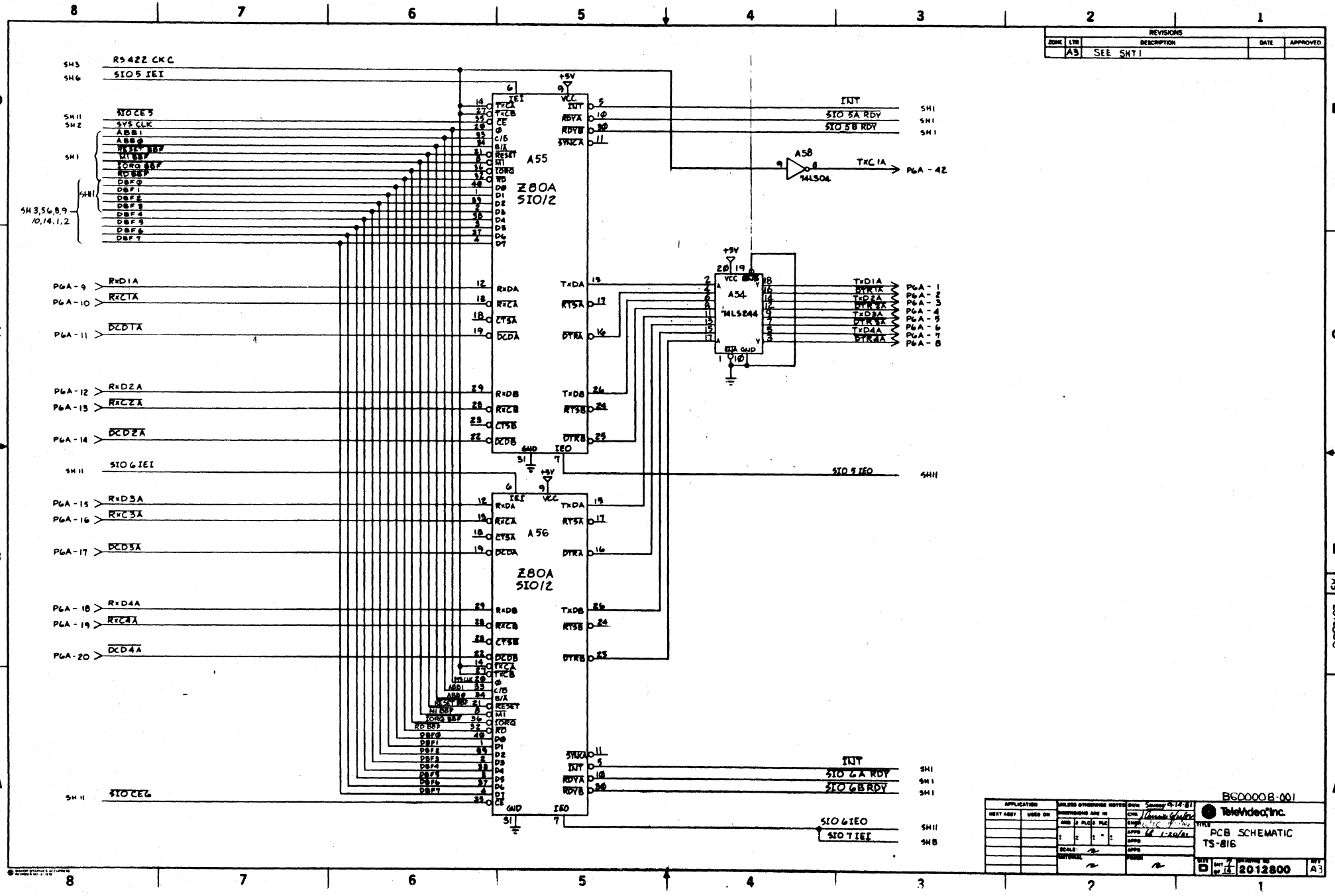
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A3 SEE SHT 1
RS422 CKC
SIO 5 IEI
SIO CE B
SYS CLK
ABB 1
ABB 0
RESET BBF
M1 BBF
IORQ BBF
RD BBF
DBF 0
DBF 1
DBF 2
DBF 3
DBF 4
DBF 5
DBF 6
DBF 7
SH 3,5,6,8,9 10,14,1,2
A55
Z80A SIO/2
A56
Z80A SIO/2
A54
74LS244
A58
74LS04
INT
SIO 5A RDY
SIO 5B RDY
TXC 1A
P6A - 42
SIO 5 IEO
SIO 6A RDY
SIO 6B RDY
SIO 6 IEO
SIO 7 IEI
SIO CE 6
RXD 1A
RXC 1A
DCD 1A
RXD 2A
RXC 2A
DCD 2A
SIO 6 IEI
RXD 3A
RXC 3A
DCD 3A
RXD 4A
RXC 4A
DCD 4A
TXD 1A
DTR 1A
TXD 2A
DTR 2A
TXD 3A
DTR 3A
TXD 4A
DTR 4A
BS00008-001
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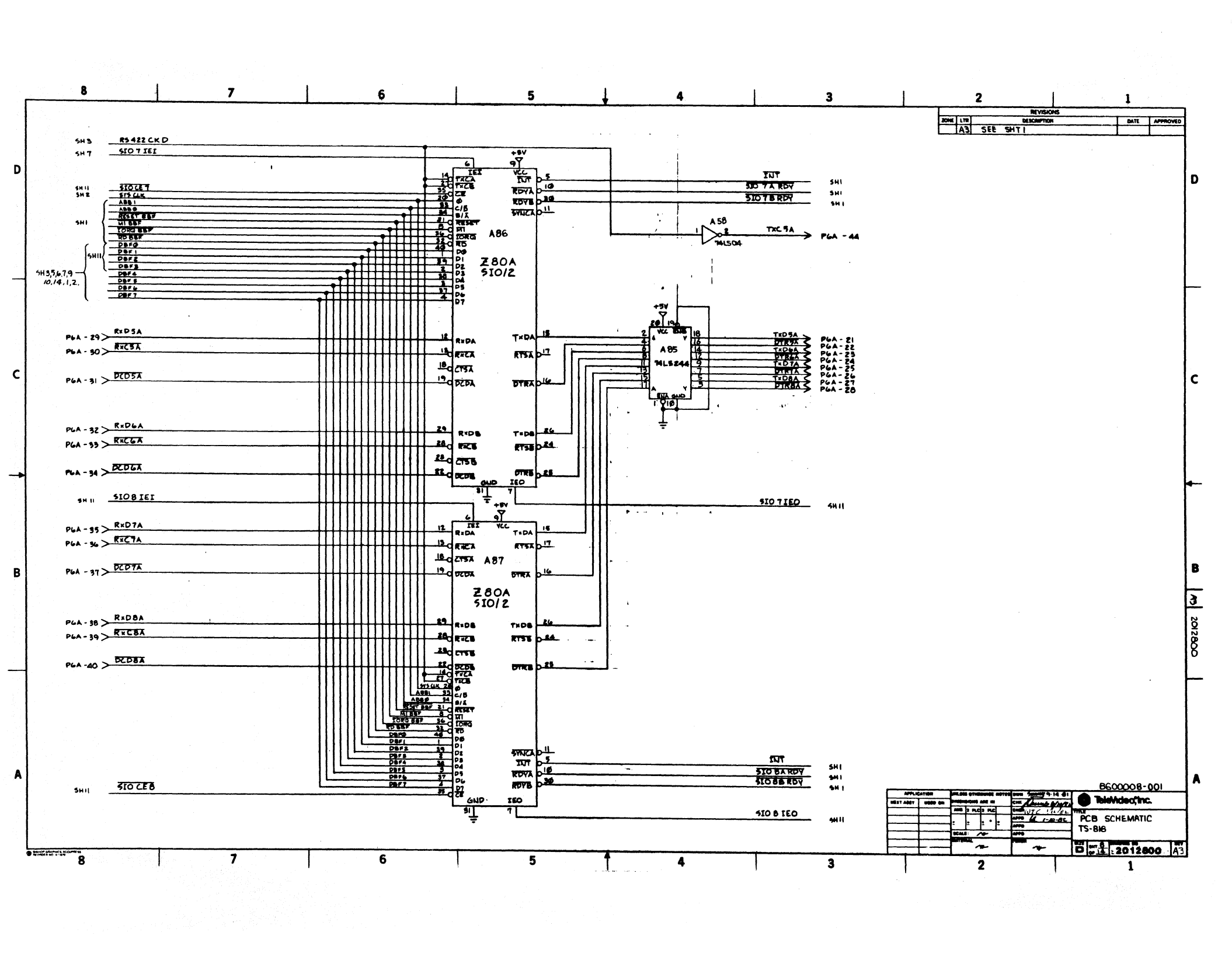
TS-816
2012800
A3


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A3 SEE SHT 1
SH3 RS422 CK D
SH7 SIO 7 IEI
SH11 SIO CE 7
SH2 SYS CLK
SH1 ABB 1
ABB 0
RESET BBF
M1 BBF
IORQ BBF
RD BBF
SH111 DBF 0
DBF 1
DBF 2
DBF 3
SH3,5,6,7,9 10,14,1,2. DBF 4
DBF 5
DBF 6
DBF 7
A86
Z80A SIO/2
A87
Z80A SIO/2
A85
74LS244
A58
74LS04
INT
SIO 7 A RDY
SIO 7 B RDY
TXC 9A
P6A - 44
SIO 7 IEO
SIO 8 A RDY
SIO 8 B RDY
SIO 8 IEO
SIO CE 8
SH11
P6A - 29 RxD 5A
P6A - 30 RxC 5A
P6A - 31 DCD 5A
P6A - 32 RxD 6A
P6A - 33 RxC 6A
P6A - 34 DCD 6A
SH11 SIO 8 IEI
P6A - 35 RxD 7A
P6A - 36 RxC 7A
P6A - 37 DCD 7A
P6A - 38 RxD 8A
P6A - 39 RxC 8A
P6A - 40 DCD 8A
TXD 5A
DTR 5A
TXD 6A
DTR 6A
TXD 7A
DTR 7A
TXD 8A
DTR 8A
P6A - 21
P6A - 22
P6A - 23
P6A - 24
P6A - 25
P6A - 26
P6A - 27
P6A - 28
B600008-001
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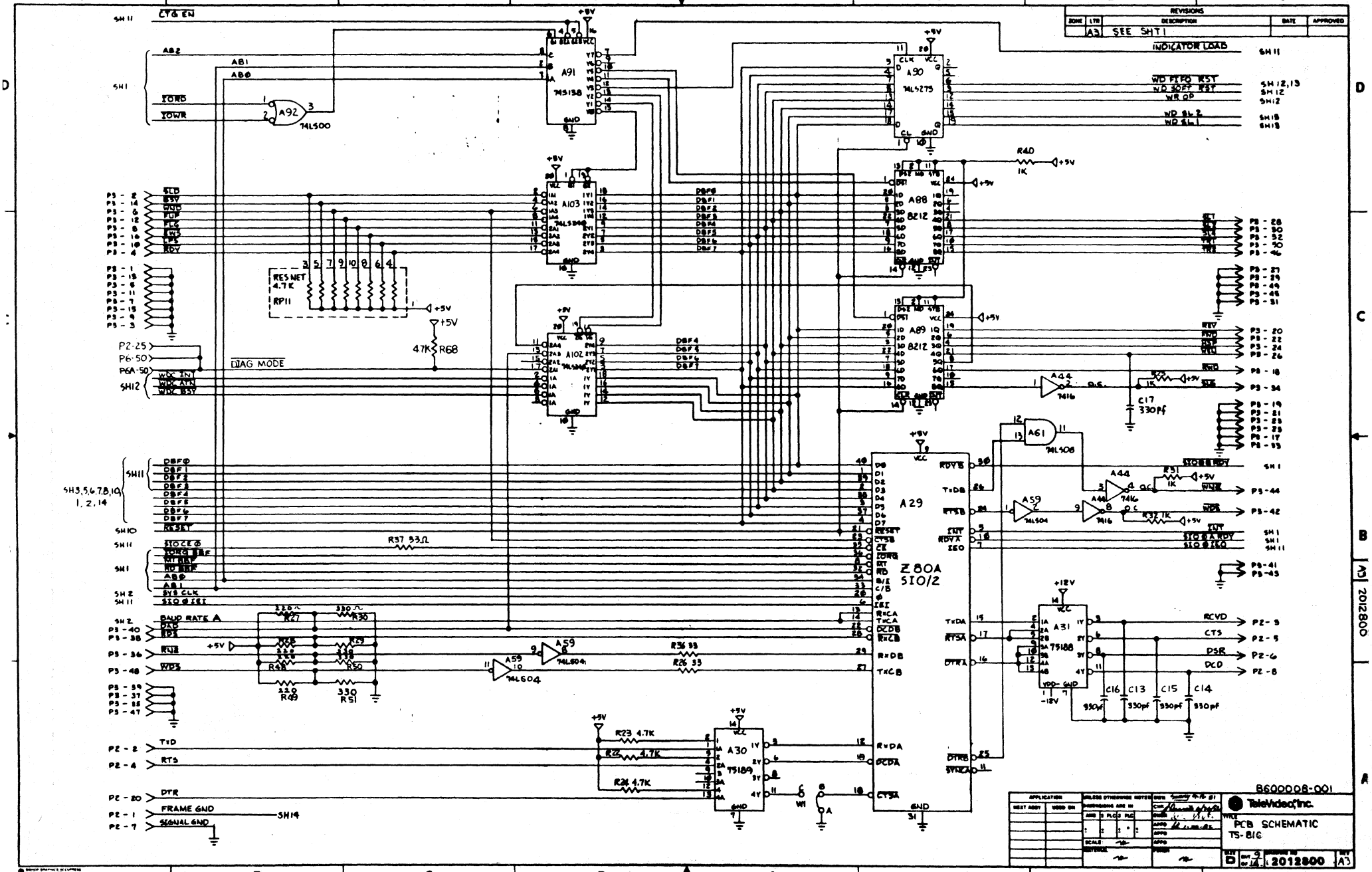
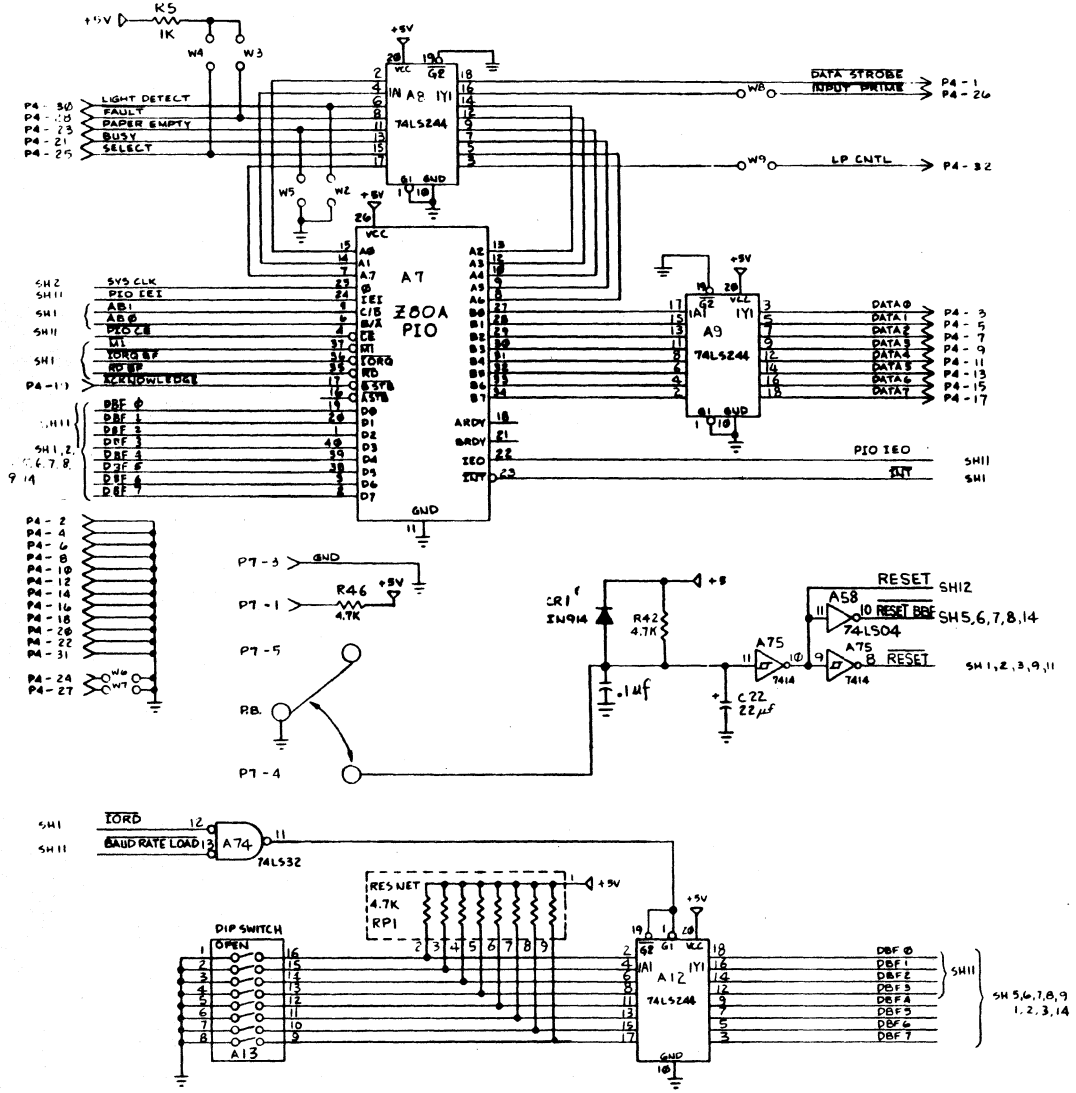
PCB SCHEMATIC
TS-818
2012800
A3


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A3 SEE SHT1
INDICATOR LOAD
WD FIFO RST
WD SOFT RST
WR OP
WD SLV 2
WD SLV 1
A91 74LS138
A90 74LS279
A88 8212
A89 8212
A103 74LS240
A102 74LS240
A29 Z80A SIO/2
A30 75189
A31 75188
A92 74LS00
A59 74LS04
A61 74LS08
A44 7416
RES NET 4.7K RP11
R68 4.7K
R37 33Ω
R40 1K
R31 1K
R32 1K
C17 330pf
C16 330pf
C13 330pf
C15 330pf
C14 330pf
R27 330Ω
R30 330Ω
R48 330Ω
R49 330Ω
R50 330Ω
R51 330Ω
R23 4.7K
R24 4.7K
R25 4.7K
R35 33
R26 33
DIAG MODE
RCVD
CTS
DSR
DCD
TXD
RTS
DTR
FRAME GND
SIGNAL GND
B600008-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-816
2012800
A3



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
A3		SEE SHT 1		

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN			DWN		TeleVideo, Inc.
NEXT ASSY	USED ON	ANG	2 PLC	3 PLC	CHK		
					ENGR		TITLE: PCB SCHEMATIC TS-816
		SCALE			APPD		
		MATERIAL			APPD		
					APPD		
					FINISH		

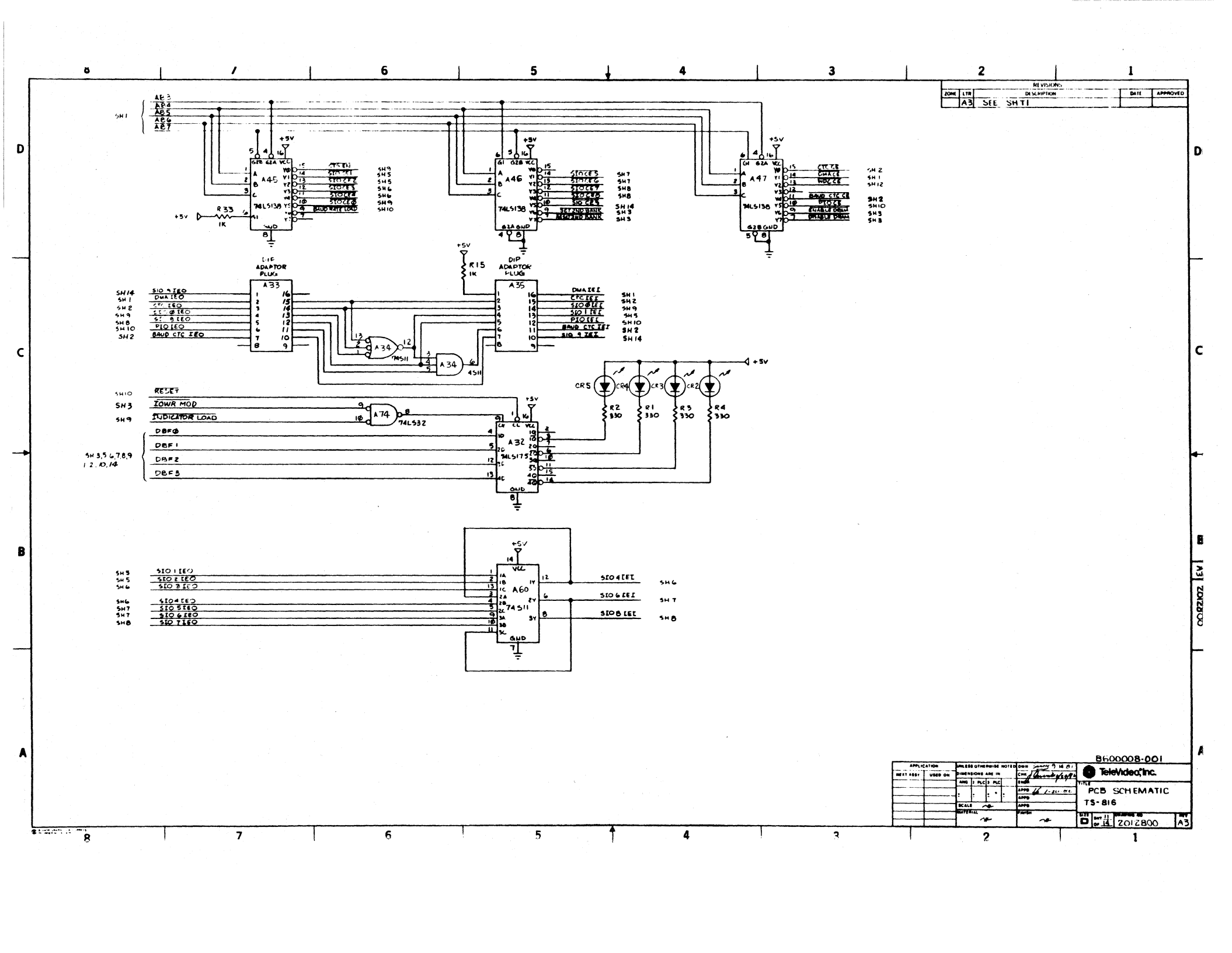
B800008-001

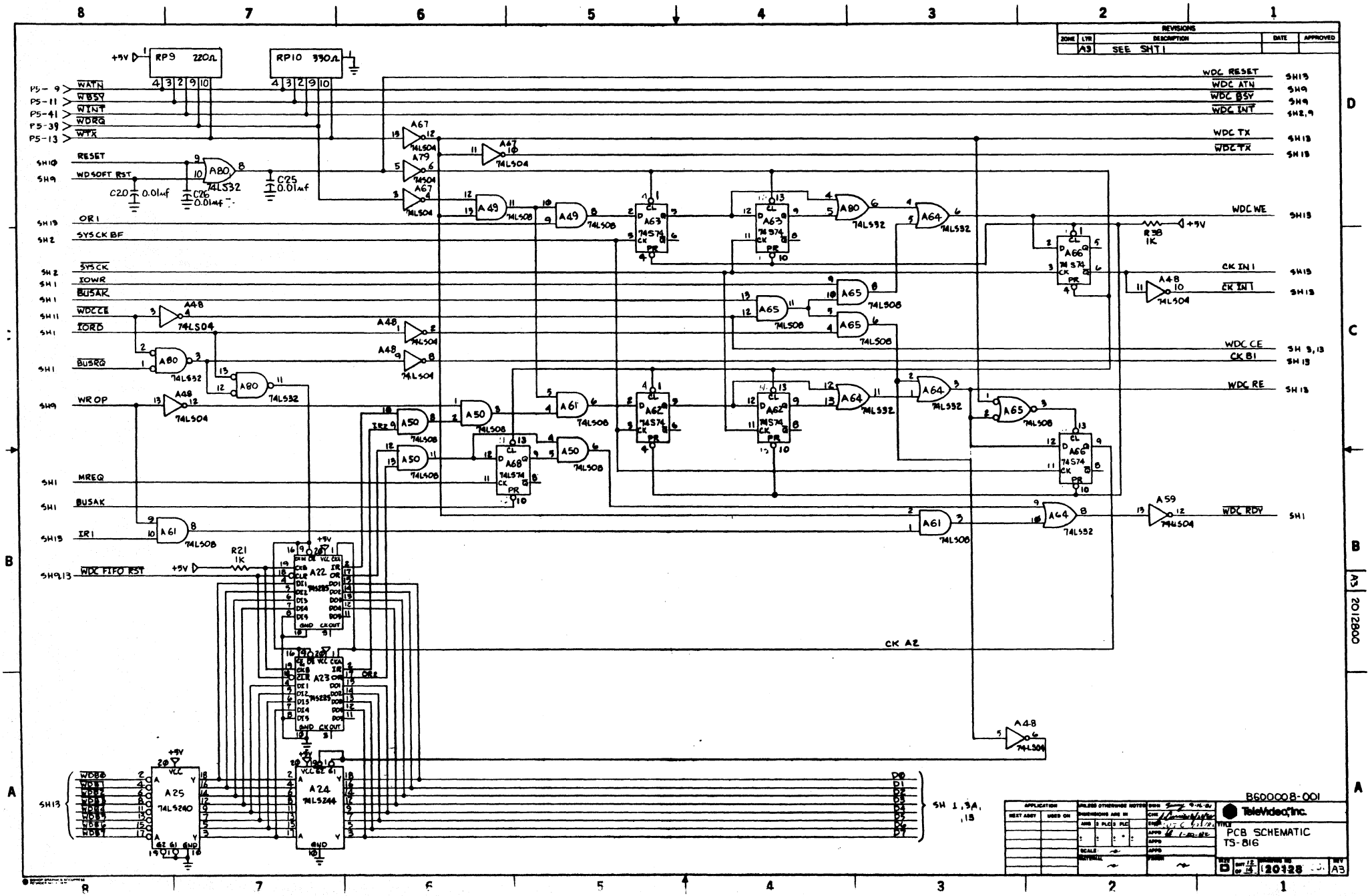
SIZE	DWG NO	REV
D	2012800	A2

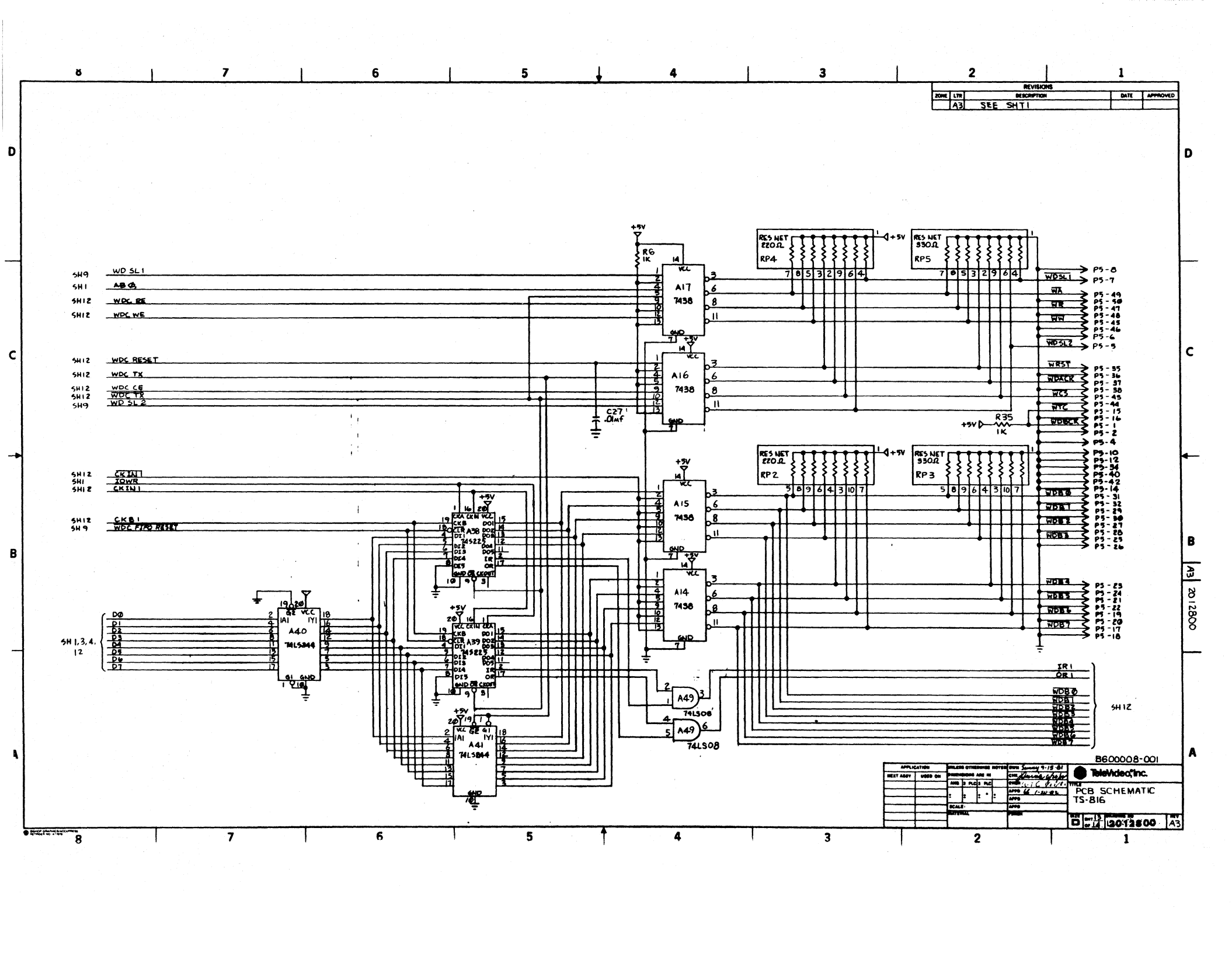
SHT 10 OF 14

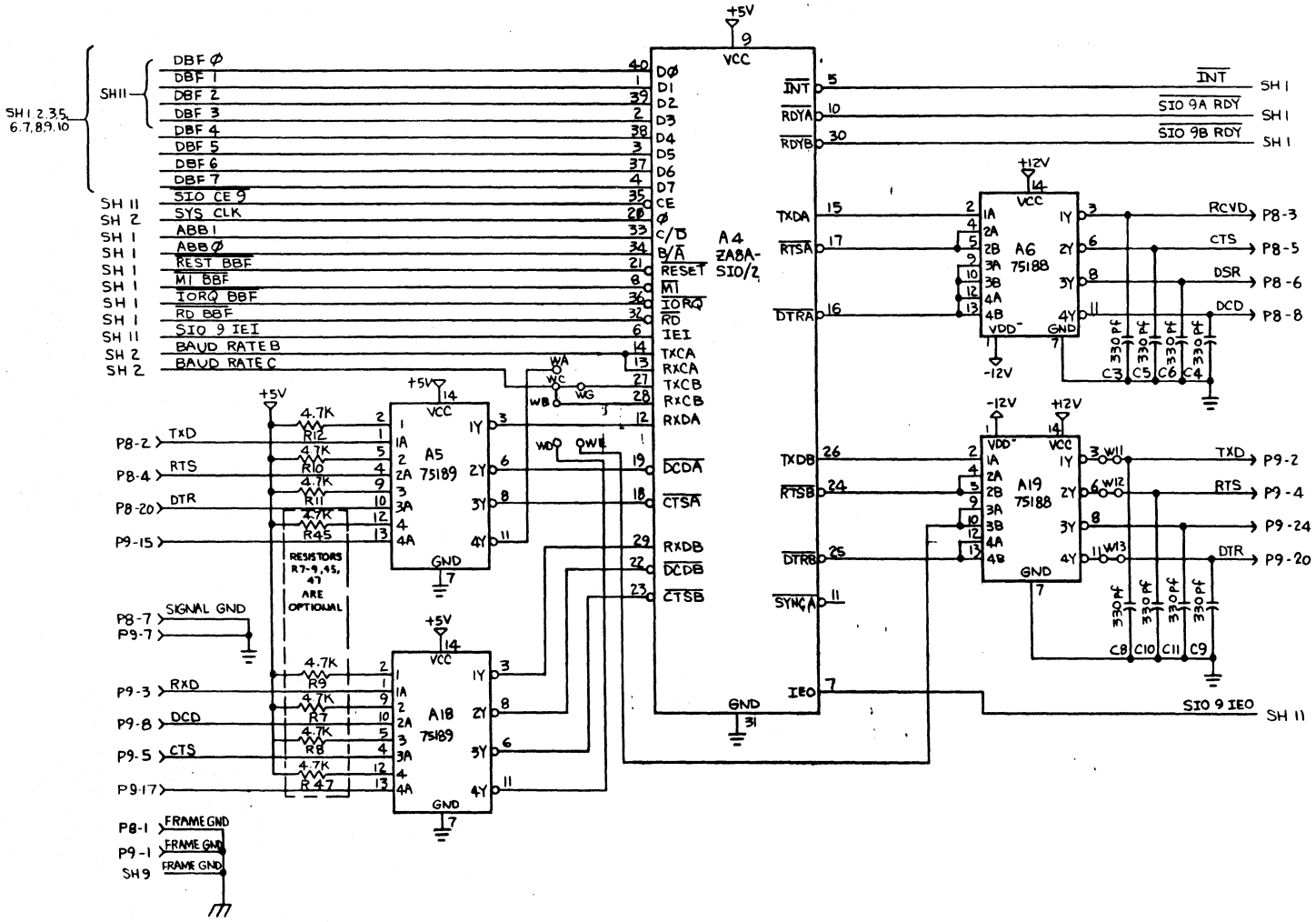
2012800

A3


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A3 SEE SH T1
A45
A46
A47
74LS138
A33
A35
A34
74S11
A74
74LS32
A32
74LS175
A60
74S11
R33 1K
R15 1K
R1 330
R2 330
R3 330
R4 330
CR1 CR2 CR3 CR4
+5V
RESET
IOWR MOD
INDICATOR LOAD
DBF0
DBF1
DBF2
DBF3
B600008-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-816
SIZE D
DRAWING NO 2012800
REV A3


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A3 SEE SHT 1
RP9 220Ω
RP10 330Ω
+5V
P5-9 WATN
P5-11 WBSY
P5-41 WINT
P5-39 WDRQ
P5-13 WTX
SH10 RESET
SH9 WDSOFT RST
C25 0.01mf
C26 0.01mf
C20 0.01mf
A80 74LS32
SH13 OR1
SH2 SYSCK BF
SH2 SYSCK
SH1 IOWR
SH1 BUSAK
SH11 WDCCE
SH1 IORD
SH1 BUSRQ
SH9 WR OP
SH1 MREQ
SH1 BUSAK
SH13 IR1
SH9,13 WDC FIFO RST
R21 1K
A22 A23 A24 A25 74LS240 74LS244 74LS245
SH13 WDB0 WDB1 WDB2 WDB3 WDB4 WDB5 WDB6 WDB7
SH 1,3A, ,13 D0 D1 D2 D3 D4 D5 D6 D7
WDC RESET SH13
WDC ATN SH9
WDC BSY SH9
WDC INT SH2,9
WDC TX SH13
WDC TX SH13
WDC WE SH13
R38 1K
CK IN1 SH13
CK IN1 SH13
WDC CE SH 3,13
CK B1 SH13
WDC RE SH13
WDC RDY SH1
CK A2
A59 74LS04
A48 74LS04
A49 74LS08
A50 74LS08
A61 74LS08
A64 74LS32
A65 74LS08
A66 74S74
A67 74LS04
A68 74S74
A62 74S74
A63 74S74
B600008-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-816
D 20128 A3
A3 20128-00


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A3 SEE SHT1
SH9 WD SL1
SH1 ABØ
SH12 WDC RE
SH12 WDC WE
SH12 WDC RESET
SH12 WDC TX
SH12 WDC CE
SH12 WDC TX
SH9 WD SL2
SH12 CKIN1
SH1 IOWR
SH12 CKIN1
SH12 CKB1
SH9 WDC FIFO RESET
SH 1,3,4, 12
D0 D1 D2 D3 D4 D5 D6 D7
A40 74LS244
A39 74S225
A41 74LS244
A17 7438
A16 7438
A15 7438
A14 7438
A49 74LS08
A49 74LS08
C27 .01mf
R6 1K
R35 1K
+5V
RES NET 220Ω RP4
RES NET 330Ω RP5
RES NET 220Ω RP2
RES NET 330Ω RP3
WDSL1
WA
WB
WN
WDSL2
WRST
WDACK
WCS
WYC
WDBCK
WDB0
WDB1
WDB2
WDB3
WDB4
WDB5
WDB6
WDB7
P5-8
P5-7
P5-49
P5-50
P5-47
P5-48
P5-45
P5-46
P5-6
P5-5
P5-35
P5-36
P5-37
P5-38
P5-43
P5-44
P5-13
P5-16
P5-1
P5-2
P5-4
P5-10
P5-12
P5-34
P5-40
P5-42
P5-14
P5-31
P5-32
P5-29
P5-30
P5-27
P5-28
P5-25
P5-26
P5-23
P5-24
P5-21
P5-22
P5-19
P5-20
P5-17
P5-18
IR1
OR1
WDB0
WDB1
WDB2
WDB3
WDB4
WDB5
WDB6
WDB7
SH12
B600008-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-816
SIZE D SHT 13 OF 14 DRAWING NO 2012800 REV A3
2012800
A3



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A3	SEE SHT 1		

B600008-001

TeleVideo, Inc.

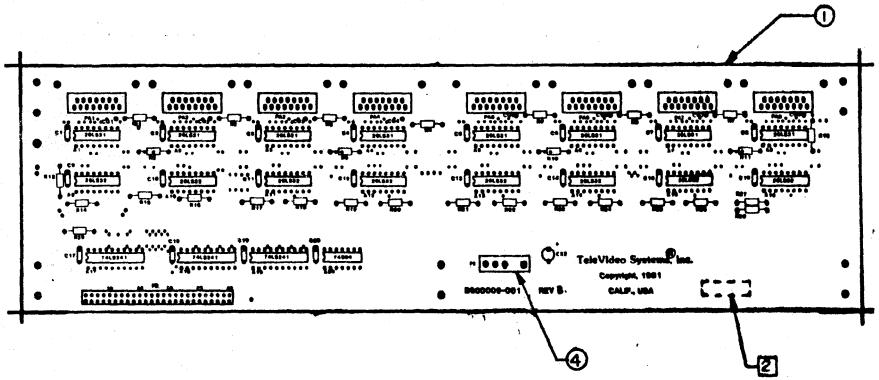
PCB SCHEMATIC
TS-816

2012800 A3

B900009-001

PART NUMBER	DESCRIPTION/TITLE	LOCATIONS REV A1
2028700	CAP. .01uf 10%	C1-20
2026100	CAP. 22uf 50V	C21
2042400	IC 26LS31	A1-8
2042600	IC 26LS32	A9-16
2042000	IC 74LS241	A17-19
2024600	IC 74S04	A20
2098700	CONN. 5 PIN (MOLEX) R/A	PD
2098000	CONN. 15 PIN D-SUB	PA1-8
2174401	CONN. HEADER 50 PIN	PB
2052100	RES. 1K 5% 1/4W	R8-11,29
2034900	RES. 100 ohm 1% 1/4W	R1-7,12-28

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	PROD REL PER ECO 0491	10/6/82	
	C	REVISED AS PER ECO 0541	10/18/82	

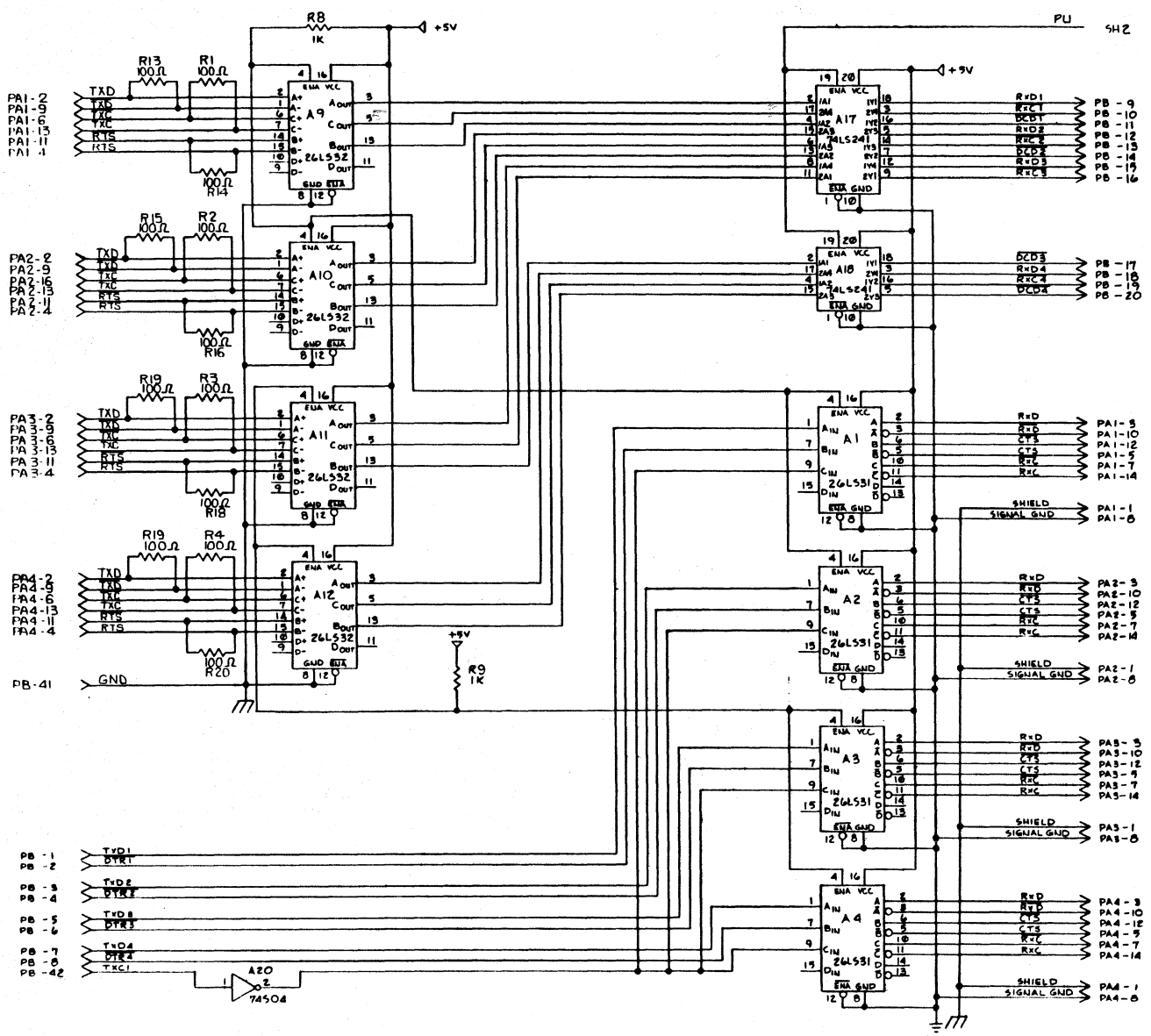


NOTE: UNLESS OTHERWISE SPECIFIED

1. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
2. SILKSCREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK 50-100R APPROXIMATELY WHERE SHOWN.
3. MADE FROM 2013100 FAB REV B.
4. PE MOLEX CONN. R/A.

TeleVideo, Inc.			
TITLE: PCB ASSY DWG TS-816 U			
SIZE: D	SHT OF:	DRAWING NO: 2013400	REV: C

2013400 C



NOTE:

DESIGNATIONS FOR SISTER BOARD PARENTHESIZED.

PA1-15 (TP)
PA2-15 (TP)
PA3-15 (TP)
PA4-15 (TP)
PA5-15 (TP)
PA6-15 (TP)
PA7-15 (TP)
PA8-15 (TP)

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 174	1-20-81	
	B	" " ECO 0491		

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN Sammy S 9 81
NEXT ASSY	USED ON		CHK
			ENGR
			APPD
			APPD
			APPD
		SCALE NONE	FINISH
		MATERIAL	

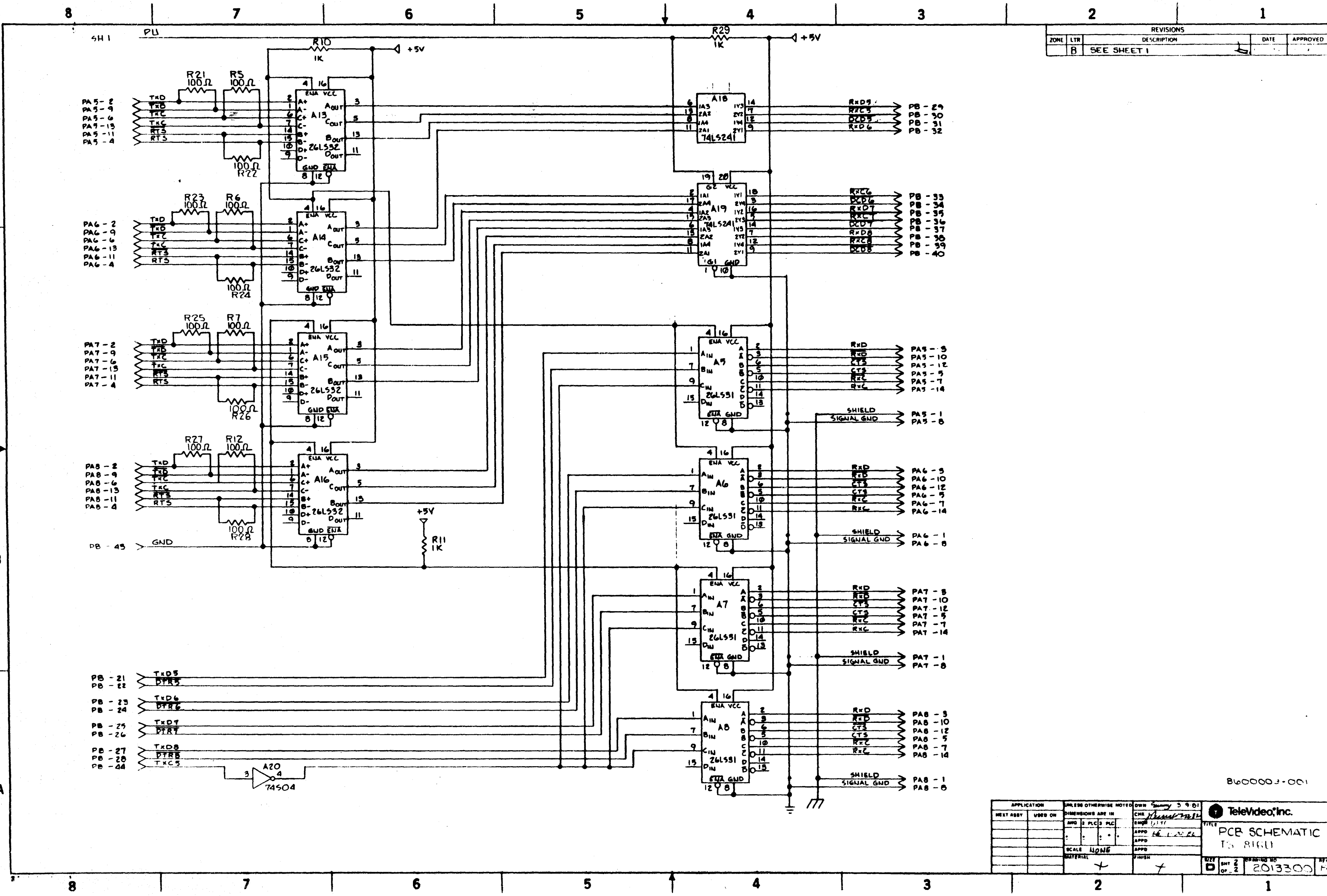
TeleVideo, Inc.

TITLE: PCB SCHEMATIC TS-816D

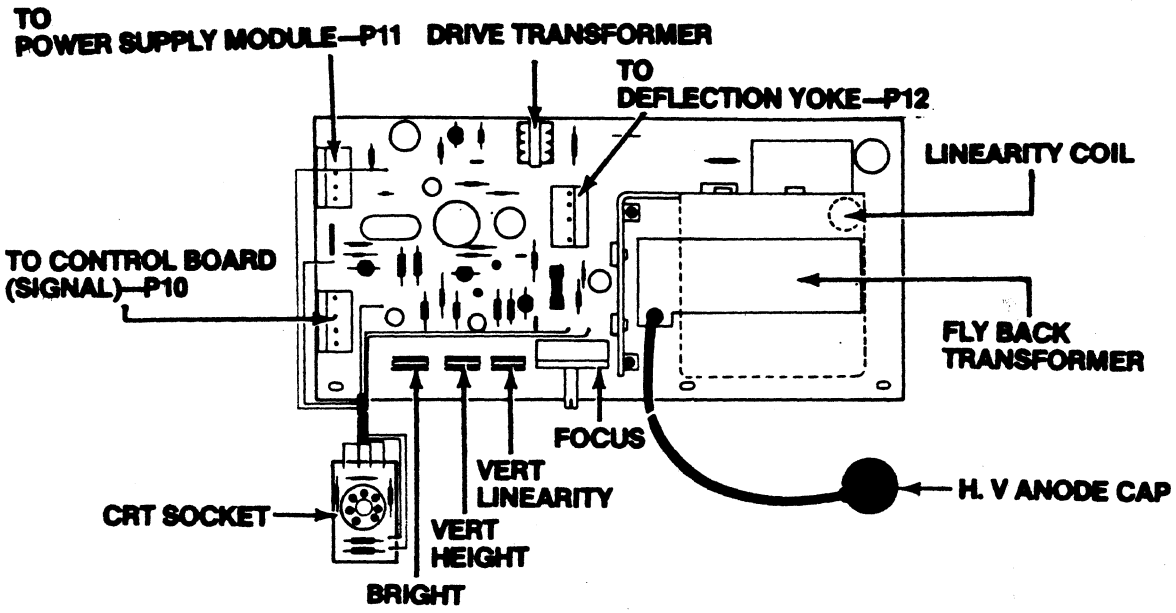
SIZE D | SHT 1 OF 2 | DRAWING NO 2013300 | REV B

B600009-001

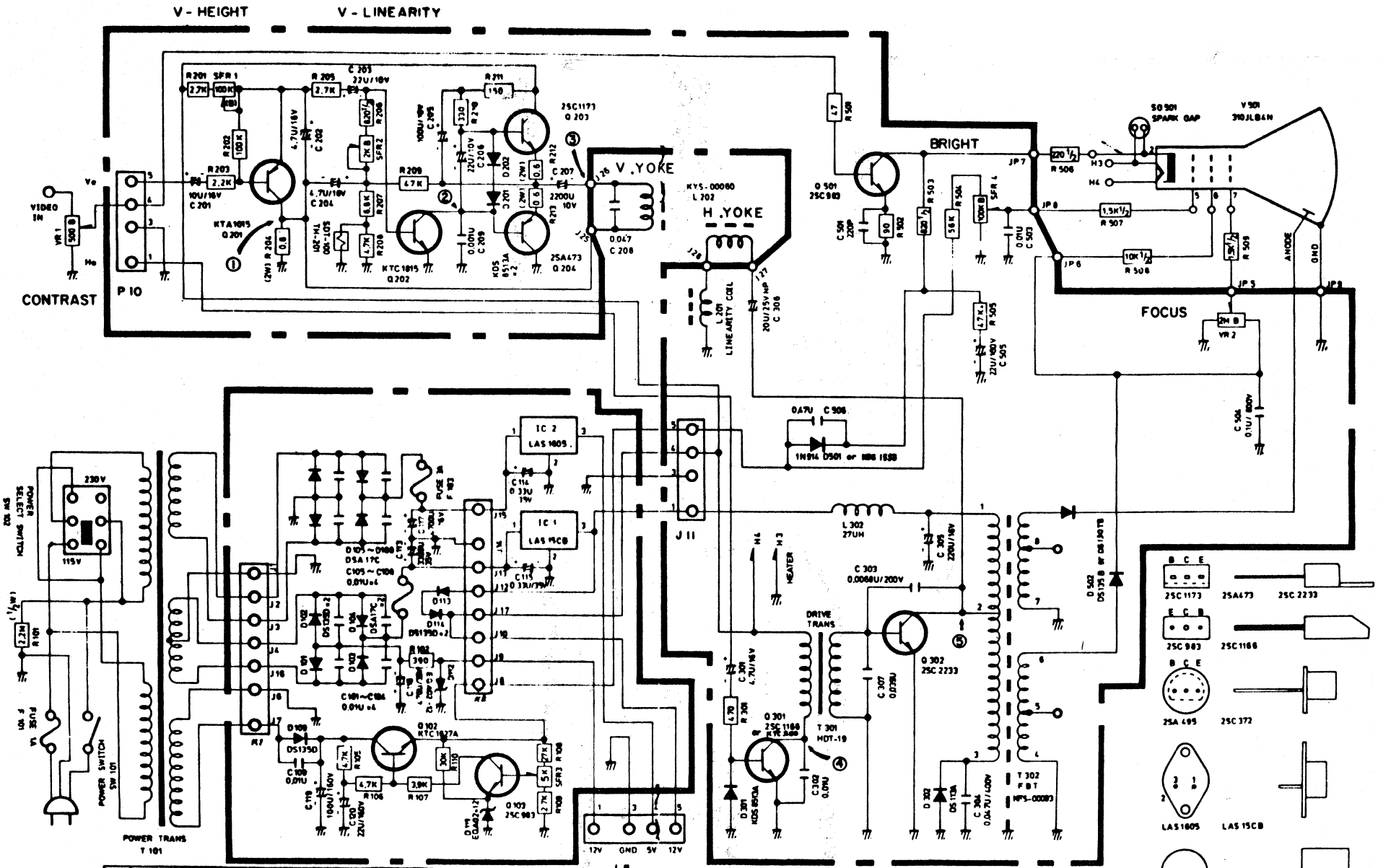
2013300



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B SEE SHEET 1
SH 1 PU
R10 1K +5V
R29 1K +5V
A13 26LS32
A14 26LS32
A15 26LS32
A16 26LS32
A18 74LS241
A19 74LS241
A5 26LS51
A6 26LS51
A7 26LS51
A8 26LS51
A20 74S04
R11 1K
PB - 45 GND
SHIELD
SIGNAL GND
B600003-001
TeleVideo, Inc.
PCB SCHEMATIC
TS 816H
SCALE NONE
DRAWING NO 2013300
SHT 2 OF 2



MONITOR BOARD



1	Vp-p 0.7	2	Vp-p 6.5	3	Vp-p 6.5	4	Vp-p 20	5	Vp-p 124

1. All resistance values in OHM K=1,000 M=1,000,000.
2. All capacitor values in FARAD U=10^{6} P=10^{12}.
3. Unless otherwise stated, working voltages of capacitors are 50 volts.
4. This schematic diagram covers basic or representative chassis only. There may be some component or partial schematic difference between actual chassis and the schematic diagram.

Part Number	Description	Locations REV A			
BC01643	CRT MODULE (VIDEO MODULE)				
TRANSISTORS					
S350100-006	KTC 1815/2N3904	Q202			
S350100-007	KTC 1627A	Q102			
S350100-009	2CS 983/2N5551/KTC 2229	Q103, Q501			
S350100-010	2SC 2233/MJE13006	Q302			
ST-10351	KTA 1015/2N3906	Q201			
ST-01353	2SC1/173/2N6121	Q203			
ST-01354	2SA473/2N6123	Q204			
ST-01361	KTC 200 (2SC1166)/2N4401	Q301			
CRT AND DIODE					
S360100-000	IN914/KDS 1553	D501			
SD-01251	DS135D/IN5391	D101, D102, D109, D113			
		D114			
SD-01252	DSA175C/IN5391	D103, D104			
SD-01253	DSA17C/MR500	D105, D106 D107, D108			

Part Number	Description	Locations REV A			
SD-01254	EQA01-12/IN759A	D111, D112			
SD-01255	DS-113A/MRI-1000	D302			
SD-01257	D130TB/IN4004	D502			
SD-01258	KDS-8513A/IN920	D201, D202			
		D301			
T300002-001	310JLB4 (N)	V501			
COIL AND TRAN					
IC-01365	CRT 858 (EI-858)	T101			
IC-01462	5.4 UH	L201			
IC-01464	27 UH	L302			
IC-01466	HDT-19	T301			
IC-01467	KFS-00093	T302			
IS-01461	KYS-00060	L202			
RESISTORS					
331243	SDT-100 THERMISTER	TH201			
R514000-004	470 OHMS, ¼W	R301			
R514000-011	4.7K OHMS ¼W	R105,106,208			

Part Number	Description	Locations REV A			
R514003-001	220 OHMS ½W	R506			
R514003-002	390 OHMS ½W	R102			
R514003-003	820 OHMS ½W	R206,503,210			
R514003-006	2.2 M ½W	R101			
R514000-017	100K OHMS, ¼W	R202			
R514000-025	47K OHMS, ¼W	R209,505			
R514000-026	150 OHMS, ¼W	R211			
R514000-043	27K OHMS, ¼W	R108			
R514000-045	47 OHMS ¼W	R501			
R514000-048	2.7K OHMS ¼W	R109,201,205			
R514000-049	90 OHMS ¼W	R502			
R514000-050	2.2K OHMS ¼W	R203			
R514000-051	3.9K OHMS ¼W	R107			
R514000-052	6.8K OHMS ¼W	R207			
R514000-053	30K OHMS ¼W	R110			
R514003-054	56K OHMS ¼W	R504			
RC02608J	0.6 OHMS 2W	R204,212,213			

Part Number	Description	Locations			
R514003-004	1.5K OHMS ½W	R507,509			
R514003-005	10K OHMS ½W	R508			
RF-07104B	EVL SOAA00B15 100K OHM POT	HEIGHT BRIGHT SFR1, SFR4			
RF-07202B	EVL SOAA00B23 sK OHM POT	SFR2 LINEARITY			
RF-07473B	EVL SOAA00B53 5K OHM POT	SFR3 75V REG.			
RV-24205B	EVL 26AS10B26 2M OHM POT	VR2 FOCUS			
RV-24501B	EVL GOAF20B52 500 OHM POT	VR1 CONTRAST			
CAPACITORS					
C700100-001	22 uf 16V	C203, 206			
C700100-010	10 uf 16V	C201			
C700100-011	4.7 uf 16V	C202, 204			
C900100-002	0.01 uf 50V	C101,102,103 104,105,106, 107,108,109, 503			
C900100-012	1KV SPARKGAP	S501			
CC-50221SL	220 uf 50V	C501			
CE-101075	100 uf 10V	C205			
CE-10226SH	22 uf 100V	C505			

Part Number	Description	Locations REV A			
CE-1607SH	100 uf 160V	C119			
CE16227S	220 uf 16V	C305			
CE-10228S	2200 uf 10V	C207			
CE-16226 SH	22 uf 160V	C120			
CE-35338S	300 uf 35V	C113			
CE-35478S	4700 uf 16V	C117			
CM 16475S	4.7 uf 16V	C301			
CM 20682H	0.0068 uf 200V	C303			
CM 50102	0.001 uf 50V	C209			
CM 50103	0.01 uf 50V	C302			
CM 50473	0.047 uf 50V	C208			
CM 50474	0.47 uf 50V	C506			
CM-60104	0.1 uf 600V	C504			
CN-15206S	20 uf 25V	C306			
CO-40473H	0.047 uf 400V	C304			
CT-35334	0.33 uf 35V	C114, C115			
CT-35338S	470 uf 35V	C116			

Part Number	Description	Locations REV A			
SWITCHES					
M200107-001	SPST 115V 10A/230V 5A	SW101			
M200108-001	DPDT 115V/230V	SW102			