TYPE RB GENERAL PURPOSE CORE MEMORIES

In addition to TYPE RB memories, Telemeter Magnetics manufactures a wide range of solid state core memories having cycle times from 24 to 1 microsecond in capacities up to a million bits or more. For buffer storage applications, TMI offers more than 40 models to choose from. The Components Division can deliver from stock a variety of ferrite storage and logic cores, arrays, and memory stacks.

Offering a combination of features not previously considered feasible in any but custom units, TYPE RB core memories incorporate such useful characteristics as high speed operation... long term reliability...wide range of capacities...low cost... random access, sequential load, sequential unload, or any combination desired.

CHARACTERISTICS

CAPACITY

128 to 1024 words
4 to 24 bits per word
Larger capacities by multiple units

OPERATING MODES

Sequential load and unload
Random access load and unload
Random access or sequential access memory with clear/write and read/restore cycles.
Operations can be intermixed in any manner desired without loss of speed.

SPEED

Load or unload a word (all bits in parallel) – 5 microseconds
Complete memory cycle – 8 microseconds

INPUT AND OUTPUT SIGNALS

A wide range of reference levels and signal amplitudes is available to assure compatibility with both tube and transistor circuits. Input signals may be either polarity and may be levels or pulses. Output signals are levels.

DIMENSIONS

Depends on word length. Up to 12 bits per word – 19 x 10½ x 16; 14 to 24 bits – 19 x 15½ x 16.

POWER SUPPLY

Self-contained – requires 115 volts, 48-63 cps, less than 250 watts.

ENVIRONMENT

Operates over the temperature range from 0°C to 70°C under humidity conditions to 90%.

TYPICAL APPLICATIONS FOR TYPE RB GENERAL PURPOSE CORE MEMORIES

TYPE RB Memories were designed for use in data systems requiring relatively small, fast memories compatible with logical control in 100-200 kc region. These versatile units are applicable to systems designed for

- ★ automatic control
- ★ data editing and format revision
- ★ multiplexing data from several sources
- ★ analog-to-digital conversion and data recording
- ★ small digital computers
- ★ complex data processing
- ★ automatic checkout programming
- ★ process control
- ★ machine tool control
- ★ weapons fire control
- ★ digital data communication
- ★ meteor burst data transmission
- ★ nuclear energy analysis and instrumentation
- ★ pulse height analysis

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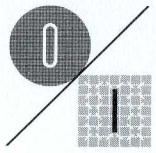
Pioneers in Development and Manufacture of Core Memory Products



Specification DF-115.1

SPECIFICATIONS
FOR TYPE RB GENERAL PURPOSE CORE MEMORIES

STORAGE CAPACITY
128 to 1024 words per unit
4 to 24 bits per word in two-bit increments
Larger capacities by combining units

OPERATING SPEED
Asynchronous to 200 kc loading or unloading for buffer operation; to 125 kc for read/restore or clear/write memory cycles.

ENVIRONMENT
Operating ambient temperature – 0°C to 50°C. Will withstand occasional excursions to 70°C. Storage conditions – from –20°C to 70°C. Relative humidity – 0% to 90%.

All materials used are non-nutrient to fungi and are protected against corrosion. Moderate vibration or shock will not affect operation.

POWER REQUIREMENTS
Self-contained power supply, incorporating regulation for all output voltages, operates from 100 to 130 volts, single phase 48 – 63 cps, less than 250 watts.

MOUNTING
Designed for mounting in a standard 19-inch relay rack. Supplied with Western Electric notching except on special order. Panel height – 10½ inches for all models up to 12-bit word length; 15¾ inches for 14 to 24-bit models.

FINISH
Supplied painted semigloss gray baked enamel, Federal Standard No. 595, Code 26231. Other panel finishes available on special order.

WEIGHT
From 40 to 85 lb net and from 60 to 120 lb shipping.

INPUT AND OUTPUT SIGNALS
A selection of input and output levels is offered to provide compatibility with other equipment. The input voltage level range is established by the output levels chosen, as shown by the table.

Output*		Input Excursion Limits #		Memory Reference
		Minimum	Maximum	
0	–6	–2 to –4	+2 to –8	–3
+6	0	+4 to +2	+8 to –2	+3
0	–12	–4 to –8	+2 to –14	–6
+6	–6	+2 to –2	+8 to –8	0
+12	0	+8 to +4	+14 to –2	+6

\# These limits are absolute values.

* Output voltages are nominal. The following design tolerances should be applied.

Nominal	Tolerance
0	–0.2 to –0.4
±6	+0.1 to –0.7
+12	+0.4 to –1.0
–12	+1.0 to –1.0

Output current available in either direction from any level is at least 5 ma. Rise or fall time depends on loading and can vary from 0.05 to 0.3 microsecond under normal load variations.

ADDRESS REGISTER
The address register consists of 7 to 10 bits according to number of words capacity.

MEMORY REGISTER
The length of the memory register is determined by the word length chosen. It varies in two-bit increments from 4 to 24 bits.

COUNT NETWORK
Optionally available for sequential addressing to a maximum of 1024 words in binary or 400 words BCD.

TRANSPOSE REGISTER
A register of the same length as the address register may be incorporated to permit storage of a previous address during either a sequential or a random operation.

SIGNAL LINES
There is one wire for each of the following except as indicated.

1. AR – address input and output (4 wires per bit)
2. MR – info input and output (4 wires per bit)
3. LS – load sync
4. ULS – unload sync
5. MR clear – memory register clear
6. AR clear – address register clear
7. OS – operating state (2 wires)
8. CLEAR – buffer clear
9. MO – memory operation
- *10. AR strobe – address register
- *11. MR strobe – memory register

* Used only in models with d-c information levels to AR and MR.

The following input signal lines of one wire each are available when a count network or transpose register is used.

12. F – forward
13. R – reverse
14. C – count
15. T – transpose

INPUT POLARITY AND IMPEDANCE
The d-c currents on each line at the input voltage which corresponds to nominal ouput voltage are

Positive pulses or double-ended levels – 4 ma

Negative pulses or double-ended levels – 1 ma

Positive or negative-going single-ended level – 5 ma

When the input voltage is positive with respect to the memory reference potential, input d-c current is zero. At other input voltages, current is from a more positive potential into the input line. In addition to the d-c current, the unit presents a capacitive input load of 0.0002 microfarad.

INPUT POLARITY SELECTION
Positive or negative-going pulses may be used for any of the following pairs of functions –

1. Load Sync and Unload Sync
2. AR Strobe and AR Clear
3. Info Strobe and MR Clear
4. Count and Transpose

Positive or negative levels may be used for –

Forward and Reverse

Positive level and positive pulse or negative level and negative pulse may be used for –

Memory Operation and Clear

Positive pulse, negative pulse, double-ended level, or single ended level may be used for –

Memory Register and Address Register

OPERATION

TYPE RB general purpose memories offer several operating modes to provide unprecedented versatility and flexibility. These units may be operated as random access memories, sequential access buffers, or any combination of both.

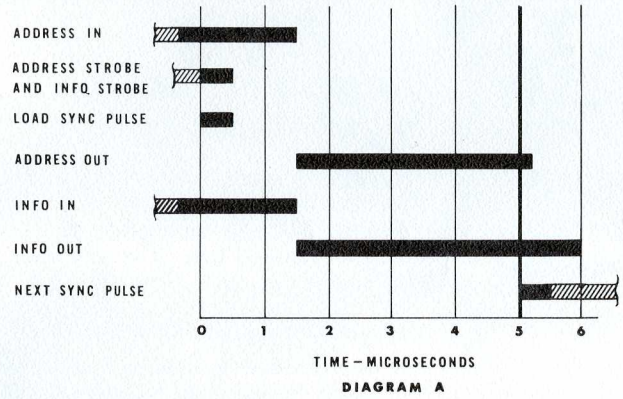


DIAGRAM A

WRITE OPERATION (Loading)

As shown by Diagram A, writing in the memory in the random access mode occurs upon receipt of address signals, the address and information strobe signals, a load sync signal, and the information levels. The operation may be repeated every 5 microseconds. To write in the sequential mode, a count or transpose signal is transmitted instead of the address and address strobe signals. The address register is then increased or decreased by one according to the control information. Note that the loaded information is available within about 1.5 microseconds for external checking or control purposes.

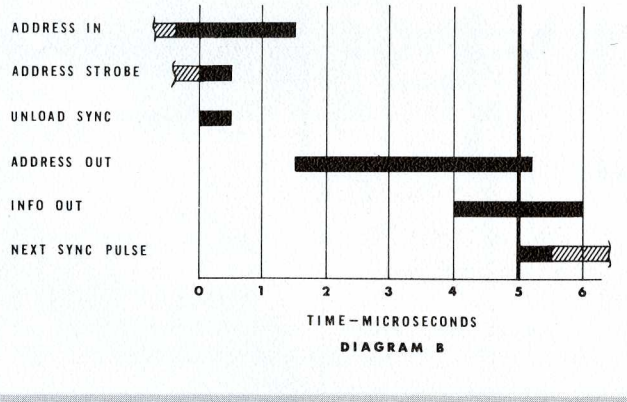


DIAGRAM B

READ OPERATION (Unloading)

Diagram B shows the reading operation, which is similar to writing except that no information is loaded into the unit. Note that unloading is a destructive readout which leaves the storage address in the proper state for a subsequent load operation.

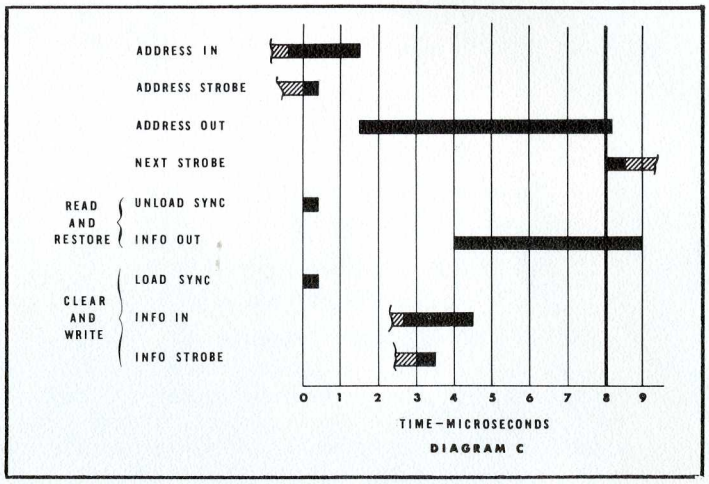


DIAGRAM C

MEMORY OPERATION

Diagram C illustrates memory operation. A clear/write cycle is initiated by a load sync signal with the memory operation line energized. A read/restore cycle is initiated by an unload sync signal with the memory operation line energized.

COUNT OPERATION

An optional count network may be included with forward or reverse counting selected by one of two d-c signals. Utilizing a logical half-adder, the counter prepares the next value during the current cycle and transmits this value to the address register upon receipt of a count signal.

The count network can be set to count in any radix from 1 to 16 to the limit of the memory capacity in number of words. The count network is organized in four-bit modules, normally set to binary but may be set to BCD. The network can be set to count as $R_1 x R_2 x R_3$, where R_1 and R_2 are 16 or less except in 128-word models when R_2 is 8. R_3 is 2 in 512-word models and 4 in 1024-word models.

TRANSPOSE OPERATION

Upon receipt of a transpose signal, the value in the address register is transferred via the count network to the transpose register; simultaneously the value from the transpose register is transferred to the address register. Thus, the values in the transpose and the address registers are exchanged, and the address register value is increased or decreased by one, depending upon whether the forward or reverse line is energized. If neither line is energized, values are unchanged during transposition.

SEQUENTIAL OPERATIONS

Incorporating the count network and the transpose register permits a great variety of format revision functions typical of many input/output problems. Among these are

★ Sequential Load – Sequential Unload.
Requires count network only. Characteristic of block-by-block magnetic tape operations. Reversible feature of counter permits reading tape backwards.

★ Interlaced Load and Unload
Uses count network and transpose register. Useful in character-by-character magnetic tape operations.

★ Load Into One Memory Area Interlaced with Clear/Write or Read/Restore in Another Area
Uses count network and transpose register. Characteristic of operations performed in conjunction with punched cards, parallel printing, and meteor burst communication.

★ Write Into One Area; Unload from Another
Uses count network and transpose register. Punched card reading applications.

★ Interlaced Use of Two Memory Areas
Uses count network and transpose register. Performs functions of two independent buffer memories and is applicable to all types of data processing.

TIMING

PULSES—To operate the TYPE RB at rated speed, pulses must rise within 0.2 microsecond, have a duration of from 0.5 to 1.0 microsecond, and fall within 0.4 microsecond. Slower rise times to one microsecond may be used, but the excess time is added to the clear time and the cycle time.

ZERO TIME t_o – The instant when LS or ULS crosses the input reference voltage.

END OF CYCLE—Memory operation, 8 microseconds; buffer operation, 5 microseconds after LS or ULS.

ADDRESS AND MEMORY SIGNALS—Single ended pulses may be used if the register is cleared one microsecond before transfer. The strobe pulse to AR or MR, either in pulse or level form, must occur by t_o. Levels must have settled within 0.25 microsecond before an MR or AR pulse begins. A strobe pulse must not occur earlier than 0.5 microsecond before end of cycle.

COUNT AND TRANSPOSE SIGNALS—Same as for AR and MR signals.

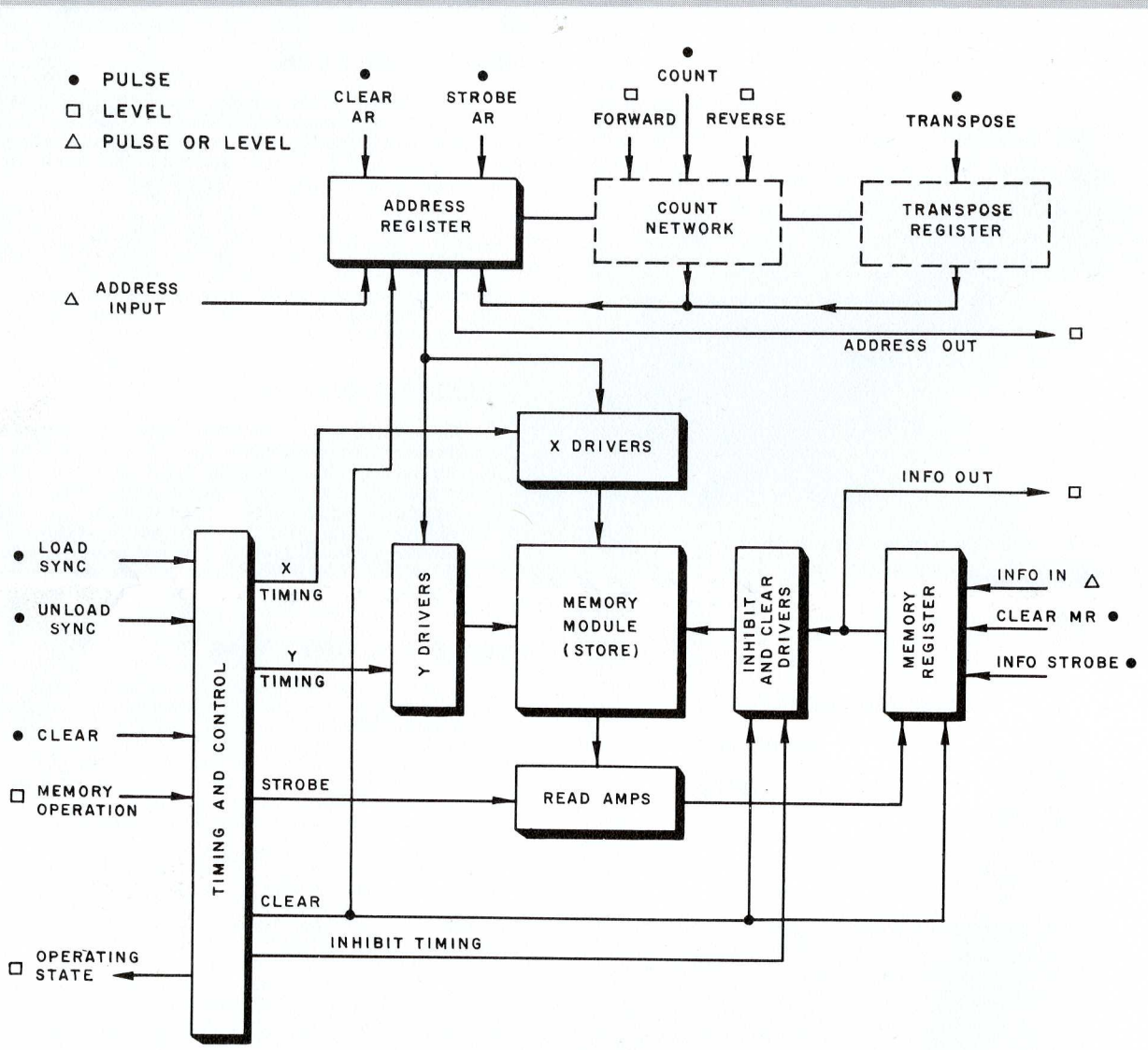
MEMORY OPERATION—This line must be in the selected state by at least $t_o - 0.5$ microsecond and maintain this state until $t_o + 4.0$ microseconds.

FORWARD, REVERSE—These lines must be settled within 4.5 microseconds before a count or transpose pulse has crossed the reference voltage and must not be changed until this occurs.

CLEAR—This pulse must occur after the end of cycle and no other pulses may be transmitted to the unit for an additional 25 microseconds. This pulse may not be transmitted again for 100 microseconds, and there shall be no more than 40 pulses in any 10 millisecond period.

OUTPUT ADDRESS INFORMATION—These lines settle within 1.5 microsecond after t_o until next t_o.

OUTPUT INFORMATION—These lines settle within 4 microseconds after t_o and maintain this state until MR is externally changed or until one microsecond after t_o if subsequent operation is unload or read.



TYPE RB
BLOCK DIAGRAM