REVISIONS

EFFECTIVITY	AUTH	LTR	DESCRIPTION	DATE	APPROVED
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CHANGE ACTIVITY PENDING, YES ☐   NO ☐

REV																											
SHEET	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
REV																											
SHEET	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52
REV STATUS	REV																										
OF SHEETS SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH:
.X = .1
.XX = .03
.XXX = .010
ANGLES = 0° 30'
DO NOT SCALE DRAWING
MATERIAL:

CONTRACT NO.

	SIGNATURE	DATE
DRAWN		
CHECK		
ENGR.	BJD	11/17/77
PROJ. ENGR.	BJD	11/17/77
QUAL. ASSURANCE		
RELIABILITY		
PROD. DESIGN		
OTHER APPROVALS		

Telefile

TITLE

T328X DISK DRIVE INTERFACE
PRODUCT SPECIFICATION

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A	51360	SS-600-0056-1A

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1.0 SCOPE

This document describes the functional characteristics of the disk drive interface in the TELEFILE T3281 Disk Controller. Section 3.0 describes the general disk drive interface function. Specifics for the T3286 disk drive interface are described in Section 4.0. Section 5.0 contains specific information for the T3282, T3283 and T3288 disk drive interfaces.

2.0 APPLICABLE REFERENCE DOCUMENTS

2.1 SS-600-0064-1B   T3281 Controller Product Specification

2.2 SS-600-0050-1A   Microprocessor Control Board Product Specification

2.3 SS-600-0053-1A   Serializer/Deserializer/ECC Product Specification

2.4 SS-600-0054-1A   Data Encoder/Decoder Product Specification

2.5 SS-600-0055-1A   T3286 Disk Drive Interface Product Specification

2.6 SS-600-0058-1A   IFX/7902 Product Specification

2.7 CDC 64709300   Product Specification for the Flat Cable Interface Storage Module Drive Family. Control Data Corporation.

2.8 Preliminary   Disk Drive Interface
    STC 8350-B2

2.9 SS-600-0080-1A   T3282/3/8 Drive Interface Product Specification

3.0 GENERAL DISK DRIVE INTERFACE

The T3281 controller is designed to interface to a wide variety of disk drives intermixed in any fashion as described in Reference 2.1. The controller hardware is designed to interface to a maximum of sixteen disk drives. The interface to the disk drives will be radial, as illustrated in Figure 3-1, with each disk drive having an independent electrical interface and control, status, and data cable set.

The microprocessor in the controller will, via microcode, generate all the protocol and timing functions required for the drive to position heads, transfer data, and execute diagnostic control functions. The CPU interface will only have minimal control capability for selection drives in order to monitor status and perform a reserve or release function during the execution of I/O commands in which the timing requirements are such that the microprocessor may not be involved.

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Figure 3-1. Controller/Disk Drive Interface
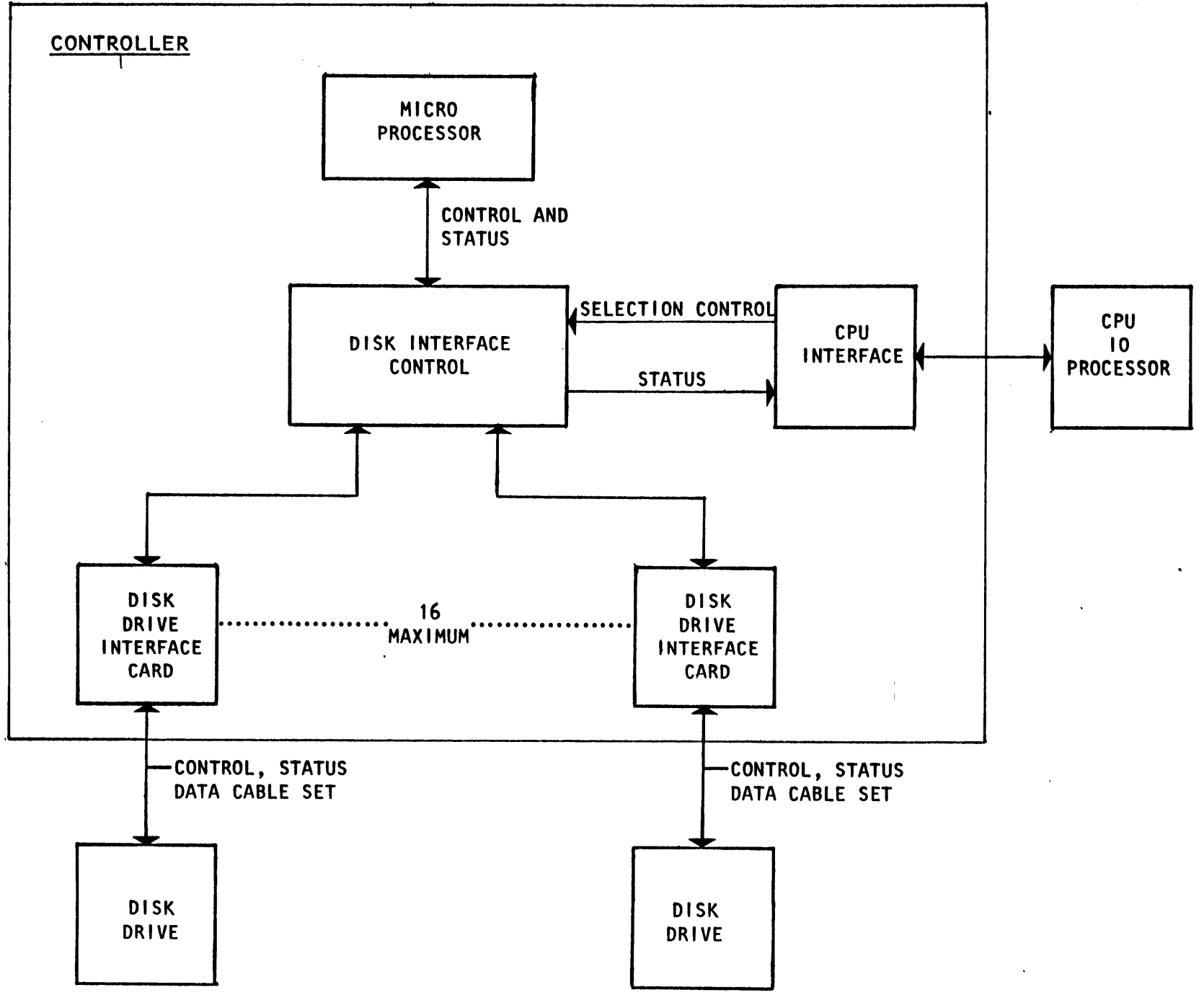
CONTROLLER

```
                    ┌──────────────┐
                    │    MICRO     │
                    │  PROCESSOR   │
                    └──────────────┘
                           ▲
                           │  CONTROL AND
                           │  STATUS
                           ▼
┌──────────────┐    ┌──────────────┐  SELECTION CONTROL   ┌──────────────┐        ┌──────────────┐
│              │    │              │ ◄────────────────────│     CPU      │        │     CPU      │
│              │    │     DISK     │                       │  INTERFACE   │ ◄─────►│      IO      │
│              │    │  INTERFACE   │        STATUS         │              │        │  PROCESSOR   │
│              │    │   CONTROL    │ ─────────────────────►│              │        │              │
│              │    └──────────────┘                       └──────────────┘        └──────────────┘
```

```
   ┌───────────┐                                      ┌───────────┐
   │   DISK    │                                      │   DISK    │
   │   DRIVE   │          16                          │   DRIVE   │
   │ INTERFACE │ ·······MAXIMUM·····················  │ INTERFACE │
   │   CARD    │                                      │   CARD    │
   └───────────┘                                      └───────────┘
        ▲                                                   ▲
        │ ─CONTROL, STATUS                                  │ ─CONTROL, STATUS
        │  DATA CABLE SET                                   │  DATA CABLE SET
        ▼                                                   ▼
   ┌───────────┐                                      ┌───────────┐
   │   DISK    │                                      │   DISK    │
   │   DRIVE   │                                      │   DRIVE   │
   └───────────┘                                      └───────────┘
```

The disk interface control function, under control of the microprocessor, will supply:

a. A generalized disk control interface function similar to that described for the T3286 disk drive in Reference 2-5 and 2-8. The interface card for any drive having a different control interface must adapt the specific interface to this general function.

b. Address translation and drive selection functions.

c. Disk parameter tables.

d. Status error checks.

The interface cards for the specific drive will supply:

a. Receivers and drivers to translate the disk drive's control, status and data lines signal level to the general TTL level interface within the controller.

b. Drive type and track format codes supplied by switches or jumpers.

c. A target sector counter to provide the rotational position interrupt window required for head positioning interrupts.

d. Logic to translate the general disk interface protocol to that required by the specific drive.

The characteristics of the elements of the general disk drive control interface are described in the following paragraphs.

3.1 GENERALIZED DISK DRIVE INTERFACE

The general control interface signals utilized in the controller are illustrated in Figure 3-2. The interface signals are described in the following paragraphs.

3.1.1 Sequence Enable

A unique signal is supplied to each drive interface card to enable power sequencing in the drive.

3.1.2 Device Bus Out

The device bus out consists of eight lines which are used to transfer operational information to the disk drives. The meaning of the information is determined by the device tag bus (see 3.1.3). Odd parity is presented for the bus information at all times.

The device bus out signals are driven by a register on the SERDES module (see 3.2.1) which may be loaded by the microprocessor. The register is illustrated in Figure 3-3.

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BUSS TO OTHER
DRIVE INTERFACE CARDS

DISK
INTERFACE
BUFFER

DEVICE BUS OUT (8 + PARITY)
DEVICE TAG BUS (3 + PARITY)
TAG GATE
SELECT HOLD
RELEASE
DEVICE BUS IN (8 + PARITY)
TAG VALID
READ DATA
WRITE DATA
CLOCK (PLO)
ADDRESS
DEVICE PRESENT
SH LATCH
ATTENTION
INTERRUPT WINDOW
DEVICE INTERFACE SELECT

DISK
DRIVE
INTERFACE
CARD

(1 OF 16)

UNIQUE
SIGNALS
PER CARD
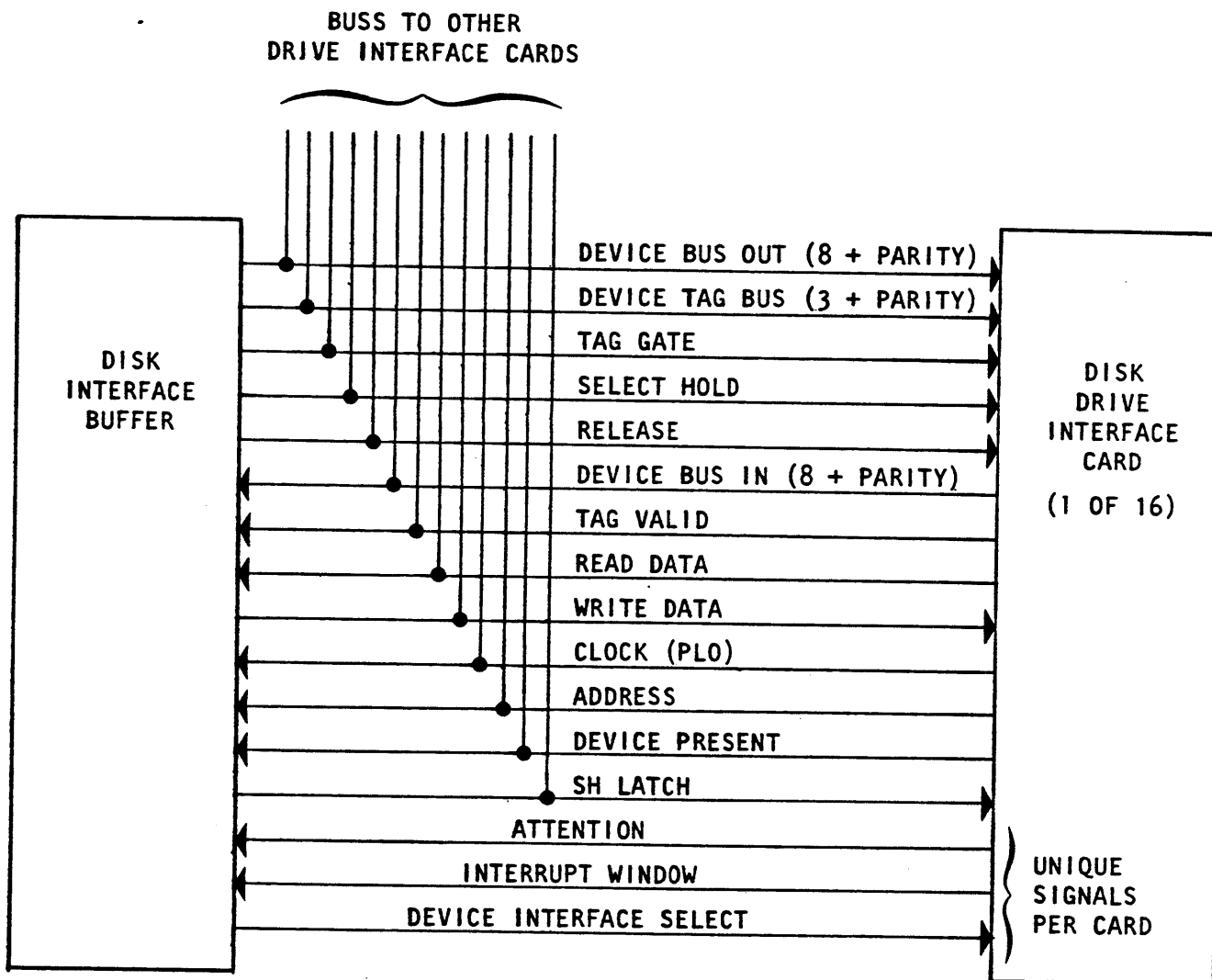
Figure 3-2. General Disk Interface

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Figure 3-3. Disk Interface Control
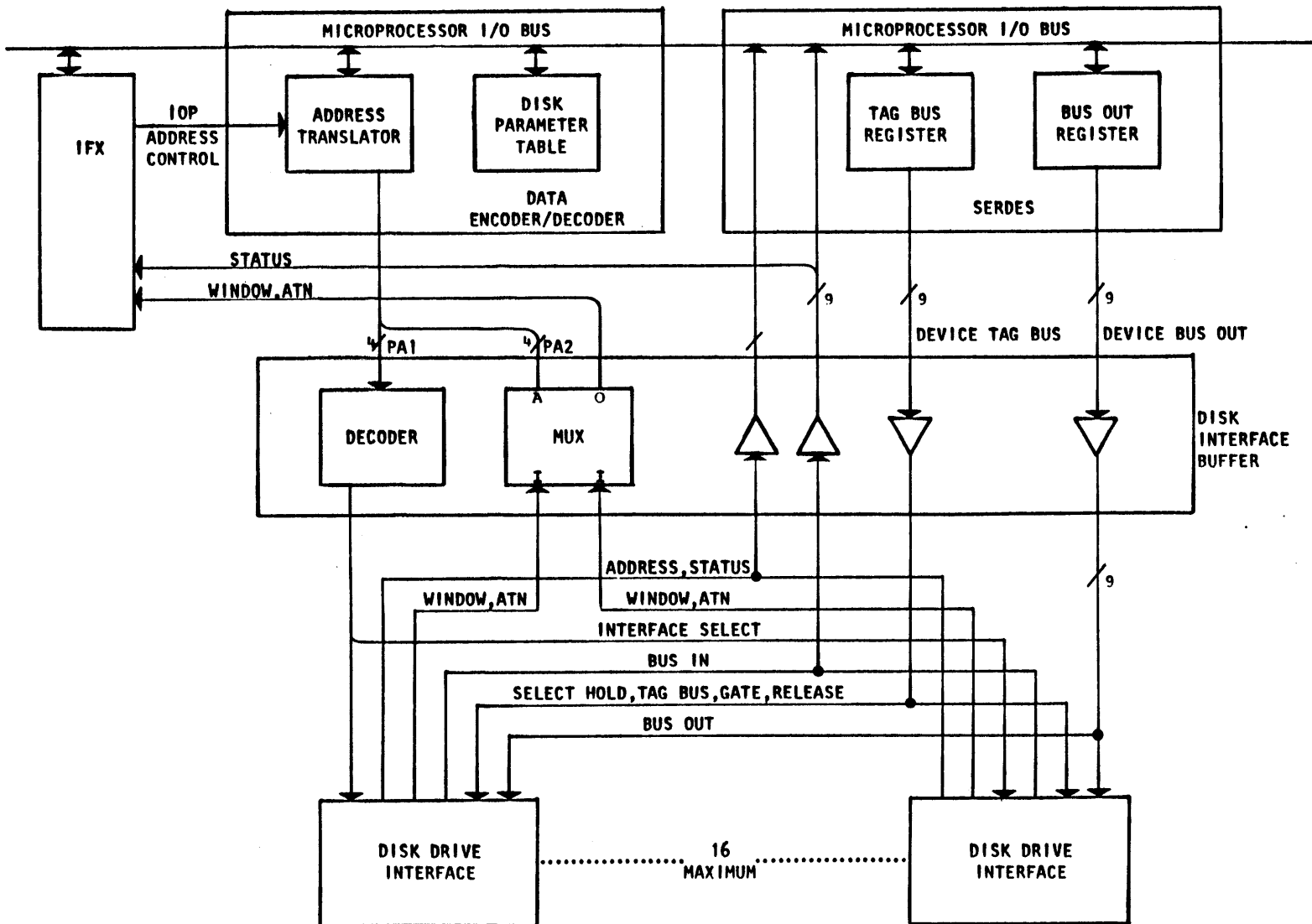
3.1.3 Device Tag Bus

The device tag bus consists of three lines which define the function of the operational information transmitted to the drive on the device bus out (see 3.1.2) and the status information received from the device on the device bus in lines (see 3.1.6). Odd parity is presented for the tag bus information at all times. The information on the tag bus is gated in the device by the tag gate signal (see 3.1.4).

The tag bus out signals are supplied by a register on the SERDES module (see 3.2.2) illustrated in Figure 3-3.

3.1.4 Tag Gate

The tag gate signal is sent to the drive to gate the tag bus and bus out information. It can be raised after the data appears on bus out and tag bus and at least a 200 nanosecond delay has elapsed. The tag gate is driven by bit 4 of the disk tag register as shown in Figure 3-3 and described in 3.2.2.

3.1.5 Select Hold

Select hold is used to maintain selection of the drive for performing operational functions. It must be raised during the tag gate for the SELECT tag code and stay up as long as communication is necessary with the selected drive. A delay of at least 200 nanoseconds should occur between the leading edge of the tag gate and the leading edge of select hold. The select hold signal is driven by bit 3 of the disk tag register shown in Figure 3-3 and described in 3.2.2.

3.1.6 Device Bus In

The device bus in consists of eight lines which carry status and sense information from the drive to the microprocessor. The status on the bus at any time depends on the tag function (see 3.1.3) being executed and the drive type. Odd parity is maintained on the bus in data. Data on these lines will be valid nanoseconds after the leading edge of tag gate. The data will be maintained as long as tag gate is up. The device in bus may be monitored by the microprocessor via an input function as described in 3.2.3.

The bit configuration of the data on the device in bus for various tag codes and drive types is described in Sections 3.4, 4.0 and 5.0.

3.1.7 Tag Valid

The tag valid signal is returned from the selected drive to indicate that device bus out (see 3.1.1) and tag bus were received with correct parity. The tag valid signal may be monitored by the microprocessor via the device interface status byte described in 3.2.4.

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3.1.8 Read Data

This line carries the read data from the selected drive to the DATA ENCODER/DECODER module (Reference 2-4). This is a TTL signal bussed between all drive interface cards. It is converted to a differential current mode signal for transmission to the DATA ENCODER/DECODER module as shown in Figure 3-4. The R/W DATA BUS on which the read data is transmitted is a bilateral line. Signal DSW produced by the DATA ENCODER/DECODER enables the driver function whenever data is being read from the disk drive.

3.1.9 Write Data

This line carries write data to all drive interface cards during write functions. Write data is transmitted from the DATA ENCODER/DECODER module (Reference 2-4) on the bilateral R/W DATA BUS as a differential current mode signal as shown in Figure 3-4. It is converted to a single ended TTL level signal prior to transmission to the drive interface cards. Signal DSW will disable the read data driver on the bilateral R/W DATA BUS during write functions.

3.1.10 Clock (PLO)

This line carries the PLO or CLOCK signal from the selected drive to the DATA ENCODER/DECODER module (Reference 2-4). The TTL signal is converted to a differential current mode signal prior to transmission to the DATA ENCODER/DECODER module as illustrated in Figure 3-4.

3.1.11 Attention

A unique signal for each drive which indicates when it is high that one of the following has occurred:

a. drive power up;
b. a head positioning function has completed;
c. a seek error has occurred;
d. a manual operator function has occurred i.e., pack change, etc.

The attention lines may be monitored by the microprocessor as described in When a line is found to be true, the microprocessor will enter this fact in the ATTENTION STORE described in Reference 2-6 and reset the attention line at the drive interface (see 4.8.2). The contents of the store will be monitored by the micro-processor during device interrupt scans (see Reference 2-6).

3.1.12 Interrupt Window

The interrupt window is a unique signal for each disk drive which defines the time in which a rotational position interrupt (on sector) may be generated to the main-frame. The signal will be set at the leading edge of the sector whose address has been sent to the drive with a SET TARGET SECTOR tag code (see 3.2.2). The pulse width of the signal will be determined by a one-shot.

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Figure 3-4. Data and Clock Interface
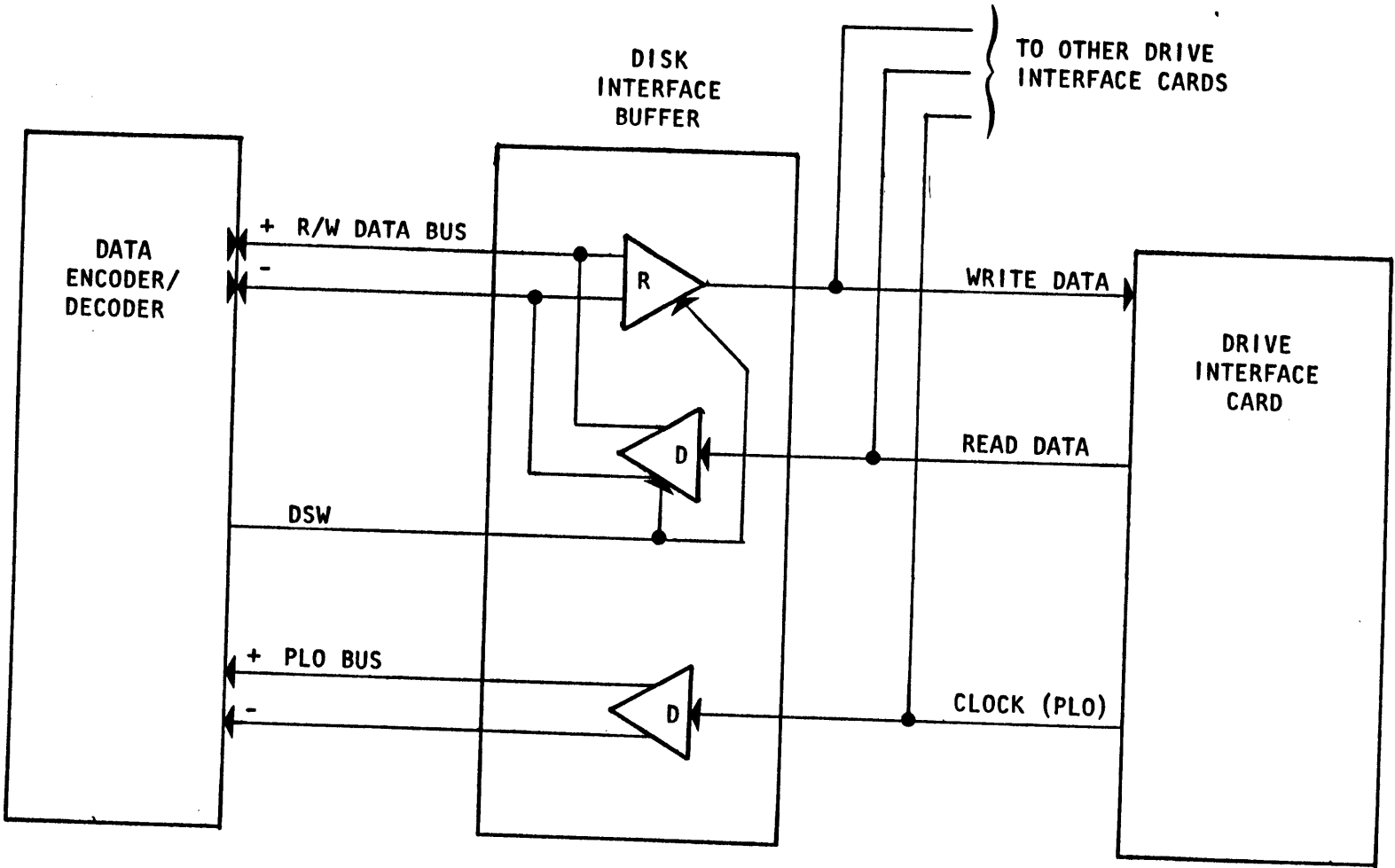
The interrupt window signals will be monitored by the microprocessor as described in Reference 2.6. The microprocessor will set an on-sector device interrupt call to the IOP when the interrupt window is high and the attention and modifier bit stores are set (Reference 2-6).

3.1.13 Device Interface Select

A unique line per drive interface (one of sixteen) which selects the drive interface card in the bussed interface system to be monitored or controlled. The lines are decoded from the four position address lines (PA) supplied by the drive address translator shown in Figure 3-3 and described in Reference 2-4.

These signals only select the interface. The drive must be functionally selected via a SELECT DEVICE tag function (see 3.4.2) in order to perform any operation on the drive or return status (except for device logical address--see 3.1.14).

3.1.14 Address

The address function consists of four lines which reflect the logical address of the disk drive as defined by the logical address plug function installed at the drive (see 3.3.1). The data on these lines may be read any time an interface is selected and DEVICE PRESENT is true (see 3.2.4).

3.1.15 Device Present

The device present signal indicates, when true, that the selected interface exists, a drive is connected, and is powered up and accessible by the controller.

3.1.16 Release

The release signal will be utilized to release a disk drive that has been reserved by the controller. It must be raised during a functional select in order for the release of the drive to be accomplished (see 3.4.2.4).

3.1.17 SH Latch

The SH LATCH signal will occur during a momentary drive select generated by an I/O command from the CPU if:

a. The microprocessor is monitoring the drive interfaces (see Reference 2-4, Section 3.14.5).

b. The SELECT HOLD (See 3.1.5) signal is set.

The SH LATCH signal will latch the SELECT HOLD function in the drive interface so that the drive will be selected when the microprocessor tag function is resumed at the end of the I/O command (see Reference 2-4, Section 3.14.5).

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3.2 DISK INTERFACE CONTROL SYSTEM

The disk interface control system, illustrated in Figure 3-3, supplies the selection, control and status monitoring interface between the microprocessor and the disk drives. It consists of:

a. the device out bus register described in 3.1.2 and Reference 2-3;

b. the device tag bus register described in 3.1.3 and Reference 2-3;

c. the device bus is described in 3.1.6 and Reference 2-3;

d. the device address/status bus described in Reference 2-3;

e. the device address translator described in Reference 2-4;

f. the disk parameter table described in Reference 2-4;

g. the disk interface buffer.

These functions are summarized in the following paragraphs:

3.2.1 Device Bus Out Register--Interface Vector Address 070_8

The function consists of a byte wide register which may be loaded or read by the processor via input/output functions utilizing interface vector address 070 octal (left bank). The outputs of the register supply the device bus out signals (see 3.1.2) to the disk drive interface. These signals transfer operational information from the microprocessor to the selected disk drive. The meaning of the information is determined by the TAG BUS register (see 3.2.2). Timing and bit significance of the device bus out signals is described in Sections 3.4, 4.0 and 5.0.

Odd parity is generated for the device bus out and transmitted to the disk drive (interface) to provide a check on the bus data received at the drive.

3.2.2 Device Tag Bus Register--Interface Vector Address 071_8

The function consists of a byte wide register which may be read or loaded by the microprocessor via input/output functions utilizing interface vector address 071 octal (left bank). The register provides the tag bus (see 3.1.3) and tag gate (see 3.1.4) functions for the control interface of the disk drives. The tag bus code defines the meaning of the information on the device bus out (see 3.2.1) and the operation to be performed on the disk drive as described in
The bit assignment of the register is:

—

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Bit	Function
0&1	Unassigned
2	RELEASE
3	SELECT HOLD
4	TAG GATE
5	TAG BUS 4
6	TAG BUS 2
7	TAG BUS 1

Bit 4 of the register supplies the tag gate (see 3.14) signal which gates bits 5 through 7 in the drive (interface to define the required function. The coding of the tag bus lines will be common to all drive types with any differences in function being accomplished within the drive interface card. The tag bus codes are:

TAG	BUS	BIT	
4	2	1	Function
0	0	0	SELECT DEVICE. The device is functionally selected so that operations may be performed (see 3.4.2).
0	0	1	SENSE INTERFACE. Status and configuration information are returned from the disk interface (see 3.4.3).
0	1	0	DIAGNOSTIC SET. Provides forcing functions in the drive to aid troubleshooting (when drive has these internal capabilities).
0	1	1	SET HEAD ADDRESS. Transmits head address information to the disk drive.
1	0	0	SET DIFFERENCE. Transmits information depending on drive type:

    a. T3286 - cylinder address difference information required for performing a seek.

    b. T3282/3/8 - extended control and address information.

1	0	1	SET TARGET SECTOR. Transmits the sector address defining the rotational position interrupt time (see 3.1.12).
1	1	0	SET CYLINDER. Transmits cylinder address information and where required (T3282/3/8) initiates a seek operation.
1	1	1	CONTROL. Transmits control information to the drive to initiate head carriage movements, initiate read or write operations, select status data or perform.

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A subset of the tag codes are drive type independent and identical in function and bus out bit significance. These are described in Section 3.4. The remaining tag functions differ either in operation or bus out bit significance for the drive types which may be intermixed on the controller. These are described in Section 4.0 and 5.0 for the T3286 drive and the T3282/3/8 drives respectively.

Bit 3 provides control for the SELECT HOLD signal described in 3.1.5 and 3.4.2.1.

Bit 2 provides the reserved drive release functions described in 3.1.16 and 3.4.2.4.

Tag bus timing is described in Sections 3.4 and the following. Odd parity is generated on the tag bus data and transmitted to the disk drive (interface) to provide a check on the tag bus code received by the drive (interface).

3.2.3 Device Bus In--Interface Vector Address 072$_8$

An input function utilizing interface vector address 072 octal (left bank) will be used to transmit the device bus in data to the microprocessor. The bus in lines provide functional status from the selected disk drive. Their content is dependent on the tag bus code supplied to the drive (see 3.2.2) as described in Sections 3.4, 4.0 and 5.0 Odd parity check is provided on these lines and any parity error may be monitored by the processor via the address status byte described in 3.2.4. The bus in lines and parity check are only valid when a drive is functionally selected (see 3.4.2) i.e., a drive select tag bus function has been executed.

3.2.4 Address/Status Bus--Interface Vector Address 073$_8$

An input function utilizing interface vector address 073 octal (left bank) will be used to read the logical address (see 3.1.14 and 3.3.1) and certain status bits presented by the selected drive interface. The format of the data byte is:

Bit	Function
0	ADDRESS/STATUS BUS ERROR. True if the parity check on the ADDRESS/STATUS BUS data (bits 3 through 7) detects an error.
1	DEVICE BUS-IN ERROR. True if the device bus-in parity check detects an error.
2	TAG VALID. Indicates the tag bus function transmitted to the disk DRIVE WAS RECEIVED SUCCESSFULLY.
3	DEVICE PRESENT. Will be true if the addressed drive interface exists and drive is connected and powered up (see 3.1.15).
4	ADDRESS 8
5	ADDRESS 4
6	ADDRESS 2
7	ADDRESS 1

Disk drive logical address (see 3.1.14)

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Bits 3 through 7 may be monitored any time a drive interface is selected i.e., the drive does not have to be functionally selected. The address contained in bits 4 through 7 will be valid only if bit 3 is true.

Bits 1 and 2 will be valid only if a drive is functionally selected i.e., a drive select tag bus function has been executed (Reference 2.5).

Only bits 2 through 7 and a parity bit are transmitted from the drive interface. Bits 0 and 1 are generated by parity checks on the SERDES module (Reference 2.3). Bit zero is generated by the parity check on bits 2 through 7.

This function will be utilized during a device address scan to establish the contents of the DEVICE ADDRESS TRANSLATOR described in 3.2.5. During the scan, the contents of bits 4 through 7 will be written into the translator RAM only if bit 3 is true.

3.2.5 Device Address Translator

The device address translator is a memory function that is utilized to translate a drive logical address, supplied by the microprocessor or by an I/O command from the CPU, to an interface position address in order to select the proper drive interface for an operation. The translator, and the address scan method utilized to establish its contents, are described in detail in Section 3.14 of Reference 2-4. The translator will normally be controlled by the microprocessor as described in 3.4.1 for selection of a drive interface.

3.2.6 Disk Parameter Table

The disk parameter table is a PROM memory which provides the microprocessor with a table look-up function used in determining disk address and track format parameters for the selected disk drive. The table is described in detail in Section 3.15 of Reference 2-4. The microprocessor will utilize the drive type code and track format code obtained from the drive interface via the SENSE INTERFACE tag code (see 3.4.3) to address the table for the look-up function.

3.2.7 Disk Interface Buffer

The disk interface buffer, shown in Figure 3-3, supplies the following functions:

a. Circuits to receive the bus out, tag bus, and control signals described in 3.1. The circuits will buffer and redrive the signals to the drive interface.

b. Circuits to receive the bus in, address and status signals from the disk drive interface. The circuits will buffer and redrive the signals to the SERDES, DATA ENCODER/DECODER and IFX modules.

c. Circuits to decode the four-bit position address code received from the device address translator (Reference 2-4) to provide the sixteen drive interface selection signals (see 3.1.13).

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d. Circuits to multiplex the attention (see 3.1.11) and interrupt window (see 3.1.12) signals to provide monitoring of the signals by the microprocessor.

e. Circuits to translate the TTL level read data, write data and PLO (clock) signals at the disk drive interface cards to the differential current mode signals required by the DATA ENCODER/DECODER module (see Reference 2-4).

All signals entering the buffer from the drive interfaces or from the other circuit modules will be received by Schmitt trigger type circuits having a high threshold and incorporating hysteresis. Any signal driven off the buffer will be capable of a fan out of at least eight TTL loads. All signals transmitted from the buffer to other circuit modules will be received with Schmitt trigger type circuits.

3.3 DEVICE ADDRESS

Any disk drive attachable to the controller will have three types of addresses associated with it. These are:

a. Logical address;

b. Position address;

c. Physical address.

These addresses are defined in the following paragraphs.

3.3.1 Logical Address

The device logical address is that utilized in mainframe I/O commands or by the microprocessor to select a device for an operation. The logical address is established at the drive by an address plug type function. This address is returned to the controller (see 3.1.14) and may be read by the microprocessor any time the drive interface is selected (see IV 073$_8$, Section 3.2.4). The logical address returned by each drive connected to the controller will be scanned periodically by the microprocessor and utilized to establish a logical/position address correspondence table for selection of the drive interface in the radial interface system corresponding to the logical address (see Reference 2.4, Section 3.14).

3.3.2 Position Address

The device position address defines the interface circuit card position in the controller (Figure 3-3) to which the device is physically cabled. The position address is normally translated from the logical address (supplied by an I/O command from the mainframe or by the microprocessor) via the address translator function described in Section 3.14 of Reference 2-4. The position address may also be supplied directly by the microprocessor during address scans to establish the logical/position address correspondence as described in Section 3.14 of Reference 2-4.

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The position address selects the device interface; the logical address (see 3.3.1) must be transmitted to the drive during a selection function (see 3.4.2) to functionally select the drive for any operation.

3.3.3 Physical Address

The device physical address is an eight-bit address hardwired within the device which uniquely identifies the device for system statistical error and usage logs. The physical address is available on the device bus in lines (see 3.1.6) during a SENSE INTERFACE tag function and may be read by the microprocessor.

3.4 COMMON DISK DRIVE CONTROL FUNCTIONS

The controller is capable of interfacing to a variety of disk drives as described in Reference 2-1. The disk drives described in Reference 2-1 utilize two different functional control interfaces. The controller microcode will utilize the general interface function and protocol described in Section 3.1 for drive control. The microcode will determine the drive type and provide the proper tag function and device bus out data format for control of the different drives. The control functions for the different drive interfaces are described in Sections 4.0 and 5.0.

There are some control functions which are drive independent and therefore common to the microcode for all drives. These functions are described in the following paragraphs.

3.4.1 Interface Selection

The drive interfaces are selected by two methods:

a. The microprocessor supplies a drive logical address to the drive address translator (see Section 3.14 of Reference 2-4). The logical address is translated to an interface position address and the corresponding interface selected and enabled for control by the microprocessor.

b. The microprocessor supplies an interface position address which bypasses the drive address translator and directly selects the drive interface.

The first method will be used in normal communication between the microprocessor and disk drives. The second method will normally be used only during a device address scan to establish the logical/position address correspondence data which is written into the address translator (see Section 3.14 of Reference 2-4).

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To establish the interface selection via the logical address method, (1) the micro-code will establish two IV bytes as shown below:

```
 0                       6   7
┌───┬───┬───┬───┬───┬───┬───┬───┐
│ X │ X │ X │ X │ X │ X │ X │ 0 │     IV 112₈ (4A)
└───┴───┴───┴───┴───┴───┴───┴───┘
```

```
 0           3   4               7
┌───┬───┬───┬───┬───────────────┐
│ X │ X │ X │ X │   LOGICAL     │     IV 110₈ (48)
│   │   │   │   │   ADDRESS      │
└───┴───┴───┴───┴───────────────┘
```
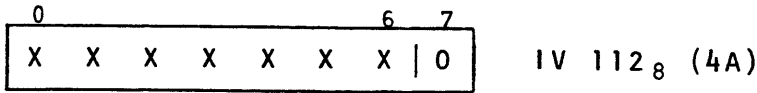
To establish the interface selection via the position address method, (2) the micro-code will establish the IV bytes as shown below:

```
 0                       6   7
┌───┬───┬───┬───┬───┬───┬───┬───┐
│ X │ X │ X │ X │ X │ X │ X │ 1 │     IV 112₈ (4A)
└───┴───┴───┴───┴───┴───┴───┴───┘
```

```
 0                               7
┌───────────────┬───┬───┬───┬───┐
│   POSITION    │ X │ X │ X │ X │     IV 110₈ (48)
│   ADDRESS     │   │   │   │   │
└───────────────┴───┴───┴───┴───┘
```
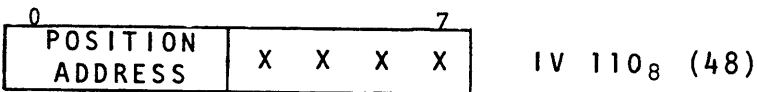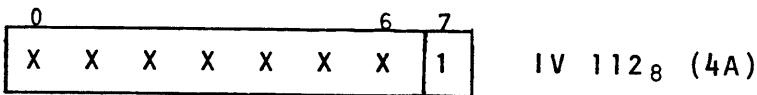
3.4.2 Device Selection

3.4.2.1 Select Tag

Tag code '0' (see 3.1.3) is utilized to select a drive for operational purposes after the interface has been selected (see 3.4.1). Prior to establishing the tag code, the logical address of the drive must be set-up on the device bus out:

```
 0           3   4               7
┌───┬───┬───┬───┬───────────────┐
│ X │ X │ X │ X │   LOGICAL     │     IV 070₈
│   │   │   │   │   ADDRESS      │
└───┴───┴───┴───┴───────────────┘
```

The logical address in bits 4 through 7 is identical to that supplied to the micro-processor for interface selection (see 3.4.1). The tag code must be established on the tag bus to the device (see 3.1.3) prior to raising the tag gate:

```
 0       2   3   4   5   6   7
┌───┬───┬───┬───┬───┬───┬───┬───┐
│ X │ X │ X │   │   │ 0 │ 0 │ 0 │     IV 071₈
└───┴───┴───┴─┬─┴─┬─┴───┴───┴───┘
              │   └──── TAG GATE
              │
              └──────── SELECT HOLD
```
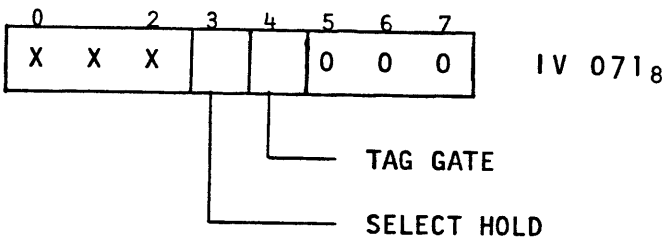
Timing of the bus out, tag bus and tag gate signals is controlled by the microcode as shown in Figure 3-5.

Tag valid (see 3.1.7) is returned from the drive if it is selected and there are no device tag bus or bus out parity check errors. If the logical address on bus out is not recognized, or if either bus out or tag bus have incorrect parity, no inbound lines, including tag valid, are activated.

Select hold (see 3.1.5) must be raised before or during the tag gate if the control sequence to the drive is to consist of more than the "select" tag function. Select hold will maintain selection of the drive and permit use of the bus out and tag bus for other functional control purposes. Select hold must be maintained as long as communication is necessary with the selected drive i.e., for the duration of any control sequence.

3.4.2.2 Machine Status Byte

If tag valid is returned by the device, then the machine status byte appearing on the device bus in (see 3.1.6) for the select tag may be utilized by the microcode for further determination of drive status. The byte, which may be monitored via IV 072_8 input functions, (see 3.2.3) has the following bit significance:

Bit	Function
0	RESERVED. This bit will be true if a dual channel drive is reserved by the other channel.
1	DEVICE INTERFACE CHECK. A device tag bus or device bus parity error has been detected, or drive is in service mode (see 3.4.3). Details can be determined using the sense interface tag (see 3.4.4).
2	DRIVE CHECK. The bit will be true if a seek error has occurred or a sector non-compare check has occurred. The conditions causing drive check are reset by check reset and FE reset (T3286) or by the fault clear function in other drives.
3	READ/WRITE CHECK. Read/write safety circuits have detected a condition that could endanger data integrity. These conditions are:

- Multiple heads selected
- Write current while reading
- No write current while writing
- No transitions while writing data
- Overrun while writing (T3286 only)
- Set read/write while not read/write enabled (not track following)
- Write gate on while not write enable
- Read gate and write gate on together
- Write gate and unsquelch on together
- Address mark control on without read gate
- Read/write interlock not present
- Index check (T3286 only)
- Low gain controls (T3286 only)

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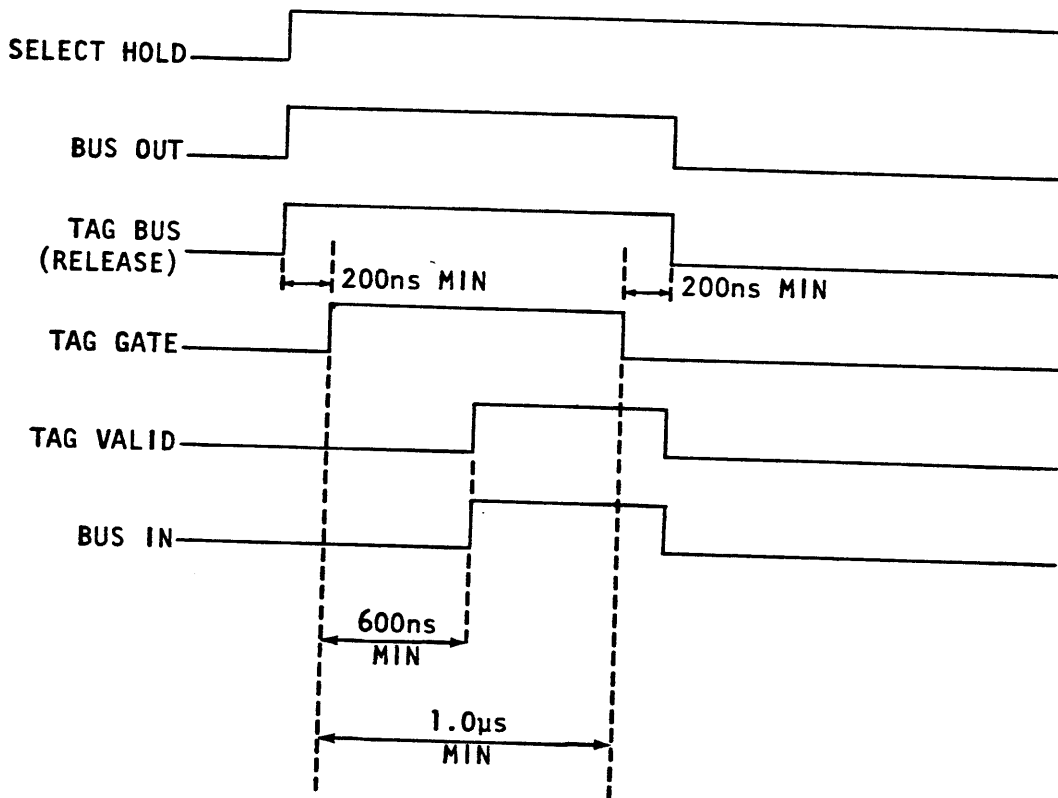
Figure 3-5. Timing for Select Device Tag '0'

SIZE	CODE IDENT NO.	SPEC. NO.
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Bit	Function

4   ONLINE. The drive start/stop switch is in the start position and the drive is 'ready'.

5   ATTENTION. The drive has been brought to the ready condition following a power sequence start signal; the drive start/stop switch has been set to the start position, or the attention switch (T3286 only) has been operated. The read/write heads are positioned over track zero when this signal is present.

6   BUSY. The drive is performing a rezero or, seek, search sector (T3286 only) or pad (T3286 only) operation. Busy is turned off by seek complete, sector complete or pad complete for a search sector operation. Busy is present again after sector compare has dropped if no attention reset is issued.

7   SEEK COMPLETE, SEARCH SECTOR, PAD COMPLETE. Seek, rezero, or pad (T3286 only) operation initiated by the controlling system has been completed or a search sector operation is in progress. The bit is true for a seek complete or a seek incomplete condition.

Seek complete is the normal end of a seek or rezero operation initiated by the controlling system. The specified track has been reached and drive check (bit 2) is off.

Seek incomplete is the abnormal end of a seek or rezero operation and is indicated by drive check (bit 2) appearing with seek complete. The drive access mechanism is in an undefined state.

Pad complete occurs when the pad cue operation reaches sector 126 prior to index (T3286 only).

3.4.2.3 Reserve of Dual Port Drive

If the selected disk drive has a dual port feature it is reserved to the controlling system during the select tag '0' function described in 3.4.2.1 if:

a. Selection occurs i.e., the logic address on the device bus out compares with that of the drive and the drive is online and;

b. No bus out or tag bus errors are indicated and;

c. The drive is not already reserved by the other channel (bit 0 of machine status 3.4.2.2).

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When the drive has been reserved by a channel via a select tag function, it will remain unavailable to the other channel until explicitly released by the reserving channel. During this time, the drive will return bit 0 of the machine status byte (see 3.4.2.2) true on any select tag function from the non-reserving channel.

3.4.2.4 Release of Dual Port Drive

A dual port drive that is reserved by a channel may be released by that channel during a select tag function (see 3.4.2.1) if the RELEASE control bit in the TAG BUS REGISTER (see 3.2.2) is set. Format of the register for release is:

```
   0   1   2   3   4   5   6   7
 +---+---+---+---+---+---+---+---+
 | X | X | 1 | 0 | 1 | 0 | 0 | 0 |      IV 071₈
 +---+---+---+---+---+---+---+---+
           |   |   |
           |   |   +------- TAG GATE
           |   +----------- SELECT HOLD
           +--------------- RELEASE
```
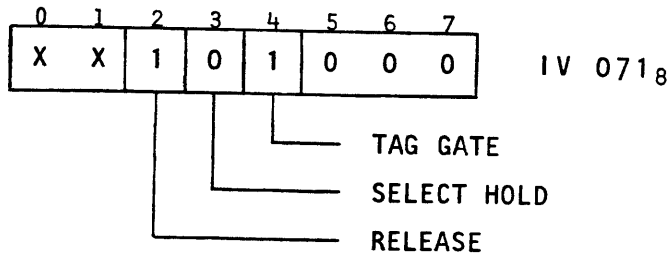
Timing for the select tag release function is illustrated in Figure 3-6.

3.4.3 Sense Interface

Tag function '1_8' is used to return status and control information from the selected drive and to transmit information to the drive to provide a communication link with the CE for remote in-line diagnostic execution. The information received or transmitted is dependent on the bit format of the device bus out. The various sense functions are decoded from the most significant four bits (0 through 3) of the bus out. The sense functions that are defined for tag functions '1' are illustrated in Table 3-1 and described briefly in the following.

3.4.3.1 Sense Interface '0'

This sense function returns data depicting conditions of the drive interface. Bit significance of the byte appearing of the device bus in is:

Bit	Function
0-2	Unassigned and equal to zero.
3	OTHER CHANNEL. This bit indicates that in-line diagnostics are not to be run by the controller. It occurs only in dual port drives and will be true only when bit 0 is true.

DEVICE BUS OUT IV 070_8 (38)								BUS IN IV 072_8 (3A)		SENSE CODE
0	1	2	3	4	5	6	7	BIT FIELD		
0	0	0	0	X	X	X	X	0-2 3 4 5 6 7	ZEROS OTHER CHANNEL CE EXECUTE SERVICE MODE DEVICE BUS OUT PARITY ERROR DEVICE TAG BUS PARITY ERROR	'0'
0	0	0	1	X	X	X	X	0-3 4-7	ZEROs DRIVE TYPE CODE	'1'
0	0	1	0	X	X	X	X	0-7	TRACK FORMAT CODE	'2'
0	0	1	1	X	X	X	X	0-7	DRIVE PHYSICAL ADDRESS	'3'
0	1	0	0	X	X	X	X			'4'
0	1	0	1	X	X	X	X	0-7	CE DATA IN	'5'
X	1	1	0	DATA 8	4	2	1	0-7	CE PROGRAM DISPLAY	'X6'
X	1	1	1	DATA 8	4	2	1	0-7	CE DATA DISPLAY	'X7'

Table 3-1.   Sense Interface Tag Format

SIZE	CODE IDENT NO.	SPEC. NO.
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Bit	Function

4   CE EXECUTE. This bit is the means of controlling communication between the CE and the microprocessor during running of in-line diagnostics remotely from the drive location. It will be set by the CE when he has set up data to be monitored by the microprocessor (SENSE '5'). The bit is set by the activation of a switch and will be reset by the trailing edge of SENSE '0' if the bit is true at the leading edge of SENSE '0'. The first setting of the bit after the drive has been placed in service mode will also cause attention (see 3.1.11) to be set.

5   SERVICE MODE. This bit indicates that the drive is being serviced and is available for in-line diagnostics but is not available for on-line operation. Bit is set when the drive is switched to service mode by the CE. It will cause DEVICE INTERFACE CHECK (see 3.4.2.2) to be set.

6   DEVICE BUS OUT PARITY ERROR. True if parity error has been detected on the bus out.

7   DEVICE TAG BUS PARITY ERROR. True if a parity error has been detected on the device tag bus.

This sense interface tag function (SENSE '0') forces tag valid even though device bus out and tag bus errors are present. The parity error latches are reset when the tag gate drops.

3.4.3.2 Sense Interface '1'

The SENSE '1' function returns the drive type code in bits 4 through 7 of the device bus in. Drive type code is utilized to determine disk pack address parameters (heads, cylinders) as described in 3.13.3 of Reference 2-4.

The drive type code is established by switches in the drive interface card.

3.4.3.3 Sense Interface '2'

The SENSE '2' function returns the track format code on the device bus in. This code defines the disk track format i.e., number of sectors, bytes per sector, gap times, etc. The function of this code is described in Section 3.13.4 of Reference 2-4. The track format code is established by switches on the drive interface card.

3.4.3.4 Sense Interface '3'

The SENSE '3' function returns the drive physical address (see 3.3.3) on the device bus in.

SIZE	CODE IDENT NO.	SPEC. NO.	
A	**51360**	SS-600-0056-1A	
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3.4.3.5   Sense Interface '4'

3.4.3.6   Sense Interface '5'

This sense function returns data on the device bus in which is set up by the CE via an
attached test panel. The data byte provides communication between the CE and the
microcode when drive diagnostics are being run from the remote drive location. The
byte is valid only if service mode is indicated by SENSE '0'.

3.4.3.7   Sense Interface '6'

This function is utilized to transmit data to a display on the CE test panel which
is attached to the drive when drive diagnostics are being run from the remote drive
location. The display provides information to the CE regarding the diagnostic
sequence. Bits 4 through 7 of the bus out contain data which is entered into the
upper or lower nibble of the display according to bit 0:

        Bit 0 = 0:   data entered into upper nibble (bits 0-3)

        Bit 0 = 1:   data entered into lower nibble (bits 4-7)

The contents of the CE program display register are returned on the device bus in
for this function. The data on bus in will reflect the data transmitted on bus out.

3.4.3.8   Sense Interface '7'

This function is identical to SENSE '6' (see 3.4.3.7) except that the data is trans-
mitted to a different display (CE DATA) on the test panel. This data will provide
results of the test to the CE. Data in bits 4 through 7 of bus out are transmitted
to the upper or lower nibble of the display according to bit 0 of bus out:

        Bit 0 = 0:   data entered into upper nibble (bits 0-3)

        Bit 0 = 1:   data entered into lower nibble (bits 4-7)

The contents of the CE data display register are returned on device bus in for this
function. The data on bus in will reflect the data transmitted on bus out.

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A	**51360**	SS-600-0056-1A	
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3.4.4 Set Target Sector

Tag function '5$_8$' transfers a sector number on the device bus out to the Target Sector Register in the drive interface. The sector number transmitted is used in rotational position sensing. The interrupt window signal (see 3.1.12) will be raised at the leading edge of the sector defined by this tag.

The contents of the target register are returned on device bus in during this tag function. The bus in lines will reflect the data transmitted on bus out if tag valid is true.

The format of the data on bus out for this tag function is:

Bus Out

Bit	Function
0	Not Used
1	Target Sector 64
2	Target Sector 32
3	Target Sector 16
4	Target Sector 8
5	Target Sector 4
6	Target Sector 2
7	Target Sector 1

4.0 T3286 INTERFACE FUNCTIONS

The control interface for the T3286 disk drive is described in the following paragraphs. Control of the drive by the microcode is executed by the device bus out, tag bus, and device bus in functions described in Section 3.2.

4.1 TAG '0$_8$' SELECT DRIVE

Tag function '0' provides selection of the disk drive for operational purposes. The device bus out data and the drive status returned on device bus in are described in Section 3.4.2.

4.2 TAG '1$_8$' SENSE INTERFACE

Tag function '1' provides return of status, format and control information from the selected disk drive and transmission of CE related data to the disk drive. The functions for tag '1', its bus out data formats and the information returned via bus in for these functions is described in Section 3.4.3.

SIZE	CODE IDENT NO.	SPEC. NO.	
A	**51360**	SS-600-0056-1A	
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4.3 TAG '2₈' DIAGNOSTIC SET

Tag function '2' is used in conjunction with device bus out to set the selected drive into predefined hardware status to aid troubleshooting. The bus out data format for the various functions possible under tag '2' is shown in Table 4-1. The device bus in is not defined for this tag. The tag '2' functions are briefly described in the following.

4.3.1 Servo Reset

This function forces the drive servo into zero mode and inhibits access movement or track following control while the tag is active.

4.3.2 Go Home

The GO HOME function causes the drive access mechanism to go to the home position, fully retracted into the head/disk assembly (HDA).

4.3.3 Force Delta

The function forces a delta IW check with an inner (odd) head selected (see 4.18.3).

4.3.4 Force Pad Gate Check

Force Pad Gate causes the device padding function to operate under diagnostic control.

4.3.5 Force Multihead Check

The Force Multihead Check command sets the odd head latch in the drive. A subsequent Set Read/Write Command forces Multihead Check if head address register (see 4.4) bit 6 is zero.

4.3.6 Decrement Difference Counter

This command causes the difference count in the drive (see 4.5) to be decreased by one.

4.4 TAG '3' SET HEAD ADDRESS REGISTER (HAR)

Tag function '3' is utilized to transfer the head address to the drive to select the head for performance of a write or read operation. The format of the data transmitted to the drive on bus out is:

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	A	**51360**	SS-600-0056-1A	
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DEVICE BUS OUT IV 070$_8$								FUNCTION
0	1	2	3	4	5	6	7	
1	0	0	X	0	X	0	0	SERVO RESET
0	1	X	0	0	X	0	0	GO HOME
0	0	1	X	0	X	0	0	FORCE DELTA
0	0	0	X	1	X	0	0	FORCE PAD GATE CHECK
0	0	0	X	0	X	1	0	FORCE MULTIHEAD CHECK
0	0	0	X	0	X	0	1	DECREMENT DIFFERENCE COUNTER

Table 4-1. Tag '2' Bus Out Data Format

SIZE	CODE IDENT NO.	SPEC. NO.
A	**51360**	SS-600-0056-1A
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Bit	Function
0	Fixed Heads 32-59
1	Fixed Heads 0-31
2	HAR 16
3	HAR 8
4	HAR 4
5	HAR 2
6	HAR 1
7	Reserved

If bits 0 and 1 are both zero, bits 2 through 6 define a movable head. If either bit 0 or bit 1 equal one, bits 2 through 6 define a fixed head.

The machine status byte described in 3.4.2.2 is returned on device bus in for this tag.

The contents of the head address register in the drive are returned on bus in by a CONTROL tag function (see 4.8.10).

4.5 TAG '4' SET DIFFERENCE

Tag '4' loads the Difference Counter of the selected drive. The Difference Counter is loaded with the difference between the current cylinder address and the desired cylinder address as calculated by the controlling system. The 256-bit and the 512-bit of the Difference Counter are loaded with tag '7' bus 'XE'. The difference value, including the 256 and 512 bits, must be set at least 8 microseconds before a Seek Start is issued.

Format of the data on bus out for the tag function is:

Bus Out
Bit	Function
0	Difference 128
1	Difference 64
2	Difference 32
3	Difference 16
4	Difference 8
5	Difference 4
6	Difference 2
7	Difference 1

The machine status byte described in 3.4.2.2 is returned on device bus in for this tag. The contents of the difference counter in the drive are returned on bus in by a CONTROL tag function (see 4.8.9).

SIZE	CODE IDENT NO.	SPEC. NO.	
A	51360	SS-600-0056-1A	
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4.6 TAG '5$_8$' SET TARGET SECTOR

Tag '5' transfers a sector number on bus out to the Target Register in the drive. This tag function is described in Section 3.4.4.

4.7 TAG '6$_8$' SET CYLINDER

Tag '6' transmits cylinder address data via the bus out to the Cylinder Address Register (CAR) in the drive. CAR is not functionally connected to the access mechanism; it serves only as a storage register to contain current position information. CAR is reset by a rezero command (see 4.8.4) to indicate that the heads are positioned over Track 0.

The bus out data format for this tag function is:

Bus Out Bit	Function
0	CAR 256
1	CAR 128
2	CAR 64
3	CAR 32
4	CAR 16
5	CAR 8
6	CAR 4
7	CAR 2

CAR 512 is transmitted to the drive by CONTROL tag '6' bus out 'XE' (see 4.8.7).

The machine status byte described in 3.4.2.2 is returned on device bus in for tag '6'. The contents of CAR are returned by a CONTROL tag function (see 4.8.8).

4.8 TAG '7$_8$' CONTROL

Tag '7' transfers control information to the selected drive. Under this tag the device bus out is divided into two groups of four bits each. Device bus out bits 4 through 7 are coded to perform 14 different functions. Bits 0 through 2 are interpreted to further control certain of these functions.

The functions performed under this tag are:

SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0056-1A
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- Seek Start
- Attention Reset
- Check Reset
- Rezero
- Drive Sync Tag
- Read/Write Check Reset
- Set Difference Hi
- Sense Cylinder
- Sense Difference Counter
- Sense Head Register
- Sense Target Register
- Sense Status
- Sense Read/Write
- Set Read/Write Control

The bus out data formats for the functions defined under tag '7' are summarized in Table 4-2. The data appearing on device bus in for each of the tag '7' functions is illustrated in Tables 4-2 and 4-3.

The tag '7' functions are described in the following paragraphs.

4.8.1 Seek Start ('X8')

Seek Start causes the drive to move the read/write heads as specified by the information contained in the Difference Counter and Head Address Register. The Difference Counter and the Head Address Register must previously have been set. If the difference count is zero, no physical accessing occurs, and the completion of the zero track seek is signaled immediately. Completion of the action initiated by Seek Start is signaled by Attention. At the termination of a Seek, the Seek Complete status bit in the machine status is on. An Access failure is indicated by the drive check bit being active with attention.

The machine status byte is returned on bus in for this function.

4.8.2 Attention Reset ('X4')

Bus out code 'X4' resets the attention signals in the selected drive. To prevent masking of attention signals, attention reset should be performed to reset attentions already present prior to the initiation of an operation resulting in an attention. Attention Reset also cancels pending Seek, Rezero, or Search Section Attention.

The machine status byte is returned on device bus in for this function.

4.8.3 Check Reset ('XC')

This code resets check conditions in the selected drive including read/write checks. The machine status byte is returned on bus in for this function.

SIZE	CODE IDENT NO.	SPEC. NO.		
A	51360	SS-600-0056-1A		
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\0	1	2	3	4	5	6	7	FUNCTION	DEVICE BUS IN (SEE TABLE 4-3)
X	X	X	X	1	0	0	0	SEEK START	MACHINE STATUS BYTE
X	X	X	X	0	1	0	0	ATTENTION RESET	MACHINE STATUS BYTE
X	X	X	X	1	1	0	0	CHECK RESET	MACHINE STATUS BYTE
X	X	X	X	0	0	1	0	REZERO	MACHINE STATUS BYTE
X	X	X	X	1	0	1	0	SYNC TAG	BUS IN NOT USED
X	X	X	X	0	1	1	0	READ/WRITE CHECK RESET	MACHINE STATUS BYTE
X	X	X	X	1	1	1	0	SET DIFFERENCE HI	MACHINE STATUS BYTE
X	X	X	X	0	0	0	1	SENSE CYLINDER	CAR CONTENTS
X	X	X	X	1	0	0	1	SENSE DIFFERENCE COUNTER	DIFFERENCE COUNTER CONTENTS
X	X	X	X	0	1	0	1	SENSE HEAD REGISTER	HEAD REGISTER CONTENTS
X	X	X	X	1	1	0	1	SENSE TARGET REGISTER	TARGET REGISTER CONTENTS
0	0	0	0	0	0	1	1	SENSE STATUS	SENSE STATUS BYTE 0
0	0	0	1	0	0	1	1	SENSE STATUS	ACCESS CONTROL STATUS
0	0	1	0	0	0	1	1	SENSE STATUS	DRIVE SWITCH STATUS
0	1	0	0	0	0	1	1	SENSE STATUS	HDA CONTROL SEQUENCE STATUS
1	0	0	0	0	0	1	1	SENSE STATUS	DRIVE CHECK STATUS
0	0	0	0	1	0	1	1	SENSE STATUS	READ/WRITE SAFETY STATUS
1	X	X	X	X	1	1	1	TRANSFER SECTOR COUNT	READ/WRITE STATUS
X	1	X	0	X	1	1	1	WRITE GATE	READ/WRITE STATUS
X	0	X	1	X	1	1	1	READ GATE	READ/WRITE STATUS
X	X	X	X	1	1	1	1	ADDRESS MARK CONTROL	READ/WRITE STATUS

DEVICE BUS OUT

↑ UNSQUELCH

Table 4-2. Tag '7' Data Format	SIZE A	CODE IDENT NO. 51360	SPEC. NO. SS-600-0056-1A
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Table 4-3. Tag '7' Device Bus In Format

FUNCTION	DEVICE BUS IN							
	0	1	2	3	4	5	6	7
MACHINE STATUS	RESERVED BY OTHER CHANNEL	INTERFACE CHECK	DRIVE CHECK	READ/WRITE CHECK	ONLINE	ATTENTION	BUSY	SEEK COMPLETE
READ/WRITE STATUS	RESERVED BY OTHER CHANNEL	I WRITE SENSE	DRIVE CHECK	READ/WRITE CHECK	ONLINE	PAD IN PROGRESS	INDEX MARK	3330 MODE
SENSE CYLINDER ('X1')	CAR 256	CAR 128	CAR 64	CAR 32	CAR 16	CAR 8	CAR 4	CAR 2
SENSE DIFFERENCE ('X9')	DIFF 128	DIFF 64	DIFF 32	DIFF 16	DIFF 8	DIFF 4	DIFF 2	DIFF 1
SENSE HEAD REGISTER ('X5')	FIXED HEADS 32-59	FIXED HEADS 0-31	HAR 16	HAR 8	HAR 4	HAR 2	HAR 1	UNUSED
SENSE TARGET REGISTER ('XD')	1	TAR 64	TAR 32	TAR 16	TAR 8	TAR 4	TAR 2	TAR 1
SENSE STATUS BYTE 0 ('03')	DIRECTION (FWD/REV)	DIFF 512	DIFF 256	CAR 512	HEAD SHORT CHECK	PAD GATE CHECK	1,2 MB FILE	FIXED HEAD INSTALLED
ACCESS CONTROL STATUS ('13')	ACCESS TIMEOUT CHECK	OVERSHOOT	SERVO OFF TRACK	REZERO MODE LATCH	SERVO LATCH	LINEAR MODE LATCH	CONTROL LATCH	WAIT LATCH
DRIVE SWITCH STATUS ('23')	DRIVE START SWITCH	GUARDBAND PATTERN	TARGET VELOCITY	TRACK CROSSING	NOT USED	AIR SWITCH	NOT USED	MOTOR AT SPEED
HDA CONTROL SEQUENCE STATUS ('43')	HDA PARITY MODE	HDA SEQUENCE LATCH 4	HDA SEQUENCE LATCH 2	HDA SEQUENCE LATCH 1	HDA TIMER CHECK LATCH	SEQUENCE CHECK LATCH	NOT USED	ODD TRACK
DRIVE CHECK STATUS ('83')	PAD IN PROGRESS	SECTOR COMPARE CHECK	MOTOR AT SPEED LATCHED	AIR SWITCH LATCHED	WRITE ENABLE	FIXED HEAD INSTALLED	SPINDLE MODE 2	SPINDLE MODE 1
READ/WRITE SAFETY STATUS ('0B')	MULTIPLE HEAD SELECT CHECK	CAPABLE/ ENABLE CHECK	WRITE OVERRUN	INDEX CHECK	DELTA CURRENT CHECK	CONTROL CHECK	WRITE TRANSITION CHECK	WRITE/ READ CHECK

4.8.4 Rezero ('X2')

Bus out code 'X2' causes the drive to place the heads over track 0 with HAR and Difference Counter reset to zero, which is the same condition as that after a head/disk assembly has completed a load sequence. Rezero is a low speed operation used to recover to a known track position after a seek error has occurred. Check reset must be issued prior to a rezero operation if an access check is present in the drive. The response after completion of this control function is similar to Seek Start. The machine status byte is returned on bus in for this function.

4.8.5 Drive Sync Tag ('XA')

Drive Sync Tag causes a signal in the drive to shift to a false level. This is used to provide oscilloscope sync pulses.

4.8.6 Read/Write Check Reset ('X6')

Read/write check reset causes these common read/write check to be reset:

- Multihead check
- Capable/Enable check
- Write Overrun
- Index check
- Interlock check
- Control check
- Transition check
- Write current check

The machine status byte (3.4.2.2) is returned on bus in for this function.

4.8.7 Set Difference Hi ('XE')

Set difference hi is used to load bus out bits 0-3 into registers in the drive. Bit significance is:

    Bit 0 - Direction (1 = in)
    Bit 1 - Difference count 512
    Bit 2 - Difference count 256 (bits 1 and 2 are extensions of the difference
            counter)
    Bit 3 - CAR bit 512 (this is an extension of cylinder address register).

The machine status byte is returned on bus in (see Table 4-3).

4.8.8 Sense Cylinder ('X1')

Cylinder address register contents are presented on bus in under tag '7' bus out 'X1'.
The value of the cylinder address register is bits 0-7 plus the high-order CAR bit,
if on, from sense status byte 0 bit 3 (see 4.8.12.1) plus the lo-order CAR bit, if on,
from HDA sequence control status bit 7, if on (see 4.8.12.4).

The bus in data format is shown in Table 4-3.

4.8.9 Sense Difference Counter ('X9')

Difference counter contents are presented on bus in under tag '7' bus out 'X9'. The
value of the difference counter is the bit significant value of bits 0-7 plus the 256
and 512 bits, if on, from sense status byte 0 bits 1 and 2 (see 4.8.12.1).

The bus in data format is shown in Table 4-3.

4.8.10 Sense Head Register ('X5')

The contents of the head address register (HAR) are presented on bus in under tag '7'
bus out 'X5'. Bus in data format is shown in Table 4-3.

For moving heads bits 0 and 1 are set to zero and bits 3-6 make up the bit significant
address of the current logical head to be used to perform read/write operations.

For fixed heads 0-31, bit 1 is on and bits 3-6 make up the address of the fixed head
to be used.

For fixed heads 32-59, bit 0 is on and 32 plus the bit significant value of bits
3-6 make up the current logical head number to be used to perform the read/write
operations.

4.8.11 Sense Target Register ('XD')

Tag '7' device bus out code 'XD' causes the contents of the target register to be
presented on the device bus in as shown in Table 4-3.

4.8.12 Sense Status ('X3')

Tag '7' device bus out code 'X3' causes one of five drive status bytes to be placed
on device bus in as determined by bits 0 through 3 of device bus out. For a summary
of each of the status bytes, refer to Tables 4-2 and 4-3.

The bit significance of the status bytes are described in the following.

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4.8.12.1 Sense Status Byte 0 ('03')

Sense Status Byte 0 is presented on bus in under tag '7' bus out '03' and is defined as follows:

Bus In Bit 0 - Direction. This bit defines the direction of the next seek

        1 = Forward (in, toward center of spindle)
        0 = Reverse (out)

Bus In Bit 1 - 512 bit of difference counter

Bus In Bit 2 - 256 bit of difference counter

Bus In Bit 3 - 512 bit of cylinder address register

Bus In Bit 4 - Head Short Check. Indicates that a short has been detected in a read/write head.

Bus In Bit 5 - Pad Gate Check. Turned on if pad gate and write gate occur simultaneously.

Bus In Bit 6 - 1.2 Megabyte File. This drive must be attached to a 1.2 megabyte CM.

Bus In Bit 7 - Fixed Heads Installed. Indicates that fixed heads are installed on this machine.

4.8.12.2 Access Control Status ('13')

Access Control Status is presented on bus in under tag '7' and bus out '13' and is defined as follows:

Bit 0 - Access Timeout Check. An access operation (seek or rezero) was not completed within 200 milliseconds and has therefore been terminated, or seek start was issued to the drive while the servo was not track following.

    Access timeout check causes a drive check.

Bit 1 - Overshoot. During a seek or rezero operation, one of the following events caused a drive check.

    a. three track crossings were detected after the difference counter decremented to zero;

    b. three track crossings were detected after the access control advanced to linear mode;

    c. a seek operation moved the carriage into the rezero pattern area.

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Bit 1 - Overshoot. During a seek or rezero operation, one of the following events caused a drive check.

    a.   three track crossings were detected after the difference counter decremented to zero;

    b.   three track crossings were detected after the access control advanced to linear mode;

    c.   a seek operation moved the carriage into the rezero pattern area.

Bit 2 - Servo Off Track. The servo has moved off track during a read or write operation. A rezero operation is required to reset this bit.

Bit 3 - Rezero Mode Latch

Bit 4 - Servo Latch

Bit 5 - Linear Mode Latch

Bit 6 - Control Latch

Bit 7 - Wait Latch. Bits 3 through 7 indicate the current state of the access control. Depending on which latch is on, the access control may be in any one of nine states.

4.8.12.3 Drive Switch Status ('23')

Drive Switch Status is presented on bus in under tag '7' bus out '23' and is defined as follows:

Bit 0 - Drive Start Switch

Bit 5 - Air Switch

Bit 7 - Motor at Speed. Bits 0, 5, and 7 indicate the condition of the interlocks for all states of the HDA sequence. The condition of each interlock is latch-stored for readout if an interlock fails during ready, or if an HDA sequence check occurs.

Bit 1 - Guardband Pattern

Bit 2 - Target Velocity

Bit 3 - Track Crossing. Bits 1, 2, and 3 are status conditions of the servo system used for diagnostic purposes.

Bit 4 and 6 - Not Used.

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4.8.12.4 HDA Sequence Control Status ('43')

HDA Sequence Control Status is presented on bus in under tag '7' bus out '43' and is defined as follows:

Bit 0 - HDA Mode Parity. Indicates that a parity error has occurred in the format selected for the HDA. This bit is generated if more than one mode is selected or if a jumper fails.

Bits 1-3 - HDA Sequence Latches 2 and 1. The condition of these latches indicates the state of the HDA Sequencer.

Bit 4 - HDA Timer Check Latch. Indicates that more than 10 seconds has elapsed between HDA sequence control states during a start sequence.

Bit 5 - HDA Sequence Check Latch. The condition of this bit (on/off) along with bits 1 through 3 indicates the sequencing state of the HDA.

Bit 6 - Not Used.

Bit 7 - Odd Physical Track. If on, the current physical cylinder address is odd. if off, the current physical cylinder address is even. This bit also represents the low-order bit of the cylinder address.

4.8.12.5 Drive Check Status ('83')

Drive Check Status is presented on bus in under tag '7', bus out '83' and is defined as follows:

Bit 0 - Pad-In-Progress. Pad-In-Progress is present when the drive has been conditioned to pad by the controller and index has not be passed.

Bit 1 - Sector Compare Check. This check indicates that two index marks have been detected without an intervening sector compare while performing a search sector operation.

Bit 2 - Motor at Speed Latched. Indicates that the latch failed while the drive was in a ready state.

Bit 3 - Air Switch Latched. Indicates that the switch failed while the drive was in a ready state.

Bit 4 - Write Enable. Indicates that the R/W or read switch on the operator panel is in the R/W position.

Bit 5 - Fixed Heads Installed. Indicates that fixed heads are installed.

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Bit 6 - Spindle Mode 2 Bit.

Bit 7 - Spindle Mode 1 Bit. Indicates the mode of operation.

Bit 6	Bit 7	Mode
0	0	Native
1	0	3330-1
1	1	3330-11

4.8.13 Read/Write Safety Status ('OB')

Read/Write Safety Status is presented on bus in under tag '7' bus out 'OB' and is defined as follows:

Bit 0 - Multiple Head Select Check. More than one head has been selected in the selected drive.

Bit 1 - Capable/Enable Check. One of the following conditions has occurred:

    a. set read/write was present while the drive was not read/write capable (track following);

    b. writing was attempted on a drive in the ready only condition.

Bit 2 - Write Overrun. Writing through an index mark has been attempted. It is permissible to write into or out of an index mark, but not both.

Bit 3 - Index Check. An invalid index check was detected while set read/write was present.

Bit 4 - Delta Current Check. Indicates that read/write cards or cables may be loose or missing.

Bit 5 - Control Check. The write gate signal has been present with the read gate signal.

Bit 6 - Write Transition Check. One of the following conditions has occurred:

    a. write transitions were not detected 54 microseconds (nominal) after write gate was turned on;

    b. write transitions were not present when write gate was turned off;

    c. write transitions were detected while reading.

Bit 7 - Write Current During Read Check. Write current was detected while reading.

SIZE	CODE IDENT NO.	SPEC. NO.	
A	**51360**	SS-600-0056-1A	
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4.8.14 Read/Write Status ('X7' or 'XF')

R/W status is presented on bus in under tag '7' bus out. R/W status bits are shown in Table 4-3 and defined as follows:

> Bits 0,2,3,4 - Same as corresponding machine status bits.
>
> Bit 1 - I Write Sense. The drive in read/write mode has sensed that write current is present at the read/write head.
>
> Bit 5 - Pad-In-Progress. The drive in read/write mode has been conditioned by the controller to pad to index.
>
> Bit 6 - Index Mark. The drive in read/write mode has detected an index mark.
>
> Bit 7 - 3330 Mode. The drive in read/write mode is operating in 3330 compatability mode.

The machine status byte is described in 3.4.2.2.

4.8.15 Machine Status Byte

The machine status shown in Tables 4-2 and 4-3 and described in 3.4.2.2 is always presented on the device bus in for any tag function except for the following:

- Under tag '7' with bus out bit 7 active bus in is defined depending on the decode of bus out bits 4 through 7.
- Under tag '7' bus out 'XA', bus in is not used.
- Under tag '2', diagnostic set, bus in is not defined.
- Under tag '1', sense interface.

4.8.16 Set Read/Write ('X7' or 'XF')

Tag '7' device bus out code 'X7' or 'XF' sets the read/write control in the device, and is established as follows:

- Device Tag Bus Bits 0, 1, and 2 are all 1's.
- Device Bus Out Bits 5, 6, and 7 are all 1's.
- Device Bus Out Bits 0 through 4 are conditioned so the various read and write controls may be transmitted to the device.
- Device tag gate is on.

The read/write controls are reset by dropping select hold. Read/write status (see 4.8.14) is presented on bus in under the set R/W tag.

The control functions defined under this tag are summarized in Table 4-2 and described in the following paragraphs. Timing relationship of the read and write gate is shown in Figure 4-1.

SIZE	CODE IDENT NO.	SPEC. NO.		
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4.8.16.1 Transfer Sector Count

If bit 0 of the device bus out is set, the contents of the sector counter are transferred to the target register for later readout.

4.8.16.2 Write Gate

Bit 1 of the device bus out, when set, allows writing to occur in the head/disk assembly.

4.8.16.3 Read Gate

Bit 3 of the device bus out, when set, causes the read amplifier, read detection, and data line drivers to be set to read mode.

4.8.16.4 Address Mark Control

Bit 4, in conjunction with bit 3, enables the read detector in the drive to detect address marks.

The bit is set in conjunction with bit 1 to allow writing of address marks on the disk.

5.0 T3282/3/8 INTERFACE FUNCTIONS

The T3282, T3283 and T3288 disk drives which may be attached to the controller as described in Reference 2.1 have a different control interface than the T3286 drive described in Section 4.0. The microcode will utilize the device bus out, tag bus, and device bus in described in Section 3.2 for control of these drives. The interface card for these drives described in Reference 2-9 will adapt the controller generalized interface (see 3.2) to the control interface of the driver. The control functions for the T3282/3/8 drives are described in the following paragraphs. The data formats for device bus out for the control functions are summarized in Table 5-1.

5.1 TAG '0_8' - SELECT DEVICE

Tag function '0' provides selection of the disk drive for operational purposes. The device bus out data and the drive status (machine status byte) returned on device bus in are described in Section 3.4.2.

5.2 TAG '1_8' - SENSE INTERFACE

Tag function '1' provides return of status; format and control information from the selected disk drive and transmission of CE related data to the disk drive.

The function for tag '1', its device bus out data formats and the information returned via the device bus in for the sense interface functions is described in Section 3.4.3.

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Figure 4-1.   Read/Write Gate Timing

Table 5-1. Device Bus Out Data Formats
For T3282/3/8 Drives

FUNCTION	DEVICE BUS OUT - IV 070₈ (38)							
	0	1	2	3	4	5	6	7
TAG '0' SELECT DEVICE	0	0	0	0	ADDRESS 8	ADDRESS 4	ADDRESS 2	ADDRESS 1
TAG '3' SET HEAD ADDRESS	0	0	0	HEAD 16	HEAD 8	HEAD 4	HEAD 2	HEAD 1
TAG '4' PRIOR TO TAG '6'	0	0	0	RESET CONTROL SELECT	WRITE DATA ENABLE	CLOCK SWITCH	CYLINDER 512	CYLINDER 256
TAG '4' FOR TAG '7'	0	0	0	RESET CONTROL SELECT	WRITE DATA ENABLE	CLOCK SWITCH	RELEASE	DATA STROBE LATE
TAG '5' SET TARGET SECTOR		SECTOR 64	SECTOR 32	SECTOR 16	SECTOR 8	SECTOR 4	SECTOR 2	SECTOR 1
TAG '6' SET CYLINDER	CYLINDER 128	CYLINDER 64	CYLINDER 32	CYLINDER 16	CYLINDER 8	CYLINDER 4	CYLINDER 2	CYLINDER 1
TAG '7' CONTROL	DATA STROBE EARLY	RTZ	AM ENABLE	FAULT CLEAR	SERVO OFFSET MINUS	SERVO OFFSET PLUS	READ GATE	WRITE GATE

SIZE **A**

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5.3 TAG '2₈' DIAGNOSTIC SET

Tag function '2' is not defined for the T3282/3/8 disk drives.

5.4 TAG '3₈' SET HEAD ADDRESS

Tag function '3' is utilized to transmit the head address to the selected disk drive to select a head for performance of a read or write operation. The format of the data transmitted to the drive on device bus out is:

        Bit 0 – Zero
        Bit 1 – Zero
        Bit 2 – Zero
        Bit 3 – HEAD 16
        Bit 4 – HEAD 8
        Bit 5 – HEAD 4
        Bit 6 – HEAD 2
        Bit 7 – HEAD 1

The read/write status byte described in 5.10 is returned on device bus in during this tag.

Bits 8 and 9 of the drive control bus (Reference 2-9) will be forced to zero by this tag. Tag '3' will transmit the Head Select (tag 2, Reference 2-7) to the disk drive.

5.5 TAG '4₈' SET DIFFERENCE

The T3282/3/8 drivers are direct addressing devices i.e., the controller need not calculate the difference in head position and transmit it to the drive in initiating a seek as in the T3286 (see 4.5). Tag '4' will be used in the T3282/3/8 drives to:

a. set-up bits 8 and 9 of the drive control bus (see Reference 2-9) prior to a SET CYLINDER or CONTROL tag;

b. reset the control select (see Reference 2-9) to the drive;

c. set internal controls in the drive interface card (see Reference 2-9) for clock switching and write data enable functions.

The bit significance of the data transmitted via device bus out for this tag is:

SIZE	CODE IDENT NO.	SPEC. NO.	
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Bits 0, 1, 2 - Zero

Bit 3 - Reset Control Select. This bit, when true, will reset the control select (see Reference 2.9) function that was previously set by a CONTROL tag (see 5.8).

Bit 4 - Write Data Enable. Enables the write data and write clock drivers at the drive interface. The signal should be set on 5 microseconds prior to the time valid data is transmitted to the drive.

Bit 5 - Clock Switch. Selects the source of the clock transmitted to the controller:

    Bit 5 = 0 Servo clock is transmitted. This clock must be selected anytime data is to be written on the disk.

    Bit 5 = 1 Read clock is transmitted. This clock must be selected anytime data is to be read from the disk.

Bit 6 - Bus 9. This bit defines control bus 2^9 described in Reference 2-9. For a SET CYLINDER tag, the bit significance will be cylinder address bit 512.

Bit 7 - Bus 8. This bit defines control bus 2^8 described in Reference 2-9. The bit has the following significance:

    SET CYLINDER '6' - cylinder address bit 256

    CONTROL '7' - Data strobe date

    Tag '4' may be used after a CONTROL tag '7' to change controls to the drive without disturbing the control select (see 5.8) function (except when bit 3 is true). The read/write status byte (see 5.10) is returned on bus in for this tag.

5.6 TAG '5_8' SET TARGET SECTOR

Tag '5' transfers a sector number on device bus out to the Target Register in the drive. This tag function is described in Section 3.4.4.

(5.7 TAG '6_8' SET CYLINDER

Tag '6' transmits cylinder address data via the device bus out to the drive and raises the cylinder address (tag 1) control to initiate a seek. The T3282/3/8 drives are direct addressing devices, the microcode need only execute the tag '6' function to initiate a seek. The format of the data on device bus out is:

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Bit 0 - Cylinder 128
Bit 1 - Cylinder  69
Bit 2 - Cylinder  32
Bit 3 - Cylinder  16
Bit 4 - Cylinder  8
Bit 5 - Cylinder  4
Bit 6 - Cylinder  2
Bit 7 - Cylinder  1
```

Cylinder address bits 256 and 512 must be established by a tag '4' function (see 5.5) prior to the tag '6'. The read/write status byte (see 5.10) is returned on device bus in for this tag function.

5.8 TAG '7_8' CONTROL

Tag '7' is utilized to set the control select function (see Reference 2-7) to enable read/write functional controls at the drive interface and to transmit the controls via the device bus out. The control select function, once set by a tag '7', will remain set until a tag '4' with bit 3 set (see 5.5) occurs. Tag '4' may be used prior to and after a tag '7' to control bits 8 and 9 of the drive control bus.

The data format of device bus out for tag '7' is shown in Table 5-1 and described in the following paragraphs. The read/write status byte (see 5.10) is returned on device bus in for this tag function. A timing diagram illustrating a read/write control sequence is shown in Figure 5-1.

5.8.1 Data Strobe Late (Tag '4', Bit 7)

When this line is true, the drive PLO Data Separator will strobe the data at a time later than nominal. Normal strobe timing will be returned when the line is false.

The data strobe late and strobe early controls are intended to be used as an aid to recover marginal data.

5.8.2 Data Strobe Early (Tag '4', Bit 0)

When this line is true, the drive PLO Data Separator will strobe the data at a time earlier than nominal. Normal strobe timing will be returned when the line is false.

5.8.3 RTZ (Tag '7', Bit 1)

A 250ns minimum, 1.0ms maximum pulse, sent to the drive will cause the actuator to seek track 0, reset the Head Register and clear the Seek Error flip-flop.

This seek is significantly longer than a normal seek to track 0, and should only be used for recalibration, not data acquisition.

SIZE	CODE IDENT NO.	SPEC. NO.	
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RESET CONTROL BUS
BITS 8 AND 9

TAG '4'

TAG '7'

READ GATE

AM ENABLE

CLOCK READ
SWITCH SERVO

WRITE GATE

CONTROL
SELECT

FIND
ADDRESS
MARK

VERIFY
HEADER

SWITCH
DRIVE
CLOCKS
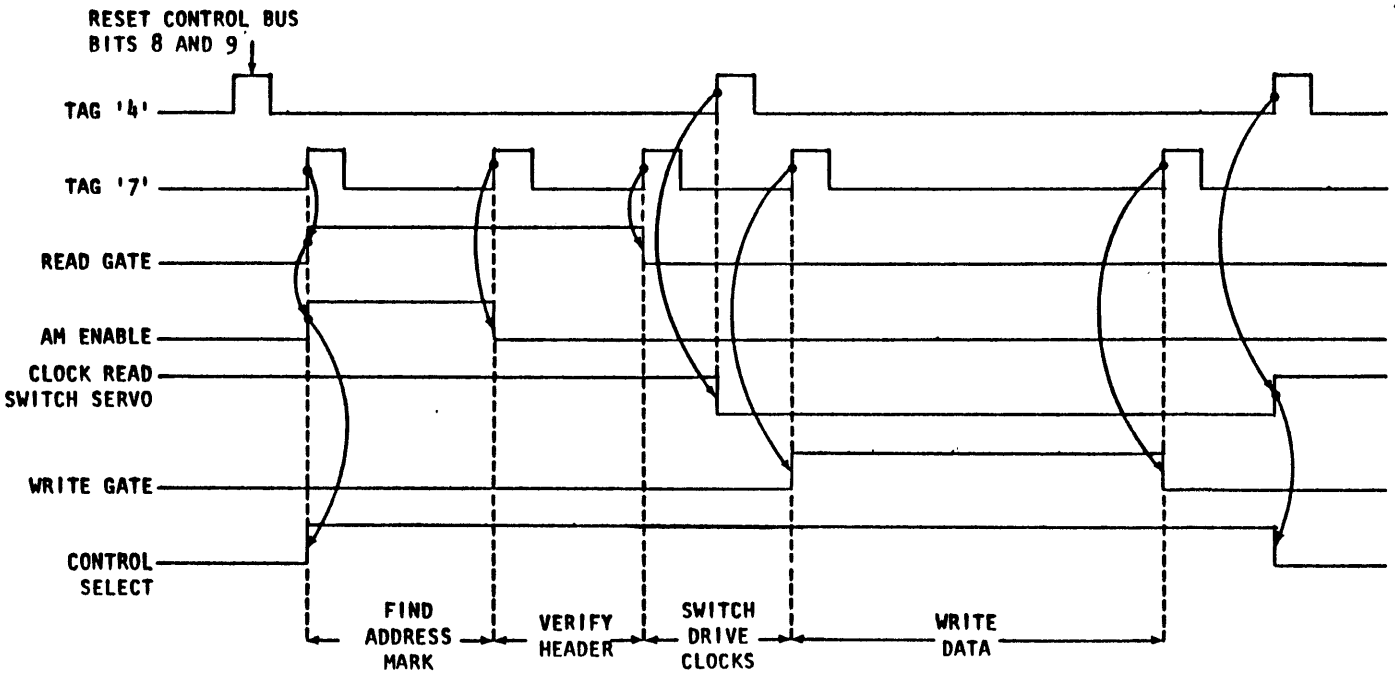
WRITE
DATA

Figure 5-1. Tag Sequence for Write
Data Operation

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SCALE

SIZE
A

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5.8.4 AM Enable (Tag '7', Bit 2)

The AM (Address Mark) Enable line, in conjunction with Write Gate or Read Gate, allows the writing or recovering of Address Marks. When AM Enable is true, while Write Gate is true, the writer will stop toggling and erase the data, creating an Address Mark. Write Fault detection in the unit is inhibited by this signal.

When AM Enable is true, while Read Gate is true, an analog voltage comparator detects the absence of read signal. If the duration of the erased area is greated than 16 bits, an Address Mark Found signal will be issued.

Address Mark should be 3.0 to 3.5 bytes in length with no transitions.

5.8.5 Fault Clear (Tag '7', Bit 3)

A 100ns minimum pulse sent to the drive will clear the fault flip-flop if the fault condition no longer exists.

5.8.6 Servo Offset Minus (Tag '7', Bit 4)

When this signal is true, the head actuator is offset from the nominal On Cylinder position away from the spindle.

5.8.7 Servo Offset Plus (Tag '7', Bit 5)

When this signal is true, the head actuator is offset from the nominal On Cylinder position towards the spindle.

NOTE: The servo Offset signals are intended to be used as an aid to recover marginal data. The carriage position returns to nominal when the respective signals go false. A carriage offsett will result in loss of On Cylinder and Seek Complete for a period of 3.2ms maximum. The maximum time for the carriage to move from forward to reverse offset or vice versa will not exceed 7ms. Data shall not be written while in the offset mode.

5.8.8 Read Gate (Tag '7', Bit 6)

This bit enables the drive to recover data from the disk pack. The leading edge triggers the data recovery system to synchronize on an all zeros data pattern. When raised with AM ENABLE (bit 2), it will allow detection of an address mark.

5.8.9 Write Gate (Tag '7', Bit 7)

This bit enables the write circuitry in the drive. When raised with AM ENABLE (bit 2), it will allow writing an address mark on the disk.

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A	**51360**	SS-600-0056-1A	
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5.9 MACHINE STATUS BYTE

The machine status byte shown in Table 5-2 and described in Section 3.4.2.2 is returned on the device bus in for the SELECT DEVICE (tag '0') tag function only.

5.10 READ/WRITE STATUS

The read/write status byte is returned on device bus in for all tag functions except:

    TAG '0' - SELECT DEVICE

    TAG '1' - SENSE INTERFACE

    TAG '5' - SET TARGET SECTOR

The status byte is summarized in Table 5-2. The bit significance of the byte is:

    Bit 0 - On Cylinder. This status indicates the servo has positioned the heads over a track. The status is cleared with any seek instruction causing carriage movement, or a zero-track seek. A carriage offset will result in loss of On Cylinder for a period of 2.75ms (nominal). For a zero track seek, On Cylinder drops for 30µs (nominal). The bit is equivalent to the BUSY bit in the machine status byte (see 3.4.2.2) for seek or RTZ commands.

    Bits 1, 2, 3, 4 - Same as corresponding machine status bits (see 3.4.2.2).

    Bit 5 - Address Mark Found. Address Mark Found is a 9µs maximum pulse which is sent to the controller following recognition of at least 16 missing transitions and the first zero of the zeros pattern.

        The controller should drop the Address Mark Enable line (see 5.8.4) upon receiving Address Mark Found (AMF) and valid data will be presented on the read data line following the AMF pulse (see Figure 5-4).

    Bit 6 - Index Mark. This signal occurs once per revolution, and its leading edge is considered the leading edge of the Sector Zero, typically 9µs. Timing integrity is retained throughout seek operations.

    Bit 7 - Write Protected. This bit indicates that the Write Protect switch is set on the drive. Attempting to write while protected will cause a read/write check status (see 3.4.2.2).

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FUNCTION	DEVICE BUS IN – IV 072$_8$ (3A)							
	0	1	2	3	4	5	6	7
TAG '0' MACHINE STATUS	RESERVED BY OTHER CHANNEL	INTERFACE CHECK	DRIVE CHECK	READ/WRITE CHECK	ONLINE	ATTENTION	BUSY.	SEEK COMPLETE
READ/WRITE STATUS	ON CYLINDER	INTERFACE CHECK	DRIVE CHECK	READ/WRITE CHECK	ONLINE	ADDRESS FOUND	INDEX MARK	WRITE PROTECTED
TAG '5' TARGET REGSITER		SECTOR 64	SECTOR 32	SECTOR 16	SECTOR 8	SECTOR 4	SECTOR 2	SECTOR 1

	SIZE	CODE IDENT NO.	SPEC. NO.	
Table 5-2. Device Bus In Data Formats For T3282/3/8 Devices	A	51360	SS-600-0056-1A	
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5.11   INTERFACE TIMING

Typical timing for the interface control function for the T3282/3/8 drives is described in the following paragraphs.

5.11.1   Tag Timing

Minimum timing requirements for any tag function will be as shown in Figure 3-7 for the SELECT TAG '0' function. An example of tag and bus timing for a control sequence is shown in Figure 5-2.

5.11.2   Read Timing

The control line associated with a read command is the Read Gate line.

The leading edge of Read Gate forces the phase locked oscillator to synchronize on an all zeros pattern. Read Gate also enables the output of the data separator onto the I/O lines after a lock-to-data internal time out. Read Gate must be dropped and raised again after going through a splice area. Read Gate may be enabled 60 ±4 clock counts after the leading edge of index or sector.

The sync pattern search may begin 88 servo clock counts after the leading edge of Read Gate.

Head switching and read amplifier stabilization (see Figure 5-3) shows the latest acceptable time at which a head can be selected in order to read the next successive sector (with the format described in 6.3).

Read Data line may not have valid data until 9µs from leading edge of Read Gate, due to phase lock synchronizing time.

Ensure that there will be no splice area after Read Gate is brought up even under worst case pack interchange conditions.

5.11.3   Write Data Timing

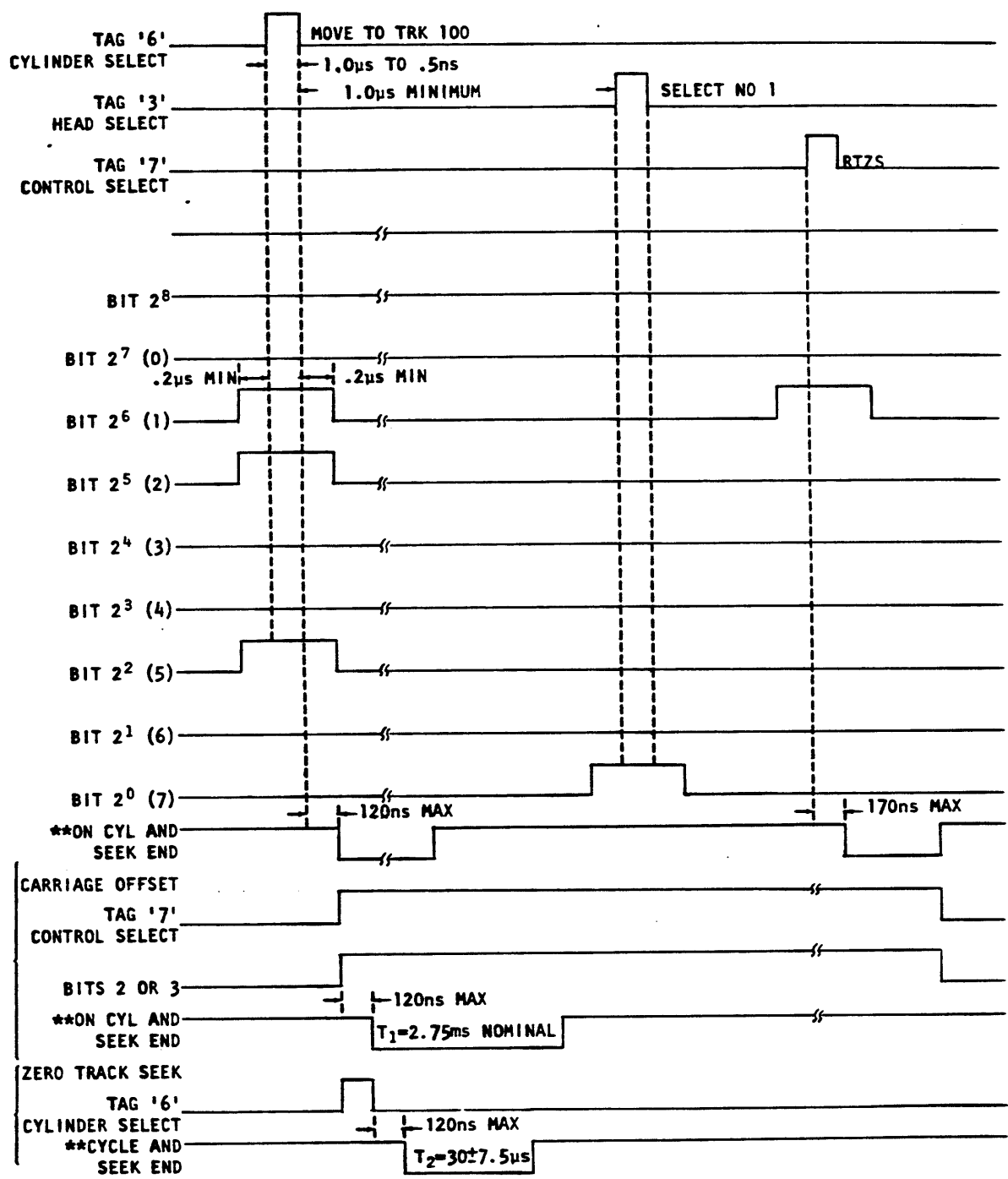The control line associated with a Write operation is Write Gate.

The sector address must always be preceded by writing the PLO sync field and sync pattern.

The Controller must provide a three bit internal delay (approximately 0.3µs) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal (see Figure 5-4). This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit.

Writing the data field must always be followed by writing the checkword and at least an eight-bit pad at the end of the checkword.

During formatting, Write Gate is raised immediately upon sensing index. During a record update, Write Gate is raised within two bits of the last bit of an address.

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TAG '6'
CYLINDER SELECT

MOVE TO TRK 100

← 1.0µs TO .5ns

← 1.0µs MINIMUM

TAG '3'
HEAD SELECT

SELECT NO 1

TAG '7'
CONTROL SELECT

RTZS

BIT 2^8

BIT 2^7 (0)

.2µs MIN → ← .2µs MIN

BIT 2^6 (1)

BIT 2^5 (2)

BIT 2^4 (3)

BIT 2^3 (4)

BIT 2^2 (5)

BIT 2^1 (6)

BIT 2^0 (7)

**ON CYL AND
SEEK END

← 120ns MAX

← 170ns MAX

CARRIAGE OFFSET
TAG '7'
CONTROL SELECT

BITS 2 OR 3

**ON CYL AND
SEEK END

← 120ns MAX

$T_1 = 2.75ms$ NOMINAL

ZERO TRACK SEEK
TAG '6'
CYLINDER SELECT

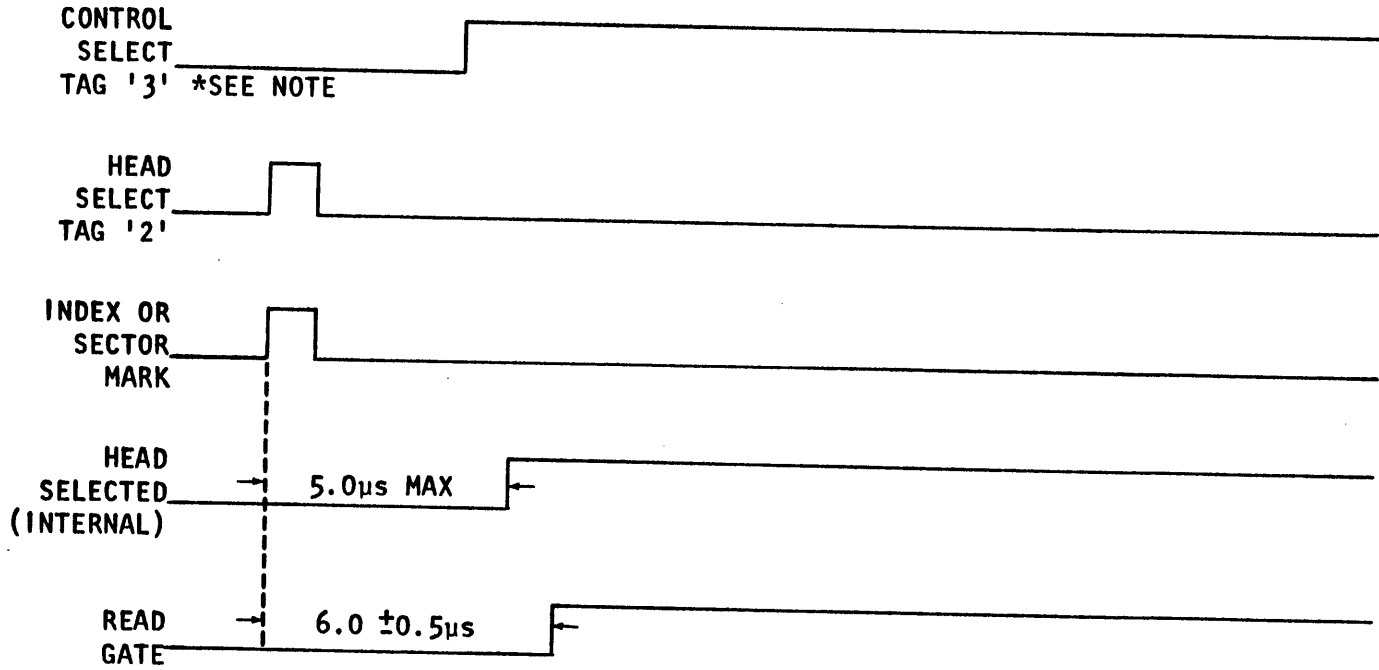**CYCLE AND
SEEK END

← 120ns MAX

$T_2 = 30 \pm 7.5µs$

** ON CYL AND SEEK END SIGNALS ARE IDENTICAL UNLESS SEEK ERROR OCCURS. SEEK ERROR
INITIATES A CONSTANT SEEK END.
TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER.

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Figure 5-2. Tag and Bus Timing T3282/3/8 Drives	**A**	**51360**	SS-600-0056-1A
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Figure 5-3. Typical Read Control Timing

CONTROL
SELECT
TAG '3' *SEE NOTE

HEAD
SELECT
TAG '2'

INDEX OR
SECTOR
MARK

HEAD
SELECTED
(INTERNAL)

5.0μs MAX

READ
GATE

6.0 ±0.5μs

NOTE: READ OPERATION HEAD SELECT MAY NOT OCCUR LATER THAN 6.0μs AFTER INDEX
OR SECTOR.

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CONTROL
SELECT
TAG '3'

WRITE HEAD GAP,
SYNC PATTERN
AND DATA FIELD

READ ADDRESS

READ
GATE

0.3μs
MIN

10μs MIN

WRITE
GATE

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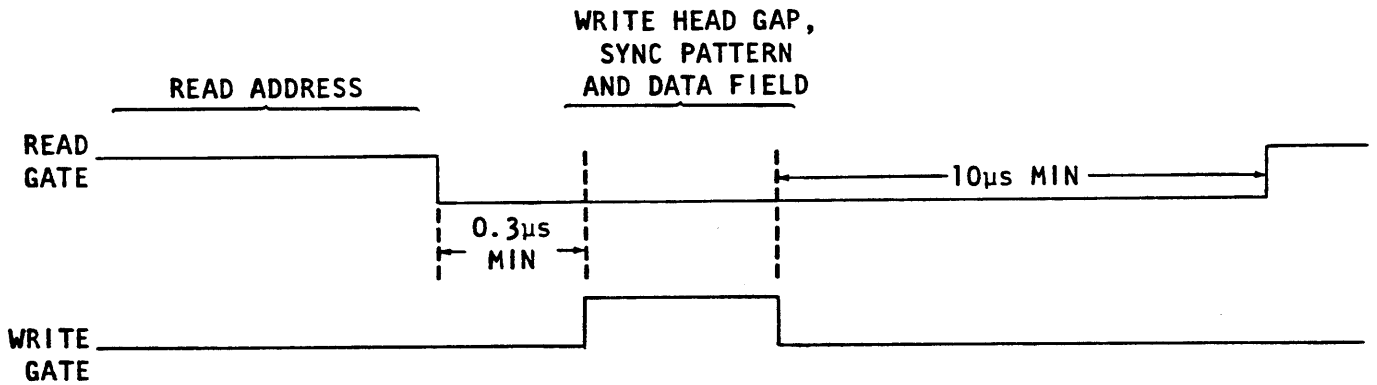
Figure 5-4. Typical Write Control Timing

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Figure 5-4. Typical Timing with Address Mark
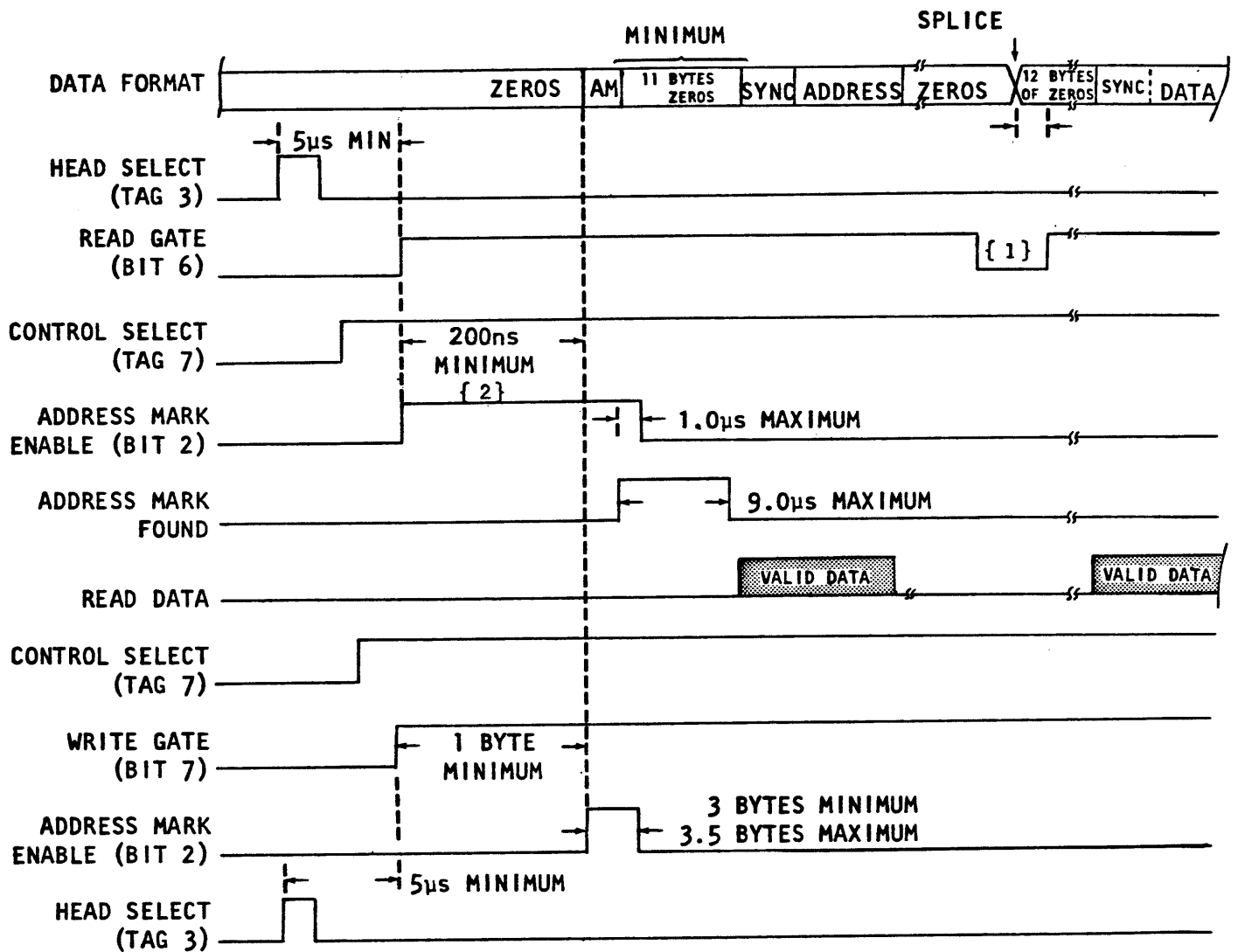
{1} READ GATE MUST BE DROPPED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF ZERO BITS REMAINING IN THE SYNC FIELD. 12 BYTE (EXAMPLE) CONSISTS OF ONE BYTE FOR WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

{2} ADDRESS MARK ENABLE SHOULD OCCUR SIMULTANEOUSLY WITH READ GATE.

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6.0 PHYSICAL

The drive interface circuit cards shown in Figures 3-1 and 3-3 are physically packaged in a small chassis isolated from the main logic chassis in the controller. Signal bussing and interconnection between the cards in the chassis is accomplished via an etched circuit backplane.

Transmission of control and status signals between the main logic chassis and the drive interface chassis is accomplished via mass terminated ribbon cables which plug into both chassis. Transmission of the R/W DATA BUS and PLO BUS signals between the chassis is accomplished via separate balanced shielded 160 ohm transmission lines.

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