Tektronix®

8301
MICROPROCESSOR DEVELOPMENT UNIT

SERVICE

INSTRUCTION MANUAL

Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

8301
MICROPROCESSOR DEVELOPMENT UNIT

SERVICE

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P.O. Box 500
Beaverton, Oregon 97077

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Product Group 61

Serial Number _____

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PREFACE

RELATIONSHIP TO OTHER EQUIPMENT

The 8301 Microprocessor Development Unit (MDU), when operated with the 8501 Data Management Unit (DMU), comprises a system designates as the 8550 Microcomputer Development Lab (MDL). A description of this system is contained in the 8550 Microcomputer Development Lab Installation Guide. Specific information on the 8501 DMU is contained in the 8501 Data Management Unit Service Manual.

ABOUT THIS REVISION

This revision to the service manual reflects changes due to the updated operating system for the 8550 Microcomputer Development Lab (DOS 50 V2.x) and general improvements to the manual since the original printing in April 1981. Generally the changes are as follows:

1. Replaces the system memory board (System/Program Memory board) with a new System RAM board.

2. Changes the nomenclature of the System/Program Memory board to Program Memory board.

3. All new 8301 units leaving the factory and some updated 8301 units in the field have installed the latest versions of the Power-Up ROM and the Boot ROM: V2.x. Therefore, this manual is revised to include both versions of each ROM: V1.x and V2.x.

4. The power-up diagnostic tests for V2.x are drastically changed from those of V1.x. Section 3, Power-up Diagnostics, of this manual is revised to reflect these changes. This section is divided into three parts:

   - Part 1 describes the V1.x power-up diagnostic tests.
   - Part 2 describes the V2.x power-up diagnostic tests.
   - Part 3 describes the Critical Function Monitor (CFM) for both versions.

5. The memory diagnostics defined in Section 4, Disc-Based Diagnostics, of this manual are changed in this revision to include additional system and program memory testing as follows:

   - System Memory -- from 32K to 64K
   - Program Memory -- from 64k to 256K

6. I/O port specifications are added to Section 6, Specifications, of this manual.

7. The data byte information for I/O port addresses was moved from Section 6 to Section 7, Technical Reference Material, of this manual.

8. Circuit description for the System RAM board is added as Section 16, System RAM Board, of this manual. The schematic diagrams for the System RAM board are added to Section 18, Diagrams, of this manual as diagram numbers 24 through 27.

MANUAL APPLICATION

This service manual describes the functions of the 8301 MDU basic circuit boards in sufficient detail to permit service technicians to perform on-site (board-level) repairs and limited field service center (component-level) repairs to the circuit boards.

ABOUT THIS MANUAL

This Manual introduces you to the software and hardware components of the 8301 MDU. In addition, this Manual describes (on a block diagram level) the operation of the hardware within the 8301. This Manual is organized into 18 sections. A brief description of each section follows:

Section 1 — This section contains general information and an introduction to the 8301 MDU.

Section 2 — Installation information is provided in this section, along with strap and jumper options for each circuit board.

Section 3 — This section is divided into three parts. Parts 1 and 2 contain descriptions of each Power-Up Diagnostic Test for Diagnostic ROM V1.x and V2.x, respectively. Part 3 describes how the tests can be used to isolate problems if any diagnostic test fails to execute properly.

Section 4 This section contains a description of each Disc-Based Diagnostic Test. It also describes how the tests can be used to isolate hardware failures if any diagnostic test fails to execute properly.

Section 5 This section describes the effects of software on hardware functions, using modified flow diagrams.

Section 6 This section contains specifications for the 8301 MDU.

Section 7 This section contains technical reference material.

Section 8 This section contains maintenance information, disassembly instructions, and calibration procedures.

Section 9 This section describes the System Controller board.

Section 10 This section describes the Communications Interface board.

Section 11 This section describes the Program Memory board.

Section 12 This section describes the Emulator Controller board.

Section 13 This section describes the Language Processor board.

Section 14 This section describes the Front Panel board.

Section 15 This section describes the Power Supplies.

Section 16 This section describes the System RAM board.

Section 17 This section contains the 8301 Replaceable Electrical Parts list.

Section 18 This section contains the 8301 Schematic Diagrams.

Section 19 This section contains the Replaceable Mechanical Parts list.

MANUAL CONVENTIONS

DMU

Throughout this manual, the term "Data Management Unit" (or "DMU") is used to specify a disc storage unit. When the 8301 is a part of the 8550 MDL, the term "DMU" refers specifically to the 8501 DMU.

SIGNAL LINE CONVENTIONS

The text and schematic drawings throughout this manual uses a high/low convention to describe the asserted state of all signal lines. The asserted (true) state of each signal line is shown as (L) for low or (H) for high, immediately following the signal line name as follows:

- SLVOPREQ(L)
- CMEM(H)
- M(L)/IO(H)

SLASHED ZEROS

Throughout the text in this manual, zeros are not slashed.

HEXADECIMAL NOTATION

All address references in this manual are represented by hexadecimal numbers. The contents of 8-bit registers and data buses are also represented by hexadecimal numbers. Exceptions are made in some instances when binary values are noted.

CHANGE INFORMATION

Change notices are issued by Tektronix, Inc. to document changes in the manual after it has been published. Change information is located in the back of this manual, following the yellow tab marked "CHANGE INFORMATION & TEST EQUIPMENT". When you receive this manual, enter any change information into the body of the manual, as indicated on the change notice.

REVISION HISTORY

As this manual is revised and reprinted, revision history information is included in the text and diagrams. Original manual pages are indicated by the "@" symbol at the bottom inside corner of the page. Existing pages of manuals that have been revised are indicated by a revision code and date (REV A AUG 1981) in place of the "@" symbol. New pages added to an existing section (whether they contain old, new, or revised information) contain the "@" symbol alongside the revision date (@ AUG 1981).

OPERATIONAL AND INSTALLATION INFORMATION

A minimum of operational and installation information is presented in this manual. Refer to the 8550 MDL System Users Guide for information regarding operating procedures. Refer to the 8550 MDL Installation Guide for information regarding system installation and initial start-up procedures.

OPTIONS

Options for the 8550 MDL are documented by individual manuals. See the Tektronix Products catalog or contact your local Tektronix Field Office or representative for a list of available options.

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

As Marked on Equipment


DANGER high voltage.


Protective ground (earth) terminal.


ATTENTION - Refer to manual.

SAFETY PRECAUTIONS

GROUNDING THE 8301 MDU

The 8301 Microprocessor Development Unit is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the equipment's power input terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your 8301.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

USE THE PROPER FUSE

To avoid fire hazard, use only the fuse specified in the parts list for your 8301. Be sure the fuse is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate the 8301 MDU in an atmosphere of explosive gases.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not remove covers or panels from the 8301 MDU. Do not operate the 8301 without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

(Refer also to the preceding Operators Safety Summary)

DO NOT SERVICE ALONE

Do not perform internal service or adjustment on the 8301 MDU unless another person capable of rendering first aid and resuscitation is present.

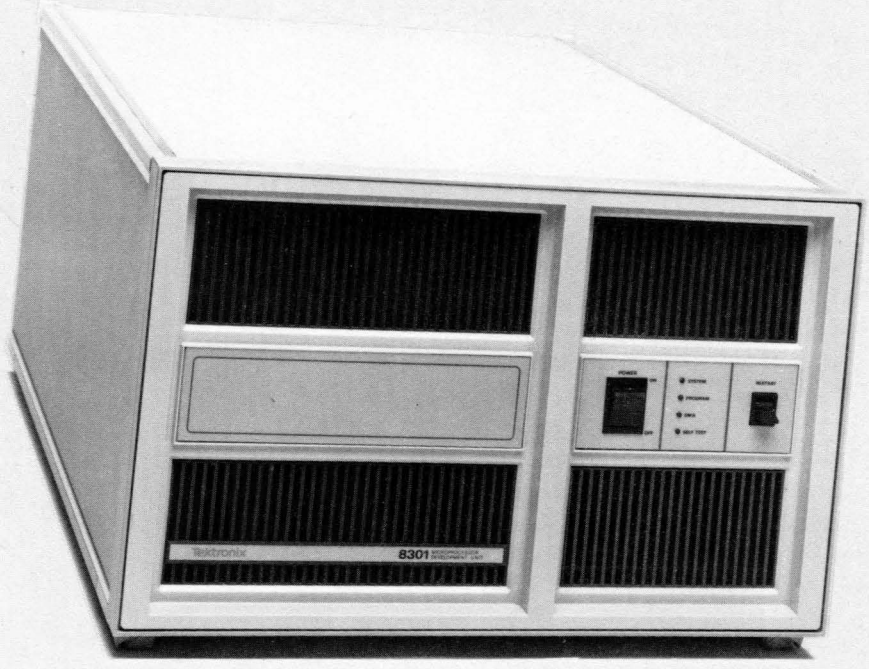
USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in the 8301. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

POWER SOURCE

The 8301 is designed to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



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8301 Microprocessor Development Unit

Section 1

GENERAL INFORMATION

INTRODUCTION TO THE 8301

The 8301 Microprocessor Development Unit (MDU) is a design aid for microprocessor-based product development. It is intended primarily to support software engineers and logic design engineers involved in prototype design of microprocessor-based systems. During the software/hardware integration phase of prototype design, in-circuit emulation of prototype hardware for selected microprocessors enable both software and hardware engineers to debug prototype programs and hardware.

FEATURES OF THE 8301

The basic structure and capabilities of the 8301 are similar to those of a general purpose minicomputer system, but with the following important additional features:

- Access to high-volume bulk storage on flexible and/or hard discs when operating with a compatible Data Management Unit (DMU).
- Extended addressing for 16-bit processors.
- In-circuit emulation of prototype hardware for selected microprocessors. This permits debugging of prototype hardware in an actual hardware environment.
- Universality or adaptability: by adding circuit boards, new processors can be supported as technology advances. Within the 8301, universality is achieved by separating application-independent (8301-related) tasks from the dependent (prototype-related) tasks.

EMULATION

Optional emulation packages are provided for selected microprocessors. An emulation package usually consists of:

- An emulator processor: a circuit board (or boards) for installation within the 8301 unit.
- A prototype control probe with connecting cables. Each emulator processor has its own unique prototype control probe. (Some emulator processors support two or more prototype control probes.)

- A software support package also unique to the associated emulator processor.

Most emulator processors support three emulation modes:

Mode 0 — Prototype program (software) development within the 8301.

Mode 1 — Prototype software/hardware development, utilizing the 8301 and/or prototype memories, with I/O (input/output) functions and clock provided by the prototype.

Mode 2 — Prototype software/hardware development utilizing the prototype memory, I/O, and clock.

By selecting the emulation mode, users can choose an environment tailored to their needs. The design engineers can proceed through prototype design phases in an orderly, effective manner. The software engineer can debug the prototype program within the known environment of the 8301. The software and hardware engineers can then integrate the software program with the prototype hardware. Software and hardware failures can be isolated and comprehensive testing of the developed product is possible.

MODE 0

Emulation mode 0 is used primarily by software designers and evaluators in debugging prototype programs. In mode 0, the prototype program utilizes the 8301 memory, clock, and I/O functions. The program is executed under full control of the active emulator processor within the 8301. As such, all debugging features of the 8301 software operating system may be fully utilized.

For most emulators , the prototype control probe may optionally be attached to the prototype hardware. The probe usually has no function in mode 0. The advantage of this mode is the capability to develop and debug prototype programs concurrent with, or prior to, hardware development.

MODE 1

In emulation modes 1 or 2, the microprocessor device is removed from its prototype socket and is replaced by the active emulator processor's prototype control probe. This arrangement gives the active emulator processor in the 8301 full debug capabilities and control over the prototype system.

In emulation mode 1, the first steps of in-circuit emulation occur: the prototype program (software) is integrated with the prototype system (hardware). The memory mapping capabilities of the 8301 may be used to map (transfer) various portions of a prototype program to the prototype's memory for integration with the prototype hardware. Any portion or all of the prototype program located in 8301 memory may be mapped and moved to the prototype memory. When all of the prototype program is mapped and moved to the prototype's memory, the program executes entirely within prototype hardware. The prototype clock and I/O functions are used in mode 1 to

control execution of the prototype program in either 8301 memory or prototype memory. Overall control and debugging functions are still retained by the active emulator processor within the 8301.

MODE 2

In this mode, the prototype program is contained entirely within the prototype's memory. The prototype clock and I/O functions control program execution, while the active emulator in the 8301 retains overall control of the prototype. The prototype control probe is connected to the prototype's microprocessor socket during this emulation mode.

Mode 2 is generally used in the final software/hardware integration phases of prototype system design, or in troubleshooting hardware systems when the software program is known to be operating properly.

SOFTWARE SUPPORT

The 8301 Microprocessor Development Unit (MDU) is supplied with a standard software package that includes:

- An operating system on flexible disc that provides a comprehensive system monitor, disc file manager, and text editor. The flexible disc operates in a compatible Data Management Unit (DMU).
- Comprehensive debugging software for breakpoint detection, program tracking, program stepping and processor control.
- Diagnostic tests detect the cause of equipment failure. Power-up tests are located in ROM. Additional tests are located on disc.

The 8301's software operating system is contained on a system disc. The assembler and debug software are provided with each emulator processor supported by the system. The following paragraphs discuss the various software components: operating system, text editor, assembler, and debug.

The operating system provides operational control of all portions of the prototype development system. It includes the monitoring and control functions relating to file handling , loading, and execution. The operating system command file capability enables the user to create customized operating commands. The operating system software permits the user to accomplish the following tasks:

- Create, edit, and assemble files.
- Obtain listed object file outputs.
- Execute programs.
- Check programs (through the debug system).

A 2K-byte ROM bootstraps the operating system monitor from the system disc into the 32K RAM of system memory. The operating system monitor then interfaces all succeeding commands with the disc. The operating systems flexible input/output capabilities enables the user to assign any logical channel to any peripheral device or file within the system. In this way, system I/O devices may be dynamically assigned, using operating system commands from the System Terminal or from the user's program. The user may write a driver routine for other peripheral devices and link them with the operating system.

The text editor is a software package that allows the user to enter and modify test files. It is line-oriented and accepts input from a terminal or a disc file. The text editor performs modifications in a workspace and outputs the revised text to the disc file.

The resident assembler translates symbolic assembly language instructions into the corresponding machine language. It generates absolute object code in hexadecimal format. The output code is loaded into the system for direct execution.

The debug software provides the user with program debugging capabilities within both a software and hardware environment. Special hardware programs, built into the development system, are used to control execution of the user's program. When the debug system is active, user programs have dynamic program trace, breakpoint, and memory modification capabilities. Status reporting on memory, program, and processor is also provided.

8301 ARCHITECTURE

Figure 1-1 is an overall functional block diagram of the 8301. Refer to Fig. 1-1 as you read the following paragraphs.

The 8301 is designed around a dual-processor concept: system (master) and program (slave) CPUs. The system CPU, a 2650A-1 microprocessor, is referred to in this manual as the system processor and is located on the System Controller circuit board. The system processor runs the operating system and text editor, in addition to performing all interactions with system I/O devices. The program CPU (emulator processor) runs user programs and interfaces with the prototype microprocessor-based system.

The dual-processor architecture permits the system to support different emulator processors with the same operating system software. Hardware provisions in the 8301 support emulator processors with up to 16-bit word length. The standard 8301 program memory is 32K bytes but may be expanded to 64K bytes.

Interaction between the system processor and the emulator processor is controlled by the Emulator Controller board, under the direction of the system processor. Both the system and the emulator processors share the basic bus structure; only one processor may be active at any one time.

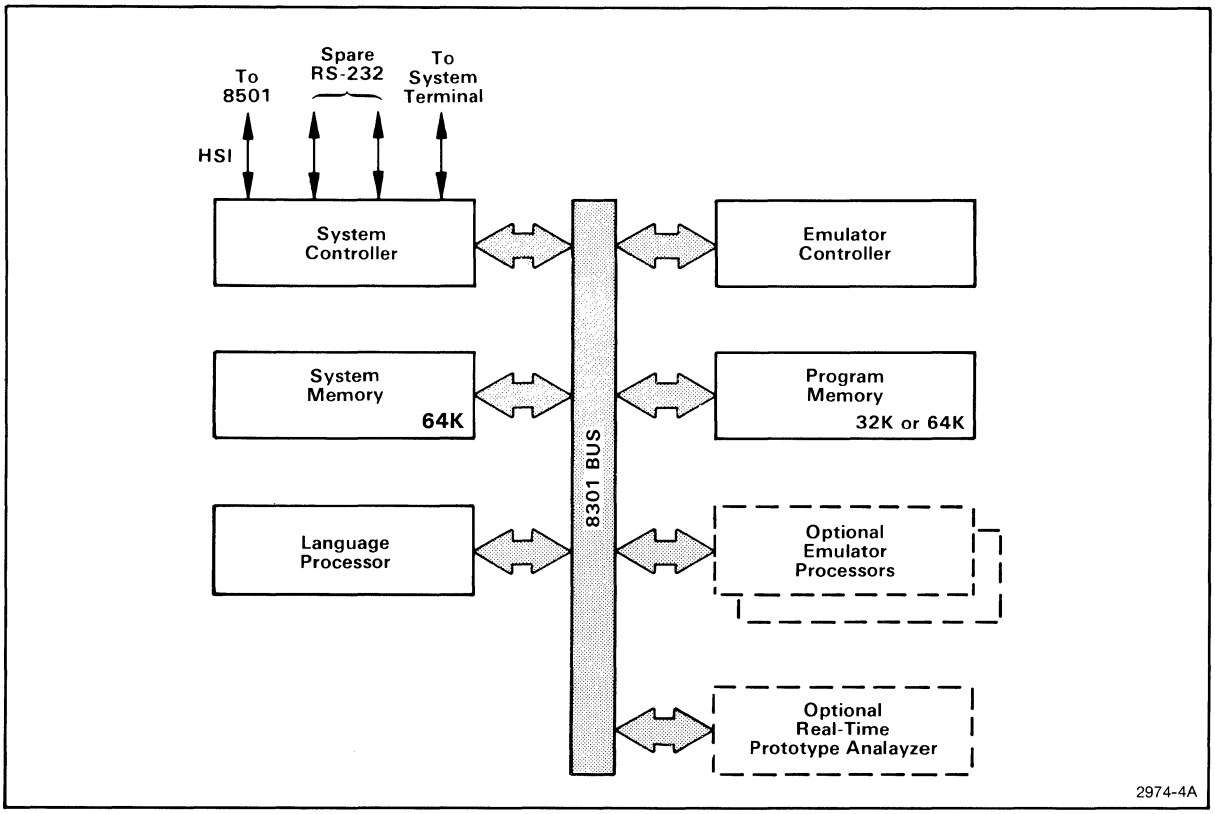


Fig. 1-1. 8301 MDU functional block diagram.

The 8301 is designed to operate with a high-volume bulk storage unit. Data is passed between the two units via a high-speed serial interface (HSI). The interface operates at 153.6k baud and is compatible with RS-422 specifications.

Circuit boards within the 8301 plug into card slot connectors attached to the Main Interconnect board. The Main Interconnect board contains the system bus structure for the entire unit. It provides address and data bus lines, as well as the control and power supply lines for each circuit board. The Emulator Controller separates the bus structure into two sections; a system section and a program section. Each circuit boards is assigned to these sections, as follows: (Figure 1-2 shows a recommended arrangement for the circuit boards in the 8301.)

System Section

- System Controller
- System RAM

Program Section

- Language Processor
- Program Memory (32K)
- Program Memory (32K) (optional)
- Emulator Processor (optional)
- Emulator Processor (optional)
- Real-Time Prototype Analyzer (RTPA) (optional)

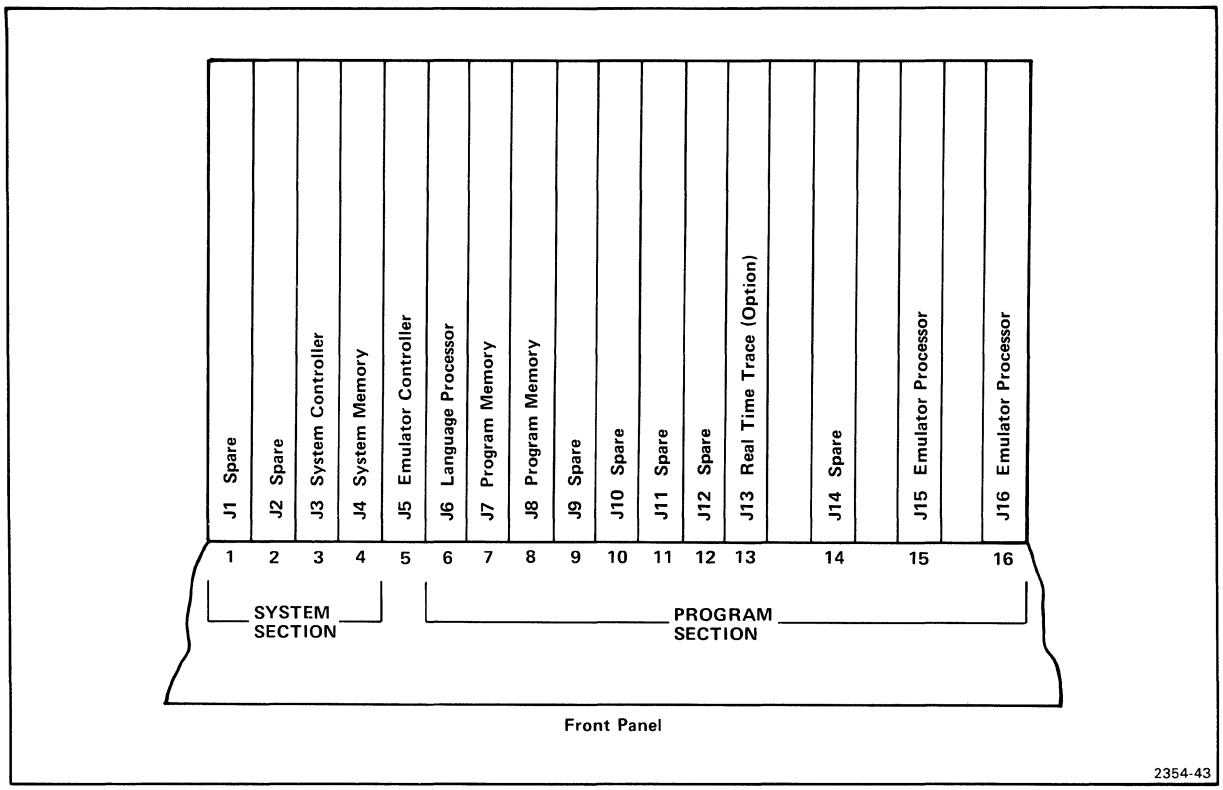


Fig. 1-2. Recommended circuit board arrangement.

8301 CONFIGURATION

The basic 8301 configuration contains the following elements:

- Mechanical Package
  - Mainframe
- Power Supplies
- Front Control Panel — Front Panel board
- System Bus
  - Main Interconnect board
- System Section
  - System Controller board
  - Communications Interface board
  - System RAM board
- Emulator Controller board
- Program Section
  - Program Memory (32K) board
  - Language Processor board

The remainder of this section briefly discusses each of these elements in turn.

MECHANICAL PACKAGE

The mechanical package consists of a mainframe, mounting hardware, and covers that house the 8301. Three power supplies are located across the lower rear portion of the mainframe. The system bus on the Main Interconnect board is located in the lower front half of the mainframe. The plug-in circuit boards are mounted upright, from left to right, across the front of the mainframe. The circuit boards are plugged into edge connectors installed on the Main Interconnect board. Ventilation is provided by two circulation fans that pull air from the front of the unit through the circuit board compartment across the power supplies and out the rear of the unit.

POWER SUPPLIES

Three power supplies (+5 Vdc, +12 Vdc, and - 12 Vdc) are located in the lower rear portion of the 8301 mainframe. The three supplies provide the following dc output voltages and currents:

+5.2 Vdc +1%/-2% at 35.0 A
+12.0 Vdc +/- 5% at 1.7 A
-12.0 Vdc +/- 5% at 1.7 A

The three supplies are connected to the system bus structure in the Main Interconnect board and furnish primary power to the plug-in circuit boards. The three power supplies operate from the primary ac voltage input supply.

FRONT CONTROL PANEL CONTROLS AND INDICATORS

Figure 1-3 shows the 8301 Front Control Panel controls and indicators. The following description of controls and indicators is keyed to the circled numbers in Fig. 1-3.

1. RESTART
   When this momentary-contact switch is toggled all the logic circuits are initialized.

2. SELF TEST
   This indicator is lit when the power-up test routines are in operation, or if an error is detected in a power-up routine.

3. DMA
   This indicator is lit when a direct memory access (DMA) operation is occurring.

4. POWER switch ON---OFF
   This is the main ac power switch.

5. PROGRAM
   This indicator is lit when the emulator processor is running.

6. SYSTEM
   This indicator is lit when the system processor is running.

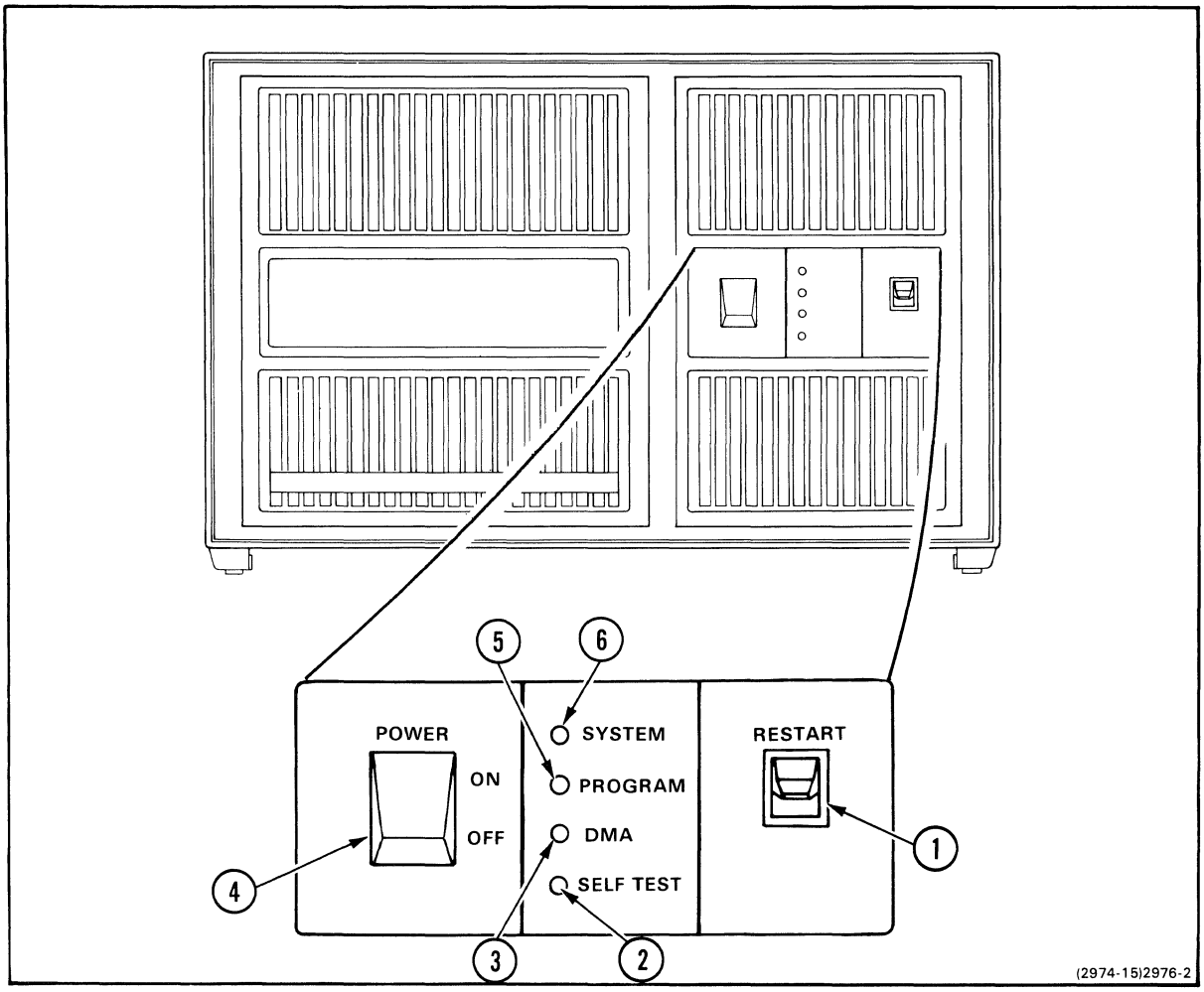


Fig. 1-3. 8301 MDU front panel controls and indicators.

FRONT PANEL BOARD

The Front Panel board is located directly behind the Front Control Panel. The RESTART switch and four LEDs are mounted on the Front Panel board and extend through the Front Control Panel.

SYSTEM BUS STRUCTURE

The system bus is a 100-line bus structure that provides most of the connections to the plug-in circuit boards in the 8301. The bus structure is shown in Fig. 1-4. The Emulator Controller board separates those control and signal lines that are dedicated either to the system section or to the program section. Note in Fig. 1-4 that most power, ground, bus, and control lines are common to all system and program section circuit boards. The Main Interconnect board contains the 8301 system bus, and can accommodate up to 16 circuit boards. Bus assignments for the 100-line system bus (including line number, line name, and description) are listed in section 7, Technical Reference Material in this manual.

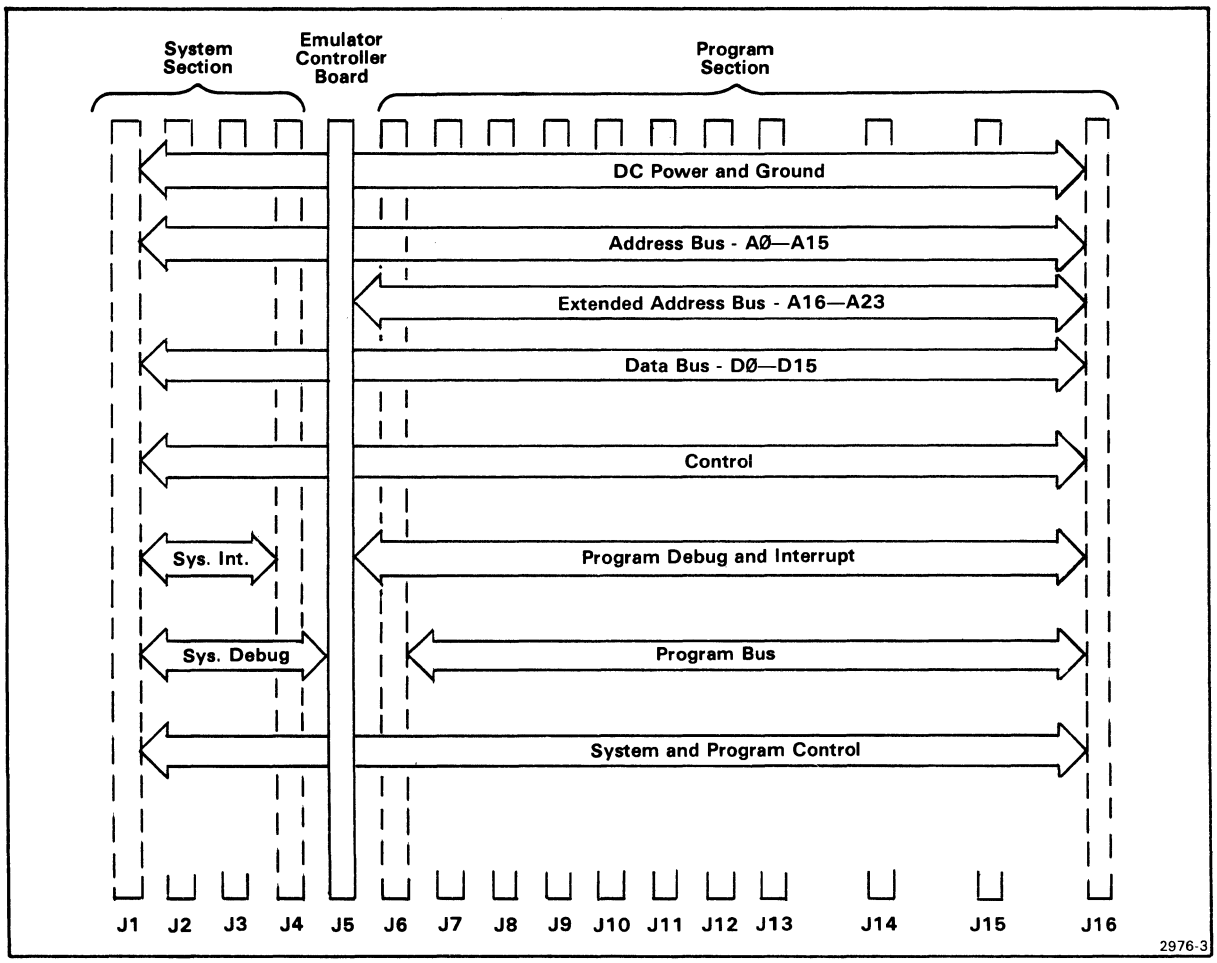


Fig. 1-4. System bus structure.

MAIN INTERCONNECT BOARD

The Main Interconnect board contains the 100-line system bus structure that is common to all plug-in circuit boards. Refer to the Diagrams Section of this manual for a line drawing of the main interconnect board.

SYSTEM SECTION

SYSTEM CONTROLLER BOARD

The System Controller board is the controlling element of the 8301. This board contains the system processor (master) (a 2650A-1 microprocessor),which provides primary control over the circuit boards in the 8301. The System Controller permits memory mapping and write protect assignments to be made to either the 8301 program memory or the prototype memory. The System Controller board encodes 16 interrupts and services up to 32 interrupts. Sixteen of these interrupts are from the other circuit boards in the 8301. The system processor communicates with the other circuit boards in the 8301 through the use of I/O port interfaces.

COMMUNICATIONS INTERFACE BOARD

The Communications Interface board is an extension of the System Controller board. It contains the baud rate generator, three RS-232-C compatible interfaces for peripheral equipment, and one RS-422 compatible interface for a Data Management Unit (mass storage device).

SYSTEM RAM BOARD

The System RAM board is a 64K dynamic RAM. The System RAM board is used to store the 8550 operating system, which is booted from a disc in the DMU. The System RAM is restricted to operating on the system side of the Emulator Controller in the Main Interconnect board.

EMULATOR CONTROLLER BOARD

The Emulator Controller board ensures that only one processor (either the system processor, emulator processor, or language processor) has control of the system buses at any time. Since all the system and program circuit boards share the same address bus, data bus, and part of the control lines, bus contention could become a problem without the Emulator Controller board. In addition to separating the system and program boards, this board controls debugging operations. The Emulator Controller contains the breakpoint registers, forced jump registers, and program counter registers used during debugging operations. Breakpoint addresses are stored in these registers and compared to the addresses placed on the system address bus by the emulator processor. If the addresses match, the Emulator Controller informs the

system controller. The Emulator Controller is under direct control of the system controller.

PROGRAM SECTION

PROGRAM MEMORY (32K) BOARD

The Program Memory board is a 32K static RAM. This memory is used to store the user or prototype programs. A second 32K memory board may be added to the program memory as an option, for a total of 64K. When both boards are present a jumper on each board selects low (0---32K) or high (32K---64K) memory.

LANGUAGE PROCESSOR BOARD

The Language Processor operates much like an emulator processor. Program memory is used by the Language Processor to translate source code (assembly language) to binary object code (machine language) for the emulator processor. The Language Processor utilizes a Z80A microprocessor and operates as a slave to the system processor. The Language Processor is invoked by software commands entered at the System Terminal.

Section 2

INSTALLATION

INTRODUCTION

This section contains the installation procedure for the 8301 Microprocessor Development Unit (MDU). The installation procedure describes the standard components of an 8301 and explains how these components must be configured for normal operation. Optional components are not described within this section. The installation procedure for each option is detailed within the service manual for that option.

This section contains only a minimum of operating information. For more information on how to operate the 8301, refer to your System Users Manual.

This section is divided into the following parts:

- Site Selection
- Unpacking and Inspection
- Removing the Top Cover
- Removing the Circuit Board Restrainer
- Internal Cables
- The Main Interconnect Board
- Jumpers and Straps
- The Circuit Breaker
- System Controller Board Configuration
- Emulator Controller Board Configuration
- Language Processor Board Configuration
- System and Program Memory Board Configuration
- Communications Interface Board Configuration
- Installing a Circuit Board
- Connecting a Prototype Control Probe
- Replacing the Top Cover

- Rear Panel Connectors
- Storage and Reshipping

SITE SELECTION

The area selected should be adequately lighted, air-conditioned, and dust-free. This area should also have a minimum of electrostatic and electromagnetic interference to prevent degradation of system performance.

General requirements for operating space and access are shown in Fig. 2-1. While rack mounting is an option, the rearward sliding top cover may be more of a consideration there, as normally the unit can be swiveled on the bench in bench-top configurations. Here are some other considerations:

- Access is required to the front, rear, and top of the unit.
- Allow for adequate air exhaust at the rear (6" minimum recommended).
- When placing this unit on a bench, position the unit so that its air intake will not draw hot exhaust air from an adjacent unit.
- Arrange the power and communications cables at the rear of the instrument in such a manner that these cables contact one another as little as possible.

Refer to your System Installation Guide for total system planning.

UNPACKING AND INSPECTION

The 8301 is packaged and shipped in a heavy-duty cardboard container. The unit is adequately protected from most types of transit abuse, being surrounded on all sides by a minimum of three inches of pre-formed expanded polystyrene end pieces.

Before unpacking the 8301, inspect the external carton. If damage is apparent:

- Immediately notify the carrier that made delivery, and request inspection.
- Contact the nearest Tektronix field engineering office or sales representative.
- DO NOT THROW AWAY THE BOXES.
- DO NOT TRY TO REPAIR THE INSTRUMENT.

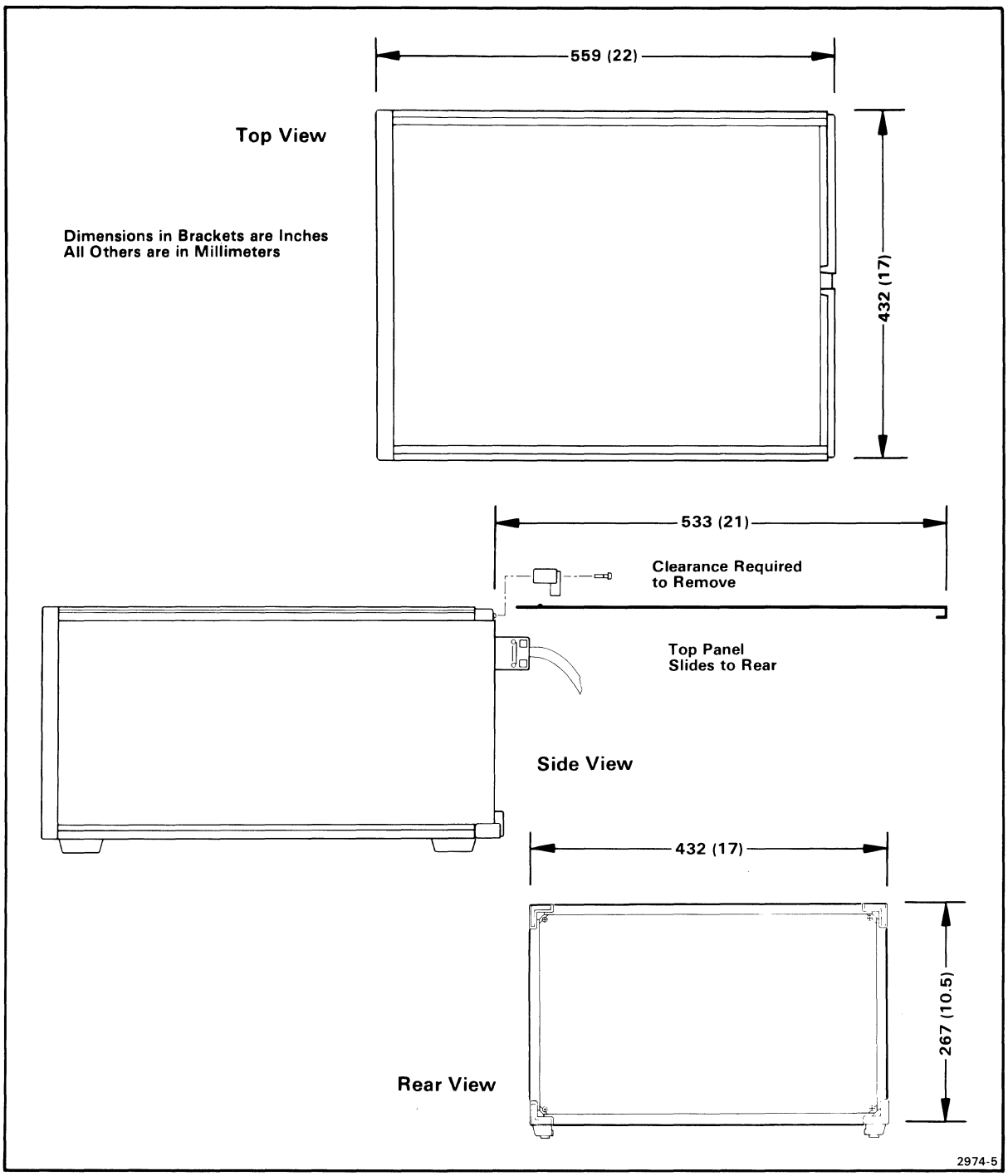


Fig. 2-1. 8301 Space Requirements.

A recessed area within each container holds all cables and standard accessories. These items are taped down and then overlaid with foam padding. Accompanying manuals are normally shipped at the same time as the 8301, but in a separate padded container. Both the 8301 and the manual packages are protected by plastic wrappers from moderate exposures to corrosive environments.

To remove the 8301 from its carton, cut the masking tape and lay the carton on either of its two largest sides. The carton can then be slid off, exposing the inner packing. Take care when removing this packing material, as cables and other accessories may be beneath the unit.

NOTE

Save all packing material for later storage or reshipping of the 8301.

REMOVING THE TOP COVER

The top cover of the 8301 is a flat metal sheet with a small flange angled downward as its rear edge. This cover is designed to fit into two grooves in the top inside edges of the instrument's two side panels. When in place, the top cover is secured by two plastic cover retainers. Each cover retainer is attached by a screw to the top corners of the rear panel. To remove the top cover, simply remove these two screws and remove the cover retainers; then slide the top cover to the rear of the instrument and free of the chassis.

REMOVING THE CIRCUIT BOARD RESTRAINER

A cardboard and foam circuit board restrainer is located directly beneath the top cover of the 8301. This restrainer is designed to protect the circuit boards from damage during transit and must be removed before power is applied to the instrument. Save the restrainers with the packing material for later reshipment of the 8301.

CAUTION

Condensation may form inside the chassis of the 8301 during transit through higher altitudes or varied climatic changes. Before operating the 8301, be certain that moisture has not collected within the instrument.

MAIN INTERCONNECT BOARD

The main interconnect board is attached to the bottom panel of the 8301 and is exposed only when the top cover and circuit board restrainer have been removed. The main interconnect board consists of sixteen 100-pin sockets that accommodate the edge connectors of the 8301 standard and optional circuit boards. Figure 2-2 illustrates the Main Interconnect board and shows how the circuit boards should be configured.

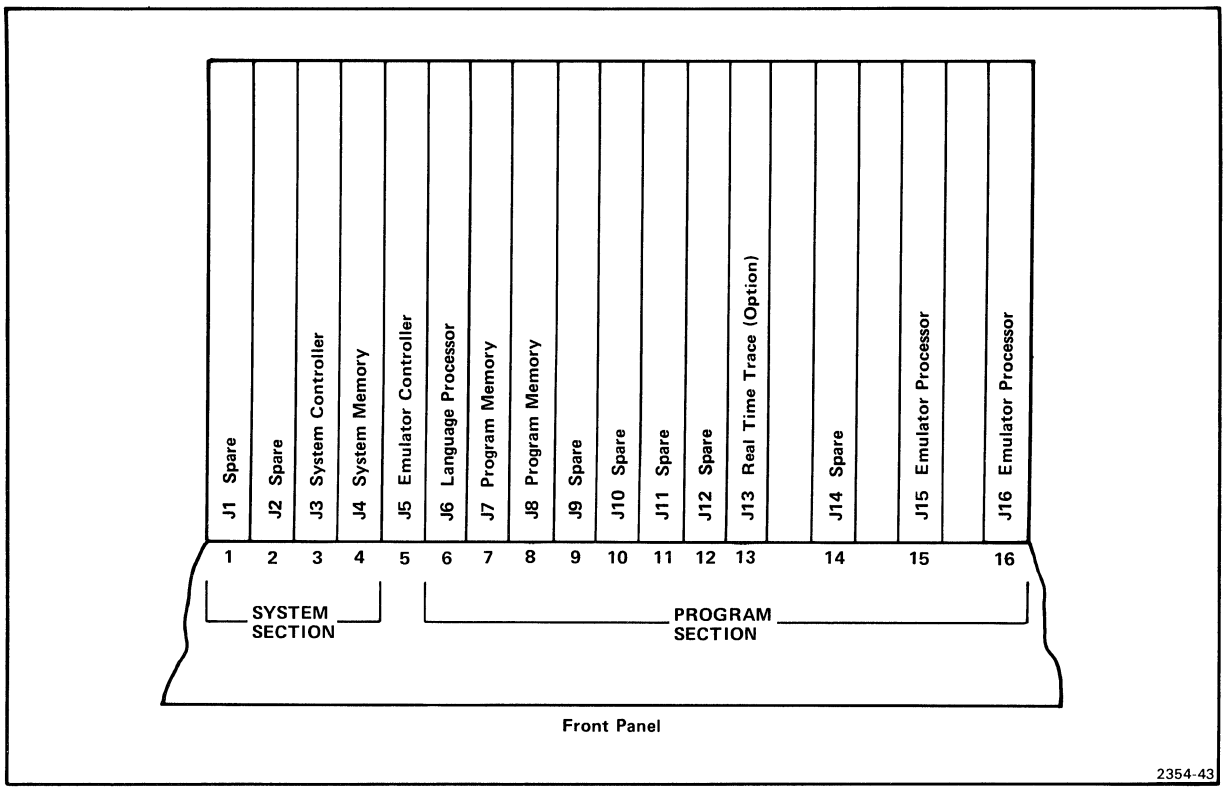


Fig. 2-2. Main Interconnect Board.

INTERNAL CABLES

The 8301 has two internal cables. A 16-line cable connects the front panel to the Main Interconnect board. A 40-line ribbon cable connects the System Controller board to the Communications Interface board. Before applying power to your 8301, verify that both cables are correctly connected, as follows:

- The 16-line cable should run between a 16-pin connector (J1) near

the bottom edge of the Front Panel circuit board and a second 16-pin connector (J17) on the edge of the Main Interconnect board that is nearest the front panel. Make sure that pin 1 of each of the cable's connectors is aligned with pin 1 of the connectors on each circuit board.

- The 40-line ribbon cable should run between a 40-pin edge connector on top of the System Controller board (the edge connector nearest the front panel) and the 40-pin edge connector on the Communications Interface board. Make sure that pin 1 of each of the cable's connectors is aligned with pin 1 of the connectors on each circuit board.

CIRCUIT BREAKER

There is a circuit breaker (S200) connected to the power supply of the 8301. A switch for this circuit breaker is located beneath a cover plate towards the rear of the instrument. This switch must be "ON" during normal operation. If activated, the circuit breaker will trip and the switch will be placed in the "OFF" position.

To gain access to the circuit breaker switch, remove the four screws on the power supply cover plate. Always replace this cover plate, when you have finished checking or resetting this circuit breaker.

JUMPERS AND STRAPS

The standard circuit boards for the 8301 are configured with certain jumpers and straps. The specific function of each jumper or strap is described with its associated circuit board. The following paragraphs describe the kinds of jumpers and straps that are used on the standard circuit boards and explain how these connectors can select alternate functions.

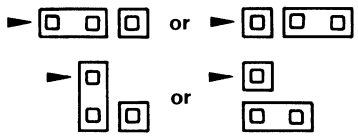
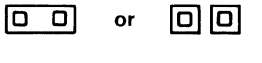
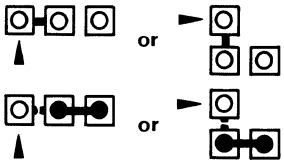
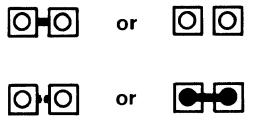
JUMPERS

In this manual, the term "jumper" refers to a small connector designed to fit across a jumper position. A "jumper position" consists of two square pins that can accommodate the placement of the jumper. Jumper positions are arranged on the circuit boards as single-position or two-position jumpers. Single-position jumpers have only two square pins, the jumper is either installed or removed. Two-position jumpers have three square pins, arranged in a straight line or "L" pattern. The jumpers may be installed on pins 1 and 2, 2 and 3, or removed. Table 2-1 shows the symbols used for jumpers in the circuit board configuration drawings that appear later in this section. Jumpers are designated with a "J".

STRAPS

In this manual, the term "strap" refers to an ECB through-hole that may be bridged with a soldered wire to select an alternate function. A strap is also associated with a "cuttable run". That is, an ECB run between two through-holes is a strap. The run must be cut before one of the through-holes can be strapped to a third through-hole. If there is a cuttable run at the location, it must be cut before the strap is bridged, to prevent system errors. Table 2-1 shows the symbols used for straps in the circuit board configuration drawings that appear later in this section. Straps are designated with a "W".

Table 2-1
Symbols for Jumpers and Straps
Used on Circuit Board Configuration Drawings

Jumper/Strap Symbols	Usage
	These two-position jumpers show the jumper across pins 1 and 2 or across pins 2 and 3.
	This single-position jumper shows the jumper across the single jumper position or the jumper removed.
	These two-position straps show the cuttable runs between pins 1 and 2. The runs may be cut and the straps bridged across pins 2 and 3.
	These single-position straps show the through-holes with or without a cuttable run. The cuttable run may be cut or the through-holes may be bridged with a strap.

SYSTEM CONTROLLER BOARD CONFIGURATION

Figure 2-3 shows the locations of jumpers and straps on the System Controller board and the type of connector at each location. There are three jumpers and eight straps on the System Controller board. In addition, Fig. 2-3 shows the locations of a DIP switch (S1100) and LEDs associated with ROM-Based Diagnostics. Table 2-2 lists the configuration required for normal operation.

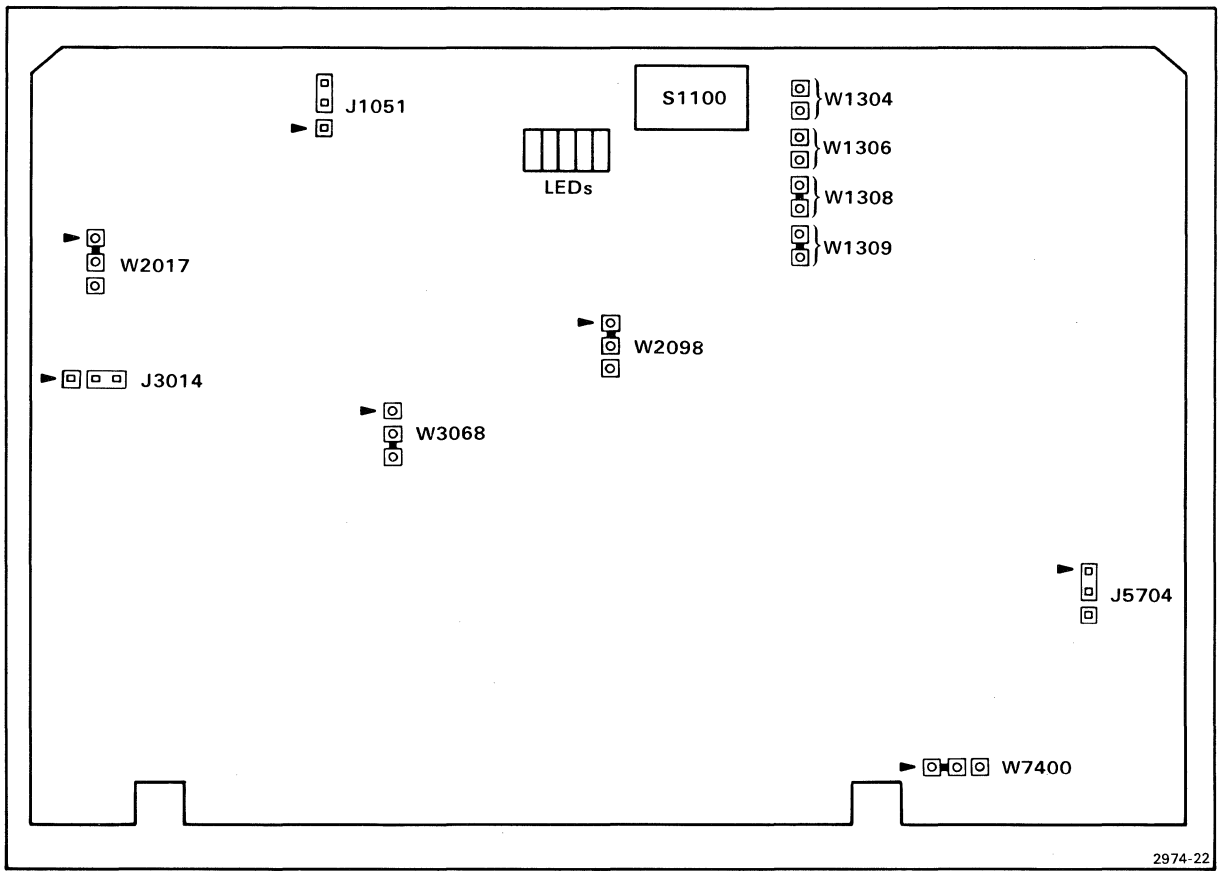


Fig. 2-3. System Controller Board.

Table 2-2
System Controller Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J5704	2650A Clock Jumper	Jumper across pins 1 and 2
J3014	Forced Diagnostic Jumper	Jumper across pins 2 and 3
W3068	Mapping/Write Protect Strap	No change in original strapping
J1051	CPU Float Jumper	Jumper across pins 2 and 3
W7400	Line Grounding Strap	No change in original strapping
W2098	Direct Interrupt Strap	No change in original strapping
W2017	Bootstrap Limiting Strap	No change in original strapping
W1306	High-Speed Interface Strap	No change in original strapping
W1308	Stop Bit Select Strap	No change in original strapping
W1309	Parity Inhibit Strap	No change in original strapping
W1304	Even/Odd Parity Strap	No change in original strapping
S1100	The Diagnostics Mode Switch	Set the six switches to ON

2650A-1 CLOCK JUMPER

J5704 is the 2650A Clock Jumper. This two-position jumper selects either a 2 MHz System Clock or a 1.25 MHz System Clock. Pins 1 and 2 select 2 MHz. Pins 2 and 3 select 1.25 MHz. For normal operation, place the jumper across pins 1 and 2.

FORCED DIAGNOSTIC JUMPER

J3014 is the Forced Diagnostic Jumper. This two-position jumper forces the Diagnostic ROM on the bus, or allows software to select the diagnostics or boot ROMs. Pins 1 and 2 select only the Diagnostic ROM. Pins 2 and 3 select the Diagnostic or Boot ROMs. For normal operation, place the jumper across pins 2 and 3.

MAPPING/WRITE PROTECT STRAP

W3068 is the Mapping/Write Protect Strap. This two-position strap enables the Mapping/Write Protect function during normal operation. If the run between pins 2 and 3 is cut and a strap is placed between pins 1 and 2, the Mapping/Write Protect function is disabled.

CPU FLOAT JUMPER

J1051 is the CPU Float Jumper. This two-position jumper determines the state of the CPU READ(L) signal. If CPU READ(L) is high, the 2650A-1 can write to the system data bus. If CPU READ(L) is low, the 2650A-1 can read the system data bus. Pins 1 and 2 select a high on CPU READ(L). Pins 2 and 3 select a low on CPU READ(L). For normal operation, place the jumper across pins 2 and 3.

LINE GROUNDING STRAP

W7400 is the Line Grounding Strap. This two-position strap grounds P1-56 (a Main Interconnect board line) during normal operation.

DIRECT/INDIRECT INTERRUPT STRAP

W2098 is the Direct/Indirect Interrupt Strap. This two-position strap provides indirect addressing of interrupts during normal operation. If the run is cut between pins 1 and 2 and a strap placed between pins 2 and 3, direct addressing is selected.

BOOTSTRAP LIMITING STRAP

W2017 is the Bootstrap Limiting Strap. This two-position strap selects a 2K-byte address space within the Boot ROM during normal operation. If the run is cut between pins 1 and 2 and a strap is soldered between pins 2 and 3, only 1K-bytes of the Boot ROM is selected.

HIGH-SPEED INTERFACE STRAP

W1306 is the High-Speed Interface Strap. This single-position strap selects an 8-bit data character length during normal operation. If a strap is soldered across this position, a 7-bit data character length is selected.

STOP BIT SELECT STRAP

W1308 is the Stop Bit Select Strap. This single-position cuttable run selects one stop bit during normal operation. If the run at this position is cut, two stop bits are selected.

PARITY INHIBIT STRAP

W1309 is the Parity Inhibit Strap. This single-position cuttable run enables parity generation and checking during normal operation. If the run at this position is cut, the parity generation and checking function is disabled.

EVEN/ODD PARITY STRAP

W1304 is the Even/Odd Parity Strap. This single-position strap selects even parity bits during normal operation. If a strap is soldered across this position and W1309 has not been cut, odd parity bits are selected.

DIAGNOSTIC MODE SWITCH

S1100 is the Diagnostic Mode Switch. This 6-position DIP switch is used to select the mode of ROM-based Diagnostics. For information on the function of this switch, refer to Section 3, the ROM-Based Diagnostics section. Each of the six positions on this switch should be set to a logic zero (set switch positions to ON or CLOSED) during normal operation.

DIAGNOSTIC LEDS

These LEDs are lighted during the running of ROM-Based Diagnostics. They indicate which test is in progress and if an error is detected, an error code is displayed on the LEDs.

EMULATOR CONTROLLER BOARD CONFIGURATION

Figure 2-4 shows the locations of jumpers and straps on the Emulator Controller board and the type of connector at each location. There are five jumpers and five straps on the Emulator Controller board. Table 2-3 lists the configuration required for normal operation.

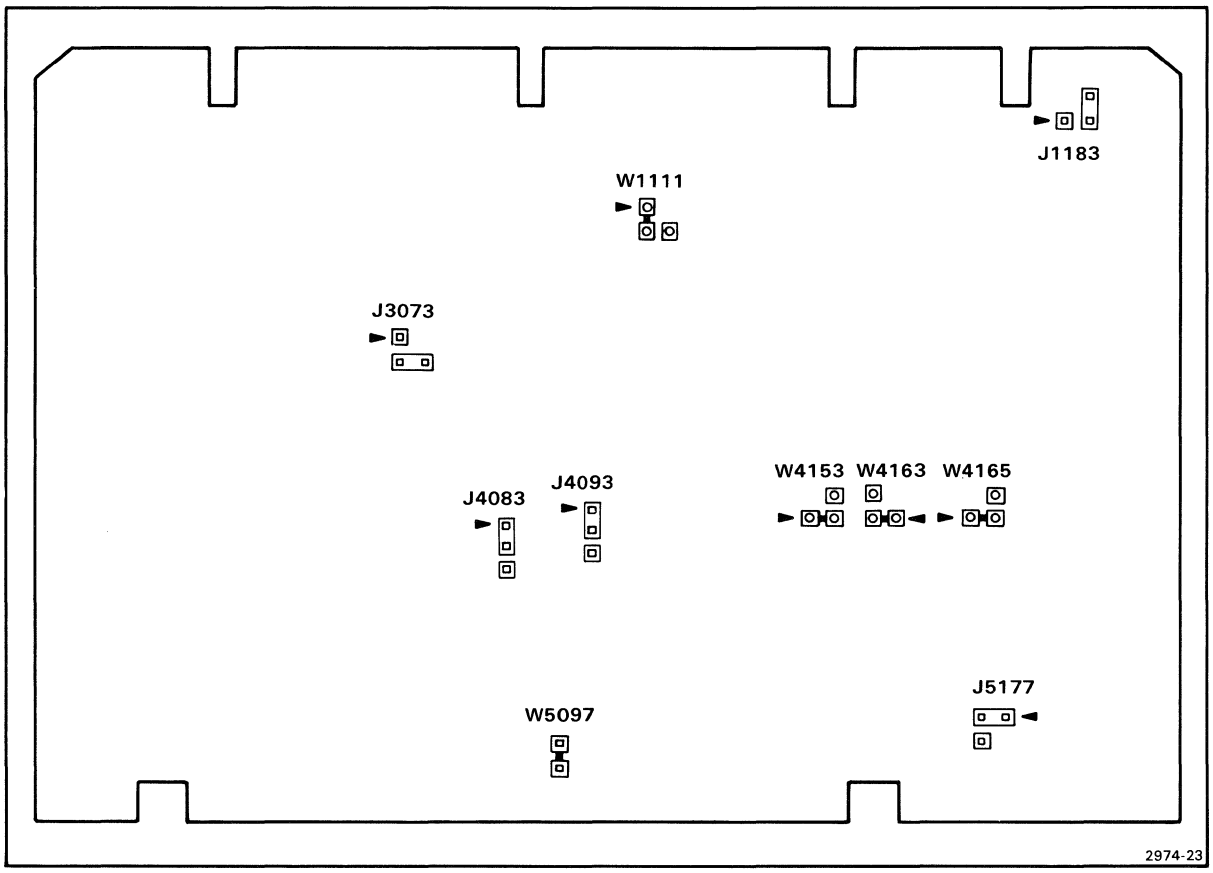


Fig. 2-4. Emulator Controller Board.

Table 2-3
Emulator Controller Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J1183	Front Panel Hold Jumper	Jumper across pins 2 and 3
W1111	Extended Address Strap	No change in original strapping
W5097	Line Grounding Strap	No change in original strapping
J4083	BP1 Extended Address Jumper	Jumper across pins 1 and 2
J4093	BP2 Extended Address Jumper	Jumper across pins 1 and 2
J5177	SVC Detection Jumper	Jumper across pins 1 and 2
J3073	Direct Interrupt Jumper	Jumper across pins 2 and 3
W4153	Immediate Interrupt Strap	No change in original strapping
W4163	Forced Jump Option Strap	No change in original strapping
W4165	Forced Jump Option Strap	No change in original strapping

FRONT PANEL HOLD JUMPER

J1183 is the Front Panel Hold Jumper. This two-position jumper enables or disables the front panel circuitry. Pins 1 and 2 enable the front panel circuitry. Pins 2 and 3 disable the front panel circuitry. For normal operation, place the jumper across pins 2 and 3.

EXTENDED ADDRESS STRAP

W1111 is the Extended Address Strap. This two-position strap enables the extended address function during normal operation. If the cuttable run between pins 1 and 2 is cut and a strap is soldered between pins 2 and 3, the extended address enable line is connected to a pull-up resistor and the extended address function is disabled.

LINE GROUNDING STRAP

W5097 is the Line Grounding Strap. This single-position cuttable run grounds P1-56 (a Main Interconnect board line) during normal operation. If the run at this position is cut, P1-56 will no longer be grounded.

BP1 EXTENDED ADDRESS JUMPER

J4083 is the BP1 Extended Address Jumper. This two-position jumper enables or disables the breakpoint 1 extended address function. Pins 1 and 2 enable the function. Pins 2 and 3 disable the function. For normal operation, place the jumper across pins 1 and 2.

BP2 EXTENDED ADDRESS JUMPER

J4093 is the BP2 Extended Address Jumper. This two-position jumper enables or disables the breakpoint 2 extended address function. Pins 1 and 2 enable the function. Pins 2 and 3 disable the function.For normal operation, place the jumper across pins 1 and 2.

SVC DETECTION JUMPER

J5177 is the SVC Detection Jumper. This two-position jumper selects SVC Detection support for modes 0, 1, and 2, or it selects SVC Detection support for mode 0 only. Pins 1 and 2 select support for all modes. Pins 2 and 3 select support for only mode 0. For normal operation, place the jumper across pins 1 and 2.

DIRECT/INDIRECT INTERRUPT JUMPER

J3073 is the Direct/Indirect Interrupt Jumper. This two-position jumper selects either direct or indirect addressing of interrupts. Pins 1 and 2 select direct addressing of interrupts. Pins 2 and 3 select indirect addressing of interrupts. For normal operation, place the jumper across pins 2 and 3.

IMMEDIATE INTERRUPT OPTION STRAP

W4153 is the Immediate Interrupt Option Strap. This two position strap supports the current configuration of a single immediate interrupt and provides a method to incorporate an additional immediate interrupt if needed. If the cuttable run between pins 1 and 2 is cut and a strap is soldered between pins 2 and 3, INT 31 FF(H) is NORed with the current immediate interrupt at U4150.

FORCED JUMP OPTION STRAPS

W4163 and W4165 are the Forced Jump Option Straps. Future requirements to provide a forced jump capability to interrupts 30 and/or 31 can be met by cutting the run between pins 1 and 2 and soldering a strap between pins 2 and 3) for each strap.

SYSTEM RAM BOARD CONFIGURATION

Figure 2-5 shows the location of the two jumpers and eight LEDs on the System RAM board. Table 2-4 lists the jumper configuration required for normal operation.

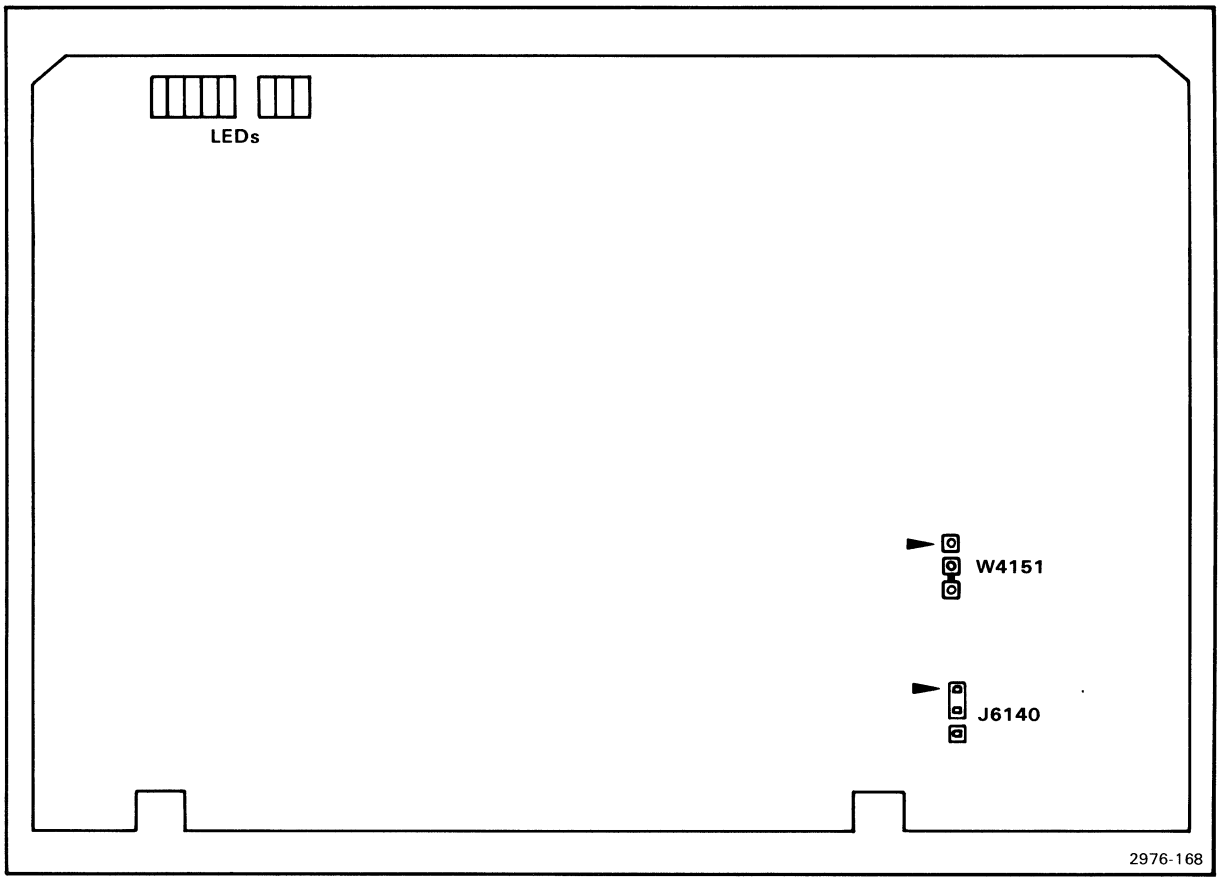


Fig. 2-5. System RAM Board.

Table 2-4
System RAM Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J6140	Test Jumper	Jumper across pins 1 and 2
W4151	Developmental Strap	No change in original strapping

TEST JUMPER

J6140 is the Test Jumper. This two-position jumper determines the board's response to the CMEM(H) line. When the jumper is on pins 1 and 2, the board is used as System Memory whenever the CMEM(H) line goes low. For special applications this jumper can be placed on pins 2 and 3 and the board now functions as a Program Memory board. In this configuration diagnostics that test various program memory functions can be conducted on the board when the CMEM(H) line goes high. When testing the board using diagnostics, the board can be physically located to either the System or Program sections of the Main Interconnect board. For normal operations retain the jumper across pins 1 and 2 and the board in the System section.

DEVELOPMENTAL STRAP

W4151 is a strap that may be used for special developmental requirements. The strapped position permits MSTR RUN(L) and OPREQ(L) to control the timing of the board. If the cuttable run between pins 2 and 3 is cut and the strap is soldered between pins 1 and 2, MSTR RUN(L) is removed from the board. This position is for special developmental requirements.

DIAGNOSTIC LEDS

Five of these eight LEDs are turned off or on during the running of Power-Up Diagnostic Tests. They indicate which test is in progress and if an error is detected, an error code is displayed on the LEDs. These LEDs are used in conjunction with the LEDs on the System Controller board. The other three LEDs monitor the status of the lower three bits from the data byte of I/O port address D2.

LANGUAGE PROCESSOR BOARD CONFIGURATION

Figure 2-6 shows the location of the one jumper and one strap on the Language Processor board and the type of connector at each location. Table 2-5 lists the configuration required for normal operation.

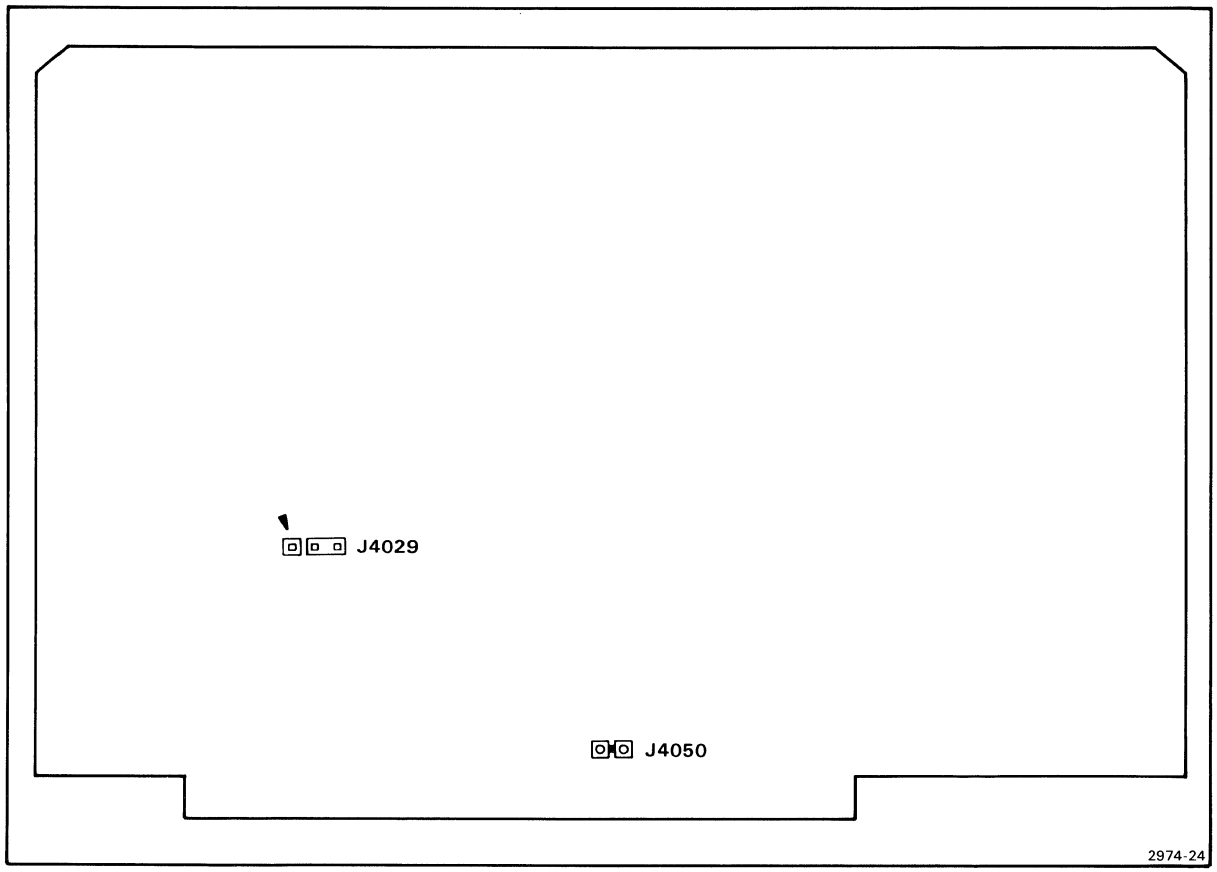


Fig. 2-6. Language Processor Board.

Table 2-5
Language Processor Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J4050	Line Grounding Strap	No change in original strapping
J4029	Slow/Fast Clock Jumper	Jumper across pins 2 and 3

LINE GROUNDING STRAP

J4050 is the Line Grounding Strap. This single-position cuttable run grounds P1-56 (a Main Interconnect board line) during normal operation. If the run at this position is cut, P1-56 will no longer be grounded.

SLOW/FAST CLOCK JUMPER

J4029 is the Slow/Fast Clock Jumper. This two-position jumper selects one of two clock speeds for the Z80 Microprocessor. Pins 1 and 2 select a 2.5 MHz clock. Pins 2 and 3 select a 4 MHz clock. For normal operation, place the jumper across pins 2 and 3.

PROGRAM MEMORY BOARD CONFIGURATION

Figure 2-7 shows the locations of the jumpers, straps, and switch on the board and the type of connector at each location. There are four jumpers and two straps on the Program Memory board. In addition, a DIP switch (S7170) is used to select the extended addressing function. Table 2-6 lists the configuration required for the normal operation of the Program Memory board.

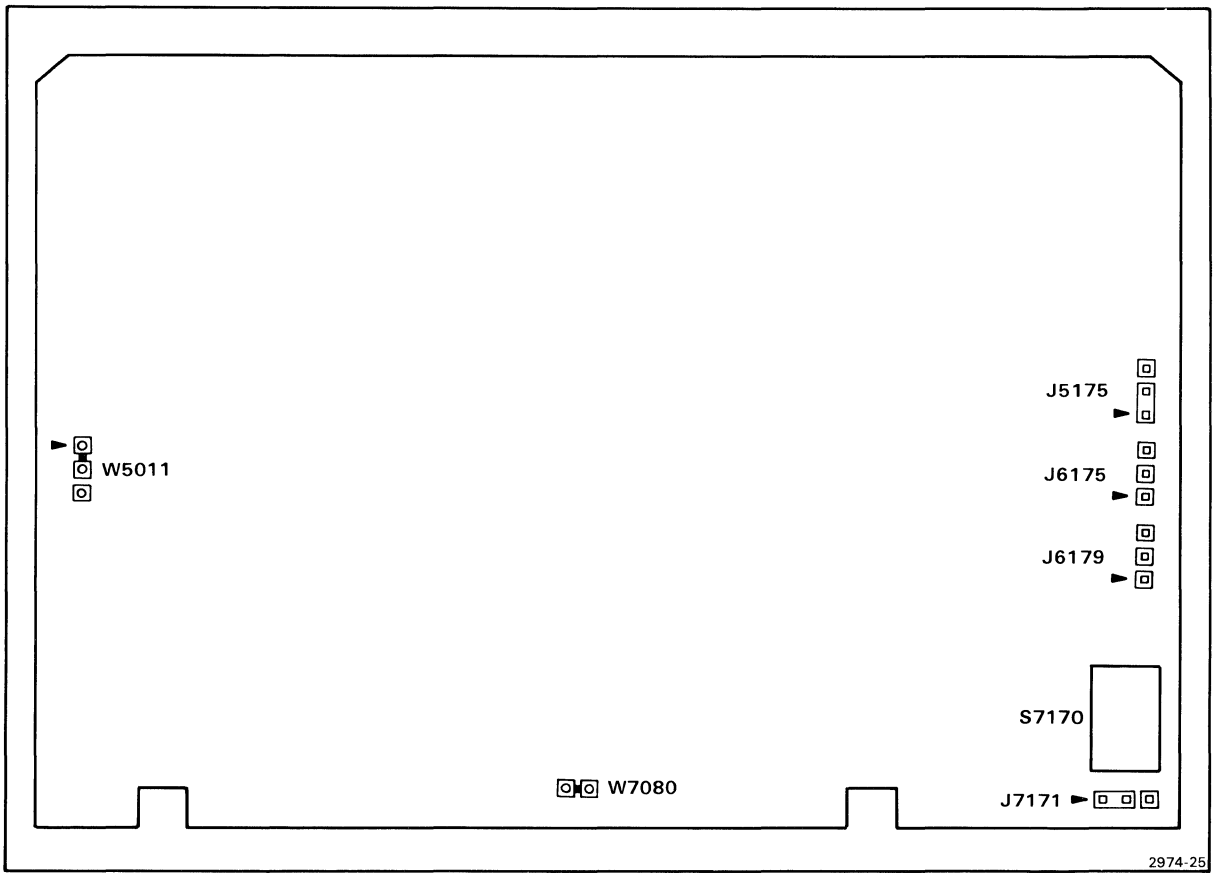


Fig. 2-7. Program Memory Board.

Table 2-6
Program Memory Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J6179	Program/System Memory Jumper	Jumper across pins 1 and 2
J6175	Low/High Memory Jumper	See description that follows
J7171	Extended Bank Jumper	Jumper across pins 1 and 2
J5175	Memory Relocation Jumper	See description that follows
W5011	Delayed Read strap	No change in original strapping (a)
W7080	Line Grounding Strap	No change in original strapping
S7170	Extended Memory DIP Switch	See description that follows

(a) Unless specified in the Emulator Processor Installation Manual.

PROGRAM/SYSTEM MEMORY JUMPER

J6179 is the Program/System Memory Jumper. This two-position jumper determines whether the board is used as Program Memory or under special applications as System Memory. Pins 1 and 2 select Program Memory. Pins 2 and 3 select a special System Memory configuration. The 8550 operating system, DOS/50, prohibits using the Program Memory board as System Memory. Therefore, for normal operations retain the jumper across pins 1 and 2.

LOW/HIGH BOARD JUMPER

J6175 is the Low/High Board Jumper. This two-position jumper determines whether the board will be used as low memory (addresses 0 to 32K) or high memory (addresses 32K to 64K). Note that although low memory exists for both System and Program Memory, high memory exists only for Program Memory. Pins 1 and 2 select high memory. Pins 2 and 3 select low memory.

EXTENDED BANK JUMPER

J7171 is the Extended Bank Jumper. This two-position jumper enables or disables the extended bank comparator function. Pins 1 and 2 enable this function. Pins 2 and 3 disable the function. For normal operation, place the jumper across pins 1 and 2.

MEMORY RELOCATION JUMPER

J5175 is the Memory Relocation Jumper. This two-position jumper enables or disables the memory relocation function. Pins 1 and 2 enable the function. Pins 2 and 3 disable the function. For System Memory normal operation with one memory board installed, place the jumper across pins 1 and 2. For Program Memory normal operation with one memory board installed, place the jumper across pins 1 and 2. When two Program Memory boards are installed, place the jumpers on both boards across pins 2 and 3.

DELAYED READ STRAP

W5011 is the Delayed Read Strap. If the cuttable run between pins 1 and 2 is cut and a strap soldered between pins 2 and 3, the READ ENBL(L) signal will no longer be delayed. This signal is delayed during normal operation.

LINE GROUNDING STRAP

W7080 is the Line Grounding Strap. This single-position cuttable run grounds P1-56 during normal operation. If the run at this position is cut, P1-56 will no longer be grounded.

EXTENDED MEMORY DIP SWITCH

S7170 is the Extended Memory DIP switch. This 8-bit DIP switch works in conjunction with the Low/High Jumper to allocate extended memory. Unless a particular setting for an option is indicated within that option's Installation Manual, all switches should be in the ON or CLOSED position.

COMMUNICATIONS INTERFACE BOARD CONFIGURATION

Figure 2-8 shows the locations of jumpers on the Communications Interface board and the type of connector at each location. There are three jumpers on the Communications Interface board. Table 2-7 lists the configuration required for normal operation.

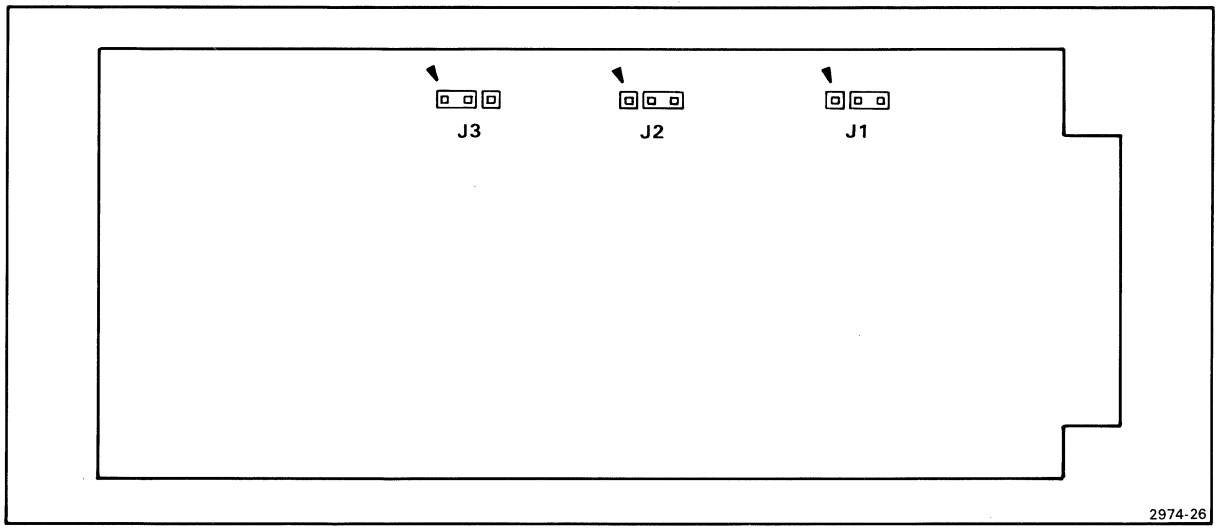


Fig. 2-8. Communications Interface Board.

Table 2-7
Communications Interface Board Normal Operating Configuration

Number	Jumper or Strap	Normal Operating Configuration
J1	RS-232-C Multiplexer Jumper	Jumper across pins 2 and 3
J2	RS-232-C Multiplexer Jumper	Jumper across pins 2 and 3
J3	External Baud Rate Jumper	Jumper across pins 1 and 2

RS-232-C CONTROL LINE MULTIPLEXER JUMPER (J102)

J1 (located on the Communications Interface board) is the RS-232-C Control Line Multiplexer Jumper for jack J102 (located on the rear panel). This two-position jumper selects the RTS(H) signal or ground as a control signal for J102. Pins 1 and 2 select the RTS(H) signal. Pins 2 and 3 select ground. For normal operation, place the jumper across pins 2 and 3.

RS-232-C CONTROL LINE MULTIPLEXER JUMPER (J101)

J2 (located on the Communications Interface board) is the RS-232 Control Line Multiplexer Jumper for jack J101 (located on the rear panel). This two-position jumper selects the CTS(H) signal or ground as a control signal for J101. Pins 1 and 2 select the CTS(H) signal. Pins 2 and 3 select ground. For normal operation, place the jumper across pins 2 and 3.

EXTERNAL BAUD CLOCK JUMPER

J3 (located on the Communications Interface board) is the External Baud Clock Jumper. This two-position jumper selects the 110 baud rate or an external baud rate clock. Pins 1 and 2 select a signal from the 110 baud rate generator. Pins 2 and 3 disconnect the line from the 110 baud rate generator and select an external signal as the baud rate. For normal operation, place the jumper across pins 1 and 2.

INSTALLING A CIRCUIT BOARD

To install a circuit board in the 8301, perform the following procedure:

1. Verify that power to the 8301 is OFF.

2. Remove the 8301 top cover, according to the procedure given earlier in this section.

3. While facing the front of the 8301, grasp the ejector levers at the upper edges of the circuit board. Align the circuit board with a socket of the Main Interconnect board, so that the board's component side faces left, as you face the instrument's front panel.

4. Slide the circuit board downward, within a vertical guide, until it reaches the Main Interconnect Board socket. Then, press down firmly and evenly on the upper edges of the circuit board until it snaps into place.

CONNECTING A PROTOTYPE CONTROL PROBE

The procedure for installing an optional Prototype Control Probe is not included in this manual. Refer to the Installation manual that describes your Prototype Control Probe for details on installing that option.

REPLACING THE TOP COVER

The top cover of the 8301 is replaced in the following manner:

1. From the rear panel, slide the top cover into the two grooves along the top edges of the instrument.

2. Continue to insert the top cover into the grooves, until the right-angle flange at its rear edge is flush with the rear panel of the 8301 chassis.

3. Place a cover retainer at each upper rear corner of the 8301, covering the right-angle flange of the top cover.

4. Thread the two screws (removed with the top cover) through the cover retainers and tighten both screws.

REAR PANEL CONNECTORS

The 8301 rear panel is shown in Fig. 2-9. The connectors shown in Fig. 2-9 are briefly described in the following paragraphs. The I/O port characteristics, which describe the peripheral interface requirements for each rear panel connector, are contained in Section 6, Specifications, of this manual.

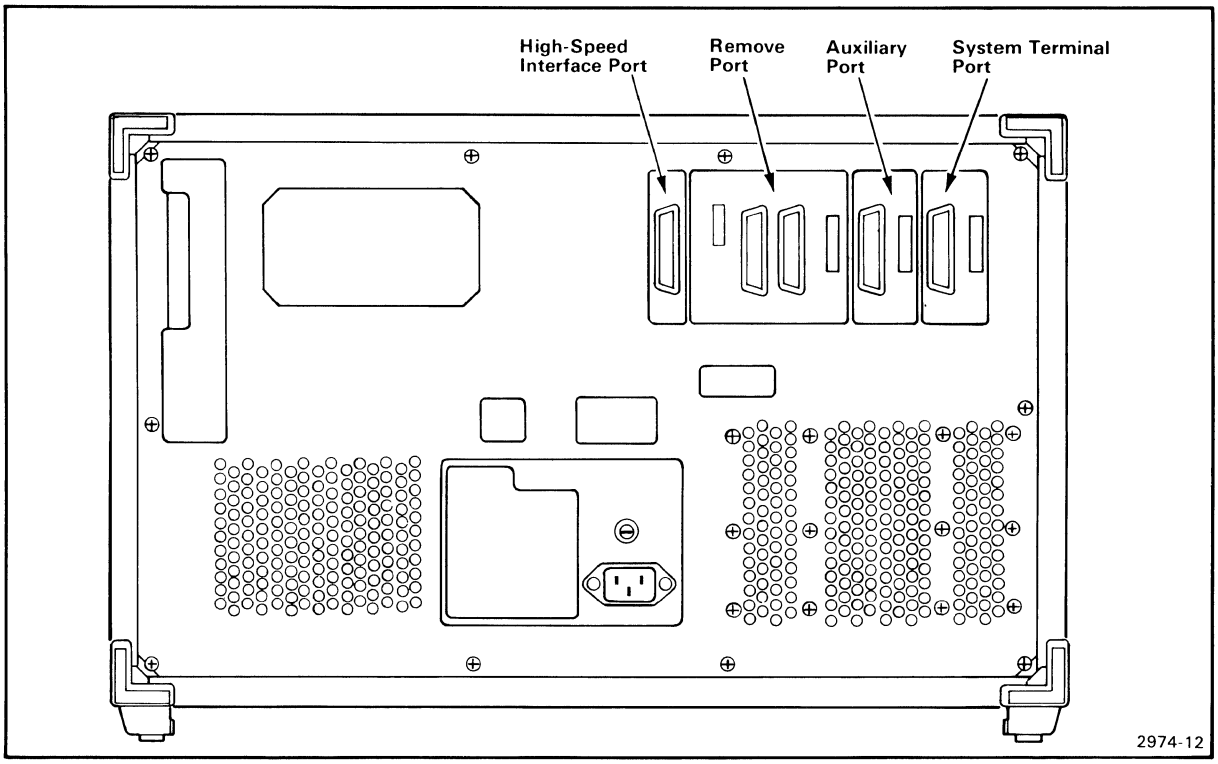


Fig. 2-9. 8301 Rear Panel.

HIGH-SPEED SERIAL INTERFACE PORT

J100 is the High-Speed Serial Interface (HSI) Port. The HSI Port is a modified RS-422 compatible serial interface designed to communicate with a data storage unit such as a DMU. This port will operate only at 153.6k baud. Table 2-8 illustrates the pin configuration of J100.

Table 2-8
HSI Port -- J100 Pin Configuration

Pin Number	Function
1	Shield
2	TX (-)
3	RX (-)
4	RTS(+)
5	CTS(+)
6---9	Not used
10	RTS(-)
11	TX (+)
12	RX (+)
13	DTR(-)
14---19	Not used
20	DTR(+)
21---24	Not used
25	CTS(-)

REMOTE PORT

J101 and J102 form the Remote Port. This port is designed to be used to interface the 8301 with a telephone modem. Both the male and female connectors of this port are RS-232-C compatible. The Remote Port has two switches associated with it. One switch selects the baud rate (refer to Fig. 2-10). A second switch selects one of four operating modes (refer to Table 2-9). Table 2-10 lists the pin configuration for connectors J101 and J102.

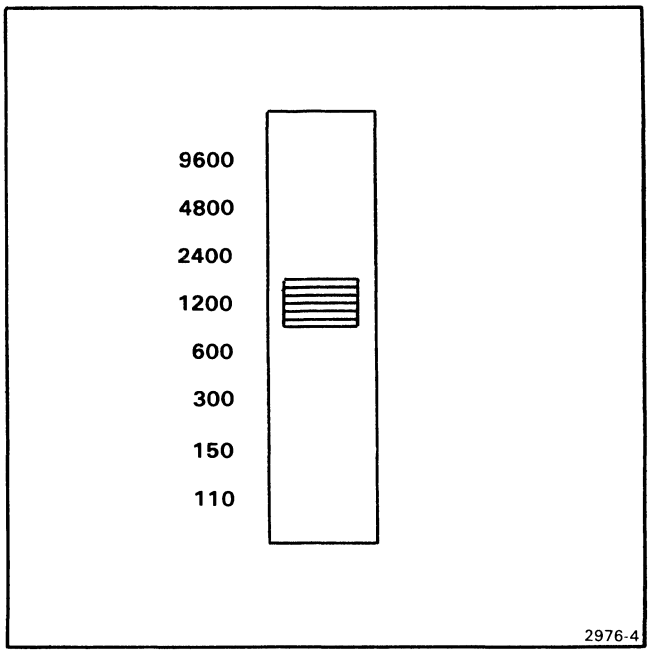


Fig. 2-10. Switch Selectable Baud Rates.

Table 2-9
Remote Port Modes

Switch Setting	Function
CNTL	No Control
DTE1	DTE with CTS control
DTE2	DTE with DSR control
DCE	DCE with control

Table 2-10
Pin Configuration for RS-232-C Compatible Ports

Pin No.	Remote Port		Auxiliary Port	Terminal Port
	J101 25-Pin Male	J102 25-Pin Female	J103 25-Pin Female	J104 25-Pin Female
1	Shield	Shield	Shield	Shield
2	TX	TX	TX	TX
3	RX	RX	RX	RX
4	RTS	RTS	RTS	RTS
5	CTS	CTS	CTS	CTS
6	DSR	DSR	DSR	DSR
7	Logic Ground	Logic Ground	Logic Ground	Logic Ground
8	DCD	DCD	DCD	DCD
9---16	Not used	Not used	Not used	Not used
17	Not used	Not used	EXT CLK	Not used
18,19	Not used	Not used	Not used	Not used
20	DTR	DTR	DTR	DTR
21---25	Not used	Not used	Not used	Not used

AUXILIARY PORT

J103 is the Auxiliary Port. This port provides communications to and from auxiliary equipment, such as a line printer. The Auxiliary Port is an RS-232-C compatible port with a switch-selectable baud rate. In addition, a jumper-selectable external baud rate is also available on pin 17 of J103. To select this external baud rate, refer to the External Baud Clock Jumper in the description of the Communications Interface Board, earlier in this section. The pin configuration for the Auxiliary Port is listed in Table 2-10. Figure 2-10 shows the baud rate switch settings.

SYSTEM TERMINAL PORT

J104 is the Terminal Port. This RS-232-C compatible port provides a communications interface between the 8301 and the system terminal. The pin configuration for the Terminal Port is listed in Table 2-10. Figure 2-10 shows the baud rate switch settings.

STORAGE AND RESHIPPING

When a precision electronic instrument, such as the 8301, is to be placed in storage or reshipped, it's best to repack it as it was originally shipped from the factory. For this reason, be sure to save the carton and packing material in which your equipment was shipped. To repack the 8301, simply follow the unpacking instructions in reverse order. The following paragraphs describe further considerations that must be made when storing or reshipping an 8301.

STORAGE

Observe the following considerations whenever you place the 8301 in storage:

- Provide adequate protection from dust.
- Do not exceed the humidity or temperature limitations of the instrument, as outlined in the Specifications, Section 6 of this manual.
- Store the carton upright. Do not compress the carton or stack heavy objects upon it.

RESHIPPING

If the unit must be shipped to the factory or service center, the following steps should be taken:

- Note the serial number of the unit on the back panel and any other relevant numbers or symbols needed for identification. (This information is required for fault notification correspondence, which should be sent separately.)
- Wrap the unit in durable waterproof material such as heavy polyethylene, and tape securely. This step should be carried out only in a dry atmosphere, and with the unit cool to the touch.
- Pack the unit in a sturdy box (heavy cardboard is acceptable for land shipments), lined with three inches (76 mm) of medium density foam or expanded polystyrene.
- Cables, adapters, and other accessories should be wrapped separately

and attached by tape to the inner liner at a break in the foam, or taped to a separate platform mounted above the foam or polystyrene (as used in the original shipping). In the latter case, a sheet of one inch (25 mm) minimum thick foam should be taped above the cable package.

- Seal the carton with reinforced packaging tape and identify the sender, the unit number, and the serial number on the outside of the carton.

- Notify the factory or your sales representative of your intent to ship the instrument, and await their acknowledgement, before you do ship an 8301.

Section 3

POWER-UP DIAGNOSTICS

INTRODUCTION

This section covers the self-testing (power-up) diagnostics tests that are conducted within the 8301. These tests are completed prior to booting the operating system from the Data Management Unit (DMU). The diagnostics are contained in a 32K (4K x 8) PROM (type 2732) device. The power-up diagnostics provide the following features:

- Power-up tests are run automatically during power-up or restart conditions. These tests are sequentially executed. The tests verify that circuitry within the 8301 hardware that is required to boot and transfer the operating system off the disc in the DMU into the 8301 system memory. If the 8301 fails any power-up test, the test is suspended and branches to the Critical Function Monitor (CFM) routine. An error code is displayed on either the System Terminal or on the 8301 LEDs (a set of five LEDs on the System Controller board, one LED on the Front Control Panel and a set of five LEDs on the System RAM board).

- The Critical Function Monitor (CFM) is a set of test routines and commands used to perform additional tests to determine the probable cause of a power-up failure. A limited set of user commands may be entered from the System Terminal. Switch-selectable options also increase the capabilities of the CFM.

At the time of this printing, there are two versions of the power-up ROM. The version in your 8301 is readily identified by two methods:

1. The 8301 Boot message is followed by a version number. The original version displays the following message:

   8301 BOOT V1.x

   The second version displays the following message:

   8301 BOOT V2.x

NOTE

The "V1 or V2" in the display designates the version number and the ".x" designates the revision number.

2. The power-up and boot ROMs are part numbered as follows:

Original Version
160-0728-00 BOOT
160-0802-00 DIAG

Second Version
160-0728-01 BOOT
160-0802-01 DIAG

The Critical Function Monitor (CFM) is (with few exceptions) identical in both versions of the power-up ROM. Therefore, this section is divided into three parts. Each part containing the following information:

Part 1 This part describes the power-up tests for the original version (V1.x) of the diagnostic ROM.

Part 2 This part describes the power-up tests for the second version (V2.x) of the diagnostic ROM.

Part 3 This part describes the functions and use of the Critical Function Monitor (CFM).

If you have the original version of the power-up ROM, Parts 1 and 3 in this section apply. If you have the second version of the power-up ROM, Parts 2 and 3 in this section apply.

PART 1---VERSION V1.X

The power-up tests for the original version of the diagnostic ROM are described in the following paragraphs.

Figure 3-1 shows the memory map for the power-up tests and work areas that are required in system memory. Note that the specific address locations of the power-up tests and CFM are not shown within the ROM. When a new version of the ROM is assembled, the various routines could be assigned different locations within the ROM.

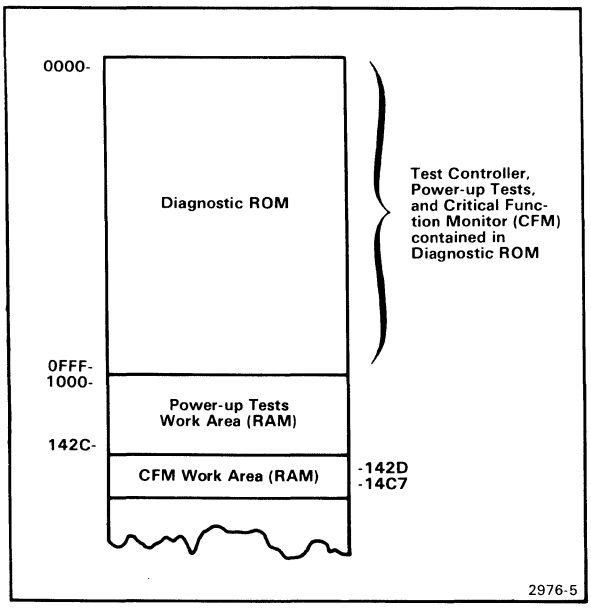


Fig. 3-1 System Memory diagnostic address space.

MODE SWITCH

During power-up or restart conditions the 8301 can be configured for several modes of operation, depending on the settings of the mode selector switch. The mode selector switch is a 6-position DIP switch located in the upper center portion of the System Controller board. Figure 3-2 illustrates the two types of DIP switches that may be used. Each switch position can be set to either OFF (Open) or ON (Closed). Figure 3-3 is a top view of the board. This figure shows the switch position numbers.

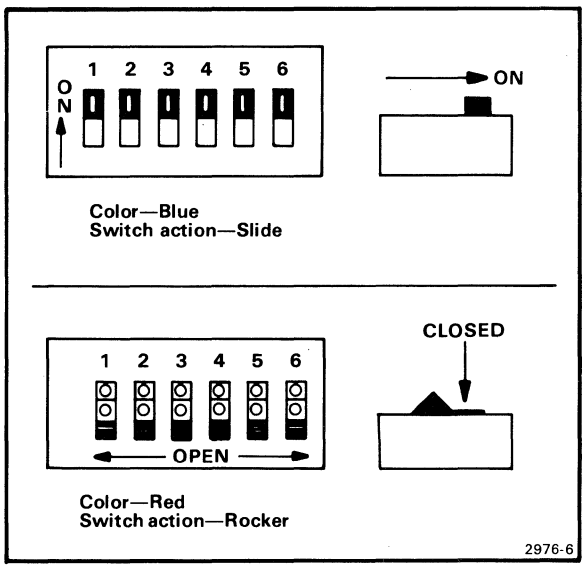


Fig. 3-2. 6-Position DIP switch (two types).

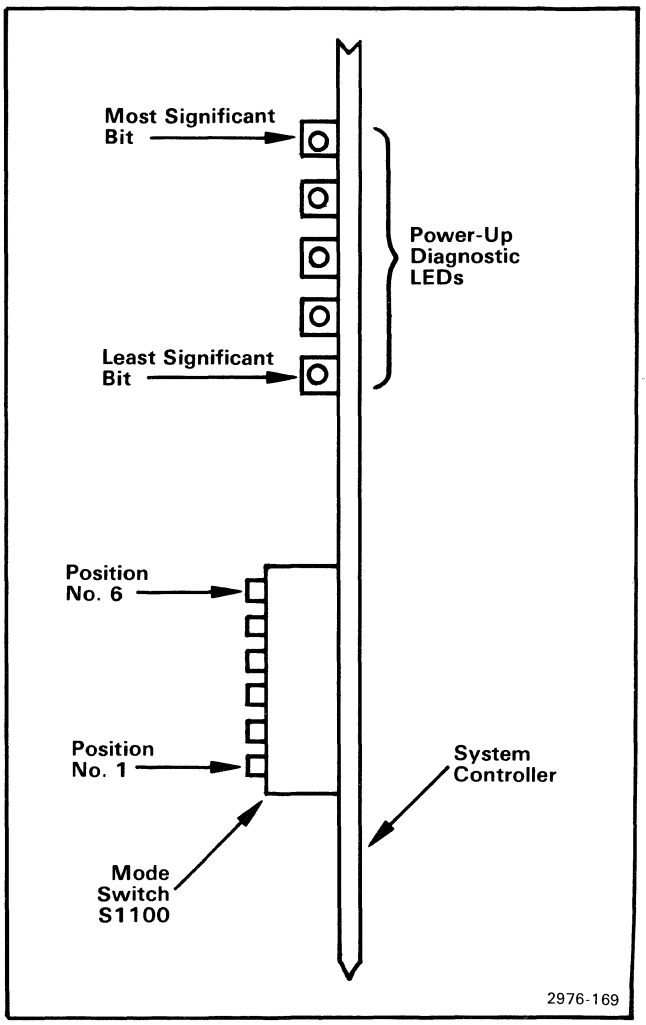


Fig. 3-3. Mode selector switch and power-up LED.

SWITCH-SELECTABLE OPTIONS

Figure 3-4 is a modified decision tree diagram showing various options that are available by changing the mode selector switch positions. This decision tree will be referred to often in the following paragraphs. There are two main branches in the decision tree: the normal (boot) branch and the CFM (no boot) branch.

The mode switch positions determine the options selected. Note in Fig. 3-4 that position 6 is read first. This position accesses the two main operating modes: normal and CFM.

Normal Mode

The normal (boot) operating mode is selected when the 8301 is operating properly (no failure indicated during power-up tests) and you want to boot the operating system from the Data Management Unit (DMU). When this mode is selected, the following options are available:

1. Power-up diagnostics can be run or bypassed.

2. Selection of interface port or booting from Manufacturing Test Unit. (Manufacturing Test Unit position is used for factory testing only.)

3. The interface port to the DMA controller is the High-speed Serial Interface (HSI) port.

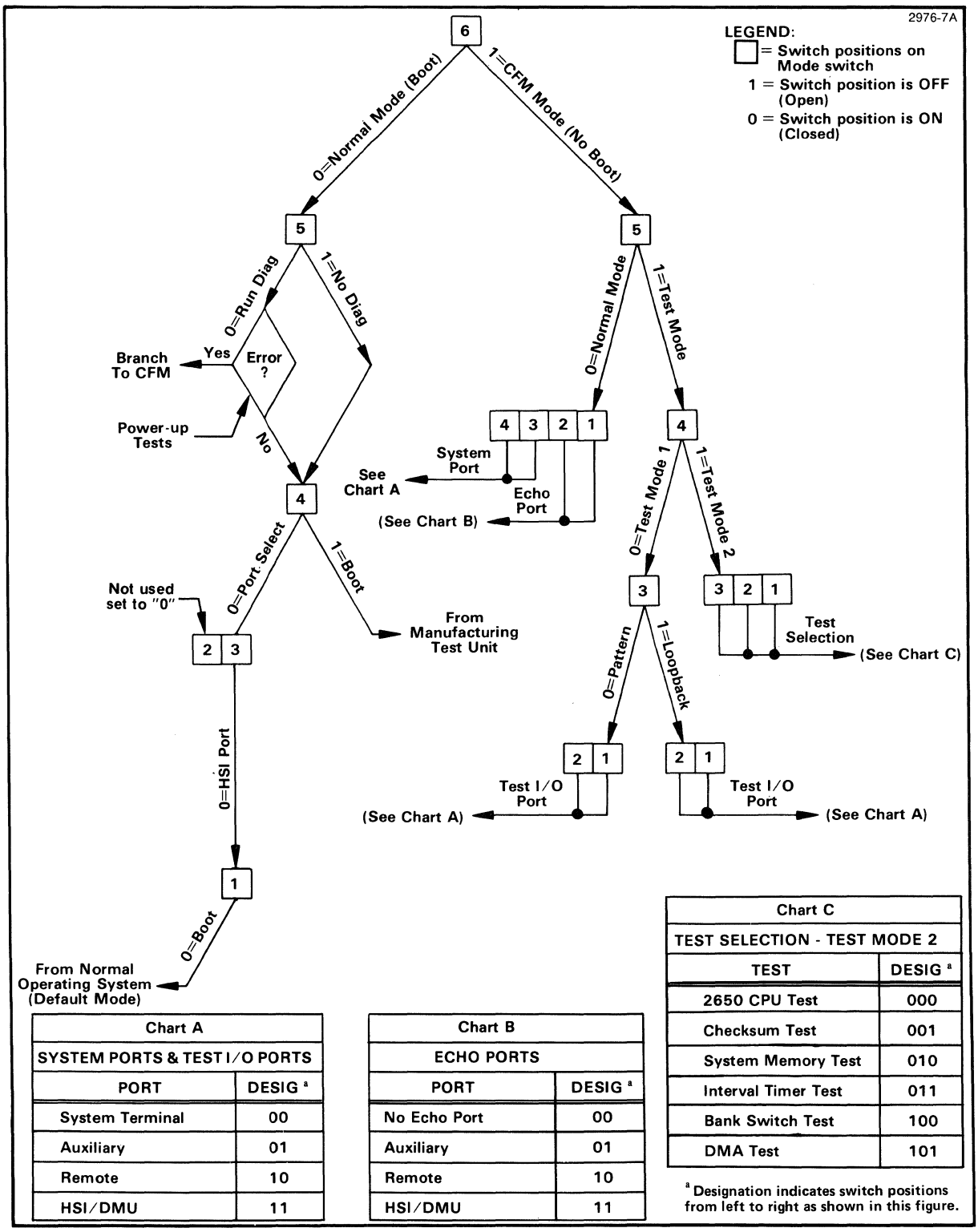


Chart A	
SYSTEM PORTS & TEST I/O PORTS	
PORT	DESIG [a]
System Terminal	00
Auxiliary	01
Remote	10
HSI/DMU	11

Chart B	
ECHO PORTS	
PORT	DESIG [a]
No Echo Port	00
Auxiliary	01
Remote	10
HSI/DMU	11

Chart C	
TEST SELECTION - TEST MODE 2	
TEST	DESIG [a]
2650 CPU Test	000
Checksum Test	001
System Memory Test	010
Interval Timer Test	011
Bank Switch Test	100
DMA Test	101

[a] Designation indicates switch positions from left to right as shown in this figure.

Fig. 3-4. Mode switch decision tree (Version V1.x).

For normal operating conditions the mode switch positions are set to "0", as shown in Table 3-1.

Table 3-1
Mode Switch Settings for Normal Operating Mode
(Version V1.x)

Switch Position	Setting	Selected Option
6	0 (ON or Closed)	normal mode (boot)
5	0 (ON or Closed)	run power-up tests
4	0 (ON or Closed)	select interface port
3	0 (ON or Closed)	HSI port selected
2	0 (ON or Closed)	switch is not used during normal (boot) mode
1	0 (ON or Closed)	boot normal operating system from DMU

CFM Mode

The CFM operating mode is selected by either of the following methods:

1. During normal operations, if one of the power-up tests fails, an error code is displayed on the System Terminal or LEDs and the power-up test branches to the CFM. In this mode, the CFM is preconfigured to use the System Terminal as the system port with no echo port. This means that CFM user commands can be entered and displayed on the System Terminal.

2. The other method of selecting the CFM is to set the mode switch position 6 to "1" (OFF or Open). This method fully utilizes the capabilities of the CFM. The CFM user commands can be entered and displayed on a choice of peripherals. It also permits the selection of either CFM normal mode, Test Mode 1, or Test Mode 2. Refer to Fig. 3-4.

Additional information on using the CFM operating mode is included later in Part 3 of this section.

POWER-UP/RESTART SEQUENCE

The power-up/restart sequence of Version V1.x for the 8301 is shown in the accompanying flow diagram, Fig. 3-5. The following steps describe this sequence. (Refer also to Fig. 3-4.)

1. The boot ROM reads mode switch position 6.

2. If switch position 6 is set to "1" (OFF or Open), the CFM mode is selected; mode switches 5, 4, 3, 2, and 1 are read to determine the mode of operation and the tests to be performed by the CFM. If switch position 6 is set to "0" (ON or Closed), the normal operating mode is selected and switch position 5 is read.

3. If switch position 5 is set to "1", the boot ROM is selected; the power-up tests are bypassed, and switch position 4 is read. If switch position 5 is set to "0", the power-up diagnostics are selected and executed. If the power-up tests fail, the Test Controller branches to the CFM for further analysis and troubleshooting. An error code is also displayed on the LEDs or the System Terminal. If the power-up tests are passed, switch position 6 is read again to verify that the switch has not been changed. If switch position 6 has been changed to "1", the CFM branch is selected (as in step 2 above). If switch position 6 is still "0", the boot ROM is selected and mode switch position 4 is read.

4. If switch position 4 is set to "1", the Manufacturing Test Unit is selected for boot-up operations. If this switch is set to "0", mode switch position 3 is read to determine interface port selection. The Manufacturing Test Unit is used during manufacturing only.

5. If switch position 3 is set to "0", the HSI port is selected for booting. Switch position 1 is then read to determine booting procedures.

6. If this switch is set to "0", the 8301 boots the normal operating system from the DMU. The interactive boot mode can specify an alternative boot source.

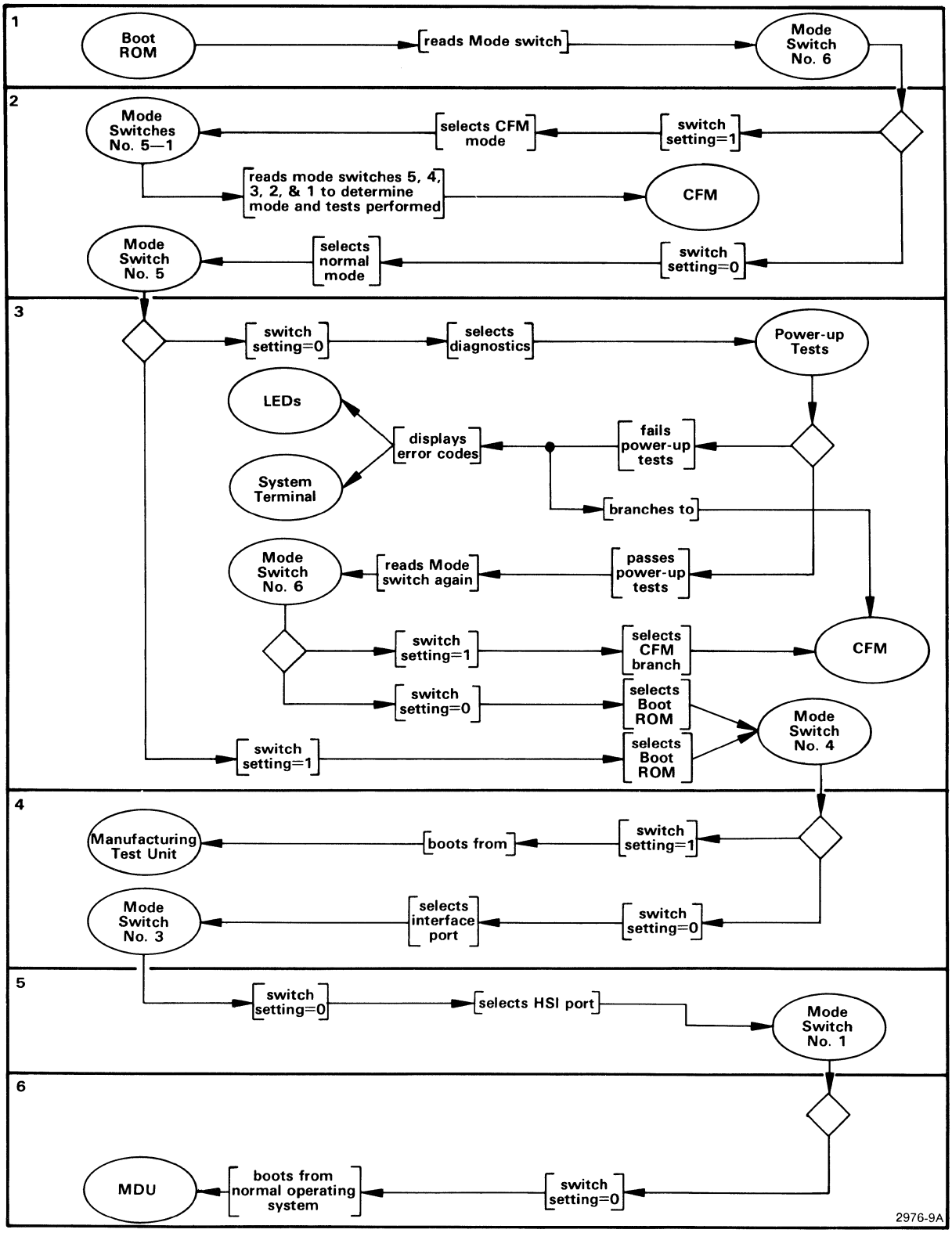


Fig. 3-5. 8301 power-up/restart sequence (Version V1.x).

POWER-UP TESTS

The first eight power-up tests are executed out of the diagnostic ROM. During the eighth power-up test, the ninth and tenth power-up tests are loaded into RAM (system memory). The last two tests are executed from RAM. Therefore, allowing the RAM area that is occupied by ROM addresses (0---4K) to be tested.

Once the power-up test sequence is started, the tests are sequentially executed unless an error is encountered during any of the tests.

MESSAGE AND ERROR CODES

There are two types of codes displayed: message codes and error codes. Message codes are only displayed on the LEDs at the start of each power-up test. Error codes are displayed on either the LEDs or the System Terminal, depending on the type of error and where it occurred during the execution of the tests.

The LEDs are located on the System Controller board (refer to Fig. 3-3) with the most significant LED on the left as viewed from the component side of the board. The error codes displayed on the LEDs are shown in the following tables with the most significant LED in the left column. A "0" in the error code indicates the LED is not lit and a "1" indicates the LED is lit.

NOTE

The LEDs on the System RAM board are not used in the Version V1.x power-up tests described here in Part 1. Disregard these LEDs.

Error codes displayed on the System Terminal appear as a register dump of the system processor. The error code is displayed in register, R0. This will be defined in greater detail later in this section.

Message Codes

Before each power-up test is executed a message code is sent to the diagnostic LEDs. This message code indicates which test is being executed. If an error code is written to the LEDs during the execution of any power-up test, the initial message code is replaced by the error code. However, if the error code is displayed on the System Terminal, the initial message code written to the LEDs at the start of the test is retained in the LEDs. This message code will verify, in addition to the error code displayed on the System Terminal, which power-up test has failed.

Table 3-2 shows the message codes written to the LEDs at the start of each test. (A "1" indicates the LED is lit and "0" indicates the LED is not lit.) Note that the code for the first nine tests is the complement of the test number. During the last two test, the message code is sent to the LEDs at the beginning and middle of the power-up tests.

Error Codes

When an error is detected during execution of the power-up tests, the test routine transfers control to the error handler routine. This routine checks the error code contained in register R0 and determines whether to display it on the diagnostic LEDs or to transfer control to the Critical Function Monitor (CFM) for display on the System Terminal. The error codes written to the LEDs indicate that the memory used by the power-up test is not accessible to the test. These memory error codes are shown in Table 3-3.

Table 3-2
Starting Message Codes for Each Power-Up Test

Power-Up Test No.	Title of Test	Front Panel LED	Message Code to Diagnostic LEDs
01	Initialization	1	1 1 1 1 0
02	Instruction Set Test	1	1 1 1 0 1
03	Diagnostic ROM Checksum Test	1	1 1 1 0 0
04	System Memory Test (4K---32K)	1	1 1 0 1 1
05	Interval Timer Test	1	1 1 0 1 0
06	Bank Switch Test	1	1 1 0 0 1
07	DMA Test	1	1 1 0 0 0
08	RAM-Based Test Loader	1	1 0 1 1 1
09,0A	System Memory Test (0---4K)	1	1 0 1 1 0
		1	1 0 1 0 1
0B,0C	Boot ROM Checksum Test	1	1 0 1 0 0
		1	1 0 0 1 1
0D	Branches to Boot ROM	1	1 0 0 1 0

LED No. 5 is shown as the leftmost bit and
LED No. 1 as the rightmost bit.

Table 3-3
Memory Error Codes to LEDs

Title of Memory Error	Memory Error Code	Power-Up Test No.
System Memory Address Error	0 0 0 0 0	4
RAM-Based Test Loader Memory Error	0 0 0 0 1	8
Diagnostic ROM Checksum Memory Error	0 0 0 1 0	3
Bank Switch Memory Error	0 0 0 1 1	6
Interrupt Handler Memory Error	0 0 1 0 0	5
DMA Memory Error	0 0 1 0 1	7

LED No. 5 is shown as the leftmost bit and
LED No. 1 as the rightmost bit.

The error codes that are passed to the CFM for display on the System Terminal are displayed in register R0. This is the first register in the display of the system processor's register dump. The register dump of all nine registers is displayed on the System Terminal as follows:

R0=XX XX XX XX XX XX XX XX XX

Where "XX" is the hexadecimal value of each register displayed in successive order as follows:

R0 R1 R2 R3 R4 R5 R6 PSU PSL

The CFM sends the error codes to all RS-232-C ports. Table 3-4 shows the error and error codes that are associated with each power-up test.

Table 3-4
Error Codes for Power-Up Tests

Title of Error	Error Code	Power-Up Test No.
Instruction Set Test Error	04	2
(Not assigned)	05	
DMA Register Stuck Type Error	06	7
(Not assigned)	07	
DMA Logic Error·	08	7
Unexpected Interrupt Error*	09	
Interrupted Interval Timer Error	0A	5
Non-Interrupted Interval Timer Error	0B	5
Bank Switch Logic Error	0C	6
System Memory Error (32K---4K)	0D	4
System Memory Error (4K---32K)	0E	4
Diagnostic ROM Checksum Error	0F	3
System Memory Error (4K---0)	2D	9
System Memory Error (0---4K)	2E	9
Boot ROM Checksum Error	2F	10

* This is a universal error, that could be displayed during any power-up test if an unexpected interrupt occurred.

Power-Up Tests and Error Codes

Table 3-5 lists the power-up tests and the related error codes for each test. In addition, Tables 3-3 and 3-4 contain cross references between error codes and the power-up tests. If an error code is displayed, you can use these tables to determine which test failed and the power-up test number where that test is described.

Table 3-5
Power-Up Tests and Related Error Codes

Power-Up Test No.	Title of Test	LED Memory Error Code	System Terminal Error Code
1	Initialization	None	None
2	Instruction Set Test	None	04
3	Diagnostic ROM Checksum Test	0 0 0 1 0	0F
4	System Memory Test (4K---32K)	0 0 0 0 0	0D,0E
5	Interval Timer Test	0 0 1 0 0	0A,0B
6	Bank Switch Test	0 0 0 1 1	0C
7	DMA Test	0 0 1 0 1	06,08
8	RAM-Based Test Loader	0 0 0 0 1	None
9	System Memory Test (0---4K)	None	2D,2E
10	Boot ROM Checksum Test	None	2F

Note in Table 3-5 that the unexpected interrupt error code 09 is not cross-referenced to any power-up test. This error code may be displayed during any of the power-up tests if an unwanted interrupt occurs.

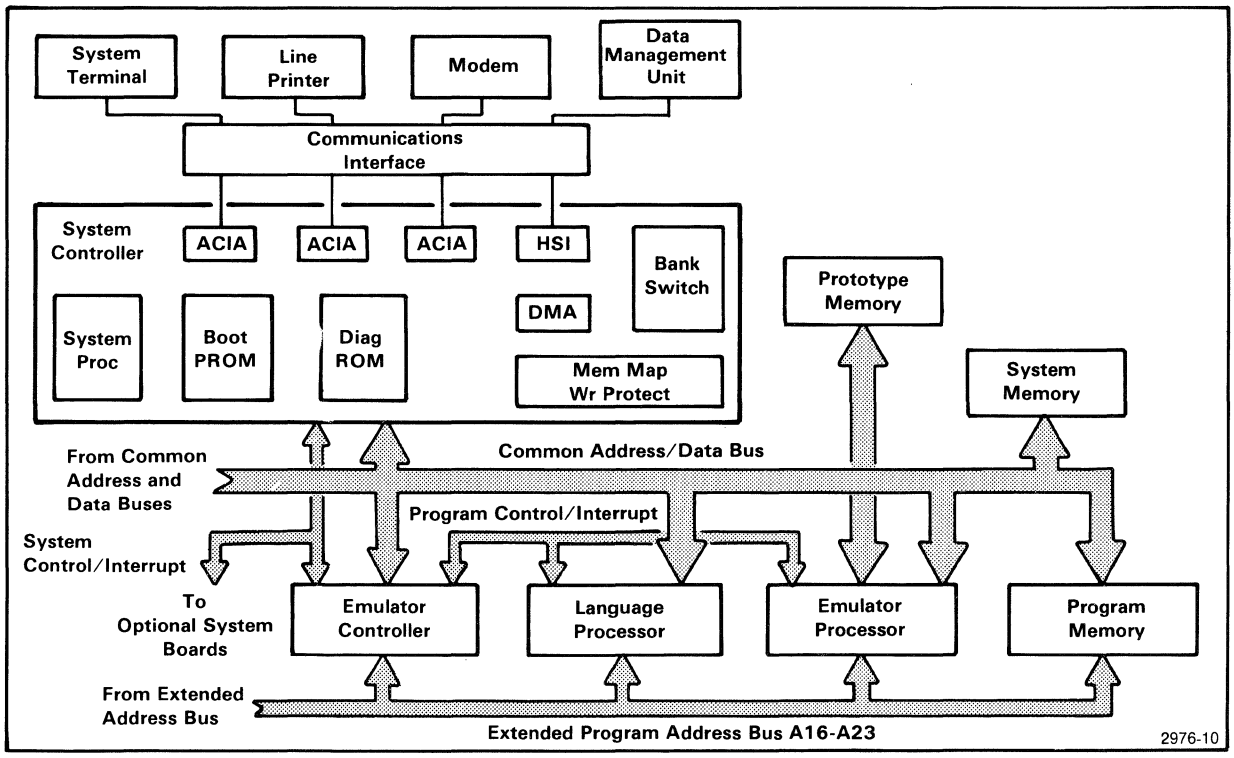


Fig. 3-6. 8301 MDU block diagram.

POWER-UP TEST NO. 1

Test

Initialization Test

Function

This test presets the 8301 to ensure that the remaining power-up tests have an initial starting reference. This is the only power-up test that does not provide an error code indication to the LEDs or to the System Terminal.

Circuit Board Involved

System Controller. (See Fig. 3-6.)

Error Codes Encountered

None.

Description

Reset RS-232 Ports

1. The test writes to the control byte of each RS-232-C I/O port address and enables the master reset in each ACIA.

Disable RS-232 Ports

2. The test writes to the control byte of each RS-232-C I/O port address and disables the transmitter and receiver in each ACIA.

Disable DMA

3. The test writes to the control byte of I/O port address 98 (DMA mode set register) and disables all four DMA channels.

Disable HSI and DMA Interrupts

4. The test writes to the control byte of I/O port address E9 (HSI and DMA control port) and disables the interrupts to the HSI and DMA devices.

Disable Disc Interrupt and Select Diagnostic ROM

5. The test writes to the control byte of I/O port address EA (Manufacturing Test control port). The control byte is set to disable the interrupt to the manufacturing test port and select the Diagnostic ROM.

Disable Interval Timer Interrupt

6. The test writes to the control byte of I/O port address EC (interval timer control port) and disables the interval timer interrupt.

Select System Memory

7. The test writes to the control byte of I/O port address EE (bank switching latch) and selects the 16K---32K bank in system memory (Bank 02).

POWER-UP TEST NO. 2

Test

Instruction Set Test.

Function

This test functionally verifies the 2650 instruction set by executing a set of tests that determine the data integrity of the registers and the correct execution of the instruction set. All addressing modes for a given instruction are also tested. If an error results from an unsuccessful comparison of expected results to the actual results, an error code is displayed on the System Terminal in register R0.

Circuit Boards Involved

System Controller, Communications Interface, and System Terminal. (See Fig. 3-6.)

Error Code Encountered

Error Code	Title	Encountered During Steps
R0=04	Instruction set test error	1 and 2

Description

Executing 2650 Instructions

1. A combination of tests are executed containing 2650 instructions. The actual results of these tests are compared to expected or predetermined values. If an error exists, the error code R0=04 is displayed on the System Terminal in register R0.

2. Additional tests (as described in step 1) are executed until all instructions are tested. The 2650 instructions WRTD, REDD, WRTD, and REDC are not used in the 8301 and are thus not tested. The HALT instruction is also not tested. If an error exists during the execution of any instruction, the error code R0=04 is displayed on the System Terminal in register R0.

POWER-UP TEST NO. 3

Test

Diagnostic ROM Checksum Test.

Function

This test checks each data byte in the ROM for correctness by using a 16-bit checksum calculation method. Error codes are displayed on LEDs or on the System Terminal if any error is detected throughout the test.

Circuit Boards Involved

System Controller, System RAM, Communications Interface, and System Terminal. (See Fig. 3-6.)

Error Codes Encountered

Error Code	Title	Encountered During Step
LEDs= 0 0 0 1 0	Diagnostic ROM checksum memory error	1
RO=OF	Diagnostic ROM checksum error	3 and 4

Description

Load Data Address

1. The low and high bytes of the Diagnostic ROM starting address are loaded into system memory. Both bytes are compared to ensure that they were actually loaded into memory. If an error is detected at either location, the error code 0 0 0 1 0 is displayed on the LEDs.

Checksum Calculations

2. The checksum is contained in the RO (low byte checksum) and R1 (high byte checksum) registers of the 2650A-1 microprocessor. The data byte from each ROM address is added to the low byte checksum (RO). The carry from the low byte is added to the high byte checksum (R1) and the end around carry from the high byte is added to the low byte checksum (RO). All bits in the checksum (RO and R1) are rotated one bit to the left, with the high byte carry again added to RO. The ROM address is then incremented by one and the calculations continue with the new data byte. These calculations continue until the contents of ROM address OFFD have been added to the checksum registers. Before comparing the high and low byte checksums, the low byte checksum is stored in register R3 and the high byte checksum is retained in register R1.

Compares High Byte Checksum

3. The expected high byte checksum is at address OFFE in the Diagnostic ROM. This expected checksum from address OFFE is loaded into system memory and compares this checksum with the actual high byte checksum retained in register R1. If they do not match, the error code RO=OF is displayed in RO on the System Terminal.

Compares Low Byte Checksum

4. The expected low byte checksum is at address OFFF in the Diagnostic ROM. This expected checksum from address OFFF is loaded into system memory and compares this checksum with the actual low byte checksum stored in register R3. If they do not match, the error code RO=OF is displayed in RO on the System Terminal.

NOTE

If an error code is displayed on the System Terminal, examine registers R1 (high byte) and R3 (low byte) to determine the actual checksum.

POWER-UP TEST NO. 4

Test

System Memory Test (4K---32K)

Function

This test verifies the data integrity for memory locations 4K---32K (1000---7FFF) in system memory during both read and write operations. The address of each location is also checked for correctness. Error codes are displayed on LEDs or on the System Terminal if any error is detected throughout the test.

Circuit Boards Involved

System Controller, System RAM, Communications Interface, and System Terminal. (See Fig. 3-6.)

Error Codes Encountered

Error Code	Title	Encountered During Steps
LEDs= 0 0 0 0 0	System memory address error	1
R0=0D	System memory error (32K---4K)	3
R0=0E	System memory error (4K---32K)	4

Description

Load Starting Address

1. The starting address (1000) is loaded into system memory. The data bytes containing the starting address are compared to ensure that the correct address was actually loaded into memory. If an error is detected, the error code 0 0 0 0 0 is displayed on the LEDs.

Generate Data in Memory (4K---32K)

2. Data is generated in system memory locations by storing the low byte of each address in that memory location. The locations are accessed sequentially. The test starts at memory location 1000 (4K) in system memory and increments to the top of memory at 7FFF (32K).

Compare Data (32K--4K)

3. The test starts at the top of system memory (7FFF), reads the data again, compares it to the lower byte of the address, complements the data, and stores it back in memory again. This is repeated for each location down to and including address 1000 (4K). If an error is detected at any location, the error code R0=0D is displayed on the System Terminal in register R0.

Compare Data (4K---32K)

4. The test once again starts at system memory address 1000 (4K) and increments to the top of system memory at 7FFF (32K). This time the test reads the data from memory, complements the data, and compares it to the lower byte of the address for each memory location. If an error is detected at any location, the error code R0=0F is displayed on the System Terminal in register R0.

POWER-UP TEST NO. 5

Test

Interval Timer Test

Function

This test is executed in two parts: non-interrupted and interrupted. The non-interrupted part verifies that the interval timer does not interrupt the 2650A-1 microprocessor when the interval timer interrupt is disabled. The interrupted part verifies that the interval timer does interrupt the 2650A-1 microprocessor when the interval timer interrupt is enabled. Error codes are displayed on LEDs or the System Terminal if any error is detected throughout the test.

Circuit Boards Involved

System Controller, System RAM, Communications Interface, and System Terminal. (See Fig. 3-6.)

Error Codes Encountered

Error Codes	Title	Encountered During Steps
LEDs= 0 0 1 0 0	Interrupt handler memory error	3 and 5
R0=0B	Non-Interrupted interval timer error	3
R0=0A	Interrupted interval timer error	5

Description

Non-Interrupted Interval Timer Test

1. The 2650A-1's on-chip interrupt is enabled.
2. The test writes to the control byte of the interval timer I/O port address (EC) and disables the interval timer interrupt.

Non-Interrupted Interval Timer Test (Cont.)

3. A flag location in system memory is chosen to represent the presence or absence of an interrupt. Ones are loaded into this flag memory location. It then passes through a delay loop 64K times. After each pass through the delay loop, the flag memory location is checked to see if there has been any change to the ones previously loaded in that location. If an interrupt occurs, zeros are loaded into the flag memory location. After the zeros are loaded, the memory location is checked to ensure the zeros are actually loaded. If not, the error code 0 0 1 0 0 is displayed on the LEDs.

   When the flag memory location is checked after each pass through the delay loop, no interrupts should have been generated and the memory location should still be loaded with ones. If the memory location is not ones, an interrupt has occurred and the error code R0=0B is displayed in register R0 on the System Terminal.

Interrupted Interval Timer Test

4. The test writes to the control byte of the interval timer I/O port address (EC) and enables the interval timer interrupt.

5. Ones are again loaded into the flag memory location. It then passes through the delay loop as in step 3. This time, the flag memory location should be changed on the first interrupt generated. When the interrupt occurs, zeros are again loaded into the flag memory location and the memory location is checked to ensure they are actually loaded. If the zeros are not loaded, a memory error code 0 0 1 0 0 occurs and is displayed on the LEDs.

   If the test passes through the delay loop 64K times without an interrupt being detected, the error code R0=0A is displayed in register R0 on the System Terminal.

Disable Interval Timer

6. The test writes to the control byte of the interval timer I/O port address (EC) and disables the interval timer interrupt. This restores the interval timer to the same conditions as at the start of this power-up test.

POWER-UP TEST NO. 6

Test

Bank Switch Test

Function

This test checks the ability of the 2650A-1 microprocessor to address its upper 16K address space. The 2650A-1 has only 15 address lines, with the ability to address 32K of address space (0000---7FFF). Bank switching provides the 2650A-1 with the ability to address up to 64K in both system and program memories. Bank switching permits 16K blocks of system and program memory addresses (on even 16K boundaries) to be switched into the 2650A-1s upper 16K address space (16K---32K). Bank switching is used whenever the 2650A-1 is addressing above 16K in system memory or addressing any portion of program memory. This test checks the bank switching of three 16K blocks of memory: 16K---32K in system memory, 0---16K in program memory, and 16K---32K in program memory.

Circuit Boards Involved

System Controller, System RAM, Program Memory, Communications Interface, and System Terminal. (See Fig. 3-6.)

Error Codes Encountered

Error Code	Title	Encountered During Steps
LEDs= 0 0 0 1 1	Bank switch memory error	1, 2, 3, 4, and 5
R0=0C	Bank switch logic error	2, 4, and 5

NOTE

Refer to Section 5, Functional Procedures No. 5 (Bank Switching) for a more detailed explanation of how the data bits associated with I/O port address EE are set. The data byte associated with I/O port address EE determines which memory bank is selected for bank switching.

Description

Zero Out Three Memory Banks

1. The test zeros out the lower 256 bytes of three 16K memory banks: 16K---32K in program memory, 0---16K in program memory, and 16K---32K in system memory. As the bytes are zeroed out a comparison is made. If any byte does not zero out, an error code 1 1 0 0 0 is displayed on the LEDs.

Bank Switching Tests

2. Ones are written into the lower 256 bytes of the 16K---32K block of program memory. As the ones are written into each memory byte a comparison is made. If any byte does not contain all ones, an error code 1 1 0 0 0 is displayed on the LEDs. The test then compares the other two memory banks to this memory bank, to verify that they are zeroed out. If the comparison shows that any data byte is not zeroed, the error code R0=0C is displayed on the System Terminal in register R0.

3. The test zeros out the lower 256 bytes of the 16K---32K block of program memory, which was loaded with ones. As the bytes are zeroed out a comparison is made. If any byte does not zero out an error code 1 1 0 0 0 is displayed on the LEDs.

4. Bank switching tests are conducted on the next memory bank, 0---16K in program memory. The same procedures are followed as described in steps 2 and 3. If an error is detected, the error codes are the same as described in steps 2 and 3.

5. Bank switching tests are conducted on the next memory bank, 16K---32K in system memory. The same procedures are followed as described in steps 2 and 3. If an error is detected, the error codes are the same as described in steps 2 and 3.

POWER-UP TEST NO. 7

Test

DMA Controller Test

Function

This test checks the DMA address and terminal count registers, performs a memory-to-memory transfer operation to two locations in both system memory and program memory, and compares the transferred data to the original data. If an error is detected in any of the tests, an error code is displayed on the System Terminal or the bank of LEDs.

Circuit Boards Involved

System Controller, System RAM, Program Memory, Communications Interface, and System Terminal. (See Fig. 3-6.)

Error Codes Encountered

Error Code	Title	Encountered During Steps
R0=06	DMA register error	3
LEDs= 0 0 1 0 1	DMA memory fault	4
R0=08	DMA logic error	11

Description

Disable DMA Ports

1. The test addresses I/O port E9 and writes zeros into the data byte. This disables the HSI interrupt and the interrupts to the four DMA channels.

2. The test addresses I/O port 98 and writes zeros into the data byte. This disables the four DMA channels.

Stuck at One and Zero Test

3. Ones are written into the address and terminal count registers of each DMA channel. The test reads the address and terminal count registers and compares the readings to the value written into the registers. If there is an error in any of the comparisons, the error code R0=06 is displayed in register R0 on the System Terminal. Zeros are then written into the address and terminal count registers of each DMA channel. The test reads the address and terminal count registers and compares the

readings to the value written into the registers. If there is an error in any of the comparisons, the same error code (R0=06) is displayed on the System Terminal.

Generate Data for Memory-to-Memory Transfers

4. The test generates 256 data bytes at addresses 1000---10FF in system memory. The data bytes are generated by writing the lower byte of the address into each system memory location. Each data byte is then compared to the address. If an error is detected, an error code 1 0 1 0 0 is written to the LEDs, signifying a memory error.

Memory-to-Memory Transfer Tests

5. The test addresses I/O ports E9 and 98, disabling the interrupts and DMA channels (as in steps 1 and 2).

6. The test programs DMA channels 0 and 1 for a DMA memory-to-memory transfer of 256 data bytes from a starting address of 1000 in system memory to a starting address of 4000 in system memory. Refer to Section 5, Functional Procedure No. 6 (Programming DMA Controller for Memory-to-Memory Transfer) for a more detailed explanation of how to program the DMA for a memory-to-memory transfer.

7. The test enables the interrupts and DMA channels. This initiates the memory-to-memory transfer. DMA channel 0 accesses system memory at the starting address, reads the data, and stores it in a holding latch. DMA channel 1 reads the data from the holding latch and writes the data into system memory at the starting address where the data is transferred. This procedure continues for each data byte until the terminal count register in both channels reach zero. Refer to Section 5, Functional Procedure No. 7 (DMA Controller Memory-to-Memory Transfer Operation) for a more detailed explanation of DMA memory-to-memory transfer operations.

8. The test programs and initiates a memory-to-memory transfer of 256 data bytes from a starting address of 4000 in system memory to a starting address of 0000 in program memory. The transfer procedure is the same as in steps 6 and 7.

9. The test programs and initiates a memory-to-memory transfer of 256 data bytes from a starting address of 0000 in program memory to a starting address of 4000 in program memory. The transfer procedure is the same as in steps 6 and 7.

10. The test programs and initiates a memory-to-memory transfer of 256 data bytes from a starting address of 4000 in program memory to a starting address of 2000 in system memory. The transfer procedure is the same as in steps 6 and 7.

Compare Original and Transferred Data

11. The test compares the 256 data bytes from the original starting address of 1000 in system memory with the 256 data bytes transferred to the starting address of 2000 in system memory. The comparison is made after the data has been transferred four times, as shown in Fig. 3-7. If the original data does not match the transferred data, the error code RO=08 is displayed in register RO on the System Terminal.

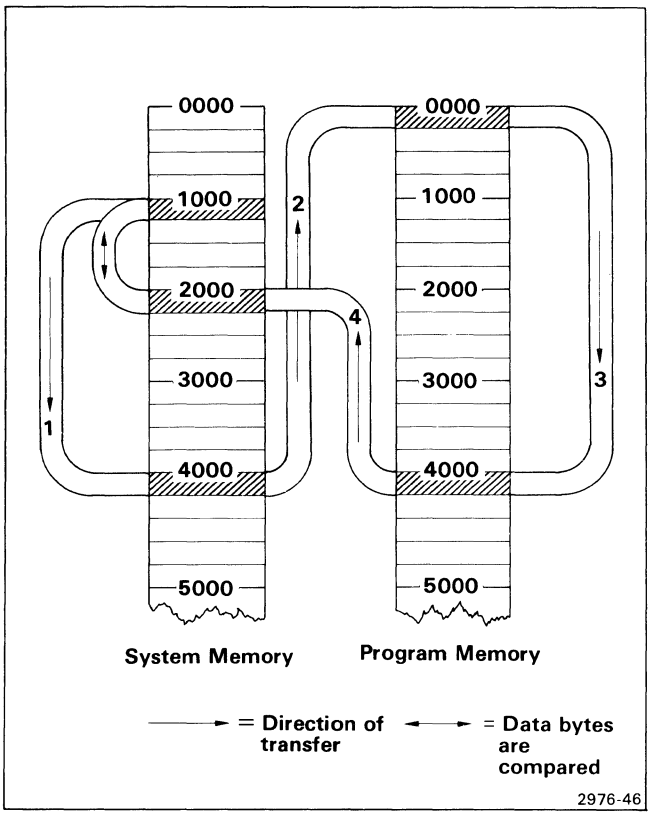


Fig. 3-7. Memory map of DMA data transfer.

POWER-UP TEST NO. 8

Test

RAM-Based Test Loader

Function

This test loads the System Memory Test (0---4K) and Boot ROM Checksum Test from the Diagnostic ROM into RAM (system memory). The Diagnostic ROM occupies addresses 0000---0FFF (0---4K). These tests are loaded into system memory at a starting address above 1000. When finished this test branches to the locations in RAM. The last two power-up tests are executed from RAM. The System Memory Test (0---4K) is the same routine as used in Power-Up Test No. 4. A template is used to change to addresses from 4K---32K to 0---4K.

Circuit Boards Involved

System Controller and System RAM. (See Fig. 3-6.)

Error Code Encountered

Error Code	Title	Encountered During Steps
LEDs= 0 0 0 0 1	RAM-Based test loader memory error	1, 2, and 3

Description

Load System Memory Test

1. The System Memory Test and the template from the Diagnostic ROM are loaded into system memory (RAM). The data written into RAM is compared to the data in ROM. If any data byte does not match, an error code 0 0 0 0 1 is displayed on the LEDs.

   This System Memory Test is the same test performed in Power-Up Test No. 4. The template modifies this test so that the system memory can be tested from 0---4K instead of 4K---32K.

Load Boot ROM Checksum Test

2. The Boot ROM Checksum Test is the same test performed in Power-Up Test No. 3. The template modifies this test so that the Boot ROM Checksum Test can be conducted. The Diagnostic ROM Checksum Test and the template from the Diagnostic ROM are loaded into system memory (RAM). The data written into RAM is compared to the data in ROM. If any data byte does not match an error code 0 0 0 0 1 is displayed on the LEDs.

Branch to Mini Test Controller

3. When the RAM Base Test Loader has finished loading the preceding tests into RAM (system memory), the test branches to RAM for the execution of the last two power-up tests.

POWER-UP TEST NO. 9

Test

System Memory Test (0---4K)

Function

This is the first of two tests executed from RAM. This test verifies data integrity for system memory locations 0---4K during both read and write operations. This test is the same as Power-up Test No. 4 with a template that modifies the memory addressing. Error codes are displayed on the System Terminal if any error is detected throughout the test.

Circuit Boards Involved

System Controller, System RAM, Communications Interface, and System Terminal. (See Fig. 3-6.)

Error Codes Encountered

Error Code	Title	Encountered During Steps
R0=2D	System memory error (4K---0)	2
R0=2E	System memory error (0---4K)	3

Description

Generate Data In Memory (0---4K)

1. Data is generated in system memory locations by storing the lower byte of the address in each memory location accessed. The test starts at the bottom of memory (0000) and increments to address 0FFF.

Compare Data (4K---0)

2. The test starts at system memory address 0FFF, reads the data stored, compares it to the lower byte of the address, complements the data, and stores it back into memory again. This procedure is repeated for each location down to and including address 0000. If an error is detected at any location, the error code R0=2D is displayed on the System Terminal in register R0.

Compare Data (0---4K)

3. The test once again starts at system memory address 0000 and increments to 0FFF. This time the test reads the data from memory, complements the data, and compares is to the lower 8 bits of the address for each memory location. If an error is detected at any location, the error code R0=2E is displayed on the System Terminal in register R0.

POWER-UP TEST NO. 10

Test

Boot ROM Checksum Test

Function

This is the second of two tests executed from RAM. This test checks each data byte in the Boot ROM for correctness, using a 16-bit checksum calculation method. Error codes are displayed on the System Terminal if any error is detected throughout the test.

Circuit Boards Involved

System Controller, System RAM, Communications Interface, and System Terminal. (See Fig. 3-6.)

Error Code Encountered

Error Code	Title	Encountered During Step
R0=2F	Boot ROM checksum error	3 and 4

Description

Load Boot ROM Starting Address

1. The high and low bytes of the Boot ROM starting address are loaded into system memory.

Checksum Calculations

2. The data byte from each ROM address is added to the low byte checksum (R0). The checksum calculations are performed in the same manner as described in Power-Up Test No. 3. The ROM address is incremented and the calculations continue until the contents of address 03FD has been added to the checksum. Before comparing the high and low bytes of the checksum, the low byte checksum is stored in register R3 and retains the high byte checksum in register R1.

Compares High Byte Checksum

3. The expected high byte checksum is at address 03FE in the Boot ROM. This expected checksum from address 03FE is loaded into system memory and compares this checksum to the actual high byte checksum retained in register R1. If they do not match, the error code R0=2F is displayed in R0 on the System Terminal.

Compares Low Byte Checksum

4. The expected low byte checksum is at address 03FF in the Boot ROM. This expected checksum from address 03FF is loaded into system memory and compares this checksum to the actual low byte checksum stored in register R3. If they do not match, the error code R0=2F is displayed in R0 on the System Terminal.

PART 2 --- VERSION V2.X

The power-up tests for the second version of the diagnostic ROM are described in the following paragraphs.

MODE SWITCH

The mode switch shown in Figures 3-2 and 3-3 together with the matching text also applies to this version of the power-up tests. Some switch position functions shown in Fig. 3-4 are modified for this version and will be discussed next.

SWITCH-SELECTABLE OPTIONS

Figure 3-8 is the mode switch decision tree for Version V2.x. This figure will be referred to often in the following paragraphs. This decision tree has two main branches: normal (boot) branch and CFM (no boot) branch. The position of the mode switches determine the various options available. Switch position 6 is read first and then the remaining switches are read in a consecutive descending order. Switch position 6 selects one of the main branches as shown in Fig. 3-8.

Normal Mode

The normal (boot) operating mode is selected when the 8301 is operating normally (no failure indicated during power-up tests) and you want to boot the operating system from the Data Management Unit (DMU). When this mode is selected, the following options are available:

1. Power-up diagnostics can be run or bypassed.
2. If an error is detected during the power-up tests you can enter the CFM or loop on the error, dependent on the setting of switch position 4.
3. Selection of booting from 8550 disc or 8540 ROM-Diagnostics.

NOTE

Version V2.x diagnostic and boot ROMs are used in both the 8301 and 8540 units. Switch position 3 is set to "0" for 8301 installations and to "1" for 8540 installations.

For normal 8301 operation conditions, set all mode switch positions to "0" as shown in Table 3-6.

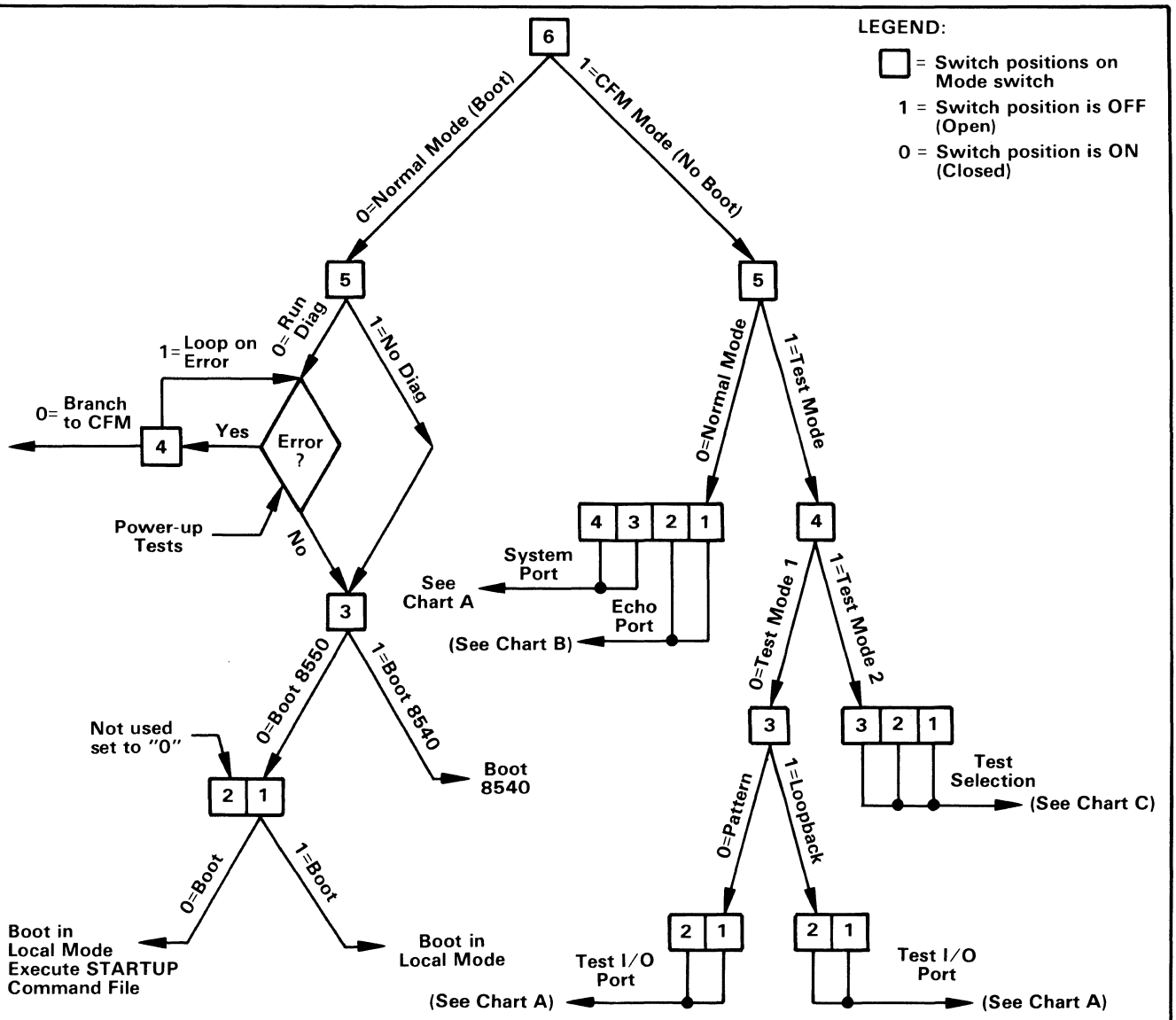


Chart A	
SYSTEM PORTS & TEST I/O PORTS	
PORT	DESIG [a]
System Terminal	00
Auxiliary	01
Remote	10
HSI/DMU	11

Chart B	
ECHO PORTS	
PORT	DESIG [a]
No Echo Port	00
Auxiliary	01
Remote	10
HSI/DMU	11

Chart C	
TEST SELECTION - TEST MODE 2	
TEST	DESIG [a]
2650 CPU	000
Refresh Interrupt	001
Parity Error Intr	010
Bank + Page Select	011
Sys Memory 0000—3FFF	100
DMA (System—System)	101

[a] Designation indicates switch positions from left to right as shown in this figure.

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Fig. 3-8. Mode switch decision tree (Version V2.x).

Table 3-6
Mode Switch Settings for 8301 Normal Operating Mode
(Version V2.x)

Switch Position	Switch Setting	Selected Option
6	0 (ON or Closed)	Normal mode (boot)
5	0 (ON or Closed)	Run power-up tests
4	0 (ON or Closed)	Branch to CFM on Error
3	0 (ON or Closed)	Boot from 8550
2	0 (ON or Closed)	Switch is not used (reserved)
1	0 (ON or Closed)	Boot operating system from 8550 disc.

CFM Mode

The CFM operating mode is selected by either of the following methods:

1. During normal operations, if one of the power-up tests fails, an error code is displayed on the LEDs and the power-up test branches to the CFM. In this mode, the CFM is preconfigured to use the System Terminal as the system port with no echo port. This means the CFM user commands can be entered and displayed on the System Terminal.

2. The other method of selecting the CFM is to set the mode switch position 6 to "1" (OFF or Open). This method fully utilizes the capabilities of the CFM. The CFM user commands can be entered and displayed on a choice of peripherals. It also permits the selection of either CFM normal mode, Test Mode 1, or Test Mode 2. Refer to Fig. 3-8.

Additional information on using the CFM operating mode is included later in Part 3 of this section.

POWER-UP/RESTART SEQUENCE

The power-up/restart sequence for Version V2.x of the 8301 is shown in the accompanying flow diagram, Fig. 3-9. The following steps describe this sequence. (Refer also to Fig. 3-8.)

1. The boot ROM reads mode switch position 6.

2. If switch position 6 is set to "1" (OFF or Open), the CFM mode is selected; mode switches 5, 4, 3, 2, and 1 are read to determine the mode of operation and the tests to be performed by the CFM. If switch position 6 is set to "0" (ON or Closed), the normal operating mode is selected and switch position 5 is read.

3. If switch position 5 is set to "1", the boot ROM is selected; the power-up tests are bypassed, and switch position 3 is read. If switch position 5 is set to "0", the power-up diagnostics are selected and executed. If the power-up tests fail, switch position 4 is read and an error message is displayed on the LEDs. If switch position 4 is set to "1", the power-up tests loop on the error. If switch position 4 is set to "0", the test branches to the CFM for further analysis and troubleshooting. If the power-up tests are passed, the boot ROM is selected and mode switch position 3 is read.

4. If switch position 3 is set to "1", the 8540 is selected for boot-up operations. If this switch is set to "0", the 8550 is selected for boot-up operations and switch position 1 is read.

5. If switch position 1 is set to "1", the 8301 boots in the Terminal Mode (Non-Local Mode). If this switch is set to "0", the 8301 boots the normal operating system from the disc in the DMU. This is the Local Mode.

POWER-UP TESTS

The eleven power-up tests of version V2.x are sequentially executed unless an error is detected during any of the tests. At which time the program displays an error code on the LEDs and looks at mode switch position 4. Switch position 4 permits looping on the error or entering the CFM. Refer to Figures 3-8 and 3-9.

TEST AND ERROR CODES

There are two codes displayed on LEDs: test codes and error codes. Test codes are displayed on the LEDs at the start of each power-up test. Error codes are displayed on the LEDs when an error is detected during the running of the tests.

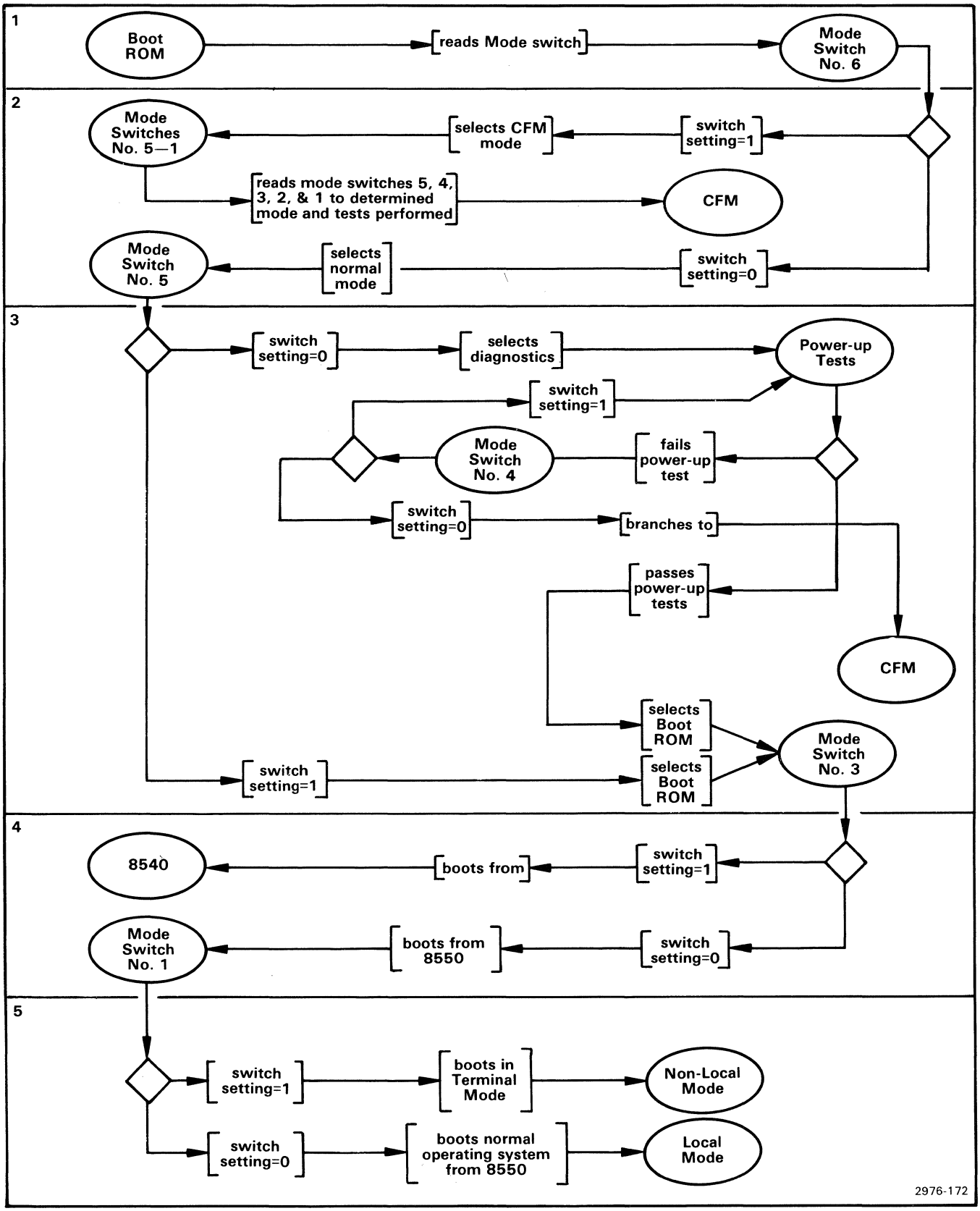


Fig. 3-9. 8301 power-up/restart sequence (Version V2.x).

LED Displays

There are three sets of LED displays: (Refer to Fig. 3-10.)

- Five LEDs on the System Controller board for diagnostic test code display.
- Eight LEDs on the System RAM board arranged in two groups:
  1. Five LEDs for diagnostic error code display.
  2. Three LEDs for showing status of the System RAM board.
- One LED on Front Panel labeled SELF TEST.

The LEDs on both boards are arranged with the most significant LED on the left as viewed from the component side of the board.

NOTE

To view the LED displays, the top cover must be removed from the unit. Refer to Section 2, Installation, of this manual for directions on removal of the top cover.

Test Codes

Before each power-up test is executed, a test code is sent to the two groups of LED displays. The group of five LEDs on the System Controller board display the test module number. The group of five LEDs on the System RAM board are zeroed out. Table 3-7 shows the test codes that are assigned to each power-up test.

Error Codes

When an error is detected during execution of the power-up tests, the program transfers control to the error routine. This routine displays the error code on the group of five LEDs on the System RAM board. Table 3-7 shows the error codes that are assigned to each test code and power-up test.

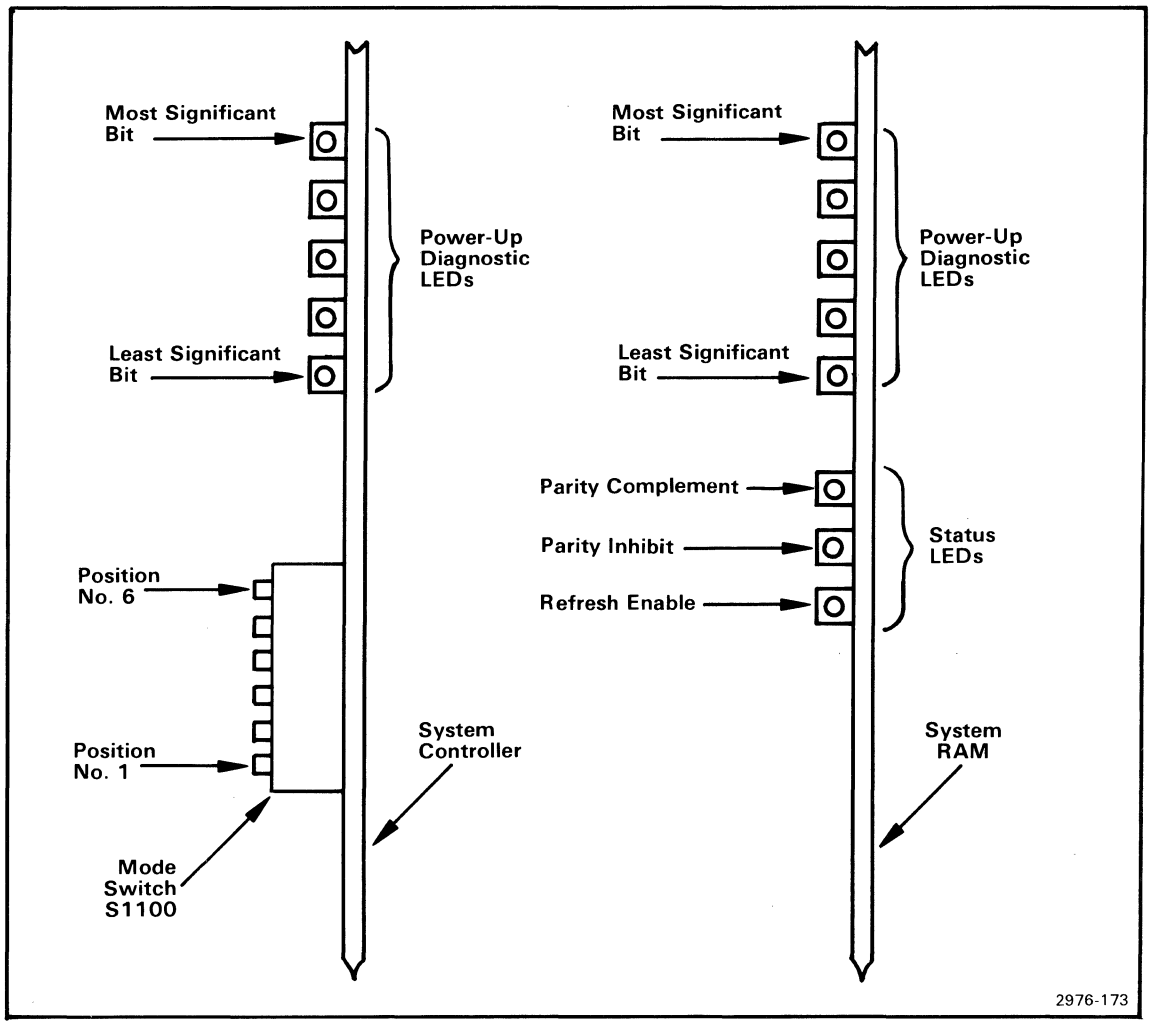


Fig. 3-10. Mode selector switch and power-up LEDs.

Front Panel LED

The LED on the Front Panel remains lighted throughout the running of the power-up tests and during the display of an error code. This is the last LED to be turned off, signifying the power-up tests are completed and no error detected.

NOTE

Both the test code and error code must be used to identify an error. In general, the error code is displayed prior to executing the test. Thus if a test hangs, the proper error code is displayed.

Table 3-7
Index of Test Codes and Error Codes

Power-Up Test No.	Title of Test	LED Indicators: Sys Cont Test Codes	LED Indicators: System RAM Error Codes	Fault
		1 1 1 1 1	1 1 1 1 1	System completely hung
1	Initialization	0 0 0 0 0	0 0 0 0 0	Hung
2	Instruction Set Test	0 0 0 0 1	0 0 0 0 0	CPU hung or failed
		0 0 0 0 1	0 0 1 0 0	System RAM board problem
3	Diagnostic ROM Checksum Test	0 0 0 1 0	0 0 0 0 0	Bad checksum
4	Memory Refresh Interrupt Test	0 0 0 1 1	0 0 0 0 0	Hung waiting for interrupt
		0 0 0 1 1	1 1 0 0 0	Wrong interrupt
		0 0 0 1 1	1 1 0 0 1	Parity error
5	Boot ROM Checksum Test	0 0 1 0 0	0 0 0 0 0	Checksum error
		0 0 1 0 0	0 0 1 0 0	Move data error
6	Parity Error Interrupt Test	0 0 1 0 0	0 0 0 0 1	No parity error interrupt
		0 0 1 0 0	1 1 0 0 0	Wrong interrupt
7	Bank Switch and Page Switch Tests	0 0 1 0 1	0 0 0 0 0	Bank error
		0 0 1 0 1	0 0 0 0 1	Page error
8	System Memory (OK--16K) Test	0 0 1 1 0	0 0 0 0 0	Non-parity error
		0 0 1 1 0	1 1 0 0 1	Parity error
		0 0 1 1 0	0 0 1 0 0	Move data error
9	DMA Test (System-to-System)	0 0 1 1 1	1 1 0 0 1	Parity error
		0 0 1 1 1	0 0 0 1 0	Hung during DMA
		0 0 1 1 1	0 0 0 1 1	Data error

Table 3-7 (cont)

Power-Up Test No.	Title of Test	LED Indicators: Sys Cont Test Codes	LED Indicators: System RAM Error Codes	Fault
10	System/Program Memory Test	0 1 0 0 1	x x x x x	Program OK--16K
		0 1 0 1 0	x x x x x	Program 16K--32K
		0 1 0 1 1	x x x x x	Program 32K--48K
		0 1 1 0 0	x x x x x	Program 48K--64K
		0 1 1 0 1	x x x x x	System 16K--32K
		0 1 1 1 0	x x x x x	System 32K--48K
		0 1 1 1 1	x x x x x	System 48K--64K
		x x x x x	0 0 0 0 0	Data error
		x x x x x	1 1 0 0 1	Parity error
11	DMA Test (System-to-Program)	1 0 0 0 0	1 1 0 0 1	Parity error
		1 0 0 0 0	0 0 0 1 0	Hung during DMA
		1 0 0 0 0	0 0 0 1 1	Data Error

NOTE

The two error code columns listed in Table 3-7 are referred to in this manual as X X X X X / X X X X X.

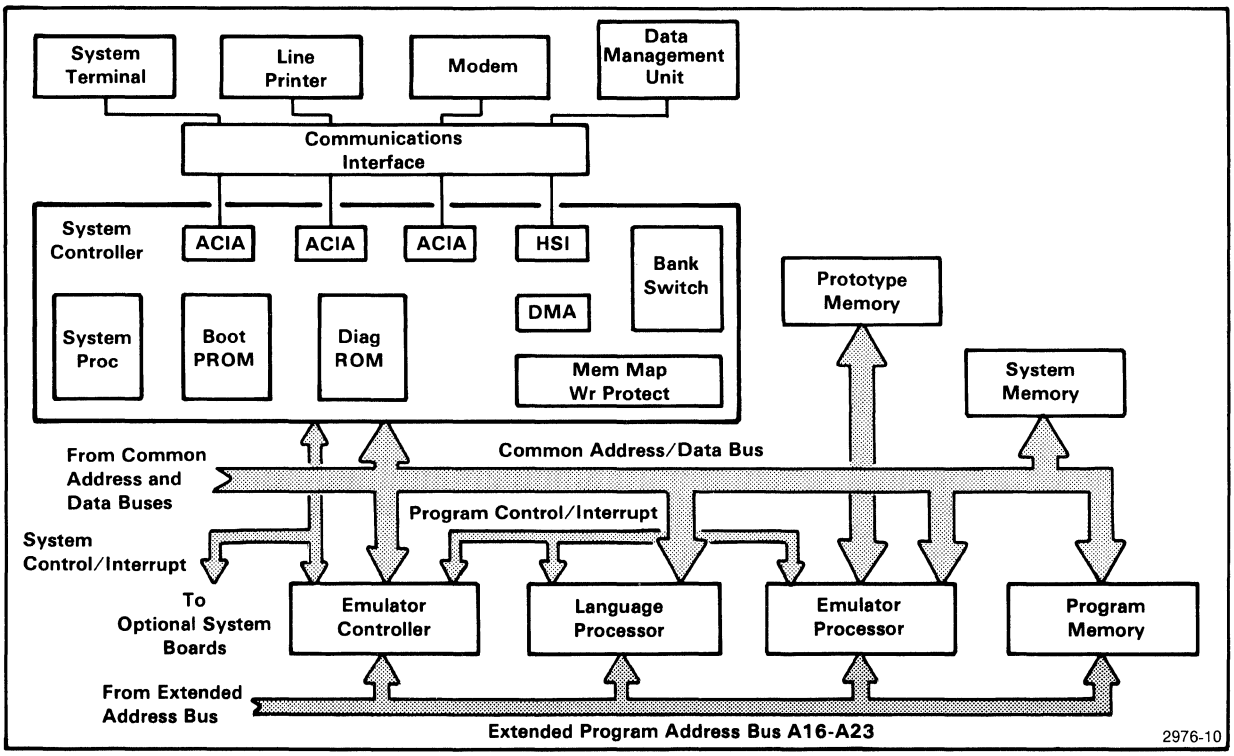


Fig. 3-11. 8301 MDU block diagram.

POWER-UP TEST NO. 1

Test

Initialization

Function

This test presets the 8301 to ensure that the remaining power-up tests have an initial starting reference.

Circuit Boards Involved

System Controller, System RAM and Program Memory. (See Fig. 3-11.)

Error Code Encountered

Error Code	Fault
0 0 0 0 0 / 0 0 0 0 0	Hung

Description

Resets and Disables RS-232-C Ports

1. The test writes a data byte "03" to each RS-232-C I/O port address (CA, CC and CE) enabling the master reset in each ACIA.

2. The test writes a data byte "15" to each RS-232-C I/O port address (CA, CC and CE) disabling the transmitter and receiver in each ACIA.

Disables Interrupts and Clears Registers

3. The test writes a data byte "00" to the following I/O port addresses:

I/O Port Address	Function
98	Disables DMA (DMA mode set register)
E9	Disables HSI and DMA interrupts
EC	Disables interval timer interrupt
F5	Clears extended jump register
F6	Clears extended address register
EA	Disables Manufacturing Test Port interrupt

4. The test clears LEDs on the System Controller and System RAM boards. The Front Panel LED remains lit through the running of all power-up tests It is turned off when the power-up tests are completed and no errors detected.

Selects and Resets Initial Function

5. The test selects the Diagnostic ROM and Bank 02 of system memory (16K--32K). The page switch register is also reset.

6. The test sets the extended bank register to "1's" by writing data byte "FF" to I/O port address F4. This selects the first 64K of program memory.

7. The test writes data byte "70" to I/O port addresses B8 and B9 for the Program Memory board(s) which:

   Resets the memory relocation counters.
   Disables the memory relocation circuitry.
   Disables the extended bank comparator.

POWER-UP TEST NO. 2

Test

Instruction Set Test

Function

This test functionally verifies the 2650 instruction set by executing a set of tests that determine the data integrity of the registers and the correct execution of the instruction set.

Circuit Board Involved

System Controller and System RAM. (See Fig. 3-11.)

Error Code Encountered

Error Code	Fault
0 0 0 0 1 / 0 0 0 0 0	CPU hung or failed
0 0 0 0 1 / 0 0 1 0 0	System RAM board problem

Description

1. A combination of tests are executed containing 2650 instructions. The actual results of these tests are compared to expected or predetermined values. If an error exists, the error code in displayed on the LEDs. If memory access is denied, the error code is also displayed.

POWER-UP TEST NO. 3

Test

Diagnostic ROM Checksum Test

Function

This test checks the Diagnostic ROM for correctness by using a 16-bit checksum calculation method.

Circuit Board Involved

System Controller and System RAM. (See Fig. 3-11.)

Error Code Encountered

Error Code	Fault
0 0 0 1 0 / 0 0 0 0 0	Bad checksum

Description

1. This test starts at ROM address OFFD. This location is read and a checksum calculated using a 16-bit checksum calculation method. The address is decremented and the calculations continued to address 0000.

2. The calculated checksum is compared with the stored checksum at locations OFFE and OFFF.

3. If an error is detected, an error code is displayed on the LEDs.

POWER-UP TEST NO. 4

Test

Memory Refresh Interrupt Test

Function

This test verifies that the memory refresh logic and the system interrupt circuitry is functioning correctly.

Circuit Boards Involved

System Controller and System RAM. (See Fig. 3-11.)

Error Codes Encountered

Error Codes	Fault
0 0 0 1 1 / 0 0 0 0 0	No interrupt
0 0 0 1 1 / 1 1 0 0 0	Wrong interrupt
0 0 0 1 1 / 1 1 0 0 1	Parity error

Description

1. The memory refresh interrupt circuitry is enabled by writing data byte "F9" to I/O port address D2. The test then enters a timing loop waiting for the refresh interrupt to occur. If a correct interrupt occurs the refresh interrupt is turned off, cleared by the interrupt handler routine, and the next test started. An error code is displayed on the LEDs if no interrupt occurs, the wrong interrupt occurs, or a parity interrupt occurs.

POWER-UP TEST NO. 5

Test

Boot ROM Checksum Test

Function

This test checks the Boot ROM for correctness by using a 16-bit checksum calculation method.

Circuit Boards Involved

System Controller and System RAM. (See Fig. 3-11.)

Error Codes Encountered

Error Codes	Fault
0 0 1 0 0 / 0 0 0 0 0	Checksum error
0 0 1 0 0 / 0 0 1 0 0	Move data error

Description

1. This test is similar to the Diagnostic ROM Checksum Test but with some exceptions. In order to read the Boot ROM, the Diagnostic ROM must be disabled. Therefore, the code to perform this test must be moved from the Diagnostic ROM to system memory prior to disabling the Diagnostic ROM.

2. The test code is moved from the Diagnostic ROM into RAM at address locations 1010--1055. After it is moved the data is verified to make sure it was written correctly. If not a move data error code is displayed on the LEDs.

3. The test then jumps to the code in RAM.

4. The Diagnostic ROM is disabled and the Boot ROM is selected.

5. The 16-bit checksum is performed over address locations 07FD--0000 of the Boot ROM. The calculated checksum is compared to the stored checksum at locations 07FE and 07FF. If an error is detected, an error code is displayed on the LEDs.

6. The Boot ROM is then disabled, the Diagnostic ROM selected, and the test jumps back to the Diagnostic ROM.

POWER-UP TEST NO. 6

Test

Parity Error Interrupt Test

Function

This test verifies that the parity error interrupt circuitry is functioning correctly.

Circuit Boards Involved

System Controller and System RAM. (See Fig. 3-11.)

Error Codes Encountered

Error Codes	Fault
0 0 1 0 0 / 0 0 0 0 1	No parity interrupt
0 0 1 0 0 / 1 1 0 0 0	Wrong interrupt

Description

1. The System RAM board parity error interrupt logic is checked by enabling the parity, inverting the parity check, and reading a memory location. When the parity is inverted, a parity error is generated on a subsequent read operation and the address it occurred at will be latched. This address is not checked for correctness in this test.

2. If no interrupt occurs or if the wrong interrupt occurs, an error code is displayed on the LEDs.

3. The parity interrupt is cleared by reading I/O port addresses D2 and D3. This is done as part of the interrupt handler routine.

POWER-UP TEST NO. 7

Test

Bank Switch and Page Switch Test

Function

This test verifies that bank switching can be uniquely selected for available system and program memory to 64K. It also verifies that page switching can be accomplished within system memory only (16K--64K).

Circuit Boards Involved

System Controller, System RAM, and Program Memory. (See Fig. 3-11.)

Error Codes Encountered

Error Codes	Fault
0 0 1 0 1 / 0 0 0 0 0	Bank error
0 0 1 0 1 / 0 0 0 0 1	Page error

Description

1. The bank switching is checked first. This test writes data into the first location of each 16K block of program and system memory as follows:

Bank	Data Written	Memory Location
00	11	Program 0K--16K
01	22	Program 16K--32K
02	33	Program 32K--48K
03	44	Program 48K--64K
04	--	Not tested
05	66	System 16K--32K
06	77	System 32K--48K
07	88	System 48K--64K

2. Each bank is then selected and the first location is read and checked. If the data read is "00", it is assumed the 16K block is not present and the data is not checked. Only half of the data byte is required to be correct to pass this test. (Example: For bank 03 the data is checked for xxxx 0100 or 0100 xxxx in binary. "x" equals don't cares.)

3. If neither half byte is correct for the location checked, an error code is displayed on the LEDs.

4. The page switching is checked next. The test writes data into the first location of each 8K block of system memory as follows:

Page	I/O Port Address D2 Data Byte	Data Written	Memory Location
02	40	11	System 16K--24K
03	60	22	System 24K--32K
04	80	33	System 32K--40K
05	A0	44	System 40K--48K
06	C0	55	System 48K--56K
07	E0	66	System 56K--64K

5. Each page is then selected and the first location in each page is read and checked. The data is checked for a correct half byte as in Step 2. If neither half byte is correct for the location checked, an error code is displayed on the LEDs.

POWER-UP TEST NO. 8

Test

System Memory (0K--16K)

Function

This test verifies the data integrity of the memory locations 0K--16K in the System RAM board.

Circuit Boards Involved

System Controller and System RAM. (See Fig. 3-11.)

Error Codes Encountered

Error Codes	Fault
0 0 1 1 0 / 0 0 0 0 0	Non-Parity error
0 0 1 1 0 / 1 1 0 0 1	Parity error
0 0 1 1 0 / 0 0 1 0 0	Move data error

Description

1. Since the Diagnostic ROM resides in the first 4K of system memory (0000--0FFF), this test is divided into two parts. The memory locations from 1010--3FFF are checked first. The code from the ROM is then moved into RAM, starting at location 1010. The lower locations from 0000--0FFF are then checked.

2. The parity is enabled during this part of the test. Starting at memory location 1010 and test writes the lower address byte into each location up to 4000.

3. Each location from 1010--4000 is then read and checked against the low byte of the address.

4. Steps 2 and 3 are repeated using the complement of the lower address byte.

5. The test code is moved from the Diagnostic ROM into RAM starting as location 1010. The code is checked for correctness after it is moved. The parity is disabled for the remainder of the test.

6. The test jumps to location 1010 and the Diagnostic ROM is disabled. The test described in Steps 2, 3 and 4 are performed in memory locations 0000-0FFF.

7. The Diagnostic ROM is enabled and the test jumps back to the ROM.

8. If an error is detected during the test, an error code is displayed on the LEDs.

POWER-UP TEST NO. 9

Test

DMA Test (System-to-System)

Function

This test verifies that a 4K block of memory can be moved from one part of system memory to another part of system memory.

Circuit Boards Involved

System Controller and System RAM. (See Fig. 3-11.)

Error Codes Encountered

Error Codes	Fault
0 0 1 1 1 / 1 1 0 0 1	Parity error
0 0 1 1 1 / 0 0 0 1 0	Hung up during DMA
0 0 1 1 1 / 0 0 0 1 1	Data error

Description

1. This test programs the DMA to transfer a 4K block of system memory from a starting address of 2000 (2000--2FFF) to a starting address of 3000 (3000--3FFF) in system memory.

2. The parity is enabled and a consecutive count pattern (00, 01, 02, 03, . . . FF) is loaded into the 4K block of system memory (2000--2FFF).

3. The transfer is started and the 4K block of system memory (2000--2FFF) is transferred to 3000--3FFF in system memory.

4. The transferred data is checked for correctness.

5. If an error is detected, an error code is displayed on the LEDs.

POWER-UP TEST NO. 10

Test

System/Program Memory Test

Function

This test verifies the data integrity of the remaining system and program memory locations to 64K. This test is similar to Power-Up Test No. 8, except the complement data test is not performed. Since system memory OK--16K was checked during Power-Up Test No. 8, it is not checked during this test.

NOTE

The circuitry tested in this power-up test is not needed to boot the system. If an error is encountered during this test, it is recommended to switch out the power-up tests (set Mode switch position 5=1) and run the disc-based diagnostics. Refer to Section 4, Disc-Based Diagnostics, of this manual.

Circuit Boards Involved

System Controller, System RAM and Program Memory. (See Fig. 3-11.)

Error Codes Encountered

Error Codes	Fault
0 1 0 0 1 / x x x x x	Program 0K--16K
0 1 0 1 0 / x x x x x	Program 16K--32K
0 1 0 1 1 / x x x x x	Program 32K--48K
0 1 1 0 0 / x x x x x	Program 48K--64K
0 1 1 0 1 / x x x x x	System 16K--32K
0 1 1 1 0 / x x x x x	System 32K--48K
0 1 1 1 1 / x x x x x	System 48K--64K
x x x x x / 0 0 0 0 0	Data error
x x x x x / 1 1 0 0 1	Parity error

NOTE

A separate error code is assigned to each 16K block. There can be a data or parity error displayed for each of the seven error codes.

Description

1. Parity is enabled during this entire test. Bank 00, 0K--16K in program memory, is addressed first. The test writes the lower address byte into each location in the 16K block. The memory is then read to verify the data at each location.

2. The next bank 01, 16K--32K in program memory, is addressed next. The test is the same as in Step 1.

3. This procedure is followed on the remaining 16K blocks of program and system memory. The order of testing is from the bottom-to-top of program memory and from 16K-to-top of system memory.

4. If an error is detected, an error code is displayed on the LEDs.

POWER-UP TEST NO. 11

Test

DMA Test (System-to-Program)

Function

This test verifies that a 16K block of memory can be moved from one part of system memory to another part of program memory.

NOTE

The circuitry tested in this power-up test is not needed to boot the system. If an error is encountered during this test, it is recommended to switch out the power-up tests (set Mode switch position 5=1) and run the disc-based diagnostics. Refer to Section 4, Disc-Based Diagnostics, of this manual.

Circuit Boards Involved

System Controller, System RAM and Program Memory. (See Fig. 3-11.)

Error Codes Encountered.

Error Codes	Fault
1 0 0 0 0 / 1 1 0 0 1	Parity error
1 0 0 0 0 / 0 0 0 1 0	Hung up during DMA
1 0 0 0 0 / 0 0 0 1 1	Data error

Description

1. Program Memory is cleared from 0000--3FFF.
2. This test programs the DMA to transfer a 16K block of system memory from a starting address of 4000 (4000--7FFF) to a starting address of 0000 (0000--3FFF) in program memory.

3. The parity is enabled and a consecutive count pattern (00, 01, 02, 03, . . . FF) is loaded into the 16K block of system memory (4000--7FFF).

4. The transfer is started and the 16K block of system memory (4000--7FFF) is transferred to 0000--3FFF in program memory.

5. The transferred data in program memory is checked of correctness.

6. If an error is detected, an error code is displayed on the LEDs.

ERROR CODES FOR VERSION V2.X POWER-UP DIAGNOSTICS

The following paragraphs list the suspected chips and/or symptoms for each error code. These lists are not comprehensive but point service personnel to the general area of concern. Usually only MSI, LSI, and buffer chips are listed. The miscellaneous SSI support logic chips are not listed.

Before attempting to troubleshoot any problem, it is advisable to remove all boards that are not necessary to run the power-up tests. Those boards required are the System Controller, System RAM, Emulator Controller, and one Program Memory Board.

NOTE

The SYNC Port (TP 2 - System Controller Bd.) is pulsed prior to each test.

Error Codes---Power-Up Test No. 1

1 1 1 1 1 / 1 1 1 1 1	System Completely Hung

Description

The system is completely hung if all LEDs remain on after turning the power on. One of the first instructions in the Diagnostic ROM is to turn off the LEDs. If this doesn't happen the 2650 probably will not operate. Listed are some of the probable things to look for.

Probable Cause

System Controller Board

1. Reseat all boards in Main Interconnect board. Install only necessary boards.

2. Verify that all voltages are proper and in tolerance.

3. Look at key signals on the System Controller board
   TP7 - S CLK - System Clock
   TP6 - OPREQ should be moving
   TP5 - R/W should be low
   TP3 - M/IO should be high
   TP8 - MSTR RUN should be low
   Pin 16 on U2050 (2650) RESET should be high

At least one of the preceding signals will probably be bad. For help in bringing up the kernel, you can float the 2650 data bus by setting J1051 to pins 1 and 2. This will cause the address lines of the 2650 to increment through the address range.

Error Codes---Power-Up Test No. 2

0 0 0 0 1 / 0 0 0 0 0	2650 CPU Instruction Set Test

Description

This error code indicates that some instructions have executed and when trying to execute all of the 2650 instructions something failed. The test will try to loop on running the 2650 CPU test but it will probably hang or get lost. This is an important step because it verifies that most of the kernel is working.

Probable Cause

System Controller Board

U2050 - 2650 CPU

0 0 0 0 1 / 0 0 1 0 0	2650 CPU Memory Access Instruction Failure

Description

This error code indicates that when trying to execute a STRA,R0 1000 (store R0 in memory at location 1000) and a LODA,R0 1000 (load R0 from memory at location 1000) an error occurred. A probable cause is the inability to access the System RAM board or a data bus error on the System RAM board. Note this is the first access to the System RAM board.

Error Code---Power-Up Test No. 3

0 0 0 1 0 / 0 0 0 0 0	Diagnostic ROM Checksum Failure

Description

This error code indicates that the 2650 can execute all of its instructions. It can also properly address and execute from memory address locations 0000--03FF. The problem is either a bad location(S) in the Diagnostic ROM or the 2650 can not address the whole ROM correctly (0000--0FFF). The data lines are probably good.

Probable Cause

System Controller Board

U5030 - Diagnostic ROM
U6050 - Address Buffer A8--A15
U4050 - Address Buffer A8--A15

Error Codes---Power-Up Test No. 4

0 0 0 1 1 / 0 0 0 0 0	Memory Refresh Interrupt Failure (No Interrupt)

Description

This is the first test of the interrupt circuitry. Until now the 2650's interrupt has been disabled. If no interrupt occurs then the 2650 may be faulty or it may not be getting the interrupt input. One check is to see if the System RAM board is generating the Refresh signal (TP 9--System RAM Board---control line REFN). The signal leaves the board on pin number P1-77. Refer to Section 7, Technical Reference Material, of this manual. If the interrupt signal is present, the problem is in the System Controller board. If not, the problem is probably in the System RAM board.

Probable Cause

System Controller Board

U5100 - Interrupt Priority Decode
U6100 - Interrupt latch
U5200 - Interrupt request to 2650 (INT REQ)
U2050 - 2650 CPU (pin 17)

System RAM Board

U2040 - Dynamic RAM Controller 8202A
U5130 - Refresh Request F/F
U5140 - Refresh Request F/F
U5150 - Refresh Request F/F
U3180 - Refresh signal buffer to backplane
U4040 - REFN (TP 9)

0 0 0 1 1 / 1 1 0 0 0	Refresh Interrupt Test - Wrong Interrupt

Description

This error code indicates that an interrupt other than the one expected was received. Two problems could cause this:

1. If an interrupt is asserted, as soon as the 2650 interrupts are enabled, an interrupt occurs.

2. When the refresh interrupt is generated it was decoded incorrectly or the vector address was generated incorrectly.

NOTE

Check the refresh test points to see if an interrupt was generated.

Probable Cause

System Controller Board

U5100 - Interrupt Priority Decoder
U6100 - Interrupt latch
U2100 - Interrupt buffer (vector address)
U6090 - Interrupt latch
U5090 - Interrupt decoder
U5400 - Interrupt Latch
U5500 - Interrupt Latch
U6400 - Interrupt Latch

| 0 0 0 1 1 / 1 1 0 0 1 | Refresh Interrupt Test - Parity Interrupt Occurred

Description

This error code indicates a parity error occurred as soon as the 2650 interrupts were enabled. Since parity is disabled at this time, the likely problem is with the Parity Interrupt line. It is probably stuck in the asserted state on the System RAM board or on the System Controller board.

Probable Cause

Refer to error code 0 0 1 0 0 / 0 0 0 0 1.

Error Code---Power-Up Test No. 5

| 0 0 1 0 0 / 0 0 0 0 0 | Boot ROM Checksum Failure

Description

This error code indicates that the Boot ROM checksum was incorrect.

Probable Cause

System Controller Board

U5040 - Boot ROM
U1040 - Boot ROM Enable I/O port (EA)

0 0 1 0 0 / 0 0 1 0 0	Boot ROM Checksum Test - Move Data Error

Description

Since the Boot and Diag ROM occupy the same memory address space, code must be moved from the Diag ROM into RAM above the address 1000 (1010--1055). The program jumps to the code in RAM, deselects the Diag ROM, selects the Boot ROM, and performs a checksum over the Boot ROM. This error indicates that after moving the data, it was incorrect.

Probable Cause

The best way to track this error down is to swap the System RAM board with a Program Memory board and run the Disc-Based Diagnostic Memory Test. See the 8301 Memory Diagnostic Test in Section 4, Disc-Based Diagnostics, of this manual.

Error Code---Power-Up Test No. 6

0 0 1 0 0 / 0 0 0 0 1	Parity Interrupt Test - No Interrupt

Description

This test is similar to the Refresh Interrupt test. It is helpful to determine if the 64K System RAM Board is generating the parity signal. Check TP-10 (PRTY) on the memory board and U3180 pin 6 (P1-63). This is the signal before it leaves the board. From previous tests, we know that the interrupt circuitry partially works because the refresh interrupt was detected correctly.

Probable Cause

System RAM Board

U5140 - Parity Latch
U3180 - Parity Signal Buffer (PRTY)
U3020 - Parity latch clock
U3150 - Parity latch enable
U4050 - I/O port latch (bit 1)

System Controller Board

U6090 - Interrupt Latch
U5090 - Interrupt decode

0 0 1 0 0 / 1 1 0 0 0	Parity Interrupt Test - Wrong Interrupt Received

Description

An interrupt was generated but the wrong one was detected.

Probable Cause

System Controller Board

U2100 - Interrupt buffer (Vector Address)
U5100 - Interrupt Latch
U6100 - Interrupt Latch
U6090 - Interrupt Latch
U5090 - Interrupt Latch

Error Code---Power-Up Test No. 7

0 0 1 0 1 / 0 0 0 0 0	Bank Switch Logic

Description

This error code indicates we cannot select each memory banks individually.

Probable Cause

System Controller Board

U2040 - Bank Switch I/O Port Buffer
U3040 - Bank Switch Mux

System RAM Board

U2040 - Dynamic RAM Controller 8202A
U5030 - Address Buffer (A13 - A15)
U2030 - Latch (SEL)

Program Memory Board

U6170 - "CS" chip select
U6110 - Support logic
U6120 - Support logic

0 0 1 0 1 / 0 0 0 0 1	Page Select Error

Description

This error code indicates we cannot individually select each page.

Probable Cause

System RAM Board

U4010 - Page Latch
U4020 - Page Mux
U5030 - Address Buffers A8--A15
U2040 - Dynamic RAM Controller 8202A
U4040 - Page I/O port logic
U4030 - Page I/O port logic
U3170 - Page I/O port logic
U3160 - Page I/O port logic

Error Codes---Power-Up Test No. 8

0 0 1 1 0 / 0 0 0 0 0	System Memory Test - 0000--3FFF

Description

The first 16K of system memory is tested during this test. The test is in two parts. The first part tests memory locations from 1010--3FFF and the second part moves code from ROM to System RAM and checks memory locations 0000--0FFF. Parity is disabled while testing 0000--0FFF. The easiest way to isolate this failure is to swap System and Program Memory boards and run the Disc-Based Diagnostic Memory Test. See the 8301 Memory Diagnostic Test in Section 4, Disc-Based Diagnostics, of this manual.

Probable Cause

System RAM Board

U1060 to U1140 - RAM Chips (0000--3FFF)
U2040 - Dynamic RAM Controller 8202A
U5050 - Input data buffer
U5100 - Data latch
U5060 - Output data buffer
U5030 - Address Buffer (A8--A15)
U5020 - Address Buffer (A0--A7)

0 0 1 1 0 / 1 1 0 0 1	System Memory Test (0000--3FFF) parity error

Probable Cause

System RAM Board

Same as Error Code 0 0 1 1 0 / 0 0 0 0 0
U5040 - Parity Generator
U5090 - Parity Checker
U1040 - Parity Support Logic
U4050 - I/O port D2 (bit 2)

0 0 1 1 0 / 0 0 1 0 0	System Memory Test (0000--0FFF) move data error

Probable Cause

See Error 0 0 1 0 0 / 0 0 1 0 0

Error Code---Power-Up Test No. 9

0 0 1 1 1 / 0 0 0 1 0	DMA (System-to-System) Test Hung

Description

The test hung up while trying to perform a DMA.

Probable Cause

System Controller Board

U2080 - DMA chip
U3090 - latch
U2300 - latch
U2400 - Mux

0 0 1 1 1 / 0 0 0 1 1	DMA (System-to-System) data error

Description

This indicates the DMA was performed but the data was not moved correctly.

Probable Cause

System Controller Board

U2080 - DMA Chip
U2030 - buffer
U2300 - latch
U2400 - Mux
U2070 - data latch
U1090 - bus driver

0 0 1 1 1 / 1 1 0 0 1	DMA (System-to-System) Parity Error

Description

This error code indicates a parity interrupt was generated either while setting up for the DMA or more likely when the data was being checked for correctness.

Probable Cause

See Parity Error Code 0 0 1 1 0 / 1 1 0 0 1

Error Codes---Power-Up Test No. 10

0 1 0 0 1 / x x x x x	Program Memory OK--16K
0 1 0 1 0 / x x x x x	Program Memory 16K--32K
0 1 0 1 1 / x x x x x	Program Memory 32K--48K
0 1 1 0 0 / x x x x x	Program Memory 48K--64K
0 1 1 0 1 / x x x x x	System Memory 16K--32K
0 1 1 1 0 / x x x x x	System Memory 32K--48K
0 1 1 1 1 / x x x x x	System Memory 48K--64K
x x x x x / 0 0 0 0 0	System/Program Memory - Data Error
x x x x x / 1 1 0 0 1	System/Program Memory - Parity Error

Description

These error codes indicate a failure in either the system or program memory boards. The test code (first five digits) indicates which 16K block of memory is failing. The error code (last five digits) indicates if it is a data or parity error. This power-up test is not required to boot the Disc-Based Diagnostics.

Probable Cause

The best way to find this error is to swap the System RAM board and Program Memory board. Then the Disc-Based Diagnostic Memory Test can be run. See the 8301 Memory Diagnostic Test in Section 4, Disc-Based Diagnostics, of this manual.

Error Codes---Power-Up Test No. 11

1 0 0 0 0 / 0 0 0 1 0	DMA (System-to-Program) - System Hung
1 0 0 0 0 / 0 0 0 1 1	DMA (System-to-Program) - Data Error
1 0 0 0 0 / 1 1 0 0 1	DMA (System-to-Program) - Parity Error

Description

These error codes indicate an error in the transfer of a 16K address block from system memory to program memory. This test is not required to boot the Disc-Based Diagnostics. In the event of a failure it is recommended that you run the Disc-Based Diagnostics as defined in the preceding Power-Up Test.

Probable Cause

System Controller Board

U2400 - CMEM Mux
U2300 - latch

See Error Codes - 0 0 1 1 1 / 0 0 0 1 0
- 0 0 1 1 1 / 0 0 0 1 1
- 0 0 1 1 1 / 1 1 0 0 1

PART 3 --- VERSION V1.X AND VERSION V2.X

Most of the functions of the Critical Function Monitor (CFM) are applicable to both version V1.x and V2.x. Where there is a difference both versions are given.

CRITICAL FUNCTION MONITOR

The Critical Function Monitor (CFM) provides a limited troubleshooting capability in the event one of the power-up tests fails and the 8301 cannot boot the operating system off the disc of the DMU. The CFM contains several test routines and a limited set of user commands that may be entered from the System Terminal.

The CFM can be accessed by either of two methods: (Refer to Fig. 3-12 or 3-13.)

1. Normal access to the CFM is via the Mode Switch. If Mode Switch position 6 is set to "1" (OFF or Open), the CFM mode is entered. This method utilizes the full capabilities of the CFM.

2. The other method is during the power-up tests. If an error is detected during execution of any power-up tests, the CFM mode is entered. This method is limited and only the user command set can be used.

Since the second method of entry into the CFM is preconfigured or fixed so that only the user command set can be entered from the System Terminal, the first or normal method of entry to the CFM will be discussed in the following paragraphs.

CFM Mode

The CFM mode is selected when mode switch position 6 is set to "1" (OFF or Open). This is the right branch of the mode switch decision tree shown in Fig. 3-12 or 3-13. Mode switches 1---5 provide selectable options for reconfiguring the CFM. Mode switch position 5 configures the CFM for either Normal Mode or Test Mode.

Normal Mode

In Normal Mode, a limited set of user commands may be entered from the system port with or without an echo port. (The user commands will be defined later in this section.) The system port is determined by mode switch positions 4 and 3. The echo port is determined by mode switch positions 2 and 1.

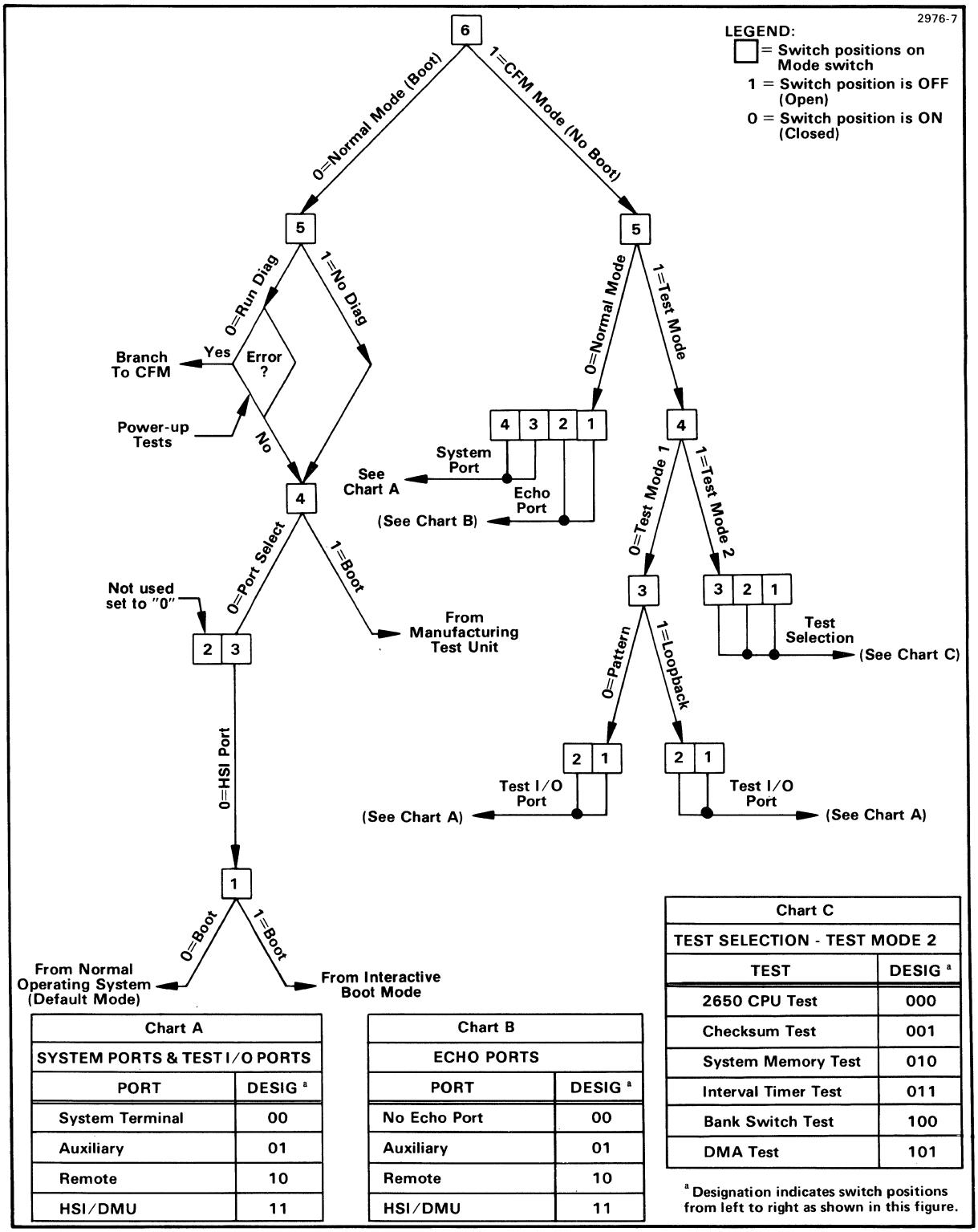


Chart A	
SYSTEM PORTS & TEST I/O PORTS	
PORT	DESIG [a]
System Terminal	00
Auxiliary	01
Remote	10
HSI/DMU	11

Chart B	
ECHO PORTS	
PORT	DESIG [a]
No Echo Port	00
Auxiliary	01
Remote	10
HSI/DMU	11

Chart C	
TEST SELECTION - TEST MODE 2	
TEST	DESIG [a]
2650 CPU Test	000
Checksum Test	001
System Memory Test	010
Interval Timer Test	011
Bank Switch Test	100
DMA Test	101

[a] Designation indicates switch positions from left to right as shown in this figure.

Fig. 3-12. Mode switch decision tree. (Version V1.x)

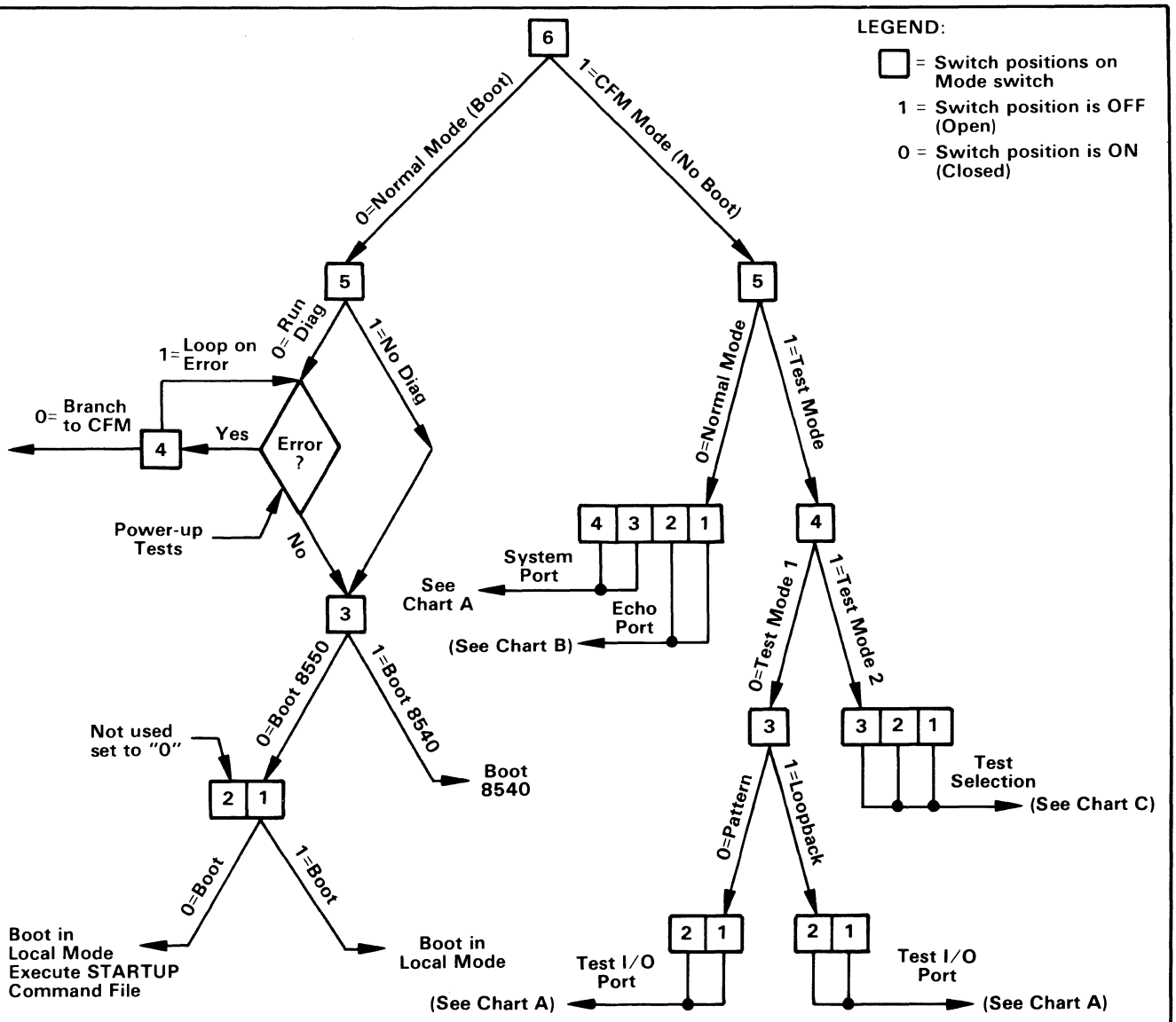


Chart A	
SYSTEM PORTS & TEST I/O PORTS	
PORT	DESIG [a]
System Terminal	00
Auxiliary	01
Remote	10
HSI/DMU	11

Chart B	
ECHO PORTS	
PORT	DESIG [a]
No Echo Port	00
Auxiliary	01
Remote	10
HSI/DMU	11

Chart C	
TEST SELECTION - TEST MODE 2	
TEST	DESIG [a]
2650 CPU	000
Refresh Interrupt	001
Parity Error Intr	010
Bank + Page Select	011
Sys Memory 0000—3FFF	100
DMA (System—System)	101

[a] Designation indicates switch positions from left to right as shown in this figure.

2976-171

Fig. 3-13. Mode switch decision tree. (Version V2.x)

Test Mode

One of two test mode options is selected by mode switch position 4: Test Mode 1 or Test Mode 2. Test Mode 1 consists of two data communications tests, pattern and loopback. These two tests provide verification of I/O ports and any devices that may be attached to the 8301. Both tests may be performed on any one of four I/O peripheral ports (system, auxiliary, remote communications, or HSI). The Pattern Test sends an ASCII string to the terminal (selected by mode switch positions 2 and 1). The test is generated continuously until one of the mode switch positions 6, 5, 4, or 3 is changed. Depending on how the Pattern Test is entered, you may need to toggle the RESTART switch to start the ASCII string. The Loopback Test accepts a character entered from a terminal (selected by mode switch positions 2 and 1) and loops it back to the same port.

Test mode 2 permits you to execute one of six power-up tests on an individual basis. The six tests are listed in Chart C of Fig. 3-12 or 3-13. The test is selected by the settings of mode switches 3, 2, and 1.

CFM USER COMMANDS

The CFM permits you to enter a limited set of user commands from the system port. Recall that the method of entry into the CFM determines whether the system port is fixed or selectable. The CFM must be in Normal Mode of operation before the user commands can be entered.

Command Conventions

The CFM command line is preceded by the CFM prompt character, a pound sign ("#"). Each command line consists of a command name or a command name and one or more parameters, followed by a carriage return. The command name and parameters are separated by spaces.

Each command name consists of two alphabetic characters. The parameters are two or four character hexadecimal addresses. An optional looping parameter "L" is available with some of the commands. (The commands are described individually later in this section.)

When the looping (L) parameter is included in the command line, the CFM command is repeatedly executed until you press any key on the keyboard. The looping parameter generates a sync pulse for each loop by addressing the Sync I/O port. This pulse may be used to trigger an oscilloscope or logic analyzer.

NOTE

When the looping parameter is included, the sync pulse is generated by addressing the sync I/O port immediately before the test starts. The sync test point is located near the top center of the System Controller board. Refer to Section 2, Installation for the location of this test point and Section 8, System Controller for additional information on the Sync I/O port.

The command name and parameters are defined for each command in a "SYNTAX" box. Command names must be entered as shown. Parameters enclosed in braces "{}" must be included in the command line. Parameters enclosed in brackets "[]" are optional. Braces and brackets are used for syntactical representation only and should not be entered as part of the command line.

CFM Error Codes

When a command name or parameter is incorrectly entered, an error code is displayed on the next line of the System Terminal. The error code is contained in register R0 of the system processor's register dump. The register dump is displayed in the following order:

R0 R1 R2 R3 R4 R5 R6 PSU PSL

The four error codes are as follows:

Error Code	Meaning
R0=40	Unrecognized command
R0=41	Illegal hexadecimal character
R0=42	Illegal delimiter
R0=43	Illegal I/O port

DESCRIPTION OF CFM COMMANDS

Table 3-8 is a list of the CFM user commands. They are described individually on the following pages.

Table 3-8
CFM User Commands

Command	Command Title	Function
DI	Dump I/O port	Allows you to examine I/O ports.
DR	Dump registers	Allows you to examine the system processor's registers.
EX	Examine or Deposit	Permits you to examine or modify system/program memory addresses.
GO	Branch to address	Permits execution of user-entered test routines.
WR	Write I/O port	Permits writing to I/O ports.

DI - Dump I/O Port

Syntax

DI {port address} [L]

PARAMETERS

port address	Enter only two digit hexadecimal address for I/O port being examined.
L	Causes the DI command to be repeatedly executed until you press any key on the keyboard.

REQUIREMENTS

This command permits you to examine the status or data registers for specific I/O port addresses. The System Terminal displays the data byte for the specified address. Table 3-9 contains a list of legal I/O port address assignments. If an illegal I/O port address is entered, the error code R0=43 is displayed on the System Terminal.

EXAMPLES

```
#DI CA
CA=0C
#
```

Displays the data byte "0C" associated with I/O port address CA. Returns the CFM prompt character.

```
#DI CE L
CE=02
CE=02
CE=02
CE=02
CE=02 <----- Key pressed on keyboard
#
```

Displays the data byte "02" associated with I/O port address CE. The "L" parameter causes this command to loop (execute repeatedly) until you press a key on the keyboard. Returns the CFM prompt character.

Table 3-9
I/O Ports Used With DI and WR Commands

Port	Read/Write	Function
CA	R/W	Remote Communications Port - ACIA control and status
CB	R/W	Remote Communications Port - ACIA data
CC	R/W	Auxiliary Port - ACIA control and status
CD	R/W	Auxiliary Port - ACIA data
CE	R/W	System Terminal Port - ACIA control and status
CF	R/W	System Terminal Port - ACIA data
E8	R/W	HSI Communications Port data
E9	R/W	HSI Communications Port control and status
EA	R/W	Flexible Disc control and status
EB	R/W	Flexible Disc data
EC	W	Interval Timer Control Port
EC	R	2650A-1 Reset (system processor)
ED	W	LED Write Port
ED	R	Switch Read Port
EE	W	Bank Switch Port (WR command only)
EF	R	Sync Test Point Port (DI command only)

DR - Dump Registers

Syntax
DR

PARAMETERS

none

REQUIREMENTS

This command displays the contents of nine registers in the system processor. You can call the Dump Registers routine from a user-entered test routine to display the register contents for a specified point (in either system or program memory) during execution of the test routine.

EXAMPLE

```
#DR
R0=0D 0F 00 00 02 00 A7 65 40
#
```

Displays the hexadecimal value in each register at time of the dump. The registers are displayed in successive order as follows:

R0 R1 R2 R3 R4 R5 R6 PSU PSL

EX - Examine or Alter Memory Contents

Syntax

EX {address} [L]

PARAMETERS

address	Enter four digit hexadecimal address of program or system memory location you wish to display or alter. Leading zeros must be included.
L	When added to command line the CFM command is repeatedly executed until you press any key on the keyboard.

NOTE

The EX command normally examines system memory which is limited to 32K or an upper address of 7FFF. Program memory can also be examined by first using the bank switching feature and writing to I/O port EE with the associated data byte of the desired 16K block of program memory. (Refer to Sections 5 and 8 in this manual for additional information on Bank Switching.) Figure 3-14 shows the relationship of the 16K blocks and associated data bytes (I/O port address EE) to the address locations in program memory. The bank switching feature switches the individual 16K blocks of program memory into the system processor's upper 16K address space (16K---32K). Therefore, if it is desired to examine address 8000 in program memory the command "WR EE 02" must be entered prior to the command "EX 8000".

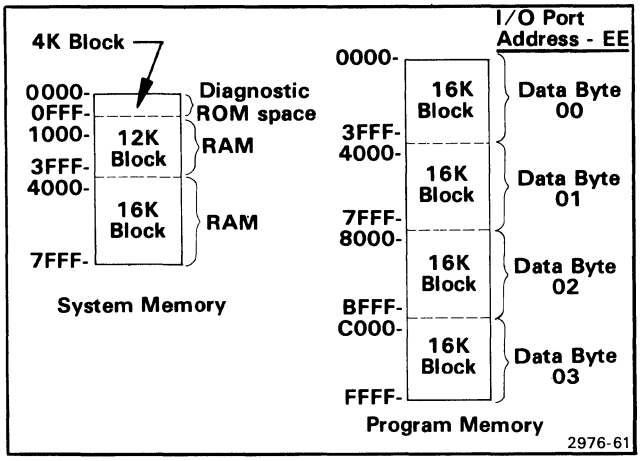


Fig. 3-14. System and program memory allocation

REQUIREMENTS

Examining Memory

This command displays the contents of a specified memory address on the System Terminal. Press RETURN key to terminate command. If the "L" parameter is included, the specified memory address and its contents are repeatedly displayed until you press any key on the keyboard.

Successive Examination of Memory

This command may also be used to display the contents of successive memory locations. When only an address parameter is entered (without the "L" parameter), you can display the contents of successive locations by repeatedly pressing the space bar. Press the RETURN key to terminate the EX command.

Altering Memory

The EX command also allows you to alter data located at the specified address and at subsequent addresses. To alter the displayed data contents, enter a two-digit hexadecimal data value (do not press the space bar). The entered digits will be displayed; the EX command outputs a space to delimit between the data bytes entered. Press the RETURN key to terminate the EX command. The EX command is used to enter user-entered test routines into memory.

You may also use the EX command to enter data continuously into the same or successive addresses. When you enter the "L" parameter, the new data byte is then repeatedly written to the location(s). Press the RETURN key to terminate the EX command.

EXAMPLES

```
#EX 2FFF
2FFF=03
#
```

Displays the data byte "03" at address 2FFF. Pressing the RETURN key terminates the command and returns the CFM prompt character.

```
#EX 2FFF
2FFF=03 0F 00 01 5C 29 89
#
```

Displays the data byte at address 2FFF. When the space bar is depressed six times, data is displayed at the next six successive addresses. Pressing the RETURN key terminates the EX command and returns the CFM prompt character.

```
#EX 2FFF
2FFF=03 FF FF FF FF FF FF FF
#
```

Displays the data byte at address 2FFF. To change the contents of the next seven addresses, enter "FF" seven times without pressing the space bar or RETURN key. Pressing the RETURN key terminates the EX command and returns the CFM prompt character.

```
#EX 2FFF
2FFF=FF 03 L
#
```

Displays the data at address 2FFF. When you enter "03" and "L", and then press the RETURN key, the new data byte "03" will be repeatedly written into the specified address. When you press the RETURN key again, the EX command is terminated and the CFM prompt character is displayed.

GO - Branch To Address

Syntax

GO {address} [L]

PARAMETERS

address	Enter a four digit hexadecimal address. This is the address where execution of the user-entered test routine is to start. Leading zeros must be entered.
L	When added to command line allows looping of the called user routine (providing the looping routine is called for in the user routine). Looping continues until you press any key on the keyboard.

REQUIREMENTS

This command allows you to direct control of the system processor to any location in memory for execution of your user-entered test routines. The GO command is an absolute branch to the specified memory location; therefore, at the end of the user-entered test routine there must be a branch to the start of the CFM or a call to the looping routine. If not, the CFM must be re-entered by toggling the RESTART switch.

EXAMPLES

```
#GO 01FF
#
```

The CFM branches to address 01FF for execution of a user-entered test routine. If the CFM prompt character is not displayed, toggle the RESTART switch.

WR - Write I/O Port

Syntax

WR {port address} {data byte} [L]

PARAMETERS

port address	Enter only two digit hexadecimal address of an I/O port.
data byte	Enter two digit hexadecimal value.
L	When added to command line causes the WR command to be repeatedly executed until you press any key on the keyboard.

REQUIREMENTS

This command permits writing to legal I/O port address listed in Table 3-9. This command is used to modify the contents of control or data registers associated with the specified I/O port address. Nothing is displayed on the System Terminal except the CFM prompt character when the WR command has completed execution. When the "L" parameter is included, data is repeatedly written to the I/O port; the prompt character is not displayed until you press a key on the keyboard. If an illegal I/O port address is entered, the error code R0=43 is displayed on the System Terminal.

EXAMPLES

```
#WR E9 FF
#
```

The data byte "FF" is written to I/O port address E9. The prompt character indicates that the command has finished executing.

```
#WR ED FF L
#
```

The data byte "FF" is written repeatedly to I/O port address ED until you

press a key on the keyboard. The CFM prompt character indicates the completion of execution.

HOW TO USE THE CFM

The CFM provides a limited capability for isolating 8301 system failures. However, to execute any of the CFM commands the system terminal must be operational.

Isolation of Typical Problems

The following paragraphs describe how the CFM may be used to isolate typical failures or problems. This discussion is not intended to be comprehensive, but instead to briefly define how the CFM commands and tests can be used to obtain information regarding various problems.

I/O Problems

I/O problems may be isolated in the following ways:

1. The CFM commands DI or WR may be used to read from or write to the various I/O ports. The looping "L" parameter may be added to the command line and a logic analyzer triggered from the 8301 sync pulse. This feature lets you verify that the 8301 data bus is being changed with the WR command or that it contains the same readout as displayed by the DI command. For specific bit information contained in the associated data byte of each I/O port address, refer to the I/O Port Specifications in Section 7 of this manual.

2. Set the mode selector switches for Test Mode 1. Refer back to Fig. 3-12 or 3-13. An ASCII pattern or loopback test can be performed on the four I/O ports: system terminal, auxiliary, remote communications, and HSI/DMU.

3. A user-entered test routine may be used to test I/O port addresses that cannot be entered with the DI and WR commands. Refer to Table 3-6 for a list of the legal I/O ports for the DI and WR commands.

System Processor Problems

The system processor can be tested for suspected problems by executing the 2650 Instruction Set Test. This test is executed by setting mode switch positions 6, 5, and 4 for Test Mode 2 and switch positions 3, 2, and 1 for 2650 CPU test. (Refer back to Fig. 3-12 or 3-13.)

System Memory Problems

System memory problems may be isolated in the following ways:

1. Set the mode switch to execute the System Memory Test in Test Mode 2. (Refer back to Fig. 3-12 or 3-13 for mode switch settings.)

2. The CFM command EX may be used to read and write to suspected bad memory locations. The EX command many also be used with the looping (L) option in the command line. An oscilloscope or logic analyzer can be triggered by the 8301 sync pulse.

Limitations in the Use of CFM Commands

When using the CFM commands, observe the following limitations:

1. If using the switchable I/O port features in "Normal Mode", when you select the same port for "system" port and "echo" port, each character is displayed twice on the terminal.

2. The CFM command DR is best used from a user-entered test routine. The DR command may be executed whenever the CFM prompt character appears. However, the displayed register contents will always be the same.

3. The CFM tests require the following workspace in system memory:

   CFM work area

   Version V1.x---142D through 14C7
   Version V2.x---1000 through 10A8

   If this work space is disturbed by user-entered routines or other causes, the results are unpredictable.

User-Entered Test Routines

User-entered test routines can be used to isolate other problems or failures. This technique requires considerable knowledge of the 2650A-1 instruction set and programming capabilities.

User-entered test routines are entered in system memory with the CFM command EX. The EX command may also be used to examine memory locations to verify that the entered test routine is correct. The CFM commands GO and DR, with the looping option (L) may be used in conjunction with the user-entered test routine. The starting addresses for these routines are as follows:

- Looping routine

  Version V1.x---0B7C
  Version V2.x---0D99

- DR command routine

  Version V1.x---096B
  Version V2.x---0BA5

- Mode select module (start of CFM)

  Version V1.x---0C55
  Version V2.x---0DDE

The looping routine, in conjunction with a user-entered test routine, will continually loop the test routine until you press any key on the keyboard. The DR command routine will dump the system processor's registers. This routine can be called at any time in your test routine. The mode select module returns your test routine to the start of the CFM. This routine should be called last in your user-entered test routine. If the looping routine is used, you do not need to use the mode select module.

User-Entered Test Routine Examples

Table 3-9 lists the legal I/O port addresses that can be written to or read from with the CFM commands WR and DI, respectively. A user-entered routine can be used to write to or read from any port address in the 8301. Here are three examples of test routines that address I/O ports for both V1.x and V2.x.

Version V1.x

Example 1. Write To I/O Port FC---Display Data Byte

```
0457     LODI,RO   057H   ;load data byte 57 in RO
D4FC     WRTE,RO   0FCH   ;write data byte to I/O
                          ;address FC
3F096B   BSTA,UN          ;branch to display registers
                          ;routine
1F0C55   BCTA,UN          ;return to start of CFM
```

Example 2. Read and Display Data Byte From I/O Port C7

```
54C7     REDE,RO   0C7H   ;read data byte at I/O
                          ;address C7
3F096B   BSTA,UN          ;branch to display registers
                          ;routine
1F0C55   BCTA,UN          ;return to start of CFM
```

Example 3. Repeatedly Write To I/O Port C2---Display Data Byte

```
04B8     LODI,R0   0B8H   ;load data byte B8 in R0
D4C2     WRTE,R0   0CEH   ;write data byte to I/O
                          ;address C2
3F096B   BSTA,UN          ;branch to display registers
                          ;routine
1F0B7C   BCTA,UN          ;branch to looping routine
```

Version V2.x

Example 1. Write To I/O Port FC---Display Data Byte

```
0457     LODI,R0   057H   ;load data byte 57 in R0
D4FC     WRTE,R0   0FCH   ;write data byte to I/O
                          ;address FC
3F0BA5   BSTA,UN          ;branch to display registers
                          ;routine
1F0DDE   BCTA,UN          ;return to start of CFM
```

Example 2. Read and Display Data Byte From I/O Port C7

```
54C7     REDE,R0   0C7H   ;read data byte at I/O
                          ;address C7
3F0BA5   BSTA,UN          ;branch to display registers
                          ;routine
1F0DDE   BCTA,UN          ;return to start of CFM
```

Example 3. Repeatedly Write To I/O Port C2---Display Data Byte

```
04B8     LODI,R0   0B8H   ;load data byte B8 in R0
D4C2     WRTE,R0   0CEH   ;write data byte to I/O
                          ;address C2
3F0BA5   BSTA,UN          ;branch to display registers
                          ;routine
1F0D99   BCTA,UN          ;branch to looping routine
```

The test routines used in these examples may be used for other I/O port addresses by substituting data bytes and/or I/O port addresses. Example 3 contains the looping routine. The data byte B8 will be continually written to I/O port address C2 until you press any key on the keyboard.

NOTE

Most of I/O port addresses contain separate write and read registers. Therefore, you cannot read the port to verify that the correct data was written to the port. However, the DMA registers have a read/write capability (I/O ports addresses 90 through 97). But, you must write and read the specified DMA port twice, because the low and high bytes of the 16-bit registers are loaded or read consecutively. Refer to Section 5, Functional Procedure No. 6 for additional information on programming the DMA device.

Entering Test Routines

The test routine is entered into system memory with the EX command. The CFM must be in the normal mode of operation. To enter Example 1 (Write to I/O Port FC), use the following commands. (Be sure the test routine is entered above the workspace in RAM. See Fig. 3-1.)

```
#EX 2000
2000=95 04 57 D4 FC 3F 09 6B 1F 0C 55
#
```

When RETURN key is pressed, address 2000 contains the data byte 95. (The data byte may vary with each examination.) The ten data bytes contained in Example 1 is then entered from the terminal. Pressing the RETURN key terminates the EX command and returns the CFM prompt character. The test routine can now be executed with the GO command, as follows:

```
#GO 2000
R0=57 30 30 00 03 02 A7 62 40
#
```

The GO command executes the test routine at address 2000, when the RETURN key is pressed. When the routine is executed, the system processor's registers are dumped immediately after the data byte is written to the I/O port. Register R0 contains the value of the data byte (57) written to I/O port FC. The values displayed in the other registers may vary. If the looping routine (1F0B7C) is substituted for the last instruction (1F0C55), the test routine is then executed as follows:

```
#GO 2000 L
```

When the RETURN key is pressed, the register dump will be repeatedly displayed until you press any key on the keyboard.

Section 4

DISC-BASED DIAGNOSTICS

INTRODUCTION

This section describes the Disc-Based Diagnostic Test Programs that are contained on a separate 8550 System Diagnostics Disc. These Diagnostic Test Programs provide an easy way of performing 8301 verification and board-level fault isolation. The test programs are executed by user-entered responses to menu displays on the system terminal. Before the disc-based diagnostic tests can be executed, the 8550 MDL DOS/50 Operating System Disc must be removed from the 8501 DMU and the 8550 System Diagnostics Disc inserted.

The disc-based diagnostic tests are entirely separate from the power-up tests discussed in Section 3 of this manual. However, these tests are dependent on the power-up tests.

This section presents an overall view of the diagnostic system, explains the menu displays, contains a detailed explanation of each diagnostic test program and near the end of the section provides a consolidated numerical listing of all error codes for the basic 8301 unit. An index of the error codes is provided in this manual's Table of Contents. The error codes are included in the paragraph headings that describe the various tests contained in this section.

DIAGNOSTIC SYSTEM OVERVIEW

Figure 4-1 shows an overview of the 8301 disc-based diagnostic tests and their dependency on the 8301/8501 power-up tests. Before the 8301 diagnostic test programs can be loaded, the 8301/8501 power-up tests must be passed. If any power-up test fails, the power-up diagnostics branch to an alternate mode, as follows:

8301 — Branches to the Critical Function Monitor (CFM) and displays an error code. User-entered commands may be entered from the system terminal, as described in Section 3 of this manual.

8501 — Branches to the Debug Mode and displays an error code. For information on user-entered commands, refer to the 8501 Data Management Unit Service Manual.

NOTE

The execution of the 8501 power-up diagnostics is transparent to the user when the system terminal is connected to the 8301. The user only receives an indication that the 8501 power-up diagnostics have (or have not) executed properly. However, if the 8501 diagnostics have not executed properly, it is unlikely that the 8301 Diagnostic Executive program will be able to boot.

The following sequence of events briefly describe the Diagnostic System as shown in Fig. 4-1:

1. Messages (8301 BOOT and 8501 BOOT) are displayed on the system terminal when the 8301/8501 power-up diagnostics have completed execution. The 8301 Diagnostic Executive (EXEC) program is then loaded. The EXEC program is the heart of the 8301 disc-based diagnostics and resides in system memory when loaded.

2. Once the EXEC is loaded, all interaction between the diagnostic programs and the user is through menus displayed on the system terminal. All of the menus have a default mode that can be entered by pressing the RETURN key. The various menus will be defined in detail later in this section.

   The first menu displayed on the system terminal is the "RUN MODE MENU". This display notifies the user that the EXEC program is loaded and lists a choice of modes that determine how the diagnostic tests will be executed. This menu lists the following modes:

   - AUTOMATIC MODE
   - SELECT MODE

   The default mode for this menu is "AUTOMATIC MODE". This means that all the diagnostic test programs are run automatically and in sequence, without user intervention. This mode is used for a fast system verification and is referred to as the AUTOMATIC SYSTEM VERIFICATION Mode. These modes will be discussed in greater detail later in this section.

3. When the Automatic System Verification (default) mode is selected, the EXEC program executes all the diagnostic test programs in proper sequence. If an error is detected during the running of any test program, an error message is immediately displayed on the system terminal and the next test program in sequence is executed. This continues until all test programs are executed.

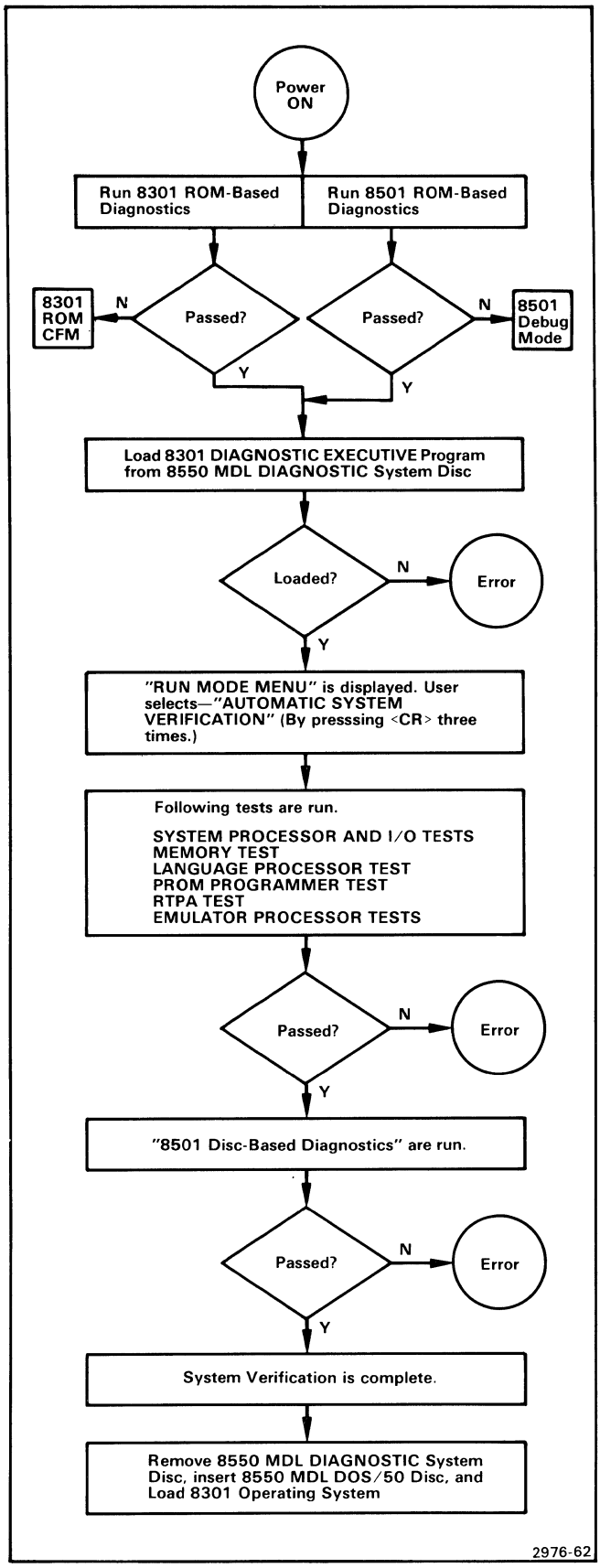


Fig. 4-1. Overview of Diagnostic System.

4. When the 8301 Disc-based Diagnostics are finished, the EXEC program branches to the 8501 Disc-based Diagnostics for execution of all 8501 diagnostic test programs.

5. The system verification is complete when both 8301 and 8501 disc-based diagnostics have completed execution and no errors are detected.

6. The 8301 MDU Diagnostic System Disc must be removed and the 8550 MDL DOS/50 Disc reinserted before the DOS/50 operating system can be loaded for normal operation.

HOW TO USE THE DISC-BASED DIAGNOSTICS

PURPOSE OF THE DIAGNOSTIC SYSTEM

The goal of the 8550 Disc-Based Diagnostic System is to provide an easy-to-use tool that will:

- verify that the 8550 system is operating correctly.
- detect failures in the 8550 system.
- display diagnostic error codes and supporting data when a failure is detected.
- designate a Primary and Secondary (in some instances) suspected failing circuit board(s).

The diagnostics are designed with a friendly user interface consisting of menu formats. Most menus have prompting statements and HELP messages that permit a user to run the diagnostic tests. It is not necessary for the user to have a technical knowledge of the circuitry within the 8550 system to obtain an overall system verification with the diagnostic tests. Those desiring more information about a particular failure, can look up the error codes in Table 4-1 where the page number for the detailed explanation of each test is provided. A consolidated listing of all error codes for the basic 8301 unit is also provided at the end of this section.

HOW TO RUN THE DIAGNOSTIC TESTS

To run the 8550 Disc-Based Diagnostic Tests, the following procedures should be followed:

1. Remove all discs from the 8501 DMU.

2. Apply power to both units (8301 and 8501). (Remember the 8501 has a primary POWER switch on the rear panel and a DC power switch on the front panel.)

3. Insert the 8550 Diagnostic Disc in the 8501.

4. Toggle the RESTART switch on both units.

5. When the power-up tests on both units are completed, the "8501 BOOT and 8301 BOOT" messages are displayed on the system terminal. In about 10 seconds the Run Mode Menu is displayed.

6. System verification is obtained by pressing the RETURN key for the first three menus (after each menu is displayed). This selects the default items from these menus. The items selected from the three menus are as follows:

    - Automatic Mode --- Run Mode Menu
    - Automatic System Verification --- Automatic Mode Menu
    - Display Messages on Terminal --- Display Option

After the RETURN key is pressed three times, no more user reaction is required, the 8301 and 8501 system verification tests run automatically. As the tests are running, messages are displayed providing the status and progress of the tests. System verification requires about five minutes to complete. When finished, if no failures are detected, a message is displayed:

SYSTEM VERIFICATION PASSED

If a failure is detected during the running of the tests, a DIAGNOSTIC FAILURE message is displayed and the test continues. Since a failure was detected, when the tests are completed, a message is displayed:

SYSTEM VERIFICATION FAILED

WHAT TO DO IN CASE OF ERROR

When a failure is detected during the running of any test in the Automatic Mode the following occurs:

- An error code and supporting data is displayed.
- The test program is terminated.
- The next test program is loaded and executed.

It is possible that several error codes may be displayed before the SYSTEM VERIFICATION FAILED message is displayed. It is advisable to correct the first failure and disregard the subsequent error code displays. The test programs are designed and sequenced such that each test assumes the preceding tests were passed. Therefore, subsequent error messages may or may not be valid. After the first failure is corrected, run the diagnostic tests again to determine if the secondary failures still occur.

It is recommended that the Select Mode be used to run specific tests on the first detected failure. If the failure is still detected, the supporting data displayed with the error code will specify a circuit board as the "Primary Suspect". On certain failures a "Secondary Suspect" is also displayed. Replacing the circuit board and rerunning the "Automatic System Verification" tests should clear the "Diagnostic Failure" display (unless a multiple failure exists).

READING THE DIAGNOSTIC FAILURE MESSAGE

When a failure is detected during the running of any diagnostic test, a "Diagnostic Failure" message is displayed on the system terminal. The message consists of an error code number and supporting data. An example of a Diagnostic Failure message is as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          Error Code = 02/0004

ACTUAL DATA   = 0000 0001
CORRECT DATA = 0000 0011
ADDRESS       = 00 4000
BANK TESTED   = 01
------------------------------
PRIMARY SUSPECT = MEMORY BOARD
------------------------------
```

A consolidated listing of all Diagnostic Failure messages (for the basic 8301) is included later in this section. This listing is in numerical order by error code. This list provides a complete breakdown of each error message and provides (where possible) a suspected device or group of devices that could cause the failure detected by the diagnostic test.

Error Code

The error code is divided into two parts: xx/yyyy. The "xx" indicates the test program number. The "yyyy" indicates a specific failure within the test program. In the example, the error code (02/0004) is read as follows:

02 = Memory and Memory Functions Test

0004 = Chip Select Error

Supporting Data

The amount of supporting data varies with each error message. It will always consist of a primary suspected circuit board and in some failures a secondary suspect also. The other data displayed is dependent on the detected failure. From this information it is sometimes possible to narrow the failure down to a single or several device(s). In the preceding failure message example, by comparing the actual data to the correct data, it can be determined that bit 1 is in error. The bank under test is "01", which is the 16K--32K bank (00 4000--00 7FFF) of Program Memory. Address 00 4000 is the failing address, which is an even address.

This information is then entered into the tables associated with the error code that is contained in the consolidated listings found at the end of this section. From these tables we determine that the suspected devices are either U2020 (RAM) or U6050 (read/write buffer) of the 0K--32K Program Memory board.

NOTE

Note that the address in the preceding failure message example contains six digits. The Memory diagnostics are capable of testing system memory up to 64K and program memory up to 256K anywhere within the 16M-byte address space. Therefore, the failing hexadecimal address is displayed within the following address ranges:

System Memory---Bank Nos. 04, 05, 06, and 07

0K--64K 00 0000--00 FFFF

Program Memory---Bank Nos. 00, 01, 02, and 03

0K--256K 00 0000--FF FFFF

Whenever four digit hexadecimal addresses are used within this manual, the address is assumed to be between 0K and 64K.

GENERAL TROUBLESHOOTING COMMENTS

When the above procedures are followed and it is determined that a certain circuit board is suspected of being faulty, perform the following steps before replacing the circuit board.

1. Remove the suspected board. (Refer to Section 2, Installation in this manual for the procedures on removal of circuit boards.)

    a. Verify that all jumpers are installed correctly. (Refer to Section 2, Installation in this manual for correct jumper positions.)

b. Make sure all socketed devices are seated properly in their sockets.

c. Clean the board edge connectors.

2. Re-insert the board and run the diagnostic tests again.

NOTE

If possible, install the board in another slot in the 8301 Main Interconnect board. (Remember do not install System boards in the Program section and vice versa. The Emulator Controller board must remain in one position: J5.)

If the above checks have not corrected the failure, replace the board and run the Automatic System Verification tests on the replaced board.

Two types of failures are difficult to diagnosis: unstable failures and intermittent failures. An unstable failure is one that fails frequently but fails differently each time. An intermittent failure is one that fails periodically but generally the same error code is displayed.

The most common cause for an unstable failure are voltage problems and contact problems. Check to ensure the voltages are properly set. (Refer to Section 15, Power Supplies in this manual.) Then clean all board contacts and check that all socketed devices are seated properly.

Intermittent failures can be caused by heat sensitive devices, pattern sensitivity problems, or noise problems. Running the tests continuously over an extended period will help to isolate and identify this type of failure. If it is difficult to determine a certain area within the 8301 where the failure occurs, the Automatic Mode --- Run Specified Test (Continually) may be selected to run several or all of the tests continuously without user interaction. If running overnight or unattended it is advisable to output the error messages on a printer (connected to 8301 AUXILIARY port). If a certain area or board is suspected of having an intermittent problem, the Select Mode allows you to select Option 0 --- Run All Tests. This provides the most exhaustive exercise for the suspected board.

ERROR CODE LISTING

A numerical listing by error code number of all error codes for the basic 8301 unit are contained near the end of this section in Tables 4-18 through 4-22. These tables contain the error codes, supporting data, and suspected boards/devices that relate to the detected failure. When an error code is displayed on the system terminal, refer to these tables for a brief description of the failure. If a more detailed explanation is needed, refer to the Error Code Index at the beginning of this section for the page number of the detailed test.

DIAGNOSTIC EXECUTIVE

The Diagnostic Executive (EXEC) program is the heart of the Diagnostic System. The EXEC program can be thought of as a simplified operating system. When loaded in 8301 system memory, the EXEC program occupies address locations 0000--1FFF (8K). The diagnostic test programs occupy locations 2100--3FFF (<8K) and if needed, the larger test programs may also occupy locations 4000--7FFF (16K). When a test program contains only 2650A-1 code, the test program is contained wholly within the 8301 system memory. When a test program contains code associated with an emulator as well as 2650A-1 code, the program is loaded into system memory and the test program calls a DMA move routine (from the EXEC) to move the emulator code to the 8301 program memory. Figure 4-2 shows the allocation of the various diagnostic programs in system memory. The EXEC Link Area (located at 2000--20FF) is used as a communications area for passing data between the test program and the EXEC. The Diagnostic EXEC program contains the frequently used utility routines. In addition, the EXEC program handles the following functions:

- user I/O
- test program loading
- error handling
- looping control
- test program sequence
- menu displays

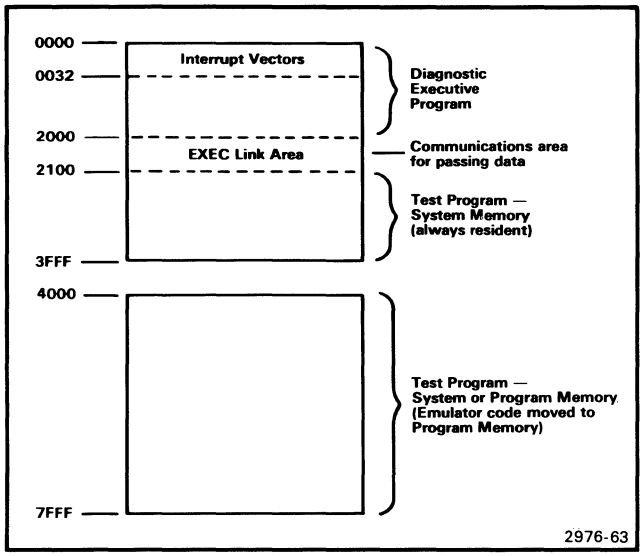


Fig. 4-2. Memory allocation of diagnostic programs.

OVERVIEW OF EXECUTIVE MENU DISPLAYS

When the EXEC program is loaded into system memory, all interaction between the Diagnostic System and the user is through the various menus displayed on the system terminal. Figure 4-3 is an overview of the menu displays executed by the EXEC program.

MENU DISPLAYS

As each menu is displayed, one or more statements are included that require some response from the user. To select the default item on any menu, simply press the RETURN or <CR> key. If any other item is selected the RETURN key must also be pressed. On most menus, a HELP item may be selected, if you desire more information on the tests available. Refer to Fig. 4-3 as a guide, as you study the following discussion on menus.

RUN MODE MENU

The Run Mode Menu is the first menu to be displayed when the disc-based diagnostics are invoked. Display 4-1 shows the menu format as displayed on the system terminal.

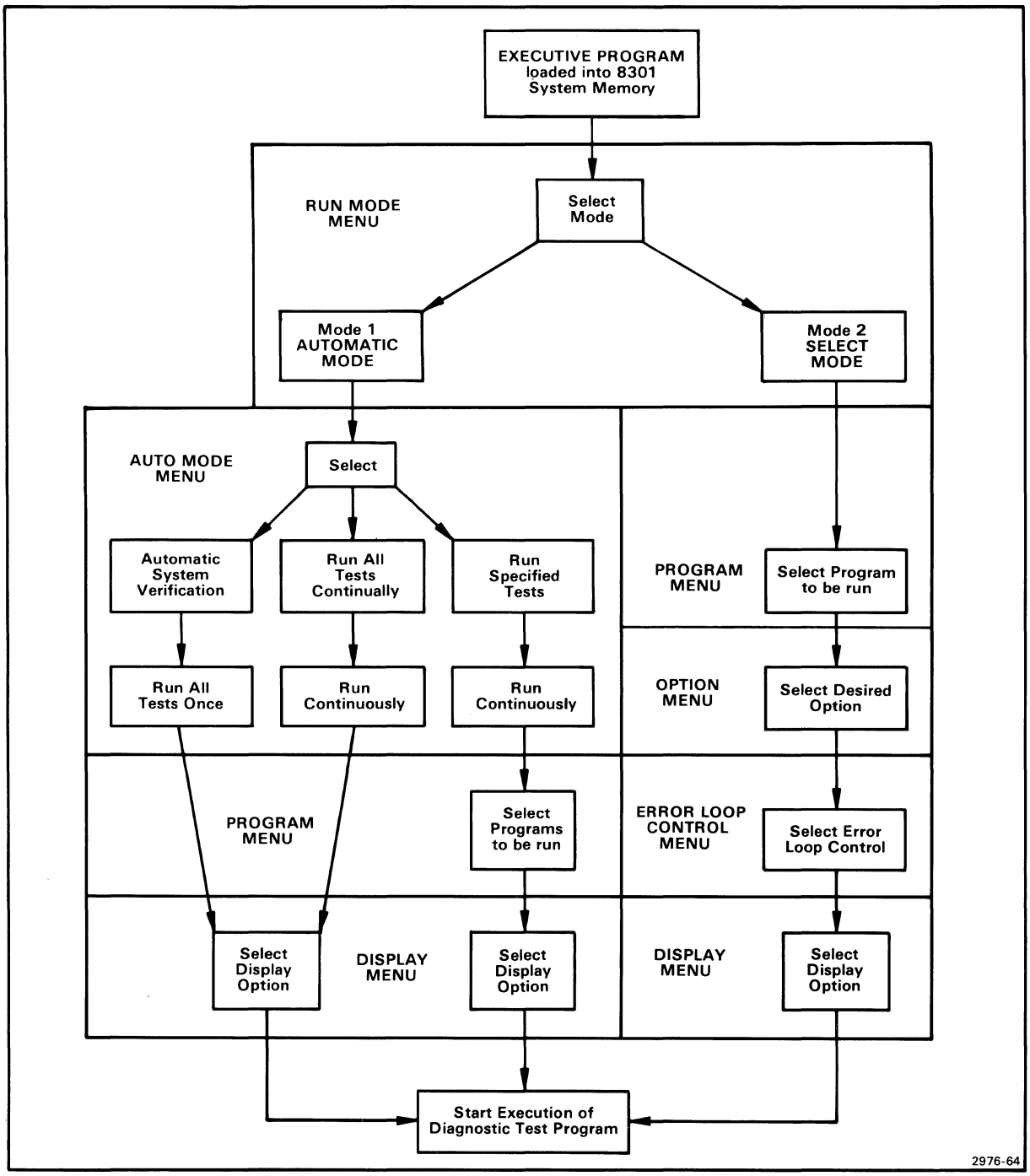
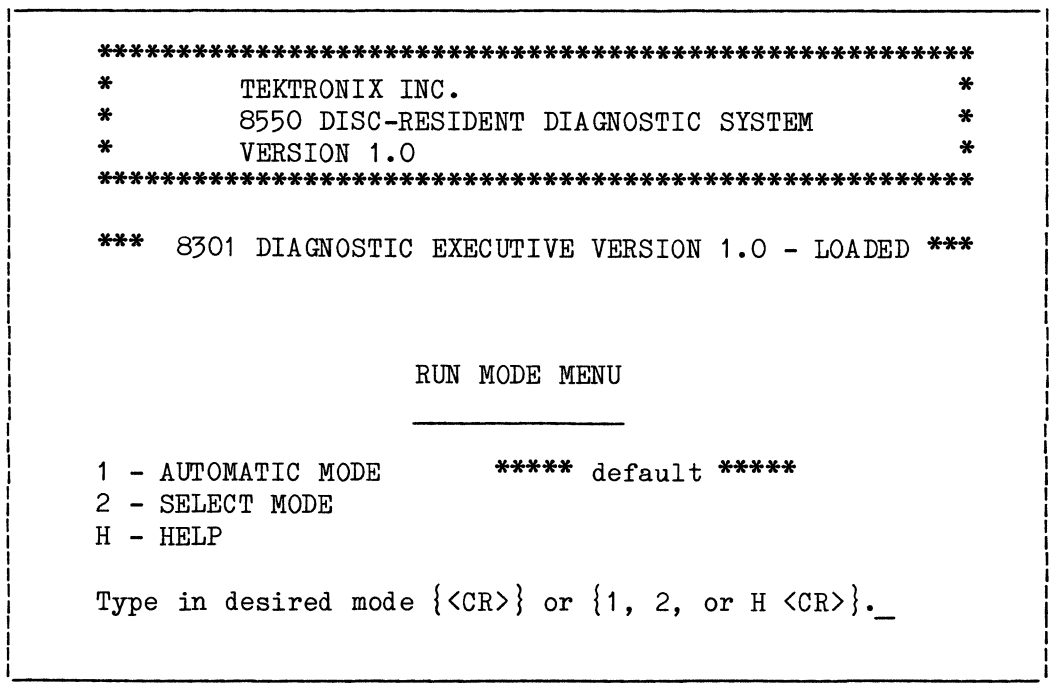


Fig. 4-3. Overview of Executive Menu Displays.



Display 4-1. Run Mode Menu Format.

Automatic Mode

This mode is selected by entering either <CR> or 1<CR>. When this mode is selected, the terminal displays the Automatic Mode Menu. The Automatic Mode is used to verify that the 8550 system is operational. This mode requires minimum user interaction.

Select Mode

This mode is selected by entering 2<CR> which replaces this menu with the Program Menu. The Select Mode is used when you want to individually run the various diagnostic test programs. Select Mode provides extensive error resolution capability. This mode is generally used after a failure is detected in Automatic Mode, or if an intermittent problem is suspected in a certain function or circuit board.

AUTOMATIC MODE MENU

The upper portion of Display 4-2 shows the Automatic Mode Menu. This menu allows you to continue in the Automatic mode. You can either execute each of the tests once or execute all of the tests continually. It also lets you select specific tests to be run. If you select either item 1 or 2 from the Automatic Mode Menu, the Display Option Menu is displayed. Display 4-2 shows these two menus.

Automatic System Verification

This is the default item which provides a one-time execution of each Automatic Mode test. The Automatic Mode tests are referred to as the AUTOMATIC SYSTEM VERIFICATION Tests.

```
                    AUTOMATIC MODE MENU
                    -------------------

1 - AUTOMATIC SYSTEM VERIFICATION          ***** default *****
2 - RUN ALL TESTS CONTINUALLY
3 - RUN SPECIFIED TESTS
H - HELP

Type in desired mode {<CR>} or {1--3 or H <CR>}._


                    DISPLAY OPTION
                    --------------

1 - DISPLAY MESSAGES ON TERMINAL           ***** default *****
2 - DISPLAY MESSAGES ON 8301 PRINTER & TERMINAL
3 - NO DISPLAY OR PRINT
H - HELP

Type in display option {<CR>} or {1--3 or H <CR>}._
```

Display 4-2. Automatic Mode and Display Option Menus.

Run All Tests Continually

This item provides continuous execution of all Automatic Mode tests. This selection is useful for detecting intermittent errors: the diagnostic testing may continue for several hours with no interaction between the diagnostic test program and the user.

Run Specified Tests

This item calls the Program Menu which permits individual tests to be selected before the Display Option menu is displayed. The specified tests are run continuously.

DISPLAY OPTION

This menu is shown in the lower portion of Display 4-2. It is displayed after item 1 or 2 from the Automatic Mode Menu is selected, or after the Program Menu display, if item 3 from the Automatic Mode Menu is selected. This menu lets you select where the messages from the diagnostic tests are displayed. The items in this menu are self-explanatory.

NOTE

The printer must be connected to the 8301 AUXILIARY port.

PROGRAM MENU

This menu may be called (when operating in the Automatic Mode) by item 3 (Run Specified Tests) from the Automatic Mode Menu. (See Display 4-2.) It may also be called (when operating in the Select Mode) by item 2 (Select Mode) from the Run Mode Menu. (See Display 4-1.) The specified tests are the same for both selections; however, the statements below the menus are not the same. Displays 4-3 and 4-4 show the two menus. The main differences are as follows:

- Program Menu (Automatic Mode) --- This menu permits you to specify one or more tests that are executed continuously. Refer to Display 4-3. If more than one test is entered, the tests are executed in the same order as they are entered. However, the order of the tests on the menu is the recommended order of execution. There is no user interaction required when these tests are running.

- Program Menu (Select Mode) --- This menu permits you to specify one test at a time to be executed. Refer to Display 4-4. The tests selected from this menu are sometimes more exhaustive than the tests executed in the Automatic Mode. Each test selected from this menu has an option menu (and sometimes a sub-option menu) that is displayed after the test is selected. These option and sub-option menus require some user interaction while the test is executing.

Additional diagnostic test programs will be added to the Program Menu as they are written for 8301 optional equipment. For example, Item 6 in both figures is listed as "Emulator Tests." This item will expand to ten or more individual test programs (one for each emulator). Thus, the Program Menu list as shown in Display 4-3 and Display 4-4 will change as new diagnostic programs are written. However, the 8501 Disc Diagnostics will remain as the last test executed.

```
                    PROGRAM MENU
                    ------------

1 - SYSTEM PROCESSOR AND I/O TEST      *** default ***
2 - MEMORY AND MEMORY FUNCTIONS TEST
3 - LANGUAGE PROCESSOR TEST
4 - RTPA TEST
5 - PROM PROGRAMMER TEST
6 - EMULATOR TESTS
7 - 8501 DISC DIAGNOSTICS
H - HELP

Type in desired programs {i.e. 1, 3, 5 <CR>} or {H <CR>}._
```

Display 4-3. Program Menu (Automatic Mode).

```
                    PROGRAM MENU
                    ------------

1 - SYSTEM PROCESSOR AND I/O TEST      *** default ***
2 - MEMORY AND MEMORY FUNCTIONS TEST
3 - LANGUAGE PROCESSOR TEST
4 - RTPA TEST
5 - PROM PROGRAMMER TEST
6 - EMULATOR TESTS
7 - 8501 DISC DIAGNOSTICS
H - HELP

Type in desired program {<CR>} or {1--7 or H <CR>}._
```

Display 4-4. Program Menu (Select Mode).

OPTION AND SUB-OPTION MENUS

When a test program is selected from the Program Menu (Select Mode), an Option Menu is displayed. Each test program listed in the Program Menu (see Display 4-4) has a unique Option Menu; some also have a Sub-Option Menu. The Option and Sub-Option Menus further control how the test program is conducted. Some selections listed in the Option and Sub-Option Menus require user interaction. Other selections execute the test program with no user interaction. Since the Option and Sub-Option Menus are closely associated

with the detailed description of the test programs, they will be presented as follows: (Refer to Display 4-4.)

- Program Menu Items 1, 2, and 3 --- These test programs are part of the basic 8301 configuration. The Option and Sub-Option Menu formats are included later in this section under the detailed description of the associated diagnostic test programs.

- Remaining Program Menu Items --- These test programs are for optional equipment to the 8301. The Option and Sub-Option Menu formats are contained in their applicable Service Manuals, under the detailed description of the diagnostic test program.

ERROR LOOP CONTROL MENU

Note in Fig. 4-3, that after the Option and Sub-Option Menus are selected, and all statements or questions have been responded to, an Error Loop Control Menu is displayed. This menu allows you to select looping options if an error is detected during the running of a test program. Display 4-5 shows the format of this menu. The items on this menu are defined as follows:

1. LOOP ON ERROR / CONTINUE IF PASS --- If this option is selected, the diagnostics will run until an error is detected. At that time, the test will loop. That is, the particular test that detected the error will be executed over and over again. If the error is not detected during a pass, looping will stop and the diagnostics will continue to the next test. Looping may be halted by pressing the ESC key (return to the Program Menu) or by pressing the BREAK key (return to the Run Mode Menu).

2. LOOP ON ERROR UNTIL RESET --- If this looping option is selected, the diagnostic program loops on any detected error until the ESC or BREAK key is pressed.

3. DO NOT LOOP ON ERROR -- CONTINUE --- If this option is selected, the diagnostics will continue running even if an error is detected. This is the no-loop option.

DISPLAY OPTION

The Display Option menus shown in Display 4-5 and Display 4-2 are the same.

```
                    ERROR LOOP CONTROL MENU
                    -----------------------

1 - LOOP ON ERROR / CONTINUE IF PASS      ***** default *****
2 - LOOP ON ERROR UNTIL RESET
3 - DO NOT LOOP ON ERROR - CONTINUE

Type in looping selection {<CR> or 1 - 3 and <CR>}._


                    DISPLAY OPTION
                    --------------

1 - DISPLAY MESSAGES ON TERMINAL          ***** default *****
2 - DISPLAY MESSAGES ON 8301 PRINTER & TERMINAL
3 - NO DISPLAY OR PRINT
H - HELP

Type in display option {<CR>} or {1 - 3 or H and <CR>}._
```

Display 4-5. Error Loop Control and Display Option Menus.

TEST RUNNING

When the last selection from the Display Option menu is made, the test program with all selected options and sub-options is executed. The option number and an indication that the test is running is displayed on the system terminal as follows:

```
---------------
| OPTION 2    |
---------------
TEST RUNNING -- XX    ITERATION # YYYY      ERRORS = ZZZZ
```

The option number selected from the option menu appears in the box. As the test is executing the cursor continues to trace a line under (and updating) the test running, iteration, and errors parameters. The test running number "XX" is the test module number. The iteration number "YYYY" is the number of times the test has executed. The number of errors encountered during the execution of the test(s) is entered in the errors parameter "ZZZZ." The displayed format showing the option number and the Test Running information may vary from that shown; however, the information is displayed and should be readily detected.

ERROR CODE DISPLAY

If an error is detected during the execution of a test program, an error code and supporting data is displayed on the system terminal. The format for a diagnostic failure is as follows:

```
<<<<<<<<<<<<<<<<   DIAGNOSTIC FAILURE   >>>>>>>>>>>>>>>>

                                        Error Code = xx/yyyy

[Supporting Data]
[Supporting Data]
----------------------------------------
PRIMARY SUSPECT = [name of circuit board]
----------------------------------------
```

The first two digits of the Error Code parameter specify the diagnostic test program that was executing when the failure occurred. This corresponds to the number on the Program Menu (see Display 4-4). The remaining four digits indicate a specific error code within the specified test program. The supporting data normally includes several lines of information regarding the failure. The cause of failure is also listed in the supporting data. This is called out as a primary suspect and in some instances a secondary suspect is also included. From the error code and supporting data you should be able to determine on which board the error occurred, and whether additional diagnostic testing is required. In some instance the failure of a test will also point to the failure of specific devices or a logic function on the circuit board. A consolidated list of error codes associated with all test programs is included at the end of this section.

8301/8501 COMMUNICATION ERRORS

Note in Fig. 4-1, if the 8301 Diagnostic Executive Program cannot load from the 8550 System Diagnostics disc, an error code is displayed on the system terminal. There are eleven error codes that can be displayed. These error codes further define the reason why the Executive Program on the disc cannot be loaded into the 8301 System Memory. Table 4-19 (at the end of this section) lists these error codes and a brief definition of each code. The error codes are displayed in the following format:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        Error Code = 00/0007

HSI Protocol Error <1E>
RUN 8501 STANDALONE DIAGNOSTICS
```

Communications between the 8301 and the 8501 is via the High-Speed Serial

Interface (HSI) port in each unit. The error codes listed in Table 4-19 in most instances refer to some type of communication problem between the two units.

Note in Table 4-19, that the statement "RUN 8501 STANDALONE DIAGNOSTICS" is displayed for each error. When any one of these errors are displayed, the 8501 standalone diagnostics should be run to determine if the failure is in the 8501 or the HSI path between the units. Prior to running the 8501 standalone diagnostics, press the RESTART switch on the 8501 and 8301 again in that order. If the error is still displayed, refer to the 8501 Data Management Unit Service Manual for instructions on running the standalone diagnostics. If the 8501 diagnostics are successfully run, the HSI circuitry in the 8301 is probably faulty. Two of the error codes contain the statement "HSI Protocol Error <xx>". The two digit error code (xx) refers to a list of some 55 protocol errors generated by the 8501. Refer also to the 8501 Data Management Unit Service Manual for a list of these protocol errors. Remember the error codes displayed on the system terminal are in hexadecimal. The error codes listed in the 8501 Service Manual may be in decimal or octal.

DIAGNOSTIC TEST PROGRAMS

The diagnostic testing of the 8301 circuit boards (including the basic configuration and optional boards) is divided into test programs. The diagnostic test programs are designed to run in a specific order. This precludes a test program from using a feature or block of logic in its test procedure that has not already been tested. The test programs and assigned priorities are listed in Table 4-1.

If the test programs are not run in the recommended sequence, any failure detected (error message displayed) may not be valid.

It is important to note that functions are tested by the diagnostic test programs and not individual circuit boards. If a specific board has multiple functions, it may be necessary to run several test programs to verify the board. For example, to verify the System Controller board, both the "System Processor and I/O Tests" and "Memory Tests" must be run.

The following paragraphs describe the operation of the first three priority test programs (listed in Table 4-1) for the basic 8301 configuration. The remaining test programs listed in Table 4-1 are associated with optional circuit boards for the 8301. The test programs for the optional circuit boards are defined in their applicable Service Manuals.

Table 4-1
Diagnostic Test Programs and Priorities

Priority	Program
1	System Processor and I/O Tests
2	Memory and Memory Functions Test
3	Language Processor Test
4	PROM Programmer Test
5	RTPA Test
6	Emulator Tests

The diagnostic test programs (priorities 1, 2, and 3 as shown in Table 4-1) are defined later in this section.

Each test program is described in this section as follows:

- A brief overview of the test program, showing how each program is divided into various test modules.
- A look at the Option and Sub-Option Menus with a brief description of each option.
- A detailed description of each test module, containing:
    1. Functions of the test program.
    2. Detailed descriptions defining the execution of each test module.
    3. Display presentations showing error code and other supporting data if an error is detected.
- At the end of this section, all error codes are listed for the System Processor and I/O Tests, Memory and Memory Functions Test, and Language Processor Test. These error code listings contain a detailed breakdown of each error code display and supporting data.

SYSTEM PROCESSOR AND I/O TEST PROGRAMS

OVERVIEW OF TEST PROGRAMS

The System Processor and I/O Test Programs provide verification of the 2650A-1 microprocessor (system processor), the three RS-232-C compatible ACIA ports, and other miscellaneous circuitry on the System Controller board. This is the first disc-based diagnostic test that is executed.

The System Processor and I/O Test Programs are divided into the following five test programs:

1. INSTRUCTION SET TEST --- This test verifies the 2650A-1 instruction set by executing a set of tests that determine the data integrity of the registers, the data and address buses, and the correct execution of the instruction set.

2. CHECKSUM TESTS (Diagnostic ROM and Boot ROM) --- This test checks each data byte in the Diagnostic ROM and the Boot ROM for correctness, using a 16-bit checksum calculation method.

3. INTERVAL TIMER TEST --- This test is executed in three parts: processor speed test, non-interrupted interval timer test, and interrupted interval timer test.

4. LED AND DIP SWITCH TEST --- This test verifies that the LEDs and the six-position DIP switch function correctly. This test is not run in Automatic Mode, but only when Select Mode Option 4 (LED and DIP Switch Test) is selected.

5. I/O TEST --- This test verifies that all ACIA ports (Remote Communications, System Terminal, and Auxiliary) function correctly. The HSI port is not tested by this test. This test is not run in Automatic Mode, but only when Select Mode Option 5 (I/O Test) is selected.

NOTE

The I/O Test requires two wrap-back connectors (male and female) to run the wrap-back test of Option 5 (I/O Test). These two connectors may be ordered together under Tektronix Part Number 067-1020-00.

The five test programs are executed with six test option selections. The six test options are divided into one or more test modules as shown in Table 4-2 for a total of 12 test modules.

Table 4-2
Relationship of Test Options, Programs, and Modules

Test Option	Test Program	Test Module Numbers
Option 0	Run All Tests	1--9
Option 1	Instruction Set Test	1--7
Option 2	Checksum Tests (Diagnostic ROM and Boot ROM)	8
Option 3	Interval Timer Test	9
Option 4	LED and DIP Switch Test	10--11
Option 5	I/O Tests	12

The test option formats for the System Processor and I/O Test Programs are described in the following paragraphs.

TEST OPTIONS

The Option Menu for the System Processor and I/O Test Program is shown in Display 4-6. This menu is displayed when Item 1 from the Select Mode--Program Menu is selected. (Refer back to Display 4-4.)

```
8301 SYSTEM PROCESSOR AND I/O DIAGNOSTICS    VERSION 0.1
------------------------------------------------------------

                    OPTION MENU
                    -----------
0 - OPTION 0 - RUN ALL TESTS            ***** default *****
1 - OPTION 1 - INSTRUCTION SET TEST
2 - OPTION 2 - CHECKSUM TESTS
3 - OPTION 3 - INTERVAL TIMER TEST
4 - OPTION 4 - LED AND DIP SWITCH TEST
5 - OPTION 5 - I/O TEST
H - HELP

Type in desired option {<CR>} or {0--5 or H <CR>}._
```

Display 4-6. Option Menu for System Processor and I/O Test Program.

Option 0 --- Run All Tests

When Option 0 is selected, Test Modules 1--9 are executed continuously until the ESC or BREAK key is pressed. (Refer to Table 4-2 for the test programs represented by Test Modules 1--9.) Two counters are displayed on the system terminal. One indicates the number of times the Test Modules 1--9 have been executed and the other indicates the number of times an error has been detected (number of failures). No user interaction is required and no checksum results are displayed.

NOTE

The ESC and BREAK keys perform the following functions during the execution of all disc-based diagnostic test programs: The ESC key suspends execution of the test or routine and returns to the Option Menu. The BREAK key terminates the test program and returns to the Run Mode Menu.

Option 1 --- Instruction Set Test

If Option 1 is selected, Test Modules 1--7 are executed continuously until the ESC or BREAK key is pressed. Two counters are displayed after each run indicating the number of times Test Modules 1--7 have been run and the number of failures. No user interaction is required.

Option 2 --- Checksum Test

When Option 2 is selected, Test Module 8 is continuously run. This test requires user interaction to the Sub-Option menu. Display 4-7 shows the Option Menu and the Sub-Option menu when Option 2 is selected.

```
8301 SYSTEM PROCESSOR AND I/O DIAGNOSTICS    VERSION 0.1
------------------------------------------------------------

                    OPTION MENU
                    -----------
0 - OPTION 0 - RUN ALL TESTS              ***** default *****
1 - OPTION 1 - INSTRUCTION SET TEST
2 - OPTION 2 - CHECKSUM TESTS
3 - OPTION 3 - INTERVAL TIMER TEST
4 - OPTION 4 - LED & DIP SWITCH TEST
5 - OPTION 5 - I/O TEST
H - HELP

Type in desired option {<CR>} or {0--5 or H <CR>}. 2



                OPTION 2 - CHECKSUM TEST
                ------------------------
 1 - DIAGNOSTIC ROM AND BOOT ROM CHECKSUMS
 2 - GENERAL CHECKSUM
 H - HELP

 Type in desired sub-option {<CR>} or {1,2, or H <CR>}. _
```

Display 4-7. Option 2 --- Checksum Test Menu.

Sub-Option 1

If Sub-Option 1 is selected, the following is displayed below the Display Option menu shown in Display 4-5.

```
--------------
| OPTION 2   |
--------------

DIAGNOSTIC ROM CHECKSUM = XXXX  PART NO = XXX-XXXX-XX
BOOT ROM CHECKSUM       = XXXX  PART NO = XXX-XXXX-XX

TEST RUNNING -- XX      ITERATION # XXXX        ERRORS = XXXX
```

The checksums and part numbers are displayed on the first run of the test module. The module continues to execute with the two counters displaying the number of times run and the number of times failed.

Sub-Option 2

If Sub-Option 2 is selected, the following statements are displayed below the Display Option menu shown in Display 4-5.

NOTE

This option is primarily used for developmental purposes.

```
---------------
| OPTION 2    |
---------------

Type in starting address.  {XXXX <CR>}
Type in ending address.    {XXXX <CR>}

CHECKSUM RESULT = XXXX
TEST RUNNING -- XX      ITERATION # XXXX        ERRORS = XXXX
```

NOTE

The ending address must be greater than the starting address. Both addresses must be in the same bank (16K block).

After you type in the starting and ending addresses, the checksum routine will run and the checksum result will be displayed. The routine will continue to run with the statements and results displayed on only the first execution of the test module. Two counters display the number of times run and number of times failed. When Sub-Option 2 is selected, there cannot be a failure or error code displayed.

Option 3 --- Interval Timer Test

When Option 3 is selected, Test Module 9 is continuously run. The system processor's speed is displayed on the first run, with the two counters displaying the number of times run and the number of times failed. The processor speed is displayed below the Display Option menu, as follows:

```
---------------
| OPTION 3    |
---------------

*** SYSTEM PROCESSOR SPEED=2 MHz  (or 1.25 MHz)

TEST RUNNING -- XX      ITERATION # XXXX        ERRORS = XXXX
```

Option 4 --- LED and DIP Switch Test

When Option 4 is selected, Test Modules 10 and 11 are continuously run. The two counters display the number of times run and the number of times failed. When this option is selected, statements are displayed below the Display Option menu that require user interaction. After the action is completed on each statement, the RETURN key is pressed and the next statement appears.

NOTE

Before you run this test, the 8301 top cover must be removed. This test is therefore conducted only on an "as called" basis when operating the diagnostics in Select Mode. Refer to Section 2 in this manual for instructions on removal of the 8301 top cover. LEDs and DIP switches are both read from the left to the right (from the component side of the board). The leftmost LED or switch is the most significant.

The following statements are consecutively displayed below the Display Option menu when Option 4 is selected.

NOTE

Before making the last selection on the Display Option menu, make certain you can see the LEDs. They will light sequentially from right to left as viewed from the component side of the board.

```
OPTION 4 - SYSTEM CONTROLLER BOARD LED AND DIP SWITCH
-----------------------------------------------------

Verify that the LEDs are lit sequentially.
When done (2 seconds) press  {Y or N <CR>} or {CR} _
```

NOTE

Make sure you wait at least 2 seconds before responding. This allows the test to complete the lighting of the LEDs. The Front Panel SELF TEST LED is the last to light. If you respond Y<CR> or <CR>, the next statement is displayed. If your response is N<CR>, an error code 01/0016 and supporting data are displayed.

```
Set the DIP switch to 101010 (1=on 0=off) and press <CR> when done _

Set the DIP switch to 010101 (1=on 0=off) and press <CR> when done _

Restore the DIP switch to 000000 (1=on 0=off) and press <CR> when done _

TEST RUNNING -- XX     ITERATION # XXXX       ERRORS = XXXX
```

The test program reads the DIP switch settings before you change the switch

settings. The last statement tells you to restore the DIP switch to its original settings (as read by the test program).

Option 5 --- I/O Tests

These tests check the three ACIA ports for proper operation. A polling routine continually polls each ACIA port in a sequence. If an output device or wrap-back connector is not connected to a port, the polling routine skips over that port and polls the next port in sequence. The tests are continuously run until the ESC key is pressed; at that time, the I/O Test Sub-Option Menu is displayed again. Pressing the ESC key twice terminates the I/O Tests and displays the Option Menu again. Display 4-8 shows the sub-option menu displayed below the Option Menu. When a selection is made from the sub-option menu, the Error Loop Control Menu and the Display Option menu are not shown. The test is conducted immediately after the sub-option selection is made.

```
8301 SYSTEM PROCESSOR AND I/O DIAGNOSTICS    VERSION 0.1
------------------------------------------------------------

                    OPTION MENU
                    -----------
0 - OPTION 0 - RUN ALL TESTS              ***** default *****
1 - OPTION 1 - INSTRUCTION SET TEST
2 - OPTION 2 - CHECKSUM TESTS
3 - OPTION 3 - INTERVAL TIMER TEST
4 - OPTION 4 - LED & DIP SWITCH TEST
5 - OPTION 5 - I/O TEST
H - HELP

Type in desired option {<CR>} or {0--5 or H <CR>}. 5


                OPTION 5 - I/O TEST
                -------------------
 1 - DEVICE EXERCISER TEST    ***** default *****
 2 - WRAP-BACK TEST
 3 - INTERACTIVE TEST
 H - HELP

 Type in desired sub-option {<CR>} or {1-3 or H <CR>}. 1
```

Display 4-8. Option 5 --- I/O Test Menu.

The two wrap-back connectors (male and female -- Tektronix Part Number 067-1020-00) are connected to the ACIA ports during the Wrap-Back Test, as shown in Table 4-3.

Table 4-3
Wrap-Back Connectors for the Wrap-Back Test

ACIA Port Designation		Mode Selector Switch	Wrap-Back Connector
Jack No.	Name		
J101	Remote (DTE)	DTE1 or DTE2	Female
J102	Remote (DCE)	DCE	Male
J103	Auxiliary	(not used)	Male
J104	Terminal	(not used)	Male

NOTE

The Mode Selector switch is used only for the Remote Communications Ports: J101 and J102. The CNTL(L) (No Control) position of the switch is not used during these tests.

Sub-Option 1

Sub-Option 1 continuously writes a complete set of ASCII characters (99 characters) to any output device detected by a polling routine. No error code is displayed and no user reaction is required for this sub-option. Also the Option box and Test Running line are not displayed for this sub-option. The string of ASCII characters is continuously displayed until the ESC key is pressed. The display is as follows:

```
ABCDEFGHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrstuvwxyz0123456789
 /.,?><;":\|`~]=-[}+_)(*&^%$#@!{ '
ABCDEFGHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrstuvwxyz0123456789
 /.,?><;":\|`~]=-[}+_)(*&^%$#@!{ '
ABCDEFGHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrstuvwxyz0123456789
 /.,?><;":\|`~]=-[}+_)(*&^%$#@!{ '
ABCDEFGHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrstuvwxyz0123456789
 /.,?><;":\|`~]=-[}+_)(*&^%$#@!{ '
ABCDEFGHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrstuvwxyz0123456789
 /.,?><;":\|`~]=-[}+_)(*&^%$#@!{ '
```

Sub-Option 2

Before Sub-Option 2 is selected, two wrap-back connectors are required: one male and one female. The proper wrap-back connector must be installed on the ACIA port under test. (Refer to Table 4-3.) When Sub-Option 2 is selected, the port identification and baud rate of the ACIA port (where the wrap-back connector is detected) are written to the other two ACIA ports. (System Processor must be operating at 2 MHz for the baud rate test.) The display is as follows:

```
ACIA PORT = REMOTE COMMUNICATION [designates placement of
BAUD RATE = 9600                      wrap-back connector]
BAUD RATE = 4800
BAUD RATE = 2400
BAUD RATE = 1200
BAUD RATE =  600
BAUD RATE =  300
BAUD RATE =  150
BAUD RATE =  110
```

In the preceding display the baud rate switch was moved from top to bottom. The data written to and read from the ACIA port (with the wrap-back connector connected) is not visible on any output device. If an error is detected, an error code and supporting data is also written to the other two ports.

NOTE

To test the system terminal port baud rate, follow this procedure:

1. Select Option 5 (I/O Test).
2. Move the system terminal to another port.
3. Install wrap-back connector on System port.
4. Enter "2" and "CR" to select Baud Rate test.

It may be necessary to type in two "2's" before the "CR" in order to select the test. This is due to an unwanted character that is generated when switching the terminal to another port. When finished, press ESC key, reconnect the system terminal to the System port, and press the ESC key again.

Sub-Option 3

If Sub-Option 3 is selected, the polling routine polls the ACIA ports for connected output devices. For the first device found, the ACIA port name is displayed and the user is asked to type in any character(s). The entered character(s) are echoed back immediately on the selected port. The ESC key is pressed to terminate this test. The display is as follows:

```
ACIA PORT = SYSTEM TERMINAL
Type in any character(s) and press <ESC> when done.
[characters typed are echoed back immediately and displayed here]
```

NOTE

During the running of I/O Tests (Option 5), the test may be terminated and the I/O Test menu displayed again by pressing the ESC key once. If the ESC key is pressed twice, the I/O Tests are terminated and the Program Menu is displayed. Pressing the BREAK key (after the ESC key is pressed once), terminates the test program and displays the Run Mode Menu. The BREAK key is not detected until the ESC key is pressed once.

The following paragraphs describe in detail each test program for the System Processor and I/O Test.

NOTE

The CT8500 terminal will only work on the System Terminal port. The 4024 and 4025 terminals will work on any of the three ports.

INSTRUCTION SET TEST (01/0001--0010)

CIRCUIT BOARD TESTED

System Controller.

FUNCTION

The Instruction Set Test consists of seven test modules that are used to verify that the 2650A-1 responds correctly to each instruction in its instruction set. Each test module checks a group of 2650A-1 instructions.

DESCRIPTION

1. The seven test modules (1--7) used to verify the 2650A-1 instruction set are executed sequentially. All addressing modes possible for a given instruction are tested. Table 4-4 lists the seven test modules with the instruction group and instructions tested.

Table 4-4
Instructions Tested for Each Test Module

Test Module	Instruction Group	Instructions Tested
1	Load/Store Group	LOD, STR
2	Arithmetic Group	ADD, SUB, DAR
3	Logical Group	AND. IOR, EOR
4	Rotate Group	RRL, RRR
5	Compare Group	COM
6	Branch and Subroutine	BCT, BCF, BRN, BIR, BDR, BXA, BST, BSF, BSN, BSXA, RET
7	Program Status Word and Miscellaneous Instruction Group	LPS, SPS, CPS, PPS, TPS, TMI, NOP

2. As the instructions for each test module are executed, they are compared to ensure each instruction is properly executed. Sixteen error codes are used to stipulate which group or instruction within the test program has failed. If an error is detected, an error code and supporting data are displayed on the system terminal. These tests branch to a looping routine if a failure is detected. The looping routine repeats the test module that contains the error. A SYNC pulse is generated each time the test module is repeated. Table 4-5 lists the error code, the failed instruction or group, and the test module that is repeated by the looping routine. The additional information displayed with the error code is as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                  Error Code = [see Table 4-5]

-----------------------------------------
PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
-----------------------------------------
```

NOTE

In the above display, the System Controller board is listed as the suspected cause of failure. These disc-based diagnostics are considered to be board-level repair. However, any failure noted in the Instruction Set Test can normally be traced to the 2650A-1 microprocessor.

Table 4-5
Instruction Set Test Error Codes

Error Code	Failed Instruction or Group	Loops on Test Module
01/0001	LOD Instruction	1
01/0002	STR Instruction	1
01/0003	ADD Instruction	2
01/0004	SUB Instruction	2
01/0005	DAR Instruction	2
01/0006	AND Instruction	3
01/0007	IOR Instruction	3
01/0008	EOR Instruction	3
01/0009	RRL Instruction	4
01/000A	RRR Instruction	4
01/000B	COM Instruction	5
01/000C	Branch Instructions	6
01/000D	Branch to Subroutine Instruction	6
01/000E	Return from Subroutine (RETC) Instruction	6
01/000F	Stack Pointer (SP0, SP1, SP2 IN PSW)	6
01/0010	Program Status Word and Miscellaneous Instructions	7

CHECKSUM TESTS (DIAG ROM/BOOT ROM) (01/0011--0012)

CIRCUIT BOARD TESTED

System Controller.

FUNCTION

This test verifies the correctness of each data byte in the Diagnostic ROM and the Boot ROM by performing a checksum calculation on both ROMs.

DESCRIPTION

1. This test (Test Module 8) performs a 16-bit checksum calculation on each ROM to obtain a calculated checksum (actual) figure. The actual checksum obtained by the test is compared to the recorded checksum contained in the ROM. The Diagnostic ROM is tested first; then, the Boot ROM is tested. If there is an error in any bit (from either ROM), the actual checksum figure will not match the correct checksum figure and an error code with supporting data are displayed on the system terminal. A separate error code is displayed for each ROM test. These tests branch to a looping routine if a failure is detected. The looping routine repeats the test where the error is detected. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                    Error Code = [see Table 4-6]

ACTUAL CHECKSUM = [calculated checksum]
CORRECT CHECKSUM = [correct value stored in each ROM]
----------------------------------------
PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
----------------------------------------
```

Table 4-6
Checksum Tests Error Codes

Error Code	Error
01/0011	Diagnostic ROM checksum error
01/0012	Boot ROM checksum error

INTERVAL TIMER TEST (01/0013--0015)

CIRCUIT BOARD TESTED

System Controller.

FUNCTION

This test checks the speed of the system processor and the interrupted/non-interrupted features of the interval timer.

DESCRIPTION

1. This test (Test Module 9) is divided into the following three tests:

    1. PROCESSOR SPEED --- This test checks the speed of the system processor.

    2. INTERRUPTED INTERVAL TIMER --- This test checks to ensure that the interval timer does interrupt the 2650A-1 microprocessor when the interval timer interrupt is enabled.

    3. NON-INTERRUPTED INTERVAL TIMER --- This test checks to ensure that the interval timer does not interrupt the 2650A-1 microprocessor when the interrupt timer is disabled.

2. If an error is detected when these tests are executed, an error code and supporting data are displayed on the system terminal. A separate error is displayed for each test. These tests branch to a looping routine if a failure is detected. The looping routine repeats the test where the error is detected. A SYNC pulse is generated each time the test is repeated.

3. The additional information displayed with the error code is as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                  Error Code = [see Table 4-7]

----------------------------------------
PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
----------------------------------------
```

Table 4-7
Interval Timer Test Error Codes

Error Code	Error
01/0013	Processor speed error
01/0014	Interrupted interval timer error
01/0015	Non-interrupted interval timer error

LED AND DIP SWITCH TEST (01/0016--0017)

CIRCUIT BOARD TESTED

System Controller.

FUNCTION

This test verifies the operation of the five LEDs on the System Controller board, one LED (SELF TEST) on the front panel, and the DIP switch located on the System Controller board. Each LED and switch position is tested. This test is only run when Select Mode, Option 4 (LED and DIP Switch Test) is selected.

DESCRIPTION

1. This test program is divided into the following two test modules:

   - Test Module 10 -- LED TEST --- This is a visual test; the user is asked to visually check the sequential lighting of the LEDs from left to right.

   - Test Module 11 -- DIP SWITCH TEST --- For this test the user is asked to manually set the six-position DIP switch to 101010 and then to 010101 (where 1=ON and 0=OFF).

     This test module checks that the values read from the switch settings are correct. At the end of this test the user is asked to restore the DIP switch to normal operating settings.

NOTE

This test requires you to remove the 8301 top cover prior to running the test. It is therefore conducted only on an "as called" basis when operating the diagnostics in the Select Mode. Refer to Section 2 in this manual for instructions on removal of the 8301 top cover.

2. If an error is detected in the LED lighting or the DIP switch settings, an error code and supporting data are displayed on the system terminal. These tests branch to a looping routine if a failure is detected. The looping routine repeats the test module where the error is detected. A SYNC pulse is generated each time the test is repeated.

3. The additional information displayed with the error code from Test Module 10 is as follows:

```
>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                          Error Code = [see Table 4-8]

----------------------------------------
PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
----------------------------------------
```

Table 4-8
LED and DIP Switch Test Error Codes

Error Code	Error
01/0016	LED error
01/0017	DIP switch error

I/O TESTS (01/0018--001D)

CIRCUIT BOARDS TESTED

System Controller and Communications Interface.

FUNCTION

These tests verify that the three RS-232-C compatible ACIA ports (Remote Communications, System Terminal, and Auxiliary) are operating correctly. These tests are only run when SELECT MODE, Option 5 (I/O Tests) is selected. The HSI port is not checked.

A polling routine, which continually polls the ACIA ports in a sequence, permits these tests to run continuously until the ESC key is pressed. The ACIAs are polled in the following order:

- Remote Communications Port
- System Terminal Port
- Auxiliary Port

DESCRIPTION

1. These tests (Test Module 12) are sub-options to Option 5, and are divided into the following three tests:

    1. DEVICE EXERCISER TEST
    2. WRAP-BACK TEST
    3. INTERACTIVE TEST

2. DEVICE EXERCISER TEST --- This test continuously writes a complete set of ASCII characters (99 characters) to any ACIA port where an output device is detected during a sequential polling of the ACIA ports. The output device(s) can be checked visually to see if the ASCII characters are sent/received correctly. No error code is displayed for this test.

3. WRAP-BACK TEST --- This test requires that a wrap-back connector be connected to one of the ACIA port connectors on the rear of the 8301. The polling routine checks all ACIA ports for an installed wrap-back connector. If one is detected, the port identification and baud rate for that port is calculated and transmitted to the other two ACIA ports. The baud rate switch can be changed and the entire range of baud rates checked for that port. After calculating the baud rate, the test transmits the values 55 and AA (0101 0101 and 1010 1010) to the selected port. The test reads the port to ensure the values received back from the port are correct. Of course, these values will not be transmitted to the other two ACIA ports. The operation of the other two ports is checked by moving the wrap-back connector to each port. When the Terminal port is under test, the system terminal can be moved to the Auxiliary port connector.

NOTE

If you are using a CT8500 terminal, it cannot be moved. It will only work when connected to the TERMINAL port.

If an error is detected in the baud rate or when the values 55 and AA are read back, an error code and supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module where the error is detected. A SYNC pulse is generated each time the test is repeated.

The additional information displayed with the error code is as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                   Error Code = [see Table 4-9]

ACTUAL RESPONSE = [value read at ACIA Port]
CORRECT RESPONSE = [0101 0101 or 1010 1010]
-----------------------------------------
  PRIMARY SUSPECT = COMM INTERFACE BOARD
SECONDARY SUSPECT = SYSTEM CONTROLLER BOARD
-----------------------------------------
```

Table 4-9
I/O Tests Error Codes

Error Code	Error
01/0018	ACIA Remote Communications Port error
01/0019	ACIA System Terminal Port error
01/001A	ACIA Auxiliary Port error
01/001B	Remote Communications Port Baud Rate Error
01/001C	System Terminal Port Baud Rate Error
01/001D	Auxiliary Port Baud Rate Error

4. INTERACTIVE TEST --- When this test is called, the user is asked to type in any character(s). The test will echo the character(s) back on the selected ACIA port until the ESC key is pressed. No error code is displayed for this test.

MEMORY AND MEMORY FUNCTIONS TEST PROGRAMS

OVERVIEW OF TEST PROGRAMS

The Memory and Memory Functions Diagnostic Test Programs provide verification of all memory boards and memory functions. They also provide board-level fault isolation for the system and program memory boards. The System Processor and I/O Diagnostic Test Program should be run prior to running this diagnostic program. Also, the first 16K of 8301 system memory must be operational before this test is run.

NOTE

The first 16K of 8301 system memory is tested during the ROM-based power-up tests.

The Memory and Memory Functions Test Programs are divided into test modules as shown in Table 4-10:

Table 4-10
Memory Test Modules

Test Module Number	Test Module
	MEMORY BOARD RAM TESTS
1	Memory Configurer
2	Bank Select Test (bank selection)
3	Row Select Test (data path test)
4	Parity Logic Test
5	Chip Select Test (data cell test)
6	Address Test
7	Refresh Test
8	Pattern Sensitivity Test (GALTCOL)
	DMA TESTS
9	DMA Static Test
10	DMA Functional Test
11	Write Protect and Memory Map Test
12	Memory Relocation Static Test
13	Memory Relocation Functional Test

The thirteen test modules are executed with six option selections. The six test options are divided into thirteen test modules as shown in Table 4-11.

Table 4-11
Relationship of Test Options, Programs, and Modules

Test Option	Test Program	Test Module Number
0	Run All Tests	1--7 and 9--13
1	Memory Board RAM Test	
	Short Test	1--7
	Exhaustive Test	1--8
2	DMA Tests	9--10
3	Write Protect and Memory Maps Static Test	11
4	Memory Relocation RAM Static Test	12
5	Memory Relocation Functional Test	13

NOTE

Test Modules 12 and 13 are bypassed if more than 32K of Program Memory is installed in the 8301 unit. These tests apply to operation with only 32K of memory.

The test option formats for the Memory and Memory Functions Test Program are described in the following paragraphs.

TEST OPTIONS

The Option Menu for the Memory and Memory Functions Test Program is shown in Display 4-9. This menu is displayed when item 2 from the Program Menu is selected. (Refer back to Display 4-4.)

```
8301 MEMORY DIAGNOSTICS                          VERSION 1.0
------------------------------------------------------------

                    OPTION MENU
                    -----------
0 - RUN ALL TESTS              ***** default *****
1 - MEMORY BOARD RAM TEST
2 - DMA TESTS
3 - WRITE PROTECT AND MEMORY MAP STATIC TEST
4 - MEMORY RELOCATION RAM STATIC TEST
5 - MEMORY RELOCATION FUNCTIONAL TEST

Type in desired option {<CR>} or {0--5 <CR>}._
```

Display 4-9. Option Menu for Memory and Memory Functions Test Program.

Option 0 --- Run All Tests

When Option 0 is selected, Test Modules 1--7 and 9--13 are continuously executed. (See Table 4-11 for a list of the test programs represented by Test Modules 1--7 and 9--13.) Two counters are displayed after each pass to indicate the number of times Test Modules 1--7 and 9--13 have executed and the number of failures encountered. On the first pass, Test Module 1 displays the system and program memory size detected and asks. "Is the memory size correct?" You must respond to this question before execution continues. On subsequent passes, the memory size and question are skipped and the memory detected from the first pass is used. Option 0 runs only the short memory tests. The long (exhaustive) tests can be run in Option 1. The display for Option 0 is as follows, when <CR> or Y<CR> (yes) is typed in response to the question on memory size:

```
---------------
| OPTION 0    |
---------------
        SYSTEM MEMORY  = 64K
        PROGRAM MEMORY = 64K
IS THE MEMORY SIZE CORRECT ? {Y or N <CR>} _

TEST RUNNING -- XX   ITERATION # XXXX       ERRORS = XXXX
```

The execution time for Option 0 at 2 MHz is as follows:

System Memory	Program Memory	Execution Time
64K	32K	3:26 min
64K	64K	4:44 min
64K	128K	7:20 min

Option 1 --- Memory Board RAM Test

If Option 1 is chosen, you can select the entire system and program memory or in 16K blocks any portion of either memory to test. You can also select a short test or exhaustive test. The short test includes Test Modules 1--7. The exhaustive test includes all tests in Test Modules 1--8. The Option 1, Sub-Option menu format is shown in Display 4-10.

The execution time for Option 1 at 2 MHz is as follows:

System Memory	Program Memory	Execution Times	
		Short	Exhaustive
64K	32K	3:15 min	23:30 min
64K	64K	4:33 min	32:54 min
64K	128K	7:09 min	51:42 min

NOTE

To properly select specific blocks of memory, the memory board must be strapped to correspond to the memory selected. Sub-Option 1 will test program memory boards that are strapped anywhere within the 16M-byte address range.

```
8301 MEMORY DIAGNOSTICS                          VERSION 1.0
-------------------------------------------------------------

                    OPTION MENU
                    -----------
0 - RUN ALL TESTS              ***** default *****
1 - MEMORY BOARD RAM TEST
2 - DMA TESTS
3 - WRITE PROTECT AND MEMORY MAP STATIC TEST
4 - MEMORY RELOCATION RAM STATIC TEST
5 - MEMORY RELOCATION FUNCTIONAL TEST

Type in desired option {<CR>} or {0--5 <CR>}. 1


                OPTION 1 - MEMORY BOARD RAM TEST
                --------------------------------
1 - ALL MEMORY                 ***** default *****
2 - SYSTEM    16K - 32K
3 - SYSTEM    32K - 48K
4 - SYSTEM    48K - 64K
5 - PROGRAM    0K - 16K
6 - PROGRAM   16K - 32K
7 - PROGRAM   32K - 48K
8 - PROGRAM   48K - 64K
9 - PROGRAM   64K - 96K
A - PROGRAM   96K - 128K
B - PROGRAM  128K - 160K
C - PROGRAM  160K - 192K
D - PROGRAM  192K - 224K
E - PROGRAM  224K - 256K

Type in desired sub-option {<CR>} or {i.e. 2,3,4 <CR>} _

1 - SHORT TESTS
2 - EXHAUSTIVE TESTS

Type in desired type test to run {<CR>} or {1,2 <CR>} _
```

Display 4-10. Option 1 --- Memory Board RAM Test.

Option 2 --- DMA Tests

When Option 2 is selected, Test Modules 9 and 10 are continuously executed. After this option is selected the sub-option menu shown in Display 4-11 is displayed. This permits you to select static and/or functional tests.

The execution time for Option 2 at 2 MHz is as follows:

Sub-Option Number	Test	Execution Time
1	Static and Functional Tests	7 sec
2	Static Test Only	1 sec
3	Functional Tests Only	6 sec

```
8301 MEMORY DIAGNOSTICS                          VERSION 1.0
------------------------------------------------------------

                    OPTION MENU
                    -----------
0 - RUN ALL TESTS              ***** default *****
1 - MEMORY BOARD RAM TEST
2 - DMA TESTS
3 - WRITE PROTECT AND MEMORY MAP STATIC TEST
4 - MEMORY RELOCATION RAM STATIC TEST
5 - MEMORY RELOCATION FUNCTIONAL TEST

Type in desired option {<CR>} or {0--5 <CR>}. 2

                     DMA TESTS
                     ---------
1 - STATIC AND FUNCTIONAL TESTS     ***** default *****
2 - STATIC TEST ONLY
3 - FUNCTIONAL TESTS ONLY

Type in desired sub-option {<CR>} or {1--3 <CR>} _
```

Display 4-11. Option 2 --- DMA Tests.

Three counters are displayed after each time the test is repeated. The counters indicate the test number, the number of times the test has executed, and the number of errors detected. They are displayed following the Display Option menu as shown in Display 4-12. The LED on the Front Panel labeled DMA flashes during the running of the DMA Functional Tests.

```
                    DISPLAY OPTION
                    --------------

1 - DISPLAY MESSAGES ON TERMINAL          ***** default *****
2 - DISPLAY MESSAGES ON PRINTER & TERMINAL
3 - NO DISPLAY OR PRINT
H - HELP

Type in display option {<CR>} or {1 - 3 or H and <CR>}._

---------------
| OPTION 2    |
---------------
TEST RUNNING -- XX      ITERATION # XXXX      ERRORS = XXXX
```

Display 4-12. Option 2 --- Test Running Display.

Option 3 --- Write Protect and Memory Maps Static Test

If Option 3 is selected, Test Module 11 is run continuously. Three counters are displayed after each pass to indicate the test number, the number of times the test has been run, and the number of failures detected. The Test Running and Option number are displayed following the Display Option menu as follows:

```
---------------
| OPTION 3    |
---------------
TEST RUNNING -- XX     ITERATION # XXXX      ERRORS = XXXX
```

The execution time for this option at 2 MHz is <1 sec.

Option 4 --- Memory Relocation Static Test

When Option 4 is selected, Test Module 12 is run continuously. Three counters are displayed after each pass to indicate the test number, the number of times the test has been run, and the number of failures detected. The Test Running and Option number are displayed following the Display Option menu as follows:

```
---------------
| OPTION 4    |
---------------
TEST RUNNING -- XX     ITERATION # XXXX      ERRORS = XXXX
```

The execution time for Option 4 at 2 MHz is <1 sec.

NOTE

This test fails if there is more than 32K of program memory installed in the unit.

Option 5 --- Memory Relocation Functional Test

When Option 5 is selected, Test Module 13 is run continuously. Three counters are displayed after each pass to indicate the test number, the number of times the test has been run, and the number of failures detected. The Test Running and Option number are displayed following the Display Option menu as follows:

```
---------------
| OPTION 5    |
---------------
TEST RUNNING -- XX    ITERATION # XXXX     ERRORS = XXXX
```

The execution time for Option 5 at 2 MHz is 5 sec.

NOTE

This test fails if there is more than 32K of program memory installed in the unit.

MEMORY BOARD RAM TEST

This test determines how much system and program memory is installed in the 8301 and then performs tests on the amount of system and program memory detected.

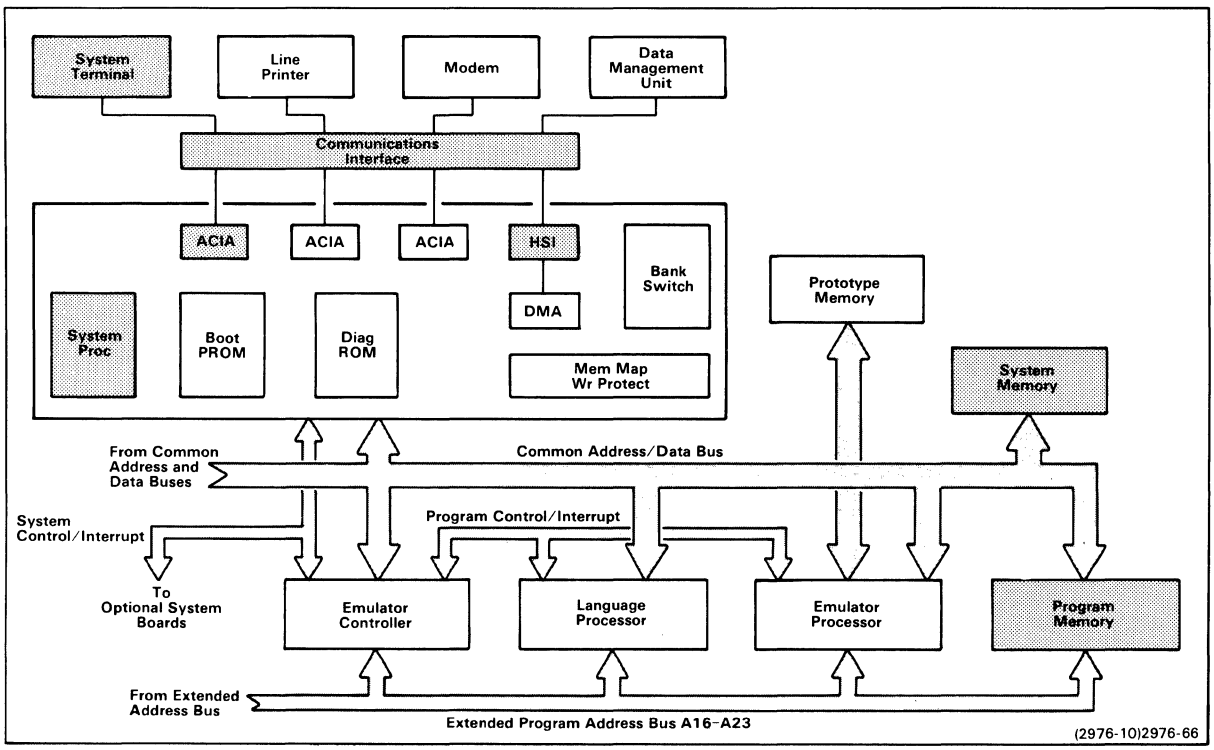


Fig. 4-4. 8301 MDU block diagram. (Memory Board RAM Tests)

MEMORY CONFIGURER (02/0001)

Circuit Boards Tested

System Controller, System RAM, and Program Memory. (See Fig. 4-4.)

Function

This test determines how much system memory and program memory is installed in the 8301. This test examines system memory (up to 64K) and program memory (up to 256K) in 4K memory blocks. The amount of memory detected in both system and program memories is stored in a memory table and displayed on the system terminal at the completion of the test.

When this test is run in the SELECT mode, the user must verify that the "MEMORY DETECTED" is correct. In the AUTOMATIC mode, the "MEMORY DETECTED" is displayed and no response from the user is required.

NOTES

1. Bank switching must be used when the system processor addresses system memory above 3FFF (4000--7FFF) or any portion of program memory. Bank switching permits 16K blocks of system or program memory addresses to be switched into the system processor's upper 16K address space (4000--7FFF). Whenever a failure is detected, the displayed error address is the true address.

2. The 32K static Program Memory board has a low and high memory array with 16K RAMs in each array. The physical layout of RAMs for each memory array consists of four rows of 4K x 1 RAM devices. The even addresses access one 4K row, while the odd addresses access another row. The four rows in the arrays are physically addressed by the system processor's upper 16K address space as follows:

First Row	All even addresses 4000--5FFE
Second Row	All odd addresses 4001--5FFF
Third Row	All even addresses 6000--7FFE
Fourth Row	All odd addresses 6001--7FFF

3. The 64K System RAM board is physically configured in four banks. Each bank is addressed in the following logical order:

Bank 1	0000--3FFF
Bank 2	4000--7FFF
Bank 3	8000--BFFF
Bank 4	C000--FFFF

4. The Program Memory board can be strapped so that it may be addressed anywhere within the 16M-byte address range. This test will scan the entire 16M-byte address range and test the first 256K detected. If this test indicates 256K of program memory is detected, but less than that is installed, verify that the extended bank jumper J7171 on the Program Memory board is in the enable position (across pins 1 and 2). Refer to Section 2, Installation, of this manual for the location of this jumper.

5. If a parity error occurs during this test the following display will appear on the system terminal:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        Error Code = 02/YYYY

***** PARITY ERROR *****
ADDRESS = XXXX

-----------------------------------
 PRIMARY SUSPECT = SYSTEM RAM BOARD
-----------------------------------
```

In the preceding display the "YYYY" is the same number displayed in the "TEST RUNNING" line. In general, another error code will also be displayed following the parity error display.

6. The following is to be used for test purposes only and only if you suspect the System RAM board to be faulty. The System RAM board can be used as program memory and the Program Memory board can be used as system memory. This configuration would be used if the power-up tests fail and the error code indicates a System RAM board memory access failure. In this configuration, the operating system can be booted and the Dics-Based Diagnostics run. The Disc-Based Diagnostics provide more exhaustive testing to the overall system. This configuration can be achieved as follows:

   a. Remove the System RAM board and move jumper J6140 from pins 1 and 2 to pins 2 and 3. Refer to Section 2, Installation, of this manual for the location of jumper J6140.

   b. Replace the System RAM board to the same location in the Main Interconnect board.

   c. Remove all of the Program Memory boards from the Main Interconect board. On one Program Memory board move jumper J6175 to pins 2 and 3, which selects the lower memory addresses OK--32K. Move jumper J6179 to pins 2 and 3, which selects a special System Memory configuration.

   d. Replace the Program Memory board to a program memory location in the Main Interconnect board.

   e. The system is now configured with the Program Memory board as system memory and the System RAM board as program memory.

   f. When this testing configuration is completed, return the jumpers and boards to their normal positions.

7. For 8301 units that have Version 1.x of the Boot ROM installed, the following message will appear before the Memory Size is printed.

---> Boot Ver 1.x - Prog. Mem. >64K not tested.

This indicates your Program Memory board(s) should be strapped with the Extended Memory feature DISABLED. (Jumper J7171 on both Program Memory boards (if installed) should be across pins 2 and 3.) If the jumper is in the ENABLED position (across pins 1 and 2), the test will think there is 256K of program memory and the test will fail.

For Boot ROM Version 2.x, the Program Memory board(s) must be strapped with the Extended Memory feature ENABLED (J7171 across pins 1 and 2).

Description

1. Starting with the second bank of system memory (4000--7FFF) (16K--32K), the 16K memory block is switched into the system processor's upper 16K address space.

2. The test examines the 16K block by accessing it at four locations. Data byte 55 is written to each address location. Each location is then read. If the data returned is 00, it is assumed that memory is not present. The results of this comparison is stored in a memory table and the next 16K block of memory is switched into the system processor's upper address space.

3. Steps 1 and 2 are repeated for the remaining 16K blocks of memory. This test will detect up to a maximum of 64K system memory. It also detects up to a maximum of 256K program memory anywhere within the 16M-byte address range (24-bit address and extended address buses).

4. When the test is completed in the Automatic Mode, the system and program memory blocks (detected by the test and stored in the memory table) are displayed on the system terminal as follows: (No user response is required.)

   SYSTEM MEMORY= [amount of memory detected]

   PROGRAM MEMORY= [amount of memory detected]

5. If the memory test is run in Select Mode, the test sequence (when completed) is suspended until you respond to questions. In addition to displaying the amount of system and program memory detected, you must respond to the questions of memory size being correct and if not correct, whether you wish to continue.

   A Y<CR> answer (for yes) to both questions starts execution of the next test module in sequence. A N<CR> answer (for no) to the first question and a Y<CR> answer for the second, starts execution of the next test module in sequence; however, only the memory detected will be tested. (Same as a yes answer to both questions.) A N<CR> to both questions

branches back to the Memory Option Menu. A SYNC pulse is provided each time the test module is rerun.

NOTE

The ESC and BREAK keys perform the following functions during the execution of most disc-based diagnostic test programs: The ESC key suspends execution of the test or routine and returns to the OPTION MENU. The BREAK key terminates the test program and returns to the RUN MODE MENU.

6. When N<CR> is answered for both questions, an error code is also displayed on the system terminal as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          Error Code = 02/0001

-----------------------------------------
  PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
SECONDARY SUSPECT = MEMORY BOARD
-----------------------------------------
```

NOTE

The error code is not displayed until after the second question is answered with a N<CR>.

BANK SELECT TEST (02/0002)

Circuit Boards Tested

System Controller, System Memory, and Program Memory. (See Fig. 4-4.)

Function

This test verifies that the Bank Select logic works correctly for the system and program memory detected in the previous test. This test verifies that the first 1K block within each 16K bank of system and program memory can be uniquely addressed. Parity is disabled for this test.

Description

1. The first 1K block within each 16K block of memory detected in the Memory Configurer test is filled with a data pattern, as listed in Table 4-12. (Table 4-12 shows a program memory configuration of 128K strapped for the bottom of the 16M-byte address space. The addresses of the program memory banks can varry from 00 0000 to FF FFFF.)

Table 4-12
Data Pattern for Memory Bank Tested

Order Tested	Memory Bank Tested	Memory Board Tested	Address of Bank	Data Pattern Loaded
(no test)	04	System Memory (0K--16K)	00 0000--00 3FFF	----
1	05	System Memory (16K--32K)	00 4000--00 7FFF	11
2	06	System Memory (32K--48K)	00 8000--00 BFFF	22
3	07	System Memory (48K--64K)	00 C000--00 FFFF	33
4	00	Program Memory (0K--16K)	00 0000--00 3FFF	44
5	01	Program Memory (16K--32K)	00 4000--00 7FFF	55
6	02	Program Memory (32K--48K)	00 8000--00 BFFF	66
7	03	Program Memory (48K--64K)	00 C000--00 FFFF	77
8	00	Program Memory (64K--80K)	01 0000--01 3FFF	88
9	01	Program Memory (80K--96K)	01 4000--01 7FFF	99
10	02	Program Memory (96K--112K)	01 8000--01 BFFF	AA
11	03	Program Memory (112K--128K)	01 C000--01 FFFF	BB

2. The first 256 locations of the 1K block within each 16K bank are then read and checked for a correct half-byte. (That is, in Bank 05 a "X1" or "1X" is looked for in each byte. "X" = don't care.) Only one good half-byte of the 256 locations checked is needed to pass the test for the entire bank. The banks are sequentially switched as noted in Table 4-12. If no correct half-byte is found, an error code and supporting data are displayed on the system terminal. The test also branches to a looping routine if an error is detected. This routine repeatedly reads the 256 locations in the failing bank starting with the first location of the bank. A SYNC pulse is provided each time the 256 locations are repeated.

3. In addition to displaying the error codes, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        Error Code = 02/0002

ACTUAL DATA = [data read on the 256th location read (last read)]
CORRECT DATA = [correct data byte]
ADDRESS = [starting address of 16K block that failed]
BANK TESTED = [16K bank under test] (See Table 4-12.)
-----------------------------------------
  PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
SECONDARY SUSPECT = MEMORY BOARD
-----------------------------------------
```

ROW SELECT TEST (02/0003)

Circuit Boards Tested

System Memory and Program Memory. (See Fig. 4-4.)

Function

The test verifies that each 4K row of RAM within each 16K block can be uniquely selected. This test is identical to the previous Bank Select Test except the block under test is 4K instead of 16K. Parity is disabled for this test.

Description

1. This test uses a similar data pattern as described for the previous test in Table 4-12. Each 4K block of memory is filled with a separate data pattern.

   This test reads the first 256 locations of each 4K block. The data byte at each of the 256 locations is checked for a correct half-byte (same as the previous test). Only one good half-byte of the 256 locations checked is needed for the 4K block under test to pass. If no correct half byte is found, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if an error is detected. This routine repeatedly loops the 256 locations in the failing block starting with the first location of the 4K block. A SYNC pulse is provided each time the 256 locations are repeated.

2. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                              Error Code = 02/0003

ACTUAL DATA = [data read on the 256th location read (last read)]
CORRECT DATA = [correct data byte]
ADDRESS = [starting address of 4K block that failed]
BANK TESTED = [16K bank under test] (See Table 4-12.)
------------------------------
PRIMARY SUSPECT = MEMORY BOARD
------------------------------
```

3. Step 1 is repeated until all 4K blocks of memory detected are tested.

PARITY LOGIC TEST (02/003A--003D)

Circuit Board Tested

System Memory (See Fig. 4-4.)

Function

This test verifies that the parity generator logic, parity check logic, parity interrupt, and the parity error address latch on the System RAM board are functioning correctly.

Description

The four parity logic tests are performed as follows:

1. The parity is turned off and also complemented. Read and write operations are performed to the same address in memory. No interrupt should occur. If an interrupt does occur, the error code displayed on the system terminal is "02/003A."

2. The parity is turned on and set for true parity. An odd parity pattern of eight bytes are written to and read from the same address location in memory. No interrupt should occur. If an interrupt does occur, the error code displayed on the system terminal is "02/003B."

NOTE

The odd parity pattern consists of a walking "1's" test as follows:

1. 0000 0001
2. 0000 0010
3.--7. (pattern continues)
8. 1000 0000

The patterns continue until 8 patterns are formed. The "1" moves one bit to the left on each succeeding pattern.

3. Parity is the same as above. An even parity pattern of four bytes are written to and read from the same address location in memory. No interrupt should occur. If an interrupt does occur, the error code displayed on the system terminal is also "02/003B."

NOTE

The even parity pattern consists of a walking "1's" test as follows:

1. 0001 0001
2. 0010 0010
3. 0100 0100
4. 1000 1000

4. Upon completion of the above tests the parity is complemented which should generate a parity error and parity interrupt. If an interrupt does not occur, the error code displayed on the system terminal is "02/003C."

5. When a parity interrupt is generated, in the above step, the address of the parity error is latched and checked for correctness. If the address is not correct, the error code displayed on the system terminal is "02/003D."

6. In addition to displaying the error code, additional supporting data is displayed as follows:

>>>>>>>>>>>>>>>> DIAGNOSTIC FAILURE <<<<<<<<<<<<<<<<

Error Code = [See Table 4-13.]

PARITY LOGIC PROBLEM

Table 4-13
Parity Logic Error

Error Code	Description
02/003A	Parity Always Enabled
02/003B	Parity Generator or Checker Problem
02/003C	Parity Always Disabled
02/003D	Parity Address Latch Incorrect

CHIP SELECT TEST (02/0004)

Circuit Boards Tested

System Memory and Program Memory. (See Fig. 4-4.)

Function

This test verifies that each individual memory device (RAM) can be selected, and that there is no interaction between the data bits. All the cells in each device are tested for static failures. This is accomplished by a "WALKING 1's" and "WALKING 0's" patterns. (See notes following this paragraph.) Parity is disabled during the "WALKING 1's" pattern and enabled during the "WALKING 0's" pattern.

NOTES

1. "WALKING 1's" Test --- The 4K block of memory under test is filled with a background pattern of "00's". The Walking "1's" test consists of four patterns as follows:

    1. 0001 0001
    2. 0010 0010
    3. 0100 0100
    4. 1000 1000

The first pattern is written to each location in the 4K block. The pattern is then read at each location. The pattern is shifted to the left and repeated. This is done 4 times or until each pattern has been written and read once. This procedure is then repeated for each 4K block of memory.

2. "WALKING 0's" Test --- The 4K block of memory under test is filled with a background pattern of "FF's". The Walking "0's" test consists of four patterns as follows:

    1. 0110 1110 -- (Generates an odd parity.)
    2. 1101 1101
    3. 1011 1011
    4. 0111 0111

The first pattern is written to each location in the 4K block. The pattern is then read at each location. The pattern is shifted to the left and repeated. This is done 4 times or until each pattern has been written and read once. This procedure is then repeated for each 4K block of memory.

Description

1. This test fills each location in the 4K block of memory under test with a background pattern of "00's". The test then writes the first test pattern of the Walking "1's" patterns to each location in the 4K block of memory. Each location is then read and compared to the pattern written. If an error is detected, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if a failure is detected. This routine writes the Walking "1's" pattern to each location of the 4K block again, up to and including the failed location. The failed location is then read 256 times. If an error is still detected the looping routine is repeated. A SYNC pulse is provided each time the failed location is read 256 times.

2. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          Error Code = 02/0004

ACTUAL DATA = [incorrect data byte]
CORRECT DATA = [correct data byte]
ADDRESS = [indicates failing address]
BANK TESTED = [16K bank under test] (See Table 4-12.)
------------------------------
PRIMARY SUSPECT = MEMORY BOARD
------------------------------
```

3. The tests in Steps 1 and 2 above are repeated for each of the four Walking "1's" patterns. (See Note 1 above for a description of the four patterns.) This completes the Walking "1's" test for the first 4K block of memory.

4. The tests in Steps 1, 2, and 3 above are repeated for each 4K block within each 16K memory bank. This completes the Walking "1's" test for both system and program memory.

5. The Walking "0's" test is also performed. This test follows the same sequence as the Walking "1's" test, except the background pattern is "FF's" at the start of the test and the four test patterns are complemented data from the Walking "1's" test patterns. (See Note 2 above for a description of the Walking "0's" test.)

ADDRESSING TEST (02/0005)

Circuit Boards Tested

System Memory and Program Memory. (See Fig. 4-4.)

Function

This test verifies that the addressing capabilities of the address decoders in each individual memory device (RAM) are operating correctly. This test uses a "MARCHING 1's" and "MARCHING 0's" patterns to provide the testing. Parity is enabled for this test.

Description

1. This test fills each location in the 16K block of memory under test with a background pattern of "00's". The Marching "1's" test is then executed. The lowest location in the block is read, a data byte of "FF" is written to the location, and the address is incremented by 1. The next location is read, a data byte of "FF" is written to the location, and the address is incremented by 1. This sequence is repeated until all addresses are read and written to. The 16K memory block is now filled with "1's". The highest location is read again, a data byte of "00" is written to the location, and the address is decremented by 1. The next location is read, a data byte of "00" is written to the location, and the address is decremented by 1. This sequence continues until all locations are read and written to. The 16K memory block is now filled with "0's". If an error is detected, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if a failure is detected. This routine

rewrites the background pattern of "00's", starts the Marching "1's" test again (up to or up and down to the failing location), and reads the location 256 times. If an error is still detected, the looping routine is repeated. A SYNC pulse is generated each time the failed location is read 256 times.

2. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          Error Code = 02/0005

ACTUAL DATA = [incorrect data byte]
CORRECT DATA = [correct data byte]
ADDRESS = [indicates failing address]
BANK TESTED = [16K bank under test] (See Table 4-12.)
------------------------------
PRIMARY SUSPECT = MEMORY BOARD
------------------------------
```

3. The Marching "0's" test is also performed. This test is the complement of the Marching "1's" test. If an error is detected the same procedure is followed as with the Marching "1's". Note that the Marching "1's" test will be conducted first and then the Marching "0's" test will run to the failed location. The same error code and supporting data are displayed on the system terminal.

4. The tests in Steps 1, 2, and 3 above are repeated for each 16K memory block in both system and program memory.

REFRESH TEST (02/0006)

Circuit Boards Tested

System Memory and Program Memory. (See Fig. 4-4.)

Function

This test verifies that data written to the RAMs is not lost when the RAMs are not addressed for a period of time. Parity is enabled for this test.

Description

1. This test sequentially fills each 16K block of memory with a count pattern (00--FF repeated). When both system and program memories are filled, a two second delay is imposed. After the delay, each location in memory is sequentially checked to ensure that the data has not changed. If an error is detected, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if a failure is detected. This routine starts reading the 16K block under test from the lowest location up to the failing location. The failed location is then read 256 times. If an error is still detected the looping routine is repeated. A SYNC pulse is generated each time the failed location is read 256 times.

2. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          Error Code = 02/0006

ACTUAL DATA = [incorrect data byte]
CORRECT DATA = [correct data byte]
ADDRESS = [indicates failing address]
BANK TESTED = [16K bank under test] (See Table 4-12.)
------------------------------
PRIMARY SUSPECT = MEMORY BOARD
------------------------------
```

PATTERN SENSITIVITY TEST (GALTCOL) (02/0009)

Circuit Boards Tested

System Memory and Program Memory. (See Fig. 4-4.)

Function

The Pattern Sensitivity Test uses a test pattern referred to as the "galloping-column" pattern (GALTCOL). The GALTCOL pattern checks address transitions between every cell in a row with respect to all other cells in that row and noise coupling between all cells in the same column. The test is run twice, once with data and once with complemented data. This is an exhaustive memory test and therefore will only be run when specifically

called for as a sub-option of the Memory Board RAM Test (Select Mode, Option 1). Parity is enabled for this test.

Description

1. This test is run using 4K blocks of memory at a time. Due to the complexity of the test, the flow diagrams used in the previous tests will not be shown. The GALTCOL pattern is generated according to the following instructions:

    1. A background pattern is written into the 4K row (all ones or zeros).

    2. A test word (complement of background) is written into location zero.

    3. A read and test cycle is executed, which checks address transitions between the test word and all other cells within the same row. During the first pass, this pattern is: READ LOC 0, LOC 64, LOC 0, LOC 128, LOC 0,.....LOC 4032, LOC 0.

    4. The test-word location (LOC 0 on first pass) is rewritten to its original value.

    5. An evaluation is performed to determine if the test word has been written into all memory locations.

    6. If not, the test word is written into the next sequential location (location two during the first pass).

    7. Steps 3 through 6 are repeated until the test word has been written into all memory locations.

    8. The test is then repeated using complemented data.

2. If an error is detected, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if a failure is detected. This routine reruns the GALTCOL pattern test on the failed 4K block of memory. A SYNC pulse is provided at the starting location of the failed 4K block.

3. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                              Error Code = 02/0009

ACTUAL DATA = [incorrect data byte]
CORRECT DATA =[correct data byte]
ADDRESS =[indicates failing address]
BANK TESTED = [16K bank under test] (See Table 4-12.)
-----------------------------
PRIMARY SUSPECT = MEMORY BOARD
-----------------------------
```

DMA TESTS

The DMA tests are divided into a static test and a functional (dynamic) test. The static test addresses six of the eight registers in the DMA device. (The 8301 does not use the other two registers.) Data is written to and read from each of the six register. The functional test transfers four blocks of data between memories to verify DMA memory-to-memory operations. The parity is enabled for all DMA tests.

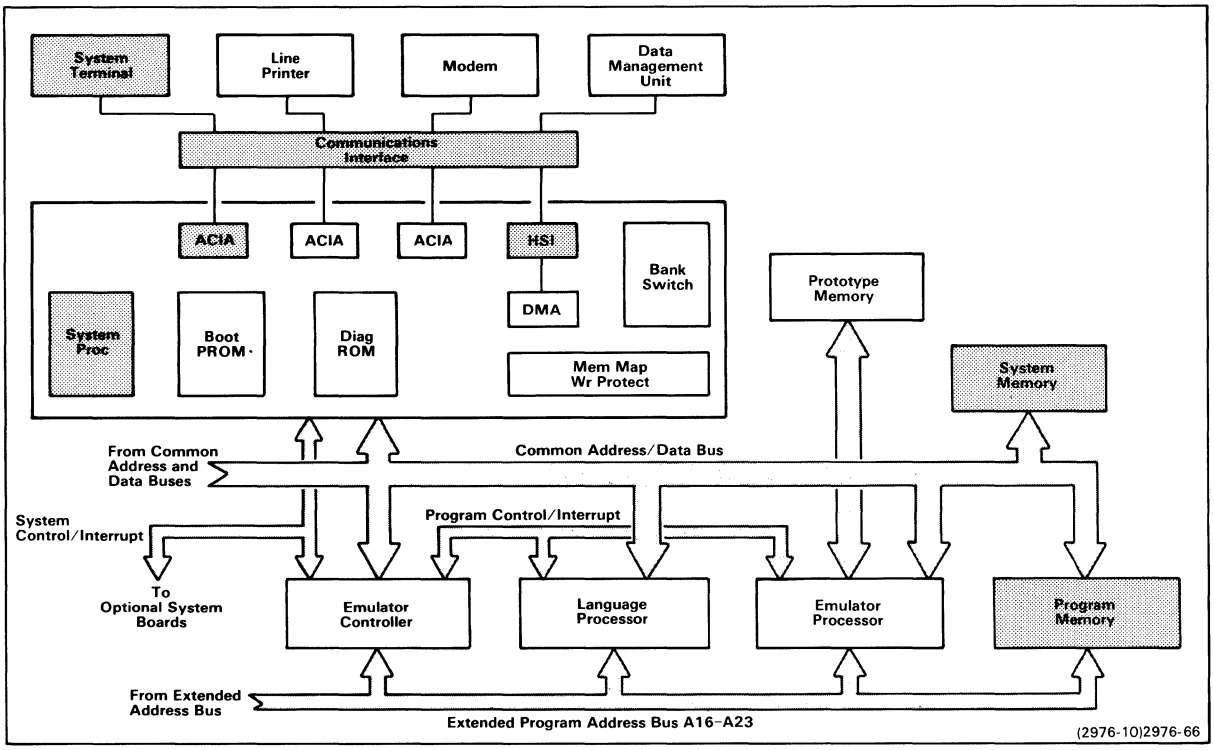


Fig. 4-5. 8301 MDU block diagram. (DMA Tests)

DMA STATIC TEST (02/000A)

Circuit Board Tested

System Controller. (See Fig. 4-5.)

Function

The DMA device contains eight (only six are tested) 16-bit registers; four Address registers and four Terminal Count (TC) registers. Each register can be addressed, written to, and read. This static test verifies that each of the six registers has these capabilities. The Walking "1's" and Walking "0's" pattern is used to test the registers. Refer to the following notes for a description of the Walking "1's" and "0's" test pattern.

NOTES

1. "WALKING 1's" Test --- The register under test is filled with a background pattern of "00's". The Walking "1's" test consists of 16 patterns as follows:

    1. 0000 0000 0000 0001

    2. 0000 0000 0000 0010

    3. 0000 0000 0000 0100

    4. 0000 0000 0000 1000

    5.--15. (Pattern continues)

    16. 1000 0000 0000 0000

    The patterns continue until 16 patterns are formed. The "1" moves one bit to the left on each succeeding pattern.

2. "WALKING 0's" Test --- The register under test is filled with a background pattern of "FF's". The Walking "0's" test consists of 16 patterns as follows:

    1. 1111 1111 1111 1110

    2. 1111 1111 1111 1101

    3. 1111 1111 1111 1011

    4. 1111 1111 1111 0111

    5.--15. (Pattern continues)

    16. 0111 1111 1111 1111

The patterns continue until 16 patterns are formed. The "0" moves one bit to the left on each succeeding pattern.

Description

1. This test starts with Channel 0 Address register and continues until all six registers are tested. The 16-bit register under test is filled with a background of "00's". Note that two writes to the register are required to load all 16 bits. The first pattern of the Walking "1's" test is written to the register. After each pattern is written, the register is then read to ensure the pattern was correctly stored in the register. When all 16 patterns are written and read, the Walking "1's" test is completed for that register. If an error is detected, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if a failure is detected. This routine repeats the entire walking test to the register under test. A SYNC pulse is generated at the start of each walking test.

2. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          Error Code = 02/000A

ACTUAL DATA = [incorrect data (2 bytes)]
CORRECT DATA = [correct data (2 bytes)]
DMA REGISTER = [register under test]
----------------------------------------
PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
----------------------------------------
```

3. In the preceding error code display, the DMA REGISTER number under test is the same as the I/O port address for the register. The relationship of I/O port address to DMA register is as follows:

90 = Channel 0 --- Address Register

91 = Channel 0 --- TC Register

92 = Channel 1 --- Address Register

93 = Channel 1 --- TC Register

94 = Channel 2 --- Address Register

95 = Channel 2 --- TC Register

4. The 16-bit register under test is filled with a background of "FF's". (Two writes are required.) All 16 patterns of the Walking "0's" test are written to and read from the register under test. Error code and supporting data displays are the same as that in Step 2 above. This completes the Walking "1's" and "0's" test for Channel 0 Address register.

5. Steps 1, 2, and 3 above are repeated for each of the remaining five registers as follows:

   Channel 0 --- TC Register

   Channel 1 --- Address Register

   Channel 1 --- TC Register

   Channel 2 --- Address Register

   Channel 2 --- TC Register

DMA FUNCTIONAL TEST (02/000B--000E)

Circuit Board Tested

System Controller. (See Fig. 4-5.)

Function

The DMA functional test consists of moving four blocks of data from memory-to-memory in four tests as follows:

1. SYSTEM -- SYSTEM --- A 4K block of data is moved from 4000--4FFF in system memory to 7000--7FFF in system memory.

2. SYSTEM -- PROGRAM --- A 16K block of data is moved from 4000--7FFF in system memory to 0000--3FFF in program memory.

3. PROGRAM -- PROGRAM --- The same 16K block of data is moved from 0000--3FFF in program memory to 4000--7FFF in program memory.

4. PROGRAM -- SYSTEM --- The same 16K block of data is moved from 4000--7FFF in program memory to 4000--7FFF in system memory.

Description

System-to-System.

1. This test sequentially fills a 4K block of system memory (4000--4FFF) with a count pattern (00--FF repeated). Each data byte is read after it is written to ensure the data is good. The test then moves the 4K block of data to another location in system memory (7000--7FFF). The data is read again to ensure the moved data is still good. If an error is detected when the data is read before or after the move, an error code and supporting data is displayed on the system terminal.

System-to-Program.

2. This test uses the same procedures as Step 1, except for the following:

   - The memory block filled with the count pattern is 16K in system memory (4000--7FFF).
   - The 16K block is moved from system memory to program memory (0000--3FFF).
   - If an error is found, the error code displayed on the system terminal is "02/000C".

Program-to-Program.

3. This test uses the same procedures as Step 2, except for the following:

   - The 16K data block is located in program memory (0000--3FFF).
   - The 16K block is moved from program memory to program memory (4000--7FFF).
   - If an error is found, the error code displayed on the system terminal is "02/000D."

Program-to-System.

4. This test uses the same procedures as Step 3, except for the following:

   - The 16K data block is located in program memory (4000--7FFF).
   - The 16K block is moved from program memory to system memory (4000--7FFF).
   - If an error is found, the error code displayed on the system terminal is "02/000E."

5. The four DMA functional tests described in Steps 1 through 4 branch to a looping routine if a failure is detected during any of the tests. This routine repeats the DMA test that is executing when the error is detected. A SYNC pulse is generated each time the test is started.

6. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        Error Code = [See Table 4-14]

ACTUAL DATA = [incorrect data byte]
CORRECT DATA = [correct data byte]
ADDRESS = [indicates failed address]
----------------------------------------
PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
----------------------------------------
```

Table 4-14
DMA Error Code and Transfer Address

Error Code	Failed Test	Failed Address	Failed Memory
02/000B	System--System	7000--7FFF	System
02/000C	System--Program	0000--3FFF	Program
02/000D	Program--Program	4000--7FFF	Program
02/000E	Program--System	4000--7FFF	System

WRITE PROTECT AND MEMORY MAP STATIC TEST

The Memory Map and Write-Protect Map RAMs are checked by two static tests. The first is a data byte test. The second is an address line test.

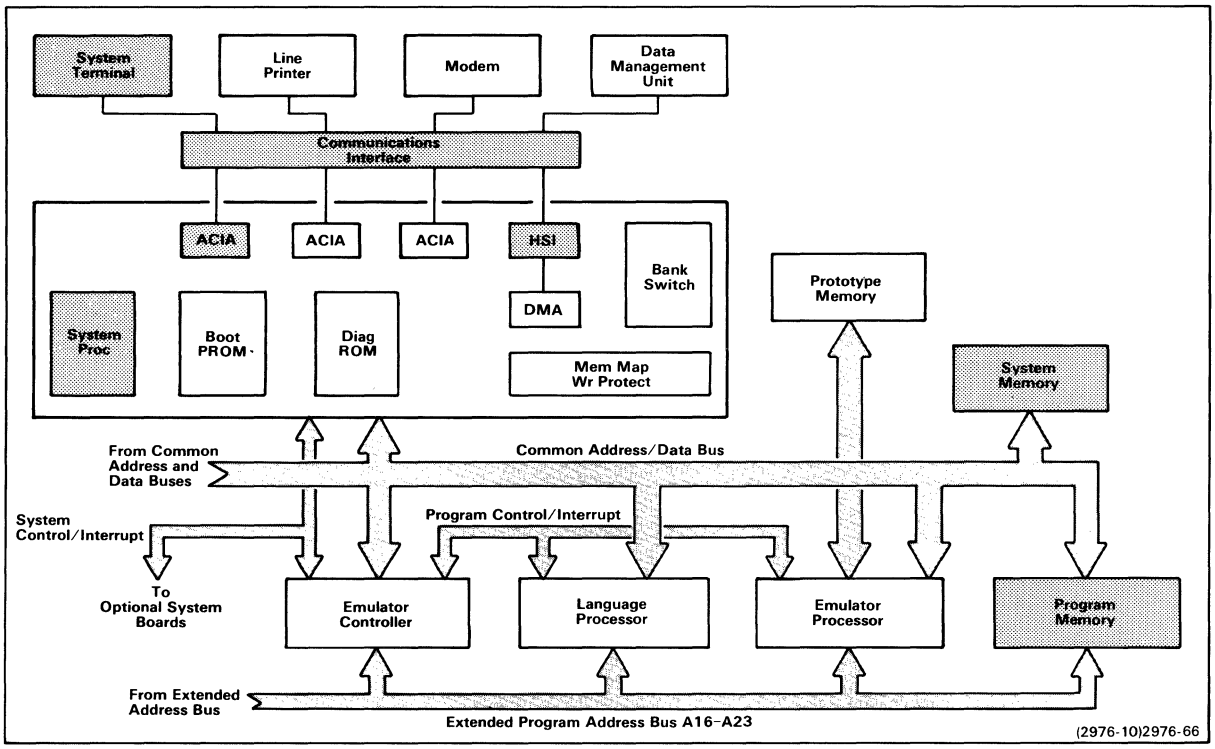


Fig. 4-6. 8301 MDU block diagram.
(Write Protect and Memory Map Static Tests)

DATA BYTE TEST (02/0010)

Circuit Board Tested

System Controller. (See Fig. 4-6.)

Function

The Memory Map and Write-Protect Map each consists of two 256x1-bit RAM storage devices, for a total of 512 bits of storage capacity in each map. The RAMs are addressed by the uppermost 512 addresses (FE00--FFFF) of the system processor's address space. When the RAMs are accessed, data bit D0 sets the bits in the Memory Map and data bit D2 sets the bits in the Write Protect Map.

Description

1. This test checks the data bits in the two sets of RAMS. The RAMs are enabled by writing a data byte "0F" to I/O port EE. This permits addresses FE00--FFFF to be written to.

2. A checkerboard pattern (00,05 repeated) is simultaneously written to both RAMs, when address locations FE00--FFFF are sequentially accessed (512 writes). Data byte "00" is written to address FE00 and a "0" is stored in each RAM. (Data bits D0 and D2 are both "0".) Data byte "05" is written to address FE01 and a "1" is stored in each RAM. (Data byte "05" converts to "0000 0101" binary, where both D0 and D2 are "1".) After address FFFF is written to, the test sequentially reads the data bits from both RAMs starting at address FE00 through FFFF (512 reads).

3. When Steps 1 and 2 are completed, the test repeats Step 2 using a reverse checkerboard pattern (05,00 repeated). When this step is completed all memory locations in both RAMS are tested.

4. The tests described in Steps 1 through 3 branch to a looping routine if a failure is detected during any read operation. This routine repeats the Data Byte Test. A SYNC pulse is generated each time the test is repeated.

5. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        Error Code = 02/0010

ACTUAL DATA = [incorrect data byte]
CORRECT DATA = [correct data byte]
ADDRESS = [indicates failing address, DE00--FFFF]
----------------------------------------
PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
----------------------------------------
```

ADDRESS ERROR TEST (02/0011)

Circuit Board Tested

System Controller. (See Fig. 4-6.)

Function

This test checks both RAMs for any address line shorts or opens. This test is executed immediately after the Data Byte Test.

Description

1. This test starts at address FE00 and simultaneously writes a data pattern (05,00,00 repeated) to both RAMs. The pattern (05,00,00) is written 170 times for 510 writes, plus two more writes of 05 and 00 for a total of 512 writes. After address FFFF is written to, the test sequentially reads the data bits from both RAMs starting at address FE00 through FFFF. If an error is detected, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if a failure is detected during any read operation. This routine repeats the Address Error Test. A SYNC pulse is generated each time the test is started.

2. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          Error Code = 02/0011

ACTUAL DATA = [incorrect data byte]
CORRECT DATA = [correct data byte]
ADDRESS = [indicates failing address, FE00--FFFF]
----------------------------------------
PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD
----------------------------------------
```

MEMORY RELOCATION TESTS

The purpose of the Memory Relocation circuitry is to relocate a 32K block of program memory (in even 4K blocks) to a 64K address space. This feature is enabled when only one Program Memory board is installed in the 8301. If your 8301 has more than 32K of Program Memory installed, these tests are bypassed. If it is desired to run these tests anyway, the upper board must be removed and J5175 on the lower board must be positioned to enable the Memory Relocation feature. Refer to Section 2, Installation for removal of the top cover and the correct setting of the jumper. The Memory Relocation tests consist of a static test and a functional test. The static test checks the data bits and address lines of the Relocation RAM, and the reset logic. The functional test relocates a 32K block of program memory (in even 4K blocks) to a 64K address space. The addresses of the relocated 4K blocks of memory are checked to verify the relocation. Refer to Section 11, System/Program Memory Board for additional information on the Memory Relocation circuitry.

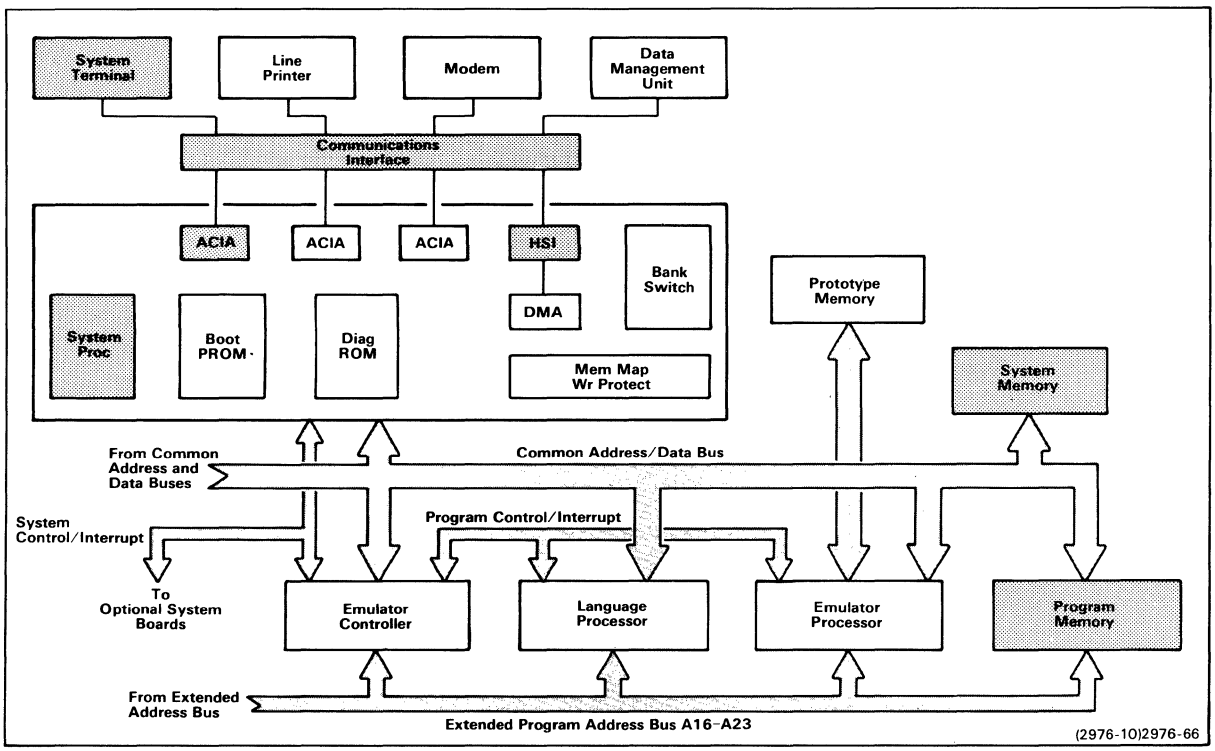


Fig. 4-7. 8301 MDU block diagram. (Memory Relocation Tests)

MEMORY RELOCATION RAM STATIC TEST (02/0014--0016)

Circuit Board Tested

Program Memory. (See Fig. 4-7.)

Function

The static test checks the Memory Relocation RAM with three tests as follows:

1. The first test uses a "WALKING "1's" and "0's" test to check the data bits in the 16 x 4-bit RAM.

2. the second test uses a count pattern (0F--00) for an address test.

3. The third test checks the reset logic circuitry associated with the RAM.

Description

Data Bit Test.

1. This test enables the Relocation RAM circuitry and resets the 16-bit counter by writting data byte "20" to I/O port address B8.

2. The test writes a WALKING "1's" and "0's" pattern to the Relocation RAM. The WALKING pattern consists of eight tests. Each test writes the same data in all RAM locations. All locations are then read before the next test pattern is written. The eight tests contain the following patterns:

1.	0001	5.	1110
2.	0010	6.	1101
3.	0100	7.	1011
4.	1000	8.	0111

The first WALKING pattern (0001) is written to all 16 locations in the RAM (16 writes). This pattern is then read from all locations (16 reads). The remaining seven patterns are then written and read (16 x 7 writes and 16 x 7 reads). If an error is detected, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if a failure is detected. This routine repeats the Data Bit test. A SYNC pulse is generated each time the test is repeated.

In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        Error Code = 02/0014

ACTUAL DATA = [incorrect data byte]
CORRECT DATA = [correct data byte]
ADDRESS = [indicates failing address, 00--0F]
BANK TESTED =[16K bank under test]
-----------------------------
PRIMARY SUSPECT = MEMORY BOARD
-----------------------------
```

Address Error Test

3. This test writes a 16 count pattern (0F, 0E, 0D, 0C, 0B, 0A, 09, 08, 07, 06, 05, 04, 03, 02, 01, and 00) to the Relocation RAM. The data in each of the 16 locations is different. Each location is then read to ensure the correct data is stored in the RAM. If an error is detected, an error code and supporting data is displayed on the system terminal. This test also branches to a looping routine if a failure is detected. This routine repeats the Address Error test. A SYNC pulse is generated each time the test is repeated.

Reset Error Test

4. This test writes a count pattern into the first 12 locations of the Relocation RAM (01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, and 0C). The last four locations still contain the pattern written by the test in Step 3 (03, 02, 01, and 00). A reset is sent to the Relocation circuitry be writing data byte "20" to I/O port address B8. The 16 RAM locations are then read to ensure the correct data is stored in the RAM. If an error is detected, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if a failure is detected. This routine repeats the Reset Error test. A SYNC pulse is generated each time the test is repeated.

5. In addition to displaying the error code, additional supporting data is displayed for Steps 3 and 4 as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        Error Code = [See Table 4-15]

ACTUAL DATA = [incorrect data byte]
CORRECT DATA = [correct data byte]
ADDRESS = [indicates failing address, 00--0F]
------------------------------
PRIMARY SUSPECT = MEMORY BOARD
------------------------------
```

Table 4-15
Memory Relocation Static Test
Address and Reset Error Code

Error Code	Error
02/0015	Address Error
02/0016	Reset Error

MEMORY RELOCATION FUNCTIONAL TEST (02/0017--001E)

Circuit Board Tested

Program Memory. (See Fig. 4-7.)

Function

The function test relocates a 32K block of program memory (in even 4K blocks) to a 64K address space. There are two address definitions that are important when discussing memory relocation.

Bus Addresses	These are the addresses that are present on the system address bus and are generated by the active processor.
Physical Addresses	These are the addresses that are presented to the chip-select decoders and the RAMs on the Program Memory board.

Physical addresses relate to the 32K block of memory to be relocated. Bus addresses relate to the 64K address space (maximum addressing capability for address bus lines A0--A15).

Figure 4-8 shows the relationship of the 32K physical addresses being relocated into the 64K address space. This is accomplished by writing data bytes to I/O port address B8. These data bytes are written to the Relocation RAM, which programs the RAM to relocate the designated physical addresses. Figure 4-9 shows the data bytes that are written into the Relocation RAM to provide the memory relocation shown in Fig. 4-8.

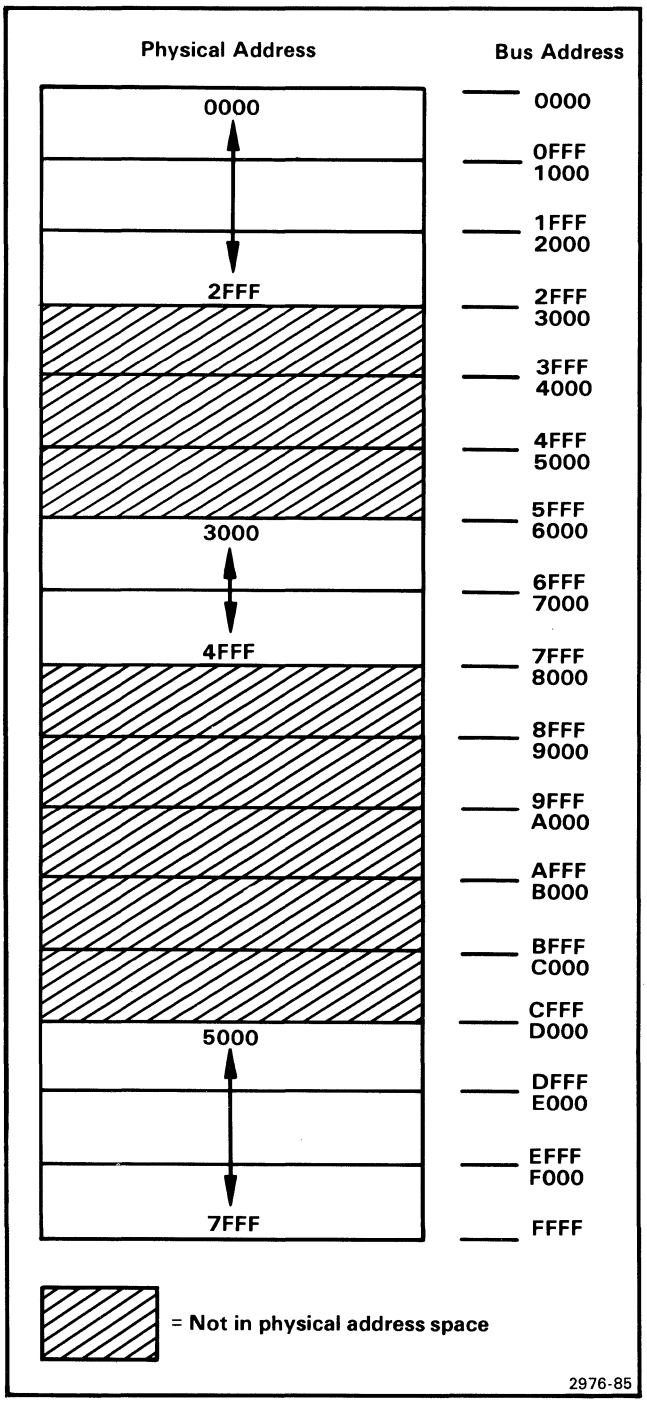


Fig. 4-8. Relationship of physical and bus addresses during memory relocation.

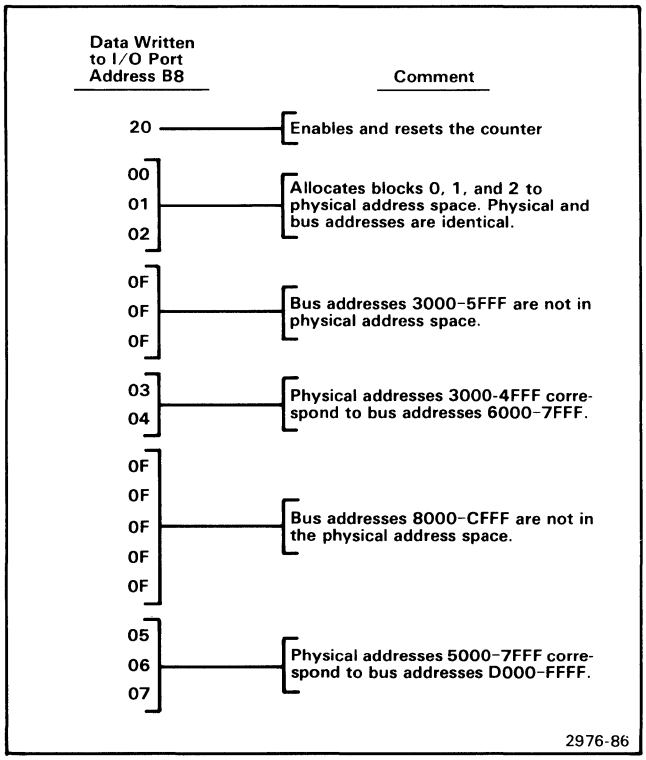


Fig. 4-9. Example of data written to the Relocation RAM.

Description

1. This function test starts by writing unique data into each 4K memory block of the lower Program Memory board (4K x 8 for a total of 32K writes). This unique data is written as follows:

Data Byte	Program Memory Addresses
11	0000--0FFF
22	1000--1FFF
33	2000--2FFF
44	3000--3FFF
55	4000--4FFF
66	5000--5FFF
77	6000--6FFF
88	7000--7FFF

2. Next the test resets the 16-bit counter and enables the Relocation RAM.

It then programs the Relocation RAM by writting the relocation data bytes into each location. Figure 4-9 shows the order and function of each byte.

3. After the Relocation RAM is programmed, the test reads those addresses (in 4K blocks) where the physical addresses are to be relocated. The correct data byte should be read. If an error is detected, an error code and supporting data are displayed on the system terminal. This test also branches to a looping routine if a failure is detected. This routine repeats the Memory Relocation Function test. A SYNC pulse is generated each time the test is repeated.

4. In addition to displaying the error code, additional supporting data is displayed as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        Error Code = [See Table 4-16]

ACTUAL DATA = [incorrect data byte]
CORRECT DATA = [correct data byte, see Table 4-16]
ADDRESS = [indicates failing bus address]
------------------------------
PRIMARY SUSPECT = MEMORY BOARD
------------------------------
```

Table 4-16
Error Codes for Memory Relocation Function Test

Error Code	Bus Addresses	Physical Addresses	Correct Data Byte
02/0017	0000--0FFF	0000--0FFF	11
02/0018	1000--1FFF	1000--1FFF	22
02/0019	2000--2FFF	2000--2FFF	33
02/001A	6000--6FFF	3000--3FFF	44
02/001B	7000--7FFF	4000--4FFF	55
02/001C	D000--DFFF	5000--5FFF	66
02/001D	E000--EFFF	6000--6FFF	77
02/001E	F000--FFFF	7000--7FFF	88

LANGUAGE PROCESSOR TEST PROGRAMS

OVERVIEW OF TEST PROGRAMS

The Language Processor Test programs provide verification of the Language Processor board and some of the logic circuitry of the Emulator Controller board. The remainder of the Emulator Controller board diagnostic testing is performed with each Emulator Processor Diagnostic Test Program (optional to the 8550 system). Therefore, if a failure is detected with both Language Processor and Emulator Processor Diagnostic Test Programs, the Emulator Controller board has probably failed. Otherwise, a single failure points to either the Language Processor or Emulator Controller boards. The Language Processor operates similar to an emulator processor. The Emulator Controller ensures that only one processor (either system processor, emulator processor, or language processor) has control of the system address and data buses at any time.

The System Processor and Memory Test Programs should be executed before the Language Processor Test Programs are run.

The Language Processor Test Programs are divided into eight distinct test programs. These programs are executed with nine option selections listed in Table 4-17. The nine options are further divided into one or more test modules as shown in Table 4-17 for a total of 14 test modules.

Table 4-17
Relationship of Test Options, Programs, and Modules

Test Option	Test Program	Test Module Number
Option 0	Run All Tests	1--14
Option 1	Processor Inactive Test	1
Option 2	Processor Reset, SVC1 Test	2
Option 3	Processor Halt Test	3
Option 4	Processor Clock Test	4
Option 5	Processor Address Test	5
Option 6	Processor Data Test	6--7
Option 7	Z-80 CPU Test	8
Option 8	Emulator Controller Test	9--14

The test option formats for the Language Processor Test Programs are described in the following paragraphs.

TEST OPTIONS

The Option Menu for the Language Processor Test Programs is shown in Display 4-13. This menu is displayed when item 3 from the Select Mode--Program Menu is selected. Refer to Display 4-4.

```
8301 LANGUAGE PROCESSOR DIAGNOSTICS       VERSION 1.0
-----------------------------------------------------

                  OPTION MENU
                  -----------

0 - OPTION 0 - RUN ALL          ***** default *****
1 - OPTION 1 - PROCESSOR INACTIVE TEST
2 - OPTION 2 - PROCESSOR RESET, SVC1 TEST
3 - OPTION 3 - PROCESSOR HALT TEST
4 - OPTION 4 - PROCESSOR CLOCK TEST
5 - OPTION 5 - PROCESSOR ADDRESS BUS TEST
6 - OPTION 6 - PROCESSOR DATA BUS TEST
7 - OPTION 7 - Z-80 CPU TEST
8 - OPTION 8 - EMULATOR CONTROLLER TEST
H - HELP

Type in desired option {<CR>} or {0--8 or H <CR>}
```

Display 4-13. Option Menu for Language Processor Test Programs.

Options 0 Through 8

When any option (0 through 8) from the Option Menu is selected, the test module(s) listed in Table 4-17 for that particular option are continuously executed. The option number selected is displayed in a box followed by the Test Running line. This line contains two counters that indicate the number of times the test module(s) are run and the number of failures encountered. The format of the display for each option is as follows:

```
---------------
| OPTION #    |
---------------
TEST RUNNING -- XX    ITERATION # = XXXX     ERRORS = XXXX
```

NOTE

The selections from the Language Processor Option Menu do not have sub-option displays or any statements requiring user reaction. The test modules are executed continuously until the ESC or BREAK key is pressed. The ESC key terminates the test and displays the Option Menu again. The BREAK key terminates the test and displays the original Run Mode Menu.

PROCESSOR INACTIVE TEST (03/0010)

CIRCUIT BOARD TESTED

Language Processor.

FUNCTION

This test verifies that the Language Processor board remains inactive when it is in the disabled state. This ensures that the language processor does not interfere with the communications between the system processor and other boards in the system.

DESCRIPTION

1. This test fills the program memory with No-Operation (NOP) instructions. The language processor is disabled and the test attempts to start it by halting the system processor. A "Halt" interrupt should be generated. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows:

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        ERROR CODE = 03/0010

CMD = FC [command byte written to I/O port address F9]
CONTROL = FF [control byte written to I/O port address F8]
EXPECTED INTERRUPTS = 0100 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-----------------------------------------
PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD
-----------------------------------------
```

PROCESSOR RESET AND SVC1 TEST (03/0020)

CIRCUIT BOARDS TESTED

Language Processor and Emulator Controller.

FUNCTION

This test verifies that the Z-80 CPU on the Language Processor board can be reset, start execution at location 0000, and generate an SVC1 interrupt.

DESCRIPTION

1. This test fills the first five locations (0000--0004) of program memory with code for generating an SVC1 interrupt. The remainder of program memory is filled with "Halt" instructions. The test then sends a "Reset" command to the language processor. A successful execution results in an "SVC1" interrupt. Otherwise, a "Halt" interrupt is likely to be generated. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        ERROR CODE = 03/0020

CMD = FC [command byte written to I/O port address F9]
CONTROL = DF [control byte written to I/O port address F8]
PC LAST WAS XXXX [PC Last value read]
PC LAST S/B 0002 [PC Last value should be]
EXPECTED INTERRUPTS = 0001 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-------------------------------------------
  PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD
SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD
-------------------------------------------
```

PROCESSOR HALT TEST (03/0030)

CIRCUIT BOARD TESTED

Language Processor and Emulator Controller.

FUNCTION

This test verifies that the language processor can return control to the system processor by executing a "Halt" instruction.

DESCRIPTION

1. This test fills all of program memory with "Halt" instructions. A "Reset" command is issued to the language processor. The language processor starts program execution at location 0000 and a "Halt" interrupt is issued after the first instruction is executed. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        ERROR CODE = 03/0030

CMD = FC [command byte written to I/O port address F9]
CONTROL = DF [control byte written to I/O port address F8]
PC LAST WAS XXXX [PC Last value read]
PC LAST S/B 0000 [PC Last value should be]
EXPECTED INTERRUPTS = 0100 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-------------------------------------------
  PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD
SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD
-------------------------------------------
```

PROCESSOR CLOCK TEST (03/0040)

CIRCUIT BOARDS TESTED

Language Processor and Emulator Controller

FUNCTION

This test verifies that the Z-80 CPU can operate with the SLOW clock (2.5 MHz) and the FAST clock (4.0 MHz). The jumper J4029 must be positioned in the FAST position. (Refer to Section 2, Installation for the location of this jumper.) The desired clock rate is selected by issuing a command to I/O port address E7. If data bit D2 is set to 1, the SLOW clock is selected. If data bit D2 is set to 0, the FAST clock is selected.

DESCRIPTION

1. This test executes a series of instructions, once with the Fast clock and again with the SLOW clock. In each case a predetermined result must be obtained to successfully pass the test. A "Halt" interrupt is generated at the end of the test. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        ERROR CODE = 03/0040

CMD = FC [command byte written to I/O port address F9]
CONTROL = DF [control byte written to I/O port address F8]
PC LAST WAS XXXX [PC Last value read]
PC LAST S/B 0037 [PC Last value should be]
EXPECTED INTERRUPTS = 0100 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-------------------------------------------
  PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD
SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD
-------------------------------------------
```

PROCESSOR ADDRESS BUS TEST (03/0050)

CIRCUIT BOARDS TESTED

Language Processor and Emulator Controller.

FUNCTION

This test verifies the proper functioning of the address lines on the Language Processor board that are under direct control of the Z-80. This test assures that the language processor can correctly address program memory.

DESCRIPTION

1. This test fills the lower program memory locations with a "Load From Memory" instruction and all other locations are filled with "Halt" instructions. Breakpoint 1 (BP1) is loaded with the operand address of the "Load From Memory" instruction. The the addresses are stepped through all address locations (A0--A15 or 0000--FFFF) and a breakpoint 1 interrupt is generated for each address value. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        ERROR CODE = 03/0050

CMD = FC [command byte written to I/O port address F9]
CONTROL = DE [control byte written to I/O port address F8]
ADDRESS LINE FAILURE XXXX
EXPECTED INTERRUPTS = 0200 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-------------------------------------------
  PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD
SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD
-------------------------------------------
```

PROCESSOR DATA BUS TESTS

These tests verify the proper functioning of the data lines on the Language Processor board that are under direct control of the Z-80 CPU. These tests assure that the language processor can correctly transfer data to/from program memory and devices in the 8301 system.

PROCESSOR DATA BUS TEST (WRITE) (03/0061)

Circuit Boards Tested

Language Processor and Emulator Controller.

Function

This test verifies that data can be written into program memory by the Z-80 CPU.

Description

1. This test loads a test program into the lower program memory locations. The remainder of program memory is loaded with ""Halt" instructions. The language processor is "Reset" and it starts executing the test program. The program writes "NOP" and "Halt" instructions into program memory. When the "Halt" instruction just written into memory is

executed, a "Halt" interrupt is generated. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats both test modules. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          ERROR CODE = 03/0061

CMD = FC [command byte written to I/O port address F9]
CONTROL = DF [control byte written to I/O port address F8]
PC LAST WAS XXXX [PC Last value read]
PC LAST S/B XXXX [PC Last value should be]
EXPECTED INTERRUPTS = 0100 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-------------------------------------------
  PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD
SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD
-------------------------------------------
```

PROCESSOR DATA BUS TEST (READ) (03/0062)

Circuit Boards Tested

Language Processor and Emulator Controller.

Function

This test verifies that data can be read from program memory by the Z-80 CPU.

Description

1. This test loads a test program into the lower program memory locations. The remainder of program memory is loaded with "Halt" instructions. The language processor is "Reset" and starts executing the test program. This program reads four different patterns from program memory (the patterns are 00, FF, AA, and 55). A "Halt" interrupt is generated at the end of this program. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping

routine repeats both test modules A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          ERROR CODE = 03/0062

CMD = FC [command byte written to I/O port address F9]
CONTROL = DF [control byte written to I/O port address F8]
FAILED AT ADDRESS = XXXX [indicates failed address]
DATA READ = XX [value of data byte read]
DATA S/B = XX [value of what data byte should be]
-------------------------------------------
  PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD
SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD
-------------------------------------------
```

Z-80 CPU TEST (03/0070)

CIRCUIT BOARD TESTED

Language Processor.

FUNCTION

This test verifies the proper functioning of all non-I/O instructions of the Z-80 CPU.

DESCRIPTION

1. This test loads a program into program memory that checks all non-I/O instructions of the Z-80 CPU. The Z-80 is forced to execute this test program. Successful completion of this program causes a "Halt" interrupt to be generated from memory location 0179. An interrupt from any other location indicates an error condition. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        ERROR CODE = 03/0070

CMD = FC [command byte written to I/O port address F9]
CONTROL = DF [control byte written to I/O port address F8]
PC LAST WAS XXXX [PC Last value read]
PC LAST S/B 0179 [PC Last value should be]
EXPECTED INTERRUPTS = 0100 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
----------------------------------------
PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD
----------------------------------------
```

EMULATOR CONTROLLER TEST

This series of tests verify proper operation of the following functions on the Emulator Controller board:

- SVC1--SVC8
- Single Cycle
- BP1 and BP2 Registers both read and write
- PC Next and PC Last Registers

EMULATOR CONTROLLER TEST (SVC1--SVC8) (03/0081)

Circuit Board Tested

Emulator Controller.

Function

This test verifies the proper operation of SVC1 through SVC8.

Description

1. This test loads a test program containing SVC1--SVC8 into program memory. A "Reset" command is sent to the emulator controller and execution starts at location 0000. When the processor reaches the first SVC and SVC1 interrupt is generated. This interrupt is verified and the language processor is restarted. This procedure is repeated for the remaining SVCs (SVC2--SVC8). If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          ERROR CODE = 03/0081

CMD = FE [command byte written to I/O port address F9]
CONTROL = DF [control byte written to I/O port address F8]
EXPECTED INTERRUPTS = 00XX [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-----------------------------------------
PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD
-----------------------------------------
```

EMULATOR CONTROLLER TEST (SINGLE CYCLE) (03/0082)

Circuit Board Tested

Emulator Controller

Function

This test verifies the proper operation of the single cycle interrupt.

Description

1. This test loads a program containing "NOP" and "Halt" instructions into program memory. A single cycle command is sent to the emulator controller. The language processor is reset and starts execution. After executing the "NOP" instruction at location 0000, a single cycle interrupt is generated. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          ERROR CODE = 03/0082

CMD = FC [command byte written to I/O port address F9]
CONTROL = CF [control byte written to I/O port address F8]
EXPECTED INTERRUPTS = 0800 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-----------------------------------------
PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD
-----------------------------------------
```

EMULATOR CONTROLLER TEST (BP1 READ) (03/0083)

Circuit Board Tested

Emulator Controller.

Function

This test verifies proper operation of Breakpoint 1 Register during a memory read instruction.

Description

1. This test loads a program into program memory that reads from a specified address and all other locations are loaded with a "Halt" instruction. The specified address is also loaded in Breakpoint 1 Register. The language processor is then reset and executes the memory

read program. A Breakpoint 1 interrupt is generated when the Z-80 CPU reads from a memory address that is the same as the Breakpoint 1 Register address. This program is repeated for different address values so that all address bits A0 through A15 are tested. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          ERROR CODE = 03/0083

CMD = FC [command byte written to I/O port address F9]
CONTROL = FC [control byte written to I/O port address F8]
EXPECTED INTERRUPTS = 0200 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-----------------------------------------
PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD
-----------------------------------------
```

EMULATOR CONTROLLER TEST (BP2 READ) (03/0084)

Circuit Board Tested

Emulator Controller

Function

This test verifies the proper operation of Breakpoint 2 Register during a memory read instruction

Description

1. This test is identical to the preceding test except that Breakpoint 2 Register is used.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                        ERROR CODE = 03/0084

CMD = FC [command byte written to I/O port address F9]
CONTROL = DB [control byte written to I/O port address F8]
EXPECTED INTERRUPTS = 0400 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-----------------------------------------
PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD
-----------------------------------------
```

EMULATOR CONTROLLER TEST (BP1 WRITE) (03/0085)

Circuit Board Tested

Emulator Controller Board.

Function

This test verifies the proper operation of Breakpoint 1 register during a memory write operation.

Description

1. This test is similar to the BP1 Read test except that a memory write is executed. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          ERROR CODE = 03/0085

CMD = FB [command byte written to I/O port address F9]
CONTROL = DD [control byte written to I/O port address F8]
EXPECTED INTERRUPTS = 0200 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-----------------------------------------
PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD
-----------------------------------------
```

EMULATOR CONTROLLER TEST (BP2 WRITE) (03/0086)

Circuit Board Tested

Emulator Controller.

Function

This test verifies the proper operation of Breakpoint 2 register during a memory write operation.

Description

1. This test is similar to the BP2 Read test except that a memory write instruction is executed. If an error is detected, an error code with supporting data are displayed on the system terminal. This test branches to a looping routine if a failure is detected. The looping routine repeats the entire test module. A SYNC pulse is generated each time the test is repeated.

2. The additional information displayed with the error code is as follows"

```
>>>>>>>>>>>>>>>>   DIAGNOSTIC FAILURE   <<<<<<<<<<<<<<<<

                                          ERROR CODE = 03/0086

CMD = FB [command byte written to I/O port address F9]
CONTROL = D7 [control byte written to I/O port address F8]
EXPECTED INTERRUPTS = 0400 [correct value]
ACTUAL INTERRUPTS = XXXX [value of actual interrupts]
-----------------------------------------
PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD
-----------------------------------------
```

CONSOLIDATED ERROR CODE LISTING

A numerical listing of all error codes and supporting data for the basic 8301 unit are consolidated in Tables 4-19 through 4-22. These tables contain the error codes, supporting data, and suspected boards/devices that relate to the detected failure. Table 4-18 is an index showing the relationship of the error code, error code listing, and where the consolidated error code listing is located. The error code is divided into two parts: xx/yyyy. The "xx" indicates the test program number. The ""yyyy" indicates a specific failure within the test program.

Table 4-18
Error Code Listing Index

Error Code Numbers	Consolidated Error Code Listing	Where Listing is Located
00/yyyy	8301/8501 Communication Errors	Table 4-19
01/yyyy	System Processor and I/O Errors	Table 4-20
02/yyyy	Memory and Memory Function Errors	Table 4-21
03/yyyy	Language Processor Errors	Table 4-22
04/yyyy	RTPA Errors	See Note
05/yyyy	PROM Programmer Errors	See Note
06/yyyy	8085 Emulator Errors	See Note
07/yyyy	Z80 Emulator Errors	See Note
08/yyyy	6800 Emulator Errors	See Note
09/yyyy	8048 Emulator Errors	See Note
0A/yyyy	8080 Emulator Errors	See Note
0B/yyyy	9900 Emulator Errors	See Note
0C/yyyy	1802 Emulator Errors	See Note
0D/yyyy	3870/F8 Emulator Errors	See Note
0E/yyyy	6500/1 Emulator Errors	See Note
0F/yyyy	6801 Emulator Errors	See Note
10/yyyy	6809 Emulator Errors	See Note
11/yyyy	Trigger Trace Errors	See Note
12/yyyy	8086 Emulator Errors	See Note
13/yyyy	Z8000 Emulator Errors	See Note
14/yyyy	M68000 Emulator Errors	See Note

NOTE

Error code numbers 00/yyyy--03/yyyy are for the basic 8301 unit and are contained in Tables 4-19 through 4-22. Error code numbers 04/yyyy and higher are for optional equipment associated with the 8550 system. These error codes are defined in the associated Service Manuals for each option.

8301/8501 COMMUNICATION ERRORS

8301/8501 Communication Errors are displayed when the 8301 Diagnostic Executive Program cannot load from the 8550 System Diagnostics disc. These error codes are displayed on the system terminal. There are eleven error codes that can be displayed. These error codes further define the reason why the Executive Program on the disc cannot be loaded into the 8301 System Memory. Table 4-19 lists these error codes and a brief definition of each code.

Table 4-19
8301/8501 Communication Errors

Error Code	Displayed Message and Definition
00/0001	Unable to CLOSE ALL 8501 files RUN 8501 STANDALONE DIAGNOSTICS --- (Error occurred after trying to send a CLOSE ALL command.)
00/0002	HSI communication terminated after 16 retries or NAK's RUN 8501 STANDALONE DIAGNOSTICS --- (Program aborted after 16 retries - return to EXEC.)
00/0003	HSI Protocol Error <xx> RUN 8501 STANDALONE DIAGNOSTICS --- (There was a HSI protocol error during the running of 8501 Diagnostics. Refer to the 8501 Service Manual for meaning of <xx> error code.)
00/0004	Unable to find 8501 Diagnostics RUN 8501 STANDALONE DIAGNOSTICS --- (Could not find DIAGS.SAV file.)
00/0005	8501 Diags loaded but did not respond correctly. RESPONSE = xx RUN 8501 STANDALONE DIAGNOSTICS --- (8501 Diagnostics were loaded but did not send correct code to indicate that they are running [correct response code = 34].)

Table 4-19 (Cont)

Error Code	Displayed Message and Definition
00/0006	HSI communication terminated after 16 retries or NAK's RUN 8501 STANDALONE DIAGNOSTICS --- (16 NAK's occurred and program was aborted.)
00/0007	HSI Protocol Error <xx> RUN 8501 STANDALONE DIAGNOSTICS --- (There was a protocol error while trying to load a file. Refer to 8501 Service Manual for meaning of error code <xx>.)
00/0008	Unknown message from 8501 Code - xx yy RUN 8501 STANDALONE DIAGNOSTICS --- (While running the 8501 diagnostics an unknown message was received. Valid codes are: xx | yy 05 | 00 51 | 32 51 | 33 51 | 35 51 | 36)
00/0009	Loadfile Checksum Error RUN 8501 STANDALONE DIAGNOSTICS --- (There was a checksum error during one of the block transfers.)
00/000A	Unable to find file. RUN 8501 STANDALONE DIAGNOSTICS --- (Tried to load a file but could not find it on the disc.)
00/000B	Timeout Occurred RUN 8501 STANDALONE DIAGNOSTICS --- (No action on the interface for about 6 seconds.)

SYSTEM PROCESSOR AND I/O ERRORS

The System Processor and I/O Tests verify the correct operation of the 2650A-1 microprocessor (system processor), the three ACIA ports (RS-232-C compatible), and other miscellaneous circuitry on the System Controller board. This test program is divided into 12 test modules. Each test module contains one or more error codes. Table 4-20 lists the error codes and defines the supporting data accompanying each error code. In addition to showing the suspected board(s), Table 4-20 also lists the suspected device(s). The devices with the highest probability of failure are listed first.

Table 4-20
System Processor and I/O Errors

Error Code	Displayed Message and Definition
	INSTRUCTION SET TEST ERRORS
01/0001	LOD Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 1. SYNC pulse is at start of module 1. Suspected Device -- U2050 - 2650A-1 CPU
01/0002	STR Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 1. SYNC pulse is at start of module 1. Suspected Device -- U2050 - 2650A-1 CPU
01/0003	ADD Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 2. SYNC pulse is at start of module 2. Suspected Device -- U2050 - 2650A-1 CPU
01/0004	SUB Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 2. SYNC pulse is at start of module 2. Suspected Device -- U2050 - 2650A-1 CPU

Table 4-20 (Cont)

Error Code	Displayed Message and Definition
01/0005	DAR Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 2. SYNC pulse is at start of module 2. Suspected Device -- U2050 - 2650A-1 CPU
01/0006	AND Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 3. SYNC pulse is at start of module 3. Suspected Device -- U2050 - 2650A-1 CPU
01/0007	IOR Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 3. SYNC pulse is at start of module 3. Suspected Device -- U2050 - 2650A-1 CPU
01/0008	EOR Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 3. SYNC pulse is at start of module 3. Suspected Device -- U2050 - 2650A-1 CPU
01/0009	RRL Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 4. SYNC pulse is at start of module 4. Suspected Device -- U2050 - 2650A-1 CPU
01/000A	RRR Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 4. SYNC pulse is at start of module 4. Suspected Device -- U2050 - 2650A-1 CPU

Table 4-20 (Cont)

Error Code	Displayed Message and Definition
01/000B	COM Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 5. SYNC pulse is at start of module 5. Suspected Device -- U2050 - 2650A-1 CPU
01/000C	Branch Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire branch group of test module 6. SYNC pulse is at start of branch group of module 6. Suspected Device -- U2050 - 2650A-1 CPU
01/000D	Branch To Subroutine Instruction Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire subroutine group of test module 6. SYNC pulse is at start of subroutine group of module 6. Suspected Device -- U2050 - 2650A-1 CPU
01/000E	Return From Subroutine Instruction (RETC) Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire subroutine group of test module 6. SYNC pulse is at start of subroutine group of module 6. Suspected Device -- U2050 - 2650A-1 CPU
01/000F	Stack Pointer (SP0, SP1,SP2, IN PSW) Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire subroutine group of test module 6. SYNC pulse is at start of subroutine group of module 6. Suspected Device -- U2050 - 2650A-1 CPU

Table 4-20 (Cont)

Error Code	Displayed Message and Definition
01/0010	Program Status Word and Miscellaneous Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 7. SYNC pulse is at start of test module 7. Suspected Device -- U2050 - 2650A-1 CPU CHECKSUM TEST ERRORS
01/0011	Diagnostic ROM Checksum Error ACTUAL CHECKSUM = [calculated checksum] CORRECT CHECKSUM = [correct value stored in DIAG ROM] PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on Diagnostic ROM section of test module 8. SYNC pulse is at start of DIAG ROM section of test module 8. Suspected Devices -- U5030 - 32K DIAG ROM U6020 - Support logic U2010 - Support logic U2020 - Support logic U1020 - Support logic
01/0012	Boot ROM Checksum Error ACTUAL CHECKSUM = [calculated checksum] CORRECT CHECKSUM = [correct value stored in Boot ROM] PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on Boot ROM section of test module 8. SYNC pulse is at start of Boot ROM section of module 8. Suspected Devices -- U5040 - 16K Boot ROM U6020 - Support logic

Table 4-20 (Cont)

Error Code	Displayed Message and Definition
	INTERNAL TIMER TEST ERRORS
01/0013	Processor Speed Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on processor speed section of test module 9. SYNC pulse is at start of processor speed section of test module 9. Suspected Devices -- U6700 - Divide network (1.25 MHz) U5700 - Divide network (2 MHz) U5600 - Divide network U2050 - 2650A-1 CPU (pin 1) 20 MHz Oscillator
01/0014	Interrupted Interval Timer Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on interrupted section of test module 9. SYNC pulse is at start of interrupted section of module 9. Suspected Devices -- U6100 - Latch U5400 - Latch U3400 - Latch U5100 - Encoder U3030 - Decoder U1060 - Buffer U2050 - 2650A-1 CPU (pin 17)
01/0015	Non-Interrupted Interval Timer Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on non-interrupted section of test module 9. SYNC pulse is at start of non-interrupted section of test module 9. Suspected Devices -- U5100 - Encoder U5200 - Support logic U6100 - Latch Latch of failing interrupt vector

Table 4-20 (Cont)

Error Code	Displayed Message and Definition
	LED AND DIP SWITCH TEST ERRORS
01/0016	LED Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 10. SYNC pulse is at start of module 10. Suspected Devices -- U1070 - Latch U2100 - Buffer U3030 - Decoder LEDs
01/0017	DIP Switch Error ACTUAL RESPONSE = [value read at DIP switch] CORRECT RESPONSE = [101010 or 010101] PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on entire test module 11. SYNC pulse is at start of module 11. Suspected Devices -- U3030 - Decoder S1100 - DIP switch pack U1100 - Buffer
	I/O TEST ERRORS
01/0018	Wrap-Back Error --- ACIA Remote Communication Port ACTUAL RESPONSE = [value read at ACIA port] CORRECT RESPONSE = [0101 0101 or 1010 1010] PRIMARY SUSPECT = COMM INTERFACE BOARD SECONDARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on wrap-back test of test module 12. SYNC pulse is at start of wrap-back test of test module 12.

Table 4-20 (Cont)

Error Code	Displayed Message and Definition
01/0018 (cont.)	Suspected Devices -- Communications Interface Board U3081 - Divide network U3080 - Buffer U1010 - Differential line receiver U3010 - Differential line driver U3030 - Decoder U3020 - Multiplexer S1060 - Baud rate switch Suspected Devices -- System Controller Board U2600 - ACIA U4700 - Latch U1400 - Buffer U1500 - Buffer U3500 - Buffer U4700 - Latch 2.4 MHz Oscillator
01/0019	Wrap-Back Error --- ACIA System Terminal Port ACTUAL RESPONSE = [value read at ACIA port] CORRECT RESPONSE = [0101 0101 or 1010 1010] PRIMARY SUSPECT = COMM INTERFACE BOARD SECONDARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on wrap-back test of test module 12. SYNC pulse is at start of wrap-back test of test module 12. Suspected Devices -- Communications Interface Board S1090 - Baud rate switch Suspected Devices -- System Controller Board U2700 - ACIA U3500 - Buffer U1200 - Buffer U1500 - Buffer

Table 4-20 (Cont)

Error Code	Displayed Message and Definition
01/001A	Wrap-Back Error --- ACIA Auxiliary Port ACTUAL RESPONSE = [value read at ACIA port] CORRECT RESPONSE = [0101 0101 or 1010 1010] PRIMARY SUSPECT = COMM INTERFACE BOARD SECONDARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on wrap-back test of test module 12. SYNC pulse is at start of wrap-back test of test module 12. Suspected Devices -- Communications Interface Board S1080 - Baud rate switch Suspected Devices -- System Controller Board U2500 - ACIA U1400 - Buffer U1500 - Buffer U3600 - Buffer
01/001B	Baud Rate Error --- ACIA Remote Communication Port PRIMARY SUSPECT = COMM INTERFACE BOARD SECONDARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on wrap-back test of test module 12. SYNC pulse is at start of wrap-back test of test module 12.
01/001C	Baud Rate Error --- ACIA System Terminal Port PRIMARY SUSPECT = COMM INTERFACE BOARD SECONDARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on wrap-back test of test module 12. SYNC pulse is at start of wrap-back test of test module 12.
01/001D	Baud Rate Error --- ACIA Auxiliary Port PRIMARY SUSPECT = COMM INTERFACE BOARD SECONDARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on wrap-back test of test module 12. SYNC pulse is at start of wrap-back test of test module 12.

MEMORY AND MEMORY FUNCTION ERRORS

The Memory and Memory Function Tests verify the correct operation of the System Memory board, the Program Memory board, and miscellaneous circuitry on the System Controller board. This test program is divided into 13 test modules. Each test module contains one or more error codes. Table 4-21 lists the error codes and defines the supporting data accompanying each error code. In addition to showing the suspected board(s), Table 4-21 also lists the suspected device(s). The devices with the highest probability of failure are listed first.

NOTE

The error code displayed when a parity error occurs refers to the test module being run at that time. Refer to Table 4-10 for a list of test module numbers. The error code does not relate to the error codes in Table 4-21. In general, one of the error codes in Table 4-21 will be displayed following a parity error.

Table 4-21
Memory and Memory Function Error Codes

Error Code	Displayed Message and Definition
	MEMORY BOARD RAM TEST ERRORS
02/0001	Memory Configurer Error PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD SECONDARY SUSPECT = MEMORY BOARD Looping -- Test loops on entire test module. SYNC pulse generated each time test is rerun. Suspected Devices -- System Controller Board U2040 - Buffer U3040 - Multiplexer U3020 - Support logic U3060 - Support logic Suspected Devices -- 32K Memory Board U6000 - data bus enable U6100 - decode ROM control logic U7120 - Board enable logic U4000 - Board enable logic U7010 - Board enable logic U6080 - Board enable logic U6090 - Board enable logic NOTE Two 32K Memory boards with jumpers positioned the same will cause this test to fail.

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
02/0002	Bank Select Error ACTUAL DATA =[data read on the 256th read] CORRECT DATA = [correct data byte] ADDRESS = [starting address of failed 16K block] BANK TESTED = [16K bank under test] PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD SECONDARY SUSPECT = MEMORY BOARD Looping -- Test loops on reading the first 256 locations in the failing bank. SYNC pulse generated each time test is rerun. Suspected Devices -- System Controller Board U2040 - Buffer U3040 - Multiplexer Suspected Devices -- 32K Memory Board U6170 - "CS" select U6110 - Support logic U6120 - Support logic Suspected Devices -- 64K System RAM Board U2040 - Dynamic RAM Controller U4010 - Page logic switch U4020 - Page logic demultiplexer U3010 - Page support logic U3020 - Page support logic U5030 - Address Buffer (A13--A15) U2030 - Latch (SEL)

Bank	Memory Board	Order Tested
00	Program Memory (0K--16K)	4
01	Program Memory (16K--32K)	5
02	Program Memory (32K--48K)	6
03	Program Memory (48K--64K)	7
00	Program Memory (64K--80K)	8
01	Program Memory (80K--96K)	9
02	Program Memory (96K--112K)	10
03	Program Memory (112K--128K)	11
04	System Memory (0K--16K)	(not tested)
05	System Memory (16K--32K)	1
06	System Memory (32K--48K)	2
07	System Memory (48K--64K)	3

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
02/0003	Row Select Error ACTUAL DATA =[data read on the 256th read] CORRECT DATA = [correct data byte] ADDRESS = [starting address of failed 4K block] BANK TESTED = [16K bank under test] PRIMARY SUSPECT = MEMORY BOARD Looping -- Test loops on reading the first 256 locations in the failing block starting at the failed address above. SYNC pulse generated each time test is rerun. Suspected Devices -- 32K Memory Board U6170 - "CS" select U6100 - Decode ROM control logic Address Buffers U6010 - A0--A3 (0000--000F) U6020 - A4--A7 (0010--00FF) U6030 - A8--A11 (0100--0FFF) U6040 - A12--A15 (1000--3FFF) Data Buffers U6130 - D0--D3 odd addresses U6140 - D4--D7 odd addresses U6050 - D0--D3 even addresses U6060 - D4--D7 even addresses Suspected Devices -- 64K System RAM Board U5030 - Address Buffer (A12) U2040 - Dynamic RAM Controller Uxxxx - Page logic (See error code 02/0002.)
02/0004	Chip Select Error ACTUAL DATA =[incorrect data byte] CORRECT DATA = [correct data byte] ADDRESS = [indicates failing address] BANK TESTED = [16K bank under test] PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD SECONDARY SUSPECT = MEMORY BOARD Looping -- Test loops on writing the 4K block then reading up to and including the failing location. That location is then read 256 times. SYNC pulse is generated each time the test is rerun.

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
02/0004 (cont.)	Suspected Devices -- 32K Memory Board (For 670-6542-XX only)

	Even Address		Odd Address		Even Address		Odd Address	
	Bank No. 00				Bank No. 01			
	0000-1FFE	2000-3FFE	0001-1FFF	2001-3FFF	4000-5FFE	6000-7FFE	4001-5FFF	6001-7FFF
	Bank No. 02				Bank No. 03			
Bad Bit	8000-9FFE	A000-BFFE	8001-9FFF	A001-BFFF	C000-DFFE	E000-FFFE	C001-DFFF	E001-FFFF
0	U4010	U3010	U4090	U3090	U2010	U1010	U2090	U1090
1	U4020	U3020	U4100	U3100	U2020	U1020	U2100	U1100
2	U4030	U3030	U4110	U3110	U2030	U1030	U2110	U1110
3	U4040	U3040	U4120	U3120	U2040	U1040	U2120	U1120
4	U4050	U3050	U4130	U3130	U2050	U1050	U2130	U1130
5	U4060	U3060	U4140	U3140	U2060	U1060	U2140	U1140
6	U4070	U3070	U4150	U3150	U2070	U1070	U2150	U1150
7	U4080	U3080	U4160	U3160	U2080	U1080	U2160	U1160

Write and read buffers -- even address
U6050 - bits 0--3 U6060 - bits 4--7
Write and read buffers -- odd address
U6130 - bits 0--3 U6140 - bits 4--7

Suspected Devices -- 64K System RAM Board

Bad Bit	Bank 04 0000-3FFF	Bank 05 4000-7FFF	Bank 06 8000-BFFF	Bank 07 C000-FFFF
0	U1060	U2060	U3060	U4060
1	U1070	U2070	U3070	U4070
2	U1080	U2080	U3080	U4080
3	U1090	U2090	U3090	U4090
4	U1100	U2100	U3100	U4100
5	U1110	U2110	U3110	U4110
6	U1120	U2120	U3120	U4120
7	U1130	U2130	U3130	U4130
Parity	U1140	U2140	U3140	U4140

U2040 - Dynamic RAM Controller U5060 - Output Data Buffer
U5050 - Input Data Buffer U5100 - Data Latch

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
02/0005	Addressing Error ACTUAL DATA =[incorrect data byte] CORRECT DATA = [correct data byte] ADDRESS = [indicates failing address] BANK TESTED = [16K bank under test] PRIMARY SUSPECT = MEMORY BOARD Looping -- Test loops by filling the 16K block with background data and then reading (using the Marching algorithm) up to the failing location. That location is then read 256 times. SYNC pulse is generated each time the test is rerun. Suspected Devices -- 32K Memory Board Addressing Logic U6010 - A0--A3 (0000--000F) U6020 - A4--A7 (0010--00FF) U6030 - A8--A11 (0100--0FFF) U6040 - A12--A15 (100--3FFF) NOTE Multi-bit errors in the incorrect data byte indicate address problem. Single bit errors normally indicate individual RAM chip problem. Suspected Devices -- 64K System RAM Board U2040 - Dynamic RAM Controller U5030 - Address Buffer (A8--A15) U5020 - Address Buffer (A0--A7) Uxxxx - Page Switch Logic (See error code 02/0002.)
02/0006	Refresh Error ACTUAL DATA =[incorrect data byte] CORRECT DATA = [correct data byte] ADDRESS = [indicates failing address (relative)] BANK TESTED = [16K bank under test] PRIMARY SUSPECT = MEMORY BOARD Looping -- Test loops on reading the 16K block from the beginning up to the failing location. That location is then read 256 times. SYNC pulse is generated each time the test is rerun.

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
02/0006 (cont.)	NOTE Failure is caused by RAM chip indicated by failing bit and address (see 02/0004). Suspected Devices -- 64K System RAM Board U2040 - Dynamic RAM Controller U4040 - Refresh Generator (REFN)
02/0009	GALTCOL Error ACTUAL DATA = [incorrect data byte] CORRECT DATA = [correct data byte] ADDRESS = [indicates failing address] BANK TESTED = [16K bank under test] PRIMARY SUSPECT = MEMORY BOARD Looping -- Test loops the running of the GALTCOL pattern on the failing 4K block. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Failure is caused by RAM chip indicated by failing bit and address (see 02/0004).
	DMA TEST ERRORS
02/000A	DMA Static Test Error ACTUAL DATA = [incorrect data (2 bytes)] CORRECT DATA = [correct data (2 bytes)] DMA REGISTER = [register under test] Register Under Test 90 = Channel 0 --- Address Register 91 = Channel 0 --- TC Register 92 = Channel 1 --- Address Register 93 = Channel 1 --- TC Register 94 = Channel 2 --- Address Register 95 = Channel 2 --- TC Register PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on writing to and reading back from the failing register. SYNC pulse is generated each time the test is rerun.

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
02/000A (cont.)	Suspected Devices -- System Controller Board U2080 - DMA device U2030 - Buffer U2090 - Support logic U4090 - Support logic
	DMA Functional Test Errors
02/000B	DMA Error (System--System failure)
02/000C	DMA Error (System--Program failure)
02/000D	DMA Error (Program--Program failure)
02/000E	DMA Error (Program--System failure)
	ACTUAL DATA = [incorrect data byte] CORRECT DATA = [correct data byte] ADDRESS = [indicates failed address] Failed Address --- 02/000B - System Memory (7000--7FFF) 02/000C - Program Memory (0000--3FFF) 02/000D - Program Memory (4000--7FFF) 02/000E - System Memory (4000--7FFF) PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on failing DMA test. SYNC pulse is generated each time the test is rerun. Suspected Devices -- For Error Code 02/000B U2080 - DMA device U2300 - Octal F/F U2400 - Multiplexer U2070 - Octal F/F U1090 - Bus driver U3090 - Support logic U3400 - Support logic U4300 - Support logic U3100 - Support logic U4100 - Support logic U5400 - Support logic Suspected Devices -- For Error Codes 02/000C, 02/000D, and 02/000E U2080 - DMA device U2070 - Octal F/F

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
	WRITE PROTECT AND MEMORY MAP STATIC TEST ERRORS
02/0010	Data Bit Error
02/0011	Address Error ACTUAL DATA = [incorrect data byte] CORRECT DATA = [correct data byte] ADDRESS = [indicates failing address (FE00--FFFF)] PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- Test loops on either a Data or Address error. SYNC pulse is generated each time the test is rerun. Suspected Devices -- System Controller Board Bad Bit / FE00--FEFF / FF00--FFFF D0: U6010 - RAM device / U5010 - RAM device D2: U6030 - RAM device / U6022 - RAM device Address Buffers U6050 - A8--A15 U6040 - A0--A7 U4010 - Address Buffer Data Buffers U1060 - Write Buffer U1030 - Read Buffer
	MEMORY RELOCATION RAM STATIC TEST ERRORS
02/0014	Data Bit Error
02/0015	Address Error
02/0016	Reset Error ACTUAL DATA = [incorrect data byte] CORRECT DATA = [correct data byte] ADDRESS = [indicates failing address, 00--0F] BANK TESTED = [16K bank under test] PRIMARY SUSPECT = MEMORY BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is repeated.

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
02/0014 02/0015 02/0016 (cont.)	Suspected Devices -- 32K Memory Board Error Code - 0014 / Error Code - 0015 U7050 - Buffer / U7020 - Address Counter U7040 - RAM / U7030 - Multiplexer U7040 - RAM Error Code - 0016 U7060 - Support logic U7070 - Support logic MEMORY RELOCATION FUNCTIONAL TEST ERRORS
02/0017	Physical Address = 0000--0FFF
02/0018	Physical Address = 1000--1FFF
02/0019	Physical Address = 2000--2FFF
02/001A	Physical Address = 3000--3FFF
02/001B	Physical Address = 4000--4FFF
02/001C	Physical Address = 5000--5FFF
02/001D	Physical Address = 6000--6FFF
02/001E	Physical Address = 7000--7FFF ACTUAL DATA = [incorrect data byte] CORRECT DATA = [correct data byte] ADDRESS = [indicates failing bus address] BANK TESTED = [16K bank under test] PRIMARY SUSPECT = MEMORY BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is repeated. Suspected Devices -- 32K Memory Board U7010 - Address Buffer U7030 - Address Buffer U7080 - Flip/Flop U7090 - Support logic U7070 - Support logic U7100 - Support logic U7140 - Support logic U7110 - Support logic

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
02/001F	ILLEGAL INTERRUPT # <xx> <xx> = [interrupt that occurred - see list of interrupts below] PRIMARY SUSPECT = SYSTEM CONTROLLER BOARD Looping -- No looping occurs and test continues. No SYNC pulse is generated. Suspected Devices -- System Controller Board U6400 - INT Flip/Flop U6090 - Interrupt logic U5090 - Interrupt logic U2100 - Interrupt logic U5100 - Interrupt logic U4080 - Support logic U1020 - Support logic Interrupt Numbers 01 - System Memory error 02 - Write Protect violation 03 - Program Parity error 04 - HSI Interface input 05 - HSI Interface output 06 - Remote Port ACIA 07 - Auxilary Port ACIA 10 - System Port ACIA 11 - Interval Timer 12 - DMA 13 - Manufacturing Test 14 - Unassigned 15 - PROM Programmer 16 - Unassigned 17 - Unassigned 20 - SVC 1 21 - SVC 2 22 - SVC 3 23 - SVC 4 24 - SVC 5 25 - SVC 6 26 - Debug SVC 1 27 - Debug SVC 2 30 - Breakpoint 1 31 - Breakpoint 2 32 - Single Cycle 33 - Emulator Halted 34 - Diagnostic 35 - TTA/RTPA (INT 29) 36 - RTPA (INT 30) 37 - RTPA (INT 31)

Table 4-21 (Cont)

Error Code	Displayed Message and Definition
02/003A	Parity Always Enabled
02/003B	Parity Generator or Checker Problem
02/003C	Parity Always Disabled
02/003D	Parity Address Incorrect

PRIMARY SUSPECT = SYSTEM RAM BOARD

Looping -- Test loops on entire test module.

Suspected Devices -- 64K System RAM Board

Error Code - 003A	Error Code - 003B
U5140 - Parity Latch	U5040 - Parity Generator
U4050 - I/O Port D2 Latch	U5090 - Parity Checker
U3150 - Parity support logic	U1040 - Parity support logic
U3180 - Parity support logic	U4050 - I/O Port D2 Latch

Error Code - 003C	Error Code - 003D
U5140 - Parity Latch	U5070 - Parity Address Latch (upper address byte)
U3180 - Parity Error Buffer	
U3020 - Parity Latch Clock	U5080 - Parity Address Latch (lower address byte)
U3150 - Parity Latch Enable	
U4050 - I/O Port D2 Latch	U5100 - Data Latch
	U3160 - I/O Latch Demultiplexer

LANGUAGE PROCESSOR ERRORS

The Language Processor Tests verify the correct operation of the Language Processor board and the majority of the Emulator Controller board. This test program is divided into 14 test modules. Each test module contains one or more error codes. Table 4-22 lists the error codes and defines the supporting data accompanying each error code. In addition to showing the suspected board(s), Table 4-22 also lists the suspected device(s). The devices with the highest probability of failure are listed first.

Table 4-22
Language Processor and Emulator Controller Errors

Error Code	Displayed Message and Definition
03/0010	PROCESSOR INACTIVE TEST ERROR CMD = FC [command byte of I/O port address F9] CONTROL = FF [control byte of I/O port address F8] EXPECTED INTERRUPTS = 0100 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U4020 U2090 U3020 U4070
03/0020	PROCESSOR RESET AND SVC1 TEST ERROR CMD = FC [command byte of I/O port address F9] CONTROL = DF [control byte of I/O port address F8] PC LAST WAS XXXX [PC Last value read] PC LAST S/B 0002 [PC Last value should be] EXPECTED INTERRUPTS = 0100 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U4020 U4030 U3030 U4040 U2090 U4060 U3080 U4070 U1080 U4080 Suspected Devices -- Emulator Controller Board U3070 U5070 U5040 U2130 U5050

Table 4-22 (Cont)

Error Code	Displayed Message and Definition
03/0030	PROCESSOR HALT TEST ERROR CMD = FC [command byte of I/O port address F9] CONTROL = DF [control byte of I/O port address F8] PC LAST WAS XXXX [PC Last value read] PC LAST S/B 0000 [PC Last value should be] EXPECTED INTERRUPTS = 0100 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U4080 Suspected Devices -- Emulator Controller Board U5100 U1170 U4140 U2130 U3190 U1130
03/0040	PROCESSOR CLOCK TEST ERROR CMD = FC [command byte of I/O port address F9] CONTROL = DF [control byte of I/O port address F8] PC LAST WAS XXXX [PC Last value read] PC LAST S/B 0037 [PC Last value should be] EXPECTED INTERRUPTS = 0100 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U3030 U2060 U2030

Table 4-22 (Cont)

Error Code	Displayed Message and Definition
03/0050	PROCESSOR ADDRESS BUS TEST ERROR CMD = FC [command byte of I/O port address F9] CONTROL = DE [control byte of I/O port address F8] ADDRESS LINE FAILURE XXXX EXPECTED INTERRUPTS = 0200 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U4030 U4050 U4040 U4080 Suspected Devices -- Emulator Controller Board U1180 U2030 U3010 U3060 U3030 U4060 U2010 U4080 PROCESSOR DATA BUS TEST ERRORS
03/0061	Processor Data Bus Test (Write) Error CMD = FC [command byte of I/O port address F9] CONTROL = DF [control byte of I/O port address F8] PC LAST WAS XXXX [PC Last value read] PC LAST S/B XXXX [PC Last value should be] EXPECTED INTERRUPTS = 0100 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U4060 U4070 Suspected Devices -- Emulator Controller Board U1040 U2070 U1050 U1010 U1020 U2050 U1030

Table 4-22 (Cont)

Error Code	Displayed Message and Definition
03/0062	Processor Data Bus Test (Read) Error CMD = FC [command byte of I/O port address F9] CONTROL = DF [control byte of I/O port address F8] FAILED AT ADDRESS = XXXX [indicates failed address] DATA READ = XX [value of data byte read] DATA S/B = XX [value of what data byte should be] PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD SECONDARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U4060 U4070 Suspected Devices -- Emulator Controller Board U1040 U2070 U1050 U1010 U1020 U2050 U1030
03/0070	Z-80 CPU TEST ERROR CMD = FC [command byte of I/O port address F9] CONTROL = DF [control byte of I/O port address F8] PC LAST WAS XXXX [PC Last value read] PC LAST S/B 0179 [PC Last value should be] EXPECTED INTERRUPTS = 0100 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = LANGUAGE PROCESSOR BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U2040

Table 4-22 (Cont)

Error Code	Displayed Message and Definition
	EMULATOR CONTROLLER TEST ERRORS
03/0081	Emulator Controller Test (SVC1--SVC8) Error CMD = FE [command byte of I/O port address F9] CONTROL = DF [control byte of I/O port address F8] EXPECTED INTERRUPTS = 00XX [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U5170 U3150 U5120 U4120 U2130 U4070
03/0082	Emulator Controller Test (Single Cycle) Error CMD = FC [command byte of I/O port address F9] CONTROL = CF [control byte of I/O port address F8] EXPECTED INTERRUPTS = 0800 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U3150 U1170
03/0083	Emulator Controller Test (BP1 Read) Error CMD = FC [command byte of I/O port address F9] CONTROL = FC [control byte of I/O port address F8] EXPECTED INTERRUPTS = 0200 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U3070 U4080 U3010 U2010 U3030 U2030

Table 4-22 (Cont)

Error Code	Displayed Message and Definition
03/0084	Emulator Controller Test (BP2 Read) Error CMD = FC [command byte of I/O port address F9] CONTROL = DB [control byte of I/O port address F8] EXPECTED INTERRUPTS = 0400 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun. Suspected Devices -- Language Processor Board U3070 U2020 U3020 U2030 U3040
03/0085	Emulator Controller Test (BP1 Write) Error CMD = FB [command byte of I/O port address F9] CONTROL = DD [control byte of I/O port address F8] EXPECTED INTERRUPTS = 0200 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun.
03/0086	Emulator Controller Test (BP2 Write) Error CMD = FB [command byte of I/O port address F9] CONTROL = D7 [control byte of I/O port address F8] EXPECTED INTERRUPTS = 0400 [correct value] ACTUAL INTERRUPTS = XXXX [value of actual interrupts] PRIMARY SUSPECT = EMULATOR CONTROLLER BOARD Looping -- Test loops on entire test module. SYNC pulse is generated each time the test is rerun.

Section 5

FUNCTIONAL PROCEDURES

INTRODUCTION

The functional procedures described in this section utilize modified flow type diagrams. These diagrams show various actions that the software/firmware performs on hardware-related functions, and how the software/firmware exercises the various devices. These diagrams do not show the actions caused by each individual instruction executed, but describe the overall effect of a combination of instructions. Figure 5-1 is an example of the diagram format. The actions or conditions are contained in brackets and are normally located near the center of the figure. The hardware devices or controlling devices either doing the action or being acted upon are shown on either side of the brackets. A hardware device may be one of the following:

- complete unit (System Terminal)
- circuit board (System Memory)
- controlling device (system processor or DMA device)
- part of a device (DMA channel 2)

Directional arrows are shown between devices and action to show the direction of action flow.

The functional procedures contained in this section are a small representation of the overall functions performed within the 8301. These procedures are provided to give you a better understanding of the interrelated actions that take place during specific operations. Table 5-1 lists the procedures that are described in this section.

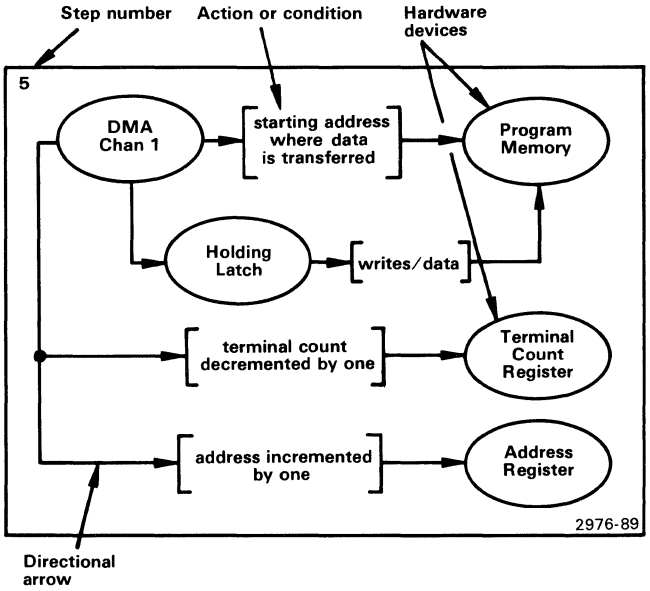


Fig. 5-1. Sample of modified flow diagram.

Table 5-1
Index of Functional Procedures

FUNCTIONAL PROCEDURE NO. 1

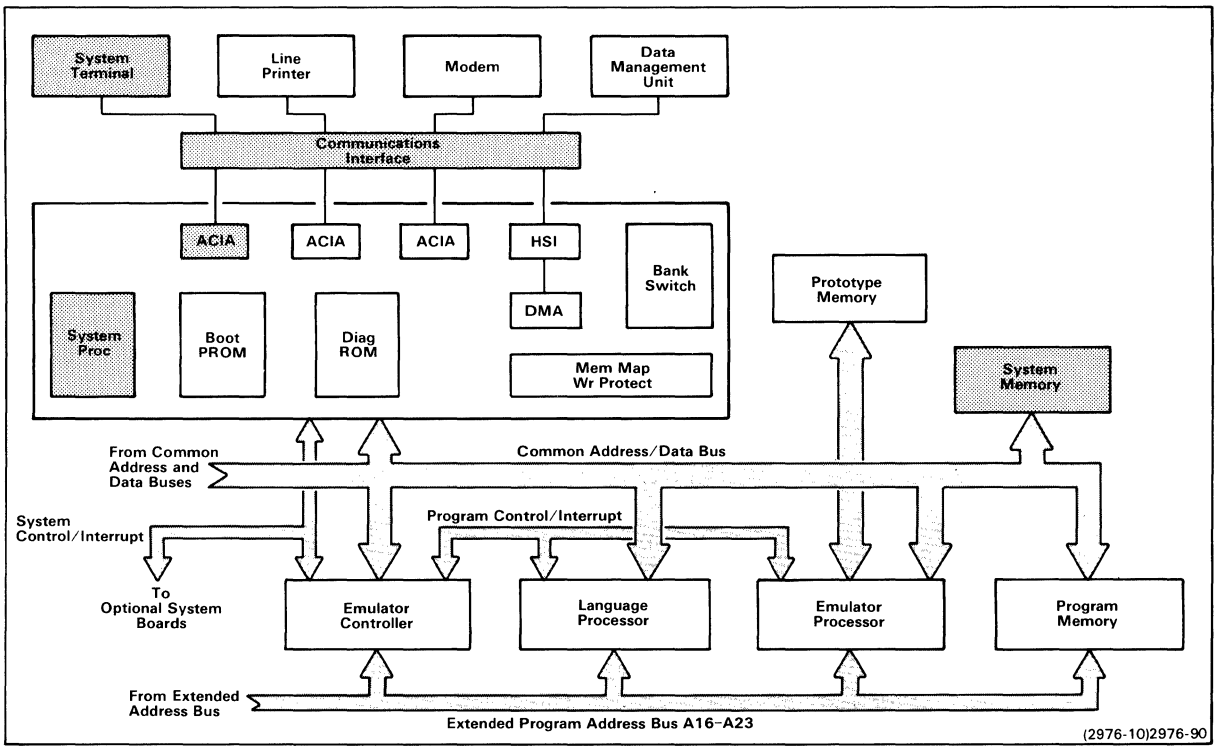


Fig. 5-2. 8301 MDU block diagram.

PROCEDURE

Entering Commands from the System Terminal.

FUNCTION

This procedure describes the sequence of actions that occur when any system command is entered from the System Terminal, until the command is executed.

BLOCKS INVOLVED

System Terminal, Communications Interface, System Controller, and System Memory. (See Fig. 5-2.)

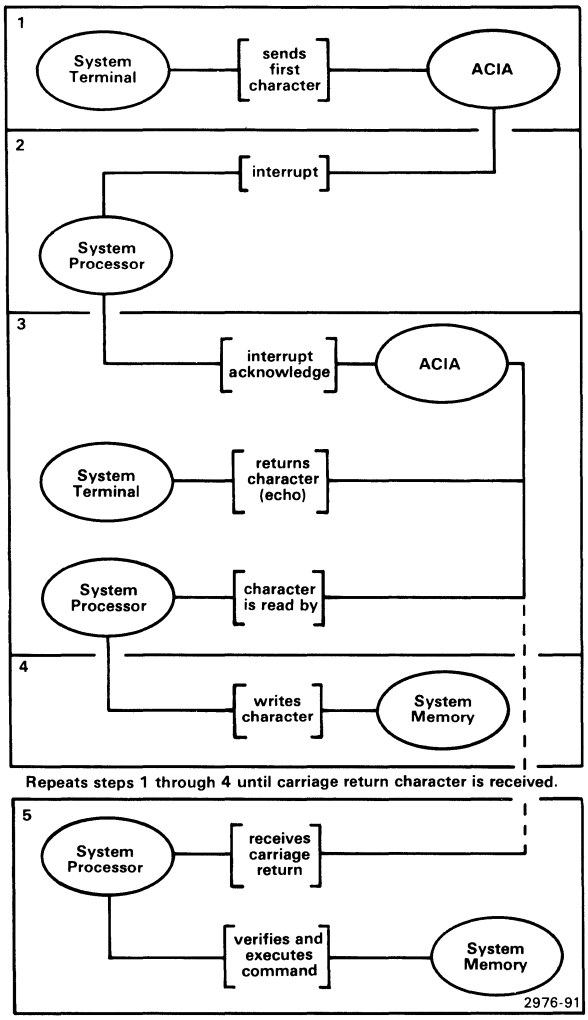


Fig. 5-3. Entering commands from the System Terminal.

DESCRIPTION

See Fig. 5-3.

1. The System Terminal sends the first character to the ACIA.

2. When the ACIA receives the complete character, it sends an interrupt to the system processor.

3. The system processor acknowledges the interrupt and reads the character from the ACIA. The ACIA also transmits the character back to the System Terminal to display the character sent (echo).

4. The system processor writes the character into System Memory.

5. Steps 1 through 4 are repeated for each character sent from the System Terminal. When the system processor receives the carriage return character from the System Terminal, it verifies that the command is valid and executes the command.

FUNCTIONAL PROCEDURE NO. 2

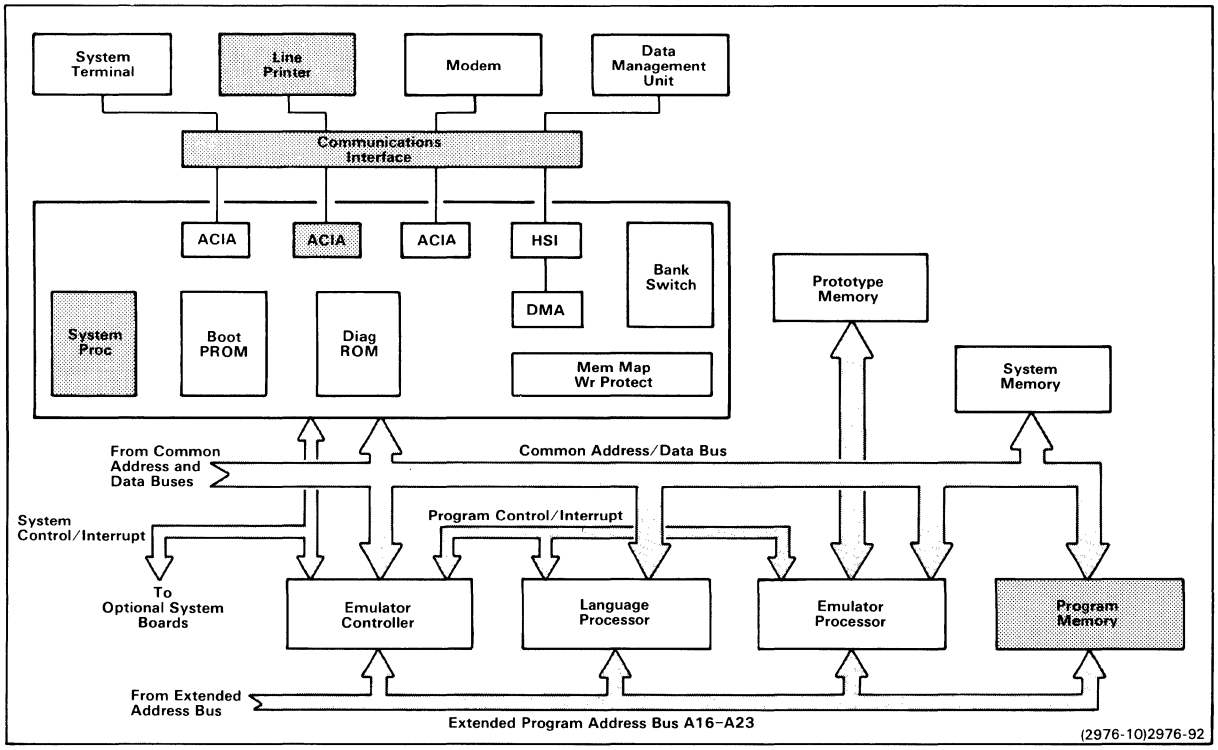


Fig. 5-4. 8301 MDU block diagram.

PROCEDURE

Writing to Line Printer

FUNCTION

This procedure describes the sequence of actions that occur when the system processor writes to the Line Printer.

BLOCKS INVOLVED

System Controller, Program Memory, Communications Interface, and Line Printer. (See Fig. 5-4.)

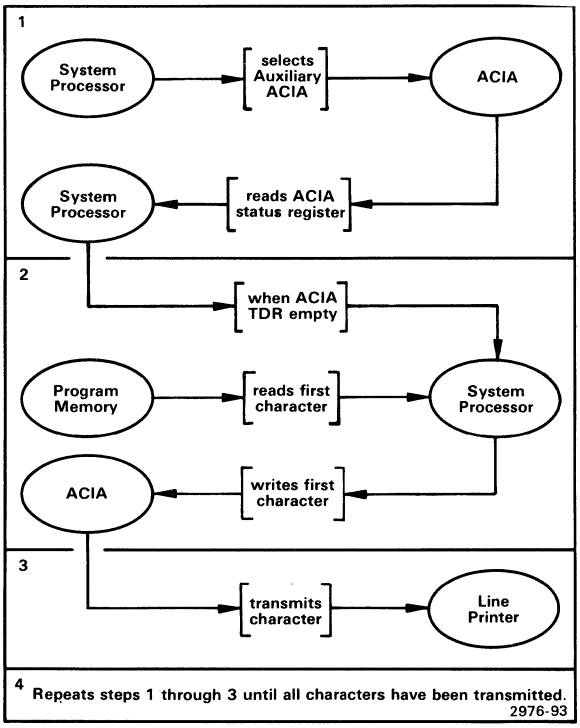


Fig. 5-5. Writing to Line Printer.

DESCRIPTION

See Fig. 5-5.

1. The system processor selects and reads the auxiliary ACIA status register.

2. The system processor reads the first character from Program Memory and writes this character to the auxiliary ACIA when the transmit data register (TDR) is empty.

3. The ACIA transmits the character to the Line Printer.

4. Steps 1 through 3 are repeated until all characters are transmitted.

FUNCTIONAL PROCEDURE NO. 3

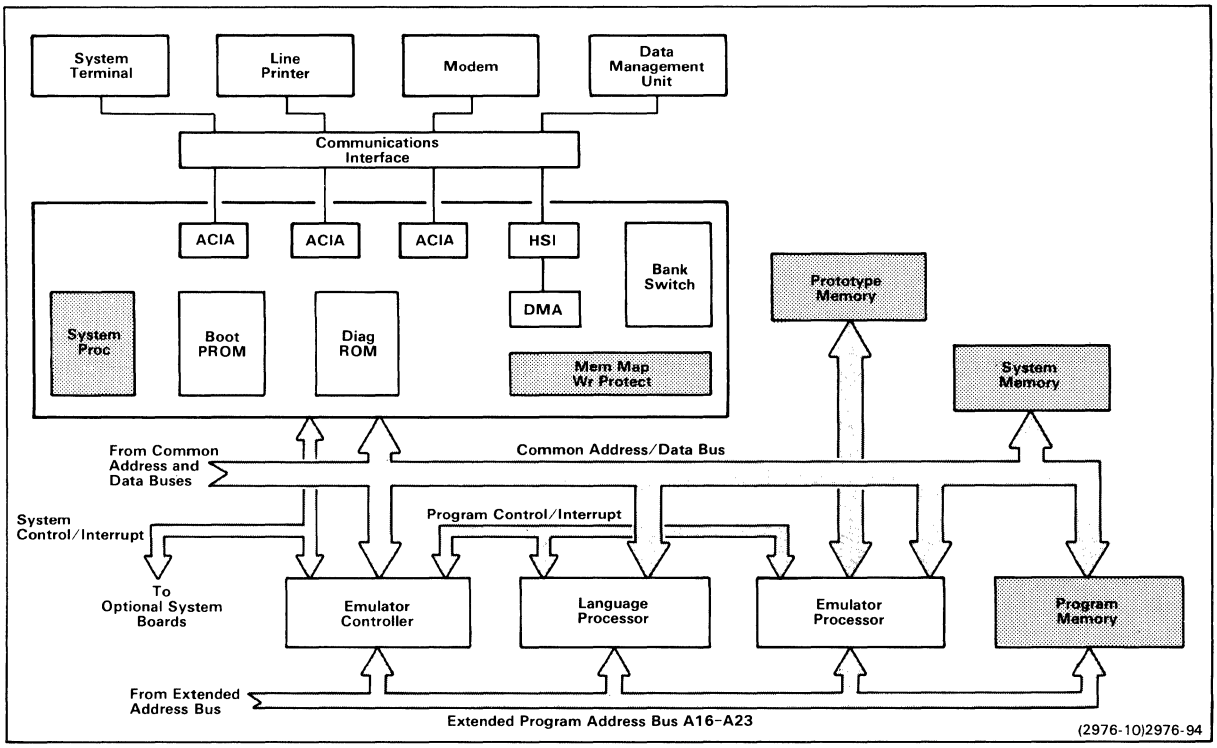


Fig. 5-6. 8301 MDU block diagram.

PROCEDURE

Memory Mapping Assignments

FUNCTION

Permits memory addresses to be assigned to either program or prototype memory. Memory addresses are assigned in 128-byte blocks. Memory mapping is available only for addresses 0000-FFFF.

BLOCKS INVOLVED

System Controller, Program Memory, and Prototype Memory. (See Fig. 5-6.)

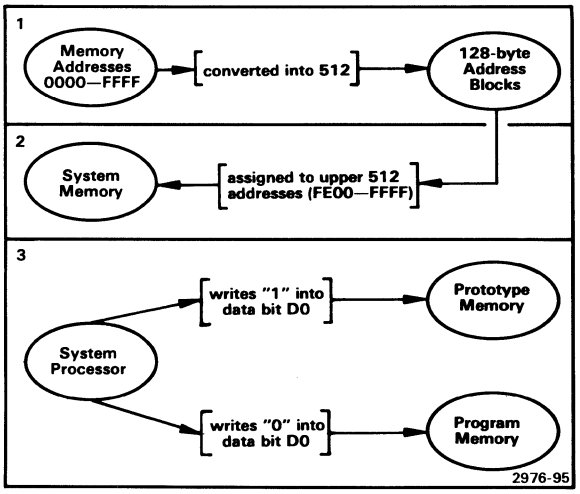


Fig. 5-7. Memory mapping assignments.

DESCRIPTION

See Fig. 5-7.

1. The 64K memory address range (0000---FFFF) is converted into 512 128-byte address blocks.

2. The 512 address blocks are assigned to the uppermost 512 addresses (FE00---FFFF) of System Memory address space.

3. The system processor writes a "1" into the associated data bit D0 for each address block assigned to the prototype memory and a "0" for each address block assigned to the 8301 Program Memory.

FUNCTIONAL PROCEDURE NO. 4

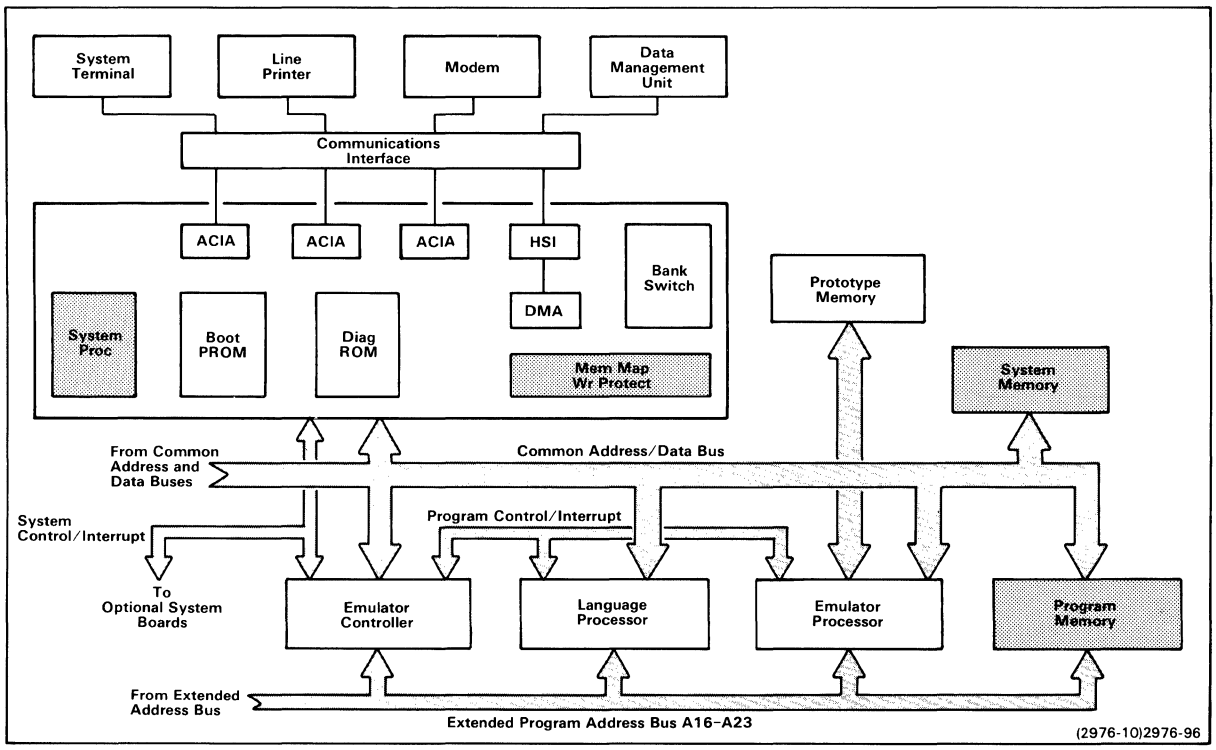


Fig. 5-8. 8301 MDU block diagram.

PROCEDURE

Write Protect Assignments

FUNCTION

Provides write protection of designated memory addresses in 8301 program memory. Memory addresses are assigned in 128-byte blocks. Write protection is available only for Program Memory addresses in the range of 0000---FFFF.

BLOCKS INVOLVED

System Controller and Program Memory. (See Fig. 5-8.)

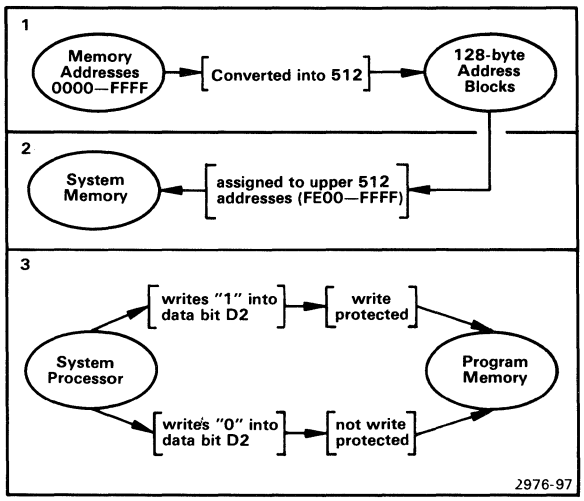


Fig. 5-9. Write protect assignments.

DESCRIPTION

See Fig. 5-9.

1. The 64K memory address range (0000---FFFF) is converted into 512 128-byte address blocks.

2. The 512 address blocks are assigned to the uppermost 512 addresses (FE00---FFFF) of System Memory address space.

3. The system processor writes a "1" into the associated data bit D2 for each address block to be write protected and a "0" for each address block to remove write protection.

FUNCTIONAL PROCEDURE NO. 5

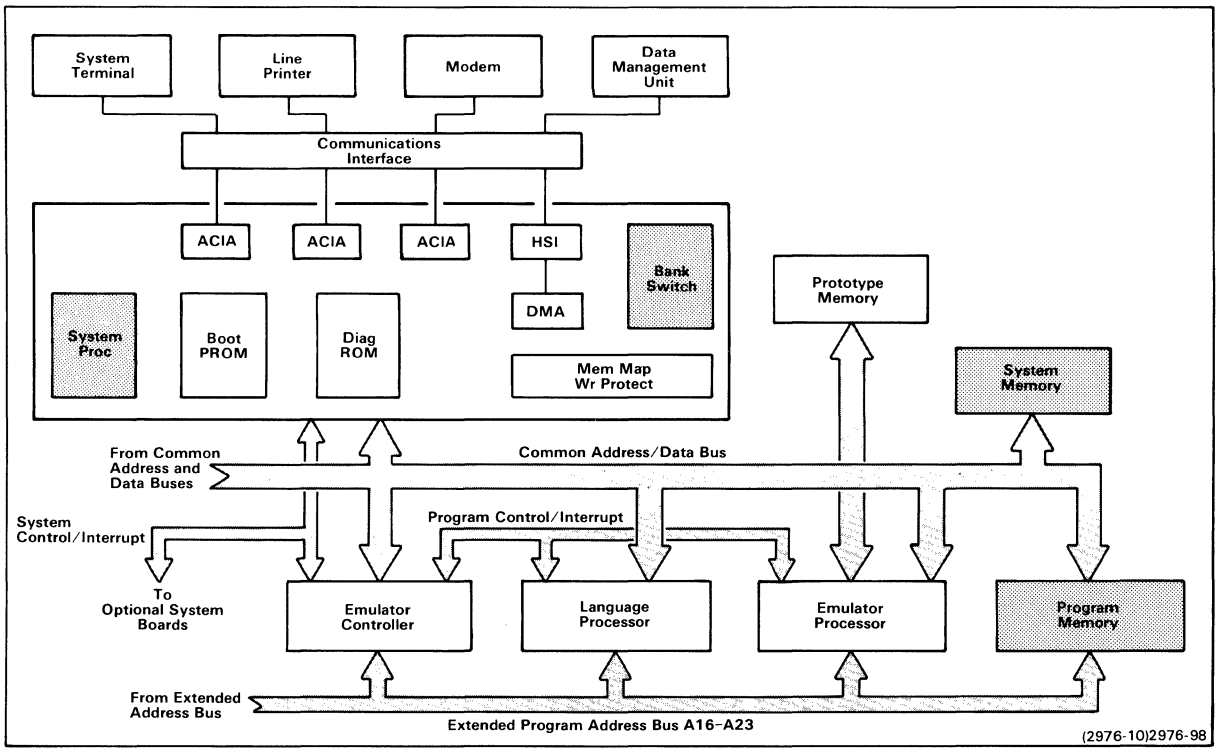


Fig. 5-10. 8301 MDU block diagram.

PROCEDURE

Bank Switching

FUNCTION

On initial power-up or restart the system processor can address only the lowest 16K addresses (0000---3FFF) in System Memory. Bank switching allows 16K-blocks of System Memory (16---64K) and Program Memory (0---64K) to be moved into the system processor's upper 16K address space (4000---7FFF). This permits the system processor to address up to 64K (on even 16K boundaries) of address space in both system and program memories.

BLOCKS INVOLVED

System Controller, System Memory, and Program Memory. (See Fig. 5-10.)

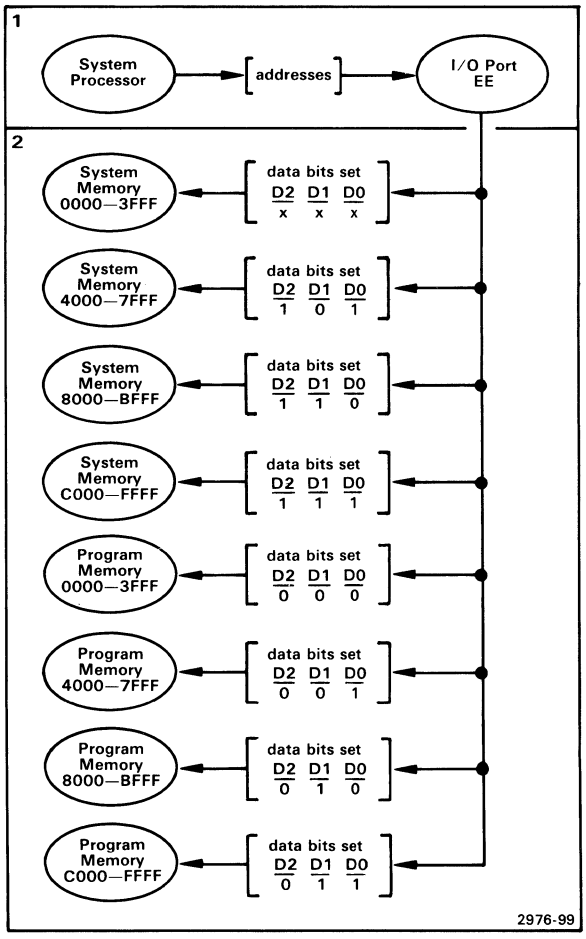


Fig. 5-11. Bank switching.

DESCRIPTION

See Fig. 5-11.

1. The system processor addresses I/O port address EE and sets the associated data bits to switch the desired 16K block into the system processor's upper address space (16---32K).

2. Data bits D0 and D1 determine which 16K address block is accessed.

D1	D0	16K Address Block Accessed
0	0	0000---3FFF
0	1	4000---7FFF
1	0	8000---BFFF
1	1	C000---FFFF

Data bit D2 specifies the memory address location.

D2	Address Location
1	System Memory
0	Program Memory

FUNCTIONAL PROCEDURE NO. 6

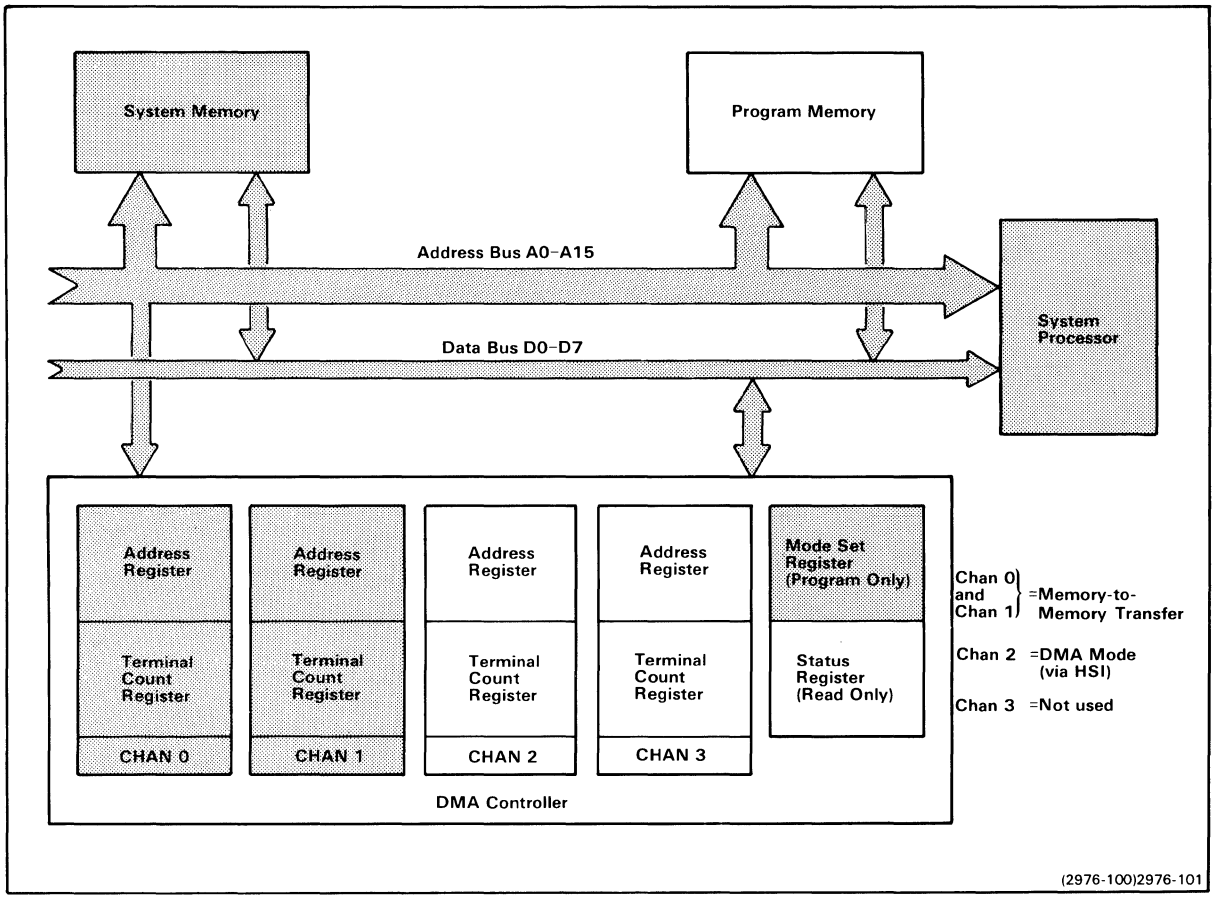


Fig. 5-12. DMA Controller functional block diagram.

PROCEDURE

Programming DMA Controller for Memory-to-Memory Transfer

FUNCTION

Channels 0 and 1 of the Direct Memory Access (DMA) controller are programmed for a memory-to-memory transfer. To program the DMA controller you must know the starting addresses in memory of where the data is located, the starting address of where the data is to be transferred and the amount of data bytes to be transferred. In this procedure, data is to be transferred from System Memory to program memory.

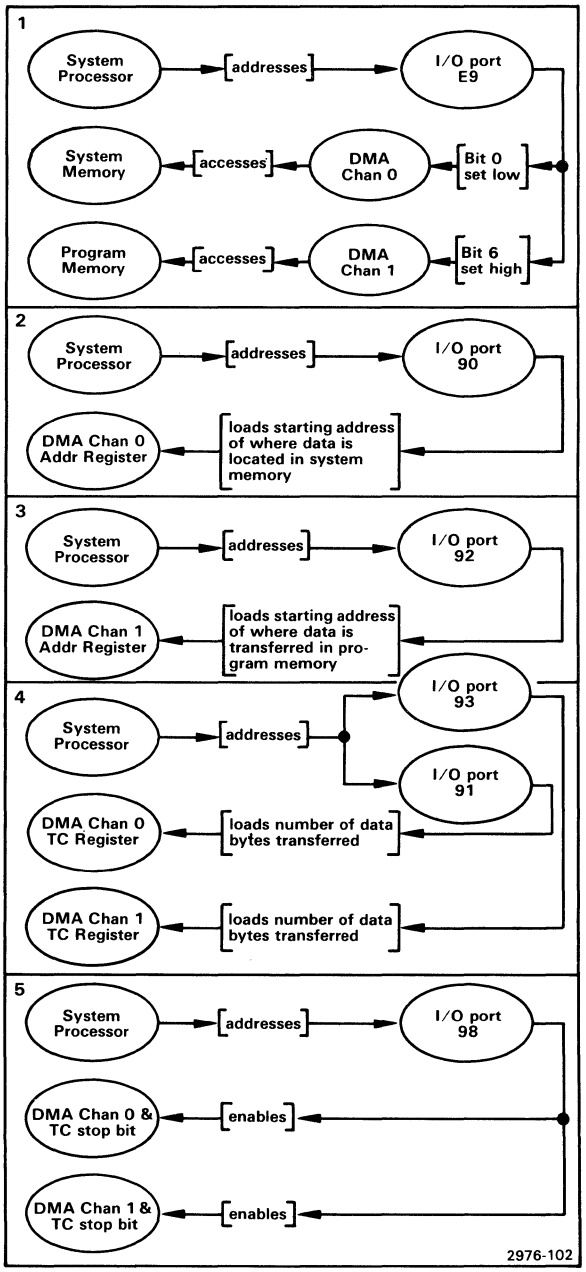


Fig. 5-13. Programming DMA for memory-to-memory transfer.

BLOCKS INVOLVED

System Processor, DMA controller, System Memory, and Program Memory. (See Fig. 5-12.)

DESCRIPTION

See Fig.5-13.

1. The system processor addresses I/O port E9 and sets DMA channel 0 to access System Memory and DMA channel 1 to access Program Memory.

2. The system processor addresses I/O port 90 and loads the starting address of where the data is located in System Memory, into DMA channel 0 address register.

3. The system processor addresses I/O port 92 and loads the starting address of where the data is to be transferred in Program Memory, into DMA channel 1 address register.

4. The system processor addresses I/O ports 91 and 93 and loads the number of data bytes transferred into the terminal count (TC) registers of DMA channels 0 and 1. DMA channel 0 is set for a DMA read cycle and DMA channel 1 is set for a DMA write cycle.

5. The system processor addresses I/O port 98, thus enabling DMA channels 0 and 1 along with the terminal count (TC) stop bit for both channels.

FUNCTIONAL PROCEDURE NO. 7

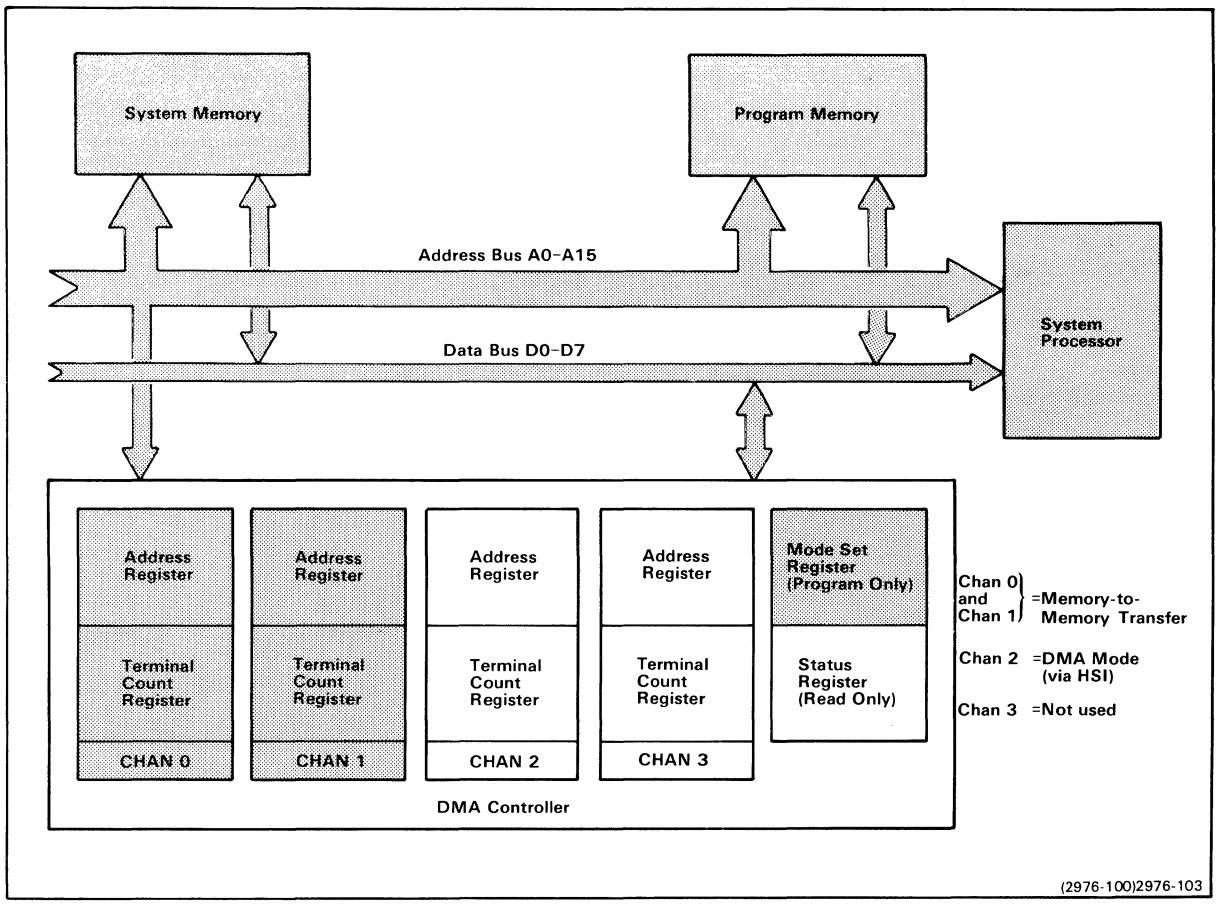


Fig. 5-14. DMA controller functional block diagram.

PROCEDURE

DMA Controller Memory-to-Memory Transfer Operation

FUNCTION

This procedure describes the sequence of actions that occur when data bytes are transferred from System Memory to Program Memory via the DMA controller. This procedure assumes the DMA controller is programmed for a memory-to-memory transfer as described in the previous procedure.

BLOCKS INVOLVED

system processor, DMA controller, System Memory, and Program Memory. (See Fig. 5-14.)

DESCRIPTION

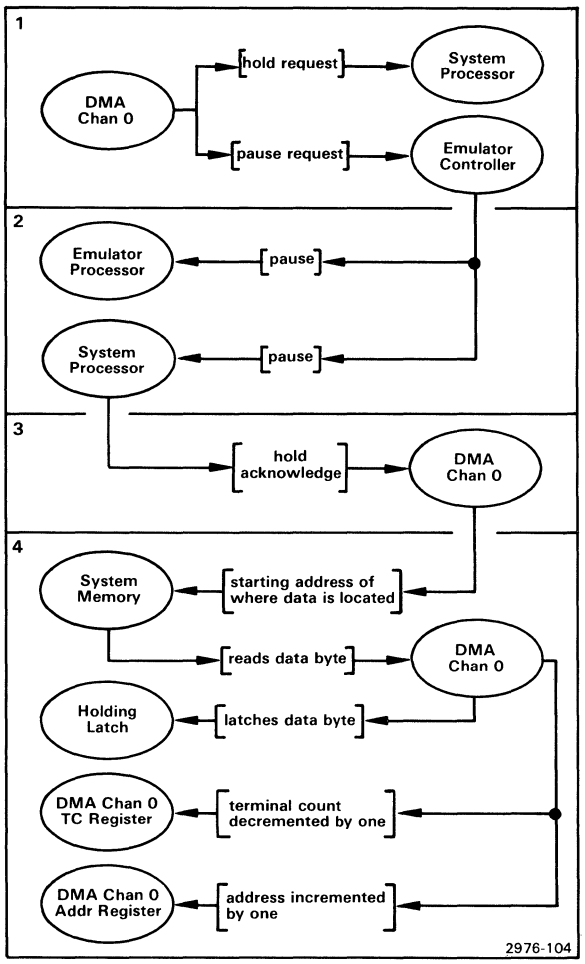


Fig. 5-15. DMA read cycle.

DMA Controller Read Cycle

See Fig. 5-15.

1. DMA channel 0 issues a hold request to the system processor and a pause request to the Emulator Controller.

2. The Emulator Controller clears the system bus by issuing a master and slave pause.

3. The system processor responds to the hold request with a hold acknowledge to DMA channel 0.

4. DMA channel 0 places the starting System Memory address on the address bus, reads the data byte from System Memory, and places the data byte in a holding latch, thus completing the DMA read cycle. The terminal count is decremented by one and the address is incremented by one in preparation for the next data character.

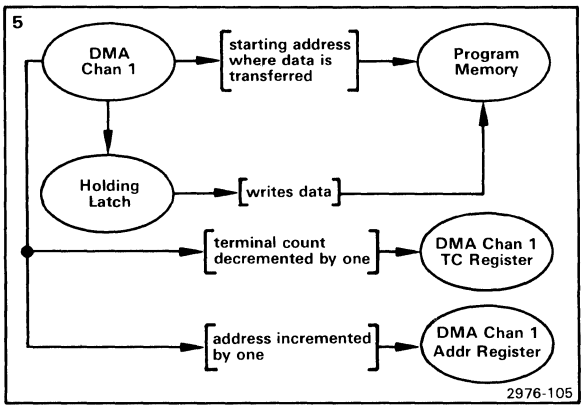


Fig. 5-16. DMA write cycle.

DMA Controller Write Cycle

See Fig. 5-16.

5. DMA channel 1 places the starting Program Memory address on the address bus and writes the data byte from the holding latch into program memory, thus completing the DMA write cycle. The terminal count is decremented by one and the address is incremented by one in preparation for the next character.

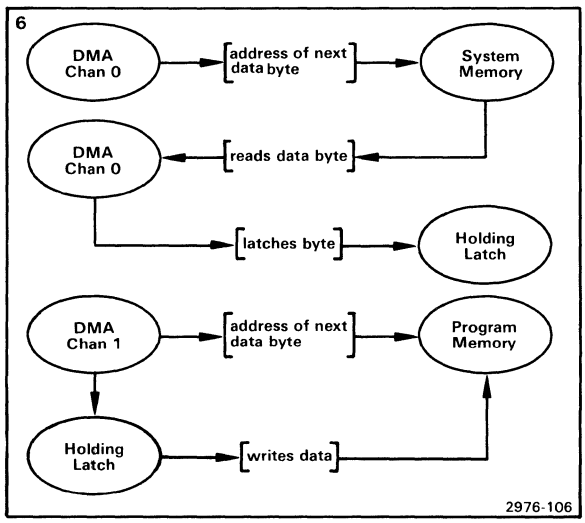


Fig. 5-17. Next data character.

Next Data Character

See Fig. 5-17.

6. Steps 4 and 5 are repeated until the terminal count register reaches zero. At that time, hold request is removed and the system processor regains control of the system buses.

FUNCTIONAL PROCEDURE NO. 8

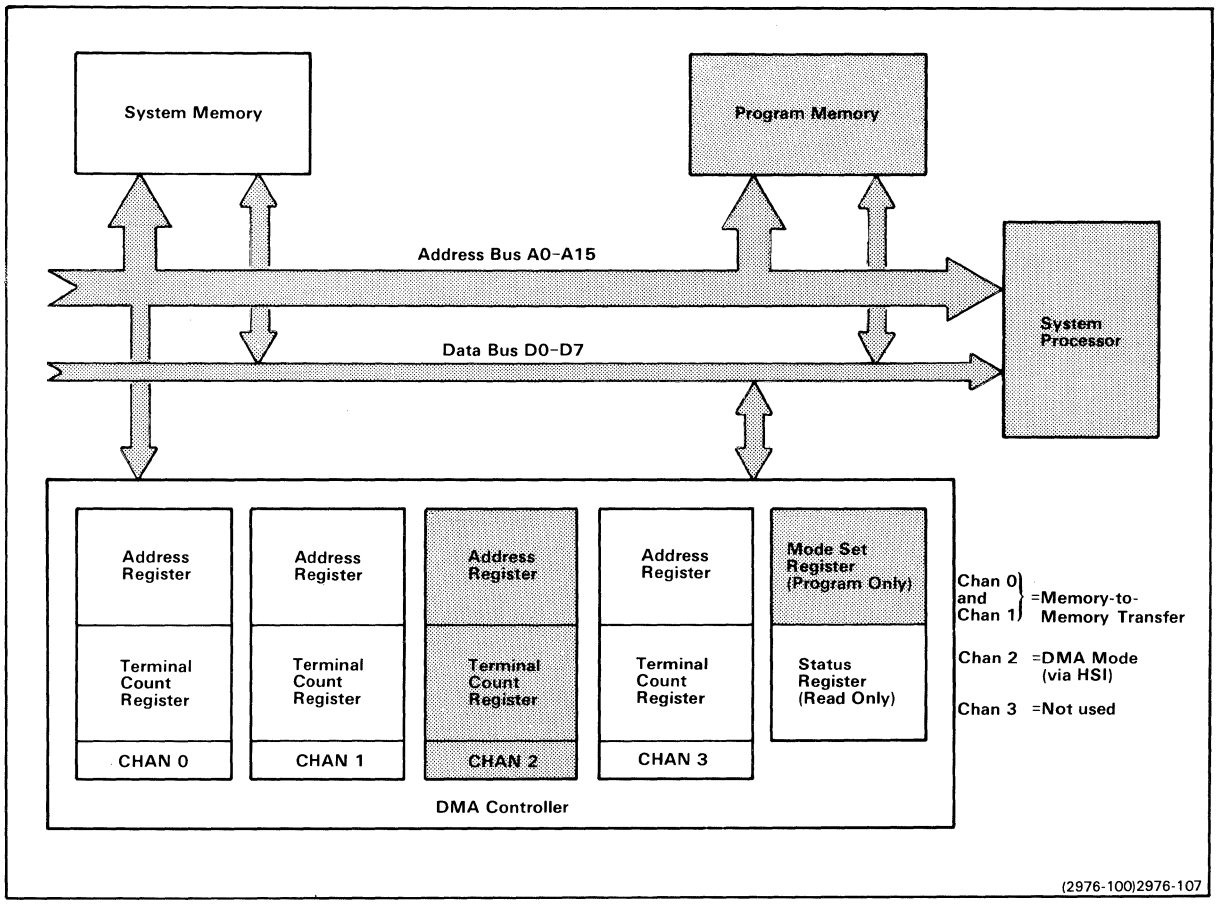


Fig. 5-18. DMA controller functional block diagram.

PROCEDURE

Programming the DMA controller for transferring a file from Program Memory to the Data Management Unit (DMU).

FUNCTION

The DMA controller must be programmed before a file can be transferred from Program Memory to the Data Management Unit (DMU). Once it is programmed, the DMA controller takes over and transfers the data file to the DMU via the HSI (high-speed serial interface).

BLOCKS INVOLVED

system processor and DMA controller. (See Fig. 5-18.)

DESCRIPTION

See Fig. 5-19.

1. The system processor addresses I/O port E9 and sets the data bits for a DMA transmit operation to the DMU, as follows:

   - Bit 1 --- set high to enable the HSI input interrupt.
   - Bit 3 --- set high to enable the DMA interrupt.
   - Bit 4 --- set high to enable a DMA read (from memory).
   - Bit 7 --- set low to enable DMA channel 2 for Program Memory access.

2. The system processor addresses I/O port 94 and loads the starting address of where the data is located in Program Memory, into DMA channel 2 address register.

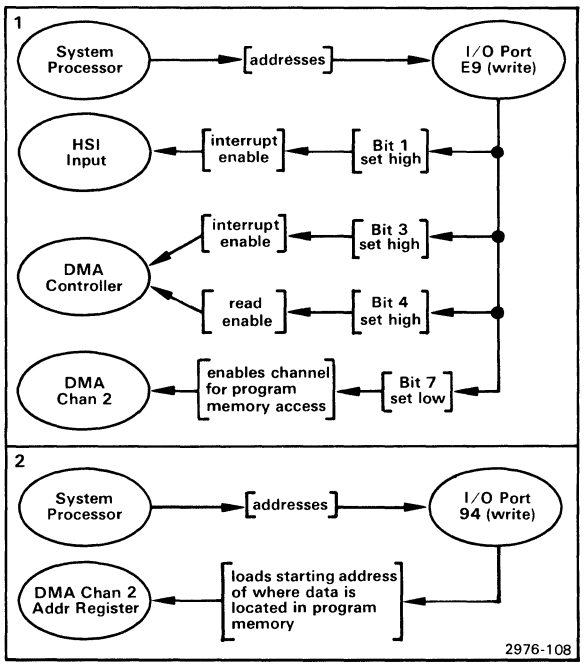


Fig. 5-19. Programming the DMA controller.

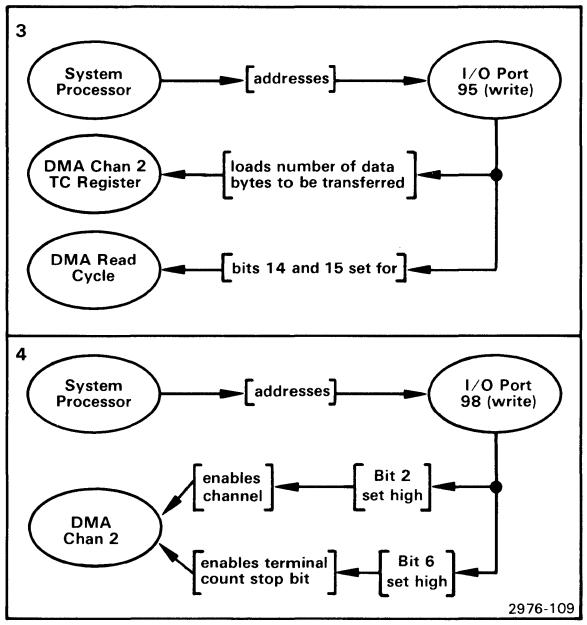


Fig. 5-20. Programming the DMA controller. (cont.)

See Fig. 5-20.

3. The system processor addresses I/O port 95 and loads the number of data bytes to be transferred into the terminal count (TC) register of DMA channel 2. Bits 14 and 15 in the terminal count register are set for a DMA read cycle (the DMA reads from memory and writes to the DMU).

4. The system processor addresses I/O port 98 and sets the data bits as follows:

   - Bit 2 --- set high to enable DMA channel 2
   - Bit 6 --- set high to enable the terminal count stop bit

FUNCTIONAL PROCEDURE NO. 9

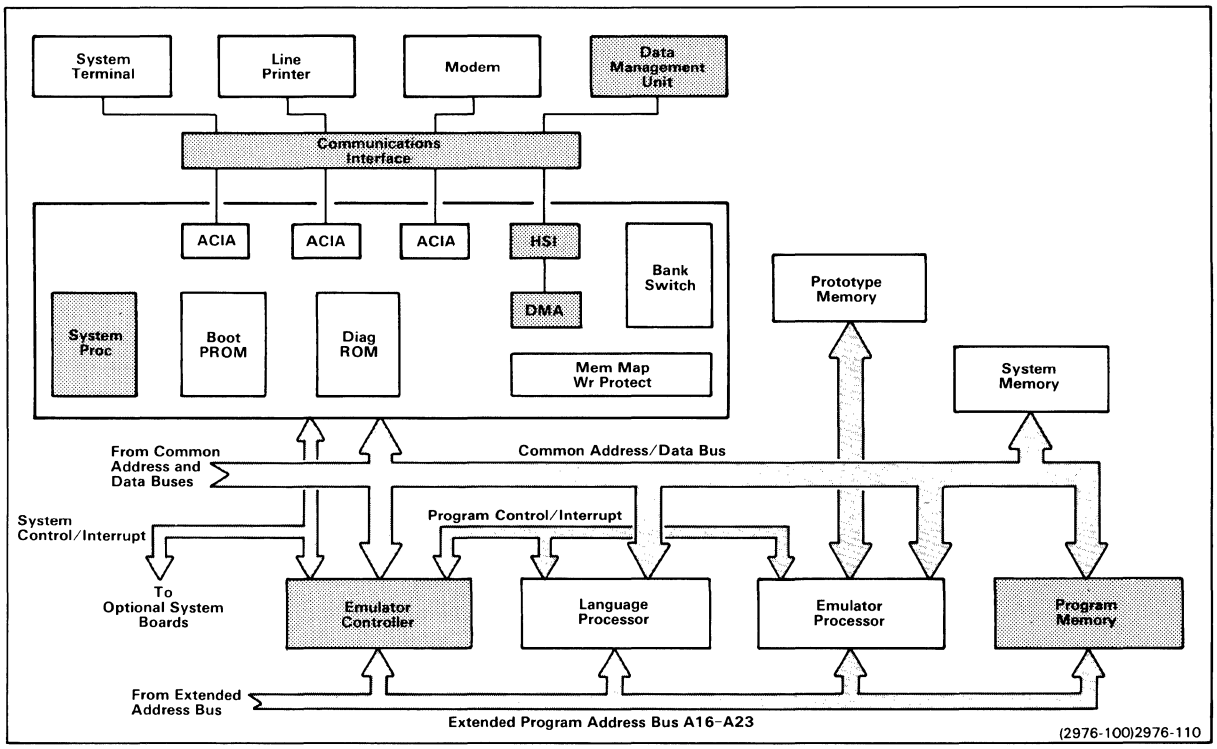


Fig. 5-21. 8301 MDU block diagram.

PROCEDURE

Transferring a file from Program Memory to the Data Management Unit (DMU).

FUNCTION

The DMA controller transfers data, one character at a time, from program memory to the DMU via the High-Speed Serial Interface ((HSI). When a character is loaded into the HSI transmitter buffer, the DMA relinquishes control of the system buses back to the system processor until the next character is ready for transmission.

BLOCKS INVOLVED

System Controller, Program Memory, Communications Interface, and Data Management Unit. (See Fig. 5-21.)

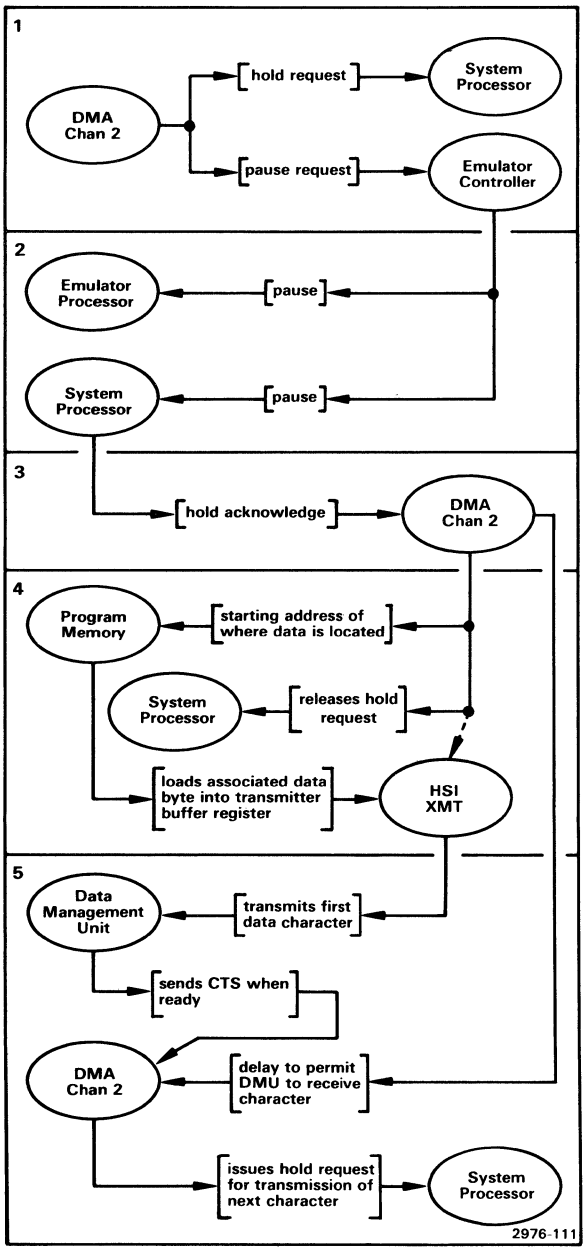


Fig. 5-22. Transmit operation.

DESCRIPTION

See Fig. 5-22.

1. DMA channel 2 issues a hold request to the system processor and a pause request to the Emulator Controller.

2. The Emulator Controller clears the system bus by issuing a master and slave pause.

3. The system processor responds to the hold request by issuing a hold acknowledge to DMA channel 2.

4. DMA channel 2 places the starting Program Memory address on the address bus and accesses the HSI. This loads the associated data byte at the starting Program Memory address into the transmitter buffer register of the HSI. The DMA relinquishes control of the system buses back to the system processor by releasing hold request.

5. The HSI serializes and transmits the first character to the Data Management Unit. A delay circuitry and the clear-to-send (CTS) line from the DMU prevents the next character's transmission until both are received by the DMA. This gives the DMU sufficient time to receive the character and process it. DMA channel 2 again issues a hold request to the system processor for transmission of the next character. Steps 1 through 5 are repeated for each character.

FUNCTIONAL PROCEDURE NO. 10

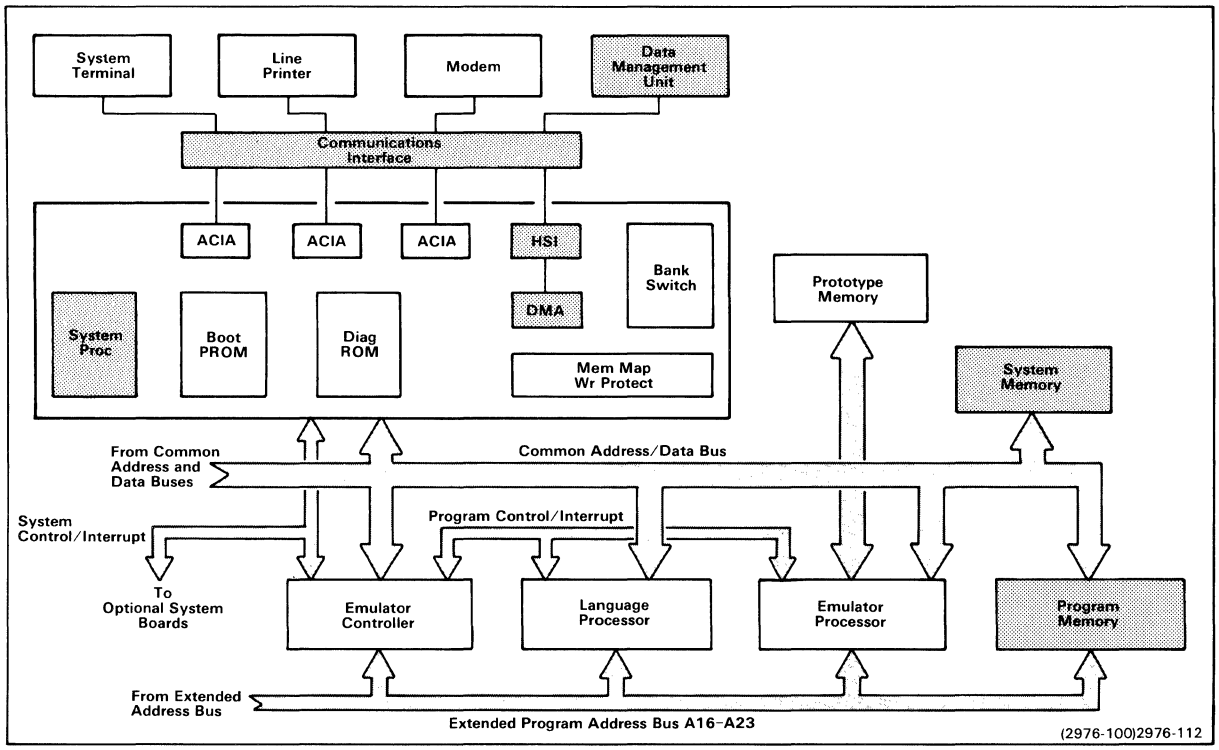


Fig. 5-23. 8301 MDU block diagram.

PROCEDURE

Transferring a file from the Data Management Unit to Program Memory.

FUNCTION

The 8301 receives the first data characters from the Data Management Unit in the non-DMA mode. Non-DMA mode involves only the HSI and the system processor. The characters are received from the DMU one at a time depending on the state of the Ready-For-Data (RFD) line. The first characters tell the system processor what is to be sent. If the first character is an "81", it signifies the start-of-header (SOH). The system processor knows that the next seven bytes (the remainder of the header) will contain protocol information and the length of the data message that follows the header. From this information the system processor programs the registers in the DMA to receive the data message following the header.

BLOCKS INVOLVED

System Controller, Program Memory, System Memory, Communications Interface, and Data Management Unit. (See Fig. 5-23.)

DESCRIPTION

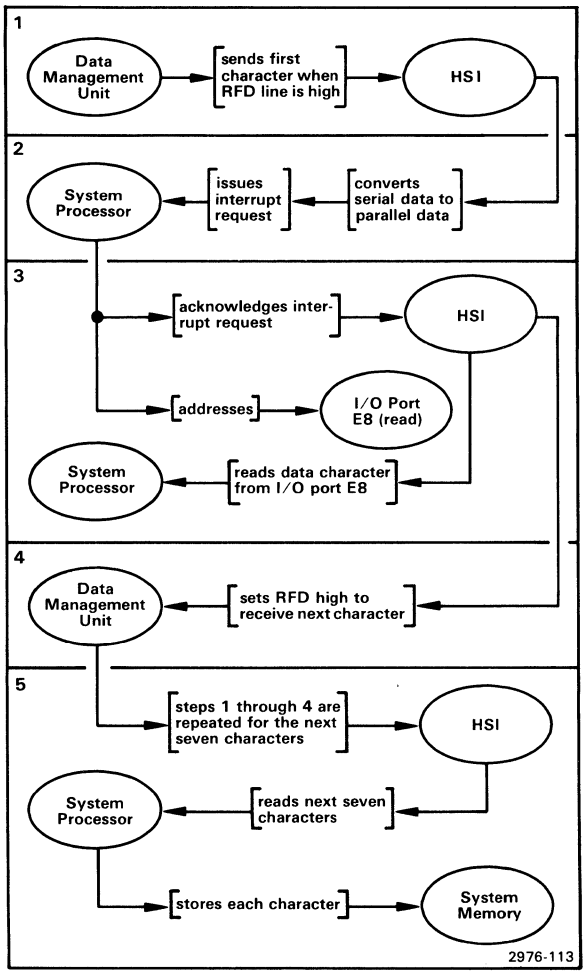


Fig. 5-24. Receiving header message.

Receiving Header Message

See Fig. 5-24.

1. Data Management Unit sends the first character via the HSI to the 8301 when the RFD (Ready-For-Data) line is high.

2. The HSI receiver converts the serial data into parallel data and issues an interrupt request to the system processor, to indicate a character has been received.

3. The system processor acknowledges the interrupt request and reads the data character from the HSI by addressing I/O port E8 (read).

4. The HSI sets RFD high in preparation for receiving the next character from the Data Management Unit.

5. Steps 1 through 4 are repeated for the next seven characters. The system processor reads each character and then stores them in System Memory.

Programming the DMA Controller

See Fig. 5-25.

6. The system processor reads the header information stored in system memory and programs the DMA controller to transfer the message file from the Data Management Unit into Program Memory. The system processor addresses I/O port 94 (write) and loads a predetermined address (established by the operating system) into the address register of DMA channel 2. This predetermined address is the starting location of the message file in Program Memory.

7. The system processor addresses I/O port 95 (write) and loads the number of data bytes to be transferred into the TC (terminal count) register of DMA channel 2. Bits 14 and 15 in the TC register are set for a DMA write cycle (the DMA reads the data from the Data Management Unit that is stored in the HSI receiver register and writes it into Program Memory).

8. The system processor addresses I/O port 98 and sets the data bits in the DMA channel 2' mode register as follows:

   - Bit 2 --- set high to enable DMA channel 2
   - Bit 6 --- set high to enable DMA channel 2 terminal count stop bit

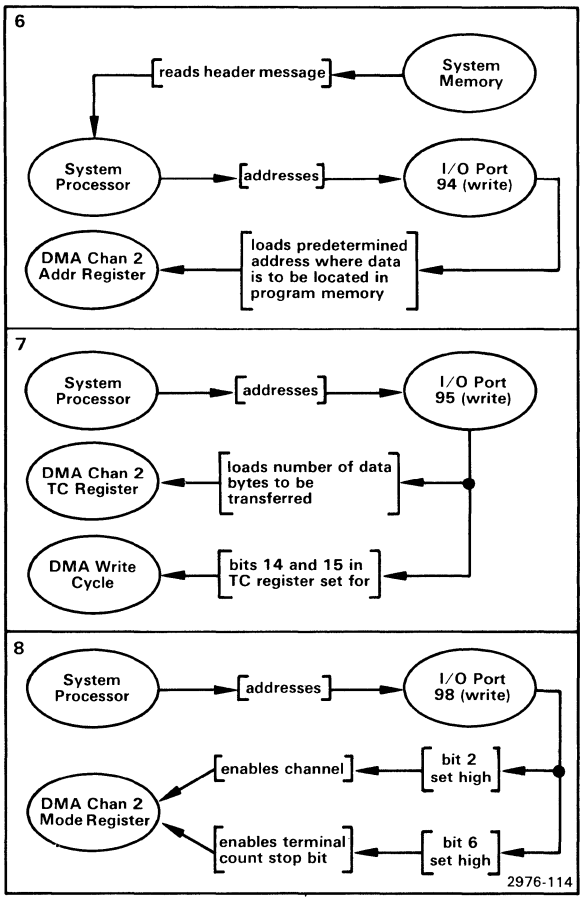


Fig.5-25. Programming the DMA Controller.

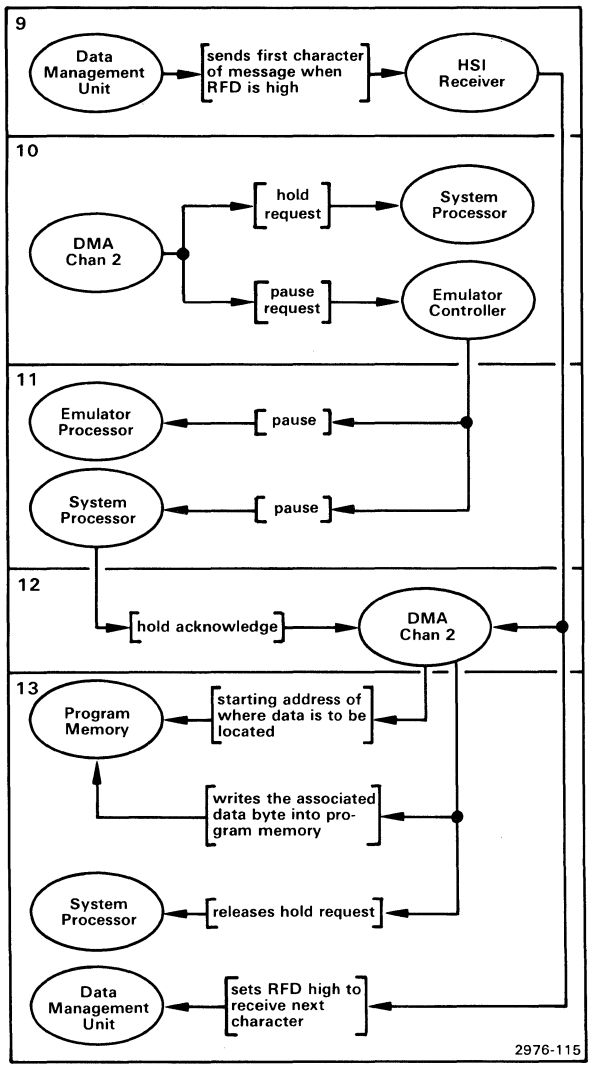


Fig. 5-26. Receive operation.

Receive Operation

See Fig. 5-26.

9. The Data Management Unit sends the first character of the message when the 8301 sets the RFD line high. The serialized data character is stripped of the start and stop bits, converted into a parallel data byte, and stored in the receiver buffer register.

10. DMA channel 2 issues a hold request to the system processor and a pause request to the Emulator Controller.

11. The Emulator Controller clears the system bus by issuing a master and slave pause.

12. The system processor responds to the hold request by issuing a hold acknowledge to DMA channel 2.

13. DMA channel 2 places the starting address of where the data is to be located in Program Memory onto the address bus. The DMA reads the HSI receiver buffer register, writes the associated data byte into program memory, and relinquishes control of the system buses back to the system processor by releasing the hold request. The HSI sets the RFD line high in preparation to receive the next data character from the Data Management Unit. Steps 9 through 13 are repeated until the terminal count register reaches zero, which is the last data byte in the message being sent by the Data Management Unit.

Section 6

SPECIFICATIONS

INTRODUCTION

This section contains the specifications for the 8301 MDU. Tables 6-1, 6-2, and 6-3 list the specifications for the entire 8301 MDU. Table 6-4 lists the specifications for each circuit board within the instrument. Tables 6-5 through 6-12 contain the 8301 I/O port characteristics for all connectors on the 8301 rear panel. These tables define the peripheral interface requirements.

Table 6-1
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
Primary Power Input Voltages	115 Vac Low, *	90 to 110 Vac
	115 Vac High, *	108 to 132 Vac
	230 Vac Low, or *	180 to 220 Vac
	230 Vac High *	216 to 250 Vac
Frequency		49 to 63 Hz
Line Fuses 115 Vac		3AG, 8 Amps, 250 Volt, medium-blow (5 sec.)
230 Vac		3AG, 4 Amps, 250 Volt, medium-blow (5 sec.)
Line Current (maximum)		7 Amps
Power Consumption (maximum)		700 Watts

Table 6-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Power Supply	+5.2 Vdc +1%/-2% **	With all boards installed *** in unit. Do not exceed maximum current of 35 Amps.
	+12.0 Vdc +/- 5% **	With all boards installed *** in unit. Do not exceed maximum current of 1.7 Amps.
	-12.0 Vdc +/- 5% **	With all boards installed *** in unit. Do not exceed maximum current of 1.7 Amps.
Heat Dissipation Typical		684 BTU/hr
Maximum		1,227 BTU/hr
Static Discharge Operating Front Panel LEDs		12.5 kV and below with no effect on operation of unit
Except for Front Panel LEDs		15 kV and below with no effect on operation of unit NOTE Static voltage must not be applied to the pins of any external connector.
Line Regulation		Within .05% for 10% line voltage change
Load Regulation		Within .05% for 50% load change

*= Set switches S300 and S301 to one of the above operating positions, determined by the primary voltage source.

**= Refer to Section 8, Maintenance, of this manual if the voltages are out of tolerance.

***= Do not exceed the recommended circuit board arrangement shown in Fig. 1-2 of Section 1.

Table 6-2
Environmental Characteristics

Characteristic	Description
Temperature	
Operating	0 C to +50 C (+32 F to +122 F)
Storage	-55 C to +75 C (-67 F to +167 F)
Humidity	
Operating	To 90% relative non-condensing
Altitude	
Operating	To 4 500 m (15,000 feet)
Storage	To 15 000 m (50,000 feet)

Table 6-3
Physical Characteristics

Characteristic	Description
Net Weight	27 kg (60 lb.)
Overall Dimensions	
Height	267 mm (10.5 in.)
Width	432 mm (17 in.)
Length	597 mm (23.5 in.)

Table 6-4
Circuit Board Power Requirements

Circuit Board	Voltage	Typical Amps	Maximum Amps
System Controller	+12 Vdc	0.019	0.023
	-12 Vdc	0.018	0.022
	+5 Vdc	2.7	3.24
Communications Interface	+12 Vdc	0.019	0.023
	-12 Vdc	0.018	0.022
	+5 Vdc	0.20	0.24
Emulator Controller	+5 Vdc	1.4	1.68
Front Panel	+5 Vdc	0.072	0.113
System RAM	+5 Vdc	1.555	2.117
Language Processor	+5 Vdc	0.52	0.63
Program Memory	+5 Vdc	3.8	4.56

Table 6-5
8301 I/O Port Characteristics
HSI Port Specifications -- J100

Characteristics	Description
Type	RS-422
Baud Rate	HSI -- 153.6K Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Even
Signal Descriptions:	
Pin 1	Shield
Pin 2	TX -- Transmit Data
Pin 3	RX -- Receive Data
Pin 4	RTS -- Request To Send (pulled-up to +5 Vdc with 200 ohm resistor)
Pin 5	CTS -- Clear To Send
Pin 10	RTS' -- Request To Send (always grounded)
Pin 11	TX' -- Transmit Data
Pin 12	RX' -- Receive Data
Pin 13	DTR' -- Data Terminal Ready
Pin 20	DTR -- Data Terminal Ready
Pin 25	CTS' -- Clear To Send

Table 6-6
8301 I/O Port Characteristics
Remote Port Specifications With DTE1 Selected -- J101
(Configured as a DTE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110 - 9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 3	RX -- Receive Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 4	RTS -- Request To Send (connected to RTS output on ACIA Type 6850 - U2600-5)
Pin 5	CTS -- Clear To Send (connected to CTS input on ACIA Type 6850 - U2600-24)
Pin 6	DSR -- Data Set Ready (ignored - connected to input of receiver Type 1489 - U3060D)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (connected to DCD input on ACIA Type 6850 - U2600-23)
Pin 20	DTR -- Data Terminal Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)

NOTE

The 8301 looks at CTS to implement the handshake on data transmissions from the peripheral to the 8301.

Table 6-7
8301 I/O Port Characteristics
Remote Port Specifications With DTE2 Selected -- J101
(Configured as a DTE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110 - 9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 3	RX -- Receive Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 4	RTS -- Request To Send (connected to RTS output on ACIA Type 6850 - U2600-5)
Pin 5	CTS -- Clear To Send (ignored - connected to input of receiver Type 1489 - U3060C)
Pin 6	DSR -- Data Set Ready (connected to CTS input on ACIA Type 6850 - U2600-24)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (connected to DCD input on ACIA Type 6850 - U2600-23)
Pin 20	DTR -- Data Terminal Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)

NOTE

The 8301 looks at DSR to implement the handshake on data transmissions from the peripheral to the 8301.

Table 6-8
8301 I/O Port Characteristics
Remote Port Specifications With CNTL(L) Selected -- J101
(Configured as a DTE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110 - 9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 3	RX -- Receive Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 4	RTS -- Request To Send (Jumper J2 on Communications Interface board selects CTS as the RTS output or continuously asserts RTS. RTS is continuously asserted for normal operation.)
Pin 5	CTS -- Clear To Send (ignored - connected to input of receiver Type 1489 - U3060C)
Pin 6	DSR -- Data Set Ready (ignored - connected to input of receiver Type 1489 - U3060D)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (ignored - connected to input of receiver Type 1489 - U3060A)
Pin 20	DTR -- Data Terminal Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)

NOTE

This configuration requires only TX, RX, and ground to be implemented by the peripheral in order to transfer data. No handshaking can take place in this configuration.

Table 6-9
8301 I/O Port Characteristics
Remote Port Specifications With CNTL(L) Selected -- J102
(Configured as a DCE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110 - 9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 3	RX -- Receive Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 4	RTS -- Request To Send (ignored - connected to input of receiver Type 1489 - U3060A)
Pin 5	CTS -- Clear To Send (Jumper J1 on Communications Interface board selects RTS as the CTS output or continuously asserts CTS. CTS is continuously asserted for normal operation.)
Pin 6	DSR -- Data Set Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 20	DTR -- Data Terminal Ready (ignored - connected to input of receiver Type 1489 - U3060D)

NOTE

This configuration requires only TX, RX, and ground to be implemented by the peripheral in order to transfer data. No handshaking can take place in this configuration.

Table 6-10
8301 I/O Port Characteristics
Remote Port Specifications With DCE Selected -- J102
(Configured as a DCE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110 - 9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to RxD input on ACIA Type 6850 - U2600-2)
Pin 3	RX -- Receive Data (connected to TxD output on ACIA Type 6850 - U2600-6)
Pin 4	RTS -- Request To Send (connected to DCD input on ACIA Type 6850 - U2600-23)
Pin 5	CTS -- Clear To Send (connected to RTS output on ACIA Type 6850 - U2600-5)
Pin 6	DSR -- Data Set Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 20	DTR -- Data Terminal Ready (connected to CTS input on ACIA Type 6850 - U2600-24)

NOTE

DTR must be used to control data transmission from the 8301 to the peripheral. RTS/CTS are used to control data transmission from the peripheral to the 8301.

Table 6-11
8301 I/O Port Characteristics
Auxiliary Port Specifications -- J103
(Configured as a DCE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110 - 9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to RxD input on ACIA Type 6850 - U2500-2)
Pin 3	RX -- Receive Data (connected to TxD output on ACIA Type 6850 - U2500-6)
Pin 4	RTS -- Request To Send (connected to DCD input on ACIA Type 6850 - U2500-23)
Pin 5	CTS -- Clear To Send (connected to RTS output on ACIA Type 6850 - U2500-5)
Pin 6	DSR -- Data Set Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 20	DTR -- Data Terminal Ready (connected to CTS input on ACIA Type 6850 - U2500-24)

NOTE

DTR must be used to control data transmission from the 8301 to the peripheral. RTS/CTS are used to control data transmission from the peripheral to the 8301.

Table 6-12
8301 I/O Port Characteristics
Terminal Port Specifications -- J104
(Configured as a DCE Port)

Characteristics	Description
Type	RS-232-C
Baud Rate	Selectable 110 - 9600 Baud
Bits/Character	8
Number of Stop Bits	1
Parity	Not Checked
Signal Descriptions:	
Pin 1	Protective Ground
Pin 2	TX -- Transmit Data (connected to RxD input on ACIA Type 6850 - U2700-2)
Pin 3	RX -- Receive Data (connected to TxD output on ACIA Type 6850 - U2700-6)
Pin 4	RTS -- Request To Send (connected to DCD input on ACIA Type 6850 - U2700-23)
Pin 5	CTS -- Clear To Send (connected to RTS output on ACIA Type 6850 - U2700-5)
Pin 6	DSR -- Data Set Ready (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 7	Signal Ground
Pin 8	DCD -- Data Carrier Detect (pulled-up to +12 Vdc with 3.3 kilohm resistor)
Pin 20	DTR -- Data Terminal Ready (connected to CTS input on ACIA Type 6850 - U2700-24)

NOTE

DTR must be used to control data transmission from the 8301 to the peripheral. RTS/CTS are used to control data transmission from the peripheral to the 8301.

Section 7

TECHNICAL REFERENCE MATERIAL

INTRODUCTION

This section contains technical reference material applicable to the 8301 MDU.

8301 SYSTEM BUS ASSIGNMENTS

The 8301 system bus is contained in the Main Interconnect board. The system bus is a 100-line bus configuration. Some of the lines are common to both the system and program sections. Other lines are dedicated to the system or program sections. Line numbers 1 through 60 and 82 through 100 are common to both system and program sections. Line numbers 61 through 81 are dedicated to each section. Table 7-1 shows the bus line number, the mnemonic name assigned, and a brief description of each line. This table is useful when reading the functional descriptions of the various circuit boards contained in this manual. It is also helpful in understanding the function of the various lines, when used in conjunction with the schematic drawings in this manual.

Table 7-1
8301 System Bus Assignments

Line No.	Mnemonic	Description
COMMON LINES, Line Nos. 1---60 (System and Program Sections)		
1---4	+5 Vdc	Primary TTL power supply.
5---8	AUX Bus	Undesignated power bus lines.
9---10	GND	Common ground with bus lines 15---16, 56, 85, and 97---100.
11---12	+12 Vdc	+12 volt power supply.
13---14	-12 Vdc	-12 volt power supply.
15---16	GND	Common ground with bus lines 9---10, 56, 85, and 97---100.

Table 7-1 (cont)

Line No.	Mnemonic	Description
COMMON LINES, Line Nos. 1---60 (System and Program Sections) (cont)		
17	A0(L)	Least significant bus address line.
18	A1(L)	Bus address line.
19	A2(L)	Bus address line.
20	A3(L)	Bus address line.
21	A4(L)	Bus address line.
22	A5(L)	Bus address line.
23	A6(L)	Bus address line.
24	A7(L)	Bus address line.
25	A8(L)	Bus address line.
26	A9(L)	Bus address line.
27	A10(L)	Bus address line.
28	A11(L)	Bus address line.
29	A12(L)	Bus address line.
30	A13(L)	Bus address line.
31	A14(L)	Bus address line.
32	A15(L)	Most significant bus address line to system and program sections.
33	CMEM(H)	Bank switch command -- When high, allows system processor to address program memory.
34	RAM INH(L)	Allows any board to override a RAM address and control the data bus.
35	WD ACCESS(L)	Enables data on 16 bits of the data bus when used in conjunction with a 16-bit emulator.
36	D0(L)	Least significant data bus line.
37	D1(L)	Data bus line.
38	D2(L)	Data bus line.
39	D3(L)	Data bus line.
40	D4(L)	Data bus line.
41	D5(L)	Data bus line.
42	D6(L)	Data bus line.
43	D7(L)	Data bus line.
44	D8(L)	Data bus line.
45	D9(L)	Data bus line.
46	D10(L)	Data bus line.
47	D11(L)	Data bus line.
48	D12(L)	Data bus line.
49	D13(L)	Data bus line.
50	D14(L)	Data bus line.
51	D15(L)	Most significant data bus line.

Table 7-1 (cont)

Line No.	Mnemonic	Description
COMMON LINES, Line Nos. 1---60 (System and Program Sections) (cont)		
52	M(L)/IO(H)	Indicates whether the active emulator is addressing memory (low) or I/O (high).
53	WRP(L)	Indicates that data on the bus is valid for a write command.
54	OPREQ(L)	Indicates when a bus operation is in progress.
55	R(H)/W(L)	Read/Write control line. Signifies a Read or Write operation to memory and I/O.
56	GND	Common ground with bus lines 9---10, 15---16, 85, and 97---100.
57	JMP CMD(L)	Issued by the Emulator Controller board to initiate a forced emulator processor jump.
58	RUN(L)	Indicates that the active Emulator Processor board is in the RUN state.
59	RESET(L)	Initializes all 8301 logic. RESET(L) is asserted with either power-on or Front Control Panel reset.
60	JMP ACK(L)	A response from the emulator processor to the Emulator Controller board to enable a jump address onto the system address bus.
DEDICATED LINES TO SYSTEM SECTION, Line Nos. 61---81		
61	INTACK(L)	Issued by the system processor in response to an interrupt request.
62	INT 0(L)	Interrupt Level 0.
63	INT 1(L)	Interrupt Level 1.
64	INT 2(L)	Interrupt Level 2.
65	INT 3(L)	Interrupt Level 3.
66	INT 4(L)	Interrupt Level 4.
67	INT 5(L)	Interrupt Level 5.

Table 7-1 (cont)

Line No.	Mnemonic	Description
DEDICATED LINES TO SYSTEM SECTION, Line Nos. 61---81 (cont)		
68	INT 6(L)	Interrupt Level 6.
69	INT 7(L)	Interrupt Level 7.
70	INT 8(L)	Interrupt Level 8.
71	INT 29(L)	Interrupt Level 29.
72	INT 30(L)	Interrupt Level 30.
73	INT 31(L)	Interrupt Level 31.
74	INT 12(L)	Interrupt Level 12.
75	INT 13(L)	Interrupt Level 13.
76	INT 14(L)	Interrupt Level 14.
77	INT 15(L)	Interrupt Level 15.
78	MSTR PSE(L)	Indicates the system processor is paused with its data, control, and address lines tristated.
79	DBG INT(L)	Line from the Emulator Controller board to the System Controller board, used for interrupt request.
80	DBG VEN(L)	Debug vector enable from the system processor, acknowledging the debug interrupt and enabling the debug interrupt vector.
81	MSTR INTD(L)	Master interrupted line from the system processor to Emulator Controller board. This line causes the emulator processor to be paused and the system processor to run.
DEDICATED LINES TO PROGRAM SECTION, Line Nos. 61---81		
61	SLV INTACK(L)	Issued by the emulator processor in response to an interrupt request.
62	SLV INT 0(L)	Slave interrupt level 0.

Table 7-1 (cont)

Line No.	Mnemonic	Description
DEDICATED LINES TO PROGRAM SECTION, Line Nos. 61---81 (cont)		
63	A16(L)	Extended bus address line to program section.
64	A17(L)	Extended bus address line to program section.
65	A18(L)	Extended bus address line to program section.
66	A19(L)	Extended bus address line to program section.
67	A20(L)	Extended bus address line to program section.
68	A21(L)	Extended bus address line to program section.
69	A22(L)	Extended bus address line to program section.
70	A23(L)	Extended bus address line to program section.
71	DBG INT 29(L)	Debug interrupt provided by the RTPA.
72	DBG INT 30(L)	Debug interrupt provided by the RTPA.
73	DBG INT(L)	Debug interrupt generated by the emulator related hardware and passed on to the system processor (open collector).
74	UPSE(L)	Generated by the emulator processor.
75	SLV OPREQ(L)	Used by the Emulator Controller board and the RTPA.
76	SLV RESET(L)	Used by the Emulator Controller board to reset the emulator processor.
77	SLV PSE(L)	Issued by the Emulator Controller board to the emulator processor.
78	RFSH NW(L)	Issued by the emulator processor to refresh the program memory.
79	SLV INOP(L)	Issued by the RTPA to reset active lines in the emulator processor.
80	SWAP(L)	Used only by the 9900 Emulator Processor to swap addresses in program memory.
81	Spare	Spare line in the program section.

Table 7-1 (cont)

Line No.	Mnemonic	Description
COMMON LINES, Line Nos. 82---100 (System and Program Sections)		
82	FETCH(L)	FETCH line from the active emulator processor, signifying an instruction fetch.
83	PAUSE(L)	Causes all processors to go to an inactive state with control, address, and data lines tristated.
84	MSTR RUN(L)	Indicates the system processor in the System Controller board is running.
85	GND	Common ground with bus lines 9---10, 15---16, 56, and 97---100.
86	BYTE ADDR(L)	Causes the memory-board address-shifting mechanism to shift the address lines down one bit position.
87	F.P. HOLD(L)	This line is a request to the system processor, indicating a breakpoint or single-step operation.
88	MSTR INTACK(L)	Master interrupt acknowledge.
89	MSTR INT 3(L)	Master interrupt 3.
90	UMAP(L)	Issued by the System Controller board indicating prototype memory mapping.
91	EMUVEN(L)	Enables interrupt vector generated by emulator related hardware.
92	SELF TEST(L)	Used for diagnostic testing.
93	SLV CLK	Clock output from the active emulator processor.
94	I/O CLK	39.06 kHz from the System Controller board.
95	2650 CLK	2 MHz (fast clock) or 1.25 MHz (slow clock) for the system processor.
96	SYS CLK	10 MHz clock from the System Controller board.
97---100	GND	Common ground with bus lines 9---10, 15---16, 56, and 85.

8301 MDU I/O PORT ADDRESS ASSIGNMENTS

The system processor communicates with circuit boards within the 8301 mainframe by means of I/O port addresses. The I/O port addresses are decoded by the circuit board being addressed. The data byte on the data bus associated with this I/O port address contains the communications. Communications take the form of:

- 8-bit parallel data (read or write)
- status information (read)
- control data (write)

The same I/O port address is often used for writing or reading the 8-bit data and another I/O port address used to write the control byte or read the status byte. The I/O port addresses associated with the circuit boards for the standard 8301 configuration are contained in the sections of this manual where the functions of the boards are described. Table 7-2 lists all I/O port addresses associated with the 8301 MDU.

Table 7-2
8301 I/O Port Address Assignments

I/O Port	Read/Write	Function or Device
90	R/W	DMA Controller Channel 0 address register.
91	R/W	DMA Controller Channel 0 terminal count register.
92	R/W	DMA Controller Channel 1 address register.
93	R/W	DMA Controller Channel 1 terminal count register.
94	R/W	DMA Controller Channel 2 address register.
95	R/W	DMA Controller Channel 2 terminal count register.
96	R/W	Not used.
97	R/W	Not used.
98	R/W	DMA Controller control and status.
B8	R/W	Program Memory board relocation control (low board).
B9	R/W	Program Memory board relocation control (high board).

Table 7-2 (cont)

I/O Port	Read/Write	Function or Device
CA	R/W	Remote port -- ACIA control and status.
CB	R/W	Remote port -- ACIA data.
CC	R/W	Auxiliary port -- ACIA control and status.
CD	R/W	Auxiliary port -- ACIA data.
CE	R/W	System terminal -- ACIA control and status.
CF	R/W	System terminal -- ACIA data.
D2	W	System RAM board diagnostic control.
D2	R	Parity error address lower order.
D3	W	System RAM board control.
D3	R	Parity error address higher order.
E7	R/W	Language Processor control and status.
E8	R/W	High-Speed Serial Communications port data.
E9	R/W	High-Speed Serial Communications control and status.
EA	R/W	Manufacturing Test port control and status.
EB	R/W	Manufacturing Test port data.
EC	W	Interval Timer control port.
EC	R	Programmed system processor reset.
ED	W	LED Write port.
ED	R	Switch Read port.
EE	W	Bank Switch.
EF	R	Sync Test port.

Table 7-2 (cont)

I/O Port	Read/Write	Function or Device
F0	R/W	Reserved (decoded but not assigned).
F1	R/W	Reserved (decoded but not assigned).
F2	R	Pending Interrupts port.
F3	W	SVC mapping port.
F4	W	Extended Bank Switch.
F5	W	Jump Address extended.
F6	R	Program Counter Next extended.
F6	W	Breakpoint 1 extended.
F7	R	Program Counter Last extended.
F7	W	Breakpoint 2 extended.
F8	W	Debug control port.
F9	W	Debug command port.
FA	W	Jump Address lower order.
FB	W	Jump Address higher order.
FC	W	Breakpoint 1 lower order.
FC	R	Program Counter Next lower order.
FD	W	Breakpoint 1 higher order.
FD	R	Program Counter Next higher order.
FE	W	Breakpoint 2 lower order.
FE	R	Program Counter Last lower order.
FF	W	Breakpoint 2 higher order.
FF	R	Program Counter Last higher order.

I/O PORT ADDRESSES 90, 92, AND 94 (READ/WRITE)

I/O port addresses 90, 92 and 94 establish the 16-bit starting addresses for DMA Channels 0, 1 and 2 respectively. Each of these ports must be accessed twice to read or write the starting address of the associated DMA Channel. When the port is first accessed, the data byte contains addresses A0--A7. When the port is accessed the second time, the data byte contains addresses A8--A15. Together these two bytes contain the starting address for the associated DMA Channel as follows:

- I/O port addresses ---- 90, 92 and 94 (read/write)
  - 90--Channel 0
  - 92--Channel 1
  - 94--Channel 2

DMA Starting Address

D0--A0/A8
D1--A1/A9
D2--A2/A10
D3--A3/A11
D4--A4/A12
D5--A5/A13
D6--A6/A14
D7--A7/A15

I/O PORT ADDRESSES 91, 93 AND 95 (READ/WRITE)

I/O port addresses 91, 93 and 95 establish the 16-bit terminal count word for DMA Channels 0, 1 and 2 respectively. Each of these ports must be accessed twice to read or write the terminal count word of the associated DMA Channel. When the port is first accessed, the data byte contains the terminal count bits C0--C7. When the port is accessed the second time, the data byte contains the terminal count bits C8--C13, plus one each read and write flag bit. Together these two bytes contain the terminal count word for the associated DMA Channel as follows:

- I/O port addresses ---- 91, 93 and 95 (read/write)
  - 91--Channel 0
  - 93--Channel 1
  - 95--Channel 2

DMA Terminal Count

D0--C0/C8
D1--C1/C9
D2--C2/C10
D3--C3/C11
D4--C4/C12
D5--C5/C13
D6--C6/WRITE
D7--C7/READ

I/O PORT ADDRESS 98

This I/O Port accesses two 8-bit registers. A write to I/O port 98 loads the DMA Mode Register and a read of I/O port 98 reads the DMA Status Register. The information contained in the read and write data bytes is as follows:

- I/O port address ---- 98 (write)

DMA Mode Register

D0--Enables DMA Channel 0 (1=enable)
D1--Enables DMA Channel 1 (1=enable)
D2--Enables DMA Channel 2 (1=enable)
D3--Enables DMA Channel 3 (not used) (set to 0)
D4--Enables rotating priority (1=enable)
D5--Enables extended write (1=enable)
D6--Enables TC stop (1=enable)
D7--Enables Autoload (1=enable)

- I/O port address ---- 98 (read)

DMA Status Register

D0--TC status for Channel 0
D1--TC status for Channel 1
D2--TC status for Channel 2
D3--TC status for Channel 3 (not used)
D4--Update flag
D5--Not used (set to 0)
D6--Not used (set to 0)

D7--Not used (set to 0)

I/O PORT ADDRESSES B8 AND B9 (WRITE)

I/O port address B8 accesses the lower memory board (0000--7FFF) and I/O port address B9 accesses the upper memory board (8000--FFFF). A write to either I/O port address places the first four bits of the control byte (the Physical Address) in the associated memory relocation RAM. The remaining bits in the control byte are used to control associated logic circuits. The information contained in the data byte is as follows:

- I/O port address ---- B8 and B9 (write)

  Low and High Memory Board Control Byte

  D0--PA0
  D1--PA1
  D2--PA2
  D3--PA3
  D4--Relocation Logic (1=disable)
  D5--Counter Reset (1=reset)
  D6--Extended Bank Comparator (1=disable)
  D7--Not used (set to 0)

I/O PORT ADDRESSES B8 AND B9 (READ)

I/O port address B8 accesses the lower memory board and I/O port address B9 accesses the upper memory board. A read from either address retrieves the status byte from the specified memory relocation logic and associated logic circuitry as follows:

- I/O port address ---- B8 and B9 (read)

  Low and High Memory Board Status Byte

  D0--PA0
  D1--PA1
  D2--PA2
  D3--PA3
  D4--Disable Latch status (1=disable)
  D5--Not used
  D6--Extended Bank disable status (1=disable)
  D7--Not used

I/O PORT ADDRESSES CA, CC, AND CE (READ/WRITE)

I/O port addresses CA, CC and CE are used to access the various ACIA ports. When any of these ports are accessed during a write operation, the associated control byte is sent to the Port's ACIA. When these addresses are read, a status byte is received from the associated Port's ACIA. The information contained in the control and status data bytes is as follows: (Refer to the manufacturer's data sheet for more detailed information on the setting of the bits in the control and status bytes.)

- CA--ACIA Remote Communications Port
- CC--ACIA Auxiliary Port
- CE--ACIA System Terminal Port
  - I/O port addresses ---- CA, CC and CE (write)

    ACIA Port Control Byte

    D0--CR0 (Counter Divide Select 1)
    D1--CR1 (Counter Divide Select 2)
    D2--CR2 (Word Select 1)
    D3--CR3 (Word Select 2)
    D4--CR4 (Word Select 3)
    D5--CR5 (Transmitter Control 1)
    D6--CR6 (Transmitter Control 2)
    D7--CR7 (Receive Interrupt Enable)

  - I/O port addresses ---- CA, CC and CE (read)

    ACIA Port Status Byte

    D0--RDRF (Receiver Data Register Full)
    D1--TDRE (Transmit Data Register Empty)
    D2--DCD (Data Carrier Detect)
    D3--CTS (Clear-to-Send)
    D4--FE (Framing Error)
    D5--OVRN (Receiver Overrun)
    D6--PE (Parity Error)
    D7--IRQ (Interrupt Request)

I/O PORT ADDRESSES CB, CD AND CF

A write to I/O port addresses CB, CD and CF loads the data byte into the associated ACIAs transmit data register for transmission to the external peripheral connected to the ACIA port. A read of these I/O port addresses reads the contents of the associated ACIAs receive data register and places the data read on the 8301 data bus.

- CB--ACIA Remote Communications Port
- CD--ACIA Auxiliary Port
- CF--ACIA System Terminal Port
  - I/O port address ---- CB, CD and CF (read/write)

ACIA Data Byte

D0--BD0
D1--BD1
D2--BD2
D3--BD3
D4--BD4
D5--BD5
D6--BD6
D7--BD7

I/O PORT ADDRESS E7

When I/O port address E7 is written to, a control byte is sent to the Language Processor board. The information contained in the data byte is as follows:

- I/O port address ---- E7 (write)

Language Processor Board Control Byte

D0--Not used
D1--Not used
D2--Debug Sequencer (1=clock slow, 0=clock fast)
D3--Not used
D4--Not used
D5--Not used
D6--Not used
D7--Active (1=board active, 0=board inactive)

I/O PORT ADDRESS E8

The HSI port's UART is activated by I/O port addresses E8 and E9. I/O port address E8 permits the system processor to read or write parallel data from/to the UART. A write to I/O port E8 permits the system processor to load parallel data from the data bus into the UARTs transmitter buffer register. The UART converts the parallel data to serial data and transmits it to the DMU.

During a read operation, the UART converts the serial data from the DMU to parallel data and stores it in the UARTs receiver buffer register. A read of I/O port E8 permits the system processor to read the parallel data in the UARTs receiver buffer register.

The data bytes associated with I/O port address E8 for both read and write operations is as follows:

- I/O port address ---- E8 (read/write)

  HSI Parallel Data Byte

  D0--D0
  D1--D1
  D2--D2
  D3--D3
  D4--D4
  D5--D5
  D6--D6
  D7--D7

I/O PORT ADDRESS E9

I/O port address E9 provides control of the HSI UART and DMA ports during a write operation and the status of the ports during a read operation. The information contained in the control and status bytes is as follows:

- I/O port address ---- E9 (write)

HSI Port Control Byte

D0--DMA Channel 0 - Memory-to-Memory Read
(0=program memory, 1=system memory)
D1--HSIN (High-speed Serial In) Interrupt Enable
(1=enable)
D2--HSO (High-speed Serial Out) Interrupt Enable
(1=enable)
D3--DENBL (DMA Interrupt Enable)
(1=enable)
D4--DMAR (DMA Read Enable)(from memory)
(1=enable)
D5--DMAW (DMA Write Enable)(to memory)
(1=enable)
D6--DMA Channel 1 - Memory-to-Memory Write
(0=program memory, 1=system memory)
D7--DMA Channel 2 - DMA-to-HSI Read/Write
(0=program memory, 1=system memory)

- I/O port address ---- E9 (read)

HSI Port Status Byte

D0--DA (HSI Data Available)
(1=data available)
D1--TBRE (HSI Transmit Buffer Register Empty)
(1=buffer empty)
D2--OE (Overrun Error)
(1=error)
D3--FE (Framing Error)
(1=error)
D4--PE (Parity Error)
(1=error)
D5--Receive Error Flag
(1=error received)
D6--Self Test LED (Front Panel)
D7--HSI Port CTS Flag
(1=clear-to-send)

I/O PORT ADDRESS EA

I/O port address EA provides control and status of the 8-bit Parallel Test Port. During a write operation the control byte is clocked into an 8-bit latch. During a read operation the status byte is gated onto the data bus. The information in the control and status bytes is as follows:

- I/O port address ---- EA (write)

  Parallel Test Port Control Byte

  D0--STRB
  D1--C0
  D2--C1
  D3--UM/WP ENBL (1=enable)
  D4--DISC INTRPT ENBL (1=enable)
  D5--BOOT ROM ENB1 (0=enable)
  D6--DIAG ROM ENBL (1=enable)
  D7--WR PTCT INTRPT ENBL (1=enable)

- I/O port address ---- EA (read)

  Parallel Test Port Status Byte

  D0--Not used
  D1--Not used
  D2--Not used
  D3--Not used
  D4--Not used
  D5--Not used
  D6--Not used
  D7--Disc Flag=1

I/O PORT ADDRESS EB

During a write operation the associated data byte of I/O port address EB contains the 8-bit parallel data for the Parallel Test Port. During a read operation the 8-bit parallel data is gated onto the system data bus. The information contained in the data bytes is as follows:

- I/O port address ---- EB (write)

  Parallel Test Port Data Output

  D0--D0D0
  D1--D0D1
  D2--D0D2
  D3--D0D3
  D4--D0D4
  D5--D0D5
  D6--D0D6
  D7--D0D7

- I/O port address ---- EB (read)

  Parallel Test Port Data Input

  D0--DID0
  D1--DID1
  D2--DID2
  D3--DID3
  D4--DID3
  D5--DID5
  D6--DID6
  D7--DID7

I/O PORT ADDRESS EC

I/O port address EC is used to enable/disable the interval timer and to reset the 2650A-1 microprocessor. A write to this port enables or disables the interval timer by setting the correct bits in the data byte. A read of this port resets the 2650A-1 (the associated data byte is disregarded).

- I/O port address ---- EC (write)

  Interval Timer Enable Byte

  D0--Interval Timer (1=enabled, 0=disabled)
  D1--Not used
  D2--Not used
  D3--Not used
  D4--Not used
  D5--Not used
  D6--Not used
  D7--Not used

- I/O port address ---- EC (read)

  Associated data byte not used

I/O PORT ADDRESS ED

I/O port address ED is used to display the status and error code messages from the ROM-Based Diagnostic (Power-Up) tests on six LEDs. This port is also used to determine the positions of the 6-bit DIP switch used during the power-up tests. When this port is written to the associated data byte is used to enable or disable the six LEDs. When this port is read the logic states of the 6-bit DIP switch are forced onto the data bus. The information in the data bytes is as follows:

- I/O port address ---- ED (write)

    LED Display Port

    D0--LED 0 (1=enabled)
    D1--LED 1 (1=enabled)
    D2--LED 2 (1=enabled)
    D3--LED 3 (1=enabled)
    D4--LED 4 (1=enabled)
    D5--Front Panel LED (self test)(1=enabled)
    D6--Not used
    D7--Not used

- I/O port address ---- ED (read)

    Power-Up Mode Switch Port

    D0--Not used
    D1--Not used
    D2--Switch position 1 (1=Open or Off)
    D3--Switch position 2 (1=Open or Off)
    D4--Switch position 3 (1=Open or Off)
    D5--Switch position 4 (1=Open or Off)
    D6--Switch position 5 (1=Open or Off)
    D7--Switch position 6 (1=Open or Off)

I/O PORT ADDRESS EE

I/O port EE is the Bank Switching port. A write to this I/O port determines which 16K memory block is accessed, selects system or program memory, and enables or disables the MAPEN(H) signal to memory map/write protect circuitry. The information contained in the data byte is as follows:

- I/O port address ---- EE (write)

    Bank Switching Byte

    D0--Address Bit BA14
    D1--Address Bit BA15
    D2--CMEM(H) (1=system memory 0=program memory)
    D3--MAPEN(H) (1=enable)
    D4--Not used
    D5--Not used
    D6--Not used
    D7--Not used

The states of BA14 and BA15 determine which 16K block of memory is accessed, as follows:

BA15	BA14	Memory selected
0	0	0000---3FFF
0	1	4000---7FFF
1	0	8000---BFFF
1	1	C000---FFFF

I/O PORT ADDRESS EF

I/O port EF is the Sync I/O port. This port is used for test purposes during a read operation. When I/O port EF is read, the control line SYNC(L) goes low. This control line can then be tested at TP-2. The data on the data bus is disregarded.

I/O PORT ADDRESS F2

I/O port address F2 provides access to the Interrupt Pending Register on the Emulator Controller board. This register contains the status of the eight interrupts that are generated on the Emulator Controller board. The information contained in the data byte is as follows:

- I/O port address ---- F2 (read)

  Interrupt Pending Register

  D0--Interrupt 31
  D1--Interrupt 30
  D2--Interrupt 29
  D3--Diagnostics
  D4--Emulator Halt
  D5--Single-cycle
  D6--BP2
  D7--BP1

I/O PORT ADDRESS F3

I/O port address F3 provides access to the SVC Mapping Register. This register allows emulator processor SVCs to be mapped to any address between 0000 and 00FF on even 16-byte boundaries. The information contained in the data byte is as follows:

- I/O port address ---- F3 (write)

  SVC Mapping Register

  D0--SVC0(H)
  D1--SVC1(H)
  D2--SVC2(H)
  D3--SVC3(H)
  D4--Not used
  D5--Not used
  D6--Not used
  D7--Not used

I/O PORT ADDRESS F4

I/O port address F4 provides access to the Extended Bank Switch Register. The system processor writes the upper eight bits of an extended bank address into this register. The information contained in the data byte is as follows:

- I/O port address ---- F4 (write)

  Extended Bank Switch Register

  D0--A16
  D1--A17
  D2--A18
  D3--A19
  D4--A20
  D5--A21
  D6--A22
  D7--A23

I/O PORT ADDRESS F5

I/O port address F5 provides access to the Extended Jump Address Register. When JMP ADR EXTD(L) is asserted, the system processor writes an 8-bit extended jump address into this register. The information contained in the data byte is as follows:

- I/O port address ---- F5 (write)

  Extended Jump Address Register

  D0--JA16
  D1--JA17
  D2--JA18
  D3--JA19
  D4--JA20
  D5--JA21
  D6--JA22
  D7--JA23

I/O PORT ADDRESS F6

I/O port address F6 provides access to the BP1 Extended Address Register during a write operation and permits reading the PC Next Extended Address Register during a read operation.

A write to I/O port F6 loads the BP1 Extended Address Register. This register is compared to each program address. When a program address is equal to the contents of the BP1 Extended Address Register, an interrupt is issued for breakpoint 1.

A read to I/O port F6 accesses the PC Next Extended Address Register. When the system processor reads this register, the PC NEXT EXTD(L) signal goes low and the address of the next program instruction is forced onto the data bus.

The information contained in the data bytes is as follows:

- I/O port address ----F6 (write)

  BP1 Extended Address Register

  D0--BA1-16
  D1--BA1-17
  D2--BA1-18
  D3--BA1-19
  D4--BA1-20
  D5--BA1-21
  D6--BA1-22
  D7--BA1-23

- I/O port address ---- F6 (read)

    PC Next Extended Address Register

    D0--PCN-16
    D1--PCN-17
    D2--PCN-18
    D3--PCN-19
    D4--PCN-20
    D5--PCN-21
    D6--PCN-22
    D7--PCN-23

I/O PORT ADDRESS F7

I/O port address F7 provides access to the BP2 Extended Address Register during a write operation and permits reading the PC Last Extended Address Register during a read operation.

A write to I/O port F7 loads the BP2 Extended Address Register. This register is compared to each program address. When a program address is equal to the contents of the BP2 Extended Address Register, an interrupt is issued for breakpoint 2.

A read to I/O port F7 accesses the PC Next Extended Address Register. When the system processor reads this register, the PC LAST EXTD(L) signal goes low and the address of the last program instruction is forced onto the data bus.

The information contained in the data bytes is as follows:

- I/O port address ---- F7 (write)

    BP2 Extended Address Register

    D0--BA2-16
    D1--BA2-17
    D2--BA2-18
    D3--BA2-19
    D4--BA2-20
    D5--BA2-21
    D6--BA2-22
    D7--BA2-23

- I/O port address ---- F7 (read)

    PC Last Extended Address Register

    D0--PLC-16
    D1--PLC-17
    D2--PLC-18
    D3--PLC-19
    D4--PLC-20
    D5--PLC-21
    D6--PLC-22
    D7--PLC-23

I/O PORT ADDRESS F8

I/O port F8 is the Debug Control Port. When this port is written to, the OUT CNTRL(L) signal goes low, and the lower five bits of the data bus are forced into the breakpoint register. The information contained in the data byte is as follows:

- I/O port address ---- F8 (write)

    Debug Control Byte

    D0--B1R - Enable BP1 on read (0=enable)
    D1--B1W - Enable BP1 on write (0=enable)
    D2--B2R - Enable BP2 on read (0=enable)
    D3--B2W - Enable BP2 on write (0=enable)
    D4--S/CY - Enable single-cycle (0=enable)
    D5--Not used
    D6--Not used
    D7--Not used

I/O PORT ADDRESS F9

I/O port F9 is the Debug Command Port. When this port is written to, the OUT CMD(L) signal goes low, and the lower five bits of the data bus act as control signals and are sent to four flip-flops and a NAND gate. The information contained in the data byte is as follows:

- I/O port address ---- F9 (write)

    Debug Command Byte

    D0--FR - Forced reset (0=reset enable)
    D1--FI - Forced interrupt (0=enable)
    D2--FJ - Forced jump (0=enable)
    D3--IM - Mask debug interrupts (0=enable)
    D4--SVC - Enable SVC (1=enable)
    D5--SE - Sequence Enable (0=enable)
    D6--Not used
    D7--Not used

I/O PORT ADDRESS FA

I/O port address FA provides access to the Low-Order Jump Address Register. When I/O port FA is written to, the JMP ADR LO(L) signal goes low, and the states of each bit of the data bus are stored in this register as the low-order byte of a forced jump address. The information contained in the data byte is as follows:

- I/O port address ---- FA (write)

    Lo-Order Jump Address Register

    D0--JA0
    D1--JA1
    D2--JA2
    D3--JA3
    D4--JA4
    D5--JA5
    D6--JA6
    D7--JA7

I/O PORT ADDRESS FB

I/O port address FB permits access to the High-Order Jump Address Register. When I/O port FB is written to, the JMP ADR HI(L) signal goes low, and the states of each bit of the data bus are stored in this register as the High-Order byte of a forced jump address. The information contained in the data byte is as follows:

- I/O port address ---- FB (write)

  High-Order Jump Address Register

  D0--JA8
  D1--JA9
  D2--JA10
  D3--JA11
  D4--JA12
  D5--JA13
  D6--JA14
  D7--JA15

I/O PORT ADDRESS FC

I/O port address FC provides access to the BP1 Low-Order Address Register during a write operation and to the PC Next Low-Order Address Register during a read operation.

A write to I/O port FC loads the BP1 Low-Order Address Register. The contents of this register are compared to the least significant byte of each program address. When the least significant byte of a program address is equal to the contents of the BP1 Low-Order Address Register, an interrupt is issued for breakpoint 1.

A read of I/O port FC accesses the PC Next Low-Order Address Register. When the system processor reads this register, the PC NEXT LO(L) signal goes low, and the Low-Order address of the next program instruction is forced onto the data bus.

The information contained in the read and write data bytes is as follows:

- I/O port address ---- FC (write)

  BP1 Low-Order Address Register

  D0--BA1-0
  D1--BA1-1
  D2--BA1-2
  D3--BA1-3
  D4--BA1-4
  D5--BA1-5
  D6--BA1-6
  D7--BA1-7

- I/O port address ---- FC (read)

  PC Next Low-Order Address Register

  D0--PCN0
  D1--PCN1
  D2--PCN2
  D3--PCN3
  D4--PCN4
  D5--PCN5
  D6--PCN6
  D7--PCN7

I/O PORT ADDRESS FD

I/O port address FD provides access to the BP1 High-Order Address Register during a write operation and to the PC Next High-Order Address Register during a read operation.

A write to I/O port FD loads the BP1 High-Order Address Register. The contents of this register are compared to the most significant byte of each program address. When the most significant byte of a program address is equal to the contents of the BP1 High-Order Address Register, an interrupt is issued for breakpoint 1.

A read of I/O port FD accesses the PC Next High-Order Address Register. When the system processor reads this register, the PC NEXT HI(L) signal goes low, and the most significant byte of the address of the next program instruction is forced onto the data bus.

The information contained in the read and write data bytes is as follows:

- I/O port address ---- FD (write)

  BP1 High-Order Address Register

  D0--BA1-8
  D1--BA1-9
  D2--BA1-10
  D3--BA1-11
  D4--BA1-12
  D5--BA1-13
  D6--BA1-14
  D7--BA1-15

- I/O port address ---- FD (read)

  PC Next High-Order Address Register

  D0--PCN8
  D1--PCN9
  D2--PCN10
  D3--PCN11
  D4--PCN12
  D5--PCN13
  D6--PCN14
  D7--PCN15

I/O PORT ADDRESS FE

I/O port address FE provides access to the BP2 Low-Order Address Register during a write operation and to the PC Last Low-Order Address Register during a read operation.

A write to I/O port FE loads the BP2 Low-Order Address Register. The contents of this register are compared to the least significant byte of each program address. When the least significant byte of a program address is equal to the contents of the BP2 Low-Order Address Register, an interrupt is issued for breakpoint 2.

A read of I/O port FE accesses the PC Last Low-Order Address Register. When the system processor reads this register, the PC LAST LO(L) signal goes low and the least significant byte of the address of the next program instruction is forced onto the data bus.

The information contained in the read and write data bytes is as follows:

- I/O port address ---- FE (write)

  BP2 Low-Order Address Register

  D0--BA2-0
  D1--BA2-1
  D2--BA2-2
  D3--BA2-3
  D4--BA2-4
  D5--BA2-5
  D6--BA2-6
  D7--BA2-7

- I/O port address ---- FE (read)

  PC Last Low-Order Address Register

  D0--PCL0
  D1--PCL1
  D2--PCL2
  D3--PCL3
  D4--PCL4
  D5--PCL5
  D6--PCL6
  D7--PCL7

I/O PORT ADDRESS FF

I/O port address FF provides access to the BP2 High-Order Address Register during a write operation and to the PC Last High-Order Address Register during a read operation.

A write to I/O port FF loads the BP2 High-Order Address Register. The contents of this register is compared to the most significant byte of each program address. When the most significant byte of a program address is equal to the contents of the BP2 High-Order Address Register, an interrupt is issued for breakpoint 2.

A read of I/O port FF accesses the PC Last High-Order Address Register. When the system processor reads this register, the PC LAST HI(L) signal goes low and the most significant byte of the address of the next program instruction is forced onto the data bus.

The information contained in the read and write data bytes is as follows:

- I/O port address ---- FF (write)

  BP2 High-Order Address Register

  D0--BA2-8
  D1--BA2-9
  D2--BA2-10
  D3--BA2-11
  D4--BA2-12
  D5--BA2-13
  D6--BA2-14
  D7--BA2-15

- I/O port address ---- FF (read)

    PC Last High-Order Address Register

    D0--PCL8
    D1--PCL9
    D2--PCL10
    D3--PCL11
    D4--PCL12
    D5--PCL13
    D6--PCL14
    D7--PCL15

I/O PORT ADDRESSES D2 AND D3 (WRITE)

When I/O port addresses D2 or D3 are written to, a control byte is sent to the System RAM board. The control byte of D2 is used by the diagnostic programs to check various functions on the System RAM board. The data byte controls the refresh interrupt, parity error interrupt, and parity complement. In addition, five bits from the control byte are used to turn five LED indicators OFF or ON. The associated control byte of D3 is used for paging selections. The information contained in the control bytes is as follows:

- I/O port address ---- D2 (write)

    Diagnostic Control Byte

    D0--Refresh Interrupt Enable (1=enable)
    D1--Parity Error (1=enable)
    D2--Parity Complement (1=complement)(0=true parity)
    D3--Diagnostic LED (1=off)
    D4--Diagnostic LED (1=off)
    D5--Diagnostic LED (1=off)
    D6--Diagnostic LED (1=off)
    D7--Diagnostic LED (1=off)

    NOTE

    All bits are set to zero at power-up.

- I/O port address ---- D3 (write)

  System RAM Control Byte

  D0--Not used
  D1--Not used
  D2--Not used
  D3--Not used
  D4--Not used
  D5--A13 (To Paging Switch)
  D6--A14 (To Paging Switch)
  D7--A15 (To Paging Switch)

I/O PORT ADDRESSES D2 AND D3 (READ)

I/O port addresses D2 and D3 accesses the parity error address latches on the System RAM board. A read from address D2 enables the lower order address latch and forces the low-order parity error address onto the data bus. A read from address D3 enables the higher order address latch and forces the high-order parity error address onto the data bus.

The information contained in the read data bytes is as follows:

- I/O port address ---- D2 (read)

  Low-Order Parity Error Address

  D0--A0
  D1--A1
  D2--A2
  D3--A3
  D4--A4
  D5--A5
  D6--A6
  D7--A7

- I/O port address ---- D3 (read)

  High-Order Parity Error Address

  D0--A8
  D1--A9
  D2--A10
  D3--A11
  D4--A12
  D5--A13
  D6--A14
  D7--A15

Section 8

MAINTENANCE

INTRODUCTION

This section describes procedures for preventing or reducing equipment malfunction, includes techniques and aids for troubleshooting, and contains disassembly instructions and calibration procedures for the power supplies. Preventive maintenance improves equipment reliability. Should the equipment fail to operate properly, corrective measures should be taken immediately; otherwise, additional problems may develop within the equipment.

STATIC-SENSITIVE DEVICES

1. Minimize the handling of static-sensitive parts.

2. Transport and store static-sensitive parts in their original containers, on a metal rail, or on conductive foam. Label any container having a static-sensitive assembly or device.

3. Discharge the static charge on yourself by using a wrist strap before handling these devices. It is recommended that servicing of static-sensitive assemblies or devices be performed only at a static-free work station by qualified personnel.

4. Do not allow anything capable of generating or holding a static charge onto the work station surface.

5. Keep the leads shorted together whenever possible.

6. Pick up the part by the body, never by the leads.

7. Do not subject the part to sliding movements over any surface.

8. Avoid handling parts in areas having a floor or work surface covering that contributes to the generation of a static charge.

9. Use a soldering iron that has a connection to earth ground.

10. Use a special anti-static suction-type desoldering tool, such as the Silverstat Soldapulit, or a wick-type desoldering tool.

REDUCING SUSCEPTIBILITY TO STATIC DISCHARGE

TEKTRONIX microprocessor emulation systems provide a number of safeguards to reduce the chance of static discharge damage.

CAUTION

Violation or modification of the following safeguards can result in ground loops and/or static discharge problems.

1. The ground (earth) wire of the primary power cable is connected to the chassis where the cable enters the unit.

2. The shields of interconnecting EIA cables are grounded to the chassis at the cable entrance or egress of each unit.

3. All interconnecting ribbon cables have a built-in ground plane which is grounded to the chassis at the cable entrance or egress of each unit.

4. Ground loops have been avoided by installing a common ground between all units. Grounding straps are utilized where necessary. Refer to your 8550 MDL Installation Guide.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, and performance checks. The preventive maintenance schedule established for the equipment should be based on the amount of use, and on the environment in which the equipment is operated.

CLEANING

Clean the equipment often enough to prevent dust or dirt from accumulating in or on it. Dirt acts as a thermal insulator and prevents efficient heat dissipation. It also provides high-resistance electrical leakage paths between conductors or components in a humid environment.

CAUTION

Do not allow water to get inside any enclosed assembly or components, such as switch assemblies, potentiometers, etc. Do not clean any plastic materials with organic cleaning solvents (such as benzene, toluene, xylene, acetone, or similar compounds); they may damage the plastic.

Exterior

Clean the dust from the outside of the equipment by cleaning the surface with a soft cloth or brush. The brush will remove dust from around the front panel selector buttons. Hardened dirt may be removed with a cloth dampened in water that contains a mild detergent. Abrasive cleaners should not be used.

Interior

Clean the interior by loosening accumulated dust with a dry, soft brush, then blow the loosened dirt away with low-pressure air. If the circuit board assemblies need cleaning, remove the circuit board and clean with a dry, soft brush. Hardened dirt or grease may be removed with a cotton-tipped applicator dampened with a solution of mild detergent and water. Abrasive cleaners should not be used.

After cleaning, allow the interior to dry thoroughly before applying power to the equipment.

VISUAL INSPECTION

After cleaning, carefully check the equipment for such defects as defective connections and damaged parts. The remedy for most visible defects is obvious. If heat-damaged parts are discovered, try to determine the cause of overheating before replacing the damaged part; otherwise, the damage may be repeated.

TROUBLESHOOTING

Your Tektronix Service Support Center is best suited to perform repairs on this unit. However, the following general troubleshooting procedures may aid you in tracing a problem to its source.

Before beginning any troubleshooting work, check your warranty or service agreement. To prevent voiding the warranty, all service must be performed by Tektronix, Inc. for the first 90 days following delivery.

GENERAL

1. Check that all cabling is installed properly.

2. Verify that the system terminal is operating correctly.

3. Check that the Emulator Controller board is in the correct slot (J5 on the Main Interconnect board).

4. After shutting off primary power to the system, remove all

circuit boards from the Main Interconnect board. Clean each boards' edge connector and replace the boards in the Main Interconnect board.

5. Check all power supply levels (these levels are usually accessible at test points on each board).

6. If a duplicate set of boards is available, try swapping the boards, one by one, to find the defective board.

8301 WILL NOT BOOT FROM 8501

With the 8550 MDL DOS/50 Disc properly installed in the 8501, press both 8301 and 8501 RESTART switches. The operating system should boot from the disc into the 8301 System Memory. If it does not, check the following:

1. The power-up tests for both 8301 and 8501 must be passed before the operating system can boot. Check the system terminal for messages ("8301 BOOT" and "8501 BOOT") indicating the units have passed their power-up tests (ROM-Based Diagnostics). If these messages are not displayed, refer to the ROM-Based Diagnostic sections in the appropriate service manuals.

2. If both messages are displayed and the operating system has not booted, try using another Operating System Disc.

3. If it still will not boot, remove the DOS/50 Disc and replace it with the 8550 Disc-Based Diagnostic Disc. Refer to Section 4 in this manual for information and instructions on using this disc.

TROUBLESHOOTING AIDS

Diagrams

Circuit diagrams are given on foldout pages in the Diagrams section, Volume II of this manual. The circuit number and electrical value of each component are shown on the diagram. (See the first tab page for definition of the symbols used to identify components in each circuit.) Components on circuit boards are assigned vertical and horizontal grid numbers which correspond to the location of the component on the circuit board. Refer to the Replaceable Electrical Parts List section for a complete description of each component and assembly. Those portions of the circuit that are on circuit boards are enclosed with a black border line, with the name and assembly number shown on the border.

NOTE

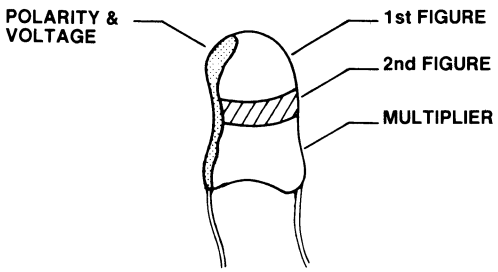
Corrections and modifications to the manual and equipment are described on inserts bound into the rear of the manual. Check this Change Information section for manual or instrument changes and corrections.

Capacitor Marking

The capacitance value of common disc capacitors and some electrolytics is marked in microfarads on the side of the component body. The white ceramic capacitors are color-coded in picofarads. Tantalum capacitors are color-coded as shown in Fig. 8-1.

Diode Code

The cathode of each glass-encased diode is indicated by a stripe, a series of stripes, or a dot. Some diodes have a diode symbol printed on one side. Figure 8-2 illustrates diode types and polarity markings that are used in this equipment.



DIPPED TANTALUM CAPACITOR MARKING

A AND B CASE
CAPACITANCE AND VOLTAGE COLOR CODE

RATED VOLTAGE VDC 25°C	COLOR	CODE FOR CAPACITANCE IN PICOFARADS		
		1st FIGURE	2nd FIGURE	MULTIPLIER
3-4	BLACK	0	0	NONE
3-6	BROWN	1	1	X10
3-10	RED	2	2	$X10^2$
3-15	ORANGE	3	3	$X10^3$
3-20	YELLOW	4	4	$X10^4$
3-25	GREEN	5	5	$X10^5$
3-35	BLUE	6	6	$X10^6$
3-50	VIOLET	7	7	$X10^7$
	GRAY	8	8	
3	WHITE	9	9	

2353-65

Fig. 8-1 Tantalum capacitor color code.

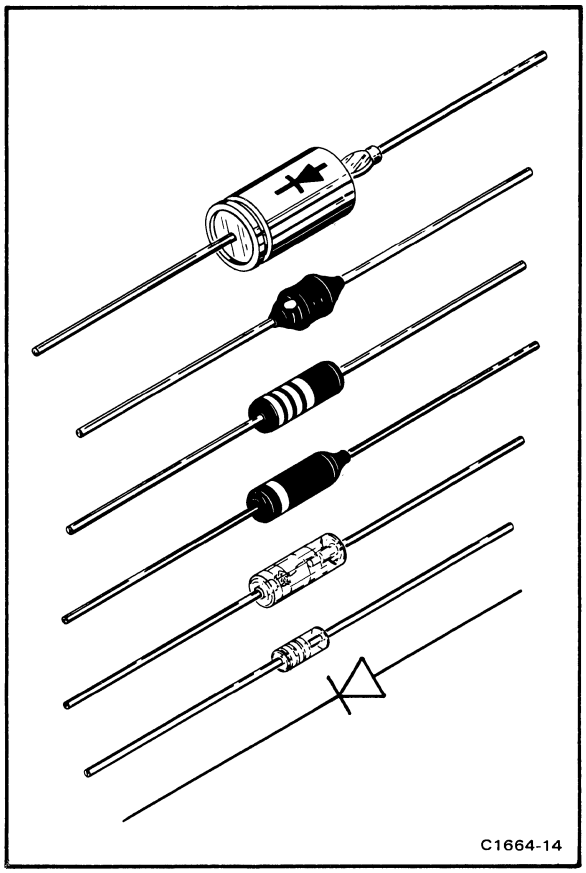


Fig. 8-2 Diode polarity marking.

Transistor and Integrated Circuit Pin Configuration

Lead identification for the transistors is shown in Fig. 8-3. IC pin arrangement diagrams are shown, when necessary, on the back of the foldout schematic diagram.

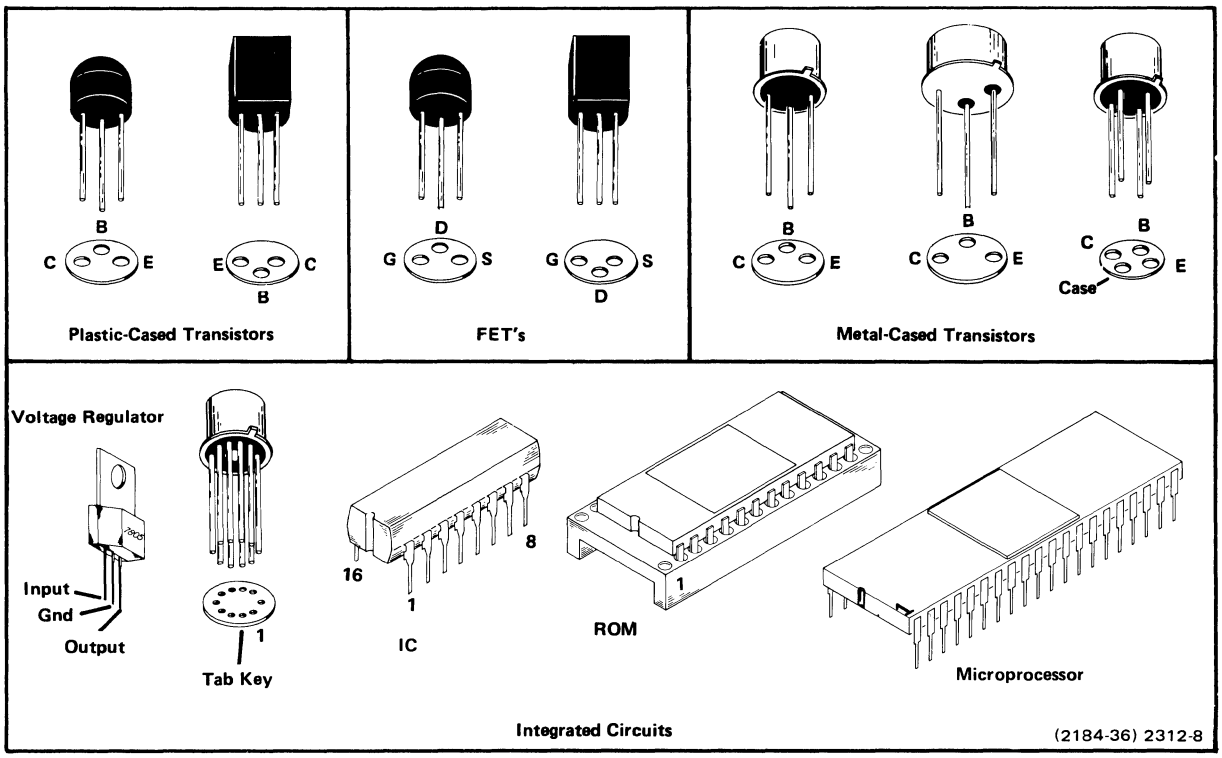


Fig. 8-3 Pin configurations for semiconductor components.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts are available through your local Tektronix Field Office or representative. The Replaceable Electrical and Mechanical Parts List sections contain information on how to order these replacement parts. Many standard electronic components can be obtained locally in less time than required to order from Tektronix, Inc. It is best to duplicate the original component as closely as possible. Parts orientation and lead dress should be duplicated, since orientation may affect circuit interaction.

If a component you have ordered has been replaced with a new or improved part, your local Field Office or representative will contact you concerning the change in the part number.

PARTS REPAIR AND EXCHANGE PROGRAM

Tektronix service centers provide replacement or repair service on major assemblies, in addition to the unit itself. Contact your local service center for this service.

PREPARING THE 8301 FOR SERVICING POWER SUPPLIES

The 8301 must be powered-down and the top cover removed to inspect, remove and replace, or calibrate the power supplies. The top cover is a flat metal sheet with a small flange angled downward at its rear edge. The cover fits into two grooves along the top of the chassis. Two plastic retainers at the rear of the cover hold it in place. The retainers are fastened to the rear panel with screws. To take off the top cover, first ensure that power to the 8301 is OFF, then remove the screws and retainers as shown in Fig. 8-4. Slide the top cover to the rear of the instrument and lift it away.

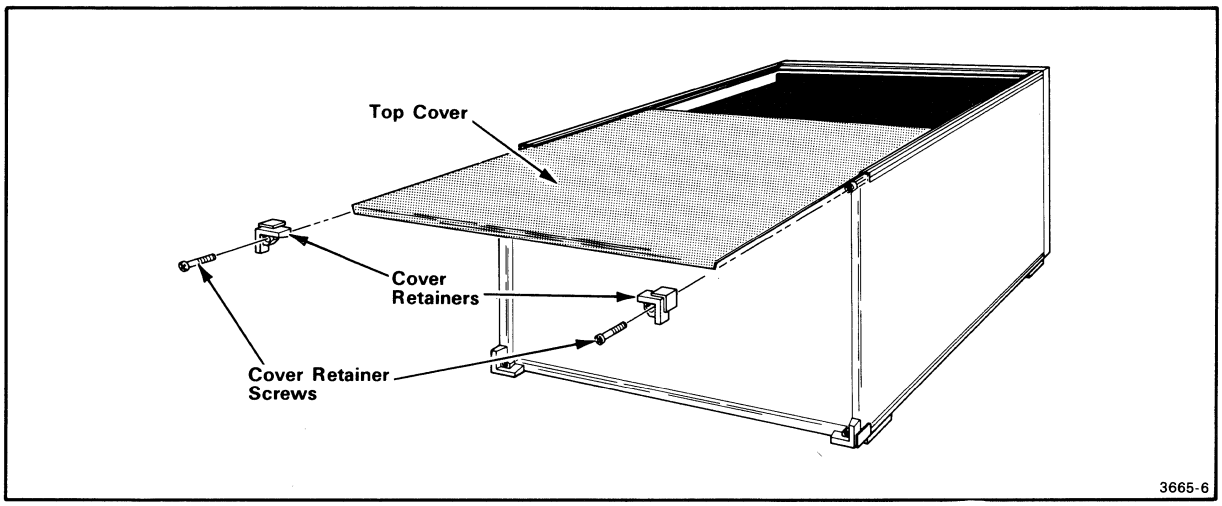


Fig. 8-4. Removing the 8301 Top Cover.

REMOVING THE POWER SUPPLIES

The 8301 contains three DC power supplies, located at the rear of the chassis. The two 12 Vdc supplies are mounted side by side, against the rear of the card cage. The 5 Vdc supply is fastened to the bottom of the chassis, next to the 12 Vdc units. Use the following procedure to remove any or all supplies.

REMOVAL OF ANY POWER SUPPLY

1. Disconnect the power cord from the 8301 chassis, then remove the unit's top cover as previously explained.

2. The optional Data Acquisition Interface board (DAIB) is shown in Fig. 8-5. It is held to the 8301 back panel by four screws. If this option is installed, locate and remove the DAIB. When removing the ribbon cable and connector attached to the DAIB, handle it carefully to avoid damaging the cable connecting to the Real Time Trace board (RTT).

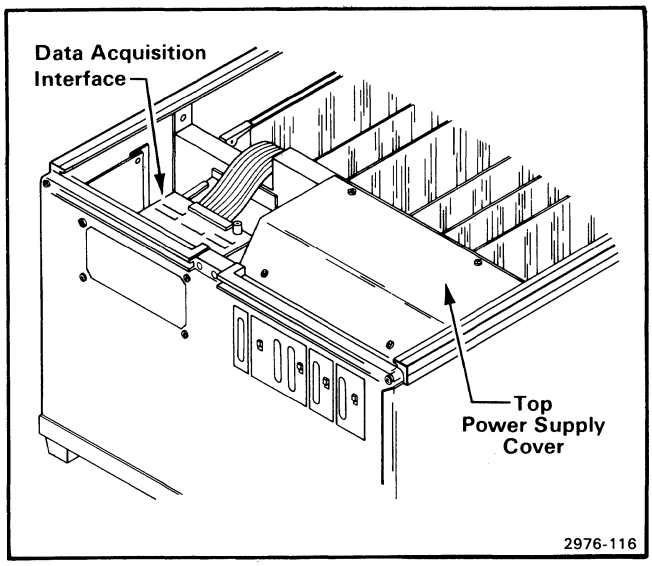


Fig. 8-5. 8301 with top cover removed.

3. Remove all circuit boards from the 8301 card cage.

CAUTION

Exercise extreme care when handling these circuit boards. Avoid flexing the boards and do NOT stack them on each other. Store them in a temporary location away from heat, liquids, and dust.

4. Locate and remove the power supply cover shown in Fig. 8-5. It is held by four screws. All three power supplies are now visible. The -/+12 Vdc supplies are mounted together, against the rear of the card cage. The +5 Vdc unit is mounted on the bottom of the chassis.

5. Locate and remove the smaller half of the power supply cover shown in Fig. 8-6. It is held by two screws through the 8301 rear panel.

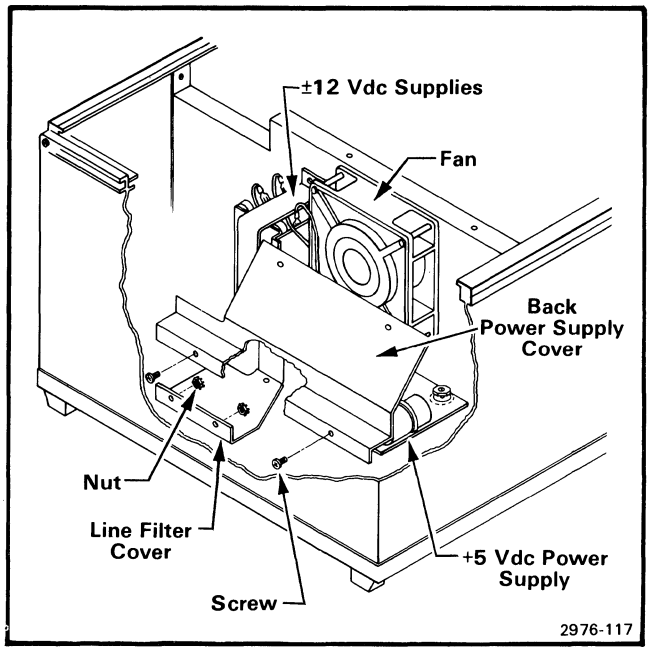


Fig. 8-6. 8301 Power Supplies.

6. Locate and remove the line filter cover shown in Fig. 8-6. It is held by two nuts and one screw. As you remove the cover, avoid damaging the wiring directly above it.

REMOVAL OF 12 VDC POWER SUPPLIES

NOTE

The next two steps in this procedure explains the removal of either 12 Vdc supply. If you wish to remove only the +5 Vdc supply, skip to step 9.

7. Both 12 Vdc power supplies are protected by a metal bracket. The bracket is held by three screws. Locate and remove the bracket.

CAUTION

Several wires interconnect the two 12 Vdc power supplies. To remove either supply, you may need to disconnect the wires from both supplies. As you remove the wires, label them to avoid later confusion.

8. Each 12 Vdc power supply is held by two screws accessible through the card cage. As you face the front of the 8301, the +12 Vdc supply is on your left. Remove the appropriate unit. Refer to the replacement instructions for tips on reassembling the equipment.

REMOVAL OF 5 VDC POWER SUPPLY

NOTE

The following instructions pertain to the removal of the +5 Vdc power supply only.

9. The fan located above the +5 Vdc supply is held by four screws and four tubular spacers. Remove the fan and lay it aside. Avoid damaging the fan's wires. Don't lose the spacers.

10. The 8301 rear panel must be removed. Figure 8-7 shows the screws that must be removed. Remove the screws in the rear panel. When the panel is loose, disconnect any remaining wiring and lay the panel carefully aside.

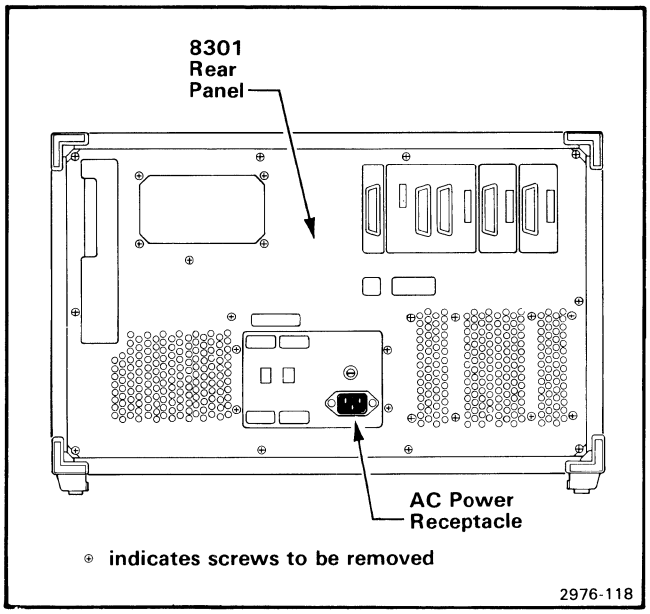


Fig. 8-7. 8301 Rear Panel.

11. The ac power cord receptacle is mounted on the bracket shown in Fig. 8-7. The bracket is held to the chassis by two screws along the lower edge. Remove the screws and swing the bracket aside. Avoid damaging the wiring.

12. Six screws fasten the +5 Vdc power supply to the bottom of the 8301 chassis. Locate and remove the screws.

13. Loosen and remove the wiring from the +5 Vdc supply. Label each wire or make a simple diagram for reference during replacement.

14. Remove the +5 Vdc power supply.

This concludes the power supply removal procedures.

REPLACING THE POWER SUPPLIES

To replace a power supply, reverse the removal instructions. The following list gives several replacement hints:

- When installing a 12 Vdc power supply, exercise extreme care to avoid pinching wires against the card cage or beneath the supply.
- When reinstalling the fan, first install both lower screws and spacers in the fan housing, then position the fan on the card cage and tighten the screws. Finish by installing the two remaining spacers and screws.
- The +5 Vdc supply wiring may carry 35 Amps during operation. Ensure that the wiring is properly installed and dressed to avoid short circuiting.

CHECKOUT/CALIBRATION PROCEDURES FOR POWER SUPPLIES

CAUTION

These power supplies are adjusted to conform to UL specifications and the appropriate adjustment pots sealed. This section includes calibration routines for readjustment of the supplies. If you service these supplies, or replace any components, perform the calibration routines carefully to ensure that the supply operates within UL specifications. Avoid power supply adjustments whenever possible.

Use these routines to check & calibrate the 8301 DC power supplies. Each routine is dependent upon the previous ones; perform them in the order listed. The routines specify a variac; if one is not available, ensure that the 8301 is receiving the specified ac power and that the voltage selection switches (on the 8301 rear panel) are set accordingly.

Several routines direct you to connect a load to the power supply output terminals. Ensure that the load's wiring and connectors have the appropriate current ratings. Do NOT connect a single, large load directly to the bus

(100-pin connectors on the Main Interconnect board). Uneven current distribution on the bus (100-pin connectors) may damage the Main Interconnect board. Large loads must be evenly distributed across the 100-pin connectors.

The 8301 power supplies should not be allowed to exceed normal operating temperatures for long periods of time. These routines involve removing the ductwork which routes airflow to the supplies. Perform the routines quickly to avoid overheating the supplies.

NOTE

The following procedures apply to a primary input voltage of either 115 or 230 volts. Where the procedures are different the 230 volt application is included in parentheses.

TEST EQUIPMENT REQUIRED

The following test equipment is required to perform the calibration procedures for the power supplies:

Variac	A general purpose variac capable of providing 0 to 132 Vac (0 to 250 Vac) depending on the normal ac supply voltage to the 8301.
DMM	A Digital Multimeter capable of resistance measurements of 1 ohm +/- 0.1 ohm and 0.1% DC voltage accuracy (TEKTRONIX DM 502 or equivalent).
Oscilloscope	General purpose capable of measuring 10, 50, and 120 mV p-p ripple voltages (TEKTRONIX 400- or 7000-Series Oscilloscopes or equivalent).
Dummy Loads	The following dummy loads to be fabricated locally:

- Two 1.7 amp loads for 12.0 Vdc.
- One 2.0 amp load for 12.0 Vdc.
- One 35.0 amp load for 5-2 Vdc.

PRIMARY AC VOLTAGE INPUT CHECK

Perform this routine if the power supplies are new or in unknown condition. This procedure checks the ac input wiring, line voltage selection switches, the primary side of transformer, and the basic integrity of the three DC power supplies. Figure 8-8 shows the power cord receptacle on the 8301 rear panel and identifies the pins.

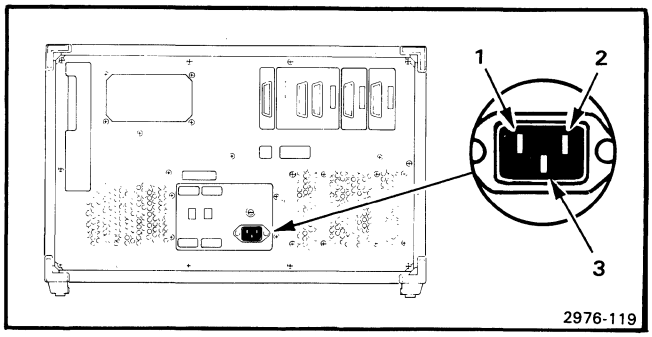


Fig. 8-8. 8301 power cord receptacle.

1. Disconnect the power cord from the rear of the 8301.

2. Remove all circuit boards from the 8301 card cage.

3. Set the 8301 POWER switch ON. Make sure the power cord is still disconnected.

4. Table 8-1 shows the correct resistances between pins 1 and 2 of the receptacle for all combinations of the two voltage selection switches. Use a DMM and the voltage selection switches to verify the resistances shown in Table 8-1. Deviations of more than 100% from the listed resistances indicate a problem.

Table 8-1
Primary Resistances

HI/LO Switch	115V/230V Switch	
	115V	230V
HI	approx 1 ohm	approx 2 ohm
LOW	approx 1 ohm	approx 2 ohm

5. Set the voltage selection switches to 115V, HI.

6. Remove the 8301 top cover.

7. Remove the power supply cover shown in Fig. 8-5.

8. Locate the the output terminals of the three DC power supplies.

9. Connect a DMM to the output of one supply. Set the meter to the appropriate voltage range.

10. Connect a variac to the 8301 power cord receptacle.

11. Ensure that the variac is set to 0 Vac, then turn it ON.

12. Monitor the power input to the 8301 in watts. Do not exceed 100 watts during this test.

13. Slowly increase the variac from 0 Vac to 120(233) Vac. At 120(233) Vac the DMM when connected to the 12 Vdc supplies should indicate a magnitude of 9 Vdc (or more), with the appropriate polarity. The DMM when connected to the +5 Vdc supply should indicate at least +4 Vdc.

14. Repeat steps 9 through 13 for the remaining two power supplies.

This concludes the primary ac voltage input check.

OVERVOLTAGE PROTECTION ADJUSTMENT

Use this routine to set the power supplies' overvoltage protection circuitry. The same procedure is used for each power supply.

1. Remove all circuit boards from the 8301 card cage.

2. Use a variac to supply normal ac power to the 8301. The normal ac supply voltage may be used in place of the variac.

3. Connect a DMM to the output terminal of the appropriate power supply.

4. Locate the OVERVOLTAGE PROTECT (OVP) pot on the power supply and set it fully clockwise (CW).

5. Locate the VOLTAGE ADJUST (VA) pot on the power supply and set it to 6.2 Vdc (for the +5 V supply) or 13.3 Vdc (for the 12 V units).

6. Turn the OVP pot counter-clockwise (CCW) until the supply shuts down, then back it off (CW) a few degrees.

7. Set the 8301 POWER switch to OFF. This resets the overvoltage protection circuitry.

8. Rotate the VA pot 1/4 turn CCW so that the OVP circuit will not trip.

9. Set the 8301 POWER switch to ON.

10. Slowly rotate the VA pot CW while watching the DMM to see where the supply shuts down. Ensure that the supply shuts down at 6.2 Vdc +/-0.1 V (for the +5 V supply) or 13.3 Vdc +/-0.2 V (for the 12 V units).

You may need to repeat steps 6 through 10 several times to ensure that the supply shuts down at the proper voltage. In step 6, try backing the OVP pot off (CW) by a slightly different amount each time.

11. If the supply is operating correctly, reset the VA pot to obtain an output of 5.2 Vdc (for the +5 V supply) or 12.0 Vdc (for the 12 V units).

This concludes the overvoltage protection adjustment routine. If the power supply is operating correctly, proceed to the current limit adjustment.

CURRENT LIMIT ADJUSTMENT

Perform this adjustment after ensuring that the overvoltage protection is set and operating properly. This procedure adjusts the current limits of all three power supplies. If all supplies are not adjusted, the designated load should still be connected to all supplies.

WARNING

This routine must be performed with the specified input line voltages to ensure that UL ratings are maintained. A variac is specified, but not necessary, as long as the correct ac voltages are supplied.

1. Use a variac to supply ac power to the 8301.
2. Set the 8301 POWER switch to OFF.
3. Set the variac to 120(233) Vac.
4. Set the 8301 voltage selection switches (on the back panel) to HI/115 (HI/230).
5. Remove all boards from the 8301 card cage.
6. Set the CURRENT LIMIT (CL) pots on all three power supplies fully clockwise (CW).
7. Connect a load capable of drawing 1.7 amps across the output terminals of each 12 Vdc power supply.
8. Connect a load capable of drawing 35 amps across the output of the +5 Vdc power supply.
9. Set the 8301 POWER switch ON.
10. Allow approximately 2 minutes for the power supplies to reach normal operating temperature.

11. Use a DMM and the VA pot to ensure that the +5 Vdc supply output is +5.20 Vdc.

12. Use a DMM and the VA pots to ensure that both 12 Vdc supply outputs are 12.0 Vdc, with the appropriate polarity.

13. Remove the 1.7 amp load from the +12 Vdc power supply.

14. Connect a 2.0 amp load across the output terminals of the +12 Vdc supply.

15. Connect a 1X oscilloscope probe to the +12 Vdc output terminal.

16. Set the oscilloscope to display 50 mV p-p.

17. Watch the oscilloscope and turn the appropriate CL pot CCW until you either obtain 50 mV p-p of ripple in the +12 Vdc supply or observe a 10 to 20 mV drop in the DC voltage.

18. Swap the loads on the two 12 Vdc power supplies. The -12 Vdc supply should now have a 2.0 amp load. The +12 Vdc supply should have a 1.7 amp load.

19. Move the oscilloscope probe to the output of the -12 Vdc supply.

20. Watch the oscilloscope and turn the appropriate CL pot CCW until you either obtain 50 mV p-p of ripple or observe a 10 to 20 mV drop in the DC voltage.

21. Replace the 2.0 Amp load with a 1.7 amp load.

22. Reset the variac to 108(216) Vac.

23. Move the oscilloscope probe to the output of the +5 Vdc supply.

24. Set the oscilloscope to display 10 mV p-p.

25. Watch the oscilloscope and turn the appropriate CL pot CCW until you either obtain 10 mV p-p of ripple or observe a 10 to 20 mV drop in the DC voltage.

This concludes the power supply current limiting adjustments. If the supplies are operating properly, proceed to the regulation check.

REGULATION CHECK

Use this routine to ensure proper operation of the voltage regulation circuits in the three power supplies. Before performing this routine, ensure that the current limit adjustment is correct.

1. Use a variac to supply normal ac power to the 8301.

2. The variac must be set according to the primary voltage selection switches on the 8301 rear panel. Table 8-2 shows the variac voltage to use for each configuration of the selection switches. Note the switch configuration on your 8301, then set the variac accordingly.

Table 8-2
Variac Settings

HI/LO Switch	115V/230V Switch	
	115V	230V
HI	108Vac to 132Vac	216Vac to 250Vac
LOW	90Vac to 110Vac	180Vac to 220Vac

3. Connect a load capable of drawing 1.7 amps to the output terminals of each 12 Vdc power supply.

4. Connect a load capable of drawing 35 amps to the output terminals of the +5 Vdc power supply.

5. Set the oscilloscope to display 120 mV p-p.

6. Connect the oscilloscope to each 12 Vdc power supply. Ensure that each supply has no more than 120 mV p-p of ripple. Excessive ripple indicates a problem within the supply.

7. Set the oscilloscope to display 50 mV p-p.

8. Connect the oscilloscope to the +5 Vdc supply. Ensure that the supply has no more than 50 mV p-p of ripple. Excessive ripple indicates a problem within the supply.

This concludes the calibration and check-out procedure for the 8301 power supplies.

Section 9

SYSTEM CONTROLLER BOARD

INTRODUCTION

The System Controller board is the controlling element within the 8301 Figure 9-1 is a functional block diagram of the major functions of the System Controller board. These functions consist of the following:

- address and data bus scheme
- system processor
- power-on reset
- memory map and write protect
- interrupt priorities
- clock generation
- interval timer
- bootstrap ROM
- diagnostic ROM
- I/O port interfaces

ADDRESS AND DATA BUS SCHEME

In Fig. 9-1, note there are two address buses and two data buses with separate designations for each, as follows:

- address bus AO(H)---A15(H)
- address bus BAO(H)---BA15(H)
- data bus DO(H)---D7(H)
- data bus BDO(H)---BD7(H)

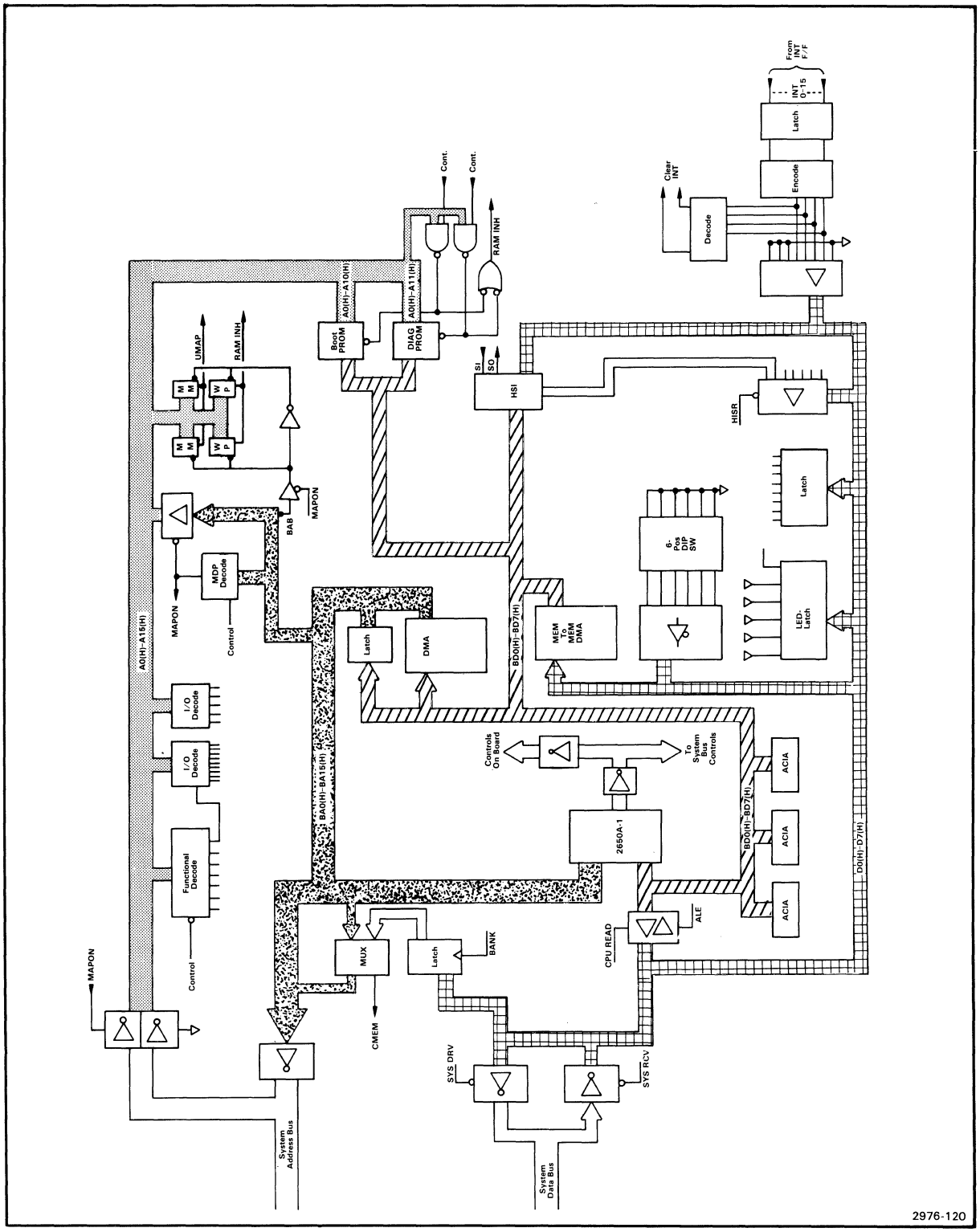


Fig. 9-1. System controller board functional block diagram.

The address bus, BA0(H)---BA15(H), and the data bus, BD0(H)---BD7(H), interface directly with the system processor. The address bus, A0(H)---A15(H), interfaces with the system address bus through directional buffers and the data bus, D0(H)---D7(H), interfaces with the system data bus through bidirectional buffers. The System Controller uses these buses as four distinct buses to permit the system processor to address and write/read data to/from the separated buses by controlling the flow of data through these buffers.

SYSTEM PROCESSOR

The system processor is a 2650A-1 microprocessor that provides overall control of the 8301. Supervisory functions are provided to the system through software control of the hardware circuitry. The software functions controlled by the system processor include:

System input/output	Directs all I/O activity for the system peripherals, including the system terminal, the line printer, and the High-speed Serial Interface (HSI).
Debugging	Executes the debug program and controls the emulator processor through separate debug hardware.
System utilities	Performs all system utility functions, such as processing messages between system peripheral devices.

The system processor has full access to both system memory and program memory. The system processor performs input/output functions to all system peripherals through I/O interface ports. It also directs all other system and program circuit boards, such as the Emulator Controller, Language Processor, System/Program Memory, and Emulator Processor boards.

POWER-ON RESET

The power-on reset circuitry is provided to initialize the 8301 system during power-up and to reset the system during a restart. The power-up detector initiates a reset signal, causing RESET(L) to go low. When low, RESET(L) causes the system processor to fetch and execute the instruction at address 0000 in the system memory. RESET(L), when low, is also used throughout the system to initialize or reset all of the circuit boards. When the RESTART switch on the Front Panel is set to the restart position, RESET(L) goes low, resetting the system processor and all of the circuit boards.

MEMORY MAP AND WRITE PROTECT

The memory map function involves both the 8301 Program Memory and the prototype memory, when operating in emulation mode 1. This function permits mapping assignments to be made to the 8301 Program Memory and/or the prototype memory. Figure 9-2 shows the functional control of the memory mapping feature. Memory mapping permits the user to assign 128-byte blocks of memory address space to either the 8301 Program Memory or the prototype memory, throughout a total address space of 64K bytes. The UMAP(L) control line determines whether the 128-byte memory block is stored in program memory or prototype memory. This function also provides write protection to the 8301 Program Memory. The memory write protect function is similar to the memory mapping, in that any 128-byte block within the 8301 Program Memory 64K address space can be write-protected. The RAM INH(L) line determines which of the 128-byte blocks of program memory are write-protected. If a write violation occurs, an interrupt is generated. The write-protect function does not affect the prototype memory.

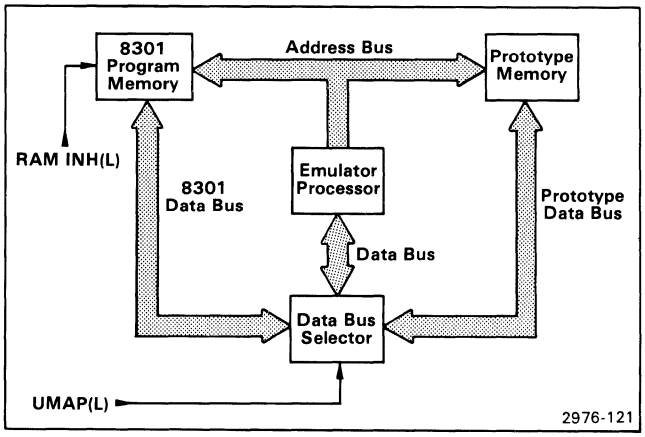


Fig. 9-2. Memory map functional control.

The memory map consists of two 256 x 1-bit RAM storage devices, for a total of 512 bits of storage capacity. The memory capacity of 64K bytes is divided into 512 blocks. Each block has 128 bytes of memory and is represented as one bit in the 512-bit memory map. Each bit in the memory map is used to define one of the 512 blocks of memory as being in the 8301 Program Memory or the prototype memory. The write-protect logic consists of two 256 x 1-bit RAM storage devices, for a total of 512 bits of storage capacity. The write-protect and memory map storage are identical, with the exception of the DI (data in) and the DO (data out) lines. Each of the 512 blocks of 8301 Program Memory can be write-protected by setting the write-protect bit for each block.

The uppermost 512 addresses (FE00 through FFFF) of the system memory address space are used to store the memory map and write-protect information in the memory map and write-protect RAM storage devices. When these addresses are accessed, data bus bits D0 and D2 are stored in the RAMs on a write operation or read from the RAMs on a read operation.

INTERRUPT PRIORITIES

The system processor (2650A-1 microprocessor) in the System Controller has vector interrupt capabilities. The starting address of a service routine (interrupt) is called an interrupt vector and is read by the system processor as a vector address from the data bus. The system processor can service up to 32 of these interrupts on a priority basis. Sixteen of the interrupts are encoded and placed on the data bus by the System Controller and sixteen are encoded and placed on the data bus by the Emulator Controller. A priority is established for each interrupt, with the System Controller interrupts having a higher priority than the Emulator Controller interrupts. Table 9-1 shows the priority assignment, vector address, and function or interrupting device for each interrupt. The priority encoding and enabling of these interrupts is controlled by logic circuitry on the System Controller and Emulator Controller boards.

Each interrupting device/function has a dedicated interrupt flip-flop/latch associated with it. When a device requests an interrupt, the corresponding interrupt flip-flop/latch is set. The priority encoders ensures that the highest priority of the 16 encoded interrupts on the System Controller board is serviced first. If more that one interrupt is present at one time, the highest priority interrupt is serviced first. The lower priority interrupt remains set in its associated flip-flop/latch and is serviced when the higher interrupts are completed.

Table 9-2 contains the following information:

- A list of the system bus interrupt lines associated with each of the 16 interrupts encoded by the System Controller board.
- The associated flip-flop/latch output control line.
- Where the interrupt is originated.
- The function of the interrupt.

Referring to Table 9-1 and 9-2, the 16 interrupts encoded by the system processor are assigned as follows:

- Seven interrupt flip-flops are located on the System Controller board.
- Three interrupts are passed from the peripheral devices through the associated ACIAs.
- Three interrupts are reserved.
- Three interrupts are not assigned.

Table 9-1
Interrupt Vectors

Priority	Vector Address	Function
0	0000	Reset
1	0002	System Memory Parity Error
2	0004	Write Protect Violation
3	0006	Reserved for Program Memory Parity Error
4	0008	H.S. Interface In
5	000A	H.S. Interface Out
6	000C	Remote Communications Port (ACIA)
7	000E	Auxiliary Port (ACIA)
8	0010	System Terminal Port (ACIA)
9	0012	Interval Timer
10	0014	DMA
11	0016	Manufacturing Test Port
12	0018	NA
13	001A	PROM Programmer
14	001C	NA
15	001E	System Memory Refresh
16	0020	Emulator SVC 1
17	0022	Emulator SVC 2
18	0024	Emulator SVC 3
19	0026	Emulator SVC 4
20	0028	Emulator SVC 5
21	002A	Emulator SVC 6
22	002C	Debug SVC 1 (Dump--Restore)
23	002E	Debug SVC 2 (Get--Put)
24	0030	Breakpoint 1
25	0032	Breakpoint 2
26	0034	Single Cycle
27	0036	Emulator Halted
28	0038	Diagnostic Interrupt
29	003A	RTPA Interrupt 29
30	003C	RTPA Interrupt 30
31	003E	RTPA Interrupt 31
		NA=Not Assigned

Table 9-2
Flip-Flop/Latch Interrupts on the System Controller Board

System Bus Line Name	Flip-Flop/Latch Output Line	Origin Of Interrupt	Function
INT 0(L)	RESET(L)	Sys. Cont. & Front Panel	Reset
INT 1(L)	SMEM PARITY(L)	System RAM	System Memory Parity Error
INT 2(L)	WRITE PROT(L)	Sys. Cont.	Write Protect Violation Interrupt
INT 3(L)	----------	----------	Reserved for Program Memory Parity Error
INT 4(L)	HS IN(L)	Sys. Cont.	H.S. Interrupt In
INT 5(L)	HS OUT(L)	Sys. Cont.	H.S. Interrupt Out
INT 6(L)	RINT(L)	ACIA (Sys. Cont.)	Remote Communications Port Interrupt (ACIA)
INT 7(L)	AINT(L)	ACIA (Sys. Cont.)	Auxiliary Port Interrupt (ACIA)
INT 8(L)	TINT(L)	ACIA (Sys. Cont.)	System Terminal Port Interrupt (ACIA)
INT 9(L)	CLOCK INT(L)	Sys. Cont.	Interval Timer Interrupt
INT 10(L)	DMA INT(L)	Sys. Cont.	DMA Interrupt
INT 11(L)	DISC INT(L)	Sys. Cont.	Manufacturing Test Port Interrupt
INT 12(L)	----------	----------	Not Assigned
INT 13(L)	INT 13(L)	PROM Prog.	PROM Programmer Interrupt
INT 14(L)	----------	----------	Not Assigned
INT 15(L)	INT 15(L)	System RAM	System Memory Refresh Interrupt

CLOCK GENERATION

The clock generation circuitry consists of two crystal oscillators, 2.4576 MHz and 20 MHz. Figure 9-3 is a functional block diagram of these oscillators. The 2.4576 MHz oscillator is used to generate a 153.6k baud rate for the high-speed serial interface (HSI). This frequency is also divided by two and fed to the Communications Interface board to generate the various baud rates for the ACIAs. The 20 MHz oscillator feeds two timing chains that provide the following clock frequencies:

Frequency	Function
10 MHz	8301 system clock
5 MHz	Not used
2 MHz	DMA clock--FAST clock for the system processor
1.25 MHz	SLOW clock for the system processor and I/O clock

The 1.25 MHz and 2 MHz frequencies are connected to the internal selector, J5704. The position of jumper J5704 selects either a SLOW or FAST clock for the system processor (2650A-1).

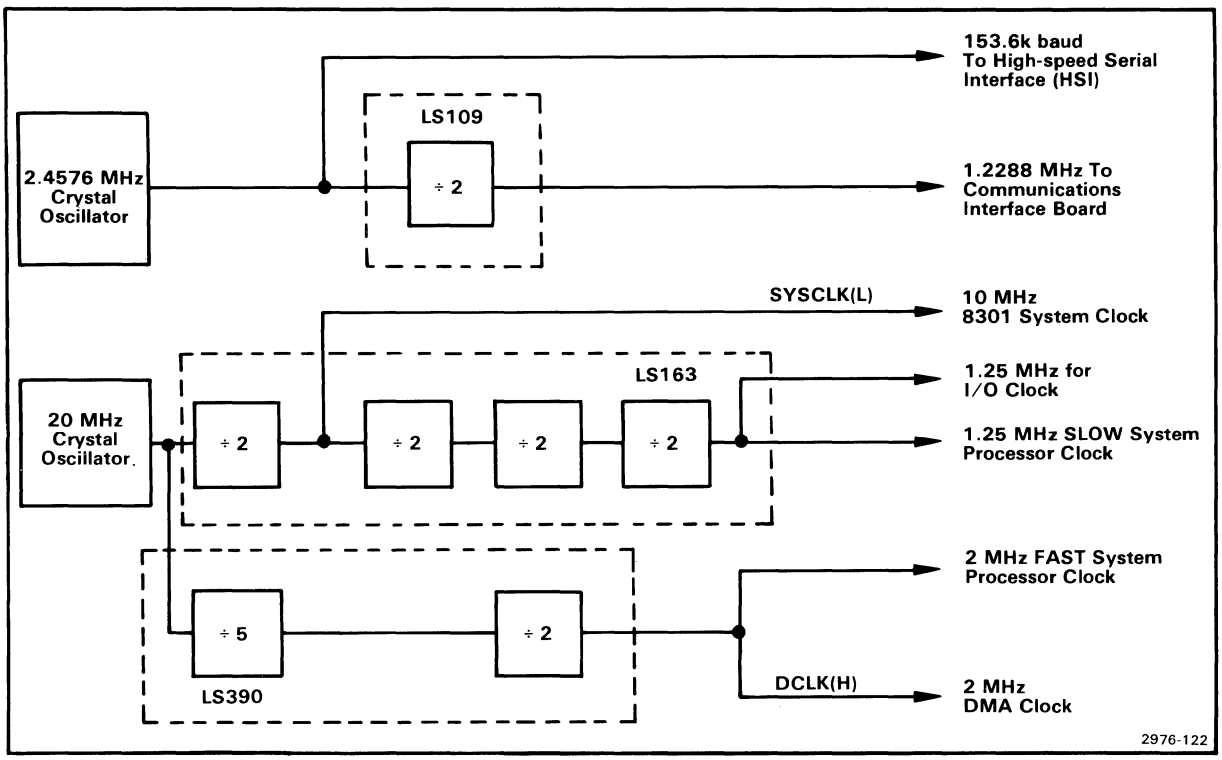


Fig. 9-3. Clock generation timers functional block diagram.

INTERVAL TIMER

The interval timer circuitry is another timing chain that generates the 100 ms interval timer clock. The 1200 Hz frequency from the baud rate generator on the Communications Interface board is divided by 120 to generate the 100 ms interval clock. Figure 9-4 is a functional block diagram of the interval timer. For additional information on the use of the interval timer, refer to the I/O Port Interfaces discussion later in this section, port address EC (write).

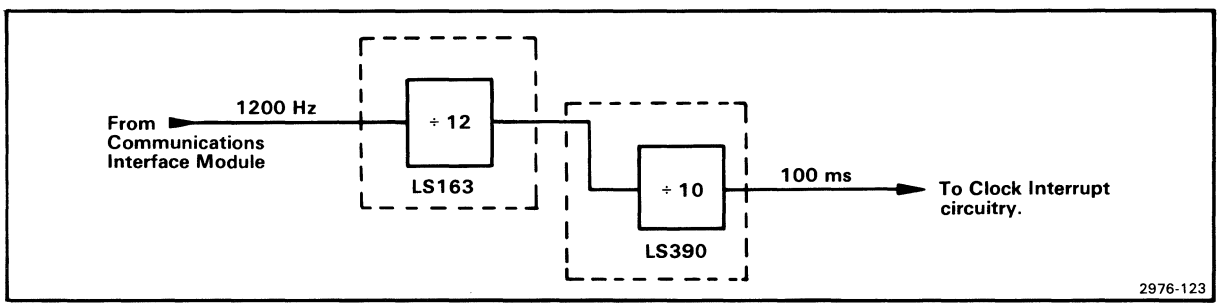


Fig. 9-4. Interval timer functional block diagram.

BOOTSTRAP ROM

The bootstrap ROM (a 2716-type device) has the capacity to store 16K bits (2K bytes) of ROM. Wire strap W2012 allows the ROM to be strapped for either 8K or 16K bits of storage. Normal strapping is 16K bits. The bootstrap ROM can be software-enabled or -disabled, but is automatically enabled when control line RESET(L) is asserted. On power-up or restart conditions (after the power-up tests have completed), the bootstrap ROM boots the operating system from the DMU disc into system memory.

DIAGNOSTIC ROM

The diagnostic ROM (a 2332-type device) is a mask programmable ROM that has a storage capacity of 32K bits (4K bytes). The diagnostic ROM occupies memory space beginning at address 0000 through OFFF. It can be enabled or disabled by software or the mode select switch. (Refer to Section 3 of this manual ROM Based Diagnostics, for additional information on the mode select switch.) The diagnostic ROM contains the power-up tests (self tests) that are executed each time the POWER or RESTART switch is activated. The diagnostic ROM is also enabled if jumper J3014 is installed in the forced diagnostic position. (Refer to Section 2 of this manual Installation, for a complete listing of all jumpers.)

I/O PORT INTERFACES

In order to perform its software functions, the system processor must be able to communicate with other circuit boards and with peripheral equipment. This is accomplished through I/O port interfaces located on the various boards. The I/O port interfaces for the System Controller board are divided into the following functions:

- Functional and I/O Decoders
- External I/O Ports
    1. Remote Communications Port (RS-232-C)
    2. Auxiliary Port (RS-232-C)
    3. System Terminal Port (RS-232-C)
    4. High-Speed Interface Port (RS-422)
    5. Flexible Disc Port
- System I/O Ports
    1. Interval Timer/CPU Reset Port
    2. Switch Read/LED Write Port

3. Bank Switching Port

4. Sync Test Port

5. DMA Interface Ports

The designation of external and system I/O ports refers to whether the I/O port interfaces with peripheral equipment external to the 8301 or interfaces with hardware circuitry within the 8301 unit. The I/O port addresses establish the correct interface, and the associated data bus contains information that takes the form of:

- status (read)
- control (write)
- data (read or write)

FUNCTIONAL AND I/O DECODERS

The lower order address bus lines, A0---A7, are decoded to determine which I/O port is accessed. Table 9-3 lists the I/O port assignments for the System Controller. Refer to Section 6 of this manual Specifications, for a complete listing of the I/O port assignments for the 8301.

I/O port addresses for the System Controller board are decoded in a functional decoder and two I/O decoders; one for read operations and one for write operations. Figure 9-5 is a simplified block diagram of these decoders.

Table 9-3
System Controller I/O Port Address Assignments

Port Address	Read/Write	Function or Device
90---9F	R/W	DMA Controller
CA	R/W	Remote Port--ACIA control and status
CB	R/W	Remote Port--ACIA data
CC	R/W	Auxiliary Port--ACIA control and status
CD	R/W	Auxiliary Port--ACIA data
CE	R/W	System Terminal Port--ACIA control and status
CF	R/W	System Terminal Port--ACIA data
E8	R/W	High-Speed Communications port data
E9	R/W	High-Speed Communications port control and status
EA	R/W	Flexible Disc status and control
EB	R/W	Flexible Disc data
EC	W	Interval Timer control port
EC	R	Programmed reset
ED	W	LED Write port
ED	R	Switch Read port
EE	W	Bank Switch
EF	R	Sync Test port

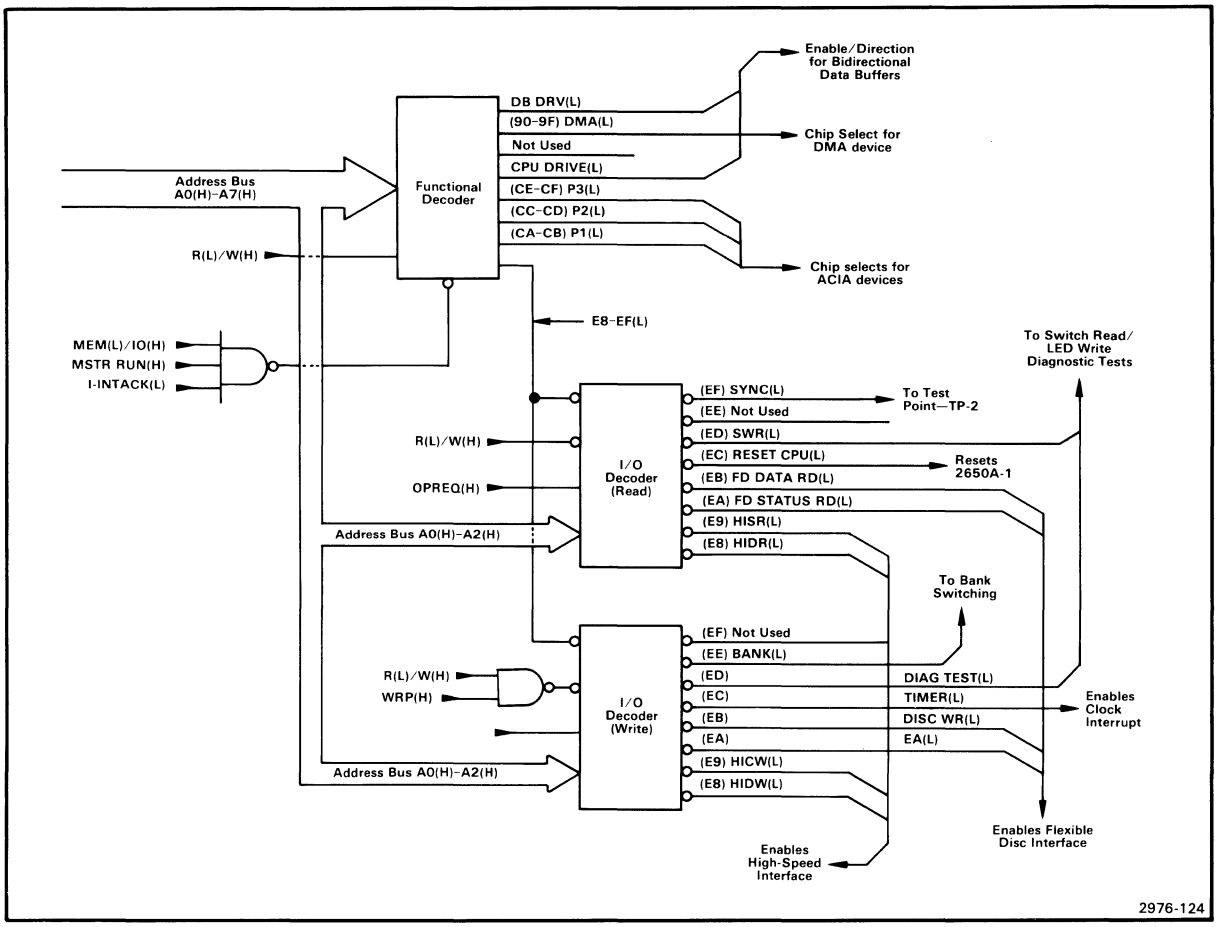


Fig. 9-5. Functional and I/O decoders block diagram.

Functional Decoder

The functional decoder utilizes a 74S472-type device (PROM) as a decoder. This decoder is enabled when all of the following conditions are met: (Refer to Fig. 9-5.)

1. when control line MSTR RUN(H) is high, indicating that the 2650A-1 is fetching and executing instructions;

2. when control line M(L)/IO(H) is high, indicating the execution of an I/O instruction; and

3. when control line I-INTACK(L) is high, indicating there is no interrupt pending or in progress.

When enabled, the functional decoder decodes the following I/O port addresses from the address bus during either a read or write operation. (Refer to Fig. 9-5.)

90 through 9F — Any of these I/O port addresses sets control line DMA(L) low, enabling the DMA device.

CA and CB — These I/O port addresses set control line P1(L) low, enabling the remote communications port ACIA.

CC and CD — These I/O port addresses set control line P2(L) low, enabling the auxiliary port ACIA.

CE and CF — These I/O port addresses set control line P3(L) low, enabling the system terminal ACIA.

E8 through EF — Any of these I/O port addresses sets control line E8---EF(L) low, enabling one of the enabling inputs to each I/O decoders. Each I/O decoder has three enabling inputs. The other two inputs are discussed later in this section.

Table 9-4 shows the states of the enabling control lines, the I/O port addresses, and the output control lines for the functional decoder. Note in Fig. 9-5, there are two other output lines from the functional decoder, DB DRV(L) and CPU DRIVE(L). These control lines are used to set the direction of data flow through the data bus directional and bidirectional buffers. This permits the system processor to be selective during read operations, and to read only the unique data buses and/or the system data bus.

Table 9-4
Functional Decoder Enabling Lines and Output Lines

Functional Decoder Enabling Control Lines						Output Control Lines	
Read/ Write Oper	MSTR RUN(H)	I-INTACK (L)	M(L)/ IO(H)	R(L)/ W(H)	I/O Port Addr	Line Name	Function
Read	1	1	1	0	90--9F	DMA(L)	Chip select for 8257 DMA Controller
Write				1			
Read	1	1	1	0	CA--CB	P1(L)	ACIA chip select for Remote Communications Port
Write				1			
Read	1	1	1	0	CC--CD	P2(L)	ACIA chip select for Auxiliary Port
Write				1			
Read	1	1	1	0	CE--CF	P3(L)	ACIA chip select for System Terminal Port
Write				1			
Read	1	1	1	0	E8--EF	E8--EF(L)	Enabling control line for I/O Decoders
Write				1			

I/O Decoders

The two I/O decoders are shown in Fig. 9-5. One decoder activates control lines during a read operation and the other decoder activates control lines during a write operation. As previously discussed, I/O port addresses E8---EF set the functional decoder output control line, E8---EF(L), low. This control line, E8---EF(L), is one of three enabling inputs to each of the I/O decoders.

The read I/O decoder is enabled during a read operation when all of the following conditions are met:

1. control line E8---EF(L) from the functional decoder is low, indicating an I/O port address between E8---EF is on the address bus;

2. control line OPREQ(H) is high, indicating a bus operation is in progress; and

3. control line R(L)/W(H) is low, indicating a read operation.

The write I/O decoder is enabled during a write operation when all of the following conditions are met:

1. the first two conditions for a read operation (listed previously) are met;

2. control line R(L)/W(H) is high, indicating a write operation; and

3. WRP(H) is high, indicating the data on the bus is valid for a write command.

When either the read or write I/O decoder is enabled, an output control line is asserted which activates an I/O port interface. The output control line asserted depends on the I/O port address on the address bus. The lower three address bits (A0, A1, and A2) and the R(L)/W(H) control line determine which I/O decoder output control line is asserted. Table 9-5 contains the following information on the I/O decoders:

- enabling control lines.
- I/O port addresses.
- output control lines for the I/O decoders.
- function of output control lines.

Table 9-5
I/O Decoders--Enabling Lines and Output Lines

I/O Port Addr	I/O Decoders Enabling Control Lines: R/W Oper	E8--EF(L)	OPREQ (H)	R(L)/W(H)	WRP (H)	Addr Bits A2 A1 A0	Output Control Lines from I/O Decoders: Line Name	Function
E8	R	0	1	0	X	0 0 0	HIDR(L)	HSI character read.
	W			1	1		HIDW(L)	HSI character load.
E9	R	0	1	0	X	0 0 1	HISR(L)	HSI status.
	W			1	1		HICW(L)	HSI control.
EA	R	0	1	0	X	0 1 0	FD STATUS RD(L)	Flexible disc status.
	W			1	1		EA(L)	Flexible disc control.
EB	R	0	1	0	X	0 1 1	FD DATA RD(L)	Flexible disc data read.
	W			1	1		DISC WR(L)	Flexible disc data write.
EC	R	0	1	0	X	1 0 0	RESET CPU(L)	2650A-1 reset.
	W			1	1		TIMER(L)	Interval timer enable.
ED	R	0	1	0	X	1 0 1	SWR(L)	Read DIP switch.
	W			1	1		DIAG TEST(L)	Diagnostic tests.
EE	W	0	1	1	1	1 1 0	BANK(L)	Bank switch load.
EF	R	0	1	0	X	1 1 1	SYNC(L)	Sync test point.

RS-232-C INTERFACE PORTS

The three peripheral interface ports provide compatible EIA standard RS-232-C interfaces. These ports are:

- remote communications port
- auxiliary port

- system terminal port

These ports use Asynchronous Communications Interface Adapter (ACIA) devices (Motorola 6850) that connect to standard 25-pin connectors. The interfacing connectors are located on the 8301 rear panel. A baud rate selector switch is located adjacent to each connector. The following baud rates are available:

110	1200
150	2400
300	4800
600	9600

The ACIA devices perform a serial-to-parallel conversion from the peripherals to the 8301 and a parallel-to-serial conversion from the 8301 to the peripherals. The status, control, and data transfer (read/write) functions of the ACIAs are software-controlled by I/O port addresses and by the associated data bytes.

The four registers in the ACIA are selected with I/O port addresses and the read/write control line. Table 9-6 shows the states of these lines and the selection of the various registers.

Table 9-6
ACIA Register Selection

Type of Operation	I/O Port Address	ACIA Input Control Lines: R(H)/W(L) (R/W)	ACIA Select (CS2)	Register Select (RS)	Function
Write	Even	0	0	0	Selects the ACIA control register (CR) and loads the control byte into the register for control of the ACIA receiver, transmitter, interrupt enables, and the peripheral equipment.
	Odd	0	0	1	Selects the ACIA transmit data register (TDR) and loads the data into the register for transmission to the peripheral equipment.
Read	Even	1	0	0	Selects the ACIA status register (SR), which contains the status of the transmitter data register, receive data register, error logic, and peripheral equipment.
	Odd	1	0	1	Selects the ACIA receive data register (RDR) and reads the data byte received from the peripheral equipment.

Referring back to Table 9-4, note that the I/O port addresses cause the functional decoder output control lines P1(L), P2(L), and P3(L) to go low. These lines are shown in Table 9-6 as the ACIA chip select input (CS2) for each ACIA.

The interfaces between the ACIA devices and the System Controller board are identical for each ACIA. The interfaces between the ACIA device and the Communications Interface board depend on the type of peripheral equipment connected to the output connectors. Figure 9-6 is a simplified schematic showing the interfaces between one of the ACIA devices and the System Controller board. The ACIA is enabled and the various registers are selected as follows:

1. The ACIA is selected when the chip select input lines CS0 and CS1 are high and CS2 is low. CS0 and CS1 are tied high; therefore, the ACIA is selected when CS2 goes low.

2. When the ACIA is selected, it is enabled (E) on the first 2560 CLK(L) pulse after OPREQ(H) goes high.

3. The read/write [R(H)/W(L)] line selects the write-only registers or the read-only registers. Refer to Table 9-6.

4. The register select (RS) line selects the transmit/receive data registers when high and the control/status registers when low. Refer to Table 9-6. This line connects to address bit A0 and is either high or low depending on whether the I/O port address on the address bus is even or odd.

As previously stated, when a register is selected, the associated data byte is either loaded into the register during a write operation or read from the register during a read operation.

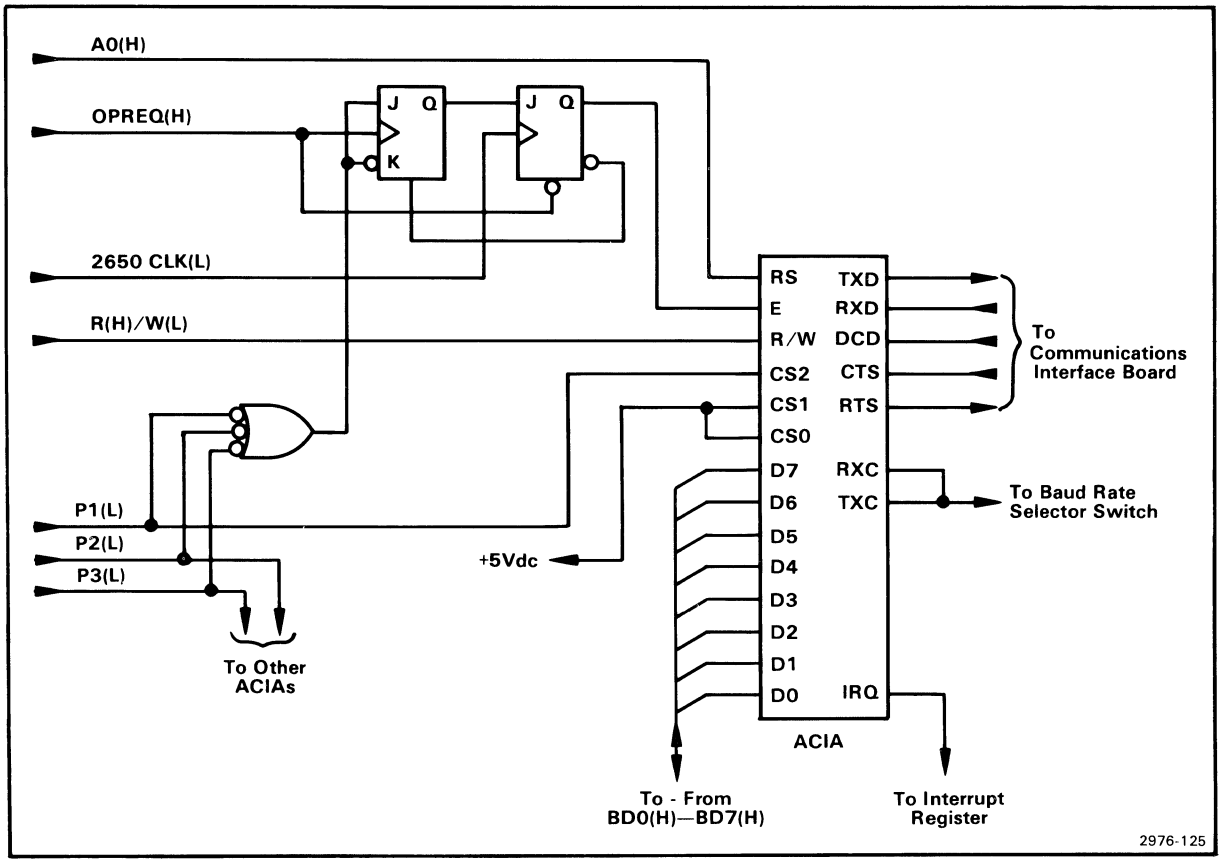


Fig. 9-6. ACIA interface to System Controller board.

Remote Communications Port

The remote communications port ACIA provides a RS-232-C compatible interface, configured to be used with a modem for telephone data communications. The port has a switch-selectable DTE/DCE (Data Terminal Equipment/Data Communications Equipment) capability. A switch on the 8301 back panel selects one of the following four possible modes:

- No control
- DTE with DSR (data send ready) control
- DTE with CTS (clear to send) control
- DCE with control

There is a male (J101) and a female (J102) connector on the 8301 back panel associated with this port. Only one can be used at a time. A baud rate selector switch (S1060) adjacent to the connectors on the 8301 back panel selects one of eight baud rates.

The remote communications port ACIA is accessed during I/O port addresses CA or CB. Refer back to Tables 9-4 and 9-6. Whenever I/O port address CA or CB is on the address bus, control line P1(L) is low. P1(L) is the chip select line for the remote communications ACIA. P1(L), in association with R(H)/W(L), and address bit A0 establishes the status/control and receive/transmit functions of the ACIA. Table 9-7 shows the relationships of these control lines.

Auxiliary Port

The auxiliary port ACIA provides a DCE (Data Communications Equipment) RS-232-C compatible interface, configured to be used with a line printer or similar equipment. A female connector (J103) on the 8301 back panel interfaces with the peripheral equipment. A baud rate selector switch (S1080) adjacent to the connector selects one of eight baud rates.

In addition, this port has provisions to input an external clock through pin 17 of connector J103. The external clock must be TTL compatible. An internal jumper, J3, on the Communications Interface board can be positioned so that the external clock is substituted for the standard 110 baud rate on the baud rate selector switch (S1080). (See Section 2, Installation, for a complete list of internal jumpers.)

The auxiliary ACIA is accessed during I/O port addresses CC or CD. Refer back to Tables 9-4 and 9-6. Whenever I/O port address CC or CD is on the address bus, control line P2(L) is low. P2(L) is the chip select line for the auxiliary ACIA. P2(L) in association with R(H)/W(L) and address bit A0 establishes the status/control and receive/transmit functions of the ACIA. Table 9-8 shows the relationships of these control lines.

Table 9-7
Remote Communications Port ACIA

Type of	I/O Port	ACIA Input Control Lines			Function
			ACIA Select	Register Select	
Read	CA	1	0	0	Selects the ACIA status register.
	CB	1	0	1	Selects the ACIA receive data register.
Write	CA	0	0	0	Selects the ACIA control register.
	CB	0	0	1	Selects the ACIA transmit data register.

Table 9-8
Auxiliary Port ACIA

Type of	I/O Port	ACIA Input Control Lines			Function
			ACIA Select	Register Select	
Read	CC	1	0	0	Selects the ACIA status register.
	CD	1	0	1	Selects the ACIA receive data register.
Write	CC	0	0	0	Selects the ACIA control register.
	CD	0	0	1	Selects the ACIA transmit data register.

System Terminal Port

The system terminal port ACIA provides a DCE (Data Communications Equipment) RS-232-C compatible interface. This interface is configured to be used with a crt terminal or console-type terminal that provides receive/display and transmit functions with full ASCII (96 characters) capabilities. A female connector (J104) on the 8301 back panel interfaces with the peripheral

equipment. The baud rate selector switch (S1090), adjacent to the connector, selects one of eight baud rates.

The system terminal ACIA is accessed during I/O port addresses CE or CF. Refer back to Tables 9-4 and 9-6. Whenever I/O port address CE or CF is on the address bus, control line P3(L) is low. P3(L) in association with R(H)/W(L) and address bit A0 establishes the status/control and receive/transmit functions of the ACIA. Table 9-9 shows the relationships of these control lines.

RS-422 INTERFACE PORT

The high-speed serial interface (HSI) provides a 153.6k baud serial interface between the 8301 and a DMU unit. An IM6402 type Universal Asynchronous Receiver Transmitter (UART) is used for this interface. The transmitter in the UART converts parallel data into a serial format, and automatically adds start, parity, and stop bits. The serial data is then transmitted over the HSI. The receiver in the UART receives the serial data over the HSI and converts the serial start, data, parity, and stop bits to parallel data. The receiver also verifies the proper code transmission, parity, and stop bits.

HSI I/O Port

The UART is activated by I/O port addresses E8 and E9. Referring back to Table 9-5, note that these addresses generate four control lines. Two of these control lines are for each address, one for read operations and one for write operations. I/O port address E8 permits the system processor to read or write data from/to the UART. I/O port address E9 provides control of the HSI and DMA ports during a write operation and the status of the ports during a read operation.

Table 9-9
System Terminal ACIA

Type of	I/O Port	ACIA Input Control Lines			Function
			ACIA Select	Register Select	
Read	CE	1	0	0	Selects the ACIA status register.
	CF	1	0	1	Selects the ACIA receive data register.
Write	CE	0	0	0	Selects the ACIA control register.
	CF	0	0	1	Selects the ACIA transmit data register.

MANUFACTURING TEST PORT

The manufacturing test port provides two 8-bit parallel communication channels between the 8301 and a factory test unit. One of the 8-bit parallel channels sends data to the factory test unit [data out, D0D0(H)---D0D7(H)]. The other 8-bit parallel channel receives data from the factory test unit [data in, DID0(H)---DID7(H)]. This interface port is enabled during I/O port addresses EA or EB. Refer back to Table 9-5. Address EA provides control to the factory test unit during a write operation and the status of the factory test unit during a read operation. Address EB clocks the data from the data bus onto the parallel data-out channels [D0D0(H)---D0D7(H)] during a write operation. Address EB also enables the input data buffers, during a read operation, gating the parallel data-in channels [DID0(H)---DID7(H)] onto the data bus. Table 9-10 lists the read and write operations for I/O port addresses EA and EB.

Table 9-10
Flexible Disc I/O Ports

Type of Operation	I/O Port Address	I/O Decoder Output Line	Function
Read	EA	FD STATUS RD(L)	Enables tristate buffer
Write	EA	EA(L)	Clocks the 8-bit control latch
Read	EB	FD DATA RD(L)	Enables the parallel input tristate buffers
Write	EB	DISC WR(L)	Clocks the 8-bit parallel output latch

INTERVAL TIMER/CPU RESET PORT

This I/O port interface is used to enable/disable the interval timer and to reset the system processor. The I/O port is accessed during I/O port address EC. Refer back to Table 9-5. When the I/O port address EC is on the address bus during a read operation, the control line RESET CPU(L) goes low. When low, this line resets a J-K flip-flop which resets the system processor on the next system clock pulse. The associated data byte on the data bus is not used for this I/O port interface.

When the I/O port address EC is on the address bus during a write operation, the control line TIMER(L) goes low. When low, this line clocks a timer flip-flop. The data bit DO of the associated data byte on the data bus is fed to the J-K inputs of this timer flip-flop. The output of the timer flip-flop enables or disables the clock interrupt flip-flop. When enabled the clock interrupt flip-flop generates an interrupt to the system processor every 100 ms. Table 9-11 shows the relationships of the control lines and the data bit DO for both the interval timer and the CPU reset I/O ports.

SWITCH READ/LED WRITE PORT

This I/O port interface is used to call up diagnostic routines (self tests). The port consists of a six-position DIP switch that can be read from the data bus lines, D2(H)---D7(H), during I/O port address ED. Various diagnostic self-tests can be conducted, depending on the settings of the DIP switch. The satisfactory completion or failure of the diagnostic tests is indicated by turning LEDs on or off. Five LEDs are located on the System Controller board, and one LED labeled SELF TEST is located on the 8301 Front Control Panel. The LEDs are turned off or on during a write operation to I/O port address ED. The system processor can determine if the SELF TEST (LED) on the front panel is turned off or on by reading bit D6 of I/O port address E9.

Table 9-12 shows the I/O decoder output lines, the affected data bus lines, and their functions during a read or write operation to I/O port address ED.

Table 9-11
Interval Timer and CPU Reset I/O Ports

I/O Port Address	Type of Operation	Output Line	Data Bit DO	Function
EC	Read	RESET CPU(L)	Not Used	The control line RESET CPU(L) resets the 2650A-1 microprocessor.
	Write	TIMER (L)	1	Enables Timer interrupt
			0	Disables Timer interrupt

Table 9-12
Switch Read/LED Write I/O Port

I/O Port Address	Type of Operation	I/O Decoder Output	Function of Control Line	
ED	Read	SWR(L)	The states of data bus lines D2(H)--D7(H) depending on the settings of the 6-position DIP switch.	When control line SWR(L) goes low, the buffer is enabled. This forces the states of the 6-position DIP switch onto the data bus. The switch settings determine which diagnostic test is conducted.
	Write	DIAG TEST(L)	Data bus lines DO(H)--D5(H) are connected to the inputs of a latch. These data lines contain the results of the conducted diagnostic test.	The latch is clocked when control line DIAG TEST(L) goes low. The latch outputs turn LEDs off or on depending on the states of the latch input lines, data bus lines DO(H)--D5(H).

BANK SWITCHING PORT

The system processor can address up to 32K of address space. It has 15 address lines (A0---A14) which have a maximum addressing capability of 7FFF. The bank switching circuitry provides the system processor with the capability of addressing up to 64K of address space in both system and program memories. Bank switching permits 16K blocks of system or program memory addresses (on even 16K boundaries) to be switched into the system processor's upper 16K address space (16K---32K).

Referring back to Table 9-5, note that during a write to I/O port address EE the control line BANK(L) is low. Figure 9-7 is a simplified schematic of the bank switching circuitry. Refer to this schematic during the following description of bank switching.

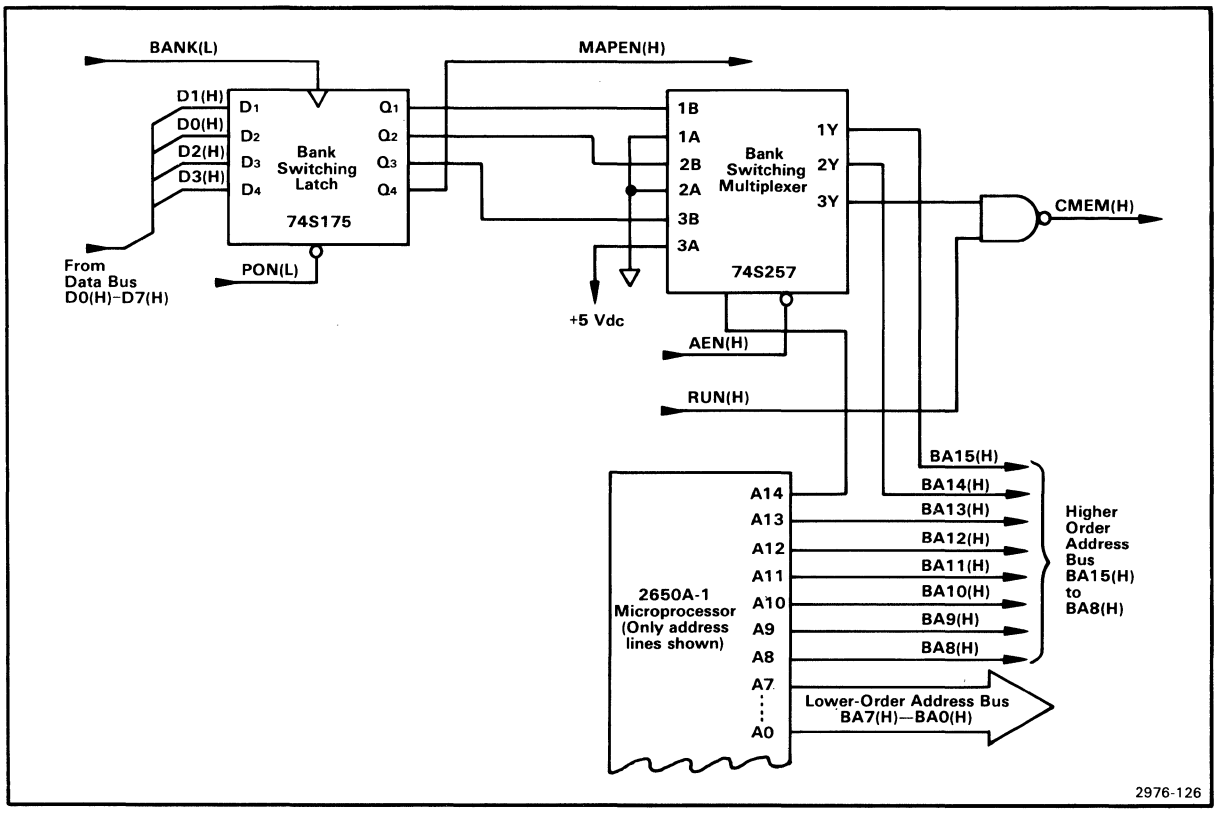


Fig. 9-7. Bank switching simplified schematic.

On power-up or restart, the system processor addresses its lower 16K address space (0000---3FFF). The state of address line A14 is low. A14 is connected to the multiplexer select input. When this input is low, the A inputs to the multiplexer are selected. This forces BA15(H) and BA14(H) low, limiting the maximum addressing to 3FFF. The 3Y output also forces CMEM(H) low, which selects the system memory. Therefore, on initial power-up or restart the

system processor is accessing the lower 16K block (0000---3FFF) of system memory. To access any portion of program memory or above 16K in system memory, the system processor must address its upper address space (16K---32K). When addressing its upper address space, the state of address line A14 is always high (4000----7FFF). When this line goes high the B inputs to the multiplexer are selected. The B inputs are controlled by the data byte written to I/O port address EE. Data bit D2(H) selects either the program or system memory. Data bits D1(H) and DO(H) select the 16K block of memory addresses accessed by the system processor in either the system or program memory. Therefore, when the system processor is accessing any portion of program memory or above 16K in system memory the bank switching circuitry is enabled. Table 9-13 shows the state of the control bits for accessing both system and program memories during a write operation.

Note in Fig. 9-7 that data bit D3(H) controls the state of MAPEN(H), when the bank switching latch is clocked. When D3(H) is high, the memory map and write protect circuitry can be enabled. MAPEN(H) is one of the inputs to the NAND gate memory map and write protect detector.

Table 9-13
Bank Switching I/O Port EE

16K Memory Block and Address	Access System/ Program Memory	Control Bits: From 2650A-1	Control Bits: Data Bus Lines			Address Bus Lines		State of CMEM(H) Control Line
		A14	D2	D1	D0	BA15	BA14	
0--16K 0000--3FFF	System	0	X	X	X	0	0	0
16K--32K 4000--7FFF	System	1	1	0	1	0	1	0
32K--48K 8000--BFFF	System	1	1	1	0	1	0	0
48K--64K C000--FFFF	System	1	1	1	1	1	1	0
0--16K 0000--3FFF	Program	1	0	0	0	0	0	1
16K--32K 4000--7FFF	Program	1	0	0	1	0	1	1
32K--48K 8000--BFFF	Program	1	0	1	0	1	0	1
48K--64K C000--FFFF	Program	1	0	1	1	1	1	1

SYNC TEST PORT

The sync test port provides a sync pulse for test purposes during a read operation. When I/O port address EF is read, the control line SYNC(L) is low. This control line terminates in a test point, TP-2. Table 9-14 shows the I/O port address and control line. The associated data byte is not used for this I/O address.

Table 9-14
Sync Test Port

I/O Port Address	Type of Operation	Output Control Line	Function of Control Line
EF	Read	SYNC(L)	Provides a sync pulse to TP-2 for test purposes.

DIRECT MEMORY ACCESS (DMA)

The direct memory access (DMA) interface utilizes an 8257 device DMA controller which is specifically designed to transfer data at high speeds and in blocks of up to 16K bytes. The DMA controller is a four-channel device; however, in the 8301 only three channels are utilized. Channels 0 and 1 are used for direct transfer of data from memory-to-memory within the 8301. Channel 2 is used to transfer over the HSI (high-speed serial interface) port.

Once the DMA device is initialized by software, it can transfer one byte to 16K bytes in a block of data (between memory-and-memory or memory-and-HSI directly) without further intervention required by the system processor. If a request for transferring data [DMA request line set high] is received over the HSI port or a request for a memory-to-memory transfer is made, the DMA controller:

1. assumes control of the system address and data buses;

2. waits for the system processor to return a hold acknowledge;

3. acknowledges receipt of hold acknowledge which activates the correct DMA channel for transferring data;

4. outputs the eight least significant bits of the memory address onto the system address bus (lines A0---A7);

5. then outputs the eight most significant bits of the memory address onto the data bus (lines D0---D7);

6. an 8-bit latch on the System Controller board transfers these memory address bits onto the system bus (lines A8---A15); and

7. generates the appropriate memory and I/O read/write control signals, causing the peripheral or memory to receive or deposit a data byte directly from or to the addressed memory location.

The DMA device will retain control of the system address and data buses and continue the transfer sequence, as long as the DMA request line is held high. When the specified number of data bytes have been transferred, the DMA device

activates its TC (terminal count) output which informs the system processor through an interrupt that the transfer operation is complete.

DMA I/O Port

The DMA controller has ten internal registers. Each of the four channels has a 16-bit DMA address register and a 16-bit terminal count register. All eight registers may be read and/or programmed. In addition, there are two general registers: one 8-bit mode set register and one 8-bit status register. The mode set register is programmed only. The status register is read only. The registers are programmed or read when the system processor executes a write or read instruction that addresses a designated register within the DMA device. Note in Table 9-4 that I/O port addresses 90 through 9F are reserved for the DMA controller. If any of these addresses appears on the address bus, control line DMA(L) goes low and enables the DMA controller [DMA(L) is connected to the CS(L), chip select, input of the DMA device]. In addition to enabling the DMA controller, I/O port addresses 90 through 98 (in conjunction with other control signals) are used to select one of the ten internal registers within the DMA device. Table 9-15 and 9-16 show the state of the control signals and address lines and the functions performed by each. Note in Table 9-15 that control lines IWR(L) and IRD(L) (input write and input read), in conjunction with DMA(L) (DMA chip select) determine whether the addressed register is programmed or read. The I/O port address bit A3 specifies whether a channel register or mode set/status register is to be accessed. When A3 is set to "0", the channel registers are accessed. When A3 is set to "1", the mode set/status registers are accessed.

Table 9-15
DMA Input Control Lines

Register Selected	Connecting DMA Input Control Lines			Program Data To or Read Data From	I/O Port Address Bit A3(H)	Function
	DMA(L)	IWR(L)	IRD(L)			
Channel (n) DMA Address Register	0	0	1	LSB of DMA Address Register	0	Program LSB of DMA Address Register
		1	0			Read LSB of DMA Address Register
	0	0	1	MSB of DMA Address Register	0	Program MSB of DMA Address Register
		1	0			Read MSB of DMA Address Register
Channel (n) Terminal Count (TC) Register	0	0	1	LSB of TC Register	0	Program LSB of TC Register
		1	0			Read LSB of TC Register
	0	0	1	MSB of TC Register	0	Program MSB of TC Register
		1	0			Read MSB of TC Register
Mode Set Register	0	0	1	Mode Set Register	1	Program Mode Set Register
Status Register	0	1	0	Status Register	1	Read Status Register

Table 9-16
DMA I/O Port Address - Register Selection

I/O Port Addr	Register Selected	Byte	I/O Port Addr Inputs A3	A2	A1	A0	F/L	System Data Bus D7	D6	D5	D4	D3	D2	D1	D0
90	Channel 0 DMA Address	LSB	0	0	0	0	0	A7	A6	A5	A4	A3	A2	A1	A0
		MSB	0	0	0	0	1	A15	A14	A13	A12	A11	A10	A9	A8
91	Channel 0 TC	LSB	0	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0
		MSB	0	0	0	1	1	Rd	Wr	C13	C12	C11	C10	C9	C8
92	Channel 1 DMA Address	LSB	0	0	1	0	0	<------Same as Channel 0------>							
		MSB	0	0	1	0	1	<------Same as Channel 0------>							
93	Channel 1 TC	LSB	0	0	1	1	0	<------Same as Channel 0------>							
		MSB	0	0	1	1	1	<------Same as Channel 0------>							
94	Channel 2 DMA Address	LSB	0	1	0	0	0	<------Same as Channel 0------>							
		MSB	0	1	0	0	1	<------Same as Channel 0------>							
95	Channel 2 TC	LSB	0	1	0	1	0	<------Same as Channel 0------>							
		MSB	0	1	0	1	1	<------Same as Channel 0------>							
96	Channel 3 DMA Address	LSB	0	1	1	0	0	<------Same as Channel 0------>							
		MSB	0	1	1	0	1	<------Same as Channel 0------>							
97	Channel 3 TC	LSB	0	1	1	1	0	<------Same as Channel 0------>							
		MSB	0	1	1	1	1	<------Same as Channel 0------>							
98	Mode Set (program only)	---	1	0	0	0	0	AL	TCS	EW	RP	EN3	EN2	EN1	EN0
	Status (Read only)	---	1	0	0	0	0	0	0	0	UP	TC3	TC2	TC1	TC0

Table 9-16 is an expansion of Table 9-15 showing the I/O port address assignments for each of the ten registers. The rightmost hexadecimal digit in the I/O port address (0---8 represented by address lines A0---A3) designates the specific register being addressed. Note that I/O port address bit A3 is shown in both tables. The least significant I/O port address bits (A0---A2) designate the specific register to be accessed. When one of the channel registers is accessed, bit A0 selects either the DMA address register (A0=0) or the terminal count register (A0=1). Bits A1 and A2 specify which one of the four channels is accessed. When A3=1 and the mode set or status registers are accessed, A0---A2 are all zero.

Since the channel registers are 16 bits wide, two program instruction cycles are required to program or read an entire register. The DMA controller has an internal first/last (F/L) flip-flop that toggles at the completion of each program or read channel operation. The state of the flip-flop determines whether the lower or upper bytes of the register are to be accessed. The F/L flip-flop is reset by the DMA reset input or whenever the mode set register is loaded. To maintain proper synchronization, all channel command instruction operators occur in pairs. The lower byte of the register is accessed first, then the upper byte. The same I/O port address is used for both bytes.

Both the DMA address register and terminal count register must be initialized before a channel is enabled. Table 9-16 shows that the DMA address register is loaded with the first memory location to be accessed. The value loaded into the 14 least significant bits (C0---C13) of the terminal count register specifies the number of DMA cycles before the terminal count (TC) output is activated. When the specified number of data bytes are transferred, the DMA controller activates its terminal count (TC) output, informing the system processor that the DMA operation is completed. A terminal count of zero causes the TC output to be active in the first DMA cycle for that channel. Therefore, the value loaded into the lower-order 14 bits should be the number of DMA cycles minus one (N-1), where N is the desired number of DMA cycles. The two most significant bits in the terminal count registers specify the type of DMA operation for that channel as follows:

Bit 15	Bit 14	Type of DMA Operation
0	0	Verify DMA cycle
0	1	Write DMA cycle
1	0	Read DMA cycle
1	1	(Illegal)

Section 10

COMMUNICATIONS INTERFACE BOARD

INTRODUCTION

The Communications Interface board is attached to the rear panel inside the 8301. It is an extension of the System Controller board and contains the following functions:

- baud rate generator and switches
- RS-232-C compatible ports
- HSI port (RS-422 compatible)

The interface between the System Controller and this board is via 40-pin edge connectors on both boards and an interconnecting ribbon cable.

BAUD RATE GENERATOR AND SWITCHES

Fig. 10-1 is a functional block diagram showing how the baud rate generator divides a 1.2288 MHz frequency into eight baud rates. The 1.2288 MHz frequency is derived in the System Controller by dividing the 2.4576 MHz crystal oscillator by two. The eight baud rates are switch selectable. The baud rate switches are located adjacent to each RS-232-C compatible interface connector. These switches are slide-type and are operated from the 8301 back panel. The eight baud rates are:

110	1200
150	2400
300	4800
600	9600

RS-232-C COMPATIBLE PORTS

There are four RS-232-C compatible port connectors for connecting peripheral equipment to the 8301. Refer to Table 10-1. These connectors are labeled:

- J101 -- REMOTE (DTE)
- J102 -- REMOTE (DCE)
- J103 -- AUXILIARY
- J104 -- TERMINAL

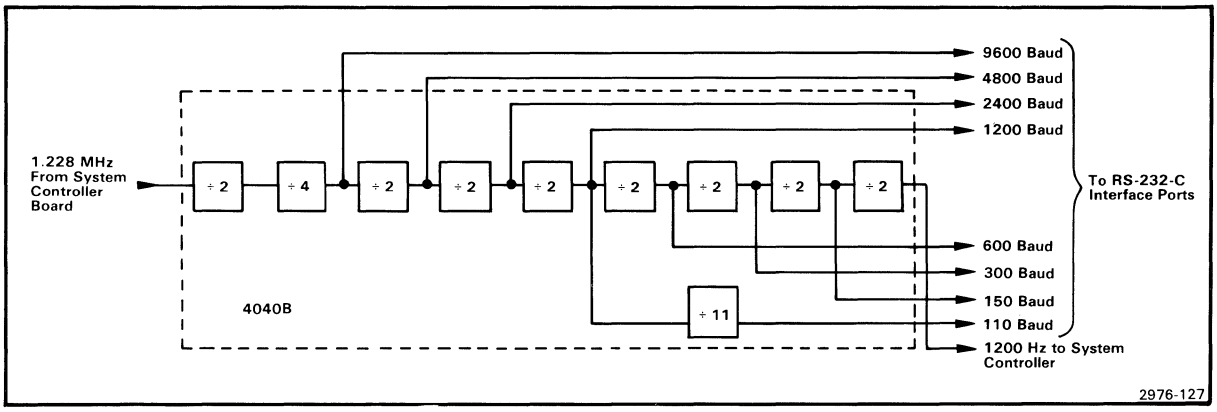


Fig. 10-1. Baud rate generator functional block diagram.

Table 10-1
Interface Connectors

Interface	Interface Connector	Connector Type	Function
Remote Communi-cations	J101	25-pin male	Interface to a Data Terminal Equipment (DTE) modem.
	J102	25-pin female	Interface to Data Communications Equipment (DCE). The selection of J101 or J102 is dependent on the setting of the MODE SELECT switch on the 8301 back panel.
System Terminal	J104	25-pin female	Interface to system terminal.
Auxiliary Terminal	J103	25-pin female	Interface to line printer or tape punch/ reader.
High-Speed Serial Interface	J100	25-pin	High-speed serial interface to DMU.

REMOTE PORT

The remote port interface is configured to use a modem for telephone data communications. This port is provided with a switch selectable DTE/DCE interface (Data Terminal Equipment/Data Communications Equipment). This switch is labeled MODE SELECT (S1030) and is operated from the 8301 back panel. The switch will select one of four interface modes as listed in Table 10-2.

Table 10-2
Mode Select Switch

Switch Label	Function
CNTL	No control
DTE1	DTE with CTS control
DTE2	DTE with DSR control
DCE	DCE with control

Refer to Section 2 of this manual Installation, for information on how to set this switch.

The remote port has two connectors: a male connector (labeled J101 -- DTE), and a female connector (labeled J102 -- DCE). Only one connector can be used at a time. The BAUD rate switch (S1060) adjacent to J102 selects one of eight baud rates for both connectors J101 and J102.

AUXILIARY PORT

The auxiliary port interface provides a DCE RS-232-C compatible interface. The BAUD rate switch (S1080) adjacent to J103 selects one of eight baud rates for this interface. In addition, an external clock baud rate connected to Pin 17 of J103 is available on a jumper-selected basis. Internal jumper J3 located on the Communications Interface board can be positioned to substitute the external baud rate for the normal 110 baud rate. See Section 2 of this manual Installation, for the location and proper setting of jumper J3. The external clock must be TTL-compatible.

TERMINAL PORT

The system terminal port interface is configured as a DCE RS-232-C compatible interface with control signals implemented. The BAUD rate switch (S1090) adjacent to J104 selects one of eight baud rates for this interface. This is the normal interface between the 8301 and the system terminal.

HSI PORT

The HSI port interface is configured as a RS-422 compatible interface. This interface is compatible with the electrical characteristics of a balanced-voltage (differential) digital interface circuit defined in the RS-422 standard. This is the normal interface between the 8301 and the DMU. The baud rate for this interface is 153.6k baud. Communications through the HSI port may be on a byte-by-byte basis under communication control lines CTS (Clear-To-Send) and DTR (Data-Terminal-Ready). Refer to Table 10-1 for information about this port.

Section 11

PROGRAM MEMORY BOARD

INTRODUCTION

The Program Memory board is a 32K static RAM. The Program Memory board has the following features:

- program/system select
- word/byte mode
- RAM inhabit
- low/high board select
- memory relocation
- extended bank
- I/O port interfaces

Four features are selected by internal jumpers: program/system select, low/high board select, memory relocation, and extended bank. The position of these internal jumpers determines the operational features and configuration selected for the memory board. The various features of the memory board are discussed in the following paragraphs. Refer to Section 2 of this manual Installation, for the location and correct setting of the internal jumpers on the memory board.

Figure 11-1 is a simplified functional block diagram of the Program Memory board. Refer to this figure as you read following paragraphs.

PROGRAM/SYSTEM SELECT

The setting of internal jumper J6179 (Program/System Jumper) determines whether the memory board will be used as Program Memory or System Memory. There is no operational difference when a memory board is used as Program or System Memory, other than the response to the state of the CMEM(H) control line. When the program/system jumper (J6179) is set for Program Memory operation, the memory board is operational when the CMEM(H) control line is high. For special applications when J6179 is set for System Memory operation, the memory board is operational when the CMEM(H) control line is low. This jumper will remain in the PROGRAM position for 8301 operations.

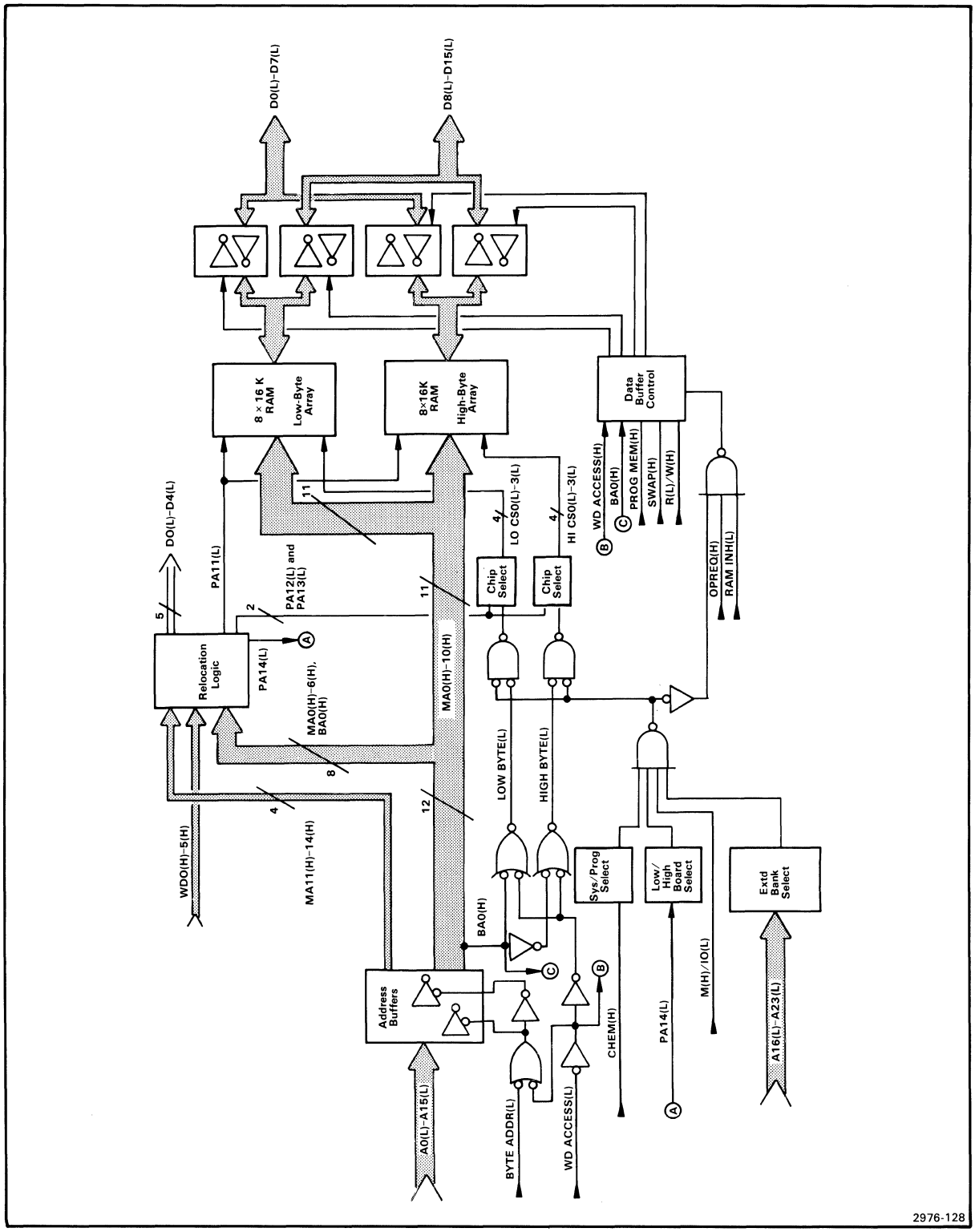


Fig. 11-1. Program Memory board functional block diagram.

WORD/BYTE MODE

The word/byte mode circuitry determines how the data from the data bus is stored in or read from the memory array banks. There are two 16K x 8 -bit memory arrays. When the byte mode is selected the two arrays are essentially arranged in series to form one array (8 x 32K). When the word mode is selected the two arrays are essentially arranged in parallel to form one array (16 x 16K). When the memory board is used as System Memory it will normally be in the byte mode position, since the system processor (2650A-1) is an 8-bit processor. When used as Program Memory the jumper will normally be in the byte mode for 8-bit emulator processors and in the word mode for 16-bit emulator processors. Word or byte mode of operation is selected by the states of the WD ACCESS(L) and BYTE ADDR(L) control lines, and the state of the BAO(H) address line, as shown in Table 11-1.

Table 11-1
Word or Byte Mode Operation

Control Lines	Mode Selection
BYTE ADDR(L) is asserted and BAO(H) is low (the bus address is even)	Byte mode is selected. Memory access line LOW BYTE(L) is asserted and the low memory is accessed.
BYTE ADDR(L) is asserted and BAO(H) is high (the bus address is odd)	Byte mode is selected. Memory access line HIGH BYTE(L) is asserted and the high memory array is accessed.
WD ACCESS(L) is asserted and BAO(H) is either high or low.	Word mode is selected. Memory access lines LOW BYTE(L) and HIGH BYTE(L) are both asserted. Both low and high memory arrays are accessed, providing storage for/reading of a 16-bit data word.

In the byte mode, the lower or higher arrays may be accessed by the upper eight data lines (D15--D8). When WD ACCESS(L) is high and SWAP(L) is low: the data is read from/written to the D15--D8 data lines, instead of D7--D0.

RAM INHIBIT

When the RAM INH(L) [RAM Inhibit] control line is asserted, the data buffer control is disabled. This disables both the read and write data buffers to/from the low and high memory arrays. All read and/or write operations to/from the memory arrays are inhibited.

LOW/HIGH BOARD SELECT

The position of the low/high board jumper (J6175) determines whether the 32K memory board responds to low or high memory access addresses. See Table 11-2.

Table 11-2
Low/High Board Jumper

Jumper Position	Memory Access Addresses
Low Board	0000 to 7FFF
High Board	8000 to FFFF

If the Low Board is selected, control line LOW BOARD(L) is asserted and the memory arrays are accessed whenever PA14(L) is high. If the High Board is selected, control line LOW BOARD(L) is unasserted and the memory arrays are accessed whenever PA14(L) is low. The state of PA14(L) is the same as that of A15(L). A15(L) is high for memory addresses 0000--7FFF and low for memory addresses 8000--FFFF. Remember, the common system address bus lines are all low on the Main Interconnect board. Refer to Section 2 of this manual Installation, for the location and correct setting of jumper, J6175.

MEMORY RELOCATION

The memory relocation circuitry permits 32K of the total 64K block of Program Memory addresses to be relocated to one 32K Program Memory board. The addresses are relocatable in 4K-byte blocks to even 4K boundaries.

Before discussing the memory relocation logic there are two address definitions that must be understood.

Bus Addresses	Those addresses present on the system address bus that are generated by the active processor.
Physical Addresses	Addresses that are presented to the chip-select decoders and the memory arrays on the memory board.

The memory relocation circuitry is enabled or disabled by internal jumper J5175. Refer to Section 2 of this manual Installation, for the location and correct setting of this jumper. When the memory relocation circuitry is enabled, addresses on the system address bus are converted or transformed to physical addresses. The four most significant bus address lines [A12(L)--A15(L)] are converted to physical address lines [PA11(L)--PA14(L)]. These physical address lines are presented to:

- the low/high board circuitry (previously discussed)
- the chip-select decoders
- the memory array address lines

Figure 11-2 is an example of how 32K of the 64K bus addresses may be relocated and converted into 32K of physical addresses. Note in the first three 4K blocks, that the bus addresses are the same as the physical addresses. However, the remaining bus addresses are converted to different physical addresses.

If a memory board is used as System Memory, memory relocation jumper J5175 must be in the "Disable" position. When a memory board is used as the Program Memory, the jumper may be set to either "Disable" or "Enable" position.

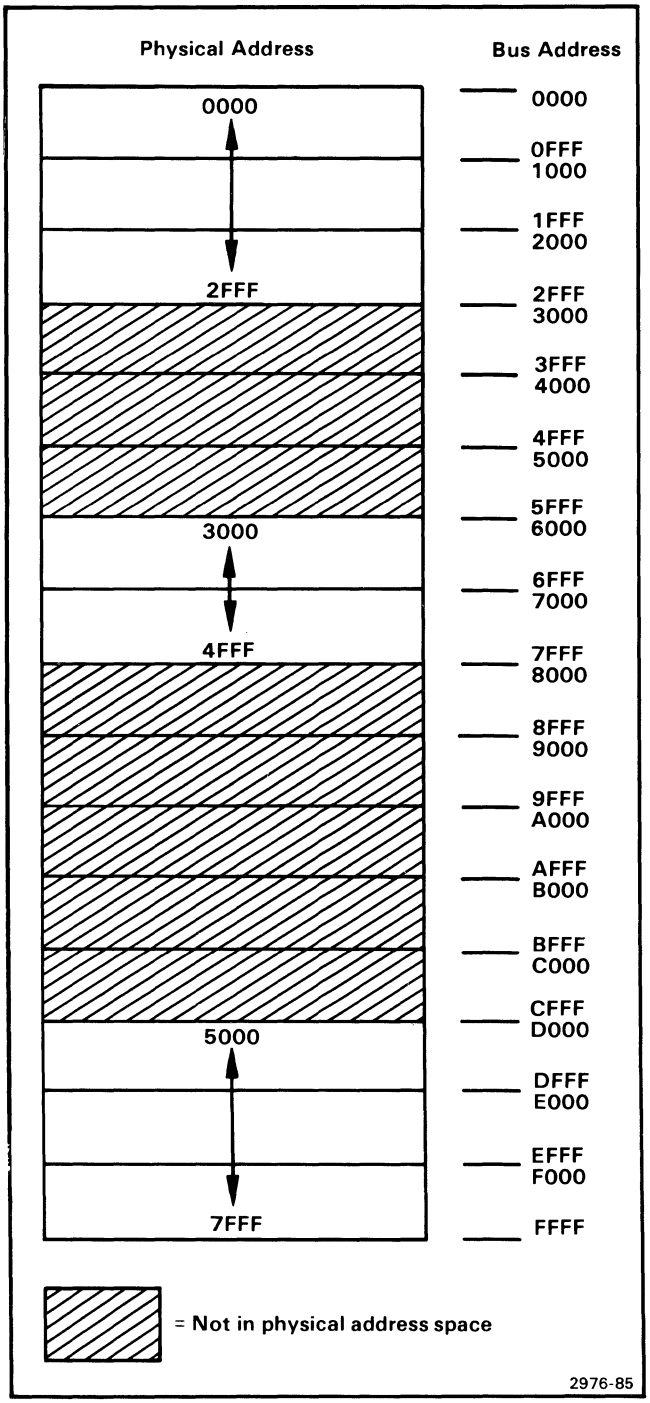


Fig. 11-2. Example of memory allocation.

EXTENDED BANK

The extended bank feature permits the utilization of the extended address lines, A16--A23, in the program section of the Main Interconnect board. The extended bank logic permits a block of program addresses (up to a maximum of 64K addresses) to be located to any even 64K address block within the 16M address space provided by the 24 address bus lines. The location of this 64K address block is determined by the settings of an eight-position DIP switch (S7170). The states of the eight most significant bits of the 24 address bus lines are set into the eight-position DIP switch. In addition, an internal jumper (J7171) is provided to enable or disable the extended bank feature. Refer to Section 2 of this manual Installation, for the location and proper settings of the switch and jumper.

I/O PORT INTERFACES

The system processor communicates with the Program Memory board through I/O port addresses E8 and E9. I/O port address E8 is used to address the low board (Program Memory addresses 0000--7FFF) and E9 is used to address the high board (Program Memory addresses 8000--FFFF). The decoder on the memory board decodes the I/O port addresses. The output of the decoder and the associated data byte of the I/O port address provides enabling and disabling of the memory relocation and extended bank features. Therefore, these features may also be enabled or disabled by software, in addition to jumpers J5175 and J7171.

NOTE

If either jumper J5175 (memory relocation) or J7171 (extended bank) is in the "Disable" position, that feature associated with the jumper cannot be enabled by software alone.

Section 12

EMULATOR CONTROLLER BOARD

INTRODUCTION

The Emulator Controller insures that only one processor (either system processor, emulator processor, or language processor) has control of the buses at any time. Since the system and program sections share the same 16-bit address and data buses (plus some of the control lines) bus contention could become a problem without the Emulator Controller. The location of the Emulator Controller board in J5 of the Main Interconnection board separates the system section from the program section for certain portions of the system bus structure. In addition, the Emulator Controller board supports the following software features that are available for any address within the total 16M program memory address space:

- Provides two program breakpoints that may be set for any address.
- Permits the emulator processor to be force-jumped to any address.
- Keeps track of the locations of the last program instruction address executed and the next program instruction address to be executed when an emulator/slave interrupt breakpoint occurs.

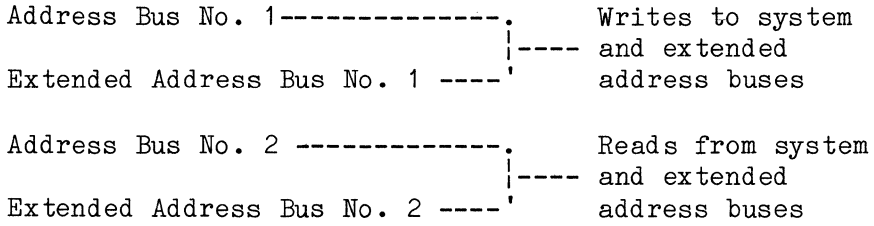
This section discusses the operation of the Emulator Controller, and is divided into the following functional categories:

1. Address and data buses
2. System processor/emulator processor control
3. Service (SVC) request detection
4. Breakpoint logic
5. Interrupt logic
6. Program Counter (PC) Last/Next storage registers
7. Forced jump logic
8. Extended bank switching
9. I/O port interfaces

ADDRESS AND DATA BUSES

Fig. 12-1 is a simplified functional block diagram of the Emulator Controller board. This figure clearly defines the four address buses and two data buses within the Emulator Controller board. These buses are listed as follows:

- Address Buses



- Data Buses

  Data Bus No. 1 ----- Data write bus

  Data Bus No. 2 ----- Data read bus

Note that all six buses are directional. The No. 1 address buses are used to transfer addresses from the Emulator Controller onto the system and extended address buses. The No. 2 address buses are used to bring addresses from the system and extended address buses to the various comparators and registers in the Emulator Controller. Data Bus No. 1 is used during a write operation to transfer data from the system data bus into the appropriate registers. Data Bus No. 2 is used during a read operation to transfer data from registers in the Emulator Controller onto the system data bus.

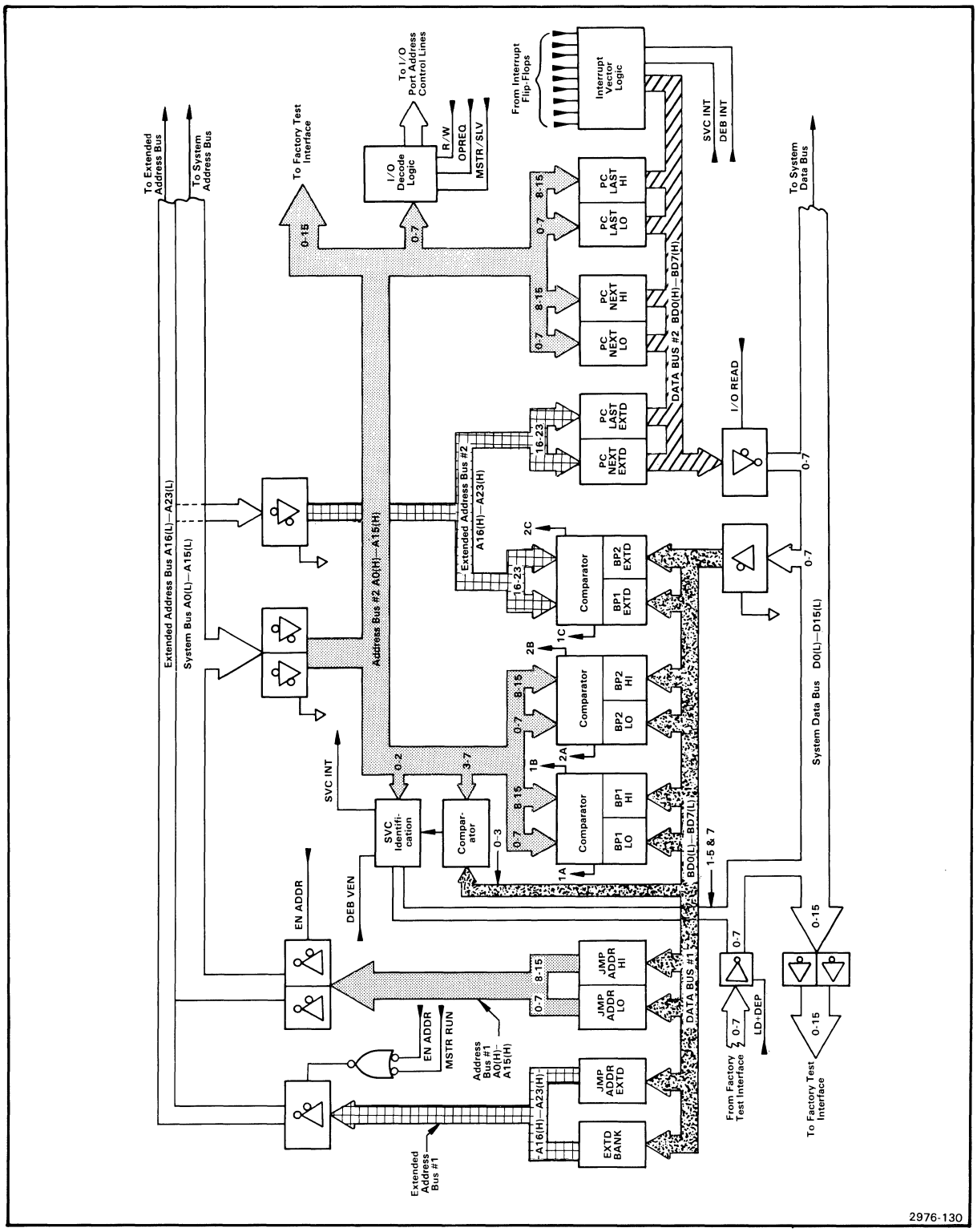


Fig. 12-1. Emulator Controller board functional block diagram.

SYSTEM PROCESSOR/EMULATOR PROCESSOR CONTROL

This function ensures that only one of the processors is allowed access to the address and data buses at a time. As previously mentioned, since the processors both share the same buses, only one is allowed to run at a time. This type of system is referred to as a master/slave arrangement. The system processor has the higher priority, and is referred to as the master. The emulator processor is the slave. Switching and control of the master/slave processors are accomplished as follows:

1. A separate control line [labeled MSTR PAUSE(L) or SLV PAUSE(L)] is monitored by each processor. When either of these lines is asserted the associated processor is halted.

2. By preventing the MSTR/SLV flip-flop from changing state until the active processor on the buses has halted, ensures that the master and slave processors will never be on the buses at the same time.

3. Flip-flops and gates are arranged to ensure that one of these PAUSE lines is always asserted, except during DMA operations. During DMA operations both the MSTR PAUSE(L) and SLV PAUSE(L) lines are asserted simultaneously. This pauses both processors and permits the DMA controller to assume control of the buses.

SERVICE (SVC) REQUEST DETECTION

SVCs allow a user's program to access data from an input device or transfer data to an output device. When an SVC is executed in a user's program, an SVC request is sent to the Emulator Controller. The SVC request logic recognizes a software "service request" from the active emulator processor and notifies the system processor of the interrupt.

An SVC mapping register allows SVCs to be mapped anywhere between 00---FF on even 16-byte boundaries. The SVC range defaults to F0---F7 on power-up or restart conditions.

An internal jumper (J5177) permits SVCs to occur during emulation modes 0 and 1. Refer to Section 2 of this manual Installation, for the location and proper setting of this jumper.

SVC mapping is accomplished by writing to I/O port address F3. SVCs are enabled or disabled by writing to bit 4 of the debug command port (I/O port address F9).

BREAKPOINT LOGIC

The breakpoint logic permits two independent breakpoints to be set into breakpoint registers for any address between 000000---FFFFFF (A0---A23). The breakpoint logic compares the address values from the system and extended address buses (A0---A23) with the values stored in the breakpoint registers. A breakpoint interrupt will occur when all of the following conditions are met:

- a match occurs between breakpoint registers and the address buses;
- the R/W line matches the break-on-read on break-or-write conditions set into the debug control register (I/O port address F8);
- no debug interrupt is pending;
- no forced jump address is in progress;
- SLV OPREQ(L) is asserted, indicating the emulator processor is active; and
- M(L)/IO(H) control line is low, permitting access to program memory.

INTERRUPT LOGIC

The Emulator Controller services all interrupts from the program section of the 8301. Priorities are assigned to these interrupts and the DBG INT(L) [debug interrupt] control line forwards the interrupt to the system processor. The interrupts are assigned priorities as follows (in desending order):

1. Service request interrupt--SVC INT
2. Breakpoint 1--BP1
3. Breakpoint 2--BP2
4. Single-cycle interrupt--S/CY INT
5. Slave halted interrupt--SLV HLT INT
6. Diagnostic interrupt--DIAG INT
7. Interrupt 29--INT 29
8. Interrupt 30--INT 30
9. Interrupt 31--INT 31

Four of the interrupts provide an immediate interrupt. That is, DBG INT(L) is generated immediately upon receipt of any of the following interrupts:

- SVC INT
- SLV HLT INT
- DIAG INT
- INT 30

The remaining interrupts provide a pending interrupt. That is, DBG INT(L) is not issued until the following FETCH cycle is received. This allows the address of the next instruction to be latched into the PC next registers prior to interrupting the active processor.

PC LAST/NEXT STORAGE REGISTERS

The PC Last/Next circuitry keeps track of the address location of the last instruction executed and the next instruction to be executed whenever a slave interrupt occurs.

When the emulator processor is executing instructions normally (that is no interrupts have occurred), the address of the current executing instruction is latched into three 8-bit PC Last latches (A0---A23). These 8-bit latches are continually updated as each program instruction is executed.

When a hardware or SVC interrupt is detected during program execution, the PC Last latches are no longer clocked and the address of the last instruction executed remains in the PC Last latches. When the emulator processor starts the execution of the next program instruction, the SLV FETCH pulse causes this instruction address to be latched into the 8-bit PC Next latches (A0---A23).

Therefore, the PC Last latches contain the address of where the program was interrupted and the PC Next latches contain the address of the next program instruction to be executed.

FORCED JUMP LOGIC

The forced jump logic forces the emulator processor to transfer program execution to a particular address. The jump address is loaded into the jump address registers with the three I/O port addresses listed in Table 12-1.

Table 12-1
Loading Jump Address Registers

I/O Port Address	Address Loaded With Associated Data Byte
FA --- (Write)	Lower eight address bits A0---A7
FB --- (Write)	Upper eight address bits A8---A15
F5 --- (Write)	Extended eight address bits A16---A23

A forced jump command (JMP CMD) is issued to the active emulator processor when any one or more of the following conditions exist:

- Bit 2 of I/O port address F9 is set low.
- Breakpoint 1 or 2 is enabled.
- Bit 4 of I/O port address F8 is set high, enabling single-cycle interrupt.
- An RTPA breakpoint is enabled (INT 29).

When a forced jump command is issued to the active emulator processor, the processor responds by asserting the jump acknowledge control line [JMP ACK(L)]. When this line is asserted, the forced jump address is gated onto the system and extended address buses.

EXTENDED BANK SWITCHING

The 8-bit extended bank switch register is loaded by writing to I/O port address F4. The extended address is gated onto the extended address bus when control line EN ADDR(L) is asserted, indicating the system processor is active. This circuitry permits the system processor to address the extended address range.

I/O PORT INTERFACES

As previously stated, the system processor communicates with the various boards by means of I/O port addresses and the associated data bytes. The I/O port addresses for the Emulator Controller board are divided into the following functions:

- Functional Decoder (Read/Write)
- I/O Decoder (Read)
- I/O Decoder (Write)

- Extended Address Decoder (Read/Write)

The lower-order address bus lines (A0---A7) are decoded to determine which I/O port is accessed. Table 12-2 lists the I/O port address assignments for the Emulator Controller.

Figure 12-2 is a simplified block diagram of the Emulator Controller decoders. Refer to this figure during the following explanation of the I/O port interfaces.

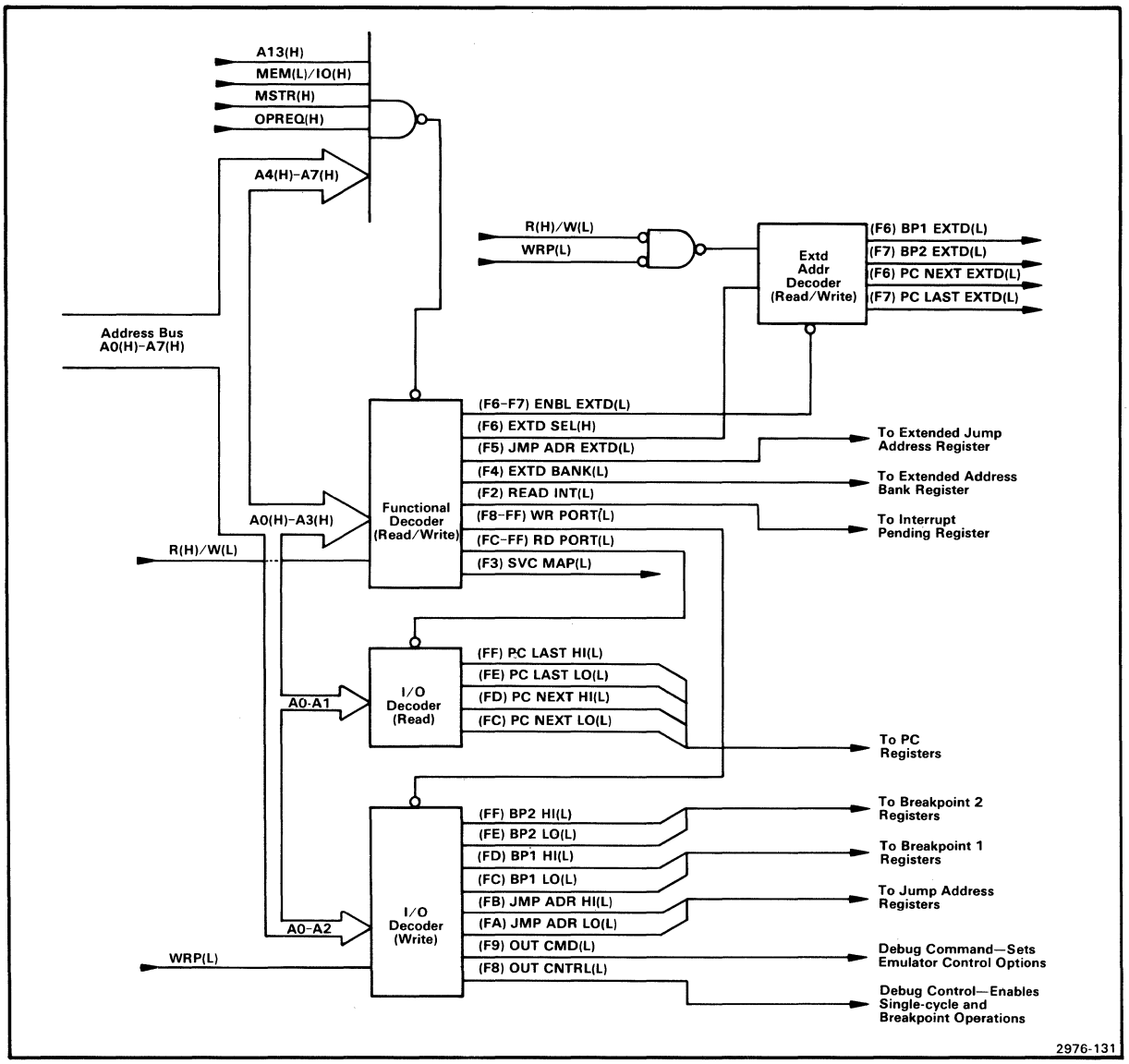


Fig. 12-2. Emulator Controller Decoders simplified block diagram.

Table 12-2
Emulator Controller I/O Port Address Assignments

Port Address	Read/Write	Function
F0	R/W	Reserved (decoded but not assigned)
F1	R/W	Reserved (decoded but not assigned)
F2	R	Pending interrupts port
F3	W	SVC mapping port
F4	W	Extended bank switch
F5	W	Jump address extended
F6	R	Program Counter Next, extended
F6	W	Breakpoint 1, extended
F7	R	Program Counter Last, extended
F7	W	Breakpoint 2, extended
F8	W	Debug control port
F9	W	Debug command port
FA	W	Jump address, lower-order
FB	W	Jump address, higher-order
FC	R	Program Counter Next, lower-order
FC	W	Breakpoint 1, lower-order
FD	R	Program Counter Next, higher-order
FD	W	Breakpoint 1, higher-order
FE	R	Program Counter Last, lower-order
FE	W	Breakpoint 2, lower-order
FF	R	Program Counter Last, higher-order
FF	W	Breakpoint 2, higher-order

FUNCTIONAL DECODER (READ/WRITE)

The functional decoder utilizes an IM5610 device (PROM) to decode the lower four address bits (A0---A3). The PROM is enabled when all of the following conditions are met: (Refer to Tables 12-3 and 12-4.)

1. control line MSTR(H) is high, indicating that the system processor is active;

2. control line MEM(L)/IO(H) is high, indicating the execution of an I/O instruction;

3. control line OPREQ(H) is high, indicating the start of a bus operation;

4. address line A13(H) is high, indicating an extended I/O address; and

5. address lines A4(H)---A7(H) are all high, indicating an I/O port address F0---FF is on the address bus.

Table 12-3
Enabling Functional Decoder

I/O Port Addresses	OPREQ(H)	MSTR(H)	MEM(L)/ IO(H)	A13	A7 A6 A5 A4	Function
F0---FF	1	1	1	1	1 1 1 1	When all input lines to the NAND gate are high during I/O port addresses F0---FF, the NAND gate's output goes low, enabling the functional decoder.

Table 12-4
Functional Decoder Input and Output Lines

Decoder Input Control Lines							Output Control Lines From Decoder	
R/W Oper	I/O Port Addr	A3	A2	A1	A0	R(H)/ W(L)	Output Control Line Name	Function
R	F2	0	0	1	0	1	READ INT(L)	Forces pending interrupts in interrupt registers onto data bus.
W	F3	0	0	1	1	0	SVC MAP(L)	Sets I/O address bits, A7--A4, for emulator SVCs.
W	F4	0	1	0	0	0	EXTD BANK(L)	Sets address bits,A23--A16, for system processor access to program memory.
W	F5	0	1	0	1	0	JMP ADR EXTD(L)	Sets extended address bits, A23--A16, of a forced jump address.
R	F6	0	1	1	0	1	EXTD SEL(H) (is low)	Sets input control line of extended address decoder to select PC NEXT EXTD register on read operation or BP1 EXTD register on write operation.
W						0		

Table 12-4 (cont)

Decoder Input Control Lines						Output Control Lines From Decoder	
R/W Oper	I/O Port Addr	A3	A2	A1	A0	R(H)/W(L)	Output Control Line Name	Function
R	F7	0	1	1	1	1	EXTD SEL(H) (is high)	Sets input control line of extended address decoder to select PC LAST EXTD register on read operation or BP2 EXTD register on write operation.
W						0		
R	F6	0	1	1	0	1	ENBL EXTD(L)	I/O port addresses F6 and F7 set control line ENBL EXTD(L) low enabling the extended address decoder during both read and write operations.
W						0		
R	F7	0	1	1	1	1		
W						0		
W	F8	1	0	0	0	0	WR PORT(L)	I/O port address F8 through FF set control line WR PORT(L) low enabling the I/O decoder (write) during all write operations to these I/O port addresses. (See Table 2-15.)
	F9	1	0	0	1			
	FA	1	0	1	0			
	FB	1	0	1	1			
	FC	1	1	0	0			
	FD	1	1	0	1			
	FE	1	1	1	0			
	FF	1	1	1	1			
R	FC	1	1	0	0	1	RD PORT(L)	I/O port addresses FC through FF set control line RD PORT(L) low enabling the I/O decoder (read) during all read operations to these I/O port addresses. (See Table 2-14.)
	FD	1	1	0	1			
	FE	1	1	1	0			
	FF	1	1	1	1			

I/O DECODER (READ)

During a read operation, I/O port addresses FC---FF cause control line RD PORT(L) from the functional decoder to be asserted. This enables the I/O decoder (read). The lower two address lines (A0 and A1) determine which I/O port is accessed. See Table 12-5. The output control lines from this decoder force the appropriate PC Next/Last address onto the data bus to be read by the system processor.

I/O DECODER (WRITE)

During a write operation, I/O port addresses F8---FF cause control line WR PORT(L) from the functional decoder to be asserted. This enables the I/O decoder (write). The lower three address lines (A0---A2) determine which I/O port is accessed. See Table 12-6. The output control lines from this decoder writes the associated data byte into the selected registers. The registers are designated by the specific I/O port address.

EXTENDED ADDRESS DECODER (READ/WRITE)

This decoder is enabled when I/O port address F6 or F7 is on the address bus. The states of the two decoder input lines determine which output line is asserted. During read operations, either I/O address F6 or F7 causes the extended PC Next/Last address to be forced onto the data bus. During write operations, either I/O address F6 or F7 permits data to be written into BP1 or BP2 registers. See Table 12-7.

Table 12-5
I/O Decoder (Read) Input and Output Lines

Decoder Enabling and Input Control Lines					Output Control Lines From Decoder	
I/O Port Addr	Type of Oper	RD PORT(L)	A1	A0	Output Control Line Name	Function
FC	Read	0	0	0	PC NEXT LO(L)	Forces A7--A0 of next instruction onto data bus after interrupt.
FD	Read	0	0	1	PC NEXT HI(L)	Forces A15--A8 of next instruction onto data bus after interrupt.
FE	Read	0	1	0	PC LAST LO(L)	Forces A7--A0 of last instruction onto data bus after interrupt.
FF	Read	0	1	1	PC LAST HI(L)	Forces A15--A8 of last instruction onto data bus after interrupt.

Table 12-6
I/O Decoder (Write) Input and Output Lines

Decoder Enabling and Input Control Lines							Output Control Lines From Decoder	
I/O Port Addr	Type of Oper	WR PORT (L)	WRP (L)	A2	A1	A0	Output Control Line Name	Function
F8	Write	0	0	0	0	0	OUT CNTRL(L)	Debug Control Port--enables S/C and BP registers.
F9	Write	0	0	0	0	1	OUT CMD(L)	Debug Command Port -- sets emulator processor control functions.
FA	Write	0	0	0	1	0	JMP ADR LO(L)	Forced Jump Address A7--A0 is loaded into jump address registers.
FB	Write	0	0	0	1	1	JMP ADR HI(L)	Forced Jump Address A15--A8 is loaded into jump address registers.
FC	Write	0	0	1	0	0	BP1 LO(L)	BP1 Address A7--A0 is loaded into BP1 comparison register.
FD	Write	0	0	1	0	1	BP1 HI(L)	BP1 Address A15--A8 is loaded into BP1 comparison register.
FE	Write	0	0	1	1	0	BP2 LO(L)	BP2 Address A7--A0 is loaded into BP2 comparison register.
FF	Write	0	0	1	1	1	BP2 HI(L)	BP2 Address A15--A8 is loaded into BP2 comparison register.

Table 12-7
Extended Address Decoder Input and Output Lines

Decoder Enabling and Input Control Lines						Output Control Lines From Decoder	
I/O Port Addr	Type of Oper	ENBL EXTD (L)	EXTD SEL (L)	R(H)/ W(L)	WRP (L)	Output Control Line	Function
F6	W	0	0	0	0	BP1 EXTD(L)	BP1 Extended Address A23--A16 is loaded into EXTD BP1 comparison register
F7	W	0	1	0	0	BP2 EXTD(L)	BP2 Extended Address A23--A16 is loaded into EXTD BP2 comparison register
F6	R	0	0	1	X	PC NEXT EXTD(L)	Forces bits A23--A16 of next instruction executed by emulator processor onto the data bus after an interrupt.
F7	R	0	1	1	X	PC LAST EXTD(L)	Forces bits A23--A16 of last instruction executed by emulator processor onto the data bus after an interrupt.

Section 13

LANGUAGE PROCESSOR BOARD

INTRODUCTION

The Language Processor utilizes a Z80A microprocessor and operates much like an emulator processor. The Language Processor uses Program Memory to translate source code (assembly language) to binary object code (machine language) for use by the emulator processor. The Language Processor operates as a slave to the system processor and is invoked by software commands entered at the system terminal.

The Language Processor board is divided into the following functions:

- Z80A CPU and Clock Generation
- Address and Data Bus Buffers
- Control Bus Signal Generation
- Execution Control
- I/O Port Interfaces

Figure 13-1 is a simplified schematic of the Language Processor board. Refer to this figure as you read the following discussions on the Language Processor functions.

Z80A CPU AND CLOCK GENERATION

The Z80A microprocessor in the Language Processor is capable of operating at two clock rates: SLOW (2.5 MHz) and FAST (4.0 MHz). An internal jumper (J4029) selects either SLOW or FAST mode. In the FAST mode, the "Debug Sequencer On" control bit (bit 2 of I/O port address E7) determines the clock rate: When this bit is high, SLOW mode is selected.

The SLOW clock is derived from the 2650 CLK (10 MHz) generated on the System Controller board. The FAST clock is derived from a 16 MHz crystal oscillator on the Language Processor board. The two clock sources (10 MHz and 16 MHz) are fed to a multiplexer. The multiplexer output (either 10 MHz or 16 MHz) depends on the position of jumper J4029 and the state of the "Debug Sequencer On" control bit. A divide-by-four circuit converts the multiplexer output to either 2.5 MHz or 4 MHz.

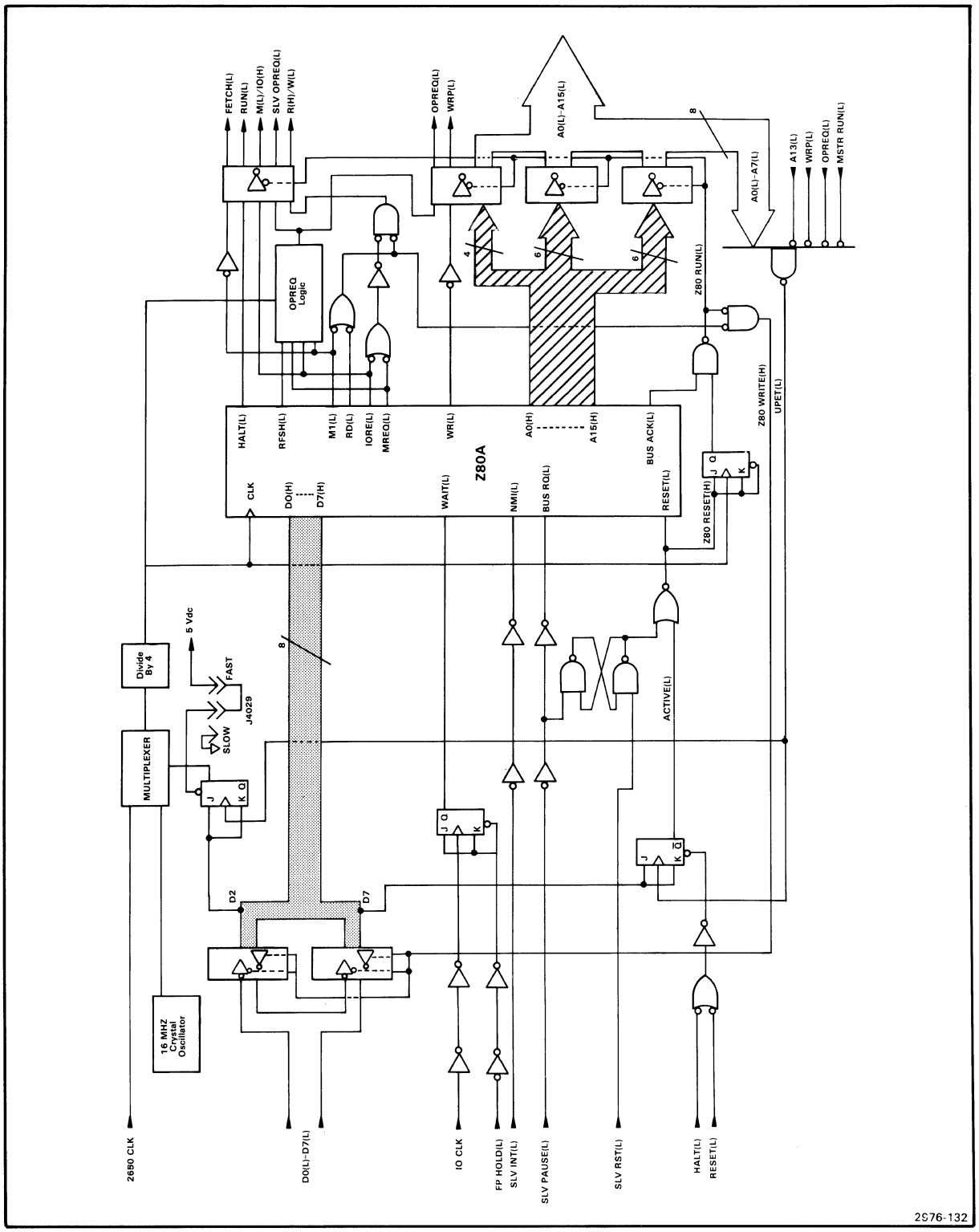


Fig. 13-1. Language Processor simplified schematic.

ADDRESS AND DATA BUS BUFFERS

The Z80A address bus is buffered by tristate buffers. These buffers are directional and are enabled whenever the Z80A is running. This forces the Z80A addresses onto the system address bus.

The Z80A data bus is also tristate buffered. These buffers are bidirectional. The direction of data through these buffers is controlled by the state of control line Z80 WRITE(H). During a write operation this control line is high, permitting the microprocessor to write data onto the system data bus. During a read operation this control line is low, permitting the Z80A to read data from the system data bus.

CONTROL BUS SIGNAL GENERATION

The Z80A control signals [M1(L), RD(L), MREQ(L), and IOREQ(L)] are converted by logic gates to 8301 control signals. These converted signals are buffered by directional buffers that are enabled whenever the Z80A is running, forcing the Z80A control signals onto the system control lines.

The Z80 OPREQ(H) is generated by a combination of Z80A control signals [M1(L), MREQ(L), IOREQ(L), and RFSH(L)] and the Z80A clock. The Z80 OPREQ(H) goes high on the next clock edge after the Z80A control signals are true and goes low immediately if any control signal becomes false. RFSH(L) is utilized to ensure that a false Z80 OPREQ signal is not generated during memory refresh operations.

EXECUTION CONTROL

The Z80A microprocessor is controlled by the Emulator Controller. Control lines from the Emulator Controller are used for execution control of the Z80A microprocessor. These control lines are:

- SLV PAUSE(L)
- SLV RESET(L)
- F.P. HOLD(L)
- RESET(L)

Control lines RESET(L) or HALT(L) generate a RESET(L) to the Z80A microprocessor by clearing the "ACTIVE" flip-flop. This causes ACTIVE(L) to go high and RESET(L) to go low, resetting the microprocessor. SLV RESET(L) sets the S-R flip-flop holding RESET(L) low.

The BUS RQ(L) input is used to suspend execution of the Z80A microprocessor and not alter the contents of the processor's registers. When SLV PAUSE(L) is asserted, a BUS RQ(L) is generated.

F.P. HOLD(L) is generated by the Emulator Controller to freeze processor execution during a Z80A machine cycle. When F.P. HOLD(L) is asserted, wait states are generated by the Z80A.

I/O PORT INTERFACES

The Language Processor is controlled by the system processor through I/O port address E7 and the associated data byte. Data bit D2 selects a slow or fast clock rate (2.5 MHz or 4.0 MHz) for the Z80A processor. Data bit D7 activates or deactivates the Language Processor board.

Section 14

FRONT PANEL BOARD

INTRODUCTION

The Front Panel board is attached to the Front Control Panel. The RESTART switch and four LEDs are mounted on the Front Panel board and extend through cutouts in the Front Control Panel.

INTERCONNECTING CABLES

Two interconnecting ribbon cables (8 conductors each) connect the Front Panel board connector (J1) to the Main Interconnect board connector (J17). The connectors on the interconnecting cables are designated, P1 and P17, corresponding to the board mounted connectors, J1 and J17 respectively. All input/output connections for the Front Panel board terminate in J1; a 16-pin harmonica connector located on the Front Panel board. Table 14-1 shows the pin connections for both J1/P1 and J17/P17.

NOTE

In Table 14-1 the pin numbers of the interconnecting connectors (P1 and P17) are shown. Note that there is no correlation between corresponding pin numbers of P1 and P17. When connecting either P1 or P17, you must match pin 1 of the "P" connector with pin 1 of the "J" connector. A small white dot designates pin 1 of the "P" connectors. A small arrowhead designates pin 1 of the "J" connectors. Use care when connecting either P1 or P17, the harmonica connectors are easily misaligned.

Table 14-1
Pin Numbers of J1/P1 and J17/P17

Front Panel Board	Main Interconnect Board	
J1/P1 Pin Number	J17/P17 Pin Number	System Bus Line Name
9	1	+5 Vdc
10	2	PAUSE(L)
11	3	RUN(L)
12	4	GROUND
13	5	SELF TEST(L)
14	6	GROUND
15	7	SLV PSE(L)
16	8	+5 Vdc
1	9	+5 Vdc
2	10	MSTR PSE(L)
3	11	GROUND
4	12	RESET(L)
5	13	GROUND
6	14	MSTR RUN(L)
7	15	GROUND
8	16	+5 Vdc

REMOVAL OF FRONT CONTROL PANEL AND FRONT PANEL BOARD

CAUTION

120/240 volts is on the main POWER switch attached to the Front Control Panel when the main power cord is attached to the 8301 mainframe. Therefore, before removing the Front Panel board or the Front Control Panel, insure that the main power cord is removed from the back of the 8301 mainframe. Never operate the 8301 MDU with the Front Control Panel removed or when the spring clips are disengaged.

The Front Panel board and the Front Control Panel are attached to the front of the 8301 mainframe by spring clips on each side of the Front Control Panel. The following procedure describes how to remove the Front Control Panel:

1. Remove main power cord from back of 8301 mainframe.

2. Remove the right top and bottom cover screws and cover retainers from the rear of the 8301.

3. Slide the right side cover to the rear of the instrument approximately three to four inches.

4. The right spring clip on the Front Control Panel may be disengaged by inserting your index finger through the square hole in the side of the mainframe.

5. Pull the Front Control Panel forward and remove the connectors from the Front Panel board. Be sure the color coding and orientation of P1 are noted. This harmonica connector can be connected backwards.

REINSTALLATION OF FRONT CONTROL PANEL

Reinstall the Front Control Panel as follows:

1. Connect all connectors.

2. Insert left side of Front Control Panel first and push panel in until the spring clips are engaged.

Section 15

POWER SUPPLIES

INTRODUCTION

This section describes the DC power supplies in the 8301. There are two 12 Vdc supplies and one 5 Vdc supply. The schematic diagrams for these power supplies are in Volume II, Section 17, Sheet 22 in this manual. Sheet 21 shows the primary power distribution and how the power supplies are connected to the primary input power transformer, T311.

The two 12 Vdc supplies are identical. One has its positive output terminal grounded and the other has its negative output terminal grounded, thereby providing a -12 Vdc and +12 Vdc power supplies. Refer to the rightmost diagrams in Volume II, Section 17, Sheets 21 and 22.

The 5 Vdc supply has its negative output terminal grounded which provides a +5 Vdc power supply. Refer to the rightmost diagram in Volume II, Section 17, Sheet 21 and the leftmost diagram on Sheet 22.

CIRCUIT DESCRIPTION

The circuit description for both 5 and 12 Vdc supplies is very similar. The control circuitry is almost identical for both supplies. The input and output components of the +5 Vdc supply are beefed-up to handle the additional current capabilities. The 5 Vdc supply has 6 series pass transistors, Q2 through Q6. These are in a series/parallel arrangement that provides a maximum output current of 35 amps. The 12 Vdc supply has only one transistor, Q1, that provides a maximum output current of 1.7 amps. Due to the similarity of the two power supplies, only the +5 Vdc power supply circuit description will be covered in this manual. Refer to the leftmost diagram in Volume II, Section 17, Sheet 22.

The control circuitry in these supplies is centered around the 723 voltage regulator device, U1. There are three functions performed by the control circuitry:

- Voltage regulation and adjustment
- Current limiting and adjustment
- Overvoltage protection and adjustment

VOLTAGE REGULATION AND ADJUSTMENT

A voltage divider network consisting of R37, R43 (Voltage Adjust), R28, R29, and R38 is across the positive and negative output terminals. Within the 723 device, pins 4 and 5 are the inputs to an error amplifier. Outside the device these pins are connected across R28. Therefore the voltage drop across R28 is the input to the error amplifier. An internal voltage regulator provides a reference voltage between pins 5 and 6. When the 5 Vdc supply output voltage drops, the voltage across R28 decreases. This decrease to the input of the error amplifier causes the voltage at pin 10 to increase. Increasing the voltage at pin 10 increases the drive through Q1 which also increases the drive of the 6 series pass transistors. This brings the output voltage up until it balances with the reference voltage.

R43 (Voltage Adjust) is in series with R28. Adjusting R43 also changes the voltage across R28 and permits adjustment of the output voltage. In the 5 Vdc supply, R43 provides an adjustment in the output voltage from 4.75 to 7.0 Vdc. In the 12 Vdc supplies, R20 provides an adjustment in the output voltage from 10.5 to 15.75 Vdc.

CURRENT LIMITING AND ADJUSTMENT

The current limiting adjustment (R23) is set for the maximum current of 35 amps for the 5 Vdc supply. (R3 is set for a maximum current of 1.7 amps for the 12 Vdc supplies.) Pins 2 and 3 of U1 are connected to the base and emitter of a transistor within the 723 device. R23 (Current Limit) and R24 form a voltage divider network that establishes a voltage at pin 2.

When the current in the 5 Vdc supply is increased, the voltage tends to decrease. This decrease increases the drive through Q1 as described previously under Voltage Regulation. This also changes the voltage drop across R23 and R24 and the voltage between pins 2 and 3 (connected to the base and emitter of the internal current limiter). If the output current of 35 amps is exceeded, the internal current limiter is turned on and the supply goes out of regulation. As you exceed the 35 amp limit, the output voltage decreases accordingly.

OVERVOLTAGE PROTECTION AND ADJUSTMENT

The overvoltage protection circuitry consists of Q9, CR9, SCR1, SCR2, and associated resistors. The emitter of Q9 is connected directly to the positive output terminal. R30 and R31 (Over Voltage) form a voltage divider across the positive and negative output terminals. The voltage at the junction of R30 and R31 determines when CR9 will turn on. As the 5 Vdc output voltage increases, the voltage drop across R31 increases until CR9 fires. This turns on Q9 whose collector is connected to the gate of SCR1; turning it on. When SCR1 is turned on two things happen:

1. SCR2 is turned on which crowbars the output.

2. The base drive to the 6 series pass transistors is reduced.

This shuts the power supply down rapidly. When SCR2 is turned on, the output drops to approximately one volt. Once this happens the main power switch must be turned off and then turned on again to reset the gates on SCR1 and SCR2. R31 is adjusted to ensure that the supply shuts down at 6.2 Vdc +/-0.1 V. (R13 for the 12 Vdc supply is adjusted to ensure shut down at 13.3 Vdc +/-0.2 V.)

POWER SUPPLY ADJUSTMENTS

The three adjustments on each power supply are interactive and require the adjustments to be made in a certain order as follows:

1. Over Voltage
2. Voltage Adjust
3. Current Limit

CAUTION

The power supplies are set at the factory to the proper voltages and currents. They are adjusted to conform to UL specifications and the adjustment pots sealed. Avoid power supply adjustments whenever possible. However, if it becomes necessary to make any changes to the adjustments, refer to Section 8 in this manual for detailed calibration procedures. Follow these procedures carefully.

REMOVAL AND REPLACEMENT OF POWER SUPPLIES

Section 8 in this manual contains step-by-step procedures for the removal and replacement of the power supplies.

Section 16

SYSTEM RAM BOARD

INTRODUCTION

The System RAM board operates in byte mode only and must be installed on the system side of the Emulator Controller board in the Main Interconnect board. This board can only be utilized as the system memory.

The System RAM board is a 64K dynamic RAM that contains the following major functions:

- Address and Data Buses
- RAM Controller and Memory Array
- Refresh Logic
- Write Protect
- Page Switching
- Parity Error Logic
- Diagnostic provisions
- I/O Port Interfaces

Figure 16-1 is a functional block diagram of the System RAM board. Refer to this figure and to the board schematics in the rear of this manual as you read the following paragraphs.

ADDRESS AND DATA BUSES

Figure 16-1 shows the one address bus and three data buses for the System RAM board. These four buses are designated as follows:

- Address Bus --- A0(H)--A15(H)
- Data Bus --- D0(H)--D7(H) (write data bus)
- Data Bus --- D00(H)--D07(H) (read data bus from memory array)
- Data Bus --- DB0(H)--DB7(H) (read data bus)

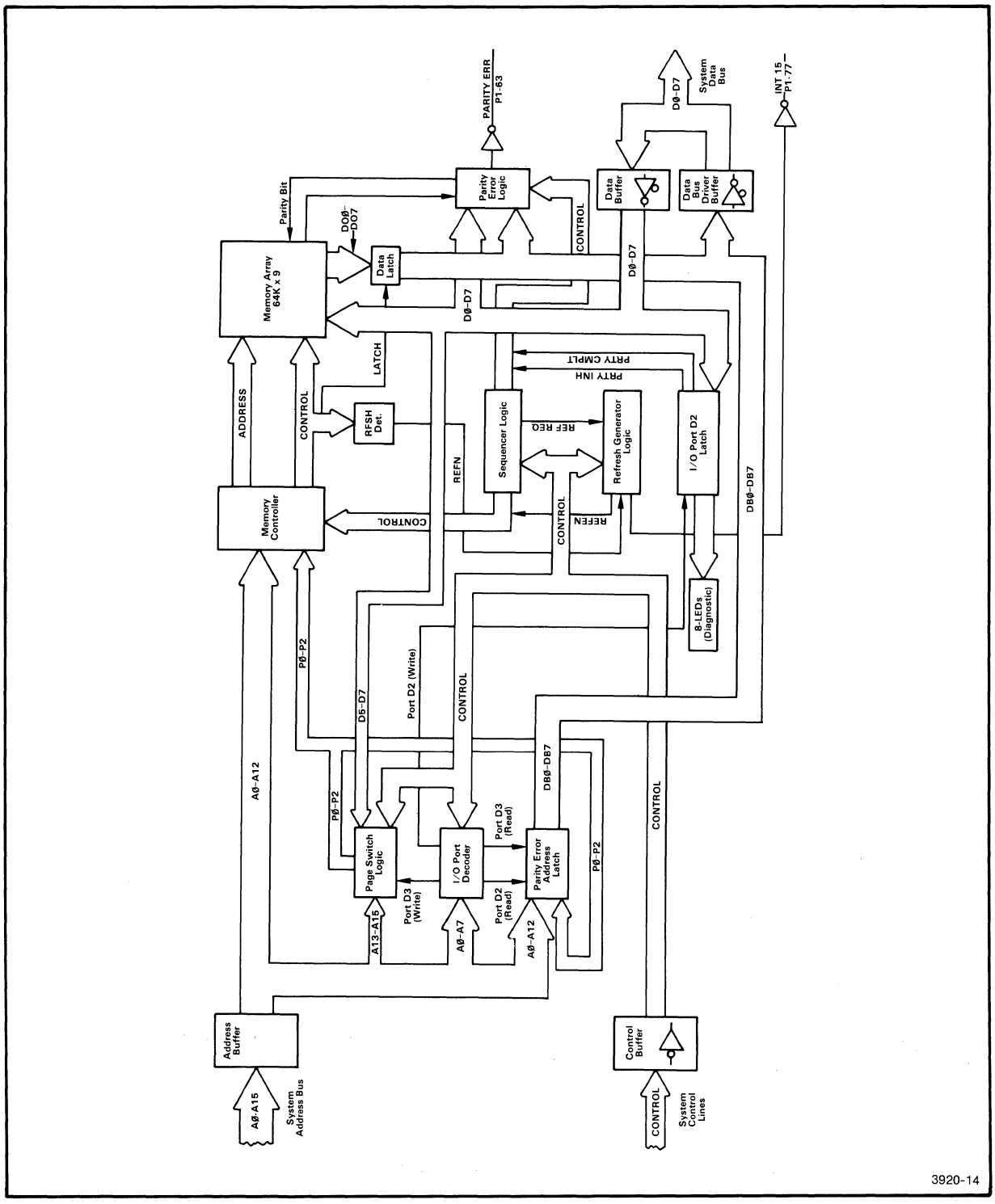


Fig. 16-1. System RAM functional block diagram.

ADDRESS BUS

The System Address Bus is complemented by directional buffers U5020 and U5030. This complemented bus, A0(H)--A15(H), is used for all addressing functions for the System RAM board.

DATA BUSES

Figure 16-2 is a simplified schematic diagram of the three data buses on the System RAM board. The associated buffers and latches ensure that the correct data is sent to or received from the System Data Bus.

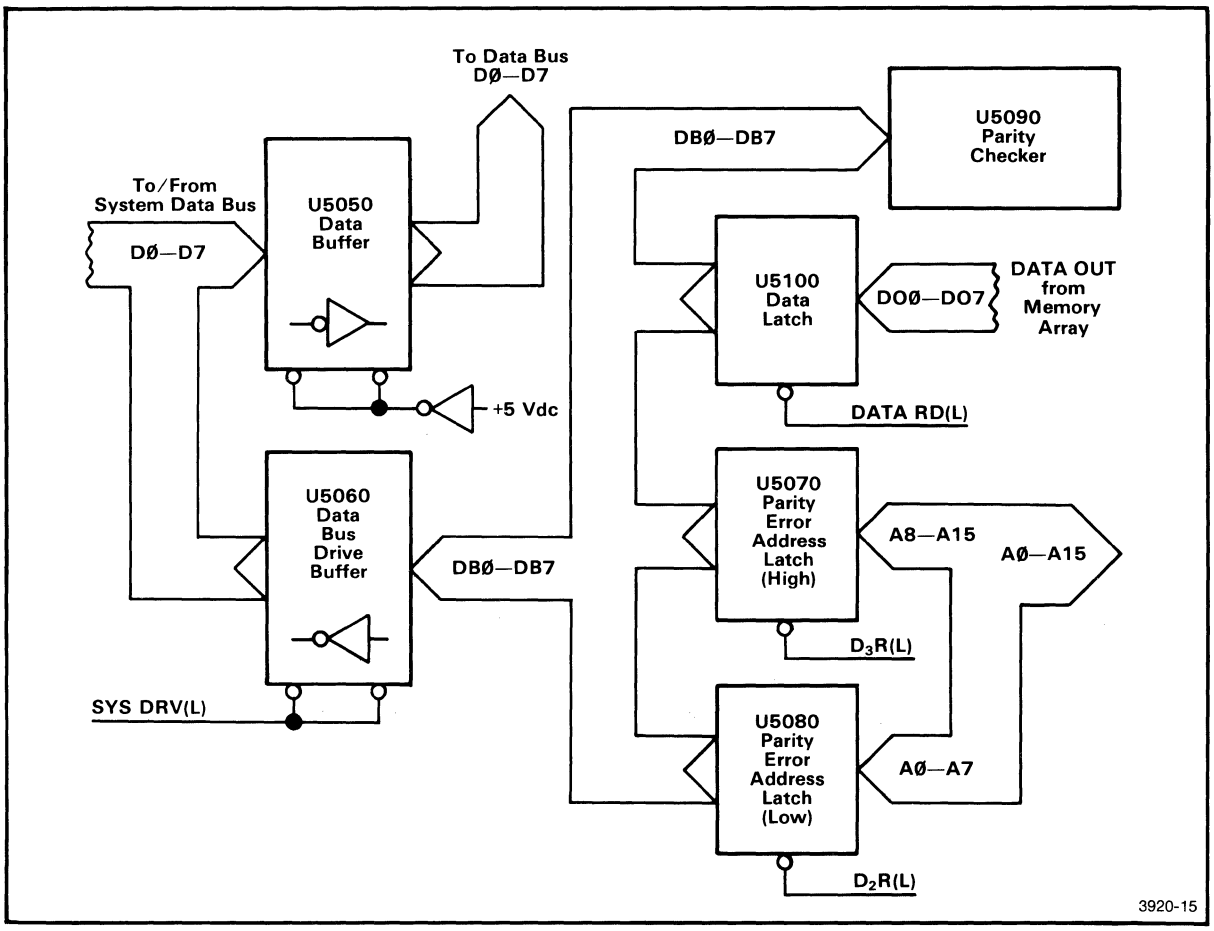


Fig. 16-2. System RAM board data buses.

On a write operation, Data Bus Drive Buffer U5060 is disabled. Since Data Buffer U5050 is always enabled, data from the System Address Bus passes through U5050 and appears on the data write bus as D0(H)--D7(H). This bus is used during a write to memory or a write to I/O ports D2 and D3.

During an I/O read to either port address D2 or D3, Data Bus Drive Buffer U5060 is enabled. D2 (read) also enables Parity Error Address Latch U5080 and D3 (read) enables Parity Error Address Latch U5070. This permits the system processor to read the low and high bytes of the parity error address.

When the system processor is not making an I/O read to either port address D2 or D3, Data RD(L) is low, enabling Data Latch U5100 and disabling Parity Error Address Latches U5070 and U5080. This latches the Data Out bus, D00(H)--D07(H), from the memory array onto the read data bus DB0(H)--DB7(H). Parity Checker U5090 checks the data from the memory array for an even parity. During a system processor memory read, SYS DRV(L) is also low, enabling Data Bus Drive Buffer U5060. The data on the data read bus, DB0(H)--DB7(H), passes through U5060 and appears on the System Data Bus.

RAM CONTROLLER AND MEMORY ARRAY

The memory array is physically configured in four banks, with nine dynamic RAM devices (type-2118) in each bank. The storage capacity of each RAM is 16K x 1-bit. Eight RAMs in each bank are used for data storage and one RAM for parity. This provides a total memory storage capacity of 64k bytes of data with parity. Internally, each RAM device has row and column addressing that defines a specific memory cell. Each RAM device has seven address inputs. Two internal 7-bit latches are clocked alternately by row and column strobes. This requires that the input addresses be multiplexed to each device. RAM Controller U2040 (type-8202A device) provides the required multiplexing, strobes, and refresh requirements for the RAM devices.

ADDRESS MULTIPLEXING

Of the 16 System Address Bus lines, 14 lines provide the low-order and high-order address lines to the multiplexer within the RAM Controller. The two most significant bits of the System Address Bus are input to the Timing Control logic within the RAM Controller. Table 16-1 shows the relationships of the system address bus lines to the RAM Controller output lines.

Table 16-1
Relationships of System Address Bus to
RAM Controller Output Lines

System Address Bus	U2040 Input Address	RAM Controller Output Lines
A0	AL0	Low-Order Address. These address inputs generate the row addresses for the multiplexer in the RAM Controller.
A1	AL1	
A2	AL2	
A3	AL3	
A4	AL4	
A5	AL5	
A6	AL6	
A7	AH0	High-Order Address. These address inputs generate the column addresses for the multiplexer in the RAM Controller.
A8	AH1	
A9	AH2	
A10	AH3	
A11	AH4	
A12	AH5	
A13	AH6	
A14	B0	Bank Address. These inputs select one of the four banks in the memory array.
A15	B1	

ROW AND COLUMN STROBES

Four row strobes (one for each memory bank) and one column strobe are generated in the Timing and Control logic within the RAM Controller. As shown in Table 6-1, the two most significant bits of the System Address Bus determine which of the four banks is selected in the memory array. Table 16-2 shows the relationship between the System Bus addresses and the banks selected by the Row Address Strobes.

Table 16-2
Relationship of Bus Addresses to Selected Memory Bank

System Bus Address	Row Address Strobe	Memory Bank
0000--3FFF	RAS0(L)	Bank 1
4000--7FFF	RAS1(L)	Bank 2
8000--BFFF	RAS2(L)	Bank 3
C000--FFFF	RAS3(L)	Bank 4

The CAS(L) (Column Address Strobe) output is common to all memory banks.

This output is used to latch the column addresses into the memory bank, which was explained earlier.

REFRESH

The RAM Controller has the capability of providing an internal refresh cycle or accepting an external refresh request. A refresh timer in the RAM Controller generates a refresh cycle if an external refresh request is not received within a specified time. The refresh timer is reset when a refresh cycle is requested internally or externally. An internal refresh counter contains the address of the row to be refreshed. This counter is incremented after each refresh cycle. The external refresh logic is discussed in the following paragraph.

REFRESH LOGIC

The memory array is refreshed by the following methods:

1. RAM controller U2040 has a refresh timing cycle that automatically provides a refresh request every 10--16 microseconds.

2. An external refresh command is issued to the RAM controller at three times:

    a. 200 ns after the leading edge of OPREQ(H).

    b. After the leading edge of each I/O clock pulse (providing the 2650A-1 or DMA is not in control of the bus). In this mode, the 8202A performs an Auto refresh between I/O clocks, due to the time between I/O clock pulses.

    c. During maintenance if the FP HOLD(L) line is asserted, indicating a breakpoint or single-step operation.

WRITE PROTECT

During a write operation to the RAMs, the RAMINH(L) control line is gated with the WRT(H) line. Therefore, if the RAMINH(L) line is asserted for any reason, the RAMs cannot be written to.

PAGE SWITCHING

Page switching is similar to, but should not be confused with, bank switching. Page switching affects 8K blocks of System Memory (RAM) only; on the other hand, bank switching affects 16K blocks of either System or Program Memory. Page switching allows any one of eight 8K blocks of System Memory (RAM) to be switched into the second 8K address space (8K--16K) of the system processor. This permits the system processor to address the following:

- System Memory (RAM) in its address space 2000--3FFF (8K--16K) with page switching.
- Either Program or System Memory in its address space 4000--7FFF (16K--32K) with bank switching.

Figure 16-3 is a simplified schematic diagram of the page switching logic. I/O port address D3 is the page switching port. When address D3 is on the address bus, PAGE(L) goes low and clocks Paging Latch U4010. The data inputs to U4010 are presented to the "B" inputs of Paging Multiplexer U4020. Address lines A13--A15 are presented to the "A" inputs of U4020.

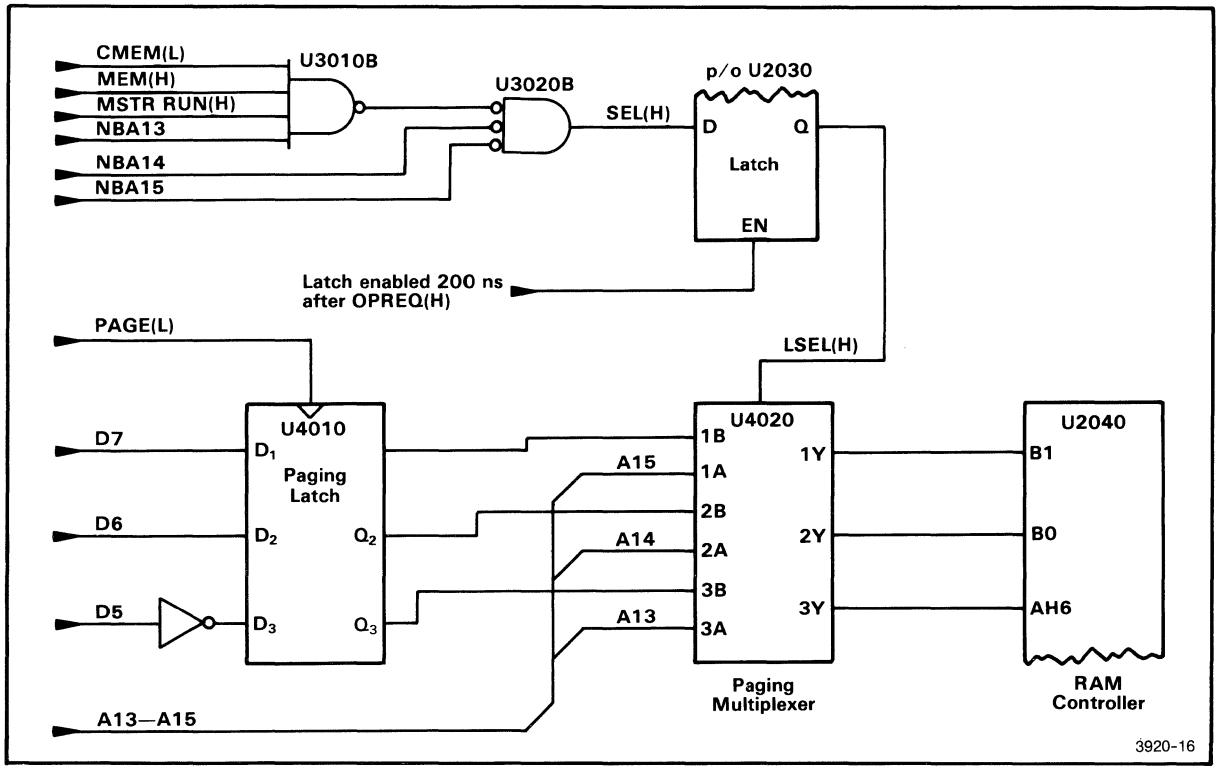


Fig. 16-3. Page Switching logic.

NAND gates U3010B and U3020B are enabled when all of the following conditions exist:

- CMEM(L) goes high, indicating that the system processor is addressing system memory.
- MEM(H) goes high, specifying a memory access.

- MSTR RUN(L) goes high, indicating that the system processor is active.

- The states of NBA13--NBA15 are such that the addresses on the address bus are between 2000--3FFF. (Binary addresses 0010 XXXX XXXX XXXX -- 0011 XXXX XXXX XXXX.)

When NAND gates U3010 and U3020 are enabled, SEL(H) and LSEL(H) are high. A high on LSEL(H) selects the "B" inputs to Multiplexer U4020. The three most significant bits (D5--D7) from the associated data byte of I/O port address D3 appear as inputs to RAM Controller U2040. The data bits are utilized as follows:

- D6 and D7 provide the bank address and select one of the four memory banks.

- D5 sets the state of the most significant bit (AH6) of the column addresses.

For addresses other than 2000--3FFF, NAND gates U3010B and U3020B are disabled and LSEL(H) goes low. This low selects the "A" inputs to Multiplexer U4020. The three most significant address bits A13--A15 are now the inputs to the RAM Controller.

PARITY ERROR LOGIC

As previously mentioned, the ninth memory device in each of the four memory array banks is used to store the parity bit. Figure 16-4 is a simplified schematic diagram of the Parity Error logic.

Parity Generator U5040 generates an even parity bit from data bus D0--D7 (data input lines to memory array). This bit is stored in the parity memory devices. If the number of high bits on the data bus is even, the parity bit is high. If the number of high bits is odd, the parity bit is low. Parity Checker U5090 adds the number of high bits from data bus DB0--DB7 (data output lines from the memory array) to the parity bit stored in the memory array. If the parity bit is high (indicating an even parity), the output of the Parity Checker is low. The high parity bit, when added to an even number of high bits, produces an odd number of high bits, and thus a low output from the Parity Checker. If no parity error exists the output of U5090 will always be low. When a parity error is detected, the output of U5090 will be high. This high output triggers flip-flop U5140A and generates a Parity Error, which is Interrupt Vector 1.

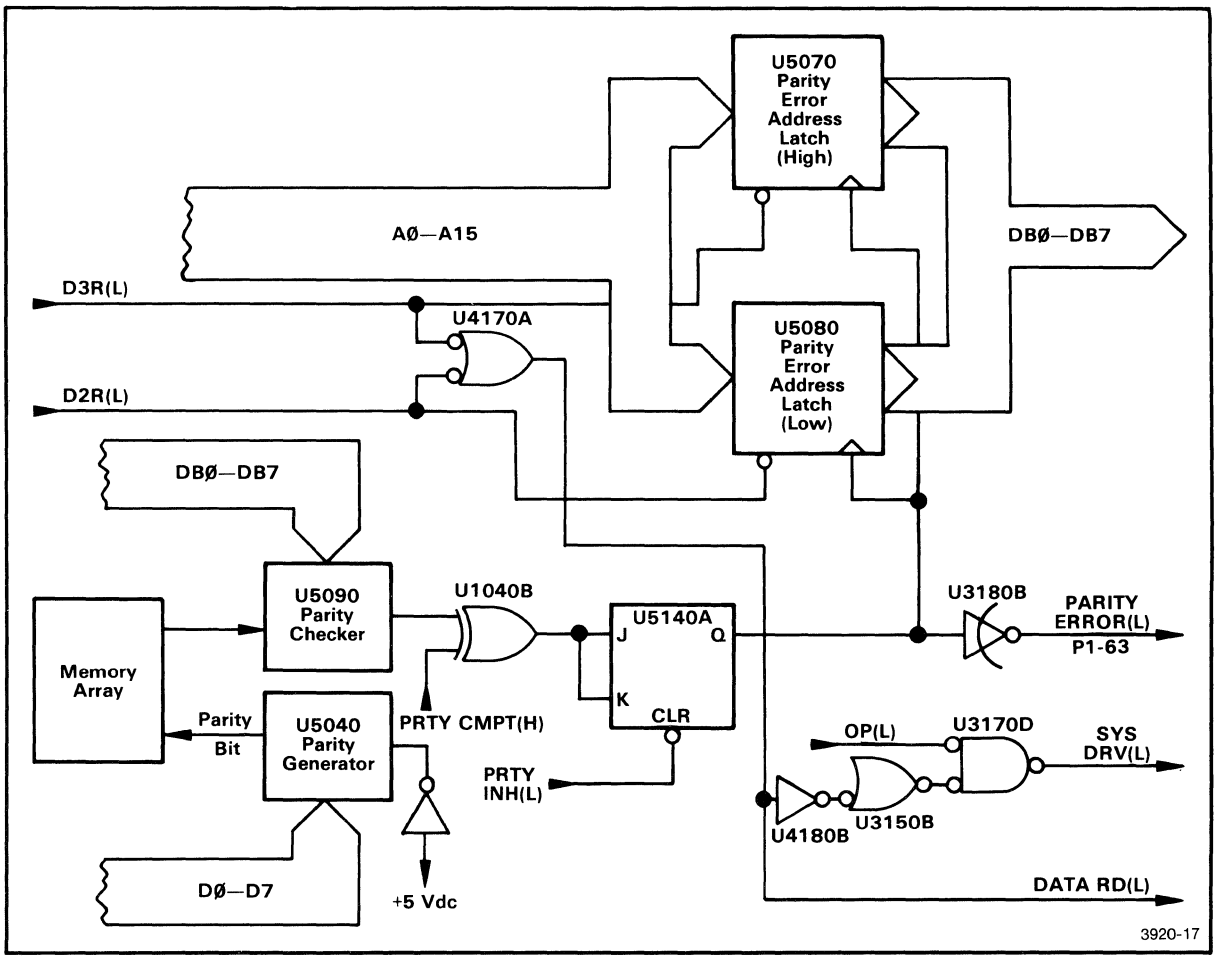


Fig. 16-4. Parity Error logic.

If a parity error is detected, the associated 16-bit address is latched in Parity Error Address Latches U5070 and U5080. The address of the parity error is available by consecutively reading I/O ports D2 and D3.

The parity bit from Parity Checker U5090 may be complemented by writing to I/O port D2. This provides a means for diagnostics to check the parity and associated Interrupt Vector 1. Interrupt Vector 1 is cleared whenever I/O port D2 is read.

DIAGNOSTIC PROVISIONS

The System RAM board provides several features to aid in diagnostic troubleshooting:

- The address of the last parity error is latched and can be read by the system processor at I/O ports D2 (low byte) and D3 (high byte).
- Interrupt Vector 15 is used to indicate a refresh operation to the

64K RAM array. This interrupt is enabled by writing to I/O port address D2.

- The parity line may be inverted by writing to I/O port address D2, thus providing a means for diagnostics to check the parity logic and Interrupt Vector 1 (System Memory Parity error).

- Five LEDs on the System RAM board may be turned on or off by writing to the data byte of I/O port address D2. Three additional LEDs monitor the status of the lower three bits of the data byte from I/O port address D2.

- J6140 is a two-position jumper, labeled TEST. For special applications, this jumper can be positioned so that the board responds to CMEM(H) control line going high. In this position, the board functions as Program Memory. This permits the program memory diagnostic tests to be run on this board when the CMEM(H) line goes high.

NOTE

Refer to Section 4, Disc-Based Diagnostics, of this manual for additional information on these diagnostic features.

I/O PORT INTERFACES

A combination of NAND gates and decoders are used to decode I/O port addresses D2 and D3. Figure 16-5 is a simplified schematic diagram showing the I/O port decoder and associated logic.

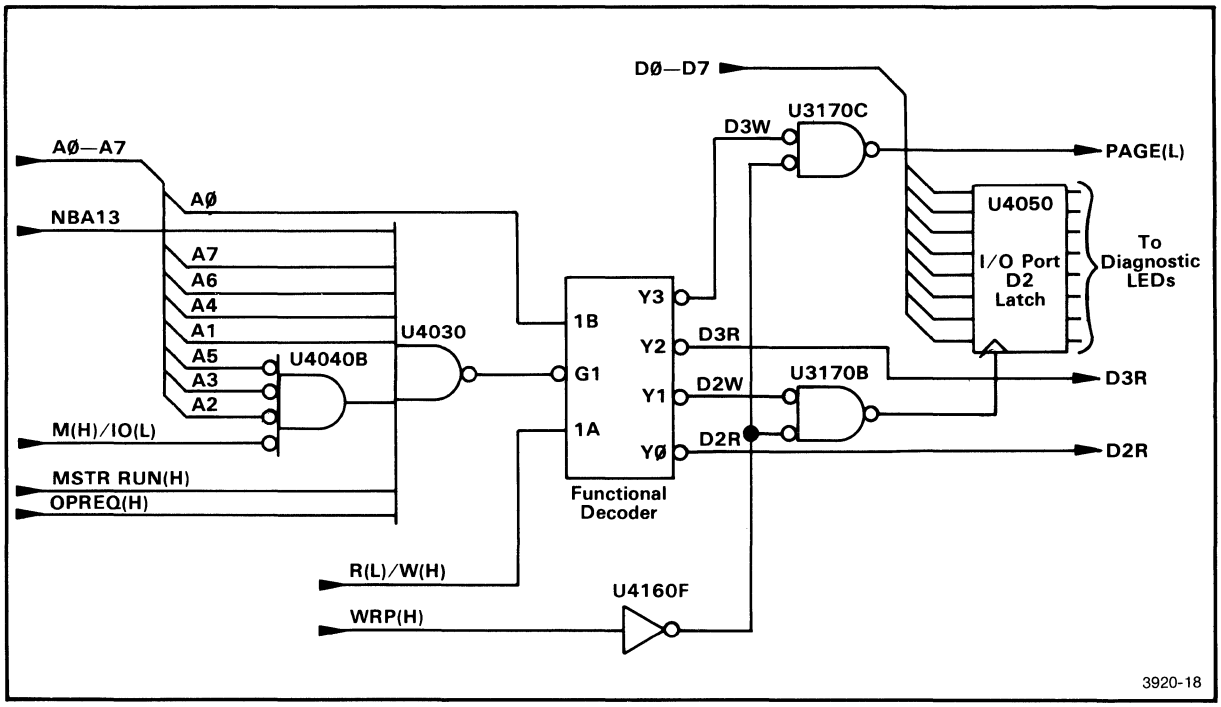


Fig. 16-5. I/O Port Decoder

NAND gates U4040B and U4030 decode I/O port addresses D2 and D3 (except for the least significant bit, AO). The output from the NAND gate decoders enables Functional Decoder U3160. The states of input lines AO and R(L)/W(H) determine which of the four output lines of U3160 are used to select the various functions. Table 16-3 shows the relationship of the enabling control lines to the output control lines. Refer to Section 6, Specifications, of this manual for a detailed breakdown of the associated data bytes of I/O port addresses D2 and D3.

Table 16-3
System RAM Functional Decoder
Enabling Control Lines and Output Control Lines

I/O Port Address	Read or Write Operation	Functional Decoder Enabling Control Lines		Line Name	Function
		A0	R(L)/W(H)		
D2	Read	0	0	D2R	Enables Parity Error Address Latch U5080.
	Write	0	1	D2W	Checks I/O Port D2 Latch U4050.
D3	Read	1	0	D3R	Enables Parity Error Address Latch U5070.
	Write	1	1	D3W	Provides control line PAGE(L) for clocking Paging Latch U4010.

SECTION 17

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

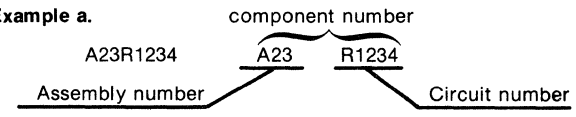
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

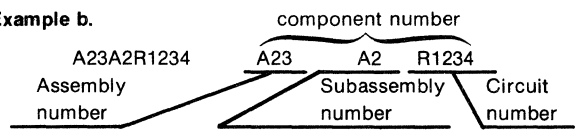
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000CG	TECCOR ELECTRONICS, INC.	1101 PAMELA DRIVE PO BOX 669	EULESS, TX 76039
000FJ	MARCOM SWITCHES INC.	67 ALBANY STREET	CAZENOVIA, N.Y. 13035
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
01807	PETERSEN RADIO COMPANY, INC.	2800 WEST BROADWAY	COUNCIL BLUFFS, IN 51501
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
09353	C AND K COMPONENTS, INC.	103 MORSE STREET	WATERTOWN, MA 02172
10582	CTS OF ASHEVILLE, INC.	MILLS GAP ROAD	SKYLAND, NC 28776
11236	CTS OF BERNE, INC.	406 PARR RD.	BERNE, IN 46711
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
15238	ITT SEMICONDUCTORS, A DIVISION OF INTER NATIONAL TELEPHONE AND TELEGRAPH CORP.	P.O. BOX 168, 500 BROADWAY	LAWRENCE, MA 01841
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
20932	EMCON DIV OF ILLINOIS TOOL WORKS INC.	11620 SORRENTO VALLEY RD P O BOX 81542	SAN DIEGO, CA 92121
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32440	ENGINEERED COMPONENTS CO.	3580 SACRAMENTO DR.	SAN LUIS OBISPO, CA 93406
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
50522	MONSANTO CO., ELECTRONIC SPECIAL PRODUCTS	3400 HILLVIEW AVENUE	PALO ALTO, CA 94304
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
56708	ZILOG INC.	14060 BUBB RD.	CUPERTINO, CA 95014
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72619	DIALIGHT, DIV. AMPEREX ELECTRONIC	203 HARRISON PLACE	BROOKLYN, NY 11237
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
75378	CTS KNIGHTS, INC.	400 REIMANN AVE.	SANDWICH, IL 60548
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
81541	AIRPAX ELECTRONICS, INC.	WOODS ROAD	CAMBRIDGE, MD 21613
82877	ROTRON, INC.	7-9 HASBROUCK LANE	WOODSTOCK, NY 12498
83003	VARO, INC.	P O BOX 411, 2203 WALNUT STREET	GARLAND, TX 75040
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A05	119-1303-01			POWER SUPPLY:	80009	119-1303-01
A06	119-1304-01			POWER SUPPLY:	80009	119-1304-01
A10	670-6541-00			CKT BOARD ASSY:COMM INTERFACE	80009	670-6541-00
A20	670-6540-00			CKT BOARD ASSY:SYSTEM CONTROLLER	80009	670-6540-00
A30	670-6542-00			CKT BOARD ASSY:SYSTEM/PROGRAM MEMORY	80009	670-6542-00
A40	670-6543-00			CKT BOARD ASSY:EMULATOR CONTROLLER	80009	670-6543-00
A50	----- -----			CKT BOARD ASY:FRONT PANEL		
A50	----- -----			(NOT REPLACEABLE ORDER 672-0884-00)		
A60	670-6545-00			CKT BOARD ASSY:MAIN INTERCONNECT	80009	670-6545-00
A60	----- -----			(NO ELECTRICAL PARTS)		
A70	670-6546-00			CKT BOARD ASSY:LANGUAGE PROCESSOR	80009	670-6546-00
A80	670-7342-00			CKT BOARD ASSY:SYSTEM RAM	80009	670-7342-00
A05	----- -----			POWER SUPPLY:4.75-7.0VDC,36A OUT		
A05C1	290-0903-00			CAP.,FXD,ELCTLT:9000UF,15V	90201	TCX902U015N2C3B
A05C2	290-0904-00			CAP.,FXD,ELCTLT:64000UF,15V	90201	CGS643U015V4C3PH
A05C3	290-0904-00			CAP.,FXD,ELCTLT:64000UF,15V	90201	CGS643U015V4C3PH
A05C4	285-0862-00			CAP.,FXD,PLSTC:0.001,10%,100V	56289	410P10291
A05C5	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A05C6	290-0903-00			CAP.,FXD,ELCTLT:9000UF,15V	90201	TCX902U015N2C3B
A05CR1	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A05CR2	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A05CR3	152-0729-00			SEMICOND DEVICE:RECT,SI,DUAL,COMMON ANODE	83003	R711A
A05CR6	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A05CR7	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A05CR9	152-0279-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZG35010RL
A05CR10	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A05Q1	151-0454-00			TRANSISTOR:SILICON,NPN	80009	151-0454-00
A05Q2	151-0633-00			TRANSISTOR:SILICON,NPN	80009	151-0633-00
A05Q3	151-0633-00			TRANSISTOR:SILICON,NPN	80009	151-0633-00
A05Q4	151-0633-00			TRANSISTOR:SILICON,NPN	80009	151-0633-00
A05Q5	151-0633-00			TRANSISTOR:SILICON,NPN	80009	151-0633-00
A05Q6	151-0633-00			TRANSISTOR:SILICON,NPN	80009	151-0633-00
A05Q7	151-0633-00			TRANSISTOR:SILICON,NPN	80009	151-0633-00
A05Q8	151-0103-01			TRANSISTOR:SILICON,NPN	04713	2N2219
A05Q9	151-0307-00			TRANSISTOR:SILICON,PNP,DUAL	07263	SP13404
A05R1	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
A05R2	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
A05R3	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
A05R4	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
A05R5	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
A05R6	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R7	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R8	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R9	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R10	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R11	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R12	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R13	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R14	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R15	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R19	301-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.50W	01121	EB8205
A05R20	301-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.50W	01121	EB8205
A05R21	301-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.50W	01121	EB8205
A05R22	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A05R23	311-2081-00			RES.,VAR,WW:TRMR,1.5K OHM,2W	10582	TYPE 110
A05R24	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
A05R25	321-0213-00			RES.,FXD,FILM:1.62K OHM,1%,0.125W	91637	MFF1816G16200F
A05R26	321-0226-00			RES.,FXD,FILM:2.21K OHM,1%,0.125W	91637	MFF1816G22100F
A05R28	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R29	321-0641-00			RES.,FXD,FILM:1.8K OHM,1%,0.125W	91637	MFF1816G18000F
A05R30	301-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
A05R31	311-2081-00			RES.,VAR,WW:TRMR,1.5K OHM,2W	10582	TYPE 110
A05R32	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R34	301-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.50W	01121	EB4705
A05R35	301-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.50W	01121	EB1525
A05R35	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A05R36	301-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.50W	01121	EB1525
A05R37	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R38	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R39	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
A05R40	301-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.50W	01121	EB5135
A05R41	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
A05R43	311-2080-00			RES.,VAR,WW:PNL,1.5K OHM,4W	11236	AW-4274
A05R49	301-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.50W	01121	EB5135
A05SCR1	151-0536-00			SCR:SI,3A,30V,TO-220	000CG	S0303LS3
A05SCR2	151-0537-00			THYRISTOR:TRIAC,10A,400V	03508	SC146DX176
A05U1	156-0071-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC1723CL

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A06	----- -----			POWER SUPPLY:10.5-75VDC,1.7A OUT		
A06C1	290-0873-00			CAP.,FXD,ELCTLT:3300UF,+50-10%,35VDC	54473	ECEBIVV332S
A06C2	290-0844-00			CAP.,FXD,ELCTLT:100UF,-10+75%,35 WVDC	54473	ECE-A35V100L
A06C3	285-0862-00			CAP.,FXD,PLSTC:0.001,10%,100V	56289	410P10291
A06C5	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A06C6	290-0844-00			CAP.,FXD,ELCTLT:100UF,-10+75%,35 WVDC	54473	ECE-A35V100L
A06CR1	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A06CR2	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A06CR3	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A06CR4	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A06CR6	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008
A06CR7	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A06F1	159-0014-00			FUSE,CARTRIDGE:3AG,5A,250V,FAST-BLOW	71400	MTH5
A06Q1	151-0454-00			TRANSISTOR:SILICON,NPN	80009	151-0454-00
A06Q2	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A06Q3	151-0310-00			TRANSISTOR:SILICON,NPN	80009	151-0310-00
A06R1	308-0827-00			RES.,FXD,WW:0.22 OHM,10%,2W	75042	BWH-R2200J
A06R2	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A06R3	311-2081-00			RES.,VAR,WW:TRMR,1.5K OHM,2W	10582	TYPE 110
A06R4	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A06R5	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A06R6	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A06R7	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A06R8	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A06R10	323-0181-00			RES.,FXD,FILM:750 OHM,1%,0.50W	75042	CECT0-7500F
A06R12	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A06R13	311-2081-00			RES.,VAR,WW:TRMR,1.5K OHM,2W	10582	TYPE 110
A06R14	301-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
A06R15	315-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.25W	01121	CB8205
A06R16	315-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.25W	01121	CB8205
A06R17	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A06R18	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A06R19	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A06R20	311-2080-00			RES.,VAR,WW:PNL,1.5K OHM,4W	11236	AW-4274
A06R23	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A06R24	301-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.50W	01121	EB4725
A06R25	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A06R26	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A06R30	307-0755-00			RES.,FXD,CMPSN:0.5 OHM,5%,0.5W	57668	R50J0.50HM
A06R31	301-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.50W	01121	EB4725
A06SCR1	151-0536-00			SCR:SI,3A,30V,TO-220	000CG	S0303LS3
A06U1	156-0071-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC1723CL

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	----- -----			CKT BOARD ASSY:COMM INTERFACE		
A10C1010	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A10C1020	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A10C1031	283-0068-00			CAP.,FXD,CER DI:0.01UF,+100-0%,500V	56289	19C241
A10C1040	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A10C1090	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A10C2010	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A10C2011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A10C3080	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A10C3082	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A10C4011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A10C4031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A10C4070	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A10J1	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 3)		
A10J2	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 3)		
A10J3	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 3)		
A10R1011	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A10R1021	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A10R1022	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A10R1023	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A10R1032	301-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
A10R2040	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R2060	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R2061	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R2070	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R2071	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R2091	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R2092	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R2097	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A10R3040	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A10R3082	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A10S1030	263-0048-00			SWITCH SL ASSY:INTERFACE MODE	80009	263-0048-00
A10S1060	263-0042-00			SWITCH SL ASSY:B-SOURCE	80009	263-0042-00
A10S1080	263-0042-00			SWITCH SL ASSY:B-SOURCE	80009	263-0042-00
A10S1090	263-0042-00			SWITCH SL ASSY:B-SOURCE	80009	263-0042-00
A10U1010	156-1315-00			MICROCKT,INTFC:QUAD DIFFERENTIAL RECEIVER	34335	AM26LS32
A10U3010	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A10U3020	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153
A10U3030	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157P3
A10U3040	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A10U3050	156-0879-00			MICROCIRCUIT,DI:QUAD LINE DRVR	80009	156-0879-00
A10U3060	156-0878-00			MICROCIRCUIT,DI:QUAD LINE RCVR	04713	MC1489L
A10U3070	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A10U3080	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A10U3081	156-0545-01			MICROCIRCUIT,DI:12 BIT BINARYCNTR,SCRN	04713	MC14040BCLD
A10U3082	156-0844-00			MICROCIRCUIT,DI:SYNC 4-BIT BIN COUNTER	34335	SN74LS161N

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20	----- -----			CKT BOARD ASSY:SYSTEM CONTROLLER		
A20C1011	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A20C1031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C1042	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C1058	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C1091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C1101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C1102	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C1401	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C1501	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C1501	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A20C1602	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C1701	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225
A20C2011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C2021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C2028	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C2041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C2061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C2071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C2091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C2097	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A20C2101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C2401	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225
A20C3018	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C3028	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C3071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C3201	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C3301	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C3401	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C3601	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C3701	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C3801	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C4038	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C4068	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C4071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C4301	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C4401	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C4601	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C4701	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C5011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C5078	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A20C5091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C5201	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C5301	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C5501	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C5701	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C5803	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	20932	201-E0-100AT820J
A20C6011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6022	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6201	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T

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A20C6301	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6401	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6501	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20C6801	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271
A20C6803	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102
A20C7021	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A20C7030	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A20C7070	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A20C7601	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A20CR5081	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20DS1083	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A20DS1084	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A20DS1085	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A20DS1086	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A20DS1087	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A20J1051	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 3)	22526	47357
A20J1080	131-0589-00 ----- -----			TERMINAL,PIN:0.46 L X 0.025 SQ (QTY 11)	22526	47350
A20J2804	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 9)	22526	47357
A20J3014	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 3)	22526	47357
A20J5704	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 3)	22526	47357
A20R1021	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R1061	307-0598-00			RES NTWK,FXD FI:7,330 OHM,2%,1.0W	91637	MSP08A01331G
A20R1064	307-0591-00			RES,NTWK,FXD FI:9,470 OHM,2%,2W	91637	MSP10A01-471J
A20R1103	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A20R1201	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A20R1404	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A20R2081	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A20R2082	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R2504	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A20R3016	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R3069	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R3104	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A20R3504	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A20R3701	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A20R4067	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R4081	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A20R4601	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R4704	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	91637	MSP06A01-103J
A20R4801	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A20R4802	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A20R5054	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A20R5071	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A20R5078	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R5104	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A20R5704	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A20R5801	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R5802	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R6021	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A20R6051	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R6064	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A20R6065	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A20R6094	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272

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A20R6104	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A20R6204	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	91637	MSP06A01-103J
A20R6802	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R6804	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A20R6805	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R6806	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A20R7200	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20S1100	260-1589-00			SWITCH,PUSH:(6)SPST,0.1A,5V	00779	435166-4
A20U1010	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A20U1020	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A20U1030	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A20U1040	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A20U1050	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A20U1060	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A20U1070	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A20U1080	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A20U1090	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A20U1100	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A20U1200	156-1310-01			MICROCIRCUIT,DI:UART 2.5MHZ,SEL	80009	156-1310-01
A20U1300	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A20U1400	156-0878-00			MICROCIRCUIT,DI:QUAD LINE RCVR	04713	MC1489L
A20U1500	156-0879-00			MICROCIRCUIT,DI:QUAD LINE DRVR	80009	156-0879-00
A20U1600	156-0844-00			MICROCIRCUIT,DI:SYNC 4-BIT BIN COUNTER	34335	SN74LS161N
A20U1700	156-0878-00			MICROCIRCUIT,DI:QUAD LINE RCVR	04713	MC1489L
A20U2010	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A20U2020	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A20U2022	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A20U2030	156-1065-00			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N OR J
A20U2040	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A20U2050	156-0986-02			MICROCIRCUIT,DI:NMOS,MICROPROC,8-BIT	18324	2650A-1I
A20U2060	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	80009	156-1111-02
A20U2070	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A20U2080	156-1202-00			MICROCIRCUIT,DI:PROGRAMMABLE DMA CONT	34649	(PORD)8257/S2876
A20U2090	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A20U2100	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A20U2300	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A20U2400	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A20U2500	156-0658-00			MICROCIRCUIT,DI:ASYNCHRONOUS COMM INT ADPT	07263	F6850PC OR DC
A20U2600	156-0658-00			MICROCIRCUIT,DI:ASYNCHRONOUS COMM INT ADPT	07263	F6850PC OR DC
A20U2700	156-0658-00			MICROCIRCUIT,DI:ASYNCHRONOUS COMM INT ADPT	07263	F6850PC OR DC
A20U3010	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A20U3020	156-1373-00			MICROCIRCUIT,DI:QUAD BUS BFR GATE W/3 ST	80009	156-1373-00
A20U3030	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A20U3040	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74S257NP3
A20U3060	156-0303-01			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S03NP3
A20U3070	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A20U3090	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A20U3100	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A20U3200	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A20U3300	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A20U3400	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A20U3500	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A20U3600	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A20U3700	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	01295	SN74LS393
A20U3800	156-0478-02			MICROCIRCUIT,DI:DUAL 4 INP & GATE,BURN-IN	01295	SN74LS21NP3
A20U4010	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A20U4020	156-1373-00			MICROCIRCUIT,DI:QUAD BUS BFR GATE W/3 ST	80009	156-1373-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20U4030	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A20U4040	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A20U4050	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A20U4060	156-0866-00			MICROCIRCUIT,DI:13 INP NAND GATES	04713	SN74LS133
A20U4070	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A20U4080	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A20U4090	156-0153-02			MICROCIRCUIT,DI:HEX INVERTER BUFFER	27014	DM8006
A20U4100	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A20U4200	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A20U4300	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A20U4400	156-1258-00			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A20U4500	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A20U4600	156-1258-00			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A20U4700	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A20U5010	156-1357-00			MICROCIRCUIT,DI:256 X 1 STATIC RAM 3 STATE	80009	156-1357-00
A20U5020	156-0478-02			MICROCIRCUIT,DI:DUAL 4 INP & GATE,BURN-IN	01295	SN74LS21NP3
A20U5030	160-0802-00			MICROCIRCUIT,DI:2048 X 8 EPROM	80009	160-0802-00
A20U5040	160-0728-00			MICROCIRCUIT,DI:2048 X 8 EPROM	80009	160-0728-00
A20U5050	160-0884-00			MICROCIRCUIT,DI:512 X 8 PROM	80009	160-0884-00
A20U5060	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A20U5070	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A20U5080	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A20U5090	156-1176-01			MICROCIRCUIT,DI:8/3 LINE PRIORITY ENCODER	80009	156-1176-01
A20U5100	156-1176-01			MICROCIRCUIT,DI:8/3 LINE PRIORITY ENCODER	80009	156-1176-01
A20U5200	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A20U5300	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A20U5400	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A20U5500	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A20U5600	156-0784-00			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	01295	SN74LS163AN
A20U5700	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A20U5800	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A20U6010	156-1357-00			MICROCIRCUIT,DI:256 X 1 STATIC RAM 3 STATE	80009	156-1357-00
A20U6020	156-0985-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	18324	N74LS260AN OR J
A20U6022	156-1357-00			MICROCIRCUIT,DI:256 X 1 STATIC RAM 3 STATE	80009	156-1357-00
A20U6030	156-1357-00			MICROCIRCUIT,DI:256 X 1 STATIC RAM 3 STATE	80009	156-1357-00
A20U6040	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A20U6050	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A20U6060	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A20U6070	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A20U6080	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A20U6090	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A20U6100	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A20U6200	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A20U6300	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A20U6400	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A20U6500	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A20U6700	156-0784-00			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	01295	SN74LS163AN
A20Y4800	158-0154-00			XTAL UNIT,QTZ:20MHZ,0.015%,PARALLEL	75378	MP 200
A20Y7806	158-0124-00			XTAL UNIT,QTZ:2.4576 MHZ,0.05% PARALLEL	75378	MP-024

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A30	----- -----			CKT BOARD ASSY:SYSTEM/PROGRAM MEMORY		
A30C1011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1061	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1071	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1091	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A30C1101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1131	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1141	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1151	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C1161	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2061	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2071	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2091	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A30C2101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2131	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2141	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2151	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C2161	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3061	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3071	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3091	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A30C3101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3131	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3141	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3151	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C3161	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4061	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4071	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A30C4091	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A30C4101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4131	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4141	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4151	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C4161	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6061	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6071	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6091	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6131	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6141	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6151	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C6171	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C7010	283-0680-00			CAP.,FXD,MICA D:330PF,1%,500V	00853	D155E331F0
A30C7011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C7031	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A30C7091	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C7101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30C7145	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A30CR7012	152-0071-00			SEMICOND DEVICE:GERMANIUM,15V,40MA	15238	G865
A30J5011	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 3)	22526	47357
A30J5175	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 3)	22526	47357
A30J6175	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 3)	22526	47357
A30J6179	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 3)	22526	47357
A30J7171	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 3)	22526	47357
A30R3161	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R3162	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R5011	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5013	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5015	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5017	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5019	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5021	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5023	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5025	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5027	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5029	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5031	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5033	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5035	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5036	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5037	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A30R5039	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R5041	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5043	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5047	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5053	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5057	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5063	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5067	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5073	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5077	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5083	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5087	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5091	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R5093	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5097	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5099	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R5101	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R5103	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5107	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5113	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5117	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5123	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5127	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5133	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5137	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5143	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5147	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5153	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5157	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5163	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A30R5167	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5168	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A30R5169	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A30R5170	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A30R5180	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A30R6101	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A30R6111	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R6121	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R7011	322-0111-00			RES.,FXD,FILM:140 OHM,1%,0.25W	91637	MFF1421G140R0F
A30R7020	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R7051	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A30R7111	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R7161	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A30R7162	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A30R7163	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A30R7164	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A30R7165	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A30S7170	260-1721-00			SWITCH,ROCKER:8,SPST,125MA,30VDC	00779	435166-5
A30U1010	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U1090	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U1100	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U1160	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U2010	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U2090	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U2100	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U2160	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U3010	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A30U3090	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U3100	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U3160	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U4000	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A30U4010	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U4090	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U4100	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U4160	156-1228-00			MICROCIRCUIT,DI:4096 X 1 SRAM	34649	CD2147
A30U6000	156-0739-00			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	80009	156-0739-00
A30U6010	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A30U6020	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A30U6030	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A30U6040	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A30U6050	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U6060	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U6070	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U6080	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U6090	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U6100	160-0822-00			MICROCIRCUIT,DI:32 X 8 PROM	80009	160-0822-00
A30U6110	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A30U6120	156-0739-00			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	80009	156-0739-00
A30U6130	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U6140	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U6150	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U6160	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U6170	156-0693-02			MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	27014	DM74S139
A30U7010	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TIRGGER BFR	01295	SN74S240J
A30U7020	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A30U7030	156-1064-02			MICROCIRCUIT,DI:QUAD 2/1 LINE TURE DATA	01295	SN74S157JP4
A30U7040	156-1189-00			MICROCIRCUIT,DI:16 X 4 RAM	34335	SN74S189J
A30U7050	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
A30U7060	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A30U7070	156-0739-00			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	80009	156-0739-00
A30U7080	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A30U7090	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3
A30U7100	156-0985-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	18324	N74LS260AN OR J
A30U7110	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A30U7120	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A30U7130	156-0707-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	01295	SN74S86N
A30U7140	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A30U7150	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A30U7160	156-1273-01			MICROCIRCUIT,DI:8 BIT EQUAL TO COMPARATOR	80009	156-1273-01

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A40	----- -----			CKT BOARD ASSY:EMULATOR CONTROLLER		
A40C1021	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A41C1040	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C1061	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C1081	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C1101	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C1121	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C1141	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C1161	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C1181	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C2021	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C2041	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C2061	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C2081	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C2101	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C2141	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C2161	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C2181	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C3021	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C3041	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C3061	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C3081	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C3101	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C3121	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C3141	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C3151	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C3161	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4021	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4041	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4061	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4081	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4091	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4101	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4121	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4141	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4161	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4171	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C4181	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C5021	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C5035	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A40C5041	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C5061	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C5081	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C5101	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C5121	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C5141	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C5161	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40C5165	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A40C5181	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A40J1093	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ	22526	47350
	----- -----			(QTY 9)		
A40J1113	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ	22526	47350
	----- -----			(QTY 9)		
A40J1133	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ	22526	47350
	----- -----			(QTY 9)		
A40J1183	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 3)		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A40J3073	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 3)		
A40J4083	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 3)		
A40J4093	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 3)		
A40J5097	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 2)		
A40J5177	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 3)		
A40R1171	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A40R1181	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A40R2121	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A40R2131	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A40R2151	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A40R5111	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A40R5151	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	MSP08A01222G
A40U1010	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U1020	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	01295	SN74LS374
A40U1030	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	01295	SN74LS374
A40U1040	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	01295	SN74LS374
A40U1050	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	01295	SN74LS374
A40U1060	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U1070	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U1080	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U1090	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U1100	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	01295	SN74LS374
A40U1110	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	01295	SN74LS374
A40U1120	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A40U1130	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	01295	SN74LS374
A40U1140	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A40U1150	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG	01295	SN74LS113NP3
A40U1160	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG	01295	SN74LS113NP3
A40U1170	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG	01295	SN74LS113NP3
A40U1180	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG	01295	SN74LS113NP3
A40U1190	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A40U2010	156-1273-00			MICROCIRCUIT,DI:8 BIT EQUAL TO COMPARATOR	80009	156-1273-00
A40U2020	156-1273-00			MICROCIRCUIT,DI:8 BIT EQUAL TO COMPARATOR	80009	156-1273-00
A40U2030	156-1273-00			MICROCIRCUIT,DI:8 BIT EQUAL TO COMPARATOR	80009	156-1273-00
A40U2040	156-1273-00			MICROCIRCUIT,DI:8 BIT EQUAL TO COMPARATOR	80009	156-1273-00
A40U2050	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U2060	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A40U2070	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A40U2080	156-1273-00			MICROCIRCUIT,DI:8 BIT EQUAL TO COMPARATOR	80009	156-1273-00
A40U2090	156-1273-00			MICROCIRCUIT,DI:8 BIT EQUAL TO COMPARATOR	80009	156-1273-00
A40U2100	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U2110	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U2120	160-0727-00			MICROCIRCUIT,DI:32 X 8 PROM	80009	160-0727-00
A40U2130	156-0219-02			MICROCIRCUIT,DI:8 BIT PRIORITY ENCODER	80009	156-0219-02
A40U2140	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A40U2150	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A40U2160	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A40U2170	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A40U2180	156-1373-00			MICROCIRCUIT,DI:QUAD BUS BFR GATE W/3 ST	80009	156-1373-00
A40U2190	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A40U3010	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A40U3020	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A40U3030	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A40U3040	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A40U3050	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A40U3060	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A40U3070	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A40U3080	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A40U3090	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A40U3100	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	01295	SN74LS374
A40U3110	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	01295	SN74LS374
A40U3120	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A40U3130	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A40U3140	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A40U3150	156-1061-00			MICROCIRCUIT,DI:DUAL J-K FLIP-FLOP	07263	74S109(PC OR DC)
A40U3160	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A40U3170	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A40U3180	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A40U3190	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A40U4010	156-0412-02			MICROCIRCUIT,DI:SYN 4 BIT UP/DOWN CNTR	01295	SN74LS193N3
A40U4020	156-0412-02			MICROCIRCUIT,DI:SYN 4 BIT UP/DOWN CNTR	01295	SN74LS193N3
A40U4030	156-0412-02			MICROCIRCUIT,DI:SYN 4 BIT UP/DOWN CNTR	01295	SN74LS193N3
A40U4040	156-0412-02			MICROCIRCUIT,DI:SYN 4 BIT UP/DOWN CNTR	01295	SN74LS193N3
A40U4050	156-0645-02	XB020745		MICROCIRCUIT,DI:HEX INV ST NANOS-NAND	01295	SN74LS14NP3
A40U4060	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157P3
A40U4070	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
A40U4080	156-0418-00			MICROCIRCUIT,DI:8-INPUT,NAND GATE	80009	156-0418-00
A40U4090	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A40U4100	156-0418-00			MICROCIRCUIT,DI:8-INPUT,NAND GATE	80009	156-0418-00
A40U4110	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A40U4120	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A40U4130	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A40U4140	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A40U4150	156-0966-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	80009	156-0966-00
A40U4160	156-0418-00			MICROCIRCUIT,DI:8-INPUT,NAND GATE	80009	156-0418-00
A40U4170	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A40U4180	156-0966-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	80009	156-0966-00
A40U4190	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A40U5020	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U5030	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A40U5040	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A40U5050	156-0953-02			MICROCIRCUIT,DI:4 BIT MAGNITUDE CMPRTR	01295	SN74LS85
A40U5060	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3
A40U5070	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A40U5080	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A40U5090	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A40U5100	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A40U5110	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A40U5120	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A40U5130	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A40U5140	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	04713	MC6888/MC8T98L
A40U5150	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A40U5160	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A40U5170	156-1061-00			MICROCIRCUIT,DI:DUAL J-K FLIP-FLOP	07263	74S109(PC OR DC)
A40U5180	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A40U5190	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A50	----- -----			CKT BOARD ASSY:FRONT PANEL		
A50C1013	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1015	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A50C2026	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50J1	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			(QTY 16)		
A50R1011	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A50R1012	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A50R1013	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A50R1014	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A50R1019	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A50R2011	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A50R2031	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A50R2032	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A50R2033	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A50U1010	156-0145-02			MICROCIRCUIT,DI:QUAD 2-INP NAND BFR	01295	SN7438
A50U1020	156-0153-02			MICROCIRCUIT,DI:HEX INVERTER BUFFER	27014	DM8006
A50U1030	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A70	----- -----			CKT BOARD ASSY:LANGUAGE PROCESSOR		
A70C1078	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70C2017	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70C2019	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	72982	8035D9AADC0G270M
A70C2028	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70C2034	283-0649-00			CAP.,FXD,MICA D:105PF,1%,300V	00853	D153F1050F0
A70C2068	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70C3018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70C3058	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70C3078	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70C4010	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
A70C4018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70C4054	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70C4068	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A70J4029	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 3)	22526	47357
A70J4050	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD (QTY 2)	22526	47357
A70Q2036	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A70R2017	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A70R2018	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A70R2021	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A70R2029	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A70R2031	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A70R2032	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A70R2033	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A70R2058	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A70R3044	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A70R4021	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A70R4078	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A70TP1	131-0589-00 ----- -----			TERMINAL,PIN:0.46 L X 0.025 SQ (QTY 8)	22526	47350
A70TP2	131-0589-00 ----- -----			TERMINAL,PIN:0.46 L X 0.025 SQ (QTY 8)	22526	47350
A70U1060	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A70U1070	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A70U1080	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A70U2020	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	04713	MC6888/MC8T98L
A70U2030	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153
A70U2040	156-0983-00			MICROCIRCUIT,DI:MICROPROCESSOR EIGHT BIT	56708	Z 80 ACS
A70U2060	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A70U2070	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A70U2080	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A70U2090	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A70U3020	156-0866-00			MICROCIRCUIT,DI:13 INP NAND GATES	04713	SN74LS133
A70U3030	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A70U3040	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A70U3060	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A70U3070	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A70U3080	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A70U4020	156-0985-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	18324	N74LS260AN OR J
A70U4030	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	04713	MC6888/MC8T98L
A70U4040	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	04713	MC6888/MC8T98L
A70U4050	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	04713	MC6888/MC8T98L
A70U4060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	18324	8T26AF
A70U4070	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	18324	8T26AF
A70U4080	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	04713	MC6888/MC8T98L
A70Y2023	158-0115-00			XTAL UNIT,QTZ:16MHZ,0.01%,SERIES	01807	7-13P

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80	670-7342-00			CKT BOARD ASSY:SYSTEM RAM	80009	670-7342-00
A80C1010	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1021	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A80C1024	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1037	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1039	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1052	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1062	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1072	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1082	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1091	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A80C1092	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1093	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A80C1094	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1102	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1111	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1112	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1122	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1132	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1142	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1161	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A80C1171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C1181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2050	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2091	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A80C2092	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2111	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C2141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3091	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A80C3092	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3111	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80C3161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C3181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C4021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C4031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C4041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C4051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C4071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C4121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C4161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C4162	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C4181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C5011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C5091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C5131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C5141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C5161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C5171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80C5172	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A80C6161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A80CR1022	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80CR1023	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80CR1031	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80CR1032	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80CR1033	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80CR1034	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80CR1035	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80CR1036	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80DL1030	119-1407-00			DELAY LINE,ELEC:100NS,TAPPED,14 PIN	32440	TTLDM100
A80J6140	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A80R1038	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A80R1053	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A80R2051	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A80RP4010	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A80RP5110	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A80RP5132	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A80U1020	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A80U1040	156-0707-03			MICROCIRCUIT,DI:QUAD 2 INP EXCL OR GATE	07263	74S86
A80U1050	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUTSER SHF RGTR	01295	SN74LS164
A80U1060	156-1552-00			MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM	34649	D2118-4
A80U1140	156-1552-00			MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM	34649	D2118-4
A80U2010	156-0304-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74S20
A80U2020	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A80U2030	156-1250-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74S373J
A80U2060	156-1552-00			MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM	34649	D2118-4
A80U2140	156-1552-00			MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM	34649	D2118-4
A80U3010	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A80U3020	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A80U3060	156-1552-00			MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM	34649	D2118-4
A80U3140	156-1552-00			MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM	34649	D2118-4
A80U3150	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A80U3160	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A80U3170	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A80U3180	156-0303-01			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S03NP3
A80U4010	156-0392-02			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	80009	156-0392-02
A80U4020	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74S257NP3
A80U4030	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80U4040	156-0985-01			MICROCIRCUIT,DI:DUAL 5 INPUT NOR GATE,SCRN	04713	SN74LS260
A80U4050	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A80U4060	156-1552-00			MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM	34649	D2118-4
A80U4140	156-1552-00			MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM	34649	D2118-4
A80U4160	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A80U4170	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A80U4180	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NANOS-NAND	01295	SN74LS14NP3
A80U5010	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A80U5020	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A80U5030	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A80U5040	156-0915-02			MICROCIRCUIT,DI:9 BIT ODD/EVENPARITY GEN	01295	SN74LS280N3
A80U5050	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A80U5060	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A80U5070	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A80U5080	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A80U5090	156-0915-02			MICROCIRCUIT,DI:9 BIT ODD/EVENPARITY GEN	01295	SN74LS280N3
A80U5100	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A80U5120	156-1058-01			MICROCIRCUIT,DI:OCTAL ST BFR W/3 STATE OUT	01295	SN74S240JP4
A80U5130	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A80U5140	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A80U5150	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A80U5170	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A80U6150	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A80U6160	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
B200	119-0215-07			FAN,TUBEAXIAL:115,13W,3200RPM	80009	119-0215-07
B201	119-0147-00			FAN,AXIAL:115V,50-60HZ,14W	82877	028021
C3181	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C5171	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
CR1013	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
CR1014	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
CR1015	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
CR2013	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
F313	159-0174-00			FUSE,CARTRIDGE:3AG,8A,250V,5 SEC (STANDARD ONLY)	71400	ABC-8
	----- -----					
F313	159-0015-00			FUSE,CARTRIDGE:3AG,3A,250V,FAST-BLOW (OPTIONS A1,A2,A3 & A4 ONLY)	71400	AGC 3
	----- -----					
FL305	119-1313-00			FILTER,RFI:10A,115-230V,50-400HZ	56289	10JX5441A
S100	260-1989-00			SWITCH,ROCKER:DPST,16A,250VAC	000FJ	1602.0121
S110	260-1867-00			SWITCH,TOGGLE:SPDT,0.4A,20V	09353	7108-J61-CB8
S200	260-2056-00			CIRCUIT BREAKER:50A,270V	81541	UPG66-7361-1
S300	260-1967-00			SWITCH,SLIDE:DPDT,5A/250V,10A/125V MKD	000FJ	4021.0512
S301	260-2039-00			SWITCH,SLIDE:DPDT,5A,250V	000FJ	4021.0513
T311	120-1296-00			XFMR,PWR,STPDN:LOW FREQUENCY	80009	120-1296-00

Section 18
DIAGRAMS

Standards

The following American National Standard Institute standards are used in the preparation of Tektronix, Inc. diagrams.

Graphic Symbols	ANSI Y32.2–1975
Logic Symbols	ANSI Y32.14–1973 (Positive logic. Logic symbols depict the logical function performed and may differ from the manufacturer's data.)
Abbreviations	ANSI Y1.1–1972
Drafting Practices	ANSI Y14.15–1966
Line Conventions And Lettering	ANSI Y14.2–1973
Letter Symbols	ANSI Y10.5–1968

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).

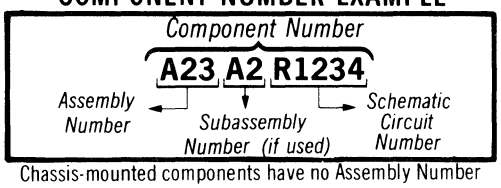
Resistors = Ohms (Ω)

The following special symbols may appear on the diagrams:

Assembly Numbers and Grid Coordinates

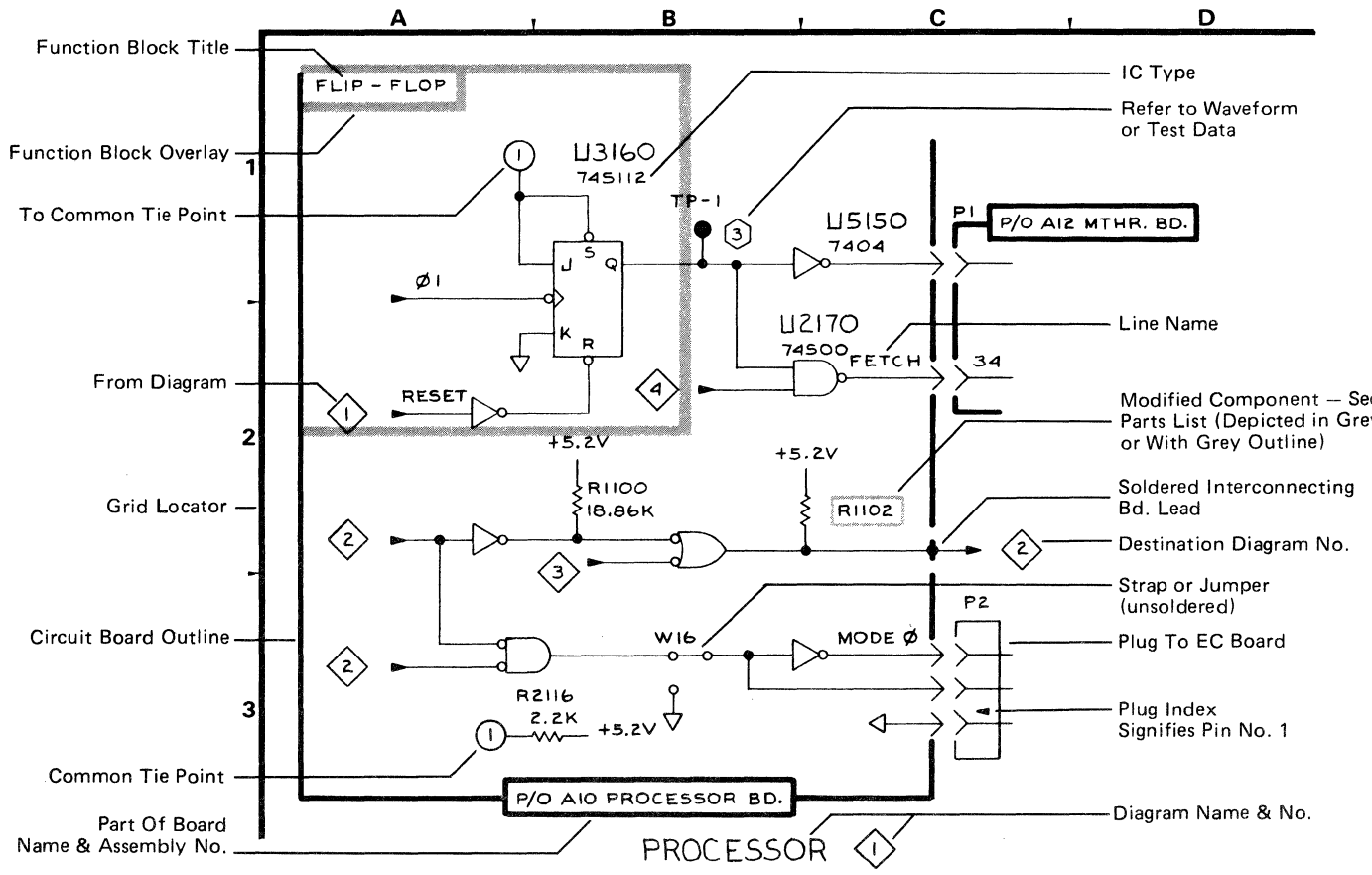
Each circuit board in the instrument is assigned an assembly number (e.g. A20). This number appears on the component location illustration, the schematics, and the component lookup table. The Replaceable Electrical Parts list also uses the number to list components by assembly. The following illustration shows an example of a component number in the Electrical Parts list.

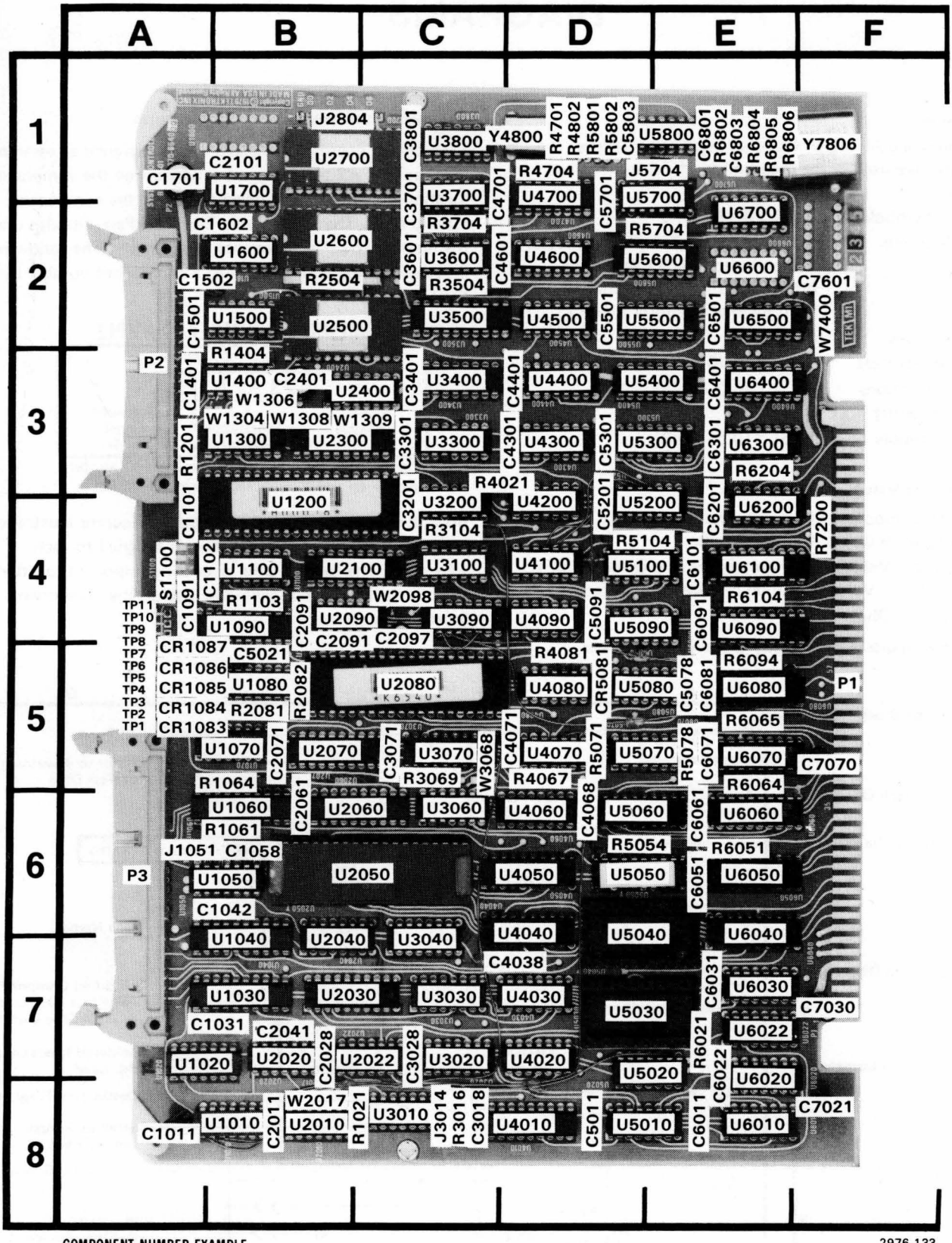
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

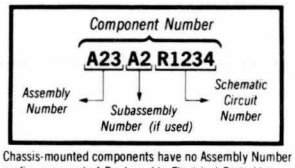
Both the schematics and the component locator illustration have locating grids. A lookup table is assigned to each schematic. The lookup table gives the component location in both the associated schematic, and on the component locator illustration.





2976-133

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 18-1. A20—System Controller Board.

Static Sensitive Devices
See Maintenance Section

Table 18-1
IC Pin Information

Device	GND	VCC	Device	GND	VCC	Device	GND	VCC
8T26	8	16	74LS113	7	14	74LS367	8	16
8T97	8	16	74LS125	7	14	74LS373	10	20
8T98	8	16	74LS133	8	16	74LS374	10	20
25LS252	10	20	74LS138	8	16	74LS390	8	16
74LS00	7	14	74LS139	8	16	74LS393	7	14
74LS02	7	14	74LS148	8	16	74LS472	10	20
74LS03	7	14	74LS151	8	16	82S116	8	16
74LS04	7	14	74LS153	8	16	1488	7	14
74LS06	7	14	74LS157	8	16	1489	7	14
74LS08	7	14	74LS161	8	16	2147	9	18
74LS10	7	14	74LS174	8	16	2332	12	24
74S10	7	14	74LS175	8	16	2650A	21	39
74LS11	7	14	74LS189	8	16	2716	12	24
74LS20	7	14	74LS191	8	16	4040B	8	16
74LS21	7	14	74LS193	8	16	6850	1	12
74LS27	7	14	74LS240	10	20	8257	20	31
74LS30	7	14	74LS244	10	20	AM26LS30	5	1
74LS32	7	14	74LS245	10	20	AM26LS32	8	16
74LS86	7	14	74LS257	8	16	IM5610	8	16
74S86	7	14	74LS260	7	14	LM723	7	12
74LS109	8	16	74LS273	10	20	MC723	7	12
74LS112	8	16	74LS348	8	16	Z80	29	11

Table 18-2
System Processor/Bank Switching Diagram 1

ASSEMBLY A20

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C7070	B1	F5	U2050	D2	C6
			U2060	B2	B6
CR5081	B1	D5	U3020A	D1	C7
			U3020A	D2	C7
J2804	C3	B1	U3040	D1	C7
			U3060B	E1	C6
P1	A1	F5	U3070	E3	C5
P1	F1	F5	U3090A	E3	C4
			U3500A	C3	C2
R1021	E1	C8	U3500E	B2	C2
R2082	C3	B5	U3500F	C3	C2
R2504	C2	B2	U4040	E2	D6
R3069	E3	C5	U4050	E2	D6
R3704	C3	C2	U4070A	E4	D5
R4067	E3	D5	U4070B	C3	D5
R4081	C1	D5	U4070F	C3	D5
R5071	B1	D5	U4080A	D4	D5
R5104	E1	D4	U4080D	D4	D5
R6051	E3	E6	U4090A	B2	D4
R6064	B1	E5	U4090C	E4	D4
R6064	F3	E5	U4090D	E1	D4
R6065	B1	E5	U4100D	E1	D4
R6094	C1	E5	U4200A	C2	D4
R6094	E4	E5	U5060	B3	D6
R6094	F3	E5	U5070C	C3	E5
R7200	C4	F4	U6060	B2	E6
			U6070H	B1	E5
TP3	D3	A5	U6080A	C4	E5
TP5	D3	A5	U6080B	C2	E5
TP6	E3	A5	U6080D	D4	E5
TP7	C3	A5	U6200A	C4	E4
TP8	E1	A5	U6200B	C2	E4
			U6200D	E3	E4
U1080A	C3	B5			
U2022E	D1	C7	W7400	C3	F2
U2040	C1	B7			

Partial A20 also shown on diagrams 2, 3, 4, 5 and 6.

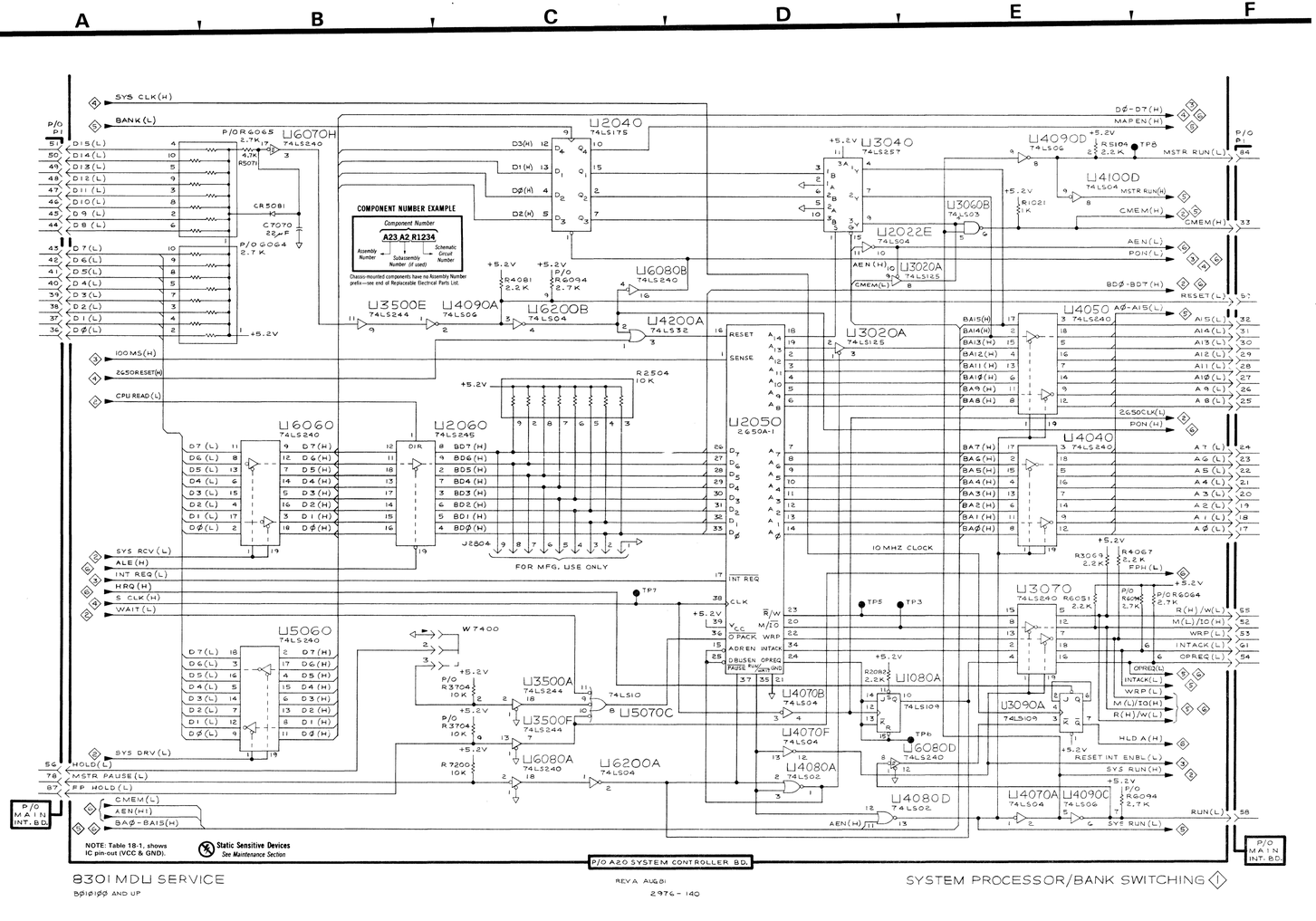


Table 18-3
ACIA Ports Diagram 2

ASSEMBLY A20					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1051	C3	A6	U1500D	E3	B2
			U1700C	E3	B1
P2	A4	A3	U1700D	E3	B1
P2	F1	A3	U2010A	B2	B8
			U2010C	B3	B8
R1404	E1	B3	U2020A	B2	B7
R1404	E2	B3	U2020B	C3	B7
R1404	E3	B3	U2500	E1	B2
R3504	E2	C2	U2600	E2	B2
R3504	E3	C2	U2700	E3	B1
R3704	D2	C2	U3060D	E2	C6
R4704	D1	D1	U3500C	E3	C2
R5104	C3	D4	U3500G	E3	C2
			U3500H	E2	C2
U1020A	B2	B7	U3600A	E1	C2
U1020C	C2	B7	U4090B	A2	D4
U1050B	B3	B6	U4700A	D1	D1
U1050C	C3	B6	U5020B	D4	D7
U1050D	C4	B6	U5040	D2	D6
U1400A	E1	B3	U5070B	C2	D5
U1400B	E1	B3	U5080D	D4	D5
U1400C	E1	B3	U6020	B2	E7
U1400D	E2	B3	U6500B	C1	E2
U1500A	E1	B2			
U1500B	E1	B2	W2017	A3	B8
U1500C	E2	B2			

Partial A20 also shown on diagrams 1, 3, 4, 5 and 6.

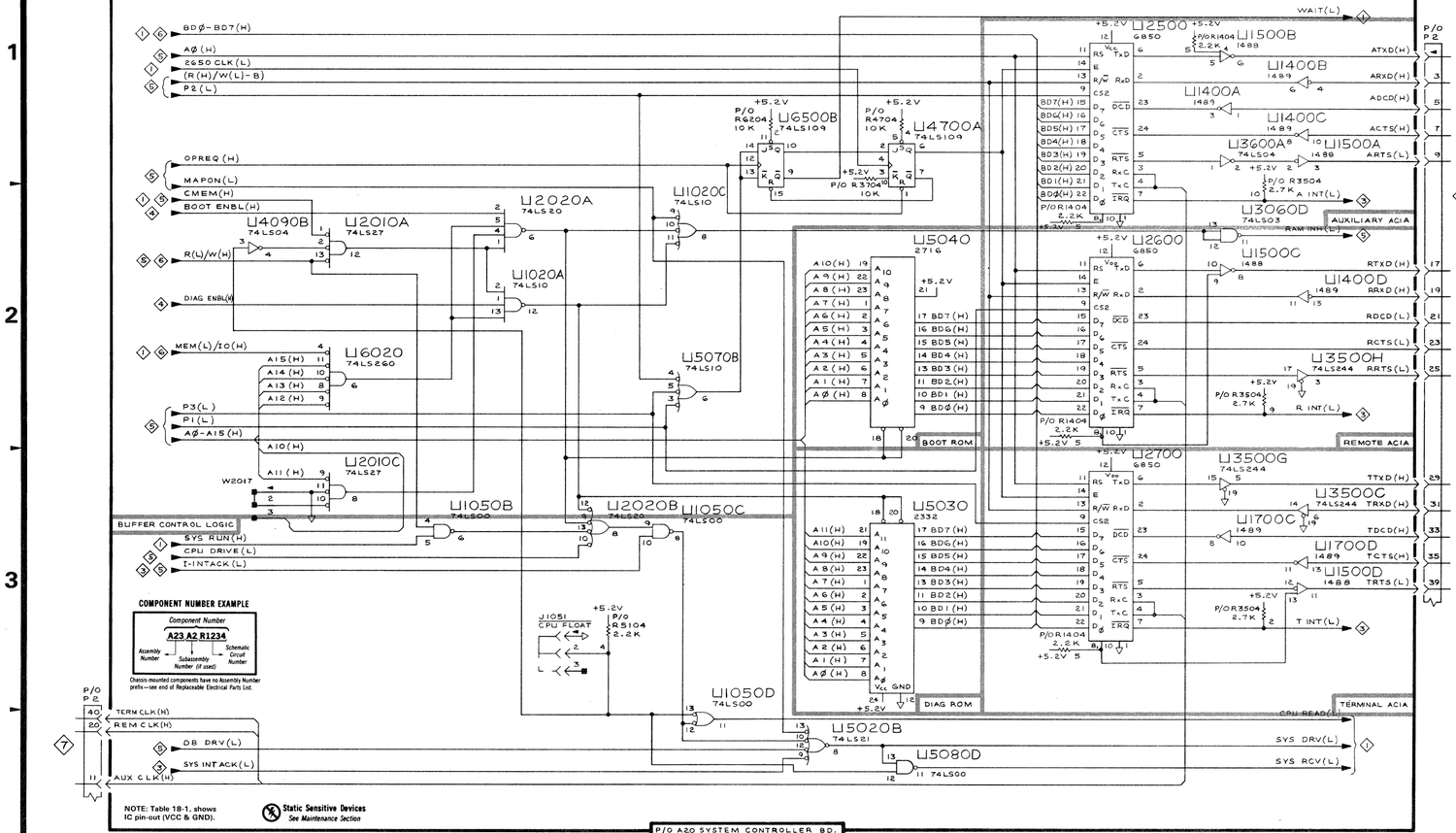


Table 18-4
Priority Interrupts Diagram 3

ASSEMBLY A20					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
CR01083	E2	A5	U1070	E2	B5
CR1084	E2	A5	U1100	E3	B4
CR1085	E2	A5	U2100	E1	B4
CR1086	E3	A5	U3200B	A4	C4
CR1087	E3	A5	U3500	B1	C2
			U3600	B2	C2
P1	A1	F5	U4100B	C3	D4
P1	F2	F5	U4200B	E3	D4
P2	A1	A3	U4200D	C3	D4
			U4500A	B2	D2
R1103	D3	B4	U4500B	E3	D2
R3504	B1	C2	U5090	D1	D4
R3504	B1	C2	U5100	D2	D4
R5104	A1	D4	U5200B	E3	D4
R5104	B3	D4	U5300	B3	D3
R5104	E1	D4	U5400B	C2	D3
R5704	B1	D1	U5500A	C3	D2
R5704	B3	D1	U5500B	B3	D2
R5704	C2	D1	U5600	B1	D2
R5704	C3	D1	U5700	B2	D1
R6065	A2	E5	U6070F	D3	E5
R6094	A1	E5	U6090	D1	E4
R6094	A2	E5	U6100	D2	E4
R6104	A1	E4	U6300	B4	E3
R6204	C2	E3	U6400A	C1	E3
			U6400B	C2	E3
S1100	D3	A4			
			W2098	E1	C4
U1010A	B4	B8			

Partial A20 also shown on diagrams 1, 2, 4, 5 and 6.

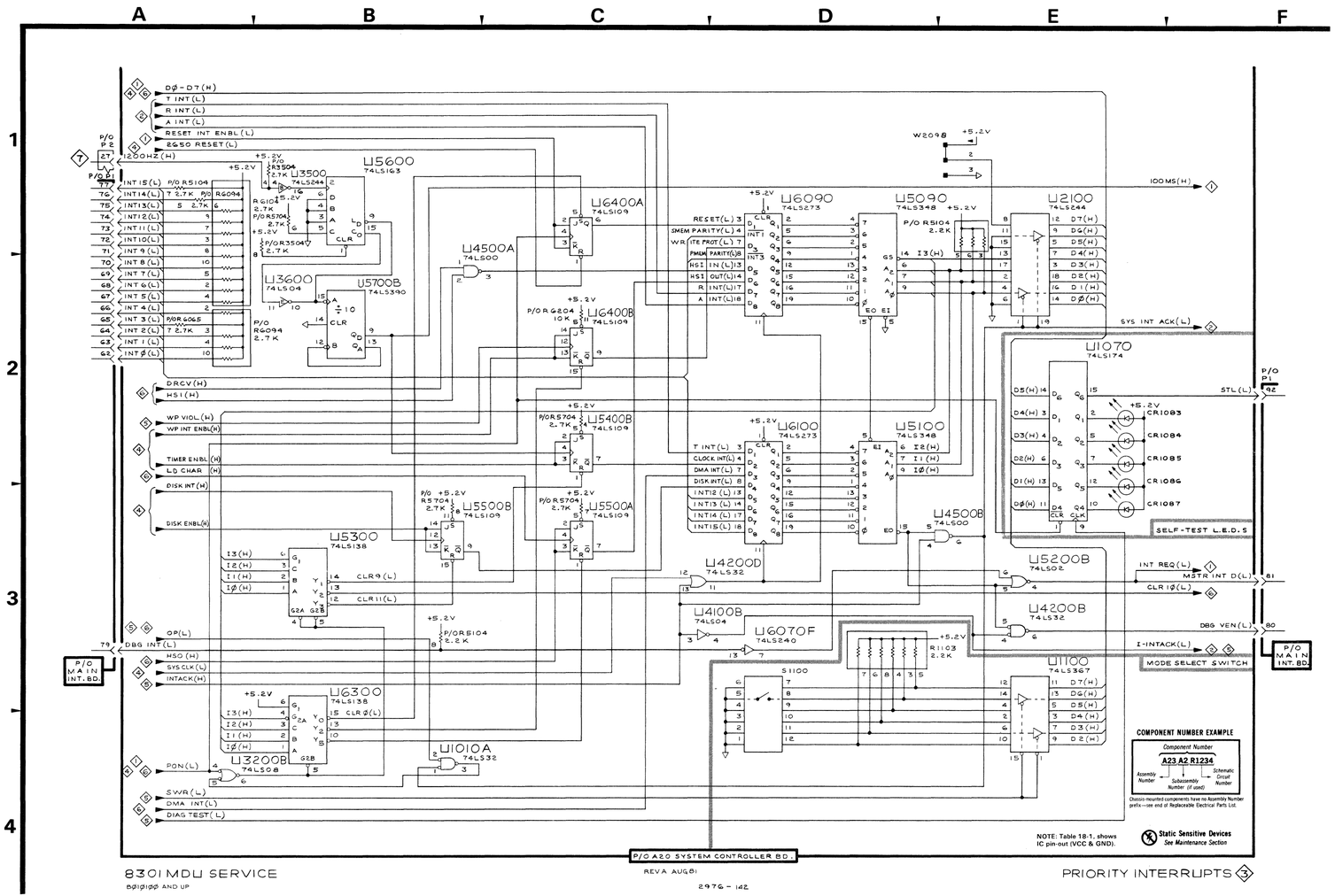


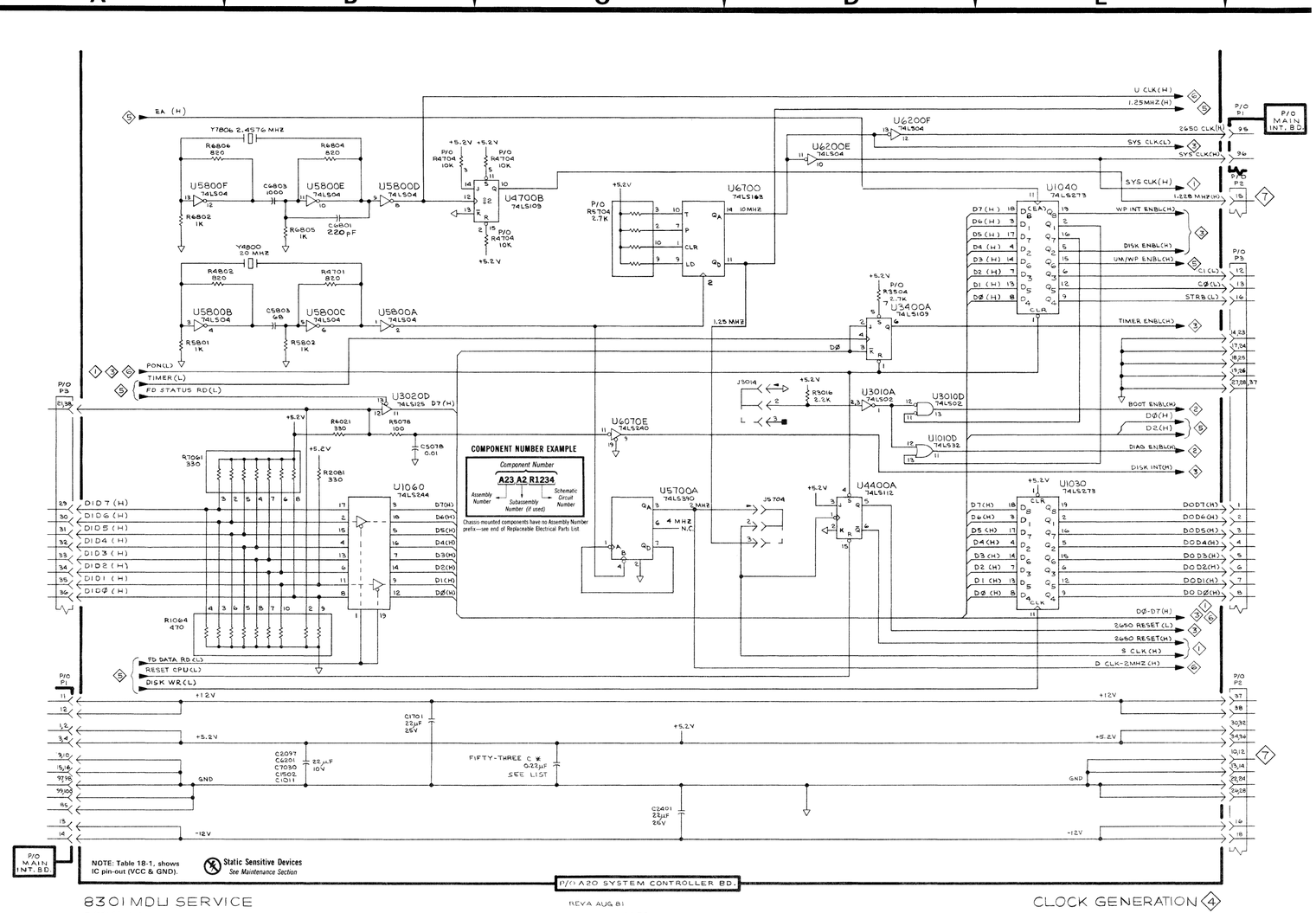
Table 18-5
Clock Generation Diagram 4

ASSEMBLY A20

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1011	B3	A8	C5091	C3*	D4	R4701	B2	D1
C1031	C3*	B7	C5201	C3*	D4	R4704	B1	D1
C1042	C3*	B6	C5301	C3*	D3	R4704	C1	D1
C1058	C3*	B6	C5501	C3*	D2	R4704	C1	D1
C1091	C3*	A4	C5701	C3*	D2	R4802	A2	D1
C1101	C3*	A4	C5803	B2	D1	R5078	B2	E5
C1102	C3*	B4	C6011	C3*	E8	R5704	C1	D1
C1401	C3*	A3	C6022	C3*	E8	R5801	A2	D1
C1501	C3*	A2	C6031	C3*	E7	R5802	B2	D1
C1502	B3	A2	C6051	C3*	E6	R6021	B2	E7
C1602	C3*	B2	C6061	C3*	E6	R6802	A1	E1
C1701	B3	A1	C6071	C3*	E5	R6804	B1	E1
C2011	C3*	B8	C6081	C3*	E5	R6805	B1	E1
C2028	C3*	B7	C6091	C3*	E4	R6806	A1	E1
C2041	C3*	B7	C6101	C3*	E4			
C2061	C3*	B6	C6101	C3*	E4	U1010D	D2	B8
C2071	C3*	B5	C6201	B3	E4	U1030	E3	B7
C2091	C3*	B4	C6301	C3*	E7	U1040	E1	B7
C2091	C3*	B4	C6401	C3*	E3	U1060	B3	B6
C2097	B3	C4	C6501	C3*	E2	U3010A	D2	C8
C2101	C3*	B1	C6801	B1	E1	U3010D	D2	C8
C2401	C4	B3	C6803	B1	E1	U3020D	B2	C7
C3018	C3*	C8	C7030	B3	F7	U3400A	D2	C3
C3028	C3*	C7	C7601	C3*	F2	U4400A	D2	D3
C3071	C3*	C5				U4700B	C1	D1
C3201	C3*	C4	J3014	D2	C8	U5700	C3	D1
C3301	C3*	C3	J5704	D3	E1	U5800A	B2	E1
C3401	C3*	C3				U5800B	A2	E1
C3601	C3*	C2	P1	A3	F5	U5800C	B2	E1
C3701	C3*	C2	P1	F1	F5	U5800D	B1	E1
C3801	C3*	C1	P2	F1	A3	U5800E	B1	E1
C4038	C3*	D7	P2	F3	A3	U5800F	A1	E1
C4068	C3*	D6	P3	A2	A6	U6070E	C2	E5
C4071	C3*	D5	P3	F2	A6	U6200E	D1	E4
C4301	C3*	D3				U6200F	D1	E4
C4401	C3*	D3	R1061	B2	B6	U6700	C1	E2
C4601	C3*	C2	R1064	B3	B5			
C4701	C3*	C1	R2081	B2	B5	Y4800	B1	D1
C5011	C3*	D8	R3016	D2	C8	Y7806	B1	F1
C5078	B2	E5	R3504	D2	C2			

Partial A20 also shown on diagrams 1, 2, 3, 5 and 6.

*indicating decoupling capacitor, 0.1 μF



8301 MDU SERVICE

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CLOCK GENERATION 4

Table 18-6
I/O Port Decode Diagram 5

ASSEMBLY A20					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P1	G3	F5	U4020D	D1	D7
			U4030	C4	D7
R4201	G3	D3	U4060	C2	D6
R5054	C2	D6	U4070C	B3	D5
R5704	F5	D1	U4070H	C4	D5
			U4080B	F4	D5
TP2	C4	A5	U4080C	D3	D5
			U4100A	B2	D4
U1010B	D2	B8	U4100C	D3	D4
U1010C	D3	B8	U5010	E1	D8
U1020B	E3	A7	U5050	C2	D6
U1600	C5	B2	U5070A	B3	D5
U2022A	F3	C7	U5080A	B4	D5
U2022B	E2	C7	U5080B	C3	E5
U2022C	D3	C7	U6010	E3	E8
U2022D	F2	C7	U6022	F1	E7
U2022F	D2	C7	U6030	F3	E7
U3030	C4	C7	U6040	B2	E6
U3060A	F3	C6	U6050	B1	E6
U3060C	F3	C6	U6070	B4	E5
U4010	D1	D8	U6080C	C5	E5
U4020A	F3	D7	U6500A	B5	E2
U4020B	E3	D7			
U4020C	C1	D7	W3068	B5	C5

Partial A20 also shown on diagrams 1, 2, 3, 4 and 6.

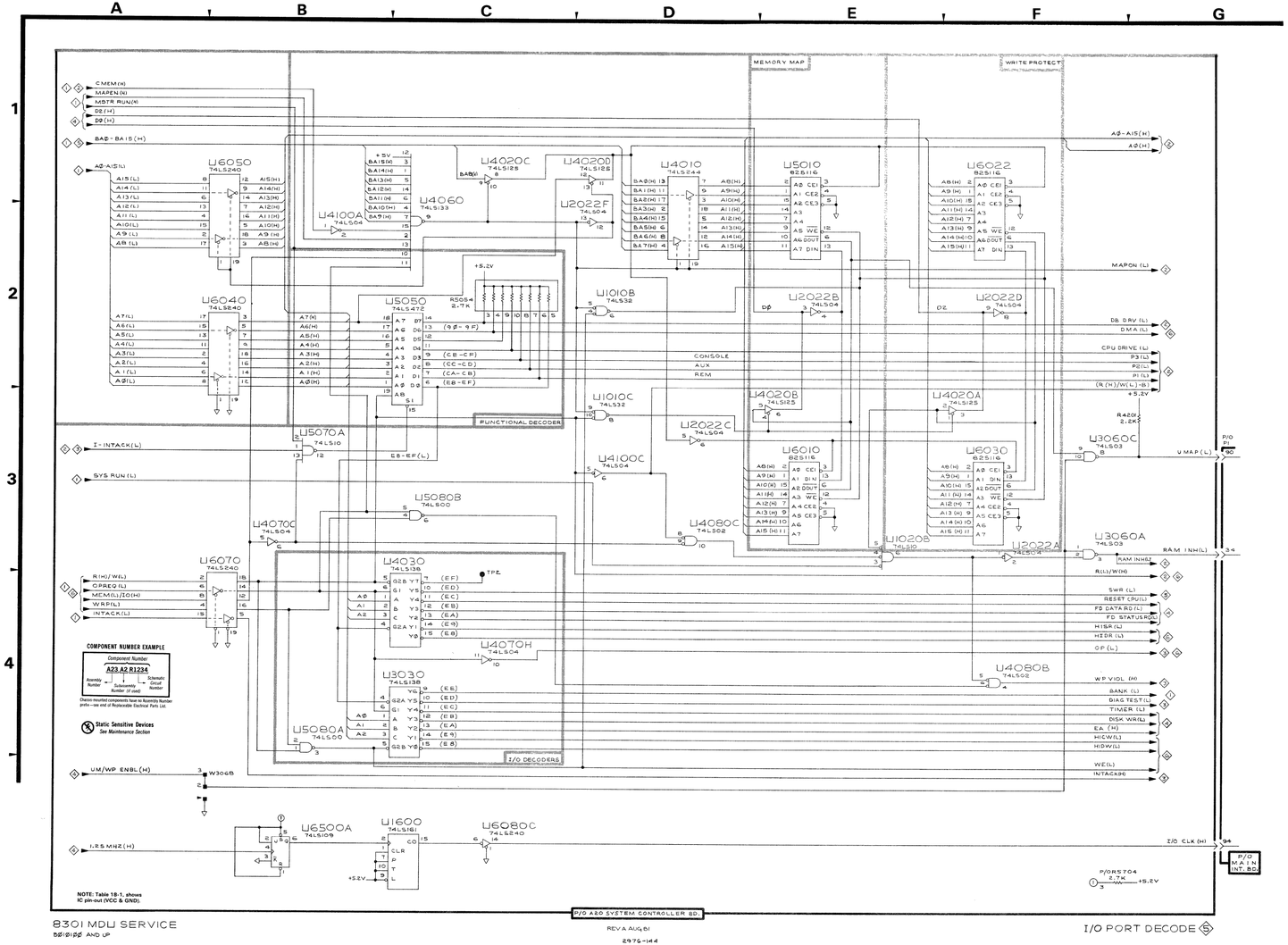
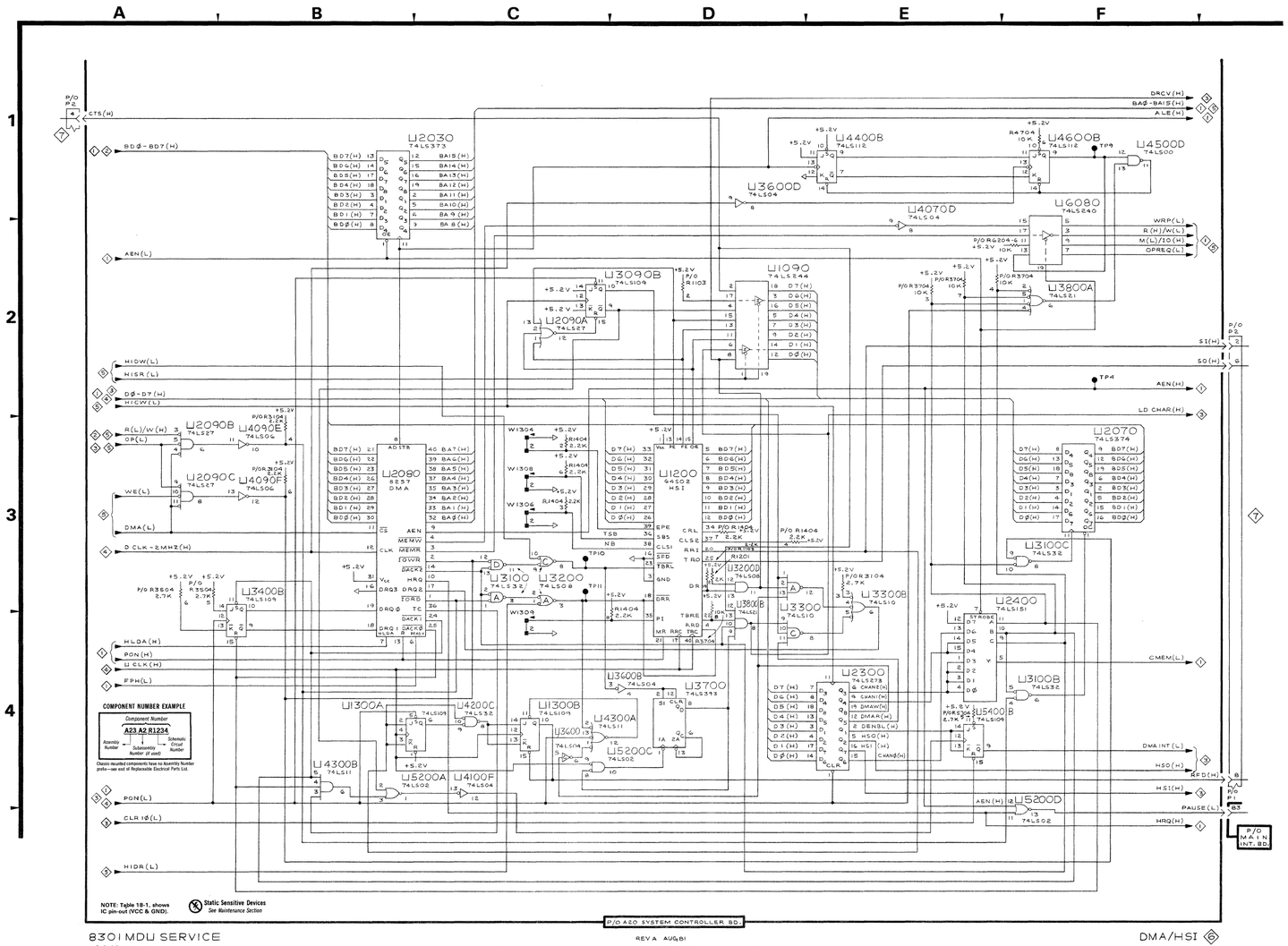
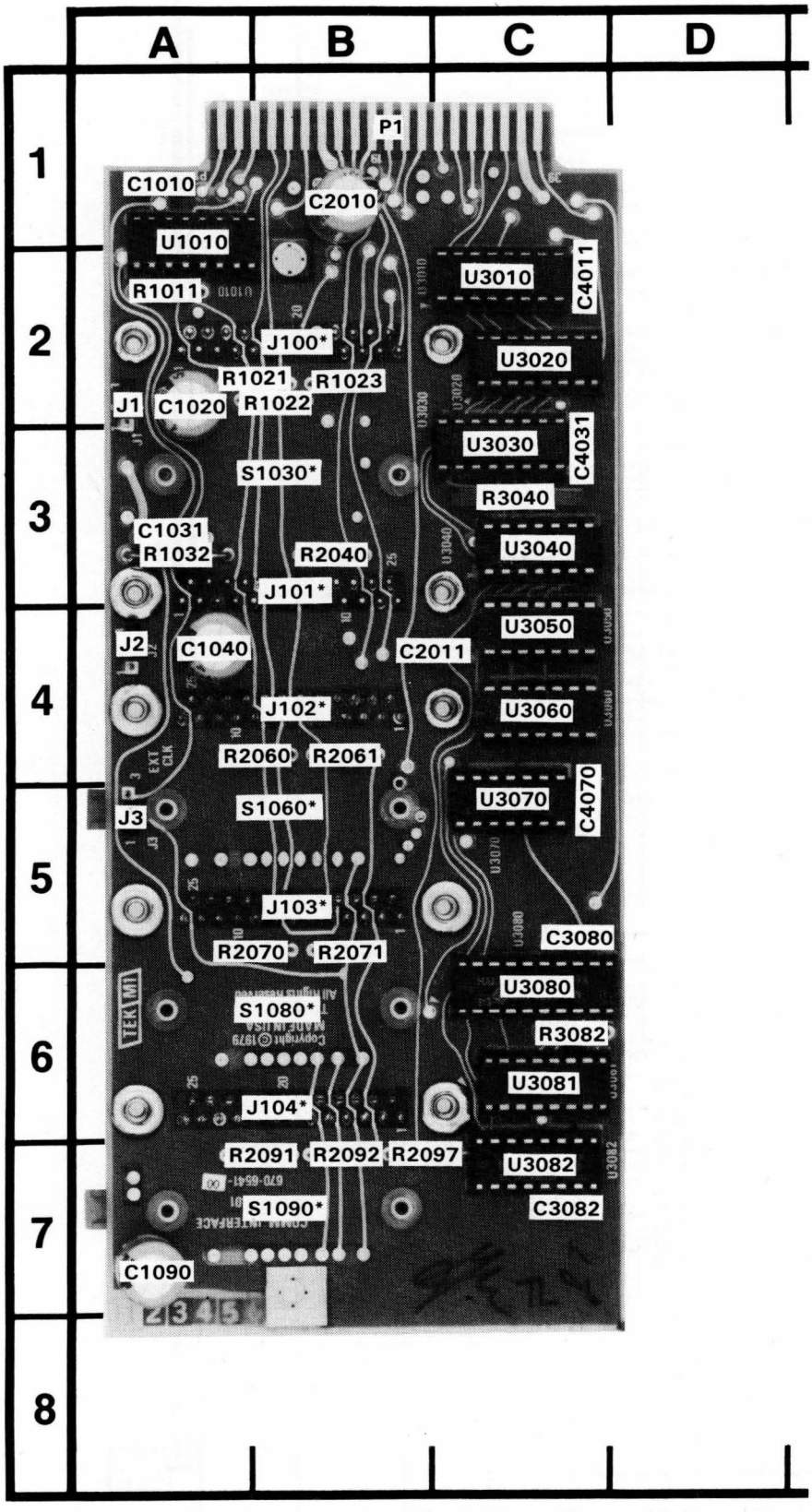


Table 18-7
DMA/HSI Diagram 6

ASSEMBLY A20					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P1	G4	F5	U3100A	C3	C4
P2	A1	A3	U3100B	F4	C4
P2	G2	A3	U3100C	F3	C4
			U3100D	C3	C4
R1103	D2	B4	U3200A	C3	C4
R1103	D3	B4	U3200C	C3	C4
R1201	D3	A3	U3200D	D3	C4
R1404	C3	B3	U3300A	D3	C3
R1404	D3	B3	U3300B	E3	C3
R3104	B3	C4	U3300C	D4	C3
R3104	E3	C4	U3400B	B4	C3
R3504	A3	C2	U3600B	D4	C2
R3704	D3	C2	U3600C	C4	C2
R3704	E2	C2	U3600D	D1	C2
R4704	F1	D1	U3700	D4	C1
R5704	E4	D1	U3800A	F2	C1
R6204	F2	E3	U3800B	D4	C1
			U4090E	B3	D4
TP4	F2	A5	U4090F	B3	D4
TP9	F1	A5	U4100F	C4	D4
TP10	C3	A5	U4200C	C4	D4
TP11	C3	A5	U4300A	C4	D3
			U4300B	B4	D3
U1090	D2	B4	U4400B	E1	D3
U1200	D3	B4	U4500D	F1	D2
U1300A	B4	B3	U4600B	F1	D2
U1300B	C4	B3	U5200A	B4	D4
U2030	B1	B7	U5200C	C4	D4
U2070	F3	B5	U5200D	F4	D4
U2080	B3	C5	U5400B	E4	E3
U2090A	C2	B4	U6080	F2	E5
U2090B	A3	B4			
U2090C	A3	B4	W1304	C3	B3
U2300	E4	B3	W1306	C3	B3
U2400	E4	C3	W1308	C3	B3
U3090B	C2	C4	W1309	C4	B3

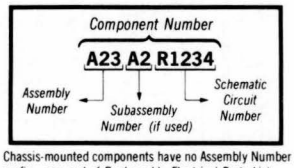
Partial A20 also shown on diagrams 1, 2, 3, 4 and 5.





*on back of board

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

Fig. 18-2. A10—Communications Interface Board.

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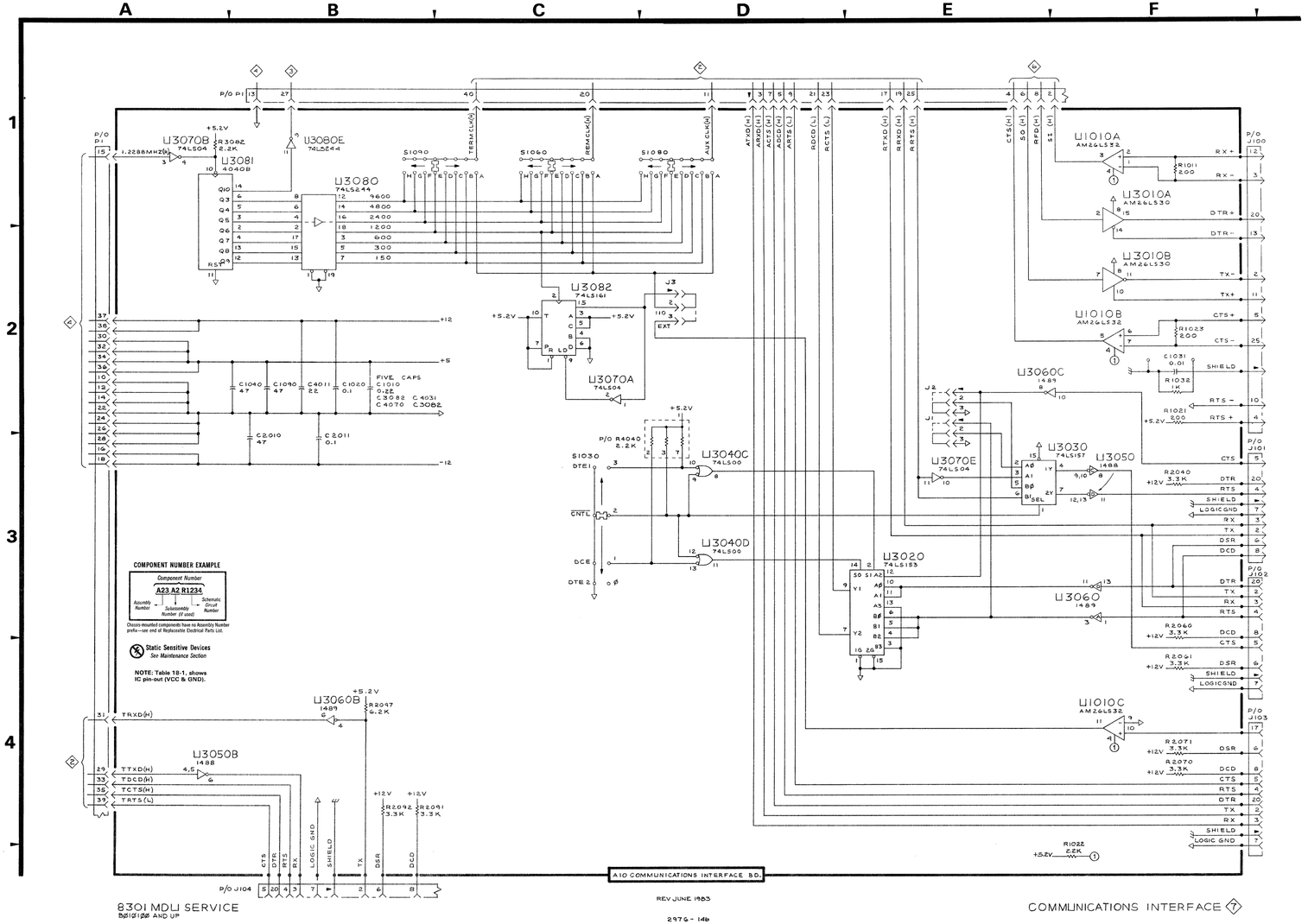
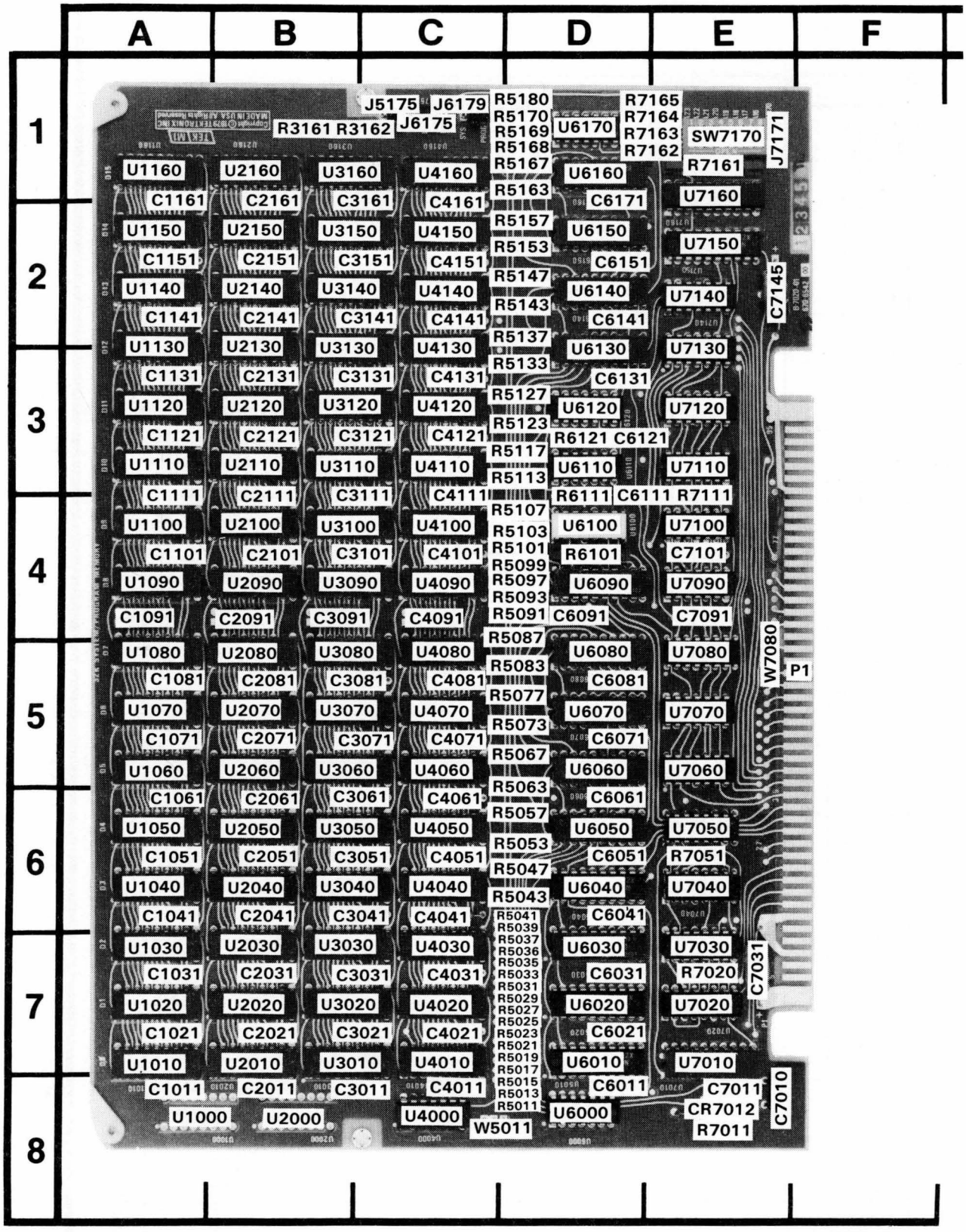
Table 18-8
Communications Interface Diagram 7

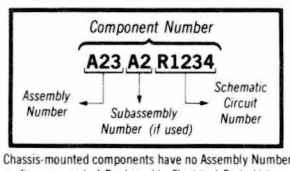
ASSEMBLY A10					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	B2	A1	R2092	B4	B7
C1020	B2	A2	R2097	B4	B7
C1031	F2	A3	R3040	D3	C3
C1040	A2	A4	R3082	A1	C6
C1090	B2	A7			
C2010	B3	B1	S1030	C3	B3
C2011	B3	C4	S1060	C1	B5*
C3082	B2	C7	S1080	D1	B6*
C4011	B2	C2	S1090	B1	B7*
C4031	B2	C3			
C4070	B2	C5	U1010A	F1	A1
			U1010B	F2	A1
J1	E2	A2	U1010C	F4	A1
J2	E2	A4	U3010A	F1	C2
J3	D2	A5	U3010B	F2	C2
J100	F1	B2*	U3020	E3	C2
J101	F3	B3*	U3030	E3	C3
J102	F3	B4*	U3040C	D3	C3
J103	F4	B5*	U3040D	D3	C3
J104	B5	B6*	U3050B	A4	C4
			U3050C	F3	C4
P1	A1	B1	U3050D	F3	C4
			U3060A	F3	C4
R1011	F1	A2	U3060B	B4	C4
R1021	F2	B2	U3060C	E2	C4
R1022	E4	B2	U3060D	F3	C4
R1023	F2	B2	U3070A	C2	C5
R1032	F2	A3	U3070B	A1	C5
R2040	F3	B3	U3070E	E3	C5
R2060	F4	B4	U3080E	B1	C6
R2061	F4	B4	U3080	B1	C6
R2070	F4	B5	U3081	A1	C6
R2071	F4	B5	U3082	C2	C7
R2091	B4	B7			

*on back of board





COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 18-3. A30—System/Program Memory Board.

Static Sensitive Devices
See Maintenance Section

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Table 18-9
Address Buffers Diagram 8

ASSEMBLY A30					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J7171	D2	E1	R7161	D2	E1
P1	A1	F1	SW7170	E1	E1
P1	C1	F1			
			U6010A	B4	D7
R5013	B4	D7	U6010B	B3	D7
R5015	B4	D8	U6020A	B3	D7
R5017	B4	D7	U6020B	B3	D7
R5021	B3	D7	U6030A	B2	D7
R5025	B3	D7	U6030B	B2	D7
R5027	B3	D7	U6040A	B1	D6
R5029	B3	D7	U6040B	B1	D6
R5035	B2	D7	U7140B	D2	E2
R5036	B2	D7	U7150	D1	E2
R5037	B2	D7	U7160	D1	E1
R5039	B2	D6			

Partial A30 also shown on diagrams 9, 10, 11 and 12.

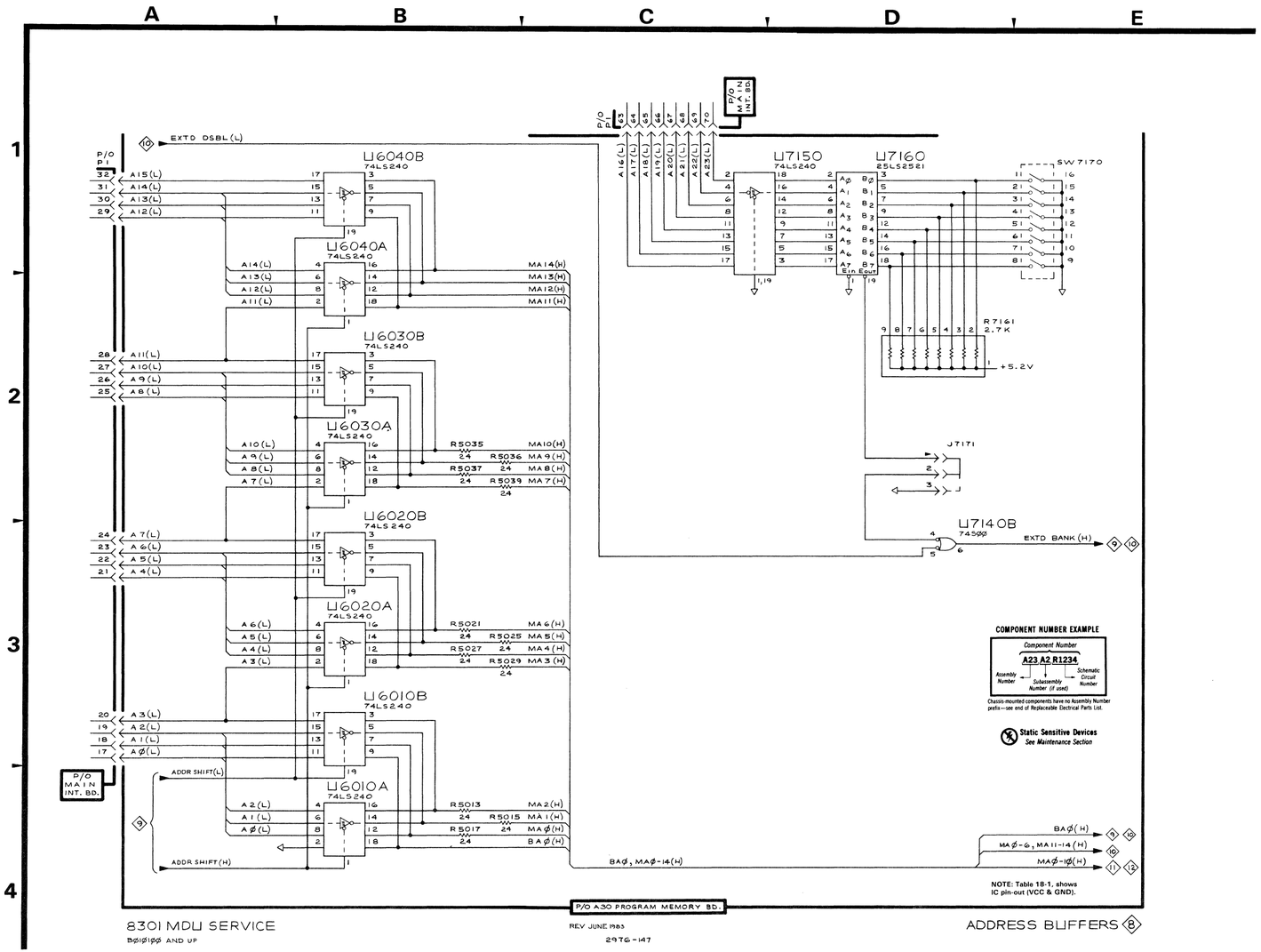


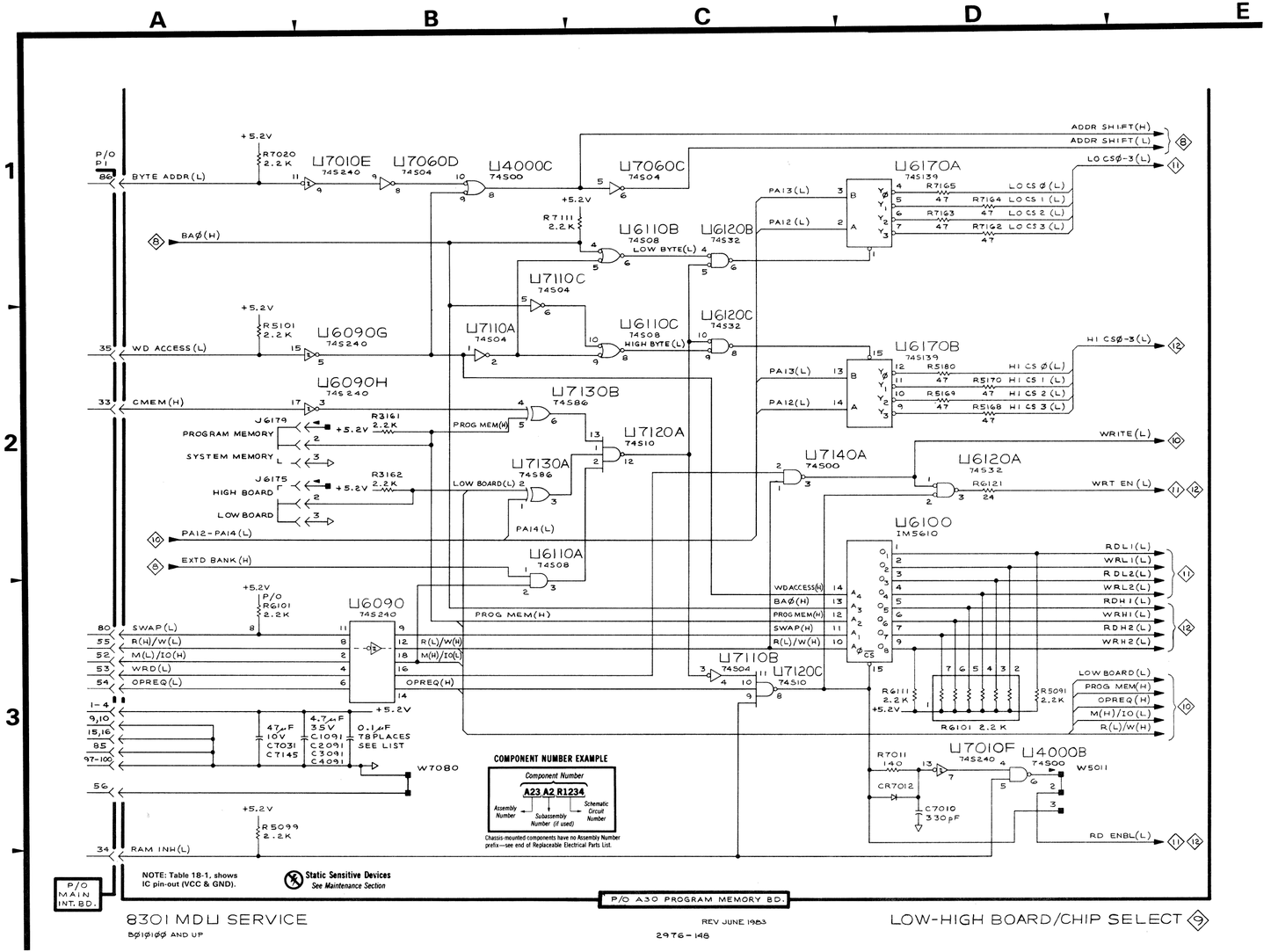
Table 18-10
Low-High Board Chip Select Diagram 9

ASSEMBLY A30

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1011	B3*	A8	C4011	B3*	C8	R5099	A3	D4
C1021	B3*	A7	C4021	B3*	C7	R5101	A2	D4
C1031	B3*	A7	C4031	B3*	C7	R5168	D2	D1
C1041	B3*	A6	C4041	B3*	C6	R5169	D2	D1
C1051	B3*	A6	C4051	B3*	C6	R5170	D2	D1
C1061	B3*	A6	C4061	B3*	C6	R5180	D2	D1
C1071	B3*	A5	C4071	B3*	C5	R6101	A3	D4
C1081	B3*	A5	C4081	B3*	C5	R6101	D3	D4
C1091	B3	A4	C4091	B3	C4	R6111	D3	D4
C1101	B3*	A4	C4101	B3*	C4	R6121	D2	D3
C1111	B3*	A4	C4111	B3*	C3	R7011	D3	E8
C1121	B3*	A3	C4121	B3*	C3	R7020	A1	E7
C1131	B3*	A3	C4131	B3*	C3	R7111	C1	E4
C1141	B3*	A2	C4141	B3*	C2	R7162	D1	D1
C1151	B3*	A2	C4151	B3*	C2	R7163	D1	D1
C1161	B3*	A2	C4161	B3*	C2	R7164	D1	D1
C2011	B3*	B8	C6011	B3*	D8	R7165	D1	D1
C2021	B3*	B7	C6021	B3*	D7			
C2031	B3*	B7	C6031	B3*	D7	U4000B	D3	C8
C2041	B3*	B6	C6041	B3*	D6	U4000C	B1	C8
C2051	B3*	B6	C6051	B3*	D6	U6090G	B2	D4
C2061	B3*	B6	C6061	B3*	D6	U6090H	B2	D4
C2071	B3*	B5	C6071	B3*	D5	U6090	B3	D4
C2081	B3*	B5	C6081	B3*	D5	U6100	D2	D4
C2091	B3	B4	C6091	B3*	D4	U6110A	B2	D3
C2101	B3*	B4	C6111	B3*	D4	U6110B	C1	D3
C2111	B3*	B4	C6121	B3*	D3	U6110C	C2	D3
C2121	B3*	B3	C6131	B3*	D3	U6120A	D2	D3
C2131	B3*	B3	C6141	B3*	D2	U6120B	C1	D3
C2141	B3*	B2	C6151	B3*	D2	U6120C	C2	D3
C2151	B3*	B2	C6171	B3*	D2	U6170A	D1	D1
C2161	B3*	B2	C7010	D3	E8	U6170B	D2	D1
C3011	B3*	C8	C7011	B3*	E8	U7010E	B1	E7
C3021	B3*	C7	C7031	A3	E7	U7010F	D3	E7
C3031	B3*	C7	C7091	B3*	E4	U7060C	C1	E5
C3041	B3*	C6	C7101	B3*	E4	U7060D	B1	E5
C3051	B3*	C6	C7145	A3	E2	U7110A	B2	E3
C3061	B3*	C6				U7110B	C2	E3
C3071	B3*	C5	CR7012	D3	E8	U7110C	B1	E3
C3081	B3*	C5				U7120A	C2	E3
C3091	B3	B4	J6175	B2	C1	U7120C	C3	E3
C3101	B3*	C4	J6179	B2	C1	U7130A	B2	E2
C3111	B3*	C4				U7130B	B2	E2
C3121	B3*	C3	P1	A1	F1	U7140A	C2	E2
C3131	B3*	C3						
C3141	B3*	C2	R3161	B2	B1	W5011	D3	D8
C3151	B3*	C2	R3162	B2	C1	W7080	B3	E5
C3161	B3*	C2	R5091	D3	D4			

Partial A30 also shown on diagrams 8, 10, 11 and 12.

*indicating decoupling capacitor, 0.1 μF



8301 MDU SERVICE

8Ø1Ø1ØØ AND UP

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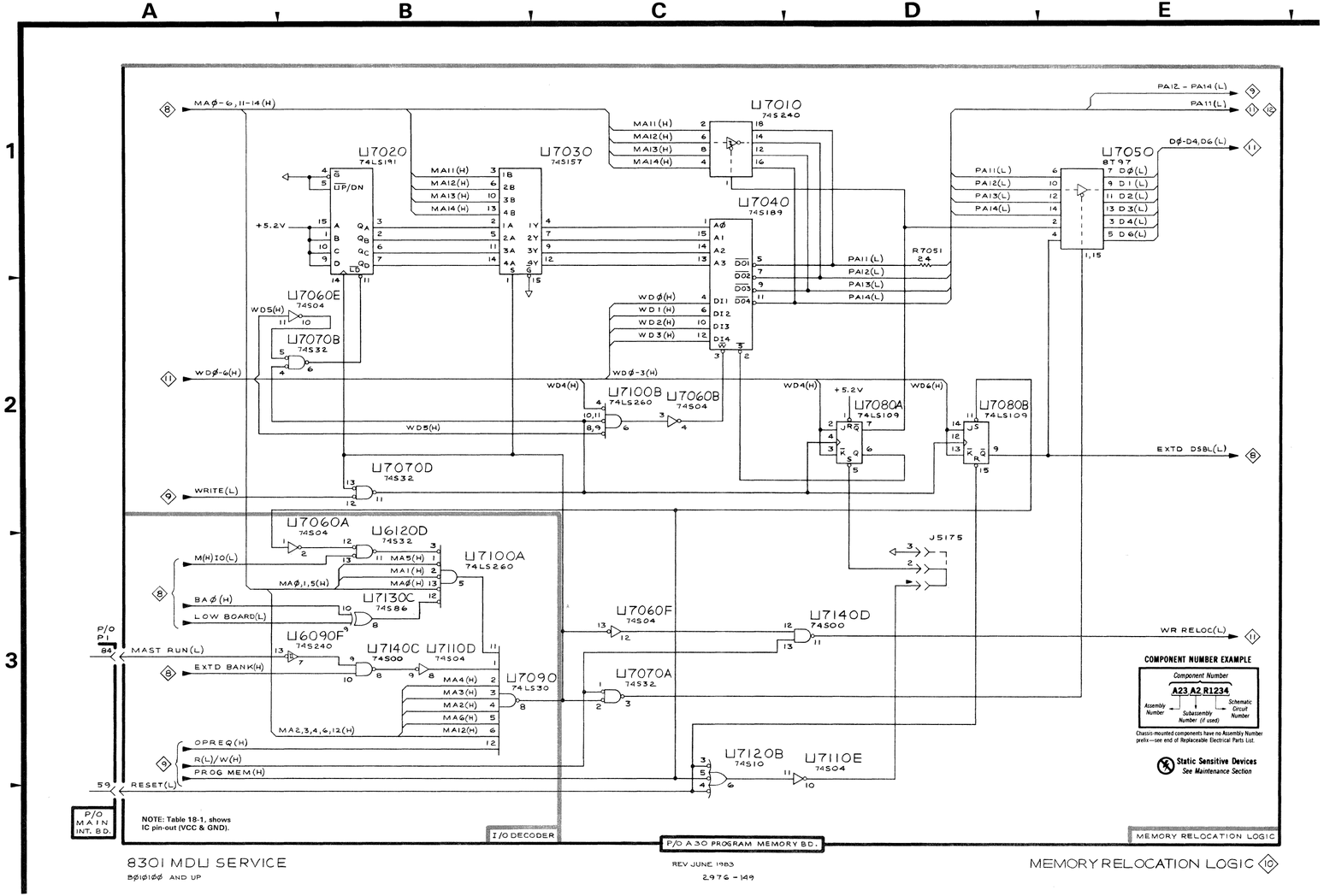
LOW-HIGH BOARD/CHIP SELECT 9

Table 18-11
Memory Relocation Logic Diagram 10

ASSEMBLY A30					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J5175	D3	C1	U7060F	C3	E5
			U7070A	C3	E5
P1	A3	F1	U7070B	B2	E5
			U7070D	B2	E5
R7051	D2	E6	U7080A	D2	E5
			U7080B	D2	E5
U6090F	B3	D4	U7090	B3	E4
U6120D	B3	D3	U7100A	B3	E4
U7010	C1	E7	U7100B	C2	E4
U7020	B1	E7	U7110D	B3	E3
U7030	B1	E7	U7110E	D4	E3
U7040	C1	E6	U7120B	C4	E3
U7050	E1	E6	U7130C	B3	E2
U7060A	B3	E5	U7140C	B3	E2
U7060B	C2	E5	U7140D	D3	E2
U7060E	B2	E5			

Partial A30 also shown on diagrams 8, 9, 11 and 12.



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MEMORY RELOCATION LOGIC 10

Table 18-12
Low Byte Memory Array Diagram 11

ASSEMBLY A30					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P1	A1	F1	U2050	D2	B6
			U2060	E2	B5
R5011	C4	D8	U2070	E2	B5
R5019	C2	D7	U2080	E2	B5
R5023	B4	D7	U3010	C3	B7
R5031	B2	D7	U3020	C3	B7
R5033	C4	D7	U3030	D3	B7
R5041	C2	D6	U3040	D3	B6
R5043	B4	D6	U3050	D3	B6
R5047	B1	D6	U3060	E3	B5
R5053	C4	D6	U3070	E3	B5
R5057	C1	D6	U3080	E3	B5
R5063	B4	D5	U4010	C4	C7
R5067	B1	D5	U4020	C4	C7
R5073	C4	D5	U4030	D4	C7
R5077	C1	D5	U4040	D4	C6
R5083	B4	D5	U4050	D4	C6
R5087	B1	D4	U4060	E4	C5
			U4070	E4	C5
U1010	C2	A7	U4080	E4	C5
U1020	C2	A7	U6000C	A4	D8
U1030	D2	A7	U6000D	A2	D8
U1040	D2	A6	U6050A	B2	D6
U1050	D2	A6	U6050B	B1	D6
U1060	E2	A5	U6060A	B1	D5
U1070	E2	A5	U6060B	B2	D5
U1080	E2	A5	U6070A	B4	D5
U2010	C2	B7	U6070B	B3	D5
U2020	C2	B7	U6080A	B3	D5
U2030	D2	B7	U6080B	B4	D5
U2040	D2	B6	U6110D	A1	D3

Partial A30 also shown on diagrams 8, 9, 10 and 12.

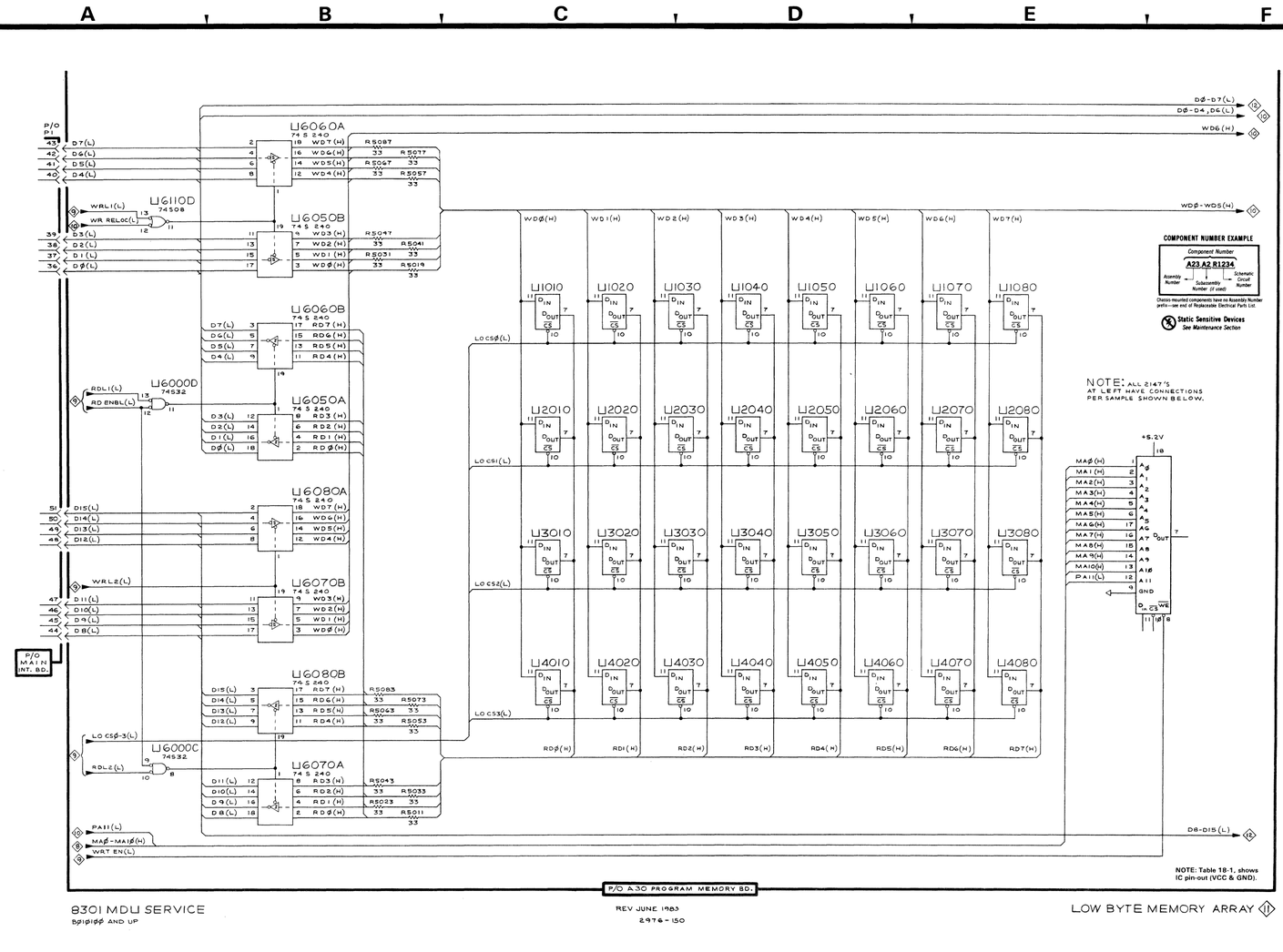
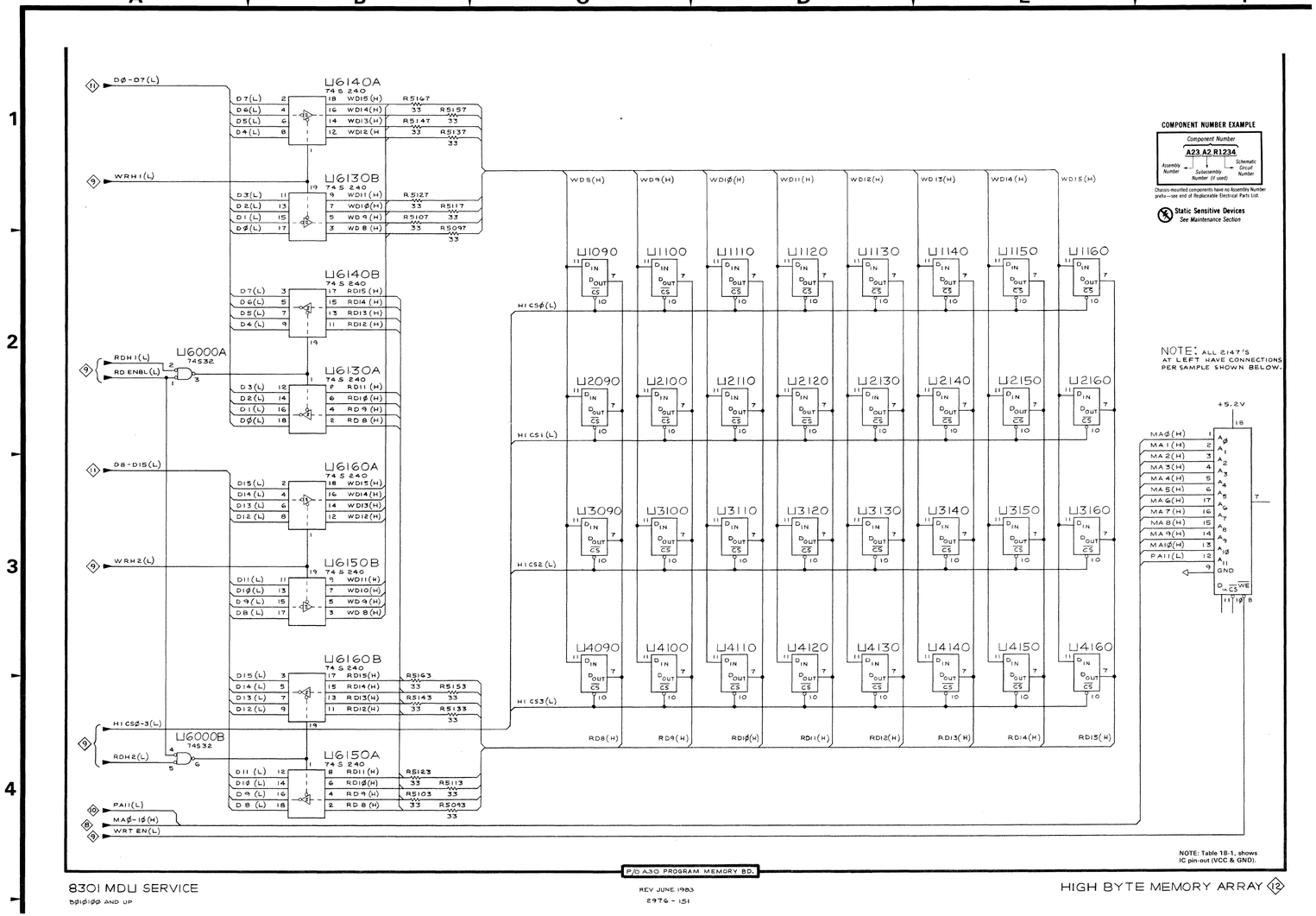


Table 18-13
High Byte Memory Array Diagram (12)

ASSEMBLY A30					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R5093	B4	D4	U2140	E2	B2
R5097	B2	D4	U2150	E2	B2
R5103	B4	D4	U2160	E2	B1
R5107	B2	D4	U3090	C3	B4
R5113	B4	D3	U3100	C3	B4
R5117	B1	D3	U3110	D3	B3
R5123	B4	D3	U3120	D3	B3
R5127	B1	D3	U3130	D3	B3
R5133	B4	D3	U3140	E3	B2
R5137	B1	D2	U3150	E3	B2
R5143	B4	D2	U3160	E3	B1
R5147	B1	D2	U4090	C4	C4
R5153	B4	D2	U4100	C4	C4
R5157	B1	D2	U4110	D4	C3
R5163	B4	D1	U4120	D4	C3
R5167	B1	D1	U4130	D4	C3
			U4140	E4	C2
U1090	C2	A4	U4150	E4	C2
U1100	C2	A4	U4160	E4	C1
U1110	D2	A4	U6000A	A2	D8
U1120	D2	A3	U6000B	A4	D8
U1130	D2	A2	U6130A	B2	D3
U1140	E2	A2	U6130B	B1	D3
U1150	E2	A2	U6140A	B1	D2
U1160	E2	A1	U6140B	B2	D2
U2090	C2	B4	U6150A	B4	D2
U2100	C2	B4	U6150B	B3	D2
U2110	D2	B4	U6160A	B3	D1
U2120	D2	B3	U6160B	B4	D1
U2130	D2	B3			

Partial A30 also shown on diagrams 8, 9, 10 and 11.



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BD10100 AND UP

P/O A30 PROGRAM MEMORY BD.

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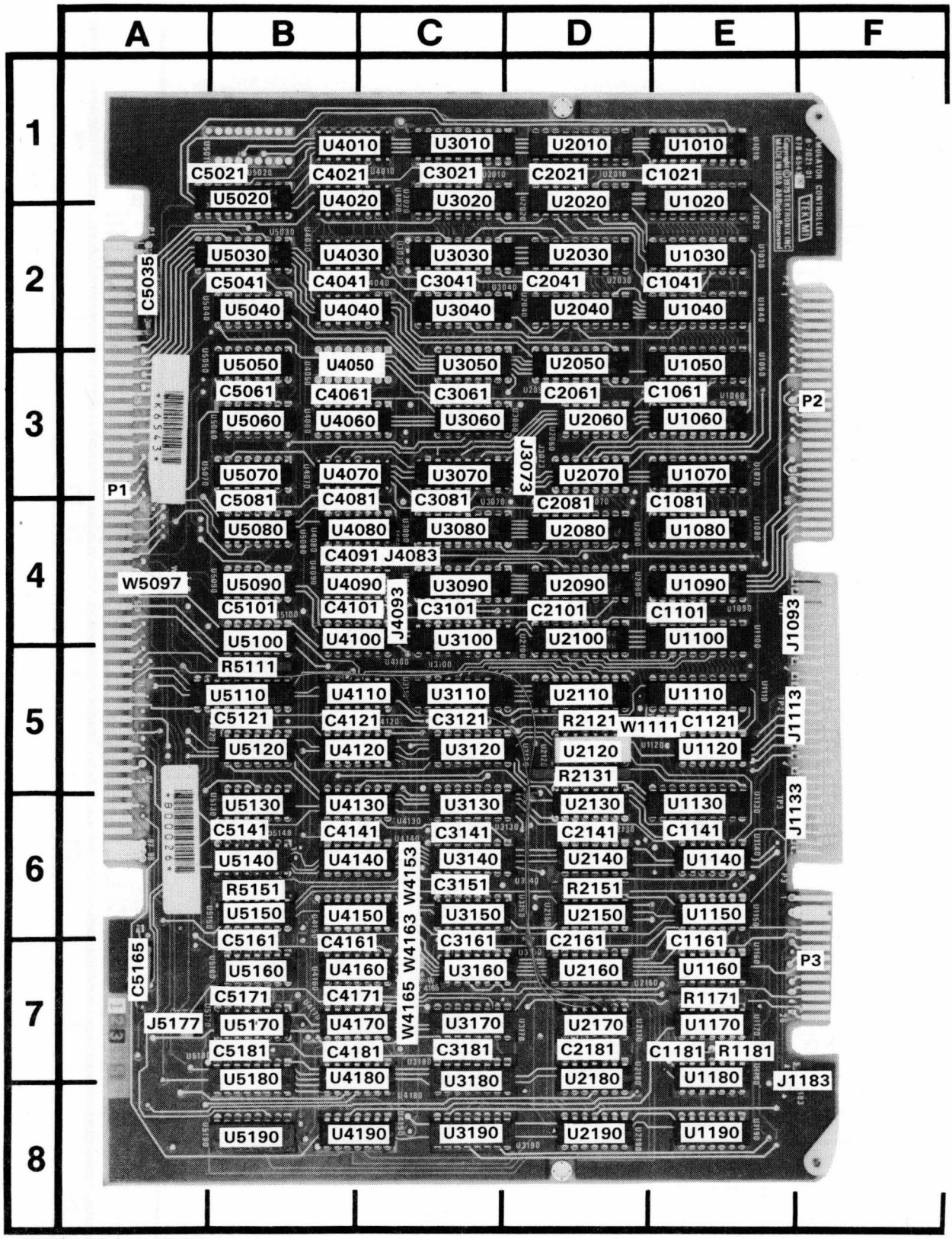
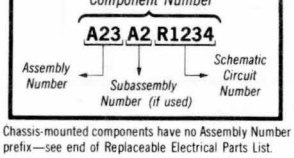
HIGH BYTE MEMORY ARRAY (12)



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 18-4. A40—Emulator Controller Board.

Static Sensitive Devices
See Maintenance Section

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Table 18-14
System/Program Processor Control Diagram 13

ASSEMBLY A40					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1133	B1	F6	U3190A	D1	C8
J1133	B2	F6	U3190B	C1	C8
J1133	D3	F6	U4050D	A2	B3
			U4120B	D2	C5
P1	A2	A3	U4130C	C1	C6
P1	E3	A3	U4130D	B2	C6
P3	A1	F7	U4140A	B1	C6
P3	E3	F7	U4140B	B2	C6
			U4140C	B2	C6
R1171	A1	E7	U4140E	D3	C6
R2151	C1	D6	U4170C	D3	C7
R2151	D4	D6	U4180B	D3	C7
R5151	A2	B6	U4190A	B3	C8
R5151	A3	B6	U5100C*	B2	B4
			U5130C	B2	B6
U3160B	D2	C7	U5150A	B3	B6
U3170A	B1	C7	U5150B	B3	B6
U3170B	B1	C7	U5150C	B3	B6
U3180A	C3	C7	U5150D	C1	B6
U3180B	C3	C7	U5160B	C3	B7

Partial A40 also shown on diagrams 14, 15, 16, 17, 18 and 19.

*See Parts List for Serial Number Ranges.

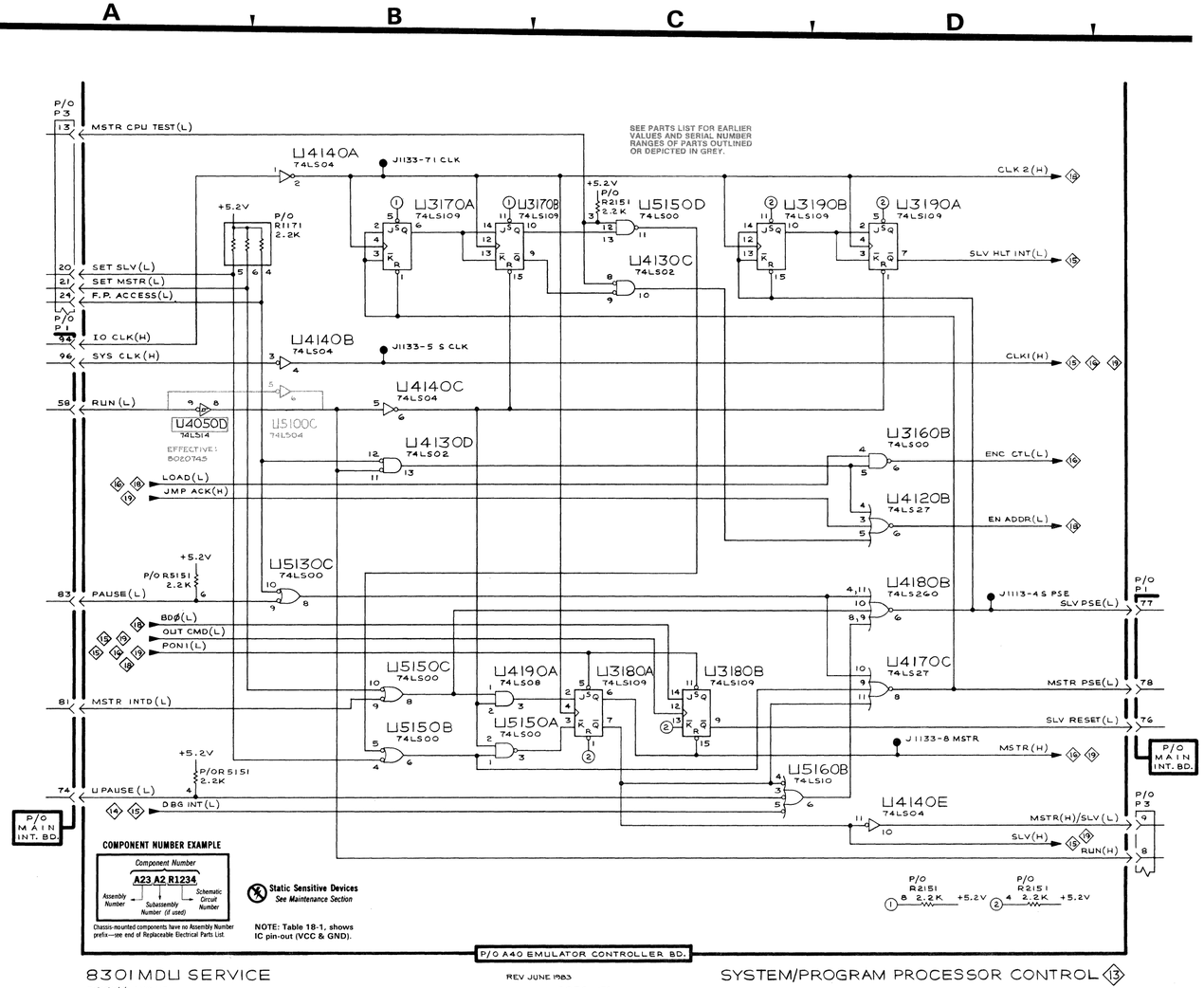


Table 18-15
Breakpoint Logic Diagram 14

ASSEMBLY A40					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1093	E2	F4	U3040	C3	C2
J1113	E1	F5	U3060	C1	C3
J1113	E2	F5	U3080	B2	C4
J4083	E2	C4	U3090	C2	C4
J4093	E1	C4	U4060	D1	B3
			U4080	E2	C4
U2010	B2	D1	U4090A	E2	C4
U2020	D2	D1	U4090B	E2	C4
U2030	B3	D2	U4090C	E2	C4
U2040	D3	D2	U4090D	E1	C4
U2080	B2	D4	U4090E	E1	C4
U2090	D2	D4	U4090F	E1	C4
U3010	B2	C1	U4100	E1	B4
U3020	C2	C1	U4110A	E3	C5
U3030	B3	C2	U5090A	D1	B4

Partial A40 also shown on diagrams 13, 15, 16, 17, 18 and 19.

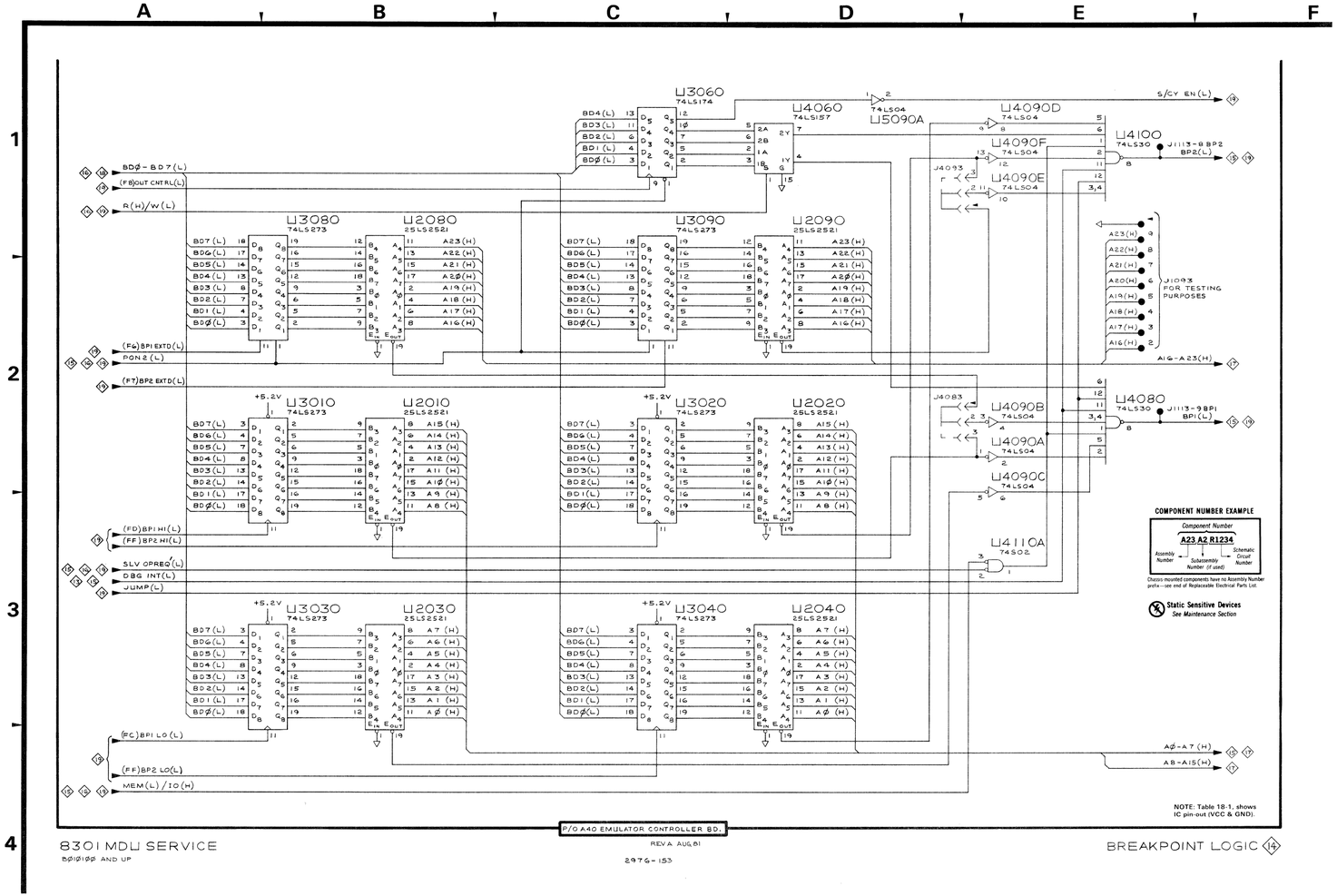


Table 18-16
Interrupt Logic Diagram 15

ASSEMBLY A40					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1113	E3	F5	U3130A	B2	C6
J3073	E3	D3	U3130B	B2	C6
J5177	D2	A7	U4070	E2	B3
			U4110D	D2	C5
P1	A2	A3	U4120A	C2	C5
P1	A3	A3	U4120C	D2	C5
P1	F1	A3	U4130B	B2	C6
P3	A3	F7	U4150A	E1	C6
			U4190B	E2	C8
R1171	A3	E7	U5040	C2	B2
R2151	A4	D6	U5050	C2	B3
R2151	B4	D6	U5070	D2	B3
R5111	A3	B5	U5080A	E2	B4
			U5080B	E2	B4
U1120C	A2	E5	U5080C	E3	B4
U1130	D3	E6	U5080D	E2	B4
U1140A	E3	E6	U5090D	C2	B4
U1150A	B3	E6	U5090E	E3	B4
U1150B	B3	E6	U5100A	E1	B6
U1160A	B3	E7	U5100E	E3	B4
U1160B	C3	E7	U5110C	B3	B5
U1170A	C3	E7	U5110D	B3	B5
U1170B	C3	E7	U5110H	A2	B5
U1180A	D3	E7	U5120A	C2	B5
U1180B	D3	E7	U5130A	C2	B6
U1190A	E1	E8	U5130B	E2	B6
U1190B	A4	E8	U5170A	B2	B7
U2130	D2	D6	U5170B	D1	B7
U2150A	D1	D6	U5180A	E2	B7
U2170E	E1	D7			
U2180A	E1	D7	W4153	E1	C6

Partial A40 also shown on diagrams 13, 14, 16, 17, 18 and 19.

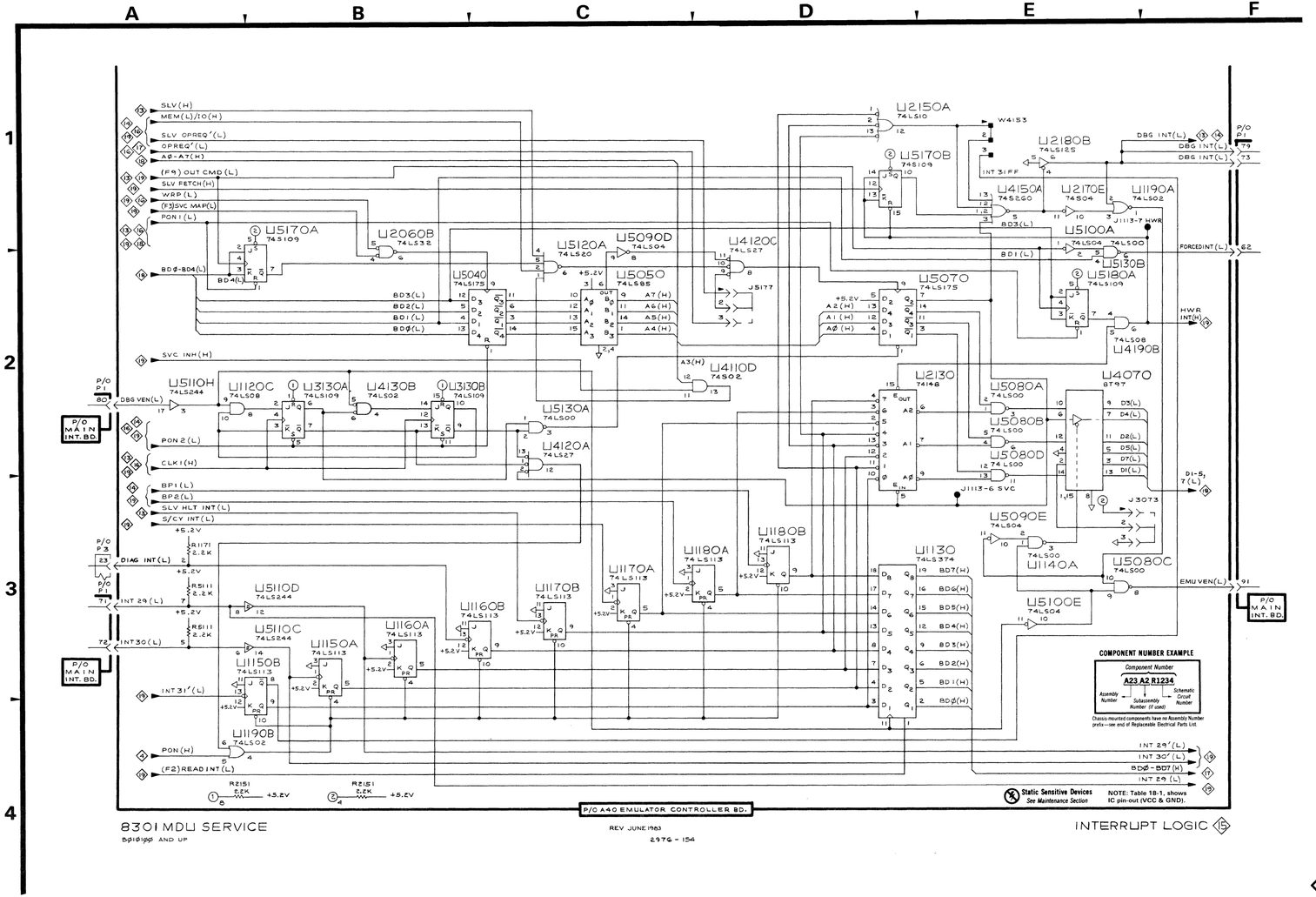


Table 18-17
Front Panel Interface Diagram 16

ASSEMBLY A40					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1021	C4*	E1	C5181	C4*	B7
C1041	C4*	E2			
C1061	C4*	E3	J1113	B4	F5
C1081	C4*	E4	J1133	B3	F6
C1101	C4*	E4	J1133	B4	F6
C1121	C4*	E5	J1183	C3	F7
C1141	C4*	E6			
C1161	C4*	E7	P1	A2	A3
C1181	C4*	E7	P1	E1	A3
C2021	C4*	D1	P2	A1	F3
C2041	C4*	D2	P2	E2	F3
C2061	C4*	D3	P3	A1	F7
C2081	C4*	D4	P3	E3	F7
C2101	C4*	D4			
C2141	C4*	D6	R1181	A1	E7
C2161	C4*	D7	R2151	A2	D6
C2181	C4*	D7	R2151	C3	D6
C3021	C4*	C1	R5111	A2	B5
C3041	C4*	C2	R5111	B2	B5
C3061	C4*	C3	R5111	B3	B5
C3081	C4*	C4	R5151	B3	B6
C3101	C4*	C4	R5151	E4	B6
C3121	C4*	C5			
C3141	C4*	C6	U1070	D3	E3
C3151	C4*	C6	U1080	D1	E4
C3161	C4*	C7	U1090	D2	E4
C3181	C4*	C7	U1140D	C3	E6
C4021	C4*	B1	U2140A	C3	D6
C4041	C4*	B2	U2140D	B2	D6
C4061	C4*	B3	U2140E	B2	D6
C4081	C4*	B3	U2140	D1	D6
C4091	C4*	B4	U2180A	B1	D7
C4101	C4*	B4	U2180D	C2	D7
C4121	C4*	B5	U2190B	B1	D8
C4141	C4*	B6	U4170B	B2	C7
C4161	C4*	B7	U5090B	C2	B4
C4171	C4*	C7	U5110A	D3	B5
C4181	C4*	C7	U5110B	C2	B5
C5021	C4*	B1	U5110E	B3	B5
C5035	C3	A2	U5110F	B3	B5
C5041	C4*	B2	U5120B	B3	B5
C5061	C4*	B3	U5130D	B3	B6
C5081	C4*	B4	U5140E	C1	B6
C5101	C4*	B4	U5140F	B1	B6
C5121	C4*	B5	U5140	B2	B6
C5141	C4*	B6	U5190A	B1	B8
C5161	C4*	B6	U5190B	C2	B8
C5165	C3	A7			
C5171	C4*	B7	W5097	B4	A4

Partial A40 also shown on diagrams 13, 14, 15, 17, 18 and 19.

*indicating decoupling capacitor, 0.1 μF

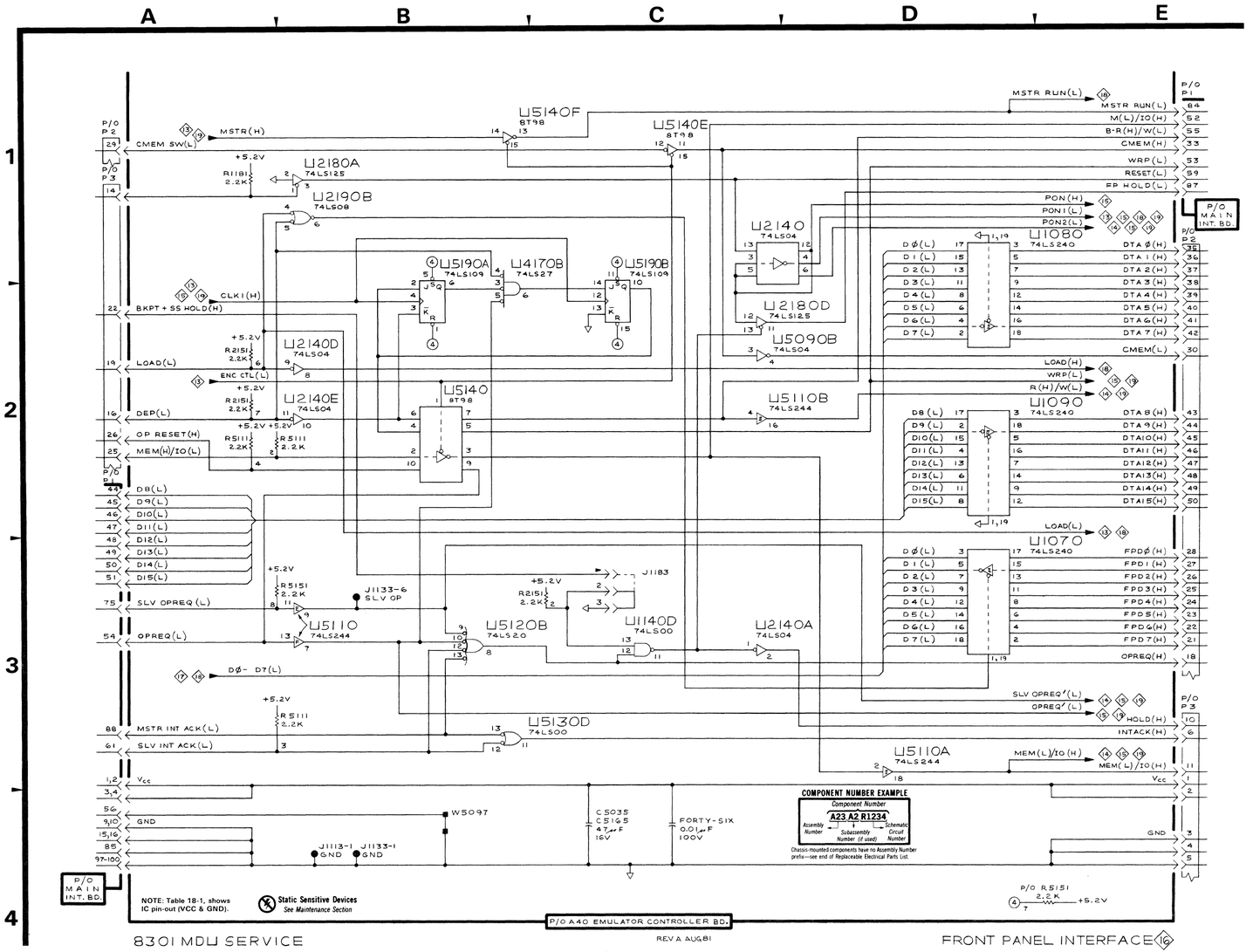
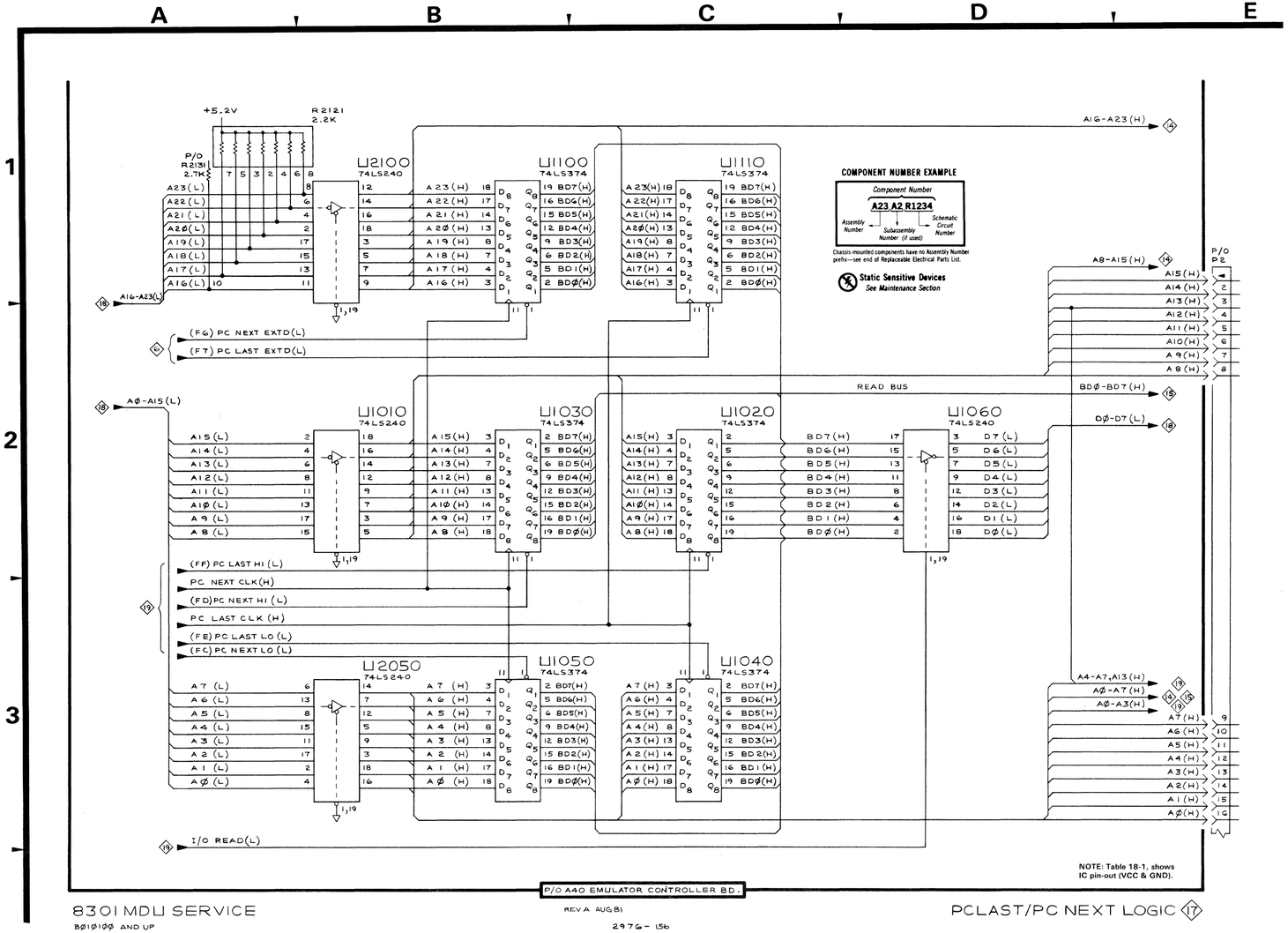


Table 18-18
PC Last/PC Next Logic Diagram 17

ASSEMBLY A40					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P2	E2	F3	U1040	C3	E2
			U1050	B3	E3
R2121	A1	D5	U1060	D2	E3
R2131	A1	D5	U1100	B1	E4
			U1110	C1	E5
U1010	B2	E1	U2050	B3	D3
U1020	C2	E1	U2100	B1	D5
U1030	B2	E2			

Partial A40 also shown on diagrams 13, 14, 15, 16, 18 and 19.



8301 MDU SERVICE
B01010 AND UP

REV A AUG 81
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PCLAST/PC NEXT LOGIC 17

Table 18-19
Jump Address Logic Diagram 18

ASSEMBLY A40					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P1	A1	A3	U2190C	C2	D8
P1	E1	A3	U2190D	C3	D8
P2	E4	F3	U3070	B1	C3
P3	A4	F7	U3100	D2	C4
			U3110	D1	C5
R2151	D4	D6	U3160C	A3	C7
R5151	A4	B6	U3160D	A2	C7
			U4010	B2	B1
U1120A	D2	E5	U4020	B2	B1
U2060A	D2	D3	U4030	B3	B2
U2060D	D2	D3	U4040	B3	B2
U2110	D1	D5	U5020	C2	B1
U2150B	B2	D6	U5030	C3	B2
U2150C	B3	D6	U5090E	A2	B4
U2160A	B2	D7	U5100B	D2	B4
U2160B	B3	D7			
U2190A	A3	D8	W1111	E2	E5

Partial A40 also shown on diagrams 13, 14, 15, 16, 17 and 19.

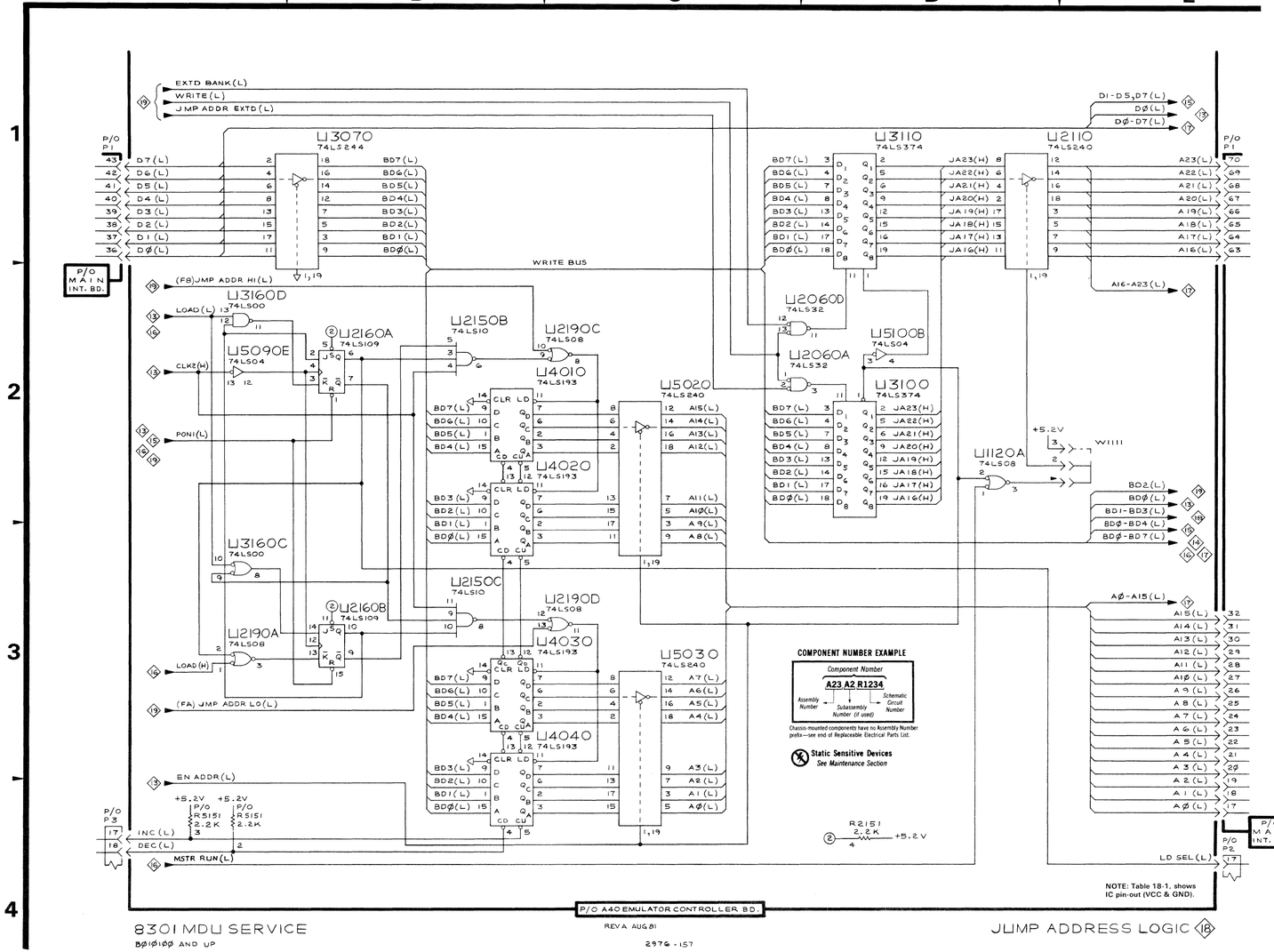
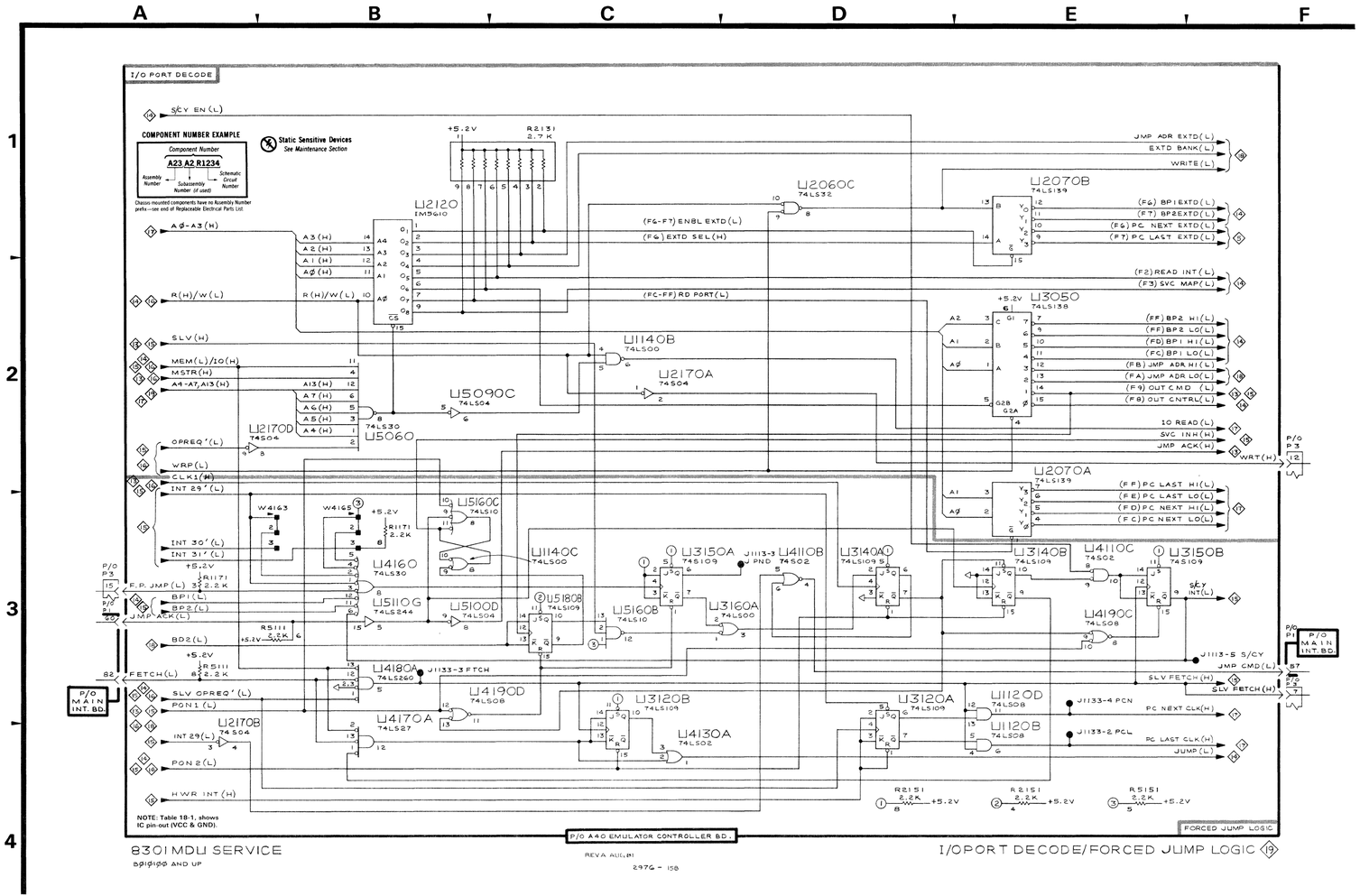
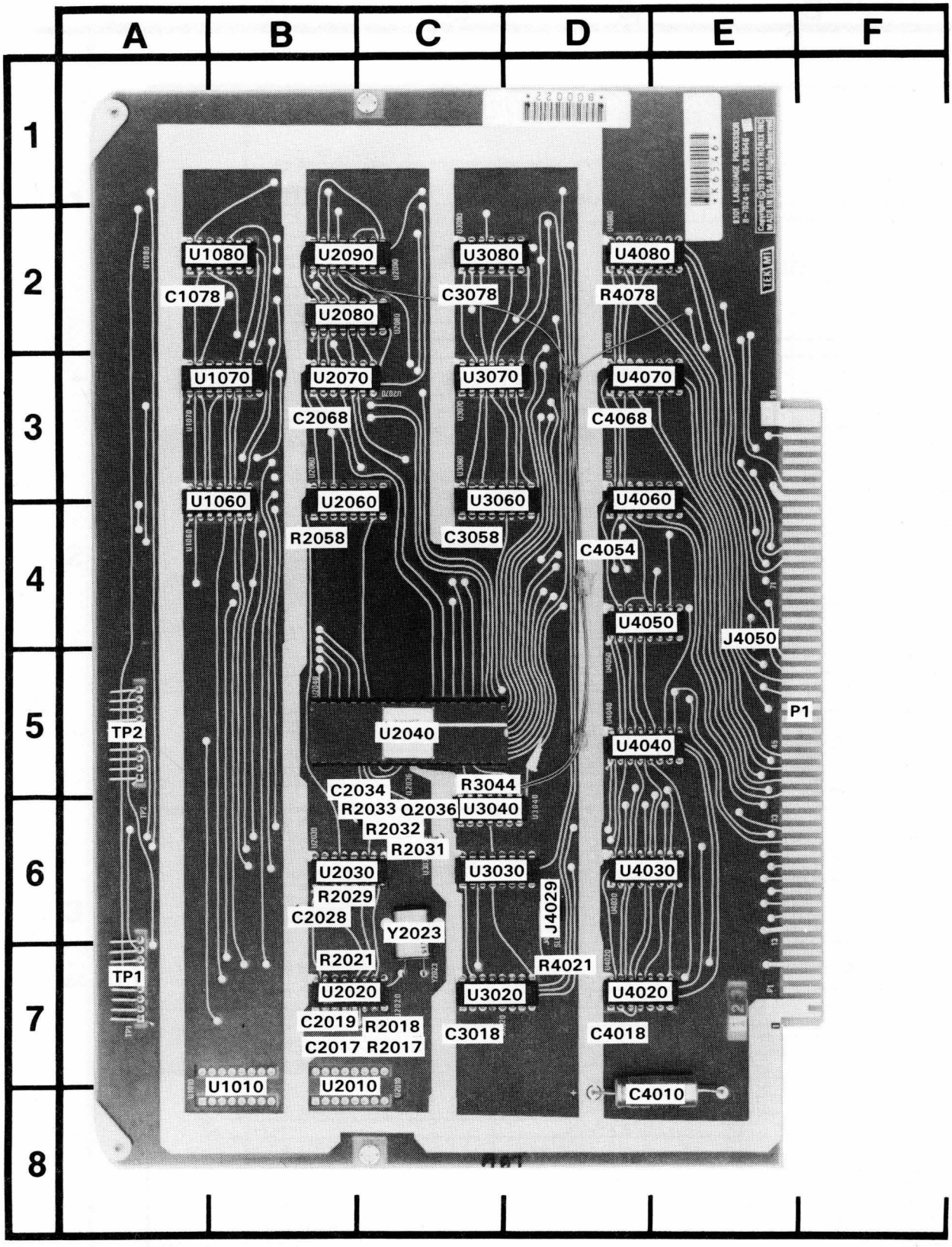


Table 18-20
I/O Port Decode/Forced Jump Logic Diagram 19

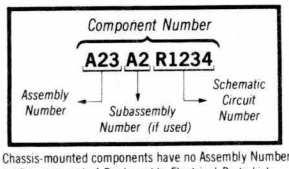
ASSEMBLY A40					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1113	D3	F5	U2170B	A4	D7
J1113	F3	F5	U2170D	A2	D7
J1133	B3	F6	U3050	E2	C3
J1133	E3	F6	U3120A	D4	C5
J1133	E4	F6	U3120B	C4	C5
			U3140A	D3	C6
P1	A3	A3	U3140B	E3	C6
P1	F3	A3	U3150A	C3	C6
P3	A3	F7	U3150B	E3	C6
P3	F3	F7	U3160A	D3	C7
			U4110B	D3	C5
R1171	A3	E7	U4110C	E3	C6
R1171	B3	E7	U4130A	C4	C6
R2131	C1	D5	U4160	B3	C7
R2151	D4	D6	U4170A	B4	C7
R2151	E4	D6	U4180A	B3	C7
R5111	A3	B5	U4190C	E3	C8
R5111	B3	B5	U4190D	B3	C8
R5151	E4	B6	U5060	B2	B3
			U5090C	B2	B4
U1120B	E4	E5	U5100D	B3	B4
U1120D	E3	E5	U5110G	B3	B5
U1140B	C2	E6	U5160B	C3	B7
U1140C	B3	E6	U5160C	B3	B7
U2060C	D1	D3	U5180B	C3	B7
U2070B	E1	D3			
U2070	E3	D3	W4163	B3	C7
U2120	B1	D5	W4165	B3	C7
U2170A	C2	D7			

Partial A40 also shown on diagrams 13, 14, 15, 16, 17 and 18.





COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 18-5. A70—Language Processor Board.

Static Sensitive Devices
See Maintenance Section

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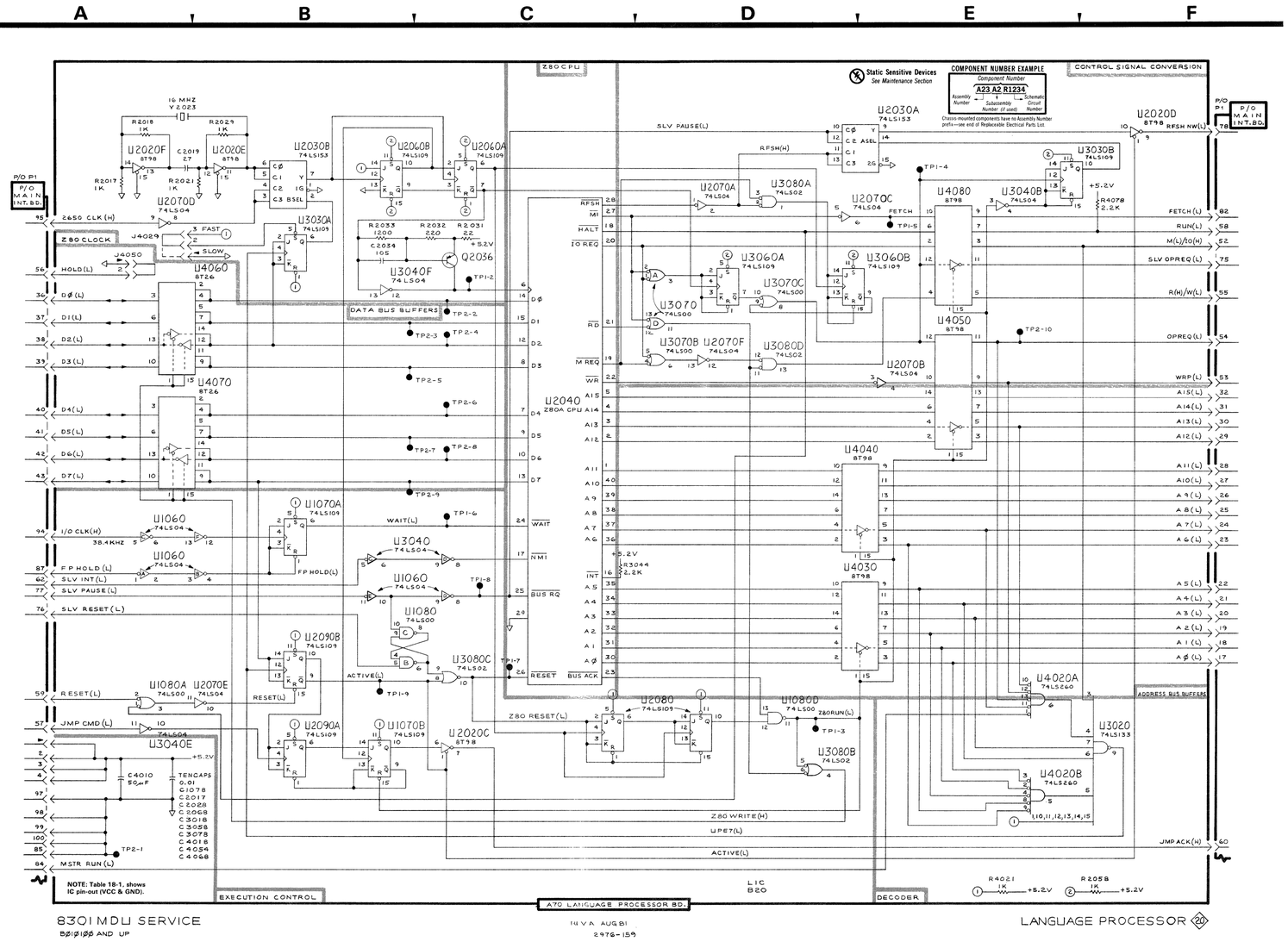
Table 18-21
Language Processor Diagram 20

ASSEMBLY A70

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1078	A4	A2	TP1-5	E1	A7	U2070B	D2	B3
C2017	A4	B7	TP1-6	C3	A7	U2070C	D1	B3
C2019	A1	B7	TP1-7	C3	A7	U2070D	A1	B3
C2028	A4	B6	TP1-8	C3	A7	U2070E	B4	B3
C2034	B2	C6	TP1-9	B3	A7	U2070F	D2	B3
C2068	A4	B3	TP2-10	E2	A5	U2080A	C4	B2
C3018	A4	C7	TP2-1	A4	A5	U2080B	D4	B2
C3058	A4	C4	TP2-2	C2	A5	U2090A	B4	B2
C3078	A4	C2	TP2-3	B2	A5	U2090B	B3	B2
C4010	A4	E8	TP2-4	C2	A5	U3020	F4	D7
C4018	A4	D7	TP2-5	B2	A5	U3030A	B1	C6
C4054	A4	D4	TP2-6	C2	A5	U3030B	D1	C6
C4068	A4	D3	TP2-7	B2	A5	U3040B	D1	C6
			TP2-8	C2	A5	U3040C	B3	C6
J4029	A1	D6	TP2-9	B3	A5	U3040D	B3	C6
J4050	A2	E4				U3040E	A4	C6
			U1060A	A3	B3	U3040F	B2	C6
P1	A1	E5	U1060B	A3	B3	U3060A	D2	C4
P1	F1	E5	U1060C	A3	B3	U3060B	D2	C4
			U1060D	B3	B3	U3070A	D2	C3
Q2036	C2	C6	U1060E	B3	B3	U3070B	D2	C3
			U1060F	A3	B3	U3070C	D2	C3
R2017	A1	C7	U1070A	B3	B3	U3070D	D2	C3
R2018	A1	C7	U1070B	B4	B3	U3080A	D1	C2
R2021	A1	C7	U1080A	A4	B2	U3080B	D4	C2
R2029	B1	B6	U1080B	B3	B2	U3080C	B3	C2
R2031	C1	C6	U1080C	B3	B2	U3080D	D2	C2
R2032	C1	C6	U1080D	D4	B2	U4020A	E4	D7
R2033	B1	C6	U2020C	C4	B7	U4020B	E4	D7
R2058	F4	B4	U2020D	F1	C7	U4030	D2	D6
R3044	B3	C5	U2020E	B1	C7	U4040	D3	D5
R3044	D3	C5	U2020F	A1	C7	U4050	D2	D3
R4021	E4	D7	U2030A	D1	B6	U4060	A2	D3
R4078	F1	D2	U2030B	B1	B6	U4070	A2	D3
			U2040	C2	C5	U4080	D1	D2
TP1-2	C2	A7	U2060A	C1	B3			
TP1-3	D4	A7	U2060B	B1	B3	Y2023	A1	C6
TP1-4	E1	A7	U2070A	D1	B3			



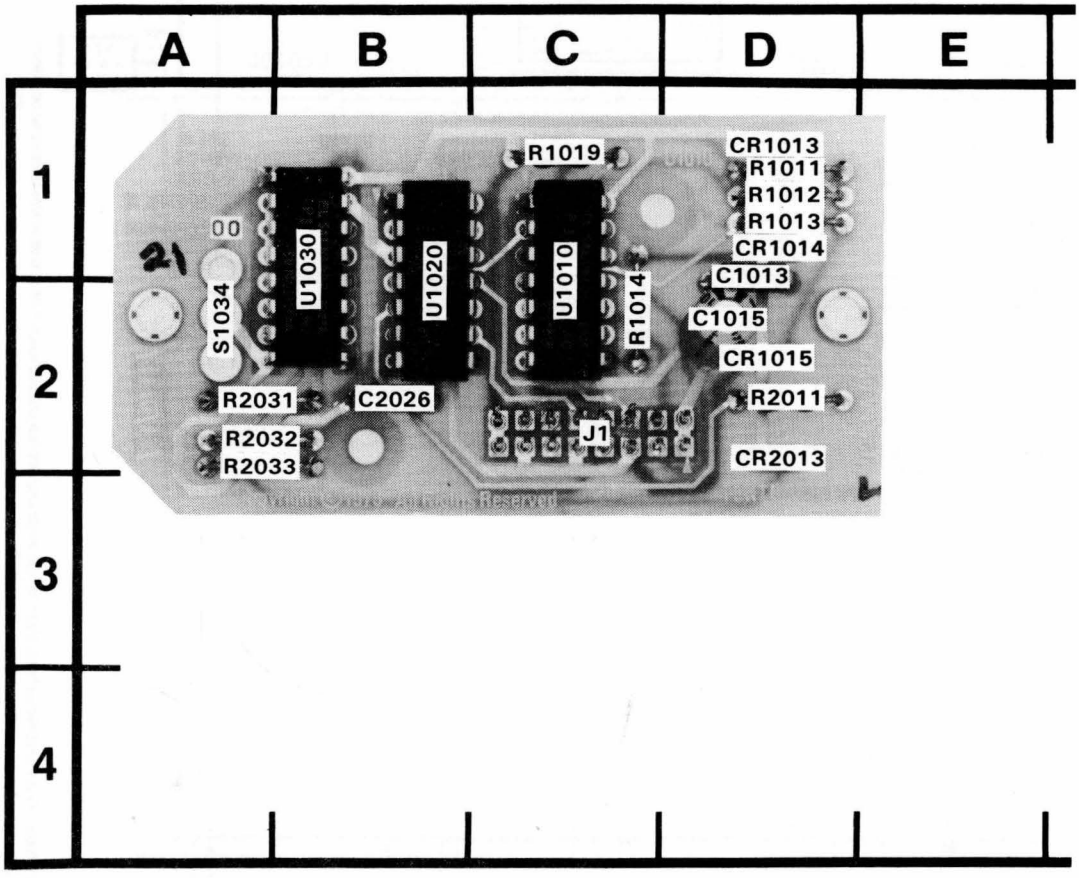
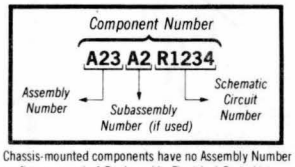


Fig. 18-6. A50—Front Panel Board.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

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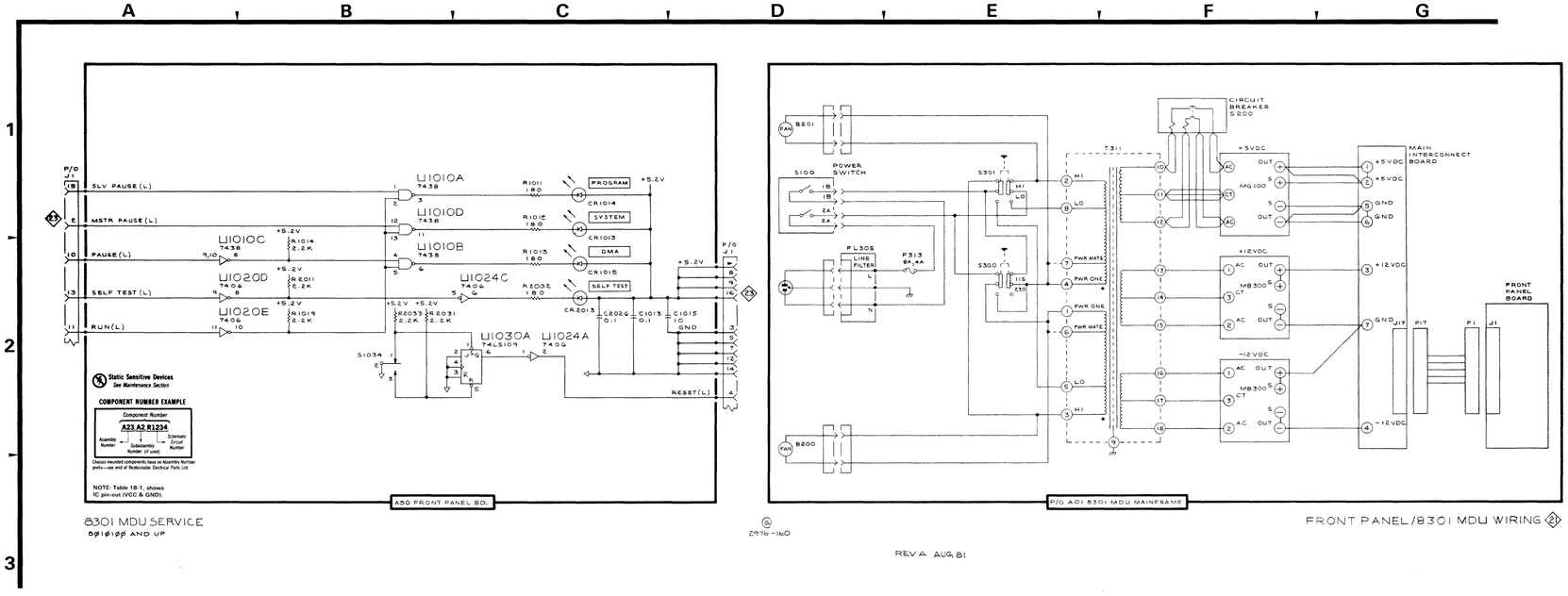
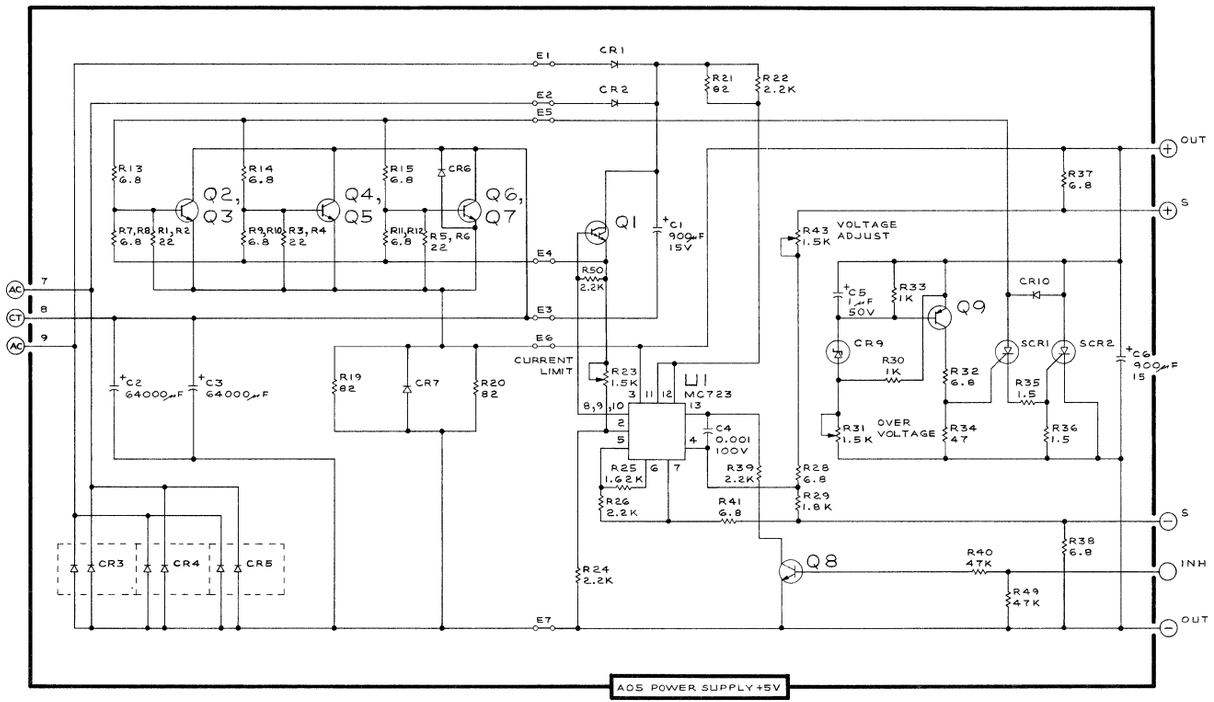
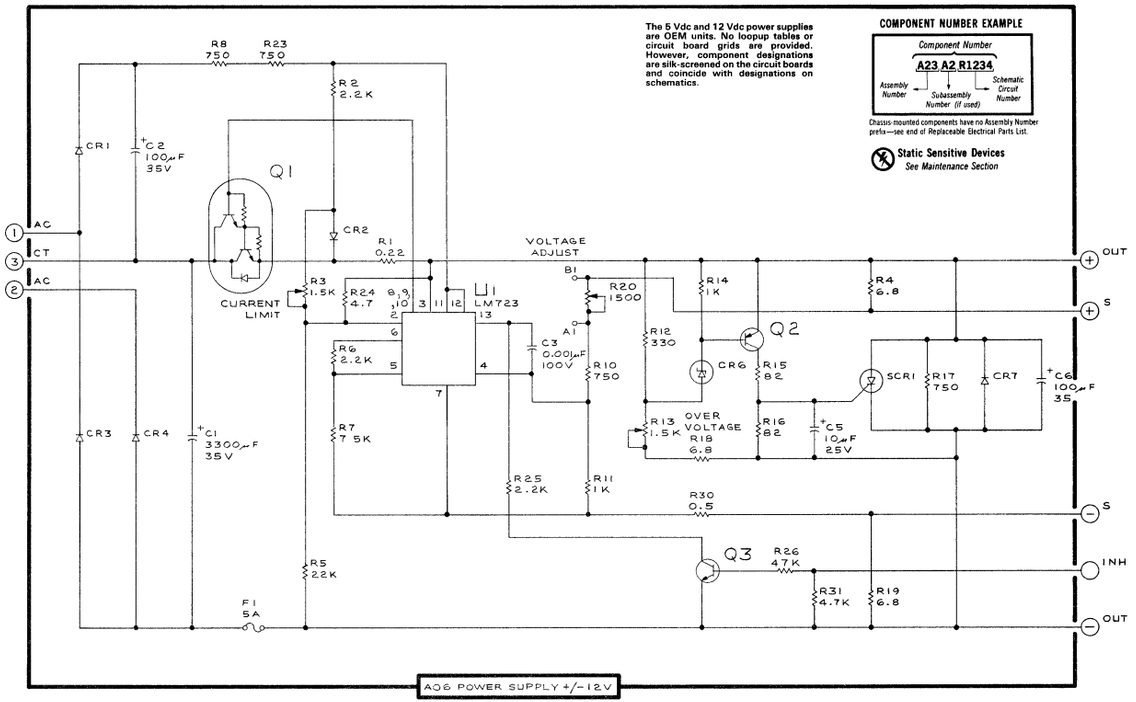
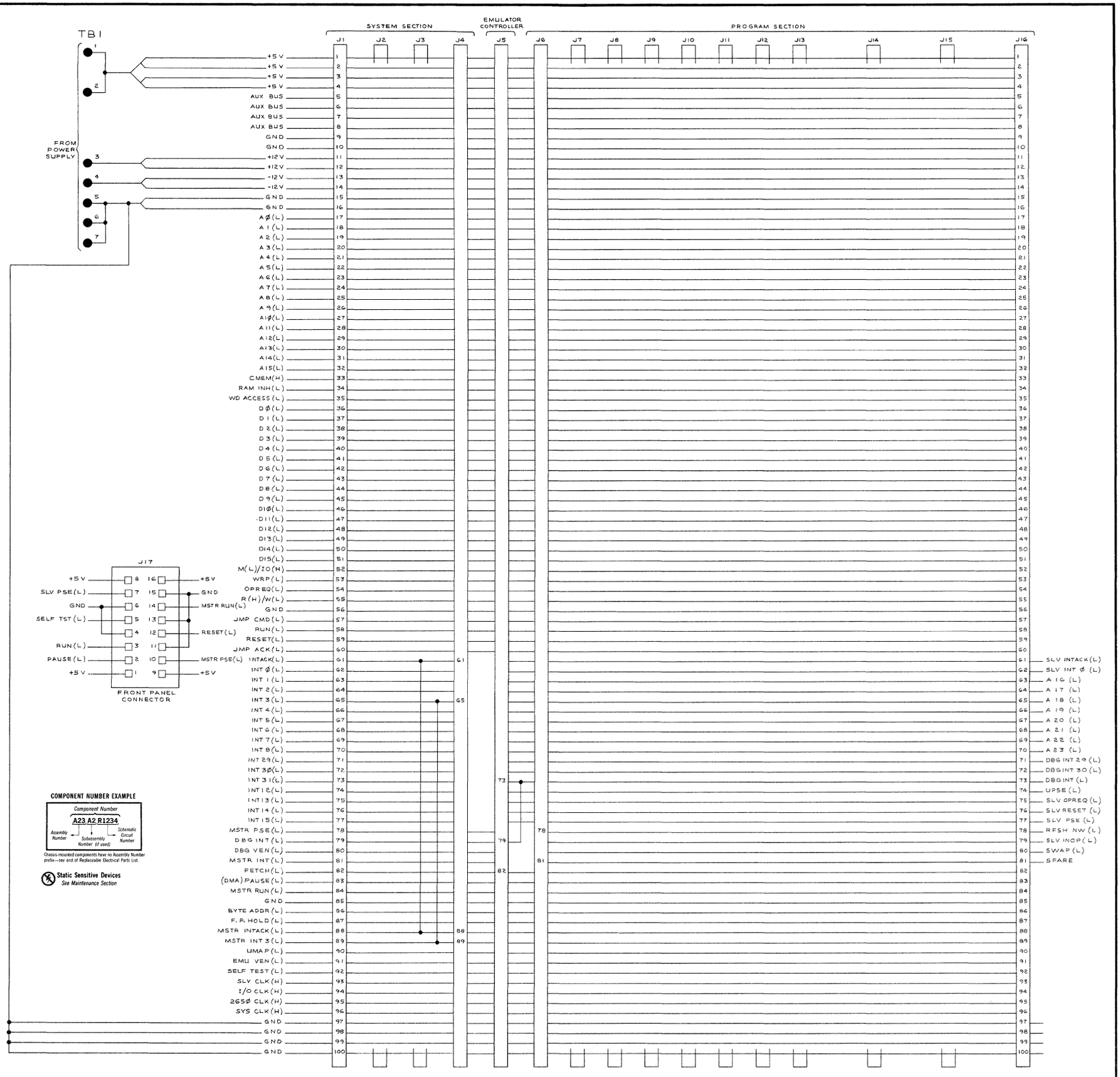
Table 18-22
Front Panel/8301 MDU Wiring Diagram 21

ASSEMBLY A50					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1013	D2	D2	R2011	B2	D2
C1015	D2	D2	R2031	B2	A2
C2026	C2	B2	R2032	C2	A2
			R2033	B2	A2
CR1013	C1	D1			
CR1014	C1	D1	S1034	B2	A2
CR1015	C2	D2			
CR2013	C2	D2	U1010A	B1	C1
			U1010B	B2	C1
J1	A1	C2	U1010C	B2	C1
J1	D2	C2	U1010D	B1	C1
			U1020A	C2	B1
R1011	C1	D1	U1020C	C2	B1
R1012	C1	D1	U1020D	B2	B1
R1013	C2	D1	U1020E	B2	B1
R1014	B2	C2	U1030A	C2	B1
R1019	B2	C1			

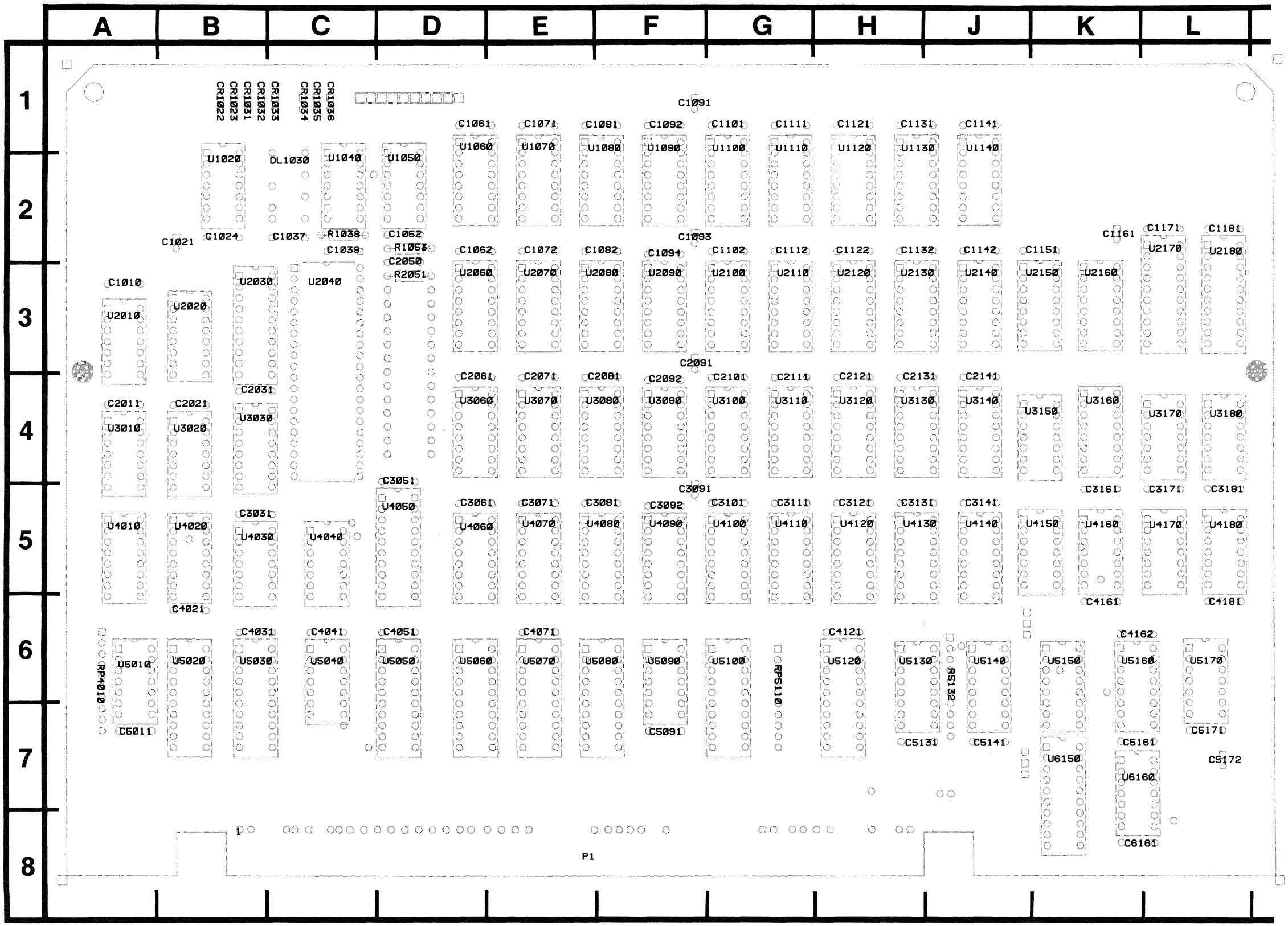



AC
CT
AC
7
8
9
E1
E2
E5
E4
E3
E6
E7
CR1
CR2
R21
82
R22
2.2K
R13
6.8
R14
6.8
R15
6.8
CR6
Q2,
Q3
Q4,
Q5
Q6,
Q7
R7,R8,R1,R2
6.8
22
R9,R10,R3,R4
6.8
22
R11,R12,R5,R6
6.8
22
Q1
+C1
900µF
15V
R50
2.2K
R43
1.5K
VOLTAGE
ADJUST
R37
6.8
OUT
S
+C5
1µF
50V
R33
1K
Q9
CR10
CR9
R30
1K
SCR1
SCR2
+C6
900µF
15
R31
1.5K
OVER
VOLTAGE
R32
6.8
R34
47
R35
1.5
R36
1.5
CURRENT
LIMIT
R23
1.5K
U1
MC723
8,9,10
3
11
12
13
2
5
4
6
7
C4
0.001
100V
R25
1.62K
R39
2.2K
R41
6.8
R26
2.2K
R28
6.8
R29
1.8K
S
INH
OUT
+C2
64000µF
+C3
64000µF
R19
82
CR7
R20
82
CR3
CR4
CR5
R24
2.2K
Q8
R40
47K
R49
47K
R38
6.8
A05 POWER SUPPLY +5V

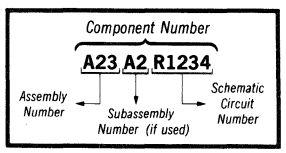

The 5 Vdc and 12 Vdc power supplies are OEM units. No loopup tables or circuit board grids are provided. However, component designations are silk-screened on the circuit boards and coincide with designations on schematics.
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
R8
750
R23
750
R2
2.2K
CR1
+C2
100µF
35V
Q1
CR2
R1
0.22
1
AC
3
CT
2
AC
CURRENT
LIMIT
VOLTAGE
ADJUST
B1
A1
R3
1.5K
R24
4.7
8,9,10
3
11
12
U1
LM723
13
2
6
5
4
7
R6
2.2K
R7
7.5K
R20
1500
R10
750
C3
0.001µF
100V
R12
330
R14
1K
R4
6.8
Q2
CR6
R15
82
SCR1
R17
750
CR7
+C6
100µF
35
OUT
S
R13
1.5K
OVER
VOLTAGE
R18
6.8
R16
82
+C5
10µF
25V
R25
2.2K
R11
1K
R30
0.5
S
INH
OUT
CR3
CR4
+C1
3300µF
35V
R5
2.2K
Q3
R26
4.7K
R31
4.7K
R19
6.8
F1
5A
A06 POWER SUPPLY +/-12V



A60 MAIN INTERCONNECT BD.



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Fig. 18-7. A80—System RAM Board.

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Static Sensitive Devices
See Maintenance Section

I/O PORTS

RES(L)
WRP(H)
R(L)/W(H)
MSTR RUN(H)
NBA13(H)
OP(H)
MEM(H)
A5(H)
A3(H)
A2(H)
A7(H)
A6(H)
A4(H)
A1(H)
A0(H)
D0(H) - D7(H)
A0(H) - A15(H)

U4160F 74LS04
U3170C 74LS32
U3170B 74LS32
U3160A 74LS139
U4040B 74LS260
U4030 74LS30
U4050 74LS273

PAGE(L)
CR1023 CR1032 CR1034 CR1036
CR1022 CR1031 CR1033 CR1035
+5V

D7(H) D6(H) D5(H) D4(H) D3(H) D2(H) D1(H) D0(H)
CL D4 D3 D5 D2 D6 D1 D7 D0 Q4 Q3 Q5 Q2 Q6 Q1 Q7 Q0

PRTY CMPLT(H)
PRTY INH(L)
REF. INT. ENABLE(H)

U4170A 74LS00
DATARD(L)
PRTY CLR(L)

OP DELAYED

P/O P1
I/O CLK
RUN(L)
PAUSE(L)
MSTR PAUSE(L)
FP HOLD(L)

U4180F 74LS14
U6150G 74LS244
U6160B 74LS27
U6160C 74LS27
U6150F 74LS244
U6150C 74LS244
U6150D 74LS244
U4160C 74LS04

RP5110-6 10K
RP5132-8 2.7K
U5130B 74LS109
RP5132-4 2.7K
RP5132-7 2.7K
U5150A 74LS109
U5170B 74LS10
RP5132-3 2.7K
RP5132-10 2.7K
U5140B 74LS109
RP5132-2 2.7K
RP5132-5 2.7K
U5130A 74LS109
U3180C 74S03

U5070 74LS374
U5080 74LS374
OUT CONT
A15(H) A14(H) A13(H) A12(H) A11(H) A10(H) A9(H) A8(H)
A7(H) A6(H) A5(H) A4(H) A3(H) A2(H) A1(H) A0(H)
1D 8D 7D 2D 3D 6D 5D 4D 1Q 8Q 7Q 2Q 3Q 6Q 5Q 4Q
DB7(H) DB6(H) DB5(H) DB4(H) DB3(H) DB2(H) DB1(H) DB0(H)

DB0(H) - DB7(H)
REF(H)
INT 15(H)
P/O P1 77

TP1049
TP1051
REFN(H)
PRTY LTCH

RP4010-7 2.7K U5010E 74LS04
RP4010-9 2.7K U5010D 74LS04
RP4010-6 2.7K U5010B 74LS04

P/O MAIN INT.BD.

COMPONENT NUMBER EXAMPLE

Component Number: A23,A2 R1234
Assembly Number; Subassembly Number (if used); Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

REFRESH CONTROL

P/O A80 SYSTEM RAM BOARD

NOTE: Table 18-1, shows IC pin-out (VCC & GND).

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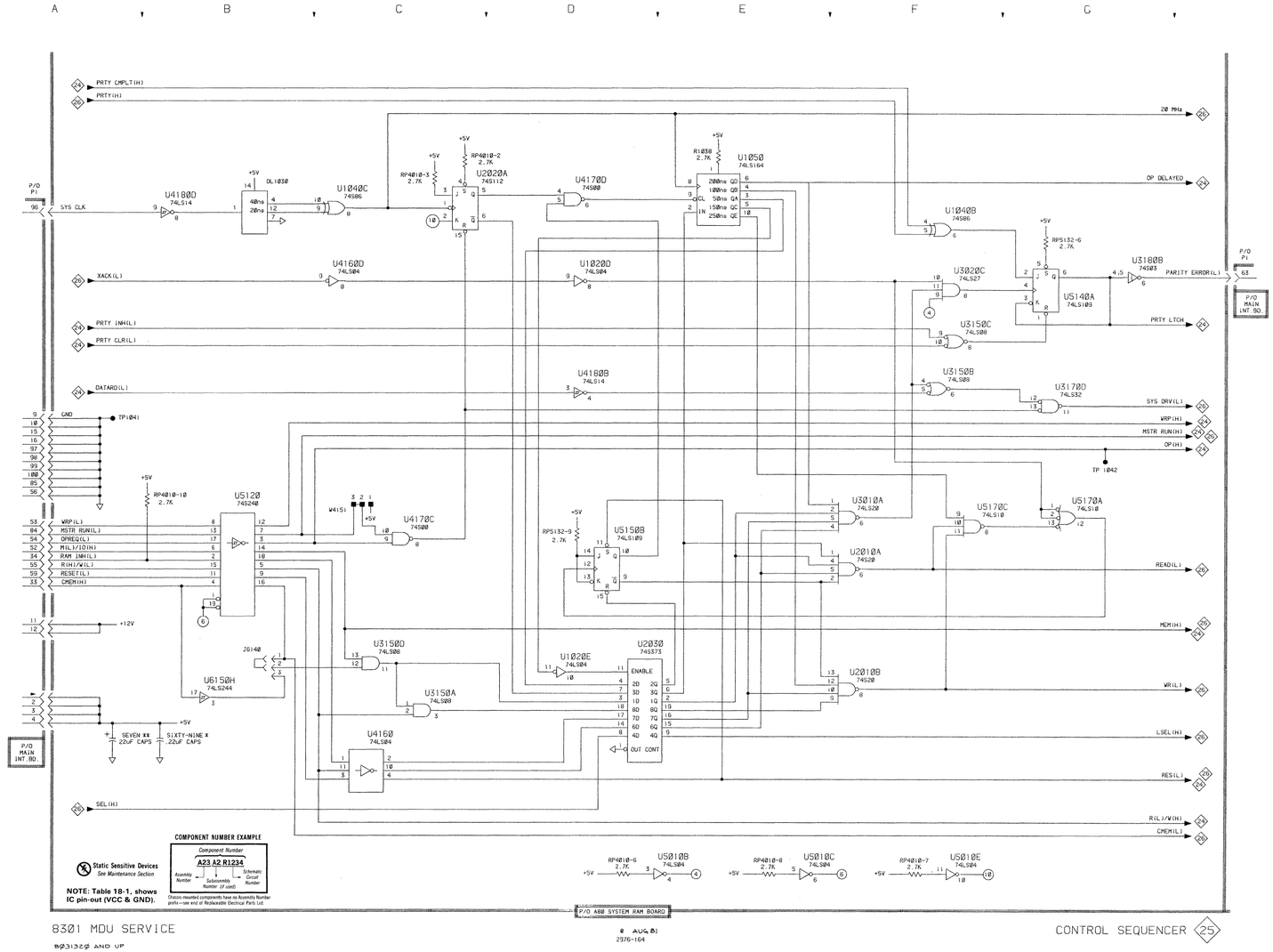
Table 18-23

Sixty-Nine .22 μF*			
C1061	C1102	C2101	C3171
C1071	C1112	C2111	C3181
C1081	C1122	C2121	C4161
C1092	C1132	C2131	C4181
C1101	C1142	C2141	C4021
C1111	C1151	C3031	C4031
C1121	C1171	C3051	C4041
C1131	C1181	C3061	C4051
C1141	C1010	C3071	C4071
C1024	C2050	C3081	C4121
C1037	C2011	C3092	C4162
C1039	C2021	C3101	C5011
C1052	C2031	C3111	C5091
C1062	C2061	C3121	C5131
C1072	C2071	C3131	C5141
C1082	C2081	C3141	C5161
C1094	C2092	C3161	C5171
			C6161

Table 18-24

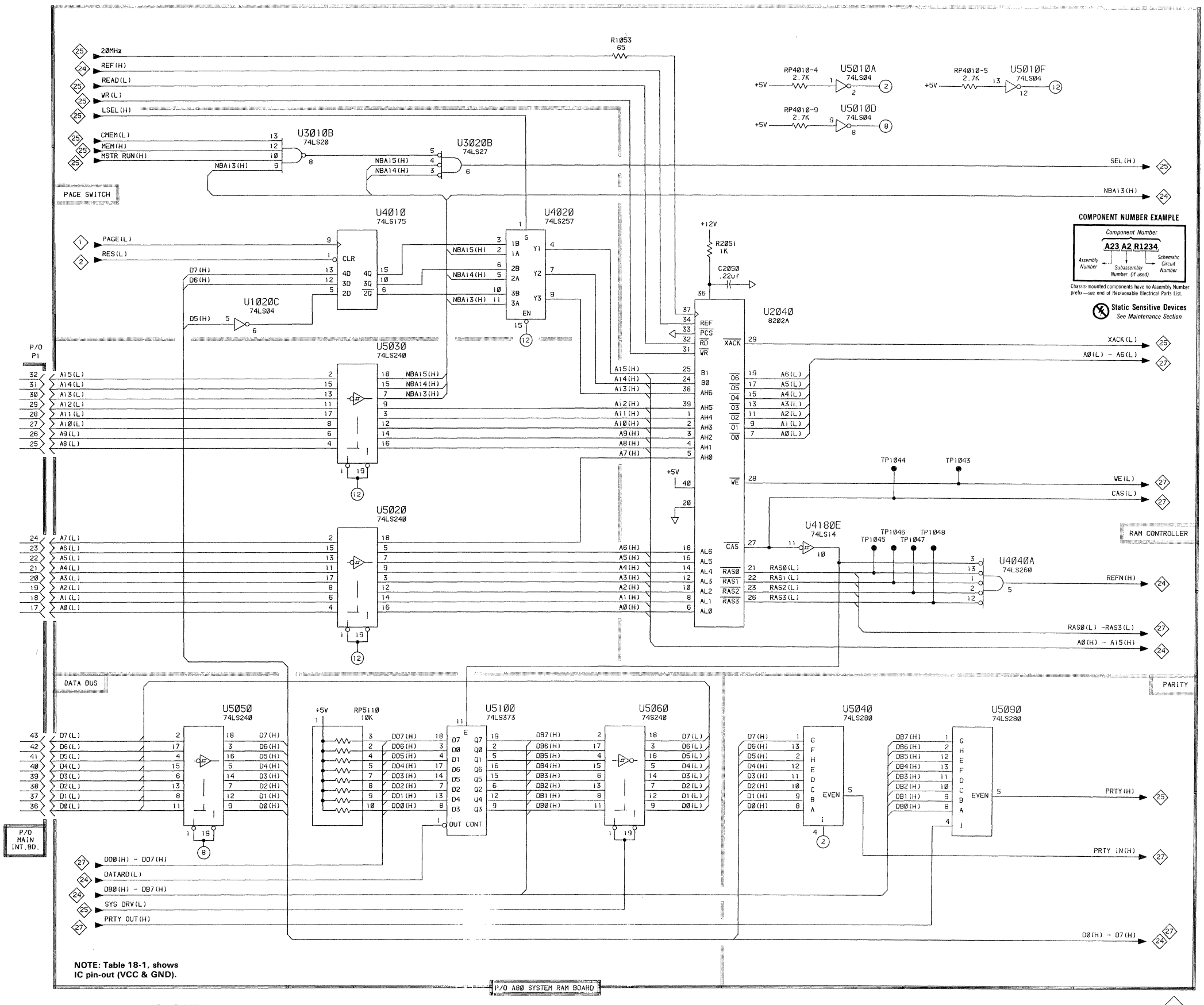
Seven 22 μF**
C1021
C1091
C1093
C2091
C3091
C5172
C1161



8301 MDU SERVICE

B030130 AND UP

CONTROL SEQUENCER 25


20MHz
REF(H)
READ(L)
WR(L)
LSEL(H)
CMEM(L)
MEM(H)
MSTR RUN(H)
NBAi3(H)
U3010B
74LS20
U3020B
74LS27
NBAi5(H)
NBAi4(H)
SEL(H)
NBAi3(H)
PAGE SWITCH
PAGE(L)
RES(L)
U4010
74LS175
U4020
74LS257
D7(H)
D6(H)
D5(H)
U1020C
74LS04
R1053
65
RP4010-4
2.7K
U5010A
74LS04
RP4010-5
U5010F
RP4010-9
U5010D
+5V
+12V
R2051
1K
C2050
.22uf
U2040
8202A
COMPONENT NUMBER EXAMPLE
Component Number
A23,A2,R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
XACK(L)
A0(L) - A6(L)
P/O P1
U5030
74LS240
U5020
74LS240
Ai5(L)
Ai4(L)
Ai3(L)
Ai2(L)
Ai1(L)
Ai0(L)
A9(L)
A8(L)
A7(L)
A6(L)
A5(L)
A4(L)
A3(L)
A2(L)
A1(L)
A0(L)
TP1044
TP1043
WE(L)
CAS(L)
U4180E
74LS14
TP1045
TP1046
TP1047
TP1048
U4040A
74LS260
RAM CONTROLLER
REFN(H)
RAS0(L) -RAS3(L)
A0(H) - A15(H)
DATA BUS
PARITY
U5050
74LS240
RP5110
10K
U5100
74LS373
U5060
74S240
U5040
74LS280
U5090
74LS280
D7(L)
D6(L)
D5(L)
D4(L)
D3(L)
D2(L)
D1(L)
D0(L)
DO7(H)
DO6(H)
DO5(H)
DO4(H)
DO3(H)
DO2(H)
DO1(H)
DO0(H)
DB7(H)
DB6(H)
DB5(H)
DB4(H)
DB3(H)
DB2(H)
DB1(H)
DB0(H)
PRTY(H)
PRTY IN(H)
D0(H) - D7(H)
P/O MAIN INT.BD.
DO0(H) - DO7(H)
DATARD(L)
DB0(H) - DB7(H)
SYS DRV(L)
PRTY OUT(H)
NOTE: Table 18-1, shows IC pin-out (VCC & GND).
P/O A80 SYSTEM RAM BOARD

PARITY RAM | BANK Ø | BANK 1 | BANK 2 | BANK 3

PRTY OUT(H) → 26

26 DØ(H) - D7(H)

26 RASØ(L) - RAS3(L)

26 PRTY IN(H)

U1140 2118: DIN 2, RASØ(L) 4, DOUT 14
U2140 2118: DIN 2, RAS1(L) 4, DOUT 14
U3140 2118: DIN 2, RAS2(L) 4, DOUT 14
U4140 2118: DIN 2, RAS3(L) 4, DOUT 14

U1060 2118: DØ(H) 2, RASØ(L) 4, DOUT 14 DØØ(H)
U1070 2118: D1(H) 2, RASØ(H) 4, DOUT 14 DØ1(H)
U1080 2118: D2(H) 2, RASØ(L) 4, DOUT 14 DØ2(H)
U1090 2118: D3(H) 2, RASØ(H) 4, DOUT 14 DØ3(H)
U1100 2118: D4(H) 2, RASØ(L) 4, DOUT 14 DØ4(H)
U1110 2118: D5(H) 2, RASØ(L) 4, DOUT 14 DØ5(H)
U1120 2118: D6(H) 2, RASØ(L) 4, DOUT 14 DØ6(H)
U1130 2118: D7(H) 2, RASØ(L) 4, DOUT 14 DØ7(H)

U2060 2118: DØ(H) 2, RAS1(L) 4, DOUT 14 DØØ(H)
U2070 2118: D1(H) 2, RAS1(L) 4, DOUT 14 DØ1(H)
U2080 2118: D2(H) 2, RAS1(L) 4, DOUT 14 DØ2(H)
U2090 2118: D3(H) 2, RAS1(L) 4, DOUT 14 DØ3(H)
U2100 2118: D4(H) 2, RAS1(L) 4, DOUT 14 DØ4(H)
U2110 2118: D5(H) 2, RAS1(L) 4, DOUT 14 DØ5(H)
U2120 2118: D6(H) 2, RAS1(L) 4, DOUT 14 DØ6(H)
U2130 2118: D7(H) 2, RAS1(L) 4, DOUT 14 DØ7(H)

U3060 2118: DØ(H) 2, RAS2(L) 4, DOUT 14 DØØ(H)
U3070 2118: D1(H) 2, RAS2(L) 4, DOUT 14 DØ1(H)
U3080 2118: D2(H) 2, RAS2(L) 4, DOUT 14 DØ2(H)
U3090 2118: D3(H) 2, RAS2(L) 4, DOUT 14 DØ3(H)
U3100 2118: D4(H) 2, RAS2(L) 4, DOUT 14 DØ4(H)
U3110 2118: D5(H) 2, RAS2(L) 4, DOUT 14 DØ5(H)
U3120 2118: D6(H) 2, RAS2(L) 4, DOUT 14 DØ6(H)
U3130 2118: D7(H) 2, RAS2(L) 4, DOUT 14 DØ7(H)

U4060 2118: DØ(H) 2, RAS3(L) 4, DOUT 14 DØØ(H)
U4070 2118: D1(H) 2, RAS3(L) 4, DOUT 14 DØ1(H)
U4080 2118: D2(H) 2, RAS3(L) 4, DOUT 14 DØ2(H)
U4090 2118: D3(H) 2, RAS3(L) 4, DOUT 14 DØ3(H)
U4100 2118: D4(H) 2, RAS3(L) 4, DOUT 14 DØ4(H)
U4110 2118: D5(H) 2, RAS3(L) 4, DOUT 14 DØ5(H)
U4120 2118: D6(H) 2, RAS3(L) 4, DOUT 14 DØ6(H)
U4130 2118: D7(H) 2, RAS3(L) 4, DOUT 14 DØ7(H)

DØØ(H) - DØ7(H) → 26

NOTE: ALL 2118'S AT RIGHT HAVE CONNECTIONS OF SAMPLE SHOWN BELOW.

2118: +5V 8; D -- 2; RAS - 4; DIN DOUT 14 DO --; 16

26 CAS(L) 15
26 WE(L) 3
A6(L) 13
A5(L) 10
A4(L) 11
A3(L) 12
A2(L) 6
A1(L) 7
A0(L) 5
26 A0(L) - A6(L)

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number | Subassembly Number (if used) | Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 18-1, shows IC pin-out (VCC & GND).

P/O A8Ø SYSTEM RAM BOARD

SECTION 19

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
\- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
\- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
\- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

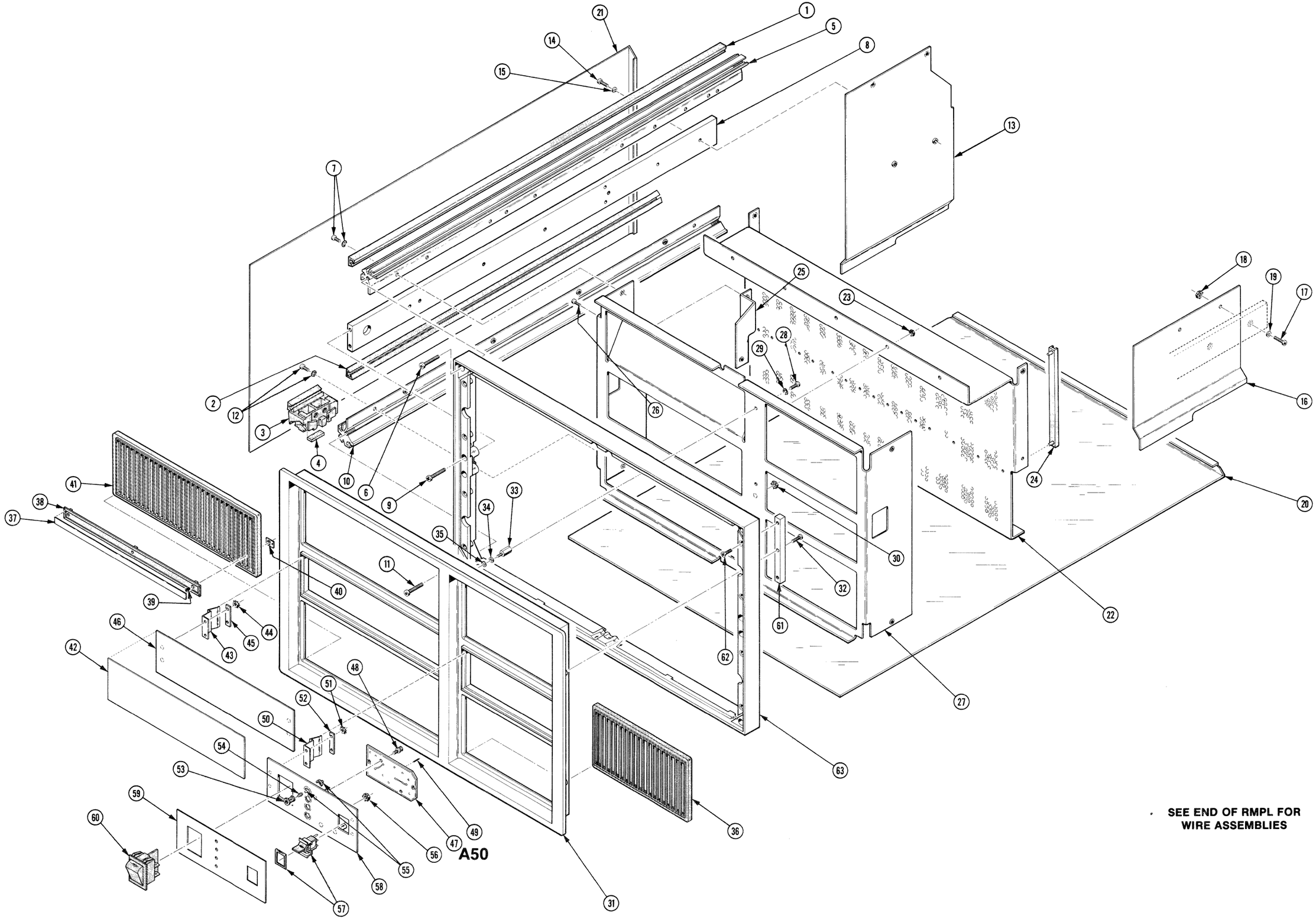
In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

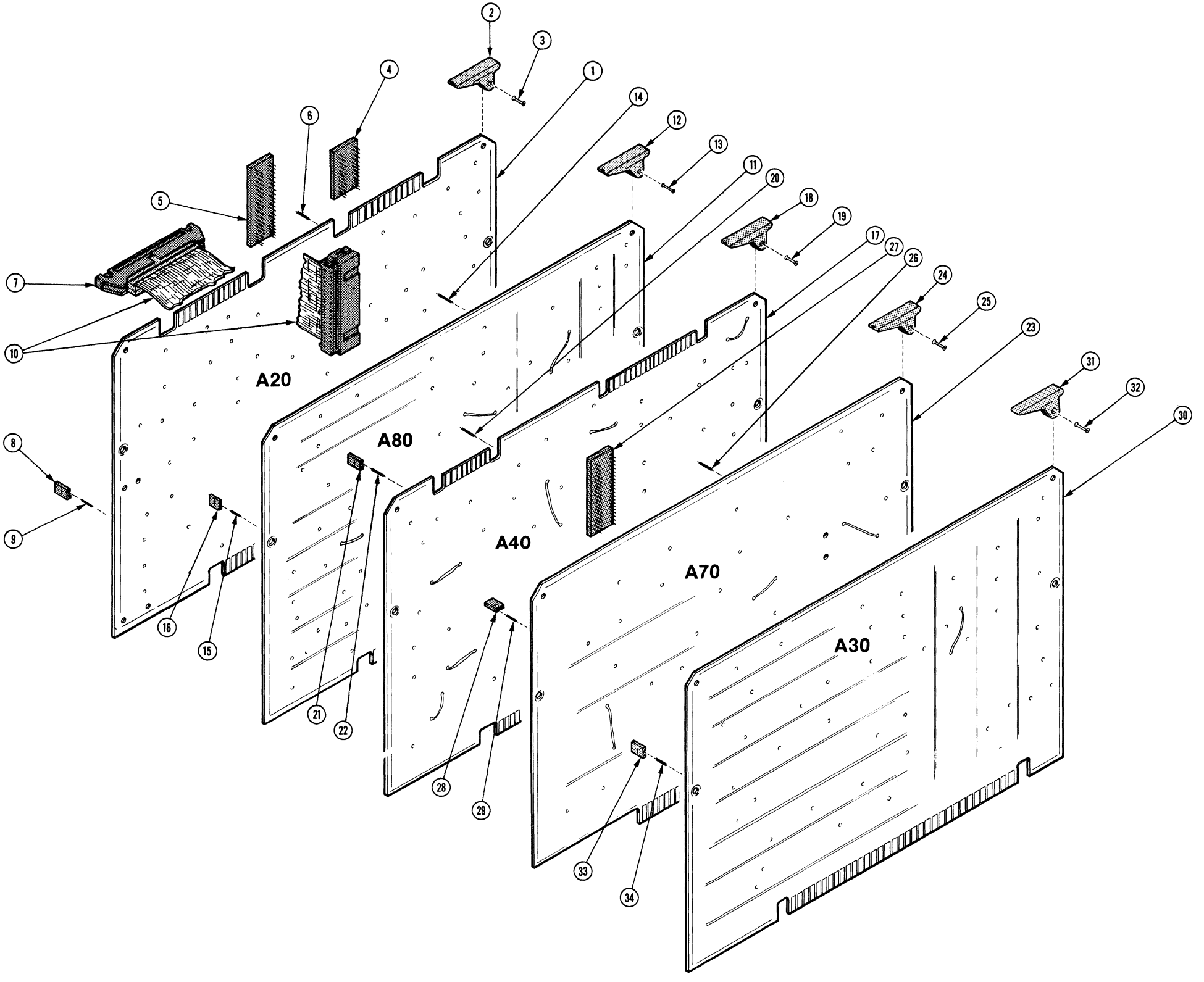
"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
S3109	C/O PANEL COMPONENTS CORP.	P.O. BOX 6626	SANTA ROSA, CA 95406
S3629	PANEL COMPONENTS CORP.	2015 SECOND ST.	BERKELEY, CA 94170
000AC	LINCOLN & ALLEN COMPANY	3460 NW INDUSTRIAL	PORTLAND, OR 97210
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
05574	VIKING INDUSTRIES, INC.	21001 NORDHOFF STREET	CHATSWORTH, CA 91311
07111	PNEUMO DYNAMICS CORPORATION	4800 PRUDENTIAL TOWER	BOSTON, MA 02199
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
16428	BELDEN CORP.	P. O. BOX 1331	RICHMOND, IN 47374
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
28520	HEYMAN MFG. CO.	147 N. MICHIGAN AVE.	KENILWORTH, NJ 07033
53387	MINNESOTA MINING AND MFG. CO., ELECTRO PRODUCTS DIVISION	3M CENTER	ST. PAUL, MN 55101
66821	SCOVILL INC. SECURITY PRODUCTS DIV.	OLD CHARLOTTE HWY. PO BOX 2588	CHARLOTTE, NC 28212
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
75037	MINNESOTA MINING & MFG CO. ELECTRO PRODUCTS DIV.	3M CENTER	ST. PAUL, MN 55101
77339	NATIONAL LOCK WASHER COMPANY	P O BOX 5115,INDUSTRIAL PARKWAY	NORTH BRANCH, NJ 08856
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80126	PACIFIC ELECTRICORD CO.	747 W. REDONDO BEACH,P O BOX 10	GARDENA, CA 90247
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
83486	ELCO INDUSTRIES, INC.	1103 SAMUELSON ROAD	ROCKFORD, IL 61101
86445	PENN FIBRE AND SPECIALTY CO., INC.	2032 E. WESTMORELAND ST.	PHILADELPHIA, PA 19134
86928	SEASTROM MFG. COMPANY, INC.	701 SONORA AVENUE	GLENDALE, CA 91201
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101



SEE END OF RMPL FOR WIRE ASSEMBLIES



SEE END OF RMPL FOR WIRE ASSEMBLIES

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	124-0367-02			2		STRIP,TRIM:CORNER,TOP,PVC,TEK TAN	80009	124-0367-02
-2	124-0366-02			2		STRIP,TRIM:CORNER,BOTTOM,PVC,TEK TAN	80009	124-0366-02
-3	348-0617-02			4		FOOT,CABINET:BOT,TEK TAN,POLYCARBONATE	80009	348-0617-02
-4	348-0596-00			4		PAD,CAB.FOOT:0.69 X 0.255 X 0.06,PU	80009	348-0596-00
-5	426-1725-00			2		FRAME SECT,CAB.:TOP CORNER	80009	426-1725-00
						(ATTACHING PARTS)		
-6	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE,FILH	93907	OBD
-7	211-0534-00			6		SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-8	426-1726-00			2		FRAME SECT,CAB.:CENTER	80009	426-1726-00
						(ATTACHING PARTS)		
-9	212-0091-00			4		SCREW,MACHINE:8-32 X 0.625",FILH STL,CD PL	93907	OBD
	211-0510-00			5		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
	210-0006-00			5		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
						- - - * - - -		
-10	426-1724-00			2		FRAME SECT,CAB.:BOTTOM CORNER	80009	426-1724-00
						(ATTACHING PARTS)		
-11	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE,FILH	93907	OBD
-12	211-0534-00			6		SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-13	386-4395-00			1		PLATE,SIDE:ALUMINUM	80009	386-4395-00
						(ATTACHING PARTS)		
-14	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
-15	210-0006-00			2		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
						- - - * - - -		
-16	386-4411-00			1		PLATE,SIDE:ALUMINUM	80009	386-4411-00
						(ATTACHING PARTS)		
-17	211-0511-00			2		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
-18	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
-19	210-0006-00			2		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
						- - - * - - -		
-20	390-0749-02			1		CABINET BOTTOM:TEK TAN	80009	390-0749-02
	390-0752-02			1		CABINET TOP:TEK TAN	80009	390-0752-02
-21	390-0750-02			2		CABINET SIDE:TEK TAN	80009	390-0750-02
-22	386-4401-00			1		PANEL,CKT BD DG:FRONT	80009	386-4401-00
						(ATTACHING PARTS)		
-23	210-0586-00			5		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
	----- -----			-		PANEL,CKT BD CG INCLUDES:		
-24	351-0087-00			16		. GUIDE,CKT BOARD:4.75 INCH LONG,PLASTIC	80009	351-0087-00
-25	407-2581-00			1		BRKT,PROM PROGR:ALUMINUM	80009	407-2581-00
						(ATTACHING PARTS)		
-26	211-0614-00			2		SCR,ASSEM WSHR:6-32 X 0.250 PNH,STL CD PL	83385	OBD
						- - - * - - -		
-27	386-4397-00			1		SUBPANEL,FRONT:	80009	386-4397-00
						(ATTACHING PARTS)		
-28	211-0510-00			3		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
-29	210-0006-00			3		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
-30	210-0457-00			3		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-31	101-0064-00			1		TRIM,DECORATIVE:FACADE	80009	101-0064-00
						(ATTACHING PARTS)		
-32	211-0511-00			4		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-33	129-0851-00			3		SPACER,POST:0.709 L W/6-32 INT THD	80009	129-0851-00
-34	210-0802-00			3		WASHER,FLAT:0.15 ID X 0.312 INCH OD	12327	OBD
-35	210-0006-00			3		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
-36	378-0149-00			2		GRILL,PLASTIC:5.62 L X 3.12W	80009	378-0149-00
-37	334-3837-00			1		PLATE,IDENT:MKD TEKTRONIXMICROPROC	80009	334-3837-00
-38	352-0586-00			1		HOLDER,IDENT,PL:ABS,TV GRAY	80009	352-0586-00
						(ATTACHING PARTS)		
-39	211-0025-00			3		SCREW,MACHINE:4-40 X 0.375 100 DEG,FLH STL	83385	OBD
-40	220-0767-00			3		NUT,SHEET SPR:4-36 X 0.38 X0.25,SST	66821	C 7000
						- - - * - - -		
-41	378-2046-00			2		GRILLE,PLASTIC:FRONT	80009	378-2046-00
-42	333-2660-00			1		PANEL,FRONT:BLANK	80009	333-2660-00

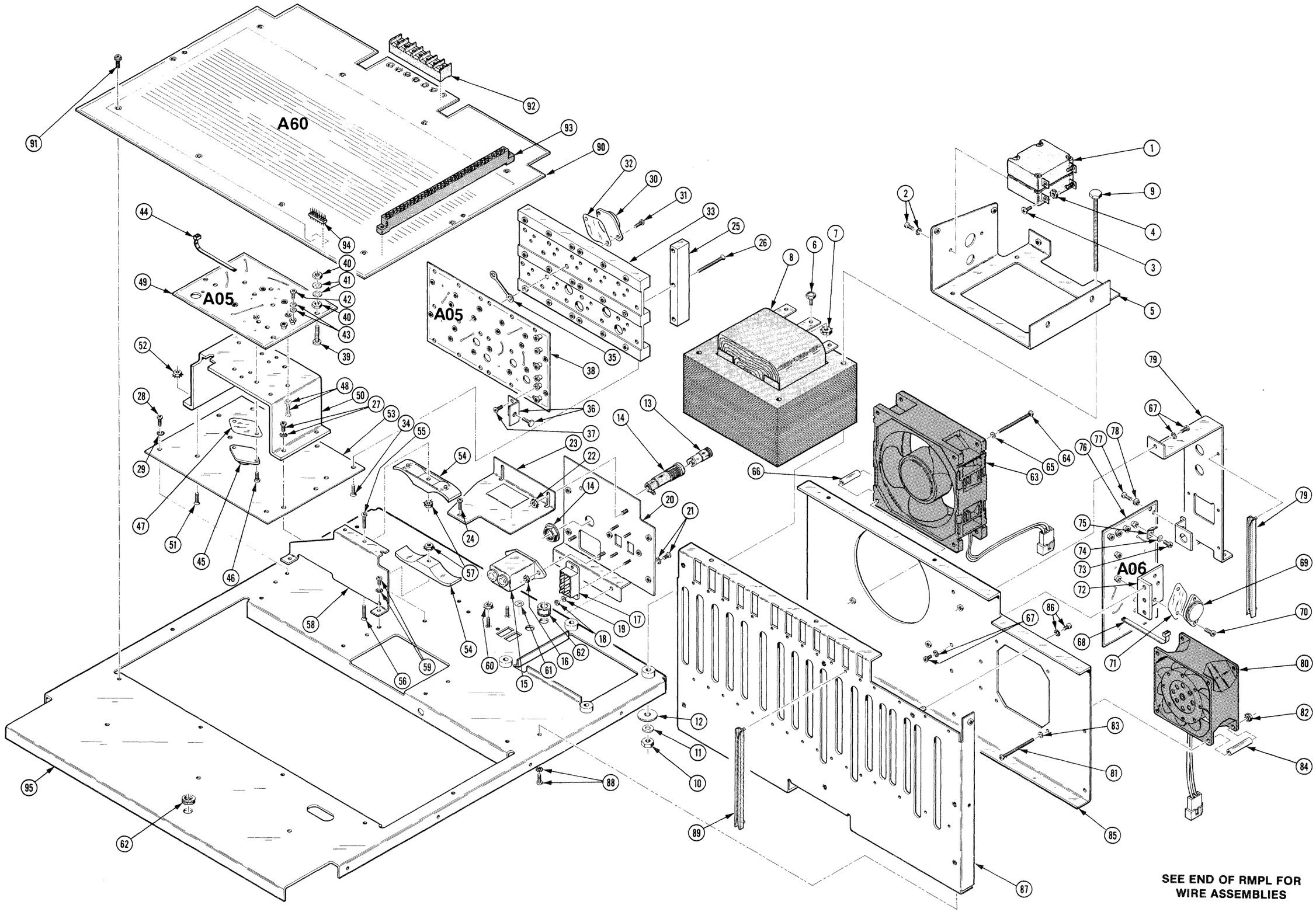
Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-43	214-2964-00			2		SPRING,PANEL:COPPER-BERYLLIUM	80009	214-2964-00
						(ATTACHING PARTS)		
-44	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-45	343-0831-00			2		RETAINER,SPR:ALUMINUM	80009	343-0831-00
						- - - * - - -		
-46	333-2659-00			1		PANEL,FRONT:BLANK	80009	333-2659-00
	672-0884-00			1		CKT BOARD ASSY:FRONT PANEL	80009	672-0884-00
-47	----- -----			1		. CKT BOARD ASSY:FRONT PANEL(SEE A50 REPL)		
						(ATTACHING PARTS)		
-48	211-0116-00			2		. SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-49	----- -----			16		. . TERMINAL,PIN:(SEE A50J1 REPL)		
-50	214-2964-00			2		. SPRING,PANEL:COPPER-BERYLLIUM	80009	214-2964-00
						(ATTACHING PARTS)		
-51	210-0586-00			4		. NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-52	343-0831-00			2		. RETAINER,SPR:ALUMINUM	80009	343-0831-00
						- - - * - - -		
-53	352-0157-00			4		. LAMPHOLDER:WHITE PLASTIC	80009	352-0157-00
-54	378-0602-01			4		. LENS,LIGHT:AMBER	80009	378-0602-01
-55	----- -----			4		. LT EMITTING DIO:(SEE A50CR1013,1014,1015 AND		
	----- -----			-		. A50CR2013 REPL)		
-56	210-0458-00			1		. NUT,PL,ASSEM WA:8-32 X 0.344 INCH,STL	83385	OBD
-57	----- -----			1		. SWITCH,TOGGLE:(SEE A50S110 REPL)		
-58	386-4396-00			1		. SUBPANEL,FRONT:	80009	386-4396-00
-59	333-2643-00			1		. PANEL,FRONT:CONTROL	80009	333-2643-00
-60	----- -----			1		. SWITCH,ROCKER:(SEE A50S100 REPL)		
-61	220-0884-00			4		NUT,BAR:0.312 SQ X 3.234 L	80009	220-0884-00
						(ATTACHING PARTS)		
-62	211-0512-00			8		SCREW,MACHINE:6-32 X 0.50" 100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-63	426-1624-02			1		FRAME,CABINET:OPEN FRONT	80009	426-1624-02

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-1	----- -----			1		CKT BOARD ASSY:SYSTEM CONTROLLER(SEE A20 REPL)		
-2	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-3	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-4	136-0578-00			2		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-5	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-6	----- -----			11		. TERM,PIN:(SEE A20J1080 REPL)		
-7	131-2597-00			1		. CONN,RCPT,ELEC:HEADER,2X20,RT ANGLE	53387	3432-120-Z
	131-2405-00			1		. CONN,RCPT,ELEC:CKT BD,2 X 25MALE	75037	3433-1202
-8	131-0993-00			3		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-9	----- -----			18		. TERMINAL,PIN:(SEE A20J1051,J2804,J3014,		
	----- -----			-		. J5704 REPL)		
-10	----- -----			1		(SEE WIRE ASSEMBLIES PARTS LIST FOR PART NUMBER)		
-11	----- -----			1		CKT BOARD ASSY:SYSTEM RAM(SEE A80 REPL)		
-12	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-13	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-14	131-0589-00			10		. TERMINAL,PIN:0.46 L X 0.025 SQ	22526	47350
-15	----- -----			3		. TERM,PIN:(SEE A80J6140 REPL)		
-16	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-17	----- -----			1		CKT BOARD ASSY:EMULATOR CONTROLLER(SEE A40 REPL)		
-18	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-19	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-20	----- -----			27		. TERM,PIN:(SEE A40J1093,J1113,J1133 REPL)		
-21	131-0993-00			5		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-22	----- -----			17		. TERMINAL,PIN:(SEE A40J1183,J3073,J4083,J4093,		
	----- -----			-		. J5097,J5177 REPL)		
-23	----- -----			1		CKT BOARD ASSY:LANGUAGE PROCESSOR(SEE A70 REPL)		
-24	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-25	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-26	----- -----			19		. TERM,PIN:(SEE A70TP1,TP2 REPL)		
-27	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-28	131-0993-00			2		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-29	----- -----			5		. TERMINAL,PIN:(SEE A70J4029,J4050 REPL)		
-30	----- -----			1		CKT BOARD ASSY:SYSTEM/PROGRAM MEM(SEE A30 REPL)		
-31	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-32	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-33	131-0993-00			5		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-34	----- -----			15		. TERMINAL,PIN:(SEE A30J5011,J5175,J6175,		
	----- -----			-		. J6179,J7171 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-1	----- -----			1		CIRCUIT BREAKER:(SEE S200 REPL)		
						(ATTACHING PARTS)		
-2	211-0614-00			2		SCR,ASSEM WSHR:6-32 X 0.250 PNH,STL CD PL	83385	OBD
						- - - * - - -		
-3	211-0614-00			2		SCR,ASSEM WSHR:6-32 X 0.250 PNH,STL CD PL	83385	OBD
-4	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
-5	407-2530-00			1		BRACKET,CMPNT:TRANSFORMER	80009	407-2530-00
-6	212-0099-00			3		SCREW,MACHINE:8-32 X 0.5 HEX HD,STL	83486	OBD
-7	210-0457-00			3		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
-8	----- -----			1		TRANSFORMER:(SEE T311 REPL)		
						(ATTACHING PARTS)		
-9	213-0781-00			4		SCREW,TPG,TC:4-24 X 0.312,TYPE BT,FLH	000BK	OBD
-10	210-0411-00			4		NUT,PLAIN,HEX.:0.25-20 X 0.438 INCH STL	73743	OBD
-11	210-0016-00			4		WASHER,LOCK:SPLIT,0.259 ID X 0.489 OD,STL	77339	6507
-12	210-1295-00			4		WASHER,LOCK:0.26 ID,INTL,0.025 THK STL	86928	5702-95-60-C2
						- - - * - - -		
-13	200-2264-00			1		CAP.,FUSEHOLDER:3AG FUSES	S3629	FEK 031 1666
-14	204-0822-00			1		SBSTR,METALIZED:50 OHM PER SQUARE	80009	204-0822-00
-15	----- -----			1		FILTER,RFI:(SEE FL305 REPL)		
						(ATTACHING PARTS)		
-16	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-17	----- -----			1		SWITCH,SLIDE:(SEE S301 REPL)		
						(ATTACHING PARTS)		
-18	210-0406-00			2		NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-19	210-0004-00			2		WASHER,LOCK:#4 INTL,0.015THK,STL CD PL	000BK	OBD
						- - - * - - -		
	----- -----			1		SWITCH,SLIDE:(SEE S300 REPL)		
						(ATTACHING PARTS)		
	210-0406-00			2		NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
	210-0004-00			2		WASHER,LOCK:#4 INTL,0.015THK,STL CD PL	000BK	OBD
						- - - * - - -		
-20	407-2527-00			1		BRKT,REAR PANEL:POWER,AL	80009	407-2527-00
						(ATTACHING PARTS)		
-21	211-0534-00			2		SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	OBD
-22	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-23	386-4394-00			1		PLATE,V SEL:ALUMINUM	80009	386-4394-00
						(ATTACHING PARTS)		
-24	211-0534-00			1		SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-25	361-1036-00			4		SPACER,PWR SPLY:ALUMINUM	80009	361-1036-00
						(ATTACHING PARTS)		
-26	211-0619-00			4		SCREW,MACHINE:6-32 X 1.5 INCH,FLH STL	83385	OBD
						- - - * - - -		
	----- -----			1		POWER SUPPLY:(SEE A05 REPL)		
						(ATTACHING PARTS)		
-27	211-0534-00			2		SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	OBD
-28	211-0504-00			2		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
-29	210-0006-00			2		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
						- - - * - - -		
	----- -----			-		POWER SUPPLY INCLUDES:		
-30	----- -----			9		. TRANSISTORS:(SEE A05Q1,Q2,Q3,Q4,Q5,Q6,		
	----- -----			-		. Q7,Q8,Q9 REPL)		
						(ATTACHING PARTS)		
-31	211-0511-00			18		. SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-32	386-0978-00			9		. INSULATOR,PLATE:TRANSISTOR,MICA	80009	386-0978-00
-33	118-0726-00			1		. BRACKET,HEAT SK:		
						(ATTACHING PARTS)		
-34	211-0512-00			4		. SCREW,MACHINE:6-32 X 0.50" 100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-35	118-0509-00			9		. SPACER,XSTR:PLASTIC		
-36	118-0725-00			3		. BRACKET,CONN:		
						(ATTACHING PARTS)		
-37	212-0023-00			3		. SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-38	----- -----			1		. CKT BOARD ASSY:POWER SUPPLY(SEE A05 REPL)		
	----- -----			-		. (NOT REPLACEABLE-ORDER NEXT HIGHER ASSY)		
-39	212-0507-00			4		. SCREW,MACHINE:10-32 X 0.375 INCH,PNH STL	83385	OBD
-40	210-0445-00			4		. NUT,PLAIN,HEX.:10-32 X 0.375 INCH,STL	83385	OBD
-41	210-0010-00			4		. WASHER,LOCK:INT,0.20 ID X0.376" OD,STL	78189	1210-00-00-0541C
-42	211-0511-00			2		. SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
-43	210-0006-00			4		. WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
	131-1041-00			2		. CONTACT,ELEC:QUICK DISCONNECT	00779	61060-2
-44	343-0149-00			2		. CLAMP,LOOP:NYLON	80009	343-0149-00
-45	----- -----			1		. SEMICOND DEVICE:(SEE A05SCR2 REPL)		
						(ATTACHING PARTS)		
-46	211-0511-00			2		. SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-47	386-0978-00			1		. INSULATOR,PLATE:TRANSISTOR,MICA	80009	386-0978-00
-48	212-0510-00			2		. SCREW,MACHINE:10-32 X 0.750INCH,PNH,STL	07111	OBD
-49	----- -----			1		. CKT BOARD ASSY:POWER SUPPLY(SEE A05 REPL)		
	----- -----			-		. (NOT REPLACEABLE-ORDER NEXT HIGHER ASSY)		
-50	118-0724-00			1		. BRACKET,CAP:		
						(ATTACHING PARTS)		
-51	211-0512-00			2		. SCREW,MACHINE:6-32 X 0.50" 100 DEG,FLH STL	83385	OBD
-52	210-0457-00			2		. NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-53	118-0728-00			1		. BASEPLATE,PWR S:		
-54	343-0930-00			2		RETAINER,CAP:NYLON	80009	343-0930-00
						(ATTACHING PARTS)		
-55	211-0513-00			1		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-56	211-0522-00			1		SCREW,MACHINE:6-32 X 0.625 FLH,100 DEG ST	83385	OBD
-57	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-58	407-2614-00			1		BRKT,CAP,RTNR:ALUMINUM	80009	407-2614-00
						(ATTACHING PARTS)		
-59	211-0614-00			2		SCR,ASSEM WSHR:6-32 X 0.250 PNH,STL CD PL	83385	OBD
						- - - * - - -		
-60	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
-61	334-3379-03			1		MARKER,IDENT:MARKED GROUNDSYMBOL	80009	334-3379-03
-62	348-0442-00			6		GROMMET,PLASTIC:BLACK,ROUND,0.375" ID	28520	SB-500-6
-63	----- -----			1		FAN,AXIAL:(SEE B201 REPL)		
						(ATTACHING PARTS)		
-64	211-0530-00			4		SCREW,MACHINE:6-32 X 1.75 INCH,PNH STL	83385	OBD
-65	210-0006-00			4		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
						- - - * - - -		
-66	361-1056-00			4		SPACER,SLEEVE:0.98 L X 0.18 ID	80009	361-1056-00
	----- -----			1		POWER SUPPLY:(SEE A06 REPL)		
						(ATTACHING PARTS)		
-67	211-0614-00			5		SCR,ASSEM WSHR:6-32 X 0.250 PNH,STL CD PL	83385	OBD
						- - - * - - -		
	----- -----			-		POWER SUPPLY ASSY INCLUDES:		
-68	343-0149-00			1		. CLAMP,LOOP:NYLON	80009	343-0149-00
-69	----- -----			1		. TRANSISTOR:(SEE A06Q1 REPL)		
						(ATTACHING PARTS)		
-70	211-0511-00			2		. SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-71	386-0978-00			1		. INSULATOR,PLATE:TRANSISTOR,MICA	80009	386-0978-00
-72	118-0723-00			1		. BRACKET,VAR RES:ALUMINUM		
-73	213-0203-00			4		. SCREW,MACHINE:5-40 X 0.25,PNH,STL CD PL,P	83385	OBD
-74	210-0006-00			4		. WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
-75	131-1041-00			2		. CONTACT,ELEC:QUICK DISCONNECT	00779	61060-2
-76	----- -----			1		. CKT BOARD SSY:POWER SUPPLY(SEE A06 REPL)		
	----- -----			-		. (NOT REPLACEABLE-ORDER NEXT HIGHER ASSY)		
						(ATTACHING PARTS)		
-77	211-0507-00			1		. SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-78	210-1160-00			1		. WASHER,NONMETAL:0.109 ID X 0.25 INCH OD	86445	OBD
						- - - * - - -		
-79	118-0722-00			1		. BRACKET,HEAT SK:ALUMINUM		
-80	----- -----			1		FAN,TUBEAXIAL:(SEE B200 REPL)		
						(ATTACHING PARTS)		
-81	211-0530-00			4		SCREW,MACHINE:6-32 X 1.75 INCH,PNH STL	83385	OBD
-82	210-0457-00			4		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
-83	210-0006-00			4		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-84	361-1055-00			4		SPACER,SLEEVE:1.24 L X 0.18 ID	80009	361-1055-00
-85	386-4399-00			1		PANEL,FAN MTG:	80009	386-4399-00
						(ATTACHING PARTS)		
-86	211-0614-00			5		SCR,ASSEM WSHR:6-32 X 0.250 PNH,STL CD PL	83385	OBD
						- - - * - - -		
-87	386-4400-00			1		PANEL,CKT BD CG:REAR	80009	386-4400-00
						(ATTACHING PARTS)		
-88	211-0534-00			4		SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		PANEL,CKT BD CG INCLUDES:		
-89	351-0087-00			16		. GUIDE,CKT BOARD:4.75 INCH LONG,PLASTIC	80009	351-0087-00
-90	----- -----			1		CKT BOARD ASSY:MAIN INTERCONNECT(SEE A60 REPL)		
						(ATTACHING PARTS)		
-91	211-0602-00			10		SCR,ASSEM WSHR:6-32 X 0.438 INCH,PNH BRS	80009	211-0602-00
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-92	124-0383-00			1		. TERMINAL BOARD:7 CONTACT,PLASTIC		
-93	131-2402-00			16		. CONN,RCPT,ELEC:EDGECARD,50/100 CONT	05574	3VH50/1CNK1
-94	131-1343-00			1		. TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
-95	386-4398-00			1		PANEL,BOTTOM:CIRCUIT BD CAGE	80009	386-4398-00



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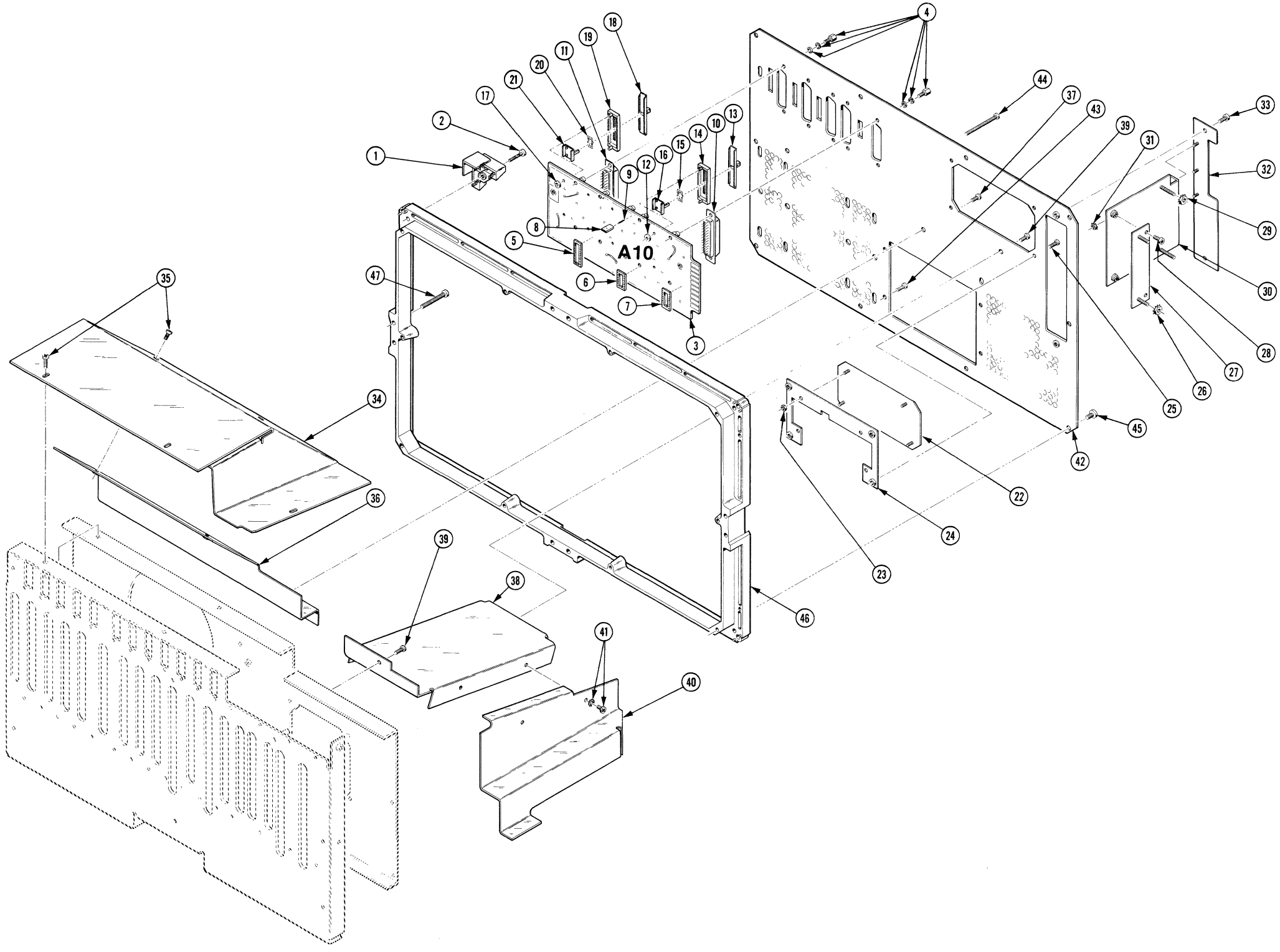

SEE END OF RMPL FOR WIRE ASSEMBLIES

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
4-1	348-0544-03			4		RTNR,CAB COVER:CORNER,TEK TAN	80009	348-0544-03
						(ATTACHING PARTS)		
-2	213-0782-00			4		SCREW,TPG,TF:8-32 X 0.625 FILH,STEEL CD PL	93907	OBD
						- - - * - - -		
-3	----- -----			1		CKT BOARD ASSY:COMM INTERFACE(SEE A10 REPL)		
						(ATTACHING PARTS)		
-4	214-3106-00			10		HARDWARE KIT:JACK SOCKET	53387	3341-1S
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
	129-0105-00			10		. POST,ELEC-MECH:0.218 OD X 0.219 INCH LONG	80009	129-0105-00
-5	136-0634-00			1		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-6	136-0269-02			4		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
-7	136-0260-02			6		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-8	131-0993-00			3		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-9	----- -----			9		. TERMINAL,PIN:(SEE A10J1,J2,J3 REPL)		
-10	131-0813-00			2		. CONN,RCPT,ELEC:CKT BD,25 CONT,FEM	80009	131-0813-00
-11	131-1437-00			3		. CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
	----- -----			1		. SWITCH,SLIDE:(SEE A10S1030 REPL)		
						(ATTACHING PARTS)		
-12	220-0828-00			2		. PUSH ON NUT:0.073 ID X 0.25 OD,PLASTIC	80009	220-0828-00
						- - - * - - -		
	----- -----			-		. SWITCH ASSY INCLUDES:		
-13	200-2227-00			1		. . COVER,SLIDE SW:5 OF 6 POSITION	80009	200-2227-00
-14	380-0542-00			1		. . HOUSING,SL SW:4 OF 6 POSN	80009	380-0542-00
-15	214-2774-00			1		. . SPRING,DETENT:SLIDE,SWITCH	80009	214-2774-00
-16	105-0738-00			1		. . ACTUATOR,CAM SW:0.6 DIA ATTENUATOR	80009	105-0738-00
	----- -----			3		. SWITCH,SLIDE:(SEE A10S1050,S1080,S1090 REPL)		
						(ATTACHING PARTS)		
-17	220-0828-00			6		. PUSH ON NUT:0.073 ID X 0.25 OD,PLASTIC	80009	220-0828-00
						- - - * - - -		
	----- -----			-		. SWITCH ASSY INCLUDES:		
-18	200-2227-00			3		. . COVER,SLIDE SW:5 OF 6 POSITION	80009	200-2227-00
-19	380-0555-00			3		. . HOUSING,SL SW:6 OF 6 POSITIONS	80009	380-0555-00
-20	214-2774-00			3		. . SPRING,DETENT:SLIDE,SWITCH	80009	214-2774-00
-21	105-0783-00			3		. . ACTUATOR,SL SW:CHOP AUTO ALTERNATE	80009	105-0783-00
-22	333-2638-00			1		PANEL,REAR:	80009	333-2638-00
						(ATTACHING PARTS)		
-23	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-24	386-4555-00			1		PLATE,CMPNT MTG:REAR PANEL,AL	80009	386-4555-00
						(ATTACHING PARTS)		
-25	211-0008-00			4		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-26	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
-27	343-0722-01			1		CLAMP,CABLE:3.125 L,ALUMINUM,W/BUSHINGS	80009	343-0722-01
						(ATTACHING PARTS)		
-28	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-29	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
-30	407-2528-00			1		BRACKET,ANGLE:STRAIN RELIEF	80009	407-2528-00
						(ATTACHING PARTS)		
-31	210-0586-00			3		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-32	200-2494-00			1		COVER,HOLE:CABLE OPENING,AL	80009	200-2494-00
						(ATTACHING PARTS)		
-33	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-34	200-2492-00	B010100	B011299	1		COVER,PWR SPLY:ALUMINUM	80009	200-2492-00
	200-2492-01	B011300		1		COVER,PWR SPLY:ALUMINUM	80009	200-2492-01
						(ATTACHING PARTS)		
-35	211-0507-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
	211-0614-00	XB011300		1		SCR,ASSEM WSHR:6-32 X 0.250 PNH,STL CD PL	83385	OBD
	129-0214-00	XB011300		1		INSULATOR,STDF:DELRIN	80009	129-0214-00
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
4-36	407-2540-00			1	BRACKET,COVER:ALUMINUM	80009	407-2540-00
					(ATTACHING PARTS)		
-37	211-0507-00			2	SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
					- - - * - - -		
-38	200-2493-00			1	COVER,XFMR:ALUMINUM	80009	200-2493-00
					(ATTACHING PARTS)		
-39	211-0507-00			2	SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
					- - - * - - -		
-40	407-2526-00	B010100	B021078	1	BRACKET,COVER:TRANSFORMER,AL	80009	407-2526-00
	407-2526-01	B021079		1	BRACKET,COVER:	80009	407-2526-01
					(ATTACHING PARTS)		
-41	211-0614-00			2	SCR,ASSEM WSHR:6-32 X 0.250 PNH,STL CD PL	83385	OBD
					- - - * - - -		
-42	333-2637-00			1	PANEL,REAR:	80009	333-2637-00
					(ATTACHING PARTS)		
-43	211-0507-00			5	SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-44	211-0553-00			8	SCREW,MACHINE:6-32 X 1.5 INCH,PNH STL	83385	OBD
-45	213-0801-00			10	SCREW,TPG,TF:8-32 X 0.312,TAPTITE,PNH	93907	OBD
					- - - * - - -		
-46	426-1595-01			1	FRAME,CABINET:REAR,10.5 X FULL RACK	80009	426-1595-01
					(ATTACHING PARTS)		
-47	212-0071-00			4	SCREW,MACHINE:8-32 X 1.000,FILH,STL,CD PL	83385	OBD
					- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						WIRE ASSEMBLIES		
	195-0621-00			2		LEAD,ELECTRICAL:12 AWG,6.0 L,2-N	80009	195-0621-00
	----- -----			-		(FROM A05 TO A60 TERMINAL)		
	195-1544-00			1		LEAD,ELECTRICAL:18 AWG,6.0 L,2-N	80009	195-1544-00
	----- -----			-		(FROM A05 TO A60 TERMINAL)		
	195-1550-00			1		LEAD,ELECTRICAL:12 AWG,7.0 L,O-N	80009	195-1550-00
	----- -----			-		(FROM A05 TO A60 TERMINAL)		
	195-1551-00			1		LEAD,ELECTRICAL:18 AWG,7.0 L,O-N	80009	195-1551-00
	----- -----			-		(FROM A05 TO A60 TERMINAL)		
	198-4351-00			1		WIRE SET,ELEC:	80009	198-4351-00
	----- -----			-		(FROM A05 TO S200)		
	198-4357-00			1		WIRE SET,ELEC:	80009	198-4357-00
	----- -----			-		(FROM A05 TO T311)		
	352-0198-00			1		. HLDR,TERM CONN:2 WIRE BLACK	80009	352-0198-00
	198-4358-00			1		WIRE SET,ELEC:	80009	198-4358-00
	----- -----			-		(FROM A05 TO T311)		
	198-4348-00			1		WIRE SET,ELEC:	80009	198-4348-00
	----- -----			-		(FROM A06(-) TO T311)		
	198-4349-00			1		WIRE SET,ELEC:	80009	198-4349-00
	----- -----			-		(FROM A06(+) TO T311)		
	198-4362-00			1		WIRE SET,ELEC:	80009	198-4362-00
	----- -----			-		(FROM A06-12V TO A60 TERMINAL)		
	198-4363-00			1		WIRE SET,ELEC:	80009	198-4363-00
	----- -----			-		(FROM A06+12V TO A60 TERMINAL)		
	175-2958-00			1		CA ASSY,SP,ELEC:40,28 AWG,300V,30.0 L	80009	175-2958-00
	----- -----			-		(FROM A10-P1 TO A40P2)		
	175-3090-00			1		CA ASSY,SP,ELEC:8,26 AWG,11.0 L,RIBBON	80009	175-3090-00
	----- -----			-		(FROM A50-J1 TO A60-J17)		
	195-1547-00			1		LEAD,ELECTRICAL:18 AWG,6.0 L,8-2	80009	195-1547-00
	----- -----			-		(FROM B200 TO T311)		
	195-0628-00			1		LEAD,ELECTRICAL:18 AWG,6.0 L,8-4	80009	195-0628-00
	----- -----			-		(FROM B201 TO T311)		
	195-1543-00			1		LEAD,ELECTRICAL:18 AWG,11.0 L,O-N	80009	195-1543-00
	----- -----			-		(FROM B201 TO T311)		
	195-1545-00			1		LEAD,ELECTRICAL:18 AWG,6.0 L,8-3	80009	195-1545-00
	----- -----			-		(FROM B201 TO T311)		
	195-1548-00			1		LEAD,ELECTRICAL:18 AWG,5.0 L,8-1	80009	195-1548-00
	----- -----			-		(FROM B201 TO T311)		
	195-0696-00			1		LEAD,ELECTRICAL:18 AWG,5.0 L,8-N	80009	195-0696-00
	----- -----			-		(FROM FL305 TO F313)		
	195-1540-00			1		LEAD,ELECTRICAL:18 AWG,3.0 L,5-4	80009	195-1540-00
	----- -----			-		(FROM FL305 TO CHASSIS GROUND)		
	175-2961-00			1		CA ASSY,SP,ELEC:4,18 AWG,31.0 L,8-N	80009	175-2961-00
	----- -----			-		(FROM S100 TO S300 & S301)		
	198-4352-00			1		WIRE SET,ELEC:	80009	198-4352-00
	----- -----			-		(FROM S200 TO T311)		
	198-4356-00			1		WIRE SET,ELEC:	80009	198-4356-00
	----- -----			-		(FROM S200 TO T311)		
	195-0630-00			1		LEAD,ELECTRICAL:18 AWG,5.0 L,8-1	80009	195-0630-00
	----- -----			-		(FROM S300 TO T311)		
	195-0631-00			1		LEAD,ELECTRICAL:18 AWG,7.0 L,8-4	80009	195-0631-00
	----- -----			-		(FROM S300 TO T311)		
	195-0627-00			1		LEAD,ELECTRICAL:18 AWG,8.0 L,8-3	80009	195-0627-00
	----- -----			-		(FROM S301 TO T311)		
	195-0629-00			1		LEAD,ELECTRICAL:18 AWG,7.0 L,8-5	80009	195-0629-00
	----- -----			-		(FROM S301 TO T311)		
	195-0638-00			1		LEAD,ELECTRICAL:18 AWG,10.0 L,8-N	80009	195-0638-00
	----- -----			-		(FROM S301 TO T311)		
	195-1549-00			1		LEAD,ELECTRICAL:18 AWG,6.0 L,8-2	80009	195-1549-00
	----- -----			-		(FROM S301 TO T311)		
	195-1261-00			1		LEAD,ELECTRICAL:18 AWG,8.0 L,O-N	80009	195-1261-00
	----- -----			-		(FROM T311 TO CHASSIS GROUND)		
	195-1541-00			1		LEAD,ELECTRICAL:18 AWG,5.0 L,5-4	80009	195-1541-00
	----- -----			-		(FROM FRONT PANEL TO FRONT SUBPANEL)		

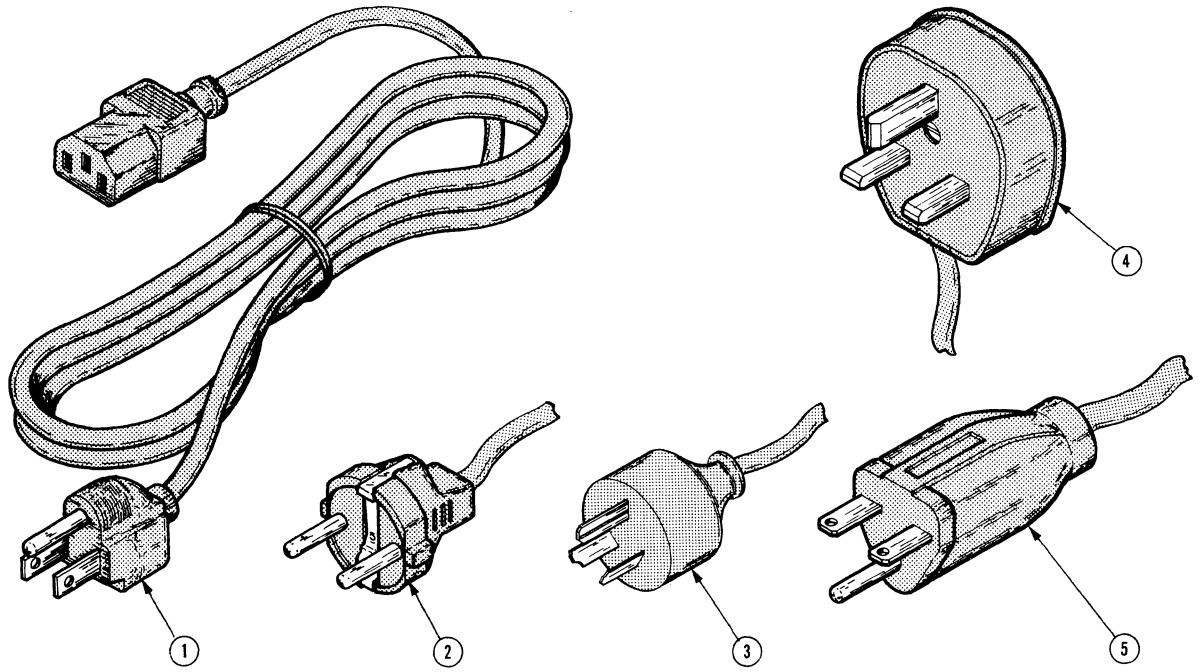

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
5-1	161-0066-00			1		CABLE ASSY,PWR,:3,18 AWG,115V,98.0 L	80009	161-0066-00
-2	161-0066-09			1		CABLE ASSY,PWR:3,0.75MM SQ,220V,96.0 L	80126	OBD
	----- -----			-		(OPTION A1 - EUROPEAN)		
-3	161-0066-10			1		CABLE ASSY,PWR:3,0.75MM SQ,240V,96.0 L	80126	OBD
	----- -----			-		(OPTION A2 - UNITED KINGDOM)		
-4	161-0066-11			1		CABLE ASSY,PWR:3,0.75MM,240V,96.0L	80126	OBD
	----- -----			-		(OPTION A3 - AUSTRALIAN)		
-5	161-0066-12			1		CABLE ASSY,PWR:3,18 AWG,240V,96.0 L	80126	OBD
	----- -----			-		(OPTION A4 - NORTH ARMERICAN)		
	016-0367-00			1		BDR,LOOSE-LEAF:2.0 CAP RING,VINYL COVER	80009	016-0367-00
	016-0370-00			1		DIV,LOOSE LEAF:1 FLEX DISC PKT	80009	016-0370-00
	062-4646-00	B010100	B010224	1		SOFTWARE PKG:DISC,8301 OPERATING SYSTEM	80009	062-4646-00
	062-4646-01	B010225		1		SOFTWARE PKG:DISC,8550 OPERATING SYSTEM	80009	062-4646-01
	062-5412-00	B010100	B020306	1		SOFTWARE PKG:8550 DIAGNOSTIC	80009	062-5412-00
	062-5412-01	B020307		1		SOFTWARE PKG:8550 DIAGNOSTIC	80009	062-5412-01
	062-5812-00			1		MANUAL,TECH:INSTRUCTION,8550 SIMPLIFYING	80009	062-5812-00
	070-2552-00			1		CARD,INFO:DISC HANDLING	80009	070-2552-00
	070-2974-00			1		MANUAL,TECH:INSTALLATION,8550 MDL	80009	070-2974-00
	070-3457-00			1		MANUAL,TECH:USERS,8550 LOGIC LAB SYSTEM	80009	070-3457-00
	070-3458-00			1		MANUAL,TECH:REFERENCE,8550 MDL	80009	070-3458-00
	070-3571-00			1		MANUAL,TECH:USERS,8550 LOGIC LAB SYSTEM	80009	070-3571-00
	070-3572-00			1		CARD,INFO:REFERENCE,8550 LOGIC LAB SYSTEM	80009	070-3572-00
	119-1182-00			2		FLOPPY DISKETTE:DOUBLE SIDED	80009	119-1182-00
	175-3316-00			1		CA ASSY,SP,ELEC:4 PR,24 AWG,96.0 L	80009	175-3316-00
						OPTIONAL ACCESSORIES		
	070-2976-01			1		MANUAL,TECH:SERVICE,8301 MDU	80009	070-2976-01
	175-3314-00			1		CA ASSY,SP,ELEC:4 PR,24 AWG,240.0 L	80009	175-3314-00
	175-3315-00			1		CA ASSY,SP,ELEC:4 PR,24 AWG,600.0 L	80009	175-3315-00

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MANUAL CHANGE INFORMATION

Date: 5-10-82 Change Reference: C3/582

Product: 8301 Microprocessor Development Unit Service Manual Part No.: 070-2976-01

DESCRIPTION

TEXT CORRECTIONS

Page 2-20, Table 2-6, the information in the Normal Operating Configuration column for Number W5011

CHANGE TO READ:

No change in original strapping unless specified in the Emulator Processor Installation Manual

REPLACEABLE ELECTRICAL PARTS LIST CORRECTIONS

Pages 17-22 and 17-23

ADD THE FOLLOWING LIST OF COMPONENTS:

A80U1070	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U1080	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U1090	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U1100	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U1110	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U1120	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U1130	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U2040	156-1599-00	MICROCIRCUIT,DI:DYNAMIC RAM CONTROLLER
A80U2060	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U2070	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U2080	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U2090	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U2100	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U2110	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U2120	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U2130	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U3070	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U3080	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U3090	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U3100	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U3110	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U3120	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U3130	15601552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U4070	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U4080	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U4090	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U4100	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U4110	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U4120	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM
A80U4130	156-1552-00	MICROCIRCUIT,DI:HMOS,16384 X 1 DRAM

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MANUAL CHANGE INFORMATION

Date: 6-25-82 Change Reference: M43797

Product: 8301 Microprocessor Development Unit Service Manual Part No.: 070-2976-01

DESCRIPTION Product Group 61

EFFECTIVE: SN B031445 and up

Page 17-3 The part number for the A20-System Controller Board

CHANGE TO:

670-6540-01

Page 17-3 The assembly listing of A30-System/Program Memory Board (670-6542-00)

ADD THIS NOTE:

Discontinued SN B031444

Page 17-3 The part number for the A80 System RAM Board (670-7342-00)

CHANGE TO:

670-7342-01

Page 17-10 The part numbers for A20U5030 and A20U5040

CHANGE TO:

A20U5030 160-0802-01 MICROCIRCUIT,DI:4096 X 8 EEPROM

A20U5040 160-0728-01 MICROCIRCUIT,DI:2048 X 8 EEPROM

Accessories Tab Page (at rear of manual)

CHANGE the part number 062-4646-01 to 062-4646-02

CHANGE the part number 070-2974-00 to 070-2974-01

CHANGE the part number 062-5412-01 to 062-5412-03

ADD these new listings:

070-3936-00 8550 MDL SYSTEM USERS MANUAL V 2

070-3937-00 8558 MDL SYSTEM REFERENCE BOOK V 2

062-5994-00 OPERATING DISC V 2

000-2775-00D