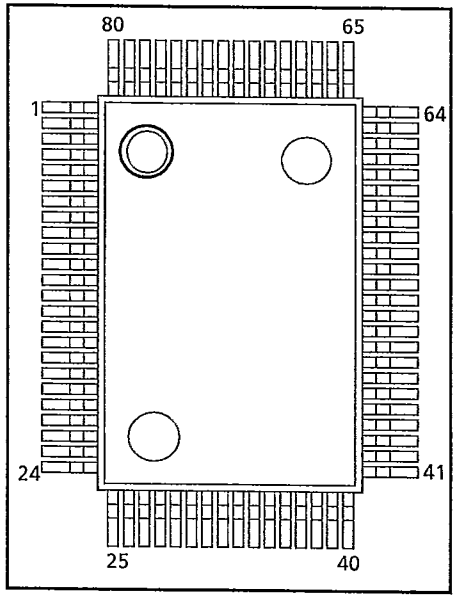
TC8569AF

Floppy Disk Controller

1. GENERAL DESCRIPTION

TC8569AF is a single chip LSI for Floppy Disk Controller, which has VFO and other circuits with FDC chip for interfacing a processor to floppy disk drive and supports data rates up to 1Mbps.



2. FEATURES

- Si-gate CMOS single chip LSI
- Single +5V power supply
- 80pin plastic flat package
- Compatible with 8080 system data and control buses
- Built-in VFO circuit
- Standby function for battery operation.
- MFM recording formats (1M / 500K / 250Kbps)
- FM recording formats (250k / 125Kbps)
- Built-in write pre-compensation circuit
- Motor enable control for 2 drives
- Built-in address decorder
- Multi-sector data transfer
- Multi-track data transfer
- Direct interface to FDD with CMOS type interface system
- Programmable step rate time
- Compatible with IBM diskette 1 and 2
- Including CRC check function ($X^{16}+X^{12}+X^5+1$)
- DMA / Non-DMA (interrupt) data transfer

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☐ TC8569AF is an improvement on the TC8569F. The differences between them are as follows.

· DMAC interface

TC8569F has the bug that DMA data transfer hangs up at using the DMA controller in verify mode [only -DACK2 is applied to FDC without -IOR and -IOW replying DRQ2], because DRQ2 is not reset.

DRQ2 is reset only by being applied -DACK2 and -IOR or -IOW at the same time. At using DAM controller in verify mode DMA controller applied only -DACK2 to FDC and therefore this trouble occurs.

TC8569AF resolves this problem. The verify mode of DMA controller is available.

· VFO part

TC8569F's built-in VFO has the bug to decrease compatibility with IBM PC's FDC circuit. TC8569F can hardly read the first sector when the all of the following conditions are satisfied.

① Adopting a record format which doesn't include a certain data pattern to re-detect Sync within, from Index position to the first sector.

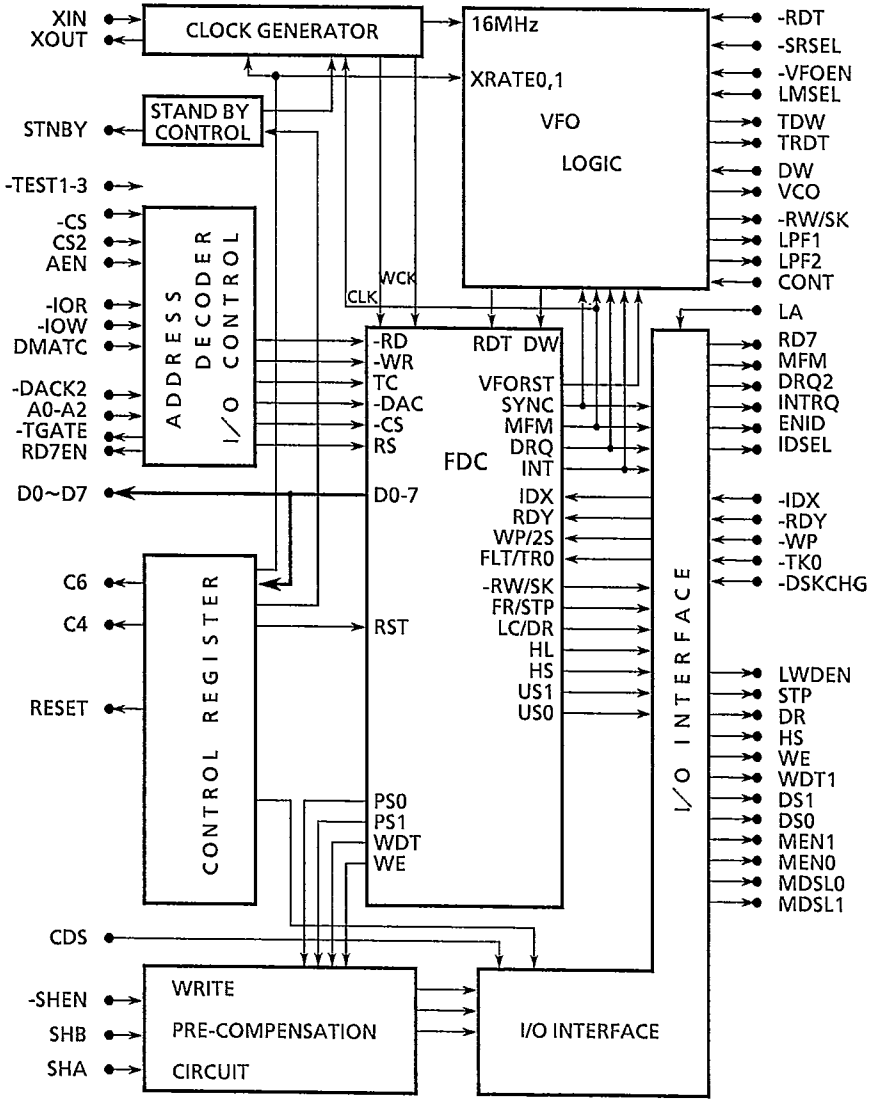
② Using FDC VFO in 2-filter mode

③ The first half of the sector data just before Index of the track is FF_{16} pattern.

TC8569AF improves this problem. Using TC8569AF in 2-filter mode, such a problem doesn't occur. TC8569AF has the same specification as TC8569F except the above two points.

3. FDC APPLICATION SYSTEM

3.1 FDC BLOCK DIAGRAM



3.2 APPLICATION SYSTEM 1

TC8569AF corresponds with each floppy by changing value of D0 and D1 (XRATE0, XRATE1) on control register 2. TABLE 3.2 shows the correlation between XRATE0, XRATE1 and these floppys.

TABLE 3.2

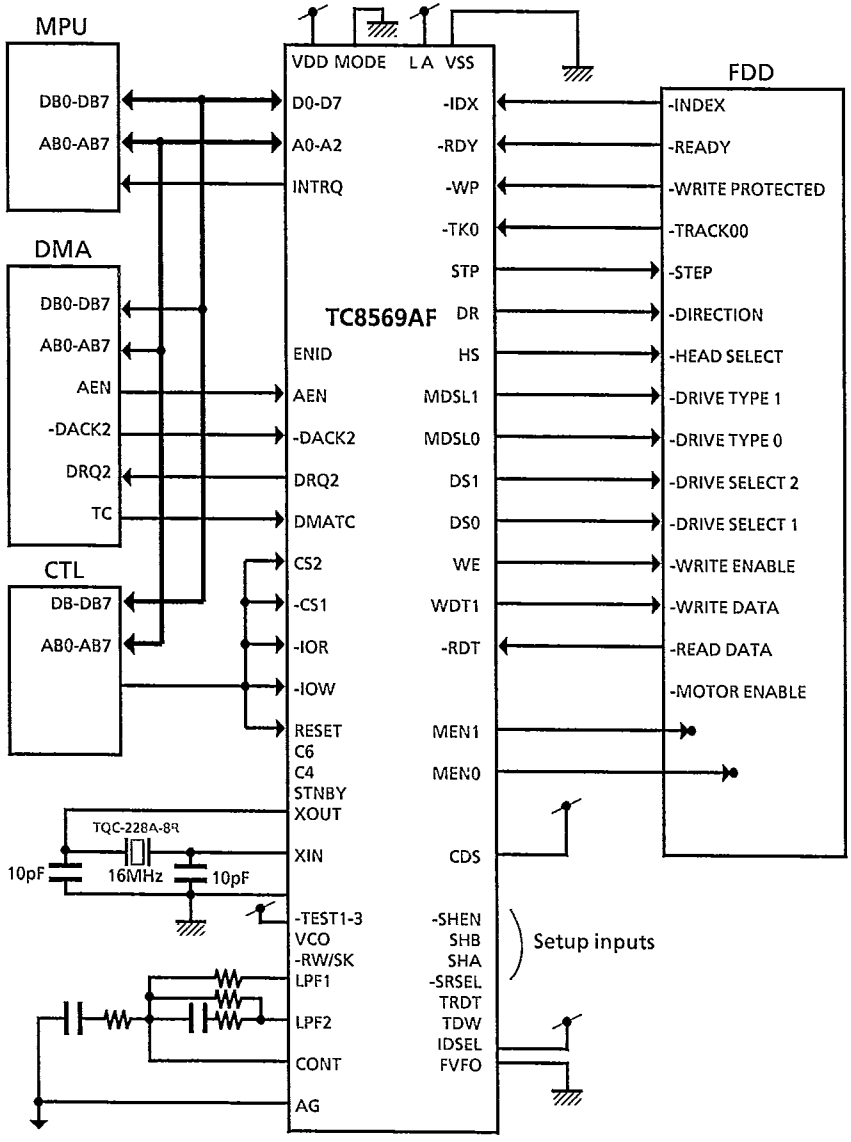
XRATE1	XRATE0	FLOPPY TYPE	CLOCK FREQ. OF INTERNAL FDC	TRANSFER RATE
0	0	Standard floppy	8MHz	500Kbps
0	1	–	–	–
1	0	Mini floppy	4MHz	250Kbps
1	1	Perpendicular magnetized floppy	16MHz	1 Mbps

This technical data is only described feature of floppys (Standard floppy, Mini floppy and Perpendicular Magnetized floppy). It's no mention of these floppy size.

1. Standard floppy
   2HD type or 8 inch floppy
   MFM recording formats (8MHz/500Kbps)
   FM recording formats (8MHz/125Kbps)
2. Mini floppy
   2D or 2DD type floppy
   MFM recording formats (4MHz/250Kbps)
   FM recording formats (4MHz/125Kbps)
3. Perpendicular Magnetized floppy
   2ED type floppy
   MFM recording formats (1Mbps)
   FM recording formats (not supported)

3.3 APPLICATION SYSTEM 2

3.3.1 ALTERNATIVE FILTER MODE



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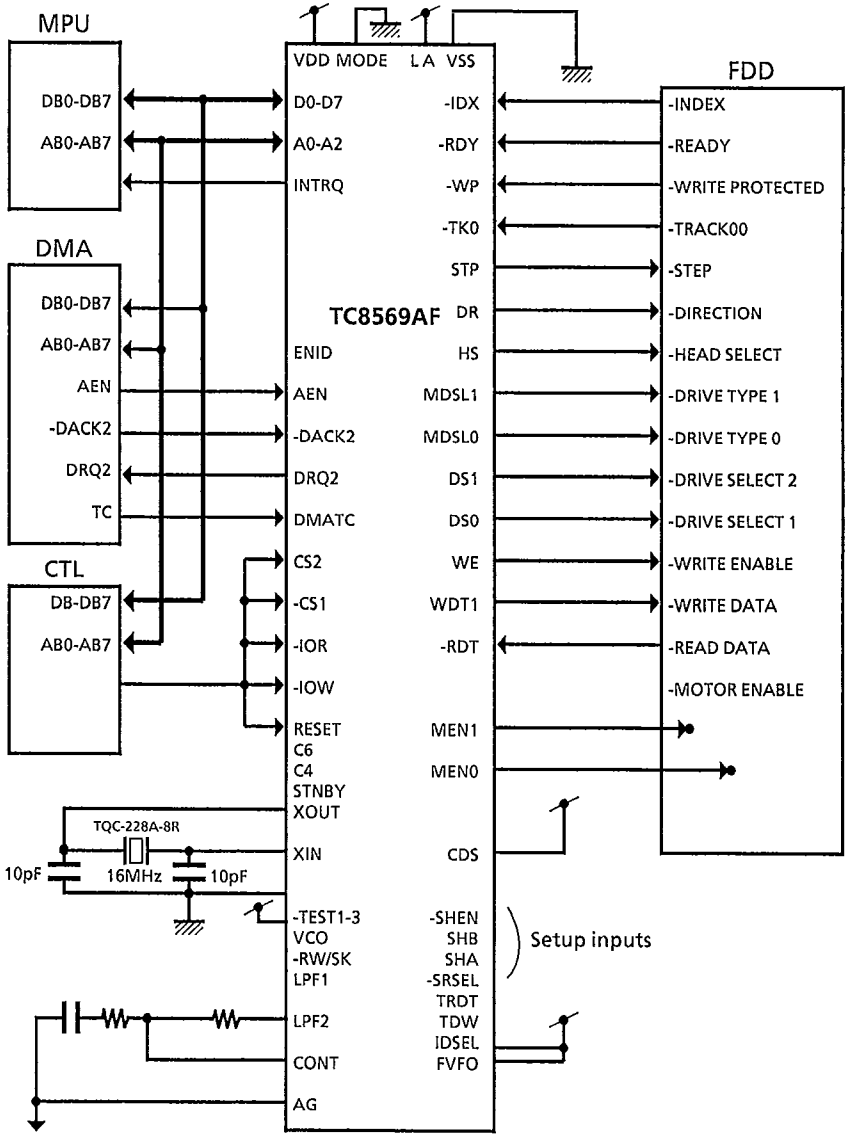
3.3.2 FIXED FILTER MODE



3.4 APPLICATION for INTERFACING to IBM PC/AT

TC8569AF has the compatible registers in the floppy controller board of the PC/AT that are CONTROL REGISTER 0 for the Digital Output Register (DOR) and CONTROL REGISTER 2 for the Data Rate Register (DRR) and Digital Input Register (DIR). Signals SA3 through SA9 and AEN in the slot of the PC/AT's system board are decoded and the decoded signal is applied to -CS1 input to be chosen 3F0H-3F7H address space to TC8569AF.

TC8569AF can support 300Kbps data transfer rate by 24MHz system clock and setting MODE input to "High". The content of CONTROL REGISTER 2 is as following table when the system clock is 24MHz and "High Level" is applied to MODE input.

TABLE 3.4 CONTENT of CONTROL REGISTER 2 (XIN = 24MHz , MODE = "High Level")

XRATE1	XRATE0	FLOPPY	SYSTEM CLOCK of FDC PART	TRANSFER RATE
0	0	Standard Floppy	8MHz	500Kbps
0	1	Mini Floppy	4.8MHz	300Kbps *
1	0	Mini Floppy	4MHz	250Kbps
1	1	—	—	—

* : FM format is not supported at 300Kbps.

The typical application circuit of the floppy disk controller board for the PC/AT is shown in FIG.3.4b.

In this application circuit, 1Mbps, 500Kbps, 300Kbps and 250Kbps can be supported. The extra reset routine is necessary to expect a correct operation when XRATE1 and XRATE0 are changed. This is because that some glitches are generated when the system clock or MODE input level is changed. The extra reset is not necessary to use TC8569AF in a fixed mode (MODE input and the system clock are not changed during the operation).

-RDY input is connected to "Low level" in this application circuit when you should pay attention to the flowing item. The ready flag in the FDC block is set to not-ready after the FDC reset is released. Then four interrupt factors occur when FDC completes the drive scanning one cycle to detect the change of ready line against the four drives. Therefore, SENSE INTERRUPT STATUS COMMAND should be issued four times to reset the interrupt factors.

As commenting in the chapter 3.5, you should pay attention to the difference between the internal FDC of TC8569AF and the conventional type of FDC in programing the application software. If you use the standby mode, the control program for FDC should be modified as follow.

The state of the CONTROL REGISTER 0 has no relation to fulfill the standby condition. Therefore, you should insert the additional procedure to set SMB bit in the CONTROL REGISTER 1 after the motor-off routine and to reset SMB bit before the motor-on routine (Cf. FIG.3.4a)

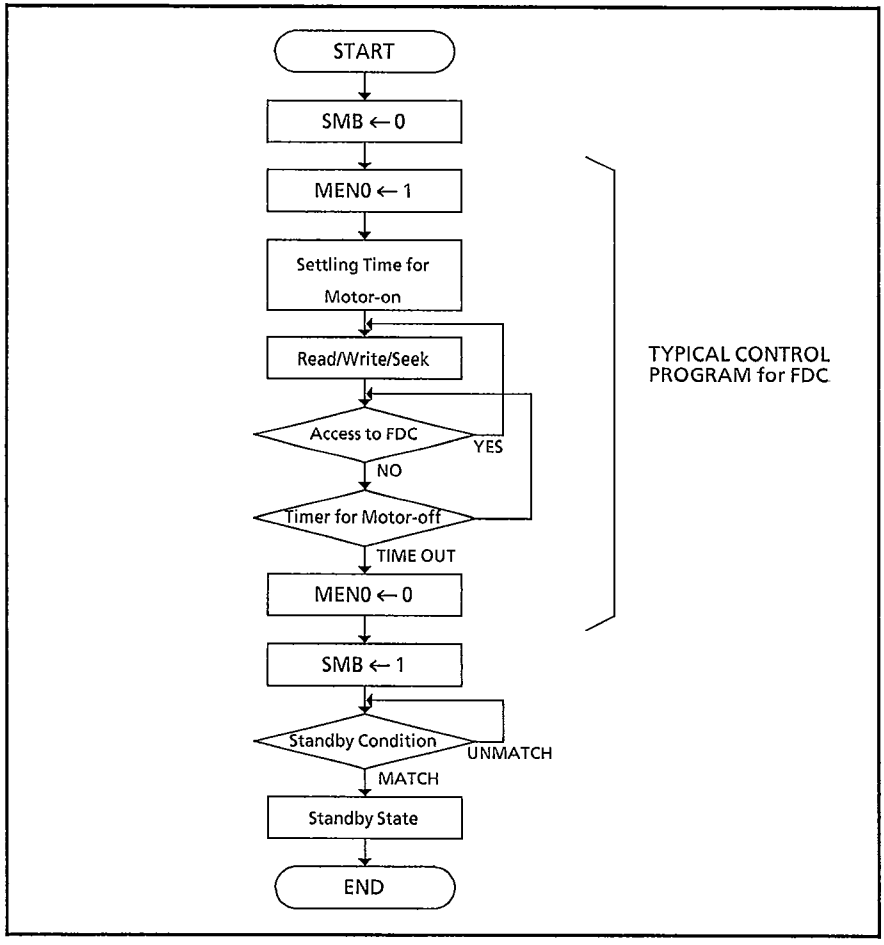


FIG.3.4a FLOW CHART for STANDBY CONTROL

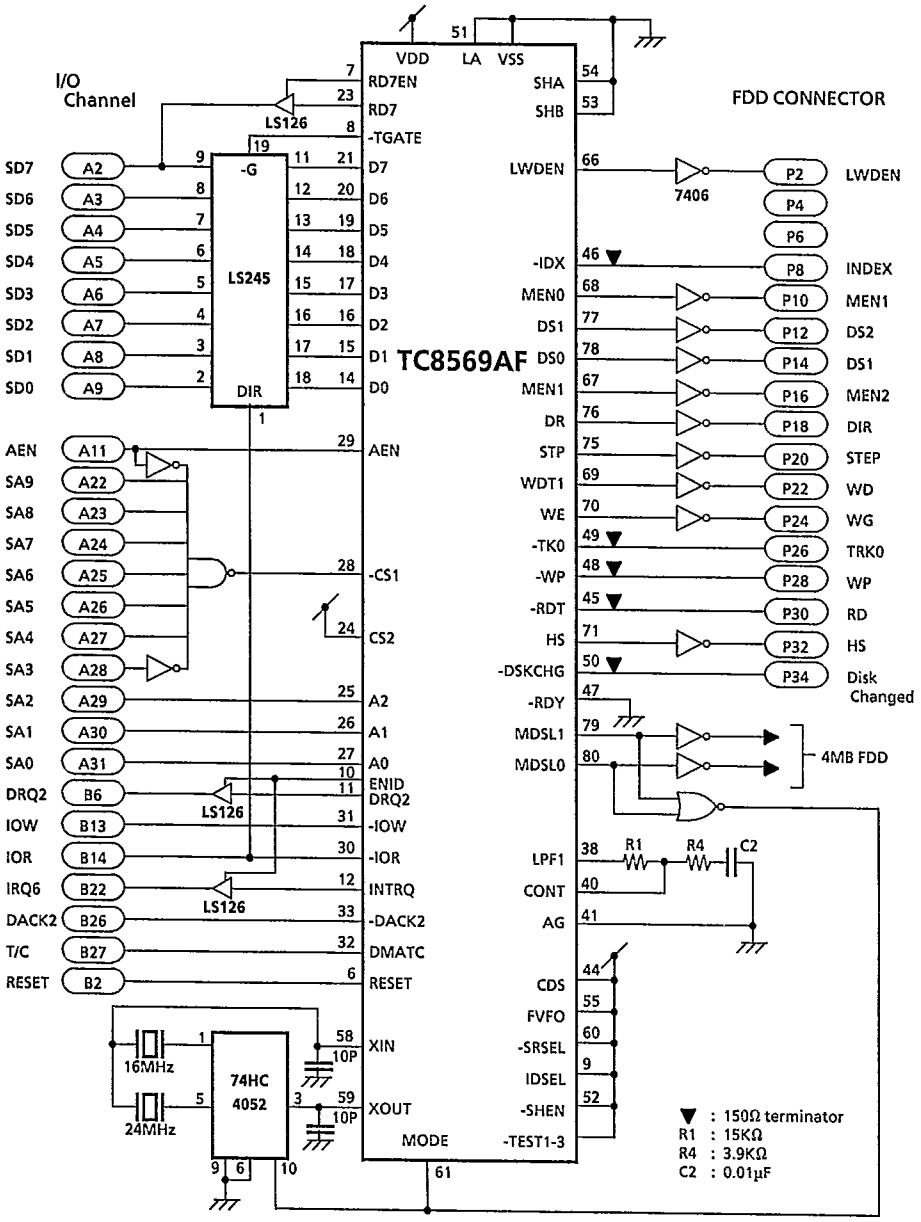


FIG.3.4b TYPICAL APPLICATION for IBM PC/AT

3.5 TC8569AF CAUTION IN PROGRAMING

3.5.1 FDC COMMAND

TC8569AF has a construction of commands which is almost compatible with that of TC8565P (compatible with µPD765A), but some commands are different from that of TC8565P. At programming, you should pay attention to the difference between TC8569AF and the conventional type of FDC as follows.

1 : Commands which is not supported with TC8569AF

TC8569AF does not have three commands that are SCAN EQUAL, SCAN LOW or EQUAL and SCAN HIGH or EQUAL.

2 : Command which has different function

SPECIFY COMMAND defines the time interval between step pulses, the head loading time and the head unloading time. But TC8569AF does not have the function of head load, then the head loading time and head unloading time have no meaning in the SPECIFY COMMAND of TC8569AF. It is necessary to find another method if the head loading time is used as the settling time for READ/WRITE operation.

3 : New Command

CONFIG COMMAND should be executed at initializing FDC.

3.5.2 CAUTION AT INITIALIZING

At initializing FDC and changing the type of floppy you should pay attention to the several points as follows.

1 : Reset operation for FDC block

TC8569AF can reset FDC block by writing 0 (zero) to bit D2 in CONTROL REGISTER 0. After TC8569AF is released from the reset state, this bit is set to 0 (zero). This bit need to be set to 1 when the FDC operation begins.

2 : Setting up the type of floppy

The standard floppy mode is set up after TC8569AF is released from the reset state. You should set up the correct floppy mode by writing to the CONTROL REGISTER 2 (XRATE1, XRATE0).

3 : Execution of CONFIG COMMAND

At initializing FDC, CONFIG COMMAND should be executed for the correct operation.

4. PIN DESCRIPTION

4.1 PIN CONNECTION

NO.	I/O	PIN NAME	NO.	I/O	PIN NAME	NO.	I/O	PIN NAME
1	O	C6	31	I	-IOW	61	I	MODE
2	O	C4	32	I	DMATC	62	O	STNBY
3	V	VDD	33	I	-DACK2	63	G	VSS
4	O	TDW	34	I	-TEST1	64	O	-RW/SK
5	O	TRDT	35	I	-TEST2	65	O	LOCK
6	I	RESET	36	I	-TEST3	66	O	LWDEN
7	O	RD7EN	37	G	VSS	67	O	MEN1
8	O	-TGATE	38	O	LPF1	68	O	MEN0
9	I	IDSEL	39	O	LPF2	69	O	WDT1
10	O	ENID	40	I	CONT	70	O	WE
11	O	DRQ2	41	AG	AVSS	71	O	HS
12	O	INTRQ	42	V	VDD	72	V	VDD
13	G	VSS	43	O	VCO	73	G	VSS
14	I/O	D0	44	I	CDS	74	O	HL
15	I/O	D1	45	I	-RDT	75	O	STP
16	I/O	D2	46	I	-IDX	76	O	DR
17	I/O	D3	47	I	-RDY	77	O	DS1
18	I/O	D4	48	I	-WP	78	O	DS0
19	I/O	D5	49	I	-TK0	79	O	MDSL1
20	I/O	D6	50	I	-DSKCHG	80	O	MDSL0
21	I/O	D7	51	I	LA			
22	G	VSS	52	I	-SHEN			
23	O	RD7	53	I	SHB			
24	I	CS2	54	I	SHA			
25	I	A2	55	I	FVFO			
26	I	A1	56	O	MFM			
27	I	A0	57	G	VSS			
28	I	-CS1	58	I	XIN			
29	I	AEN	59	O	XOUT			
30	I	-IOR	60	I	-SRSEL			

4.2 DESCRIPTION OF PIN FUNCTION

NO.	PIN NAME	I/O	PIN FUNCTION
1	C6	O	Output port of C6 bit in a CONTROL REGISTER 1.
2	C4	O	Output port of C4 bit in a CONTROL REGISTER 1.
3	VDD	V	+ 5V power supply
4	TWD	O	These terminals for test. Use in non-connect.
5	TRDT	O	
6	RESET	I	RESET CONTROL REGISTERS. The [-FRST] bit on the CONTROL REGISTER 0 is also reset, and consequently the internal FDC block is reset.
7	RD7EN	O	Output control signal for DISK CHANGED. When DISK CHANGE which is output to [RD7] is connected to the system bus via LS126, use this output for the gate signal for LS126.
8	-TGATE	O	When the data bus is connected to the system bus via LS245, use this signal for the gate signal for LS245.
9	IDSEL	I	[DRQ2] and [INTRQ] become three state output when "Low Level" is applied to this input. When ENID in the CONTROL REGISTER 0 is set to 0 (zero), [DRQ2] and [INTRQ] output become high-impedance state. When "High Level" is applied to this input, [DRQ2] and [INTRQ] become totem-pole output.
10	ENID	O	Side output of ENID bit in a CONTROL REGISTER 0.
11	DRQ2	O	Request signal for DMA transfer. This signal is the delayed [DRQ] from internal FDC chip. This signal is disabled to "Low level" with setting 0 (zero) on the ENID bit in the CONTROL REGISTER 0.
12	INTRQ	O	Interrupt request signal for system from internal FDC chip. This signal is disabled to "Low level" with setting 0 (zero) on the ENID bit in the CONTROL REGISTER 0.
13	VSS	G	Chips ground for digital circuits.
14	D0	I/O	Bidirectional 8 bit data bus.
15	D1	I/O	
16	D2	I/O	
17	D3	I/O	
18	D4	I/O	
19	D5	I/O	
20	D6	I/O	
21	D7	I/O	
22	VSS	G	Chips ground for digital circuits.

NO.	PIN NAME	I/O	PIN FUNCTION
23	RD7	O	DISK CHANGE output. When the address (A2 = 1, A1 = 1, A0 = 1)is accessed in the read operation (-IOR = Low), this output signal shows the inverting logic level which is applied to the [-DSKCHG] input. This output signal become high-impedance state in another condition.
24	CS2	I	Chip select input. High active control signal.
25	A2	I	Address 2 input
26	A1	I	Address 1 input.
27	A0	I	Address 0 input.
28	-CS1	I	Chip select input. Low active control signal.
29	AEN	I	Address enable input. "Low level" on [-CS1] and [AEN] and "High level" on [CS2] select the FDC-III, and allows [-IOR] and [-IOW] to be effective.
30	-IOR	I	Low active control signal to transfer data from the FDC to the Data-Bus.
31	-IOW	I	Low active control signal to transfer data from the Data-bus to the FDC-III.
32	DMATC	I	High active DMA transfer terminating signal. When the FDC works DMA MODE, this signal terminates the DMA transfer.
33	-DACK2	I	Low active DMA cycle executing signal. When the FDC works DMA MODE, this signal controls DMA I/O.
34	-TEST1	I	These input terminals for LSI test. "High level" should be applied.
35	-TEST2	I	
36	-TEST3	I	
37	VSS	G	Chips ground for digital circuits.
38	LPF1	O	The charge pump output for external low pass filter. This output will activate when PLL circuit force to lock the read signal (Pull-in mode).
39	LPF2	O	The charge pump output for external low pass filter. This output will be selected after PLL has pulled in the read signal and use low gain filter.
40	CONT	I	Analog voltage input for VCO.
41	AVSS	AG	Analog ground for VCO and PLL circuits.
42	VDD	V	+5V power supply.
43	VCO	O	The output terminal for LSI test. Use in non-connect.
44	CDS	I	When "High Level" is applied to this input, the decode signal of bit 0 in CONTROL REGISTER 0 is selected for [DS1] and [DS0]. When "Low Level" is applied to this input, the non-decode signals of US1 and US0 of FDC block are selected for [DS1] and [DS0].
45	-RDT	I	The input for the READ DATA from the floppy disk drive.
46	-IDX	I	Index pulse input from FDD system interface.

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NO.	PIN NAME	I/O	PIN FUNCTION
47	-RDY	I	Drive ready signal from FDD system interface.
48	-WP	I	Write protected indicate signal from FDD system interface.
49	-TK0	I	Head position indicate signal from FDD system interface. Low level on this terminal means that the head of FDD is on the TRACK #0 position.
50	-DSKCHG	I	Disk change signal from FDD system interface.
51	LA	I	Physical active level select on the output of FDD system interface signal, that is WDT1, WE, HS, STP, DR, HL, LWDEN, MEN0~1, DS0~1 and MDSL0~1. High level on this terminal means that these signal will be low active and can connect to directly FDD which has CMOS type interface specification.
52	-SHEN	I	If "High level" on the terminal, no pre-compensation shifting will be done.
53	SHB	I	Refer to the section 5.1.8.
54	SHA	I	
55	FVFO	I	This signal decides the operation of the internal VFO circuit. The VFO operates in fixed filter non-switching mode when "High", and operates in alternative filters (high gain and low gain filters) switching mode when "Low".
56	MFM	O	This output terminal will show the recording format of the operation of FDC. "High level" on this terminal shows that the FDC works at MFM recording format and otherwise shows FM recording format.
57	VSS	G	Chips ground for digital circuits.
58	XIN	I	This input connects the crystal oscillator or external clock signal. In the standard usage, use 16MHz crystal oscillator.
59	XOUT	O	This output is inverted signal of [XIN], or connected the crystal oscillator.
60	-SRSEL	I	"High Level" is applied to this input. If "Low Level" is applied, you will be able to program the step rate (Ref. SPECIFY COMMAND) at the step of 1ms in mini floppy mode.
61	MODE	I	"Low level" should be applied.
62	STNBY	O	This signal shows that FDC-III is in a standby mode. In a standby mode, all internal clock is stopped for saving power dissipation and following signals are inactive states WDT1, WE, HS, STP, DR, HL, LWDEN, MEN0~1, DS0~1 and MDSL0~1.
63	VSS	G	Chips ground for digital circuits.
64	-RW/SK	O	"Low" shows that read / write operation is selected, and "High" shows that seek operation is selected.
65	LOCK	O	The terminal for test. Use in non-connect.
66	LWDEN	O	Low density output for FDD. Low active when LA = High.

NO.	PIN NAME	I/O	PIN FUNCTION
67	MEN1	O	Motor enable for drive #1 for FDD. Low active when LA = High.
68	MEN0	O	Motor enable for drive #0 for FDD. Low active when LA = High.
69	WDT1	O	Pre-compensated write data for FDD. Low active when LA = High.
70	WE	O	Write enable signal for FDD. Low active when LA = High.
71	HS	O	Head select signal when LA = High / when LA = Low High Head0 Head1 Low Head1 Head0
72	VDD	V	+ 5V power supply.
73	VSS	G	Chips ground for digital circuits.
74	HL	O	The terminal for test. Use in non-connect.
75	STP	O	Decoded step pulse signal, connected disk drives for FDD. Low active when LA = High.
76	DR	O	Decoded direction signal for head seek. when LA = High LA = Low Low inner seek outer seek High outer seek inner seek
77	DS1	O	Drive select 1 signal for FDD. Low active when LA = High. Refer to TABLE 5.1.11a.
78	DS0	O	Drive select 0 signal for FDD. Low active when LA = High. Refer to TABLE 5.1.11b.
79	MDSL1	O	These outputs signals show the FDD type which this controller expects. Refer to TABLE 5.1.9.
80	MDSL0	O	

5. FUNCTIONAL DESCRIPTION

5.1 CONTROL REGISTER and PART of PERIPHERAL CIRCUIT

5.1.1 RELATION of ADDRESS LINE and EACH REGISTER

AEN	-CS	CS2	A2	A1	A0	-IOR	-IOW	SELECTION
H	×	×	×	×	×	×	×	NO-SELECTION
×	H	×	×	×	×	×	×	
×	×	L	×	×	×	×	×	
L	L	H	L	L	×	×	×	
L	L	H	L	H	L	L	H	
						H	L	CONTROL REGISTER 0
L	L	H	L	H	H	×	×	NO SELECTION
L	L	H	H	L	L	L	H	MAIN STATUS REGISTER
						H	L	CONTROL REGISTER 1
L	L	H	H	L	H	L	H	DATA REGISTER
						H	L	
L	L	H	H	H	L	×	×	NO SELECTIN
L	L	H	H	H	H	L	H	CONTROL REGISTER 2
						H	L	
×	×	×	×	×	×	L	L	INHIBIT
×	×	×	×	×	×	H	H	NO SELECTION

H : High L : Low × : Don't Care

5.1.2 CONDITION OF STANDBY STATE

LSI will enter into standby mode after several times elapsed, when the SBM bit in the CONTROL REGISTER 1 is set to "1" and following conditions are filled. The waiting time is decided by the state of internal FDC mode. Usually, 6ms to 8ms in MINI floppy mode and 3ms to 4ms in STANDRAD floppy mode. Additional condition is as follows.

- ○ -FRST bit of CONTROL REGISTER 1 is set to "1".
- ○ FDC is in the state that it is waiting command from the host.

The output terminal [STNBY] is activated when FDC is in the standby state, and X'tal oscillation stops. Standby state allows the drive output signals WDT1, WE, HS, STP, DR, HL, LWDEN, MEN0~1, DS0~1and MDSL0~1 to be inactive.

LSI will take off from the standby state when one of following conditions is detected.

- ○ SBM bit is set to "0".
- ○ -FRST bit is set to "0".
- ○ FDC receives a command.

5.1.3 CONTROL REGISTER 0

5 bit register for write only

BIT	SYMBOL	NAME	MEANING
D7		RESERVED	
D6		RESERVED	
D5	MEN1	MOTOR ENABLE 1	Radial motor on signal for #1 Drive
D4	MEN0	MOTOR ENABLE 0	Radial motor on signal for #0 Drive
D3	ENID	ENABLE INT & DMA REQUEST	INTRQ and DRQ2 are enabled when this bit is "High level".
D2	-FRST	NOT · FDC · RESET	0 on this bit will reset the internal FDC block. For normal operation, this bit should be set to 1.
D1		RESERVED	Drive Select bit : 0 on this bit indicates that drive A is selected, 1 indicates that drive B is selected.
D0	DSA	DRIVE SELECT A	

If RESET signal get to "High ", all bits are cleared.

5.1.4 CONTROL REGISTER 1

4 bit register for write only

BIT	SYMBOL	NAME	MEANING
D7	ENABLE 6		When 1 is applied to this bit during byte write operation of this register, the value of C6 becomes to D6. When 0 is applied to this bit during byte write operation of this register, the value of C6 is to be copy of D6.
D6	C6	CONTROL 6	
D5	ENABLE 4		
D4	C4	CONTROL 4	
D3	ENABLE 2		When 1 is applied to this bit, FDC enables to transfer into standby mode.
D2	SBM	STANDBY MODE	
D1	ENABLE 1		FDC terminal count control bit. This bit will be used to terminate data transfer in Non-DMA
D0	FDCTC	FDC TERMINAL COUNT	

D7, D5, D3 and D1 are the write enable bit for the each lower bit. For example, when 03H is written to the register, only D0 can be set to 1.

5.1.5 CONTROL REGISTER 2

3 bit register for write and read

BIT	SYMBOL	I/O	NAME	MEANING
D7	DCHG	O	DISK CHANGE	Use RD7 wired with D7. Refer to FIG. 5.1.5.
D6~D2			RESERVED	
D1	XRATE1		TRANSFER RATE 1	Refer to TABLE 3.2
D0	XRATE0		TRANSFER RATE 0	

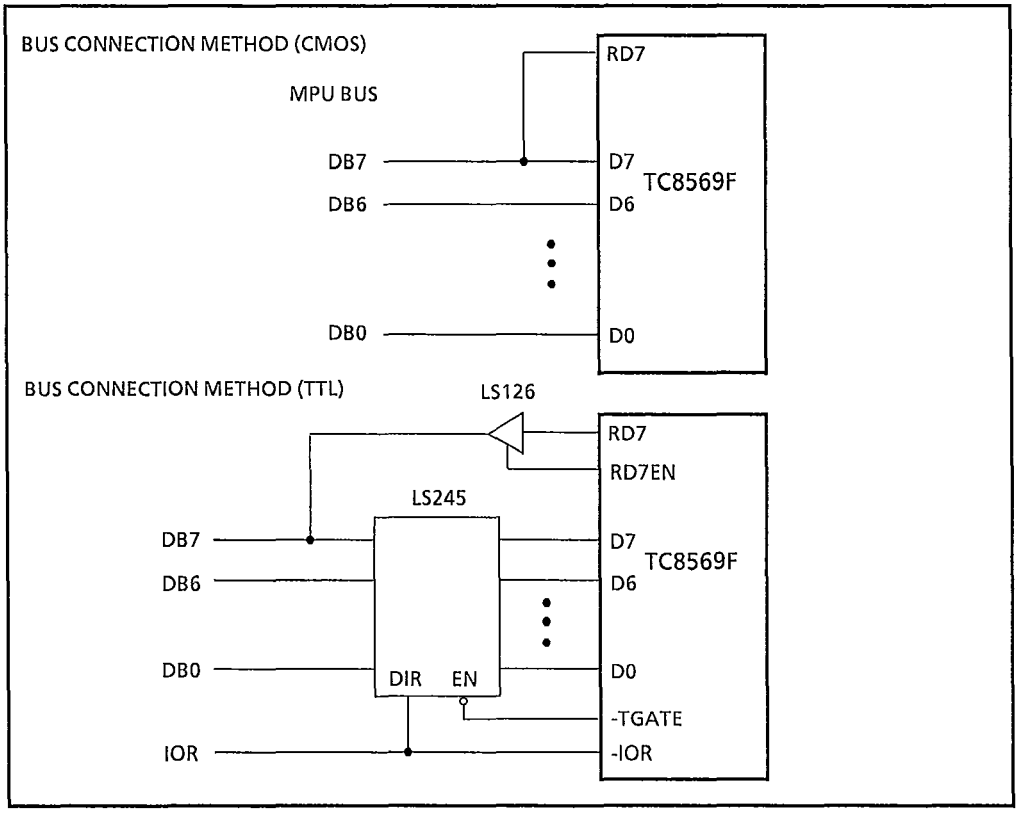
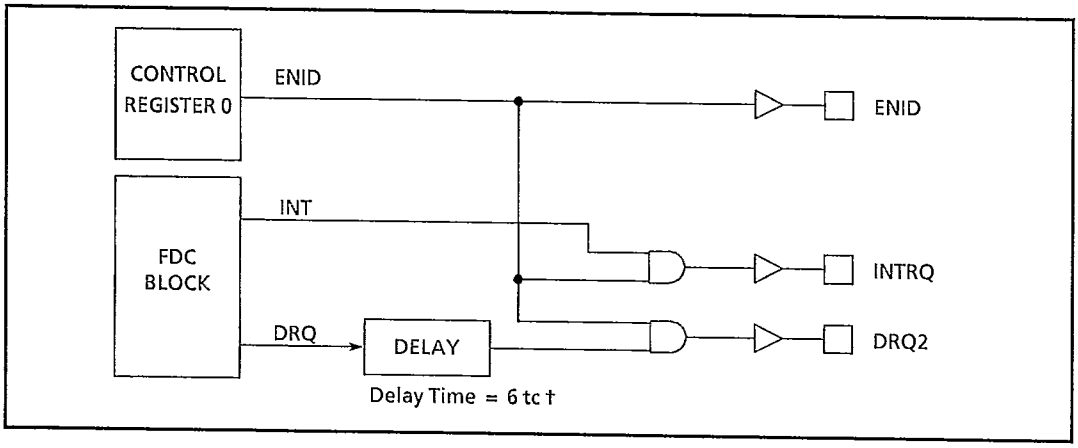


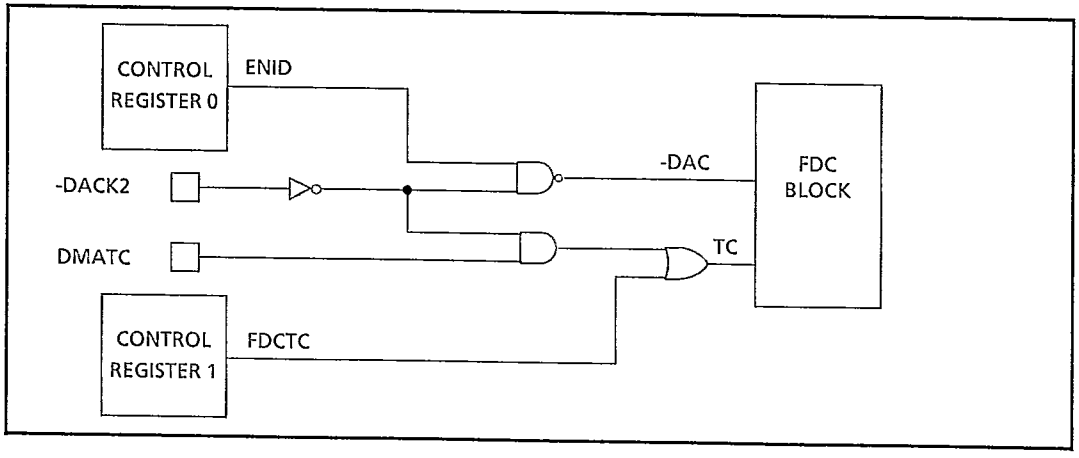
FIG.5.1.5 BUS CONNECTION METHOD

5.1.6 RELATION OF ENID, INT, INTRQ, DRQ, DRQ2



† tc : tc = 62.5ns (1Mbps)
125ns (500Kbps)
250ns (250Kbps)

5.1.7 RELATION OF ENID, -DACK2, DMATC, FDCTD



5.1.8 WRITE COMPENSATION CIRCUIT

-SHEN	XRATE1	XRATE0	SHB	SHA	SHIFT	TRANSFER RATE
H	×	×	×	×	0 ns	×
L	L	L	L	L	62.5 ns	500 Kbps
L	L	L	L	H	125.0 ns	
L	L	L	H	L	187.5 ns	
L	L	L	H	H	250.0 ns	
L	L	H	×	×	–	–
L	H	L	L	L	125.0 ns	250 Kbps
L	H	L	L	H	250.0 ns	
L	H	L	H	L	375.0 ns	
L	H	L	H	H	500.0 ns	
L	H	H	L	L	62.5 ns	1 Mbps
L	H	H	L	H	125.0 ns	
L	H	H	H	L	187.5 ns	
L	H	H	H	H	250.0 ns	

5.1.9 FLOPPY DISK DRVE MODE CHANGE

TABLE 5.1.9 FLOPPY DISK DRIVE MODE CHANGE

XRATE1	XRATE0	MDSL0	MDSL1	LWDEN
0	0	H	L	H
0	1	H	H	L
1	0	L	L	L
1	1	L	H	(L)

LA input = "High"

5.1.10 GATE OUTPUT FOR BUS TRANSCEIVER

-DACK2	AEN	-CS1	CS2	A2	A1	A0	-IOR	-IOW	-TGATE
H	H	×	×	×	×	×	×	×	H
H	×	H	×	×	×	×	×	×	H
H	×	×	L	×	×	×	×	×	H
×	×	×	×	×	×	×	L	L	INHIBIT
H	L	L	H	L	L	L	×	×	H
H	L	L	H	L	L	H	×	×	H
H	L	L	H	L	H	L	L	H	H
H	L	L	H	L	H	L	H	L	L
H	L	L	H	L	H	L	H	H	H
H	L	L	H	L	H	H	×	×	H
H	L	L	H	H	L	L	L	H	L
H	L	L	H	H	L	L	H	L	L
H	L	L	H	H	L	L	H	H	H
H	L	L	H	H	L	H	L	H	L
H	L	L	H	H	L	H	H	L	L
H	L	L	H	H	L	H	H	H	H
H	L	L	H	H	H	L	×	×	H
H	L	L	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	L	L
H	L	L	H	H	H	H	H	H	H
L	×	×	×	×	×	×	×	×	L

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5.1.11 DRIVE SELECT OUTPUT

CDS = High, LA = High

TABLE 5.1.11a

BIT 0 of the CONTROL REGISTER 0	US1 of FDC BLOCK	US0 of FDC BLOCK	DS1	DS0
1	×	×	Low	High
0	×	×	High	Low

× : Don't Care

CDS = Low, LA = High

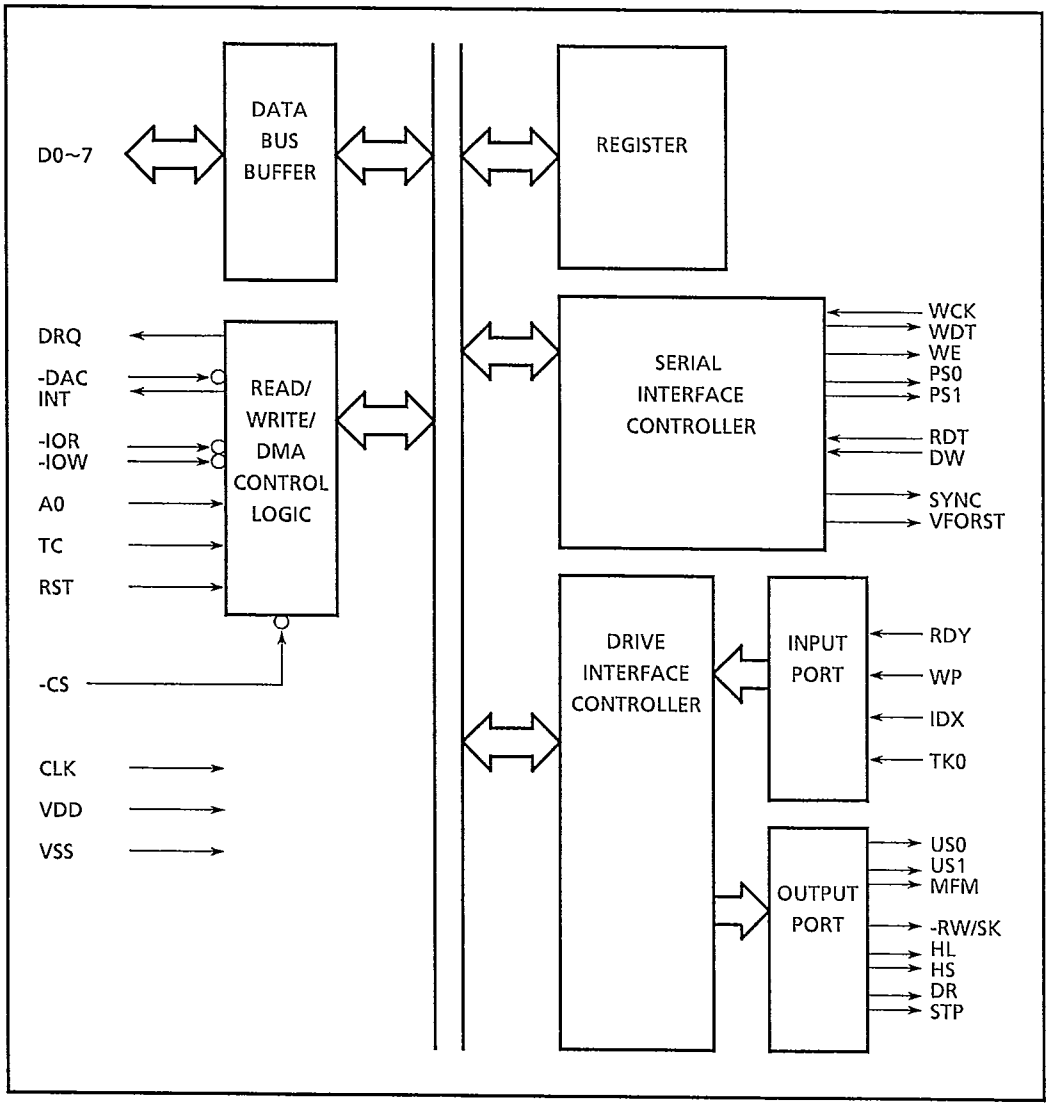
TABLE 5.1.11b

BIT 0 of the CONTROL REGISTER 0	US1 of FDC BLOCK	US0 of FDC BLOCK	DS1	DS0
×	0	0	High	High
×	0	1	High	Low
×	1	0	Low	High
×	1	1	Low	Low

× : Don't Care

5.2 PART OF FDC

5.2.1 DIAGRAM OF FDC



FLOPPY DISK CONTROLLER

5.2.2 FDC'S REGISTER AND CPU INTERFACE

FDC has two 8-bit registers accessible by the main system processor. One is a Main Status Register, and the other is a Data Register. The Main Status Register indicates the status information of the FDC and is always accessible.

The Data Register is used for data transfer between the FDC and the main processor. Command bytes are written into the Data Register in order to program the FDC, and also Status bytes are read out of the Data Register in order to obtain the result after execution of the commands.

Main Status Register may be read and is used to facilitate the data transfer between the processor and the FDC. The relationship between Main Status Register and [-IOR], [-IOW] and [A0] signals is shown below.

CS2 = A2 = 1, A1 = 0, AEN = 0

[-CS1]	[A0]	[-IOR]	[-IOW]	FUNCTION
H	X	X	X	Non Select
L	L	L	L	Illegal
L	L	L	H	Read Main Status Register
L	L	H	L	Write into CONTROL REGISTER 1
L	H	L	L	Illegal
L	H	L	H	Read from Data Register
L	H	H	L	Write into Data Register

Each bit in the Main Status Register are defined as TABLE 5.2.2. The RQM and DIO bits in the Main Status Register indicate whether Data Register is ready or not and in which direction data will be transferred on Data Bus.

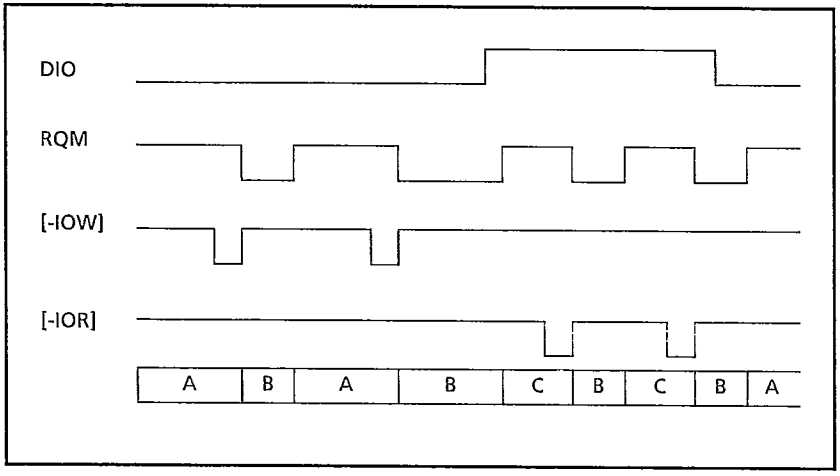


FIG.5.2.2 MAIN STATUS REGISTER TIMING

A	:	(DIO = "Low" and RQM = "High")	The processor may write the data in Data Register.
B	:	(RQM = "Low")	Data Register is not ready.
C	:	(DIO = "High" and RQM = "High")	In data register, data byte which will be read out by processor is already prepared.

FLOPPY DISK CONTROLLER

TABLE 5.2.2 MAIN STATUS REGISTER

BIT	SYMBOL	NAME	MEANING
D7	RQM	REQUEST for MASTER	Indicates that Data Register is ready to send the data to or to receive the data from the processor.
D6	DIO	DATA INPUT/ OUTPUT	Indicates the direction of data transfer between Data Register and the processor. When DIO is a "High", transfer is from Data Register to the processor. When DIO is a "Low", transfer from the processor to Data Register.
D5	NDM	Non-DMA mode	Indicates that the FDC is Non-DMA mode. It is set only during Execution-Phase in Non-DMA mode.
D4	CB	FDC BUSY	Indicates that FDC is in Execution-Phase of a read/write command, in Command-Phase, or in Result-Phase.
D3	D3B	FDD 3 BUSY	FDD number 3 is in the Seek mode.
D2	D2B	FDD 2 BUSY	FDD number 2 is in the Seek mode.
D1	D1B	FDD 1 BUSY	FDD number 1 is in the Seek mode.
D0	D0B	FDD 0 BUSY	FDD number 0 is in the Seek mode.

FDC supports thirteen different commands. Each of commands is initiated by a multi-byte transfer from the processor, and the result after executing of the command is a multi-byte transfer to the processor. Because the multi-byte information is interchanged between the FDC and the Processor, it is regarded that each command consists of following three phases.

Commands-Phase : The FDC receives the necessary information to perform a particular operation from the processor.

Execution-Phase : The FDC performs the specified operation.

Result-Phase : After the operation Result Status information or other information is sent to the processor.

In the Command-Phase or the Result-Phase, the processor must read out the Main Status Register before each byte of information is written into or read out from the Data Register.

When each byte of the command and the parameter is written into the FDC, bit D7 and D6 in the Main Status Register must be in high level and low level, respectively.

Because most of the Commands need multiple bytes, the Main Status Register must be read out before each byte is transferred to the FDC. In the Result-phase, the bit D7 and D6 in Main Status Register must be both in high levels before each byte is read out from the Data Register.
The reading out of the Main Status Register before each byte transfer to the FDC is necessary only in the Command-Phase and the Result-Phase, but it is not always necessary in the Execution-Phase.

When the FDC is in Non-DMA mode, the receipt of each data byte (if the FDD is now reading out data from the FDD) is indicated by the Interrupt signal [INTRQ].

The generation of the Read signal ([-IOR]=0) will not only output the data on the data bus but also reset the [INTRQ] signal. If the processor can not deal with interrupts fast enough (within 7.0μs for Perpendicular FDD mode), then it examines the Main Status Register, and then bit 7 (RQM) functions just like the Interrupt signal. Similarly in the Write command, Write signal resets the Interrupt signal.

If the FDC is in the DMA mode, then the Interrupt signal is not generated during the Execution-Phase. When the each data byte is available, the FDC generates [DRQ2] (DMA request) signal. Then the DMA controller generates both DMA Acknowledge signal and Read signal ([-DACK2]=0 and [-IOR]=0).

In a Read command, when the DMA acknowledge signal becomes low level, the FDC automatically resets the [DRQ2]. In a Write command, [-IOW] is substituted for [-IOR]. If the Execution-Phase is terminated (Terminal Count has been inputted), the Interrupt request is generated. This means the beginning of the Result-Phase. When the first data byte is read during the Result-Phase, Interrupt signal is automatically reset. During the Result-Phase, all data bytes shown in the COMMAND TABLE must be read.

For example, the READ DATA COMMAND has seven data bytes in the Result-Phase. All seven data bytes must be read out in order to complete the READ DATA COMMAND. This FDC will not accept the next command until all these seven data bytes are read out. In the same way, all the data bytes of the other commands must be read out during the Result-Phase. The FDC has five Status Registers. The Main Status Register mentioned above can always be read out by the processor. The other four Result Status Register (ST0, ST1, ST2, ST3) is available only in the Result-Phase, and read out only after the termination of the command.

The specified command determines how many the Result Status Registers will be read. The COMMAND TABLE shows the data bytes that are sent to the FDC in the Command-Phase and read out from the FDC in the Result-Phase. That is, the command code must be sent first, and the other bytes must be sent in order. So the Command-Phase and the Result-Phase can not be shorten. When the last data byte in the Command-Phase is sent to the FDC, the Execution-Phase automatically starts. Similarly, when the last byte in the Result-Phase is read out, the command is automatically terminated, and then the FDC is ready for a new command.

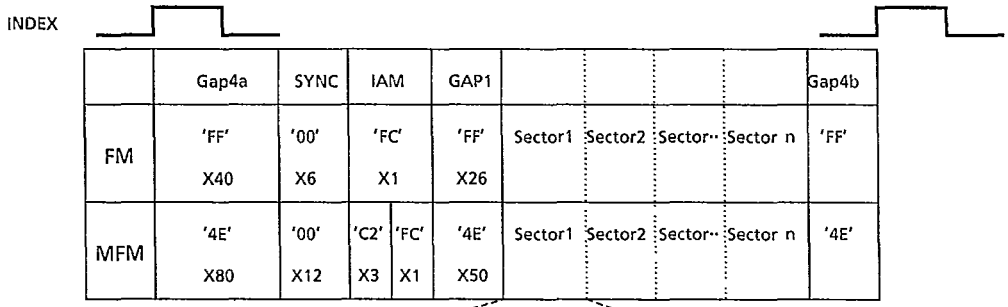
5.2.3 FUNCTION OF POLING IN FDC

After the SPECIFY COMMAND has been sent to the FDC, the drive select signals, the DS1 and DS0, are automatically in the polling mode. Between the commands (and between the step pulses in the seek mode), the FDC checks the four FDDs looking for a change of the ready signals from drive units.

If the Ready Signal is changed, then the FDC generates the Interrupt Signal. After the processor has issued the SENSE INTERRUPT STATUS COMMAND, the Result Status Register 0 (ST0) is read out, and the Not Ready bit (NR) in ST0 shows the present status. Because of the polling of Ready Signal between the commands, the processor can notice which drives are on line or which drives are off line.

5.2.4 TRACK FORMAT

(1) IBM FORMAT



	Gap4a	SYNC	IAM		GAP1				Gap4b
FM	'FF' X40	'00' X6	'FC' X1		'FF' X26	Sector1	Sector2	Sector··	Sector n	'FF'
MFM	'4E' X80	'00' X12	'C2' X3	'FC' X1	'4E' X50	Sector1	Sector2	Sector··	Sector n	'4E'

Repeat Until
Number of Sector

		SYNC	IDAM		C	H	R	N	CRC	Gap2	SYNC	DAM (DDAM)		DATA *1	CRC	Gap3 *1
IBM	FM	'00' X6	'FE' X1		X1	X1	X1	X1	X2	'FF' X11	'00' X6	'FB' ('F8') X1			X2	'FF'
IBM	MFM	'00' X12	'A1' X3	'A1' X3	X1	X1	X1	X1	X2	'4E' X22	'00' X12	'A1' X3	'FB' ('F8') X1		X2	'4E'
Pre-Erase	MFM	'00' X12	'A1' X3	'A1' X3	X1	X1	X1	X1	X2	'4E' X41	'00' X12	'A1' X3	'FB' ('F8') X1		X2	'4E'

(*1) Programmable

Missing Clock of Address Mark

AM	FM		MFM	
	DATA	CLOCK	DATA	CLOCK
IAM	FC	D7	C2	14
IDAM	FE	C7	A1	0A
DAM	FB	C7	A1	0A
DDAM	F8	C7	A1	0A

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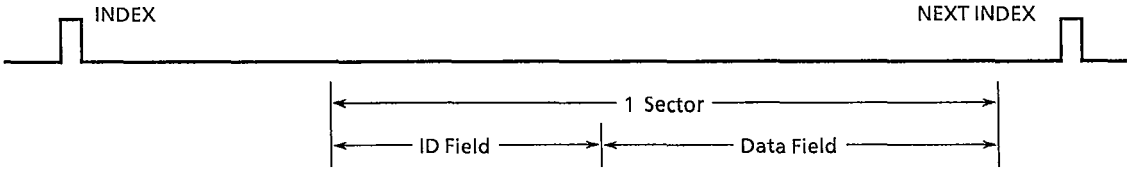
(2) PFD Format



	Gap0	SYNC	IAM		Gap1	SYNC	IDAM		ID	CRC	Gap2	SYNC	DAM		DATA	CRC	Gap3	Gap4	SECTOR /TRACK
Bytes	80	12	3	1	50	12	3	1	4	2	41	12	3	1	256	2	62	515	61
															512		83	518	36
															1024		113	494	20
Data	4E	00	C2*	FC	4E	00	A1*	FE			4E	00	A1*	FE /F8			4E	4E	

* : Include Missing Clock Bits.

Data	Clock
C2	14
A1	0A

FIG 5.2.4 WIDE ERASE FORMAT

5.2.5 MFM RULES (USE IN IBM DISKETTE 2D)

The data bit is written where the each bit will correspond to the center of the bit sell with "1". The clock bit is written at the head of the bit cell with "0" whose previous bit cell has "0".

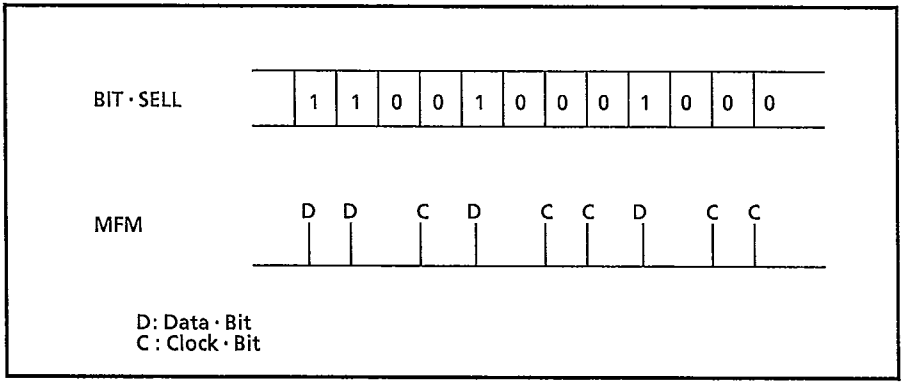


FIG.5.2.5 MFM RULES

5.2.6 COMMAND TABLE

(X : Don't care)

READ DATA COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	MT	MFM	SK	0	0	1	1	0	Command code
		×	×	×	×	×	HS	DS1	DS0	
		C								*
		H								*
		R								*
		N								*
		EOT								* ID information of starting sector of command execution
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* * ID information of
		H								* end sector of
		R								* command
		N								* execution

WRITE DATA COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	MT	MFM	0	0	0	1	0	1	Command code
		×	×	×	×	×	HS	DS1	DS0	
		C								*
		H								*
		R								*
		N								*
		EOT								* ID information of starting sector of command execution
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* * ID information of
		H								* end sector of
		R								* command
		N								* execution

WRITE DELETED DATA COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	MT	MFM	0	0	1	0	0	1	Command code
		×	×	×	×	×	HS	DS1	DS0	
		C								*
		H								*
		R								*
		N								*
		EOT								* ID information of starting sector of command execution
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* * ID information of
		H								* end sector of
		R								* command
		N								* execution

READ DELETED DATA COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	MT	MFM	SK	0	1	1	0	0	Command code
		×	×	×	×	×	HS	DS1	DS0	
		C								*
		H								*
		R								*
		N								*
		EOT								* ID information of starting sector of command execution
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* * ID information of
		H								* end sector of
		R								* command
		N								* execution

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READ DIAGNOSTIC COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	0	MFM	0	0	0	0	1	0	Command code
		×	×	×	×	×	HS	DS1	DS0	
		C								*
		H								*
		R								R = No meaning
		N								*
		EOT								* ID information of starting sector of command execution
		GPL								
		DTL								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								* * ID information of
		H								* end sector of
		R								* command
		N								* execution

READ ID COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	0	MFM	0	0	1	0	1	0	Command code
		×	×	×	×	×	HS	DS1	DS0	
E										
R	R	ST0								
		ST1								
		ST2								
		C								* * ID information
		H								* which read out
		R								* during execution-
		N								* phase

FORMAT COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	0	MFM	0	0	1	1	0	1	Command code
		×	×	×	×	×	HS	DS1	DS0	
		N								
		SC								
		GPL								
		D								
E										Data transfer
R	R	ST0								
		ST1								
		ST2								
		C								*
		H								*
		R								* * = No meaning
		N								

SEEK COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	0	0	0	0	1	1	1	1	Command code
		×	×	×	×	×	×	DS1	DS0	
		NCN								
E										Seek

RECALIBRATE COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	0	0	0	0	0	1	1	1	Command code
		×	×	×	×	×	×	DS1	DS0	
E										RECALIBRATE

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SENSE INTERRUPT COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	0	0	0	0	1	0	0	0	Command code
R	R	ST0								
		PCN								

SPECIFY COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	0	0	0	0	0	0	1	1	Command code
		SRT				×	×	×	×	
		×	×	×	×	×	×	×	ND	

SENSE DEVICE STATUS COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	0	0	0	0	0	1	0	0	Command code
		×	×	×	×	×	HS	DS1	DS0	
R	R	ST3								

CONFIG COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	0	0	0	1	0	0	1	0	Command code
		×	×	×	×	×	×	WG	FMT	

INVALID COMMAND

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
C	W	The other command code								
R	R	ST0								ST0 = 80H

TABLE 5.2 SYMBOLS in the COMMAND TABLE (1/2)

SYMBOL	NAME	DESCRIPTION
C	Cylinder Number	Indicates the cylinder number.
D	Data	Indicates the data pattern which is going to be written into data field.
D7-D0	Data Bus	8 bit data bus , D7 is MSB and D0 is LSB.
DS1, 0	Drive Select	Indicates the drive number (0, 1, 2, 3).
DTL	DATA Length	IF N = 00, indicates the data length per sector which is going to be processed.
EOT	End of Track	Indicates the last Sector of a cylinder.
FMT	Format	Indicates whether IBM format or pre-erase format is used.
GPL	Gap Length	Indicates the length of Gap 3 (see 5.2.4 Track Format).
H	Head Address	Indicates the logical head address.
HS	Head Select	Indicates the physical head address.
MFM	MFM mode	If "Low", FM mode is selected. If "High", MFM mode is selected.
MT	Multi Track	If "High", multi track operation is to be performed.
N	Number	N is the code which indicates the number of data bytes written in a sector.
NCN	New Cylinder Number	Indicates the new cylinder number to be reached as a result of the seek operation.
ND	Non-DMA	Indicates the Non-DMA mode. Defined by the Specify Command.
PCN	Present Cylinder Number	Indicates the cylinder number when the Sense Interrupt Status Command has completed.
R	Record	Indicates the sector number.
R/W	Read/ Write	Indicates whether Read or Write.
SC	Sector	Indicates the number of sector per cylinder.
SK	Skip	Indicates the skip of the sector which has DDAM or DAM.

TABLE 5.2 SYMBOLS in the COMMAND TABLE (2/2)

SYMBOL	NAME	DESCRIPTION
SRT	Step Rate Time	Indicates the step rate of FDD which is defined by Specify Command.
STP	Step	In scan operation, when STP is set to "1", sector's are processed continuously. When STP is set to "2", sector's are processed one by one.
PFD	Per-pendicular (Vertical) FDD	The drive which has wide pre-erase head system.
MFD	Conven-tional FDD	The drive which has tunnel-erase or straddle-erase hard system.
WG	Write Gate Timing	Indicates the timing of Write Gate during write operation.

5.2.7 COMMAND DESCRIPTION

During the Command-Phase, the CPU must examine the Main Status Register before the writing of the each data byte into the Data Register. The DIO and RQM in the Main Status Register must be in a low level and a high level, respectively, before each byte is written into the FDC.

READ DATA COMMAND

The FDC needs nine data bytes in order to execute the read data command. After the read data command has been issued, the FDC begins to search ID address marks and read ID fields. If ID information stored in the ID register agrees with ID information in ID field read from the diskette, then the FDC outputs data from the data field byte-by-byte to the main system via the data bus.

After the read operation of the current sector has been completed, the sector number (R) is incremented by one, the FDC reads the data from the next sector, and outputs the data on the data bus.

This continuous read function is called a "Multi-Sector Read Operation". The read data command may be terminated by receiving a terminal count (TC) signal. If the FDC receives a TC signal, the FDC stops outputting data to processor, but continues to read data from the current sector, and checks the CRC (Cyclic Redundancy Code) bytes, and then terminates the read data command at the end of the sector.

The amount of data which can be handled with a single command to the FDC depends on MT (Multi-Track), MFM (MFM/FM), and N (Number of bytes/sector). The transfer capacity is shown in TABLE 5.2.7a below.

TABLE 5.2.7a

MT	MFM	N	MAXIMUM TRANSFER CAPACITY		FINAL SECTOR	
			BYTES/ SECTOR	NUMBER OF SECTOR		
0	0	00	128	26	Side 0	Sector 26 or
	1	01	256		Side 1	Sector 26
1	0	00	128	52	Side 1	Sector 26
	1	01	256			
0	0	01	256	15	Side 0	Sector 15 or
	1	02	512		Side 1	Sector 15
1	0	01	256	30	Side 1	Sector 15
	1	02	512			
0	0	02	512	8	Side 0	Sector 8 or
	1	03	1024		Side 1	Sector 8
1	0	02	512	16	Side 1	Sector 8
	1	03	1024			

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The FDC can read out the data from both sides of the diskette by the Multi-Track function. Data transfer will be performed from the Sector 1 of Side 0 to the last Sector of Side 1 for a particular cylinder at a time. But this function is effective to only one cylinder of the diskette.

After the reading out of the last sector, the FDC must receive the terminal count. If the FDC does not receive the terminal count signal, then the FDC sets the EN (end of cylinder) flag of ST1 to a high level and terminates the read data command (bits 7 and 6 of ST0 is also set to a low level and a high level respectively : abnormal termination).

When N = 0, DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the data bus, but the FDC reads the whole sector internally, and then checks CRC bytes. When N ≠ 0 DTL has no meaning.

If the FDC can not find out the right sector until the FDC detects the index hole twice, and the FDC sets the ND (No Data) flag in ST1 to a high level, and the read data command will be abnormal terminated (bit 7 and bit 6 in ST0 set to a low level and a high level respectively).

After the reading of the ID field and the data field of the each sector, the FDC checks the CRC bytes. If a read error (incorrect CRC bytes in the ID field) is detected, the FDC sets the DE (Data Error) flag of ST1 to a high level, and if data error in the data field is detected, the DD (Data Error in Data Field) flag in ST2 is set to a high level, and then the read data command is abnormal terminated.

If the FDC read a deleted data address mark in the diskette, and SK bit (D5 bit in the command code) is not set, then the FDC sets CM (Control Mark) flag to a high level after reading out all the data in the sector, and terminates the read data command. When SK = 1, the FDC skips the sector that has DDAM, and read out the next sector.

During the data transfer between the FDC and the processor, the FDC must receive the service from the processor within 7.9μs at the mode of Perpendicular Magnetized FDD, within 13μs in MFM mode and 27μs in FM mode at the mode of Standard FDD. If the FDC does not receive this service in time, the FDC sets OR (Over Run) flag to a high level, and terminates the read data command (abnormal termination).

If a read (or write) operation is terminated by inputting the terminal count signal, the information of Result-Phase is defined by MT bit and EOT byte. TABLE 5.2.7b shows the value for C, H, R and N when the command is normally terminated.

5.2.7b ID INFORMATION AT NORMAL TERMINATION

MT	EOT	FINAL TRANSFERRED SECTOR	ID INFORMATION IN RESULT-PHASE			
			C	H	R	N
0	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	C + 1	NC	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	NC	R = 01	NC
1	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	NC	LSB	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	LSB	R = 01	NC

NOTE : NC (No Change) : The same value as the one at the beginning of command execution.
LSB (Least Significant Bit) : The least significant bit of H is complemented.

FLOPPY DISK CONTROLLER

WRITE DATA COMMAND

The FDC needs nine data bytes in order to execute the write data command. If the write data command has been issued, the FDC begins to read the ID field. If the sector number stored in ID register (IDR) matched with the sector number read from the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs to the FDD.

After the writing the data into the current sector, the FDC increments the sector number stored in R by one, and then the FDC writes the next data field. The FDC continues this Multi-Sector write operation until the terminal count signal is issued. Even if the FDC has received the terminal count signal, the FDC continues writing for the sector, and the data field will be completed. If the FDC receives the terminal count signal while the FDC is writing data in data field, then the remained data field will be filled with 00.

The FDC reads out the each sector of ID field, and checks the CRC bytes. If the FDC finds out the Read Error in ID field (incorrect CRC bytes), the FDC sets DE (Data Error) of ST1 to a high level, and terminates the write data command (abnormal termination).

The rules of the write commands are much similar to the rules of the read data command. The following items are same, see the previous section READ DATA COMMAND.

- ☐ Transfer Capacity
- ☐ EN flag
- ☐ ID information at the normal termination
- ☐ Meaning of DTL when N = 0 and when N ≠ 0

During the execution of the write data command, the data transfer between the processor and the FDC must be performed within 7.0μs at the mode of Perpendicular Magnetized FDD, within 14μs in MFM mode and 29μs in FM mode at the mode of Standard FDD. If it is not performed, the FDC sets OR flag of ST1 to a high level, and terminates the command (abnormal termination).

WRITE DELETED DATA COMMAND

This command is the same command as the write data command except that the FDC writes the DDAM (Deleted Data Address Mark) at the beginning of the data field instead of the normal DAM (Data Address Mark).

READ DELETED DATA COMMAND

This command is the same as the read data command except that the FDC reads the sectors with DDAM instead of those with DAM at the beginning of a data field. If the FDC detects DAM and SK = 0, then the FDC will read the whole sector and set CM flag in ST2 to a high level and terminate the command (normal termination). If the FDC finds out DAM and SK = 1 then the FDC will skip the sector with DAM and read the next sector.

READ DIAGNOSTIC COMMAND

This command is the same as the read data command except that the FDC reads all the data continuously from each sector of a track. Just after the FDC receives the index signal, the FDC begins to read out all the data field on the track as a continuous block. Even if the FDC finds out the CRC error in ID or data field, the FDC continues to read data from the track. The FDC compares the ID information read out from each sector with the value stored in IDR, and if there is no comparison, the FDC sets ND flag to a high level. This command has neither the Multi-Track function nor the skip function.

This command will be terminated when EOT number of sectors have been read out. When ID address mark on the diskette is not found out until the FDC finds out the index hall twice, MA (Missing Address Mark) in ST1 is set to a high level, and the command is terminated (abnormal termination).

READ ID COMMAND

This command is used to inform the processor of the current head point. The FDC stores the first ID information to be read out. If the right ID address mark is not found on the diskette until the FDC finds out the index hall twice, the FDC sets MA flag in ST1 to high level, and if there is no ID field without CRC error, ND flag in ST1 is set to a high level, and the command is terminated (abnormal termination).

FORMAT COMMAND

The format command allows an entire track to be formatted. After the index hall is detected, the FDC writes data on the diskette. Gaps, address marks, ID fields and data fields on IBM system 34 (double density) or IBM system 3740 (single density) or pre-erase format are recorded. The particular format is controlled by the values programmed in N, SC, GPL and D during the command-phase. The data byte stored in D is written into the processor. That is, the FDC requests four data bytes per sector for C, H, R and N. This function allows the diskette to be formatted with non-sequential sector numbers.

After the each sector is formatted, the processor must send the new values of C, H, R and N to the FDC for the next sector on the track. After a sector is formatted, the contents of the R-register is incremented by one. Thus, when the R register is read out during the result-phase, it contains a value of R+1. This incrementing and formatting continues for the track until the FDC detects the index hall for the second time. When the FDC finds the index hall twice, the command is terminated.

If the ready signal changes to a low level at the beginning of the command execution, then the command is terminated. TABLE 5.2.7c shows the relationship of N, SC and GPL for various sector sizes.

TABLE 5.3.7c RELATIONSHIP of SECTOR SIZES

FORMAT	SECTOR SIZE BYTE / SECTOR	N (16)	N (16)	N (16)	REMARKS
IBM Format FM mode	128	00	1A	1B	IBM Diskette 1
	256	01	0F	2A	IBM Diskette 2
	512	02	08	3A	
	1024	03	04	–	
	2048	04	02	–	
	4096	05	01	–	
IBM Format MFM mode	256	01	1A	36	IBM Diskette 2D
	512	02	0F	54	
	1024	03	08	74	IBM Diskette 2D
	2048	04	04	–	
	4096	05	02	–	
	8192	06	01	–	
Pre-erese Format	256	01	3D	3E	Vertical FDD MFM mode
	512	02	24	53	
	1024	03	14	71	

*Note : GPL defines the length of GAP placed just after each sector.

SEEK COMMAND

This command is used to move the read/write head from cylinder to cylinder. The FDC compares the PCN which is current head position with the NCN. If there is a difference, the FDC performs the following operation.

PCN < NCN : Direction signal to the FDD is set to a high level (LA=low), and the step pulses are issued (Step in).

PCN > NCN : Direction signal to the FDD is set to a low level (LA=low), and the step pulses are issued (Step out).

The rate of outputting the step pulses is controlled by the SRT (step rate pulse) in the specify command. The FDC compares NCN with PCN at outputting the step pulses, and if NCN=PCN, then SE (seek end) flag in ST0 is set to a low level, and the command is terminated. The FDC is in FDC busy state during the command-phase of this command, but the FDC is in non-busy state, the FDC accepts another seek command. This function allows the FDC to do the parallel seek operation for up to 4 FDDs at a time.

If the FDD is in the not ready state at the beginning of the execution-phase of this command or during the seek operation, the NR (not ready) flag in ST0 is set to a high level and the command is terminated.

RECALIBRATE COMMAND

The read/write head within the FDD is moved to the track 0 position under control of the recalibrate command. The FDC clears the contents of PCN register, and checks the track 0 signal. If the track 0 signal is in a low level, the FDC sets the direction signal to a low level, and issues the step pulses.

When the track 0 signal changes to a high level, the FDC sets SE (seek end) flag to a high level, and terminates the command. If the track 0 signal is still low after the FDC has issued the 255 step pulses, SE flag and EC flag in ST0 are set to both high levels, and the command is terminated. The recalibrate command is the same as the seek command about the function to overlap the operation to multiple FDDs and about the loss of the ready signal.

SENSE INTERRUPT STATUS COMMAND

The FDC generates the interrupt signal by the following reasons.

(1) The beginning of result-phase in the following commands :
   a. Read Data Command
   b. Read Diagnostic Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   g. Write Deleted Data Command

(2) The change of ready line of FDD.

(3) At the end of the Seek or Recalibrate Command

(4) During the execution-phase in the non-DMA mode.

Interrupts caused by reason 1 and 4 occur during the normal command operation, and the processor can notice the interrupts easily. But the interrupts caused by the reason 2 and 3 may be identified with the request of issuing the sense interrupt status command. When this command is issued, interrupt signal is reset, and bit 5, bit 6 and bit 7 in ST0 indicate the reason of the interrupt.

FLOPPY DISK CONTROLLER

TABLE 5.2.7d SEEK AND INTERRUPT CODE

INTERRUPT CODE		SEEK END	MEANING
BIT 7	BIT 6	BIT 5	
1	1	0	Changing of the state of the Ready Line
0	0	1	Normal termination of the Seek and Recalibrate Command
0	1	1	Abnormal termination of the Seek and Recalibrate Command

Neither the seek nor the recalibrate command has a result-phase. Therefore, it is necessary to use the sense interrupt command after these commands in order to terminate them effectively and confirm the head position (PCN).

SPECIFY COMMAND

This specify command initializes the values of internal timer. The SRT defines the time interval between step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F = 1ms, E = 2ms,....,0 = 16ms).

The interval times mentioned above are a direct function of the clock. The times indicated above are for a 8MHz clock. If the clock frequency is 4MHz (mini floppy), all the times are twice as long as the times indicated above. If the clock frequency is 16MHz (Perpendicular Magnetized Floppy), all the times are half as long as the times indicated above. The ND bit is a flag to select the DMA operation or non-DMA operation. If ND is in a high level then non-DMA mode is selected, and if ND is in a low level then DMA mode is selected.

SENSE DEVICE STATUS COMMAND

The processor may use this command whenever it wishes to know the status of the FDDs. The drive status information is contained in ST3.

CONFIGURATION COMMAND

This command is used to select the data format and write gate timing. The FMT bit indicated the data format. When this bit is "1" pre-erase format is selected, and standard IBM format is selected when this bit is "0".

The WG bit indicates the write gate timing. When this bit is "1" the timing for pre-erase head is selected. In this case write gate is activated after 3 byte following ID area. When this bit is "0" conventional timing is selected. In this case write gate is activated from SYNC area. Default value of these bits are "0" (Conventional FDD).

TABLE 5.2.7e FMT/WG VALUE vs. DRIVE/MEDIA COMBINATIONS

DRIVE	MEDIA	FMT	WG
Perpendicular Magnetized FDD	Perpendicular Magnetized FDD	1	1
	Conventional FDD	0	1
Conventional FDD	Conventional FDD	0	0

INVALID COMMAND

If an invalid command (a command not defined above) is send to the FDC, the FDC terminates the command. The FDC does not generate the interrupt signal during the Result-Phase. Bit 6 and bit 7 in the main status register set to both high levels indicates to the processor that the FDC is in the Result-Phase and that the contents of ST0 must be read out. ST0 is set to a 80H showing that an invalid command was received.

The sense interrupt status command must be sent after and interrupt of the seek command or recalibrate command has occurred, otherwise the FDC regards this command as invalid. The users may use this command as a non-Op command to place the FDC in a stand-by or non-operation state.

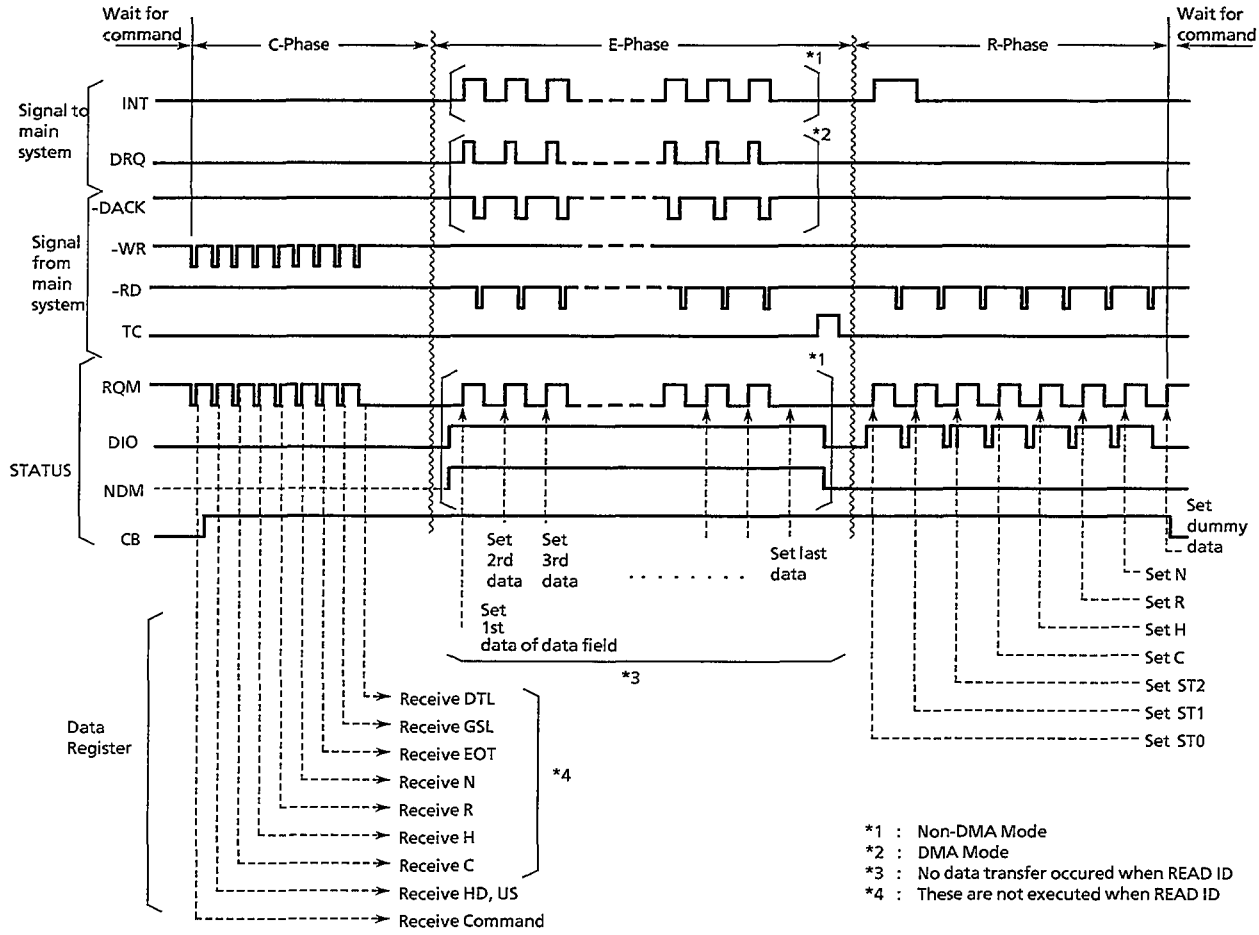


FIG.5.2a READ DATA, READ DELETED DATA, READ DIAGNOSTIC, READ ID

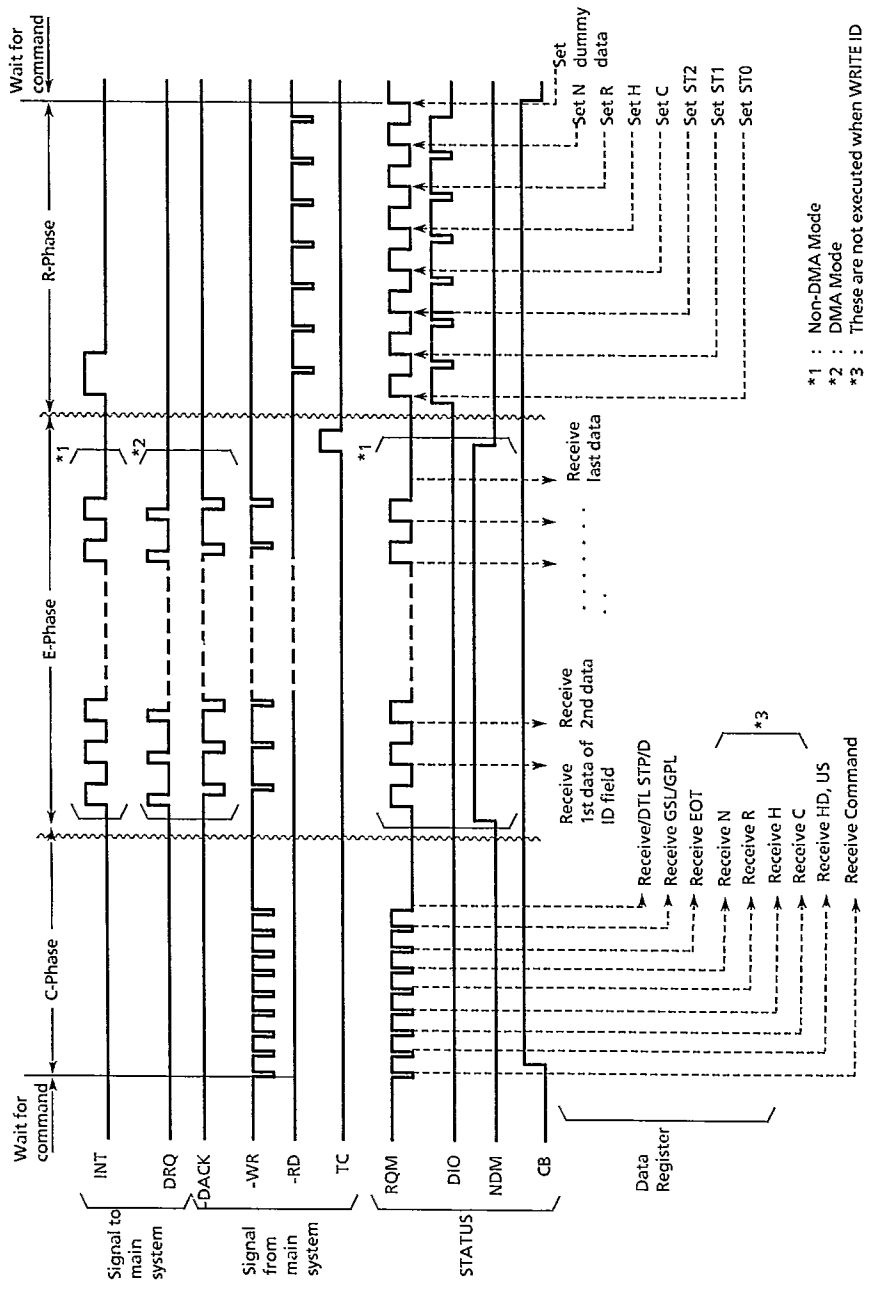


FIG 5.3b WRITE DATA, WRITE DELETED DATA, WRITE ID

FLOPPY DISK CONTROLLER

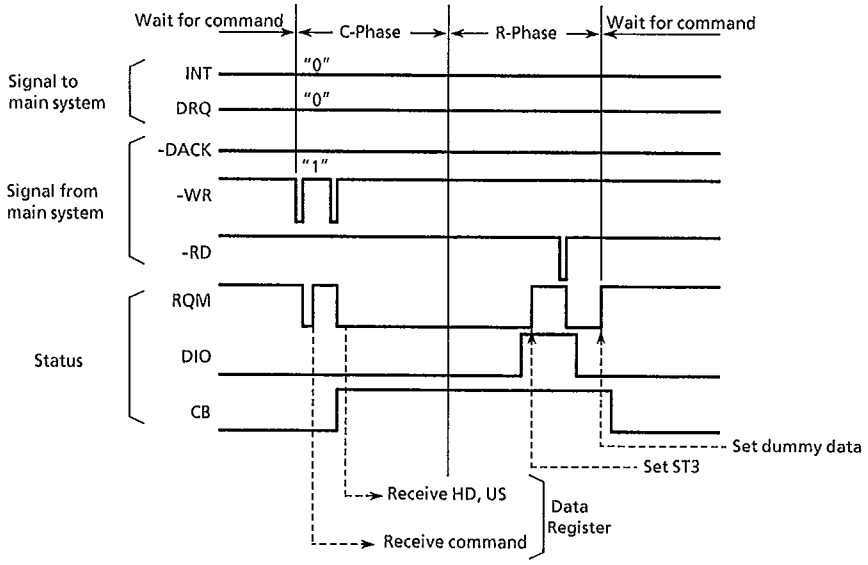


FIG 5.3c SENSE DEVICE STATUS

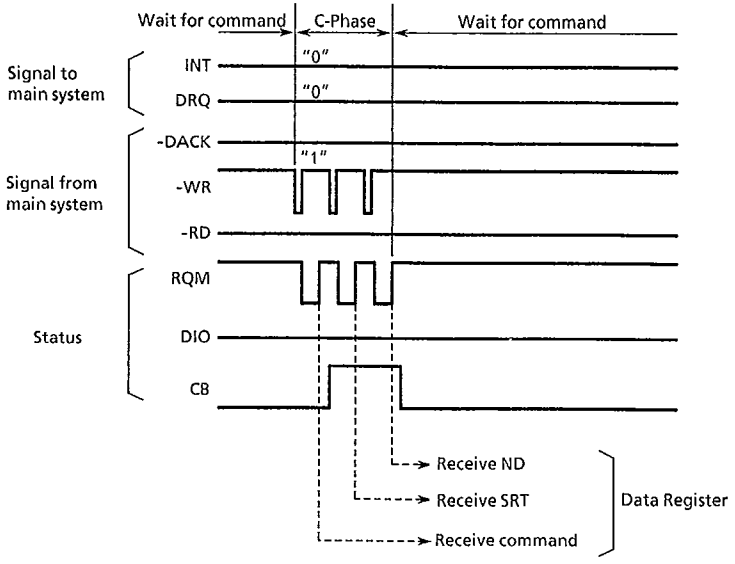


FIG 5.3d SPECIFY

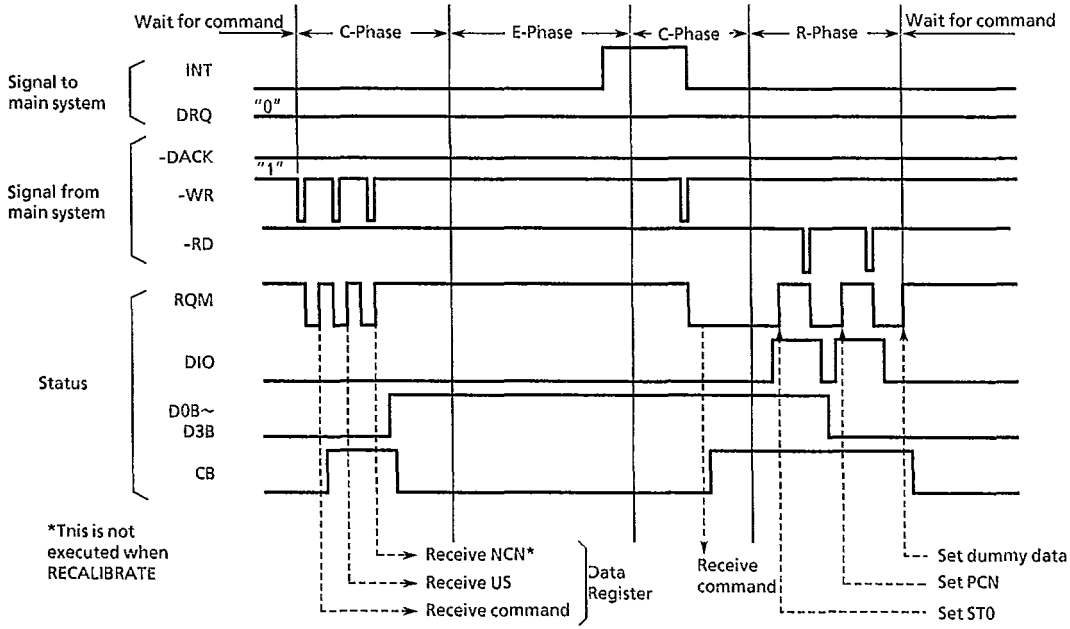


FIG 5.3e SEEK, RECALIBRATE & FIG 5.3f SENSE INTERRUPT STATUS

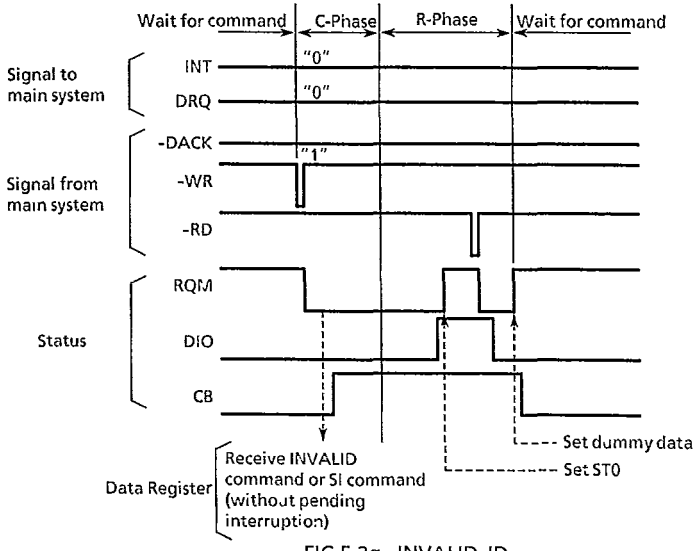


FIG 5.3g INVALID ID

FLOPPY DISK CONTROLLER

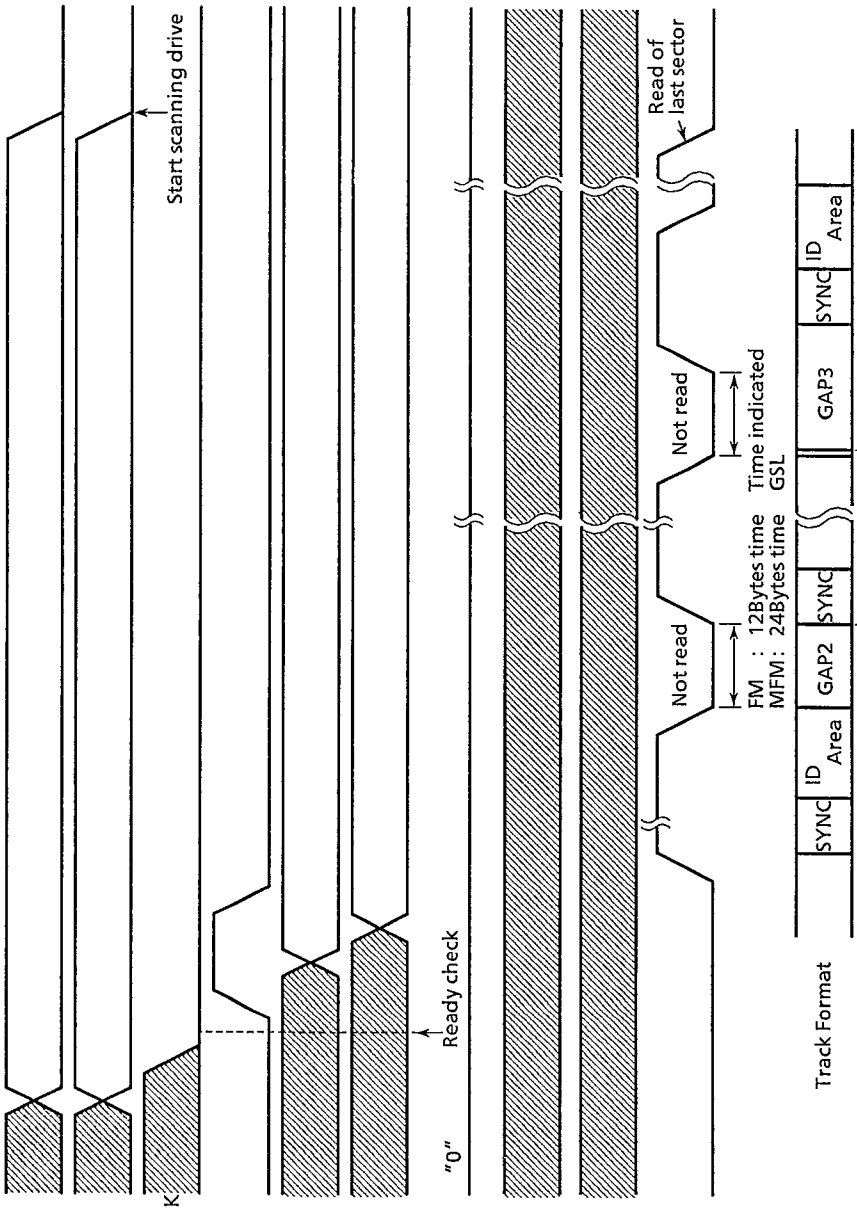


FIG 5.3h READ DATA, READ DELETED DATA, READ DIAGNOSTIC READ ID

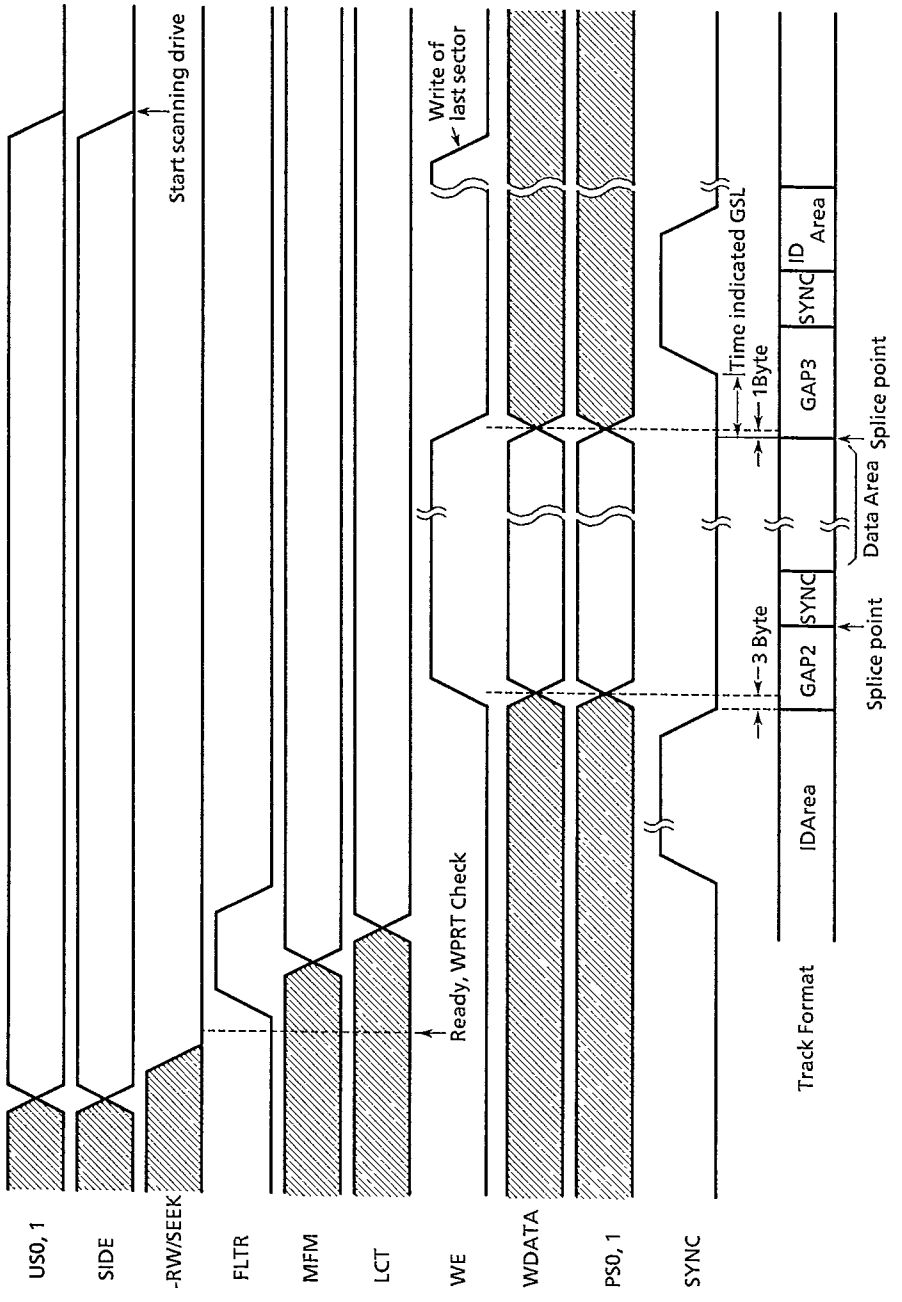


FIG 5.3i WRITE DATA, WRITE DELETED DATA (PFD)

FLOPPY DISK CONTROLLER

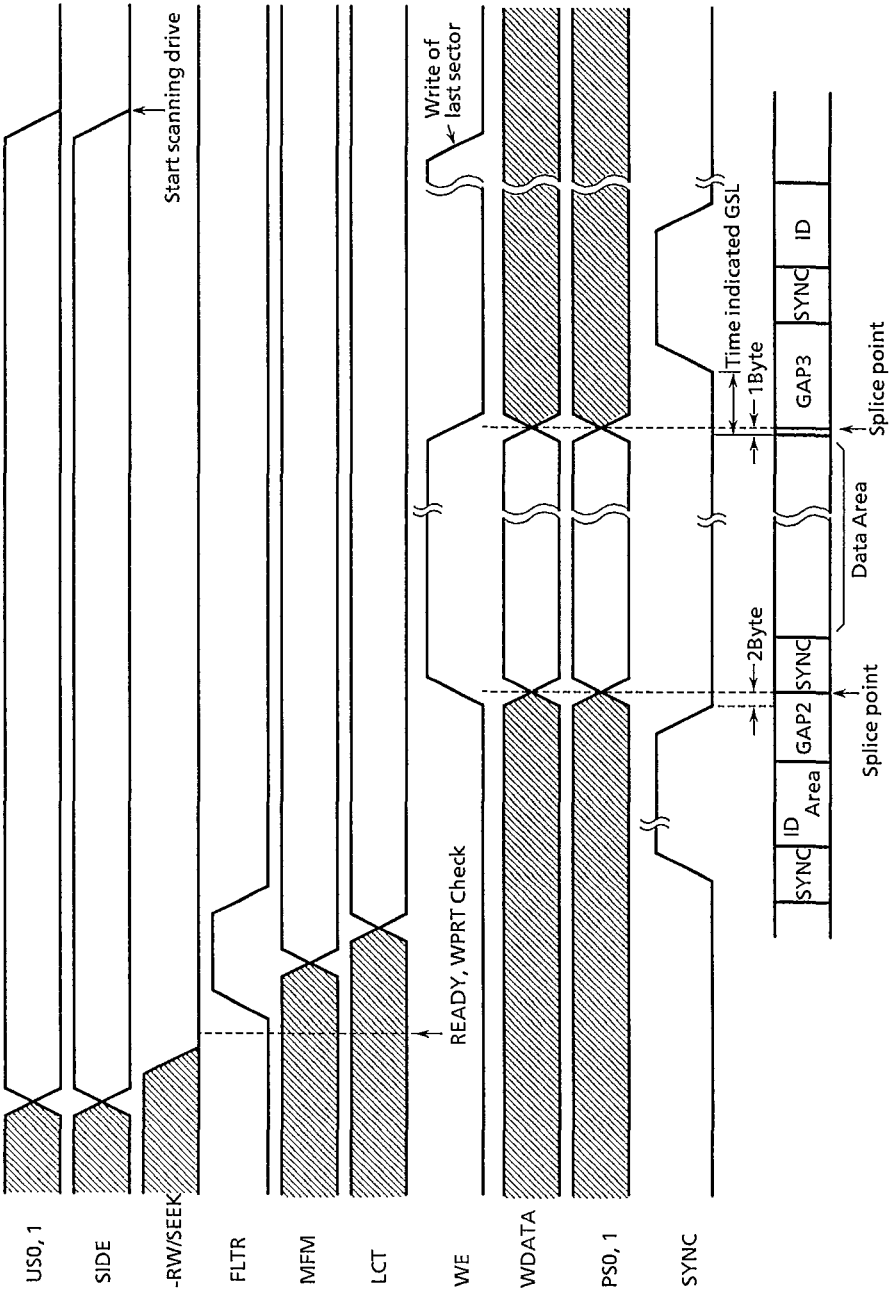


FIG 5.3j WRITE DATA, WRITE DELETED DATA (MFD)

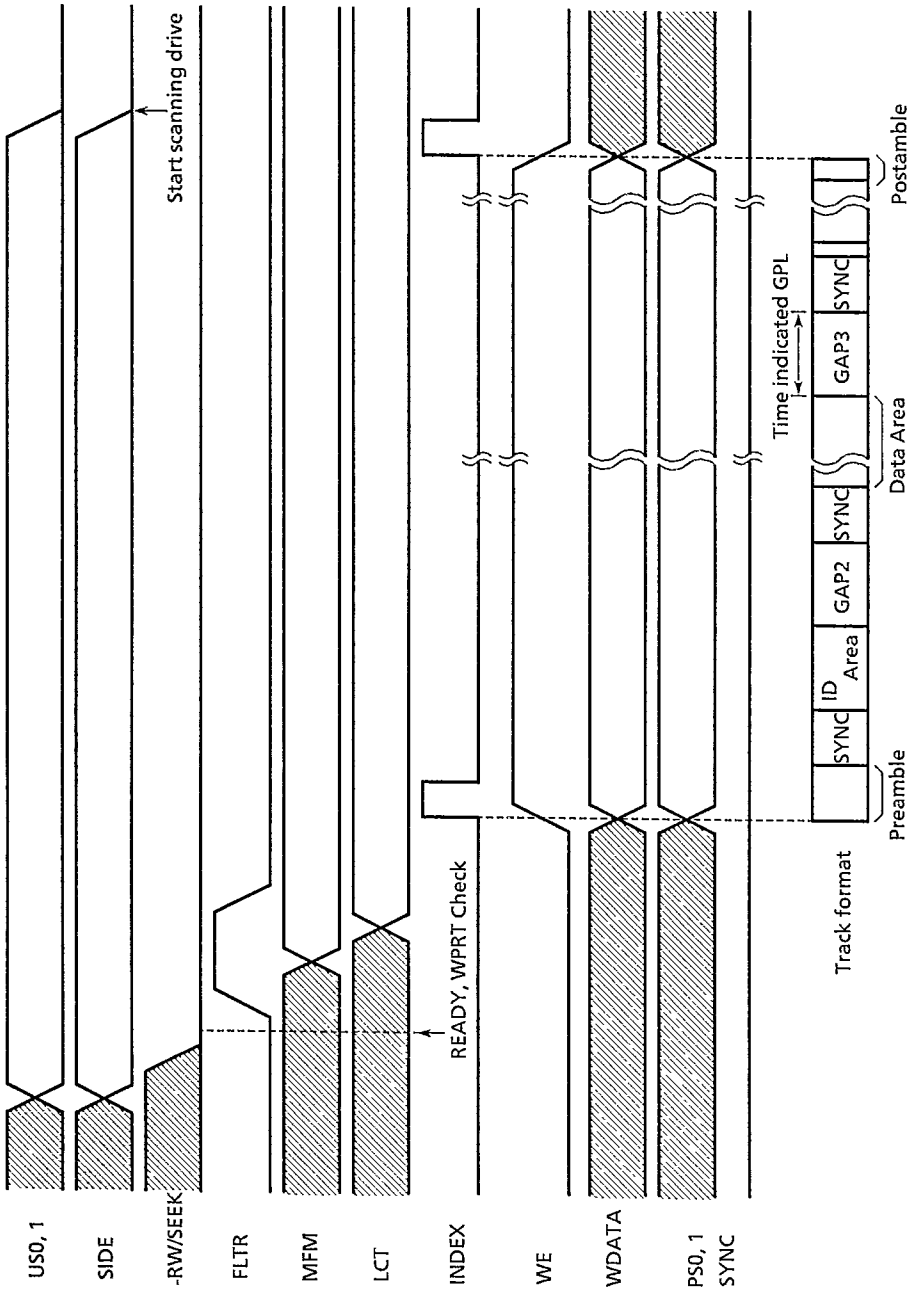
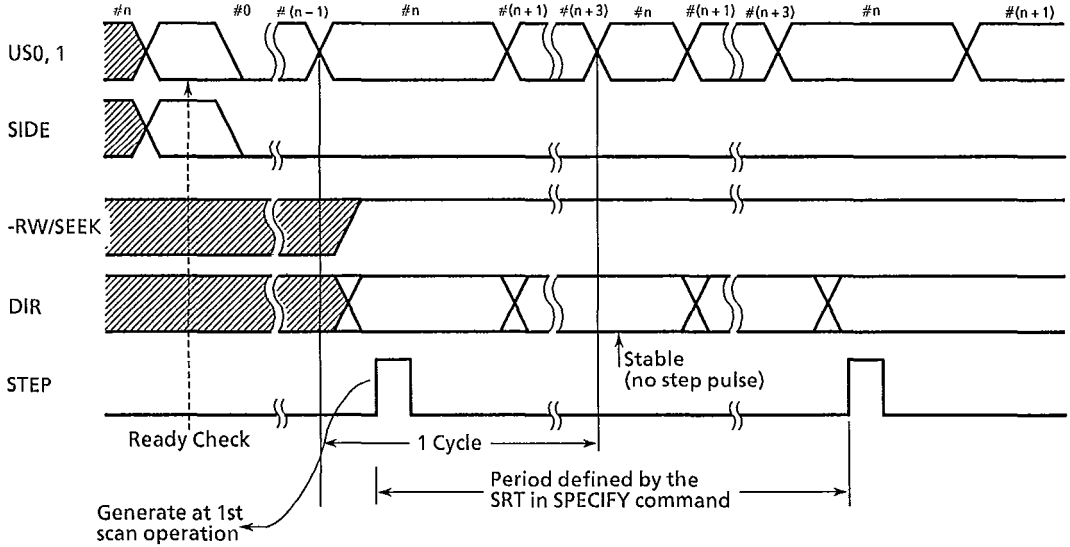


FIG 5.3k WRITE ID

FLOPPY DISK CONTROLLER



- #n means the drive number which is assigned by US0, 1
  (Drive number is 0 to 3, so that, n = 3 then n + 1 means 0)
- The READY check is done to the drive which assigned by US0, 1

FIG 5.3l SEEK, RECALIBRATE

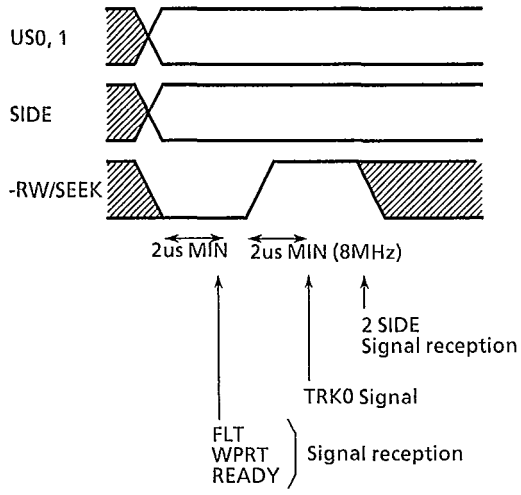


FIG 5.3m SENSE DEVICE STATUS

5.2.8 RESULT STATUS REGISTER

RESULT STATUS REGISTER 0 (ST0)

BIT	SYMBOL	NAME	DESCRIPTION
D7 D6	IC	Interrupt code	D7 = 0 and D6 = 0 Normal termination of command (NT), command was completed and properly executed.
			D7 = 0 and D6 = 1 Abnormal termination of command (AT). Command execution was started, but was not successfully completed.
			D7 = 1 and D6 = 0 Command was invalid command (IC). The command which has been issued was not started.
			D7 = 1 and D6 = 1 Abnormal termination because of the changing of the ready line from the FDD during the execution of command.
D5	SE	Seek End	This flag is set to a "1", when the seek command was completed.
D4	EC	Equipment Check	When the track 0 signal was not set to a "1" after 255 step pulses during the recalibrate command, this flag is set to a "1".
D3	NR	Not Ready	When the FDD is in the not-ready state and a read/write command is issued, this flag is set. For example, when a read/write command is issued for side 1 of a signal sided drive, this flag is set.
D2	HD	Head Select	This flag indicates the state of the head at interrupt.
D1 D0	DS1 DS0	Drive Select 0,1	These flags indicate the drive number at interrupt.

FLOPPY DISK CONTROLLER

RESULT STATUS REGISTER 1 (ST1)

BIT	SYMBOL	NAME	DESCRIPTION
D7	EN	End of Cylinder	This flag is set when the FDC tries to access a sector beyond the last sector of a cylinder.
D6	–		
D5	DE	Data Error	This flag is set when the FDC finds the CRC error either in the ID field or the data field.
D4	OR	Over Run	This flag is set when the FDC does not receive the service from the main system during data transfers within a certain time interval.
D3	–		
D2	ND	No Data	☐ This flag is set when the FDC can not find out the sector specified in the IDR during the execution of following commands. READ DATA READ DELETED DATA WRITE DATA WRITE DELETED DATA ☐ This flag is set when the FDC can not find the ID field without the CRC error during the execution of the READ ID COMMAND. ☐ This flag is set when the starting sector cannot be found during the executing the READ DIAGNOSTIC COMMAND.
D1	NW	Not Writable	This flag is set if the FDC detects the write protect signal from the FDD durig the executing folowing commands. WRITE DATA WRITE DELETED DATA FORMAT
D0	MA	Missing Address Mark	☐ This flag is set if IDAM cannot be found out until the FDC finds the index hall twice. ☐ This flag is set if the FDC cannot find the DAM or DDAM. The MD flag of ST2 is also set in this case.

RESULT STATUS REGISTER 2 (ST2)

BIT	SYMBOL	NAME	DESCRIPTION
D7	–		
D6	CM	Control Mark	While executing the READ DATA, this flag is set when the FDC finds out the sector with the DDAM. During executing the READ DELETED DATA COMMAND, this flag is set when the FDC finds out the sector with the DAM.
D5	DD	Data Error in Data Field	This flag is set when the FDC detects a CRC error in data field.
D4	NC	No Cylinder	This flag is set when the contents of C on the medium is differrent from that stored in the IDR. This flag is related with the ND flag.
D3	–		This bit has no meaning.
D2	–		This bit has no meaning.
D1	BC	Bad Cylinder	This flag is set if the content of C on the medium is FF and differs from that stored in IDR. This bit is related with the ND bit.
D0	MD	Missing Address Mark in Data Feld	This flag is set if the FDC cannot find out the DAM or DDAM while the data are read from the medium.

RESULT STATUS REGISTER 3 (ST3)

BIT	SYMBOL	NAME	DESCRIPTION
D7			This bit has no meaning.
D6	WP	Write Protect	This bit indicates the state of the write protect signal from the FDD.
D5	RDY	Ready	This bit indicates the state of the ready signal from the FDD.
D4	TK0	Track 0	This bit indicates the state of the track 0 signal from the FDD.
D3			This bit has no meaning.
D2	HD	Head Address	This bit indicates the state of the head select signal to the FDD.
D1	DS1	Drive Select 1	This bit indicates the state of the drive select 1 signal to the FDD.
D0	DS0	Drive Select 0	This bit indicates the state of the drive select 0 signal to the FDD.

5.3 VFO UNIT

5.3.1 VFO UNIT BLOCK DIAGRAM

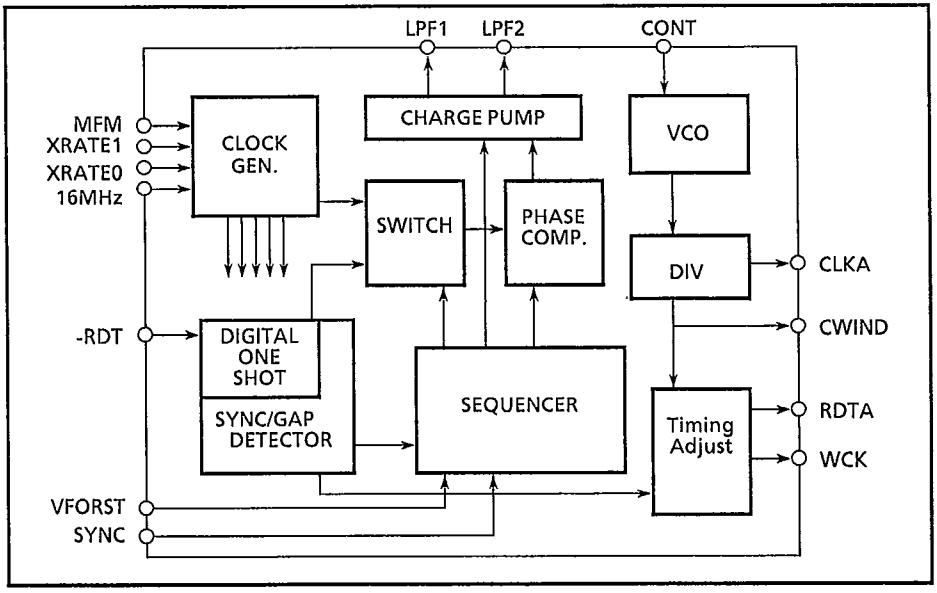


FIG.5.3.1 VFO BLOCK DIAGRAM

5.3.2 DESCRIPTION OF EACH BLOCKS

(1) Time base generator/Divider circuit

This block consists of 16MHz crystal oscillator and divider. It generates all timing signals for VFO operation. The operation mode MFM and MIN signals change the divisor of these timings.

XRATE0	XRATE0	FLOPPY MODE	MODULATION	fDW (KHz)
0	0	Standard Floppy	MFM	500
			FM	250
0	1	–	–	–
1	0	Mini Floppy	MFM	250
			FM	125
1	1	Vertical Floppy	MFM	1000
			FM	

(2) Sync gap detector/digital one-shot

SYNC pattern detect circuit when the FDC begins the read operation. SYNC pattern "00" is continuance pulse series whose interval is TSYNC. This circuit judges to be SYNC the pulse series whose interval is within TSYNC, and the other pulse series to be GAP. When 16MHZ clock is applied in [XIN] terminal, the value of TSYNC are as follows.

XRATE0	XRATE0	FLOPPY MODE	MODULATION	TSYNC (μs)
0	0	Standard Floppy	MFM	1.68 ~ 2.25
			FM	3.38 ~ 4.93
0	1	–	–	–
1	0	Mini Floppy	MFM	3.38 ~ 4.93
			FM	6.80 ~ 10.0
1	1	Vertical Floppy	MFM	~ 1.20
			FM	

(3) Voltage Controlled Oscillator (VCO)

This VCO is automatically adjust its center frequency using PLL circuit. When 16MHz is used for [XIN] clock, 2MHz is the frequency at VCONT voltage is 2.5V. The conversion gain via voltage on VCONT terminal is as follows.

$K_V = 2.5 \times 10^6$ [rad/sec V]

(4) Timing Adjusting Circuit

This circuit regenerates data and clock bit in MFM signal so as to get best read margin against the peak shift phenomenon in the data from the FDD.

(5) Sequencer

VFO start its operation with the starting of read request from the FDC. The sequencer controls all operation that is, hunting SYNC pattern, detecting address mark, changing PLL filter constant etc.

5.3.3 VFO OPERATION FLOW OF VFO

The operation of the VFO part is explained as the combination of the control mode of each circuit. The mode of each part which concerns the VFO operation is as follows.

[Phase Comparator]

One input of the phase comparator is the window signal which is the divided signal of the VCO output. The other input is either the read data or standardized clock from [XIN] whose frequency is the same as window signal.

There are things to switch the charge pump outputs and to change the gain of phase comparator in order to distinguish lock state from unlock state of the VCO.

[External Input]

SYNC : Input to indicate that the FDC is in read data.

VFORST : Pulse generated by internal FDC when the FDC becomes SYNC state, and when the first data byte after sync detection is not address mark and the FDC begins to search next sync pattern.

VFO has three transition states as follows.

Q_F	VCO is tracing for basic clock from[XIN] 16MHz with high gain.
Q_H	VCO is tracing for read data with high gain.
Q_L	VCO is tracing for read data with low gain.

There is SYNC/GAP detector to control state transition except mentioned above. This circuit always checks read data pulses. If there is a pulse without regular interval time, GAP is outputted. This output is held for 8 bit time, SYNCD is outputted when there is no GAP output during 4 byte time FIG.5.3.3a shows VFO states transition flow. FIG.5.3.3b shows the timing of VFORST which the FDC outputs.

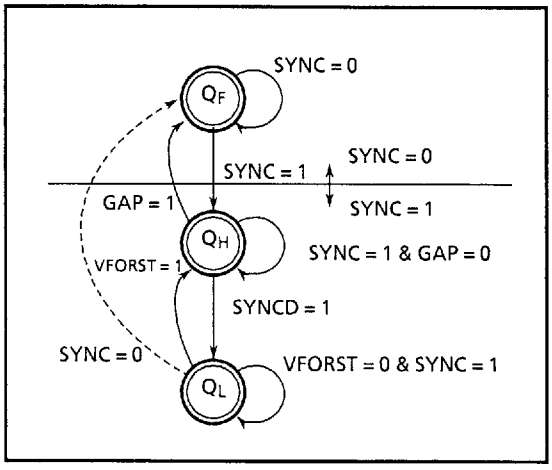


FIG.5.3.3a VFO STATUS TRANSITION

FLOPPY DISK CONTROLLER

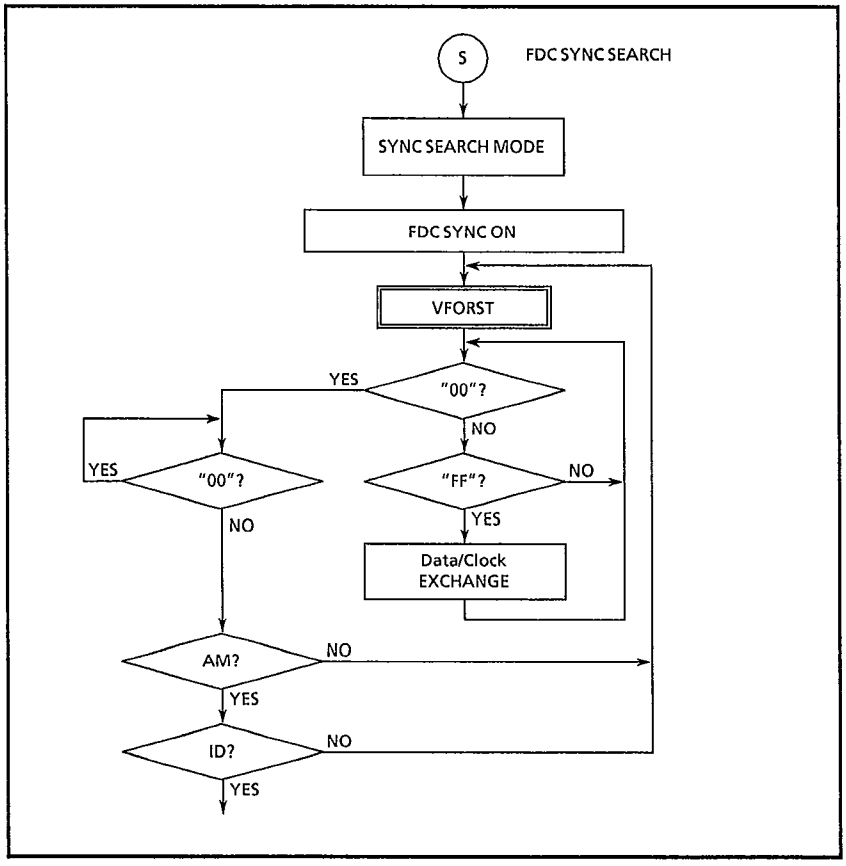


FIG.5.3.3b VFORST TIMING

5.3.4 FILTER CR CONSTANT OF VFO

When the VFO is used in the alternative filter switching mode, the external components for the low pass filter are needed as follows.

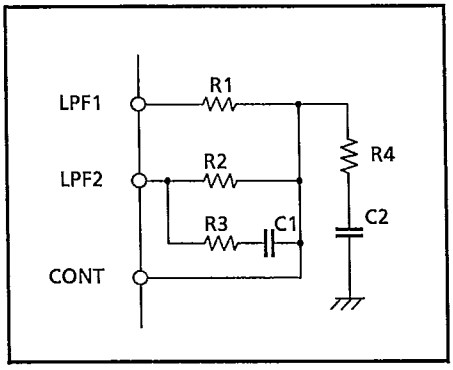


FIG.5.3.4 FILTER CIRCUIT

Recommended CR constant for 1Mbps, 500Kbps and 250Kbps is as follows. The accuracy of component is less than 5% each.

R1	1KΩ
R2	68KΩ
R3	15KΩ
R4	1KΩ
C1	1000pF
C2	0.01μF

Also, when the VFO is used in a fixed filter non-switching mode, the external components for the low pass filter are needed as follows.

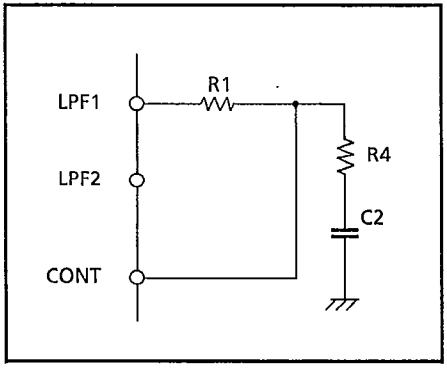


FIG.5.3.4b FILTER CIRCUIT

Recommended CR constant for MIN and STD mode is as follows.

R1	15KΩ
R4	3.9KΩ
C2	0.01μF

5.3.5 VFO TIME MARGIN

(1) Outline of time margin

Raw data being read from floppy disk drive have dynamic/static data rate variations on account of the variation in the rotational speed of disk (for example, wow flatter). On high density recording, magnetic effects cause read data to move to early or late position, which is called peak shift. Raw read data are influenced by the variation in disk speed on both writing and reading, which is regarded as low speed variation. The VFO is designed to track this variation. On the other hand, it is necessary to reduce the variation by peak shift, because its frequency is near the data transfer frequency.

Example : Waveform in case of data 6B2 in MFM mode for mini-floppy

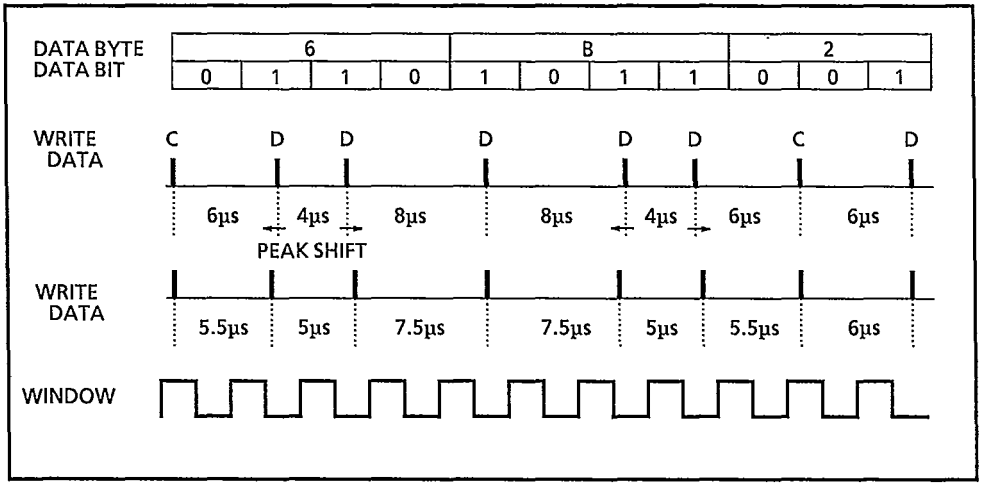


FIG.5.3.5a EXAMPLE of PEAK SHIFT

In the example above, there are +0.5µs pulse jitters by peak shift. The VFO operates to track the variation in disk rotation but to ignore the variation of this peak shift, and then generates the WINDOW signal to sample data accurately. The time margin is the tolerance for the peak shift. This value in the case of an ideal VFO is a half of the cycle of the bit transfer rate. It is 2µs in MFM mode for mini-floppy (250Kbps).

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0V (GND)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	−0.5 ~ +7.0	V
Input Voltage	V_{IN}	VSS − 0.5 ~ VDD + 0.5	V
Operating Temperature	T_{OPR}	−30 ~ +70	°C
Storage Temperature	T_{STG}	−65 ~ +125	°C
Output Current	I_{OUT1}	±2 (*1)	mA
Output Current	I_{OUT2}	±8 (*2)	mA
Output Current	I_{OUT3}	±3 (*3)	mA
Power Dissipation	P_D	300	mW

(note) If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended conditions. If these conditions are exceeded, reliability of LSI may be adversely affected.

*1 (Output terminal group 1) : XOUT
*2 (Output terminal group 2) : WDT1, WE, HS, HL, MEN0~1, DS0~1, STP, DR, MDSL0~1, LWDEN
*3 (Output terminal group 3) : The other output terminals and Data bus

6.2 RECOMMENDED OPERATING CONDITIONS

VSS = 0V (GND)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Operating Temperature	t_{OPR}		−30	+70	°C
Supply Voltage	V_{DD}		4.75	5.25	V
Clock Frequency	F_C		15.5	16.5	MHz

6.3 DC CHARACTERISTICS

TENTATIVE

VDD = 5.0V ± 5%, VSS = 0V (GND), tOPR = −30~ +70°C

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Hysteresis Width	(*2)	V_{HS2}	0.2			V
High Level Input Current	(*1)	I_{IH1}	2.5		500	μA
VIN = VDD	(*2) (*3)	I_{IH23}	−10		10	μA
Low Level Input Current	(*1)	I_{IL1}	−500		−2.5	μA
VIN = 0V	(*2) (*3)	I_{IL23}	−10		10	μA
High Level Input Voltage	(*1)	V_{IH1}	3.5		VDD	V
	(*2)	VI_{H2}	2.4		VDD	V
	(*3)	V_{IH3}	2.2		VDD	V
Low Level Input Voltage	(*1)	V_{IL1}	0		1.2	V
	(*2)	V_{IL2}	0		0.58	V
	(*3)	V_{IL3}	0		0.8	V
High Level Output Current	(*4)	I_{OH1}			−0.5	mA
VOH = VDD − 0.4V	(*5)	I_{OH2}			−3.0	mA
	(*6)	I_{OH3}			−2.0	mA
Low Level Output Current	(*4)	I_{OL1}	0.5			mA
VOL = 0.4V	(*5)	I_{OL2}	6.0			mA
	(*6)	I_{OL3}	2.0			mA
Power Supply Current	(*1)	I_{DD1}		20	40	mA
Standby Current		I_{DD2}			100	μA

*1 (Input terminal group 1) : XIN
*2 (Input terminal group 2) : Schmitt trigger input : -RDT, -IDX, -RDY, -WP, -TK0, -DSKCHG
*3 (Input terminal group 3) : The other input terminals and Data bus
*4 (Output terminal group 1) : XOUT
*5 (Output terminal group 2) : Output from FDD : WDT1, WE, HS, HL, MEN0~1, DS0~1, STP, DR, MDSL0~1, LWDEN
*6 (Output terminal group 3) : The other Output terminals and Data bus

6.4 AC CHARACTERISTICS

TENTATIVE

VDD = 5.0V ± 5%, VSS = 0V (GND), tOPR = −30~ +70°C

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock cycle time		t_{CY}	40			ns
Clock high level width		t_{CH}	20			ns
AEN setup time before -IOR		t_{AENR}	0			ns
AEN hold time after -IOR		t_{RAEN}	0			ns
-CS setup time before -IOR		t_{SR}	0			ns
-CS hold time after -IOR		t_{RS}	0			ns
Address setup time before -IOR		t_{AR}	20			ns
Address hold time after -IOR		t_{RA}	0			ns
Data delay time from -IOR		t_{RD}			100	ns
Data float delay time after -IOR		t_{DF}	20		100	ns
Pulse width of -IOW		t_{RR}	200			ns
AEN Setup time before -IOW		t_{AENW}	0			ns
AEN hold time after -IOW		t_{WAEN}	0			ns
-CS setup time before -IOW		t_{SW}	0			ns
-CS hold time after -IOW		t_{WS}	0			ns
Address setup time before -IOW		t_{AW}	20			ns
Address hold time after -IOW		t_{WA}	10			ns
Data setup time before -IOW		t_{DW}	20			ns
Data hold time after -IOW		t_{WD}	10			ns
Pulse width of -IOW		t_{WW}	200			ns
INTRQ delay time from -IOR	(*1)	t_{RIR}			250	ns
	(*2)	t_{RIR}			500	ns
INTRQ delay time from -IOW	(*1)	t_{WIR}			250	ns
	(*2)	t_{WIR}			500	ns
DMA cycle time	(*1)	t_{DRQ2CY}	7.5			μs
	(*2)	t_{DRQ2CY}	13			μs
DRQ2 delay time from -DRQ	(*1)	t_{DDRQ}		375		ns
	(*2)	t_{DDRQ}		750		ns

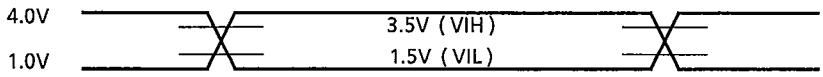
TENTATIVE

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
DRQ delay time from -DACK2		t_{ACDRQ2}			200	ns
-IOR delay time from DRQ2		t_{DRQ2R}	0			ns
-IOW delay time from DRQ2		t_{DRQ2W}	0			ns
-IOR / -IOW delay time from DRQ2	(*1)	t_{DRQ2RW}			7.0	µs
	(*2)	t_{DRQ2RW}			12	µs
Pulse width of -DACK2	(*1)	t_{AA}	125			ns
	(*2)	t_{AA}	250			ns
-DACK2 setup time before -IOR	(*3)	t_{ACR}	0			ns
-DACK2 hold time after -IOR	(*3)	t_{RAC}	0			ns
-DACK2 setup time before -IOW	(*3)	t_{ACW}	0			ns
-DACK2 hold time after -IOW	(*3)	t_{WAC}	0			ns
Pulse width of DMATC	(*1)	t_{TC}	63			ns
	(*2)	t_{TC}	125			ns
RD7EN delay time from -IOR		t_{7ENR}			100	ns
RD7EN delay time from -IOR		t_{7ENF}			100	ns
RD7 delay time from -IOR		t_{RD7D}			100	ns
RD7 flaot delay time		t_{RD7F}	20		100	ns
DS setup time before STP	(*1)(*4)	t_{DSST}	10			µs
	(*2)(*4)	t_{DSST}	20			µs
DS hold time after STP	(*1)(*4)	t_{STDS}	2			µs
	(*2)(*4)	tS_{TDS}	4			µs
DR setup time before STP	(*1)(*4)	t_{DST}	0.5			µs
	(*2)(*4)	t_{DST}	1			µs
DR hold time after STP	(*1)(*4)	t_{STD}	12			µs
	(*2)(*4)	t_{STD}	24			µs
Pulse width of STP	(*1)	t_{STP}	3	3.5		µs
	(*2)	t_{STP}	6	7		µs
Pulse width of WDT1	(*1)	t_{WDD1}		250		ns
	(*2)	t_{WDD1}		500		ns
-RDT low level width		t_{RDD1}	130			ns
-RDT high level width		t_{RDD2}	130			ns
-IDX low level width	(*1)	t_{IDX}	125			ns
	(*2)	t_{IDX}	250			ns

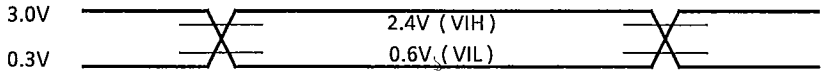
*1 : Value for Perpendicular magnetized floppy mode
*2 : Value for Standard mode. In case of mini floppy mode, each value is twice
*3 : AEN = "High" during the DMA cycle
*4 : CDS = "Low"

6.4.1 AC TEST INPUT WAVE FORM

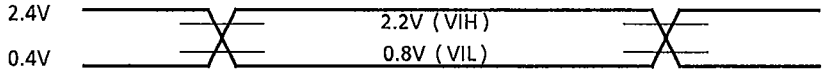
Input terminal group 1 : XIN



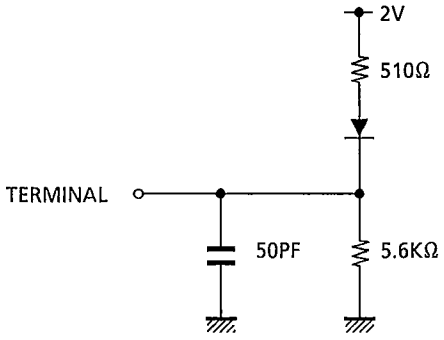
Input terminal group 2 : Schimitt trigger input



Input terminal group 3 : The other input terminals and Data bus

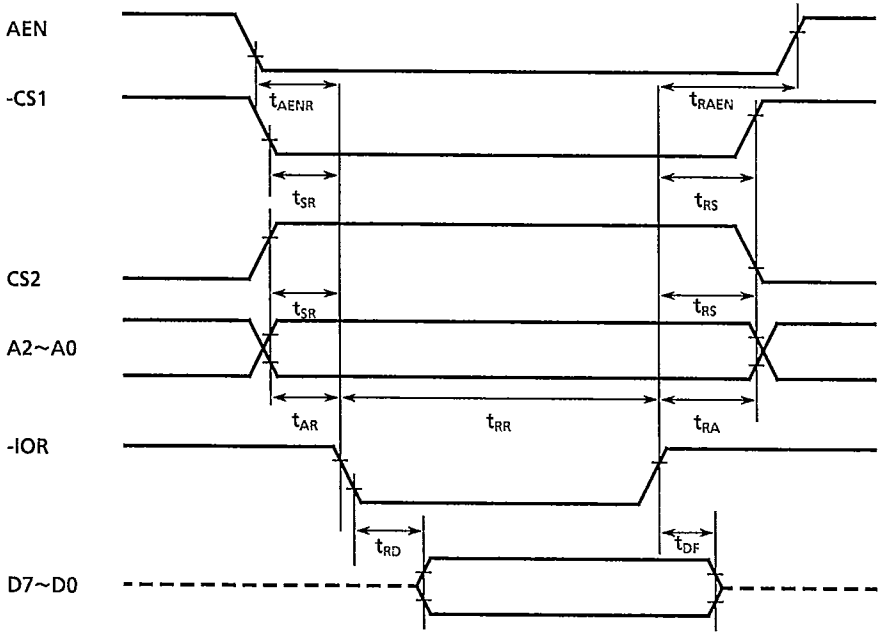


6.4.2 OUTPUT LOAD CIRCUIT

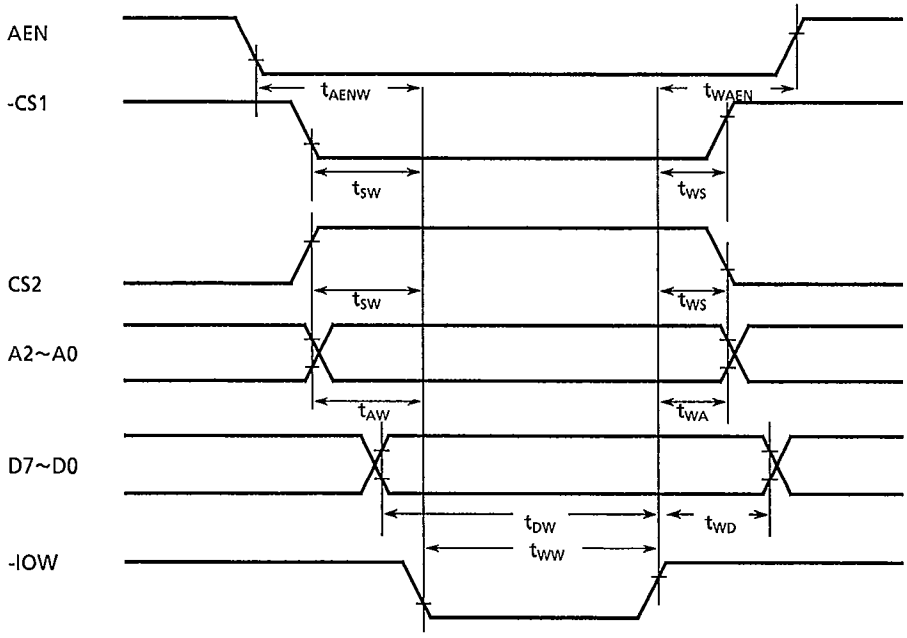


6.4.3 TIMING CHART

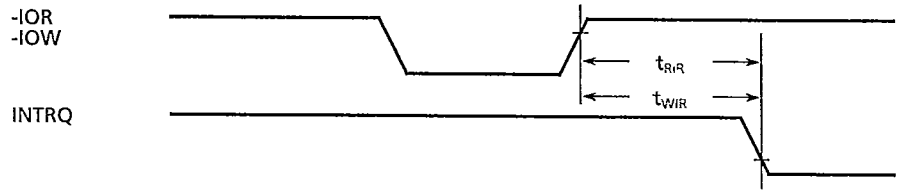
① Read Operation



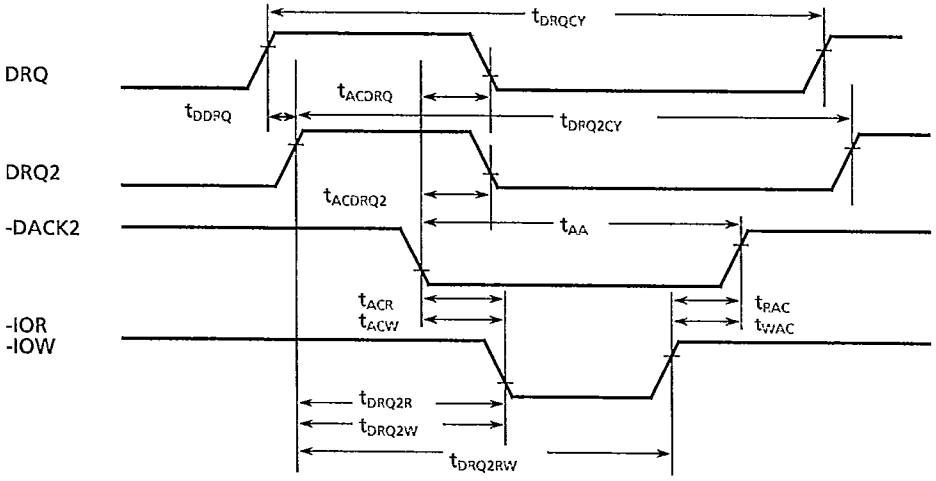
② Write Operation



③ Non-DMA Operation



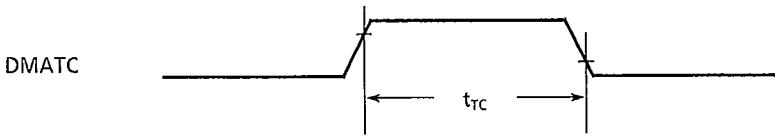
④ DMA Operation



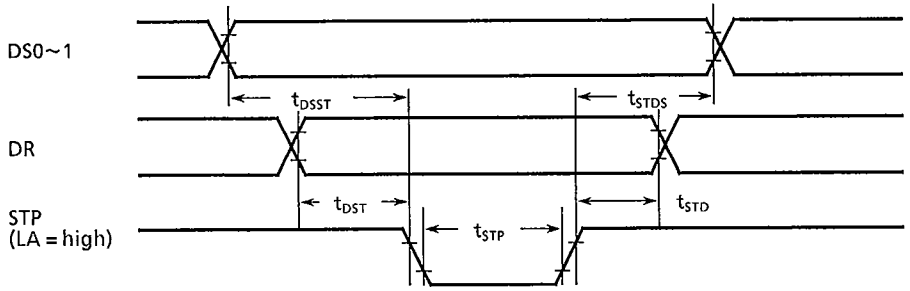
6

FLOPPY DISK CONTROLLER

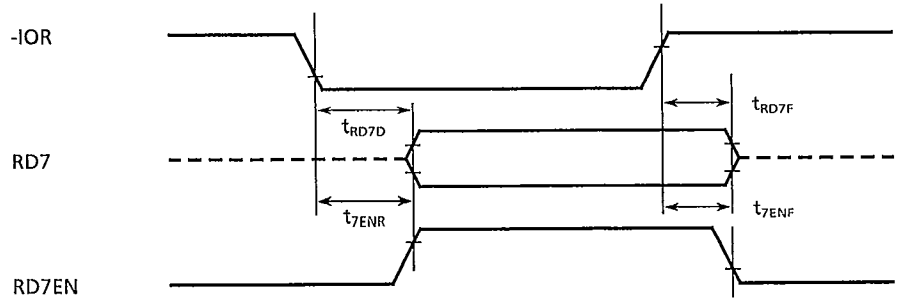
⑤ Wave form of Terminal Count



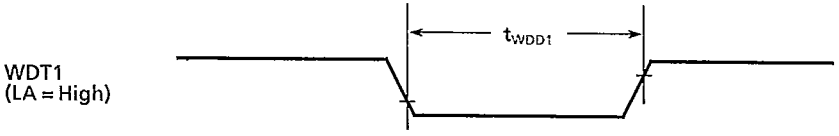
⑥Seek Operation (For CDS = Low, DS0~1)



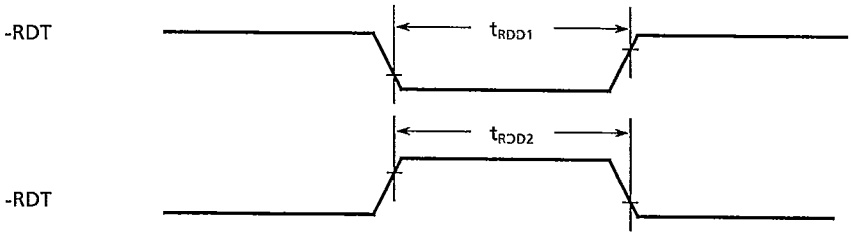
⑦ Wave form of RD7,RD7EN



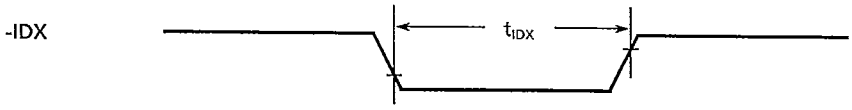
⑧ Wave form of Write Data



⑨ Wave form of Read Data

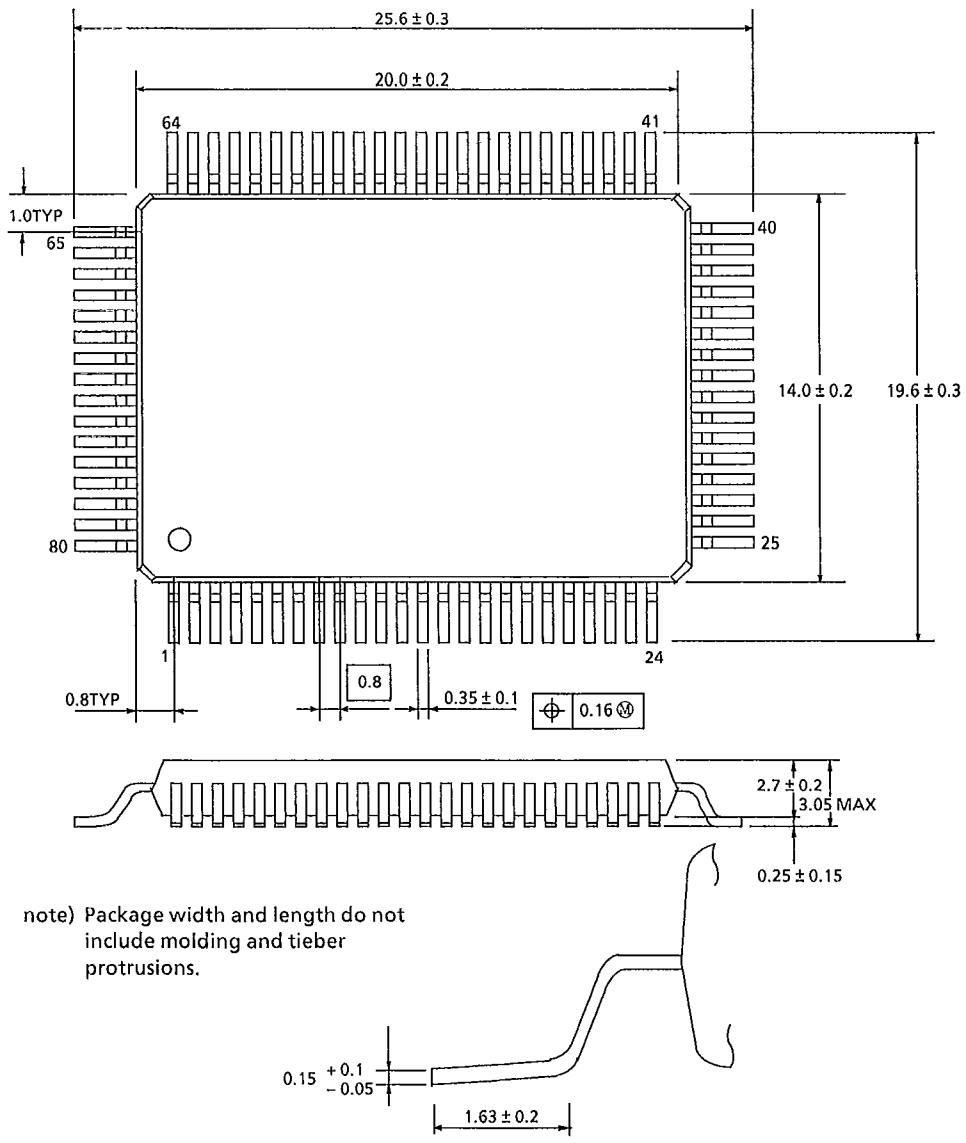


⑩ Wave form of INDEX



7. PACKAGE DIMENSION

QFP80-P-1420 Unit : mm



note) Package width and length do not include molding and tieber protrusions.