MODEL 9400 DISK STORAGE SYSTEM

TECHNICAL MANUAL
VOLUME 1

System Industries

System Industries

9400-11-01

TECHNICAL MANUAL

INSTALLATION AND MAINTENANCE INSTRUCTIONS

9400 DISK STORAGE SYSTEM WITH RP04 OR RM03 EMULATORS FOR PDP-11 COMPUTERS

VOLUME 1

SYSTEM INDUSTRIES

The technical data in this manual represents the best information available as of the date of publication. This information is subject to change.

System Industries reserves the right to make changes and/or improvements to its products without prior notification, and without incurring any obligation to incorporate such changes or improvements in equipment previously sold or shipped.

Applicable change information will be furnished by System Industries' Customer Service Department in the form of Customer Service Bulletins, and through changes issued to this manual.

 Comments on this manual or its use are invited and should be addressed to System Industries, Technical Publications, P. O. Box 9025, Sunnyvale, CA 94086, USA.

1 APRIL 1979

Change 2 - 21 April 1980

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGE PAGE. DESTROY SUPERSEDED PAGES.

Dates of issue for original and changed pages are : Original 1 April 1979

Change 1 15 August 1979, Change 2 21 April 1980

TOTAL NUMBER OF PAGES IN THIS PUBLICATION IS 482 CONSISTING OF THE FOLLOWING

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGE PAGE. DESTROY SUPERSEDED PAGES.

11-76	blank	0	11-139		0	11-202	blank	0
11-77		1	11-140	blank	0	11-203		0
11-78	blank	0	11-141		0	11-204	blank	0
11-79		1	11-142	blank	0	11-205		0
11-80	blank	0	11-143		1	11-206	blank	0
11-81		1	11-144	blank	0	11-207		1
11-82	blank	0	11-145		1	11-208	blank	0
11-83		1	11-146	blank	0	11-209		0
11-84	blank	0	11-147		0	11-210	blank	0
11-85		1	11-148	blank	0	11-211		1
11-86	blank	0	11-149		0	11-212	blank	1
11-87		1	11-150	blank	0	11-213		1
11-88	blank	0	11-151		0	11-214	blank	1
11-89		1	11-152	blank	0	11-215		1
11-90	blank	0	11-153		0	11-216	blank	1
11-91		1	11-154	blank	0	11-217		1
11-92	blank	0	11-155		0	11-218	blank	1
11-93		1	11-156	blank	0	11-219		1
11-94	blank	0	11-157		0	11-220	blank	1
11-95		1	11-158	blank	0	11-221		1
11-96	blank	0	11-159		0	11-222	blank	1
11-97		1	11-160	blank	0	11-223		1
11-98	blank	0	11-161		1	11-224	blank	1
11-99		1	11-162	blank	0	11-225		1
11-100	blank	0	11-163		0	11-226	blank	1
11-101		1	11-164	blank	0	11-227		1
11-102	blank	0	11-165		0	11-228	blank	1
11-103		1	11-166	blank	0	11-229		1
11-104	blank	0	11-167		0	11-230	blank	1
11-105		1	11-168	blank	0	11-231		1
11-106	blank	0	11-169		0	11-232	blank	1
11-107		1	11-170	blank	0	11-233		1
11-108	blank	0	11-171		0	11-234	blank	1
11-109		0	11-172	blank	0	11-235		1
11-110	blank	0	11-173		0	11-236	blank	1
11-111		0	11-174	blank	0	11-237		1
11-112	blank	0	11-175		1	11-238	blank	1
11-113		0	11-176	blank	0	11-239		1
11-114	blank	0	11-177		0	11-240	blank	1
11-115		0	11-178		0	11-241		1
11-116	blank	0	11-179		0	11-242	blank	1
11-117		1	11-180	blank	0	11-243		2
11-118	blank	0	11-181		0	11-244	blank	1
11-119		1	11-182	blank	0	11-245		2
11-120	blank	0	11-183		0	11-246	blank	1
11-121		1	11-184	blank	0	11-247		2
11-122	blank	0	11-185		0	11-248	blank	2
11-123		2	11-186	blank	0	11-249		2
11-124	blank	0	11-187		0	11-250	blank	2
11-125		2	11-188	blank	0	11-251		2
11-126	blank	0	11-189		1	11-252	blank	2
11-127		2	11-190	blank	0	11-253		2
11-128	blank	0	11-191		0	11-254	blank	2
11-129		1	11-192	blank	0	11-255		2
11-130	blank	0	11-193		1	11-256	blank	2
11-131		0	11-194	blank	0	11-257		2
11-132	blank	0	11-195		0	11-258	blank	2
11-133		0	11-196	blank	0			
11-134	blank	0	11-197		0			
11-135		0	11-198	blank	0			
11-136	blank	0	11-199		0			
11-137		0	11-200	blank	0			
11-138	blank	0	11-201		0			

RECORD OF CHANGES

Change Number	Date	Title or Brief Description	Entered By

TABLE OF CONTENTS
VOLUME 1

TABLE OF CONTENTS
VOLUME 2

LIST OF ILLUSTRATIONS
VOLUME 1

LIST OF ILLUSTRATIONS
VOLUME 2

LIST OF TABLES
VOLUME 1

LIST OF TABLES
VOLUME 2

ABBREVIATIONS, ACRONYMS, AND MNEMONICS

AA	Any Attention
AC	Alternating Current
ACE	Any CPA Error
ACK	Acknowledge
ADD	Address
ADDR	Address
ADR	Address
AE	Any Error
AFMT	Auto Format
AOE	Adress Overflow Error
APE	Address Parity Error
ATA	Attention Active
ATN	Attention
ATTN	Attention
AV	Address Verify
AVF	Address Verify File
B	Buffer
BA	Bus Address
BA	Bus Available
BADR	Buffer Address Register
BAE	Bus Address Extension
BAI	Bus Address Increment Inhibit
BAR	Block Address Register
BAVAIL	Buffer Available
BBF	Bad Block Flag
BBSY	Bus Busy
BC	Buffer Counter
BDI	Buffer Data In
BDO	Buffer Data Out
BE	Bus Enable
BEMTY	Buffer Empty
BG	Bus Grant
BIDI	Bidirectional (Bus)
BPAR	Buffer Parity Error
BR	Bus Request
BRDY	Buffer Ready
BREQ	Buffer Request
BUFF	Buffer
C0	Control 0
C1	Control 1
CBAR	Computer Buffer Address Register
CC	Current Cylinder
CDC®	Control Data Corporation
C.FD.BK	Common Feedback
CI	Computer Interface
CLK	Clock
CLR	Controller Clear
CMD	Command
CMP	Compare
CNT	Count
CNTR	Counter
CP	Clock Pulse
CPA	Computer Port Adapter
CPECF	CPA Error And Control Flag
CPEVF	CPA Event Flag
CPL	CPU Power Low
CPS	Computer Port Select
CPU	Central Processor Unit
CRC	Cyclic Redundancy Check
CREQ	Computer Request
CSL	Control Status Low
CTRL	Control
CTU	Controller Test Unit
DB	Data Buffer
	Data Bus
DBAR	Disk Buffer Address Register
DBC	Data Buffer Counter
DBL	Double Word
DC	Desired Cylinder
DCK	Data Check
DEC®	Digital Equipment Corporation
	Decrement
DECR	Decrement
DEG	Disk Enable Gate
DERF	Data Error Flag
DEVF	Data Event Flag
DF	Drive Fault
DI	Drive Interface
DIA	Drive Interface Address
DIAG	Diagnostic
DIB	Drive Input Bus
DIC	Drive Interface Control
DIP	Drive Interface Port
DIR	Data Input Register
DMA	Direct Memory Access
DMAR	Direct Memory Access Register
DOB	Drive Output Bus
DOC	Data Operation Control
DOC IDF	Data Operation Control Inhibit Data Field
DOC RBC	Data Operation Control Reset Buffer Controls
DOR	Data Out Register
DPA	Data Port Address
DPE	Data Parity Error
DREQ	Data Request
DRY	Drive Ready
DSK	Disk
DST	Disk Start
DSW	Data Switch
DTC	Data Transfer Control
DV	Data Verify
DVRS	Drivers
EC	Error Clear
ECC	Error Correction Code
ECCI	Error Correction Code Inhibit
ECH	ECC Hard Error
ECF	Error Control Flag
EMTY	Empty
EN	Enable

ENAB	Enable
EOH	End of Header
EOS	End of Sector
ERR	Error
ESI	Error Stop Inhibit
EW	Even Word
EX	External
EXT	Extended
	Extension
EXT EM	Extended Emulation
EVF	Event Flag
FAR	File Address Register
FDR	File Data Register
FDRH	File Data Register High Byte
FDRL	File Data Register Low Byte
FLG	Flag
FIFO	First-in First-out Register
FLT	Fault
FMT	Format
FPLA	Field Programmable Logic Array
FSU	Field Service Unit
GC	Go Command
GT	Grant
HCE	Header Compare Error
HCI	Header Compare Inhibit
HCRC	Header CRC Error
HDR	Header
HI	High
IAE	Invalid Address Error
IB	Input Bus
IDF	Inhibit Data Field
IE	Interrupt Enable
ILF	Illegal Function
INCR	Increment
INIT	Initialize
INT	Interrupt
INTR	Interrupt Request
	Interrupt
INTRPT	Interrupt
I/O	Input/Output
IPCK	Invert Parity Check
IR	Interrupt Request
IRQ	Interrupt Request
IV	Interrupt Vector
LD	Load
LD/LR	Line Driver/Line Receiver
LO	Low
LST	Last Sector Transfered
MAR	Memory Address Register
MCK	Master Clock
MBD	Main Data Bus
MEM	Memory
MOL	Medium On-line
MP	Microprocessor
MPD	Microprocessor Data
MPU	Microprocessor Unit
MR	Master Ready
MRDY	Memory Ready
MSTR	Master
MSYN	Master Sync
MUX	Multiplxer
MXCA	control signal
MXCB	control signal
MXF	Missed Transfer
MXG2	control signal
MXC4	control signal
MXG8	control signal
NED	Non-Existant Drive
NEM	Non-Existant Memory
NMI	Non-Maskable Interrupt
NP	Non-Processor
NPG	Non-Processor Grant
NPR	Non-Processor Request
NRZ	Non-Return to Zero
OD0	Operator Display 0
OD1	Operator Display 1
OE	Output Enable
OFS	Offset Information
O'FLO	Overflow
OP	Operation
OW	Odd Word
PE	Poll Enable
PER	Programming Error
PGE	Programming Error
PGM	Program
PHYS	Physical
PLS	Pulse
POR	Power-On Reset
PR	Programmed Reset
PROM	Programmable Read-Only Memory
PSA	Physical Sector Address
R	Register
RAM	Random Access Memory
RBC	Reset Buffer Control
RBRDY	Read Buffer Ready
RD	Read
	Read Data
RDB	Read Bus
RDFDBK	Read Feedback
RDST	Read Start
RDY	Ready
REG	Register
REQ	Request
RF	Register File
RHBAE	RP04 Bus Adress Extension Register
RHCS3	RP04 Control and Status Register 3
RLE	Receiver Latch Enable
RMT	Remote
RPAK	Resistor Pack
RPAS	RP04 Attention Summary Register
RPBA	RP04 Bus Address Register

RPCC	RP04 Current Cylinder Register
RPCS1	RP04 Control and Status Register 1
RPCS2	RP04 Control and Status Register 2
RPDA	RP04 Desired Address Register
RPDB	RP04 Data Buffer
RPDC	RP04 Desired Cylinder Register
RPDS	RP04 Drive Status Register
RPDT	RP04 Drive Type Register
RPEC1	RP04 ECC Register 1 - Position
RPEC2	RP04 ECC Register 2 - Pattern
RPER1	RP04 Error Register 1
RPER2	RP04 Error Register 2
RPER3	RP04 Error Register 3
RPLA	RP04 Look-Ahead Register
RPMR	RP04 Maintenance Register
RPOF	RP04 Offset Register
RPSN	RP04 Serial Number Register
RPWC	RP04 Word Count Register
RSEL	Register Select
RST	Reset
R/W	Read/Write
SA	Sector Address
SACK	Selection Acknowledge
SC	Special Condition
SCT	Sector
SD	Serializer - Deserializer
S/D	Serializer/Deserializer Sector Decode
SDACK	Serializer - Deserializer Acknowledge
SEL	Select
SEL DOC	Select Data Operation Control
SEL OPNL	Select Operators Maintenance Panel (FSU)
SKI	Seek Incomplete
SP0	Scratch Pad 0
SP1	Scratch Pad 1
SR	Shift Register System Reset
SSYN	Slave Sync
STRB	Strobe
SVC	Service
SYS	System
TA	Track Address
TC	Transfer Complete
TCC	Transfer Check Code
TO	Time-out
TRANS	Transfer
TRE	Transfer Error
U	Unit Select
UAB	Unibus Address Bus
UB	Unibus
UBA	Unibus Address
UBD	Unibus Data
UBUS	Unibus
UDB	Unibus Data Bus
UNS	Unsafe
USEL	Unit Select
VMA	Valid Memory Address
VV	Volume Valid
WC	Word Count Word Counter
WCE	Write Check Error
WC OFLO	Word Counter Overflow
WCR	Word Count Register
WD	Write Data
WLE	Write Lock Error
WPF	Write Protect Flag
WR	Write
WRB	Write Bus
WRL	Write Lock
WRFDBK	Write Feedback
WRSP	Write Scratchpad
XCEIVER	Transceiver
XFR	Transfer
ZF	Zero Flags
ZFILL	Zero Fill
ZT	Zero Test
2×F	Two Times Frequency (2MHz)
4×F	Four Times Frequency (4MHz)
μOP	Micro-operation
μP	Microprocessor
μPC	Microprocessor Control
μPDR	Microprocessor Data Register

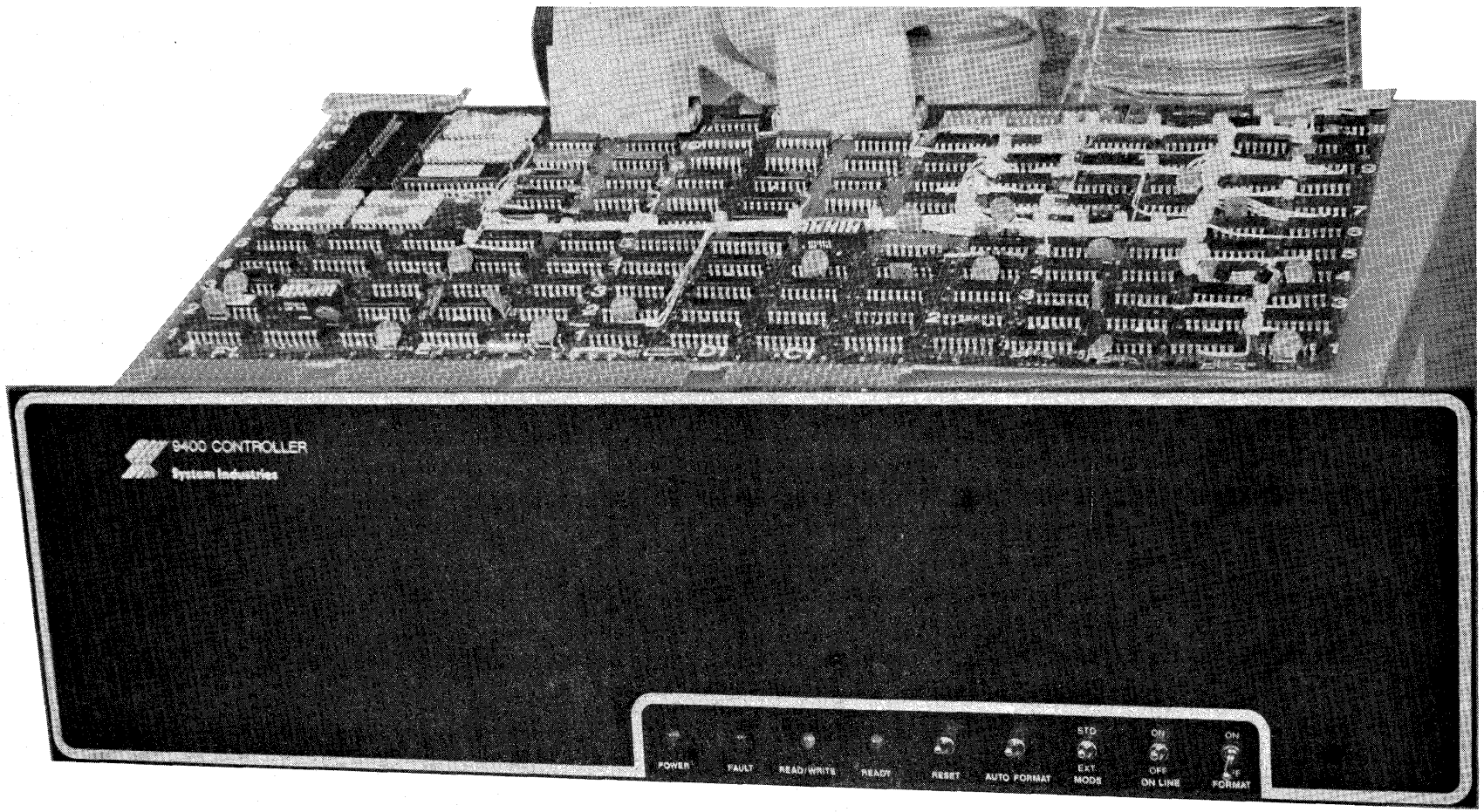


Figure 1-1. System Industries Series 9400 Disk Controller

CHAPTER 1
GENERAL INFORMATION

1-1. **SCOPE.** This manual contains site preparation, installation, operation, checkout, alignment and maintenance instructions, theory of operation, and parts lists for the System Industries' Series 9400 Disk Controller installed on Digital Equipment Corporation PDP-11 Computers.

This manual is divided into eleven chapters. Chapter 1 contains a general description of the equipment, its performance specifications, and descriptions of tools and test equipment required to install and maintain the equipment. Chapter 2 contains the equipment installation procedures. Chapter 3 provides information on equipment controls and indicators; and turn-on and operating procedures. Chapter 4 comprises equipment diagnostic and checkout procedures. Chapter 5 provides the equipment theory of operation. Chapter 6 addresses optional features available for the Series 9400 Disk Controller. Chapter 7 lists the periodic maintenance requirements for the equipment. Chapter 8 provides alignment and calibration procedures for the equipment. Chapter 9 lists mechanical parts and electronics subassemblies. Chapter 10 details model differences created by factory and field engineering changes. Chapter 11 contains the equipment foldout schematics, block and interconnect diagrams.

1-2. **GENERAL DESCRIPTION.** The System Industries' Series 9400 Disk Controllers provide the capability to connect from one to four Control Data Corporation (CDC) 9762 (80 Megabyte) or 9766 (300 Megabyte) Storage Module Drives to Digital Equipment Corporation (DEC) PDP-11 Computer Systems.

Interface options permit the storage module drives to be attached to the controller in a daisy chain or a radial configuration. A multiport option allows two to four PDP-11 CPUs to share the disk controller and storage module drive(s).

Emulator routines in the Series 9400 Disk Controller provide a compatibility with the PDP-11 operating system software. An emulator is available for PDP operating systems utilizing RP04 disk drives.

The standard RP04 or RM03 emulation routines will support up to four CDC 9762 Storage Module Drives (with a size parameter change to the operating system software for 80 Megabytes storage on each drive); or four CDC 9766 Drives with three RP04 or RM03 logical drives of 100 Megabytes each, on CDC 9766.

1-3. **STANDARD FEATURES.** The following features are included as part of the standard System Industries Series 9400 Disk Controller:

1. One to four drive attachments.
2. CDC Storage Module Drives, 80 or 300 Megabytes per unit, or up to 1200 Megabytes per subsystem.
3. Multiple sector data buffering; 1024 words.
4. CRC serial data checking on header fields.
5. Write protect at drive levels.
6. Internal error flag logic.
7. Header address verification on all non-format writes or reads.
8. Multiple sector block read or write.
9. Automatic head/sector/cylinder switching across boundaries.
10. Defect flagging and detection.
11. Thirty-three sectors per track for RP04, thirty-two sectors per track for RM03.
12. Implied seek on read or write.
13. Microprocessor, and microprocessor programmed architecture.
14. Resident and non-resident microdiagnostics.
15. Error termination control; continues operation past error.
16. Automatic performance degradation without loss of data on slow or I/O bound minicomputers.
17. Maintenance indicators.
18. Data buffer parity check.
19. ECC; 11-bit burst error correction capability for each sectors data field.
20. Power fail detection and controlled abort.

1.4 **OPTIONAL FEATURES.** The following features are optional with the System Industries Series 9400 Disk Controller. Refer to Chapter 6 for a complete description of optional features.

1. Computer Multiport; two to four radially connected, command set, transparent ports.
2. Radial Drive Interface; 2, 3 or 4 Storage Module Drives.

3. Daisy Chain Drive Interface; up to 8 Storage Module Drives.

4. Auto Format; executes offline disk pack formatting.

5. Logical Copy; (extended emulation only, 2 or more physical drives required).

1.5 **FUNCTIONAL CHARACTERISTICS.** The functional characteristics of the Series 9400 Disk Controller are listed in Table 1-1. For the functional characteristics of the applicable CDC Storage Module Drive, refer to Chapter 2, Installation; or the appropriate CDC manuals listed in Table 1-2.

1-6. **LIMITED WARRANTY.**

a. Series 9400 Disk Controller. System Industries warrants that its products are free from defects in materials and workmanship and meet System Industries' performance specifications. The warranty period is ninety (90) days from the date of shipment to Buyer. This warranty is limited by the paragraphs below.

Return to Factory. If Buyer discovers a defect in a System Industries product covered by this agreement, Buyer's exclusive remedy is to ship the product back to System Industries' Sunnyvale factory where System Industries will at its option, either repair or replace the product. This remedy applies if System Industries receives the returned product on or before the tenth day after the expiration of the warranty period and Buyer notifies System Industries of the defect before returning the product.

Cost to Buyer of Repairs or Replacement. Buyer must prepay freight charges to System Industries. System Industries will pay return freight to Buyer. There is no other charge for repair or replacement during the warranty period.

b. Transferrable Disk Drive Warranty. In addition to the forgoing warranty, System Industries also provides to Buyer the transferrable warranty, if any, provided to System Industries by the disk drive manufacturer. (NOTE: Neither System Industries nor disk drive manufacturers warrant read/write heads or subsequent damage sustained as a result of head/disk interference. Head/disk interference can be prevented by carefully following the disk drive and disk pack manufacturers' recommended operating and preventive maintenance procedures.)

c. Limitation of Warranty and Liability. The foregoing constitutes System Industries' entire warranty, expressed, implied, and/or statutory (except as to title), and states the full extent of System Industries' liability to Buyer or to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential. OTHER THAN AS EXPRESSLY PROVIDED IN THIS DOCUMENT, NO WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, ARE MADE. NO EMPLOYEE, REPRESENTATIVE, OR AGENT OF SELLER HAS ANY AUTHORITY, EXPRESSED OR IMPLIED, TO ALTER OR TO SUPPLEMENT THE TERMS OF THIS WARRANTY.

1-7. **SAFETY PRACTICES.** Normal safety precautions should be practiced whenever working around electrically powered equipment. This equipment contains potentially lethal voltages. Prior to inspection or servicing, ensure that power has been disconnected. In this manual activities that can jeopardize human safety to the extent of causing personal injury or death are prefixed by a WARNING statement. Activities which can cause damage to the equipment are prefixed by a CAUTION statement.

1-8. **REFERENCE DATA.** The Series 9400 Disk Controller is built by System Industries, 525 Oakmead Parkway, P.O. Box 9025, Sunnyvale, CA 94086. Telephone (408) 732-1650. Telex 346459.

Equipment, accessories, and documents supplied as part of the 9400 Disk Controller are listed in Table 1-2.

Special tools, test equipment, and publications required but not supplied with the 9400 Disk Controller, are listed in Table 1-3.

1-9. **MANUFACTURER SERVICES.** System Industries offers the following services to users of System Industries' products.

1. Training
2. On-Site Service
3. Maintenance Spares
4. Factory Repair
5. Maintenance Documentation

a. Maintenance Training. System Industries offers regularly scheduled maintenance training classes on all of its products (including System Industries' vended disk drives) at the Sunnyvale, California Training Center. These classes, taught by professional instructors, cover System Industries' products from a maintenance viewpoint. By contacting the Training Center, customers may arrange for on-site classes, or classes tailored to special needs. For additional details, contact Customer Service, in Sunnyvale, California and ask for training information.

b. On-Site Service. System Industries' nation wide Field Service Organization provides timely, competent service for customers requiring on-site corrective maintenance. A variety of services can be provided as follows:

1. Installation of controller and drives
2. Time and material service calls

Table 1-1. Functional Characteristics

Input Power	250W (Typical), 115±11 Vac, Single Phase, 47 to 66 Hz, 1364 BTU/hour (maximum) 250W (Typical), 230±23 Vac, Single Phase, 47 to 66 Hz, 1364 BTU/hour (maximum)
Enclosure Dimensions	
Height:	5.25 inches (13.335 cm)
Depth:	22.00 inches (55.88 cm)
Width:	19.00 inches (48.26 cm)
Weight:	
CCA Sizes	
Basic Control:	15.1×21.3 inches (38.35×54.10 cm)
Control Store:	7×3.5 inches (17.78×8.89 cm)
Computer Interface:	3.85×16.5 inches (9.78×41.91 cm)
Disk Interface:	4.3×16.5 inches (10.92×41.91 cm)
Computer Port Adapter:	8.8×15.6 inches (20.32×39.62 cm)
Temperature	
Operating:	40°F to 120°F (4.4°C to 48.9°C) with max gradient of 5°F per hour
Non-Operating:	−40°F to 130°F (−40°C to 54.4°C)
Humidity	
Operating:	10% to 80% relative humidity with no condensation.
Non-Operating:	5% to 95% relative humidity with no condensation.
Cables	
Controller/Disk Cables:	(1) Flat TWP, 100Ω, 28 AWG, 100 foot maximum (1) Flat shielded ribbon, 130Ω, 28 AWG, 50 foot maximum
Controller/CPA Cables:	(2) Flat ribbon, 125Ω, 10 foot standard
Altitude	
Operating:	−1000 to 7000 feet (−305 to 2134 meters)
Non-Operating:	−1000 to 15,000 feet (−305 to 4572 meters)

Table 1-2. Equipment, Accessories, and Documents Supplied

QTY	NOMENCLATURE	PART NO.	DIMENSIONS	WEIGHT/VOL
1	Series 9400 Disk Controller	9410-7101 (60 Hz) or 9410-7102 (50 Hz)	5.25H×19.0W×22.0D (13.335H×48.26H×55.88D (cm))	
1	Series 9400 Disk Controller Technical Manual	9400-11-01	N/A	N/A
1	Software Patches RSTS/RS11/RSS11D/and IAS Technical Manual	9400-11-03	N/A	N/A
1[1]	CDC Storage Module Drive BK4XX, BK5XX (9762) Hardware Maintenance Manual, Volume 1	CDC83322150	N/A	N/A
1[1]	CDC Storage Module Drive BK4XX, BK5XX Hardware Reference Manual (9762)	CDC83322200	N/A	N/A
1[1]	CDC Storage Module Drive BK5XX (9762) Hardware Maintenance Manual, Volume 2	CDC83322240	N/A	N/A
1[1]	CDC Storage Module Drive BK6XX, BK7XX (9766) Hardware Maintenance Manual	CDC83322310	N/A	N/A
1[1]	CDC Storage Module Drive BK6XX, BK7XX (9766) Hardware Reference Manual	CDC83322320	N/A	N/A
1[2]	Computer Port Adapter Circuit Card Assembly	9400-6011[3] or 9400-6031	8.80H×15.68W (202.5×400 (cm))	
1[2]	Cable, Controller to SMD (A)	3225-7007	16 ft.	N/A
1[2]	Cable, Controller to SMD (B)	3225-7008	16 ft.	N/A
2[2]	Cable, Controller to CPU	9400-7007	10 ft.	N/A
1[4]	Cache Address and Control Circuit Card Assembly	9400-6101	N/A	N/A
1[4]	Cache Control Buffer Circuit Card Assembly	9400-6102	N/A	N/A
1[4]	Cache Data Circuit Card Assembly	9400-6103	N/A	N/A

NOTES:

[1]Applicable manuals are shipped with CDC Storage Module Drives when ordered from System Industries with Series 9400 Disk Controller.

[2]Quantities listed are for single drive, single CPU systems.

[3]9400-6021 for RH70 (Cache) Systems.

[4]Used only for PDP-11/70 RH70 (Cache) Systems.

Table 1-3. Recommended Test Equipment and Tools

NAME	MANUFACTURER	PART NO.	APPLICATION
Card Extender	CDC	54109700	Field Repair of 9762, 9766 SMDs
CE Disk Pack	CDC	70438700	Alignment of 9762 SMDs
CE Disk Pack	CDC	70430003	Alignment of 9766 SMDs
Deck Support Bracket	CDC	87073000	Field Repair of 9762, 9766 SMDs
Oscilloscope	Tektronix	454 or equivalent	Field and Depot Repair and Alignment of SMDs and Controller
Head Alignment Tool	CDC	75018803	Alignment of 9762, 9766 SMDs
Torque Screwdriver	CDC	12218425	Alignment of 9762, 9766 SMDs
Torque Screwdriver Bit	CDC	87016701	Alignment of 9762, 9766 SMDs
Field Test Unit	CDC	77449300	Field Repair and Alignment of 9762, 9766 SMDs
Digital Volt/Ohmmeter	Fluke	8020A or equivalent	Field Repair of SMDs and Controller

3. Short term (monthly) Service Agreements
4. Annual Service Agreements
5. Special On-Site Service Plans
6. Telephone Consultation

On-site service is directed from System Industries' three Regional Offices. The field staff consists of dedicated Senior Field Engineers with advanced problem solving abilities. Questions concerning on-site support can be answered by contacting any of the Regional Offices as follows:

Western Regional Office - Irvine, California
telephone (714) 754-6555
Midwest Regional Office - Cincinnati, Ohio
telephone (513) 771-0075
Eastern Regional Office - Englewood, New Jersey
telephone (201) 568-1317

c. Maintenance Spares. System Industries, through the Customer Service Parts and Repair Center in Sunnyvale, stocks a large selection of maintenance spares. In addition to sales of parts, the Parts and Repair Center offers Circuit Card Assembly (CCA) exchanges as shown. On all Circuit Card Assembly exchanges customer must pay freight costs to and from System Industries and must submit a purchase order for the entire cost of the exchange Circuit Card Assembly. System Industries will credit the customer the appropriate amount indicated below, when System Industries receives the defective CCA from the customer within 30 days after System Industries ships the exchange CCA.

1. System Industries manufactured products.

a) Customer will receive full credit minus shipping charges for CCA's that fail during first 30 days of warranty period.

b) Customer will receive full credit, minus shipping charges and $50.00 or 15% of current CCA list price, whichever is greater, for CCA's that fail after the first 30 days of warranty period.

c) Customer will receive full credit, minus shipping charges and 60% of current CCA list price, fo CCA's that fail after warranty period.

2. System Industries vended products (Disk Drives).

Table 1-4. Production Change Orders

CHANGE NUMBER	NOMENCLATURE	DESCRIPTION

a) Customer will receive full credit minus shipping charges for CCAs that fail during first 30 days of warranty period.

b) Customer will receive full credit, minus shipping charges and $50.00 or 15% of current CCA list price, whichever is greater, for CCAs that fail after first 30 days of warranty period.

c) For price of out of warranty exchanges contact the Customer Service Parts and Repair Center in Sunnyvale, California.

d. Factory Repair. Factory repair of complete units and subassemblies is done in the Parts and Repair Center. Complete upgrade and modification of older equipment is also available through the Parts and Repair Center. Repairs and upgrades are handled by a Technical Staff utilizing sophisticated automated test equipment. The Parts and Repair Center provides quality repairs and minimum turn-around-time. On all repairs, the customer must pay freight costs to and from System Industries. Prior to returning any parts or equipment to System Industries, the customer must contact Customer Service and request Return Authorization. A Return Authorization number will be issued, and this number must be marked on the shipment and all the accompanying paperwork. Details of Circuit Card Assembly repairs are shown below. For further details, contact Customer Service and ask for the Parts and Repair Center.

1. System Industries manufactured products.

a) For CCAs covered under warranty, customer pays only freight charges.

b) For CCAs that are out of warranty, customer pays 25% of current CCA list price plus freight charges. A purchase order is required. Turn-around-time is ten days.

2. System Industries vended products.

a) For CCAs and subassemblies covered under the manufacturer's warranty, customer pays only freight charges.

b) For a price quotation on out of warranty repairs, contact Customer Service in Sunnyvale, California and ask for the Parts and Repair Center.

e. Maintenance Documentation. System Industries produces Customer Service Bulletins covering all of its products. These bulletins detail changes in System Industries' products that affect form, fit, or function. The bulletin identifies the methods the customer can use to implement those product changes that affect a customer's operation. To receive Customer Service Bulletins fill out the request form following this page, and mail to System Industries.

CHAPTER 2
INSTALLATION

2-1. INTRODUCTION. This chapter contains information on site preparation, equipment unpacking, damage reporting, equipment installation, and reshipping instructions.

2-2. SITE PREPARATION. Prior to receiving the System Industries 9400 Controller and CDC Storage Module Drives, provisions must be made for physical space requirements, grounding and AC power. Space must be allocated to allow for servicing of the equipment. The air conditioning system must have sufficient capacity to handle the additional heat generated by the 9400 Controller and CDC Storage Module Drives.

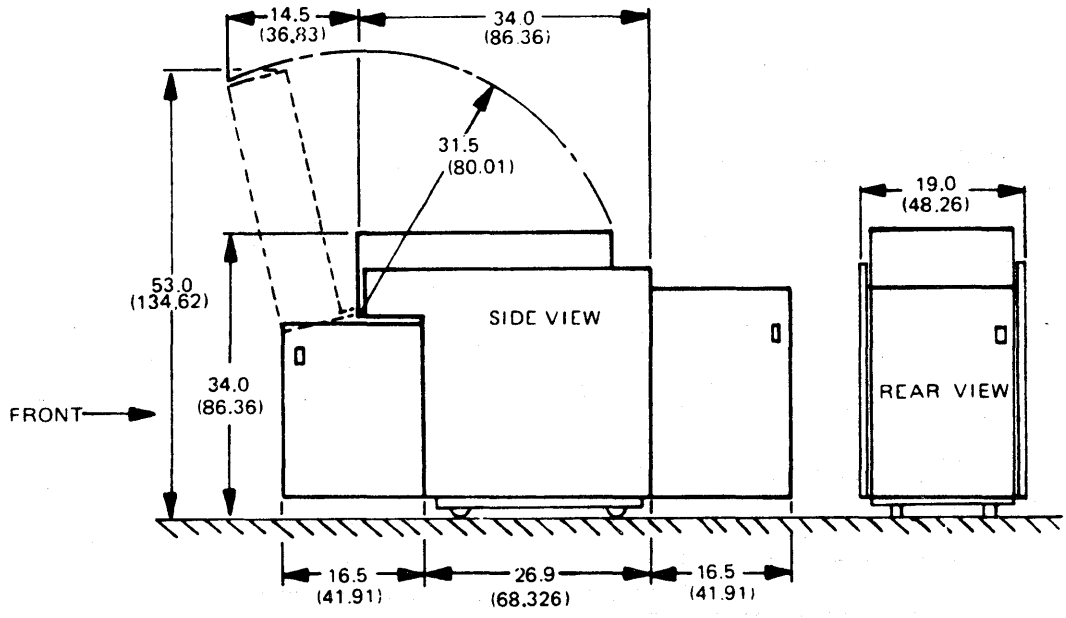
2-3. SPACE ALLOCATION. Space requirements for the 9400 Controller and CDC Storage Module Drives is as follows.

a. CDC Storage Module Drives. Dimensions for the various CDC 9762 (80 megabyte) Storage Module Drives are shown in Figures 2-1 through 2-5. Dimensions of the CDC 9766 (300 megabyte) Storage Module Drive are shown in Figure 2-6.

b. 9400 Controller. The 9400 Controller mounts in a standard 19 inch equipment rack, and requires 5.25 inches of rack space. Depth of the controller is 22 inches, and requires an equipment rack at least 24 inches in depth. A minimum of 30 inches of clear space in front of the controller, when mounted, is recommended for servicing (see Figure 2-7).

2-4. GROUNDING. The controller and its attached drives must be connected to earth ground. The permissible grounding schemes, listed in perferred order are:

1. Controller and drives connected to qualified site floor ground. A qualified ground would be a floor grid where the horizontal and vertical components of the grid are mechanically secure and have ground straps or their equivalent joining them to assure a constant ground potential. The grid must be connected to a good earth ground. An alternate qualified floor ground is a grounding grid or grounding bus system provided under the false floor (Figure 2-8).



NOTE 1. DIMENSIONS ARE GIVEN IN INCHES AND (CM).

Figure 2-1. Clearances - CDC 9762 Pedestal Cabinet

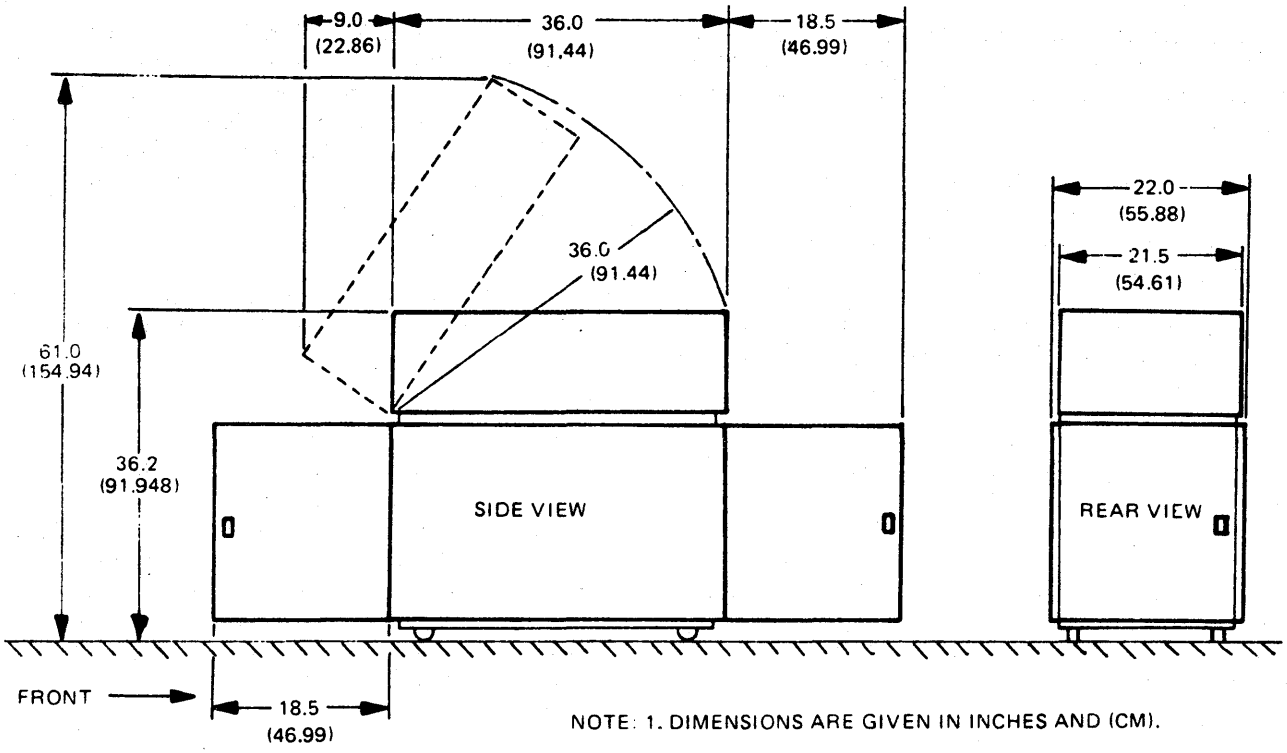


Figure 2-2. Clearances - CDC 9762 Acoustic Cabinet

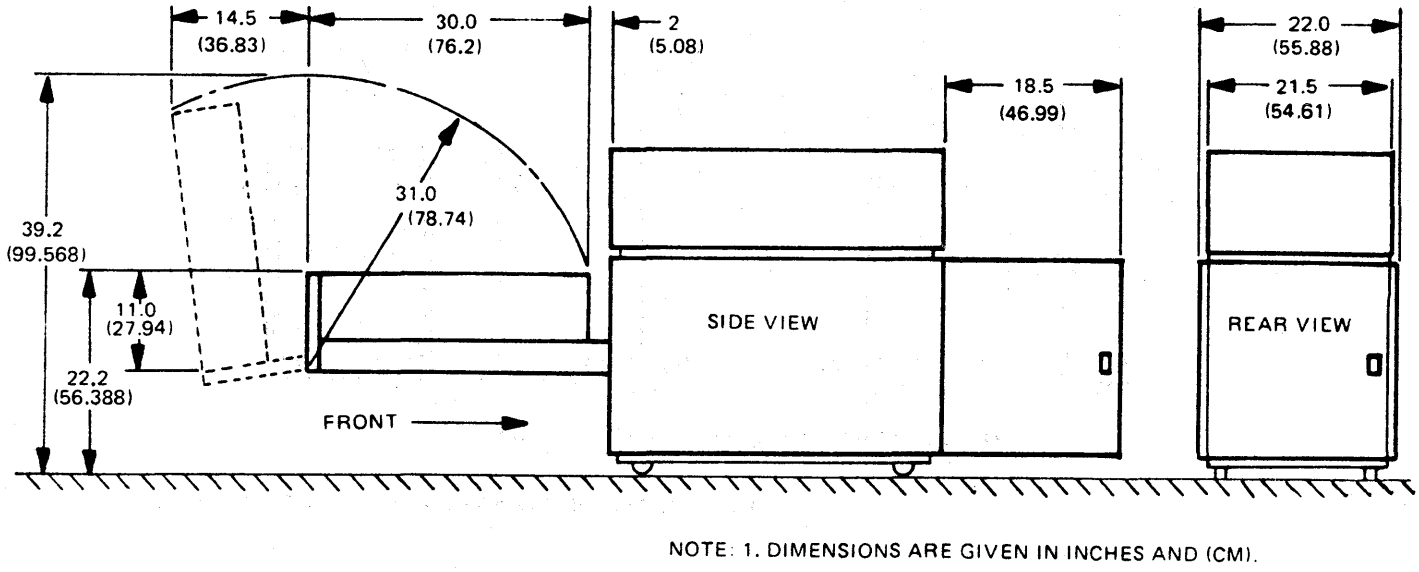
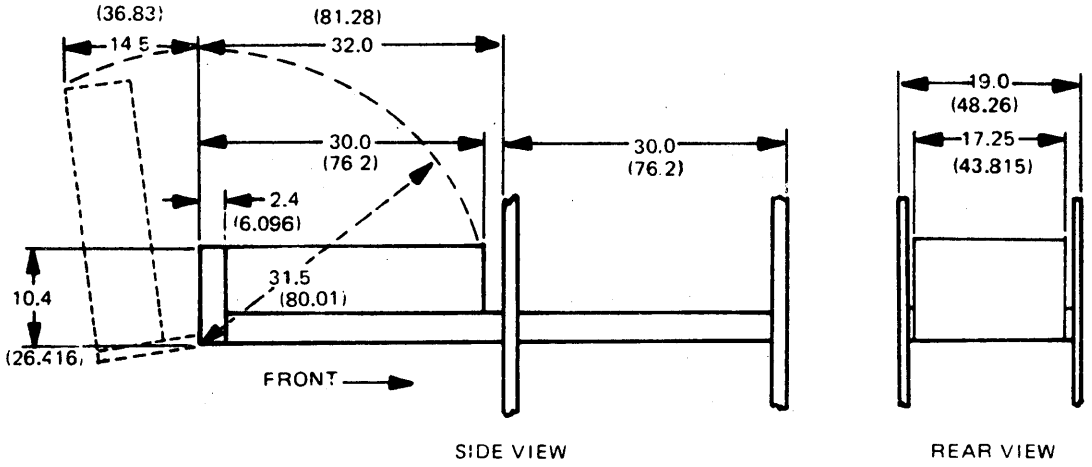
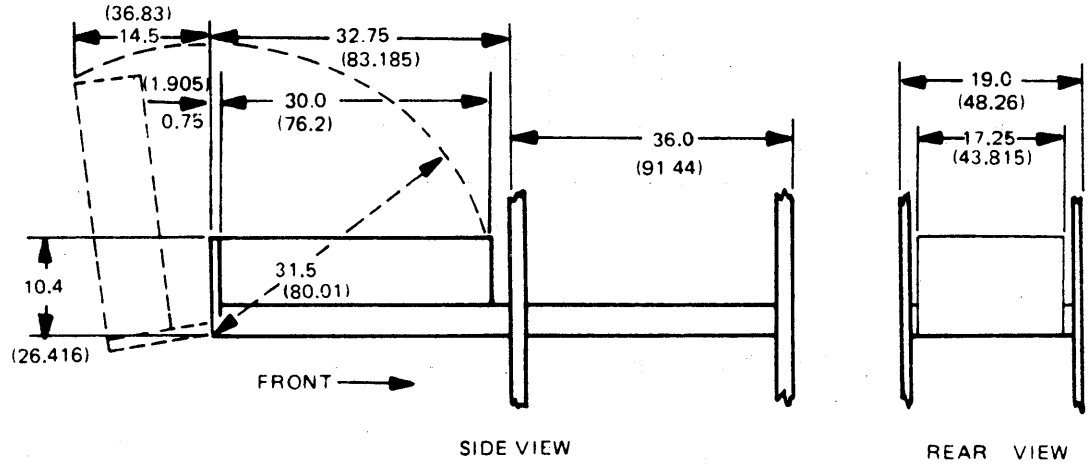


Figure 2-3. Clearances - CDC 9762 Acoustic Drawer



NOTE 1. DIMENSIONS ARE GIVEN IN INCHES AND (CM)

Figure 2-4. Clearances - CDC 9762 30-Inch Rack



NOTE 1. DIMENSIONS ARE GIVEN IN INCHES AND (CM).

Figure 2-5. Clearances - CDC 9762 36-Inch Rack Mount

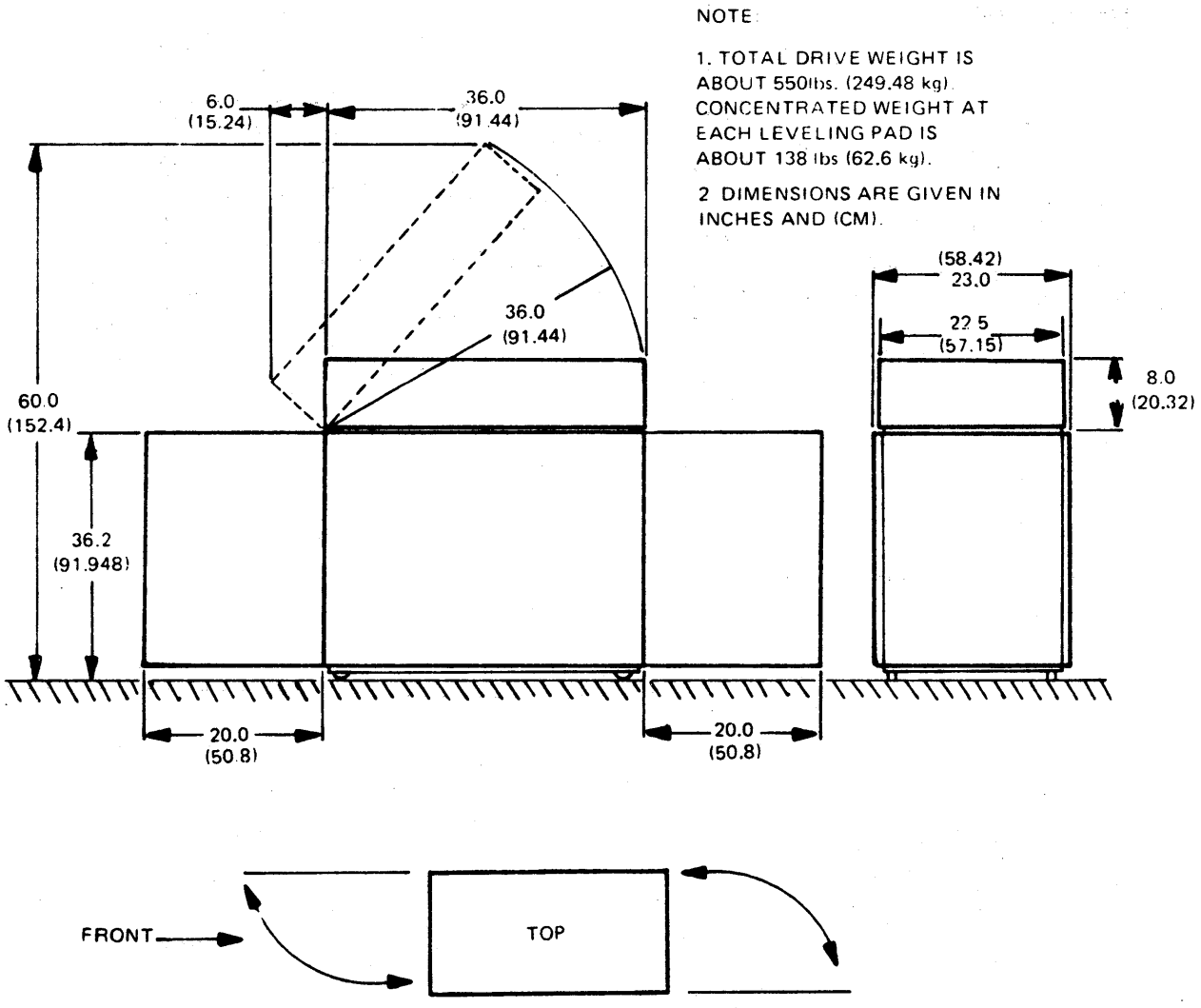


Figure 2-6. Space Requirements - CDC 9766 Drive.

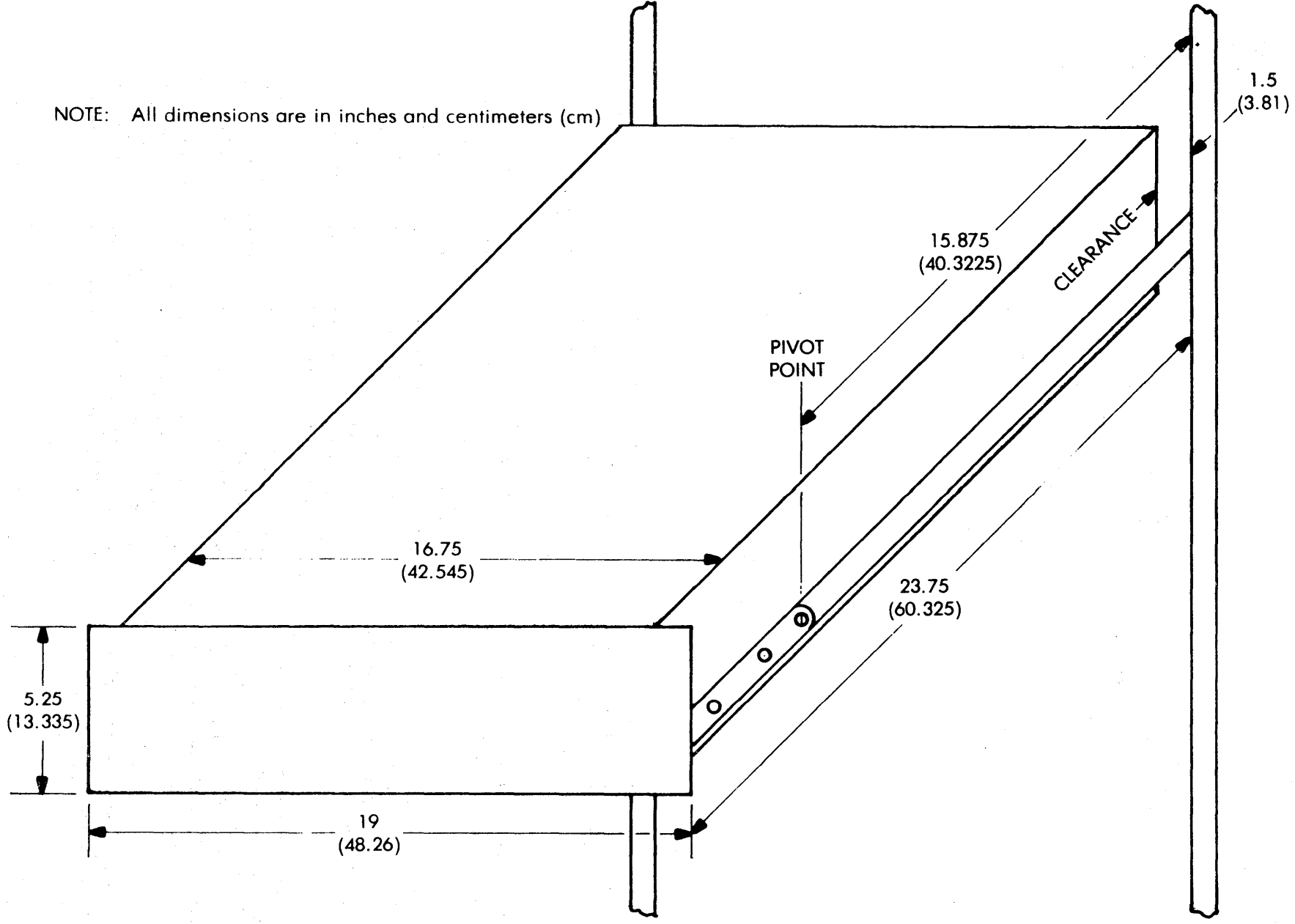


Figure 2-7. Space Requirements - 9400 Controller

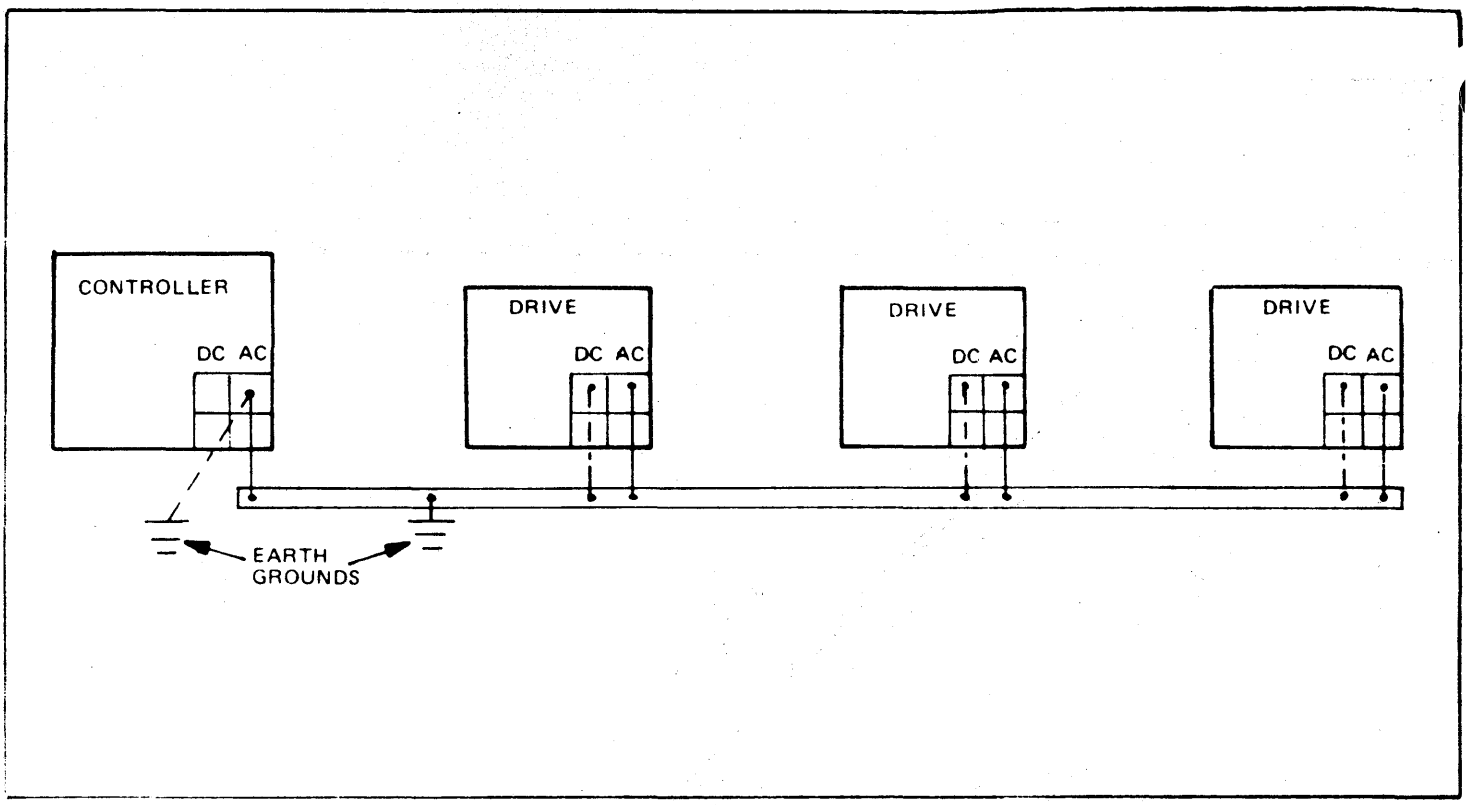


Figure 2-8. Floor Grid Grounding System

2. Controller and drives connected to otherwise qualified floor grid, except that floor grid is isolated from earth ground. In this case, controller is then connected to earth ground to ground the system.

3. No site floor grid available: Controller and drives connected to each other in a daisy chain configuration. Controller connected to earth ground (Figure 2-9).

Special attention should be given to power system grounding. The site AC power system must have provisions for correct equipment safety grounding. To provide a safe AC system, all of the following conditions must be met.

1. The branch circuit supplying AC power to the drive must have safety ground provisions. Therefore, this circuit must include an insulated grounding conductor that is identical to the grounded and ungrounded branch circuit conductors. The insulated ground conductor should be either green or green with a yellow stripe.

2. The grounding conductor specified in Step 1 is to be grounded at the service equipment.

3. The power receptacles must be at a common ground potential to prevent shock hazards if two equipments are touched simultaneously. It is the customer's responsibility to provide a safe AC power for the 9400 System.

2-5. **AC POWER.** All computers and their attached peripherals require clean, noise-free AC power and proper grounding to operate at peak efficiency. In order to ensure the most reliable system operation, System Industries recommends that all components of the computer system be powered from the dedicated secondary of a distribution transformer. A dedicated AC power line will reduce the effects of conducted power line transients that are introduced when other equipment is switched on or off the line.

If for some reason a dedicated distribution system is not feasible, an isolation transformer should be used to protect the system from conducted line transients.

When considering the capacity of the AC power system, it is important to account for the start-up surge of each unit on the line. The start-up surge current of the disk drives is particularly important and is specified in Figures 2-10 and 2-11.

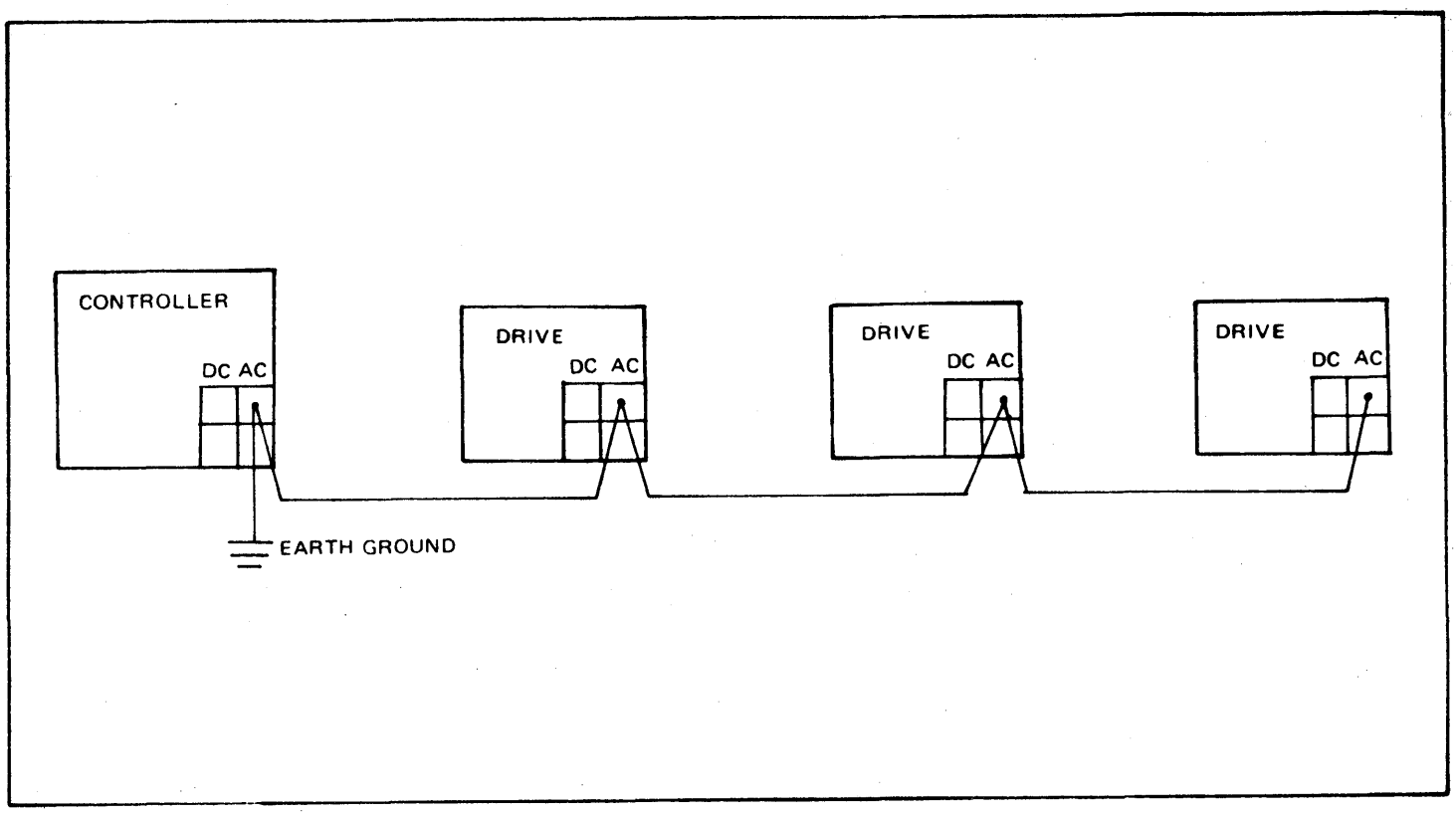


Figure 2-9. Daisy Chain Grounding System

Whenever possible the CPU, 9400 Controller and attached disk drive(s) should be powered from the same AC line in order to avoid ground loops.

2-6. **POWER REQUIREMENTS.** The power requirements of the 9400 Controller and CDC Storage Module Drives are as follows.

a. 9400 Controller. The 9400 Controller requires 115 Vac at 3 amps, and is supplied with a standard grounded duplex connector as shown in Figure 2-12. If the controller is to be used on 230 Vac this connector should be replaced with a suitable 230 volt, single phase connector.

b. CDC 9762 Storage Module Drives. Power requirements of the 9762 Storage Module Drives are listed in Table 2-1. Sixty Hertz drives are supplied with a standard grounded duplex connector as shown in Figure 2-12. Fifty Hertz drives do not come with a power connector. The drive has a 6-foot (182.9 cm) power cable and requires a dedicated 15-amp circuit.

c. CDC 9766 Storage Module Drives. Power requirements of the 9766 Storage Module Drives are listed in Table 2-2. Sixty Hertz drives are supplied with a twist-lock connector as shown in Figure 2-13. The mating female AC outlet is Hubbell Part Number 2326, NEMA configuration L6-20R, Bryant Part Number 70620, Arrow Hart Part Number 6210, or Hubbell Part Number 2320. Fifty Hertz drives are supplied without a connector. The drive has a 6-foot (182.9 cm) power cable and requires a dedicated 20-amp circuit.

2-7. **SHIPPING DAMAGE.** Prior to accepting delivery of the equipment, each shipping container should be carefully inspected for obvious signs of damage. If signs of damage are found, they should be noted on the waybill and signed by the delivering agent. The transfer company must be immediately notified of damage and a damage report submitted to the transfer company and System Industries Customer Service Department. If no obvious exterior damage exists, the boxes should be unpacked as indicated in Paragraph 2-8, and the equipment inspected for hidden damage. If hidden damage is found, immediately notify the transfer company of the damage. Save all packing material for the transfer company's inspection, file a damage report with the transfer company and notify System Industries Customer Service Department of any damage. System Industries is not responsible for damage under warranty. All repairs for shipping damage will be billed. Prompt notification of damage will ensure that the transfer company, or its insurance agent, will pay for all necessary repairs.

2-8. **EQUIPMENT UNPACKING.** The 9400 Controller System will be shipped in several boxes. One box will contain the 9400 Disk Controller, cables, manuals, and rack mounting hardware (Figure 2-15).The box should be carefully opened to avoid damaging the enclosed

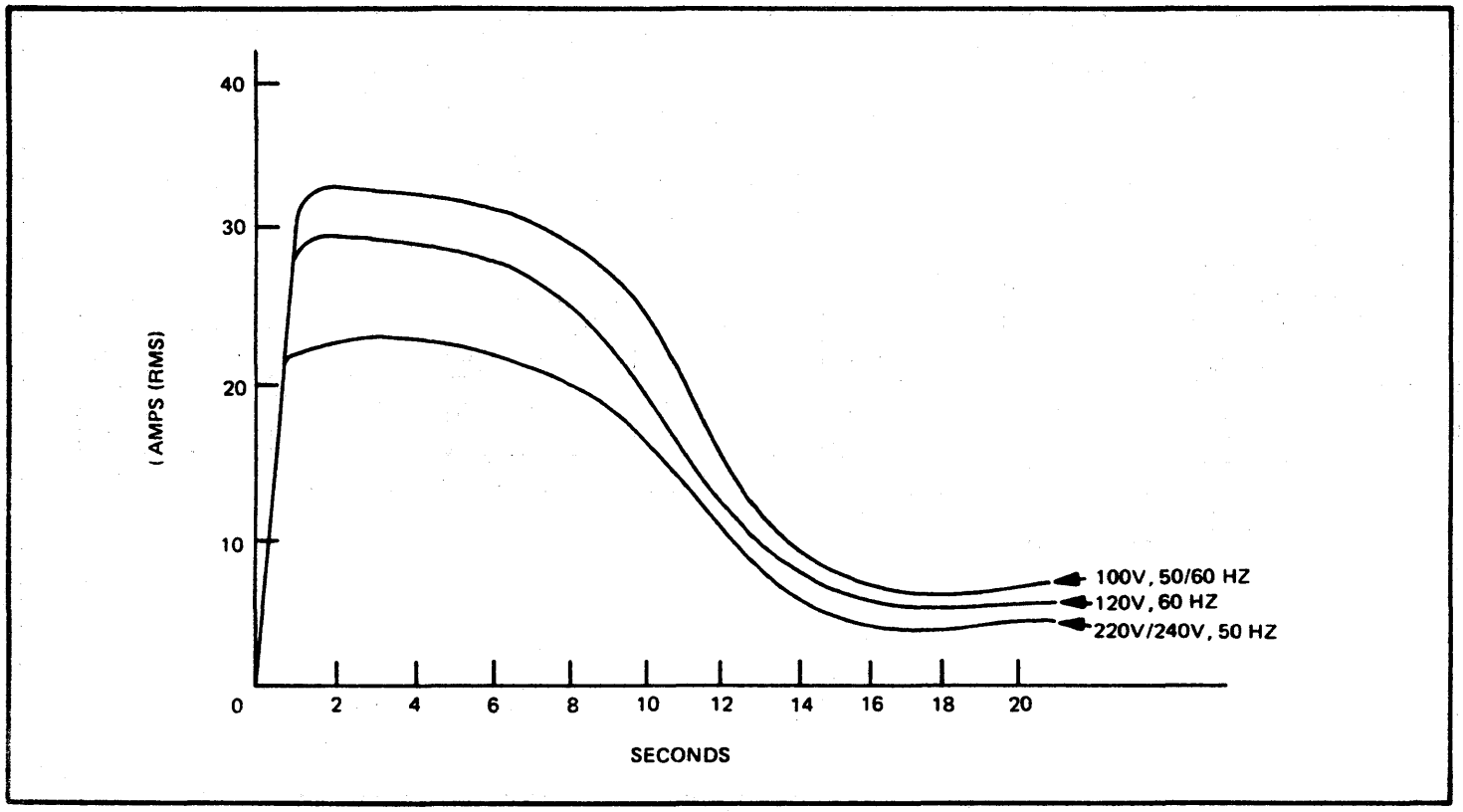


Figure 2-10. 9762 Line Current Versus Start-Up Time

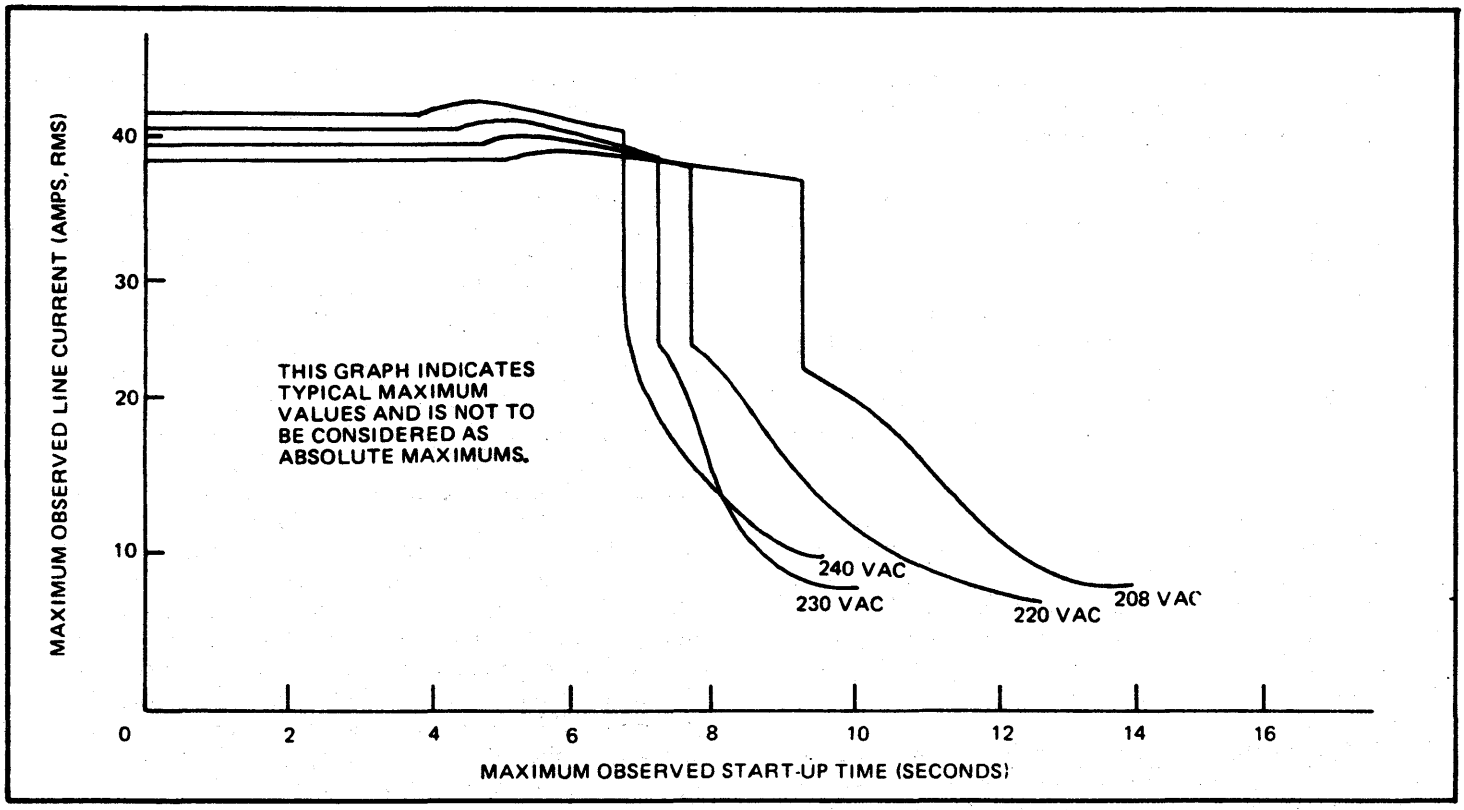


Figure 2-11. 9766 Start-Up Current

Table 2-1. CDC 9762 SMD Functional Characteristics

Temperature	
Operating:	59°F to 90°F (15°C to 32.2°C)
Non-Operating: (In Original Shipping Container)	-40°F to 158°F (-40°C to 70°C)
Maximum Gradient:	12°F (6.7°C) per hour
Humidity	
Operating:	20% to 80% with no condensation
Non-Operating:	5% to 95% with no condensation
Altitude	
Operating:	-1000 to 6500 feet (-305 to 1981 meters)
Non-Operating:	-1000 to 15,000 feet (-305 to 4572 meters)
Power (Single Phase)	
Standby:	100±10 Vac, 60±0.1 Hz, 1.5A, 460 BTU 115±13 Vac, 60±0.1 Hz, 1.5A, 553 BTU 215±20 Vac, 49 to 50.5 Hz, 1.4A, 945 BTU 235±22 Vac, 49 to 50.5 Hz, 1.5A, 1100 BTU
Operating:	100±10 Vac, 60±0.1 Hz, 8.2A, 2150 BTU 115±13 Vac, 60±0.1 Hz, 8.2A, 2580 BTU 215±20 Vac, 49 to 50.5 Hz, 4.2A, 2680 BTU 235±22 Vac, 49 to 50.5 Hz, 5.0A, 3070 BTU

Table 2-2. CDC 9766 SMD Functional Characteristics

Temperature	
Operating:	59°F to 90°F (15°C to 32.2°C)
Non-Operating: (In Original Shipping Container)	-40°F to 158°F (-40°C to 70°C)
Maximum Gradient:	12°F (6.7°C) per hour
Humidity	
Operating:	20% to 80% with no condensation
Non Operating:	5% to 95% with no condensation
Altitude	
Operating:	-1000 to 6500 feet (-305 to 1981 meters)
Non-Operating:	-1000 to 15,000 feet (-305 to 4572 meters)
Power (Single Phase)	
Standby:	400W, 200.8±21.8 Vac, 59 to 60.6 Hz, 2A, 1400 BTU 400W, 222±24 Vac, 59 to 60.6 Hz, 1.8A, 1400 BTU 500W, 216±21 Vac, 49 to 50.5 Hz, 2.5A, 1750 BTU 500W, 235±22 Vac, 49 to 50.5 Hz, 2.3A, 1750 BTU
Operating:	1200W, 200.8±21.8 Vac, 59 to 60 Hz, 8A, 4200 BTU 1200W, 222±24 Vac, 59 to 60.6 Hz, 7.2A, 4200 BTU 1300W, 216±21 Vac, 49 to 50.5 Hz, 9.5A, 4200 BTU 1300W, 235±22 Vac, 49 to 50.5 Hz, 8.7A, 4200 BTU

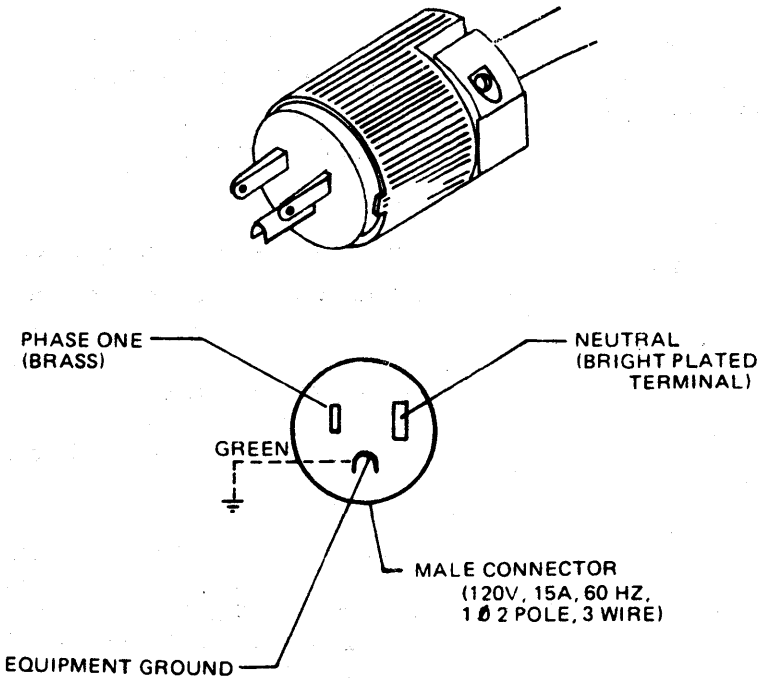
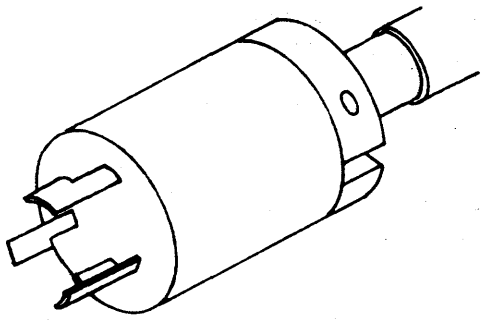


Figure 2-12. CDC 9762 60 Hz AC Power Connector



60 HZ

Figure 2-13. CDC 9766 60 Hz Power Connector

equipment. Save all packaging material for possible reuse in reshipping the system.

2-9. INSTALLATION. The following procedures for installing the 9400 Disk Controller and CDC Storage Drive(s) must be read and understood in its entirety prior to starting the installation. Each step should be followed in the specified sequence to ensure a troublefree installation.

a. Equipment Inspection.

1. Remove the screws securing the top and bottom covers of the 9400 Controller. Remove covers and inspect the controller for any signs of internal damage.

2. Thoroughly inspect the CDC Storage Module Drives for any external or internal signs of shipping damage as indicated in the CDC Storage Module Drive Installation and Checkout Manual.

b. SMD Checkout.

1. Check setting of sector switches on LTV card in CDC drive. Card is in position A06 for 9766 (300 Mb) SMDs, and position B08 for 9762 (80 Mb) SMDs. Sector switches should be set as follows:

33 Sectors		32 Sectors	
0	Open	0	Closed
1	Closed	1	Closed
2	Closed	2	Open
3	Open	3	Open
4	Closed	4	Open
5	Open	5	Closed
6	Open	6	Open
7	Closed	7	Closed
8	Closed	8	Closed
9	Open	9	Open
10	Open	10	Open
11	Open	11	Open

Switches are numbered in etch along top edge of board.

NOTE

Drive is set for 32 sectors for checkout with CDC Field Test Unit TB304, and set for 33 sectors when used with the 9400.

2. Set all circuit breakers to off and connect CDC Storage Module Drives to ground and power, as indicated in the CDC Storage Module Drive Installation and Checkout Manual.

3. Perform the Clean Shroud on Spindle Procedures called out in the Preventive Maintenance section of the CDC Manual.

4. Set all circuit breakers to ON, and verify that the SMD blower starts. Allow blower to operate for at least ten minutes before proceeding to Step 5.

5. Install scratch disk pack.

6. Press START switch on the CDC SMD and verify the following:

a) START indicator lights.

b) Drive motor and disk pack come up to speed in approximately 30 seconds.

c) Heads load when disk pack comes up to speed, and READY indicator lights.

7. Connect CDC Field Test Unit TB304 (CDC P/N 77449300) to Storage Module Drive and exercise the head positioner.

8. Press START switch on the SMD and wait for the disk pack to stop spinning. Remove the scratch pack and mount a CDC CE disk pack.

9. Press START switch on the SMD and perform alignment checks as called out in the CDC Storage Module Drive Installation and Checkout Manual.

10. After completion of tests, press the START switch on the SMD and wait for the disk pack to stop spinning. Remove the CE pack from the SMD and store the pack in a safe place.

11. Reset sector switches for 33 sectors as indicated in Step 1.

c. 9400 Controller Mechanical Installation.

1. Attach the rack slides to the controller and to the cabinet with the hardware supplied as shown in Figure 2-16. Rack slide extensions are provided for use on nonstandard cabinets. Ensure adequate clearance between the controller and other devices in the cabinet, so that the controller may be extended from the cabinet.

NOTE

The lengths of the cables from the controller to the Computer Port Adapter card are 10 or 35 feet long. Therefore, the controller should be mounted in the equipment cabinet as close as possible to the CPU or Small Peripheral Extension Cabinet, where the Computer Port Adapter card is to be installed.

2. Insert the controller into the cabinet rack slides and extend the controller from the cabinet.

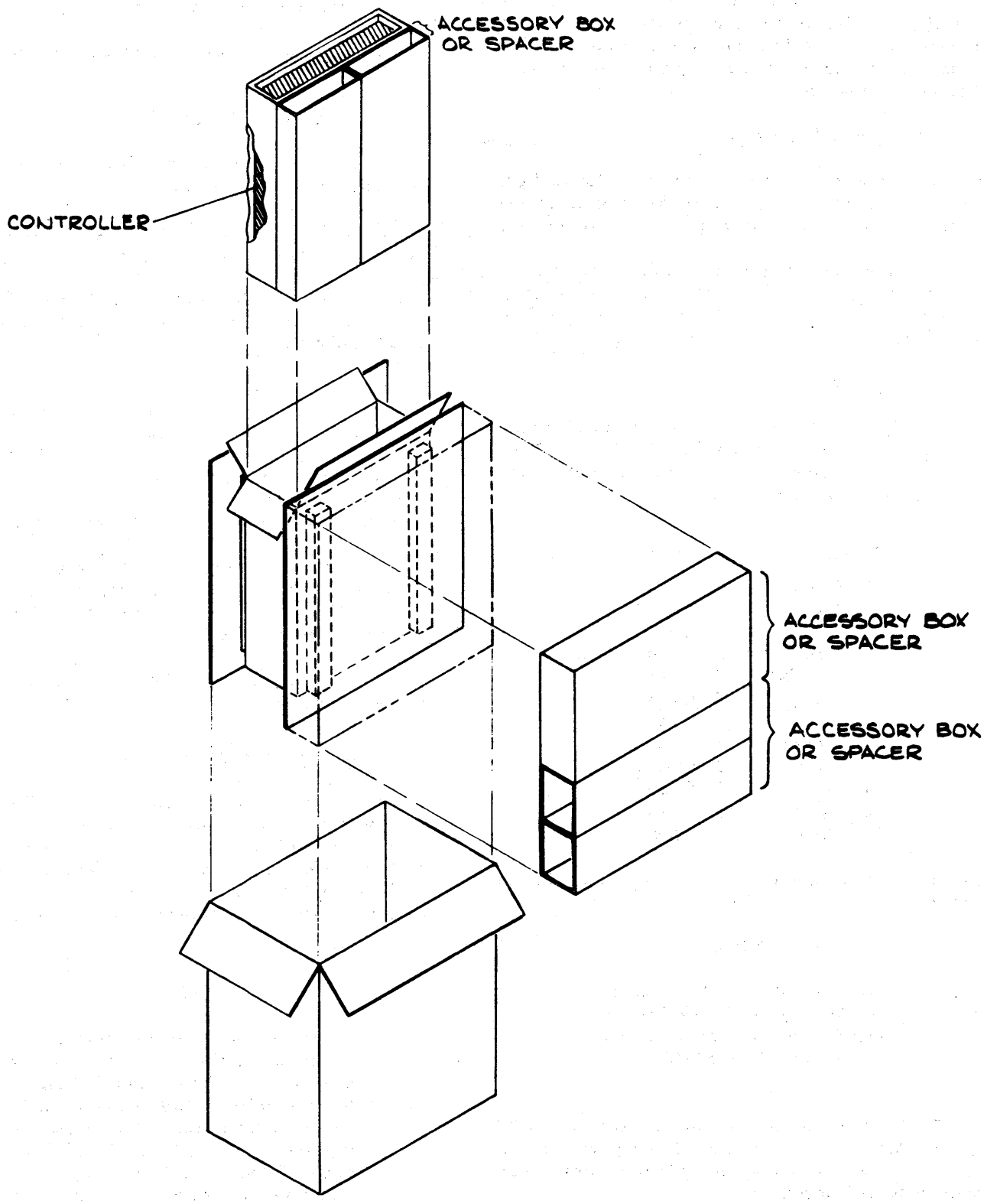


Figure 2-15. 9400 Controller Packing

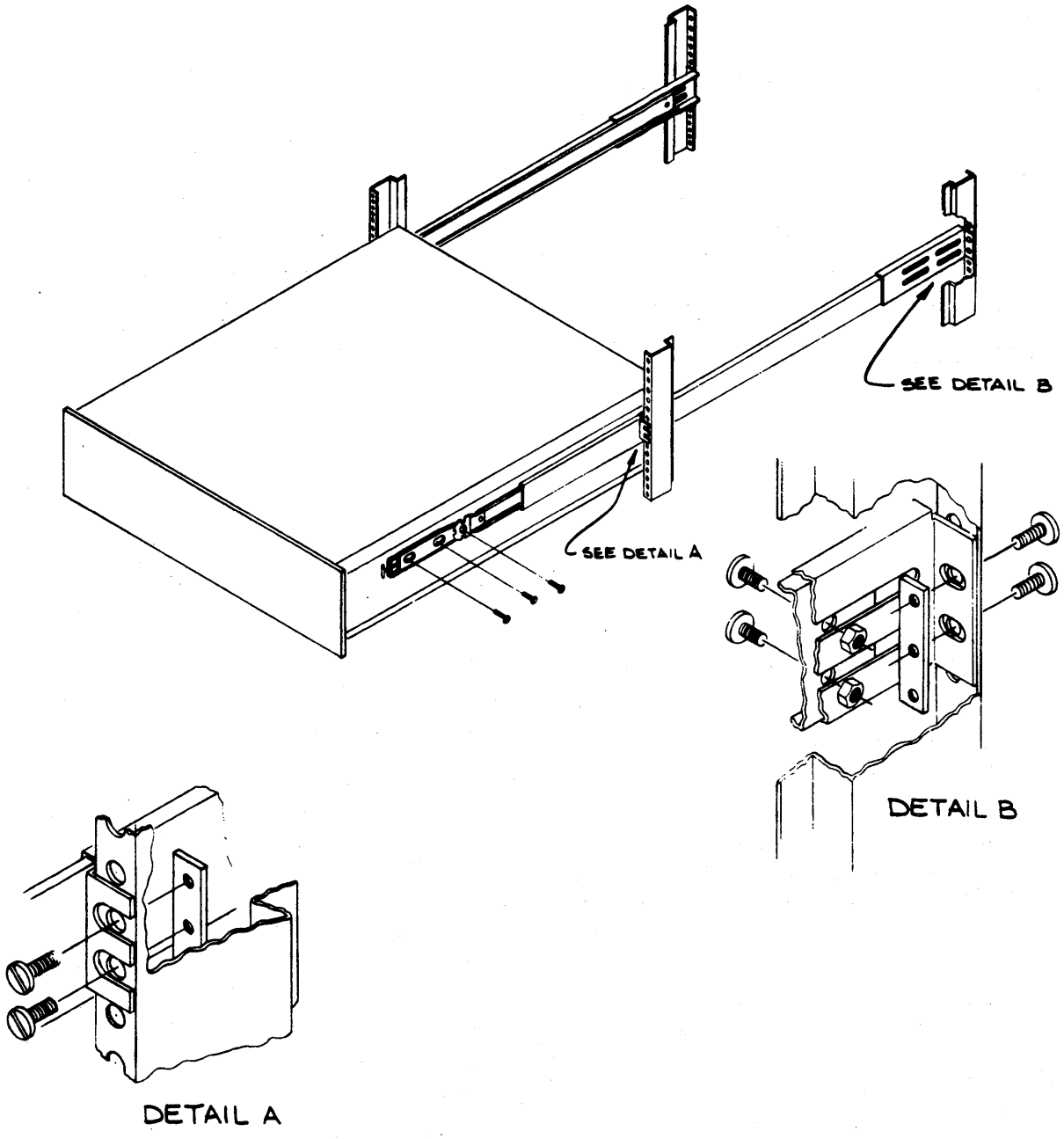


Figure 2-16. 9400 System Installation

3. Ensure that the circuit card assemblies are properly seated, and inspect the interior of the Controller for any signs of damage.

d. SMD Installation. (Radial)

1. Remove knurled nuts from posts holding down Drive Interface board(s) (P/N 9400-6008) (Figure 2-17). Gently pull out from board(s) the black Zero-Insertion-Force connector locking lever, and remove board(s).

NOTE

If drive being installed is Dual Channel, and the Drive Interface board is a 9400-6008, jumper W9 on the Drive Interface Board must be removed. Jumper W9 is not changed on 9400-6028, and 9400-6038.

2. Install cable P/N 3225-7007 from CDC Storage Module Drive connector 1J3 (Figure 2-17) to Drive Interface board (P/N 9400-6008) connector P1. Refer to Figure 2-17 for Controller board locations and Drive Interface board cable connection.

3. Install cable P/N 3225-7008 from CDC Storage Module Drive connector 1J2 to Drive Interface board connector P2.

4. Plug CDC terminator on Storage Module Drive connector 1J4.

5. Install Logical Address Plug 0 into the switch receptacle under the READY indicator on the CDC Storage Module Drive front panel

6. Set the Port Attention/Port Selection switch U210 on the Drive Interface board (P/N 9400-6008) (Figure 2-18) for Port 0 as follows: Set switch 1 (as marked on the DIP switch) to ON. Set switches 2, 3, 4, 5, and 6 to OFF.

7. Set the Drive Model switch U612 on the Drive Interface board for the proper model as follows:

a) For 9762 (80 Mb) SMD.

S8 ON
S7 OFF
S6 OFF
S5 OFF
S4 OFF
S3 OFF
S2 OFF
S1 ON

NOTE

If drive is to be run unmapped (direct) S7 must be ON.

b) For 9766 (300 Mb) SMD.

S8 ON
S7 OFF
S6 OFF
S5 OFF
S4 OFF
S3 OFF
S2 ON
S1 ON

NOTE

Switch numbers called out in this step are as marked on the DIP switch and do not correlate with switch numbers as marked on the logic diagrams.

8. Ensure that the Zero-Insertion-Force (ZIF) connector locking lever is pulled out on the Drive Interface board and install the board into the 9400 Controller. Lock the ZIF connector by pushing in on the locking lever.

9. Most Storage Module Drives have the Index and Sector signals in the A-cable, and jumpers W1, W4, W5, and W8 will be installed on the Drive Interface board. If a drive is used that has the Index and Sector signals in the B-cable, jumpers W1, W4, W5, and W8 must be removed, and jumpers W2, W3, W6, and W7 must be installed.

10. If only one drive is to be installed, proceed to Step 11. If more than one drive is to be installed proceed to Step 12.

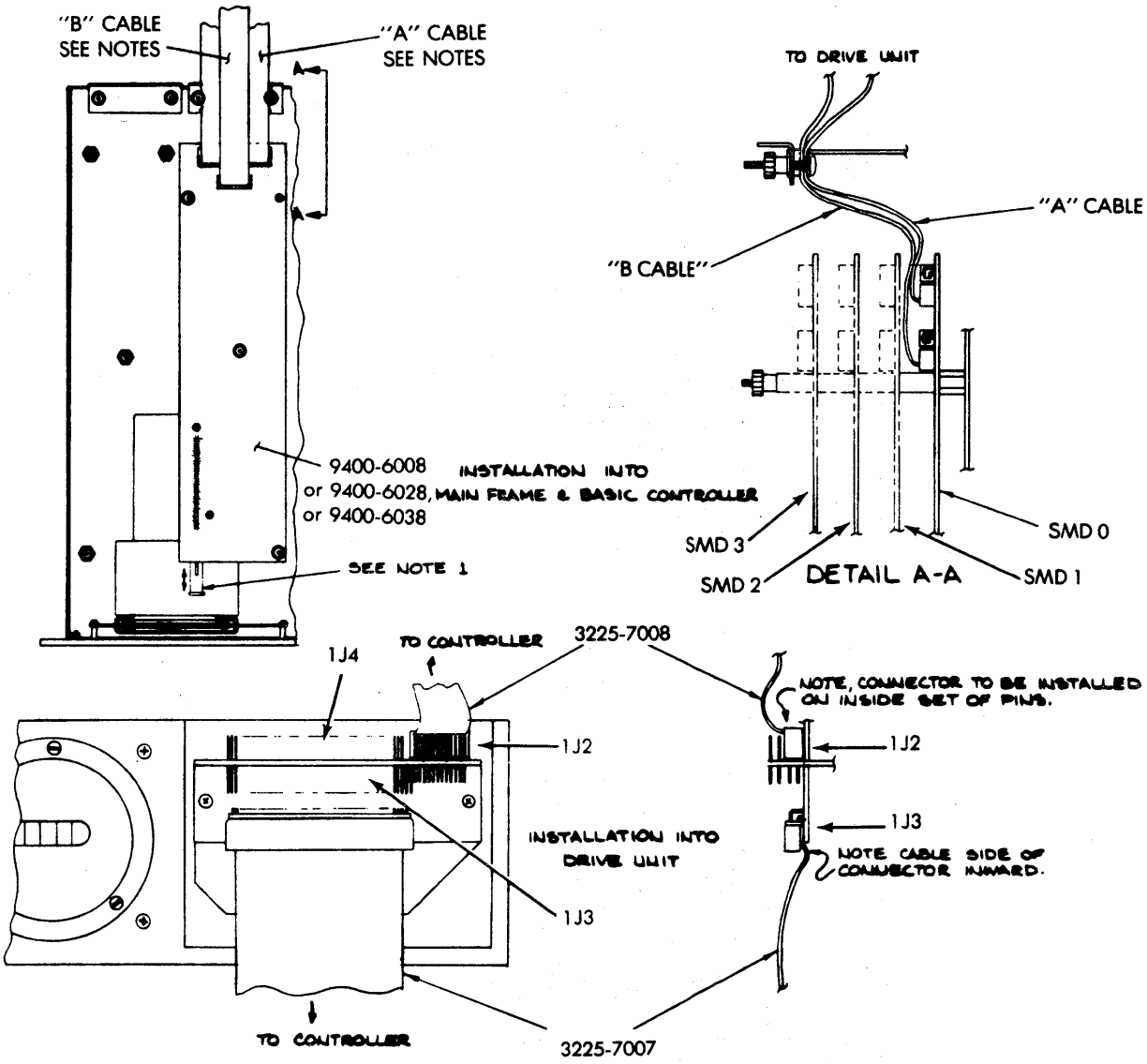
11. Install nuts on support rods to hold down the Drive Interface board and route cables through the cable hold-down at rear of the 9400 Controller. Proceed to Paragraph e, 9400 Controller Electrical Installation.

12. To install second drive, perform Steps 2 through 4 for second Storage Module Drive and second Drive Interface board.

13. Install Logical Address Plug 1 into the switch receptacle under the READY indicator on the second Storage Module Drive front panel.

14. Set the Port Attention/Port Selection switch U210 on the Drive Interface board for Port 1 as follows: Set switch S1 (as marked on DIP switch) to OFF, S2 to ON, S3 and S4 to OFF, S5 to ON, and S6 to OFF.

15. Set the Drive Model switch U612 as instructed in Step 7.



NOTES:

1. Push slowly to lock connector closed. Pull gently to open connector.
2. "A" Cable for flat cable (BK) SMD may be P/N 3225-7007 (16'), or P/N 3225-7009 (32'), or P/N 3225-7011 (48').
3. "B" Cable for flat cable (BK) SMD may be P/N 3225-7008 (16'), or P/N 3225-7010 (32'), or P/N 3225-7012 (48').
4. "A Cable" used with 9400-6028 and round cable (BJ) SMD may be P/N 3225-7034 (16'), or P/N 3225-7036 (30'), or P/N 3225-7038 (50').
5. "B" Cable used with 9400-6028 and round cable (BJ) SMD may be P/N 3225-7035 (16'), or P/N 3225-7037 (30'), or P/N 3225-7039 (50').

Figure 2-17. Drive Interface Feature Installation

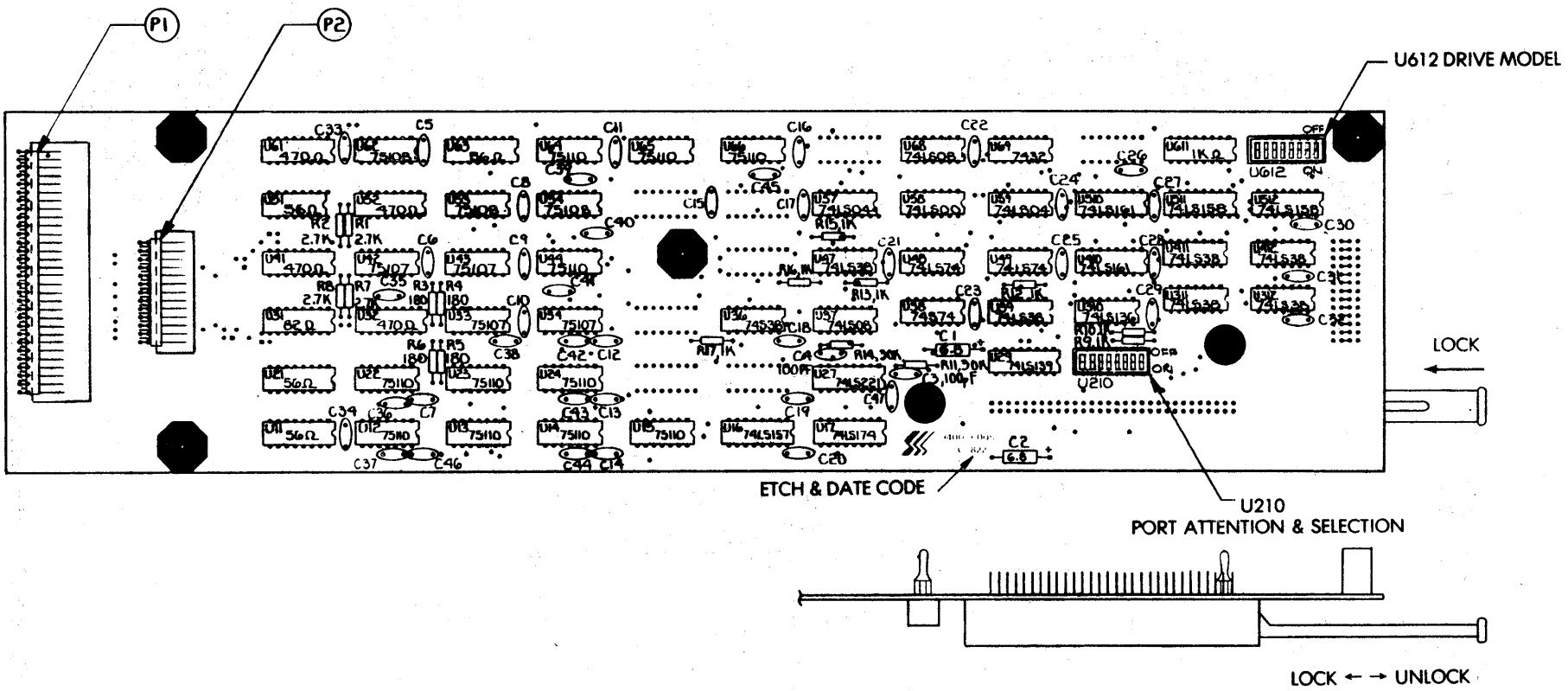


Figure 2-18. SMD Interface Switch Locations

16. Install the Drive Interface board in the 9400 Controller as instructed in Step 8. If no more drives are to be installed, proceed to Step 27.

17. To install a third drive, perform Steps 2 through 4 for third Storage Module Drive and third Drive Interface board.

18. Install Logical Address Plug 2 into the switch receptacle under the READY indicator on the third Storage Module Drive front panel

19. Set the Port Attention/Port Selection switch U210 on the Drive Interface board for Port 2 as follows: Set switches S1 and S2 (as marked on DIP switch) to OFF, S3 to ON, S4 and S5 to OFF and S6 to ON.

20. Set the Drive Model switch U612 as instructed in Step 7.

21. Install the Drive Interface board in the 9400 Controller as instructed in Step 8. If no more drives are to be installed, proceed to Step 27.

22. To install a fourth drive, perform Steps 2 through 4 for fourth Storage Module Drive and fourth Drive Interface board.

23. Install Logical Address Plug 3 into the switch receptacle under the READY indicator on the fourth Storage Module Drive front panel

24. Set the Port Attention/Port Selection switch U210 on the Drive Interface board for Port 3 as follows: Set switches S1, S2, and S3 (as marked on DIP switch) to OFF; S4, S5, and S6 to ON.

25. Set the Drive Model switch U612 as instructed in Step 7.

26. Install the Drive Interface board in the 9400 Controller as instructed in Step 8.

27. Route the SMD cables through the cable hold-down at the rear of the 9400 Controller. Install nuts on support rods to hold down the Drive Interface boards, and tighten nuts on board and cable hold-downs.

e. 9400 Controller Electrical Installation.

1. Remove knurled nuts from posts holding down Computer Interface board(s) (P/N 9400-6007) (Figure 2-19). Gently pull out from board(s) the black ZIF connector locking lever, and remove board(s).

2. Install cable P/N 9400-7007 from RP04 Computer Port Adapter board (P/N 9400-6011) connector J1 to Computer Interface board (P/N 9400-6007) connector J1.

3. Install cable P/N 9400-7007 from RP04 Computer Port Adapter board connector J2, to Computer Interface board connector J2.

4. Set the UNIBUS Address switch 2B, on the Computer Port Adapter board (Figure 2-20) as follows:

Primary 776700	Secondary 776300
1. N.C.	1. N.C.
2. OFF	2. OFF
3. OFF	3. OFF
4. OFF	4. OFF
5. ON	5. ON
6. OFF	6. ON
7. OFF	7. OFF
8. OFF	8. OFF

5. Set the Interrupt Vector switch 5J, on the Computer Port Adapter board (Figure 2-20) as follows:

Primary Vector 254	Secondary Vector 150
1. N.C.	1. N.C.
2. OFF	2. ON
3. ON	3. OFF
4. OFF	4. OFF
5. ON	5. ON
6. OFF	6. OFF
7. OFF	7. ON
8. ON	8. ON

6. Set the Throttle Count switch 11R, on the Computer Port Adapter board (Figure 2-20) for a one, two, four, or eight word transfer as follows:

S4	S3	S2	S1	Transfer
ON	OFF	OFF	OFF	1
OFF	ON	OFF	OFF	2
OFF	OFF	ON	OFF	4
OFF	OFF	OFF	ON	8

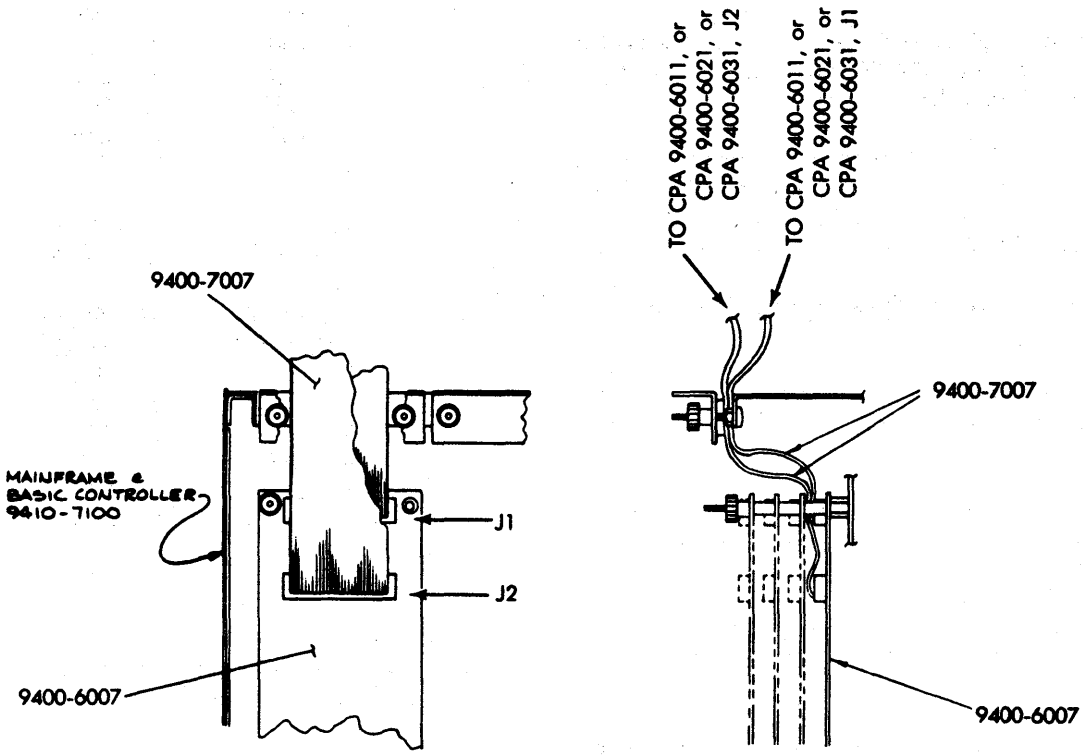
7. Check the Bus Request jumper W6 on the Computer Port Adapter board. Normal priority is BR5, which requires that jumper W6 is connected to 10. For BR4, W6 would connect to 9, for BR6 to 11, and for BR7 to 12.

8. Check the Bus Grant jumpers W1, W2, W3, W4, W5, and W7 on the Computer Port Adapter board. Normal priority is BG5, which requires that W1 be connected to 2; W2, W4, and W5 be installed; W3 should not be installed; and W7 should be connected to 7.

Other priorities are as follows:

Priority	W1	W2	W3	W4	W5	W7
4	1	OUT	IN	IN	IN	8
6	3	IN	IN	OUT	IN	6
7	4	IN	IN	IN	OUT	5

9. For 9400 Controllers with a 9400-6011 Computer Port Adapter circuit card assembly installed, check MASSBUS/UNIBUS NPR jumper W8 on the Computer Port Adapter circuit card assembly. W8 must be connected to B for systems transferring data on the



NOTES:

1. Cables may be P/N 9400-7007 (10'), or P/N 9400-7008 (20' obsolete), or P/N 9400-7013 (35').

Figure 2-19. CPU Interface Feature Installation

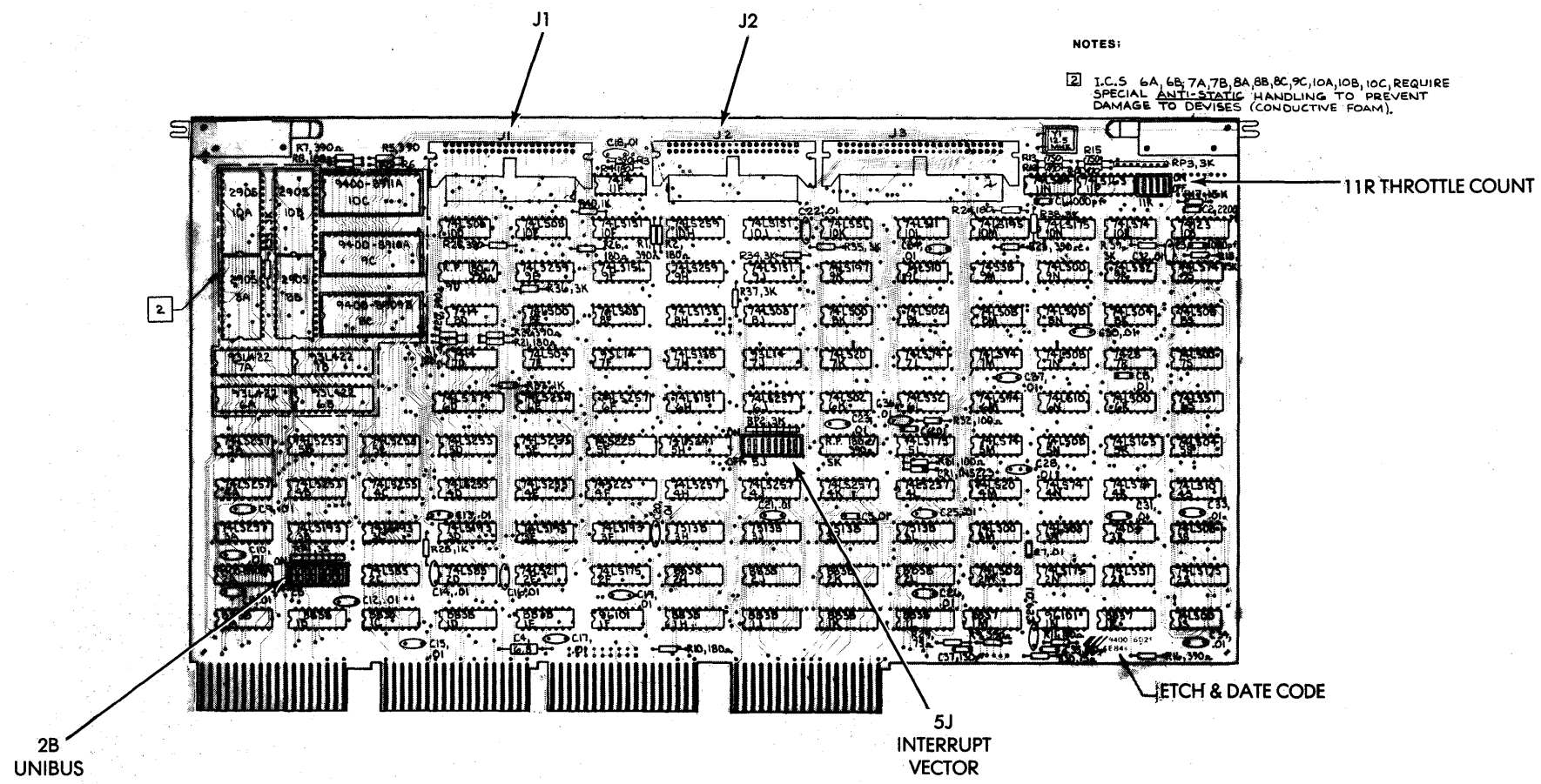


Figure 2-20. CPA Switch Locations

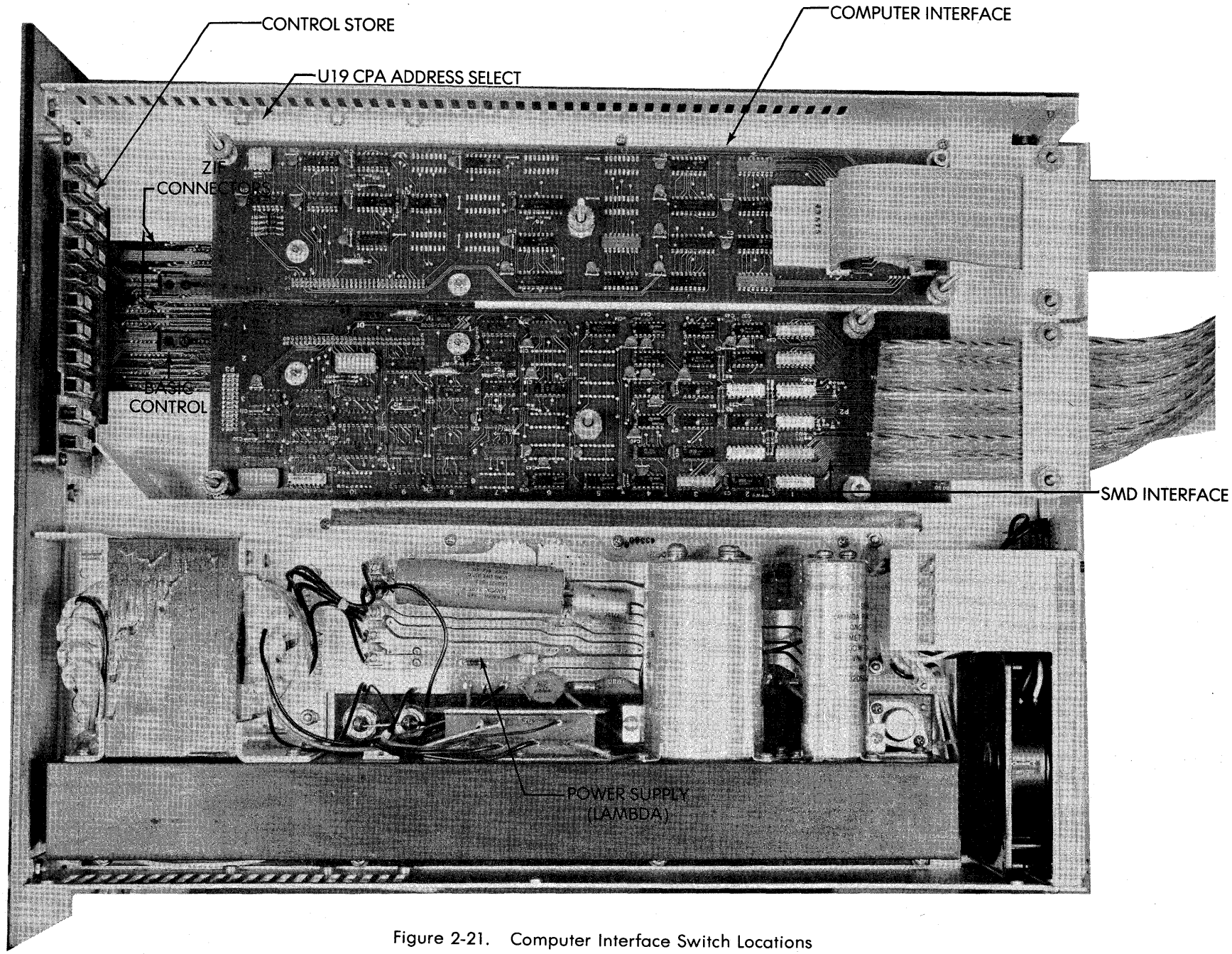


Figure 2-21. Computer Interface Switch Locations

UNIBUS, and connected to A for systems transferring data on a Cache Memory bus (PDP-11/70 with optional System Industries' Cache Memory Interface). Normal connection is W8 to B.

NOTE

The following portion of this step is applicable only to 9400-6021 or 9400-6031 circuit card assemblies installed in a PDP-11/70 equipped with the RH70 Cache Memory Interface.

When a 9400-6021 or 9400-6031 Computer Port Adapter circuit card assembly is installed in a spare SPC slot of a PDP-11/70 equipped with a Cache Memory Interface, the SPC slot CAI to CBI backplane jumper need not be cut. Instead, cut the W8 link (NPG line) etched on the 9400-6021 or 9400-6031 circuit card assembly so the 9400 Controller can communicate directly with the Cache Memory bus for data transfers. If the SPC slot CAI to CBI backplane jumper is already cut, do not cut link W8 on the 9400-6021 or 9400-6031 circuit card assembly. Refer to Chapter 10 of this manual for more information concerning the PDP-11/70 Cache Bus Interface.

10. Set the CPA Address Selection switch U19 on the Computer Interface board (P/N 9400-6007) (Figure 2-21) for CPA 0 as follows: Set S1 and S2 to OFF.

11. Ensure that the ZIF connector locking lever is pulled out on the Computer Interface board and install the board into the 9400 Controller. Lock the ZIF connector by pushing in on the locking lever.

12. If only one computer is to be connected to the 9400 Controller, proceed to Step 13. If more than one computer is to be connected to the 9400 Controller, proceed to Step 14.

13. Install nuts on support rods to hold down the Computer Interface board and route cables through the cable hold-down at rear of the 9400 Controller. Proceed to Step 24.

14. To connect the 9400 Controller to the second computer, perform Steps 2 through 9 for the second Computer Port Adapter, and Computer Interface boards.

15. Set the CPA Address Selection switch U19 on the second Computer Interface board for CPA 1 as follows: Set S1 to OFF, and S2 to ON.

16. Install the Computer Interface board in the 9400 Controller as instructed in Step 11. If no more computers are to be connected to the 9400 Controller, proceed to Step 23.

17. To connect the 9400 Controller to the third computer, perform Steps 2 through 9 for the third Computer Port Adapter, and Computer Interface boards.

18. Set the CPA Address Selection switch U19 on the third Computer Interface board for CPA 2 as follows: Set S1 to ON, and S2 to OFF.

19. Install the Computer Interface board in the 9400 Controller as instructed in Step 11. If no more computers are to be connected to the 9400 Controller, proceed to Step 23.

20. To connect the 9400 Controller to the fourth computer, perform Steps 2 through 9 for the fourth Computer Port Adapter, and Computer Interface boards.

21. Set the CPA Address Selection switch U19 on the fourth Computer Interface board for CPA 3 as follows: Set S1 to ON, and S2 to ON.

22. Install the Computer Interface board in the 9400 Controller as instructed in Step 11.

23. Route the cables through the cable hold-down at the rear of the 9400 Controller. Install nuts on support rods to hold down the Computer Interface boards, and tighten nuts on board and cable hold-down.

24. Check the Data Word Length Selection jumpers W4, W5, W6, W7, W8, and W9 on the Basic Control board (P/N 9400-6004) (Figure 2-22). Standard word length is 16 bits; and requires that jumpers W4, W5, W6, W7, W8, and W9 be installed, and that no jumpers are installed across IC 1H pins 1, 2, 4, and 5. For other word lengths the jumpers must be as follows:

a) For 12-bit word.
W4 OUT
W5 IN
W6 IN
W7 IN
W8 OUT
W9 OUT

Jumper together IC 1H pins 1, 2, and 4.

b) For 8-bit word.
W4 IN
W5 OUT
W6 IN
W7 OUT
W8 OUT
W9 OUT

Jumper together IC 1H pins 1, 2, 4, and 5.

f. PDP-11 Computer Connection.

1. Turn off all power to PDP-11 computer(s).

2. Plug Computer Port Adapter board(s) into Small Peripheral Controller (SPC) slot in computer(s). One CPA board per computer. CPA board(s) must be plugged in front of any Bus Repeaters. 9400 Controllers plugged in after a Bus Repeater will not operate properly.

3. Modify PDP-11 SPC backplane wiring as follows (refer to Figure 2-23 for pin identification):

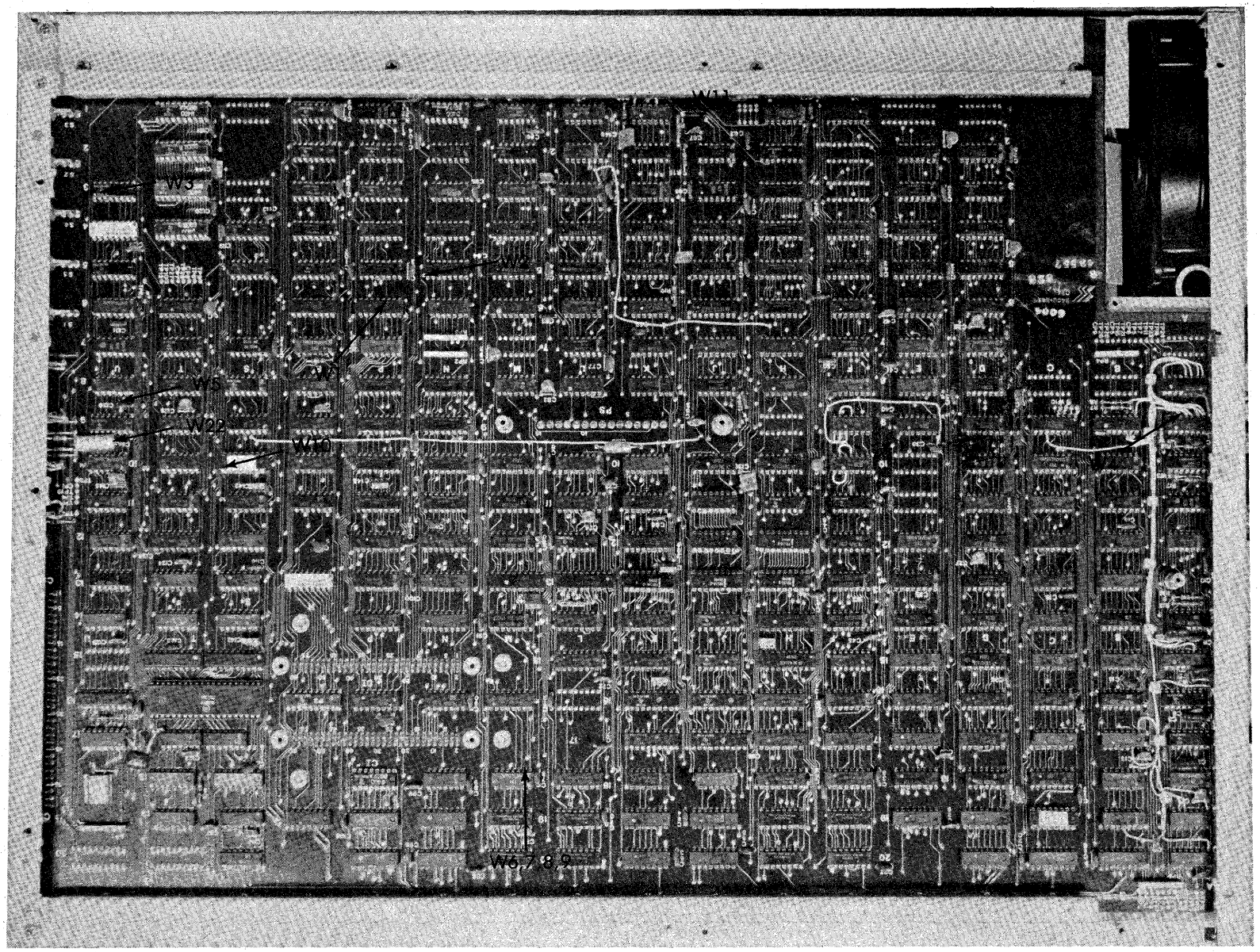


Figure 2-22. Basic Control Board Jumpers

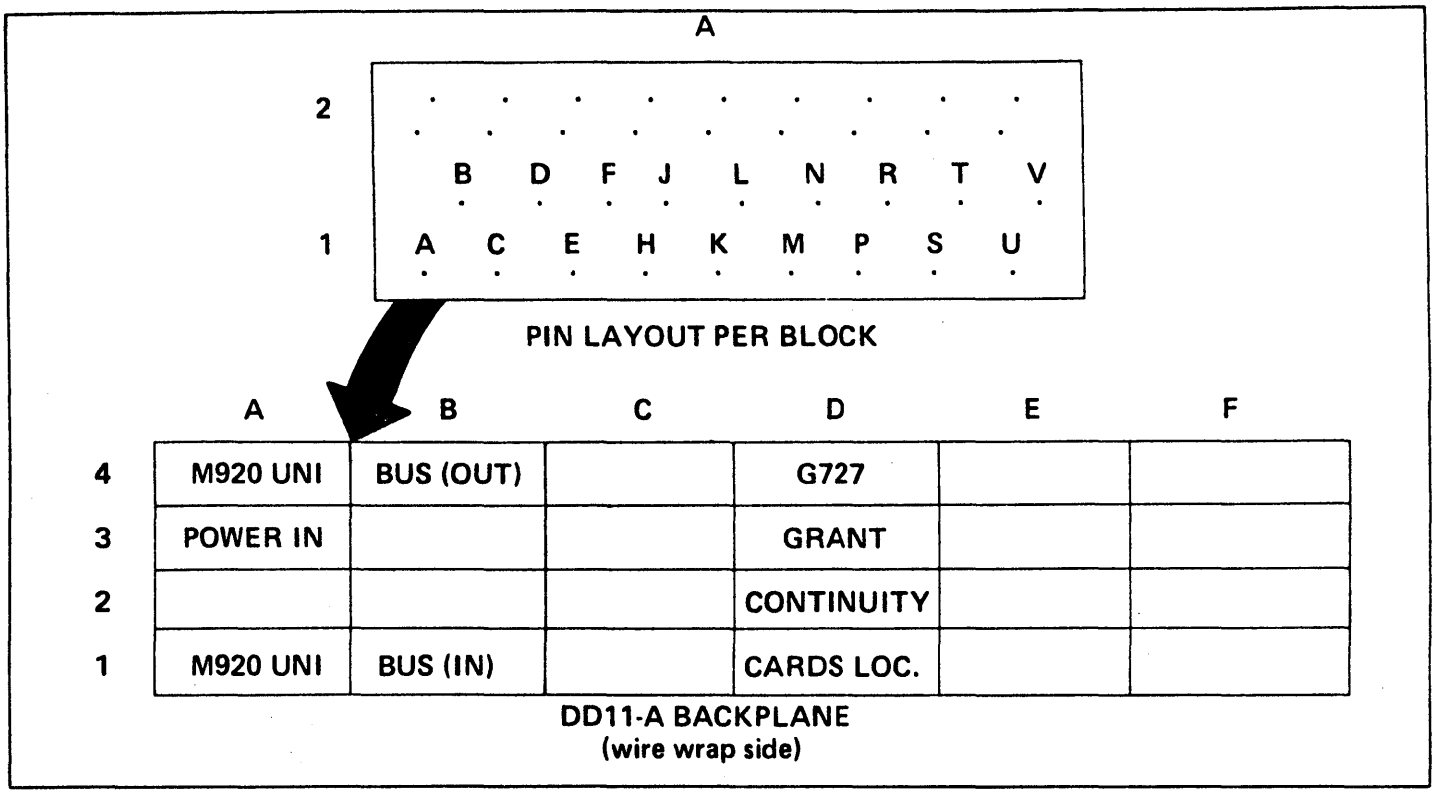


Figure 2-23. SPC Backplane

a) SPC Backplane type DD11-A.

Wiring changes using slot 1 for CIB.

Delete	Add	Signal
A01U1 to A04U1	A01U1 to C01A1	NPG IN
C01A1 to C02A1	C01B1 to A04U1	NPG OUT
C01B1 to C02B1	*F01J1 to A04S2	NPR
	B01F1 to C01V1	ACLO

*Check to see if this connection is installed.

b) SPC Backplane types DD11-B, DD11-C, and RH11.

Wiring changes using slot 1 for CIB

Delete	Adds
C01A1 to C01B1	None

Check the following wiring for continuity.

From A01U1 to C01A1
C01B1 to C02A1
C02A1 to C02B1 to A04U1

4. Connect ground straps from drives and controllers to system ground.

5. For RH70 (Cache) installation, refer to Chapter 10.

6. Connect 9400 Controller power cord to AC Power.

7. Apply power to Storage Module Drive(s).

8. Apply power to 9400 Controller.

9. Apply power to PDP-11 Computer(s).

10. Set 9400 Controller ON LINE switch to ON, FORMAT switch to OFF, and MODE switch to STD.

11. Perform checkout and diagnostic procedures in Chapter 4.

CHAPTER 3
OPERATION

3-1. **INTRODUCTION.** This chapter contains illustrations and listings of the Series 9400 Disk Controller controls and indicators as well as equipment turn-on and turn-off procedures.

3-2. **CONTROLS AND INDICATORS.** Refer to Figure 3-1 and Table 3-1 for the Series 9400 Disk Controller front panel controls and indicators; and to Figure 3-2 and Table 3-2 for the Series 9400 Disk Controller rear panel controls and indicators.

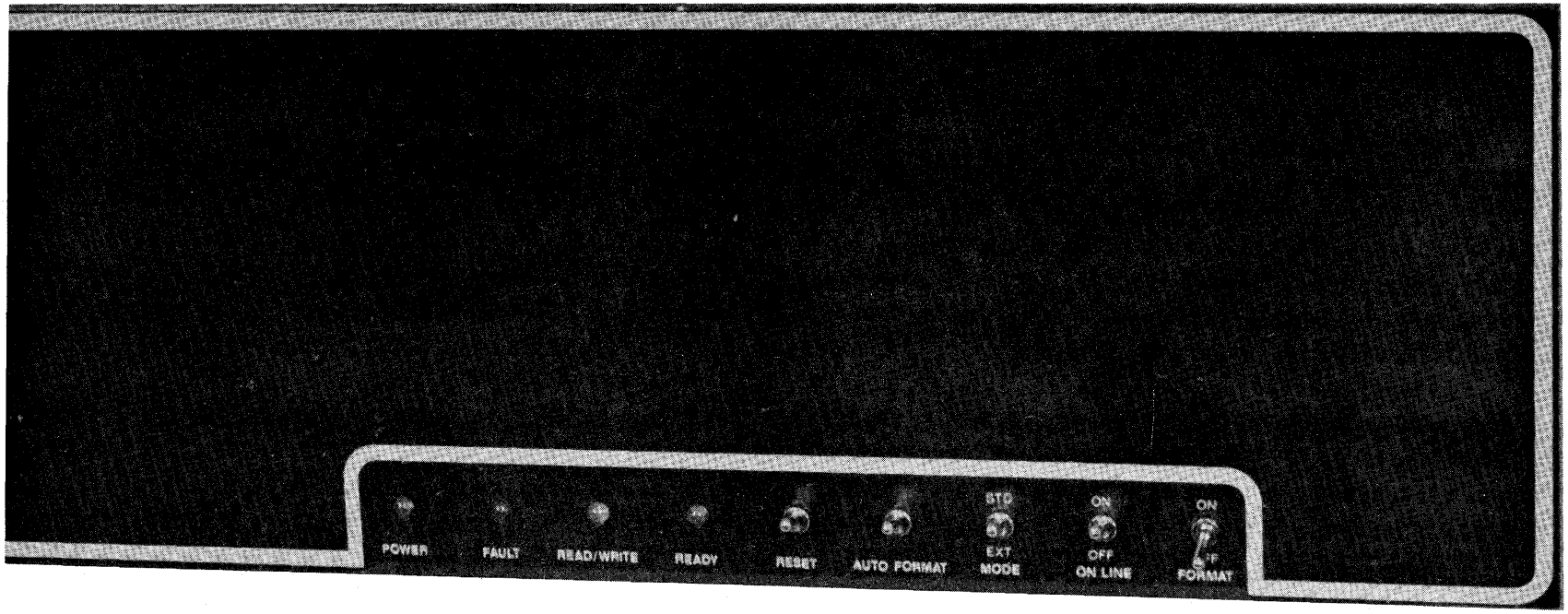


Figure 3-1. Series 9400 Disk Controller Controls and Indicators, Front Panel

Table 3-1. Front Panel Controls and Indicators

NOMENCLATURE	POSITION	FUNCTION
FORMAT Switch	ON	Disk can be formatted or a write protected sector rewritten.
	OFF	Rejects format commands. Attempts to write protected sectors are aborted and appropriate status is reported.
ON LINE switch	ON	Normal system operation. Microdiagnostics execute if the RESET switch is activated.
	OFF	Enables AUTO FORMAT switch.
MODE switch	Standard	Provides standard emulation upon power-up or reset.
	Extended	Provides extended emulation upon power-up or reset. See options in Chapter 1. Requires system operating software changes.
AUTO FORMAT Switch	DOWN (Momentary Contact)	Formats drives off-line if ON LINE Switch is OFF and optional firmware is installed.
	UP	Normal System Operation.
RESET Switch	Momentary Contact	Reset microprocessor initiating restart routine.
POWER ON Indicator	Illuminated	Indicates DC power is is present.
READY Indicator	Illuminated	Indicates controller is ready for system usage. If indicator remains off, a microdiagnostic fault may have been detected.
FAULT Indicator	Illuminated	Positively indicates a fault has been found in the controller by the microdiagnostic or microcontrol.
READ/WRITE Indicator	Illuminated	Indicates controller is performing a read or write operation.

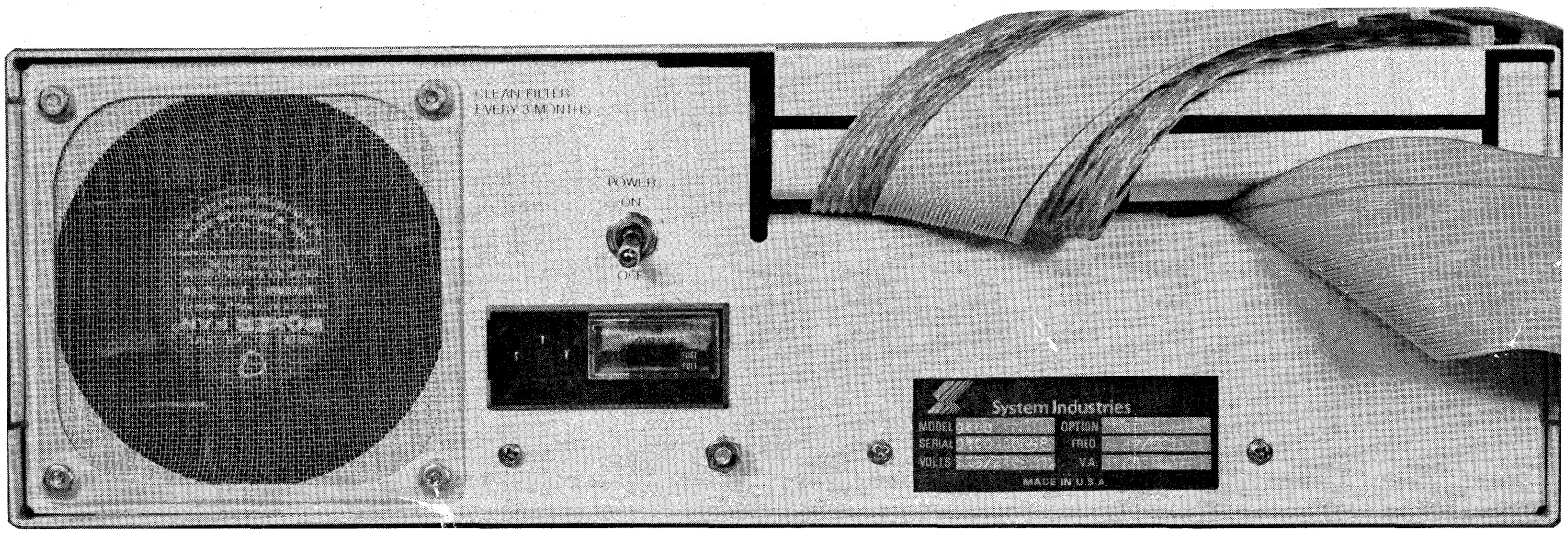


Figure 3-2. Series 9400 Disk Controller Controls and Indicators, Rear Panel

Table 3-2. Rear Panel Controls and Indicators

NOMENCLATURE	POSITION	FUNCTION
AC Switch	ON	Provides AC power to the controller.
	OFF	Disables AC power to the controller.

CHAPTER 4

DIAGNOSTICS AND CHECKOUT

4-1. INTRODUCTION. This chapter contains information and procedures to set up, run, and interpret mainframe diagnostics supplied by System Industries.

4-2. 94EXOR--9400 EXERCISER OPERATING INSTRUCTIONS.

a. Loading and Starting 94EXOR. 94EXOR is supplied as a paper tape. It is also available at extra cost on 9-track magnetic tape (800 BPI). The following instructions are for loading and using the paper tape.

1. Load the DEC absolute binary loader tape into the paper tape reader, and boot the paper tape reader.

2. When paper tape stops, remove the absolute binary loader tape, and load the 94EXOR tape.

3. Press CONTINUE on the CPU, to load the 94EXOR tape.

4. Set the 9400 Controller front panel switches as follows:

FORMAT to ON
MODE to EXT
ON LINE to ON

5. When the tape has finished loading, console device will print out:

9400 EXORCISOR V2.2
FILL COUNT

Type <0> for DECwriter Terminal
or <2> for ASR-33 Teletype
or <10> for CRT
followed by a carriage return <CR>.

6. Console device will print out:

STATUS?

Type <CR> for RP04 systems (776700)
or other beginning address of status registers for custom systems.

7. Console device will print out:

VECTOR?

Type <150> <CR> for RM03 systems
or <CR> for RP04 systems (254) or other interrupt vector address for custom systems.

8. Console device will print out:

ENTER TESTS TO BE RUN

Type in an octal number to select tests to be run. To select a test, its bit must be a one (1). Tests are as follows:

Bit 0 = Format
Bit 1 = Read Entire Disk Test
Bit 2 = Read/Write Test
Bit 3 = Random Read/Write Test
Bit 4 = Seek Test
Bit 5 = Interrupt Test
Bit 6 = ECC Test

examples:

Type <CR> to select all tests and format disk (177_8)
or <176> <CR> to select all tests without formatting disk
or <001> <CR> to format disk only

9. Console device will print out: (Only when Read/Write test is selected.)

ENTER PATTERN NUMBER

Type <CR> for pattern = address of buffer location (0)
or <1> <CR> for pattern = 133333
or <2> <CR> for pattern = 125252
or <3> <CR> for pattern = 177777
or <4> <CR> for pattern = 000000

10. Console device will print out:

ENTER RUN PARAMETERS

Type in an octal number to select appropriate run parameters. To select a parameter, its bit must be a one (1). Parameters are as follows:

Bit 0 = Short Pass
Bit 1 = Do Not Type Errors
Bit 2 = Format Every Pass
Bit 3 = Halt On Error
Bit 4 = Loop On Error
Bit 5 = Do Not Type Test Names or Pass Numbers

examples:

Type <CR> to format first pass and test all cylinders (0)

or <04> <CR> to format every pass and test all cylinders
or <20> <CR> to format first pass and loop on errors
or <11> <CR> to run short pass and halt on error.

11. If short pass has been selected, console device will print out: (If short pass is not selected, proceed to Step 13.)

ENTER NUMBER OF CYLINDERS

Type in a number representing total number of cylinders to be tested. Highest number of cylinders for both 9762 and 9766 drives is 823 (Octal 1467, direct systems only) . A number must be typed in, no default value has been preset.

examples:

Type <100> <CR>
or <1467> <CR>
or <50> <CR>

12. If short pass has been selected, console device will print out:

ENTER STARTING CYLINDER

Type in a number representing the cylinder the test is to start on. Note that the starting cylinder number plus the number of cylinders to test in Step 11, must not exceed 823. (i.e.; if Step 11 was 823, Step 12 must be 0.)

examples:

Type <CR> to set starting cylinder to 0.
or <10> <CR> to start at ten (Step 11 must be 813 or less)
or <100> <CR> to start at 100 (Step 11 must be 723 or less).

13. Console device will print out:

DISK TO TEST

Type in an octal number to select drives to be tested. To select a drive, its bit must be a one (1). Any combination of 1 to 8 drives may be tested as follows:

Bit 0 = Unit 0
Bit 1 = Unit 1
Bit 2 = Unit 2
Bit 3 = Unit 3
Bit 4 = Unit 4
Bit 5 = Unit 5
Bit 6 = Unit 6
Bit 7 = Unit 7

examples:

Type <1> <CR> to test unit 0
or <2> <CR> to test unit 1
or <3> <CR> to test units 0 and 1
or <377> <CR> to test units 0 through 7
A number must be typed in, no default value has been preset.

14. Console device will print out selected parameters as follows:

PASS # 000001
UNIT # 00000X (X = selected unit)
RP04 (or RM03) 9762 (or 9766) MAPPED (or DIRECT)

Console device will then print out tests as they begin to run.

FORMATTING
FORMAT CHECK TEST
READ DISK TEST
READ WRITE TEST
RANDOM R/W TEST
SEEK TEST
INTERRUPT TEST
ECC TEST

b. Restarting and Changing 94EXOR Parameters. The operator always has control of the CPU and the 94EXOR program from the console device. The following commands are available:

1. Control C (↑C) = Restart, program begins as in 4-2a., Step 5.
2. Control E (↑E) = Restart, program begins as in 4-2a, Step 8.
3. Control F (↑F) = Print cylinder, head, and sector.
4. Control H (↑H) = Enable halt on error.
5. Control L (↑L) = Enable loop on error.
6. Control O (↑O) = Enable print error messages.
7. Control Q (↑Q) = Proceed.
8. Control R (↑R) = Restart with same arguments.
9. Control S (↑S) = Halt.
10. Control U (↑U) = Enable print pass number.

The 94EXOR program is resident in memory beginning at address 1600. Control IC returns to address 1600, while Control R returns to address 1604, and Control E returns to address 1610.

c. Interpreting 9400EXOR Error Messages. A typical 94EXOR error message is shown below.

FORMAT CHECK TEST
DRIVE STATUS ERROR 000002

PC	*RPCS1*	*RPCS2*	*RPDS*	*RPER1*
006446	*144252*	*041100*	*150700*	*100100*

RPER2	*RPER3*	*RPDA*	*RPDC*
000000	*000000*	*005402*	*000054*

Each register has its contents listed in octal. By referring to Figure 5-3, RP04 CPA Register Summary on Page 5-11, and Figure 5-3a, RM02/03 CPA Register Summary on Page 5-24a, the register bits can be deciphered as follows:

PC
006446

Refers to the program counter at the time of the error. Indicates program step in 94EXOR program.

RPCS1
144252

- 52 — Function Code = Write Check Header and Data
- 4 — Bit 14 (TRE) set = Transfer Error (set by MXF, WCE)
- 1 — Bit 15 (SC) set = Special Condition (set by TRE)

RPCS2
041100

- 40 — Bit 9 (MXF) set = Missed Transfer
- 100 — Bit 14 (WCE) set = Write Check Error

RPDS
150700

- 700 — Bit 14 (ERR) set = Error (set by RPER1, 2, or 3)
- 100000 — Bit 15 (ATA) set = Attention Active

RPER1
100100

- 100 — Bit 6 (ECH) set = ECC Hard Error
- 100000 — Bit 15 (DCK) set = Data Check Error (set by ECH)

RPDA
005402

- 02 — Sector Address = 2
- 5 — Track Address = 11

RPDC
000054

- 54 — Desired Cylinder = 44

Result: Controller detected a noncorrectible ECC error during a Write Check Header and Data operation at sector 2, track 11, cylinder 44.

4-3. 9400 DIAGNOSTIC—USER INSTRUCTIONS.

Overview—The program comprises of several modules. These are as follows:

	LISTING		*TEXT FILE*	
94DIAG			V1.2	9-JAN-80
CARD			V1.2	19-DEC-79
DBOOT	V7.1	9-JAN-80	V7.0	26-DEC-79
MONITR	V1.2	3-JAN-80	V1.1	7-DEC-79
CPA	V1.2	2-JAN-80	V1.1	7-DEC-79
DRIVE	V1.2	2-JAN-80	V1.1	7-DEC-79
SYSTEM	V1.2	2-JAN-80	V1.1	7-DEC-79

It is to be noted that the listing and documentation version numbers and dates are not the same. This is because any changes made to the program since the documentation was prepared had no effect on the programs operation.

The module '94DIAG' is this text file.

The module 'CARD' is purely a document to act as a pocket guide to the user.

The overall name to which the released versions will be referred is 94DIAG.

Operation—When the routine is called, the following message will appear on the consol terminal:

Boot V7.0 26-DEC-79

BOOT UNIT:-

If help is required then enter a '?' and the following help message will appear:

Format is XX (N:SSSSSS (,VVV)) <CR>
Where XX is the only item required as the boot will default to unit 0 and the standard address's.
XX is as follows:

KA	9500 (174700)
AR	RK05 RT11
RR/DR	RM03 (176300)
MT	TU10 (172522)
WT	TU10 WRITE BOOT
RT	9500 RT11

RP/DP RP03 (176710)
ST 3500 (166100)
MM TU16 (172440)
WM TU16 WRITE BOOT
RK/DK RK05 (177400)
RB/DB RP04 (176700)
SF 4500 (166100)

N is unit # (optional)
SSSSSS is status register (optional)
Preselected status is in brackets
(,VVV) is vector for RT logical only (optional)
For RT11 the status and vector will be loaded to block 0 words 474 and 476 after reading it in.

BOOT V7.0 26-DEC-79

BOOT UNIT:-

The program has only the one entry point at which the user may request to boot a device or write the program (either boot or the user program plus boot) to a MagTape.

The instructions are broken down as follows:

The first two characters must be a valid device mnemonic for one of the devices currently included in this version of boot. All other items are optional; i.e., all devices will default to unit 0 with its standard status, and where applicable vector address's. The device mnemonic is followed by the unit # then a ':' if a status and or vector is to follow.

Below is a list of the current devices with their applicable mnemonics and their special peculiarities.

KA Boot 9500 disks by port # (physical units).

RT Boot 9500 RT11 logical units changing words 474 and 476 in memory on completion to the specified status and vector address's before executing from address 0.

RK/DK Either mnemonic is acceptable to boot an RK05 or an Aries unit.

AR As RK/DK but is for System Industries modified RT11 systems to change words 474 and 476 in memory to different status and vector address's.

RP/DP Either mnemonic is acceptable to boot RP02 or RP03.

RB/DB Either mnemonic is acceptable to boot RP04, RP05, RP06, RM03 or any 9400 disk unit.

RR/DR Either mnemonic is acceptable to boot RP04, RP05, RP06, RM03 or any 9400 disk unit with System Industries modified RT11 system to enable the change of words 474 and 476 in memory for a new status and vector address.

ST Boot System Industries 3500 disk units.

SF Boot System Industries 4500 disk units.

MT Boot TU10.

MM Boot TU16 or System Industries 9700 Series.

WT Write bootable program to TU10.

WM Write bootable program to TU16 or System Industries 9700 Series.

For the disk bootstraps (KA, RT, RK, DK, AR, RP, DP, RB, DB, RR, DR, ST and SF) block 0 of the requested unit is read into memory location 0 and then executed from that location.

For the MagTape bootstraps (MT and MM) the first record of the tape (identity record) is skipped and the second record (256 words) is read into memory address 0 and then executed from that location.

For writing bootable MagTapes (WT and WM) place a blank MagTape in the drive then enter the command. The tape will rewind if required then a filename will be written out followed by the boot block, both the filename and the boot block are 256 words long, then the program will be written, upon completion of the write the following message will appear:

****WRITTEN****

The program will then return to the entry point. The program written on the tape will be bootable from either TU10 or TU16 type systems.

The diagnostic's basic task is to let the user build up a string of commands or tests to be run, to run the tests, and to report the results of these tests. The diagnostic is designed to give the user a great deal of flexibility in doing this. With a single command, he can run an entire diagnostic, a related group of tests, or he can string together tests in any order he choses. He can specify how many times each test is to be run before going on to the next test, or how many times any combination of tests is to be run before going on. He can specify what each test is to do in case of error (e.g.; pause, loop, or ignore it). He can also specify what information will be reported in case of error.

a. Basic Conventions.

(1). Command Levels. The diagnostic has two command levels. The normal command level is the one in which the user enters commands into the command string, responds to initialization queries and requests from various tests. The normal command level is indicated by >> before each line of output or input. For example:

```
>> ENTER NEW CMDS
>>
```

The second command level is the dynamic command level. This takes priority over the normal command. The system stops what it is doing on the normal command level and begins executing the dynamic command. Dynamic command level is indicated by ** before each line of output. For example:

```
** (^E) ERR SPEC (C)=?
```

(2). Keyboard Inputs. All inputs that the operator makes to the keyboard (except dynamic commands) must be followed by <RETURN> for them to be entered. Before <RETURN> is pressed, the operator may delete characters one at a time with the <RUBOUT> key. Each time he rubs out a character, the terminal prints < until there are no more characters to rub out. After several rubouts, the user may be confused as to the actual contents of the line. He can review the line as it actually exists after the rubouts by pressing <LINE FEED>.

When the system prints a question ending with something inside a parenthesis, this is either a default value or an existing parameter which may be changed. If the operator presses <RETURN> without entering anything, the default will be chosen or the existing parameter will remain unchanged. In other words, by entering nothing, the operator has actually entered the value in parenthesis. Examples:

```
>> STD CPA LOC (Y)?
>> PR04 REGS BASE ADDR ('176700)? =
```

In the first example, the default answer is yes. The operator must enter N to indicate no. In the second example, the existing parameter is 176700 which will remain unchanged if the operator enters nothing else. If the operator enters something unexpected, such as a negative number in the second example above, the system will print ?? and repeat the question.

(3). Number Systems. All numbers printed at the console are normally in the decimal number system. An octal number will be preceded by an apostrophe ('), and a hexadecimal number will be preceded by the letter H-. Examples:

```
256 DECIMAL
'400 OCTAL
H-10 HEXADECIMAL
```

The number system shown in the default is the same as that assumed in the reply expected from the operator. Example:

```
** (^P) DATA PATTERNS
CUR ('125252)? =
```

The number entered by the operator is assumed to be octal.

b. Initialization. Before the diagnostic can begin testing, it must know what disc system is present as well as other details about the system. It determines this in a dialog with the operator as follows:

```
>> DATE (MM-DD-YY)
>> TIME (HH:MM:SS)
```

The user may enter date and time exactly as shown in parenthesis. The time is on the 24 hour system with the hours falling between 00 and 23. The user may not wish to enter date and time. In this case he simply presses <RETURN> to go on to the next question.

```
>> CRT OR TTY (C)? =
```

The system needs to know the terminal type in order to supply the correct number of fill characters. The default is CRT. If using a teletype, the operator should enter "T".

```
>> STD CPU LOC (Y)?
```

If the operator answers yes, the next two questions are skipped. The system will assume a 9400 interrupt vector address of 000254, and a 9400 registers base address of 176700.

```
>> 9400 INT VECT ADDR ('000254)? =
>> 9400 REGS BASE ADDR ('176700)? =
```

The operator may enter the nonstandard values in place of the standard ones shown in parenthesis. If the diagnostic has been loaded from a system disc, this is the time to replace the system disc with a scratch pack. Next, the system asks the operator to reset the controller:

```
>> RST CTLR, HIT <RET>
```

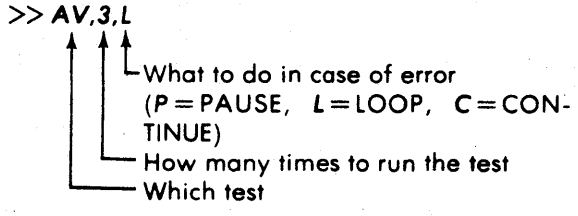
It then prints a summary of what drives and drive types are present and asks the operator if this is ok. If so, the initialization is complete and testing can begin. If the system cannot identify the drive type or if the summary is not satisfactory to the operator, a series of questions and answers will allow the operator to enter the drive

characteristics. However, it is strongly recommended that the operator determine why the system cannot identify the drive type before continuing. Check RPDT and RPSN registers (using CTL X Command). See Section 4-3, h, CPA Registers.

The system automatically defaults to the upper five cylinders of each unit. It tells the operator this in a message before inviting him to enter a command string.

c. Normal Commands. Once the initialization dialog is completed, the system is ready to begin testing. The operator may specify which tests are to be run, in which sequence and how many times. The operator may specify what action is to be taken when an error occurs, what information is to be reported in case of error, and when an error summary is to be given. The operator does this by means of the command language. This is made up of commands which tell the system what to do. Most of the commands tell the system which test or tests to run, some control the sequence of tests, and some control the execution of the tests and the error reporting.

A command consists of a mnemonic and two parameters. A carriage return terminates the command entry. For example:



This command means: run the address verify test three times. If there is an error, loop on the error until told to stop. Notice that commas are used to separate the mnemonic and the parameters. The operator does not need to enter the parameters if he wishes to use the default values. Thus:

```
>> AV
```

Means: run the address verify test once, continue on error. This is equivalent to entering:

```
>> AV,1,C
```

The operator may enter only one of the parameters and take the default value for the other. For example:

```
>> AV,P
```

is equivalent to:

```
>> AV,1,P
```

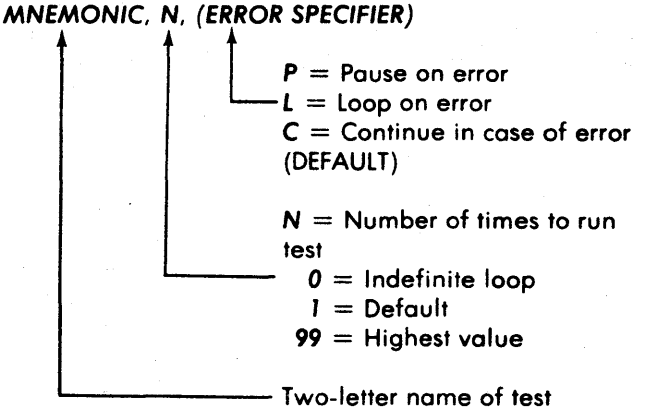
Another example:

```
>> AV,12
```

is equivalent to:

```
>> AV,12,C
```

(1). Primitive Commands. Many of the commands are primitive commands. That is, the command refers to a single test or operation. These commands take the following form:



Primitive commands may be strung together in any order as many as desired. For example:

```
>> AV,2,C
>> BB,3,P
>> CI,4
>> CR
>> CS
>> /
```

The slash (/) is the command to begin executing the command string. It also indicates the end of the command string. When the system has finished executing the command string, it is ready to accept a new string.

In the above examples, the commands execute from first to last and then the execution ends. It is also possible to loop back on the string a specified number of times. This is done with two additional commands:

```
LUP, N     LOOP TO LPT N TIMES
LPT        LOOP BACK TO HERE
```

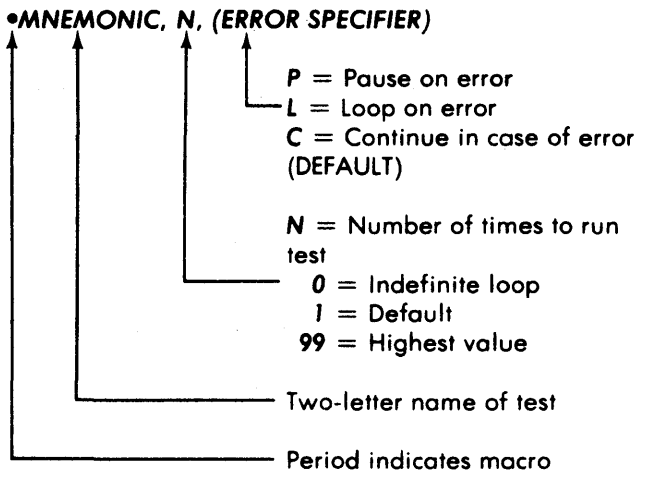
Example:

```
>> AV,2,C
>> LPT
>> BB,3
>> CI,4
>> LUP,6
>> CR
```

```
>> CS
>> /
```

After running *AV* twice, it will run *BB* three times, *CI* four times, then repeat this six times before running *CR* and *CS*.

(2). Macro Commands. The macro command is intended to test a group of similar hardware components. Each macro command in the command string automatically calls a sequence of primitive commands. Each primitive command is run once unless told to loop on error. The macro commands take the following form:



Example:

```
>> .RG,3,C
```

This means: run the set of register tests three times, continue on error. It is exactly equivalent to the following string of primitive commands:

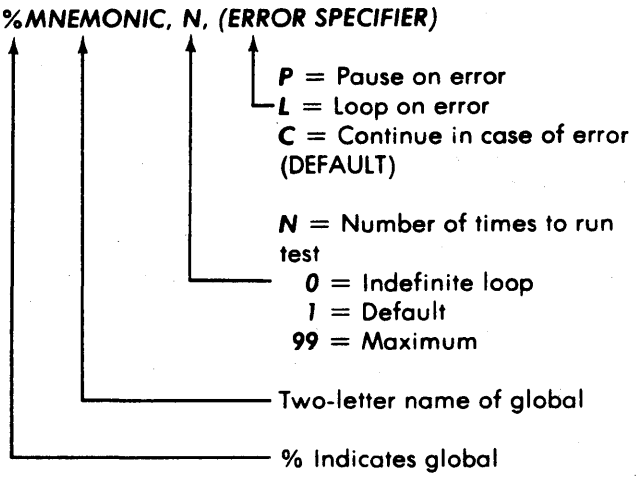
```
>> LPT
>> EK,1,C
>> EM,1,C
>> LUP,3
```

The operator may string together several macros, may use loop commands, may mix in primitive commands as he choses. Example:

```
>> .BC,3,C
>> LPT
>> .DR,2
>> .FI,P
>> LUP,4
>> MW
>> /
```

Macro commands are for convenience only. The same operation may be performed with the appropriate string of primitive commands.

(3). Global Commands. Global commands are intended to diagnose an entire hardware module. Each global command automatically calls a sequence of macro commands, each of which in turn calls a sequence of primitive commands. The global commands take the following form:



Example:

```
>> %DD,0,C
```

Means: run the drive diagnostic, repeating indefinitely. Continue in case of error. This is exactly equivalent to:

```
>> LPT
>> .IN,1,C
>> .PS,1,C
>> .DX,1,C
>> LUP,0
```

This in turn, is exactly equivalent to:

```
>> LPT
>> US,1,C
>> ST,1,C
>> MD,1,C
>> SC,1,C
>> SS,1,C
>> LS,1,C
>> OS,1,C
>> RS,1,C
>> WD,1,C
>> LUP,0
```

The operator may intermix global, macro and primitive commands, using the loop commands as desired. The global command is for convenience only. The same

result can be achieved by the equivalent string of macro commands or primitive commands.

(4). Utility commands.

ES Means print an error summary.

LPT Means loop back to this point in the command string.

LUP,N Means loop back to ***LPT N*** times, then go on.

/ Means end of command string. It is also the signal to begin executing the command string.

****** Means repeat the last command string. Eliminates the need to reenter it.

NP Means get the next data pattern from the table of eight patterns and use it as the current data pattern.

PN Prints the pass number. May be placed anywhere in the command string but is most logically placed at the end of a loop.

RE Means clear the error summary and the log of words written and read.

RL Means register load. It allows the user to load the front panel switches into any desired CPA register and displays the result. The error specifier means:

L = Go into a tight scope loop.
P = Keep asking for a new CPA address.
C = Load one register, then go to next test.

Example (where the data pattern is 125252):

```
>> ENTER COMMAND STRING
>> RL,P
>> /
    --RL (REGISTER LOAD)
>> ADDRESS ('176700)? = 176702
  = '125252
>> ADDRESS ('176702)? =
```

In this example, the switches (125252) were loaded into location 176702 and the contents were read as 125252. The system then asked for the next address. If the user enters an odd number for the address, the system will round it down to the next lower even number. If the user enters the address of a nonexistent memory location, the system will first trap, and then restart the diagnostic at the beginning of the initialization.

Another example:

```
>> ENTER NEW CMDS
>> RL,L
>> /
    --RL (REGISTER LOAD)
>> ADDRESS ('176700)? = 176702
>> LOOPING---
```

In this example, the system is in a tight scope loop, loading the address 176702 with the contents of the front panel switches over and over again. The operator may change the data pattern at any time by changing the switches. He may use the ^C command to stop the looping, or he may use the ^E command to change the error specifier.

RP Means get a random number and use it as the current data pattern.

TD Means print the date and time of day.

d. Dynamic Commands. Dynamic commands may be entered at any time. Any operation will be suspended until the dynamic command is completed. Another dynamic command may be given before the present one is completed. The present one will be aborted at that instant, and the new command will be executed. When the operation returns to the normal command level, the current line of input/output will be reviewed up to the point where the dynamic command interrupted. Lines of output at the dynamic command level are preceded by double asterisk (**). For example:

```
** (^P) DATA PATTERNS
CUR (^125252) =
```

CTL A (CURRENT ADDRESS): This command prints the current disc address in the format:

UNIT-CYLINDER-HEAD-SECTOR

CTL B (BOOTSTRAP): This command transfers control to the bootstrap program which allows the user to load software from the specified device. The system will print:

BOOT UNIT:-

The operator may then enter the unit from which he wishes to boot. This may be RP03, RP05 or paper tape. For paper tape, it is not necessary to use the absolute loader tape. If the user is in doubt as to what to enter, enter '?' and instructions will be given.

CTL C (CLEAR COMMAND STRING): This command immediately terminates the execution of the command string, and requests a new command string from the user. This command is essential for ending an infinite loop in the command string, or for terminating the unwanted remainder of a command string.

CTL E (ERROR SPECIFIER): This command allows the user to change the error specifier for the test currently being run. The command prints:

***** (^E) ERR SPEC (L)? =***

The letter in parenthesis indicates the current error specifier. If no letter is entered, the current specifier is retained. Also, the operator may enter one of the following letters:

L = LOOP ON ERROR
P = PAUSE ON ERROR
C = CONTINUE ON ERROR (IGNORE IT)

This will then become the current specifier until the next test or until the next loop of the same test.

CTL F (ERROR FORMAT): This command allows the user to specify what information he wants reported in case of error. Each piece of information is identified by a two-letter mnemonic:

BA, = RPBA
BE, = BELL
CC, = RPCC
DA, = RPDA
DC, = RPDC
DS, = RPDS
DT, = DATE
EA, = ADDRESS-#ERRORS
EM, = TEST'S ERROR MESSAGE
GB, = GOOD-BAD
LA, = LOGICAL ADDRESS
PA, = PHYSICAL ADDRESS
PC, = PROGRAM COUNTER
R1, = RPER1
R2, = RPER2
R3, = RPER3
S1, = RPCS1
S2, = RPCS2
WC, = RPWC

0 = NONE OF THE ABOVE
1 = ALL OF THE ABOVE

The command first reports the current format. For example:

***** (^F) FORMAT = BE,DT,PC,LA,PA,WC,DS,DA***

It then requests the new format:

***** NEW FORMAT =***

The user then enters the desired mnemonics all on a single line, each one separated from the next by a comma. See Section 4-3, f, for a full description of the Error Report.

CTL I (INITIALIZE): This command allows the user to reinitialize the system. He will go through the same initialization dialog as when he first started the diagnostic.

CTL K (ERROR LIMIT, RETRY LIMIT): This command allows the user to define how many errors a drive will be allowed to make before being dropped from testing. The default value of zero indicates infinite errors allowed. Once a drive is dropped, that fact will be indicated by a message to the console. Also, a notation will be made in the error summary. If all the drives are dropped, testing will be aborted. Clearing the error summary will allow drives to be picked up again. This command also allows the operator to set how many retries will be attempted before a hard error is logged.

CTL N (ERROR SUMMARY): The user is given the choice to clear the error summary after printing or allow it to accumulate. This will not clear this summary of words written and read. This command prints an error summary in five categories for each unit being tested. In each of the first four categories, the first number is hard errors, the second is soft errors. Following this is a summary of the number of words written and read by each unit being tested. Since this can be a very large number, it is given in scientific notation.

***** (^N) ERR SUM***
>> CLEAR AFTER PRINTING (N)?

-- ES (ERROR SUMMARY)

	ADDR VER	*DATA VER*	*ECC ERROR*
UNIT 0	3/5	120/200	0/0

CRC ERROR	*MISC ERROR*
0/0	5/0

UNIT 0 ***WDS WRITTEN = 2.56 E2. READ = 2.56 E2***

CTL 0 (ECIB TABLE): This command prints the latest version of the ECIB Table to be stored in the CPU memory. For description of ECIB Table, see Section 4-3, g, ECIB Table.

CTL P (DATA PATTERN): This command displays the current data pattern and allows the user to change it. For example:

***** (^P) DATA PATTERNS***
CUR ('125252)? =

The program expects an octal number. Following this the pattern table is displayed item by item, allowing the user to change it. If the user does not want to change the table, he can hit <ESC>.

CTL Q (TITLE SUPPRESS): This command allows the user to allow or suppress the printing of titles.

CTL R (RESUME): This command allows the user to resume operation under any of the following conditions:

1. When a test has paused on error.
2. When a test is suspended by the ***CTL S*** command.

CTL S (SUSPEND): This command suspends all testing until the ***CRL R*** command is given. Other dynamic commands may be executed during this suspension, but upon their completion, the testing will remain suspended. However, the ***CTL C*** command will cancel the suspension.

CTL U (DISC ADDRESS): This command allows the user to know the disc address upper and lower limits. The user may enter a new value or may retain the old one by pressing <RETURN> without entering a value. The program expects positive decimal integers whose value does not exceed the limits established at initialization. Example:

```
(^U)
  ** UPPER LIM (2-410-18-21)
  ** LOWER LIM (0-0-0-0)
```

The first number is unit number, the second is cylinder, the third is head and the fourth is sector. If a new address is to be entered, all four numbers must be given.

It is not advisable to change the limits while a test is running. Better to abort the test with ***CTL C***, change the address limits, then use \ to re-execute the command string.

CTL V (SET BAD BLOCK FLAG): Allows user to set the bad block flag in any sector. The user enters this in the format UN-CY-HO-SC. For example:

```
** (CTL: V) SET BB FLAG
** AT: 0-27-0-0     <CR>
** AT: 0-139-1-17   <CR>
** AT: <CR>
>>
```

A carriage return without entering anything will terminate the command.

CTL W (REVIEW COMMAND STRING): If this command is executed while the command string is still being built, it will list all commands entered before the last carriage return. If executed while a command is executing, it will list all the commands in the string. In addition, an arrow will point to the test currently running, and a number beside the arrow will indicate how many iterations are left. For example:

```
SS,1,C
LS,9,L <--5
OS,5,P
\
```

In addition, if a loop is being executed, an additional arrow at the LUP command will indicate how many iterations are left. Example:

```
LPT
SS,1,C
LS,9,L <--5
LUP,5 <--2
LPT
BB,1,C
CR,3,3
LUP,6
```

If the user has built the command string from macro (Group of Tests) or global (Complete Diagnostics), the command interpreter will expand these to the primitive commands (Tests). The review of the command string will show the primitive tests called by the macros or globals. For example:

```
>> ENTER NEW CMDS
>> .PS
>> SC,C
>>
     ** (^W) CMD SUMMARY
LPT
SS,1,L
LS,1,L
OS,1,L
RS,1,L
LUP,1
SC,1,C
/
>> >>
```

The macro command .PS has been expanded into its component tests.

CTL X (CPA REGISTERS): This command prints the contents of the CPA registers for each unit specified from the lower to the upper limit. See Section 4-3, h, for a full description of the CPA Registers.

e. Test Summaries.

(1). Summary of Primitive Tests.

		GLOBAL	MACRO
AV	= ADDRESS VERIFY	%SD	.FI
BB	= BAD BLOCK	%SD	.FI
CR	= CRC ERROR TEST	%SD	.FI
CS	= CYLINDER SWITCH TEST	%SD	.BC
DV	= DATA VERIFY TEST	%SD	.FI
EC	= ECC ERROR TEST	%SD	.FI
EK	= ECHO TEST	%CD	.RG
EM	= EMULATION TEST	%CD	.RS
ES	= PRINT ERROR SUMMARY	(UTILITY)	
FM	= FORMAT TEST	%SD	.DR
HD	= HEADER TEST	%SD	.BC
HS	= HEAD SWITCH TEST	%SD	.BC
IT	= CPU INTERRUPT TEST	%CD	.CF
LPT	= START OF LOOP	(UTILITY)	
LS	= LONG SEEK TEST	%DD	.PS
LUP	= LOOP COMMAND	(UTILITY)	
MI	= MPU INTERRUPT TEST	%CD	.CF
MW	= MAXIMUM WORD TRANSFER TEST	%SD	.BC
NP	= NEXT DATA PATTERN	(UTILITY)	
OS	= OSCILLATING SEEK TEST	%DD	.PS
OT	= OSCILLATING TRACK TEST	%SD	.DR
PN	= PRINT PASS NUMBER	(UTILITY)	
RC	= HALF READ CPU TEST	%CD	.DC
RE	= RESET ERROR SUMMARY	(UTILITY)	
RL	= REGISTER LOAD	(UTILITY)	
RP	= NEXT RANDOM DATA PATTERN	(UTILITY)	
RS	= RANDOM SEEK TEST	%DD	.PS
RT	= RANDOM TRACK WRITE/READ TEST	%SD	.DR
SC	= SECTOR COUNTER TEST	%DD	.IN
SS	= SEQUENTIAL SEEK TEST	%DD	.PS
ST	= UNIT STATUS TEST	%DD	.IN
SW	= SINGLE WORD TRANSFER TEST	%SD	.BC
TD	= PRINT THE DATE	(UTILITY)	
WC	= HALF WRITE CPU TEST	%CD	.DC
WD	= HALF WRITE/READ DRIVE TEST	%DD	.DX
WH	= WRITE HEADER	(UTILITY)	
WP	= WRITE PROTECT TEST	%SD	.FI
ZR	= ZIG-ZAG READ TEST	(UTILITY)	

(2). Macro and Global Definitions.

%CD = COMPUTER INTERFACE DIAGNOSTIC

.RG = REGISTER TESTS
EK = ECHO TEST
NP = NEXT DATA PATTERN
EK
NP
EK
NP
EK
NP
EM = EMULATION TEST

.CF = CPU/FORMATTER TESTS
IT = CPU INTERRUPT TEST
MI = MPU INTERRUPT TEST

.DC = CPU/DMA TESTS
WC = HALF WRITE CPU TEST
RC = HALF READ CPU TEST

%DD = DRIVE DIAGNOSTIC

.IN = INTERFACE TESTS
ST = UNIT STATUS TEST
SC = SECTOR COUNTER TEST

.PS = POSITIONER TESTS
SS = SEQUENTIAL SEEK TEST
LS = LONG SEEK TEST
OS = OSCILLATING SEEK TEST
RS = RANDOM SEEK TEST

.DX = DRIVE/DMA TESTS
WD = HALF WRITE/READ DRIVE TEST

%SD = SYSTEM DIAGNOSTIC
  .FI = FAULT INJECTION TESTS
    WP = WRITE PROTECT ERROR TEST
    BB = BAD BLOCK ERROR TEST
    CR = CRC ERROR TEST
    EC = ECC ERROR TEST
    AV = ADDRESS VERIFY TEST
    DV = DATA VERIFY TEST
  .BC = BOUNDARY CONDITION TESTS
    SW = SINGLE WORD TRANSFER TEST
    MW = MAXIMUM WORD TRANSFER TEST
    HS = HEAD SWITCH TEST
    HD = HEADER TEST
    CS = CYLINDER SWITCH TEST
  .DR = DATA RELIABILITY TESTS
    FM = FORMAT TEST
    OT = OSCILLATING TRACK TEST
    RT = RANDOM TRACK READ/WRITE TEST

f. Error Report: The error report consists of three parts:

1. The contents of various registers as requested by the user.

2. An analysis of the error bits contained in the error registers.

3. An error message from the test itself.

Since standard emulation tests use different registers than the extended emulation tests do, the error report will look different for these two types of tests. The full error report for a standard emulation test will appear as follows:

```
M/D/Y - H:M:S          PC = PGM CNTR          RPER1 = ERR REG #1
RPER2 = ERR REG #2     RPER3 = ERR REG #3     RPCS1 = CTL & STAT #1
RPCS2 = CTL & STAT #2  PRDS = DRIVE STAT      RPDA = HEAD/SECT ADDR
RPDC = DESIRED CYL     RPCC = CURRENT CYL     RPBA = BUS ADDRESS
RPWC = WORD COUNT      GD-BAD = EXP'D-REC'D   EA = ADDRESS-#ERRORS

   >> CPA REG STATUS:DISC ADDR = UN-CY-HD-SC
        (ANALYSIS OF ERROR BITS IN CPA REGISTERS)
   !! (MESSAGE FROM TEST)
```

For a full description of the contents of the CPA Registers, see Section 4-3, h.

The full error report for extended emulation tests will appear as follows:

```
M/D/Y - H:M:S          LOG ADR = UN-CY-HD-SC   PHYS ADDR = UN-CY-HD-SC
PC = PGM CNT           GD-BAD = EXP'D-REC'D    EA = ADDRESS-#ERRORS

   >> ECIB TABLE STATUS:
        (ANALYSIS OF ERROR BITS IN ECIB TABLE)
   !! (MESSAGE FROM TEST)
```

If the user wishes to examine the ECIB Table following an extended emulation test, he may use the ***CTL O*** dynamic command. For a full description of the contents of the ECIB Table, see Section 4-3, g.

g. ECIB Table.

ECOS1 (HEX) - OPERATION STATUS 1:

80 - ANY ERROR
40 - DEFERRED (NOT IMPLEMENTED)
20 - UNIT FAULT
10 - END OF HEADER TIMEOUT
 8 - END OF SECTOR TIMEOUT
 4 - DATA BUFFER TIMEOUT
 2 - PARITY ERROR HIGH
 1 - PARITY ERROR LOW

ECOS2 (HEX) - OPERATION STATUS 2:

80 - HARDWARE/FIRMWARE PROTECT
40 - SOFTWARE PROTECT
20 - ADDRESS VERIFY ERROR
10 - DATA VERIFY ERROR
 8 - CRC ERROR
 4 - ECC ERROR
 2 - ECC CORRECTION
 1 - RETRY CORRECTION (NOT IMPLEMENTED)

ECOS3 (HEX) - OPERATION STATUS 3:

80 - PACK OVERRUN
40 - BAD BLOCK
20 - LAST SECTOR ON PACK
10 - UNIT SELECT FAULT
 8 - SEEK COMPLETE TIMEOUT
 4 - UNIT ACCESS ERROR
 2 - ILLEGAL COMMAND IMPLEMENTATION
 1 - CPA ERROR

ECUS1 (HEX) - PRIMARY DRIVE STATUS:

80 - ATTENTION
40 - DUAL PORT BUSY
20 - SEEK ERROR
10 - UNIT SELECTED
8 - WRITE PROTECTED
4 - FAULT
2 - ON CYLINDER
1 - READY

ECUS2 (HEX): MODEL BYTE OR SECTOR COUNT

ECPORT: PORT NUMBER ON WHICH DRIVE WAS FOUND (0-3)

ECCPA: COMPUTER PORT ADAPTER (CPA) NUMBER (0-3)

ECFC (HEX) - FUNCTION CODE:

0 - CLEAR CONTROLLER
1 - SENSE MODEL STATUS, PUT IN ECUS2
2 - SENSE SECTOR COUNT, PUT IN ECUS2
3 - SENSE DIAGNOSTIC STATUS, PUT IN ECUS2
4 - SENSE FAULT STATUS, PUT IN ECOS1, ECOS2, ECOS3
5 - FIRMWARE RESERVE
6 - FIRMWARE RELEASE
7 - SET FIRMWARE WRITE PROTECT
8 - CLEAR FIRMWARE WRITE PROTECT
9 - CLEAR DRIVE ATTENTION
A - INITIATE RECALIBRATE
B - INITIATE SEEK
C - WRITE DATA
D - READ DATA
E - READ VERIFY DATA
F - WRITE HEADER
10 - READ HEADER
11 - READ VERIFY HEADER
12 - WRITE HEADER AND DATA
13 - READ HEADER AND DATA
14 - READ VERIFY HEADER AND DATA

ECLUC: PHYSICAL DRIVE NUMBER

ECLCYH: LOGICAL CYLINDER ADDRESS MSB

ECLCYL: LOGICAL CYLINDER ADDRESS LSB

EECLHED: LOGICAL HEAD ADDRESS

ECLSEC: LOGICAL SECTOR ADDRESS

ECPCYH: PHYSICAL CYLINDER ADDRESS MSB

ECPCYL: PHYSICAL CYLINDER ADDRESS LSB

ECPSEC: PHYSICAL SECTOR ADDRESS

ECFCM (HEX) - FUNCTION CODE MODIFIER:

80 - HALF OPERATION
40 - CPU SIDE (IF HALF OPERATION)
20 - INCLUDE ECC/CRC IN TRANSFER
10 - ECC CORRECTION INHIBIT
8 - ADDRESS COMPARE INHIBIT
4 - CRC ERROR INHIBIT

ECMSB (HEX) - MAP STATUS BYTE

80 - NEW HEAD
40 - NEW CYLINDER
20 - LAST SECTOR ON PACK

ECWCH: WORD COUNT MSB (2'S COMPLEMENT)

ECWCL: WORD COUNT LSB (2'S COMPLEMENT)

ECSSO: STARTING STROBE OFFSET (NOT IMPLEMENTED)

ECRPT: REPEAT COUNT FOR EACH STROBE/OFFSET (NOT IMPLEMENTED)

ECRTY: TOTAL RETRY COUNT (NOT IMPLEMENTED)

ECFLAG (HEX) - FLAG BYTE

80 - WRITE PROTECTED FLAG
40 - BAD SECTOR FLAG

ECUSER: USER BYTE

h. CPA Registers.

176700 - RPCS1 (CONTROL AND STATUS 1 REGISTER):

100000 - SPECIAL CONDITION: TRANSFER ERROR OR ATT'N I/O BUS PARITY ERROR
40000 - TRANSFER ERROR: DATA LATE, OR WRITE CHECK ERROR, OR PARITY ERROR, OR NON-EXISTENT DRIVE, OR NONEXISTENT MEMORY, OR PROGRAM ERROR, OR MISSED TRANSFER, OR MASS DATA BUSS OR DRIVE ERROR DURING TRANSFER
20000 - BUS PARITY ERROR (NOT USED, SET TO 0)
4000 - DRIVE AVAILABLE (NOT USED, SET TO 1)
2000 - PORT SELECT (NOT USED, SET TO 0)
1000 - UNIBUS ADDRESS EXTENSION BIT
400 - UNIBUS ADDRESS EXTENSION BIT
200 - READY
100 - INTERRUPT ENABLE
74 - READ MICRO-CONTROL (EXTENDED EMULATION)
72 - READ HEADER AND DATA
70 - READ DATA
64 - WRITE MICRO-CONTROL (EXTENDED EMULATION)

62 - WRITE HEADER AND DATA
60 - WRITE DATA
54 - JUMP MICRO-CONTROL (EXTENDED EMULATION)
52 - WRITE CHECK HEADER AND DATA
50 - WRITE CHECK DATA
30 - SEARCH COMMAND
22 - PACK ACKNOWLEDGE
16 - RETURN TO CENTERLINE
14 - OFFSET COMMAND
12 - RELEASE (DUAL PORT OPERATION)
10 - DRIVE CLEAR
6 - RECALIBRATE
4 - SEEK
2 - UNLOAD (STANDBY)
0 - NO OPERATION
1 - GO BIT

176702 - RPWC (WORD COUNT REGISTER):
WORD COUNT (2'S COMPLEMENT)

176704 - RPBA (UNIBUS ADDRESS REGISTER):
STARTING ADDRESS OF DMA TRANSFER.

176706 - RPDA (DESIRED SECTOR/TRACK ADDRESS REGISTER):

X174XX - DESIRED TRACK ADDRESS #37

X004XX - DESIRED SECTOR ADDRESS #1

XXXX27 - DESIRED SECTOR ADDRESS #27

XXXX00 - DESIRED SECTOR ADDRESS #0

176710 - RPCS2 (CONTROL AND STATUS 2 REGISTER):

100000 - DATA LATE (NOT USED, SET AT 0)
40000 - WRITE CHECK ERROR
20000 - PARITY ERROR (NOT USED, SET AT 0)
10000 - NONEXISTENT DRIVE
4000 - NONEXISTENT DRIVE
2000 - PROGRAM ERROR
1000 - MISSED TRANSFER
400 - MASS DATA BUSS PARITY ERROR (NOT USED, SET AT 0)
200 - OUTPUT READY
100 - INPUT READY (NOT USED, SET AT #1)
40 - CONTROLLER CLEAR
20 - PARITY TEST (NOT USED, SET AT 0)
10 - INHIBIT UNIBUS INCREMENT
7 - SELECT DRIVE #7
↓
0 - SELECT DRIVE #0

176712 - RPDS (DRIVE STATUS REGISTER):

100000 - ATTENTION ACTIVE
40000 - ERROR IN RPER1, RPER2, OR RPER3
20000 - POSITIONING IN PROGRESS (NOT USED, SET AT 0)
10000 - MEDIUM ON LINE
4000 - WRITE LOCK
2000 - LAST SECTOR TRANSFERRED
1000 - PROGRAMMABLE (NOT USED, SET AT 0)
400 - DRIVE PRESENT (NOT USED, SET AT 1)
200 - DRIVE READY
100 - VOLUME VALID
1 - RM03 = OFFSET MODE. RP04 = (NOT USED)

176714 - RPER1 (ERROR REGISTER 1):

100000 - DATA CHECK, ECC ERROR
40000 - UNSAFE
20000 - OPERATION INCOMPLETE (NOT USED, SET AT 0)
10000 - DRIVE TIMING ERROR (NOT USED, SET AT 0)
4000 - WRITE LOCK ERROR
2000 - INVALID ADDRESS ERROR
1000 - ADDRESS OVERFLOW ERROR
400 - HEADER CRC ERROR
200 - HEADER COMPARE ERROR
100 - ECC HARD ERROR
40 - WRITE CLOCK FAIL (NOT USED, SET AT 0)
20 - FORMAT ERROR
10 -PARITY ERROR
4 - REGISTER MODIFICATION REFUSED (NOT USED, SET AT 0)
2 - ILLEGAL REGISTER (NOT USED, SET AT 0)
1 - ILLEGAL FUNCTION

176716 - RPAS (ATTENTION SUMMARY REGISTER):

200 - DRIVE ATTENTION 7
100 - DRIVE ATTENTION 6
40 - DRIVE ATTENTION 5
20 - DRIVE ATTENTION 4
10 - DRIVE ATTENTION 3
4 - DRIVE ATTENTION 2
2 - DRIVE ATTENTION 1
1 - DRIVE ATTENTION 0

176720 - RPLA (LOOK AHEAD REGISTER):
NOT EMULATED

176722 - RPDB (DATA BUFFER REGISTER):
DATA BUFFER

176724 - RPMR (MAINTENANCE REGISTER):
MAINTENANCE REGISTER (NOT EMULATED)

176726 - RPDT (DRIVE TYPE REGISTER):

20000 - MOVING HEAD DISC TYPE
4000 - DUAL CONTROLLER OPTION AVAILABLE
24 - RM03
20 - RP04

176730 - RPSN (SERIAL NUMBER REGISTER):
USED TO INDICATE FURTHER DRIVE INFORMATION:

IF RP04

100400 = MAPPED 9762
140400 = DIRECT 9762
101400 = MAPPED 9766
141400 = DIRECT 9766

IF RM03

100400 = 9762
101400 = 9766
102200 = 9448-32 FIXED
102000 = 9448-32 REMOVABLE
102600 = 9448-64 FIXED
102400 = 9448-64 REMOVABLE
103200 = 9448-96 FIXED
103000 = 9448-96 REMOVABLE

176732 - RPOF (OFFSET REGISTER):

100000 - SIGN CHANGE (NOT USED, SET AT 0)
10000 - FORMAT BIT (NOT USED, SET AT 0)
4000 - ERROR CORRECTION CODE INHIBIT
2000 - HEADER COMPARE INHIBIT

RP04:

260 - OFFSET = −1200 MICRO-INCHES
240 - OFFSET = − 800 MICRO-INCHES
220 - OFFSET = − 400 MICRO-INCHES
060 - OFFSET = +1200 MICRO-INCHES
040 - OFFSET = +800 MICRO-INCHES
020 - OFFSET = +400 MICRO-INCHES
000 - RETURN TO TRACK CENTERLINE

RM03:

200 - OFFSET TOWARDS SPINDLE

176734 - RPDC (DESIRED CYLINDER REGISTER):

777 - DESIRED CYLINDER ADDRESS
↓
000 - DESIRED CYLINDER ADDRESS

176736 - RPCC (CURRENT CYLINDER REGISTER):

RP04:

777 - CURRENT CYLINDER ADDRESS
↓
000 - CURRENT CYLINDER ADDRESS

RM03:

176742 - RPER3 (ERROR REGISTER 3):

100000 - OFF CYLINDER (NOT USED, SET AT 0)
40000 - SEEK INCOMPLETE
100 - LOW 5 VOLT DC (RP04 ONLY)
40 - LOW AC (RP04 ONLY)
10 - HEAD RETRACT HAS OCCURRED (RP04 ONLY)
2 - VELOCITY UNSAFE (NOT USED, SET AT 0)
1 - PACK SPEED UNSAFE (NOT USED, SET AT 0)

176744 - RPEC1 (ECC POSITION REGISTER)
ECC POSITION REGISTER (NOT EMULATED)

176746 - RPEC2 (ECC PATTERN REGISTER):
ECC PATTERN REGISTER (NOT EMULATED)

176750 - RMBA (BUS ADDRESS EXTENSION REGISTER)
PDP-11/70 ONLY
77
↓ - EXTENDED HIGH ORDER BUS ADDRESS
00

176752 - RMSC3 (CONTROL & STATUS 3) PDP-11/70 ONLY

100000 - ADDRESS PARITY ERROR
40000 - DATA PARITY ERROR ODD WORD
20000 - DATA PARITY ERROR EVEN WORD
2000 - LAST MEMORY XFER WAS A DOUBLE WORD OPERATION
100 - INTERRUPT ENABLE

4-4. (%DD) DRIVE DIAGNOSTIC. The %DD diagnostic tests those portions of the controller which are most closely associated with the drive. The tests make minimal usage of the CPA registers and the emulation firmware. All instructions and status are handled via the extended emulation.

a. (ST) Status Test.

Execution Time: 4 Seconds
Prerequisites: None
Type of Emulation: Extended

Tests the status bits in ECUS1 as follows:

(1). Performs a recal and checks that the "ON CYLINDER" bit has set in a reasonable time. If not, it flags an error and returns to the monitor. If "ON CYLINDER" sets, it checks the status bits in ECUS1 which should be as shown:

ECUS1

Bit 7 = 0/1 Attention
Bit 6 = 0 Dual Port Busy
Bit 5 = 0 Seek Error
Bit 4 = 1 Unit Selected
Bit 3 = 0/1 Write Protected
Bit 2 = 0 Fault
Bit 1 = 1 On Cylinder
Bit 0 = 1 Ready

If not, the test flags an error and returns to the monitor.

(2). Seeks to cylinder #1 and checks that the "ON CYLINDER" bit has set in a reasonable time. If not, it flags an error and returns to the monitor.

(3). Seeks to an impossible cylinder (177777), and waits for either "SEEK ERROR" or "ON CYL" bit to set in a reasonable time. If not, it flags an error and returns to the monitor. If so, it checks the status bits in ECUS1 which should be as shown:

ECUS1

Bit 7 = 0/1 Attention
Bit 6 = 0 Dual Port Busy
Bit 5 = 1 Seek Error
Bit 4 = 1 Unit Selected
Bit 3 = 0/1 Write Protected
Bit 2 = 0 Fault
Bit 1 = 1 On Cylinder
Bit 0 = 1 Ready

(4). Does a long seek. Checks that the "ON CYL" bit is clear while the drive is seeking, and that it sets at the end of the seek.

Applicable error report options:

PA: Contains Drive Address
LA:

EM: Gives Error Message From Test

b. (SC) Sector Counter Test.

Execution Time: 10 Seconds
Prerequisites: None
Type of Emulation: Extended

The test requests the sector count and places it in a buffer. It continues to do this as fast as the firmware can supply the count until the buffer is full. It then analyzes the numbers in the buffer and determines that every integer between 0 and the maximum sector count given at initialization is present. If any integers are missing, the test flags an error and returns to the monitor.

Applicable error report options:

GB: The First Number Is the Expected Sector Count, the Second Number Is That Received (Octal)

LA: Address Shows Which Unit Is Failing
PA:

EM: Gives Error Message From the Test

c. (SS) Sequential Seek Test.

Execution Time: 2 Minutes (80 Mbyte)
Prerequisites: Upper Cylinder Limit Must Be Greater Than Lower Limit
Type of Emulation: Extended

Performs sequential seeks from the lower to upper cylinder address. One pass through the test will sequentially ascend and descend through all the cylinder addresses once. After each seek, the test checks status and reports any error.

Applicable error report options:

PA: Contains the Seek Address Which Caused the Error
LA:

EM: Gives Error Message From Test

d. (LS) Long Seek Test

Execution Time: 1 Second
Prerequisites: Upper Cylinder Limit Must Be Greater Than Lower Limit
Type of Emulation: Extended

This test seeks from the lower limit cylinder address to the upper limit cylinder address and back again. It checks status after each seek. If the status shows an error, it flags an error and returns to the monitor.

Applicable error report options:

PA: Contains the Seek Address Which Caused the Error
LA:

EM: Gives Error Message From Test

e. (OS) Oscillating Seek Test.

Execution Time: 5 Minutes 57 Seconds (80 Mbyte)
Prerequisites: Upper Cylinder Limit Must Be Greater Than Lower Limit
Type of Emulation: Extended

Seeks from the lowest cylinder to the lowest+1 and back again. Then it seeks from the lowest to lowest+2 and back again. It continues seeking from the lowest to successively higher addresses until the upper limit is reached. Then it successively reduces the upper address until it equals lowest+1 again.

Applicable error report options:

PA: Contains the Seek Address Which Caused the Error
LA:

EM: Gives Error Message From the Test

f. (RS) Random Seek Test.

Execution Time: 1 Minute 30 Seconds (80 Mbyte)
Prerequisites: Upper Cylinder Limit Must Be Greater Than Lower Limit
Type of Emulation: Extended

Seeks from one random cylinder address to another within the domain bounded by the upper and lower limits of the cylinder address as set by the dynamic command ^T. It continues until all the cylinders within that domain have been addressed. It checks status after each seek and reports the first error. It tallies successive errors in the error summary.

Applicable error report options:

PA: Contains the Seek Address Which Caused the Error
LA:

EM: Gives Error Message From the Test

g. (WD) Half R/W Drive Test.

Execution Time: 2 Seconds
Prerequisites: None
Type of Emulation: Extended

Fills the RAM buffer with an incrementing data pattern one word at a time using the WMC command in extended emulation. Does a half write header and data to the drive. Clears the RAM. Does a half read header and data from the drive. Checks data in the RAM one word at time.

The RAM data buffer is loaded as follows:

LOCATION (HEX)	*CONTENTS (HEX)*	
1000	00	{HEADER (FOR DISC ADDRESS 0-0-0-0)}
1001	10	
1002	00	
1003	00	
1004	00	
1005	00	
1006	00	
1007	00	
1008	00	}DATA{
1009	01	
100A	02	
↓	↓	
1107	FF	
1108	00	
1109	01	
↓	↓	
1206	FE	
1207	FF	

Applicable error report options:

GB: This Gives the Expected Data and the Actual Data. Since the Data is Stored In RAM In 8-Bit Bytes, the Right Hand Side of the Number Will Be the Data Byte, the Left Hand Side of the Number Will Always Be Zero.

EA: This Gives the Address In RAM (Octal) Where the First Error Occurred (the One Reported In GB). The Number to the Right of This Is the Total Number of Errors That Occurred During the Transfer.

EM: Gives Error Message From the test

4-5. (%CD) COMPUTER INTERFACE DIAGNOSTIC TEST PHILOSOPHY. The (%CD) diagnostic tests those portions of the computer interface which communicate the least with the disk. For example, this diagnostic deals only with computer interface-controller communications where possible.

These tests include:

(.RG) REGISTER TESTS

(EK) REGISTER ECHO TESTS
(EM) REGISTER EMULATION TESTS

(.CF) CPU/FORMATTER TESTS

(IT) CPU INTERRUPT TEST
(MI) MICROPROCESSOR INTERRUPT TEST

(.DC) CPU DMA TESTS

(RC) RAM BUFFER TEST
(WC) HALF WRITE CPU TEST

a. (EK) Register Echo Test.

Execution Time: 1 Second
Prerequisites: Must Have Version 1.3 (RM03) or 2.1 (RP04) of the Firmware, and CPA Board 9400-6031 Date Code A913 or A907
Type of Emulation: Standard

Tests the ability of each computer interface register to accept and hold data. This is accomplished by targeting each register for test. The target register is loaded with the user specified pattern (see ^P), except control and read only bits. All other computer interface registers are loaded with the complement of the user specified pattern. This allows detection of addressing or continuous loading errors. Then the contents of the target register is recalled and compared to the user specified pattern. If the comparison is not equal, an error report is displayed as follows:

The applicable error report options are: (^F)

BE, LA, GB, EA, EM ONLY

!!!!ERROR(S):

GB = EXP'D-RVC'D PATTERNS,
EA = ADDR-#ERRS
PC = PGM. CNTR
LA = UN-CY-HD-SC
GB = EXP'D-RCV'D
EA = ADDR-#ERRORS

EXP'D-RVC'D = Data pattern loaded into the target register and expected to be read back—data pattern read back (received) from target register

ADDR-#ERRS = Target register address—number errors (always 1)

See error report summary in Section 4-3, f, Error Report.

NOTE

To insure a complete test, (EK) should be run four times in sequence using the following four data patterns:

1. 177777
2. 000000
3. 125252
4. 052525

This is done automatically when running the %CD global command.

b. (EM) Register Emulation Tests.

Execution Time: 1 Second
Prerequisites: Must Have Version 1.3 (RM03) or 2.1 (RP04) of the Firmware
Type of Emulation: Standard

Test those bits of the computer interface registers which could not, for one reason or another, be tested by the (EK) test.

The bits are (in order tested):

1. MOL, DRY, or VV Stuck at Zero
2. ATA Stuck at One
3. SC, TRE For Stuck at One
4. RDY For Stuck at Zero
5. RDY For Stuck at Zero after Controller Function
6. ATA Stuck at Zero
7. ERR Stuck at One
8. RDY For Stuck at One During Write
9. GO For Stuck at Zero
10. GO For Stuck at One after Write
11. PGE For Stuck at One
12. PGE For Stuck at Zero
13. IR, CLR Stuck at Zero
14. SC, TRE Stuck at Zero
15. ERR Stuck at Zero

The error report is the same as the (EK) test.

See error report summary in Section 4-3, f.

c. (IT) CPU Interrupt Test.

Execution Time: 1 Second
Prerequisites: None
Type of Emulation: Standard

Requests a computer interface interrupt at a priority level of seven and tests that an interrupt does not occur level six and seven. Tests that an interrupt does occur at level five. And that it does not occur after it has been serviced.

The applicable error report options are: (^F)

BE, PC ONLY

See error report summary in Section 4-3, f.

d. (MI) Microprocessor Interrupt Test.

Execution Time: 1 Second
Prerequisites: None
Type of Emulation: Standard

Loads unit seven into RPCS2, loads 40 (CONTROLLER CLEAR) into RPCS2, and waits for the IR bit to be set by the microprocessor. If the IR bit is not set after a small wait, an error is reported.

The applicable error report options are: (^F)

BE,PC ONLY

See error report summary in Section 4-3, f.

e. (RC) RAM Data Buffer Test.

Execution Time: 4 Seconds
Prerequisites: None
Type of Emulation: Extended

Tests the two extended emulation functions; write microcode, read microcode, and consequently the 1024 words of microprocessor RAM. The test is implemented by writing and reading microcontrol one byte at a time of the user specified pattern (see ^P), over to and back from the RAM area. The data sent is compared to the data received and errors are reported.

The applicable error report options are: (^F)

BE, GB, LA, PA, EM

The report is the same as the (EK) test, except
EA = Lowest Erroneous RAM Addr—# of RAM Errors

See error report summary in Section 4-3, f.

f. (WC) Half Write CPU Test.

Execution Time: 2 Seconds
Prerequisites: None
Type of Emulation: Extended

Tests the ability of the CPU interface-controller to write DMA to the microprocessor RAM area. This is verified by reading the RAM back to the CPU by using read microcontrol commands. The data sent is compared to the data received and errors are reported.

The applicable error report options are: (^F)

GB = DMA Write Pattern—Read Microcontrol Pattern

EA = Lowest Erroneous RAM ADDR—# of RAM Errors

EM = Error Message From Test

See error report summary in Section 4-3, f.

4-6. 9400 (%SD) SYSTEM DIAGNOSTIC. The %SD diagnostic tests all the parts of the disc system which have previously been tested individually, or which have not yet been tested. In the data reliability tests, the standard emulation firmware is tested for the first time, and all elements of the system are brought into play.

NOTE

The test descriptions below, the execution time and number of bits transferred is given for an 80 megabyte mapped drive, and the diagnostic operating in 28K of memory. Larger capacity drives will require longer execution times and transfer more bits of data in many of the tests. Smaller memory size will increase the execution time in many of the tests.

a. (WP) Write Protect Error Test.

Execution Time: 2 Seconds (Approx)
Prerequisites: None
Type of Emulation: Extended
Data Pattern: 000000 and 177777

Tests the operation of the write protect bit in the header. Writes a sector of all zeros data with the write protect bit in the header set. Then it attempts to write all ones data in the same sector. Checks that the write protect error bit sets. It verifies that the all one data did not get written into the sector by reading the sector and seeing that the data is still all zeros.

Applicable error report options:

EM: Error Message Will Explain Contents

b. (BB) Bad Block Error Test.

Execution Time: 3 Seconds (Approx)
Prerequisites: None
Type of Emulation: Extended
Data Pattern: 000000 and 177777

Tests the operation of the bad block bit in the header. Writes a sector with all zero data and the bad block bit set in the header. Attempts to write all ones into that sector. Checks that the bad block error bit is set. Attempts to read data from that sector. Checks that the bad block error bit sets. Removes the bad block bit from the header, reads the header and verifies that the data is still all zeros. If it is all ones, then the system wrote in spite of the bad block bit in the header.

Applicable error report options:

EM: Error Message Will Explain Contents

c. (CR) CRC Error Test.

Execution Time: 3 Seconds (Approx)
Prerequisites: None
Type of Emulation: Extended
Data Pattern: 177777

Checks the validity of the CRC check word in the header. First, it writes a header, then reads the header and CRC word. It then compares this CRC word with a software generated CRC word and verifies that the two are the same. Finally, it writes a header with an erroneous CRC word and verifies that the CRC error bit is set when the header is read back.

Applicable error report options:

EM: Error Message Will Explain Contents

d. (EC) ECC Error Test.

Execution Time: 7 Seconds (Approx)
Prerequisites: None
Type of Emulation: Extended
Data Pattern: Set by ^P Command

Checks the validity of the ECC error detection and correction system. The test writes a sector of data and reads it back, checking status and data. Compares the ECC remainder with a software generated ECC remainder and verifies that they are the same. It then creates 11 consecutive errors in the data and writes it and the ECC remainder. Upon reading the data again, it verifies that the data error was corrected, and that a correctable ECC error bit was posted. This time it creates 12 consecutive errors in the data and writes it and the ECC remainder. Upon reading the data back again, it verifies that the hard ECC error bit was posted.

Applicable error report options:

EM: Error Message Will Explain Contents

e. (AV) Address Verify Test.

Execution Time: 14 Seconds (Approx)
Bits Transferred: 3.28×10^4 Bits
Prerequisites: None
Type of Emulation: Extended
Data pattern: 000000 and 177777

Checks the ability of the system to detect a discrepancy between the address written in the header, and the actual physical address of the sector being accessed. It does this by writing an incorrect address in a header and then attempting to read the sector, verifying that the address verify bit sets. It performs the test four times, setting errors in each of the four elements of the address in the header, namely: head, sector, cyclinder HI, and cylinder LO.

Applicable error report options:

EM: Error Message Will Explain Contents

f. (DV) Data Verify Test.

Execution Time: 1 Second (Approx)
Bits Transferred: 4096 Bits
Prerequisites: None
Type of Emulation: Standard
Data Pattern: Set by ^P Commands

Verifies the operation of the write check function. Writes data then performs a write check operation, checking status. It alters the data in CPU memory and performs a write check operation again, verifying that the write check error bit sets.

Applicable error report options:

EM: Error Message Will Explain

g. (SW) Single Word Transfer Test.

Execution Time: 1 Second (Approx)
Bits Transferred: 16 Bits
Prerequisites: None
Type of Emulation: Standard
Data Pattern: 125252

Tests the system's ability to transfer less than a full sector of data, in this case a single word. It fills the entire data buffer with 125252, but writes only a single word. It then clears the buffer, reads back a single word, and verifies that only that single word got read back into the buffer.

Applicable error report options:

EM: Error Message Will Explain

h. (MW) Maximum Word Transfer Test.

Execution Time: 1 Second (Approx)
Bits Transferred: 8.60×10^4 (Depending On Memory Size)
Prerequisites: None
Type of Emulation: Standard
Data pattern: Set by ^P Command

Tests the system's ability to handle large multi-sector data transfers. It sizes the available memory space in the CPU and makes the largest data transfer possible.

Since the memory space is variable depending on the size of the command string and the amount of memory available, the test prints out the size of the data transfer for the operator's information. The test formats and individually writes data in enough sectors to cover the transfer. It then reads all the data in a single multi-sector read.

Applicable error report options:

EM: Error Message Will Explain

i. (HS) Head Switch Test.

Execution Time: 4 Seconds (Approx)
Bits Transferred: 2.95×10^5 Bits
Prerequisites: None
Type of Emulation: Standard
Data Pattern: 125252, 000000, and 177777

Tests the system's ability to perform multi-sector transfers across head boundaries. First, it individually writes a sector on either side of the boundary, then does a 2-sector read of the two sectors. Then it does a 2-sector write across a head boundary and performs two single sector reads of the same sectors. It repeats this over all the head boundaries.

Applicable error report options:

EM: Error Message Will Explain

j. (HD) Header Test.

Execution Time: 14 Seconds (Approx)
Bits Transferred: 3.28×10^4 Bits
Prerequisites None
Type of Emulation: Extended
Data Pattern: 000000 and 177777

Checks the ability of the system to detect a discrepancy between the address written in the header, and the actual physical address of the sector being accessed. It does this by writing an incorrect address in a header and then attempting to read the sector, verifying that the address verify bit sets. It performs the test four times, setting errors in each of the four elements of the address in the header, namely: head, sector, cylinder HI, and cylinder LO.

Applicable error report options:

EM: Error Message Will Explain Contents

k. (CS) Cylinder Switch Test.

Execution Time: 1 Second (Approx)
Bits Transferred: 6.55×10^4 Bits
Prerequisites: None
Type of Emulation: Standard
Data Pattern: 125252, 000000, and 177777

Tests the system's ability to perform multi-sector transfers across cylinder boundaries. First, it individually writes a sector on either side of the boundary, then does a 2-sector read of the two sectors. Then it does a 2-sector write across a cylinder boundary and performs two single sector reads of the same sectors. It repeats this over four different cylinder boundaries.

Applicable error report options:

EM: Error Message Will Explain

l. (FM) Format Test.

Execution Time: 5 Minutes 15 Seconds (80 Mbyte)
Bits Transferred: 5.44×10^8 Bits Written
5.39×10^8 Bits Read
Prerequisites: None
Data Pattern: Current Pattern

Formats the disc between the limits set by the operator, using the largest multi-sector transfers that memory size will allow. Reads the headers in a mass transfer, checking status.

	RP04		***RM03***
	HEADER		HEADER
WD 1	100000+CYLINDER	WD 1	150000+CYLINDER
WD 2	HEAD-SECTOR	WD 2	HEAD-SECTOR
WD 3	000000		
WD 4	000000		
	DATA		DATA
WD 1	000001	WD 1	000001
WD 2	000000	WD 2	000000
WD 3	000000	WD 3	000000
WD 4	000000	WD 4	000000

RP04

WD 5 CURRENT PATTERN

WD 256 CURRENT PATTERN

RM03

WD 5 CURRENT

WD 256 CURRENT PATTERN

Applicable error report options:

EM: Error Message Will Explain

NOTE

When formatting a pack for system use, first set the current data pattern to 177777 using the ***CTL P*** command. This will allow for proper handling of bad blocks.

m. (OT) Oscillating Track Test.

Execution Time: 7 Minutes 5 Seconds (80 Mbyte)
Bits Transferred: 1.69×10^7
Prerequisites: Disc Must First Be Formatted (WH Command or FM Test)
Type of Emulation: Standard
Data Pattern: Set by ^P Command

This is a data reliability test wherein data is written on ascending cylinder addresses, and read from oscillating cylinder addresses. Data is read one sector at a time, always from sector 0 of any head or cylinder. First from the lowest cylinder, lowest head, then from the highest cylinder, highest head. After each read, the lower head address is incremented and the upper head address is decremented. The test reads back and forth between the upper and lower addresses until the two meet in the middle.

Applicable error report options:

EM: Error Message Will Explain

n. (RT) Random Track Test.

Execution Time: 10 Minutes (80 Mbyte)
Bits Transferred: 2.70×10^8 Bits
Prerequisites: Disc Must First Be Formatted (WH Command or FM Test)
Type of Emulation: Standard
Data Pattern: Set by ^P Command

Writes a track at a time on random cylinder addresses and reads a track at a time from random cylinder addresses.

Applicable error report options:

EM: Error Message Will Explain

o. (WH) Write Header Utility.

Execution Time: 3 Minutes 14 Seconds (80 Mbyte)
Bits Transferred: 5.44×10^8 Bits
Write 0 Bits Read
Prerequisites: None
Type of Emulation: Standard
Data Pattern: Current Pattern

This command allows the operator to write headers and data. He can write header for a single sector, or for any contiguous group of sectors, or for all the sectors on a disc. The command sizes the available memory space to perform the largest multi-sector write possible. It writes header and data in all sectors between the lower and upper address limits.

p. (ZR) Zig-Zag Read Utility.

This is identical to the read portion of the OT Test, Section 4-6, m.

CHAPTER 5
THEORY OF OPERATION

5-1. **INTRODUCTION.** This chapter contains block diagrams, flow diagrams, and functional theory of operation for the System Industries Series 9400 Controller with RP04 Emulator.

5-2. **9400 DISK CONTROLLER SYSTEM.** The System Industries Series 9400 Disk Controller System consists of one to four Computer Port Adapter (CPA) circuit card assemblies, one 9400 Controller Assembly, one to four Storage Module Drives (SMDs), and associated cables (Figure 5-1).

The Computer Port Adapter Circuit Card plugs into the PDP-11 mainframe (one card per PDP-11 system). The CPA circuit card is connected to the 9400 Controller Assembly by two flat ribbon cables, normally ten feet long. Refer to Figure 5-2 for the signal flow diagram, and Table 5-3 for the interconnect wire list.

The 9400 Controller Assembly connects to the Storage Module Drive(s) with one 60-pin flat twisted wire pair cable, and one flat shielded ribbon cable. Refer to Figure 5-2 for the signal flow diagram, and Tables 5-1 and 5-2 for the interconnect wire lists.

5-3. **RP04 COMPUTER PORT ADAPTER.** The PDP-11 RP04 Computer Port Adapter (CPA) provides the required interface between the PDP-11 Unibus and the 9400 Basic Controller. The CPA in combination with the RP04 Emulator firmware in the 9400 Basic Controller enables emulation of Digital Equipment Corporation's (DEC) RJP04 disk subsystem, using Control Data Corporation's (CDC) 9762 or 9766 Storage Module Drives (SMDs).

Operating Systems (OS) supported by the standard RP04 Emulator are DEC RSX11-D, RSX11-M, RSTS-E, DOS, and IAS; and Bell UNIX. Revisions to operating systems may require changes to firmware, and are field upgradable.

a. Computer Port Adapter Functions. The following functions are provided by the CPA.

1. Storage of command parameters, and drive status accessible to both the DEC CPU and the 9400 Microprocessor located in the Basic Controller. Drive status is stored for each attached SMD, and the Unit Select Register (USEL 0, 1, 2) steers the file access requests to the appropriate register. Parameters and drive status are stored in a RAM register file, or discrete registers. Simultaneous access requests to the file, from the CPU and the microprocessor are resolved by tie-breaker circuitry, with each request being serviced.

2. Control Status (RPCS1, RPCS2) is maintained in a combination of discrete and register file locations, which respond as the addressed register to CPU or microprocessor requests. Individual GO bits are maintained for each drive, to support overlapped seek operations.

3. The GO and READY bits in the control status registers are processed with automatic interaction and respond to resets, for orderly communication between the CPU and Basic Controller.

4. Detection of programmed resets, and processor initialize to generate Event Flags and Interrupt Requests to the microprocessor.

Automatic and transparent generation of interrupt requests to the DEC Computer System for two types of interrupt conditions.

a) Command completion.
b) Asynchronous event completion.

Command completion preempts event completion and sets the controller ready (RDY) bit, signaling the completion of the command processing. Event completion interrupt conditions are command set defined and firmware interpreted. A 5-bit field is associated with each event completion interrupt condition for identification of the asynchronous event or as a parameter associated with the event.

5. Detection of programming error; new parameter given by the CPU when the controller is still processing a command.

6. Unibus Programmed Input/Output (PIO) Controls.

7. Unibus Direct Memory Access (DMA) Controls and Memory Addressing.

8. Direct Memory Access transfer throttle control with selectable burst control, along with Non-Processor

Request (NPR) and Bus Request (BR) monitoring of other devices.

9. Interrupt logic and interrupt vector address generation.

10. Register file buffering and addressing for the microprocessor bus.

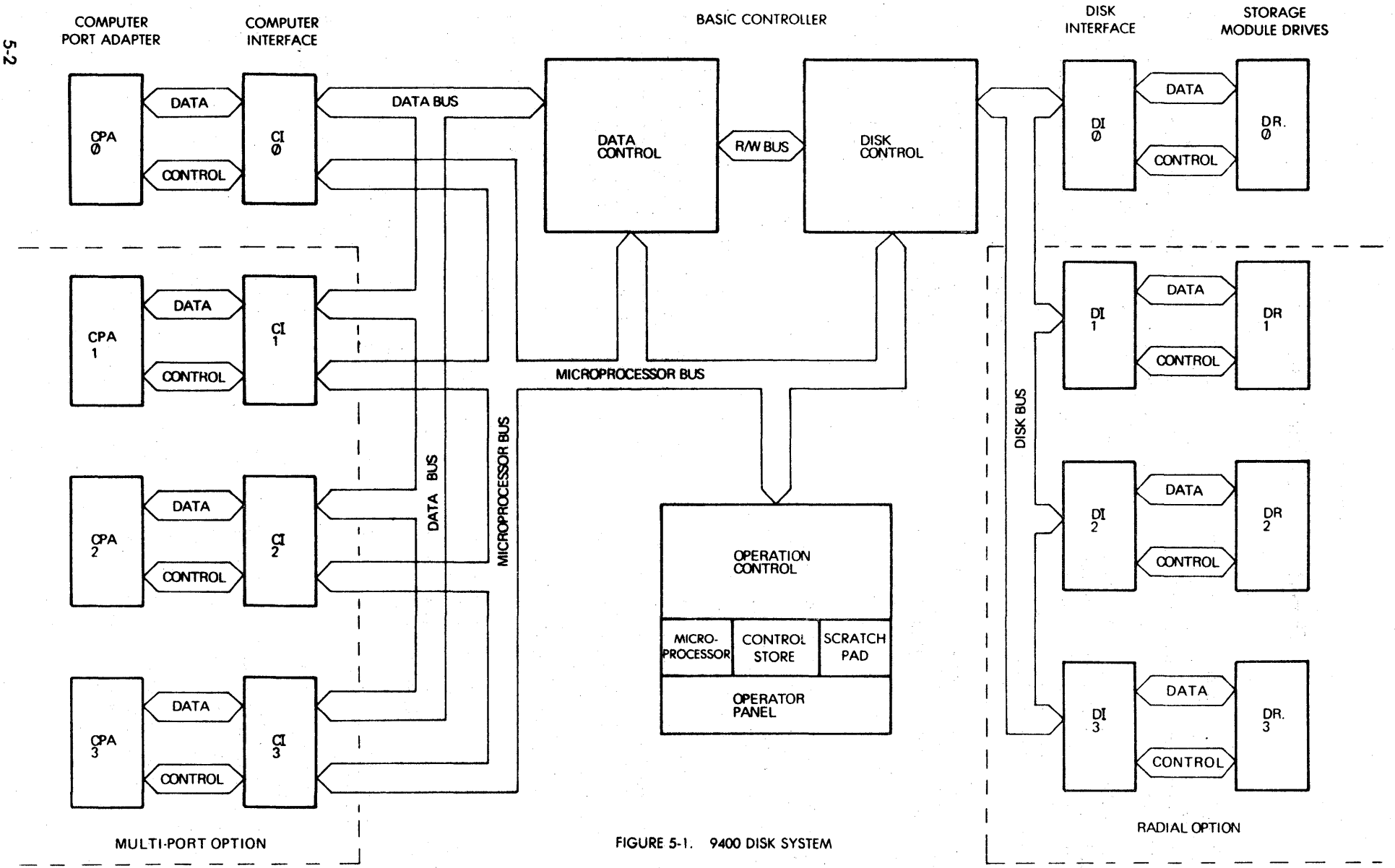


FIGURE 5-1. 9400 DISK SYSTEM

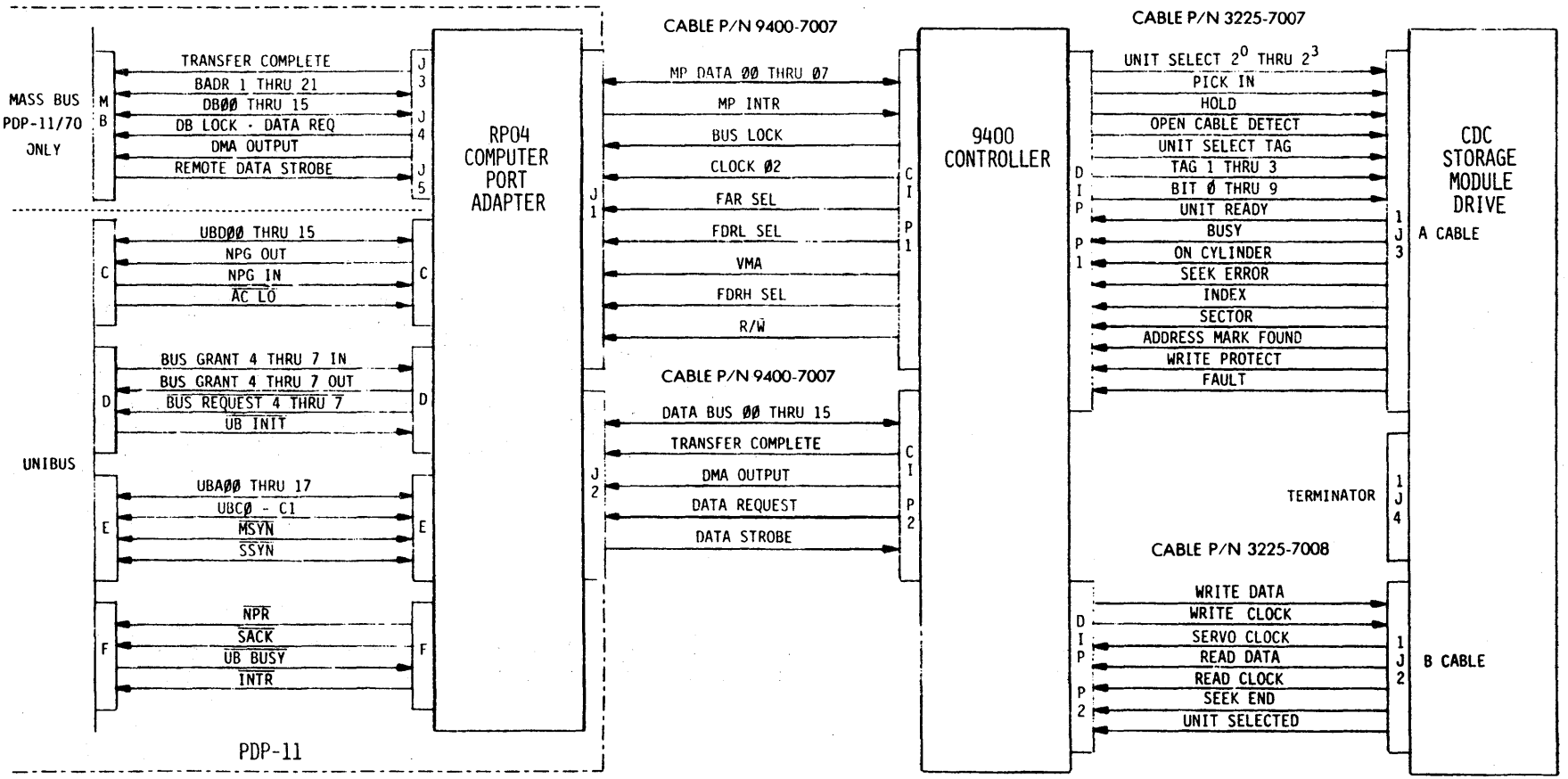


FIGURE 5-2. 9400 DISK SYSTEM SIGNAL INTERCONNECT FLOW DIAGRAM

Table 5-1. Controller to SMD (A Cable) Signal List

Controller Connection	Signal	SMD Connection
J1-1	TAG 1 (CYL) –	1J3-1
J1-2	TAG 2 (HEAD) –	1J3-2
J1-3	TAG 3 (CONTROL) –	1J3-3
J1-4	(BIT 0) WRT GATE –	1J3-4
J1-5	(BIT 1) RD GATE –	1J3-5
J1-6	(BIT 2) OFF + –	1J3-6
J1-7	(BIT 3) OFF – –	1J3-7
J1-8	(BIT 4) FAULT CLR –	1J3-8
J1-9	(BIT 5) ADDR MARK ENB –	1J3-9
J1-10	(BIT 6) RTZ –	1J3-10
J1-11	(BIT 7) STROBE EARLY –	1J3-11
J1-12	(BIT 8) STROBE LATE –	1J3-12
J1-13	(BIT 9) RELEASE –	1J3-13
J1-14	OPEN CABLE DETECT –	1J3-14
J1-15	FAULT –	1J3-15
J1-16	SEEK ER –	1J3-16
J1-17	ON CYL –	1J3-17
J1-18	INDEX –	1J3-18
J1-19	UNIT RDY –	1J3-19
J1-20	ADDR MARK FOUND –	1J3-20
J1-21	BUSY –	1J3-21
J1-22	UNIT SEL TAG –	1J3-22
J1-23	UNIT SEL 2^0 –	1J3-23
J1-24	UNIT SEL 2^1 –	1J3-24
J1-25	SECTOR –	1J3-25
J1-26	UNIT SEL 2^2	1J3-26
J1-27	UNIT SEL 3^3	1J3-27
J1-28	WR PROT –	1J3-28
J1-29	POWER PICK –	1J3-29
J1-30	SPARE	1J3-30
J1-31	TAG 1 (CYL) +	1J3-31
J1-32	TAG 2 (HEAD) +	1J3-32
J1-33	TAG 3 (CONTROL) +	1J3-33
J1-34	(BIT 0) WRT GATE + B0	1J3-34
J1-35	(BIT 1) RD GATE + B1	1J3-35
J1-36	(BIT 2) OFFSET + + B2	1J3-36
J1-37	(BIT 3) OFFSET – + B3	1J3-37
J1-38	(BIT 4) FAULT CLR + B4	1J3-38
J1-39	(BIT 5) ADDR MARK ENB + B5	1J3-39
J1-40	(BIT 6) RTZ + B6	1J3-40
J1-41	(BIT 7) STROBE EARLY + B7	1J3-41
J1-42	(BIT 8) STROBE LATE + B8	1J3-42
J1-43	(BIT 9) RELEASE + B9	1J3-43
J1-44	OPEN CABLE DETECT +	1J3-44

Table 5-1. Controller to SMD (A Cable Signal List (Continued)

Controller Connection	Signal	SMD Connection
J1-45	FAULT +	1J3-45
J1-46	SEEK ER +	1J3-46
J1-47	ON CYL +	1J3-47
J1-48	INDEX +	1J3-48
J1-49	UNIT RDY +	1J3-49
J1-50	ADDR MARK FOUND +	1J3-50
J1-51	BUSY +	1J3-51
J1-52	UNIT SEL TAG +	1J3-51
J1-53	UNIT SEL 2^0 +	1J3-53
J1-53	UNIT SEL 2^1 +	1J3-54
J1-55	SECTOR +	1J3-55
J1-56	UNIT SEL 2^2 +	1J3-56
J1-57	UNIT SEL 2^3 +	1J3-57
J1-58	WR PROT +	1J3-58
J1-59	POWER HOLD −	1J3-59
J1-60	SPARE	1J3-60

Table 5-2. Controller to SMD (B Cable) Signal List

Controller Connection	Signal	SMD Connection
J2-1	GND	1J2-1
J2-2	SERVO CLK –	1J2-2
J2-3	RD DATA –	1J2-3
J2-4	GND	1J2-4
J2-5	RD CLK –	1J2-5
J2-6	WR CLOCK –	1J2-6
J2-7	GND	1J2-7
J2-8	WR DATA – (NRZ)	1J2-8
J2-9	UNIT SEL +	1J2-9
J2-10	SEEK END –	1J2-10
J2-11		
J2-12		
J2-13		
J2-14	SERVO CLK +	1J2-14
J2-15	GND	1J2-15
J2-16	RD DATA +	1J2-16
J2-17	RD CLK +	1J2-17
J2-18	GND	1J2-18
J2-19	WR CLOCK +	1J2-19
J2-20	WR DATA + (NRZ)	1J2-20
J2-21		
J2-22	UNIT SEL –	1J2-22
J2-23	SEEK END +	1J2-23
J2-24		
J2-25		
J2-26		

Table 5-3. Controller to CPA Signal List

Computer Interface (Controller) Connection	Signal	Computer Port Adapter Connection
J1-1	GND	J1-1
J1-2	R/W	J1-2
J1-3	GND	J1-3
J1-4	FDRH SEL	J1-4
J1-5	GND	J1-5
J1-6	VMA	J1-6
J1-7	GND	J1-7
J1-8	FDRL SEL	J1-8
J1-9	GND	J1-9
J1-10	FAR SEL	J1-10
J1-11	GND	J1-11
J1-12	CLOCK 02	J1-12
J1-13	GND	J1-13
J1-14	BUS LOCK	J1-14
J1-15	GND	J1-15
J1-16	MP INTR	J1-16
J1-17	GND	J1-17
J1-18		J1-18
J1-19	GND	J1-19
J1-20		J1-20
J1-21	GND	J1-21
J1-22		J1-22
J1-23	GND	J1-23
J1-23		J1-24
J1-25	GND	J1-25
J1-26	MP DATA 03	J1-26
J1-27	GND	J1-27
J1-28	MP DATA 04	J1-28
J1-29	GND	J1-29
J1-30	MP DATA 05	J1-30
J1-31	GND	J1-31
J1-32	MP DATA 01	J1-32
J1-33	GND	J1-33
J1-34	MP DATA 07	J1-34
J1-35	GND	J1-35
J1-36	MP DATA 06	J1-36
J1-37	GND	J1-37
J1-38	MP DATA 02	J1-38
J1-39	GND	J1-39
J1-40	MP DATA 00	J1-40
J2-1	GND	J2-1
J2-2	DATA STROBE	J2-2
J2-3	GND	J2-3
J2-4	DATA BUS 13	J2-4

Table 5-3. Controller to CPA Signal List (Continued)

J2-5	GND	J2-5
J2-6	DATA BUS 12	J2-6
J2-7	GND	J2-7
J2-8	DATA BUS 14	J2-8
J2-9	GND	J2-9
J2-10	DATA BUS 15	J2-10
J2-11	GND	J2-11
J2-12	DATA BUS 09	J2-12
J2-13	GND	J2-13
J2-14	DATA BUS 08	J2-14
J2-15	GND	J2-15
J2-16	DATA BUS 10	J2-16
J2-17	GND	J2-17
J2-18	DATA BUS 11	J2-18
J2-19	GND	J2-19
J2-20	DATA REQUEST	J2-20
J2-21	GND	J2-21
J2-22	DMA OUTPUT	J2-22
J2-23	GND	J2-23
J2-24	TRANSFER COMPLETE	J2-24
J2-25	GND	J2-25
J2-26	DATA BUS 04	J2-26
J2-27	GND	J2-27
J2-28	DATA BUS 07	J2-28
J2-29	GND	J2-29
J2-30	DATA BUS 05	J2-30
J2-31	GND	J2-31
J2-32	DATA BUS 06	J2-32
J2-33	GND	J2-33
J2-34	DATA BUS 02	J2-34
J2-35	GND	J2-35
J2-36	DATA BUS 03	J2-36
J2-37	GND	J2-37
J2-38	DATA BUS 01	J2-38
J2-39	GND	J2-39
J2-40	DATA BUS 00	J2-40

11. Data transfer controls and interface to the Basic Controller's Data Bus.

12. Command queueing in a First In First Out (FIFO) register accessible to the microprocessor.

13. Attachment port for the DEC PDP-11/70 Cache Bus Interface.

b. CPA Communication Conventions. The PDP-11 program and the Basic Controller microprocessor control, synchronize communication through the GO and RDY bits in the CPA's RPCS1 register. The CPA automatically performs some processing of the GO and RDY bits to ensure orderly communication.

The RDY bit is reset by the CPA when the CPU initiates a data transfer. The GO bit sets an Event Flag to inform the microprocessor that a command is ready for processing.

The GO bit is reset by the CPA when the microprocessor posts drive status at the end of an operation.

The CPA sets the RDY bit when the microprocessor addresses and writes RPDS, to indicate command completion. An interrupt request to the CPU is generated if Interrupt Enable (IE) is set.

Resets to the Basic Controller are initiated by the PDP-11 by using the programmed reset command, or the Bus Initialize signal. When either signal is received by the CPA, it sets an Event Flag and generates an interrupt to the microprocessor. To protect against potential loop failures in the firmware, CPA polling by the microprocessor is not relied on to detect the reset. The reset is limited to the CPA issuing it (in multiple CPU systems). The microprocessor clears the register file and posts drive status upon receiving the reset interrupt request.

1. Processor initialize (BUS INIT) signal. Upon receipt of a BUS INIT signal the CPA performs the following functions.

a) Resets the interrupt control.
b) Sets the RDY bit and clears all GO bits.
c) Sends an interrupt to the microprocessor with the Set Ready (SR) event flag set. This event flag and interrupt request occur on the leading edge of the BUS INIT signal.

The microcontrol deallocates any drives and the data control allocated to the CPA, reinitializes the event queue and waits for a new command.

2. System resets. A variety of reset commands are available in the RP04 command set and each result in a combination of CPA hardware and Basic Controller firmware activity. The reset functions are listed in Table 5-4. Initialize (INIT), Controller Clear (CLR), and Error Clear (EC), generate interrupts to the controller, while Data Transfer (DT) and Drive Clear (CLR) set the Command Ready Flag indicating action is required by the microprocessor.

3. Programming error. Any attempt by the CPU to initialize a data transfer operation while RDY is cleared will cause the PER Error Flag to set, and will set PGE. Writing of the function code and setting of the GO bit to the selected drive is enabled.

4. Interrupt conditions. The CPA handles two types of interrupts; event completion and control ready. The CPA sets the RDY INT REQ flip-flop when the microcontrol signals the completion of the execution of a command by writing into RPCS1. An interrupt request to the PDP-11 Unibus is generated if IE is set.

The CPA sets the EV INT REQ when the microprocessor loads the Event Interrupt Address (EV INT ADR) with the identity of the asynchronous event that occurred. IE must be set to generate an interrupt request to the PDP-11 Unibus. The state of RPCS1 bits 12 through 15 enables the CPU interrupt routine to identify the different interrupt conditions.

Interrupt requests are presented to the Bus Control only when control is ready, and is inhibited when control is not ready. The CPA handles only one asynchronous event interrupt at a time. Any other events are queued in the microcontrol and synchronization is provided by the Poll Enable Event Flag.

c. CPA Register. The CPA contains registers sufficient for emulation of the RP04 command set, and will respond to all RP04 register addresses. Most of the required registers are located in a RAM register file, with the remainder implemented as discrete logic on the CPA. Eight register file locations are used to emulate registers normally located in each RP04 drive.

Both the CPU and the microprocessor have access to the register set, and simultaneous requests are resolved by a tie-breaker circuit which services each request sequentially. Drive status information is written into the file at the beginning and end of a data transfer operation, and periodically during controller idle periods.

Discrete registers include Bus Address (RPBA), Attention Summary (RPAS); and selected bits in RPCS1, RPCS2, and RPDS. Discrete GO bits are maintained for each of the 8 logical drives.

1. Microprocessor registers. The CPA contains a set of registers designed to speed microprocessor identification of a need for service, and to test error conditions following completion of an operation. The microprocessor also has access to all the registers available to the CPU.

Table 5-4. System Resets

SIGNAL	CPA ACTION	FIRMWARE ACTION
Unibus INIT or Controller Clear	Clear BA, Unit Select, IE, BAI, A16, A17, ATTN 0-7, GO 0-7, Set RDY	Terminate current operation, initialize register file
Data Transfer Command (GO=1)	Set GO, Clear RDY, ATTN	Clear TRE, RPCS2 bits 8-15
Error Clear	No Operation	Clear TRE, RPCS2 bits 8-15
Drive Clear	No Operation	Clear ERR, Drive Errors

Microprocessor register accesses are initiated by writing a command (read or write), and an address into the File Address Register. If the command is a write, the appropriate data must have been written into the File Data Registers (high and low bytes). If the command is a read, the CPA will load the addressed register into the File Data Register for access by the microprocessor.

CPA registers available only to the microprocessor are the File Address Register (FAR), the File Data Register HI (FDRH), the File Data Register LO (FDRL), the CPA Error and Control Flag Register (CPECF), and the CPA Event Flag Register (CPEVF).

2. Shared registers. CPA registers accessible to both the CPU and the microprocessor reside partly in discrete logic and partly in a RAM register file. Information to and from the registers takes place on an internal 3-state Main Data Bus (MDB), with arbitration logic to resolve simultaneous requests. Unibus register addresses are mapped through a PROM for conversion to CPA register addresses, while microprocessor accesses to the registers are direct.

d. CPA Register Organization. A summary of all the RP04 CPA registers is shown in Figure 5-3. The left hand columns give the register name and Unibus address. The right hand column gives the CPA address used by the microprocessor. (NE) indicates that the register is not emulated, although it physically exists on the CPA. The first eight registers in Figure 5-3 are replicated eight times, one for each physical RP04 drive emulated. Following Figure 5-3 is a complete breakdown of all the registers by bit and function.

Figure 5-3a provides a summary of all the RM02/03 Registers. Following Figure 5-3a, only the RM02/03 Registers and bits are described that differ functionally or in terminology from the RP04 Registers and bits listed in Figure 5-3 and the associated descriptive breakdown.

	UB ADDR (OCTAL)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	CPA ADDR (OCTAL)
RPCS1	(776700)	SC*	TRE*	0	0	1	0	A17*	A16*	RDY*	IE*	F4	F3	F2	F1	F0	GO	0 THRU 7
RPDS	(776712)	ATA	ERR	0	MOL	WRL	LST	0	1	DRY	VV	0	0	0	0	0	0	10 THRU 17
RPDA	(776706)	0	0	0	TA_{16}	TA_8	TA_4	TA_2	TA_1	0	0	0	SA_{16}	SA_8	SA_4	SA_2	SA_1	20 THRU 27
RPER1	(776714)	DCK	UNS	0	0	WLE	IAE	AOE	HCRC	HCE	ECH	0	FER	BPAR	0	0	ILF	30 THRU 37
RPSN	(776730)	SN_{38}	SN_{34}	SN_{32}	SN_{31}	SN_{28}	SN_{24}	SN_{22}	SN_{21}	SN_{18}	SN_{14}	SN_{12}	SN_{11}	SN_8	SN_4	SN_2	SN_1	40 THRU 47
RPDC	(776734)	0	0	0	0	0	0	0	DC_{256}	DC_{128}	DC_{64}	DC_{32}	DC_{16}	DC_8	DC_4	DC_2	DC_1	50 THRU 57
RPCC	(776736)	0	0	0	0	0	0	0	CC_{256}	CC_{128}	CC_{64}	CC_{32}	CC_{16}	CC_8	CC_4	CC_2	CC_1	60 THRU 67
RPOF	(776732)	0	0	0	1	ECCI	HCI	0	0	OFS_7	OFS_6	OFS_5	OFS_4	OFS_3	OFS_2	OFS_1	OFS_0	70 THRU 77
RPWC	(776702)	WC_{15}	WC_{14}	WC_{13}	WC_{12}	WC_{11}	WC_{10}	WC_9	WC_8	WC_7	WC_6	WC_5	WC_4	WC_3	WC_2	WC_1	WC_0	100
RPLA	(776720)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	101 (NE)
RPDB	(776722)	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	102
RPMR	(776724)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	103 (NE)
RPDT	(776726)	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	104
RPER2	(776740)	ACU	0	DF	30VU	0	0	0	0	0	0	0	0	0	0	0	0	105
RPER3	(776742)	0	SKI	0	0	0	0	0	0	0	DCL	ACL	0	UWR	0	0	0	106
RPEC1	(776744)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	107 (NE)
RPEC2	(776746)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	110 (NE)
RHCS3	(776752)	APE	DPEO	DPEE	0	0	DBL	0	0	0	IE	0	0	0	0	0	0	111 (PDP-11/70 Only)
RPBA	(776704)	BA_{15}	BA_{14}	BA_{13}	BA_{12}	BA_{11}	BA_{10}	BA_9	BA_8	BA_7	BS_6	BA_5	BA_4	BA_3	BA_2	BA_1	BA_0	120
RHBAE	(776750)	0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16	121 (PDP-11/70 Only)
RPCS2	(776710)	0	WCE	0	NED	NEM	PGE	MXF	0	OR	IR	CLR	0	BA1	U2	U1	U0	122
RPAS	(776716)									ATA_7	ATA_6	ATA_5	ATA_4	ATA_3	ATA_2	ATA_1	ATA_0	123
FIFO		F4	F3	F2	F1	F0	$USEL_2$	$USEL_1$	$USEL_0$									123
CPEVF										GC	EC	0	CPL	PE	PR	SR	ACE	124
CPECF		/APE	/PEO	/PEE	0	/DBL	/CPR	0	0									124
FDR		$FDRH_{15}$	$FDRH_{14}$	$FDRH_{13}$	$FDRH_{12}$	$FDRH_{11}$	$FDRH_{10}$	$FDRH_9$	$FDRH_8$	$FDRL_7$	$FDRL_6$	$FDRL_5$	$FDRL_4$	$FDRL_3$	$FDRL_2$	$FDRL_1$	$FDRL_0$	
FAR										R/W	FA_{64}	FA_{32}	FA_{16}	FA_8	FA_4	FA_2	FA_1	

8 LOGICA DRIVES

*These bits in RPCS1 are controller bits and are emulated only once, all other bits in RPCS1 are drive bits and are emulated eight times.

Figure 5-3. RP04 CPA Register Summary

1. Control and status 1 (RPCS1) register (776700).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	0	0	1	0	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO

BIT	NAME	FUNCTION
15	SC (Special Condition) Read Only	Set by TRE or ATTN. Cleared by Unibus INIT, Controller Clear, or by removing the ATTN condition.
14	TRE (Transfer Error) Read/Write	Set by WCE, NED, NEM, PGE, MXF, or a drive error during a data transfer. Cleared by Unibus INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set.
13	Not Used	Set to 0 by controller.
12	Not Used	Set to 0 by controller.
11	Not Used	Always read as a 1.
10	Not Used	Always read as a 0 with Cache option present. Without Cache, controller sets it to 0.
09-08	A17-A16 (Unibus Address Extension Bits) Read/Write	Upper extension bits of the BA register. Cleared by Unibus INIT, Controller Clear, or by writing 0's in these bit positions.
07	RDY (Ready) Read Only	RDY normally = 1. During data transfers, RDY = 0. When a data transfer command code (51_8-77_8) is written into RPCS1, RDY is reset. At the termination of the data transfer, RDY is set.
06	IE (Interrupt Enable) Read/Write	IE is a control bit which can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by Unibus INIT, Controller Clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.
05-01 00	F4-F0 and GO bit Read/Write	F4-F0 and the GO bit (00) are function (command) code control bits.

F4	F3	F2	F1	F0	
0	0	0	0	0	No Operation
0	0	0	0	1	Unload (Standby)
0	0	0	1	1	Recalibrate
0	0	1	0	0	Drive Clear
0	0	1	0	1	Release (Dual Port Operation)

1. Control and status 1 (RPCS1) register (776700). Continued

BIT	NAME	FUNCTION					
		0	1	1	0	0	Search Command
		1	0	1	0	0	Write Check Data
		1	0	1	0	1	Write Check Header and Data
		1	1	0	0	0	Write Data
		1	1	0	0	1	Write Header and Data
		1	1	1	0	0	Read Data
		1	1	1	0	1	Read Header and Data
		0	0	0	1	0	Seek Command
		0	0	1	1	0	Offset Command
		0	0	1	1	1	Return to Centerline
		0	1	0	0	1	Pack Acknowledge
		0	1	0	0	0	Read-In-Preset
		1	0	1	1	0	Call Microcontrol
		1	1	0	1	0	Write Microcontrol
		1	1	1	1	0	Read Microcontrol
		1	1	1	1	1	Illegal Function

The GO bit (RPCS1, bit 0) must be sent to cause the controller to respond to a command. The GO bit is reset by the controller after command execution. The function code bits are stored in the FIFO. Cleared by Unibus INIT or Controller Clear.

2. Drive status (RPDS) register (776712).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	0	MOL	WRL	LST	0	1	DRY	VV	0	0	0	0	0	0

BIT	NAME	FUNCTION
15	ATA (Attention Active) Read Only	An attention condition from a drive will set the ATA bit and the ATA summary line. It is cleared by Unibus INIT, Controller Clear, loading a command with the GO bit set, or loading a 1 in the RPAS register corresponding to the drive's unit number. An attention condition is caused by: any error in the error registers (except during the data transfers); the completion operation; the completion of a start-up cycle (with the MOL bit set); dual controller operation with drive presently available (drive was requested before but was not available).
14	ERR (Error) Read Only	Set when one or more of the errors in the error registers (RPER1, RPER2, or RPER3) for a selected drive is set. Cleared by Unibus INIT, Controller Clear, or Drive Clear.
13	Not Used	Always read as a 0.
12	MOL (Medium On-line) Read Only	Set for the drive upon the successful completion of the start up cycle. Cleared when the spindle is powered down or the device is switched off-line (with the spindle still up to speed) for diagnostic purposes.

2. Drive status (RPDS) register (776712). Continued

BIT	NAME	FUNCTION
11	WRL (Write Lock) Read Only	Set when the drive will not accept Write commands.
10	LST (Last Sector Transferred) Read Only	Set when last addressable sector on the disk pack has been read or written.
09	Not Used	Always read as a 0.
08	Not Used	Always read as a 1.
07	DRY (Drive Read) Read Only	Set at the completion of every command, data handling or mechanical motion. Cleared at the initiation of a command. If this bit is reset, the controller cannot issue another command. When set, this bit indicates the readiness of the drive to accept a new command.
06	VV (Volume Valid) Read Only	Set by the Pack Acknowledge or Read-In Preset Command. Cleared whenever drive cycles up from the off state. When reset, this bit indicates when the drive has been put off-line and on-line and a disk pack may have been changed.
05-00	Not Used	Always read as a 0.

3. Desired sector track address (RPDA) register (776706).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	TA16	TA8	TA4	TA2	TA1	0	0	0	SA16	SA8	SA4	SA2	SA1

BIT	NAME	FUNCTION
15-13	Not Used	Set to 0 by controller.
12-08	TA (Track Address) Read/Write	Set by the program to specify the track on which a transfer is to start. Cleared by Unibus INIT. Updated by the controller at the end of the operation to address the next logical track.
07-05	Not Used	Set to 0 by controller.
04-00	SA (Sector Address) Read/Write	Set by the program to specify the sector on which a transfer is to start. Cleared by Unibus INIT. Updated by the controller at the end of the operation to address the next logical sector.

4. Error (RPER1) register 01 (776714).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	0	0	WLE	IAE	AOE	HCRC	HCE	ECH	0	FER	BPAR	0	0	ILF

BIT	NAME	FUNCTION
15	DCK (Data Check) Read/Write	Set during a read operation when the ECC hardware has detected an ECC error after the ECC bytes have been looked at. Cleared by a Drive Clear command. Unibus INIT, Controller Clear, or by writing 0's into the register.
14	UNS (Unsafe) Read/Write	Drive Fault detected. Cleared by a Drive Clear, Unibus INIT, or Controller Clear.
13	Not Used OPI (Operation Incomplete)	Set to 0 by controller.
12	Not Used DTE (Drive Timing Error)	Set to 0 by controller.
11	WLE (Write Lock Error) Read/Write	Set when the operating system attempts to issue a write command on write-locked device (device in WRITE PROTECT mode). A manual (WRITE PROTECT) switch can place the device in WRITE PROTECT mode during normal operations. Cleared by Unibus INIT, Drive Clear, Controller Clear, or by writing 0's into the register.
10	IAE (Invalid Address Error) Read/Write	Set when the address in the Desired Cylinder register (RPDC) or the Desired Sector/Track Address register (RPDA) is invalid and a seek or search operation is initiated. Cleared by Unibus INIT, Drive Clear, Controller Clear, or by writing 0's into the register.
09	AOE (Address Overflow Error) Read/Write	Set when the Desired Cylinder register (RPDC) overflows during a read or write. Cleared by Unibus INIT, Drive Clear, Controller Clear, or by writing 0's into the register. Setting of this bit indicates that the Desired Cylinder Address register has exceeded the maximum cylinder address.
08	HCRC (Header CRC Error) Read/Write	Set by a CRC error in the header. Cleared by Unibus INIT, Drive Clear, Controller Clear, or by writing 0's into the register.
07	HCE (Header Compare Error) Read/Write	If the sector counter is equal to the desired sector field, the header associated with that sector is compared with the desired header words. If the header matches the desired cylinder and desired sector/track address, the header field is the required one. If the header does not match the desired cylinder and sector/track address, the HCE bit is set. If the sector address and sector count match but a CRC error is detected following the header compare, the HCE bit is reset and the HCRC bit is set. Cleared by Unibus INIT, Drive Clear, Controller Clear, or by writing 0's into the register.
06	ECH (ECC Hard Error) Read	Set when the conclusion of the error correction procedure indicates that the error was a noncorrectable ECC error. Cleared by Unibus INIT Drive Clear, Controller Clear, or by writing 0's into the register.

4. Error (RPER 1) register 01 (776714). Continued

BIT	NAME	FUNCTION
05	Not Used (WCF) Write Clock Fail	Set to 0 by controller.
04	FER (Format Error)	Format switch in wrong position while attempting a format operation.
03	BPAR (Buffer Parity Error) Read/Write	Set when a parity error is detected during data transmission over the data bus to the buffer. Cleared by a Drive Clear command, an Initialize pulse or by writing 0's into the register.
02	Not Used (RMR) Register Mod Refused	Set to 0 by controller.
01	Not Used (ICR) Illegal Register	Set to 0 by controller.
00	ILF (Illegal Function) Read	Set when the function code in the Control register does not correspond to an implemented command on this drive. Cleared by Unibus INIT, Drive Clear, Controller Clear, or by writing 0's into the register.

5. Serial number (RPSN) register(776730).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SN_{38}	SN_{34}	SN_{32}	SN_{31}	SN_{28}	SN_{24}	SN_{22}	SN_{21}	SN_{18}	SN_{14}	SN_{12}	SN_{11}	SN_{8}	SN_{4}	SN_{2}	SN_{1}

The purpose of this register is to distinguish a drive from similar drives attached to the same controller. The serial number provides a means of distinguishing between different drives with identical characteristics and which are connected to the same controller.

6. Desired cylinder (RPDC) register (776734).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	DC_{256}	DC_{128}	DC_{64}	DC_{32}	DC_{16}	DC_{8}	DC_{4}	DC_{2}	DC_{1}

BIT	NAME	FUNCTION
15-09	Not Used	Always read as a 0.
08-00	DC (Desired Cylinder)	Specifies the Requested Cylinder Address.

7. Current cylinder (RPCC) register (776736).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	CC_{256}	CC_{128}	CC_{64}	CC_{32}	CC_{16}	CC_{8}	CC_{4}	CC_{2}	CC_{1}

BIT	NAME	FUNCTION
15-09	Not Used	Always read as a 0.

7. Current cylinder (RPCC) register (776736). Continued

BIT	NAME	FUNCTION
08-00	CC (Current Cylinder)	This register is a read-only register and operates in conjuction with the Desired Cylinder Address register. It is updated at the end of each operation, and contains the positioner location. The Current Cylinder Address register will reset to zero under the following conditions: 1. Recalibrate instruction. 2. Completion of the cycle-up process (heads loaded). 3. Receipt of an INIT Pulse. The Current Cyclinder Address register will not reset to zero if: 1. A Drive Clear command is issued.

8. Offset (RPOF) register (776732).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	1	ECCI	HCI	0	0	OFS_7	OFS_6	OFS_5	OFS_4	OFS_3	OFS_2	OFS_1	OFS_0

BIT	NAME	FUNCTION
15-13	0	Set to 0 by controller.
11	ECCI (Error Correction Code Inhibit)	Set when the software desires to inhibit error correction. If ECI is set, error correction code is disallowed; if ECI is reset, the error correction process is allowed. Cleared by Read-In Preset command.
10	Not Used	Status of this bit is ignored by the controller.
09-08	Not Used	Set to 0 by controller.
07-00	OFS (Offset Information)	Set under software control. Cleared by Read-In Preset command or at the completion of the offset operation.

9. Word count (RPWC) register (776702).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC_{15}	WC_{14}	WC_{13}	WC_{12}	WC_{11}	WC_{10}	WC_9	WC_8	WC_7	WC_6	WC_5	WC_4	WC_3	WC_2	WC_1	WC_0

BIT	NAME	FUNCTION
15-00	WC (Word Count) Read/Write	Set by the program to specify the number of words to be transferred (2's complement form). This register is cleared only by writing zeros into it. This register is updated by the controller at the completion of the DMA transfer.

10. Look-ahead (RPLA) register (776720).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
15-00	None	This register is not emulated and is set to 0 by controller.

11. Data buffer (RPDB) register (776722).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

BIT	NAME	FUNCTION
15-00	DB (Data Buffer) Read/Write	Contains the bad data word on a Data Compare operation.

12. Maintenance (RPMR) register (776724).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
15-00	None	This register is not emulated and is set to 0 by controller.

13. Drive type (RPDT) register (776726).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

BIT	NAME	FUNCTION
15-00	None	This register is set to 020020_8 by controller.

14. Error (RPER2) register (776740).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ACU	0	DF	30VU	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
15	ACU (AC Unsafe)	Power low condition detected in the controller.
14	None	Set to 0 by controller.
13	DF (Drive Fault)	Set when a drive fault occurs.
12	30VU (30 Volts Unsafe)	Power low condition detected in the controller.
11-00	None	Set to 0 by controller.

15. Error (RPER3) register (776742).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	SKI	0	0	0	0	0	0	0	DCL	ACL	0	UWR	0	0	0

BIT	NAME	FUNCTION
15	None	Set to 0 by controller.
14	SKI (Seek Incomplete) Read/Write	Set when a seek operation fails to complete within 400 ms from a seek initiation.
13-07	None	Set to 0 by controller.
06	DCL (DC Low)	Power low condition detected in the controller.
05	ACL (AC Low)	Power low condition detected in the controller.
04	None	Set to 0 by controller.
03	UWR	Power low condition detected in the controller.
02-00	None	Set to 0 by controller.

16. ECC Position (RPEC1) register (776744).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
15-00	None	This register is not emulated and is set to 0 by controller.

17. ECC Pattern (RPEC2) register (776746).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
15-00	None	This register is not emulated and is set to 0 by controller.

18. Control and status 3 (RHCS3) register (776752)(PDP-11/70 only).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
APE	DPEO	DPEE	0	0	DBL	0	0	0	IE	0	0	0	0	0	0

BIT	NAME	FUNCTION
15	APE (Address Parity Error) Read Only	Set if the address parity error line indicates that the memory detected a parity error or address and control information during a memory transfer. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.
14-13	DPE,OW (Data Parity Error, Odd Word) (Data Parity Error, Even Word) Read Only	Set if a parity error is detected on data from memory when the control is performing a Write or Write Check command. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.
12-11	Not Used	Always read as zero.
10	DBL (Double Word) Read Only	Set if the last memory transfer was a double word operation. Cleared by Unibus INIT, Controller Clear, or loading a data transfer command with GO set.
09-07	Not Used	Set to 0 by controller.
06	IE (Interrupt Enable) Read/Write	A control bit under program control. When = 1, an interrupt may occur due to RDY or SC being asserted. Cleared by Unibus INIT, Controller Clear, or when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.
05-00	Not Used	Set to 0 by controller.

19. Unibus address (RPBA) register (776704).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA_{15}	BA_{14}	BA_{13}	BA_{12}	BA_{11}	BA_{10}	BA_9	BA_8	BA_7	BA_6	BA_5	BA_4	BA_3	BA_2	BA_1	BA_0

BIT	NAME	FUNCTION
15-00	BA_{15}-BA_0 (Unibus Address) Read/Write	Loaded by the program to specify the starting memory address of a transfer. Cleared by Unibus INIT, or by Controller Clear. The BA register is incremented by 2 after each transfer of a word to or from memory.

20. Bus address extension (RHBAE) register (776750)(PDP-11/70 only).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}

BIT	NAME	FUNCTION
15-06	None	Always read as 0.
05-00	A_{21}-A_{16} (Address)	Extended high order bus address bits. Used for PDP-11/70 only.

21. Control and status 2 (RPCS2) register (776710).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	WCE	0	NED	NEM	PGE	MXF	0	OR	IR	CLR	0	BAI	U2	U1	U0

BIT	NAME	FUNCTION
15	Not Used DLT (Data Late) Read Only	Always read as a 0.
14	WCE (Write Check Error) Read Only	Set when the controller is performing a Write-Check operation and a word on the disk does not match the corresponding word in memory. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. WCE causes TRE to set. If a mismatch is detected during a Write-Check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RPBA (and extension) is the address of word following the one which did not match (if BAI is nmot set). The mismatched data word from the disk is displayed in the data buffer (RPDB).
13	Not Used PE (Parity Error) Read/Write	Always read as 0.
12	NED (Nonexistant Drive) Read Only	Set when the program initiates a request for a drive which does not exist, or is powered down. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. NED sets TRE.

21. Control and status 2 (RPCS2) register (776710). Continued

BIT	NAME	FUNCTION
11	NEM (Nonexistant Memory) Read Only	Set when the controller is performing a DMA transfer and the memory address specified in RPBA is nonexistant (does not respond to MSYN within 10 μs. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. NEM sets TRE. The RPBA contains the address +2 of the memory location causing the error.
10	PGE (Program Error) Read Only	Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. PGE sets TRE. The data transfer command code is inhibited from being written.
09	MXF (Missed Transfer) Read/Write	Set if the controller fails to detect an End of Header or End of Sector, or the data buffer fails to empty during a data transfer. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. MXF sets TRE. This bit can be set or cleared by the program for diagnostic purposes.
08	Not Used MDPE (Mass Data Bus Parity Error)	Always read as a 0.
07	OR (Output Ready) Read Only	Set by the controller to indicate a word is in RPDB.
06	IR (Input Ready) Read Only	Always read as a 1.
05	CLR (Controller Clear) Write Only	When a 1 is written into this bit, the controller and all drives are initialized. Unibus INIT also causes Controller Clear to occur.
04	Not used	Always read as a 0.
03	BA1 (Unibus Address Increment Inhibit) Read/Write	When BA1 is set, the controller will not increment the BA register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by Unibus INIT, or Controller Clear. When set during a data transfer, all data words are read from or written into the same memory location.
02-00	U_2U_0 (Unit Select) Read/Write	These bits are written by the program to select a drive. Cleared by Unibus INIT, or Controller Clear. The unit select bits can be changed by the program during data transfer operations, without interfering with the transfer.

22. Attention Summary (RPAS) register (776716).

07	06	05	04	03	02	01	00
ATA_7	ATA_6	ATA_5	ATA_4	ATA_3	ATA_2	ATA_1	ATA_0

BIT	NAME	FUNCTION
07-00	ATA (Attention Active) Read/Write	Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by Unibus INIT, or Controller Clear. Individual bits are cleared by loading a function code with the GO bit, or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect. Each drives' ATA bit is displayed individually in bit 15 of RPDS. Each drive responds in the bit position which corresponds to its unit number; e.g., drive 02 responds in bit position 02.

23. First-in first-out (FIFO) register.

15	14	13	12	11	10	09	08
F_4	F_3	F_2	F_1	F_0	$USEL_2$	$USEL_1$	$USEL_0$

BIT	NAME	FUNCTION
15-11	F_4-F_0 (Function Codes)	Refer to function code listing under RPCS1 register.
10-08	$USEL_2$-$USEL_0$ (Unit Select)	Refer to unit select U_{02}-U_{00} under RPCS2 register.

24. CPA event flag register (CPEVF).

07	06	05	04	03	02	01	00
GC	EC	0	CPL	PE	PR	SR	ACE

BIT	NAME	FUNCTION
07	GC (Go Command)	This eight (8) discrete bit register provides event flags to the Microprocessor.
06	EC (Error Clear)	
05	Not Used	Always read as a 0.
04	CPL (CPU Power Low)	
03	PE (Poll Enable)	
02	PR (Programmed Reset)	
01	SR (System Reset)	
00	ACE (Any CPA Error)	

25. CPA error and control flag register (CPECF).

15	14	13	12	11	10	09	08
/APE	/PEO	/PEE	0	/DBL	/CPR	0	0

BIT	NAME	FUNCTION
15	/APE (Not Address Parity Error)	This eight (8) discrete bit register provides CPA error information to the Microprocessor.
14	/PEO (Not Parity Error Odd Word)	
13	/PEE (Not Parity Error Even Word)	
12	Not Used	Always read as a 0.
11	/DBL (Not Double Word Transfer)	
10	/CPR (Not Cache Interface Present)	
09-08	Not Used	Always read as a 0.

26. File data register (FDR).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
$FDRH_{15}$	$FDRH_{14}$	$FDRH_{13}$	$FDRH_{12}$	$FDRH_{11}$	$FDRH_{10}$	$FDRH_{09}$	$FDRH_{08}$	$FDRL_{07}$	$FDRL_{06}$	$FDRL_{05}$	$FDRL_{04}$	$FDRL_{03}$	$FDRL_{02}$	$FDRL_{01}$	$FDRL_{00}$

BIT	NAME	FUNCTION
15-08	File Data Hi File Data Lo	The File Data register is a 16-bit register accessible only to the Microprocessor. Data to and from the CPA registers and the Microprocessor is via this register.

27. File address register (FAR).

07	06	05	04	03	02	01	00
R/W	FA_{64}	FA_{32}	FA_{16}	FA_{8}	FA_{4}	FA_{2}	FA_{1}

BIT	NAME	FUNCTION
07	R/W	Direction bit. 0 = read and 1 = write.
06-00	FA_{64}-FA_{1} (File Address)	The File Address register is an 8-bit register accessible only to the Microprocessor. The adapter register address is written into this register whenever access to the CPA is required.

	UB ADDR (OCTAL)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	CPA ADDR (OCTAL)
RMCS1	(776700)	SC*	TRE*	0	0	1	0	A17*	A16*	RDY*	IE*	F4	F3	F2	F1	F0	GO	0 THRU 7
RMDS	(776712)	ATA	ERR	0	MOL	WRL	LST	0	1	DRY	VV	0	0	0	0	0	OM	10 THRU 17
RMDA	(776706)	0	0	0	TA_{16}	TA_8	TA_4	TA_2	TA_1	0	0	0	SA_{16}	SA_8	SA_4	SA_2	SA_1	20 THRU 27
RMER1	(776714)	DCK	UNS	0	0	WLE	IAE	AOE	HCRC	HCE	ECH	0	FER	BPAR	0	0	ILF	30 THRU 37
RMSN	(776730)	SN_{38}	SN_{34}	SN_{32}	SN_{31}	SN_{28}	SN_{24}	SN_{22}	SN_{21}	SN_{18}	SN_{14}	SN_{12}	SN_{11}	SN_8	SN_4	SN_2	SN_1	40 THRU 47
RMDC	(776734)	0	0	0	0	0	0	0	DC_{256}	DC_{128}	DC_{64}	DC_{32}	DC_{16}	DC_8	DC_4	DC_2	DC_1	50 THRU 57
RMHR	(776736)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	60 THRU 67
RMOF	(776732)	0	0	0	1	ECCI	HCI	0	0	OFD	0	0	0	0	0	0	0	70 THRU 77
RMWC	(776702)	WC_{15}	WC_{14}	WC_{13}	WC_{12}	WC_{11}	WC_{10}	WC_9	WC_8	WC_7	WC_6	WC_5	WC_4	WC_3	WC_2	WC_1	WC_0	100
RMLA	(776720)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	101 (NE)
RMDB	(776722)	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	102
RMMR1	(776724)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	103 (NE)
RMDT	(776726)	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	104
RMMR2	(776740)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	105
RMER2	(776742)	0	SKI	DF	IVC	0	0	0	0	0	0	0	0	0	0	0	0	106
RMEC1	(776744)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	107 (NE)
RMEC2	(776746)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	110 (NE)
RMCS3	(776752)	APE	DPEO	DPEE	0	0	DBL	0	0	0	IE	0	0	0	0	0	0	111 (PDP-11/70 Only)
RMBA	(776704)	BA_{15}	BA_{14}	BA_{13}	BA_{12}	BA_{11}	BA_{10}	BA_9	BA_8	BA_7	BS_6	BA_5	BA_4	BA_3	BA_2	BA_1	BA_0	120
RMBAE	(776750)	0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16	121 (PDP-11/70 Only)
RMCS2	(776710)	0	WCE	0	NED	NEM	PGE	MXF	0	OR	IR	CLR	0	BA1	U2	U1	U0	122
RMAS	(776716)									ATA_7	ATA_6	ATA_5	ATA_4	ATA_3	ATA_2	ATA_1	ATA_0	123
FIFO		F4	F3	F2	F1	F0	$USEL_2$	$USEL_1$	$USEL_0$									123
CPEVF										GC	EC	0	CPL	PE	PR	SR	ACE	124
CPECF		/APE	/PEO	/PEE	0	/DBL	/CPR	0	0									124
FDR		$FDRH_{15}$	$FDRH_{14}$	$FDRH_{13}$	$FDRH_{12}$	$FDRH_{11}$	$FDRH_{10}$	$FDRH_9$	$FDRH_8$	$FDRL_7$	$FDRL_6$	$FDRL_5$	$FDRL_4$	$FDRL_3$	$FDRL_2$	$FDRL_1$	$FDRL_0$	
FAR										R/W	FA_{64}	FA_{32}	FA_{16}	FA_8	FA_4	FA_2	FA_1	

8 LOGICAL DRIVES

*These bits in RMCS1 are controller bits and are emulated only once, all other bits in RMCS1 are drive bits and are emulated eight times.

Figure 5-3a. RM02/03 CPA Register Summary

1. Control and status 1 (RMCS1) register (776700).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	0	0	1	0	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO

BIT	NAME	FUNCTION
07	RDY (Ready) Read Only	RDY normally = 1. During data transfers, RDY = 0. When a data transfer command code (51_8 - 73_8) is written into RMCS1, RDY is reset. At the termination of the data transfer, RDY is set.

The GO bit (RMCS1, bit 0) must be sent to cause the controller to respond to a command. The GO bit is reset by the controller after command execution. The function code bits are stored in the FIFO. Cleared by Unibus INIT or Controller Clear.

2. Drive status (RMDS) register (776712).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	0	0	MOL	WRL	LST	0	1	DRY	VV	0	0	0	0	OM

BIT	NAME	FUNCTION
05-01	Not Used	Always read as 0.
00	OM (Offset Mode) Read Only	Set when offset command is issued to drive. When set, and a Read Command is received, the offset is performed prior to the execution of the Read. Reset by any of the following actions: 1. Power-Up 2. Mid-Transfer Seek 3. Read-In Preset 4. Write Data or Write Header and Data 5. Return to Centerline 6. Write Desired Cylinder 7. Re-Calibrate

3. Error (RMER1) register (776714).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	0	0	WLE	IAE	AOE	HCRC	HCE	ECH	0	FER	BPAR	0	0	ILF

BIT	NAME	FUNCTION
10	IAE (Invalid Address Error) Read/Write	Set when the address in the Desired Cylinder register (RMDC) and the Desired Sector/Track Address register (RMDA) is invalid and a seek or search operation is initiated. Cleared by Unibus INIT, Drive Clear, Controller Clear, or by writing 0's into the register.
09	AOE (Address Overflow Error) Read/Write	Set when the Desired Cylinder register (RMDC) overflows during a read or write. Cleared by Unibus INIT, Drive Clear, Controller Clear, or by writing 0's into the register. Setting of this bit indicates that the Desired Cylinder Address register has exceeded the maximum cylinder address.

4. Holding (RMHR) register (776736).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
15-00	Not Used	Always read as 0.

5. Offset (RMOF) register (776732).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	1	ECCI	HCI	0	0	OFD	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
07	OFD (Offset Information)	Set when the offset direction is toward the spindle. When reset, the offset direction is away from the spindle. The offset direction bit is invalid if the following three conditions are met. 1. Read Command is loaded into the Control register (RMCS1) (bits 0-5) 2. RMCS1 GO bit is set 3. The offset mode bit (RMDS bit 00) is set
06-00	Not Used	Set to 0 by controller.

6. Maintenance (RMMR2) register (776740).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
15-00	None	Not emulated, set to 0 by the controller.

7. Error (RMER2) register (776742).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	SKI	DF	IVC	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
15	Not Used	Set to 0 by controller.
14	SKI (Seek Incomplete) Read/Write	Set when a seek operation fails to complete within 400 ms from a seek initiation.
13	DF (Drive Fault)	Set when a drive fault occurs.
12	IVC (Invalid Command) Read/Write	Set when volume valid (RMDS bit 6) is reset or unit ready is not active and any command other than read-in preset or pack acknowledge is received. Also set if Drive Clear or No-OP is received. Cleared by INIT, power-up cycle, or by writing 0's into this register.
11-00	Not Used	Set to 0 by controller.

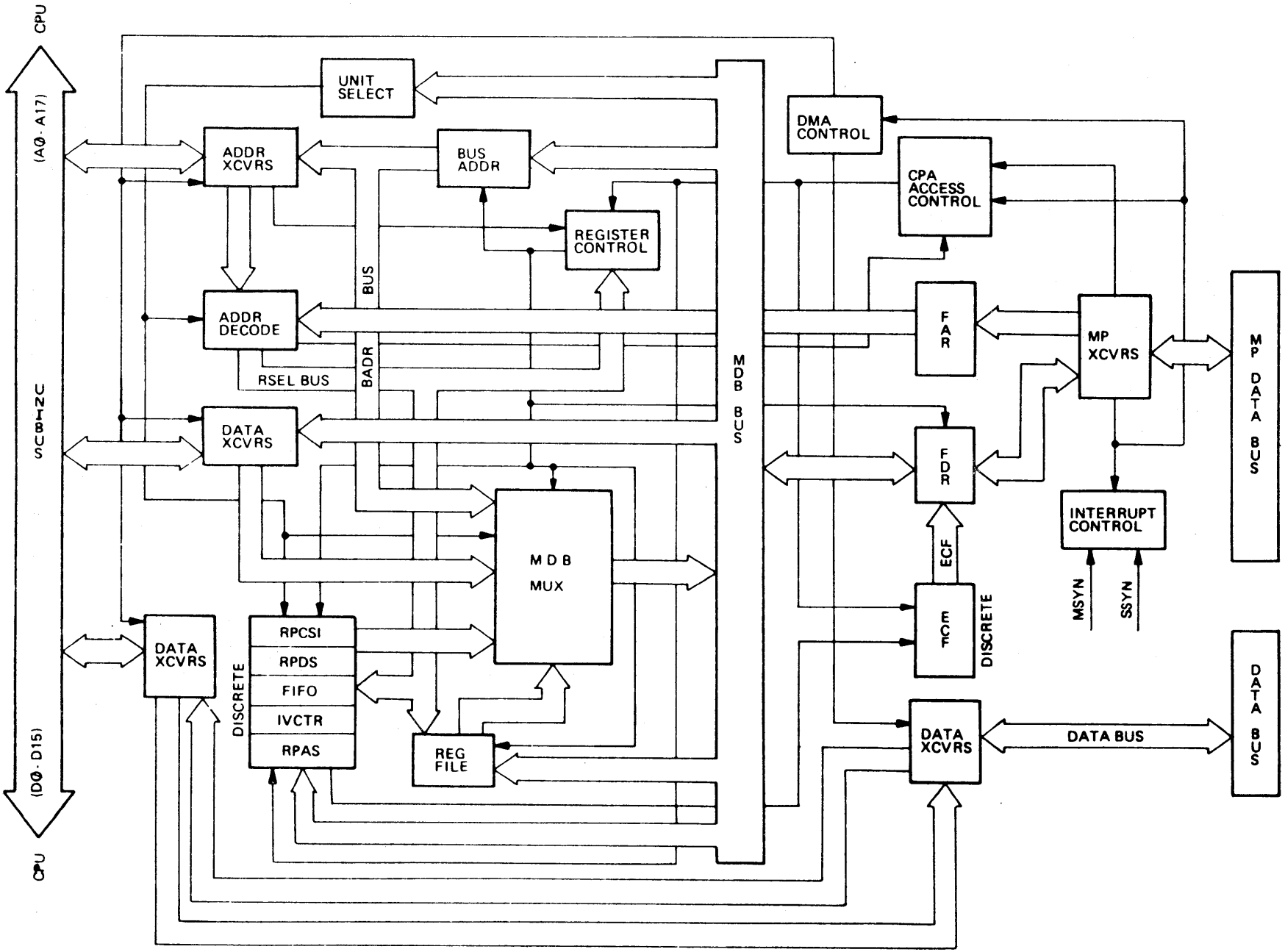
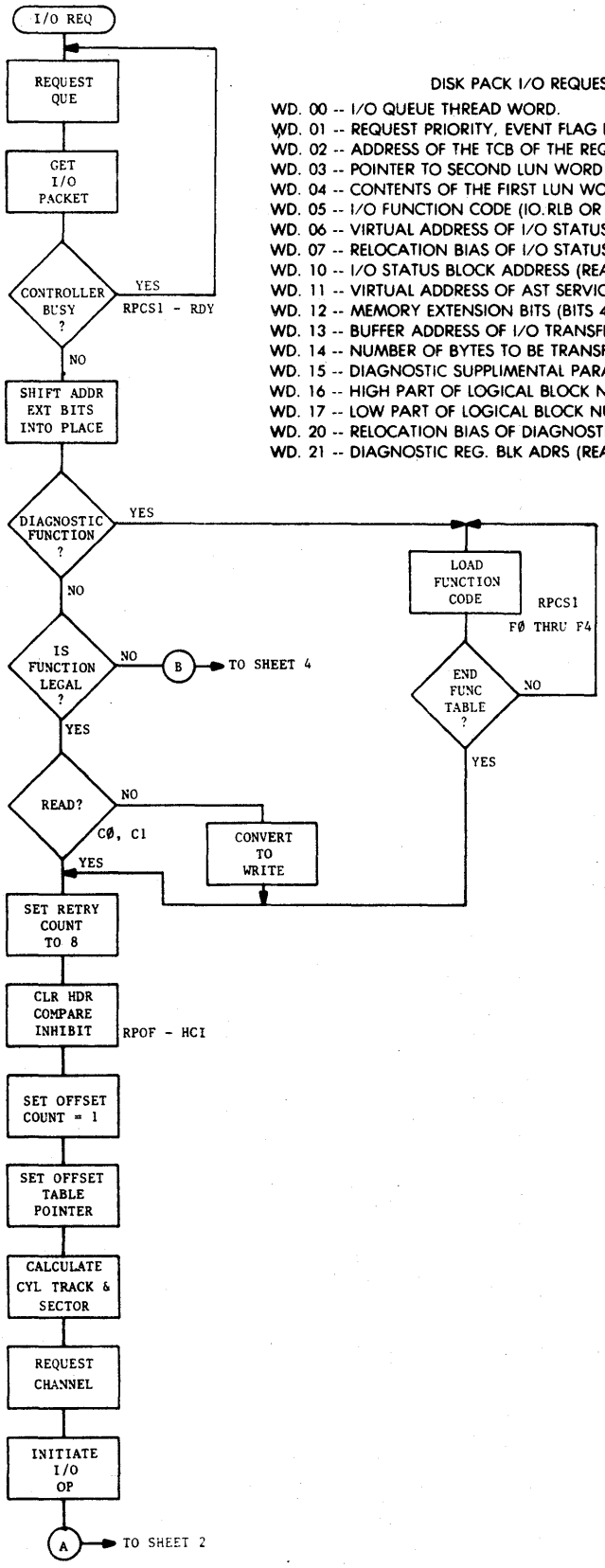


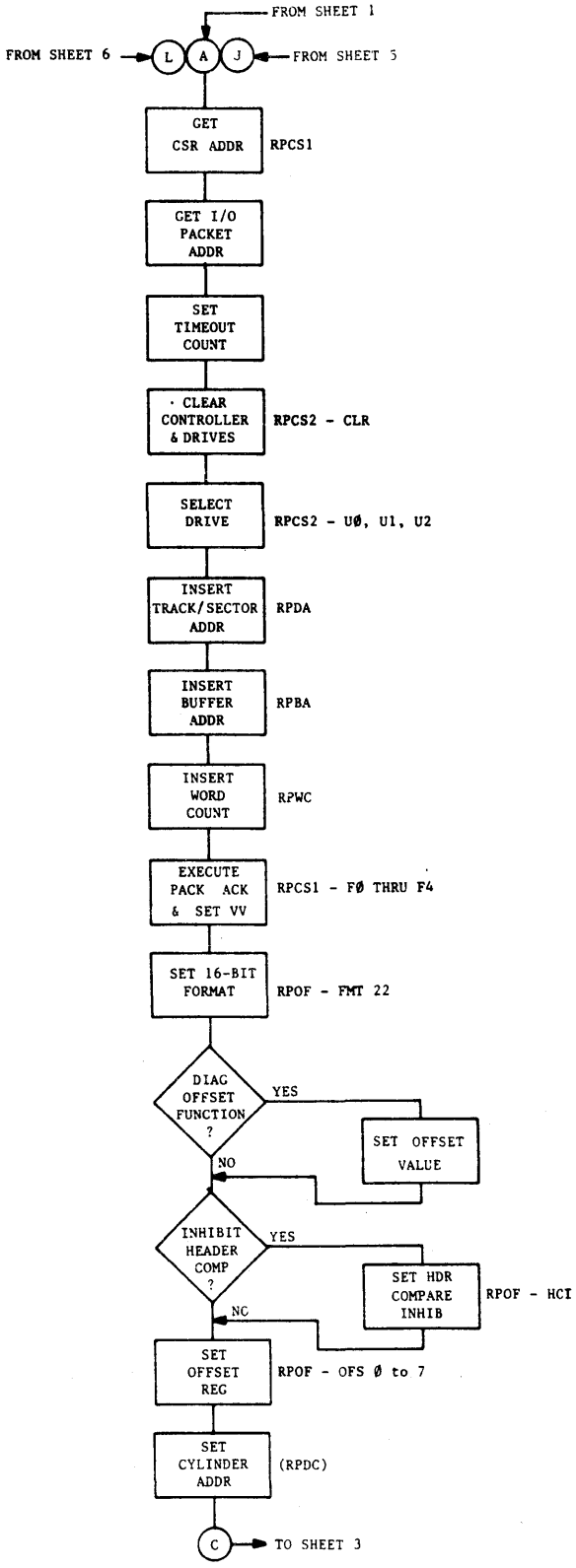
FIGURE 5-4. RP04 CPA BLOCK DIAGRAM



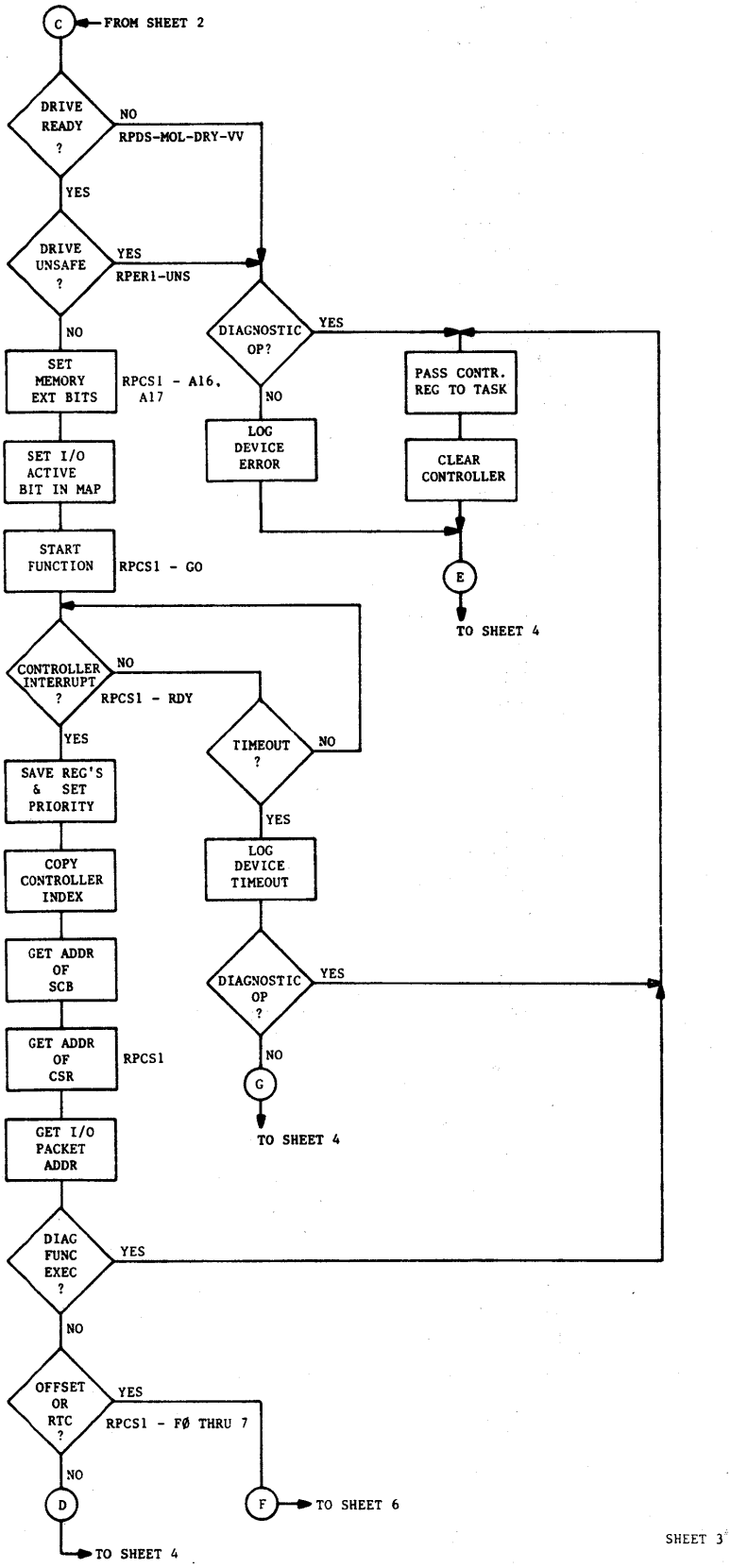
DISK PACK I/O REQUEST PACKET FORMAT

WD. 00 -- I/O QUEUE THREAD WORD.
WD. 01 -- REQUEST PRIORITY, EVENT FLAG NUMBER.
WD. 02 -- ADDRESS OF THE TCB OF THE REQUESTER TASK.
WD. 03 -- POINTER TO SECOND LUN WORD IN REQUESTER TASK HEADER.
WD. 04 -- CONTENTS OF THE FIRST LUN WORD IN REQUESTER TASK HEADER (UCB).
WD. 05 -- I/O FUNCTION CODE (IO.RLB OR IO.WLB).
WD. 06 -- VIRTUAL ADDRESS OF I/O STATUS BLOCK.
WD. 07 -- RELOCATION BIAS OF I/O STATUS BLOCK.
WD. 10 -- I/O STATUS BLOCK ADDRESS (REAL OR DISPLACEMENT + 140000).
WD. 11 -- VIRTUAL ADDRESS OF AST SERVICE ROUTINE.
WD. 12 -- MEMORY EXTENSION BITS (BITS 4 AND 5) OF I/O TRANSFER.
WD. 13 -- BUFFER ADDRESS OF I/O TRANSFER.
WD. 14 -- NUMBER OF BYTES TO BE TRANSFERRED.
WD. 15 -- DIAGNOSTIC SUPPLIMENTAL PARAMETER ELSE NOT USED.
WD. 16 -- HIGH PART OF LOGICAL BLOCK NUMBER AND HIGH BYTE NOT USED.
WD. 17 -- LOW PART OF LOGICAL BLOCK NUMBER OF I/O REQUEST.
WD. 20 -- RELOCATION BIAS OF DIAGNOSTIC REG. BLK ADRS.
WD. 21 -- DIAGNOSTIC REG. BLK ADRS (REAL OR DISPL. + 140000).

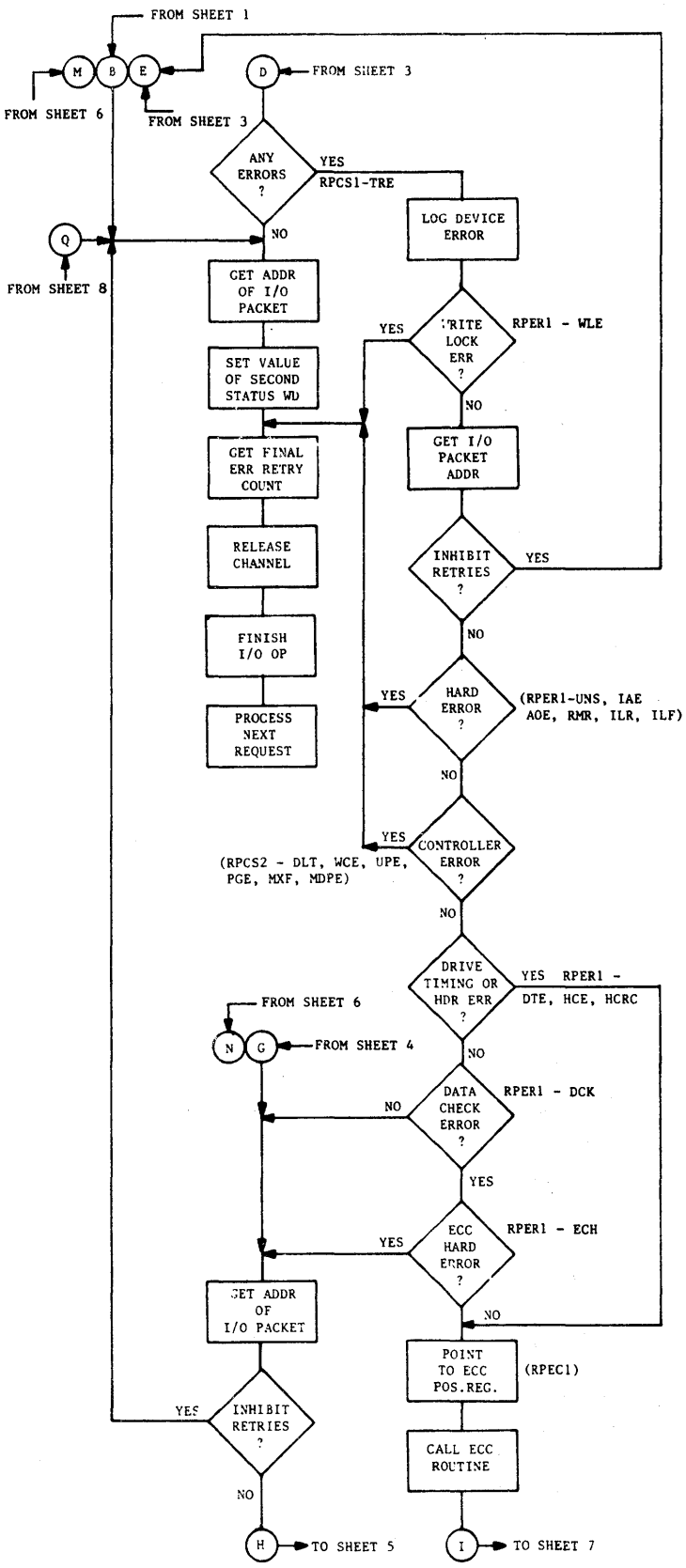
FIGURE 5-5. PDP-11 RP04 DISK HANDLER FLOW CHART


FROM SHEET 1
FROM SHEET 6
L
A
J
FROM SHEET 3
GET CSR ADDR
RPCS1
GET I/O PACKET ADDR
SET TIMEOUT COUNT
CLEAR CONTROLLER & DRIVES
RPCS2 - CLR
SELECT DRIVE
RPCS2 - UØ, U1, U2
INSERT TRACK/SECTOR ADDR
RPDA
INSERT BUFFER ADDR
RPBA
INSERT WORD COUNT
RPWC
EXECUTE PACK ACK & SET VV
RPCS1 - FØ THRU F4
SET 16-BIT FORMAT
RPOF - FMT 22
DIAG OFFSET FUNCTION ?
YES
SET OFFSET VALUE
NO
INHIBIT HEADER COMP ?
YES
SET HDR COMPARE INHIB
RPOF - HCI
NO
SET OFFSET REG
RPOF - OFS Ø to 7
SET CYLINDER ADDR
(RPDC)
C
TO SHEET 3

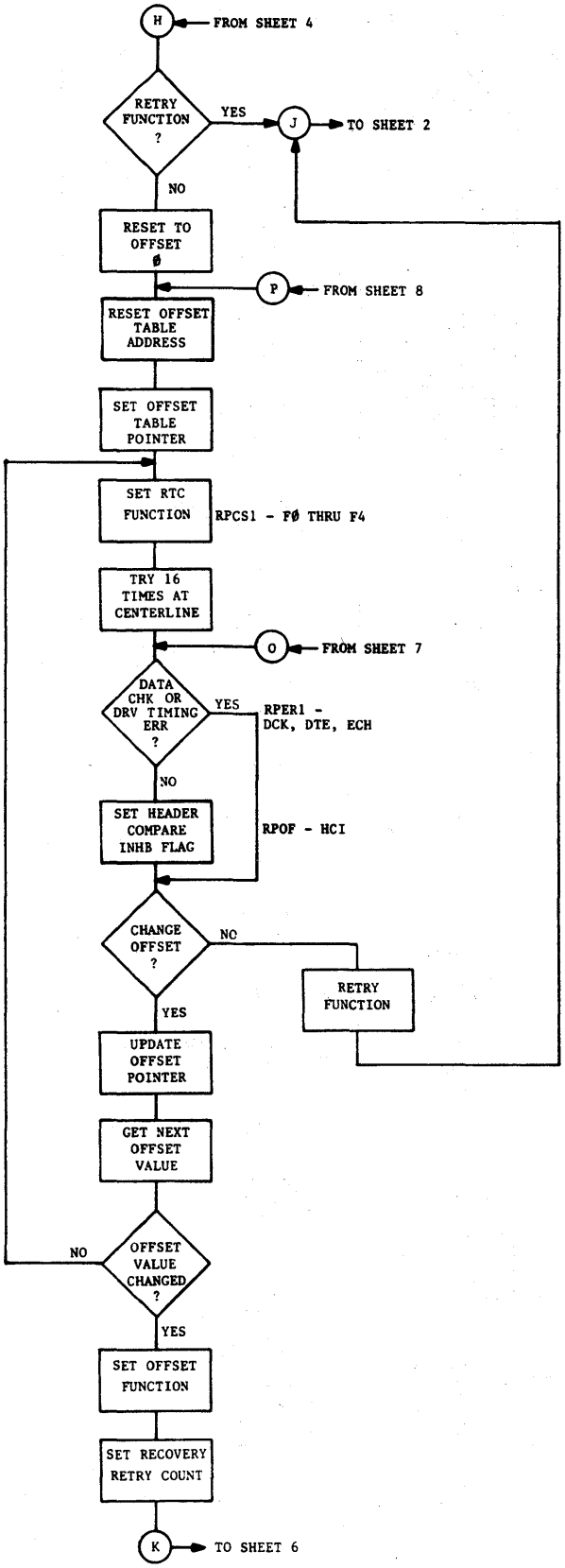
SHEET 2


C
FROM SHEET 2
DRIVE READY ?
NO
RPDS-MOL-DRY-VV
YES
DRIVE UNSAFE ?
YES
RPER1-UNS
NO
SET MEMORY EXT BITS
RPCS1 - A16, A17
SET I/O ACTIVE BIT IN MAP
START FUNCTION
RPCS1 - GO
DIAGNOSTIC OP?
YES
NO
LOG DEVICE ERROR
PASS CONTR. REG TO TASK
CLEAR CONTROLLER
E
TO SHEET 4
CONTROLLER INTERRUPT ?
NO
RPCS1 - RDY
YES
TIMEOUT ?
NO
YES
LOG DEVICE TIMEOUT
SAVE REG'S & SET PRIORITY
COPY CONTROLLER INDEX
GET ADDR OF SCB
GET ADDR OF CSR
RPCS1
GET I/O PACKET ADDR
DIAGNOSTIC OP ?
YES
NO
G
TO SHEET 4
DIAG FUNC EXEC ?
YES
NO
OFFSET OR RTC ?
YES
RPCS1 - FØ THRU 7
NO
D
TO SHEET 4
F
TO SHEET 6

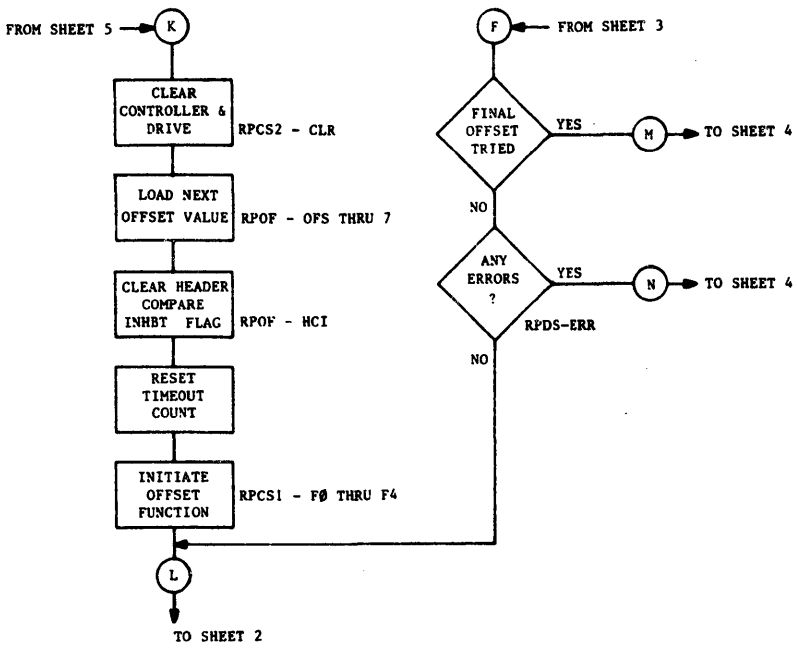
SHEET 3


FROM SHEET 1
M
B
E
FROM SHEET 6
FROM SHEET 3
D
FROM SHEET 3
ANY ERRORS ?
YES
RPCS1-TRE
LOG DEVICE ERROR
NO
Q
FROM SHEET 8
GET ADDR OF I/O PACKET
WRITE LOCK ERR ?
YES
RPER1 - WLE
NO
SET VALUE OF SECOND STATUS WD
GET FINAL ERR RETRY COUNT
GET I/O PACKET ADDR
RELEASE CHANNEL
INHIBIT RETRIES ?
YES
NO
FINISH I/O OP
HARD ERROR ?
YES
(RPER1-UNS, IAE AOE, RMR, ILR, ILF)
NO
PROCESS NEXT REQUEST
CONTROLLER ERROR ?
YES
(RPCS2 - DLT, WCE, UPE, PGE, MXF, MDPE)
NO
DRIVE TIMING OR HDR ERR ?
YES RPER1 - DTE, HCE, HCRC
FROM SHEET 6
N
G
FROM SHEET 4
NO
DATA CHECK ERROR ?
NO
RPER1 - DCK
YES
ECC HARD ERROR ?
YES
RPER1 - ECH
NO
GET ADDR OF I/O PACKET
POINT TO ECC POS.REG.
(RPEC1)
INHIBIT RETRIES ?
YES
CALL ECC ROUTINE
NO
H
TO SHEET 5
I
TO SHEET 7

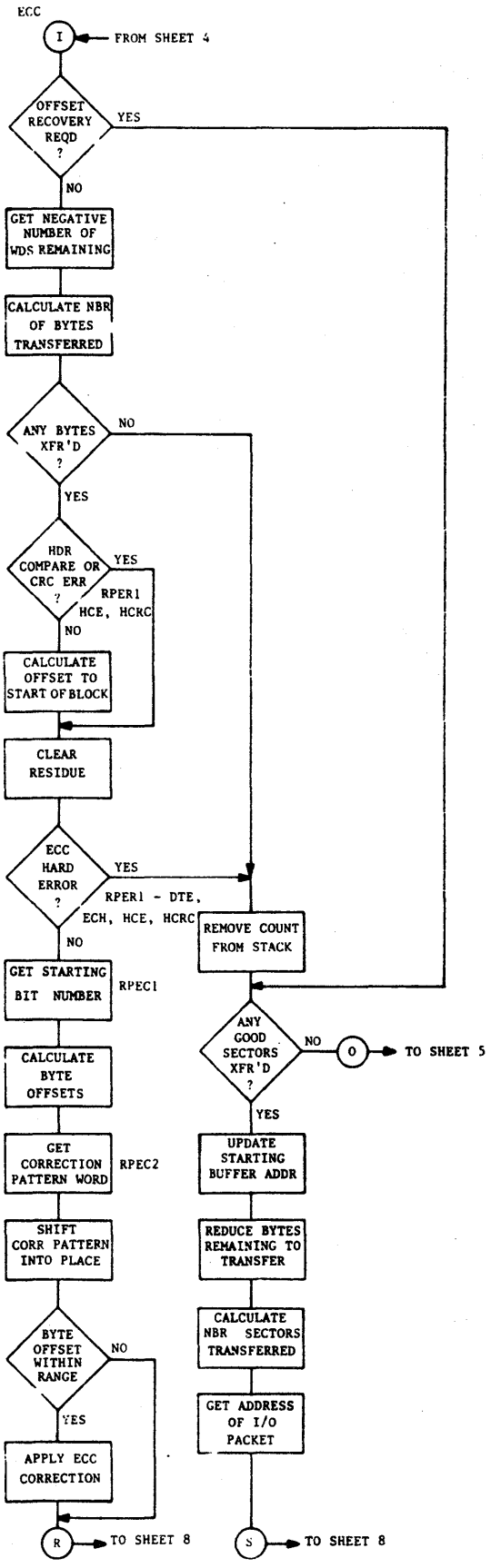
SHEET 4


H
FROM SHEET 4
RETRY FUNCTION ?
YES
J
TO SHEET 2
NO
RESET TO OFFSET Ø
P
FROM SHEET 8
RESET OFFSET TABLE ADDRESS
SET OFFSET TABLE POINTER
SET RTC FUNCTION
RPCS1 - FØ THRU F4
TRY 16 TIMES AT CENTERLINE
O
FROM SHEET 7
DATA CHK OR DRV TIMING ERR ?
YES
RPER1 - DCK, DTE, ECH
NO
SET HEADER COMPARE INHB FLAG
RPOF - HCI
CHANGE OFFSET ?
NO
RETRY FUNCTION
YES
UPDATE OFFSET POINTER
GET NEXT OFFSET VALUE
OFFSET VALUE CHANGED ?
NO
YES
SET OFFSET FUNCTION
SET RECOVERY RETRY COUNT
K
TO SHEET 6

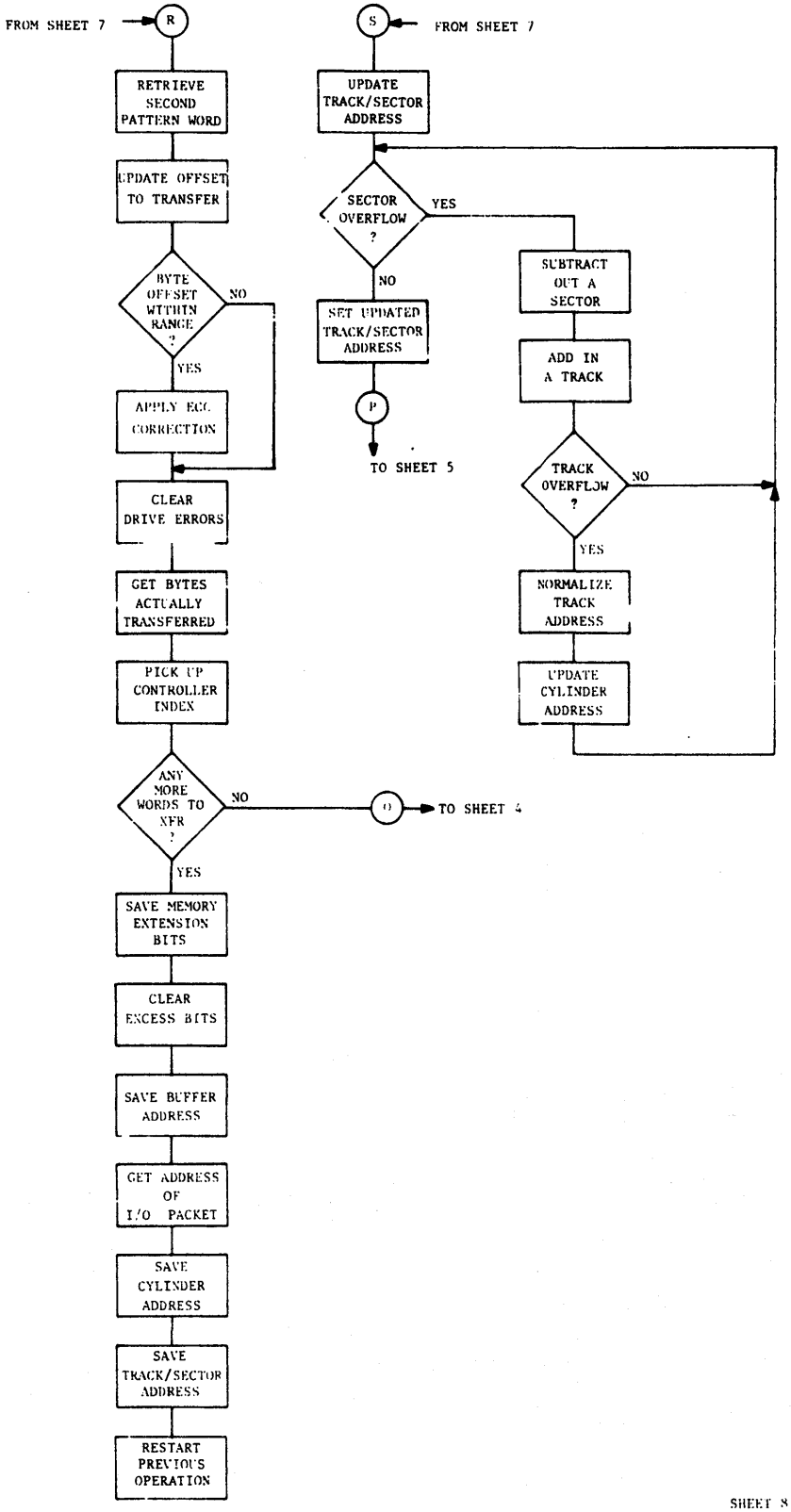
SHEET 5


FROM SHEET 5
K
CLEAR CONTROLLER & DRIVE
RPCS2 - CLR
LOAD NEXT OFFSET VALUE
RPOF - OFS THRU 7
CLEAR HEADER COMPARE INHBT FLAG
RPOF - HCI
RESET TIMEOUT COUNT
INITIATE OFFSET FUNCTION
RPCS1 - FØ THRU F4
L
TO SHEET 2
F
FROM SHEET 3
FINAL OFFSET TRIED
YES
M
TO SHEET 4
NO
ANY ERRORS ?
YES
N
TO SHEET 4
RPDS-ERR
NO

SHEET 6


ECC
I
FROM SHEET 4
OFFSET RECOVERY REQD ?
YES
NO
GET NEGATIVE NUMBER OF WDS REMAINING
CALCULATE NBR OF BYTES TRANSFERRED
ANY BYTES XFR'D ?
NO
YES
HDR COMPARE OR CRC ERR ?
YES
RPER1
HCE, HCRC
NO
CALCULATE OFFSET TO START OF BLOCK
CLEAR RESIDUE
ECC HARD ERROR ?
YES
RPER1 - DTE, ECH, HCE, HCRC
NO
REMOVE COUNT FROM STACK
GET STARTING BIT NUMBER
RPEC1
CALCULATE BYTE OFFSETS
GET CORRECTION PATTERN WORD
RPEC2
SHIFT CORR PATTERN INTO PLACE
BYTE OFFSET WITHIN RANGE
NO
YES
APPLY ECC CORRECTION
ANY GOOD SECTORS XFR'D ?
NO
O
TO SHEET 5
YES
UPDATE STARTING BUFFER ADDR
REDUCE BYTES REMAINING TO TRANSFER
CALCULATE NBR SECTORS TRANSFERRED
GET ADDRESS OF I/O PACKET
R
TO SHEET 8
S
TO SHEET 8

SHEET 7


FROM SHEET 7
R
RETRIEVE SECOND PATTERN WORD
UPDATE OFFSET TO TRANSFER
BYTE OFFSET WITHIN RANGE ?
NO
YES
APPLY ECC CORRECTION
CLEAR DRIVE ERRORS
GET BYTES ACTUALLY TRANSFERRED
PICK UP CONTROLLER INDEX
ANY MORE WORDS TO XFR ?
NO
O
TO SHEET 4
YES
SAVE MEMORY EXTENSION BITS
CLEAR EXCESS BITS
SAVE BUFFER ADDRESS
GET ADDRESS OF I/O PACKET
SAVE CYLINDER ADDRESS
SAVE TRACK/SECTOR ADDRESS
RESTART PREVIOUS OPERATION
S
FROM SHEET 7
UPDATE TRACK/SECTOR ADDRESS
SECTOR OVERFLOW ?
YES
NO
SET UPDATED TRACK/SECTOR ADDRESS
P
TO SHEET 5
SUBTRACT OUT A SECTOR
ADD IN A TRACK
TRACK OVERFLOW ?
NO
YES
NORMALIZE TRACK ADDRESS
UPDATE CYLINDER ADDRESS

SHEET 8

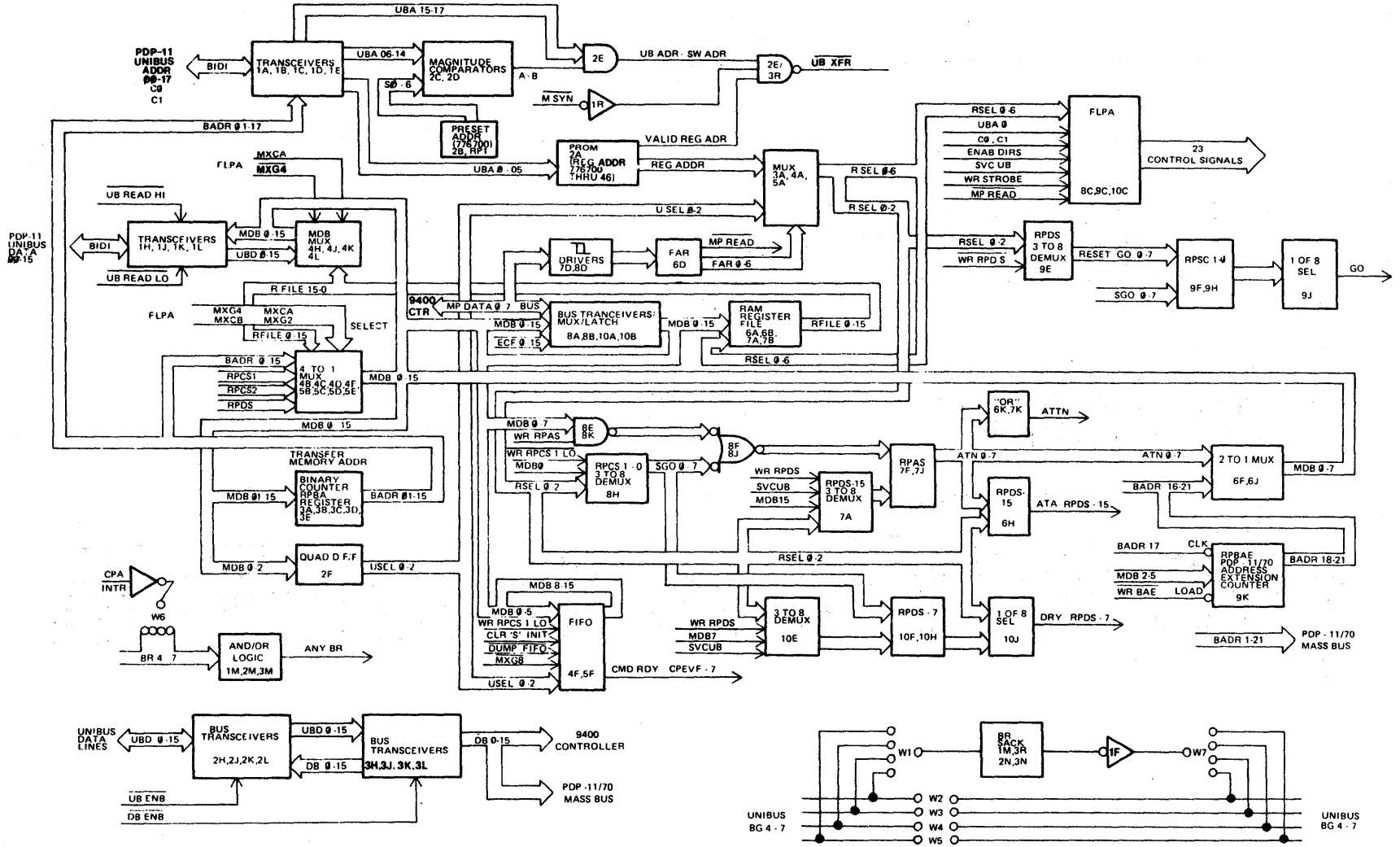


FIGURE 5-6. 9400 RP04 CPA LOGIC BUS DIAGRAM

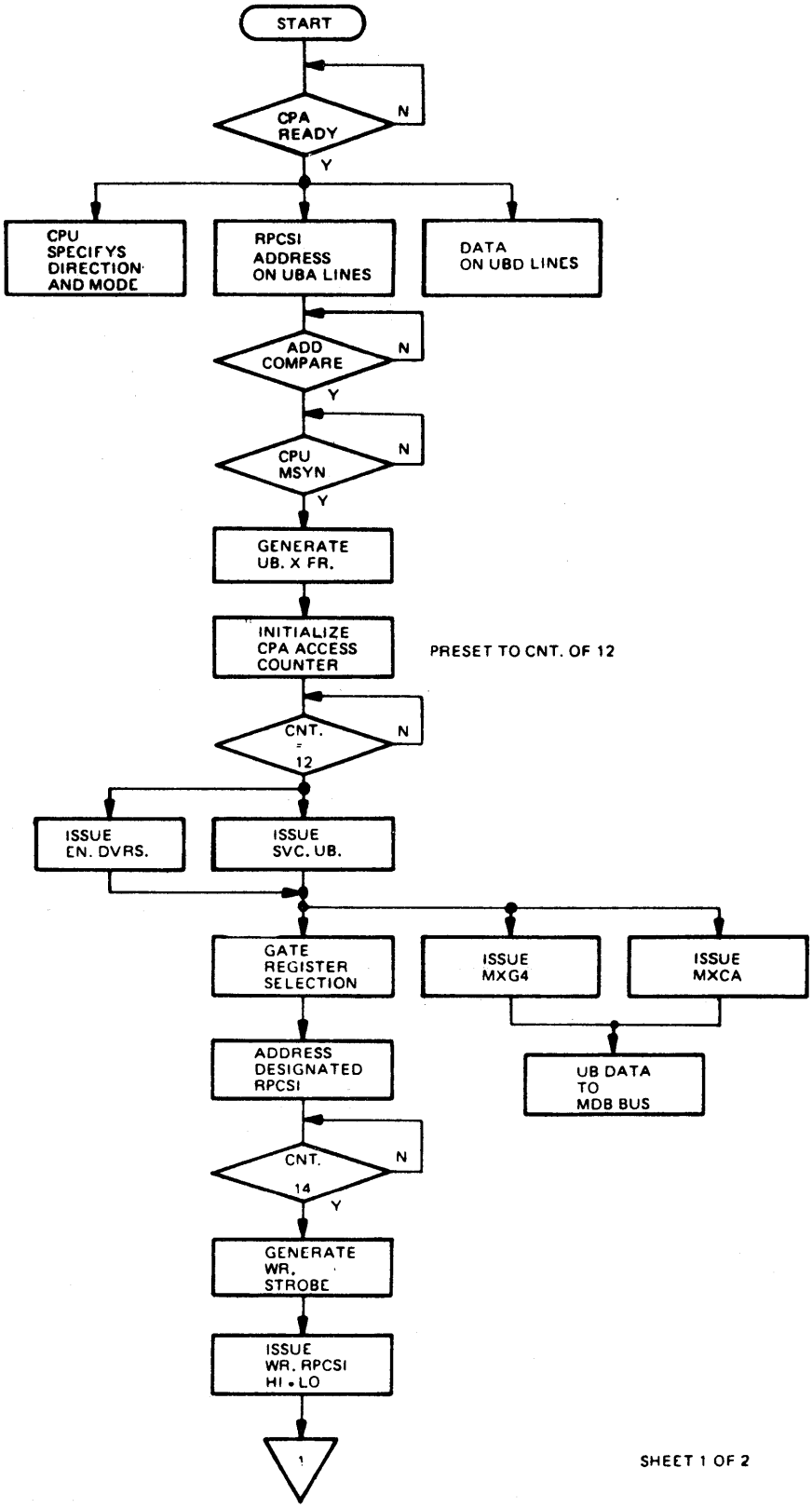
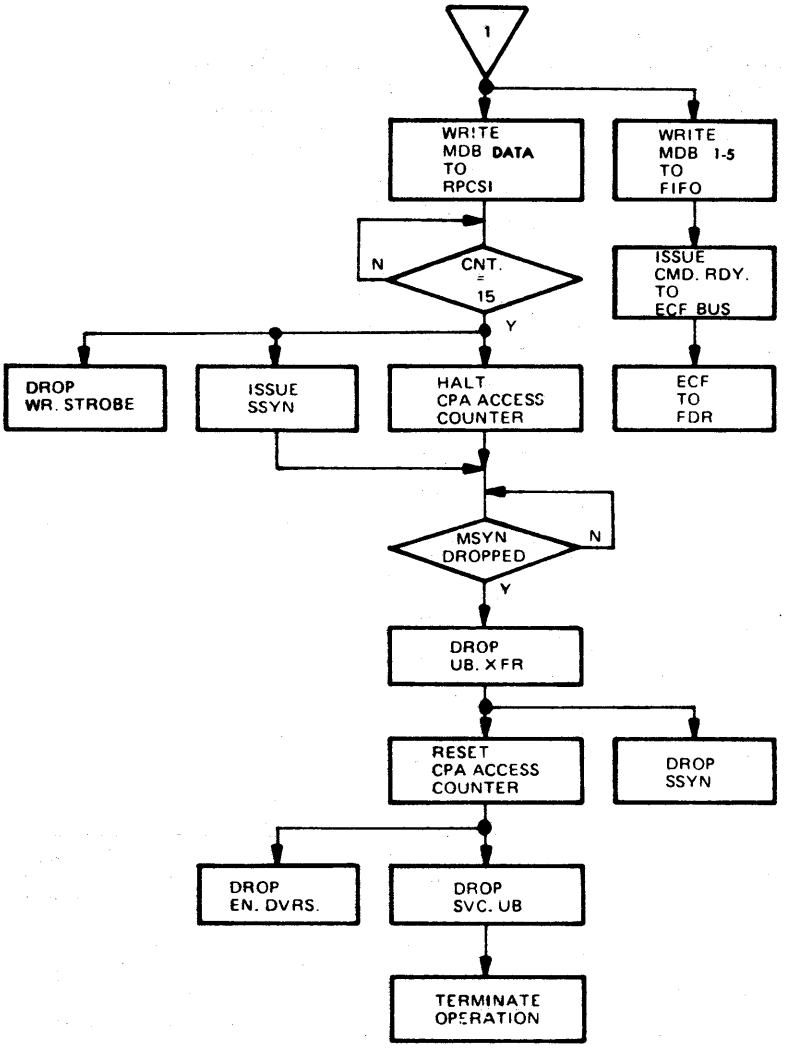


FIGURE 5-7. 9400 RP04 CPA, CPU REGISTER WRITE (RPCS1) FLOW CHART

CPU REGISTER WRITE
(RPCSI)



SHEET 2 OF 2

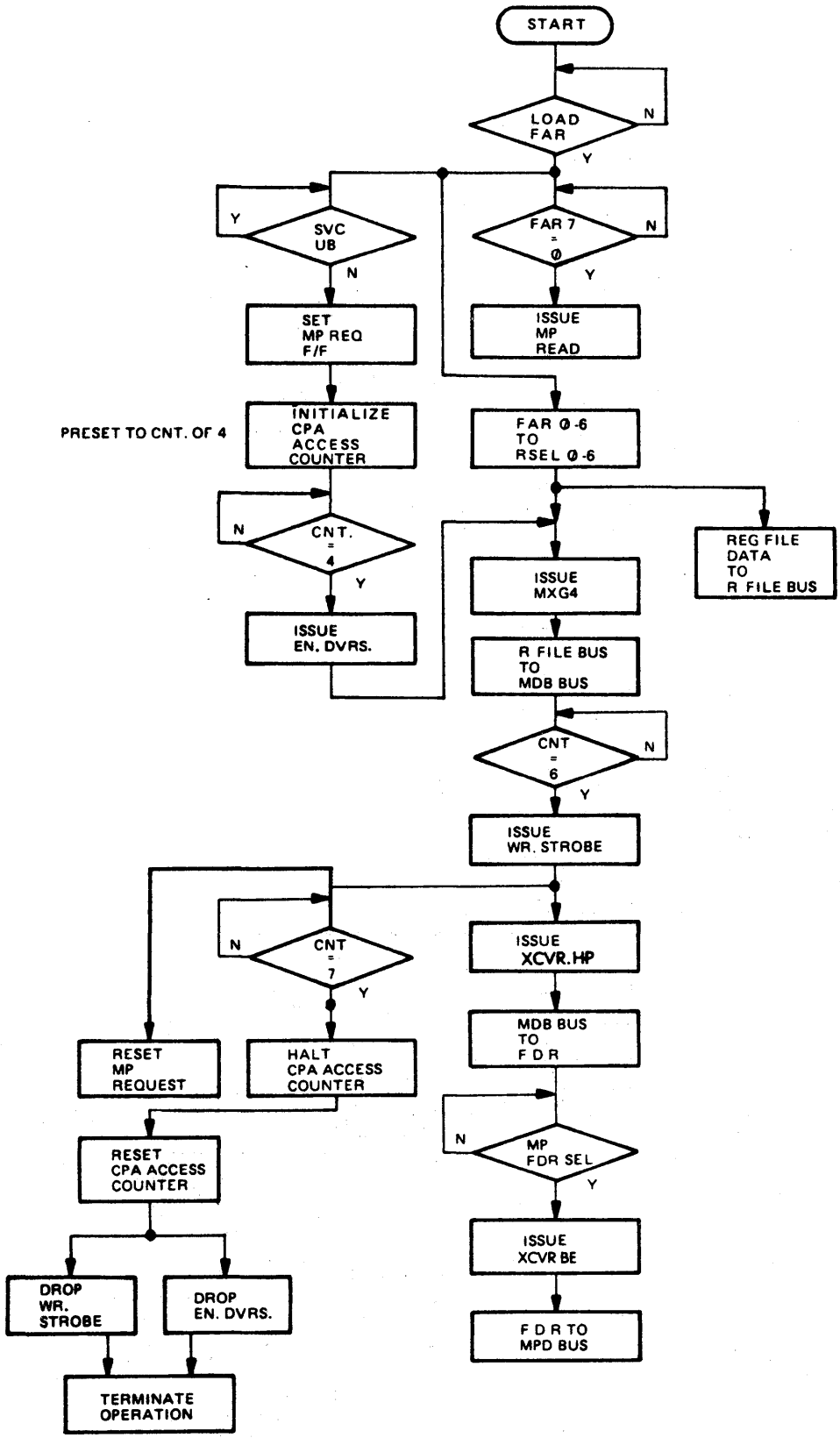
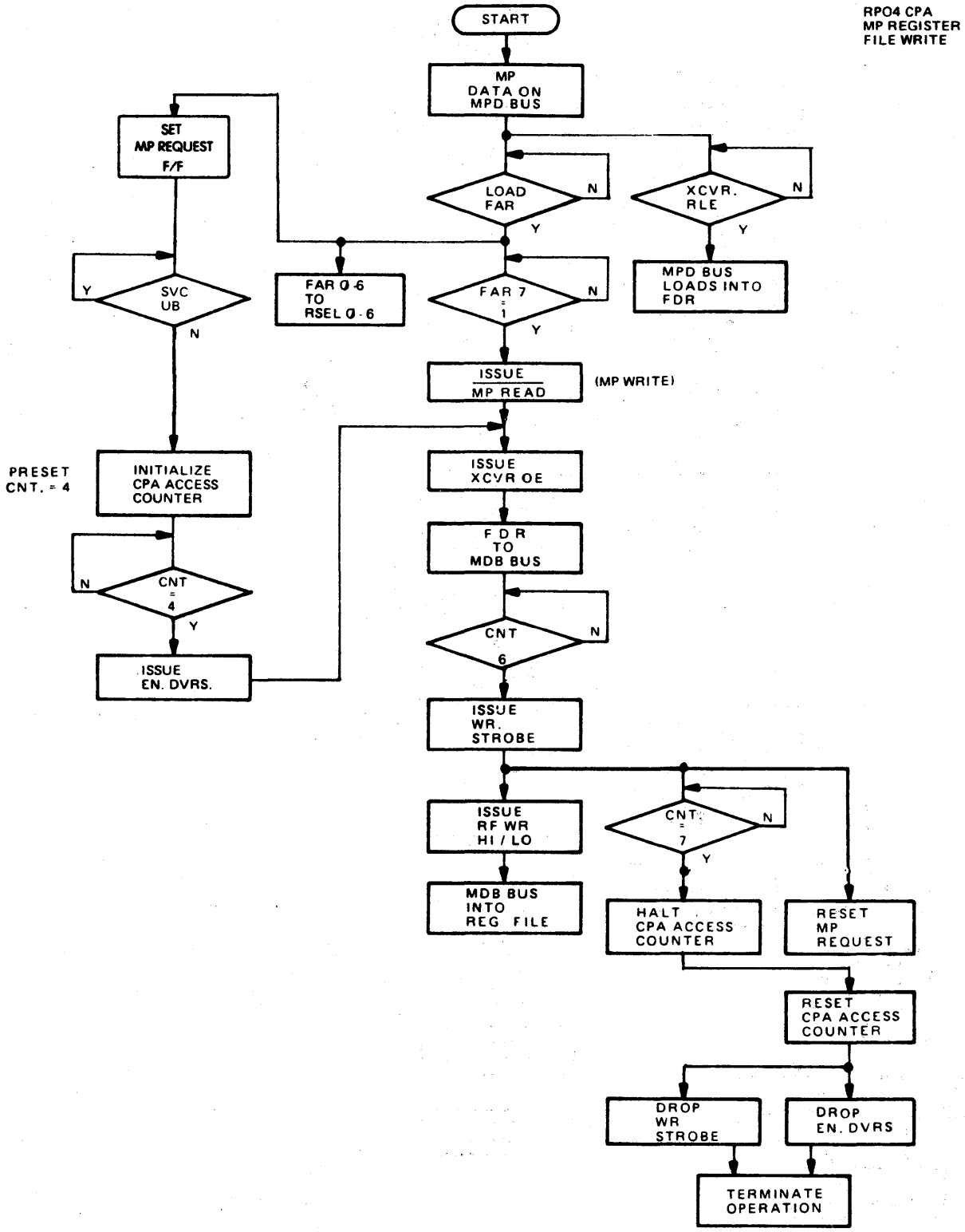


FIGURE 5-8. 9400 RP04 CPA, MICROPROCESSOR REGISTER FILE READ FLOW CHART



SHEET 1 OF 1

FIGURE 5-9. 9400 RP04 CPA, MICROPROCESSOR REGISTER FILE WRITE FLOW CHART

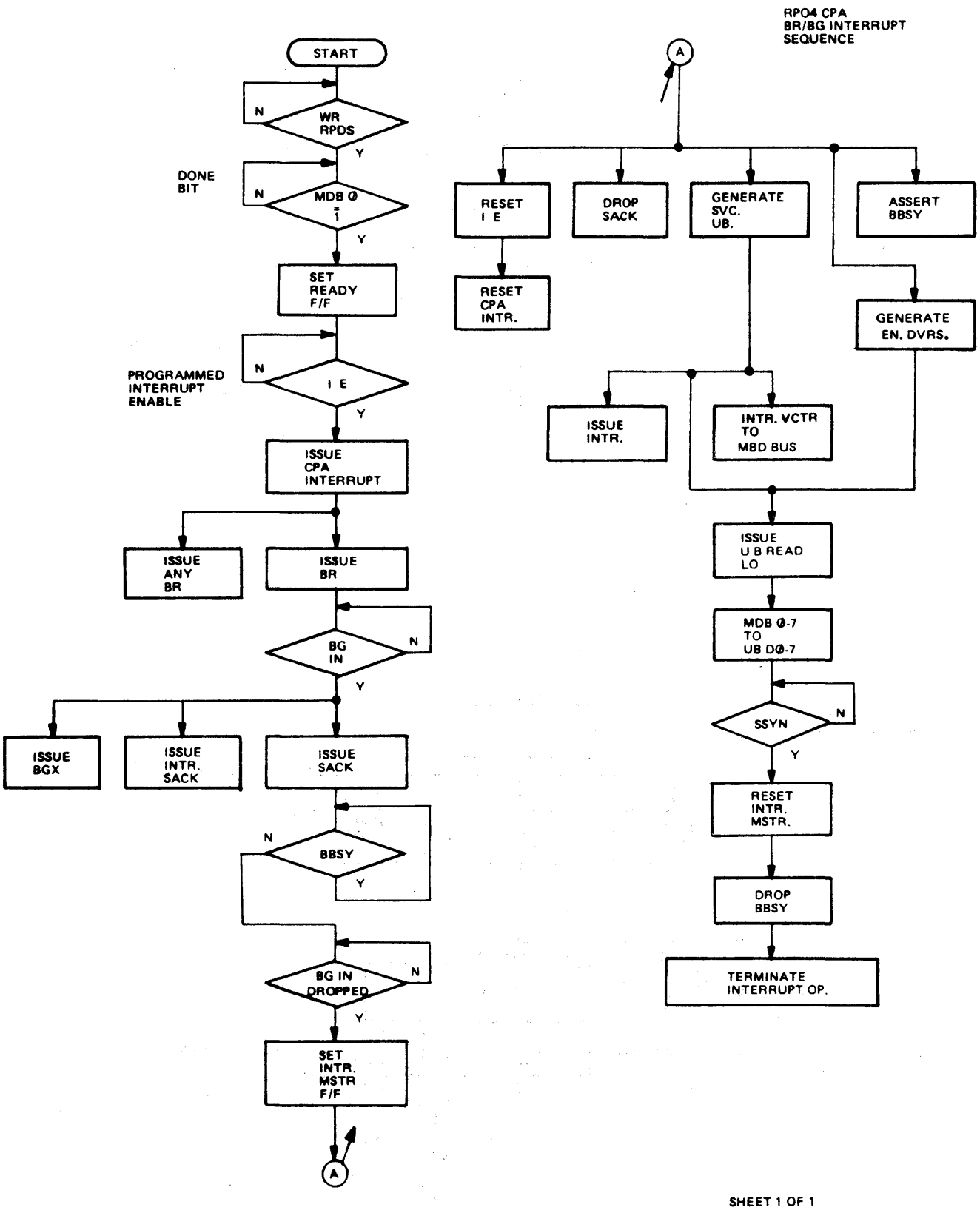


FIGURE 5-10. 9400 RP04 CPA, BUS REQUEST/BUS GRANT INTERRUPT SEQUENCE FLOW CHART

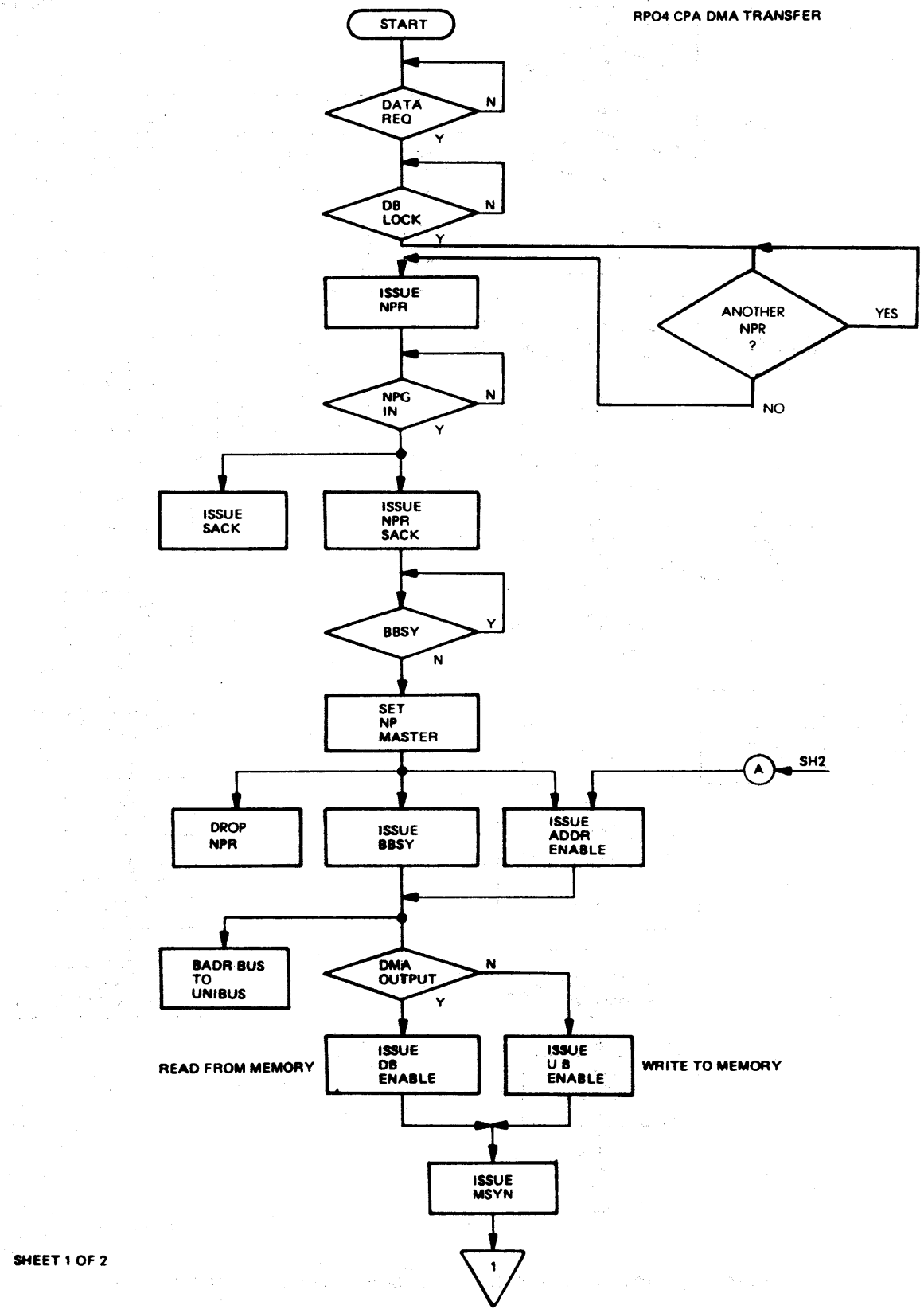
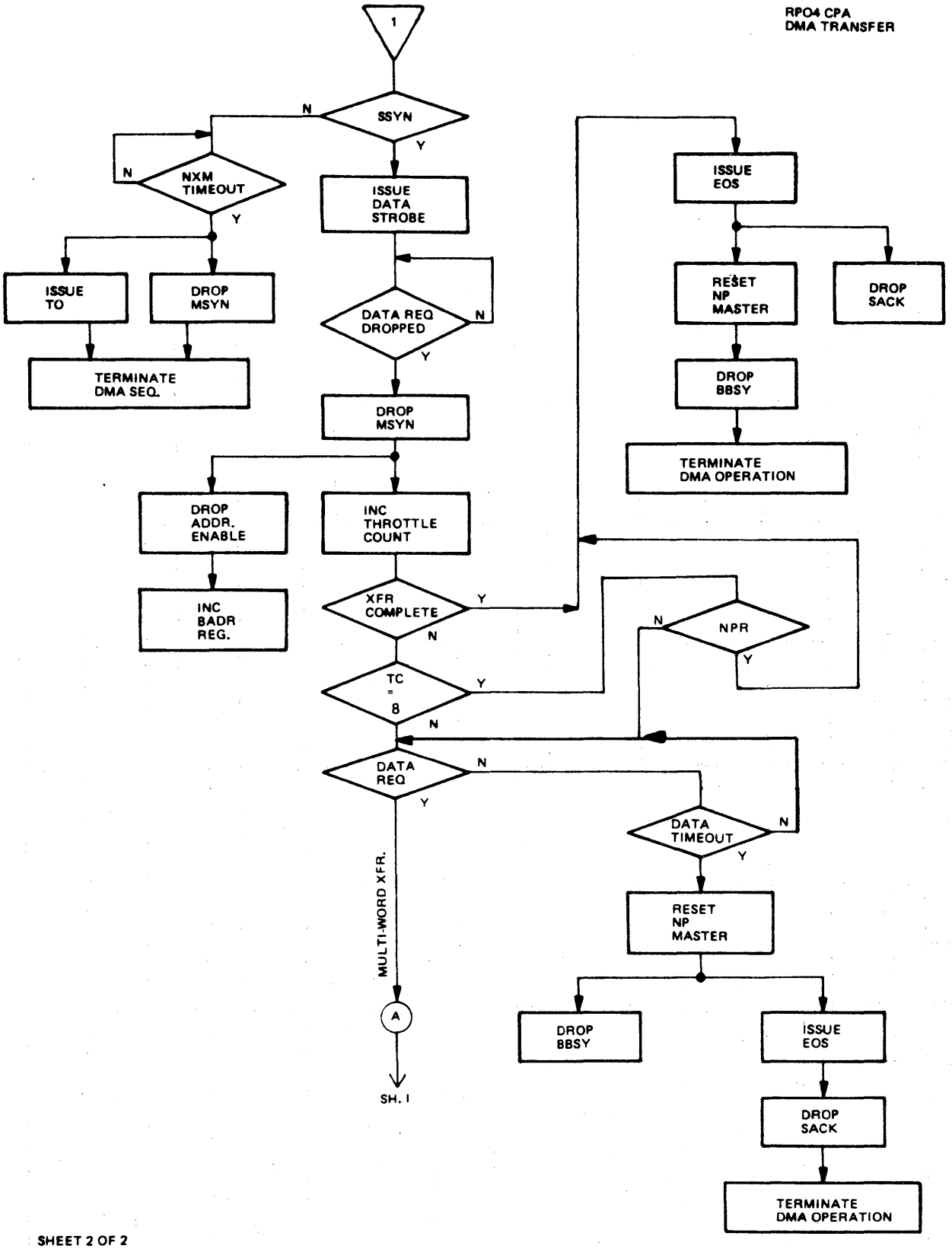


FIGURE 5-11. 9400 RP04 CPA, DIRECT MEMORY ACCESS TRANSFER FLOW CHART


RPO4 CPA
DMA TRANSFER
1
SSYN
N
Y
NXM TIMEOUT
N
Y
ISSUE DATA STROBE
ISSUE TO
DROP MSYN
TERMINATE DMA SEQ.
DATA REQ DROPPED
N
Y
DROP MSYN
DROP ADDR. ENABLE
INC BADR REG.
INC THROTTLE COUNT
XFR COMPLETE
Y
N
TC = 8
Y
N
NPR
N
Y
DATA REQ
N
Y
MULTI-WORD XFR.
A
SH. 1
DATA TIMEOUT
N
Y
RESET NP MASTER
DROP BBSY
ISSUE EOS
DROP SACK
TERMINATE DMA OPERATION
ISSUE EOS
RESET NP MASTER
DROP SACK
DROP BBSY
TERMINATE DMA OPERATION

SHEET 2 OF 2

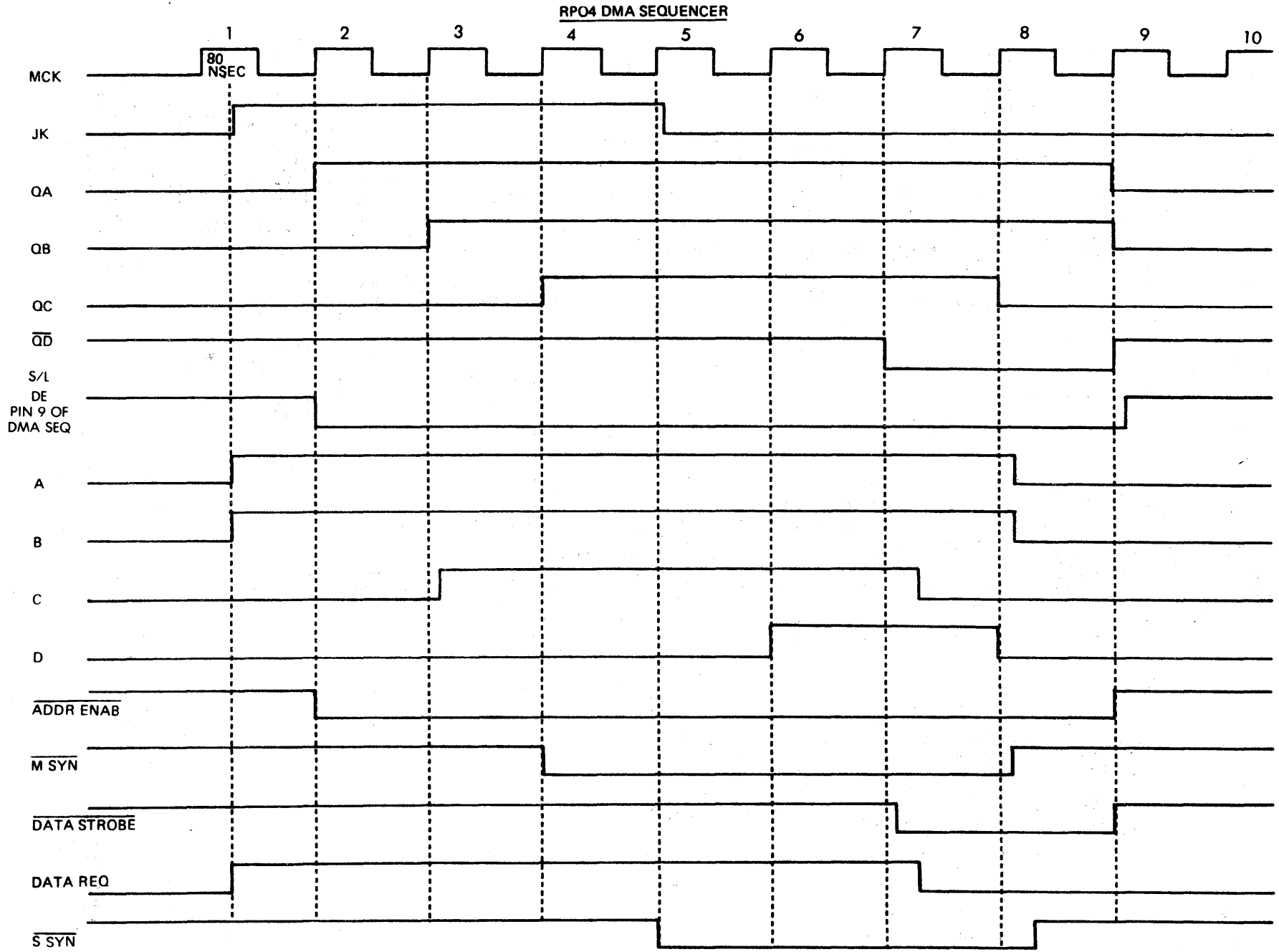


FIGURE 5-12. 9400 RP04 CPA, DIRECT MEMORY ACCESS SEQUENCER TIMING DIAGRAM

Table 5-5. RP04 CPA UNIBUS Address Decode PROM (IC 2A) Map

Binary Address					Octal Address	Output Data								Octal	Selected Register
E	D	C	B	A		D8	D7	D6	D5	D4	D3	D2	D1		
0	0	0	0	0	00	1	0	0	0	0	0	0	0	200	RPCS1
0	0	0	0	1	01	1	1	0	0	0	0	0	0	300	RPWC
0	0	0	1	0	02	1	1	0	1	0	0	0	0	320	RPBA
0	0	0	1	1	03	1	0	0	1	0	0	0	0	220	RPDA
0	0	1	0	0	04	1	1	0	1	0	0	1	0	322	RPCS2
0	0	1	0	1	05	1	0	0	0	1	0	0	0	210	RPDS
0	0	1	1	0	06	1	0	0	1	1	0	0	0	230	RPER1
0	0	1	1	1	07	1	1	0	1	0	0	1	1	323	RPAS
0	1	0	0	0	10	1	1	0	0	0	0	0	1	301	RPLA
0	1	0	0	1	11	1	1	0	0	0	0	1	0	302	RPDB
0	1	0	1	0	12	1	1	0	0	0	0	1	1	303	RPMR
0	1	0	1	1	13	1	1	0	0	0	1	0	0	304	RPDT
0	1	1	0	0	14	1	0	1	0	0	0	0	0	240	RPSN
0	1	1	0	1	15	1	0	1	1	1	0	0	0	270	RPOF
0	1	1	1	0	16	1	0	1	0	1	0	0	0	250	RPDC
0	1	1	1	1	17	1	0	1	1	0	0	0	0	260	RPCC
1	0	0	0	0	20	1	1	0	0	0	1	0	1	305	RPER2
1	0	0	0	1	21	1	1	0	0	0	1	1	0	306	RPER3
1	0	0	0	0	22	1	1	0	0	0	1	1	1	307	RPEC1
1	0	0	1	1	23	1	1	0	0	1	0	0	0	310	RPEC2
1	0	1	0	0	24	X	1	0	1	0	0	0	0[1]	021[2]	RHBAE[4]
1	0	1	0	1	25	X	1	0	0	1	0	0	1[1]	011[3]	RHCS3[4]
1	0	1	1	0	26	0	-	-	-	-	-	-	0	000	Not Used
1	0	1	1	1	27	0	-	-	-	-	-	-	0	000	Not Used
1	1	0	0	0	30	0	-	-	-	-	-	-	0	000	Not Used
1	1	0	0	1	31	0	-	-	-	-	-	-	0	000	Not Used
1	1	0	1	0	32	0	-	-	-	-	-	-	0	000	Not Used
1	1	0	1	1	33	0	-	-	-	-	-	-	0	000	Not Used
1	1	1	0	0	34	0	-	-	-	-	-	-	0	000	Not Used
1	1	1	0	1	35	0	-	-	-	-	-	-	0	000	Not Used
1	1	1	1	0	36	0	-	-	-	-	-	-	0	000	Not Used
1	1	1	1	1	37	0	-	-	-	-	-	-	0	000	Not Used

Notes: [1] X equals a 1 for PDP-11/70, 0 for all others

[2] Output is Octal 321 for PDP-11/70

[3] Output is Octal 311 for PDP-11/70

[4] Used for PDP-11/70 only

1. RPBA

   a) UB WRITE RPBA

      /WR BADR
      MXG4
      MXCA

   b) MP WRITE RPBA

      /WR BADR
      XCVR OE

   c) UB READ RPBA

      UB READ HI
      UB READ LO
      MXG2
      MXCB

   d) MP READ RPBA

      MXG2
      MXCB
      XCVR CP

2. RPCS1

   a) UB WRITE RPCS1

      WR RPCS1 H/L
      MXG4
      MXCA

   b) MP WRITE RPCS1

      WR RPCS1 H/L
      XCVR OE

   c) UB READ RPCS1

      UB READ HI
      UB READ LO
      MXG2

   d) MP READ RPCS1

      MXG2
      XCVR CP

3. RPCS2

   a) UB WRITE

      WR RPCS2 HI/LO
      MXG4
      MXCA

   b) MP WRITE

      WR RPCS2 HI/LO
      XCVR OE

   c) UB READ

      UB READ HI/LO
      MXG2
      MXCA
      MXCB

   d) MP READ

      MXG2
      MXCA
      MXCB
      XCVR CP

4. RPDS

   a) UB WRITE - Not Permitted

   b) MP WRITE

      WR RPDS
      XCVR OE

   c) UB READ

      MXCA
      MXG2
      UB READ HI/LO

   d) MP READ

      MXCA
      MXG2
      XCVR CP

5. RPAS/FIFO*

   a) UB WRITE

      MXCA
      MXG4
      WR RPAS

   b) MP WRITE - Not Permitted

   c) UB READ

      MXG8
      UB READ LO

   d) MP READ *MP ONLY

      MXG8
      XCVR CP

6. RPBAE

   a) UB WRITE

      MXCA
      MXG4
      WR BAE

b) MP WR

XCVR OE
WR BAE

c) UB READ

MXCA
MXG8
UB READ LO

d) MP READ

MXCA
MXG8
XCVR CP

7. ALL OTHER REGISTERS

a) UB WRITE

MXCA
MXG4
RF WR HI/LO

b) MP WRITE

XCVR OE
RF WR HI/LO

c) UB READ

MXG4
UB READ HI/LO

d) MP READ

MXG4
XCVR CP

8. ECF

a) MP READ

XCVR SEL
XCVR CP

RP04 CPA
FPLA REGISTER CONTROL OUTPUTS

Inputs required to generate FPLA control output signals appear directly below the numbered FPLA control output signals.

1. /WR BADR (ADDR=120)

   C1 · SVC UB · WR STROBE · RSEL6 · /RSEL5 · RSEL4 · /RSEL3 · /RSEL2 · /RSEL1 · /RSEL0
   + /SVC UB · WR STROBE · /MP RD · RSEL6 · /RSEL5 · RSEL4 · /RSEL3 · /RSEL2 · /RSEL1 · /RSEL0

2. /WR BAE (ADDR=121)

   C1 · SVC UB · WR STROBE · RSEL6 · /RSEL5 · RSEL4 · /RSEL3 · /RSEL2 · /RSEL1 · RSEL0
   + /SVC UB · WR STROBE · /MP RD · RSEL6 · /RSEL5 · RSEL4 · /RSEL3 · /RSEL2 · /RSEL1 · RSEL0

3. /WR RPCS1 HI (ADDR=0-7)

   C1 · /C0 · SVC UB · WR STROBE · /RSEL6 · /RSEL5 · /RSEL4 · /RSEL3
   + C1 · C0 · A00 · SVC UB · WR STROBE · /RSEL6 · /RSEL5 · /RSEL4 · /RSEL3
   + /SVC UB · WR STROBE · /MP RD · /RSEL6 · /RSEL5 · /RSEL4 · /RSEL3

4. /WR RPCS1 LO (ADDR=0-7)

   C1 · /C0 · SVC UB · WR STROBE · /RSEL6 · /RSEL5 · /RSEL4 · /RSEL3
   + C1 · C0 · /A00 · SVC UB · WR STROBE · /RSEL6 · /RSEL5 · /RSEL4 · /RSEL3
   + /SVC UB · WR STROBE · /MP RD · /RSEL6 · /RSEL5 · /RSEL4 · /RSEL3

5. /WR RPCS2 HI (ADDR=122)

   C1 · /C0 · SVC UB · WR STROBE · RSEL6 · /RSEL5 · RSEL4 · /RSEL3 · /RSEL2 · RSEL1 · /RSEL0
   + C1 · C0 · SVC UB · A00 · WR STROBE · RSEL6 · /RSEL5 · RSEL4 · /RSEL3 · /RSEL2 · RSEL1 · /RSEL0
   + /SVC UB · /MP RD · WR STROBE · RSEL6 · /RSEL5 · RSEL4 · /3 · /2 · 1 · /0

6. /WR RPCS2 LO (ADDR=122)

   C1 · /C0 · SVC UB · WR STROBE · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0
   + C1 · C0 · /A00 · SVC UB · WR STROBE · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0
   + /SVC UB · /MP RD · WR STROBE · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0

7. XCVR SEL - SELECT ECF REGISTERS

   RSEL6 · /5 · 4 · /3 · 2 · /1 · /0

8. XCVR CP - LOCK MDB INTO LATCHES

   /SVC UB · MP RD · WR STROBE

9. XCVR OE - DRIVE MDB

   /SVC UB · /MP RD · ENAB DVRS

10. /RF WR HI (ADDR=0-77, 100-117, 122)

SVC UB · C1 · /C0 · WR STROBE · /RSEL6
+ SVC UB · C1 · /C0 · WR STROBE · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0
+ SVC UB · C1 · C0 · A00 · WR STROBE · /RSEL6
+ SVC UB · C1 · C0 · A00 · WR STROBE · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0
+ /SVC UB · /MP RD · WR STROBE · /RSEL6
+ /SVC UB · /MP RD · WR STROBE · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0
+ SVC UB · C1 · /C0 · WR STROBE · RSEL6 · /5 · /4
+ SVC UB · C1 · C0 · A00 · WR STROBE · RSEL6 · /5 · /4
+ /SVC UB · /MP RD · WR STROBE · RSEL6 · /5 · /4

11. /RF WR LO (ADDR=0-77, 100-117, 122)

SVC UB · C1 · /C0 · WR STR · /RSEL6
+ SVC UB · C1 · /C0 · WR STR · RSEL6 · /5 · /4
+ SVC UB · C1 · /C0 · WR STR · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0
+ SVC UB · C1 · C0 · /A00 · WR STROBE · /RSEL6
+ SVC UB · C1 · C0 · /A00 · WR STR · RSEL6 · /5 · /4
+ SVC UB · C1 · C0 · A00 · WR STR · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0
+ /SVC UB · /MP READ · WR STR · /RSEL6
+ /SVC UB · /MP READ · WR STR · RSEL6 · /5 · /4
+ /SVC UB · /MP READ · WR STR · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0

12. /WR RPDS (ADDR 10-17)

/SVC UB · /MP RD · WR STROBE · /RSEL6 · /5 · /4 · 3

13. WR RPAS (ADDR 123)

SVC UB · C1 · WR STROBE · RSEL6 · /5 · 4 · /3 · /2 · 1 · 0
+ /SVC UB · /MP READ · WR STROBE · RSEL6 · /5 · 4 · /3 · /2 · 1 · 0

14. DUMP FIFO (ADDR 50-57)

/SVC UB · MP RD · WR STROBE · /RSEL6 · 5 · /4 · 3

15. MXCA MUX "A" SELECT

SET FOR FOLLOWING REGISTERS:

UNIBUS WRITE
RPCS2 READ
RPDS READ
RPBAE READ

SVC UB · C1 · /IVEN
+ SVC UB · /C1 · /RSEL6 · /5 · /4 · 3 · /IVEN
+ SVC UB · /C1 · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0 · /IVEN
+ SVC UB · /C1 · RSEL6 · /5 · 4 · /3 · /2 · /1 · 0 · /IVEN
+ /SVC UB · MP RD · /RSEL6 · /5 · /4 · 3 · /IVEN
+ /SVC UB · MP RD · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0 · /IVEN
+ /SVC UB · MP RD · RSEL6 · /5 · 4 · /3 · /2 · /1 · 0 · /IVEN

16. MXCB MUX "B" SELECT

SET FOR FOLLOWING CONDITIONS:

RPBA READ
RPCS2 READ

SVC UB · /C1 · RSEL6 · /5 · 4 · /3 · /2 · /1 · /0
+ SVC UB · /C1 · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0
+ /SVC UB · MP RD · RSEL6 · /5 · 4 · /3 · /2 · /1 · /0
+ /SVC UB · MP RD · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0

17. MXG2 MUX "ENABLE 2"

ENABLE LINE FOR MUX SWITCHING:

RPCS1
RPCS2
RPDS
RPBA

SVC UB · /C1 · ENAB DVRS · /RSEL6 · /5 · /4 · /3 · /IV EN
+ SVC UB · /C1 · ENAB DVRS · /RSEL6 · /5 · /4 · 3 · /IV EN
+ SVC UB · /C1 · ENAB DVRS · RSEL6 · /5 · 4 · /3 · /2 · /1 · /0 · /IV EN
+ SVC UB · /C1 · ENAB DVRS · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0 · /IV EN
+ /SVC UB · MP RD · ENAB DVRS · /RSEL6 · /5 · /4 · /3 · /IV EN
+ /SVC UB · MP RD · ENAB DVRS · /RSEL6 · /5 · /4 · 3 · /IV EN
+ /SVC UB · MP RD · ENAB DVRS · RSEL6 · /5 · 4 · /3 · /2 · /1 · /0 · /IV EN
+ /SVC UB · MP RD · ENAB DVRS · RSEL6 · /5 · 4 · /3 · /2 · 1 · /0 · /IV EN

18. MXG4 MUX "ENABLE 4"

ENAB LINE FOR:

UB TO CPA WRITE
RFILE READ (LOC'NS 20-117)

SVC UB · C1 · ENAB DVRS · /IV EN
+ SVC UB · /C1 · /RSEL6 · RSEL5 · ENAB DVRS · /IV EN
+ SVC UB · /C1 · /RSEL6 · 4 · ENAB DVRS · /IV EN
+ /SVC UB · MP RD · ENAB DVRS · /RSEL6 · 5 · /IV EN
+ /SVC UB · MP RD · ENAB DVRS · /RSEL6 · 4 · /IV EN
+ /SVC UB · MP RD · ENAB DVRS · RSEL6 · /RSEL5 · /4 · /IV EN

19. MXG8 MUX "ENAB 8"

ENAB LINE FOR:

RPBAE
RPAS

SVC UB · /C1 · ENAB DVRS · RSEL6 · /5 · 4 · /3 · /2 · /1 · 0
+ SVC UB · /C1 · ENAB DVRS · RSEL6 · /5 · 4 · /3 · /2 · 1 · 0
+ /SVC UB · MP RD · ENAB DVRS · RSEL6 · /5 · 4 · /3 · /2 · /1 · 0
+ /SVC UB · MP RD · ENAB DVRS · RSEL6 · /5 · 4 · /3 · /2 · 1 · 0

20. /UB READ HI

TRUE FOR ALL UB READS EXCEPT RPBAE, RPAS (121, 123)

SVC UB · /C1 · ENAB DVRS · /RSEL6 · /IV ENAB
+ SVC UB · /C1 · ENAB DVRS · RSEL6 · /RSEL4 · /IV ENAB
+ SVC UB · /C1 · ENAB DVRS · RSEL6 · RSEL4 · /RSEL0 · /IV ENAB

21. /UB READ LO

TRUE FOR ALL UB READS

SVC UB · /C1 · ENAB DVRS + IV ENAB

22. WRCS1 + CS3 (ADD 0-7, 111)

STROBE FOR IE

SVC UB · C1 · /C0 · WR STROBE · /RSEL6 · /RSEL5 · /RSEL4 · /RSEL3
+ SVC UB · C1 · C0 · /A00 · WR STROBE · /RSEL6 · /RSEL5 · /RSEL4 · /RSEL3
+ /SVC UB · WR STROBE · /MP RD · /RSEL6 · /RSEL5 · /RSEL4 · /RSEL3
+ SVC UB · C1 · /C0 · WR STROBE · RSEL6 · /RSEL5 · /RSEL4 · RSEL3 · /RSEL2 · /RSEL1 · RSEL0
+ SVC UB · C1 · C0 · /A00 · WR STROBE · RSEL6 · /RSEL5 · /RSEL4 · RSEL3 · /RSEL2 · /RSEL1 · RSEL0
+ /SVC UB · WR STROBE · /MP RD · RSEL6 · /RSEL5 · /RSEL4 · RSEL3 · /RSEL2 · /RSEL1 · RSEL0

23. SEL BAE + CS3 (ADD 111, 121)

RSEL6 · /RSEL5 · RSEL3 · /RSEL2 · /RSEL1 · RSEL0
+ RSEL6 · /RSEL5 · RSEL4 · /RSEL3 · /RSEL2 · /RSEL1 · RSEL0

5-4. **CONTROLLER.** The System Industries 9400 Controller is a 5¼-inch high rack mountable enclosure with slide rails. The enclosure contains a power supply with a cooling fan, a Basic Control Circuit Card Assembly (CCA), a Control Store CCA, one to four Computer Interface CCAs, and one to four Drive Interface CCAs. Each interface CCA has connectors for attaching the Computer Port Adapter or Storage Drive cables.

The controller provides the minicomputer with a means of attaching from one to four physical disk drive units. Interface options permit the drives to be attached to the controller via daisy chain or radial connection. Up to four minicomputers may share the controller and attached disk drives with the computer multiport option.

The Basic Controller provides a standardized signal interface to the Computer Port Adapter (CPA), and the adapter is unique to each specific minicomputer. The Computer Port Adapter, as its name implies, adapts the minicomputers programmed I/O bus and DMA bus to the controllers standardized interface. The basic controller in addition contains an associated set of firmware for each Computer Port Adapter, to interpret commands and map control parameters required by the basic controller and disk drive. Status conditions are transmitted to the adapter in the format required by the minicomputer. The basic controller standardized interface is broken into two separate independent paths; one for data and one for control information. The basic controller interprets and executes commands to the disk, generates status and interrupts to the minicomputer via the CPA, and in addition, provides standard disk formatter functions, multisector data buffering, and error detection and correction options.

An important feature of the controller is the capability to emulate certain disk controllers and drives normally supplied by popular minicomputer manufacturers and to provide compatibility with the mainframes operating system software. The emulation feature permits volume characteristics to be emulated, but not performance, however, in many cases performance of the emulated disk will be exceeded. Diagnostic compatibility with those supplied by the mainframe manufacturer will not be ensured, however, System Industries supplies its own diagnostic package, both macro and micro levels. Disk format compatibility is not provided during emulation due to the physical drive characteristics being different, and the need to standardize the format. The emulation normally does not utilize the full capacity of the attached disk drive. To achieve full capacity utilization, each emulator has a mode which can be selected, called Extended Emulation. In the extended mode a minimal system software change is required to increase the addressing capability for cylinder, head, and sector parameters.

The basic controller contains a general purpose 8-bit microprocessor to provide control over the functional elements, supervision of data transfers, handling of communication between the port adapter and controller, mapping of various control parameters, disk control, error correction code calculations to provide correction of data, and implementation of special features. The microprocessor is one chip of a microcomputer imbedded in the controller design. The microprogram which directs controller functions is implemented on a control store CCA consisting of read only memory (PROM) and a scratchpad (RAM).This control program is referred to as firmware, and many functions normally performed by hardware are implemented by a combination of firmware and microcomputer. Hardware registers, including the data buffer, in the basic controller are treated as a portion of the memory addresses accessed directly by micro instructions executed by the microprocessor.

The basic controller provides data buffering of up to four full sectors to match the minicomputers DMA data rate to that of high speed disk drives. Data late or data overrun conditions caused by slow responses from the minicomputer during block data transfers are entirely eliminated. Furthermore, if a minicomputer attached is much slower characteristically or due to system loading, and the data buffer cannot be filled or emptied within the time required to maintain sector synchronization with the disk, no errors occur. Instead, the controller allows performance to degrade and simply waits for the disk to take a revolution until the associated sectors data can be moved to or from the buffer. With ECC data errors encountered in disk data which are classified as soft or correctable errors are automatically corrected within the data buffer before it is transmitted to the system. The ECC thereby becomes transparent to the host system, with the only noticeable effect one of a slowdown in data transfer when errors are detected. Error correction will take one disk revolution or less. The controllers data buffering also permits it to be connected anywhere on the system's bus as far as priority is concerned due to data transfer speeds.

The controller performs a cyclic redundancy check (CRC) on all header fields and automatic address verification ahead of all data fields read or written. The sector data has ECC appended to detect errors in the serial disk data. The CRC code is implemented with a sixteen bit polynomial, capable of detecting single, double, and triple bit errors. The ECC option is implemented with a 56-bit polynomial, capable of detecting error bursts of 22 bits in length and correcting all error bursts of 11 bits length or less. Data integrity may be further assured with the Data Buffer Parity Check option in the basic controller which generates and checks parity on each 8-bit byte of data stored in the buffer during write, read, or verify operations.

Many optional features may be installed on the controller, including Computer Multiport, Check Data Command, and Auto Formatting. All of the optional features are not available to the attached system when operating with an emulation package, however, a third mode called System Industries Standard is available to allow all features to be used. The System Industries Standard is not compatible with existing operating systems, but allows for utilization by customers generating their own software. The System Industries Standard cannot coexist in the controller with the Standard Emulator or Extended Emulator, but a controller can be field upgraded from an emulation package to System Industries Standard with selected features.

Servicing of the controller is enhanced by incorporating microdiagnostics into the design. The microdiagnostics are capable of isolating faults to a particular functional element or PCB within the controller and communicating error messages by displaying error codes in a set of maintenance indicators. The microdiagnostics checks for basic functioning by performing go, no-go type tests.

a. Controller Functional Elements. The 9400 Controller is comprised of six functional elements; Computer Port Adapter, Computer Interface, Operation Control, Data Control, Disk Control, and Disk Interface Port. The functions of each of these elements will be covered individually in the following subsections. Figure 5-1 provides a block diagram of these elements and the bus and interface structure used.

1. Computer port adapter. The Computer Port Adapter provides the interface between the host minicomputer and the 9400 Controller. In conjunction with the operations control it provides the capability for emulation of some disk controllers and drives normally supplied by popular minicomputer manufacturers.

Only a general description of the CPAs operation as it relates to the controller is provided in this section. For more comprehensive and detailed information refer to paragraph 5-3.

The CPA provides the adaptation required between the minicomputer I/O bus, DMA bus and the basic controller. The adapter contains interface circuits to communicate with the minicomputer's I/O bus and DMA Channel as well as interfaces to the basic controller's microprocessor bus and data bus via the Computer Interface CCA.

The primary means of communicating between the I/O bus and microprocessor bus is provided through a register file accessible by both the minicomputer and microprocessor. The minicomputer loads control and addressing parameters into the register file, reads status conditions and registers from the file. The microprocessor can read or write any location in the file, and extracts the control and addressing parameters to initiate disk operations, posts status conditions for the drive and controller into the file, as well as updating registers which contain DMA word counts and memory addresses.

Logic is provided to control the data transfer between the controllers data bus and the minicomputer's DMA bus. DMA addresses are supplied by the CPA prior to each data word transfer. The address is incremented after each word transferred, provided the MAR increment inhibit is false. Once a data operation is started the controller's data bus becomes logically connected to one port adapter, and the microprocessor bus is free to perform control functions if required on other drives. Part of the adapter's function is to provide a CPU bus throttle control over DMA data bursts. The CPU bus is monitored, when applicable, for other devices requesting service and after the adapter completes a burst of 1 to 16 words (selectable) if other device requests exist, other than the adapters, the DMA bus will be released for access by the other device before making another request. If no other device requests the DMA bus, upon completion of the burst, the bus is not released by the adapter and another burst of up to 16 words is performed.

The adapter contains logic to request an interrupt and present an interrupt vector address to the minicomputer. All interrupt requests are initiated by the microprocessor. The interrupt logic may be enabled or disabled under program control.

Errors detected by the adapter such as transfer time-out, are communicated to the microprocessor via the adapter Error Flag Register. A logical "OR" of all adapter errors will also set a bit in the adapter Event Flag Register. Asynchronous events such as errors, System Reset, initiation of commands by the minicomputer, etc., set bits in the adapter Event Flag Register which also is read by the microprocessor. Error Flags and Event Flags are reset by the microprocessor.

The DMA address register is loaded by the microprocessor after obtaining the starting memory address from the register file. This register cannot be read directly by the minicomputer to avoid loss of interlock with the microprocessor. After termination of a data operation, the microprocessor reads the register to obtain the ending memory address and posts the address in the assigned register file location.

The register file is a high speed RAM with multiplexed access from the minicomputer I/O bus or microprocessor bus. On the microprocessor bus side, two 8-bit, byte addressable, holding registers are used to buffer data to and from the microprocessor, and a 6-bit address register is loaded from the microprocessor

with the desired register file address. The data holding, and address registers are assigned unique microprocessor memory addresses.

Each port adapter is addressed from the microprocessor by a 2-bit select register, and decoded to select port 0-3. To read a specific register file the microprocessor loads the address register with the requested address and the direction bit = 0. The file is then accessed and all 16 bits are read into the holding registers. The microprocessor can then read either byte. To write into the register file, the microprocessor first loads both byte holding registers and then loads the address register with the file address and the direction bit = 1. The register file is then accessed and the 16 bits in the holding registers are written into the file. If the minicomputer and microprocessor both attempt to access the register file simultaneously, the adapter resolves which goes first with tie-breaker logic and after one access is completed, it switches and services the second path. Each access is held to less than 100 ns, to avoid response delays. When 8-bit minicomputers are attached, the register file access by the microprocessor will accordingly be byte oriented.

2. Computer interface. One Computer Interface CPA is required for each CPA port. This CCA contains the line drivers and receivers required to maintain signal levels over the cables between the CPA and the controller. In addition, the computer interface contains the logic required to decode the Port Address. Each port is addressed from the microprocessor in operation control and the binary address 0-3 is decoded on the CI. Each CI is assigned a unique switch selectable address to provide a logical connection to the CPA port.

3. Operation control. The operation control section of the controller contains a microcomputer consisting of the following elements:

1. Microprocessor
2. Control Store PCB
3. Master Clock
4. Operator Control Panel

The microcomputer in Operation Control provides intelligent control and supervision of all operations initiated by the minicomputer via the CPU Port Adapter. In addition, the Operation Control is capable of executing many tasks transparent to the host minicomputer, such as automatic error correction, automatic retry of operations when errors are encountered, automatic disk formatting (option) , and self-diagnosis of controller functions through microdiagnostics.

The microcomputer controls the microprocessor bus which connects the Computer Port Adapter, Data Control, Disk Control, and Operator Panel. The microcomputer contains a single chip Motorola 6800 microprocessor, up to 8K bytes of PROM to contain the microprogram, up to 256 bytes of RAM scratchpad, and Microprocessor Clock. The microprocessor is capable of executing 72 instructions and addressing 65K bytes of storage. The Control Store PCB, consisting of the combination of PROM and RAM scratchpad occupy an assigned space in the microprocessor's addressing range. In addition, all registers in the Data Control and Disk Control are assigned specific address locations permitting them to be directly accessed by the microprocessor just the same as the Control Store PCB. The Computer Port Adapters are also assigned microprocessor addresses, but registers within them are accessed in a different manner as described under the Computer Port Adapter.

An important feature of the direct addressing of internal registers by the microprocessor is the capability to access the RAM data buffer contained in the Data Control. Data stored in this buffer by either the minicomputer or disk drive can be searched, compared, or altered (ECC) by the microprocessor.

The microcomputer polls the Computer Port Adapter(s) to determine when the register file has been loaded with command parameters by the minicomputer to initiate disk operations, check for asynchronous event requests, or check for errors detected in the adapter. The command function, control bits, logical drive address, cylinder address, head address, sector address, starting memory address, and word count are extracted from the file by the microprocessor. Disk address parameters are then mapped corresponding to the attached physical disk requirements depending upon the operational mode: Standard Emulation, Extended Emulation, or System Industries Standard.

Power fail detection by the controllers power supply causes a Non-maskable Interrupt to the microprocessor. This interrupt signal is to be generated from the power supply at least 5 milliseconds prior to DC voltages dropping to an unusable level. The microprocessor upon being interrupted will stop any data transfer operation in progress at the end of the current sector being processed, set a Power Low status bit in the Port Adapter, and generate an interrupt request to the host minicomputer. In the case of multiple CPU ports, all are notified of the impending power loss. If the power fail indication is from an attached disk drive, a data transfer operation in progress will only be terminated if it is on the drive giving the Power Low indication. Drive power loss is posted in the Port Adapters Drive Status Register for the indicating drive. If a Port Adapter receives a Power Low Control signal from the minicomputer, the microprocessor is notified by an Event Flag. However, no action is taken unless a data transfer is in progress on that port, and if so, the operation will be aborted at the end of the current sector being processed.

Initial power up causes the Power On Reset signal from the power supply to reset all registers in the Data Control and Disk Control, and resets the microprocessor, which then enters its intialization or start-up routine. The microprocessor initializes controller functions, clears Port Adapter register files, collects and posts drive status to all adapters, and generates Control Ready status in all adapters. A master clear from the minicomputer will set an Event Flag in the Port Adapter and clear the adapters control status register (except Control Ready which is set true). The microprocessor, upon detecting this master clear event flag request, clears the controller if no operations are in progress for other adapters. A programmed reset is handled in a similar manner, except Controller Ready will be set by the microprocessor upon execution of the requested reset. Both resets generate an interrupt request to the microprocessor.

When the microprocessor is interrupted by the controllers power fail indication, a timer is started and if timeout occurs it assumes the power loss was a false or transient indication and enters its restart routine. However, since the Computer Port Adapters have already been flagged and any data operation in progress terminated, the restart is to start polling adapters for a new command from a minicomputer.

a) Microprocessor. The microprocessor used in Operation Control is a bidirectional, bus oriented 8-bit parallel processor, with 16 bits of address. The microprocessor is driven at a basic clock cycle rate of 1 MHz. Instruction execution time ranges from 2 to 12 clock cycles (2 to 12 microseconds). The microprocessor has a set of 72 different instructions and 7 different addressing modes. For additional information refer to the Motorola M6800 Microprocessor System Design Data Manual.

b) Master Clock. The Master Clock, a Motorola MC6875 Clock Generator/Driver, is used to supply the non-overlapping 01 and 02 clocks required by the microprocessor. A 4 MHz crystal is used for frequency determination. The MC6875 also supplies a 2×F and 4×F clock which are two and four times the MPU clock rate and is used as system sync signals. The 01 clock is used internally by the MPU and data transfers to/from the microprocessor are during the 02 time. Clock frequency is at a 1 MHz rate. (One microsecond cycle time.)

c) Operator Control Panel. Definition of the controls and indicators located on the Operator Control Panel is contained in Chapter 3.

d) Control Store. The Control Store CCA has 8K bytes of PROM memory. This PROM memory contains the resident microcode (firmware) required for operation of the controller hardware and the emulation of a specific manufacturers disk system. In addition, a 256 bytes RAM scratchpad memory is provided with the capability of adding 256 bytes as an option.

Both the PROM and RAM memory occupy an assigned space in the microprocessor's addressing range. The microprocessor bus interfaces the Data Control and Disk Control via this CCA.

4. Data Control. Data Control handles the DMA communication path between the Computer Port Adapter and Disk Control.

b. Block Address Assignments. Each functional element, ie., Control Store, Scratchpad Memory, Data Control, Disk Control, CPA, Operator Control Panel, Data Buffer, and Controller Test Unit are assigned a block of unique addresses. These address assignments allow the microprocessor direct access to each functional element, and to the registers within these elements. These Block Address assignments are shown in Table 5-7. Register Address assignments are covered in the section on the Data and Disk Control. Table 5-6 provides a Memory Map of the block addresses for addressing a specific functional element.

c. Interface Description. The Controller has several defined interfaces which are used to communicate between functional elements. For descriptive purposes, those interfaces which provide a communication path between external units or elements and the basic controller, will be referred to as External Interfaces; and those which provide logical signal flow between internal elements of the basic controller will be referred to as Internal Interfaces. External interfaces require line drivers and receivers, which are not required for the internal interfaces.

The External Interface to the PDP-11 minicomputer is provided by the Computer Port Adapter. The External Interface for the disk drive is provided by the Disk Interface Port. Internal interfaces between functional elements require no line drivers and receivers, however buffers are provided between the microprocessor in Operation Control and the Data Control and Disk Control logical elements. The interface to the microprocessor is referred to as the Microprocessor Bus, which includes address, data and control signals. The Microprocessor Bus Interface to the Computer Interface, Data Control, Disk Control, Operator Panel and Controller Test Unit utilize the following common signals, with address bits varying with the specific interface.

MP Data Bus 0-7
MP Address Bus 0-15
MP Valid Memory Address
MP Read/Write
MP Clock 02

Table 5-6. Memory Map

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
WT_2	32K	16K	8K	4K	2K	1K	512	256	128	64	32	16	8	4	2	1	Octal Addresses	Function
	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	000000-000777	Scratchpad
	0	0	0	0	0	1	-	-	-	-	-	-	-	0	X	X	002000-002003	CPA Ports 0-3
	0	0	0	0	0	1	-	-	-	-	-	-	-	1	X	X	002004-002007	OP/Control Panel
	0	0	0	0	1	-	-	-	-	0	X	X	X	X	X	X	004000-004077	Data Control
	0	0	0	0	1	-	-	-	-	1	X	X	X	X	X	X	004100-004177	Disk Control
	0	0	0	1	-	X	X	X	X	X	X	X	X	X	X	0	010000-013776	Data Buffer Hi
	0	0	-	1	-	X	X	X	X	X	X	X	X	X	X	1	010001-013777	Data Buffer Lo
	1	1	1	0	0	0	0	X	X	X	X	X	X	X	X	X	160000-160777	Ex Control Store 0
	1	1	1	0	0	0	1	X	X	X	X	X	X	X	X	X	161000-161777	Ex Control Store 1
	1	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	162000-162777	Ex Control Store 1
	1	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	163000-163777	Ex Control Store 3
	1	1	1	0	1	0	0	X	X	X	X	X	X	X	X	X	164000-164777	Ex Control Store 4
	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	165000-165777	Ex Control Store 5
	1	1	1	0	1	1	0	X	X	X	X	X	X	X	X	X	166000-166777	Ex Control Store 6
	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	167000-167777	Ex Control Store 7
	1	1	1	1	0	0	0	X	X	X	X	X	X	X	X	X	170000-170777	Control Store 0
	1	1	1	1	0	0	1	X	X	X	X	X	X	X	X	X	171000-171777	Control Store 1
	1	1	1	1	0	1	0	X	X	X	X	X	X	X	X	X	172000-172777	Control Store 2
	1	1	1	1	0	1	1	X	X	X	X	X	X	X	X	X	173000-173777	Control Store 3
	1	1	1	1	1	0	0	X	X	X	X	X	X	X	X	X	174000-174777	Control Store 4
	1	1	1	1	1	0	1	X	X	X	X	X	X	X	X	X	175000-175777	Control Store 5
	1	1	1	1	1	1	0	X	X	X	X	X	X	X	X	X	176000-176777	Control Store 6
	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	177000-177777	Control Store 7

X = 1 or 0
- = Don't Care
0 = Must be Zero
1 = Must be One

Table 5-7. Block Address Assignments

Functional Element	Block Address$_{10}$	Byte Capacity
Scratch Pad 0	0000 to 255	256
Scratch Pad 1 (Optional)	0256 to 0511	256
CPU Port 0-3	1024 to 1027	4
OP/Control Panel	1028 to 1031	4
Data Control	2048 to 2079	32
Disk Control	2080 to 2111	32
Data Buffer	4096 to 6143	1K
Ex Control Store	57,344 to 61,439	4K
Control Store 0-7	61,440 to 65,535	4K

Table 5-8. Microprocessor Interface Bus Signals

MP Data Bus 0-7 - is an 8-bit bidirectional bus used to transfer data between the Microprocessor and Control Store, Computer Port Adapter, Data Control, Disk Control and Maintenance Panel.

MP Address Bus 0-15 - is a unidirectional address bus from the microprocessor used to address assigned locations for Control Store, and registers throughout the controller. All address bits are not required by each functional element, therefore only those needed are routed to each for decoding.

MP Valid Memory Address - is an output signal from the microprocessor indicating when there is a valid address on the MP Address Bus.

MP Read/Write - is an output signal from the microprocessor to indicate whether the microprocessor is in a read or write state. A reset initializes it to read state. The Control Store and registers use this signal to enable data from the MP Data Bus to be loaded or the contents read to be placed on the bus.

MP Clock 01,02 - is the two phase, 1 MHz clock. MP Clock 02 is used by the scratchpad, PROM, and controller registers to determine when data on the Data Bus to/from the microprocessor is valid. Data is strobed on the trailing edge of 02. Clock 01 is used only by the microprocessor for timing. Clock 02 is 500 ± 50 ns in width.

MP Interrupt Request - is used to request an interrupt sequence be generated. The microprocessor waits until it completes the current instruction before recognizing the interrupt. If not masked, the Index Register, Program Counter, Accumulators, and Condition Code Register are all stored on the stack. The microprocessor then is pointed to a vector address in locations FFF8 and FFF9.

MP Non-maskable Interrupt - is an interrupt request also but is non-maskable. The microprocessor is pointed to a vector address in locations FFFC and FFFD. The AC low signal from the controller's power supply is connected, through a buffer circuit, to NMI.

MP Data Bus Enable - is an input signal to the microprocessor, connected to Clock 02 to enable the bus drivers during a write. During a read the bus drivers are disabled internally by the microprocessor.

MP Halt - is an input signal to the microprocessor used to halt all activity at the end of an instruction. The halt signal must not occur during the last half of Clock 01. This signal will be used by the Controller Test Unit to perform single instruction operation. During single OP, the halt signal must go false for at least one clock cycle.

MP Reset - is an input signal used to reset and start the microprocessor. The line is connected, through a buffer circuit, to the controller's power supply Power On Reset Signal. When the signal goes false, all high order address lines are forced high and the last two memory locations, FFFE and FFFF are used for the restart or initial start-up.

MP Bus Available - Not used.

MP Three-state Control - Not used.

1. External Interface. The External Interface to the Computer Port Adapter is via the Computer Interface CCA. This CCA contains the CPA Port Select logic and the line drivers and receivers which control the signal lines to and from the CPA. Each computer interface CCA contains two defined external interfaces. The two interfaces are described below and shown in Figure 5-13.

a) Computer Port Adapter - Operation Control. This interface to each CPA is used for programmed I/O communication between the microprocessor bus in Operation Control and the CPA. Each CPA is radially connected to the controller via the Computer Interface CCA. All signals are ground true.

b) Computer Port Adapter - Data Control. This interface to each CPA provides the means to perform DMA type data transfers between Data Control and the selected CPA. Once the logical connection to the CPA is established the control path to the microprocessor bus from other CPAs is free for use. The CPA data bus runs autonomously during block transfers. The width of the data bus is 16 bits allowing for 8, 12, or 16 bit parallel data transfers. All signals are ground true.

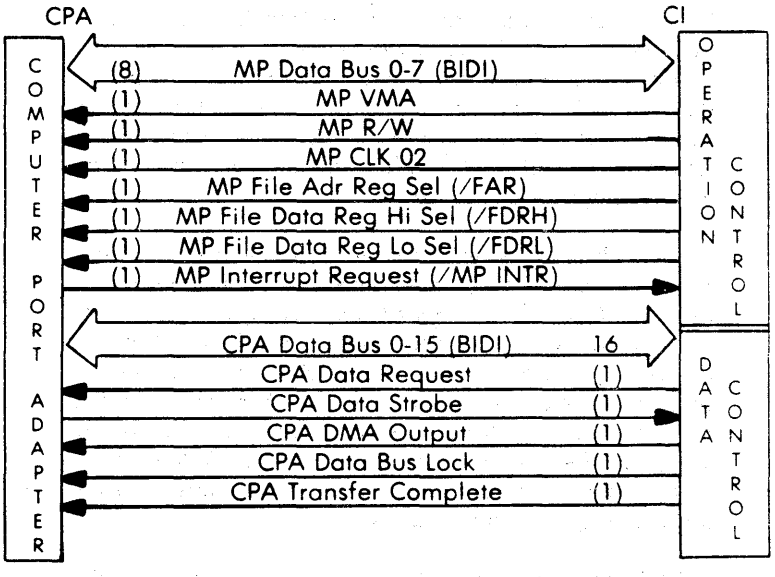


Figure 5-13. CPA Computer Interface

Table 5-9. CPA Computer Interface Signal Definition

MP Data Bus 0-7 - used by the microprocessor to transfer control information to/from the Computer Port Adapter.

File Address Register Select - used to select the FAR in the selected CPA.

File Data Register Hi Select - used to select FDR Hi in the selected CPA.

File Data Register Lo Select - used to select FDR Lo in the selected CPA.

MP Valid Memory Address - used by each CPA to qualify the register select signals.

MP Read/Write - used by each CPA to determine the direction of data transmission between the microprocessor and the File Address Register or File Data Register.

MP Clock 02 - used by each CPA to strobe data into the addressed register at the trailing edge of 02. During microprocessor read, the register selected is gated onto the data bus at the leading edge of VMA and remains valid throughout VMA. The data bus is to be guaranteed valid for 100 ns prior to the trailing edge of 02 during read to ensure the microprocessor adequate data set-up time.

MP Interrupt Request - used by the CPA to interrupt the microprocessor when power fail is detected in the minicomputer; if indication available and when a System Master Clear or Programmed Reset is detected.

CPA Data Bus 0-15 - 16-bit bidirectional bus used to transfer data words to the Data Control during write operations. When an 8 or 12 bit minicomputer is interfaced, the word is justified to the low order bits, with bit 0 the LSD and bit 15 the MSD.

Data Request - is a signal from the Data Control which is activated for each word requested during writes, or when the Data Control has a word ready to transfer during reads. The signal remains true until the leading edge of Data Strobe is detected. Read Data on the bus will remain stable through Data Request and to the trailing edge of Data Strobe.

Data Strobe - is a signal from the selected CPA which is sent in response to Data Request to strobe a word into the Data Control during writes or acknowledge acceptance of a word on the bus during reads. Data on the bus during writes must be valid 100 ns prior to the rise of Data Strobe, and remain stable throughout to the trailing edge of Data Request. Data Strobe in the selected CPA may only be activated when Data Request is true and must fall within 100 ns after detecting the trailing edge of Data Request.

DMA Output - is a signal from the Data Control to the selected CPA to indicate whether data transfer is to the CPA or to the Data Control, and false indicates a read, or data is to the CPA. This signal is activated when the CPA becomes logically connected, and remains stable throughout the connection.

Data Bus Lock - is the signal from the Computer Interface to the CPA which establishes a logical connection or selection between the two for a data transfer operation. All CPAs are radially connected and DB Lock is activated based on the contents of the Port Address stored in the Data Control to only one of four adapters. This signal gates all line drivers and receivers. The two CPA Data Select lines, 1 and 2, are routed to the appropriate Computer Interface for decode. Selection is dependent upon the setting of address switches on each Computer Interface CCA.

Transfer Complete - is a signal generated when the word counter overflows indicating the last word has been transferred, or the CPU Enable Bit is false, or an error has been detected.

2. Internal Interface. The internal interfaces of the 9400 Controller are as follows.

a) Operation Control - Data Control. The internal interface between Data Control and the Microprocessor Bus in Operation Control provide a communication path for microprocessor control of data transfer operations. Registers in Data Control are assigned addresses directly accessible to the microprocessor including the DMA Data Buffer. Most registers may be read or written by the microprocessor, however, some are read only.

Data Control is assigned a block of addresses and decodes the address bus lines from the microprocessor to determine which register or buffer location is to be selected.

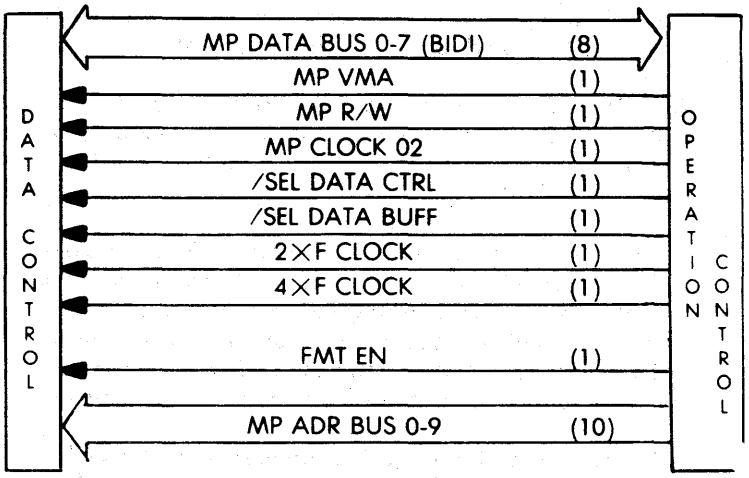


Figure 5-14. OP Control - Data Control Interface

Table 5-10. OP Control - Data Control Signal Definitions

MP Data Bus 0-7 - is an 8-bit bus to the Data Control from the Microprocessor Data Bus used to transfer control information to/from the address register.

MP Address Bus 0-9 - is decoded by the Data Control to determine which specific register or buffer location to read or write.

MP Valid Memory Address - used by the Data Control to qualify the address on the bus.

MP Read/Write - is used by the Data Control to determine if the addressed register is to be written into from the MP Data Bus or read onto the MP Data Bus.

MP Clock 02 - used by the Data Control to time register transfers to/from the microprocessor. Data on the bus is strobed into a register during write at the trailing edge of 02. During register reads, the contents are gated onto the bus by VMA and remain stable until the trailing edge of VMA, ensuring data set-up time during Clock 02.

2×F Clock - is a 2×F clock available for pulse generation and clocking; in sync with microprocessor.

4×F Clock - is a 4×F microprocessor clock.

/SEL DATA CTRL - signal generated by the decoded high order MP Address Bus to select the Data Control.

/SEL DATA BUFF - signal generated by the decoded high order MP Address Bus to select the Data Buffer in Data Control.

FMT EN - signal enabled by setting the Format Switch and used to over-ride the Write Protect flag in Data Control.

b) Data and Operation Control - Computer Interface. The Internal Interface from the Data Control and Operation Control to the Computer Interface provides the communication path for data transfers and control signals. These signals are defined in Table 5-10. This interface also has two additional signals which are defined below.

Signal Definitions:

CPA MP SEL 1 CPA MP SEL 2	Two lines used to select one physical port to the microprocessor. The binary address is stored in Operation Control and sent to each Computer Interface CCA. Switch settings on the Computer Interface CCA determine the address assignment. MP Data Bus bits 0 and 1 are used by the microprocessor to load the Binary Port Address.

c) Operation Control - Disk Control Interface. The internal interface between the Disk Control and the Microprocessor Bus in Operation Control provides a means for the microprocessor to control communication with the attached disk drives and establishes an interface to the ECC logic in Disk Control. All ECC registers may be read by the microprocessor but not written. Other registers in Disk Control may be written but not read.

The Disk Control is assigned addresses in the same block as Data Control with unique assignments for individual registers.

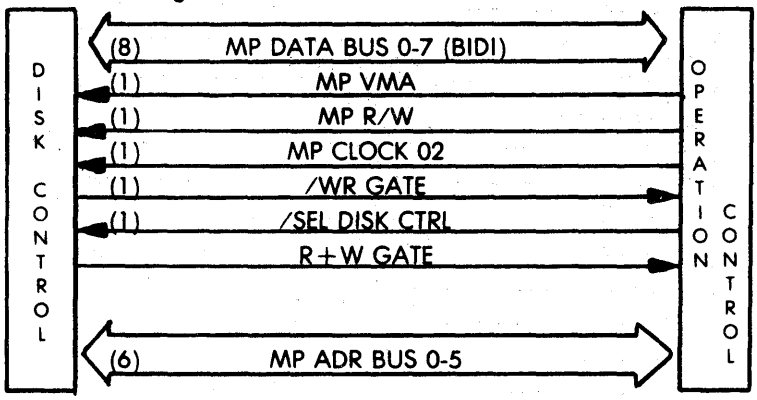


Figure 5-15. Operation Control - Disk Control

Table 5-11.
Operation Control - Disk Control Signal Definitions.

MP Data Bus 0-7 - is an 8-bit bus to the Disk Control from the microprocessor data bus used to transfer command, control, address, and status information.

MP Address Bus 0-5 - is decoded by the Disk Control to determine which register is to be read or written. The Disk Control addresses are in the same block assigned to the Data Control, but occupy the higher 64 addresses and require their own decode.

MP Valid Memory Address - used by the Disk Control to qualify the address bus.

MP Read/Write - is used by the Disk Control to determine if the addressed register is to be read or written.

MP Clock 02 - is used by the Disk Control and Disk Interface to time transfers to/from the microprocessor; similar to Data Control.

/Write Gate - signal to Operation Control that a write operation is in progress. Prevents the detection of a power fail condition until the current write operation is completed.

/SEL DISK CTRL - signal generated by the decoded high order MP Address Bus to select the Disk Control.

d). Data Control - Disk Control Interface. This internal interface is used to control the exchange of data between the data buffer in Data Control and the Serializer/Deserializer Shift Register in the Disk Control.

Errors detected by the Disk Control are sent to Data Control to be communicated to the microprocessor.

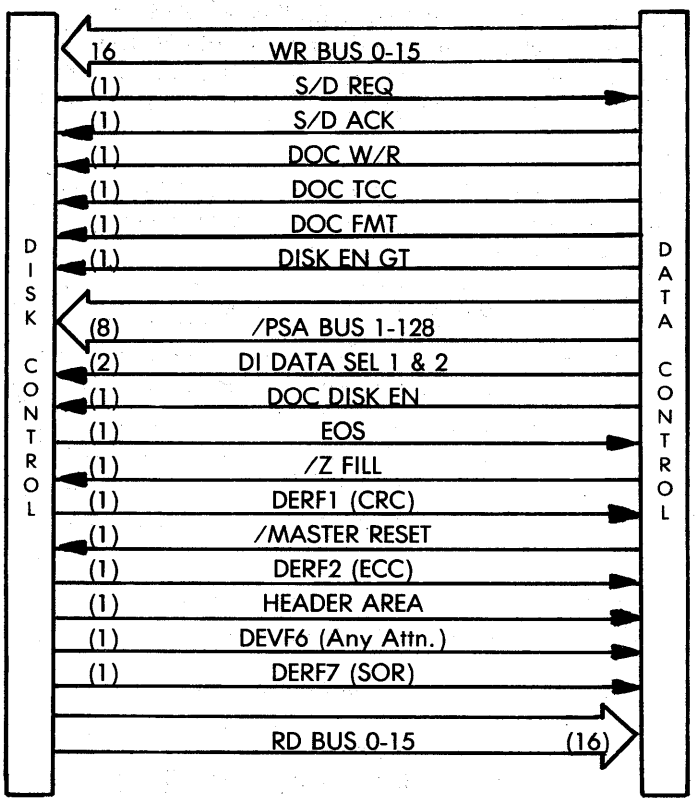


Figure 5-16. Data Control - Disk Control Interface

Table 5-12.
Data Control - Disk Control Interface Signal Definitions

Disk WR Bus 0-15 - is a 16-bit bus over which parallel write data is transferred from the data buffer to the S/D registers.

Disk RD Bus 0-15 - is a 16-bit bus over which parallel read data is transferred to the data buffer from the S/D shift registers. The RD Bus is also compared directly against the Address Verify Register by the Data Control during header address verification.

S/D Request - is a signal from the Disk Control to the Data Control generated when the S/D is ready to accept a word during writes or has a word available on the RD Bus during reads. Disk Enable and Sector Compare must be true in order to generate S/D REQ. The signal switches false during writes in response to S/D ACK to indicate loading of the word into the shift register. During reads S/D ACK indicates acceptance of the data word on the RD Bus and S/D REQ switches false within 100 ns of the leading edge of S/D ACK. S/D ACK then switches false within 100 ns of S/D REQ going false.

S/D Acknowledge - is a signal from the Data Control to the Disk Control generated to transfer a word on the WR Bus during writes or accept the word on RD Bus during reads. The signal is interlocked with S/D Ready as described above.

Physical Sector Address 1-128 - eight lines which contain the physical sector address stored in the Data Control to be compared against the drive's sector counter by the Disk Control.

Header Area - is a signal to the Data Control from the format controls in the Disk Control indicating when the header field is being read or written. The signal rises after the sync byte preceding the header and falls when the last byte of header information is read or written; prior to header CRC.

DOC FMT - this signal from the OP Reg in the Data Control indicates when a disk format operation is to be performed. It is used in conjunction with R/W mode to let the Disk Control know when to write the sector format, i.e., gap, sync, and header field starting from Sector Pulse. Format true during read does not alter the Disk Control function, but the data control will store the header field in the data buffer and not perform address verification.

DOC TCC - this signal is generated from the OP Reg in the Data Control during diagnostics to cause the Disk Control to request the CRC/ECC bytes from the data buffer and write them on the disk in lieu of the hardware generated code. During read, the CRC/ECC bytes read from the disk are transferred to the data buffer in addition to the header or data field.

DERF1 - indicates a CRC error was detected when the header or data field was read. The signal is sent to the Data Control to permit the microprocessor to detect it in the Error Flag Register.

DERF2 - indicates an ECC error was detected when the data field was read. The signal is sent to the Data Control for detection by the microprocessor in the Error Flag Register.

DI DATA SEL 1 & 2 - these two lines contain the binary address of the Drive Interface Port to select during data transfers.

DOC W/R - indicates whether data is to be read or written. The signal is generated from a bit in the OP Reg of the Data Control which is loaded by the microprocessor. R/W mode true indicates write, and false indicates read. Disk Enable must be true for R/W mode to be significant.

Disk EN GT - is a signal generated in the Data Control from a bit in the OP Register set by the microprocessor. The signal must be true to enable transfers to or from the Disk Control and disk drive. Disk Enable to the Disk Control is gated in the Data Control by buffer conditions which indicate buffer space is available during reads or when a buffer block is full during writes.

DOC Disk EN - is OP Register, bit 5. If the bit is false, errors detected in the Disk Control are reset. Enables R/W operations to be performed between Data and Disk Control.

EOS' - is a signal from the Disk Control which indicates the format control is at the end of the data fields CRC/ECC during read, or at the end of the guard gap written after the CRC/ECC during write.

/Zero Fill - in a signal from Data Control to Disk Control used to cause the sector to be written with zeros from sector the last Data Word transferred to the CRC/ECC bytes. The signal switches true upon detection of Buffer Empty at the trailing edge of SD ACK. The word loaded into the Serializer by SD ACK is the last Data Word transferred and written in that sector. The Disk Control inhibits any further SD requests and fills the remainder of the data field with zeros.

DEVF6 - the Any Attention Flag which is generated by a drive on the Disk Interface Port.

/MASTER RESET - is an "OR" of power on Reset from activation of the Restart Switch. Signal used to reset selected registers in the Disk Control.

DERF7 - indicates a Sector Overrun error. The signal is sent to the Data Control to permit the microprocessor to detect it in the Error Flag Register.

e) Disk Control - Drive Interface Port. This internal interface provides a standardized interface between the Disk Control and Drive Interface Ports. Up to four Drive Interface Ports may be installed with the radial option, and all use this common interface in communication with the controller. The Driver Interface Port is tailored to provide specific drive types requirements for interfacing to the controller. However, each Drive Interface Port contains logic functions which are common irrespective of the drive attached and communication conventions over the internal interface are standardized. Only one port at a time is logically connected to the Disk Control for a data operation, but the microprocessor has access to all other ports during the transfer to execute control operations.

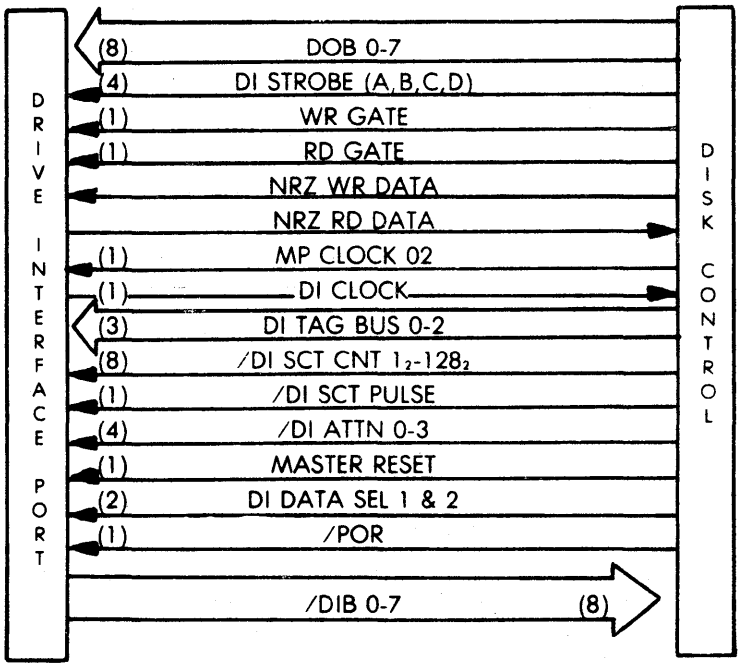


Figure 5-17. Disk Control - Drive Interface Port

Table 5-13.
Disk Control - Drive Interface Port Signal Definitions

DI Output Bus 0-7 - is an 8-bit bus from the Disk Control to all ports over which the microprocessor transfers port, drive, cylinder, and head addresses, commands, or other control information from an Output Register to the Drive Interface Port. Only the port selected transmits the information to the attached disk drive.

DI Input Bus 0-7 - is an 8-bit bus from the Drive Interface Port over which the microprocessor reads selected drive status, drive model type, and drive error codes.

DI Tag Bus 0-2 - is a 3-bit bus which carries binary coded tag functions from the microprocessor to the selected DI Port which then decodes the tag bus and generates the appropriate signal to the disk drive. The DI Tag Bus defines the type of information on the DI Input Bus. TAG2 is used with the CDC Drives to generate Control Select (CDC TAG3) to the drive, with the DI Output Bus defining functions to the drive.

/DI SCT CNT 1-128 - these eight lines contain the contents of the selected port/drive sector counter which is sent to the Disk Control for comparison with the Physical Sector Address. When all eight bits are not used, the high order binary weighted bits unused are always zero (false). The Sector Count resets to zero at Index and advances on the leading edge of Sector Pulse.

/DI SCT PULSE - is generated by the selected port and drive and is transmitted to the Disk Control for use in sector read/write start-up. Sector Pulse is used in the DI Port to step the Sector Counter on CDC interfaces.

/DI ATTN 0-3 - is one line from each Drive Interface Port installed, 0-3, which is sent to the Disk Control to permit the microprocessor to read the Attentions from the DI Flag Register. The attention is generated by the attached disk drive(s) on a DI Port and stored in the port until drive status for that port is read by the microprocessor.

DI Strobe (A,B,C,D) - is a pulse to the selected port used to generate a tag or strobe to the attached disk drive. The corresponding strobe is generated once each time the Control Register in the Disk Control is loaded with bits 3, 4, 5, or 6 = 1. Pulse width is dependent upon the clock frequency.

DI Write Gate - is generated by the Disk Control to the selected port and disk drive to control the period data is to be written on the disk. Data Select must be true to send Write Gate to the disk drive.

DI Read Gate - is generated by the Disk Control to the selected port and disk drive to control the period data is read from a disk sector. Data Select must be true to send Read Gate to the disk drive.

DI NRZ Write Data - is the serial data line to the selected port and drive used to transmit data during Write Gate active from the Disk Control. When NRZ Write Data is

true (high), "ones" are written, and when it is false (low), "zeros" are written. This signal changes state on the trailing edge of the clock supplied by the selected drive.

DI NRZ Read Data - is the serial data line from the selected port and drive over which data is read to the Disk Control during Read Gate active. When NRZ Read Data is true (high), "ones" are read, and when it is false (low), "zeros" are read. The signal changes state on the trailing edge of the clock supplied by the selected drive, and is to be strobed into the S/D Shift Register on the leading edge of the clock.

MP Clock 0-2 - is used in the Drive Interface Port to time the Attention Flip-Flop reset, etc.

DI Clock - this signal is generated by the selected disk drive and transmitted to the Disk Control from the selected DI Port for use in clocking read/write serial data. The clock frequency is dependent upon the drive attached, however, logic in the Disk Control is designed to handle rates up to 12 MHz.

Master Reset - is an "OR" of Power On Reset from activation of the Restart Switch. Master Reset sets the Port Attention Flip-Flop in the Drive Port and resets all others.

DI Data Select 1 & 2 - these two lines are used to maintain selection of one of four Drive Interface Ports during a data operation. The DS is generated from the Drive Port Address stored in the Port Register of the Data Control. Only the Drive Interface Port with its associated DS active is logically connected at the time the microprocessor sets Disk Enable. That DI Port remains connected to the Data Control and Disk Control for Data OPS until a different port address is loaded into the Port Register by the microprocessor. DS provides a gating function in the DI Port for Write Gate, Read Gate, NRZ Write Data, NRZ Read Data. R/W Clock, Sector Counter, and Sector Pulse to/from the Disk Control and DI Port.

/POR - is a signal generated by the power supply when the DC voltage drops to less than 4.75 volts. The POR signal will be used to inhibit the CDC Drive Interface (Open Cable Detect).

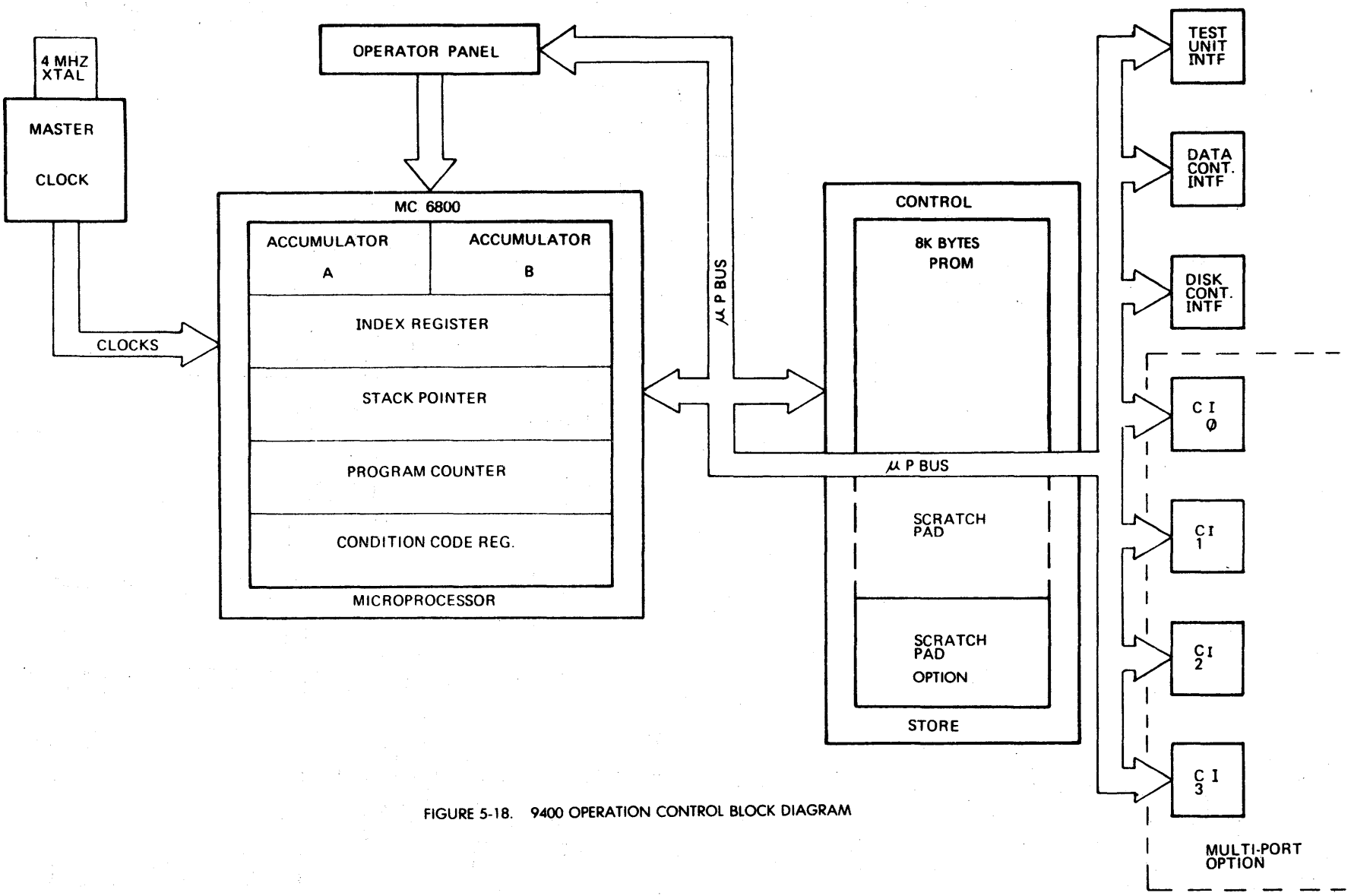


FIGURE 5-18. 9400 OPERATION CONTROL BLOCK DIAGRAM

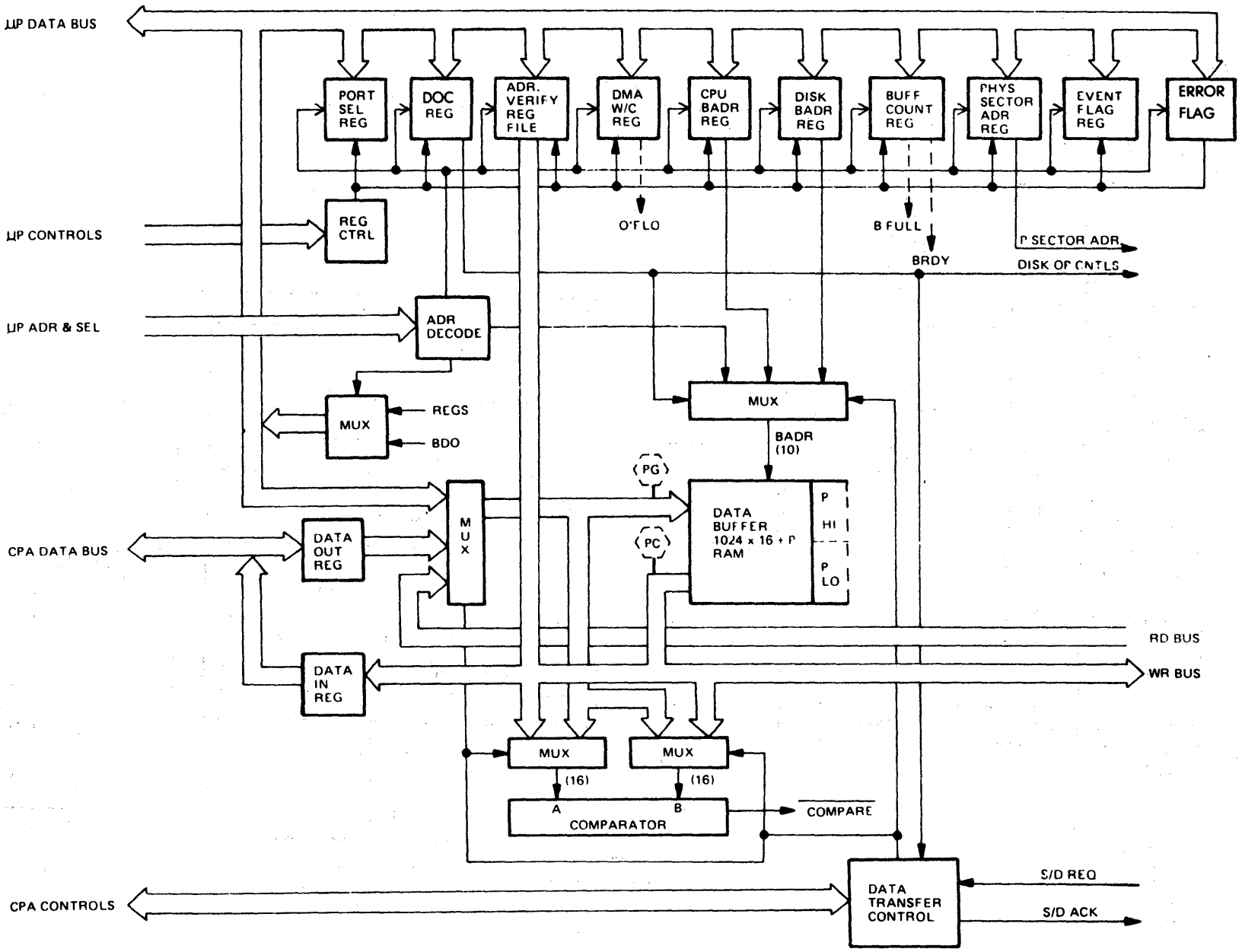


FIGURE 5-19. 9400 DATA CONTROL BLOCK DIAGRAM

Data Control Registers.

1. Address Verify Cylinder Hi (AVCYLH)(004000).

15	14	13	12	11	10	09	08
-	-	-	-	-	C_{1024}	C_{512}	C_{256}

BIT	NAME	FUNCTION
15-11	Not Used	Not Used
10-08	C_{1024}-C_{256} R/W	High order cylinder bits used in address verification.

2. Address Verify Cylinder Lo (AVCYLL)(004001).

07	06	05	04	03	02	01	00
C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1

BIT	NAME	FUNCTION
07-00	C_{128}-C_1 R/W	Low order cylinder bits used in address verification

3. Address Verify Head (AV HD) (004002).

15	14	13	12	11	10	09	08
H_{128}	H_{64}	H_{32}	H_{16}	H_8	H_4	H_2	H_1

BIT	NAME	FUNCTION
15-08	H_{128}-H_1 R/W	Head Address bits used in address verification.

4. Address Verify Logical Sector (AV LS) (004003).

07	06	05	04	03	02	01	00
S_{128}	S_{64}	S_{32}	S_{16}	S_8	S_4	S_2	S_1

BIT	NAME	FUNCTION
07-00	S_{128}-S_1 R/W	Sector address bits used in address verification

5. Flag Byte (004010).

15	14	13	12	11	10	09	08

BIT	NAME	FUNCTION
15-08	R/W	User Definable

6. User Byte (004011).

07	06	05	04	03	02	01	00

BIT	NAME	FUNCTION
07-00	R/W	User Definable

7. Keyword #1 (4004-4005)

HI								LO							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

8. Keyword #2 (4006-4007)

HI								LO							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Keyword information is User Defined.

9. DMA Word Count Hi (DMAWCH) (004020).

15	14	13	12	11	10	09	08
W_{32K}	W_{16K}	W_{8K}	W_{4K}	W_{2K}	W_{1K}	W_{512}	W_{256}

BIT	NAME	FUNCTION
15-08	W_{32K}-W_{256} R/W	Two's complement of high order word count bits used for CPU data transfers. Hardware incremented following each word transfer to or from memory.

10. DMA Word Count Lo (DMAWCL) (004021).

07	06	05	04	03	02	01	00
W_{128}	W_{64}	W_{32}	W_{16}	W_{8}	W_{4}	W_{2}	W_{1}

BIT	NAME	FUNCTION
07-00	W_{128}-W_{1} R/W	Two's complement of low order word count bits used for CPU data transfers. Hardware incremented following each word transfer to or from memory.

11. Disk Buffer Address Hi (DBARH) (004022).

15	14	13	12	11	10	09	08
-	-	-	-	-	-	A_{512}	A_{256}

BIT	NAME	FUNCTION
15-10	Not Used	Not Used
09-08	A_{512}-A_{256} R/W	High order address bits used by the Storage Module Drive to access the next block or buffer of the data buffer. Initialized by the microprocessor and each carry from DBAR Lo will increment DBAR Hi.

12. Disk Buffer Address Lo (DBARL) (004023).

07	06	05	04	03	02	01	00
A_{128}	A_{64}	A_{32}	A_{16}	A_8	A_4	A_2	A_1

BIT	NAME	FUNCTION
07-00	A_{128}-A_1R/W	Low order address bits used by the Storage Module Drive to access the data buffer during reads or writes. Initialized by the microprocessor and incremented +1 by each disk request.

13. Computer Buffer Address Hi (CBARH) (004024).

15	14	13	12	11	10	09	08
-	-	-	-	-	-	A_{512}	A_{256}

BIT	NAME	FUNCTION
15-10	Not Used	Not Used
09-08	A_{512}-A_{256} R/W	High order address bits used by the CPU Port to access the next block or buffer of the data buffer. Initialized by the microprocessor, and each carry from CBARL increments CBARH.

14. Computer Buffer Address Lo (CBARL) (004025).

07	06	05	04	03	02	01	00
A_{128}	A_{64}	A_{32}	A_{16}	A_8	A_4	A_2	A_1

BIT	NAME	FUNCTION
07-00	A_{128}-A_1 R/W	Low order address bits used by the CPU Port to access the data buffer during reads or writes. Initialized by the microprocessor and incremented +1 by each CPU DMA request.

15. Buffer Counter Hi (DBCH) (004026).

15	14	13	12	11	10	09	08
-	-	-	-	-	B_{1K}	B_{512}	B_{256}

BIT	NAME	FUNCTION
15-11	Not Used	Not Used
10-08	B_{1K}-B_{256} R/W	High order bits of the difference count between words transferred in and out of the Data Buffer by the CPU and the SMD. A signal (Buffer Ready) is generated to indicate that at least one buffer is ready to transfer. If the counter overflows, the Buffer Full flip-flop sets to make the SMD wait during reads, or the CPU wait during writes.

16. Buffer Counter Lo (DBCL) (004027).

07	06	05	04	03	02	01	00
B_{128}	B_{64}	B_{32}	B_{16}	B_8	B_4	B_2	B_1

BIT	NAME	FUNCTION
07-00	B_{128}-B_1 R/W	Low order bit of the difference count between words transferred in and out of the Data Buffer by the CPU and the SMD.

17. Data Event Flags (DEVF) (004030).

07	06	05	04	03	02	01	00
AE	AA	BA	BR	BE	TC	ES	EH

BIT	NAME	FUNCTION
07	AE (Any Error) Read Only	Set by hardware for an error condition.
06	AA (Any Attention) Read Only	Set by hardware for any attention condition.
05	BA (Buffer Available) Read Only	Set by hardware to indicate data buffer is available for data transfers.
04	BR (Buffer Ready) Read Only	Set by hardware to indicate data buffer is ready to transfer data.
03	BE (Buffer Empty) Read Only	Set by hardware to indicate all data in the buffer has been transferred.
02	TC (Transfer Complete) Read Only	Set at completion of data transfer. Reset when Word Counter is loaded.

17. Data Event Flags (DEVF) (004030). Continued

BIT	NAME	FUNCTION
01	ES (End of Sector) Read Only	Set by hardware. Reset when Physical Sector Address is loaded
00	EH (End of Header) Read Only	Set by hardware. Reset when Physical Sector Address is loaded.

18. Data Error Flags Hi (DERFH) (004031).

07	06	05	04	03	02	01	00
-	-	BBF	WPF	-	-	-	-

BIT	NAME	FUNCTION
07-06	Not Used	Not Used
05	BBF (Bad Block Flag) Read Only	Flag indicating error detected by hardware during data operation. Set by hardware when error occurs. Reset when microprocessor sets CPU Enable, Disk Enable False.
04	WPF (Write Protect Flag) Read Only	Flag indicating error detected by hardware during data operation. Set by hardware when error occurs. Reset when microprocessor sets CPU Enable, Disk Enable False.
03-00	Not Used	Not Used

19. Data Error Flags Lo (DERFL) (004032).

07	06	05	04	03	02	01	00
SO	BPH	BPL	DVE	AVE	ECE	CE	ESI

BIT	NAME	FUNCTION
07	SO (Sector Overrun)	Flag indicating error detected by hardware during data operation. Set by hardware when error occurs. Reset when microprocessor sets CPU Enable, Disk Enable False.
06	BPH (Buffer Parity Error Hi)	Same as bit 07.
05	BPL (Buffer Parity Error Lo)	Same as bit 07.
04	DVE (Data Verify Error)	Same as bit 07.
03	AVE (Address Verify Error)	Same as bit 07.
02	ECE (ECC Error)	Same as bit 07.
01	CE (CRC Error)	Same as bit 07.
00	ESI (Error Stop Inhibit)	Set by microprocessor

20. Data Port Address (DPA) (004033).

07	06	05	04	03	02	01	00
-	DP2	DP1	-	-	-	CP2	CP1

BIT	NAME	FUNCTION
07	Not Used	Not Used
06-05	DP2-DP1 (Drive Port) R/W	Binary coded Drive Interface Port 0-3, used to maintain selection of the Drive Interface Port during data transfer.
04-02	Not Used	Not Used
01-00	CP2-CP1 (Computer Port) R/W	Binary coded Computer Port 0-3, used to maintain selection of the Computer Port during data transfer.

21. Physical Sector Address (PS A) (004034).

07	06	05	04	03	02	01	00
SA_{128}	SA_{64}	SA_{32}	SA_{16}	SA_8	SA_4	SA_2	SA_1

BIT	NAME	FUNCTION
07-00	SA_{128}-SA_1 (Sector Address) R/W	Computed sector address used for comparison with rotational position counter of the Storage Module Drive.

22. Data Operation Control (DOC) (004035).

07	06	05	04	03	02	01	00
RBC	CE	DE	TCC	IDF	CD	F	R/W

BIT	NAME	FUNCTION
07	RBC (Reset Buffer Controls) R/W	When Set, resets the buffer controls.
06	CE (Computer Enable) R/W	When Set, enables the computer. If reset along with bit 05, enables the microprocessor to access the Data Buffer.
05	DE (Disk Enable) R/W	When Set, enables the Storage Module Drive. If reset along with bit 06, enables the microprocessor to access the Data
04	TCC (Transfer Check Code) R/W	
03	IDF (Inhibit Data Field) R/W	

22. Data Operation Control (DOC) (004035). Continued

BIT	NAME	FUNCTION
02	CD (Compare Data) R/W	
01	F (Format) R/W	
00	$\overline{R/W}$ (Read/Write) R/W	When Set, data operation is a write. When reset, data operation is a read.

23. Data Buffer Hi (DBH) (even addresses 010000 to 013776)

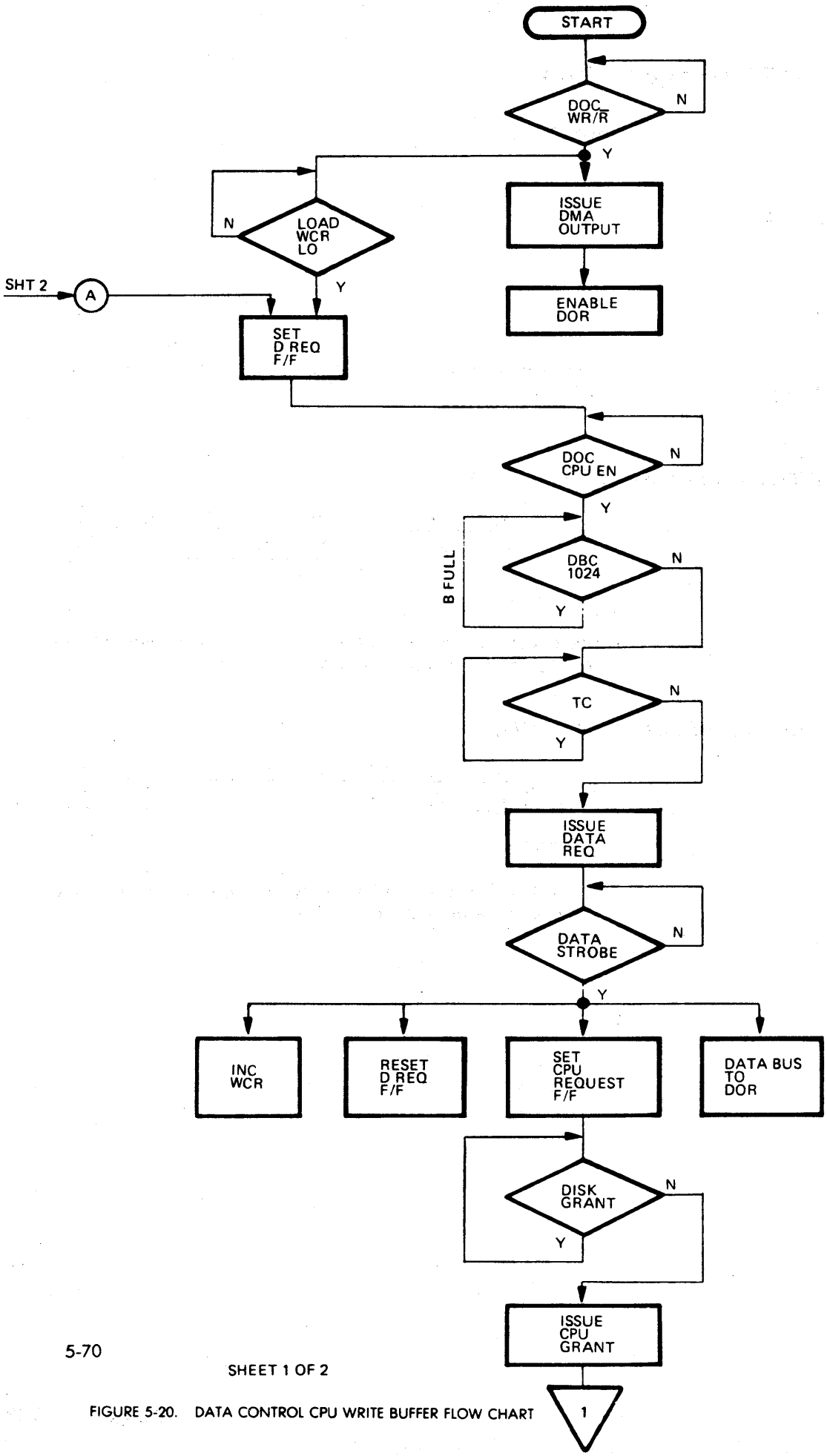
15	14	13	12	11	10	09	08
D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8

BIT	NAME	FUNCTION
15-08	D_{15}-D_8 R/W	Upper bytes of words to be transferred between memory and the Storage Module Drive (bits 08-15).

24. Data Buffer Lo (DBL) (odd address 010001 to 013777).

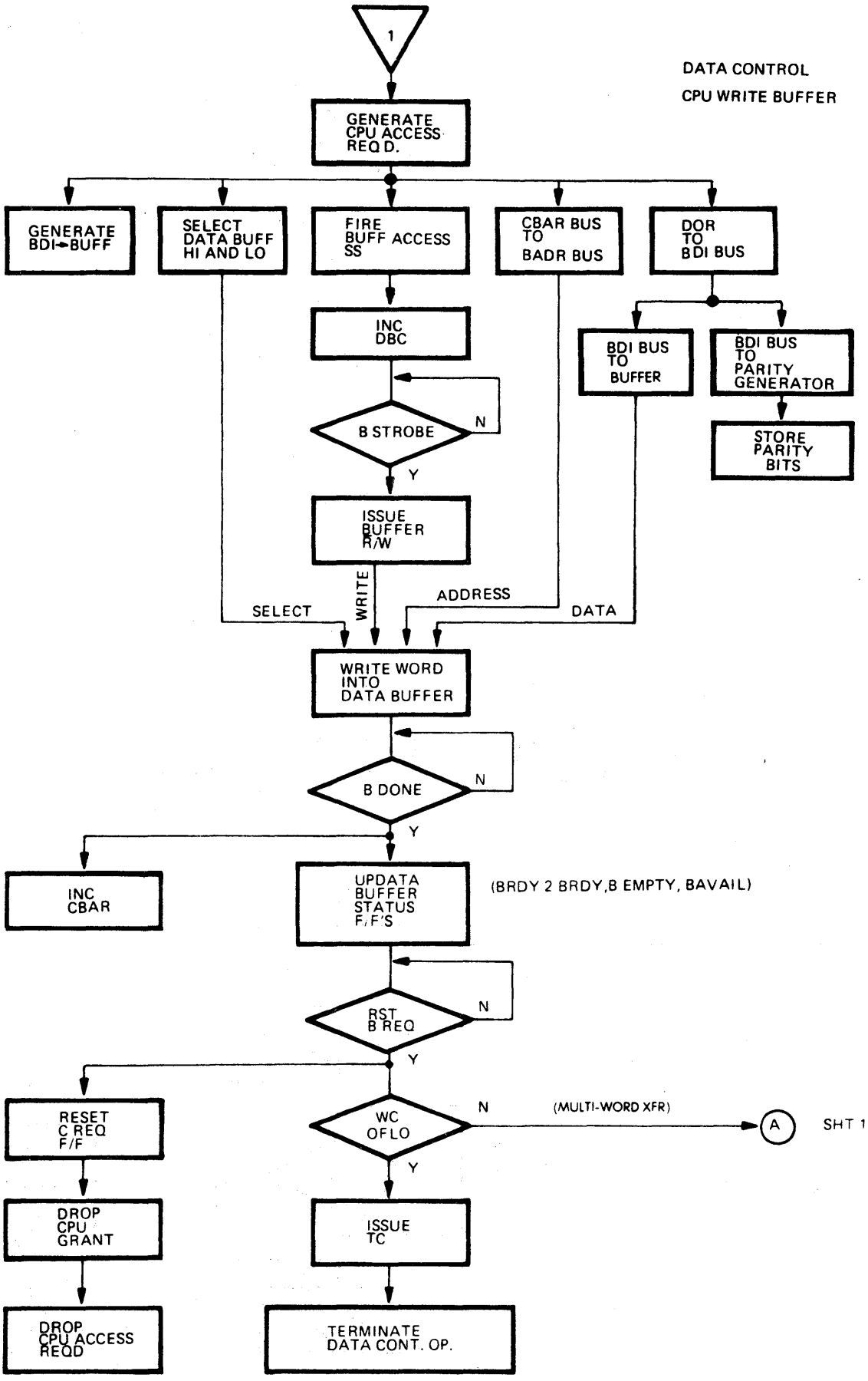
07	06	05	04	03	02	01	00
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

BIT	NAME	FUNCTION
07-00	D_7-D_0 R/W	Lower bytes of words to be transferred between memory and the Storage Module Drive (bits 07-00).



SHEET 1 OF 2

FIGURE 5-20. DATA CONTROL CPU WRITE BUFFER FLOW CHART


DATA CONTROL
CPU WRITE BUFFER
1
GENERATE CPU ACCESS REQ D.
GENERATE BDI→BUFF
SELECT DATA BUFF HI AND LO
FIRE BUFF ACCESS SS
CBAR BUS TO BADR BUS
DOR TO BDI BUS
INC DBC
BDI BUS TO BUFFER
BDI BUS TO PARITY GENERATOR
STORE PARITY BITS
B STROBE
N
Y
ISSUE BUFFER R/W
WRITE
SELECT
ADDRESS
DATA
WRITE WORD INTO DATA BUFFER
B DONE
N
Y
INC CBAR
UPDATA BUFFER STATUS F/F'S
(BRDY 2 BRDY,B EMPTY, BAVAIL)
RST B REQ
N
Y
RESET C REQ F/F
WC OFLO
N
(MULTI-WORD XFR)
A
SHT 1
Y
DROP CPU GRANT
ISSUE TC
DROP CPU ACCESS REQD
TERMINATE DATA CONT. OP.

SHEET 2 OF 2

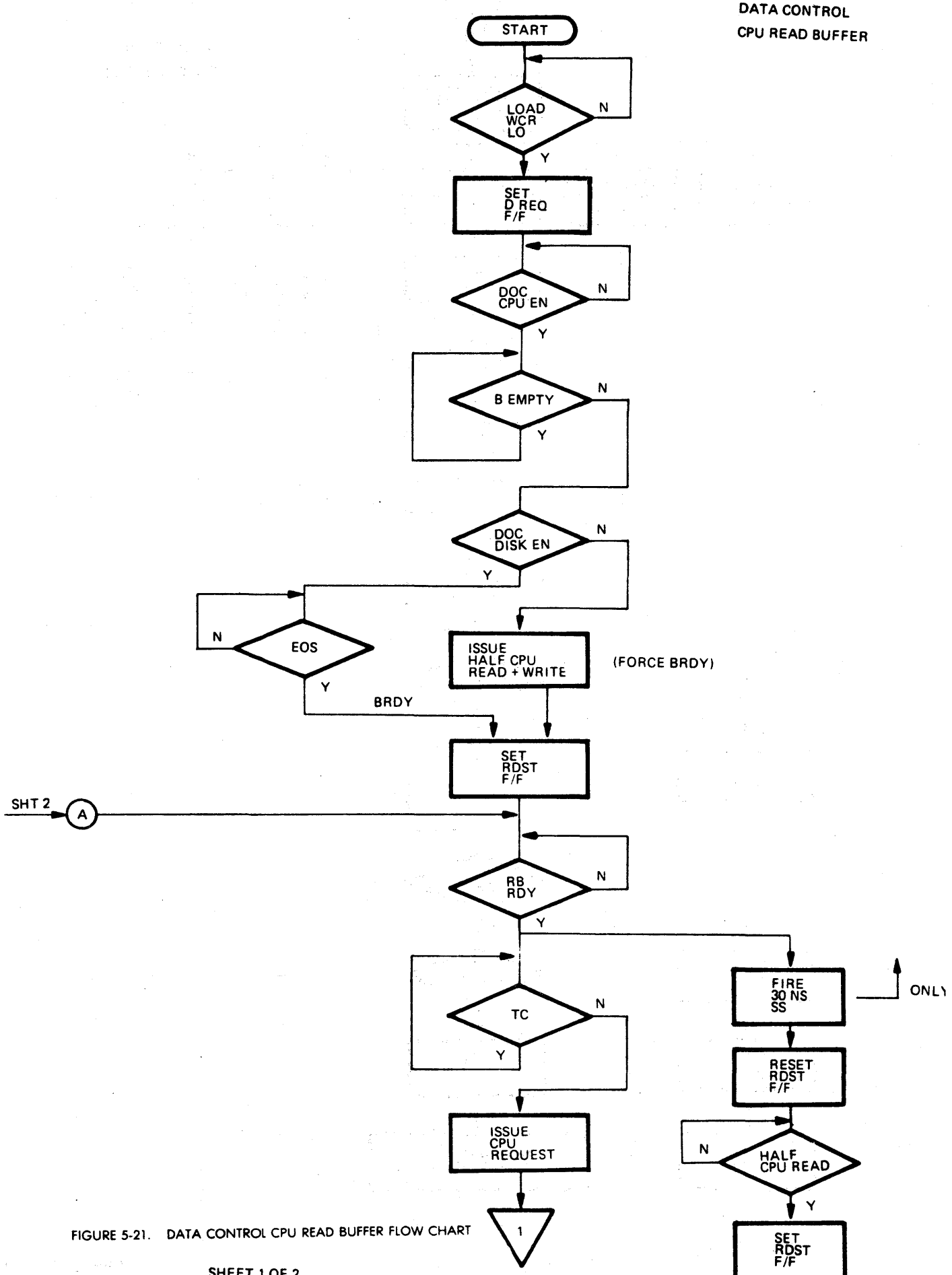
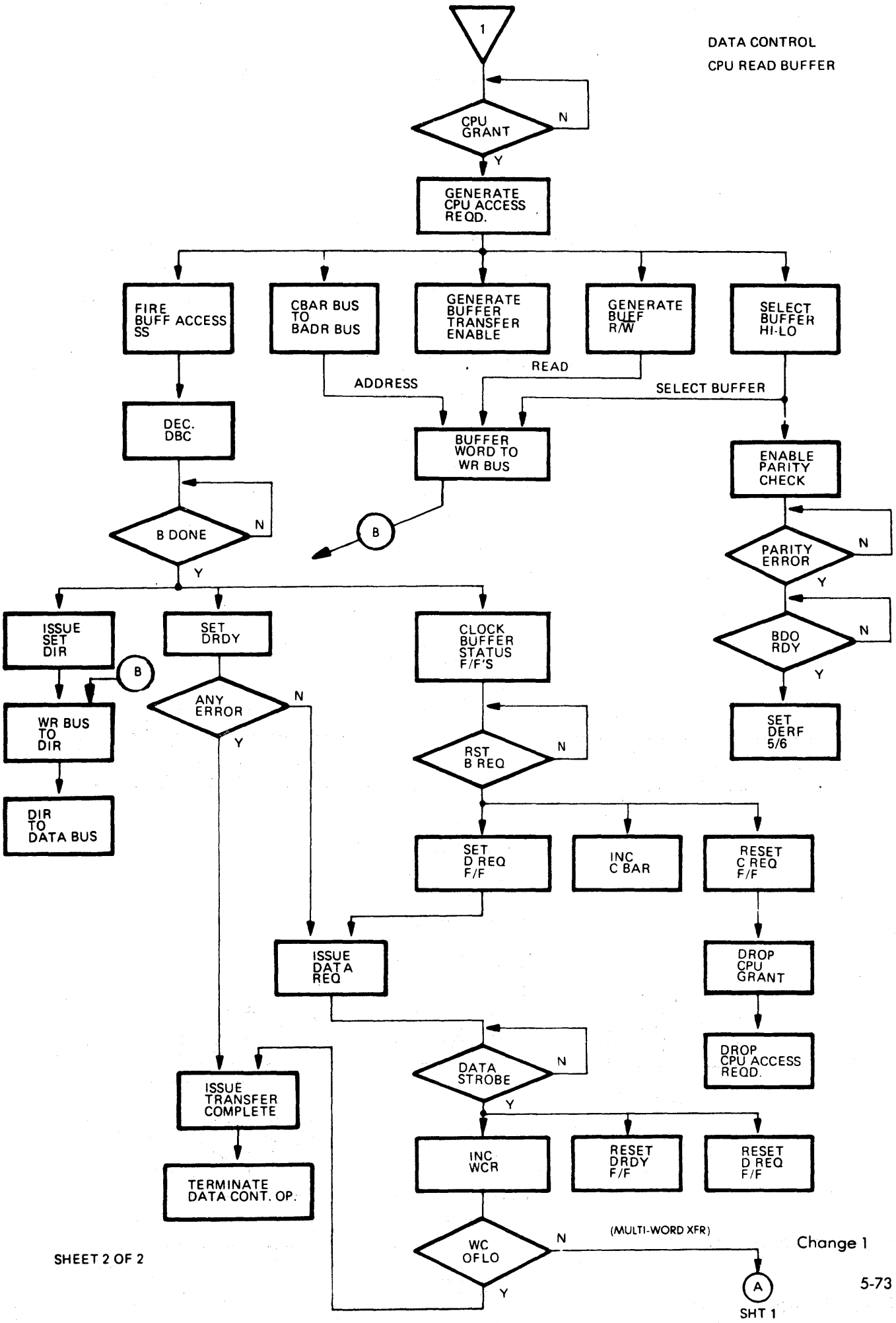


FIGURE 5-21. DATA CONTROL CPU READ BUFFER FLOW CHART

SHEET 1 OF 2


1
CPU GRANT
N
Y
GENERATE CPU ACCESS REQD.
FIRE BUFF ACCESS SS
CBAR BUS TO BADR BUS
GENERATE BUFFER TRANSFER ENABLE
GENERATE BUFF R/W
SELECT BUFFER HI-LO
READ
ADDRESS
SELECT BUFFER
DEC. DBC
BUFFER WORD TO WR BUS
ENABLE PARITY CHECK
B DONE
N
Y
B
PARITY ERROR
N
Y
BDO RDY
N
Y
ISSUE SET DIR
B
SET DRDY
CLOCK BUFFER STATUS F/F'S
WR BUS TO DIR
ANY ERROR
N
Y
SET DERF 5/6
DIR TO DATA BUS
RST B REQ
N
SET D REQ F/F
INC C BAR
RESET C REQ F/F
ISSUE DATA REQ
DROP CPU GRANT
DROP CPU ACCESS REQD.
DATA STROBE
N
Y
ISSUE TRANSFER COMPLETE
INC WCR
RESET DRDY F/F
RESET D REQ F/F
TERMINATE DATA CONT. OP.
WC OFLO
N
(MULTI-WORD XFR)
Y
A
SHT 1

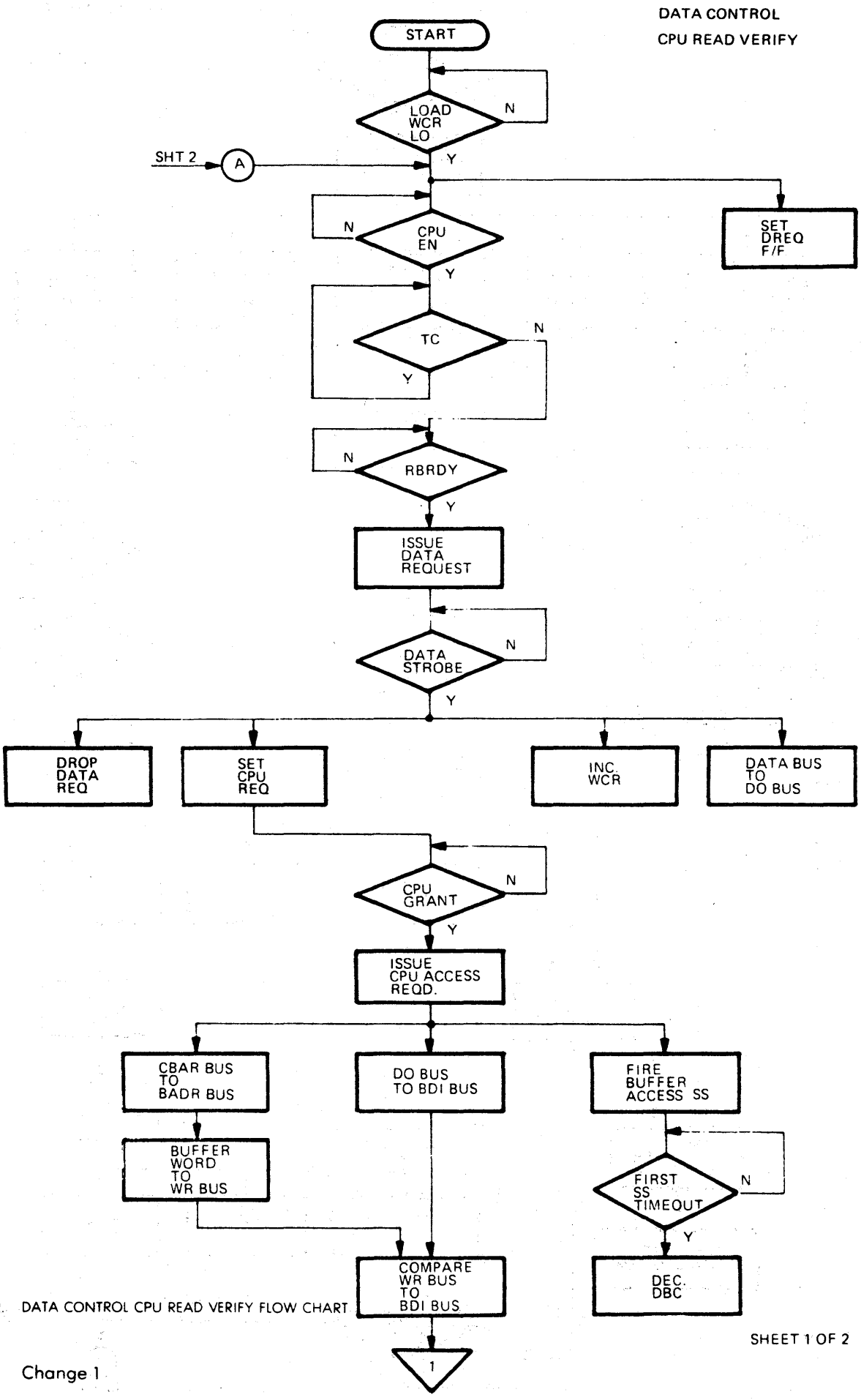
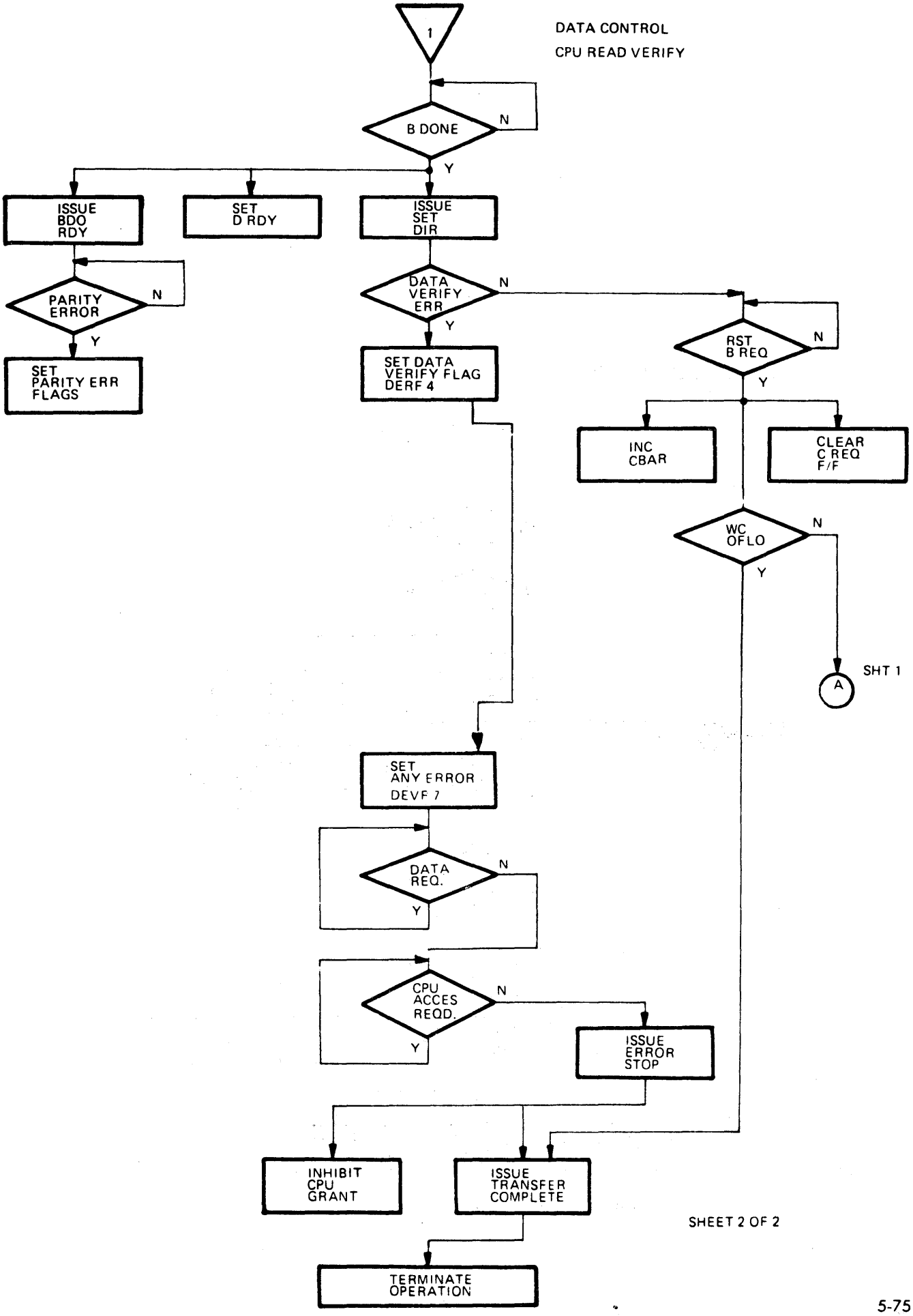
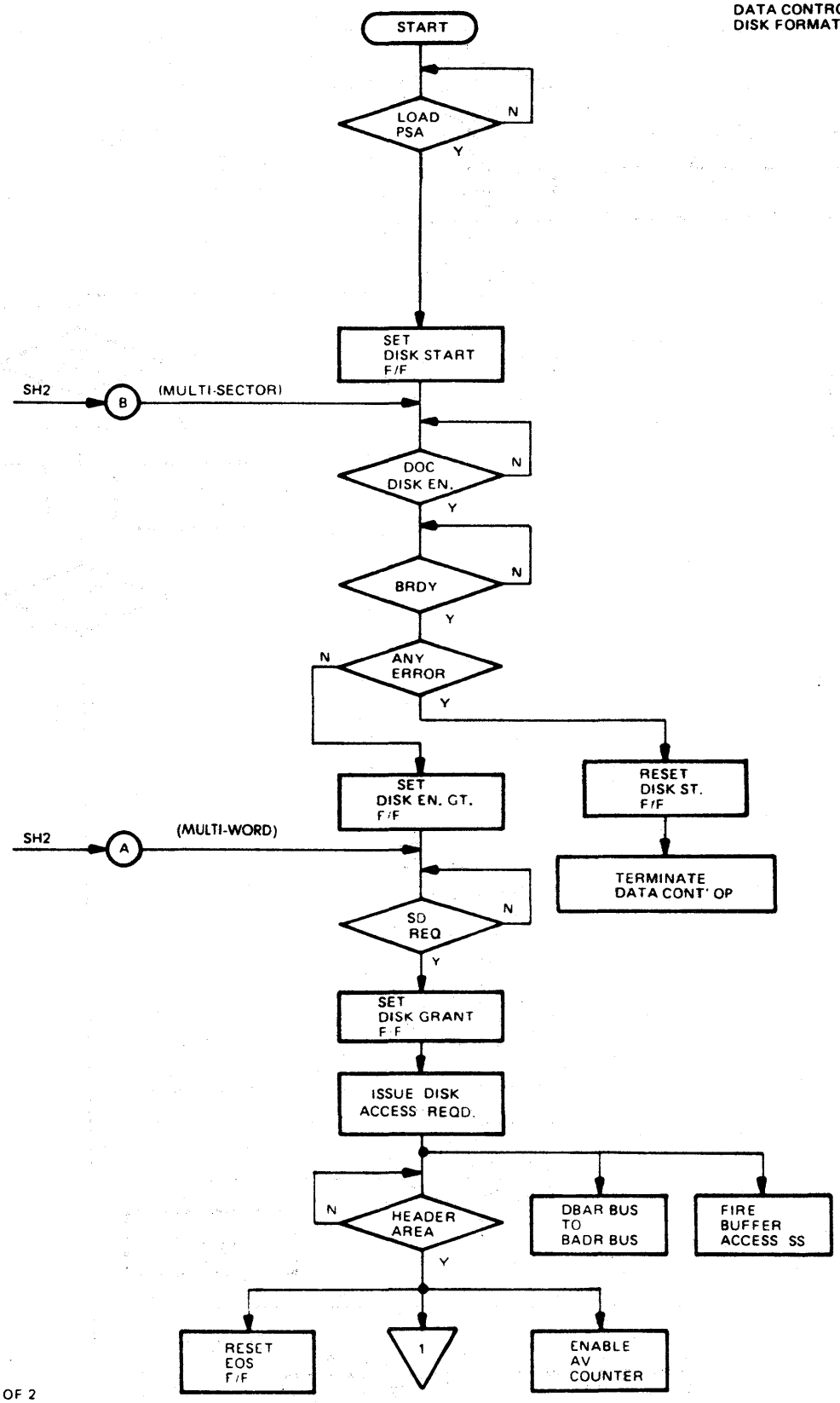


FIGURE 5-22. DATA CONTROL CPU READ VERIFY FLOW CHART

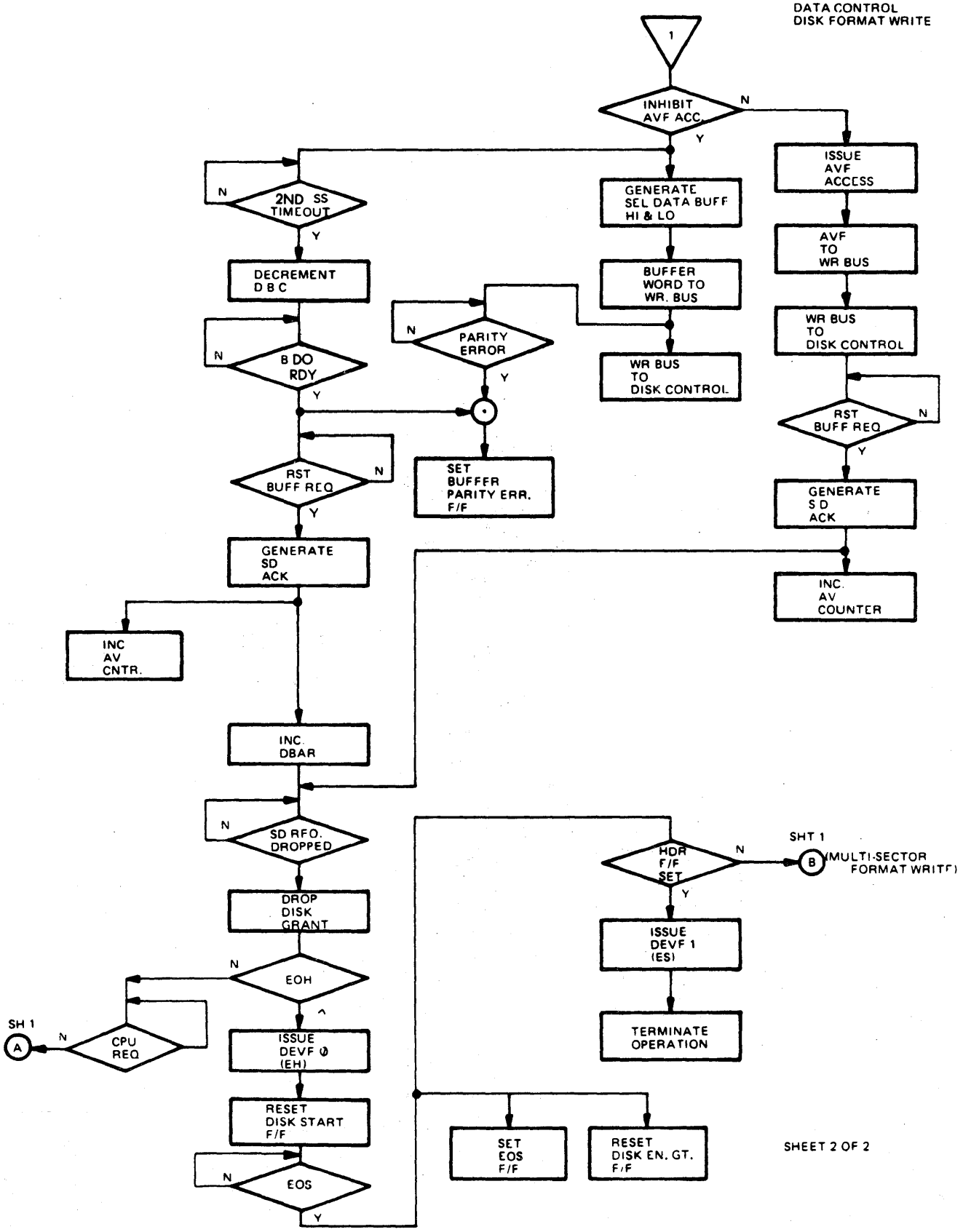
SHEET 1 OF 2


1
DATA CONTROL
CPU READ VERIFY
B DONE
N
Y
ISSUE BDO RDY
SET D RDY
ISSUE SET DIR
PARITY ERROR
N
Y
SET PARITY ERR FLAGS
DATA VERIFY ERR
N
Y
SET DATA VERIFY FLAG DERF 4
RST B REQ
N
Y
INC CBAR
CLEAR C REQ F/F
WC OFLO
N
Y
SHT 1
A
SET ANY ERROR DEVF 7
DATA REQ.
N
Y
CPU ACCES REQD.
N
Y
ISSUE ERROR STOP
INHIBIT CPU GRANT
ISSUE TRANSFER COMPLETE
TERMINATE OPERATION
SHEET 2 OF 2

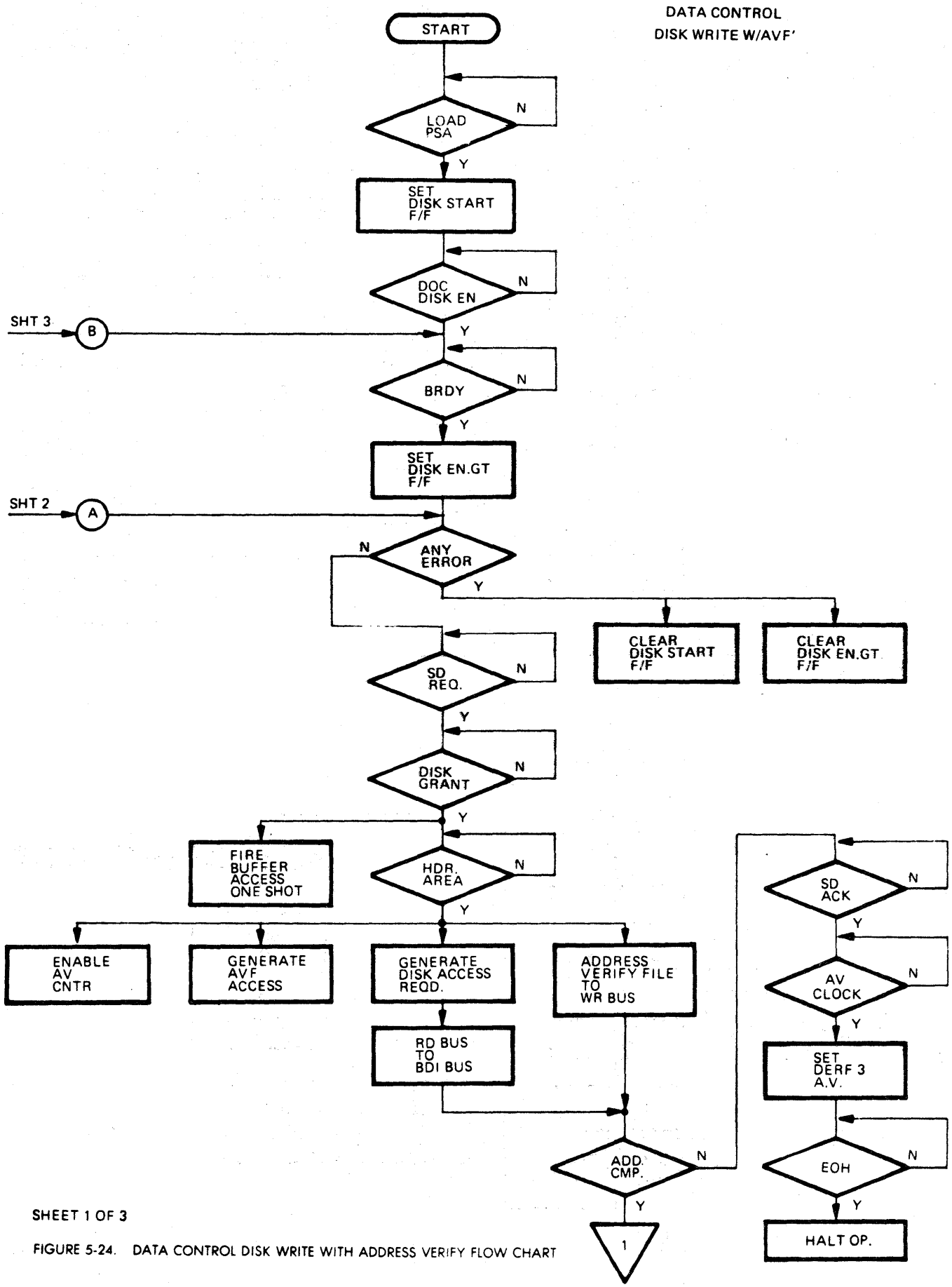


SHEET 1 OF 2

FIGURE 5-23. DATA CONTROL DISK FORMAT WRITE FLOW CHART


1
INHIBIT AVF ACC.
N
Y
ISSUE AVF ACCESS
AVF TO WR BUS
WR BUS TO DISK CONTROL
RST BUFF REQ
N
Y
GENERATE S D ACK
INC. AV COUNTER
GENERATE SEL DATA BUFF HI & LO
BUFFER WORD TO WR. BUS
WR BUS TO DISK CONTROL
N
2ND SS TIMEOUT
Y
DECREMENT D B C
N
B DO RDY
Y
N
PARITY ERROR
Y
SET BUFFER PARITY ERR. F/F
RST BUFF REQ
N
Y
GENERATE SD ACK
INC AV CNTR.
INC. DBAR
N
SD RFO. DROPPED
DROP DISK GRANT
N
EOH
SH 1
A
N
CPU REQ
ISSUE DEVF Ø (EH)
RESET DISK START F/F
N
EOS
Y
SET EOS F/F
RESET DISK EN. GT. F/F
HDR F/F SET
N
SHT 1
B
(MULTI-SECTOR FORMAT WRITE)
Y
ISSUE DEVF 1 (ES)
TERMINATE OPERATION

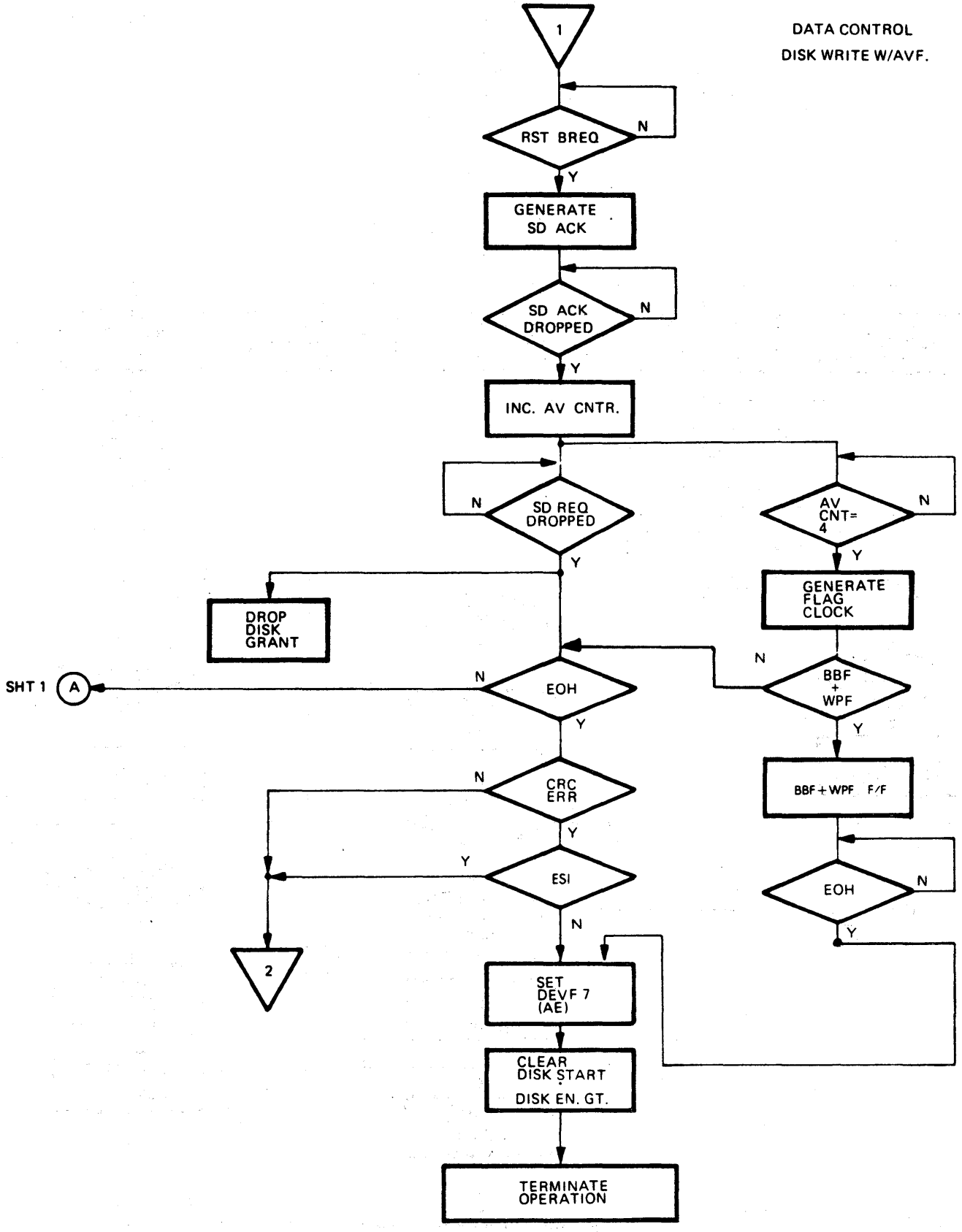
SHEET 2 OF 2



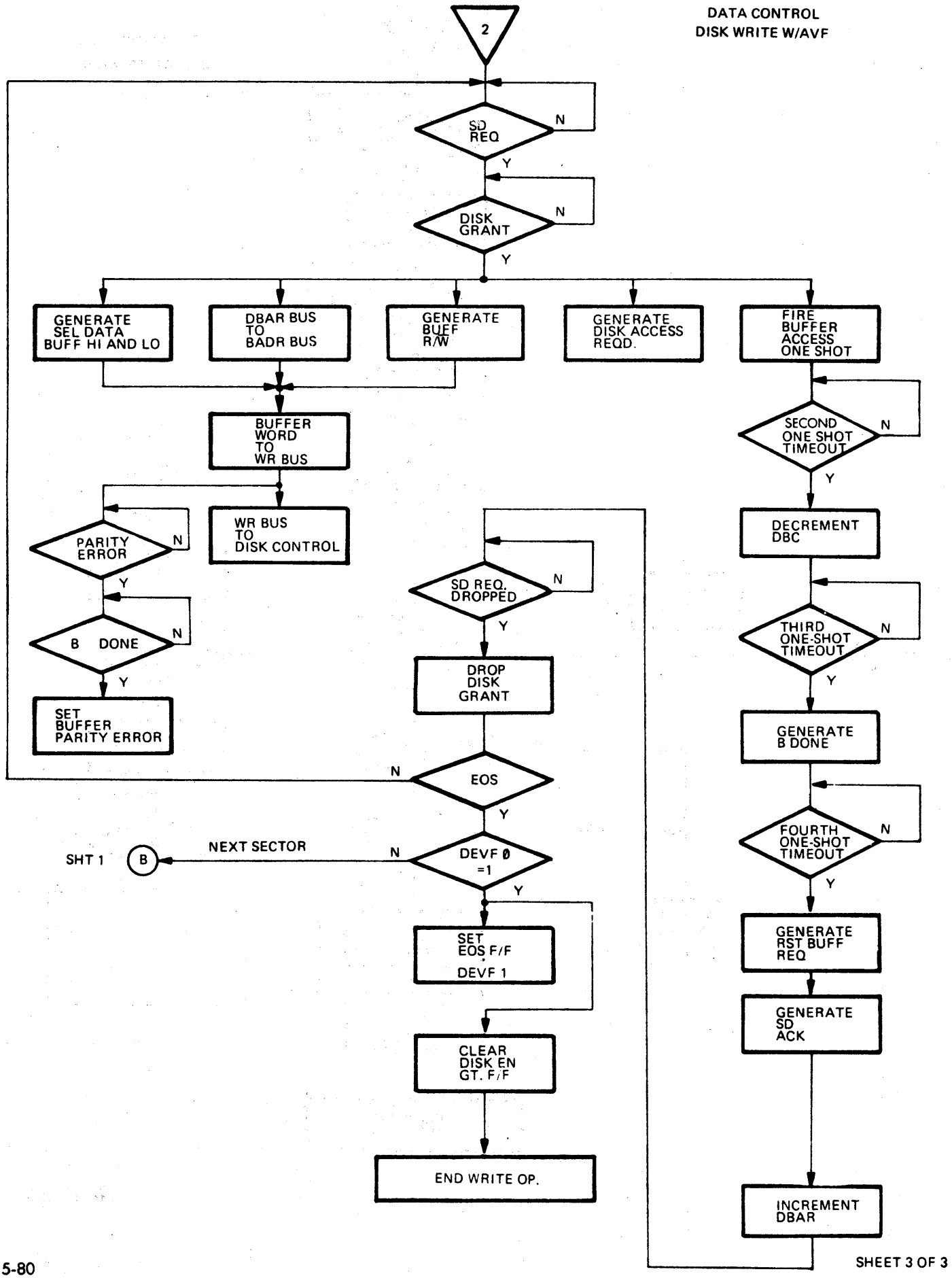
SHEET 1 OF 3

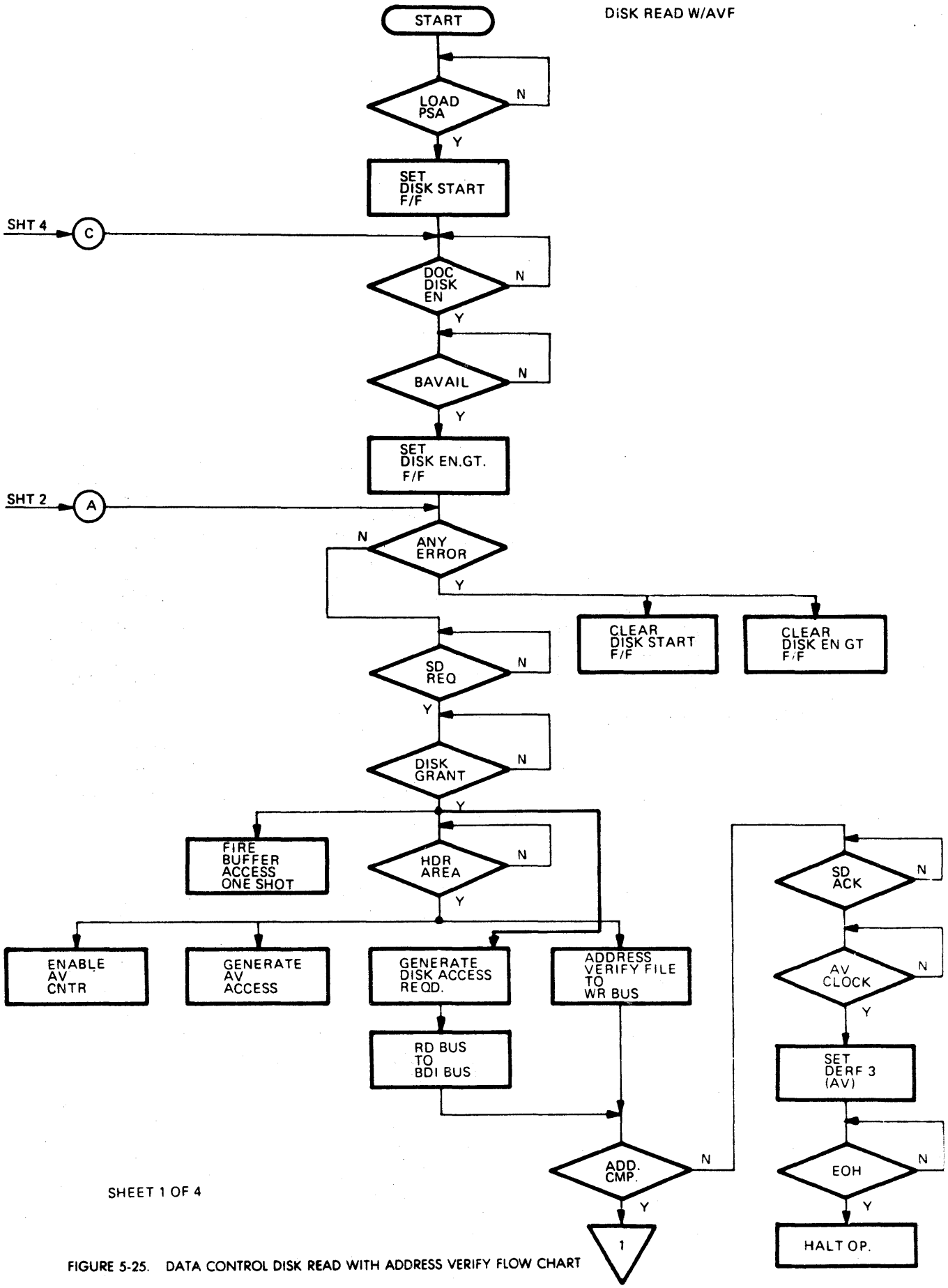
FIGURE 5-24. DATA CONTROL DISK WRITE WITH ADDRESS VERIFY FLOW CHART

DATA CONTROL
DISK WRITE W/AVF.



SHEET 2 OF 3

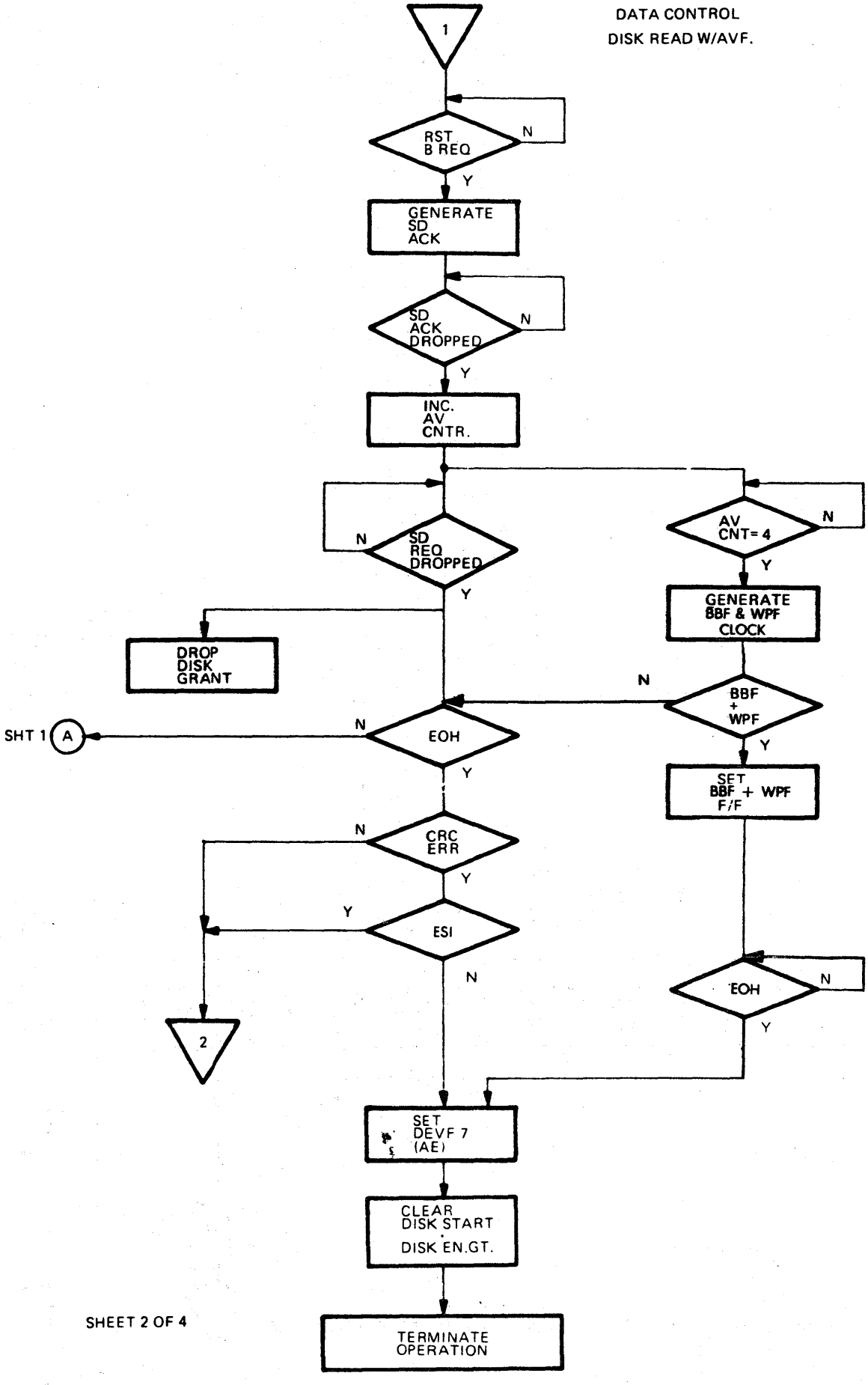

2
SD REQ
N
Y
DISK GRANT
N
Y
GENERATE SEL DATA BUFF HI AND LO
DBAR BUS TO BADR BUS
GENERATE BUFF R/W
GENERATE DISK ACCESS REQD.
FIRE BUFFER ACCESS ONE SHOT
BUFFER WORD TO WR BUS
SECOND ONE SHOT TIMEOUT
N
Y
PARITY ERROR
N
Y
WR BUS TO DISK CONTROL
DECREMENT DBC
B DONE
N
Y
SD REQ. DROPPED
N
Y
THIRD ONE-SHOT TIMEOUT
N
Y
SET BUFFER PARITY ERROR
DROP DISK GRANT
GENERATE B DONE
N
EOS
Y
FOURTH ONE-SHOT TIMEOUT
N
Y
SHT 1
B
NEXT SECTOR
N
DEVF Ø =1
Y
GENERATE RST BUFF REQ
SET EOS F/F
DEVF 1
GENERATE SD ACK
CLEAR DISK EN GT. F/F
END WRITE OP.
INCREMENT DBAR



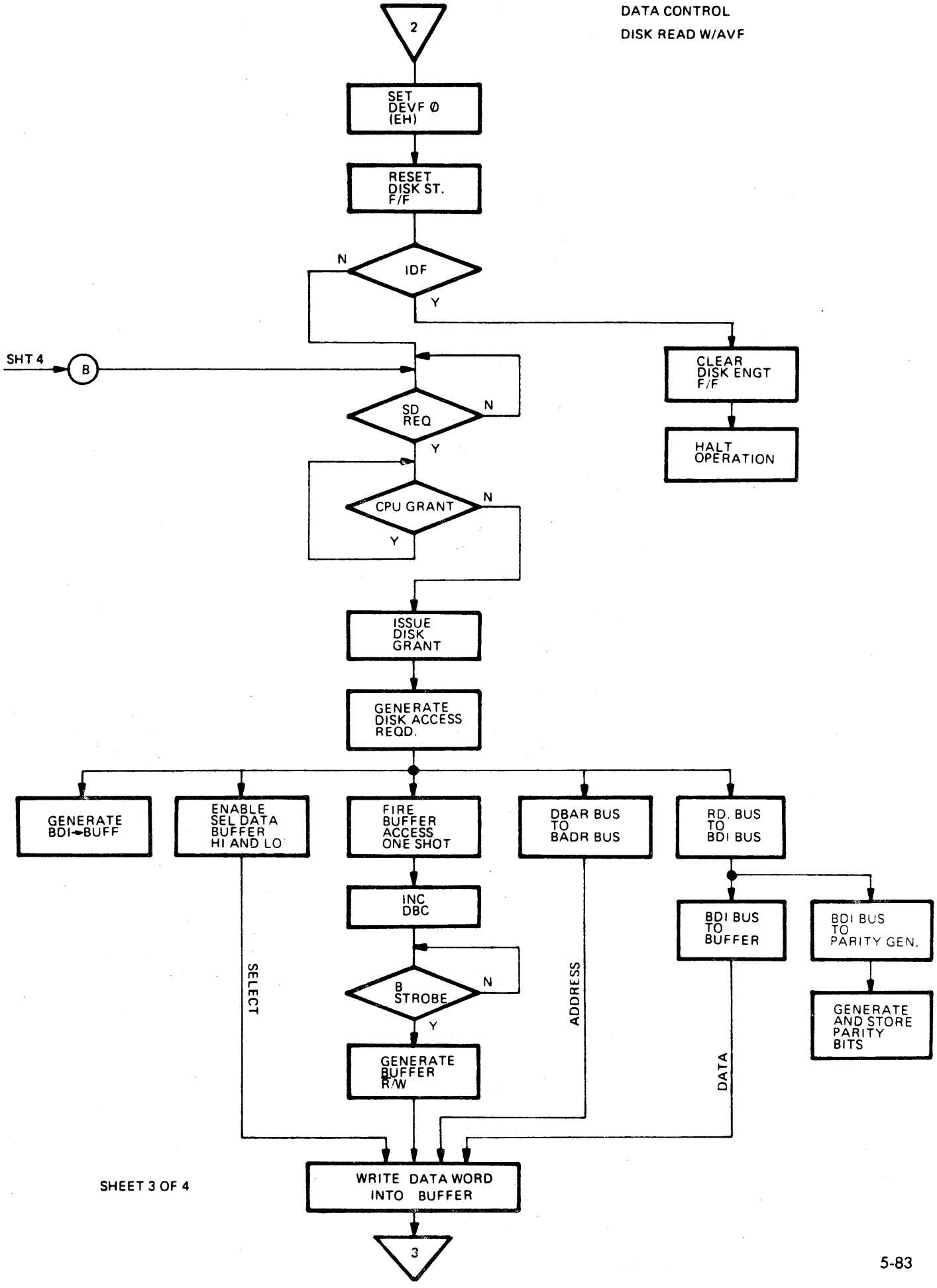
SHEET 1 OF 4

FIGURE 5-25. DATA CONTROL DISK READ WITH ADDRESS VERIFY FLOW CHART

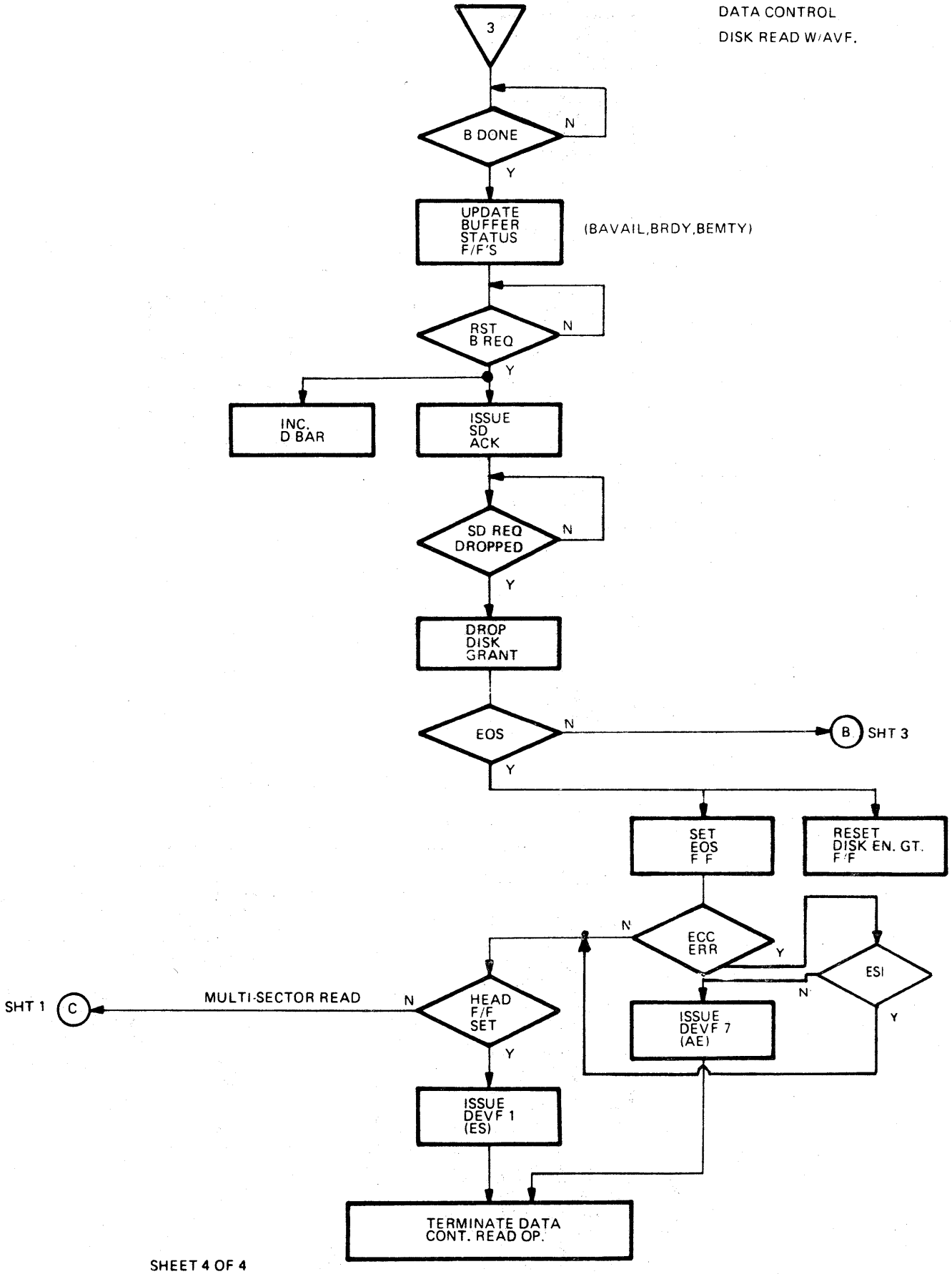
DATA CONTROL
DISK READ W/AVF.



SHEET 2 OF 4


2
SET DEVF Ø (EH)
RESET DISK ST. F/F
IDF
N
Y
SHT 4
B
CLEAR DISK ENGT F/F
HALT OPERATION
SD REQ
N
Y
CPU GRANT
N
Y
ISSUE DISK GRANT
GENERATE DISK ACCESS REQD.
GENERATE BDI→BUFF
ENABLE SEL DATA BUFFER HI AND LO
FIRE BUFFER ACCESS ONE SHOT
DBAR BUS TO BADR BUS
RD. BUS TO BDI BUS
INC DBC
B STROBE
N
Y
GENERATE BUFFER R/W
BDI BUS TO BUFFER
BDI BUS TO PARITY GEN.
GENERATE AND STORE PARITY BITS
SELECT
ADDRESS
DATA
WRITE DATA WORD INTO BUFFER
3

SHEET 3 OF 4


DATA CONTROL
DISK READ W/AVF.
3
B DONE
N
Y
UPDATE BUFFER STATUS F/F'S
(BAVAIL,BRDY,BEMTY)
RST B REQ
N
Y
INC. D BAR
ISSUE SD ACK
SD REQ DROPPED
N
Y
DROP DISK GRANT
EOS
N
B
SHT 3
Y
SET EOS F F
RESET DISK EN. GT. F/F
ECC ERR
N
Y
ESI
N
Y
ISSUE DEVF 7 (AE)
SHT 1
C
MULTI-SECTOR READ
HEAD F/F SET
N
Y
ISSUE DEVF 1 (ES)
TERMINATE DATA CONT. READ OP.

SHEET 4 OF 4

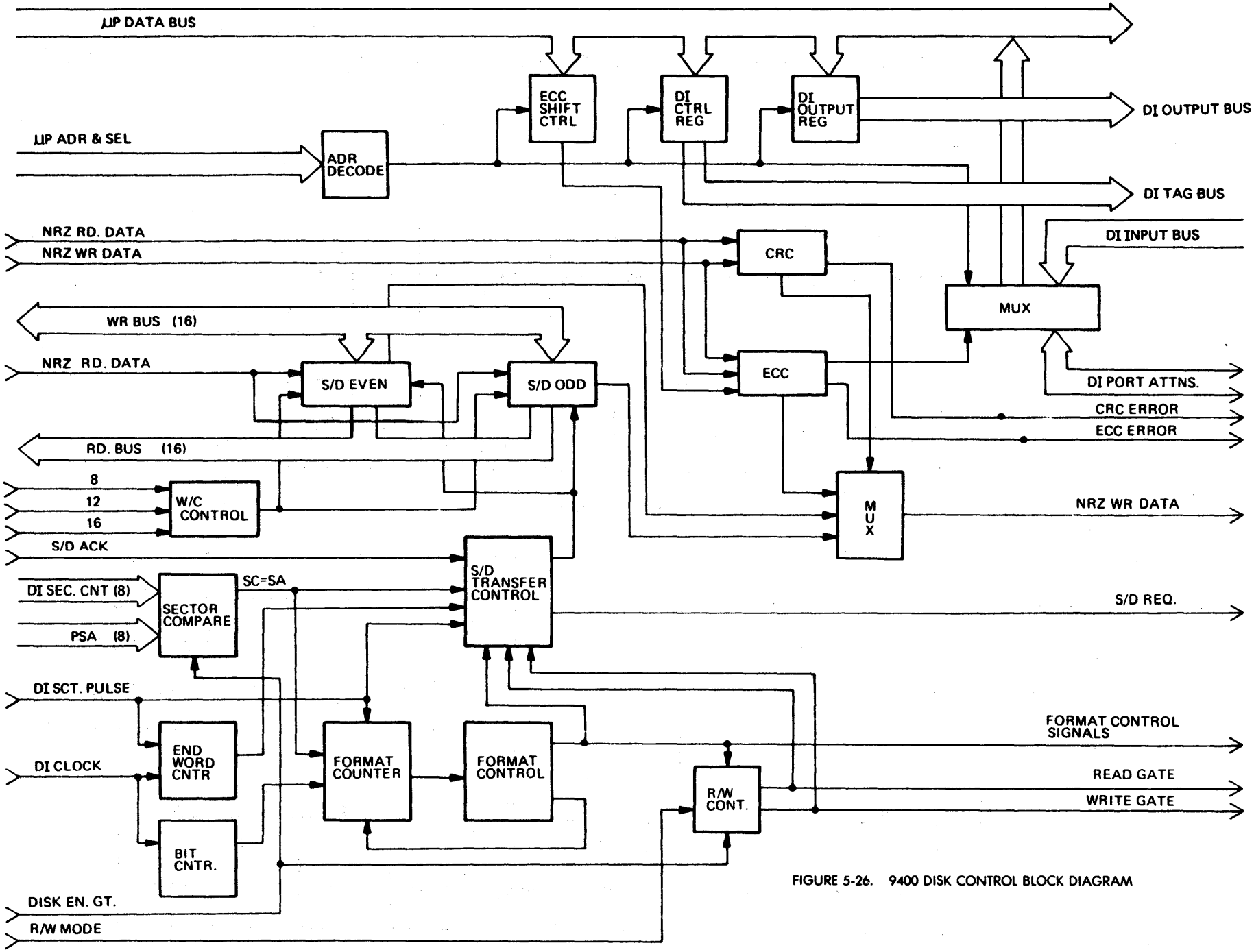
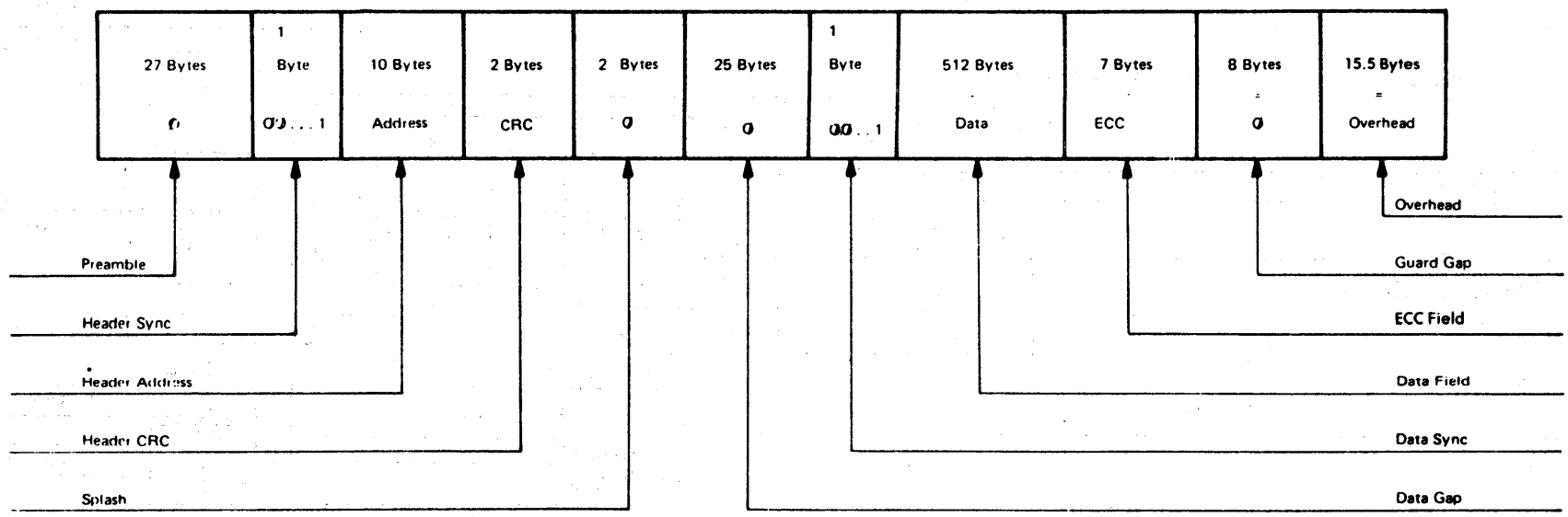
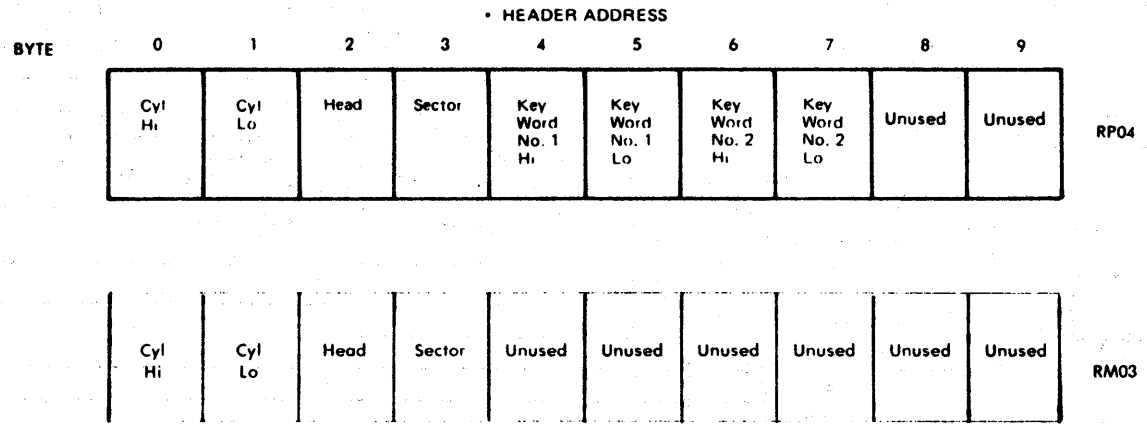


FIGURE 5-26. 9400 DISK CONTROL BLOCK DIAGRAM





NOTE: All ten header address bytes are timed although only cylinder, head, and sector are read.

Figure 5-27. 9400 Controller RP04 and RM03 Disk Sector Formats

DIC PROM SIGNALS	SIGNAL GOES TRUE BYTE COUNT	SIGNAL GOES FALSE BYTE COUNT
BOS #1	1	2
SET READ GT #1	11	12
BOS #2	24	25
WR H · D · CC REQ #1	25	37
HEADER AREA	25	40
LOAD SYNC BYTE #1	27	28
HEADER FIELD	27	37
RD H · D · CC REQ #1	29	40
IN WR CRC + ECC #1	35	37
CRC FIELD	37	39
SPLASH	41	42
IN RD CRC + ECC #1	39	41
DATA GAP	42	43
SET RD GT #2	50	51
BOS #3	64	65
DATA FIELD	67	580
LOAD SYNC BYTE #2	67	68
WR H · D · CC REQ #2	65	585
RD H · D · CC REQ #2	69	589
IN RD CRC + ECC #2	581	589
IN WR CRC + ECC #2	577	585
ECC FIELD	579	587
EOS	595	596

Disk Control Registers.

1. Disk Interface Input (DIB) (004100).

07	06	05	04	03	02	01	00
DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0

BIT	NAME	FUNCTION
07-00	DI_7-DI_0 Read Only	Stores drive status, error codes, drive model number, sector counter, etc. of the selected drive to be read by the microprocessor.

2. Disk Interface Flags (DIF) (004101)

07	06	05	04	03	02	01	00
-	-	-	-	ATN_3	ATN_2	ATN_1	ATN_0

BIT	NAME	FUNCTION
07-04	Not Used	N/A
03-00	ATN_3-ATN_0 Read Only	Drive Interface Port Attention 0-3. Provides interface flags to μP of selected interface. Reset with Strobe C on the CDC interface.

3. Disk Interface Output (DIO) (004104).

07	06	05	04	03	02	01	00
DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0

BIT	NAME	FUNCTION
07-00	DO_7-DO_0 Write Only	Select number, drive commands, cylinder number, lead number, etc. Cleared when strobed to applicable drive.

4. Disk Interface Control (DIC) (004105).

07	06	05	04	03	02	01	00
-	ST_D	ST_C	ST_B	ST_A	TB_2	TB_1	TB_0

BIT	NAME	FUNTION
07	Not Used	N/A
06	Strobe D Write Only	Select Tag to CDC drive.
05	Strobe C Write Only	Load Cylinder Hi to CDC drive. Must be issued prior to Cylinder Tag. Resets selected drive's attention flip-flop in the CDC interface.
04	Strobe B Write Only	Head Tag to CDC drive.
03	Strobe A Write Only	Cylinder Tag to CDC drive.

4. Disk Interface Control (KDIC) (004105). Continued

BIT	NAME	FUNCTION
02-00	Tag Bus_{2-0} Write Only	Tag Bus 2 1 0 0 0 0 Unused 0 0 1 Select Sector Counter 0 1 0 Select Sense 0 1 1 Select Status 1 0 0 Select Control 1 0 1 Reserved 1 1 0 Reserved 1 1 1 Reserved

5. ECC Shift Control (ECCSC) (004106).

07	06	05	04	03	02	01	00
-	-	-	-	SP_3	SP_2	SP_1	SP_0

BIT	NAME	FUNCTION
07-04	Not Used	N/A
03	Shift P_3 Write Only	Shift ECC data in polynomial register 3 under μP control.
02	Shift P_2 Write Only	Shift ECC data in polynomial register 2 under μP control.
01	Shift P_1 Write Only	Shift ECC data in polynomial register 1 under μP control.
00	Shift P_0 Write Only	Shift ECC data in polynomial register 0 under μP control.

6. ECC Byte 0 (ECCB0) (004110)

07	06	05	04	03	02	01	00
EC_{48}	EC_{49}	EC_{50}	EC_{51}	EC_{52}	EC_{53}	EC_{54}	EC_{55}

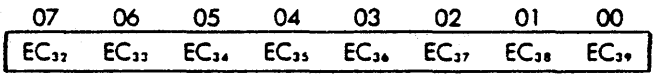
BIT	NAME	FUNCTION
07-00	EC_{48}-EC_{55} Read Only	One byte of the ECC data.

7. ECC Byte 1 (ECCB1) (004111).

07	06	05	04	03	02	01	00
EC_{40}	EC_{41}	EC_{42}	EC_{43}	EC_{44}	EC_{45}	EC_{46}	EC_{47}

BIT	NAME	FUNCTION
07-00	EC_{42}-EC_{47} Read Only	One byte of the ECC data.

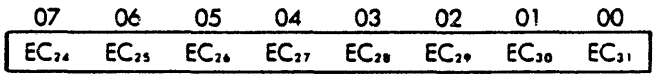
8. ECC Byte 2 (ECCB2) (004112).



07	06	05	04	03	02	01	00
EC_{32}	EC_{33}	EC_{34}	EC_{35}	EC_{36}	EC_{37}	EC_{38}	EC_{39}

BIT	NAME	FUNCTION
07-00	EC_{32}-EC_{39} Read Only	One byte of the ECC data.

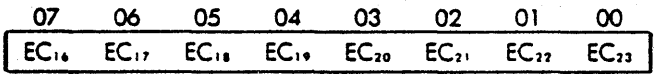
9. ECC Byte 3 (ECCB3) (004113).



07	06	05	04	03	02	01	00
EC_{24}	EC_{25}	EC_{26}	EC_{27}	EC_{28}	EC_{29}	EC_{30}	EC_{31}

BIT	NAME	FUNCTION
07-00	EC_{24}-EC_{31} Read Only	One byte of the ECC data.

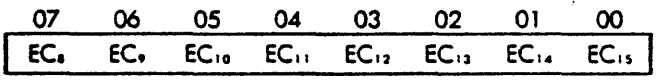
10. ECC Byte 4 (ECCB4) (004114).



07	06	05	04	03	02	01	00
EC_{16}	EC_{17}	EC_{18}	EC_{19}	EC_{20}	EC_{21}	EC_{22}	EC_{23}

BIT	NAME	FUNCTION
07-00	EC_{16}-EC_{23} Read Only	One byte of the ECC data.

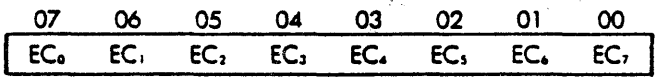
11. ECC Byte 5 (ECCB5) (004115).



07	06	05	04	03	02	01	00
EC_{8}	EC_{9}	EC_{10}	EC_{11}	EC_{12}	EC_{13}	EC_{14}	EC_{15}

BIT	NAME	FUNCTION
07-00	EC_{8}-EC_{15} Read Only	One byte of the ECC data.

12. ECC Byte 6 (ECCB6) (004116).



07	06	05	04	03	02	01	00
EC_{0}	EC_{1}	EC_{2}	EC_{3}	EC_{4}	EC_{5}	EC_{6}	EC_{7}

BIT	NAME	FUNCTION
07-00	EC_{0}-EC_{7} Read Only	One byte of the ECC data.

13. ECC Zero Flags (ECCZF) (004117).

07	06	05	04	03	02	01	00
-	-	-	-	$P3_z$	$P2_z$	$P1_z$	$P0_z$

BIT	NAME	FUNCTION
07-04	Not Used	N/A
03	P3 zero Read Only	Set when ECC polynomial register 3 is zero.
02	P2 zero Read Only	Set when ECC polynomial register 2 is zero.
01	P1 zero Read Only	Set when ECC polynomial register 1 is zero.
00	P0 zero Read Only	Set when ECC polynomial register 0 is zero.

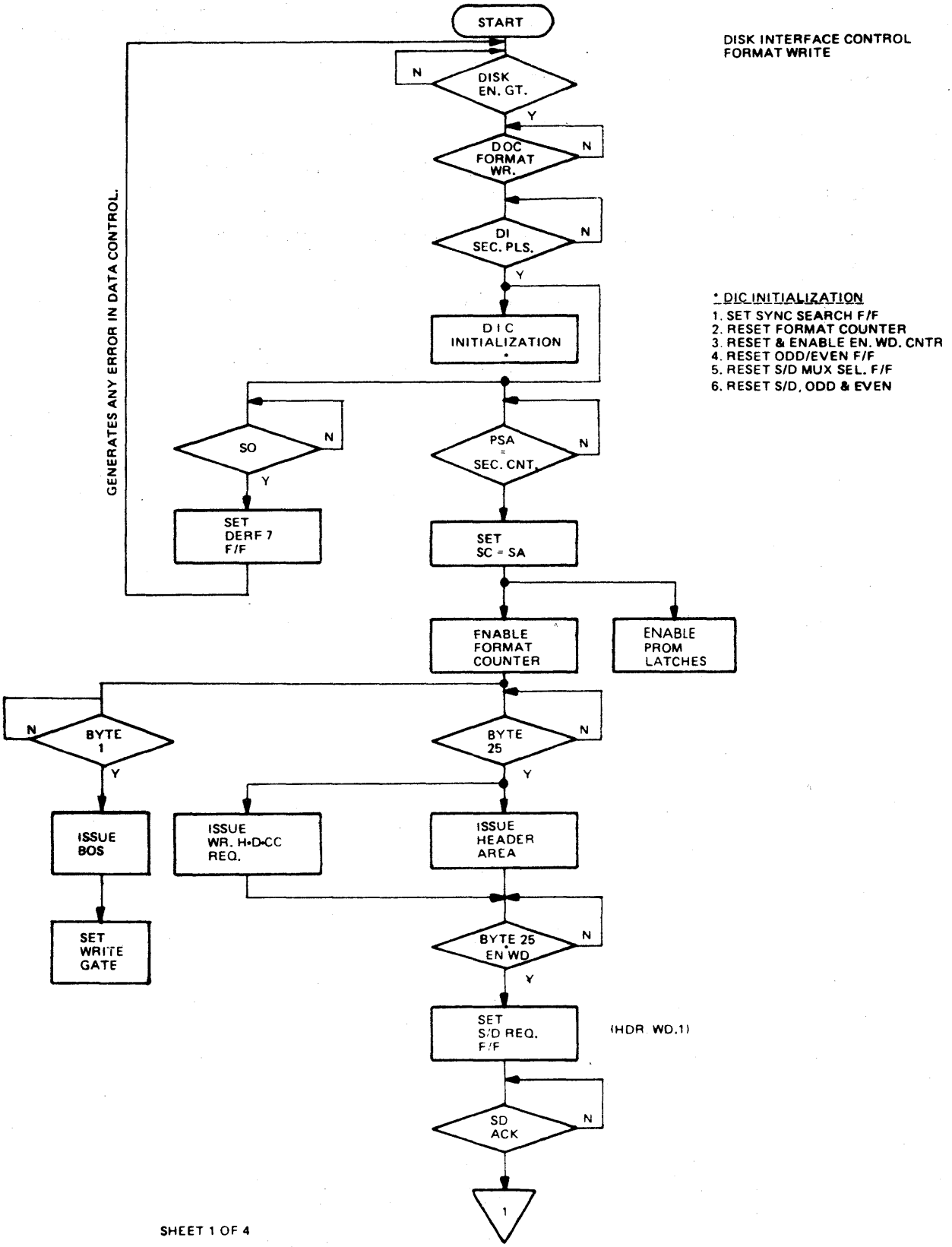
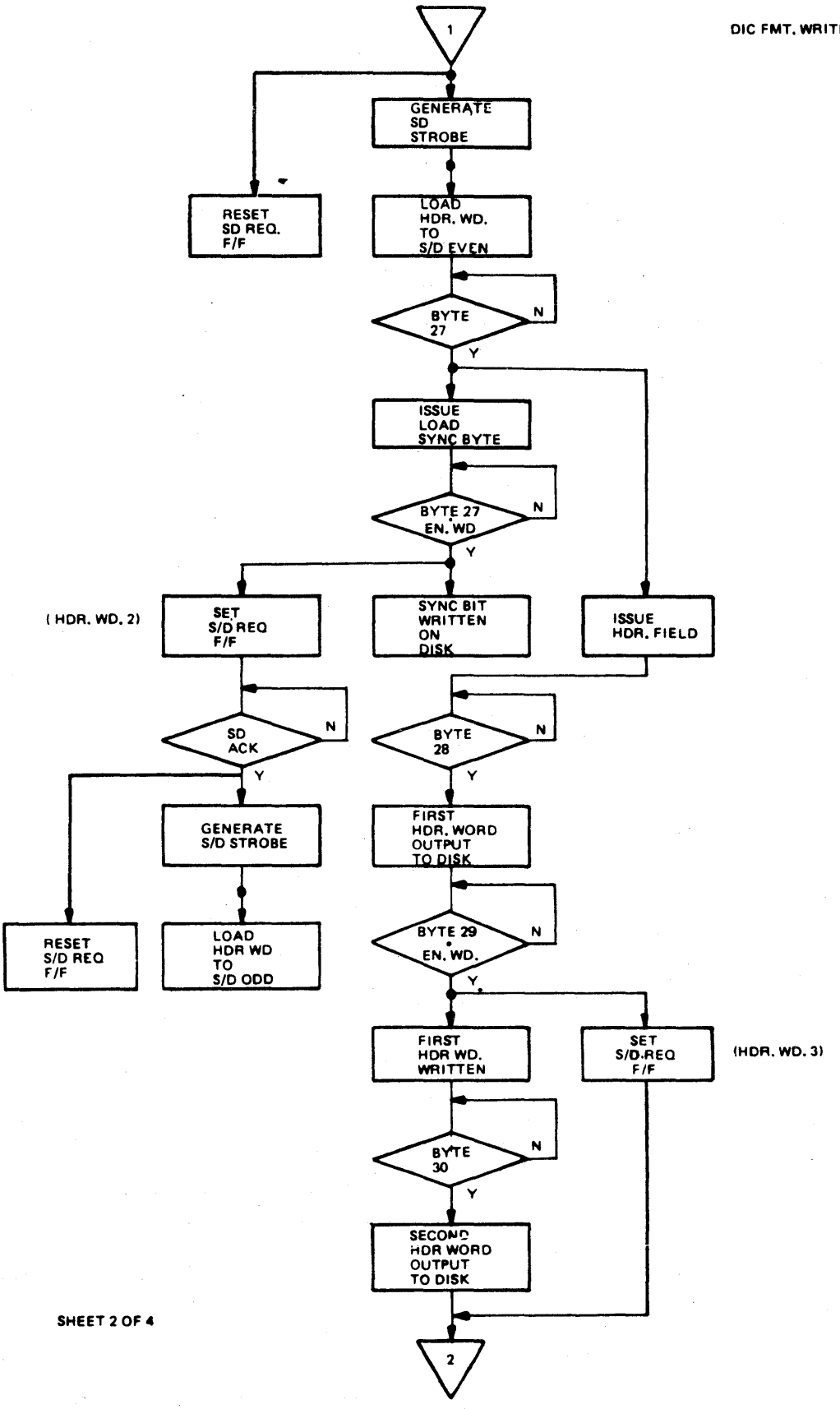
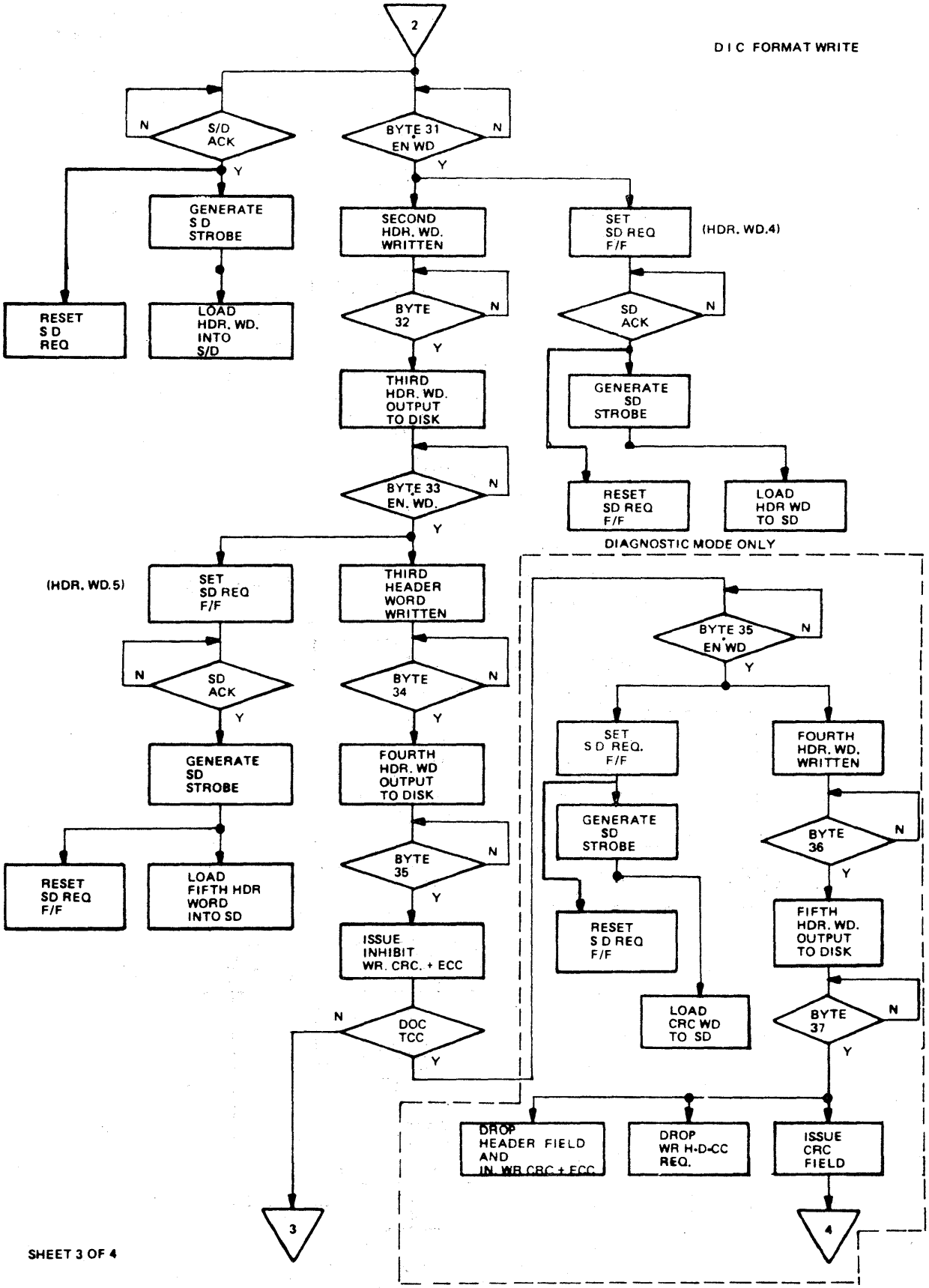


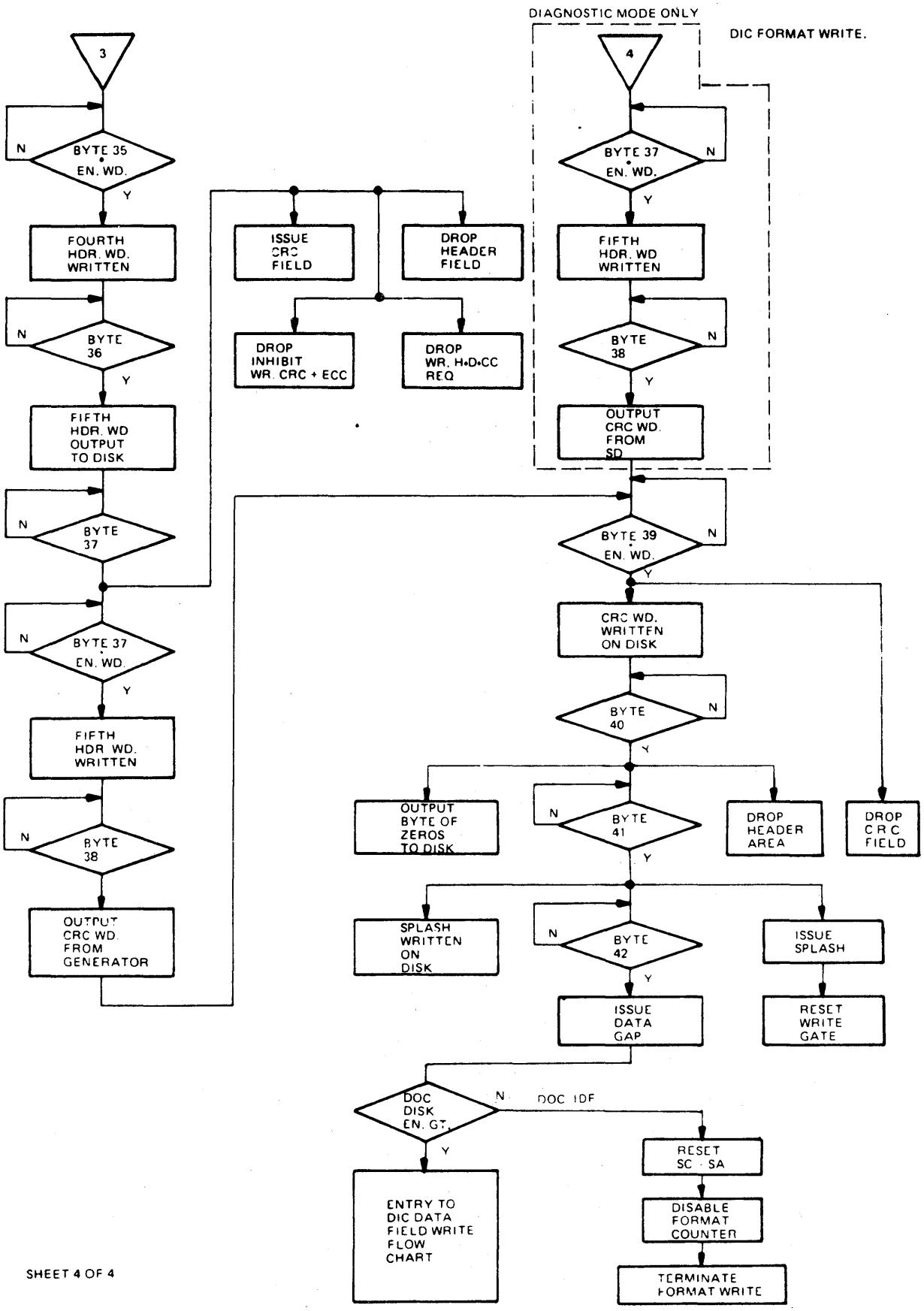
FIGURE 5-28. DISK INTERFACE CONTROL FORMAT WRITE FLOW CHART


1
GENERATE SD STROBE
RESET SD REQ. F/F
LOAD HDR. WD. TO S/D EVEN
BYTE 27
N
Y
ISSUE LOAD SYNC BYTE
BYTE 27 EN. WD
N
Y
(HDR. WD. 2)
SET S/D REQ F/F
SYNC BIT WRITTEN ON DISK
ISSUE HDR. FIELD
SD ACK
N
Y
BYTE 28
N
Y
GENERATE S/D STROBE
FIRST HDR. WORD OUTPUT TO DISK
RESET S/D REQ F/F
LOAD HDR WD TO S/D ODD
BYTE 29 EN. WD.
N
Y
FIRST HDR WD. WRITTEN
SET S/D REQ F/F
(HDR. WD. 3)
BYTE 30
N
Y
SECOND HDR WORD OUTPUT TO DISK
2

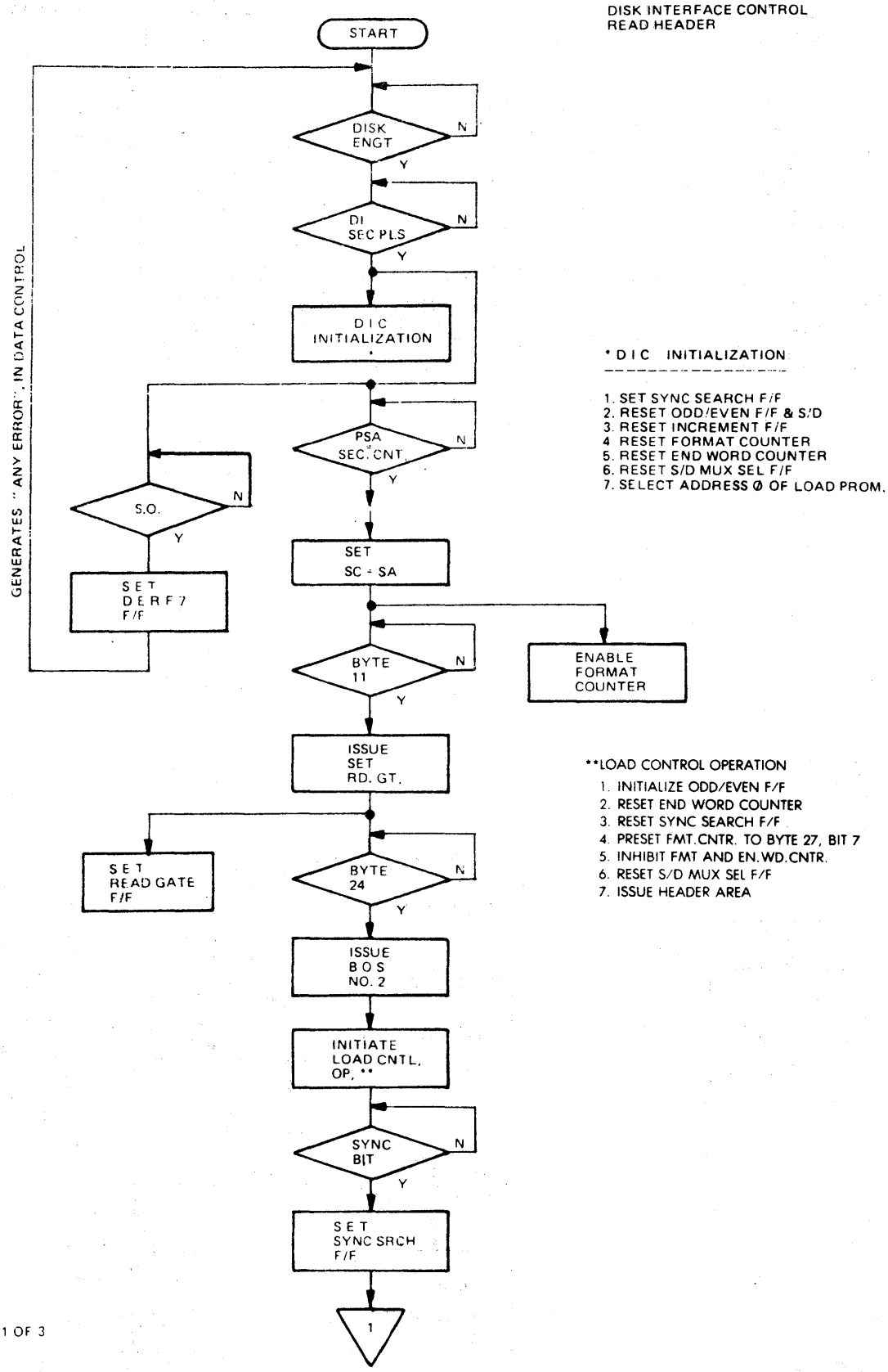
SHEET 2 OF 4


2
D I C FORMAT WRITE
N
S/D ACK
Y
GENERATE S D STROBE
RESET S D REQ
LOAD HDR. WD. INTO S/D
BYTE 31 EN WD
N
Y
SECOND HDR. WD. WRITTEN
BYTE 32
N
Y
THIRD HDR. WD. OUTPUT TO DISK
BYTE 33 EN. WD.
N
Y
SET SD REQ F/F
(HDR. WD.4)
SD ACK
N
GENERATE SD STROBE
RESET SD REQ F/F
LOAD HDR WD TO SD
DIAGNOSTIC MODE ONLY
(HDR. WD.5)
SET SD REQ F/F
N
SD ACK
Y
GENERATE SD STROBE
RESET SD REQ F/F
LOAD FIFTH HDR WORD INTO SD
THIRD HEADER WORD WRITTEN
BYTE 34
N
Y
FOURTH HDR. WD OUTPUT TO DISK
BYTE 35
N
Y
ISSUE INHIBIT WR. CRC. + ECC
N
DOC TCC
Y
3
BYTE 35 EN WD
N
Y
SET S D REQ. F/F
GENERATE SD STROBE
RESET S D REQ F/F
LOAD CRC WD TO SD
FOURTH HDR. WD. WRITTEN
BYTE 36
N
Y
FIFTH HDR. WD. OUTPUT TO DISK
BYTE 37
N
Y
DROP HEADER FIELD AND IN. WR CRC + ECC
DROP WR H-D-CC REQ.
ISSUE CRC FIELD
4

SHEET 3 OF 4

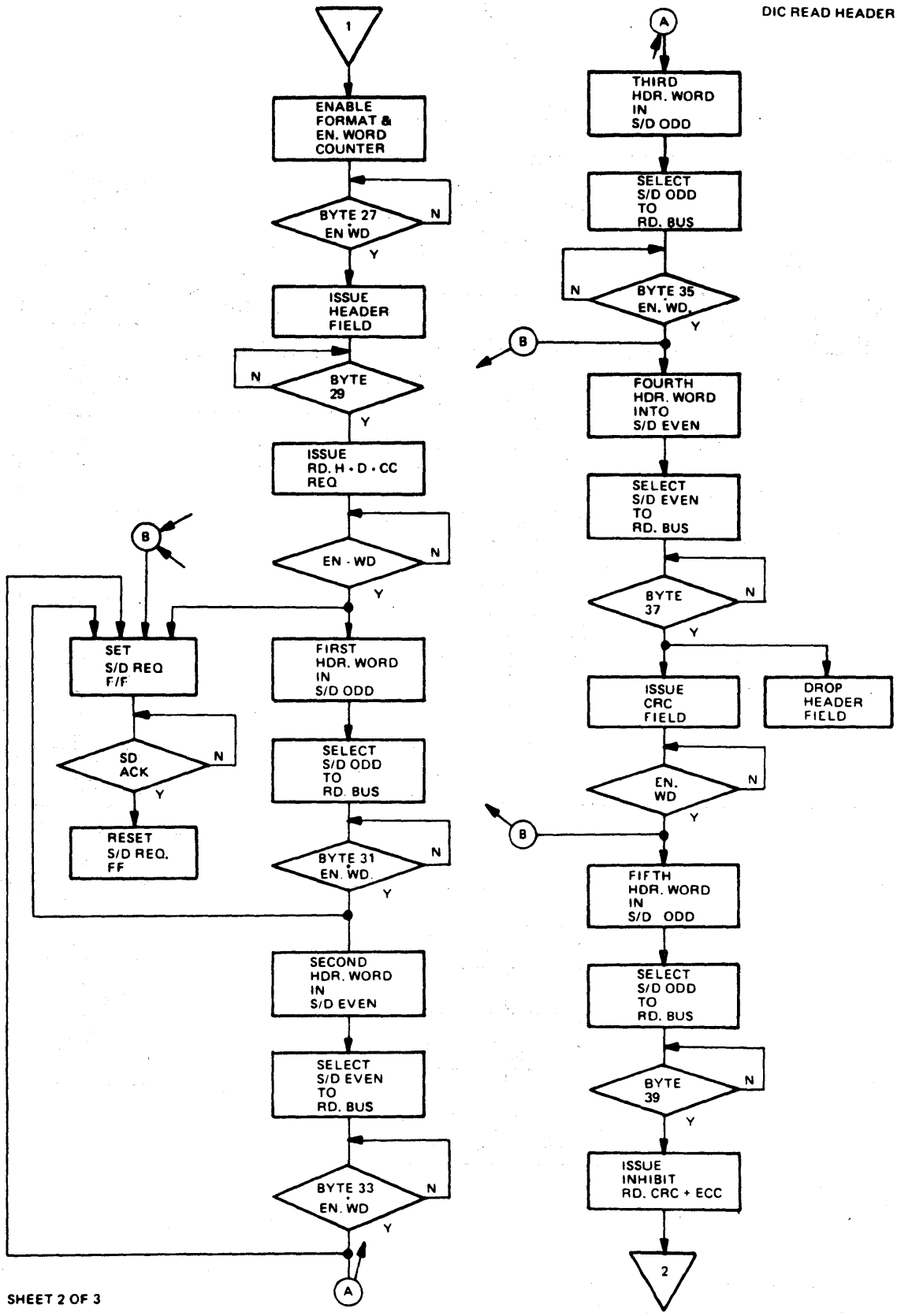

DIAGNOSTIC MODE ONLY
DIC FORMAT WRITE.
3
4
BYTE 35 • EN. WD.
FOURTH HDR. WD. WRITTEN
BYTE 36
FIFTH HDR. WD OUTPUT TO DISK
BYTE 37
BYTE 37 • EN. WD.
FIFTH HDR. WD. WRITTEN
BYTE 38
OUTPUT CRC WD. FROM GENERATOR
ISSUE CRC FIELD
DROP HEADER FIELD
DROP INHIBIT WR. CRC + ECC
DROP WR. H•D•CC REQ
BYTE 37 • EN. WD.
FIFTH HDR. WD WRITTEN
BYTE 38
OUTPUT CRC WD. FROM SD
BYTE 39 • EN. WD.
CRC WD. WRITTEN ON DISK
BYTE 40
OUTPUT BYTE OF ZEROS TO DISK
BYTE 41
DROP HEADER AREA
DROP C R C FIELD
SPLASH WRITTEN ON DISK
BYTE 42
ISSUE SPLASH
ISSUE DATA GAP
RESET WRITE GATE
DOC DISK EN. GT.
DOC IDF
RESET SC : SA
DISABLE FORMAT COUNTER
TERMINATE FORMAT WRITE
ENTRY TO DIC DATA FIELD WRITE FLOW CHART
N
Y

SHEET 4 OF 4

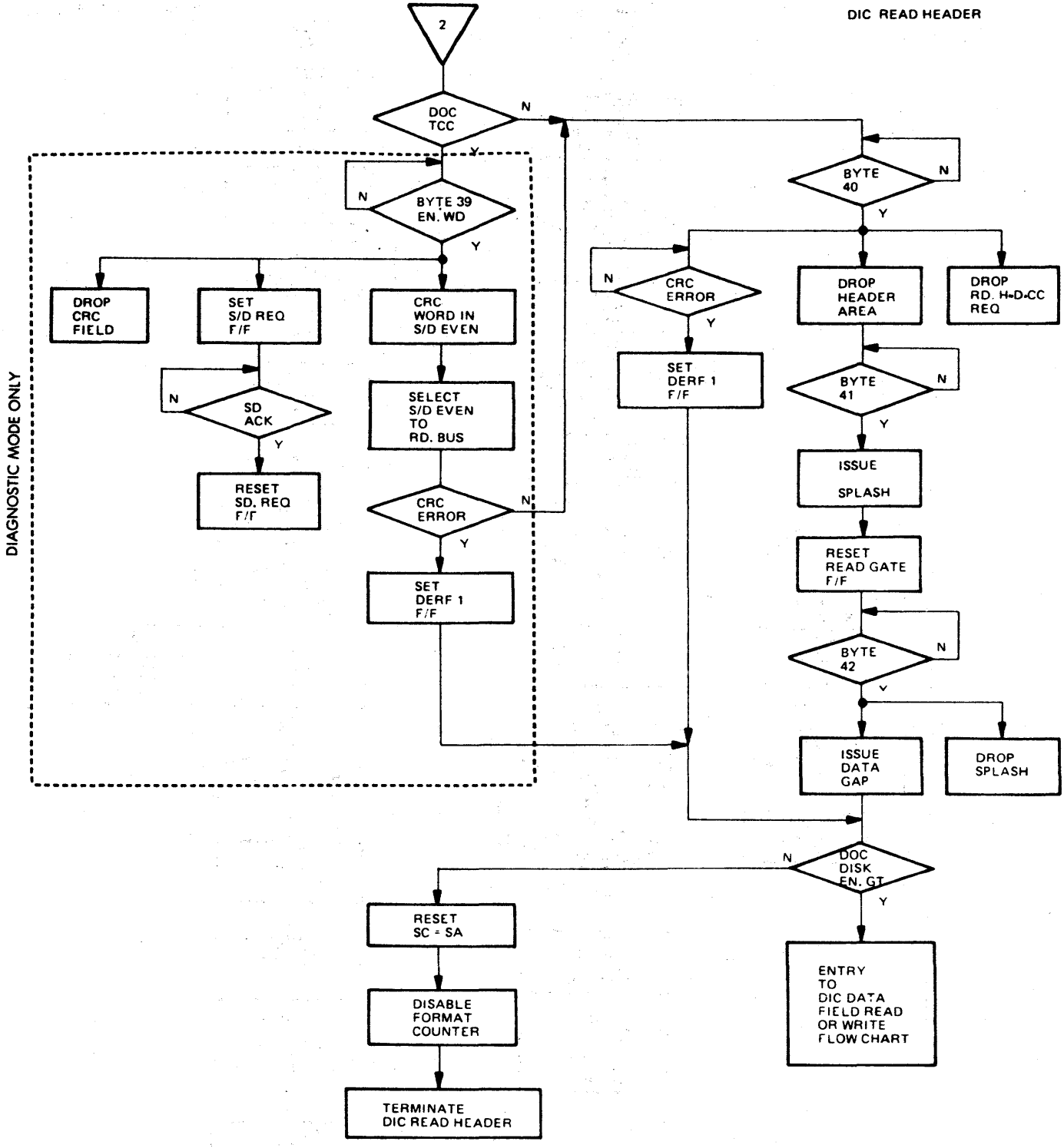


SHEET 1 OF 3

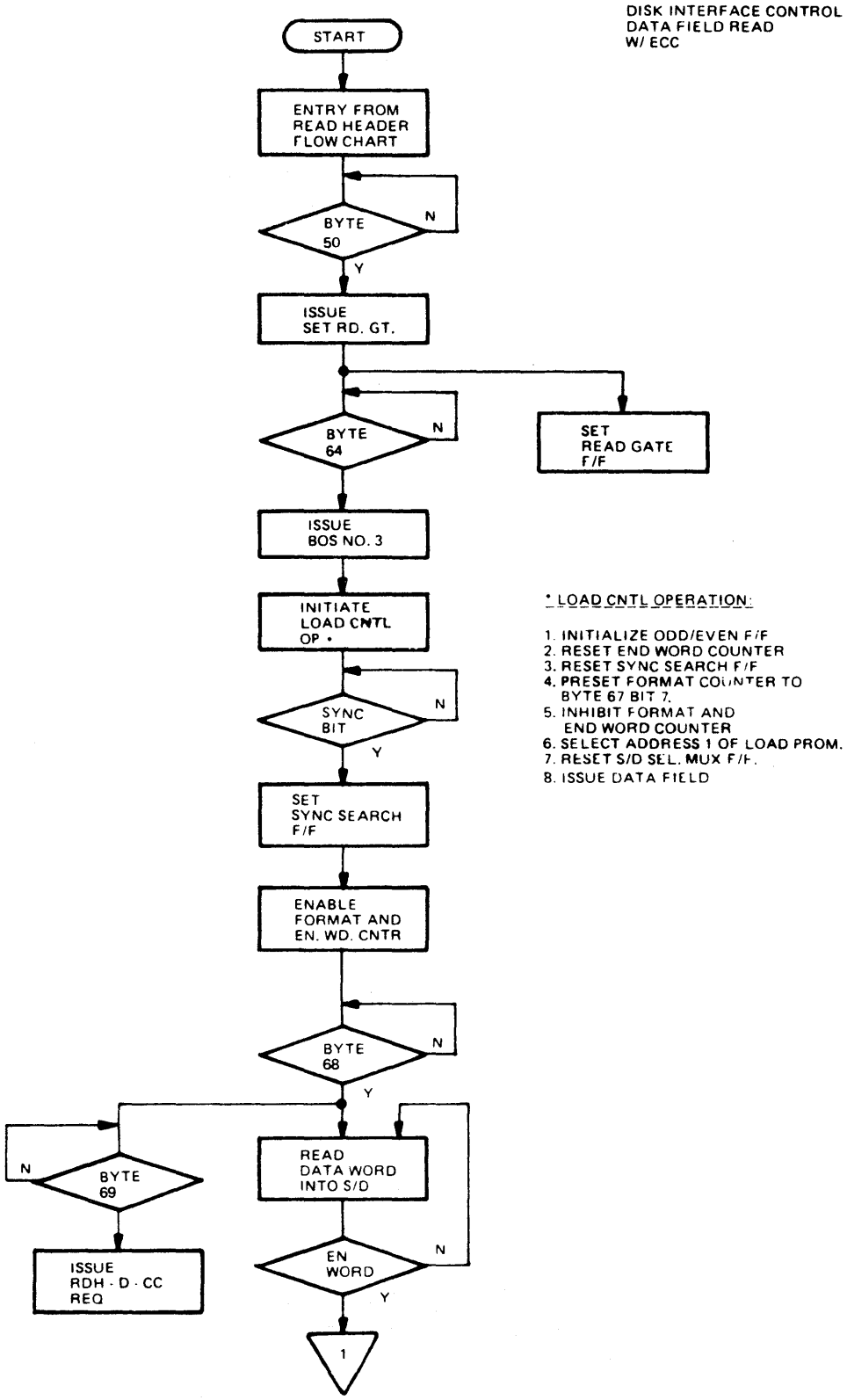
FIGURE 5-29. DISK INTERFACE CONTROL READ HEADER FLOW CHART


1
ENABLE FORMAT & EN. WORD COUNTER
BYTE 27 EN WD
N
Y
ISSUE HEADER FIELD
N
BYTE 29
Y
ISSUE RD. H • D • CC REQ
EN • WD
N
Y
B
SET S/D REQ F/F
SD ACK
N
Y
RESET S/D REQ. FF
FIRST HDR. WORD IN S/D ODD
SELECT S/D ODD TO RD. BUS
BYTE 31 EN. WD.
N
Y
SECOND HDR. WORD IN S/D EVEN
SELECT S/D EVEN TO RD. BUS
BYTE 33 EN. WD
N
Y
A
A
THIRD HDR. WORD IN S/D ODD
SELECT S/D ODD TO RD. BUS
N
BYTE 35 EN. WD.
Y
B
FOURTH HDR. WORD INTO S/D EVEN
SELECT S/D EVEN TO RD. BUS
BYTE 37
N
Y
ISSUE CRC FIELD
DROP HEADER FIELD
EN. WD
N
Y
B
FIFTH HDR. WORD IN S/D ODD
SELECT S/D ODD TO RD. BUS
BYTE 39
N
Y
ISSUE INHIBIT RD. CRC + ECC
2

SHEET 2 OF 3


DIC READ HEADER
2
DOC TCC
N
Y
BYTE 39 EN. WD
N
Y
DROP CRC FIELD
SET S/D REQ F/F
CRC WORD IN S/D EVEN
N
SD ACK
Y
RESET SD. REQ F/F
SELECT S/D EVEN TO RD. BUS
CRC ERROR
N
Y
SET DERF 1 F/F
DIAGNOSTIC MODE ONLY
BYTE 40
N
Y
N
CRC ERROR
Y
SET DERF 1 F/F
DROP HEADER AREA
DROP RD. H-D-CC REQ
BYTE 41
N
Y
ISSUE SPLASH
RESET READ GATE F/F
BYTE 42
N
Y
ISSUE DATA GAP
DROP SPLASH
N
DOC DISK EN. GT
Y
RESET SC = SA
DISABLE FORMAT COUNTER
TERMINATE DIC READ HEADER
ENTRY TO DIC DATA FIELD READ OR WRITE FLOW CHART

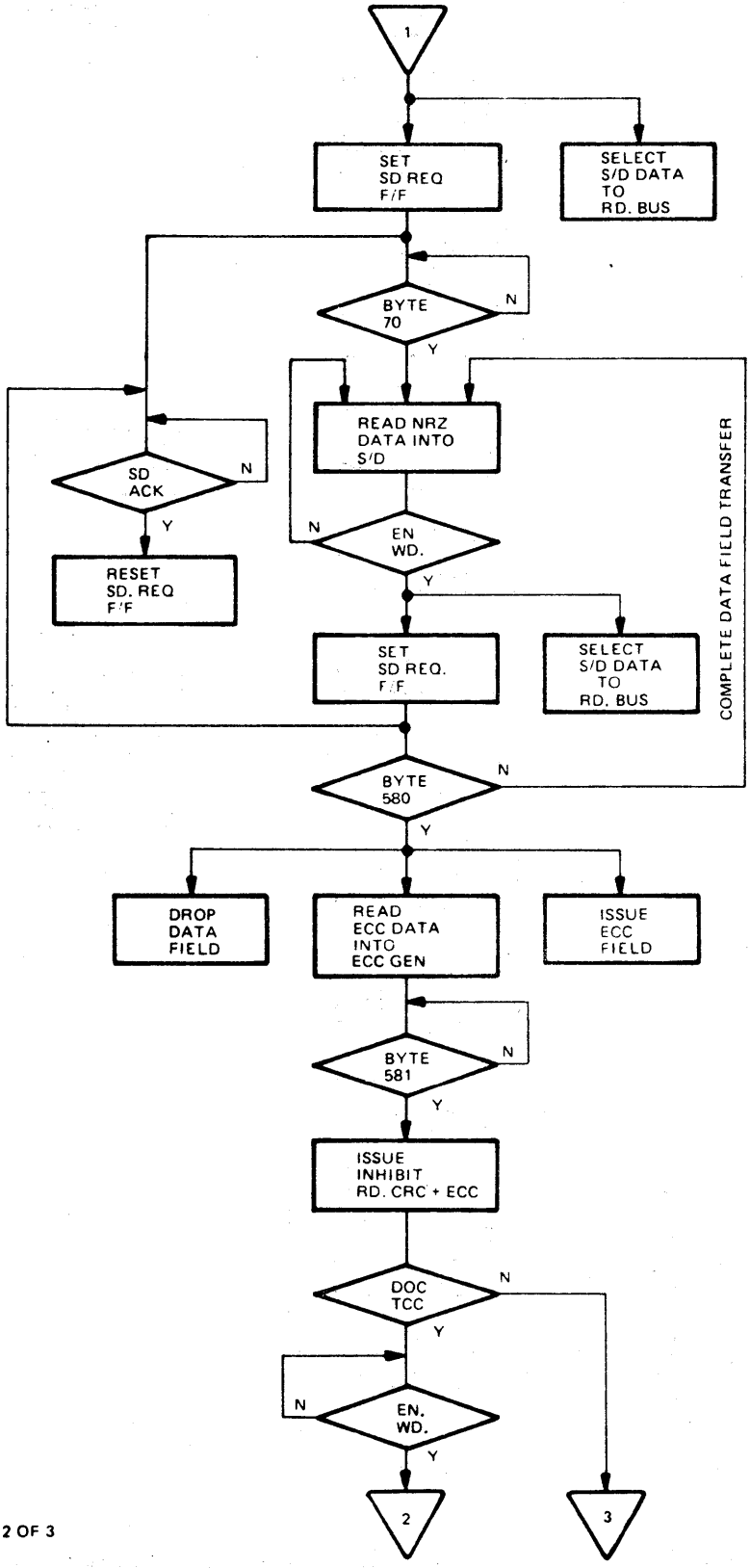
SHEET 3 OF 3



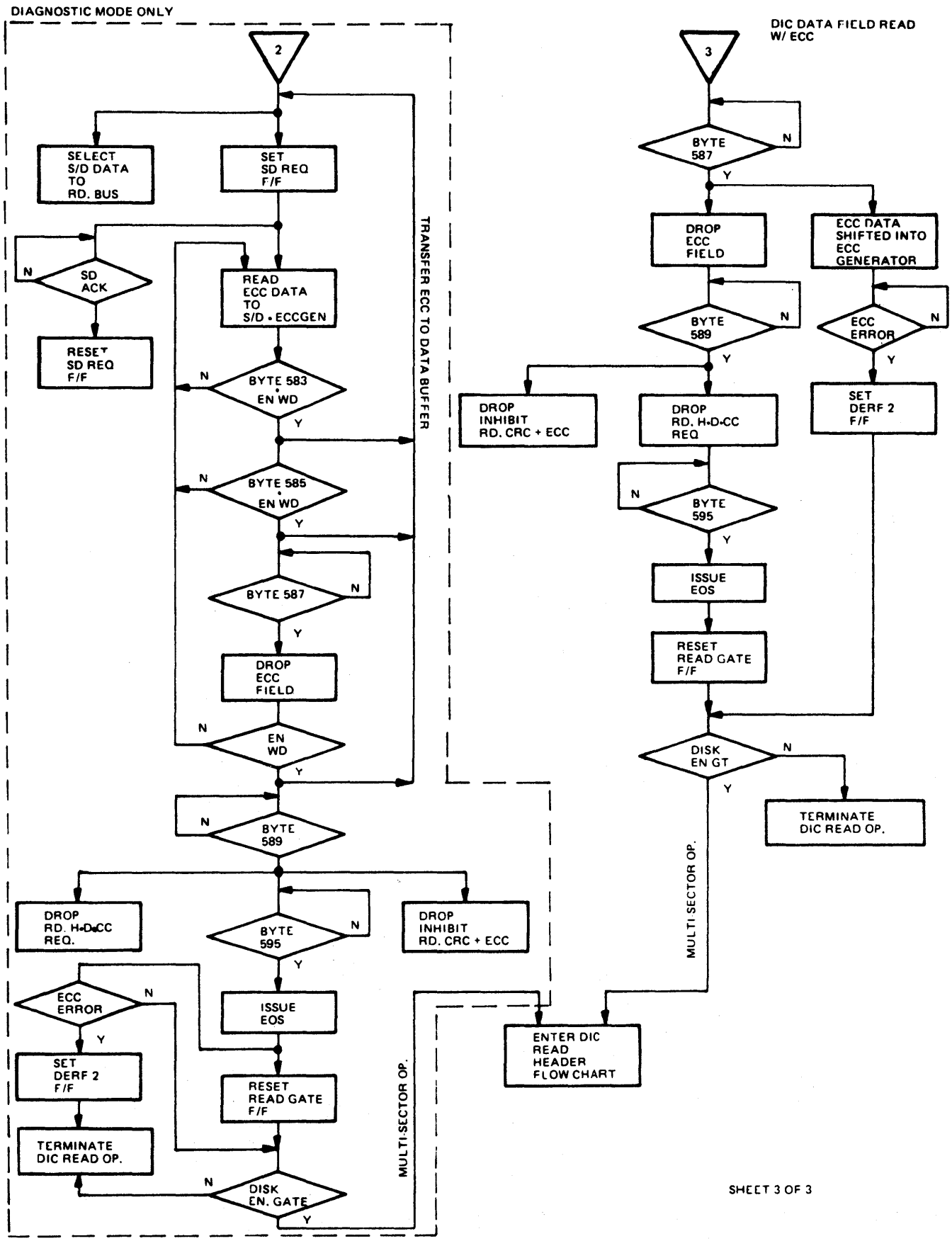
SHEET 1 OF 3

FIGURE 5-30. DISK INTERFACE CONTROL DATA FIELD READ WITH ECC FLOW CHART

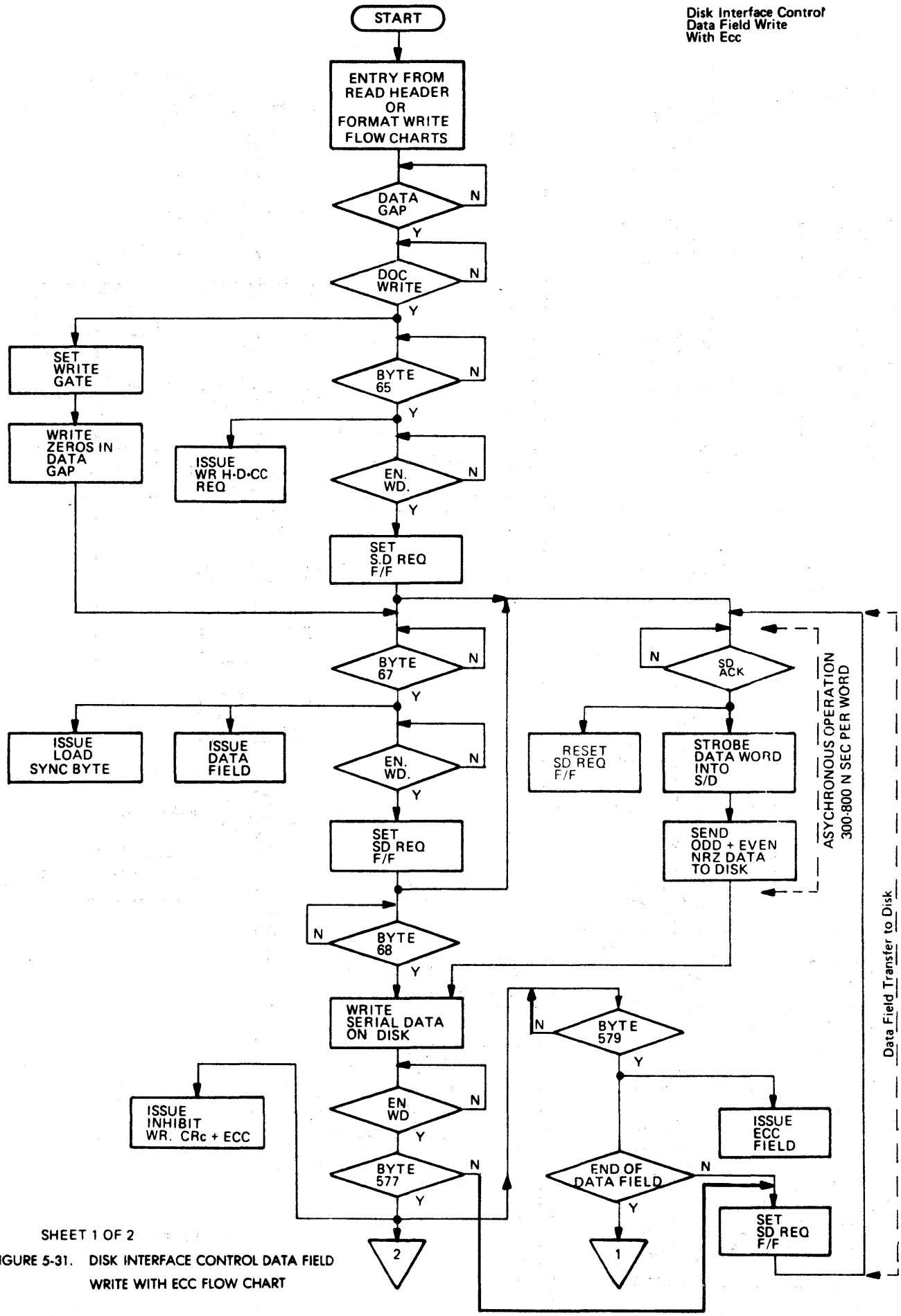
DIC DATA FIELD READ W/ ECC



SHEET 2 OF 3

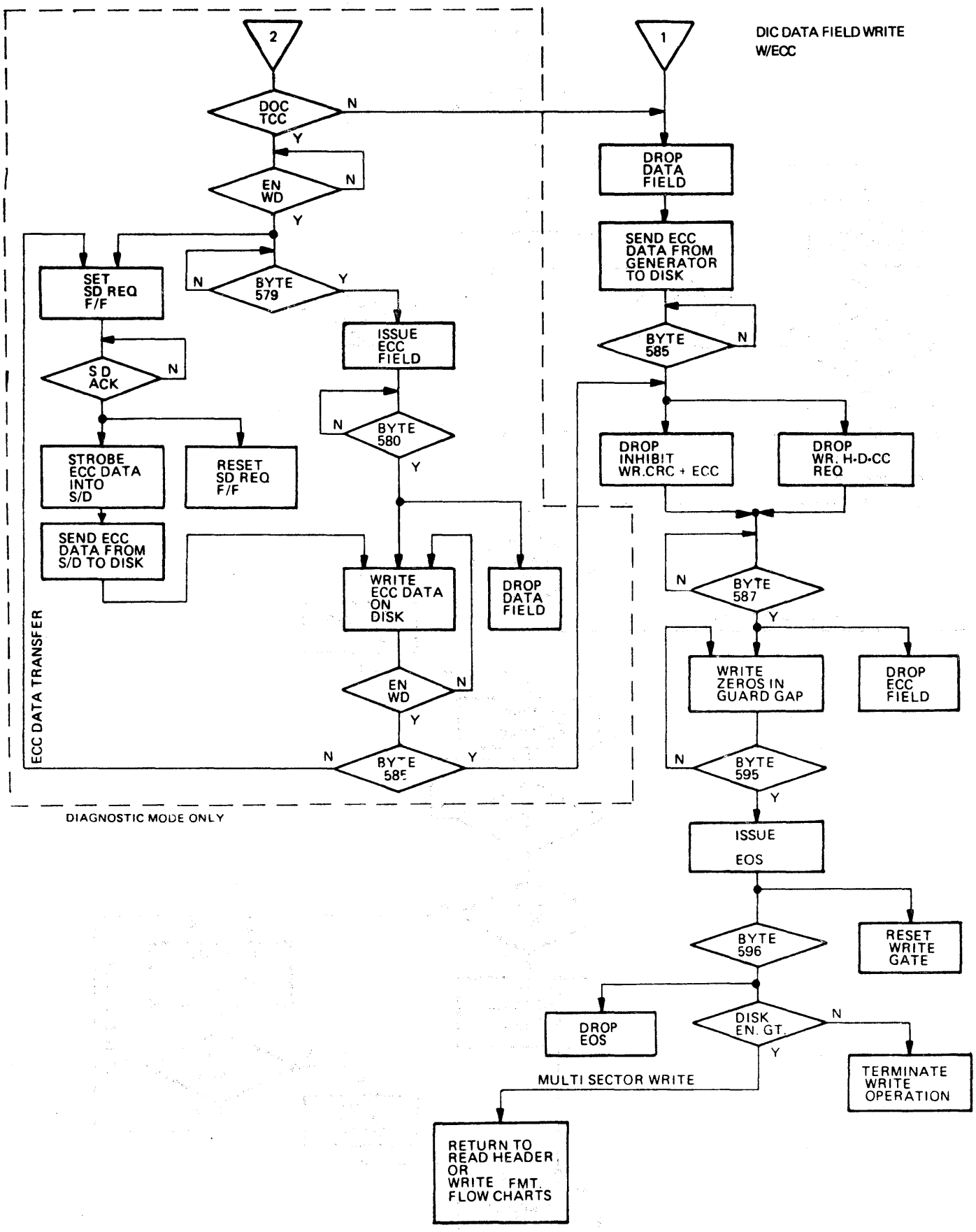

DIAGNOSTIC MODE ONLY
DIC DATA FIELD READ W/ ECC
2
3
SELECT S/D DATA TO RD. BUS
SET SD REQ F/F
SD ACK
N
RESET SD REQ F/F
READ ECC DATA TO S/D • ECCGEN
BYTE 583 • EN WD
BYTE 585 • EN WD
BYTE 587
DROP ECC FIELD
EN WD
BYTE 589
DROP RD. H-D-CC REQ.
BYTE 595
ISSUE EOS
ECC ERROR
SET DERF 2 F/F
TERMINATE DIC READ OP.
RESET READ GATE F/F
DISK EN. GATE
DROP INHIBIT RD. CRC + ECC
TRANSFER ECC TO DATA BUFFER
MULTI-SECTOR OP.
ENTER DIC READ HEADER FLOW CHART
DROP ECC FIELD
ECC DATA SHIFTED INTO ECC GENERATOR
DROP RD. H-D-CC REQ
DISK EN GT
TERMINATE DIC READ OP.
Y
N

SHEET 3 OF 3



SHEET 1 OF 2

FIGURE 5-31. DISK INTERFACE CONTROL DATA FIELD WRITE WITH ECC FLOW CHART


DIC DATA FIELD WRITE W/ECC
2
1
DOC TCC
N
Y
EN WD
N
Y
SET SD REQ F/F
N
BYTE 579
Y
S D ACK
N
STROBE ECC DATA INTO S/D
RESET SD REQ F/F
SEND ECC DATA FROM S/D TO DISK
ISSUE ECC FIELD
N
BYTE 580
Y
WRITE ECC DATA ON DISK
DROP DATA FIELD
EN WD
N
Y
N
BYTE 585
Y
ECC DATA TRANSFER
DIAGNOSTIC MODE ONLY
DROP DATA FIELD
SEND ECC DATA FROM GENERATOR TO DISK
BYTE 585
N
DROP INHIBIT WR.CRC + ECC
DROP WR. H-D-CC REQ
N
BYTE 587
Y
WRITE ZEROS IN GUARD GAP
DROP ECC FIELD
N
BYTE 595
Y
ISSUE EOS
BYTE 596
RESET WRITE GATE
DROP EOS
DISK EN. GT.
N
Y
TERMINATE WRITE OPERATION
MULTI SECTOR WRITE
RETURN TO READ HEADER OR WRITE FMT. FLOW CHARTS

SHEET 2 OF 2

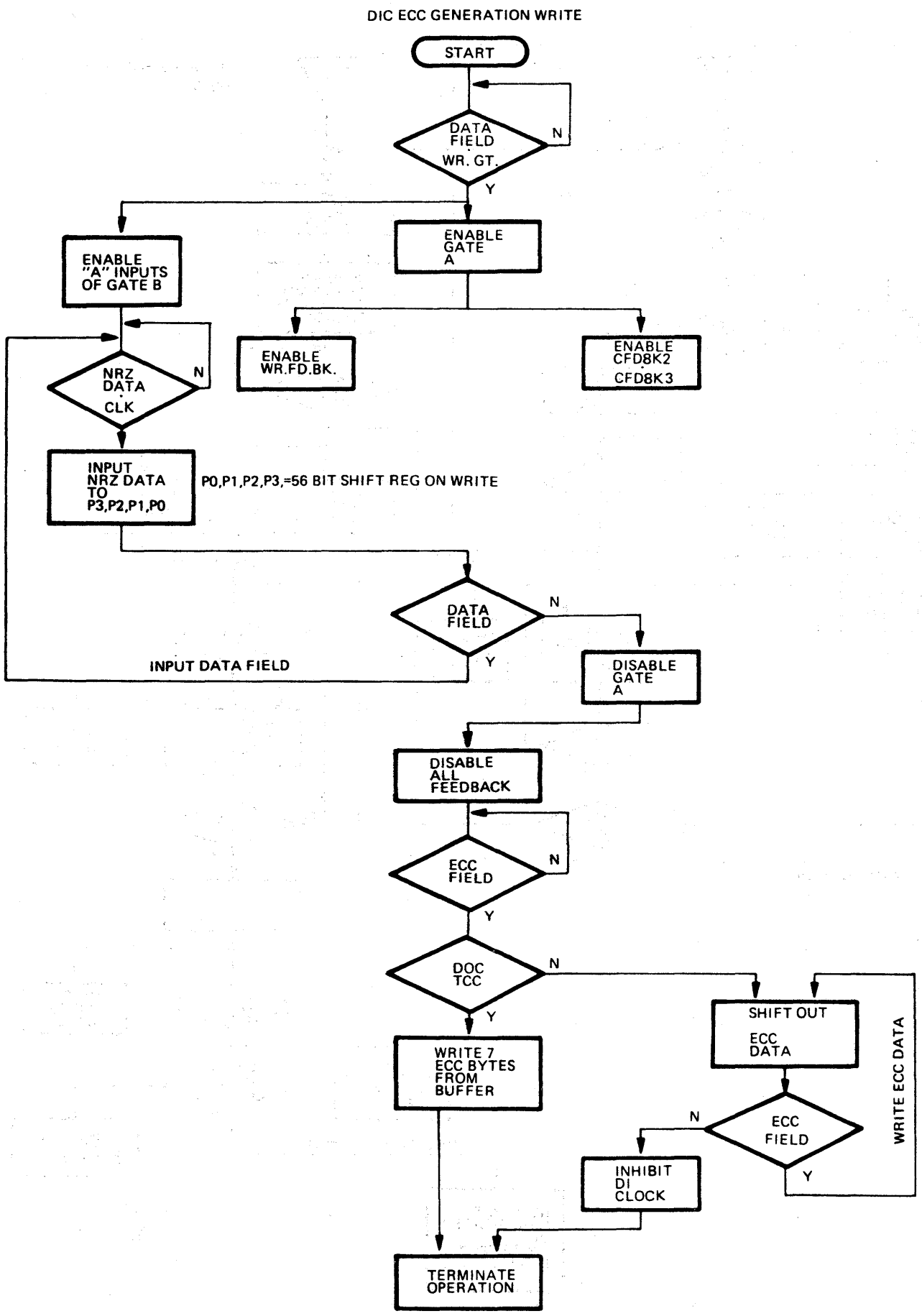


FIGURE 5-32. DISK INTERFACE CONTROL ECC GENERATION WRITE FLOW CHART

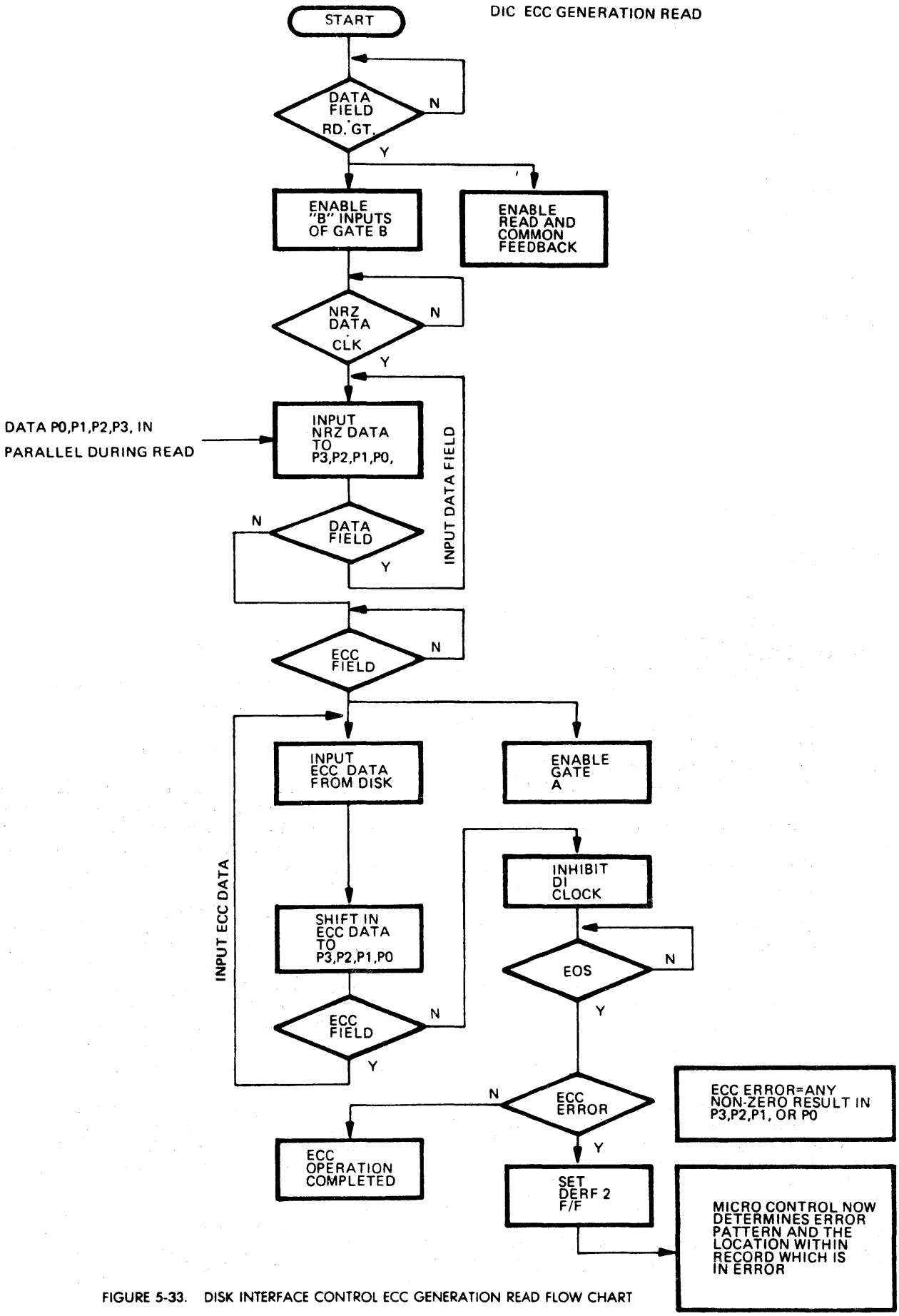
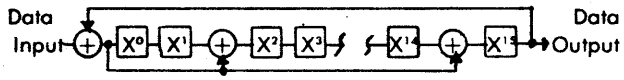


FIGURE 5-33. DISK INTERFACE CONTROL ECC GENERATION READ FLOW CHART

5-5. CRC AND ECC OPERATION.

a. Cyclic Redundancy Check. The CRC code implemented is a 16-bit polynomial, $X^{16}+X^{15}+X^2+1$. When header data is written, the serial data is divided by the polynomial. The CRC shift registers contain the remainder of this division at the end of the field being written. This 16-bit remainder is then appended to the data by altering the CRC shift registers to perform standard shifting without feedback and writing the serial CRC from bit-15, shifting out one bit at a time.

When the header field is read, the same division process takes place on the serial read data. The remainder generated in the CRC registers is then compared bit for bit with the 16-bit CRC code read in from the disk. This comparison is accomplished by shifting the serial CRC code into the registers with feedback enabled. If the registers contain all zeros at the end of 16 shifts, there is no error. If the results are non-zero, a CRC error is indicated, and the CRC Error latch is set. Implementation of the CRC is shown below:



where:

+	= Exclusive OR
□	= Flip-Flop
X^0	= CRC polynomial term "1"
X^{15}	= CRC polynomial term "X^{16}"

The CRC implemented has the following characteristics:

1. The code will check a length of 2^{15}-1 = 32767 bits or less.
2. Capable of checking single burst length of 16 or less.
3. Capable of checking any combination of two bursts with a length of 1 and 2.
4. Code will detect all single, double, and triple bit errors.

b. Error Correction Code. The Error Correction Code implemented is a 56-bit polynomial, $X^{56}+X^{55}+X^{49}+X^{45}+X^{41}+X^{39}+X^{38}+X^{37}+X^{36}+X^{31}+X^{22}+X^{19}+X^{17}+X^{16}+X^{15}+X^{14}+X^{12}+X^{11}+X^9+X+1$. The ECC is a Fire Code with high speed decode. When data is written the serial data field is divided by the generator polynomial by the ECC hardware. The remainder produced by this arithmetic process resides in the ECC shift registers at the end of the data field. The remainder is appended to the data field by disabling the feedback and shifting each bit out of the registers, writing the 56 bits of ECC from bit 55. When the data field is read the serial data is divided by the polynomial, and the ECC bytes at the end of the data field read into the shift registers, with the feedback enabled. After the last ECC bit is shifted in, the contents of the registers will be zero if no error occurred. If any shift register is non-zero, the data is in error, and the ECC Error Flag will be set. The microprocessor examines the shift registers to determine if the error is correctable or uncorrectable.

The decoding process during read is accomplished in a parallel manner by breaking the ECC polynomial into factors to allow fast computation of error displacement. The polynomial factors accept the serial read data in parallel, with each factor performing a division of the input data stream. The polynomial factors are essentially contained in four shift registers, with Exclusive OR feedback for each term; the four registers are called P0, P1, P2, and P3. All four must be zero after a read to indicate no error. The read polynomial factors are:

$$P0 = X^{22}+1$$

$$P1 = X^{11}+X^9+X^7+X^6+X^5+X^1+1$$

$$P2 = X^{12}+X^{11}+X^{10}+X^9+X^8+X^7+X^6+X^5+X^4+X^3+X^2+X^1+1$$

$$P3 = X^{11}+X^7+X^6+X^1+1$$

The ECC code implemented is capable of detecting most errors caused by 3330-11 type media. Single burst errors of 22-bits length or less will be detected. Capability for correction of single burst errors of 11-bits length or less is provided using the ECC.

1. Write Implementation. When the data field is written in a sector, the 56 bits of ECC are generated by four shift registers P0, P1, P2, and P3 with Exclusive OR feedback connected as shown in Figure 5-34. The P0 shift register is 22 bits long, P1 is 11 bits long, P2 is 12 bits long, and P3 is 11 bits long. The 56-bit ECC is physically implemented using 14 Motorola 8504 sixteen-pin DIPs. Each DIP contains 4 XORs and 4 flip-flops as well as a zero detect gate.

Serial write data is shifted through registers P3, P2, P1, and P0 with gate A enabled. When the last data bit is shifted into P3, the gate is disabled and the 56 bits of ECC are then shifted out of P0 bit-55 and written as each bit is shifted.

2. Read Implementation. When the data field is read from a sector, each serial data bit is shifted into P3, P2, P1, and P0 with gate B enabled. The shift

registers and Exclusive OR feedbacks are connected as shown in Figure 5-35. After the last ECC bit is shifted in, gate B is disabled, and all register bits checked for zero. Any shift register containing non-zero results indicates an error and the ECC Error flag is set. The microprocessor is then notified of the error condition.

3. Error Correction. Upon detection of an ECC Error, the microprocessor examines all four shift registers, P0, P1, P2, and P3. All must contain non-zero results or the error is uncorrectable.

The microprocessor then shifts P0, pattern register, using the ECC Control Register and counts the number of shifts until all non-zero bits are contained in the low order eleven bits (left most 11 in Figure 5-35) and zeros are in the high order eleven bits. The error pattern is then contained in the low order eleven bits, with each 1 bit representing a read data bit in error. If it is not possible to get the eleven high order bits zeroed in 21 shifts or less, the error is uncorrectable.

Upon completion of the P0 shifting to contain the error pattern in the low order eleven bits, P1 is then shifted while counting the number of shifts until the contents of P1 match that of P0 bit for bit in the low order eleven bits. If P1 cannot be made to match P0 (low order) in 89 shifts or less, the error is uncorrectable. If a P0, P1 match is accomplished, then P2 is shifted while counting shifts looking for a match between P0 and P2. If P2 cannot be made to match P0 (low order), in 13 shifts or less, the error is uncorrectable. If P2 matches P0, then P3 is shifted while counting shifts and looking for a match between P3 and P0 (low order). If P3 cannot be shifted to match P0 in 23 shifts or less, the error is uncorrectable. All shifting is performed with feedback enabled.

If P1, P2, and P3 all can be shifted to match the low order contents of P0, the microprocessor computes the displacement using the following formula:

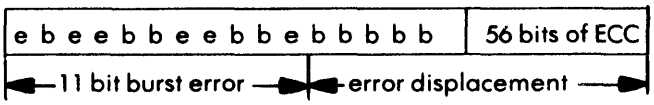
$$D = -133055\ SC_{P0} + 72358\ SC_{P1} - 270204\ SC_{P2} - 254540\ SC_{P3}$$

Where SC_{P0}, SC_{P1}, SC_{P2}, SC_{P3}, are the shifts counted for P0, P1, P2, and P3 respectively during the pattern match. The result obtained from the above, D, then has the integer 585442 added or subtracted until:

0 result 585442

Then the displacement, D = 585442 - result.

This displacement value is the number of bits from the *end* of the ECC to the first bit in error measured *from* the end of the field.



b = Data Bit OK, e = Data Bit in Error

The microprocessor then adjusts the bit displacement obtained above to a byte boundary and calculates the displacement, in bytes, to the first byte in error from the end of the data field rather than the last ECC byte. If the displacement is 0, the error lies in the ECC bytes, and if it is 1 or 2, the error may still be partially in the ECC bytes. This calculation may also be performed on the bit displacement value without adjustment to a byte boundary. If the unadjusted value is less than 56, part or all of the error is in the ECC bits. Only that portion of the "error pattern" not in the ECC bits, or pertaining to data need be used to correct the data stored in the buffer. If the displacement value, D, exceeds the length of the data field plus ECC bytes, the error is also uncorrectable. If the displacement is close to the data length plus ECC, recheck the error pattern to ensure it matches the requirement for a correctable error.

Upon conclusion of displacement calculation and obtaining the eleven bit error pattern, the microprocessor enables access to the data buffer in the Data Control. Data transfer was automatically suspended by the hardware, and remains so until ECC Error flag is reset by the microprocessor. The location(s) in the data buffer which are in error as indicated by the displacement are then exclusive ORed with the "error pattern"; eleven bit pattern plus 5 zeros to complete one word (2 eight-bit bytes). The results are stored in the buffer locations in error, thus correcting each bit in error as indicated by a "1" in the data pattern and leaving any bits where a "0" was indicated unchanged.

The microprocessor then re-enables the data transfer between the computer and disk and the data transfer resumes. If an ECC Error is found to be uncorrectable, appropriate status is posted and the operation terminated.

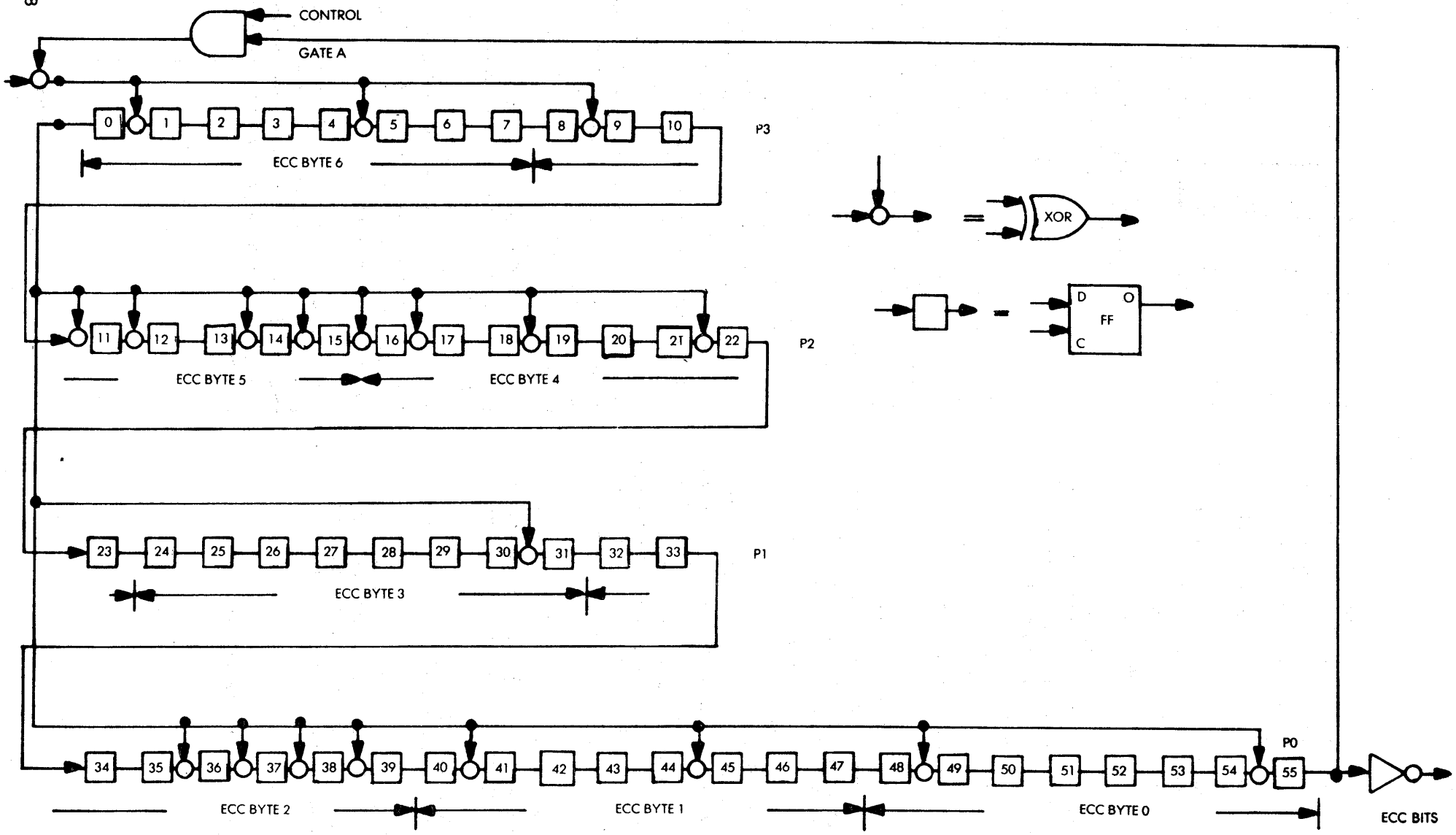


Figure 5-34. ECC Hardware During Write Operation

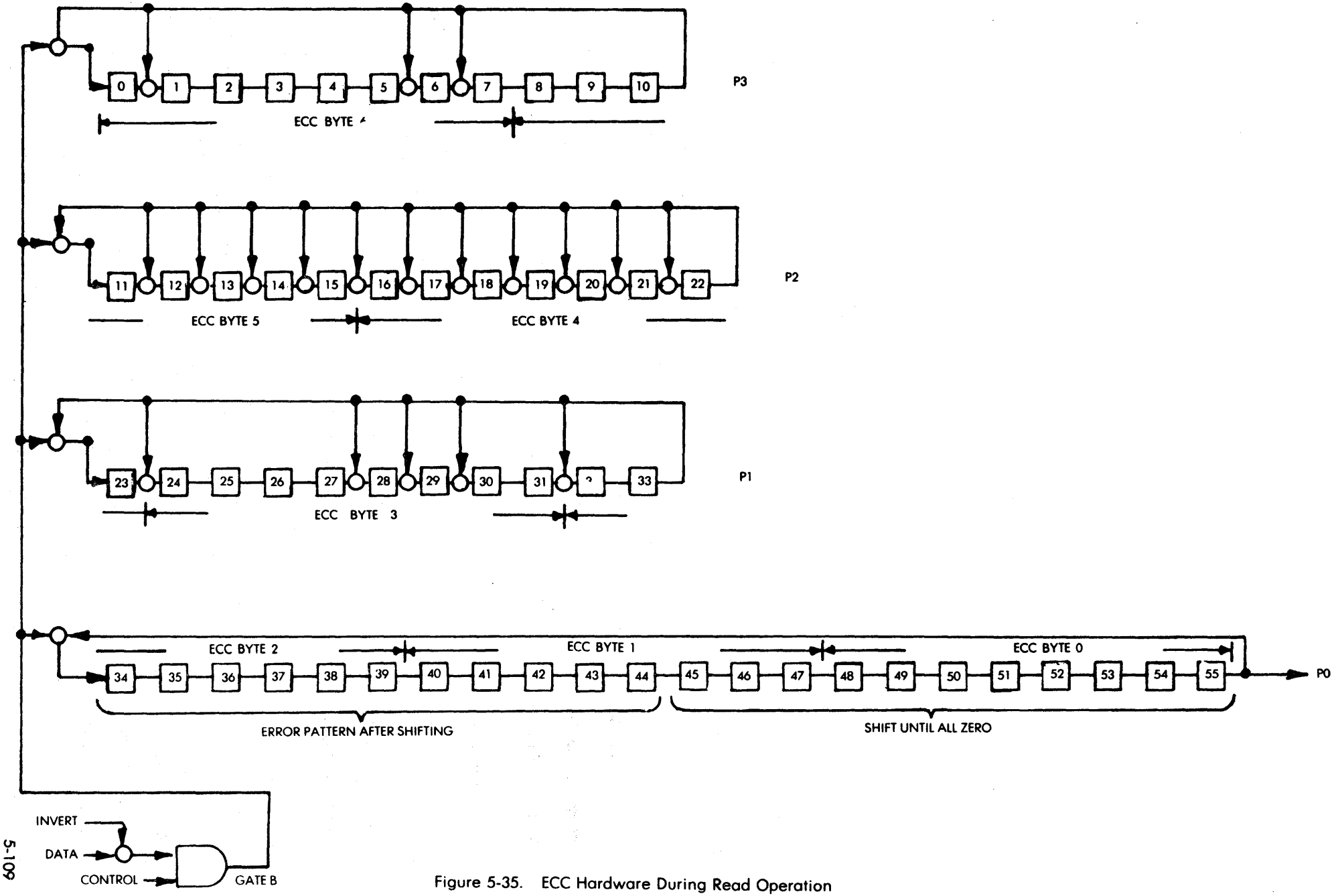


Figure 5-35. ECC Hardware During Read Operation

Disk Interface Output Registers

1. Select Port and Drive

07	06	05	04	03	02	01	00
-	P_2	P_1	0	0	D_4	D_2	D_1

BIT	NAME	FUNCTION
07	Not Used	N/A
06-05	P_2-P_1	Disk Port Select

P_2	P_1	Port
0	0	0
0	1	1
1	0	2
1	1	3

04-03	Not Used	Always 0.
02-00	D_4-D_1	Disk Drive Select 0-7.

2. Cylinder High

07	06	05	04	03	02	01	00
-	-	-	-	-	-	C_{512}	C_{256}

BIT	NAME	FUNCTION
07-02	Not Used	N/A
01-00	C_{512}-C_{256}	High order cylinder address bits.

3. Cylinder Low.

07	06	05	04	03	02	01	00
C_{128}	C_{64}	C_{32}	C_{16}	C_8	C_4	C_2	C_1

BIT	NAME	FUNCTION
07-00	C_{128}-C_1	Low order cylinder address bits.

4. Head

07	06	05	04	03	02	01	00
-	-	-	H_{16}	H_8	H_4	H_2	H_1

BIT	NAME	FUNCTION
07-05	Not Used	N/A
04-00	H_{16}-H_1	Head Select bits.

5. Control

07	06	05	04	03	02	01	00
RLS	RTZ	-	FC	S−	S+	DSL	DSE

BIT	NAME	FUNCTION
07	Release	Used only for Dual Channel Drives. Resets the Reserve and Disable flip-flops for both channels, releasing the Reserve and Priority Select commands.
06	RTZ Seek	Causes actuator to seek to track zero, clears seek error latch and head address register.
05	Not Used	N/A
04	Fault Clear	Clears fault latch if fault condition no longer exists.
03	Servo Offset−	Offsets actuator from nominal on cylinder position, away from spindle.
02	Servo Offset+	Offset actuator from nominal on cylinder position, toward spindle.
01	Data Strobe Late	Enables the PLO data separator to strobe the data at a time later than optimum.
00	Data Strobe Early	Enables the PLO data separator to strobe the data at a time earlier than optimum.

Disk Interface Input Registers

1. Status Byte

07	06	05	04	03	02	01	00
ATN	DPB	SKE	0	WP	FLT	AB	RDY

BIT	NAME	FUNCTION
07	ATTENTION	Set by drive to inform controller that status needs to be checked.
06	Dual Port Busy	Enabled on a dual channel drive when a unit selection is attempted and the drive is already reserved by the other controller.
05	Seek Error	Set when drive is unable to complete a seek within 500 ms, or the carriage has moved to a position outside the recording field. Also occurs if an address greater than 410 (40 Mb - 9760), or 822 (80 Mb - 9762 and 300 Mb - 9766) has been selected.
04	Not Used	Always 0
03	Write Protect	Set when drive write circuits are disabled by a fault, setting Write Protect on the drive front panel, or during head alignment.

Disk Interface Input Registers (Continued)

BIT	NAME	FUNCTION
02	Fault	Set by one of the following faults; DC Power, Write, Write or Read while off cylinder, and Write Gate during a Read operation.
01	Access Busy	
00	Ready	Set when drive is selected, up to speed, heads are loaded, and no fault exists.

2. Sector Counter Byte

07	06	05	04	03	02	01	00
S_{128}	S_{64}	S_{32}	S_{16}	S_8	S_4	S_2	S_1

BIT	NAME	FUNCTION
07-00	S_{128}-S_1	Drive Sector Count.

3. Model Byte

07	06	05	04	03	02	01	00
CDC	0	0	0	FH	M_4	M_2	M_1

BIT	NAME	FUNCTION
07	CDC	Always a 1 if CDC drive is installed.
06-04	Not Used	Always zero.
03	Fixed Head	Always a zero.
02-00	Model $_{4-1}$	

M_4	M_2	M_1	Drive
0	0	0	9760
0	0	1	9762
0	1	0	9764
0	1	1	9766
1	0	0	Not Used
1	0	1	Not Used
1	1	0	Not Used
1	1	1	Not Used

CHAPTER 6
OPTION FEATURES

6-1. **INTRODUCTION.** This chapter contains a description of options and upgrade kits available for the standard 9400 Disk Controller System.

6-2.

CHAPTER 7
PERIODIC MAINTENANCE

7-1. **INTRODUCTION.** This chapter describes the maintenance procedures to be performed on a regularly scheduled basis. Instructions are provided for preventive maintenance including cleaning and inspection. For maintenance requirements of the Storage Module Drives, refer to the appropriate CDC manual as listed in Table 1-2.

7-2. **SAFETY PRECAUTIONS.** High voltage is used in the operation of this system. Before working inside the equipment, turn off the AC circuit breakers for the Controller and disconnect the AC power cord.

7-3. **SCHEDULED MAINTENANCE ACTIONS.** Required scheduled maintenance actions are listed in Table 7-1.

a. Cables and Wiring. Check cables and wiring for the following:

1. Frayed, burned, or damaged insulation.
2. Connectors tight and secure.
3. Loose ties or clamps.

b. Front and Rear Panels. Check equipment panels for the following:

1. Loose controls or indicators.
2. Illegible markings.
3. Burned out indicators.
4. Broken controls or mounting hardware.
5. Improper alignment of controls.

Table 7-1. Scheduled Maintenance Actions

Periodicity	Maintenance Action	Reference Paragraph
Semiannually	Cleaning	7-4
Semiannually	Inspection	7-5
As Required	Lubrication	7-6

7-4. **CLEANING.** Accumulated dust should be blown out of equipment with dry air, or a bellows. Dust that adheres to equipment can be wiped away with a soft cloth. The air filter should be removed, washed in soapy water, dried, and replaced. The front panel may be cleaned with a soft lint-free cloth and isopropyl alcohol.

7-5. **INSPECTION.** A physical inspection of the system should be made semiannually, to check for conditions that could result in equipment failure. Inspection consists of a visual examination of both the interior and exterior of the system and interconnecting cables.

c. Equipment Enclosures and Slides. Check equipment enclosures and slides for the following:

1. Blocked air inlet or louvers.
2. Binding of slides.
3. Loose hardware.
4. Loose circuit card assemblies.
5. Overheated components.
6. Damaged wiring and loose connectors.

7-6. **LUBRICATION.** The system contains no points that require regular scheduled lubrication. If the enclosure slides bind, lubricate with a medium weight synthetic based oil or light weight synthetic based grease as required.

CHAPTER 9
PARTS LISTS

9-1. **INTRODUCTION.** This chapter contains illustrations and parts lists for mechanical parts and electrical subassemblies. Parts breakdowns are given to the major, field replaceable subassembly level only.

9-2. **PARTS LISTS.** The parts lists present a breakdown of all intermediate level replaceable items, listed in disassembly sequence (when disassembly sequence is significant). The parts lists present information under the following column headings:

FIGURE AND INDEX NUMBER

PART NUMBER

DESCRIPTION

UNITS PER ASSEMBLY

NOTES

a. Figure and Index Number. This column identifies the figure which illustrates each listed item, and the index number which identifies the item on the illustration.

b. Part Number. This column provides the System Industries part number of each item listed in the parts lists.

c. Description. This column lists all intermediate level replaceable items within the equipment in disassembly sequence (where applicable). An indented column arrangement is utilized to show the relationship between a part and that part's next higher assembly. The top assembly of each listing appears in indention 1. Primary subassemblies and their attaching parts appear in indention 2.

d. Units Per Assembly. The quantity shown in this column reflects the total quantity of a part required by that part's next higher assembly. This quantity is not necessarily the total used for the complete equipment. Some bulk materials are called out by length and are so identified in the column. The abbreviation REF is used to indicate that the quantity of an item used per assembly is listed in the next higher assembly.

e. Notes. Comments in this column note obsoleted and newly released parts. Not all newly released parts can be used to replace older parts, without making other concurrent changes to a controller. For information regarding parts compatibility, contact System Industries in Sunnyvale, California. Telephone (408) 732-1650 and ask for Customer Service.

Parts Lists

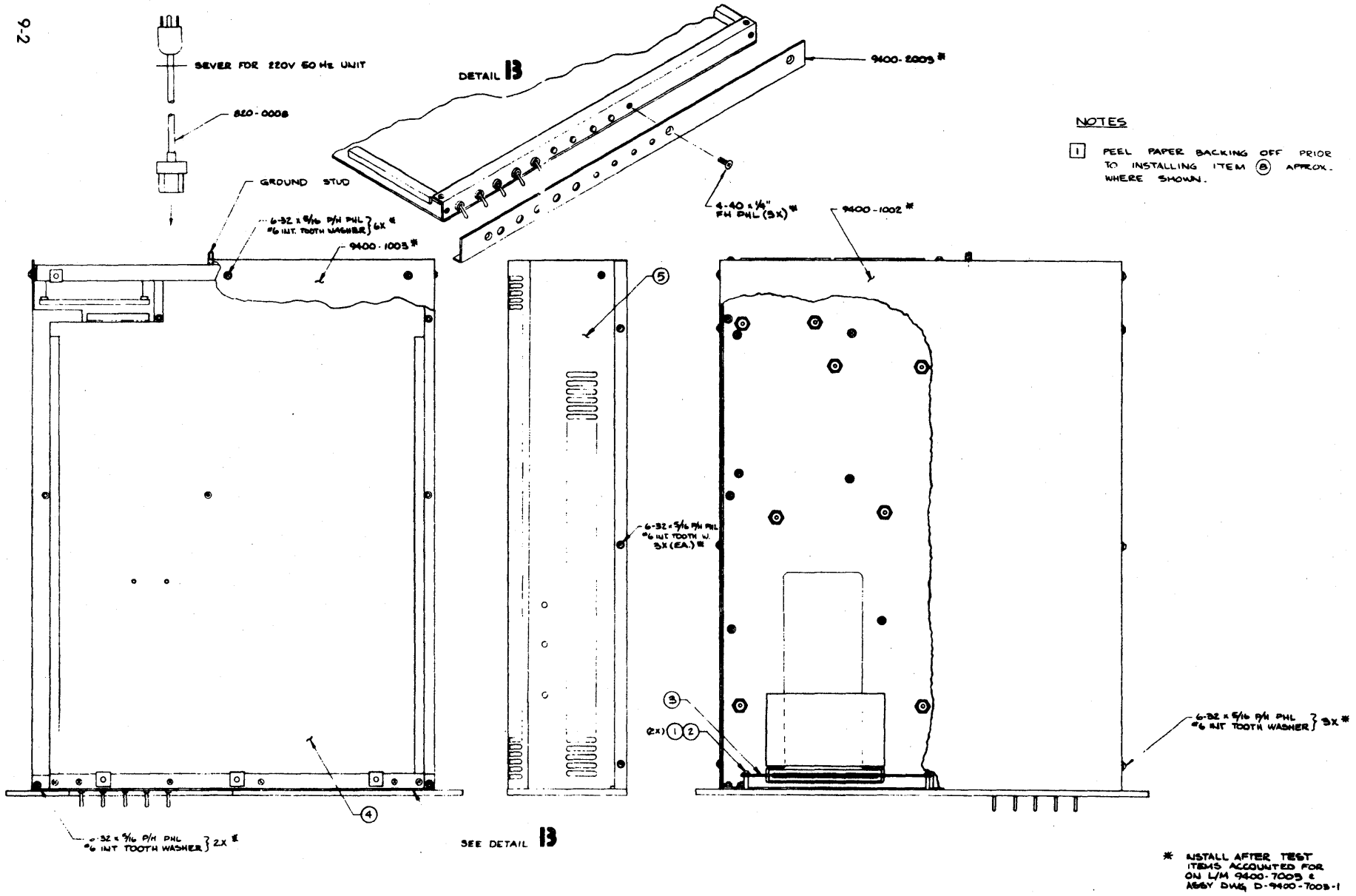


Figure 9-1. Mainframe and Basic Controller Assembly

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-1	9410-7100	Mainframe and Basic Controller	REF	
- 1	506-0013	• Screw, Machine, 6-32 ½ PH PHL	2	
- 2	550-0002	• Lockwasher, #6 Internal Tooth	2	
- 3	9400-6002	• PCB Assy, Control Store	1	
- 4	9400-6004-01	• PCB Assy, Basic Control, RP04	1	
- 4	9400-6004-02	• PCB Assy, Basic Control, RM03	1	
- 4	9400-6014-01	• PCB Assy, Basic Control, RP04, 2 MHz	1	Replaces 9400-6004
- 4	9400-6014-02	• PCB Assy, Basic Control, RM03, 2 MHz	1	Replaces 9400-6004
- 5	9400-7003	• Base Assy	1	Fig. 9-2

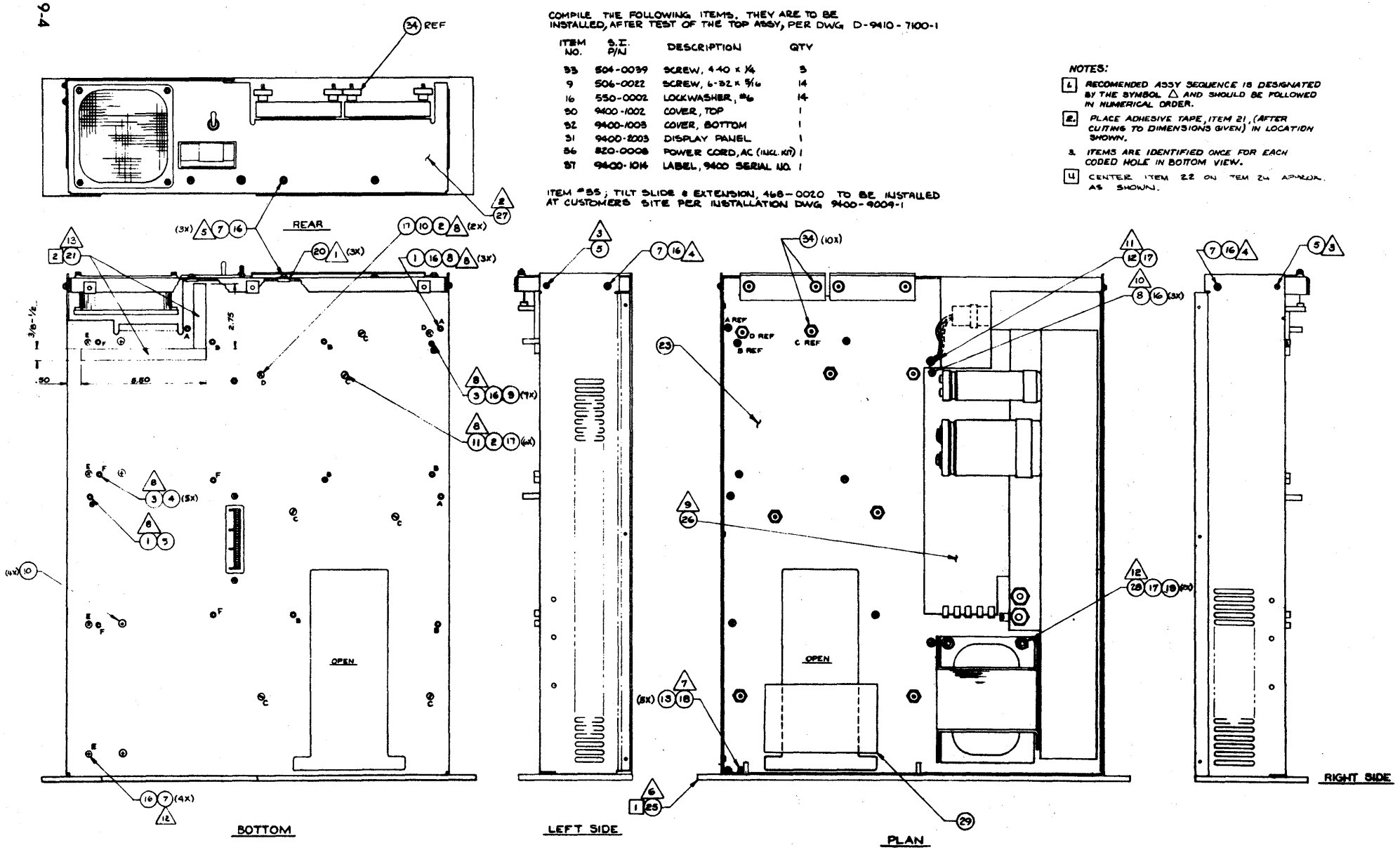
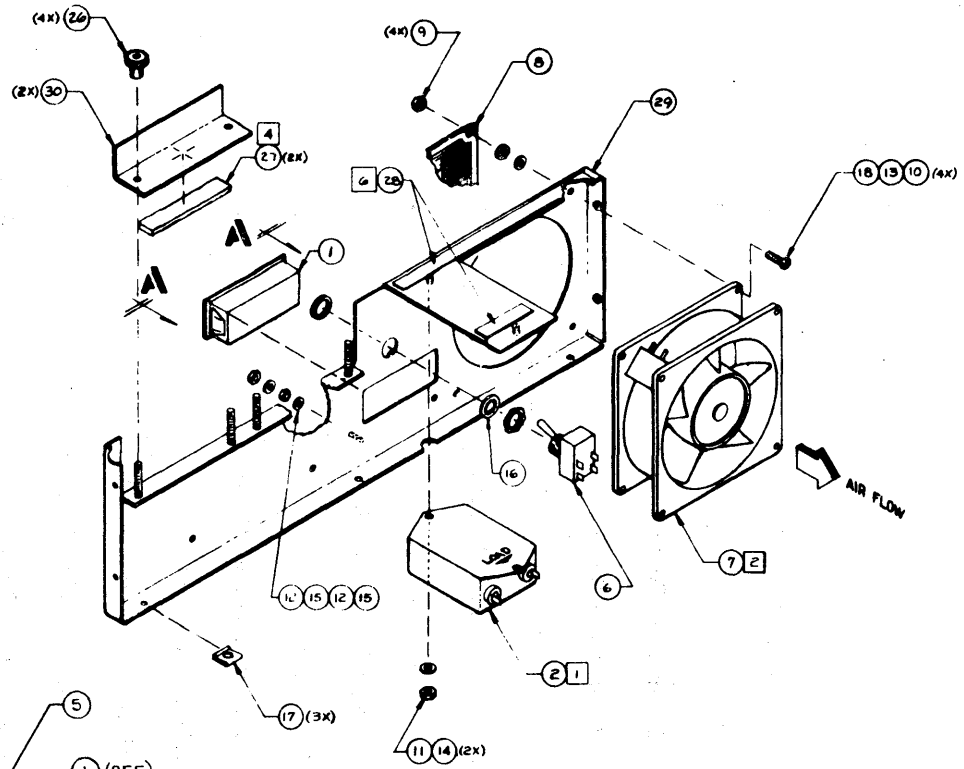
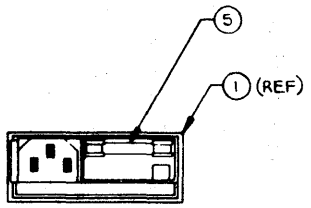


Figure 9-2. Base Assembly

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-2	9400-7003	BASE Assy	REF	
- 1	318-0023	• Standoff, ¼ Dia. ¾ Long, 6-32	4	
- 2	318-0024	• Standoff, ½ Dia. ⅜ Long, 8-32 Hex	8	
- 3	318-0025	• Standoff, ¼ Dia. ¼ Long, 6-32 INS	12	
- 4	506-0008	• Screw, Machine, 6-32 ¼ FH PHL	5	
- 5	506-0009	• Screw, Machine, 6-32 ⅜ FH PHL	3	
- 7	506-0012	• Screw, Machine, 6-32 ⅜ PH PHL	9	
- 8	506-0013	• Screw, Machine, 6-32 ½ PH PHL	6	
- 9	506-0022	• Screw, Machine, 6-32 6/16 PH PHL	21	
- 10	508-0008	• Screw, Machine, 8-32 ½ PH PHL	6	
- 11	508-0018	• Screw, Machine, 8-32×3 ½ RND HD	6	
- 12	528-0001	• Nut, Hex, ⅛, 0.338 Thick	1	
- 13	530-0001	• Nut, Hex, ⅛ 0.365 Thick	5	
- 16	550-0002	• Lockwasher #6 Internal Tooth	36	
- 17	550-0003	• Lockwasher #8 Internal Tooth	11	
- 18	550-0004	• Lockwasher #10 Internal Tooth	5	
- 19	555-0003	• Washer, #8 Flat, Stainless Steel	2	
- 20	560-0002	• Clip, SHET 6-32, 0.081-0.072 Thick	3	
- 21	620-0014	• Tape, Adhesive Foam, ¼ Thick ⅜ Wide	8.25-in.	
- 23	9400-1001	• Base	1	
- 25	9400-2002	• Front Panel	1	
- 26	9400-7005	• Power Supply Assy.	1	
- 27	9400-7004	• Rear Panel Assy.	1	Fig. 9-3
- 28	508-0007	• Screw, Machine, 8-32 ⅜ PH PHL	2	
- 29	9400-3001	• Insulator, PCB	1	
- 30	9400-1002	• Top Cover	1	
- 31	9400-2003	• Display Panel	1	

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-2	9400-7003	Base Assy (Continued)	REF	
- 32	9400-1003	• Rear Panel	1	
- 33	504-0034	• Screw, Machine, 4-40 ¼ FH PHL	3	
- 34	532-0001	• Nut, $^{5}/_{8}$ RND HD Thumb Nut, 8-32 THRU	10	
- 35	468-0020	• Slides, Rack Mount, 90° Tilt Lock	1	
- 36	820-0008	• Cable, Power Cord	1	
- 37	9400-1014	• Label, 9400 Serial No.	1	

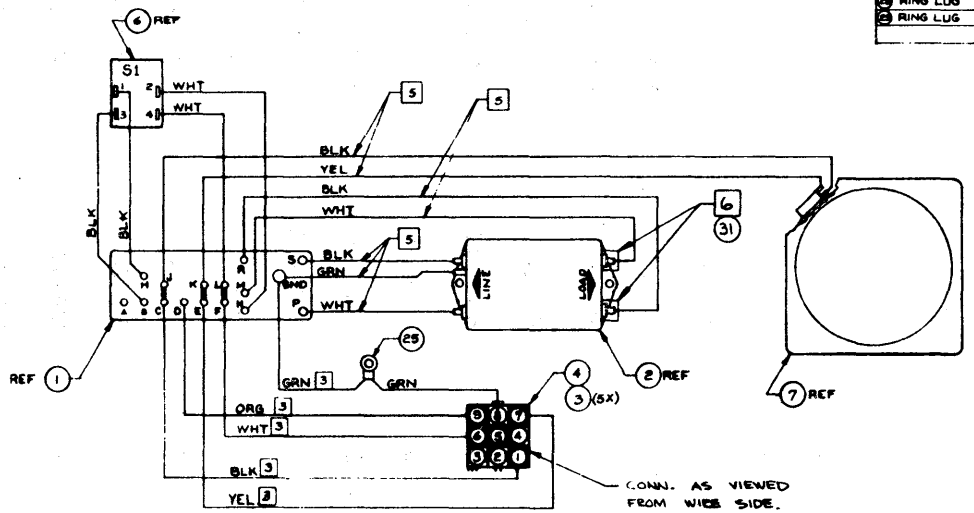




VIEW A-A

SCALE 1:1

FROM ITEM/DISCRIP.	TO ITEM/DISCRIP.	WIRE [6] LENGTH	COLOR
(6) S1-1	(1) A.C. MOD-H	3.5	BLK
(6) S1-3	(1) -B	3.5	BLK
(6) S1-2	(1) -N	3.5	WHT
(6) S1-4	(1) -L	3.5	WHT
(7) FAN	(1) -J	6.5	BLK
(7) FAN	(1) -K	6.5	YEL
(2) LINE FILTER	(1) -M	8.0	WHT
(2)	(1) -R	6.0	BLK
(2)	(1) -S	6.0	BLK
(2)	(1) -P	5.0	WHT
(2) LINE FILTER	(1) -GND	6.0	GRN
(4) CONN-1	(1) -C	4.5	BLK
(4) CONN-9	(1) -D	4.5	ORG
(4) CONN-7	(1) -E	4.5	YEL
(4) CONN-6	(1) -F	4.8	WHT
(25) RING LUG	(1) A.C. MOD-GND	5.0	GRN
(25) RING LUG	(4) CONN-5	1.6	GRN



NOTES:

1. SOLDER 18 GA. WIRES TO ITEM (2) BEFORE INSTALLING. INSTALL ITEM (2) TO ITEM 26 BEFORE INSTALLING ITEMS (6)(7) OR (1).
2. SOLDER 18 GA. WIRES TO ITEM (7) BEFORE INSTALLING ON ITEM (8).
3. COVER 18 GA. WIRES WITH 2.5 INCHES OF ITEM (13).
4. CENTER 3" OF ITEM (27), CENTERING IT BETWEEN HOLES IN ITEM (30). PRESS IN APPROX LOCATION SHOWN.
5. TWIST WIRES APPROX 1 TURN PER INCH.
6. SHRINK FIT 1" OF ITEM (31) OVER TERMINALS.

Figure 9-3. Rear Panel Assembly

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-3	9400-7004	Rear Panel Assy.	REF	
- 1	312-0034	• Connector, 3-pole, Line Outlet with Voltage Selector	1	
- 2	312-0035	• Line Filter, Power Input	1	
- 3	314-0010	• Connector Pin, Female for 1991 Series	5	
- 4	335-0025	• Connector, Molex, Female W/O Ears, 9-pin	1	
- 5	344-0018	• Fuse, MDA8, 8 A 250 V, Slo-Blo	1	
- 6	350-0002	• Switch, Toggle, DPST, 125 V 15 A/250 V 10 A	1	
- 7	370-0002	• Fan, 110 V, 20 W, 50-60 Hz	1	
- 8	370-0005	• Filter, Fan	1	
- 9	526-0001	• Nut, Hex, 6-32, $^5/_{16}$, 0.0110 Thick	4	
- 10	526-0002	• Nut, Hex, 6-32, $^3/_{32}$, 0.145 Thick	4	
- 11	528-0001	• Nut, Hex, 8-32, $^1/_8$, 0.338 Thick	2	
- 12	530-0001	• Nut, Hex, 10-31, $^1/_8$, 0.365 Thick	2	
- 13	550-0002	• Lockwasher, #6, Internal Tooth	4	
- 14	550-0003	• Lockwasher, #8, Internal Tooth	2	
- 15	550-0004	• Lockwasher, #10, Internal Tooth, Stainless Steel	2	
- 16	550-0021	• Lockwasher, ½-inch, Internal Tooth	1	
- 17	560-0013	• Clip, Shet, 6-32, $^4/_{64}$ Thick	3	
- 18	506-0015	• Screw, Machine, 6-32, ¾ PH PHL	4	
- 19	580-0014	• Sleeve, PVC, $^5/_{16}$ Black	2.5-in.	
- 20	808-0044	• Insulation, 18 Gauge, White PVC 105	24.5-in.	
- 21	808-0047	• Wire, 18 AWG UL, 1015 Orange	4.5-in.	
- 22	808-0041	• Insulation, 19 Gauge, Green PVC 105	12.5-in.	
- 23	808-0042	• Insulation, 18 Gauge, Yellow PVC 105	11-in.	
- 24	808-0043	• Wire, 19 AWG UL, 1015 Black	30-in.	
- 25	312-0038	• Terminal, Ring Crimp, 12-10 GA #8	1	
- 26	532-0001	• Nut, $^5/_8$, RND HD Thumb Nut, 8-32 THRU	4	

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-3	9400-7004	Rear Panel Assy. (Continued)	REF	
- 27	620-0005	• Tape, Foam, ¾ - ¼	6-in.	
- 28	620-0017	• Tape, Adhesive, Foam	8-in.	
- 29	9400-1004	• Rear Panel	1	
- 30	9400-1006	• Cable Clamp	2	
- 31	580-0016	• Tubing, Shrink, ¼ White	2-in.	

TO BE SUPPLIED

Figure 9-4. Computer Interface Feature

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-4	9420-7200	Computer Interface	REF	
- 1	9400-6007	• PCB Assy, Computer Interface	1	

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-4	9420-7201	Computer Interface, RP04 10'	REF	
- 1	9400-6007	• PCB Assy, Computer Interface	1	
- 2	9400-6011-01	• PCB Assy, 9400 RP04 CPA	1	
- 2	9300-6031-01	• PCB Assy, 9400 RP04 CPA, with Cache Interface	1	replaces 9400-6011
- 3	9400-7007	• Cable Assy, CPU Interface 10-foot	2	

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-4	9420-7202	Computer Interface, RP04 20'(Obsolete)	REF	
- 1	9400-6007	• PCB Assy, Computer Interface	1	
- 2	9400-6011-01	• PCB Assy, 9400 RP04 CPA	1	
- 2	9400-6031-01	• PCB Assy, 9400 RP04 CPA, with Cache Interface	1	replaces 9400-6011
- 3	9400-7008	• Cable Assy, CPU Interface 20-foot	2	

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-4	9420-7205	Computer Interface, RP04 35'	REF	
- 1	9400-6007	• PCB Assy, Computer Interface	1	
- 2	9400-6011-01	• PCB Assy, 9400 RP04 CPA	—	
- 2	9400-6031-01	• PCB Assy, 9400 RP04 CPA, with Cache I/F	1	Replaces 9400-6001
- 3	9400-7013	• Cable Assy, CPU Interface, 35'	2	

TO BE SUPPLIED

Figure 9-5. 9400 Configuration Feature

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-5	9432-7001	9400 RP04 Configuration Feature #1	REF	
- 1	9432-8901A	• PROM, EFPGO Configuration #1 Single CPU	1	V1.3
- 1	9432-8901B	• PROM, EFPGO Configuration #1, Dual CPU	1	V1.5
- 1	9432-8901C	• PROM, EFPGO Configuration #1, Dual CPU	1	V1.6
- 1	9432-8901D	• PROM, EFPGO Configuration #1, Dual CPU	1	V2.0
- 2	9400-6002	• PCB Assy, Control Store	REF	9-1

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-5	9432-7007	9400 RP04 Configuration Feature #7	REF	
- 1	9432-8907A	• PROM, EFPGO Configuration #7, Single CPU	1	
- 1	9432-8901B	• PROM, EFPGO Configuration #7, Dual CPU	1	V1.5
- 1	9432-8901C	• PROM, EFPGO Configuration #7, Dual CPU	1	V1.6 V1.7
- 1	9432-8901D	• PROM, EFPGO Configuration #7, Dual CPU	1	V2.0
- 2	9400-6002	• PCB Assy, Control Store	REF	9-1

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-5	9432-7010	9400 RM03 Configuration Feature	REF	
- 1	9432-8904A	• PROM, RM03 Configuration	1	V1.1 V1.2
- 1	9432-8904B	• PROM, RM03 Configuration	1	V1.3

TO BE SUPPLIED

Figure 9-6. CDC Radial Drive Interface Feature

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-6	9450-7100	Feature I, CDC Radial Drive I/F	REF	
- 1	3225-7007	• Cable Assy, SMD A, 16-foot, Flat	1	Flat Cable Drive
- 1	3225-7034	• Cable Assy, SMD A, Flat to Round SMD, 16-foot	1	Rnd. Cable Drive
- 2	3225-7008	• Cable Assy, SMD B, 16-foot, Flat	1	Flat Cable Drive
- 2	3225-7035	• Cable Assy, SMD B, Flat to Round SMD, 16-foot	1	Rnd. Cable Drive
- 3	9400-6008	• PCB Assy, CDC Interface, Radial, Flat Cable	1	
- 3	9400-6028	• PCB Assy, CDC Interface, Radial, Flat & Round Cable	1	replaces 9400-6008

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-6	9450-7101	Feature II, CDC Radial Drive I/F	REF	
- 1	3225-7009	• Cable Assy, SMD A, 32-foot, Flat	1	Flat Cable Drive
- 1	3225-7036	• Cable Assy, SMD A, Flat to Round SMD, 30-foot	1	Rnd. Cable Drive
- 2	3225-7010	• Cable Assy, SMD B, 32-foot, Flat	1	Flat Cable Drive
- 2	3225-7037	• Cable Assy, SMD B, Flat to Round SMD, 30-foot	1	Rnd. Cable Drive
- 3	9400-6008	• PCB Assy, CDC Interface, Radial, Flat Cable	1	
- 3	9400-6028	• PCB Assy, CDC Interface, Radial, Flat & Round Cable	1	replaces 9400-6008

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-6	9450-7102	Feature III, CDC Radial Drive I/F	REF	
- 1	3225-7011	• Cable Assy, SMD A, 48-foot, Flat	1	Flat Cable Drive
- 1	3225-7038	• Cable Assy, SMD A, Flat to Round SMD, 50-foot	1	Rnd. Cable Drive
- 2	3225-7012	• Cable Assy, SMD B, 48-foot, Flat	1	Flat Cable Drive
- 2	3225-7039	• Cable Assy, SMD B, Flat to Round SMD, 50-foot	1	Rnd. Cable Drive
- 3	9400-6008	• PCB Assy, CDC Interface, Radial, Flat Cable	1	
- 3	9400-6028	• PCB Assy, CDC Interface, Radial, Flat & Round Cable	1	replaces 9400-6008

TO BE SUPPLIED

Figure 9-7. Cache Interface Feature

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-7	9420-7203	Cache Interface Feature, 10-foot	REF	
- 1	9400-6101	• PCB Assy, Address and Control	1	
- 2	9400-6102	• PCB Assy, Control Buffer	1	
- 3	9400-6103	• PCB Assy, Data	1	
- 4	9400-6007	• PCB Assy, Computer Interface	1	
- 5	9400-6021-01	• PCB Assy, 9400 RP04 CPA	1	
- 5	9400-6021-02	• PCB Assy, 9400 RM03 CPA	1	
- 5	9400-6031-01	• PCB Assy, 9400 RP04 CPA	1	Replaces 9400-6021
- 5	9400-6031-02	• PCB Assy, 9400 RM03 CPA	1	Replaces 9400-6021
- 6	9400-7010	• Cable Assy, Address and Control	1	
- 7	9400-7011	• Cable Assy, Data, 10-foot	1	
- 8	9400-7007	• Cable Assy, CPU Interface	2	

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-7	9420-7204	Cache Interface Feature 20-foot (Obsolete)	REF	
- 1	9400-6101	• PCB Assy, Address and Control	1	
- 2	9400-6102	• PCB Assy, Control Buffer	1	
- 3	9400-6103	• PCB Assy, Data	1	
- 4	9400-6007	• PCB Assy, Computer Interface	1	
- 5	9400-6021-01	• PCB Assy, 9400 RP04 CPA	1	
- 5	9400-6021-02	• PCB Assy, 9400 RM03 CPA	1	
- 5	9400-6031-01	• PCB Assy, 9400 RP04 CPA	1	Replaces 9400-6021
- 5	9400-6031-02	• PCB Assy, 9400 RM03 CPA	1	Replaces 9400-6021
- 6	9400-7010	• Cable Assy, Address and Control	1	
- 7	9400-7012	• Cable Assy, Data, 20-foot	1	
- 8	9400-7008	• Cable Assy, CPU Interface	2	

FIG & INDEX NO.	PART NUMBER	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	NOTES
9-7	9420-7206	Cache Interface Feature, 35-foot	REF	
- 1	9400-6101	• PCB Assy, Address and Control	1	
- 2	9400-6102	• PCB Assy, Control Buffer	1	
- 3	9400-6103	• PCB Assy, Data	1	
- 4	9400-6007	• PCB Assy, Computer Interface	1	
- 5	9400-6021-01	• PCB Assy, 9400 RP04 CPA	1	
- 5	9400-6021-02	• PCB Assy, 9400 RM03 CPA	1	
- 5	9400-6031-01	• PCB Assy, 9400 RP04 CPA	1	Replaces 9400-6021
- 5	9400-6031-02	• PCB Assy, 9400 RM03 CPA	1	Replaces 9400-6021
- 6	9400-7010	• Cable Assy, Address and Control	1	
- 7	9400-7014	• Cable Assy, Data, 35-foot	1	
- 8	9400-7013	• Cable Assy, CPU Interface	2	

CHAPTER 10
DIFFERENCE DATA

10-1. **INTRODUCTION.** This chapter contains difference data sheets that delineate minor differences in hardware and firmware caused by changes to operating software systems and product improvements.

10-2. **PDP-11/70 CACHE BUS INTERFACE.**

a. Physical Construction. The PDP-11/70 CPU assembly provides dedicated space for up to 4 high speed I/O controllers. There are 4 slots reserved for each of these controllers. In addition, the CPU assembly provides space for hex SPC PCBs.

In the DEC configuration, an RH70 Controller may be fitted into each of the 4 available spaces (Figure 10-5). The RH70 Controller has 4 hex PCBs and may control either disk or magnetic tape storage systems. The high speed I/O controller interfaces to the UNIBUS for control and interrupts, but directly to the Cache of the PDP-11/70 for data transfer. The high data transfer rate is then achieved by not having to go via the UNIBUS MAP and the width of the data transfer is 32 bits.

b. Installation. In order to connect a 9400 Controller, the CPA board 9400-6021, or 9400-6031 is fitted into one of the 4 hex SPC slots A, B, C, or D. This provides the 9400 Controller with its interface to the UNIBUS. Three more boards for the Cache Interface are then fitted into the space reserved for one of the high speed controllers. The fourth position is left unused as this is the UNIBUS connection for an RH70.

The cable connected to J1 of the CPA board from the 9400 Controller, is identical to the cable used in other PDP configurations. The cable connected to J2 of the CPA board, carrying the DMA data and control, is made into a 3-way cable and is routed from the 9400 Controller to the data board of the Cache Interface and then to J2 of the CPA. A third cable connects the CPA to the address and control board of the Cache Interface.

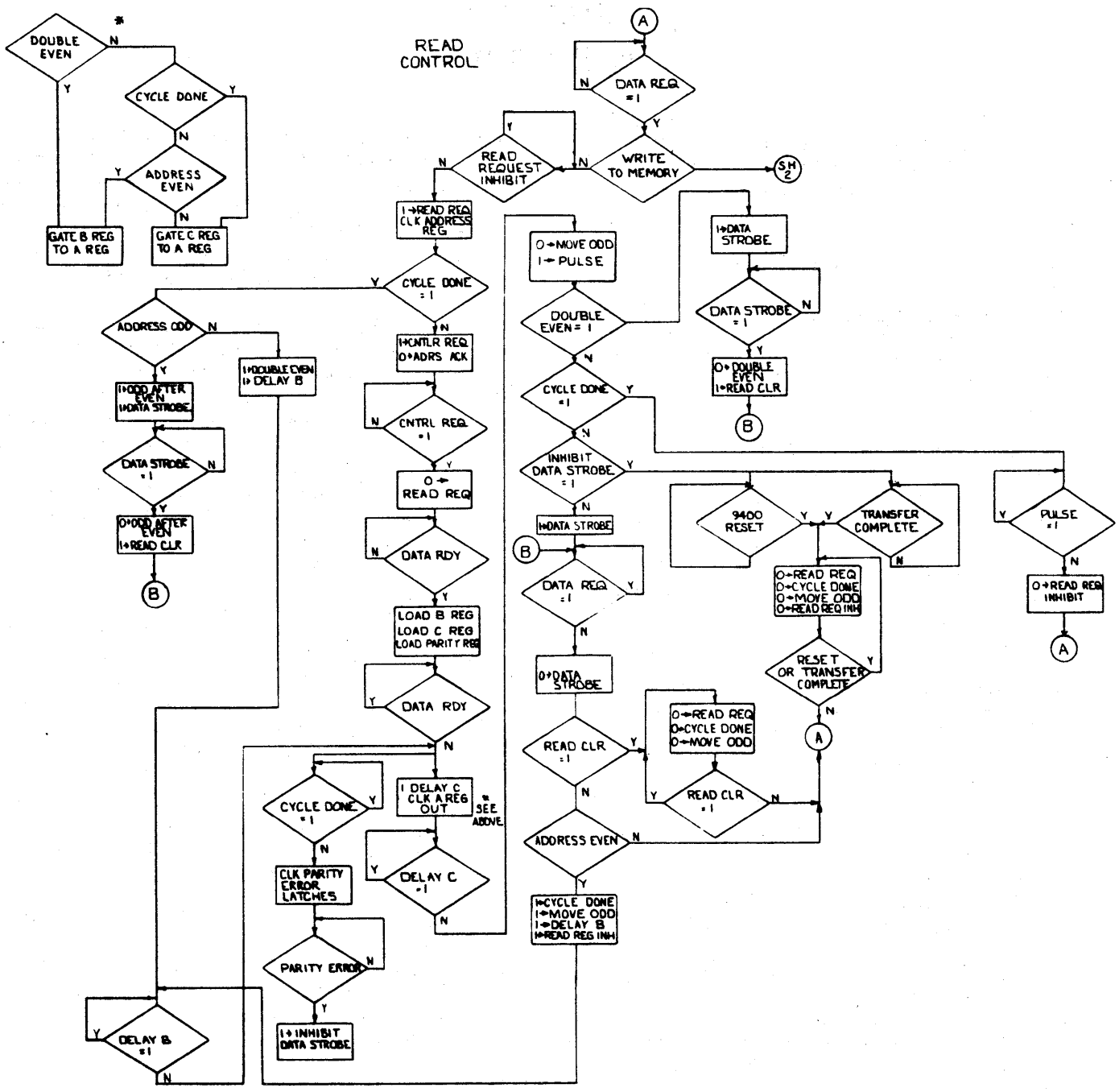
c. Logical Description

1. RP04 Computer Port Adapter. This board in its behavior is little different than in smaller PDP configurations. The main difference is that all DMA transfers are done via the Cache Interface and are inhibited from being done by the UNIBUS. This means that no NPR is raised by this board and NPG is simply passed down the UNIBUS. The register selection PROM is also changed to allow the UNIBUS access to the Buffer Address Extension Register, which extends the memory address bus to 22 bits, and to RHCS3.

2. Cache Interface Address and Control Board. This board interfaces all the memory address and control lines between the PDP-11/70 Cache and the CPA board. Its main function is to control the buffer of the 32-bit data bus of the Cache and the 16-bit data bus of the 9400 Controller. It has the capability of doing 16-bit data transfers to the Cache for start and finish addresses if necessary. A 22-bit address (actually 21, as bit 0 is unused) is sent from the CPA with each data request. It also sends back to the CPA various status conditions which are mainly detected errors.

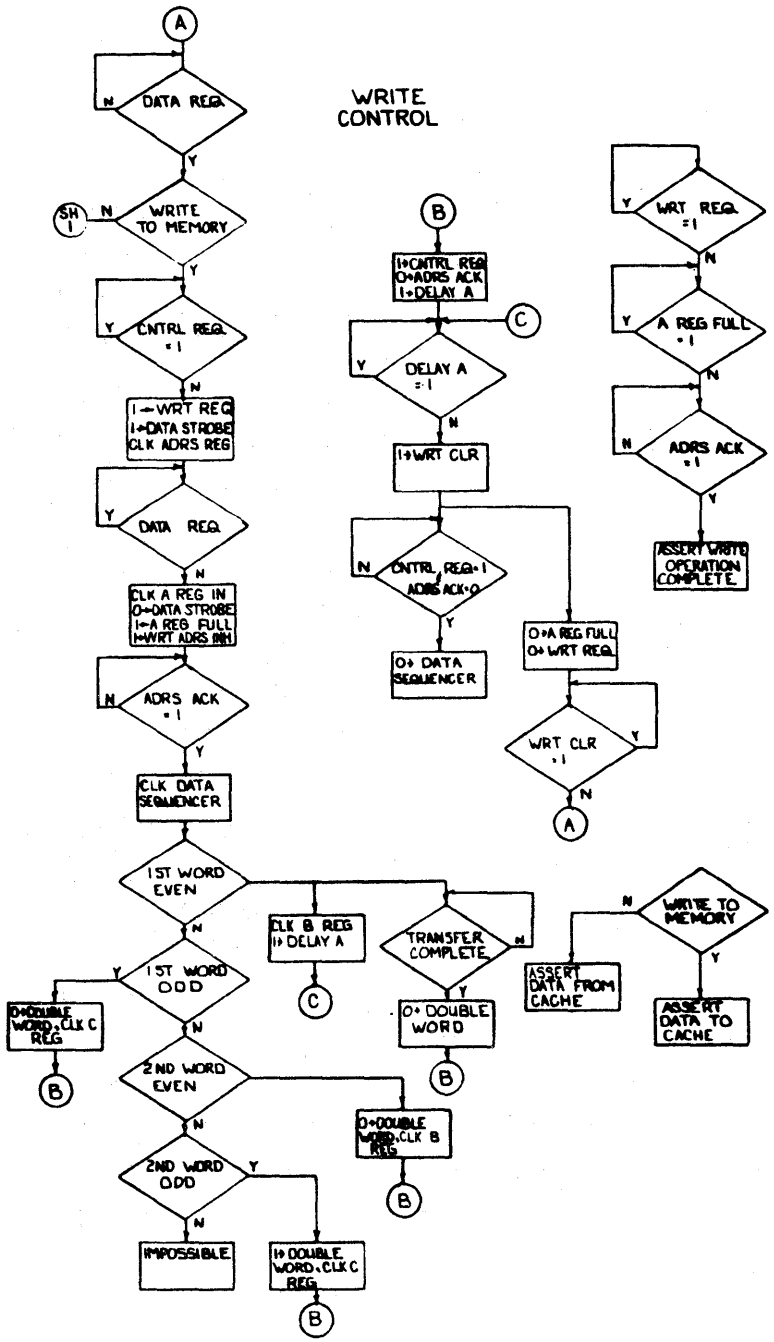
3. Cache Interface Data Board. This board has two 16-bit buffers to interface the data buses of the Cache and of the 9400 Controller. When reading from memory, 32-bits of data are read and stored into the 2 buffers. The buffers are sent to the 9400 Controller in turn. When writing to memory, 16-bits of data are sent from the 9400 Controller and loaded into the first buffer. The next 16 bits are loaded into the second buffer and a write cycle is then initiated to the Cache. The necessary actions are performed for 16-bit transfers to the Cache if the start or finish address of the DMA transfer is an odd address.

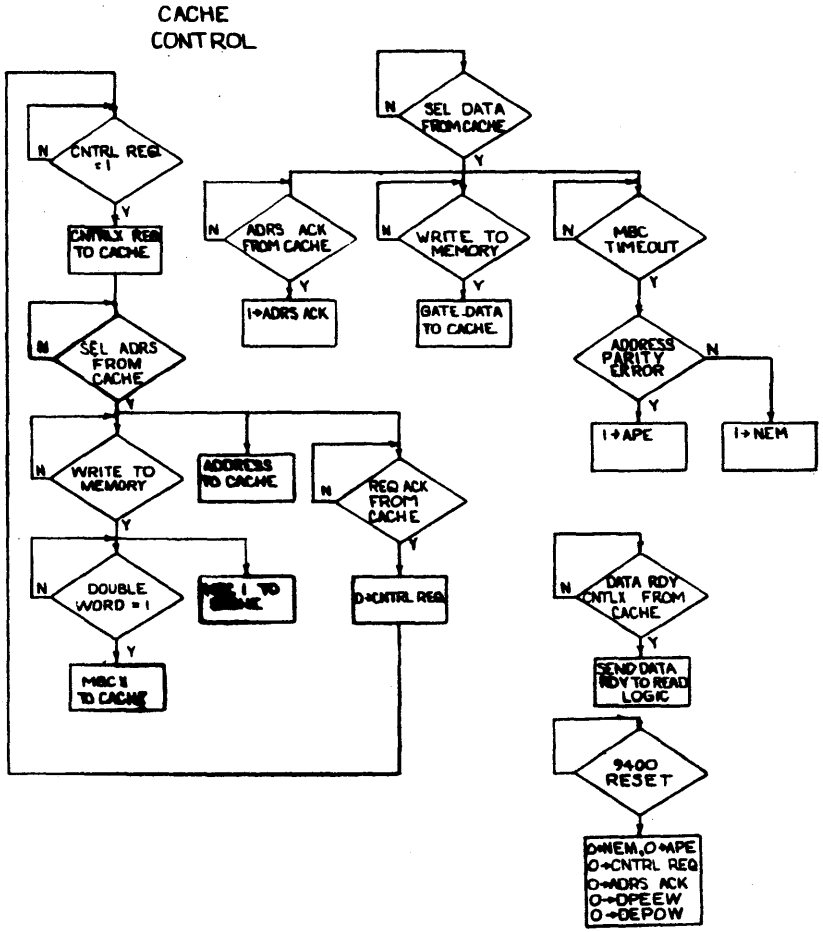
4. Cache Interface Control Buffer. This board has only one integrated circuit and is used to route signals between the address and control board and the data board. It is necessary so that there are no wiring changes required to the backplane of the high speed I/O controller.



Sheet 1 of 2

Figure 10-1. Cache Interface Flow Diagram


WRITE CONTROL
A
DATA REQ.
N
Y
SH 1
WRITE TO MEMORY
CNTRL REQ. = 1
1→WRT REQ
1→DATA STROBE
CLK ADRS REG
DATA REQ.
CLK A REG IN
0→DATA STROBE
1→A REG FULL
1→WRT ADRS RIN
ADRS ACK = 1
CLK DATA SEQUENCER
1ST WORD EVEN
1ST WORD ODD
0→DOUBLE WORD, CLK C REG
B
2ND WORD EVEN
2ND WORD ODD
IMPOSSIBLE
1→DOUBLE WORD, CLK C REG
CLK B REG
1→DELAY A
C
TRANSFER COMPLETE
0→DOUBLE WORD
0→DOUBLE WORD, CLK B REG
ASSERT DATA FROM CACHE
WRITE TO MEMORY
ASSERT DATA TO CACHE
1→CNTRL REG
0→ADRS ACK
1→DELAY A
DELAY A = 1
1→WRT CLR
CNTRL REG = 1
ADRS ACK = 0
0→ DATA SEQUENCER
0→A REG FULL
0→WRT REQ.
WRT CLR = 1
WRT REQ. = 1
A REG FULL = 1
ADRS ACK = 1
ASSERT WRITE OPERATION COMPLETE


CACHE CONTROL
CNTRL REQ = 1
CNTRL REQ TO CACHE
SEL ADRS FROM CACHE
WRITE TO MEMORY
DOUBLE WORD = 1
MBC 1 TO CACHE
ADDRESS TO CACHE
REQ ACK FROM CACHE
0→CNTRL REQ
SEL DATA FROM CACHE
ADRS ACK FROM CACHE
1→ADRS ACK
WRITE TO MEMORY
GATE DATA TO CACHE
MBC TIMEOUT
ADDRESS PARITY ERROR
1→APE
1→NEM
DATA RDY CNTLR FROM CACHE
SEND DATA RDY TO READ LOGIC
9400 RESET
0→NEM, 0→APE
0→CNTRL REQ
0→ADRS ACK
0→DPEEW
0→DEPOW

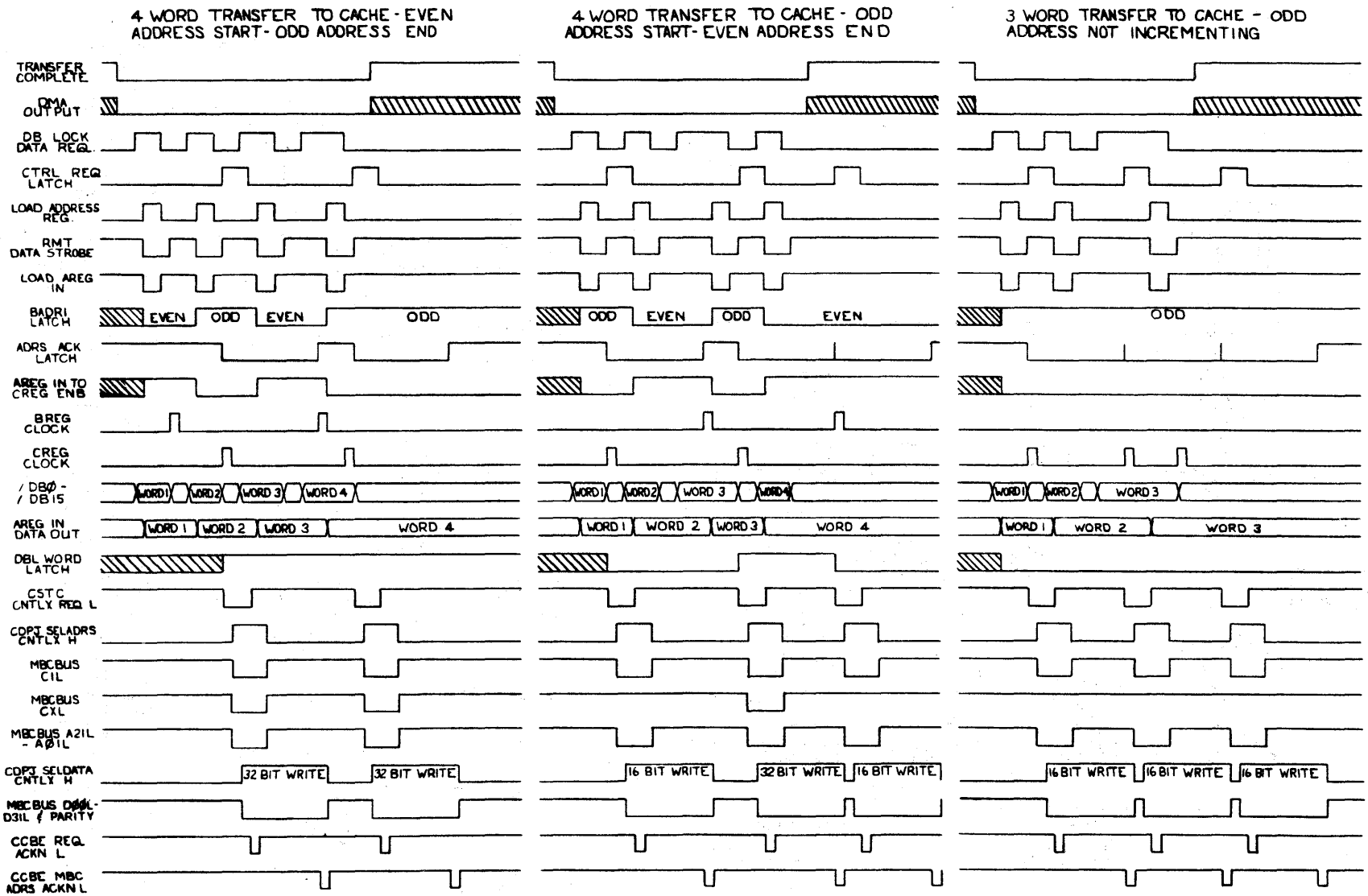


Figure 10-2. Timing Diagram, Cache - Write

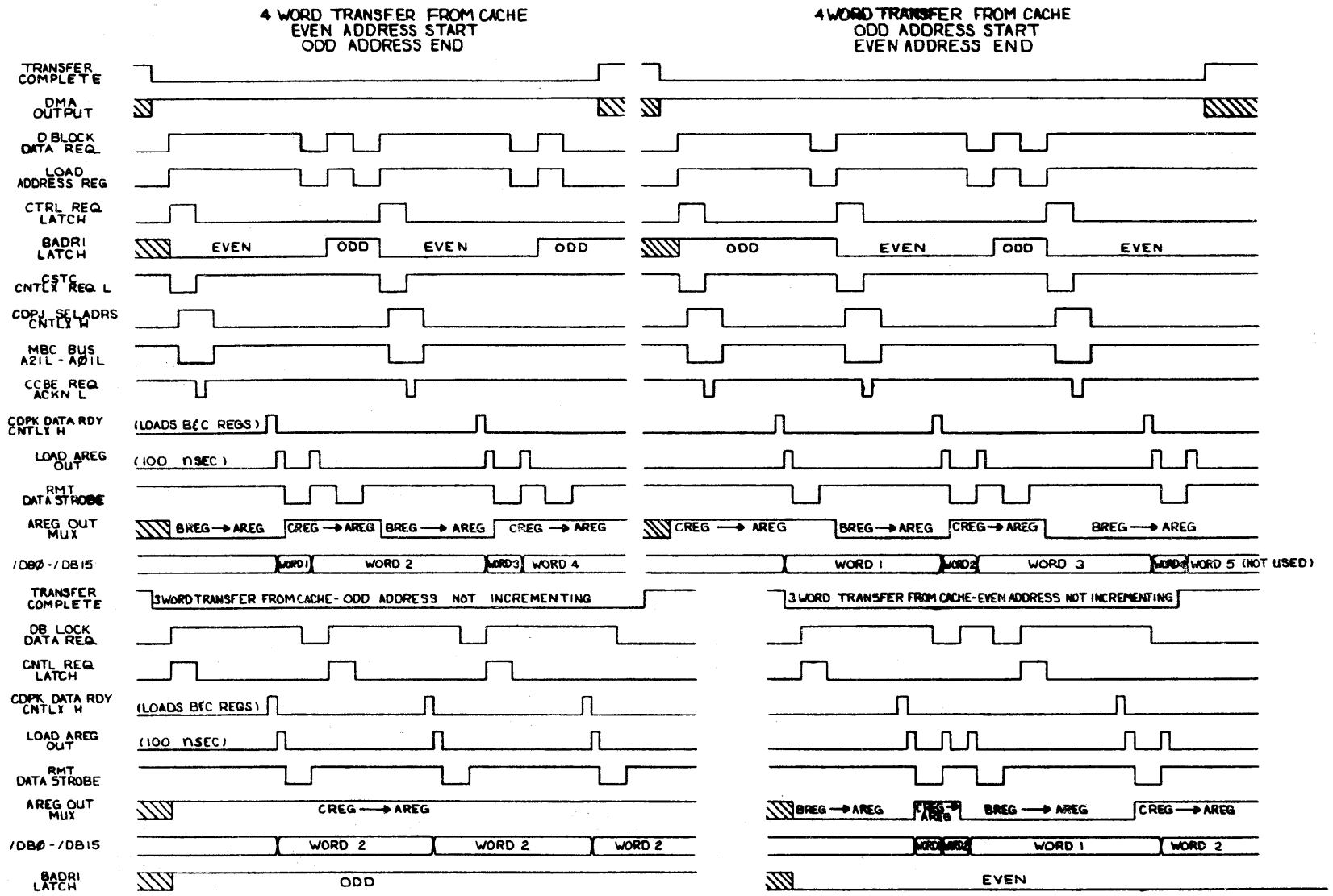


Figure 10-3. Timing Diagram, Cache - Read

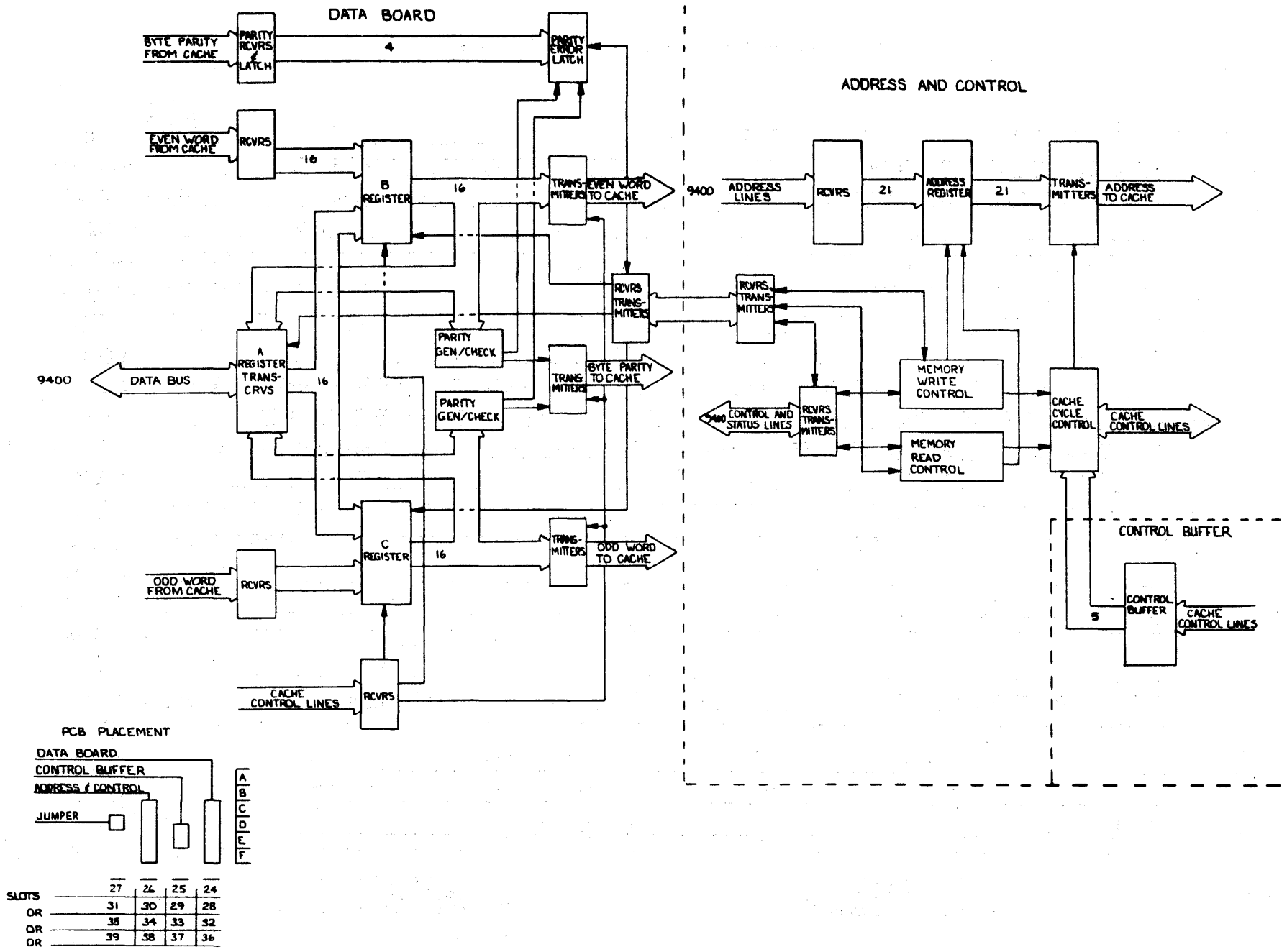
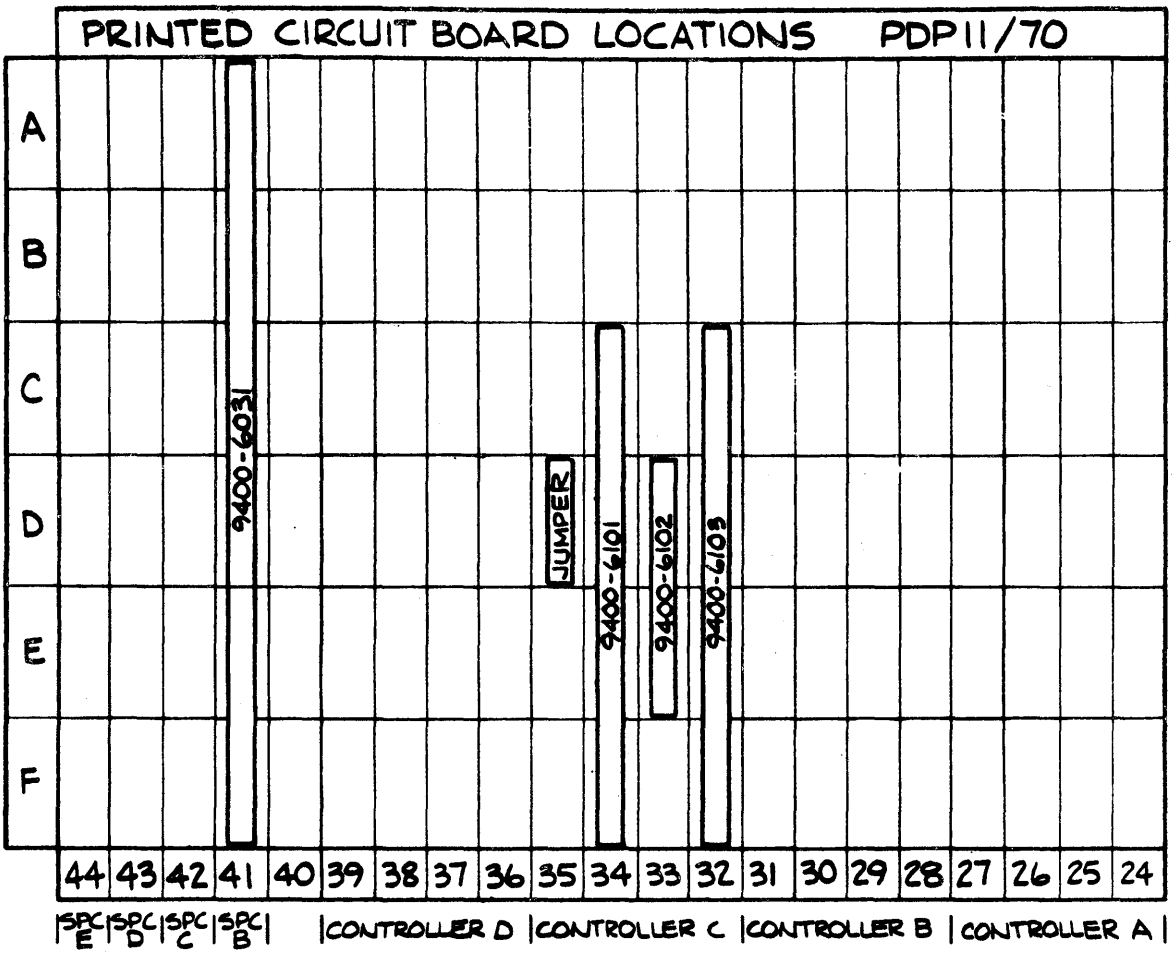


Figure 10-4. Cache Interface Block Diagram



PARTS REQUIRED

1.	PCB RP04 CPA	9400-6031	5.	Cable Cache Data Cable	9400-7011 or 9400-7014
2.	PCB Cache Address & Control	9400-6101			
3.	PCB Cache Control Buffer	9400-6102	6.	Cable Cache Address & Control Cable	9400-7010
4.	PCB Cache Data	9400-6103	7.	Cable 9400 - CPA Cable	9400-7007

CONFIGURATION REQUIRED

It is necessary to have, within the CPU assembly of the 11/70, an available RH70 position which is comprised of 4 slots, and an available SPC slot.

The following table gives the 4 possible positions of the available RH70 positions and the slots in which the cache interface PCBs may be fitted.

	BUS GRANT JUMPER CARD	9400-6101	9400-6102	9400-6103
SLOTS	27	26	25	24
OR	31	30	29	28
OR	35	34	33	32
OR	39	38	37	36

The 6101 & 6103 PCBs are quad high PCBs and should be fitted into positions C to F of the required slot. The 6102 PCB is double high and should be fitted into positions D & E of its slot. The bus grant jumper card should be already in position D of its slot and should be left there.

The 6031 PCB should be fitted into a spare SPC slot in the CPU assembly. The possible SPC slots 40, 41, 42, or 43. There should be a bus grant jumper card in any unused SPC slot which must be removed prior to the fitting of the 6031 PCB. It is possible to avoid the necessity of cutting the jumper on the backplane of the SPC slot from CAI to CBI by cutting the link W8 on the 6031 PCB. If however the link on the backplane is cut, it is necessary to leave link W8 in on the PCB, so that one and only one of these two links is cut.

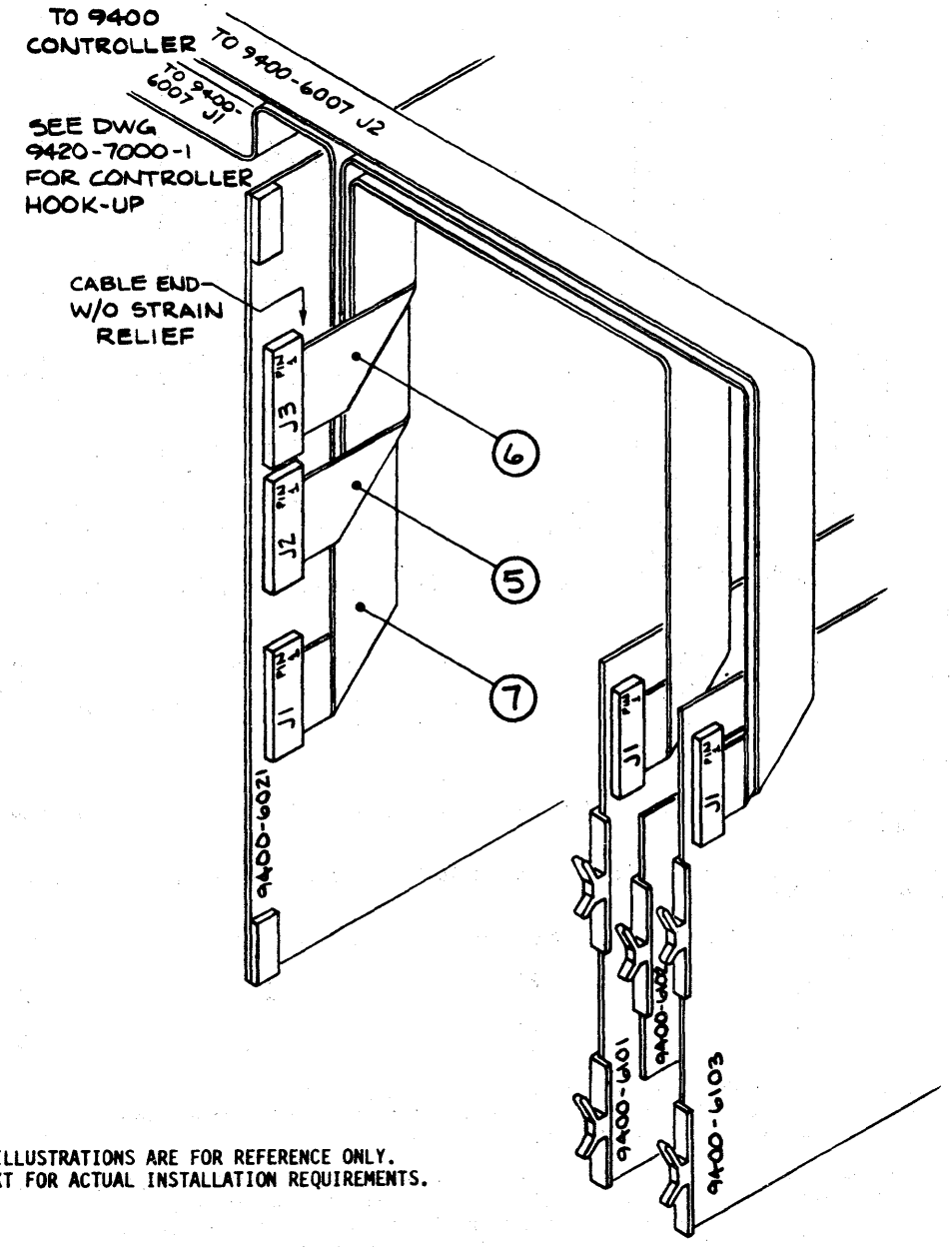
CABLE CONNECTION

The 15 inch, 50 pin Cache Address & Control Cable (9400-7010) connects J3 of the 6031 PCB to J1 of the 6101 PCB. The end of the cable without the strain relief connects to J3 of the 6031 PCB and the end with the strain relief to J1 of the 6101 PCB.

The three way Cache Data Cable (9400-7011) connects J2 of the CIB PCB within the 9400 Controller to J1 of the 6103 PCB and then to J2 of the 6031 CPA PCB. It should be noted that Pin 1 is connected to Pin 1 although the cable comes out of the bottom of the connector which goes to J2 of the 6031 CPA PCB.

The 9400 - CPA Cable (9400-7011) connects J1 of the CIB PCB within the 9400 Controller to J1 of the 6031.

Figure 10-5. Installation oF 9400 Cache Interface to PDP-11/70



NOTE: THESE ILLUSTRATIONS ARE FOR REFERENCE ONLY.
SEE TEXT FOR ACTUAL INSTALLATION REQUIREMENTS.

Figure 10-5. Installation of 9400 Cache Interface to PDP-11/70 (Continued)

Sheet 2 of 2

System Industries 525 Oakmead Parkway, Sunnyvale, California 94086, (408) 732-1650

SI Computer Systems, Ltd.
Guildford Road
Woking, Surrey
England GU22 7HB
Phone: (04862) 5077
Telex: 859124

System Industries GmbH
Am Forsthaus Gravenbruch 9-11
D6078 Neu Isenburg 2,
West Germany
Phone: (06102) 5464/5
Telex: 417606

System Industries, Inc. Scandinavia AB
Grev Magnigatan 5,
S-114 55 Stockholm
Sweden
Phone: 08-63 62 74
Telex: 12697