sun microsystems

Sun 3004 CPU Board Configuration Procedures

Sun Microsystems, Inc. • 2550 Garcia Avenue • Mountain View, CA 94043 • 415-960-1300

Part No: 813-2047-06
Revision A of 27 October 1987

CAUTION **This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.**

WARNING ***There is a Lithium Battery (BBCV2), Matsushita Electric Type No. BR2325, located on the Sun CPU Board. This battery is NOT a customer replaceable part. The battery is marked as follows: "Warning— Replace battery with MATSUSHITA ELECTRIC or PANASONIC Part No. BR2325 only. Use of another battery may present a risk of fire or explosion."***

The battery may explode if mistreated. Do not dispose of the battery in fire, attempt to recharge or disassemble the battery.

Sun 3004 CPU Board Configuration Procedures

General Description

The Sun 3004 CPU board features an MC68020 Central Processing Unit (CPU) with on-chip instruction cache, an MC68881 Floating Point Coprocessor (FPC) and interface circuitry that supports the VMEbus, Ethernet and two RS423 serial ports. It has 4 Megabytes of on-board RAM.

A 16.67 Mhz clock provides timing for internal data processing. A 32-bit data bus provides a high-bandwidth path between both the CPU and Direct Virtual Memory Access (DVMA) devices and main memory.

The Memory Management Unit (MMU) translates virtual addresses into physical addresses to provide access to devices such as main and video memory, the VMEbus master interface, and I/O. It protects and manages these devices, and allows them to be shared.

This procedure covers the Sun PN 501-1164 and PN 501-1208 versions of the Sun 3004 board.

PN 501-1164 Configuration Jumpers

The table on the following page shows the factory configuration of jumpers on the 501-1164 CPU Board which is imprinted with the bare board part number 270-1164. The table lists coordinates that aid in locating the jumper-blocks. The same information for a later version of the board, imprinted with PN 270-1208 and listed as the 501-1208 CPU Board, follows in Table 2.

The board has grid markings that form an X-Y coordinate system. Letters of the alphabet define the X coordinate and numbers define the Y coordinate of the grid. For example, the location "A-3" in the *Location* column of the following table indicates that jumper-block J2502 is located at the intersection of coordinates "A" and "3".

The *Configuration* column on the table indicates whether or not the board is shipped with the referenced jumper installed on the indicated pins. "1-2" in that column means that the jumper is installed across pins 1 and 2. "IN" means that the board is shipped with the jumper installed. "OUT" means that the jumper is not installed at the factory. The illustrations that follow show the orientation of the jumper blocks.

Pin 1 of each jumper-block is to the left of the v-shaped mark on the board, as it is on IC packages.

The *Description* heading describes the function of a jumper when installed in the indicated position.

Table 1 *Factory Configuration of Jumpers on the 501-1164 CPU Board*

Jumper	*Location*	*Configuration*	*Description*
J2502	A-3	1-2, IN	Enable VME Clock
J1200	A-3	1-2, OUT	For 27256 Boot PROM
J1201	A-3	1-2, IN	For 27512 Boot PROM
J2501	B-6.5	1-2, IN	Enable Ethernet Clock
J2503	B-6.5	1-2, OUT	VCC to Ethernet Connector
J2301	B-21	1-2, IN	Enable Video Clock
J1001	E-32	1-2, IN	Enable SCC Clock
J3101	K-11	1-2, OUT	Enables 2MB CPU Board
J3102	K-11	1-2, IN	Enables 4MB CPU Board
J100	K-11	1-2, OUT	Cache Disable
J2505	K-11	1-2, OUT	Select Ethernet Level†
J400	N-11	1-2, IN	Select 16.67 Mhz CPU Clock
J400	N-11	3-4, OUT	Select 12.5Mhz CPU Clock
J400	N-11	5-6, OUT	Select Asynch. 12.5 Mhz FPC Clock
J400	N-11	7-8, IN	Select Synch. 16.67 Mhz FPC Clock
J300	R-5	1-2, OUT	Null
J300	R-5	3-4, IN	VME Interrupt Level 1
J300	R-5	5-6, IN	VME Interrupt Level 2
J300	R-5	7-8, IN	VME Interrupt Level 3
J300	R-5	9-10, IN	VME Interrupt Level 4
J300	R-5	11-12, IN	VME Interrupt Level 5
J300	R-5	13-14, IN	VME Interrupt Level 6
J300	R-5	15-16, IN	VME Interrupt Level 7
J2703	R-12	1-2, IN	CPU is VME Reset Master
J2702	R-12	1-2 OUT	CPU is VME Reset Slave
J2701	R-12	1-2, IN	CPU is VME Arbiter & Requester
J2700	R-12	1-2, OUT	CPU is VME Requester Only

† This jumper is IN for Level 1 Ethernet; OUT for Level 2

Figure 1 *A-H Section of 501-1164 Board*

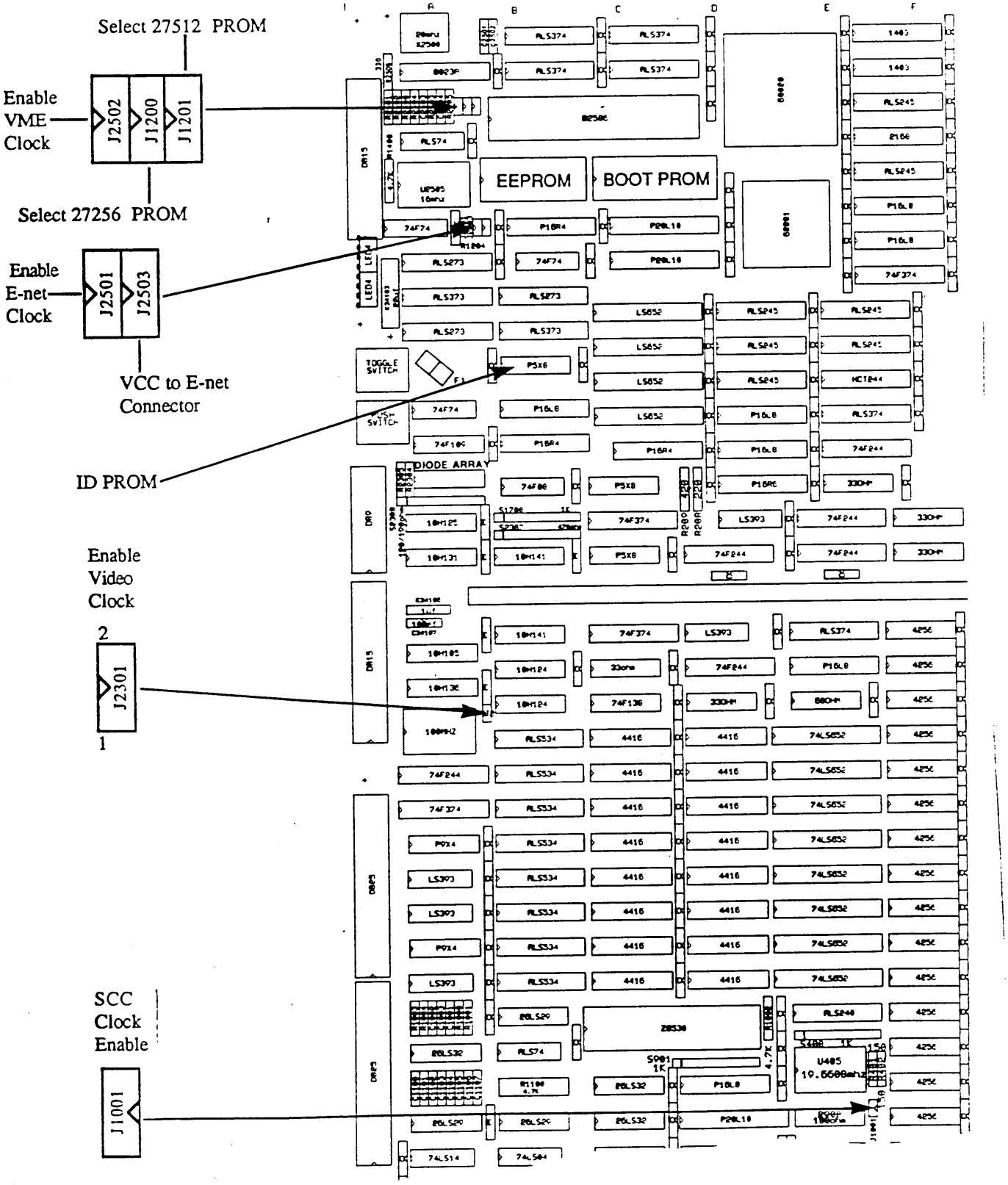

Figure 2 *H-T Section of 501-1164 Board*

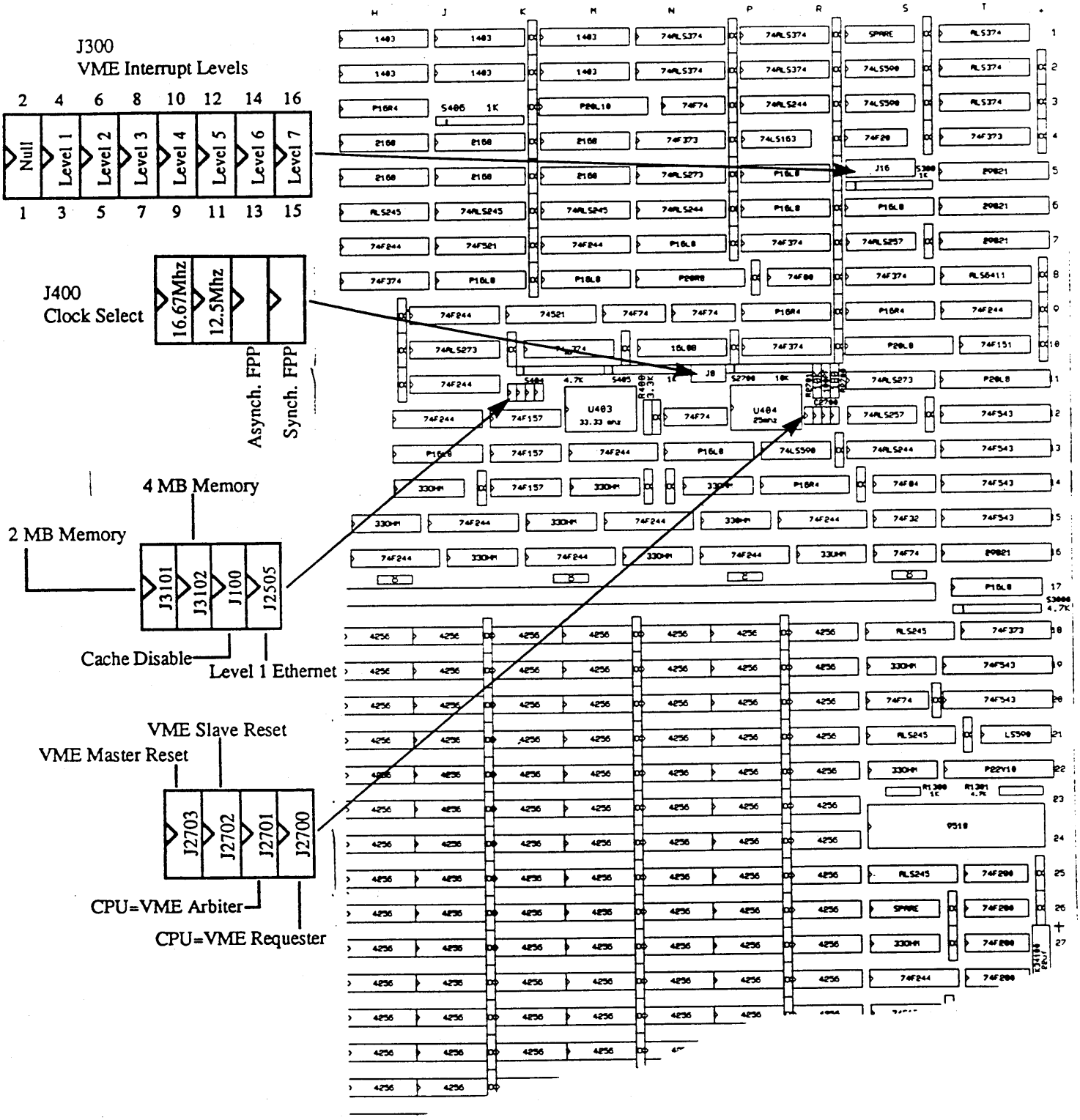

Table 2 *Factory Configuration of Jumpers on the 501-1208 CPU Board*

Jumper	*Location*	*Configuration*	*Description*
J2502	A-3	1-2, IN	Enable VME Clock
J1200	A-3	1-2, OUT	For 27256 Boot PROM
J1201	A-3	1-2, IN	For 27512 Boot PROM
J2501	B-6.5	1-2, IN	Enable Ethernet Clock
J2503	B-6.5	1-2, OUT	Select Ethernet Level †
J2301	B-21	1-2, IN	Enable Video Clock
J1001	E-32	1-2, IN	Enable SCC Clock
J3101	K-11	1-2, OUT	Enables 2MB CPU Board
J3102	K-11	1-2, IN	Enables 4MB CPU Board
J100	K-11	1-2, OUT	Cache Disable
J400	N-11	1-2, IN	Select 16.67 Mhz CPU Clock
J400	N-11	3-4, OUT	Null
J400	N-11	5-6, OUT	Null
J400	N-11	7-8, IN	Select 16.67 Mhz FPC Clock
J300	R-5	1-2, OUT	Null
J300	R-5	3-4, IN	VME Interrupt Level 1
J300	R-5	5-6, IN	VME Interrupt Level 2
J300	R-5	7-8, IN	VME Interrupt Level 3
J300	R-5	9-10, IN	VME Interrupt Level 4
J300	R-5	11-12, IN	VME Interrupt Level 5
J300	R-5	13-14, IN	VME Interrupt Level 6
J300	R-5	15-16, IN	VME Interrupt Level 7
J2703	R-12	1-2, IN	CPU is VME Reset Master
J2702	R-12	1-2 OUT	CPU is VME Reset Slave
J2701	R-12	1-2, IN	CPU is VME Arbiter & Requester
J2700	R-12	1-2, OUT	CPU is VME Requester Only

† This jumper is IN for Level 1 Ethernet; OUT for Level 2

Figure 3 *A-H Section of 501-1208 Board*

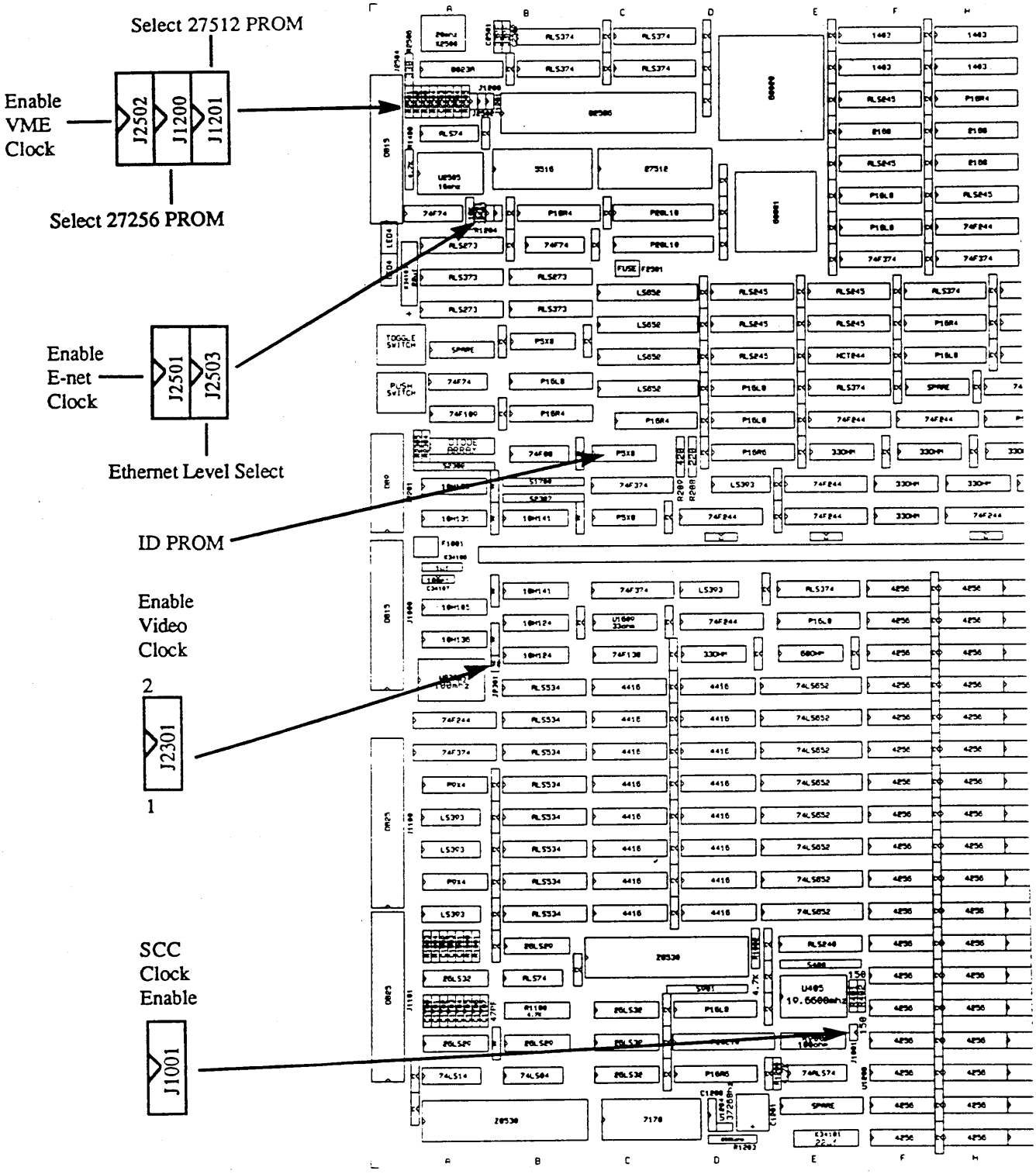

Figure 4 *H-T Section of 501-1208 Board*

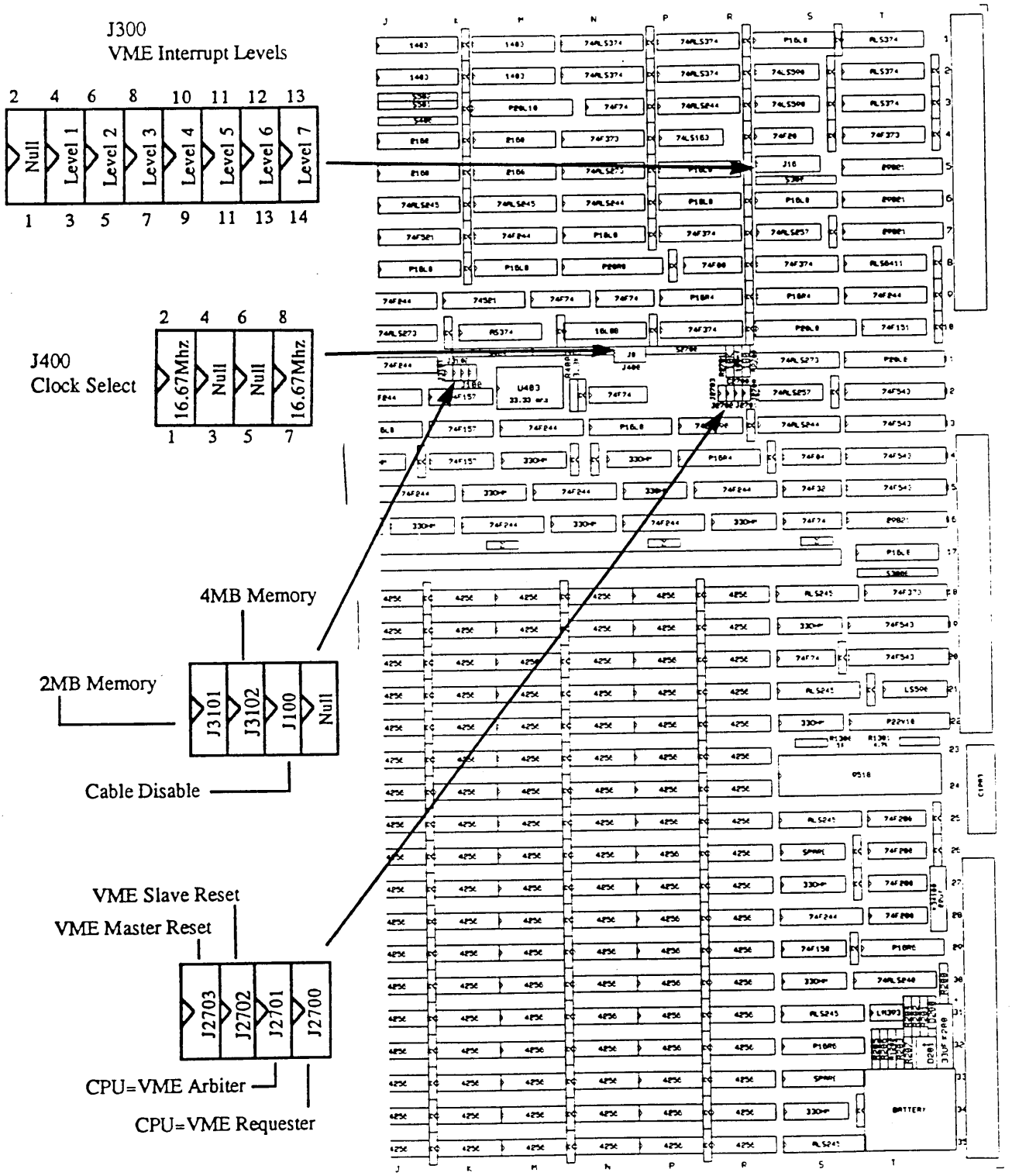

Table 3 *Revision History*

Revision	Date	Comments
01-1	10 July 1987	Alpha Draft of this Configuration Procedure, which adds the 501-1208 version of the board to the original 501-1164 board configuration procedure and renders that procedure, PN 813-2028, obsolete.
A-5	10 August 1987	Production release of this Configuration Procedure to replace the Sun 501-1164 CPU Board Configuration Procedure (PN 813-2028).
A-6	27 October 1987	Jumper configuration corrections on the 501-1208 board—took out extra clock, and jumpers J2701 & 2702 were transposed on chart.