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Engineering Manual

for the

Sun-2/120 Memory Board

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Revision History

Revision	Date	Comments
50	28 September 1984	First release of this Theory of Operation Manual.

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Preface

Purpose and Audience

The purpose of this manual is to enable Sun customers and licensors of the Sun Workstation design to understand the memory board. Licensors of the Sun Workstation design should use this manual to aid them in modifying the memory board design.

Organization

This manual provides a memory board overview and block diagram, the Theory of Operation for the memory board, and relevant timing information. Memory board diagnostics are also included in this manual.

At the end of this manual, we have supplied a reader comment form. Please use the comment form to list errors and omissions. Your responses help a great deal in our efforts to keep our documentation up to date.

Notations Used In This Manual

When possible, the schematics were drawn to standard drafting conventions. Signal flow is shown from left to right, and top to bottom. Connected sections of the design are logically grouped together, as much as the available space allows.

Conventions used for hardware signal names in this manual are:

- Both active-high and active-low signals are used. A signal name that is followed by a minus sign (-) indicates that the signal is active LOW (<0.4V). For example, the Column Address Strobe, M.CAS0-, is such a low-active signal.
- A signal that is *not* followed by a minus sign is understood to be a HIGH active signal (>2.0V). An example of such a signal would be the parity error signal, PARERR.
- For signals with multiple meanings or synonyms, the signal names are listed as separated by a slash (/). An example of this would be the on-board, memory expansion select signal, PM.OB-/P2. A high signal is understood to be an assertion of the P2 bus, while a low signal is an assertion of on-board status.
- Bus signals are indicated by a common prefix followed by a number. For example, a 16-bit data bus might be labelled D0, D1, D2, and so on until D15.
- A group of signals that is part of a signal vector is denoted by a common prefix separated from its suffix by a period. For example, all P1 signals start with the prefix "P1.", and P1 bus address signals are P1.A00, P1.A01, etc.
- Connector signals are distinguished by a suffix of "[]" with an optional string enclosed inside the square brackets identifying the connector name.

Components

Components in the schematics are identified by *component name* (this is also referred to as the “body name” in the wirelist). Components are named according to their generic or industry standard names. The way the components are drawn reflects their circuit function rather than the manufacturer’s definition.

Each component carries a *location label* identifying its component type and approximate location in the schematics. Location labels consist of a letter followed by three digits. For instance, U300 is a DIP positioned on page three of the schematics.

The letter stands for the type of component, and is one of the following:

Letter	Component Type
C	Standard Capacitor
D	Diode
K	Electrolytic Capacitor
L	Inductor
X	Decoupling Capacitor
J	Jumper or Connector
R	Resistor
S	Single-in-Line Component
U	Dual-in-Line Component
P..L..	Programmable Logic Array

Programmable logic components, such as PALs and PROMs, are described in a high-level functional language from which they are translated automatically into the bit patterns for programming. Programmable logic elements are identified by name.

Chapter 1

Sun-2 One-Megabyte Memory Board

This manual describes the theory of operation of the one-megabyte memory board for the Sun-2 architecture machines. The main features are:

- one megabyte of dynamic RAM on one board
- no-wait-state operation with Sun-2 CPU
- byte-parity-error detection
- Multibus (IEEE-796 bus)-compatible sized board
- 5-Volt-only operation
- low-power operation

1.1. Functional Description

This section describes the operation of the Sun-2 one-megabyte memory board. You should be familiar with the Sun-2 CPU operation and backplane. For your convenience, a copy of the memory board schematics is included as an Appendix to refer to as you are reading this manual.

1.1.1. Address Bit Assignments

The various translated and non-translated address bits from the Sun-2 CPU are used as follows:

Figure 1-1: Memory Address Usage

MA22 - MA18		PA	MA16 - MA11					PA	MA	PA08 - PA01												
22	21	20	19	18	09	16	15	14	13	12	11	10	17	08	07	06	05	04	03	02	01	00
Board Select		CAS Decoding			Column Address							Row Address							not available			

Note: PA09 is also the low-power bank-select bit

The row address is composed of untranslated address bits PA01 - PA08. Untranslated bits are used to avoid memory management delays (MA bits). Since these bits arrive before MA20 - MA22, which do board selection, all RAM boards will receive a row address strobe with the row address which will cause the RAMs to consume large amounts of power. In order to minimize power consumption, untranslated bit PA9 is used to select one of two 512K byte banks of each board so that only half of the RAMs are active.

The column address is composed of PA10 and MA11 - MA17. Note that MA17 is swapped with PA9. In addition to being used for low power bank selection, PA9 is used with MA18 and MA19 to decode one out of eight column address strobes.

1.2. Block Diagram

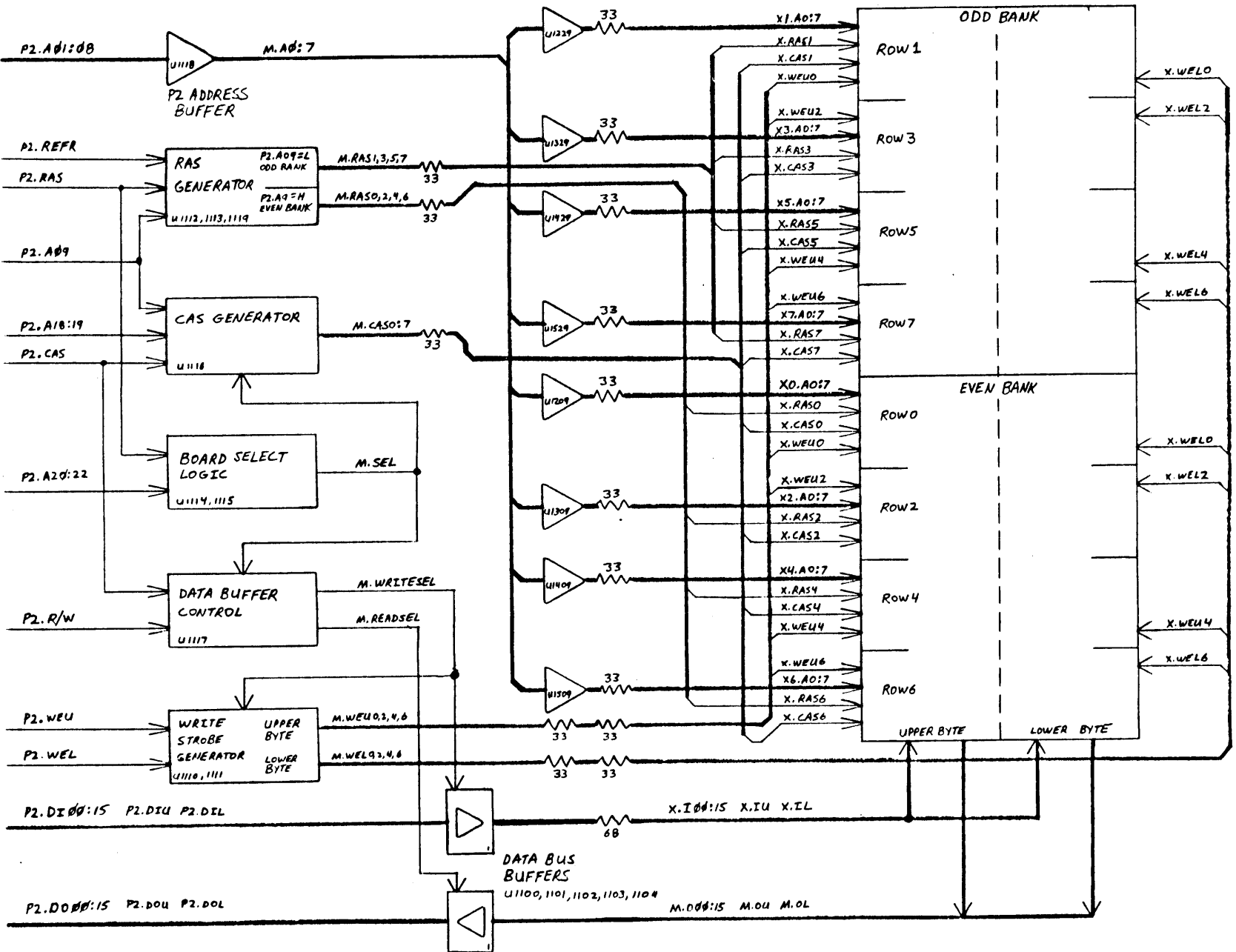


Figure 1-2: Memory Board Block Diagram

1.2.1. Memory Array

The memory is arranged as eight rows of eighteen bits. Nine bits form the upper byte and parity bit (X.I08:15, X.IU, M.O08:15, M.OU), and the other nine form the lower byte and parity bit (X.I00:07, X.IL, M.O00:07, M.OL). The eight rows are separated into two banks — the odd rows in the odd bank and the even rows in the even bank. This is due to the low power feature where only half of the array gets a RAS and consumes large quantities of electrons.

1.2.2. Row and Column Address Path

The row and column addresses are multiplexed onto the P2.A01:08 bus by the CPU with row address followed by column address. The address is received by buffer U1118 and is then distributed to eight additional buffers, one set per row. U1118 is required to reduce loading on the P2 bus. One set of buffers per row is used to minimize memory access time skew by reducing the RAM input capacitance each buffer must drive. By limiting the number of RAMs driven by a buffer to 18, the variability of input capacitance becomes negligible which stabilizes access times.

1.2.3. Board Select Logic

P2.A20:22 are decoded by U1114 into eight signals: one per megabyte of memory space. Dipswitch U1115 selects one of the eight decoded signals. The selected signal is the megabyte range for which the board will be active. This board select signal (M.SEL-) will persist beyond the end of a memory cycle so P2.RAS- is used to terminate the board select function.

1.2.4. Data Buffer Control

There are read and write buffers that connect the memory array with the P2 bus. U1117 is used to select which set of buffers is enabled. M.SEL- and P2.CAS- enable the buffers only if the board is selected and only during the CAS part of the memory cycle. P2.R/W- then selects whether the read or write buffers are to be enabled.

1.2.5. Data Paths

There are two data buses, the data and parity IN bus (X.I00:15, X.IL, X.IU) and the data and parity OUT bus (M.O00:15, M.OL, M.OU). The two buses are required because late writes are done to the board. The data out buffer of the dynamic RAM chip becomes active during late writes so the buses are separate to avoid bus conflict. Separate buses also allows for READ-MODIFY-WRITE cycles.

1.2.6. Write Strokes

Write strokes are generated on an upper- and lower-byte basis. U1110 generates the lower byte write strokes when M.WRITESEL- and P2.WEL- are both low. U1111 generates the upper byte write strokes in a similar manner. Note that data will be written into a particular dynamic RAM only when RAS, CAS, and the write strobe are all active.

1.2.7. RAS Generator

U1112, 1113, and 1119 generate the RAS signals during memory accesses and refresh operations. For memory cycles, P2.A09 selects the odd or even bank and P2.RAS- enables the M.RAS outputs for the selected bank. P2.REFR- will cause all eight M.RAS outputs to go active during refresh operations. A function table for U1112 is included to aid in your understanding.

Table 1-1: RAS Function Table

P2			Memory				Meaning
P	P	P	M	M	M	M	
2	2	2	R	R	R	R	
R	A	R	A	A	A	A	
A	0	E	S	S	S	S	
S	9	F	0	1	2	3	
-	-	R	-	-	-	-	
		-					
H	X	X	H	H	H	H	outputs forced high : no cycle
L	L	H	H	L	H	L	B inputs selected : odd bank
L	H	H	L	H	L	H	A inputs selected : even bank
L	X	L	L	L	L	L	A and B inputs all high so all outputs low independent of P2.A09 : refresh cycle

1.3. Timing Information

A typical timing diagram is provided. Actual times depend on when address strobe is issued by the 68010, the rise and fall times of the RAS and CAS signals, and the row and column access times. This diagram is intended to give the reader an idea of the timing relationships of the various memory board signals.

1.3.1. Timing Diagram

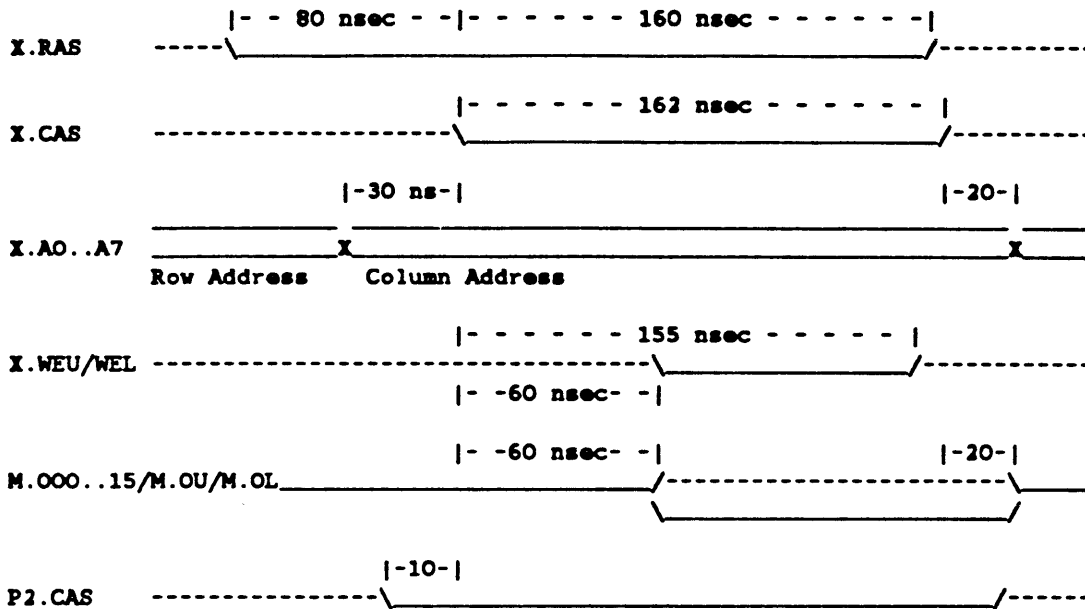
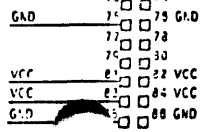
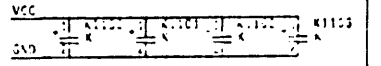
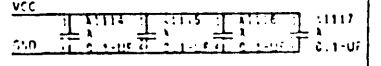
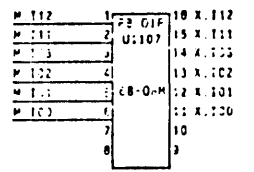
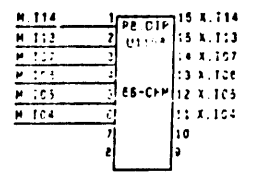
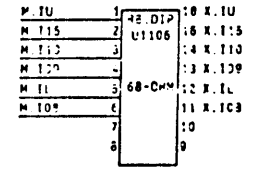
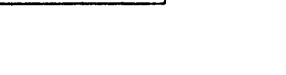
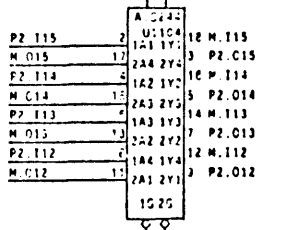
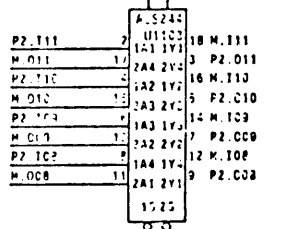
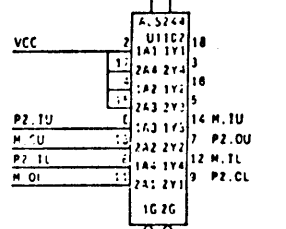
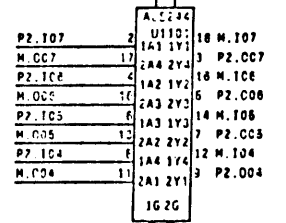
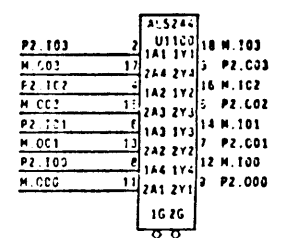
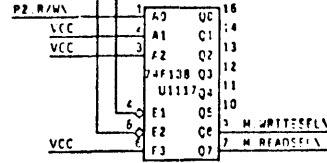
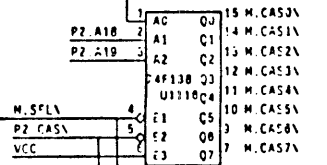
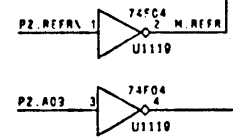
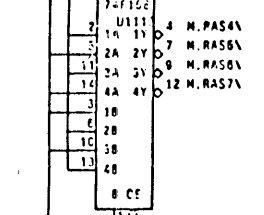
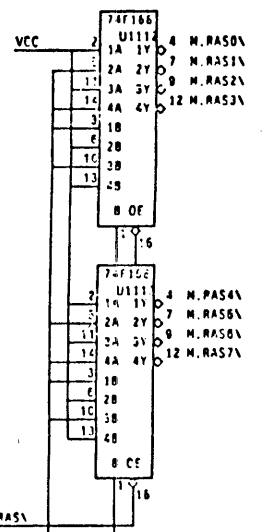
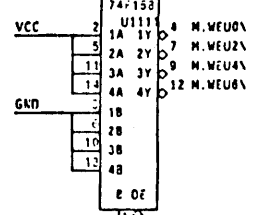
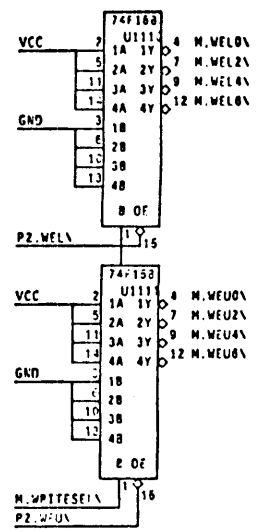
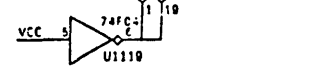
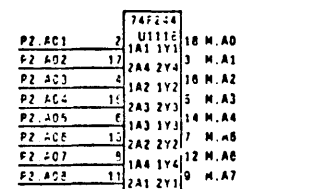
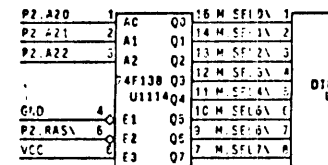
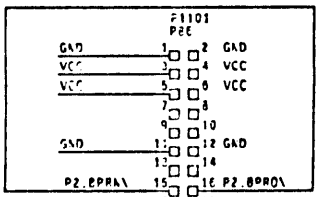


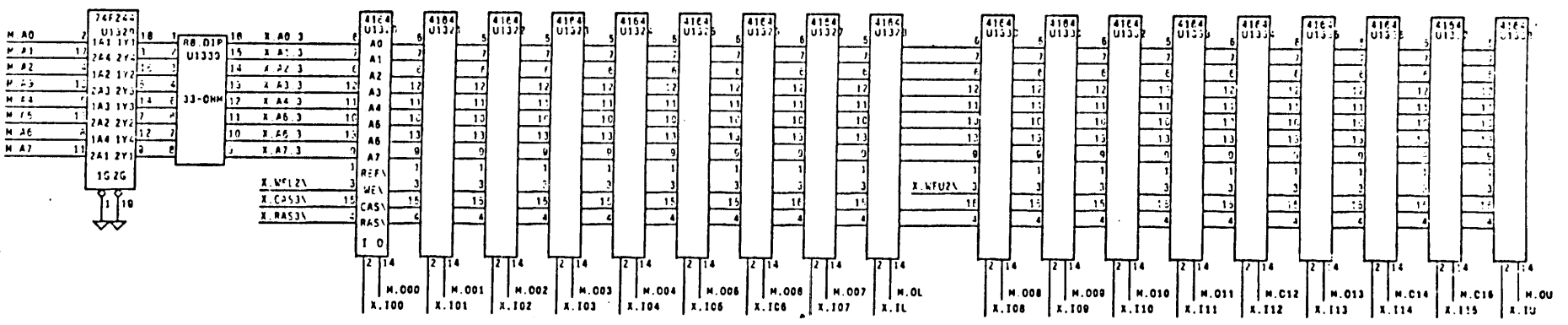
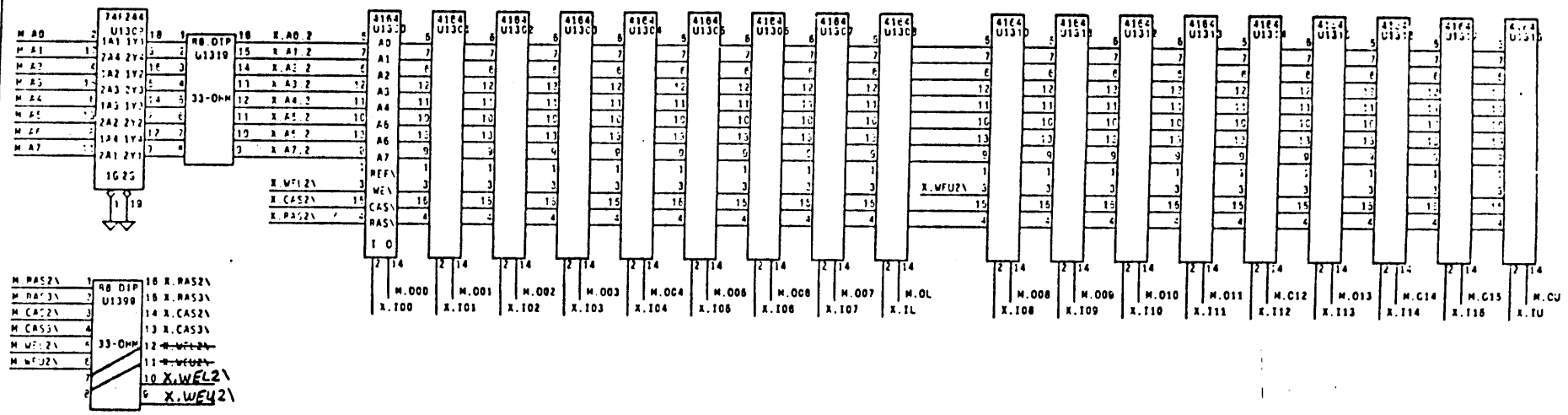
Figure 1-3: Memory Typical Timing Information

Appendix A

Memory Board Schematics

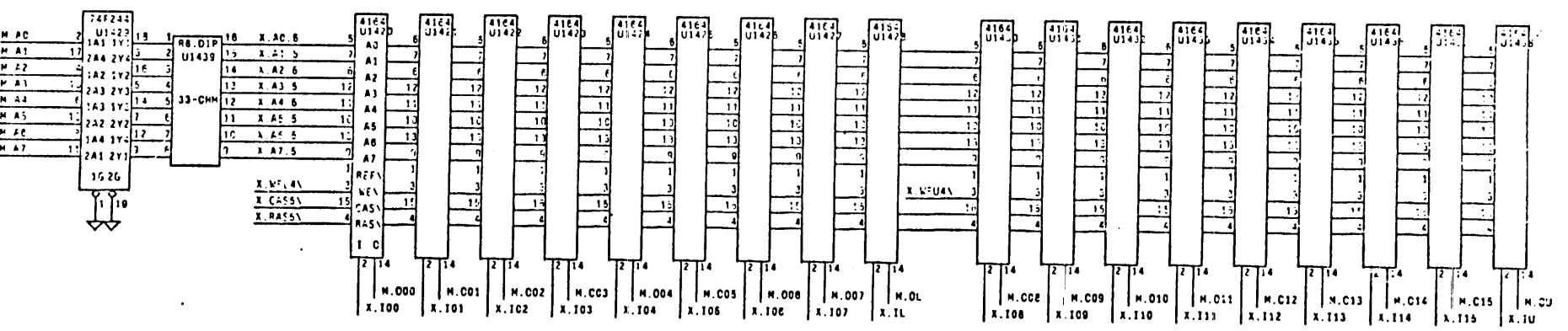
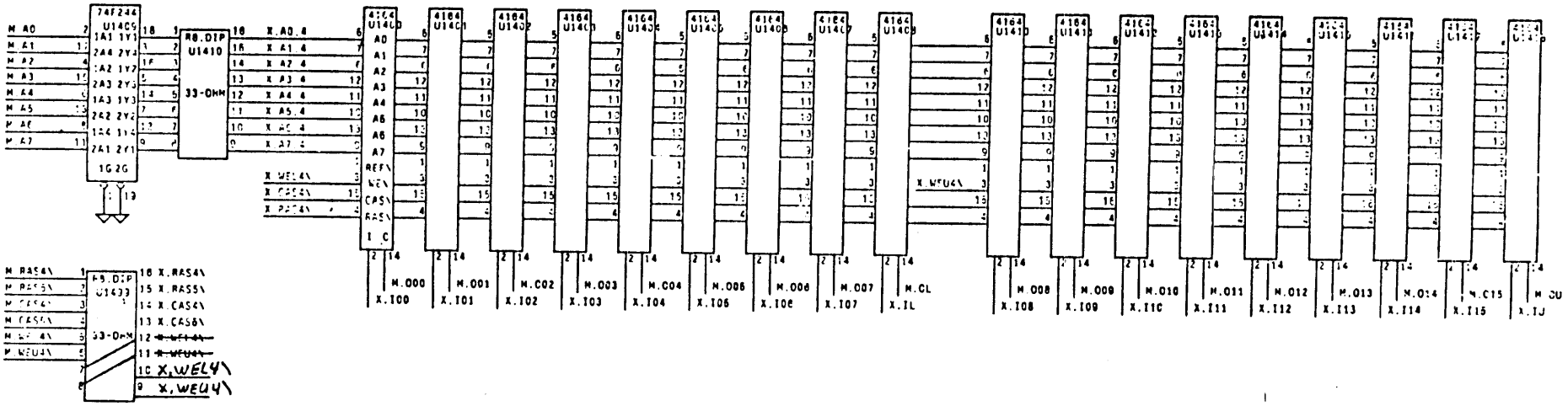
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P2.A11	3	P2.A20	4
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P2.WAITN	7	P2.WELN	8
P2.T00	9	P2.P00	10
P2.T01	11	P2.C01	12
P2.T02	13	P2.A21	14
P2.T03	15	P2.P02	16
P2.T04	17	P2.C03	18
P2.T05	19	P2.A22	20
P2.T06	21	P2.P04	22
P2.T07	23	P2.C05	24
P2.T08	25	P2.RFRN	26
P2.T09	27	P2.P06	28
P2.T10	29	P2.C07	30
P2.T11	31	GND	32
P2.T12	33	P2.CL	34
P2.T13	35	P2.OU	36
P2.T14	37	GND	38
P2.T15	39	P2.C08	40
P2.T16	41	P2.P09	42
P2.T17	43	GND	44
P2.T18	45	P2.O10	46
P2.T19	47	P2.O11	48
P2.T20	49	P2.R/W	50
P2.T21	51	P2.C12	52
P2.T22	53	P2.O13	54
P2.T23	55	P2.WEN	56
P2.T24	57	P2.C14	58
P2.T25	59	P2.O15	60





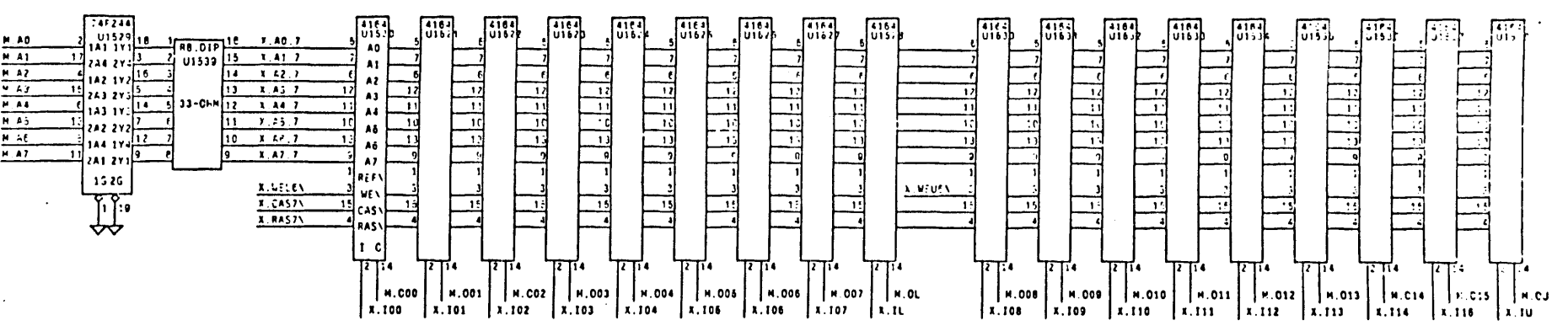
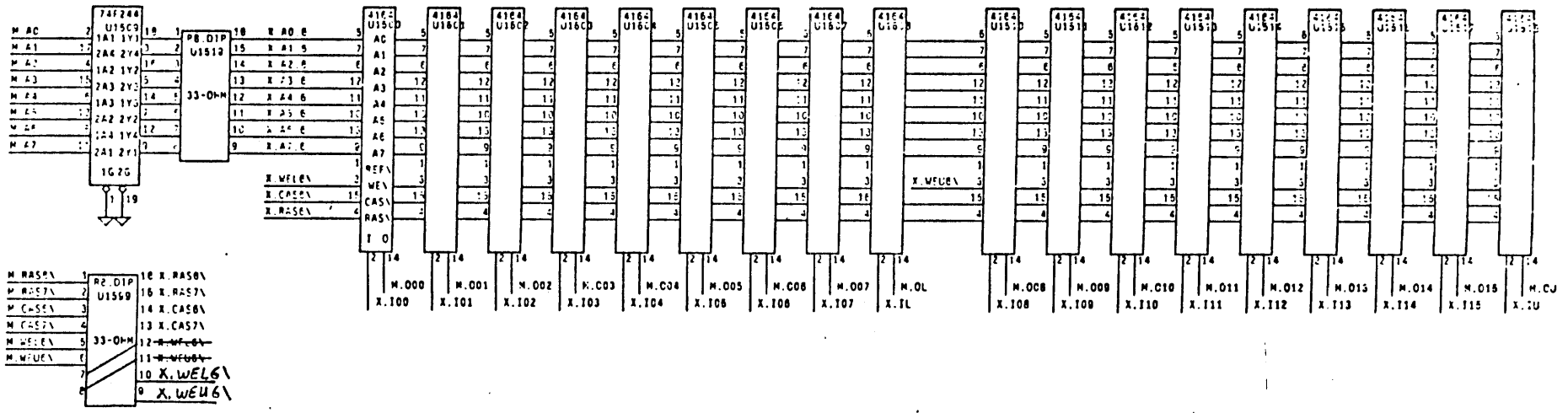
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GND	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X

VCC	1	X1320	1	X1321	1	X1322	1	X1323	1	X1324	1	X1326	1	X1326	1	X1327	1	X1328	1	X1330	1	X1331	1	X1332	1	X1333	1	X1334	1	X1335	1	X1336	1	X1337	1	X1338
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VCC	1	X1400	1	X1401	1	X1402	1	X1403	1	X1404	1	X1405	1	X1406	1	X1407	1	X1408	1	X1409	1	X1410	1	X1411	1	X1412	1	X1413	1	X1414	1	X1415	1	X1416	1	X1417	1	X1418	1	X1419	1	X1420
GND	2	X1400	2	X1401	2	X1402	2	X1403	2	X1404	2	X1405	2	X1406	2	X1407	2	X1408	2	X1409	2	X1410	2	X1411	2	X1412	2	X1413	2	X1414	2	X1415	2	X1416	2	X1417	2	X1418	2	X1419	2	X1420

VCC	1	X1420	1	X1421	1	X1422	1	X1423	1	X1424	1	X1425	1	X1426	1	X1427	1	X1428	1	X1429	1	X1430	1	X1431	1	X1432	1	X1433	1	X1434	1	X1435	1	X1436	1	X1437	1	X1438	1	X1439	1	X1440
GND	2	X1420	2	X1421	2	X1422	2	X1423	2	X1424	2	X1425	2	X1426	2	X1427	2	X1428	2	X1429	2	X1430	2	X1431	2	X1432	2	X1433	2	X1434	2	X1435	2	X1436	2	X1437	2	X1438	2	X1439	2	X1440

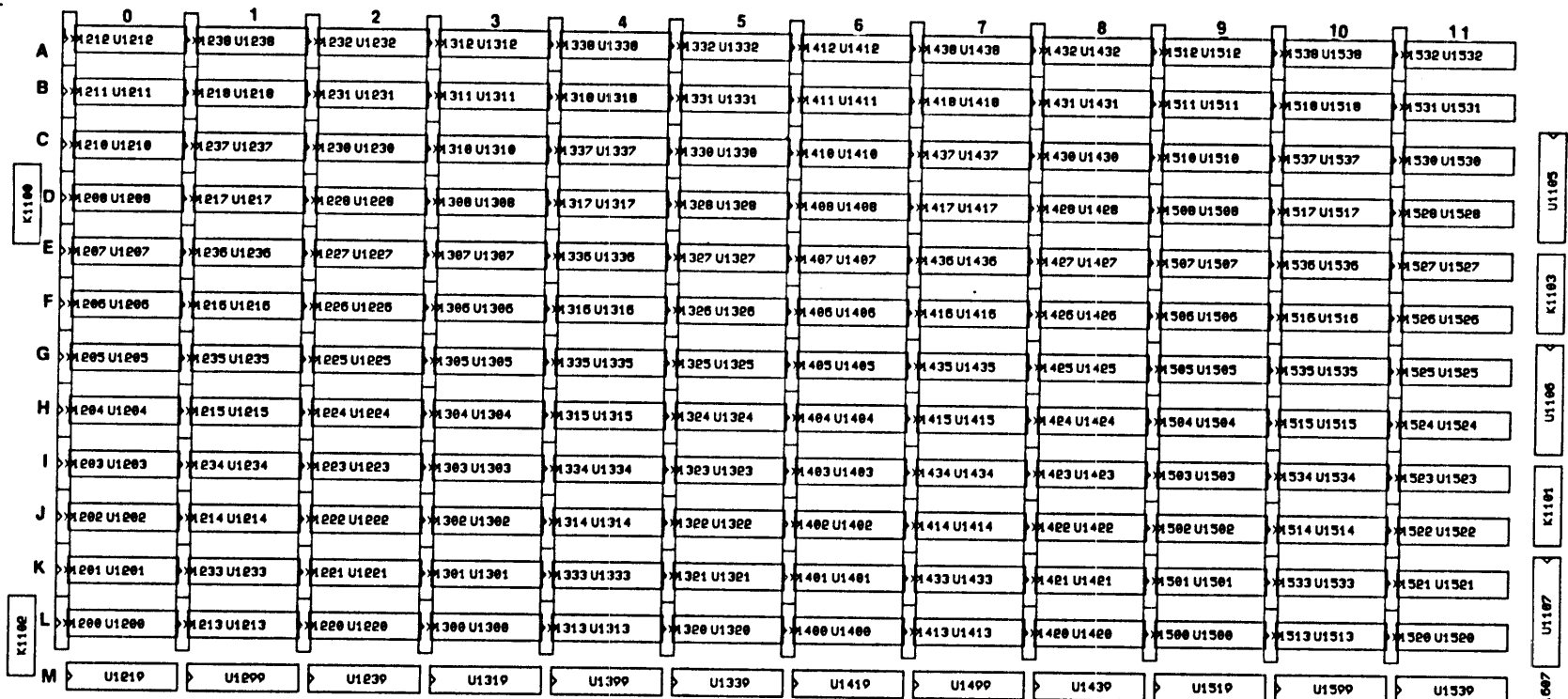


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GND	C 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF

VCC	X1520	X1521	X1522	X1523	X1524	X1525	X1526	X1527	X1528	X1530	X1531	X1532	X1533	X1534	X1535	X1536	X1537	X1538
GND	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF	D 1-1UF

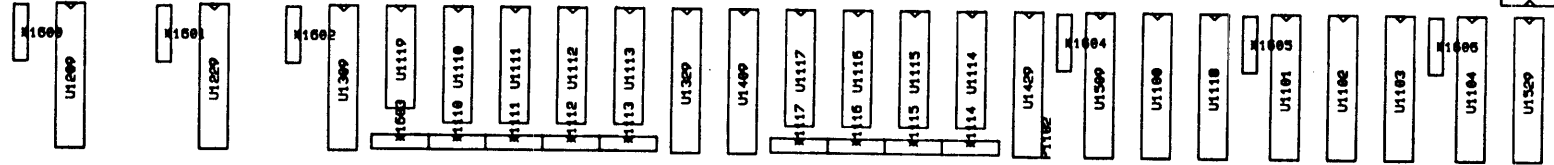


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