SUN 68000 Board Rev D

Documentation Package

February 28, 1982

VLSI SYSTEMS INC.

This is the engineering documention for the SUN graphics board. It includes:

How to read the logic diagrams:

Signal Definitions:

Negated logic signals, that is signals that are asserted active low, are indicated by a backslash "\" following the signal name.

For signals with multiple meanings or synonyms, the synonyms are listed separated by a slash "/". If a signal has multiple functions that are exclusive of each other, the names are listed separated by a vertical bar or "|".

For example, the signal name for a read-write signal that is active low for write is "READ/WRITE\". The inverted version of this signal would be "READ\/WRITE". A clock that is asserted either in state 3 or 5 will be marked: C.S3|5.

Often a group of signals share the same property. Such groups of signals typically share the same prefix, separated from a suffix with ".". For example, all signals driving the Multibus are prefixed with "B.".

Signals that are part of busses usually share the same prefix followed by a number. For example, the 16 data bus signals are labelled "D0", "D1", "D2", and so on up to "D15".

Clock signals names typically contain information about their nature as part of their signal name. There are two kinds of clocks:

1) periodic clocks that are labelled C##.##-##, where the first number is the clock period, the second number the beginning of the active clock phase, and the third number the end of the active clock phase.
2) clocks that derive from 68000 states. These clocks are labelled C.S# where # is the 68000 state they become active.
3) user-programmable clocks that are named according to their function, for example C.TIMER1 is the clock from timer 1.

Part Numbers:

Part Numbers consist of one letter followed by three digits. The letter indicates the type of component and is one of:

C	discrete Capacitor
J	Jumper of Connector
K	decoupling capacitor
M	Memory Chip
R	discrete Resistor
S	single-in-line component
U	dual-in-line component
X	Decoupling capacitor

The three digits give the approximate component position on the board, with the first digit indicating the row position and the last two digits

numbering the position along each row.

GENERIC	QTY	BRAND	PART NUMBER	DESCRIPTION
2148	7	INTEL	D2148H-3	1K-BY-4 STATIC RAM 55 NSEC
26LS29	1	AMD	AM26LS29PC	QUAD RS-423 DRIVER
26LS32	1	AMD	AM26LS32PC	QUAD DIFFERENTIAL LINE RECEIVER
2764	4	INTEL	D2764	8K-BY-8 EPROM
3622	1	SIG	N82S131	512-BY-4 BIPOLAR PROM
4164	36	ANY	4164	64K-BY-1 DYNAMIC RAM 200 NSEC
7201	1	NEC	UPD7201	DUAL UART
7406	1	TI	SN7405N	HEX BUFFER OPEN COLLECTOR OUTPUT
74LS04	1	TI	SN74LS04N	HEX INVERTER
74LS05	1	TI	SN74LS05N	HEX INVERTER OPEN COLLECTOR OUTPUT
74LS148	1	TI	SN74LS148N	8-LINE TO 3-LINE PRIORITY DECODER
74LS163	1	TI	SN74LS163N	BINARY SYNCHRONOUS 4-BIT COUNTER
74LS20	1	TI	SN74LS20	DUAL 4-INPUT NAND GATES
74LS244	3	TI	SN74LS244N	OCTAL NONINVERTED BUFFERS
74LS257	1	TI	SN74LS257N	QUAD DATA SELECTOR
74LS299	1	TI	SN74LS299N	EIGHT-BIT UNIVERSAL SHIFT REGISTER
74LS374	1	TI	SN74LS374N	OCTAL REGISTER
74LS534	3	AMD	SN74LS534N	OCTAL REGISTER INVERTING
74LS74	2	TI	SN74LS74	DUAL D-TYPE FLIPFLOPS
74S00	1	TI	SN74S00N	QUAD 2-INPUT NAND GATES
74S02	1	TI	SN74S02N	QUAD 2-INPUT NOR GATES
74S08	1	TI	SN74S08N	QUAD 2-INPUT AND GATES
74S08	1	TI	SN74S08N	QUAD 2-INPUT AND GATES
74S139	1	TI	SN74S139N	DUAL 2-TO-4 LINE DECODER
74S158	1	TI	SN74S158N	QUAD INVERTING 2-TO-1-LINE MUX
74S163	1	TI	SN74S163N	BINARY SYNCHRONOUS 4-BIT COUNTER
74S240	2	TI	SN74S240N	OCTAL INVERTING BUFFER
74S244	1	TI	SN74S244N	OCTAL NONINVERTED BUFFERS
74S288	2	TI	TBP18S030N	32-BY-8 BIPOLAR PROM
7660	1	INTSIL	ICL7660CPA	VOLTAGE INVERTER
8205	1	INTEL	P8205	3-TO-8 DECODER
8211	1	INTSIL	ICL8211CPA	PRECISION VOLTAGE COMPARATOR
8226	4	INTEL	P8226	QUAD BUS TRANSCEIVERS
8289	1	INTEL	D8289	MULTIMASTER BUS CONTROLLER
82S62	2	AMD	N82S62N	9-INPUT PARITY CHECKER
8303B	3	AMD/NAT	DP8303N	OCTAL INVERTING TRANSCEIVER
8304B	4	AMD/NAT	DP8304BN	OCTAL NON-INVERTING TRANCEIVER
AM2966	3	AMD	AM2966PC	OCTAL DYNAMIC RAM DRIVER
AM9513	1	AMD	AM9513PC	LSI TIMER
C	58	AVX	MD015C104MAA	DIPGUARD CAPACITORS 0.1 UF
J.50	2	AUGAT	110-50001-102	50-PIN PCB SOLDERTAIL HEADER
K1114A	1	MOTOROL	LOCOII-16MHZ	CRYSTAL OSCILLATOR
LS2518	1	AMD	AM25LS2518	QUAD D-REGISTER
MC68000	1	MOTOROL	MC68000L	CPU 8 MHZ
R7.SIP	3	BURNS	4308R-101-XXX	RESISTOR SIP, 7 RESISTORS
R9.SIP	5	BURNS	4310R-101-XXX	RESISTOR SIP, 9 RESISTORS

LOC	DIPTYPE	BODY	FILE	POS
C100	C	C	P4	B8
C101	C	C	P4	A8
C300	C	C	P4	B8
C301	C	C	P4	B8
C304	C	C	P4	D1
C400	C	C	P4	B5
C401	C	C	P4	B7
J1	J.50	J.50	P6	A2
J2	J.50	J.50	P6	A5
J100	J.8	J.8	P6	A7
J101	K.2	K.2	P6	B5
J102	K.2	K.2	P5	D8
J400	K.8	K.8	P6	C7
J800	J.4	J.4	P6	B7
J900	K.2	K.2	P3	D7
J901	J.10	J.10	P6	B7
J902	J.16	J.16	P6	A7
J903	J.4	J.4	P6	C7
K100	C	C	P6	D1
K106	C	C	P6	D2
K200	C	C	P6	D2
K201	C	C	P6	D3
K300	C	C	P6	D3
K400	C	C	P6	D4
K402	C	C	P6	D4
K403	C	C	P6	D5
K500	C	C	P6	D5
K501	C	C	P6	D1
K502	C	C	P6	D2
K700	C	C	P6	D2
K800	C	C	P6	D3
K801	C	C	P6	D3
K802	C	C	P6	D4
K900	C	C	P6	D4
K901	C	C	P6	D5
K902	C	C	P6	D5
M100	4164	4164	P2	A3
M101	4164	4164	P2	A4
M102	4164	4164	P2	A5
M103	4164	4164	P2	A6
M104	4164	4164	P2	A7
M105	4164	4164	P2	C3
M106	4164	4164	P2	C4
M107	4164	4164	P2	C5
M108	4164	4164	P2	C6
M200	4164	4164	P2	A4
M201	4164	4164	P2	A4
M202	4164	4164	P2	A5
M203	4164	4164	P2	A6

M204	4164	4164	P2	C7
M205	4164	4164	P2	C4
M206	4164	4164	P2	C4
M207	4164	4164	P2	C5
M208	4164	4164	P2	C6
M300	4164	4164	P2	B3
M301	4164	4164	P2	B4
M302	4164	4164	P2	B5
M303	4164	4164	P2	B6
M304	4164	4164	P2	B7
M305	4164	4164	P2	D3
M306	4164	4164	P2	D4
M307	4164	4164	P2	D5
M308	4164	4164	P2	D6
M400	4164	4164	P2	B4
M401	4164	4164	P2	B4
M402	4164	4164	P2	B5
M403	4164	4164	P2	B6
M404	4164	4164	P2	D7
M405	4164	4164	P2	D4
M406	4164	4164	P2	D4
M407	4164	4164	P2	D5
M408	4164	4164	P2	D6
R300	R	R	P4	D1
R301	R	R	P4	D1
R302	R	R	P4	D1
R900	R	R	P3	D7
S100	R9.SIP	R9.SIP	P3	C1
S101	R9.SIP	R9.SIP	P3	C1
S102	R9.SIP	R9.SIP	P4	D6
S600	R9.SIP	R9.SIP	P1	D2
S601	R7.SIP	R7.SIP	P1	D3
S602	R7.SIP	R7.SIP	P1	D4
S603	R7.SIP	R7.SIP	P1	D6
S900	R9.SIP	R9.SIP	P5	D3
U100	26LS32	26LS32	P4	A7
U101	2764	2764	P3	A1
U102	2764	2764	P3	A3
U103	2764	2764	P3	A2
U104	2764	2764	P3	A5
U105	7201	7201	P4	A4
U106	AM2966	AM2966	P2	A1
U107	74LS244	74LS244	P3	C2
U108	74LS244	74LS244	P3	C2
U109	7406	7406	P4	C5
			P4	C3
			P4	D2
			P4	D4
U110	74LS74	74LS74	P5	C8
			P5	D7
U200	26LS29	26LS29	P4	B7
U201	82S62	82S62	P5	C4
U202	82S62	82S62	P5	C4
U203	74S02	74S02	P5	C5
		74S02\	P5	C7

		74S02	P5	C3
			P5	C3
U300	74LS04	74LS04	P5	A5
			P5	A4
			P4	B6
			P4	B6
			P4	A6
			P4	B6
U301	AM9513	9513	P4	A2
U302	8211	8211	P4	D2
U400	7660	7660	P4	B6
U401	K1114A	K1114A	P5	A1
U402	MC68000	68000	P1	B1
U403	LS2518	LS2518	P1	A1
U404	2148	2148	P1	A5
U405	2148	2148	P1	A3
U406	2148	2148	P1	A4
U407	AM2966	AM2966	P2	C1
U408	8226	8226	P2	A8
U409	8226	8226	P2	B8
U410	8226	8226	P2	C8
U411	8226	8226	P2	D8
U500	74S158	74S158	P5	B6
U501	74S240	74S240	P1	C5
U502	74S288	74S288	P1	C3
U503	3622	3622	P1	C7
U504	8304B	8304B	P1	A7
U505	8304B	8304B	P1	A7
U600	74LS163	74LS163	P5	A5
U601	74LS299	74LS299	P5	A7
U602	74S288	74S288	P1	C3
U603	74LS05	74LS05	P4	D3
			P4	C3
			P4	C3
			P4	D1
			P4	C8
			P4	C8
U604	2148	2148	P1	B6
U605	2148	2148	P1	B5
U606	2148	2148	P1	B3
U607	2148	2148	P1	B4
U611	AM2966	AM2966	P2	B1
U700	74LS20	74LS20\	P5	B4
		74LS20	P5	B3
U701	74S163	74S163	P5	A3
U702	74LS74	74LS74	P3	C5
			P4	D6
U703	74LS257	74LS257	P1	C5
U800	8205	8205	P1	D7
U801	74S00	74S00	P5	B3
		74S00\	P5	B4
			P1	D7
		74S00	P1	D7
U802	74S08	74S08\	P3	C8
		74S08	P3	C8

			P4	D8
		74S08\	P1	D7
U804	8304B	8304B	P1	C7
U805	8304B	8304B	P1	B7
U900	74LS244	74LS244	P3	C4
U901	74S244	74S244	P3	C6
U902	8289	8289	P3	D4
U903	74S240	74S240	P3	C8
U904	74LS534	74LS534	P3	B6
U905	74LS374	74LS374	P5	D5
U906	74LS148	74LS148	P5	D7
U907	74LS534	74LS534	P3	A6
U908	74LS534	74LS534	P3	A6
U909	8303B	8303B	P3	A8
U910	8303B	8303B	P3	B8
U911	8303B	8303B	P3	A8
U912	74S139	74S139	P2	D1
			P3	C6
X100	C	C	P6	C1
X101	C	C	P6	C2
X102	C	C	P6	C2
X103	C	C	P6	C3
X104	C	C	P6	C3
X105	C	C	P6	C4
X106	C	C	P6	C4
X107	C	C	P6	C5
X108	C	C	P6	C5
X200	C	C	P6	D1
X201	C	C	P6	D2
X202	C	C	P6	D2
X203	C	C	P6	D3
X204	C	C	P6	D3
X205	C	C	P6	D4
X206	C	C	P6	D4
X207	C	C	P6	D5
X208	C	C	P6	D5
X300	C	C	P6	D1
X301	C	C	P6	D2
X302	C	C	P6	D2
X303	C	C	P6	D3
X304	C	C	P6	D3
X305	C	C	P6	D4
X306	C	C	P6	D4
X307	C	C	P6	D5
X308	C	C	P6	D5
X400	C	C	P6	D1
X401	C	C	P6	D2
X402	C	C	P6	D2
X403	C	C	P6	D3
X404	C	C	P6	D3
X405	C	C	P6	D4
X406	C	C	P6	D4
X407	C	C	P6	D5
X408	C	C	P6	D5

Mnemonic	Description
A0..A23	68000 Address Bus
ACK\	Acknowledge
AEN	Address Enable
AS	68000 Address Strobe
B.A0\..A19\	Multibus address bus (20)
B.AACK\	UNUSED, Multibus advanced acknowledge
B.BCLK\	Multibus bus clock
B.BHEN\	Multibus byte high enable
B.BPRN\	Multibus priority in
B.BPRO\	Multibus priority out
B.BREQ\	Multibus bus request
B.BUSY\	Multibus busy
B.CBRQ\	Multibus common bus request
B.CCLK\	Multibus constant clock
B.D0\..D15\	Multibus data bus (16)
B.INH1\..2\	Multibus inhibit lines
B.INIT\	Multibus init
B.INT0\..INT7\	Multibus interrupt request
B.INTA\	UNUSED Multibus interrupt acknowledge
B.IORC\	Multibus I/O read control
B.IOWC\	Multibus I/O write control
B.MRDC\	Multibus memory read control
B.MWTC\	Multibus memory write control
B.XACK\	Multibus trasfer acknowledge
BCLK\	Onboard Bus Clock
INIT\	Onboard INIT
B/L\	Bus/Local\
BERR	Bus Error
BHEN	Bus High Enable
BOOT	Boot
BOOTREAD	Boot and Read
C.P1	Clock Serial Port 1
C.P2	Clcck Serial Port 2
C.REFRESH	Clock Refresh
C.TIMER1	Clock Timer 1
C.TIMER2	Clock Timer 2
CAS0\..3\	Column Address Strobe 0..3
CE.BYTE\	Chip Enable Byte Buffer
CE.PMAP\	Chip Enable Page Map
CE.PROM0\	Chip Enable PROM Set 0
CE.PROM1\	Chip Enable PROM Set 1
CE.SIO\	Chip Enable Serial I/O
CE.SMAP\	Chip Enabel Segment Map
CE.SPARE\	UNUSED
CE.WORD\	Chip Enable Word Buffer
CEN\	Multibus Control Enable
CLR.BOOT\	Clear Boot State
CTSA\	Clear to Send Port A
CX0..3	Context Register (4)

D0..15	Data Bus (16)
DCDA\	Data Carrier Detect Port A
DIRTY	Modify Bit in Page Map
DS	Data Strobe
DTACK	Data Transfer Acknowledge
DTRA\	Data Terminal Ready Port A
EN.PMAX\	Enable Page Map Extension
FC0..2	68000 Function Codes (3)
HALT\	68000 Halt
HARDRESET	Power On Reset
IN0..16	Input Port (16)
INIT	Onboard INIT
INT.SIO\	Interrupt Serial I/O
INT.TIMER2\	Interrupt Timer 2
INT1S\..7S\	Interrupt Synchronized (7)
IO/M\	IO/Memory\
IPL0\	68000 Interrupt Priority Level (3)
LDS	Lower Data Strobe
M.A0\..A7\	Memory Address Bus
M.CAS0\..CAS3\	Memory Column Address Strobes (4)
M.DI0..M.DI15	Memory Data In Bus (16)
M.DIL	Memory Data In Parity Lower
M.DIU	Memory Data In Parity Upper
M.DO0..M.DO15	Memory Data Out Bus (16)
M.DOL	Memory Data Out Parity Lower
M.DOU	Memory Data Out Parity Upper
M.RASL\	Memory Row-Address Strobe Lower
M.RASU\	Memory Row-Address Strobe Upper
M.REF\	Memory Refresh
M.WE\	Memory Write Enable Strobe
MA11..22	Mapped Address (12)
MRDC\	Memory Read Control
MWTC\	Memory Write Control
OE.CX\	Output Enable Context Register
OE.PORT\	Output Enable Port
OE.RAM\	Output Enable RAM
OE.TIMER\	Output Enable Timer
P1.CTS	Port1 Clear To Send
P1.DSR	Port1 Data Set Ready
P1.DTR	Port1 Data Terminal Ready
P1.RTS	Port1 Ready To Send
P1.RXD	Port1 Receiver Data
P1.TXD	Port1 Transmitter Data
P2.RXD	Port2 Receiver Data
P2.TXD	Port2 Trasmitter Data
PAR.EN	Parity Enable
PAR.ERR	Parity Error
PARERRL	Parity Error Lower
PARERRU	Parity Error Upper
PMAP.ERR\	Page Map Error
PROT0..3	Protection (4)
PU..PU3	Pull-up
R/W\	Read/Write\
RDD\	Read Data from Multibus
RESET	68000/7201 Reset

RTSA\	Ready To Send A
RXDA	Receive Data A
RXDB	Receive Data B
SET.INIT\	Set Init\
SMAP.ERR\	Segment Map Error
SYS.ACCESS\	System Access
TIMEOUT	Timeout Error
TXDA	Transmit Data Port A
TXDB	Transmit Data Port B
UDS	Upper Data Strobe
USED	Used (Accessed) Bit in Page Map
VCC	+5V
VEE	-5V
WE.CX\	Write Enable Context Register
WE.PMAP\	Write Enable Page Map
WE.PMAX\	Write Enable Page Map Extension
WE.RAM\	Write Enable RAM
WE.SMAP\	Write Enable Segment Map
WE.TIMER\	Write Enable Timer
XA15..20	Intermediate Address (6)
XACK	Transfer Acknowledge

On-board Device Addresses

All addresses are in hexadecimal.
The actual amount of physical RAM and PROM depends on the system configuration.
Note that unused address bits are not further decoded.
All locations are read and write, except those explicitely marked.

Address	Data	Description
000000..1FFFFF	0..15	Logical address space. (Write-Only during boot).
000000..03FFFF	0..15	PROM0 during boot state (Read-Only).
200000..FFFFFF	0..15	System address space (available to supervisor only).
200000..23FFFF	0..15	On-Board PROM0 (Read-Only). Exit boot state (Write-Only).
400000..43FFFF	0..15	On-board PROM1.
600000..600006	8..15	UART
		600000 Uart A Data Register 600002 Uart A Command Register 600004 Uart B Data Register 600006 Uart B Command Register
800000..800002	0..15	Timer
		800000 Timer Data Register 800002 Timer Command Register
A00000..BFF800	0..15	Page Map.
	0..11	Physical Address Bits 11..22
	12..13	Physical Address Space 0 - On-board RAM 1 - Non-existing page 2 - Multibus memory space 3 - Multibus I/O space
	14	Modified Bit
	15	Accessed Bit
		The page map is addressed through the segment map and via address bits A11..A14 from the processor. The lower order 11 address bits are ignored. When the segment map is initialized to idendity, page n is located at address A00000 + n * 2↑11.
		A00000 Page 0 A00800 Page 1

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                        ...
                        BFF800  Page 3FF

C00000..DFF800  0..15   Segment Map

                0..5    Virtual address bits 15..20
                6..7    Reserved for future use
                8..11   Protection bits
                12..15  Current Context (Read-Only)

                        Segment n is located at address C00000 + n * 2↑15.
                        The lower order 15 address bits are discarded.

                        C00000  Segment 0
                        C08000  Segment 1
                        ...
                        DF8000  Segment 3F

E00000          0..15   16-bit input port (Read-Only)
                12..15  4-bit context register (Write-Only)
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Connectors, Cables, and Jumpers:

".." indicates a connector pair

"::" indicates default (pre-wired) connection

J1-Connector:

Prewired to be a DCE on Port 1 and a DTE on Port 2.

VCC	J1-01	Serial Port 1 Pin 25, +5 Volt
P1.TXD	J1-03	Serial Port 1 Pin 2, Transmit Data
P1.RXD	J1-05	Serial Port 1 Pin 3, Receive Data
P1.GND	J1-13	Serial Port 1 Pin 7, Signal Ground
SET.INIT\	J1-18	Serial Port 1 Pin 18, Set.INIT\
P2.TXD	J1-28	Serial Port 2 Pin 2, Transmit Data
P2.RXD	J1-30	Serial Port 2 Pin 3, Receive Data
P2.GND	J1-38	Serial Port 2 Pin 7, Signal Ground

J1-Cable:

Use a 50-wire flat cable and split it into two 25-wire strands. Connect a female DB-25 flat cable connector pin 1 to wire 1 of cable (terminal side) and connect a male DB-25 flat cable connector pin 1 to wire 25 of cable (computer side).

J2-Connector:

IN0	J1-01	Input Bit 0
IN1	J1-03	Input Bit 1
IN2	J1-05	Input Bit 2
IN3	J1-07	Input Bit 3
IN4	J1-09	Input Bit 4
IN5	J1-11	Input Bit 5
IN6	J1-13	Input Bit 6
IN7	J1-15	Input Bit 7
IN8	J1-17	Input Bit 8
IN9	J1-19	Input Bit 9
IN10	J1-21	Input Bit 10
IN11	J1-23	Input Bit 11
IN12	J1-25	Input Bit 12
IN13	J1-27	Input Bit 13
IN14	J1-29	Input Bit 14
IN15	J1-31	Input Bit 15
SET.INIT\	J1-45..46	Active contact of INIT toggle
M.REF\	J1-47	Halt indicator output
VCC	J1-49	Halt indicator supply

P2 Serial Port:

Prewired to be a DTE on Port 2.

P2.RxD	J100-1::2	Connects P2.RxD as DTE
P2.TxD	J100-3::4	Connects P2.TxD as DTE
P2.RxD	J100-1..3	Connects P2.RxD as DCE
P2.TxD	J100-2..4	Connects P2.TxD as DCE

PROM Type:

Prewired for 2732/2764 EPROMs.

2764/2732	J100-7::8	Connects U101::U104(23) to A12
2716	J100-5..6	Connects U101::U104(23) to VCC

Multibus Signals:

Prewired for a system where the 68000 is reset-master and clock-master.

B.INIT\	J901-1..2	Drive INIT from Multibus Remove J901-3::4 if used.
B.INIT\	J901-3::4	Drives INIT to Multibus
B.BCLK\	J901-5::6	Drives BCLK to Multibus
B.BPRN\	J901-7::8	Grounds BPRN for last master in chain.
B.CCLK\	J901-9::10	Drives CCLK to Multibus
B.MRDC\	J900-1..2	Connect for operation without 8218.
B.MWTC\	J900-3..4	Connect for operation without 8218.
B.IORC\	J900-5..6	Connect for operation without 8218.
B.IOWC\	J900-7..8	Connect for operation without 8218.
ADEN\	J900-9..10	Connect for operation without 8218.

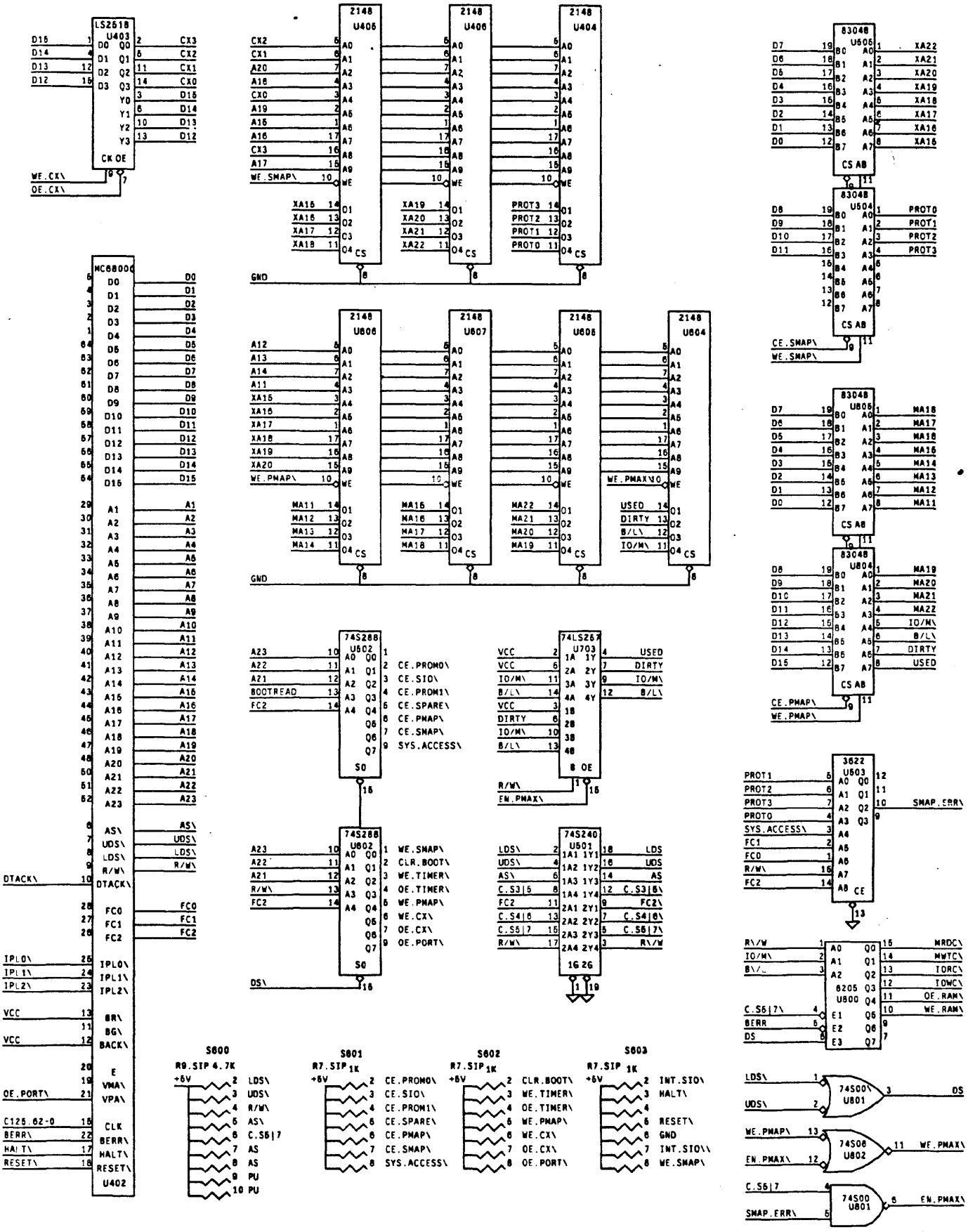
Interrupt Level Assignment:

Prewired to standard interrupt assignments
with on-board interrupts isolated from Multibus.

B.INT7	J902-1..2	non-maskable interrupt, used by refresh timer
B.INT6	J902-3..4	used by on-board Timer2
B.INT5	J902-5..6	used by on-board UART
B.INT4	J902-7::8	
B.INT3	J902-9::10	
B.INT2	J902-11::12	
B.INT1	J902-13::14	
B.INT0	J902-15::16	not used

Memory expansion board:

M.CAS0\	J903-1..3	Drives M.CAS0\ from M.CAS2\
M.CAS1\	J903-2..4	Drives M.CAS1\ from M.CAS3\



TITLE	FILE	DATE	PAGE	OF
(C) 1981 VSI, SUN 68000, CPU,	P1[SUNAVB]	10-Jan-82 15:31	1	7

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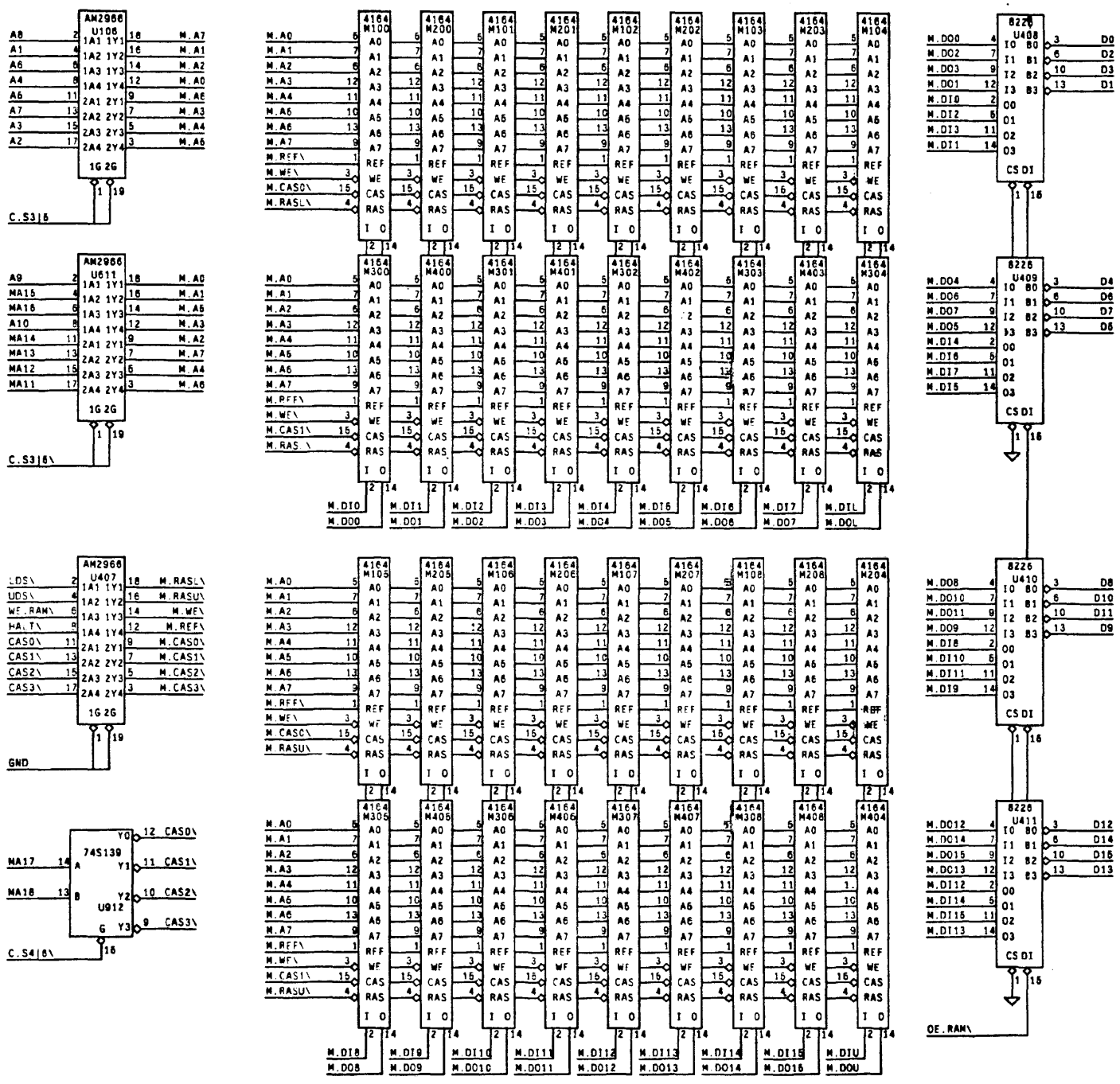

TITLE	FILE	DATE	PAGE	OF
(C) 1981 VSI, SUN 68000, RAM,	P2[SUNAVB]	10-Jan-82 15:32	2	7

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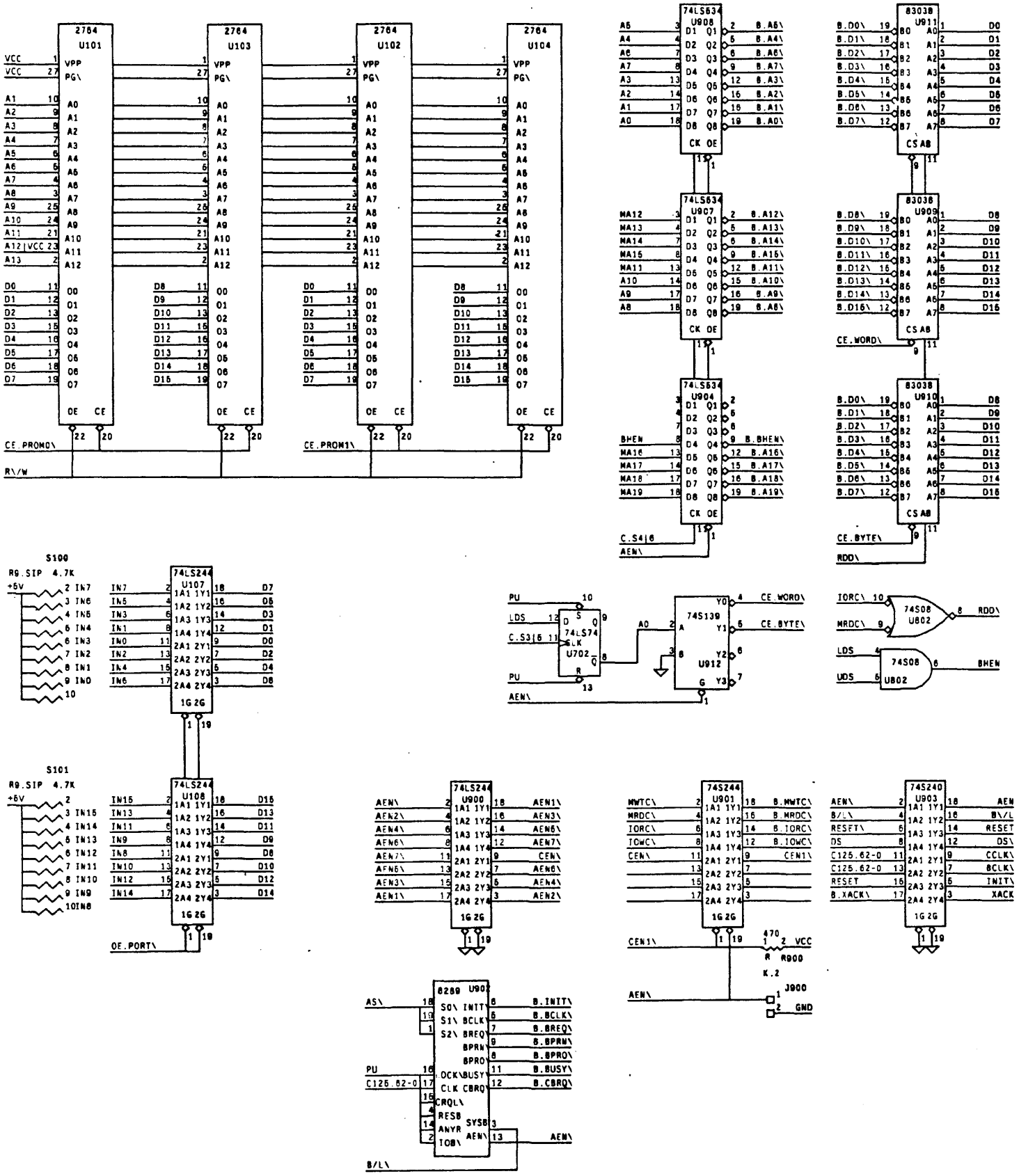

TITLE	FILE	DATE	PAGE	OF
(C) 1981 VSI, SUN 68000, MULTIBUS INTERFACE,	P3[SUNAVB]	10-Jan-82 15:33	3	7

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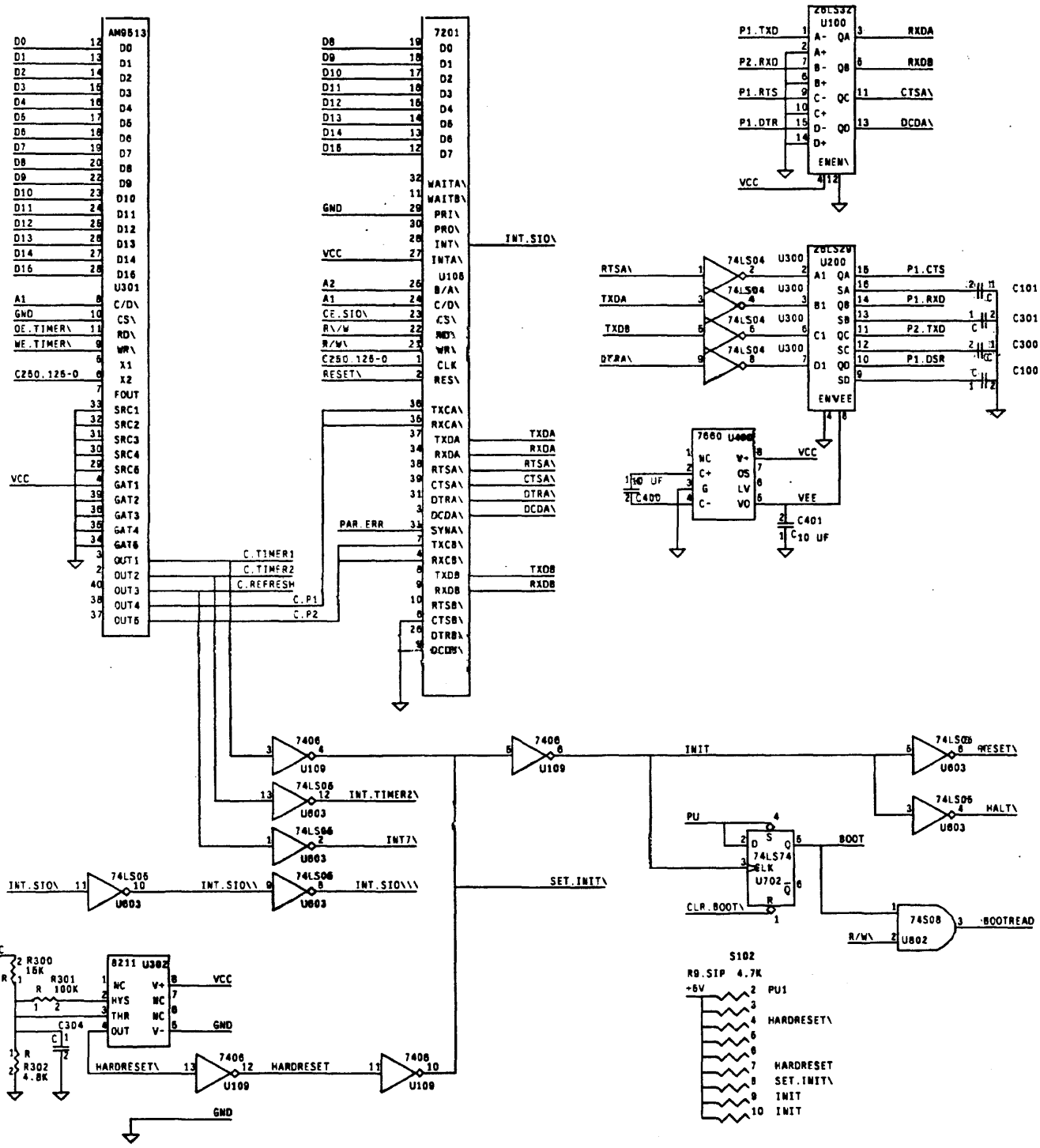

TITLE	FILE	DATE	PAGE	OF
(C) 1981 VSI, SUN 68000, I/O AND INIT,	P4 [SUNAVB]	10-Jan-82 16:41	4	7

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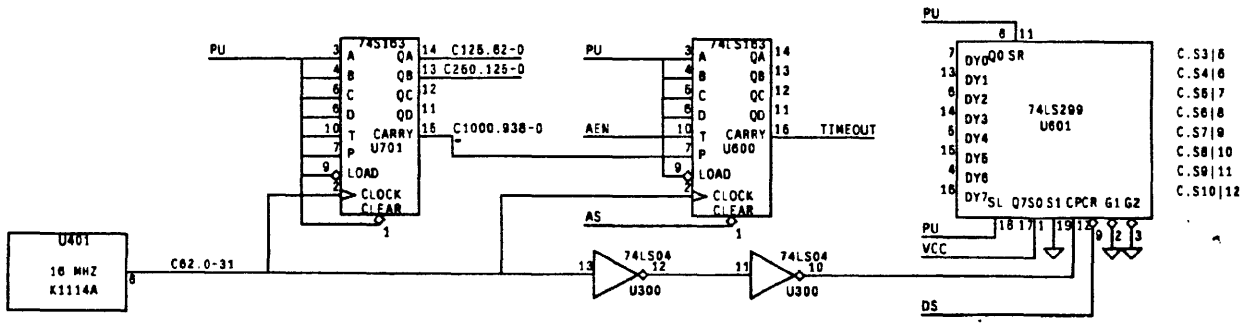

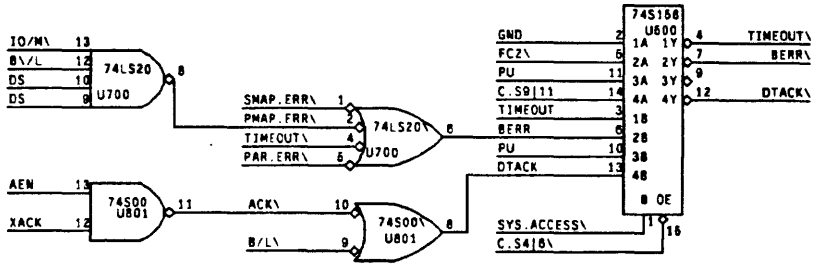

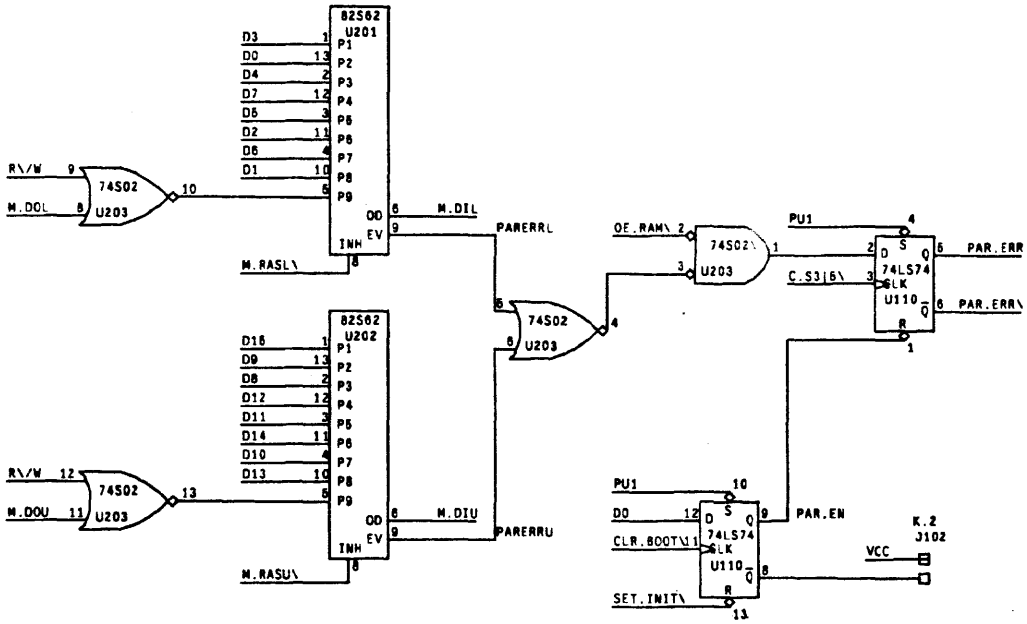

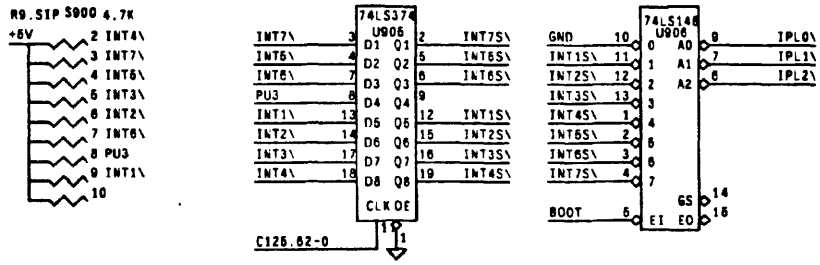

TITLE	FILE	DATE	PAGE	OF
(C) 1981 VSI, SUN 68000, CLOCK AND CONTROL,	P5[SUNAVB]	10-Jan-82 15:34	5	7

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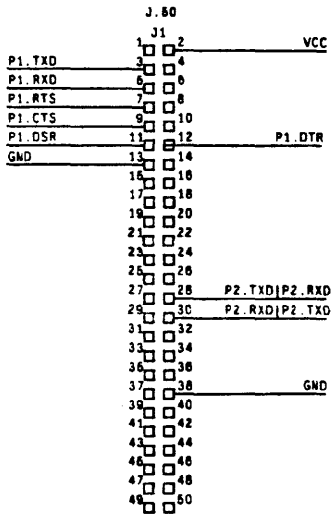
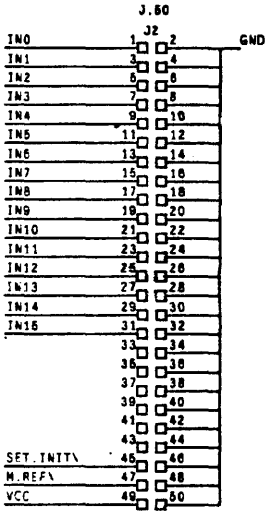
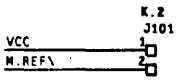
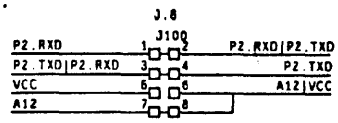
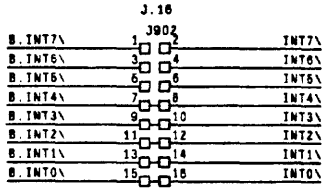
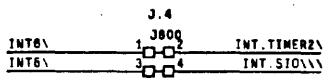


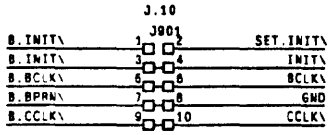


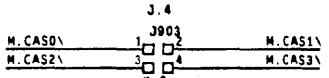


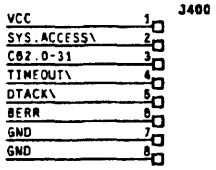


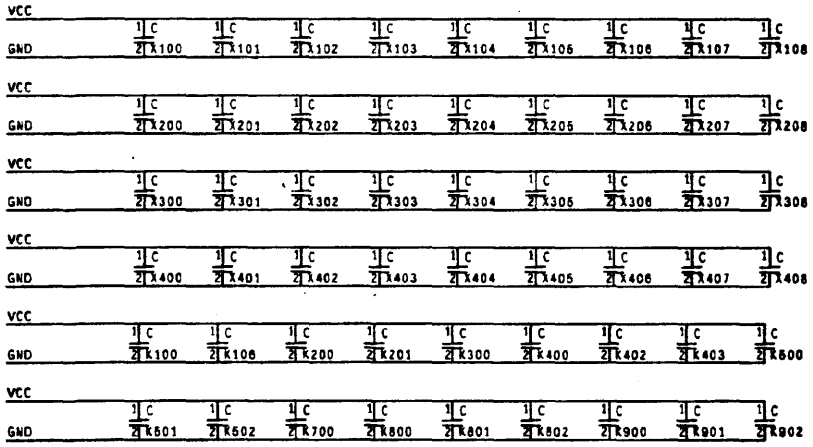




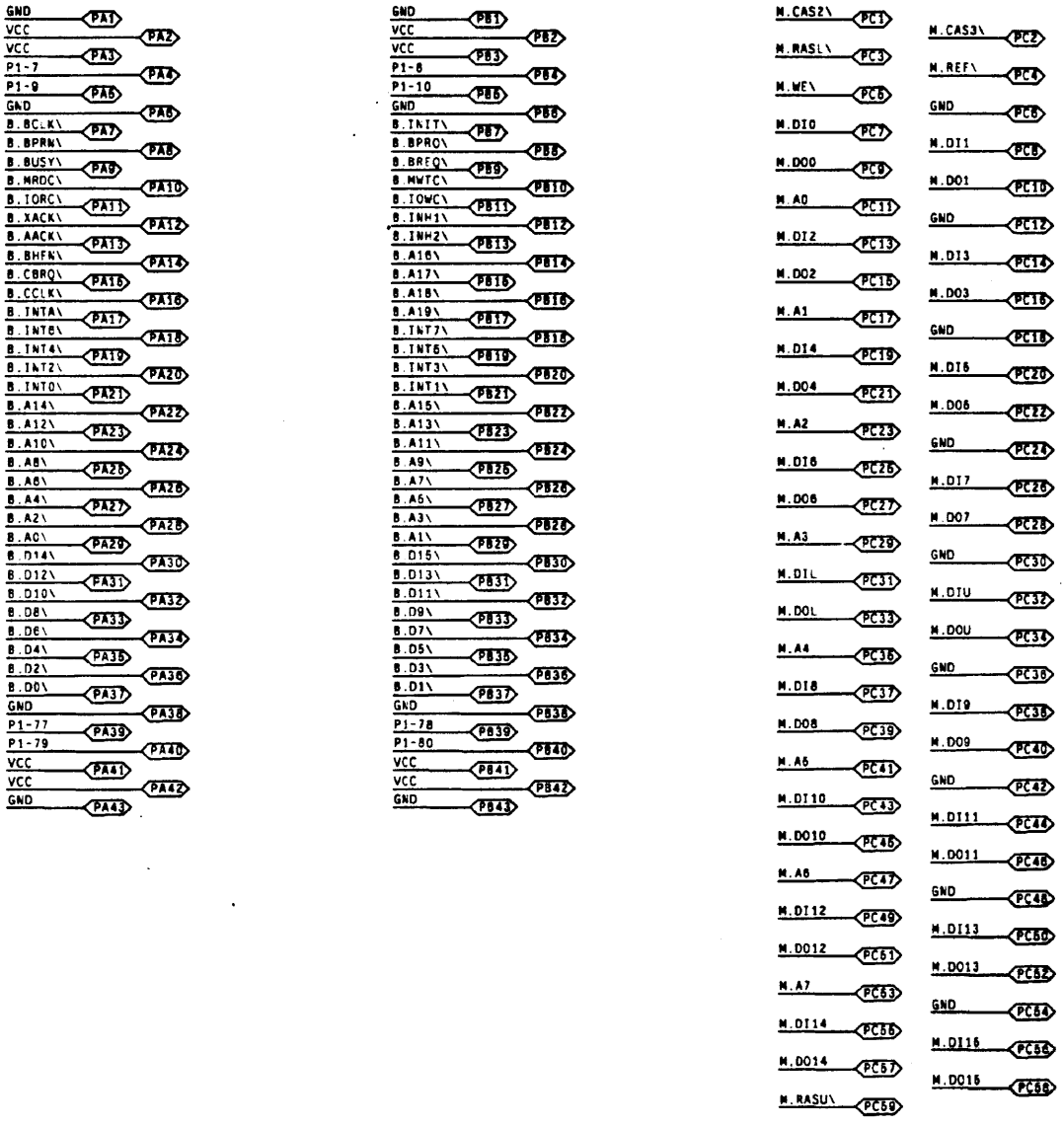








TITLE	FILE	DATE	PAGE	OF
(C) 1981 VSI, SUN 68000, J-CONNETORS,	P6[SUNAVB]	10-Jan-82 16:38	6	7



TITLE	FILE	DATE	PAGE	OF
(C) 1981 VSI, SUN 68000, P-CONNECTORS,	P7[SUNAVB]	10-Jan-82 15:36	7	7

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```
comment Proprietary VLSI SYSTEMS INC.;
begin "p0"
require "prom.sai" sourcefile;
$32;

define

a23     =[a0],
a22     =[a1],
a21     =[a2],
boot    =[a3],
fc2     =[a4],

adrs    =[(cvb(a23)*d2 + cvb(a22)*d1 + cvb(a21)*d0)],

s.access=[(boot ∨ (adrs > 0))],
ce.prom0=[(fc2 ∧ ((adrs=1) ∨ boot ∧ (adrs=0)))],
ce.prom1=[(fc2 ∧ (adrs=2))],
ce.sio  =[(fc2 ∧ (adrs=3))],
ce.timer=[(fc2 ∧ (adrs=4))],
ce.pmap =[(fc2 ∧ (adrs=5))],
ce.smap =[(fc2 ∧ (adrs=6))];

prombegin

prom(0, d0,     ¬ce.timer);
prom(0, d1,     ¬ce.prom0);
prom(0, d2,     ¬ce.sio);
prom(0, d3,     ¬ce.prom1);
prom(0, d4,     0);
prom(0, d5,     ¬ce.pmap);
prom(0, d6,     ¬ce.smap);
prom(0, d7,     ¬s.access);

promend;
writeprom("p0",0);
end;
```

```
comment Proprietary VLSI SYSTEMS INC.;
begin "p1"
require "prom.sai" sourcefile;
$32;

define

a23     =[a0],
a22     =[a1],
a21     =[a2],
read    =[a3],
fc2     =[a4],

adrs    =[(cvb(a23)*d2 + cvb(a22)*d1 + cvb(a21)*d0)],
write   =[(¬read)],

clr.boot=[(fc2 ∧ write ∧ (adrs=1))],
oe.timer=[(fc2 ∧ read  ∧ (adrs=4))],
we.timer=[(fc2 ∧ write ∧ (adrs=4))],
we.pmap =[(fc2 ∧ write ∧ (adrs=5))],
we.smap =[(fc2 ∧ write ∧ (adrs=6))],
oe.cx   =[(fc2 ∧ read  ∧ (adrs=6))],
we.cx   =[(fc2 ∧ write ∧ (adrs=7))],
oe.port =[(fc2 ∧ read  ∧ (adrs=7))];

prombegin

prom(0, d0,     ¬we.smap);
prom(0, d1,     ¬clr.boot);
prom(0, d2,     ¬we.timer);
prom(0, d3,     ¬oe.timer);
prom(0, d4,     ¬we.pmap);
prom(0, d5,     ¬we.cx);
prom(0, d6,     ¬oe.cx);
prom(0, d7,     ¬oe.port);

promend;
writeprom("p1",0);
end;
```

```
comment Proprietary VLSI SYSTEMS INC.;
begin "p2"
require "prom.sai" sourcefile;
$512;

define

prot1           =[a0],
prot2           =[a1],
prot3           =[a2],
prot0           =[a3],
sys.access.i    =[a4],
fc1             =[a5],
fc0             =[a6],
read            =[a7],
fc2             =[a8],

prot            =[(cvb(prot0)*d0
                  +cvb(prot1)*d1
                  +cvb(prot2)*d2
                  +cvb(prot3)*d3)],
sys.access      =[(¬sys.access.i)],
execute.cycle   =[( fc1 ∧ ¬fc0 ∧ read)],
read.cycle      =[(¬fc1 ∧  fc0 ∧ read)],
write.cycle     =[(¬fc1 ∧  fc0 ∧¬read)],

protcode        =[(case prot of (
                "_____",
                "__x__",
                "r____",
                "r_x__",
                "rw___",
                "rwx__",
                "r__r_",
                "rw_r_",
                "r__rw",
                "rw_rw",
                "rw_r_x",
                "rw_rwx",
                "r_xr_x",
                "rwxr_x",
                "rwx__x",
                "rwxrwx")
                )],

en.access       =[(¬sys.access ∧ (
                  fc2 ∧ read.cycle ∧ protcode[1 for 1]="r"
                ∨ fc2 ∧ write.cycle ∧ protcode[2 for 1]="w"
                ∨ fc2 ∧ execute.cycle ∧ protcode[3 for 1]="x"
                ∨¬fc2 ∧ read.cycle ∧ protcode[4 for 1]="r"
                ∨¬fc2 ∧ write.cycle ∧ protcode[5 for 1]="w"
                ∨¬fc2 ∧ execute.cycle ∧ protcode[6 for 1]="x"
                ))];

prombegin

prom(0, d0,     0);
prom(0, d1,     0);
prom(0, d2,     en.access);
prom(0, d3,     ¬en.access);

promend;
writeprom("p2",0);
end;
```

```
:10000000EF6F6F6F6F6F6F6F6F6F6F6F6F6F6F80
:10001000EF6E672F6D4F6B6F6D6E672F6D4F6B6F50
:0000000000
```

```
:10000000FFFFFFFFFFFFFFFFFFFFFFFFFFFFFF00
:10001000FFFBFFFEFDEFFFDFFFF7FFBFFFFFFF7FEF
:0000000000
```

```
:10000000080808080808080808080808080808080870
:10001000080808080808080808080808080808080860
:10002000080808080808080808080808080808080850
:10003000080808080808080808080808080808080840
:10004000080808080808080808080808080808080830
:10005000080808080408080808080808040408043O
:10006000080808080808080808080808080808080810
:10007000080808080808080808080808080808080800
:100080000808080808080808080808080808080808F0
:100090000808080808080808080808080808080808E0
:1000A0000808080808080808080808080808080808D0
:1000B0000808080804040408080808080404040D8
:1000C000080808080808080808080808080808080B0
:1000D000080808040404040808080804040404040C4
:1000E000080808080808080808080808080808080890
:1000F000080808080808080808080808080808080880
:10010000080808080808080808080808080808086F
:10011000080808080808080808080808080808085F
:10012000080808080808080808080808080808084F
:10013000080808080808080808080808080808083F
:10014000080808080808080808080808080808082F
:10015000080804080804080408080404040404043
:1001600008080808080808080808080808080808080F
:1001700008080808080808080808080808080808FF
:10018000080808080808080808080808080808EF
:10019000080808080808080808080808080808DF
:1001A0000808080808080808080808080808080CF
:1001B000080808080808040404040408080404DB
:1001C000080808080808080808080808080808AF
:1001D000080404040404040804040404040404D7
:1001E000080808080808080808080808080808088F
:1001F000080808080808080808080808080808087F
:0000000000
```