DIGITAL DESIGNS
TVT-II
32 TO 64 CHARACTER/LINE MODIFICATION

If you are using your TVT-II as a computer I/0 you may have found the 32 character/line format somewhat limiting. By making minor modifications to the TVT-II board you can lengthen the 32 character line to 64 characters/line and thereby expand your system's capabilities.

The TVT-II memory is continuously being addressed through nine address lines to generate the video data used by the television display. The tenth address line (A9) is used to switch from page one to page two. By using the A9 address line for continuous addressing, the TVT-II can be modified to display 64 characters/line. Since the additional 512 characters being displayed are what used to be page two, additional memory will have to be added to provide storage of a second page.

HOW IT WORKS

The basic design of the TVT-II make the modifications required to make it display 64 characters/line quite simple. IC21 and IC14 on the main TVT-II board normally count up 32 characters and upon reaching the 33rd count pin 11, IC14 and address A0 go high which disables the "dot clock" until the next line is started. Being in the 33rd character position also enables the video blanking circuit through IC12C and IC5B. With the "dot clock" disabled and the video blanking circuit enabled the line is blanked until a new line is started. By allowing the video generation and the "dot clock" to continue operating until the 65th character position is reached, 64 characters/line will be counted. This can be done by disconnecting pin 11, IC14 from the video blanking circuit and connecting it to address line A9, after having disconnected A9 from the page l-2 flip-flop. Pin 11, IC14 is also tied to pin 14, the input of the unused counter in IC14 whose output (pin 12) is then tied to the video blanking circuit. Thus we have effectively added an additional 32 counts to the address lines through pin 12, IC14 and transferred the video blanking function to the 65th character position through pin 12. Since the RC oscillator network of the "dot clock" IC18B was originally tuned for 32 characters/line, capacitor C4 will have to be replaced with an 18 pF unit to provide the dot rate required for 64 characters/line.

Since we are now addressing the memory continuously through ten address lines/page, the cursor compare circuitry must be modified to provide comparison of the A9 address bit. This modification will require providing an additional cursor position count bit and a comparator. The designer used a 74193 BCD counter to allow preloading the additional cursor bit through a computer cursor position interface tend still minimize the components required. The additional 74193 (IC1 FIGURE 1) is attached to the carry and borrow bits of the original cursor counter IC35 after disconnecting them from the 5th bit flip-flop IC27A. Carry and borrow bits are generated by the new counter through NAND gates IC4A, and IC4B and are sent to the original 5th

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bit flip-flop IC27A. The cursor count bit generated by IC1 is tied to pin 15, IC42 on the main board and compared with the A4 address bit. The output of the 5th bit flip-flop IC27A which was originally compared with the A4 address is brought on to the new circuitry and compared with address A9 by the comparator IC2. The cascaded "=" pulse from IC42 on the main board is inputted to IC2 whose output "=" pulse is sent to IC41. Thus we have provided an additional cursor count bit which is compared with address A4. Our new A9 address is compared to the old 5th bit flip-flop whose output has now become the 6th bit count. IC42 and IC41 on the main board IC2 in the new circuit provide the compare pulse required to position the cursor on the 64 character line.

Since we are now addressing the full 1024 addresses in the memory continuously, an additional six 2102's will be required to store a second page of data. By tying the CE gins of each group of memories to pins 8 and 9 of the page flip-flop IC27B the pages will role over as originally designed.

ASSEMBLY

The modifications will require cutting the foil traces at several points on the main board. This can be done quite easily with a single edge razor blade. Care should be taken to avoid getting the small pieces of foil removed in between the pins of the ICs on the board. Several jumper wires must be installed from the main board to the auxiliary cursor count board. These jumpers should be made with 26 Ga. or finer insulated wire cut as short as possible. Loops and crossovers should be avoided to minimize noise.

To provide the 64 character count the following connections should be made on the main board.

( ) Cut the trace between pin 11, IC14 and pin 9, IC12.

( ) Connect pin 11, IC14 to pin 14, IC14.

( ) Connect pin 12, IC14 to pin 9, IC12.

( ) Cut the trace between pin 9, IC27 and J7-9.

( ) Connect pin 11, IC14 to J7-9. This is the new A9 address line.

The cursor modifications can now be made. The new circuitry is contained on the 3 in. by 2 in. single sided board shown in Figure 2. This board has been designed to be mounted directly above the +5 v. and GND buses which run across the center of the main board. Mounting of the board should not be done until all other connections axe complete. The components should now be mounted on the board from the silk screened side. Refer to Figure 3 to verify component positioning.

( ) Mount IC1, 74193 BCD counter.

( ) Mount IC2, 7485 comparator

( ) Mount IC3, 7404 hex inverter

( ) Mount IC4, 7400 quad NAND gate

( ) Mount C1, 0.1 mfd disc capacitor

The following cuts and connections should now be made on the main board.

( ) Cut the trace between pin 9, IC28 and pin 13, IC35.

( ) Cut the trace between pin 10, IC28 and pin 12, IC35.

( ) Cut the trace between pin 12, IC35 and pin 11, IC33.

( ) Cut the trace between pin 13, IC35 and pin 13, IC33.

( ) Connect pin 9, IC28 to pin 13, IC33.

( ) Connect pin 10, IC28 to pin 11, IC33.

( ) Cut the trace between pin 6, IC42 and pin 3, IC41.

( ) Cut the trace between pin 15, IC42 and the plated throug111 hole immediately adjacent to IC42.

We are now ready to hake the following connections from the main board to the auxiliary board.

( ) Connect pin 14, IC35 to B

( ) Connect pin 11, IC34 to C

( ) Connect pin 12, IC35 to D

( ) Connect pin 13, IC35 to E

( ) Connect the plated through hole adjacent to IC42 to G

( ) Connect pin 13, IC33 to H

( ) Connect pin 11, IC33 to J

( ) Connect pin 6, IC42 to K

( ) Connect pin 15, IC42 to I

( ) Connect pin 3, IC41 to L

( ) Connect pin 11, IC14 to F

NOTE: Connection point A is for the cursor count preload and will not be made at this time.

( ) Mount the auxiliary board on the main board using heavy gauge wire. M is connected to the +5 volt bus and N to the GND bus. Note that the M & N connecting. points are positioned such that the board can be mounted directly above the bus traces running across the center of the board.

( ) Replace the 38 pf capacitor C4 on the main board with an 18 pf capacitor.

MEMORY MODIFICATIONS

Modification of the original memory is not required if you do not need two pages of I/0. If you would like to have two page capabilities two methods are available. You can use the 2 K memory board shown in Figure 4 or you can piggyback the additional memory onto the original TVT-II memory board. If you are using the 2 K memory board the instructions are given below.

2K MEMORY INSTRUCTIONS

The 2K memory board not only provides two page storage for the 64 character/line TVT-II but also provides storage of the seventh ASCII data bit. Storage of this bit is essential for complete communications to the computer when using the Screen Read option. The original TVT-II memory board does not provide this capability.

( ) Install capacitors Cl-C14, 0.10 pfd. Note: These are decoupling capacitors and are not necessarily needed, however at least one should be present on each column (C8-C14).

( ) Install connectors J7 and J8.

( ) Connect pin 8, IC27 to J7 terminal 10 on the main board.

( ) Omit this step if sockets are used Solder ICs Zl-Z6 and Z8-Z13, 2102 memories to the board using, care to avoid solder bridges. Refer to Figure 4 for proper positioning. Note: These are MOS devices and care should be taken to avoid static discharge to the pins. Use only a fully grounded soldering iron.

( ) Solder in ICs Z7 and Z14 if the board is to be used with the Screen Read option.

( ) If sockets are used solder in place and carefully load ICs Zl-Z6 and Z8-Z13, 2102 memories as stated above. Load ICs Z7 and Z14 if the board is to be used with the Screen Read option.

( ) Connect a short length of wire to pin 9, IC27 on the main board. The other end of this lead as to be connected to the CE terminal on the memory board. This connection should be made with some type of slip on connector to facilitate easy removal of the memory board.

NOTE: Connections D7OA, D7IA, D7OB and D7I1B are for the seventh ASCII data bit and will not be used when the Screen Read option is not being used.

The memory board is now complete and is ready for testing on the main board.

PIGGYBACKING INTSTRUCTIONS

If you are not using the 2K memory board but would like to have two pages of data this can be done by piggybacking six additional 2102s onto the existing six on the original TVT-II memory board. The procedure follows.

( ) Cut the trace between the $\overline{CE}$ trace and ground on the memory board.

This short section is located directly above IC6 on the board. The $\overline{CE}$ trace goes to pin 13 of all the memories.

( ) Connect the $\overline{CE}$ trace to pin 8, IC27 on the main board.

( ) Carefully bend pin 13 of six new memories out so that it is parallel to the chip.

( ) Carefully position each of these chips on top of the existing memory chips on the board. Solder each of the 15 unbent pins to the pins of the existing memories. You should now have six 2102s piggybacked on top of the existing 2102s. Note: Use grounded soldering iron.

( ) Carefully connect the $\overline{CE}$ pins of the new chips, together with a length of wire. This is the page two $\overline{CE}$ line.

( ) Connect this wire to pin 9, IC27 on the main board.

You note have two pages of data which are automatically rolled over by the page flip-flop IC27 which enables the CE line of either six 2102s.

EARLY TVT-II MEMORY MODIFICATION

You may have an early design TVT-II which uses the CE line on the memories. If you have one of these units terminal 10, J7 will have a trace leading to it. If you have one of these units the memory modification will require the following additional procedures.

( ) Cut the traces between pins lands 1 and 2, 4 and 5 and between these pins and the ground bus of IC4 on the auxiliary board.

( ) Connect pin 8, IC3 to pins 1 and 4, IC4.

( ) Cut the trace between pin 8, IC17 and terminal 10, J7 just before it reaches J7.

( ) Connect pin 8, IC17 to pin 9, IC3 on the auxiliary board.

( ) Connect pin 8, IC27 to pin 2, IC4 on the auxiliary board.

( ) Connect pin 9, IC27 to pin 5, IC4 on the auxiliary board.

( ) Pins 3 and 6 of IC4 should now be used in place of pins 8 and 9 of IC27 for driving the two lines. IC3 inverts the normal CE pulse which is then NANDed with the output of IC27B, the page flip-flop. The NANDed signal is then used to address either page of memory through the $\overline{CE}$ lines.

START UP

After checking all connections and foil cuts the power can be turned on with the memory board out. The screen will be filled with either ? or @ symbols, R38 should be adjusted to provide a stead display. R6 and R4 can then be used to center the display on the screen. If the characters appear smeared, your TV has a limited bandpass and cannot be used with a 64 character display without modifications. Most TV's should be able to handle the increased display density with no problems.

You are now ready to shut the power off and install the memory board. Turn the pourer back on and enjoy the 64 character/line display. Don't forget to revise your TVT-TI schematic with the modifications that you have made.

PARTS LIST

64 CHARACTER BOARD

IC1	74193
IC2	7485
IC3	7404
IC4	7400
C1	0.10 mfd disc
C4	on main board 18 pf
Wire	26 Ga.

2K MEMORY BOARD

Z1-Z6, Z8-Z13	2102 memories
C1-C14	0.10 mfd capacitors
Z7, Z14 (Optional)	2102 memories
Wire	26 Ga.
J7, J8	15 pin Molex board connectors

The auxiliary board and 2K memory boards shown are available from DIGITAL DESIGN, BOX 4241 VICTORIA, TEXAS 77901. Both boards are Mil spec with tin/lead fused plating and silk screened component placement. The auxiliary board is single-sided whereas the 2K board is double-sided with plated through holes. The auxiliary board is $6.50 The 2K board is $13.50. If ordered together they are $18.00 Shipping is included in board prices. Shipment within 3 weeks is guaranteed. Texas orders add 5% sales tax.

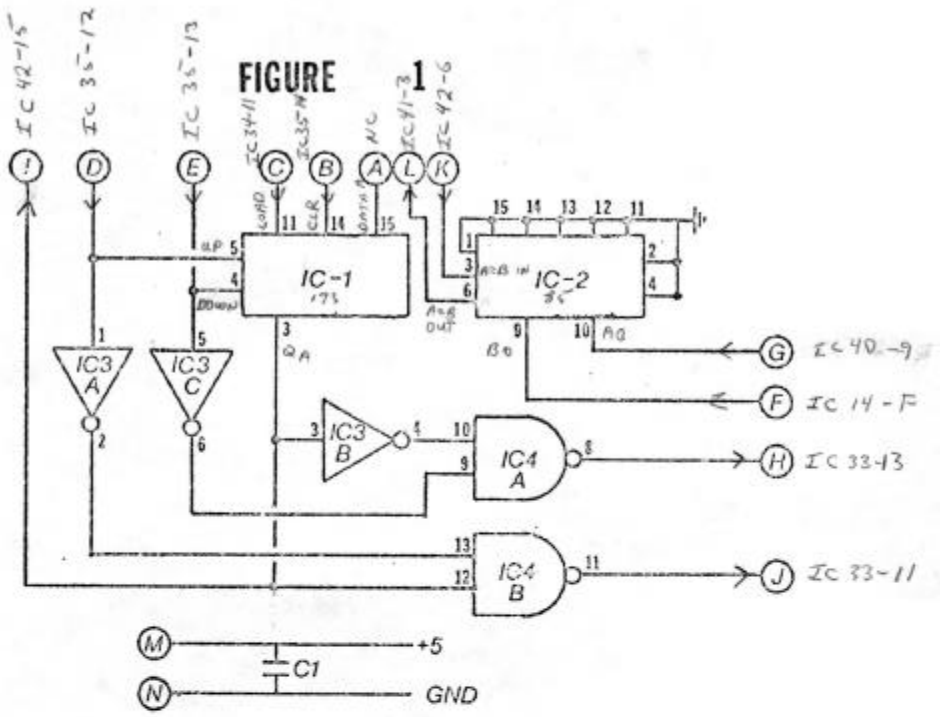


FIGURE 2

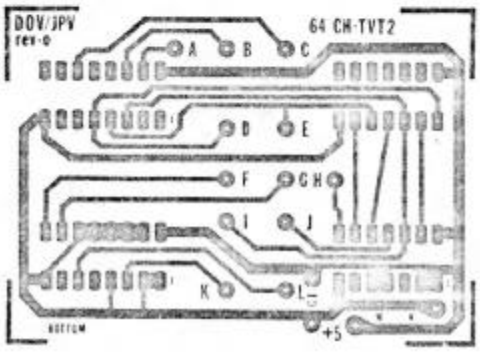


FIGURE 3

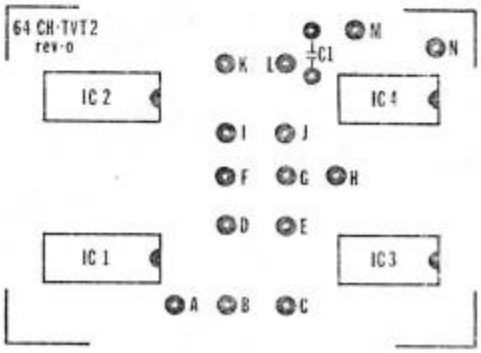
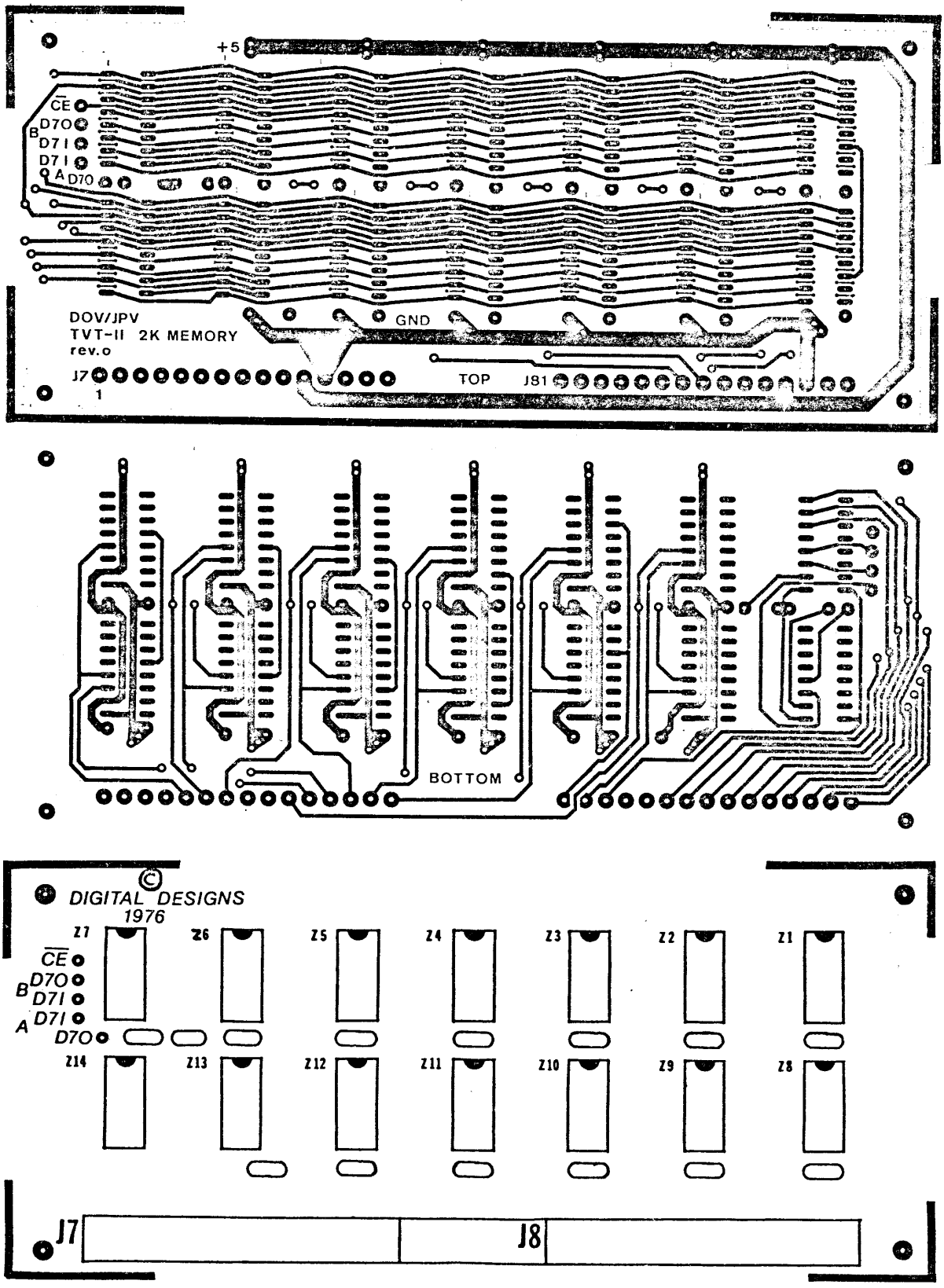


FIGURE 4


+5
CE
B D70
D71
D71
A D70
DOV/JPV
TVT-II 2K MEMORY
rev.o
GND
J7
1
TOP
J81
BOTTOM
©
DIGITAL DESIGNS
1976
Z7
Z6
Z5
Z4
Z3
Z2
Z1
CE
B D70
D71
A D71
D70
Z14
Z13
Z12
Z11
Z10
Z9
Z8
J7
J8