OMTI 5098
AT COMPATIBLE
INTERFACE CHIP
REFERENCE MANUAL
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OMTI 5098 AT COMPATIBLE INTERFACE CHIP

REFERENCE MANUAL

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SECTION 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The OMTI 5098 "AT" Compatible Interface chip provides all the function required for a winchester controller to interface to an AT compatible system when used with the OMTI 5055 Kombo Controller Chip. This chip provides a compatible 8 bit register set for all command, control and status along with a 16 bit data path to and from the host to the Winchester controller. The OMTI 5098 chip also includes the floppy decode logic required for a combination Winchester and floppy controller.

1.2 OMTI 5098 "AT" COMPATIBLE INTERFACE CHIP

* Direct Interface to "AT" Compatible systems
* No external logic required with OMTI 5055
* Support for external floppy controller
* High current drivers for host interface
* SCHMITT trigger inputs form host interface
* Configurable primary or secondary address
* 3 micron SLM CMOS Standard Cell Technology
* 84-Pin PLCC Package or 80-Pin PFP package

1.3 FUNCTIONAL OVERVIEW

Figure 1 illustrates the internal block diagram of the OMTI 5098 "AT" Compatible Interface Chip. Each logic block is discussed in the following sections.

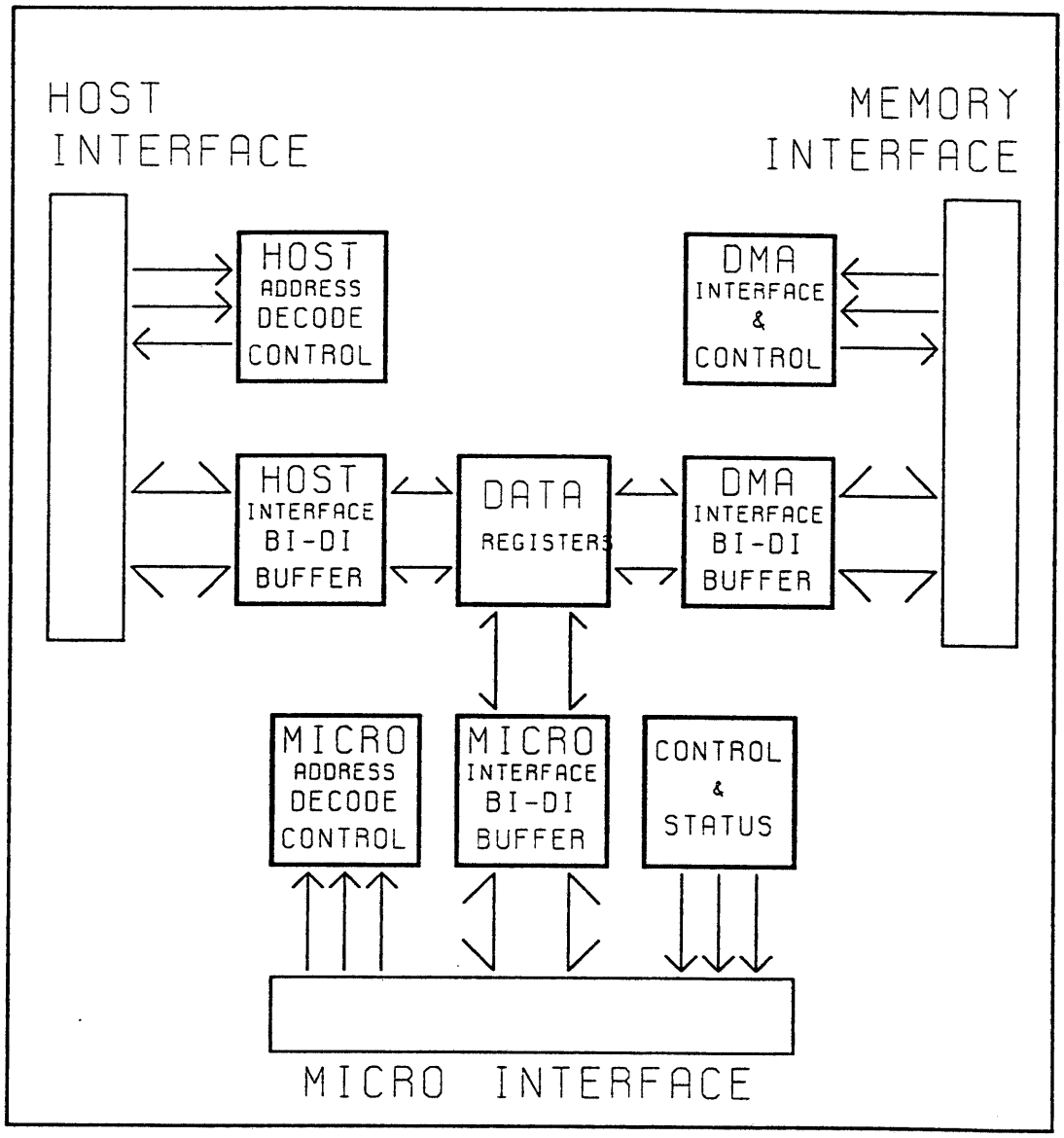


Figure 1. Internal Block Diagram

1.3.1 Host Interface and Decode

This block contains all the logic to interface an AT compatible computer to a winchester controller. This includes all the I/O address decode logic along with all the host read write registers.

1.3.2 Host Data Bus

This blocks contains the 16 bit bi-directional registers used to interface the Host to the microcomputer on the controllers microcomputer and also the memory data bus.

1.3.3 Winchester Interface Logic

This section controls the select logic for the external winchester, along with directing the disk drive status to the host computer.

1.3.4 Floppy Interface Logic

This section controls the select logic for the external floppy controller chip along with the control of the external floppy speed control logic.

1.3.5 Memory Data Interface

This section controls the transfer of data to and from the external eight bit buffer memory to and from the sixteen bit host computer. It is in this block that the 8 bit to 16 bit packing and unpacking in accomplished.

1.3.6 Microcomputer Interface and Decode

This blocks interfaces the microcomputer on the controller to the read write registers in which the host interfaces and also allows the microcomputer to initialize the OMTI 5098 Interface chip.

1.4 CONTROLLER BLOCK DIAGRAM

Figure 2 illustrates a complete controller block diagram using the OMTI 5098 "AT" Compatible Interface Chip along with an OMTI 5055 Kombo controller chip and an OMTI 5070 or OMTI 5027 Encode / Decode / VCO chip.

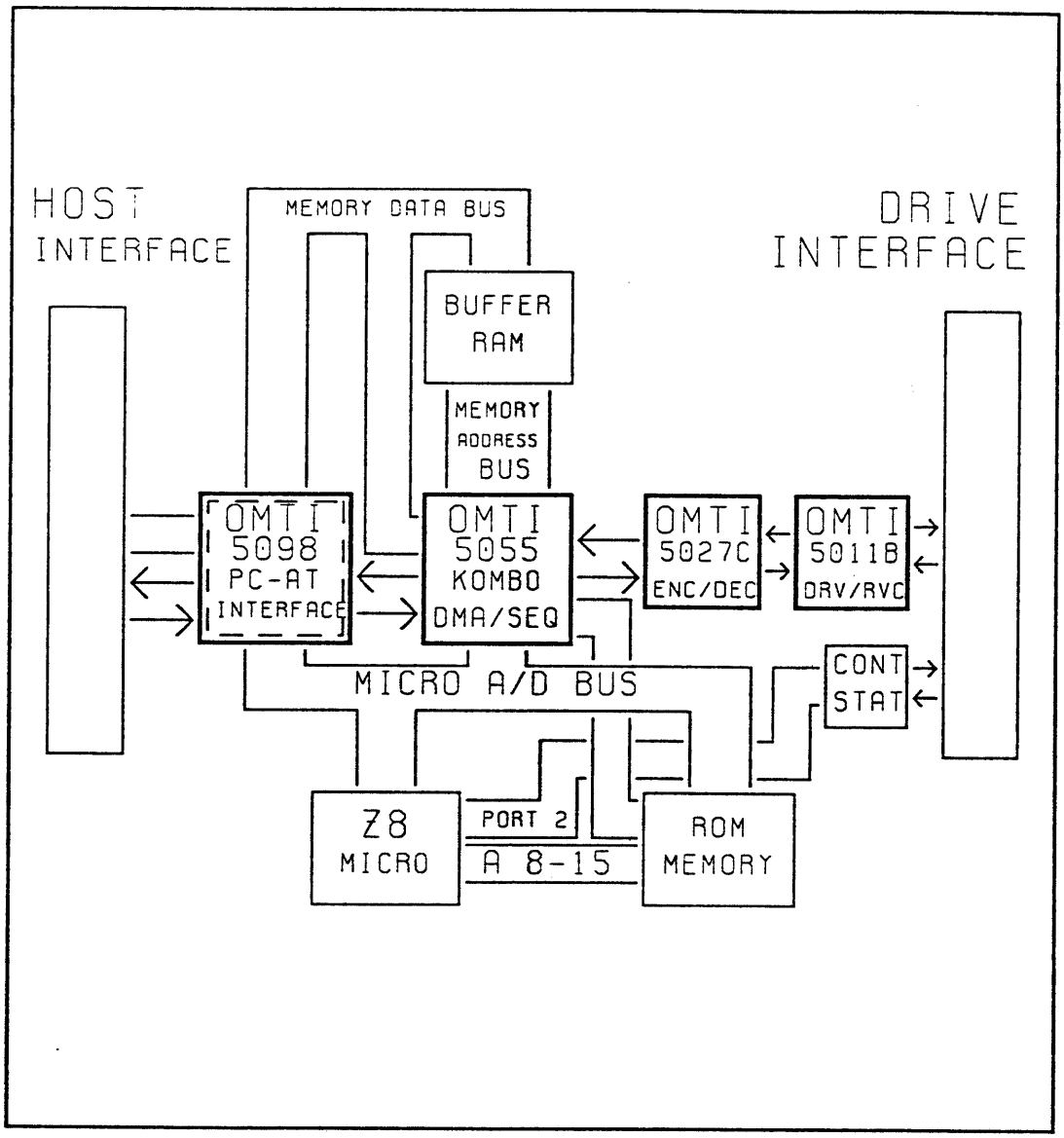


Figure 2. Controller Block Diagram

SECTION 2

INTERFACING

2.1 PIN DESCRIPTIONS

Symbol	Type	Pin #	Name and Function
AEN	I	2	ADDRESS ENABLE (HOST): This signal is asserted during a DMA cycle. It is used to disable the decoding of the HOST I/O ADDRESS BUS during DMA cycles.
-IOWR	I	3	I/O WRITE (HOST): This input signal is asserted to write data from an I/O address (A9 - A0, AEN is de-asserted).
-IORD	I	4	I/O READ (HOST): This input signal is asserted to read data from an I/O address (A9 - A0, AEN is de-asserted).
D_(7:0)	I/O	5-11 13	DATA BUS (HOST): These bi-directional, tri-state signals are used to transfer data between the HOST and the 5098 internal/external registers. During WORD data transfers, these signals are the least significant byte of the data word.
-WRITE_DATA	O	12	WRITE DATA (CONTROLLER, REV C ONLY): This output signal is asserted during a HOST write to the DATA REGISTER 1F0(170).
ALE	I	14	ADDRESS LATCH ENABLE (HOST): This input signal is asserted to indicate that the HOST I/O ADDRESS is valid on the falling edge.
-DS_0	O	15	DRIVE SELECT ZERO: This open drain output is asserted when a '0' is written to BIT 4 of WRITE REGISTER 1F6(176). If the 5098 is in the NON-SELECT MODE, this output is only asserted during reads to REGISTER 1F7(177) or the controller is BUSY.
IO_CH_RDY	O	16	I/O CHANNEL READY (HOST): This open drain, 24 MA. output signal is de-asserted to lengthen an I/O data cycle. This signal is only active during WORD MODE data transfers at I/O ADDRESS 1F0(170).

Symbol	Type	Pin #	Name and Function
~IO_CS_16	O	18	I/O CHIP SELECT 16 BIT (HOST): This open drain, 24 ma. output signal is asserted to indicate that the present HOST data transfer is a 16-bit, 1 wait-state I/O cycle. It is derived from the 5098 DATA REGISTER 1F0(170) decode.
~DS_1	O	19	DRIVE SELECT ZERO: This open drain output is asserted when a '1' is written to BIT 4 of WRITE REGISTER 1F6(176). If the 5098 is in the NON-SELECT MODE, this output is only asserted during reads to REGISTER 1F7(177) or the controller is BUSY.
RESET_IN	I	20	RESET IN (HOST): This input signal is asserted to indicate that a power-up or low voltage condition exist.
~RESET_OUT	O	21	RESET OUT: This output is an inverted copy of the RESET_IN signal or is asserted for a minimum of 1 microsecond indicating that the 5098 has an internal power-on reset.
~RESET_SOFT	O	23	SOFT RESET: This output signal is asserted as long as BIT 2 of WRITE REGISTER 3F6(376) is asserted.
~READY	I	24	READY: This input signal is available on BIT 6 of READ REGISTER 1F7(177).
~INDEX	I	25	INDEX: This input signal is available on BIT 1 of READ REGISTER 1F7(177).
DMA_INTRQ	I	26	DMA INTERRUPT REQUEST: When enabled, this level sensitive input causes the 5098 to become BUSY. The polarity of this signal is programmable and should be connected to the DMA INTERRUPT signal of the DMA controller.
DECODE_A	I	27	ADDRESS DECODE A (HOST): This internally pulled-up signal specifies the 5098 HOST I/O address range. If no connection is made to this signal the 5098 HOST REGISTER A range is 1F0 - 1F7 (HEX). If this signal is grounded, the 5098 HOST REGISTER A range is 170 - 177 (HEX).

Symbol	Type	Pin #	Name and Function
DECODE_B	I	28	ADDRESS DECODE B (HOST): This internally pulled-up signal specifies the 5098 HOST I/O address range. If no connection is made to this signal the 5098 HOST REGISTER B range is 3F0 - 3F7 (HEX). If this signal is grounded, the 5098 HOST REGISTER B range is 370 - 377 (HEX).
CONFIG	I	29	PROCESSOR CONFIGURATION (CONTROLLER): This internally pulled-up signal specifies the controller processor strobe inputs. If no connection is made to this signal, the 5098 is configured for a Z8-type processor. In this case, ALE_~AS = ~AS, ~IORD_~DS = ~DS, ~IOWR_RW = RW and IO_~MEM_~DM = ~DM. If this signal is grounded, the 5098 is configured for an 8051-type processor. In this case, ALE_~AS = ALE, ~IORD_~DS = ~IORD, ~IOWR_RW = ~IOWR and IO_~MEM_~DM = IO_~MEM.
DMA_ACK	I	30	DMA ACKNOWLEDGE: This input signal, initiated by the DMA controller, indicates that a DMA transfer is taking place.
DMA_REQ	O	31	DMA REQUEST: In conjunction with DMA_ACK, this output signal is asserted by the 5098 on the trailing edge of an IORD or IOWR to HOST ADDRESS 1F0(170) during data transfers.
READ_DATA	O	32	READ DATA (CONTROLLER, REV C ONLY): This output signal is asserted during a HOST read to the DATA REGISTER 1F0(170).
~INENA	I	33	INPUT ENABLE: This input signal is asserted by the DMA controller to enable the 5098 to drive the MEMORY Data bus.
~OUTCLK	I	34	OUT CLOCK: This input signal is asserted by the DMA controller to save data into the 5098 form the MEMORY Data bus.
MEM_D(7:0)	I/O	35-42	MEMORY DATA: These bi-directional signals are used to transfer data between the HOST and the Controller DMA Buffer Memory.

Symbol	Type	Pin #	Name and Function
AD_(7:0)	I/O	44-51	ADDRESS/DATA BUS (CONTROLLER): These bi-directional, tri-state signals are used to transfer address and data between the 5098 and the controller processor. The processors ADDRESS is latched on the falling edge (8051-mode) or the rising edge (Z8-mode) of the ALE_~AS signal. the processors DATA is either read from or written to the 5098 (if selected) on the processors ~IORD_~DS/~IOWR_RW data strobes.
ALE_~AS	I	52	ADDRESS LATCH ENABLE/ADDRESS STROBE (CONTROLLER): This input signal is asserted to latch the controller microcomputers address into the 5098. In 8051 mode, this input is active high. In Z8 mode, this input is active low.
~IOWR_RW	I	53	I/O WRITE (8051) READ/WRITE (Z8) (CONTROLLER): This input signal is asserted in 8051 mode, to gate data from the controller to the 5098 (if selected). If the Z8-mode is selected, this input signal is low to indicate a write function and high to indicate a read function.
SYS_CLK	I	54	SYSTEM CLOCK (HOST, REV C ONLY): This input is used to synchronize the IO_CH_RDY output to the system clock.
~IORD_~DS	I	55	I/O READ (8051) DATA STROBE (Z8) (CONTROLLER): This input signal is asserted to gate data from the 5098 (if selected) to the ADDRESS/DATA BUS of controller processor (8051-mode). If the Z8-mode is selected, this input signal is used to gate data from (READ) or to (WRITE) the 5098 (if selected).
IO_~MEM_~DM	I	56	I/O ~MEMORY (8051) ~DM (Z8) (CONTROLLER): This input signal is used for as a chip select for the 5098. In 8051 mode, this input is active high. In Z8 mode, this input is active low.

Symbol	Type	Pin #	Name and Function
-COMMAND	O	57	COMMAND: This output signal is asserted to indicate that a command has been written into WRITE REGISTER 1F7(177) It is de-asserted by writing the INTERNAL CONTROL REGISTER bit 2 with a '1' or a RESET.
-WRT_GATE	I	58	WRITE GATE: This input signal is available on BIT 6 of READ REGISTER 3F7(377).
-DCHG	I	59	DISK CHANGED: This internally pulled-up signal is available on BIT 7 of READ REGISTER 3F7(377). If this signal is not used, BIT 7 of READ REGISTER 3F7(377) can be TRI-STATED by writing a '1' to BIT 4 of the INTERNAL CONTROL REGISTER F8.
RATE_1	O	60	FLOPPY DATA RATE 1: This output signal along with RATE_0 determine the flexible disk data rate.
RATE_0	O	61	FLOPPY DATA RATE 0: This output signal along with RATE_1 determine the flexible disk data rate.
-FDD_REG	O	62	FLOPPY DATA REGISTER: This output signal is asserted during an IOWR to HOST ADDRESS 3F2(372).
-CS_FDC	O	63	FLOPPY CONTROLLER SELECT: This output signal is asserted during an IOWR or IORD to HOST ADDRESS 3F4-3F5(374-375).
INTRQ	O	65	INTERRUPT REQUEST: This TRI-STATE output signal indicates that the 5098 needs attention. It is enabled or disabled by writing a '0' or '1' respectively to BIT 1 of WRITE REGISTER 3F6(376). It is asserted by writing a '1' to BIT 0 of the INTERNAL CONTROL REGISTER F8 and is de-asserted by writing a '0' to BIT 0 of the INTERNAL CONTROL REGISTER F8, reading SYSTEM REGISTER 1F7(177) or writing SYSTEM REGISTER 1F7(177). REV C: Writing a '0' to BIT 0 of the INTERNAL CONTROL REGISTER will not de-assert the INTRQ signal.

Symbol	Type	Pin #	Name and Function
D_(15:8)	I/O	66-73	DATA BUS (HOST): These bi-directional, tri-state signals are used to transfer the most significant byte of HOST data to or from the 5098 DATA REGISTER.
A_(9:0)	I	75-84	I/O ADDRESS BUS (HOST): These input signals constitute the 10 BIT 5098 HOST I/O ADDRESS BUS and are internally decoded for the selection of internal and external 5098 registers.
VSS			GROUND: Pins 1,17,43,74
VDD			POWER: Pins 22,64

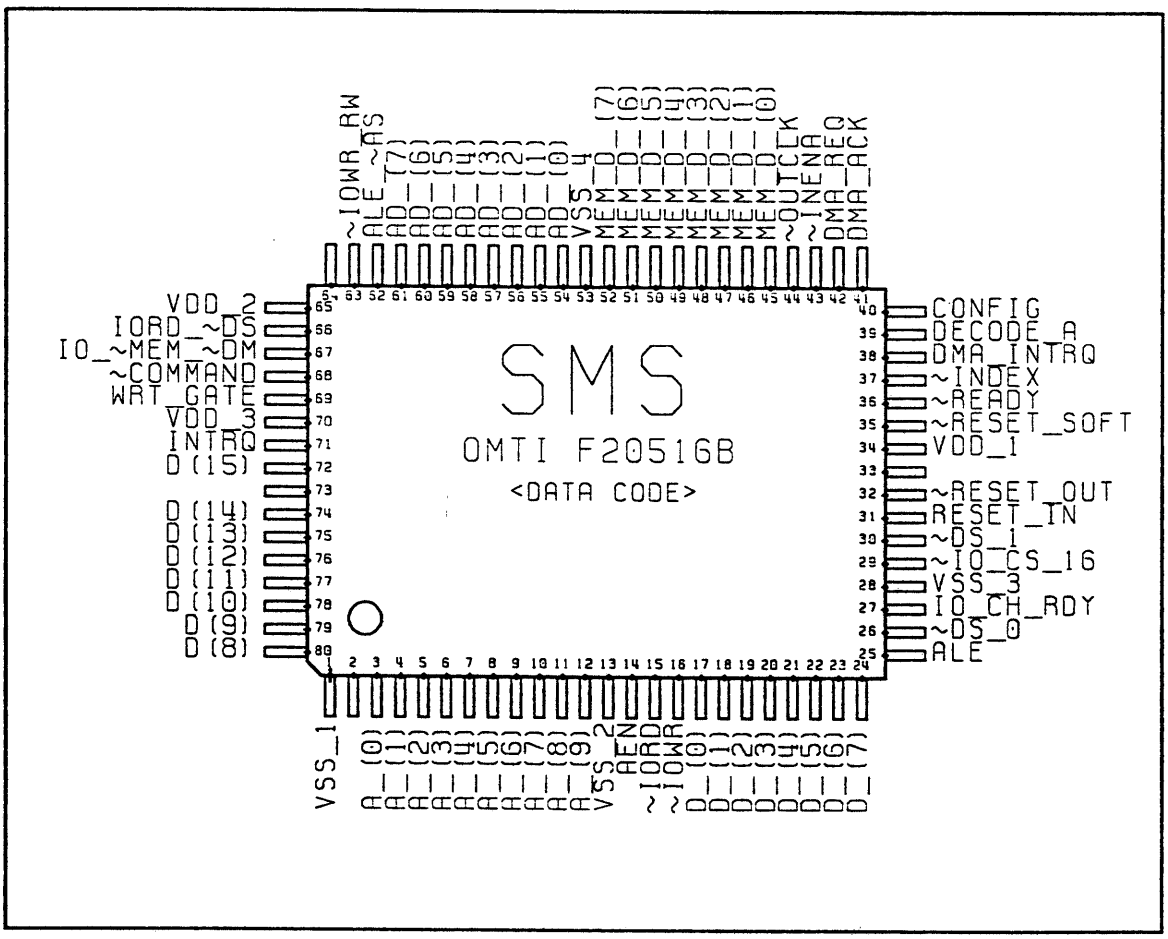


Figure 3. Pin Assignment 5098B 80 Pin PFP

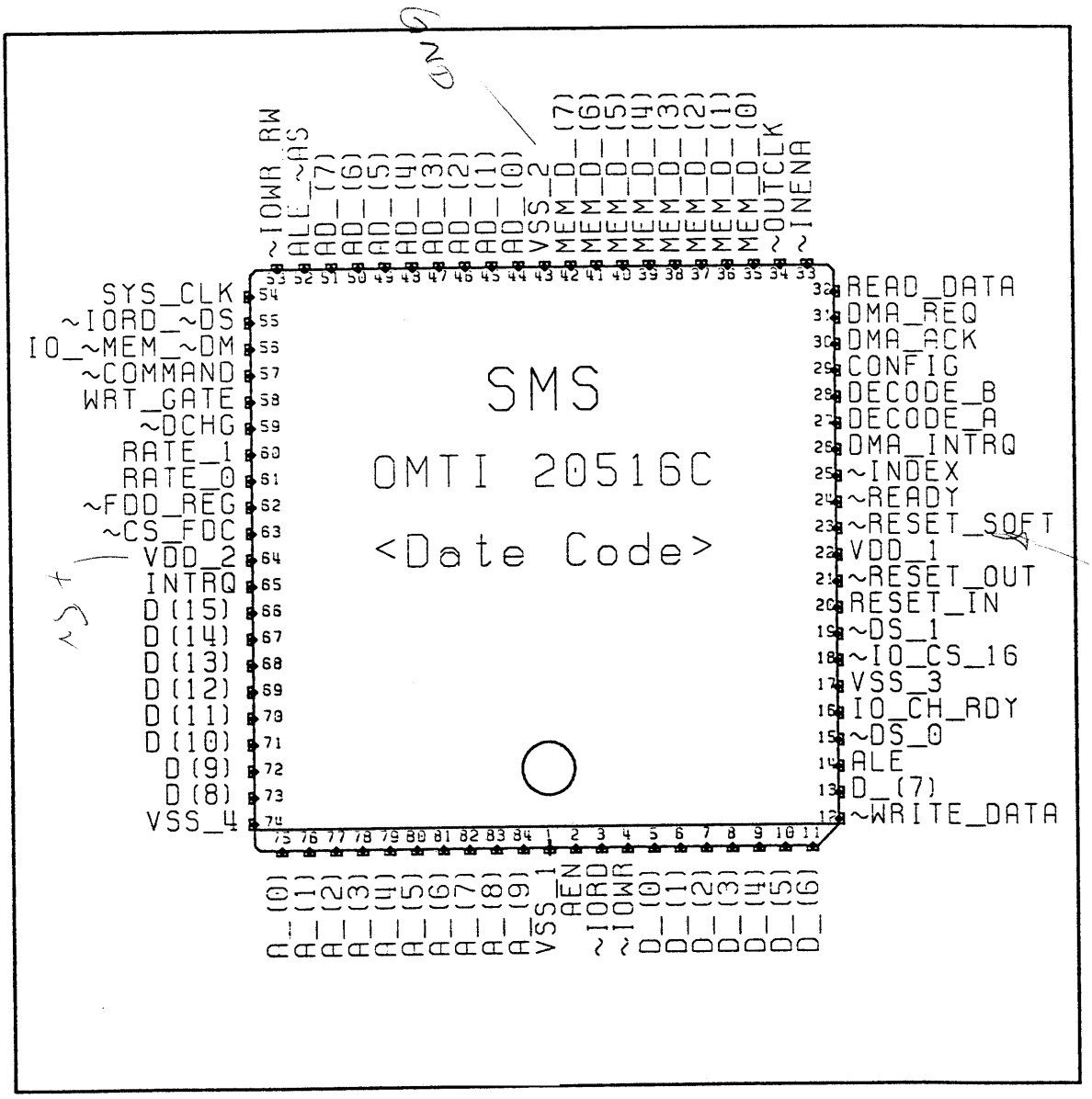


Figure 3. Pin Assignment 5098C 84 Pin PLCC

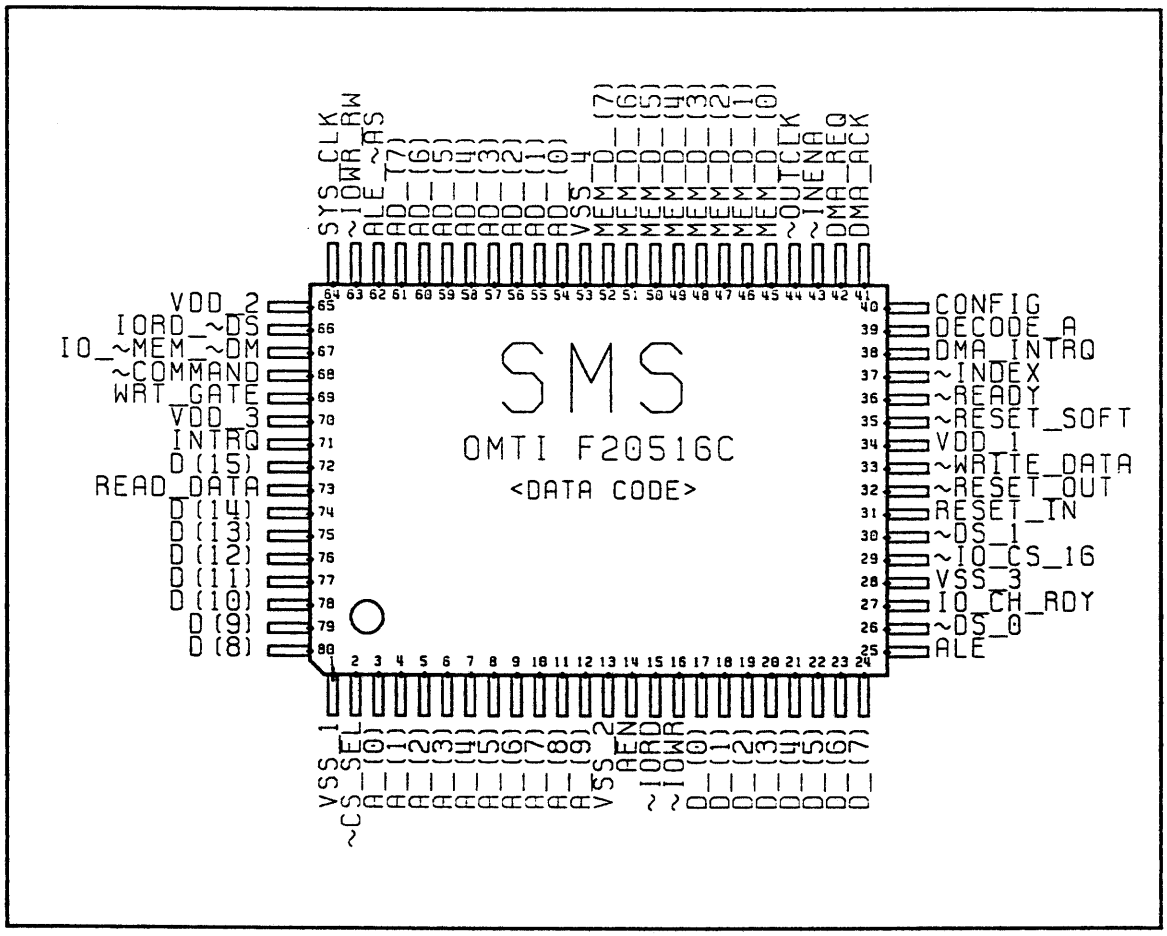


Figure 3. Pin Assignment 5098C 80 Pin PFP

SECTION 3

INTERFACE REGISTERS

3.1 HOST INTERFACE REGISTERS

The OMTI 5098 contains 10 registers by which the HOST can communicate with the controller. The register organization described in this document relate to an 'AT' compatible Winchester/Floppy Controller application. However, these registers are general purpose READ/WRITE registers and except for some hardware specific bits, can be defined to suit other applications. Decoding for an optional FLOPPY SELECT/CONTROL REGISTER and a FDC 765 FLOPPY DISK CONTROLLER is also available.

3.2 HOST REGISTER ASSIGNMENT

I/O ADDRESS PRIMARY(SECONDARY)	READ	WRITE
1F0(170)	DATA REGISTER	DATA REGISTER
1F1(171)	ERROR REGISTER	PRECOMPENSATION REGISTER
1F2(172)	SECTOR COUNT REGISTER	SECTOR COUNT REGISTER
1F3(173)	SECTOR NUMBER REGISTER	SECTOR NUMBER REGISTER
1F4(174)	CYLINDER REGISTER (LSB)	CYLINDER REGISTER (LSB)
1F5(175)	CYLINDER REGISTER (MSB)	CYLINDER REGISTER (MSB)
1F6(176)	SDH REGISTER	SDH REGISTER
1F7(177)	STATUS REGISTER	COMMAND REGISTER
3F2(372)		FLOPPY SELECT/CONTROL
3F4(374)	FDC MAIN STATUS	
3F5(375)	FDC DATA	FDC DATA
3F6(376)	SECONDARY STATUS	CONTROL REGISTER
3F7(377)	HEAD/SELECT STATUS	FLOPPY RATE SELECT

TABLE 1 HOST REGISTER ASSIGNMENT

3.3 HOST READ REGISTER DESCRIPTION

3.3.1 DATA REGISTER 1F0(170)

This register transfers controller data between the 5098 and the HOST. In WORD MODE, 16 bits of data are transferred requiring ~IO_CS_16 to be asserted and possibly de-asserting IO_CH_RDY. In BYTE MODE, 8 bits of data are transferred leaving ~IO_CS_16 de-asserted and IO_CH_RDY asserted.

3.3.2 ERROR REGISTER 1F1(171)

This register contains the ERROR STATUS of the last command executed by the controller. It can only be accessed while the controller is in the NOT BUSY state. This register is not affected by RESET. The bit definitions are:

BIT 7 - BAD BLOCK FOUND. This indicates that the specified track has previously been formatted with the BAD TRACK flag set in the ID field. It is not possible to access data on this track and the command will be terminated.

BIT 6 - ECC ERROR. This indicates that a NON-ZERO syndrome was detected in a specified data field. If the data error was corrected by ECC, BIT 2 of the STATUS REGISTER will also be SET and the command will continue if more sectors are specified. If the data error was NOT corrected by ECC, BIT 0 of the STATUS REGISTER will be SET and the command terminated.

BIT 5 - NOT USED. Set to zero.

BIT 4 - ID NOT FOUND. This indicates that the controller was able to locate the correct cylinder and head numbers but was unable to locate the correct sector number. An ID CRC error can also generate this error condition.

BIT 3 - NOT USED. Set to zero.

BIT 2 - ABORTED COMMAND. The current command issued by the HOST has been aborted due to an undefined COMMAND OPCODE, or a WRITE FAULT/NOT READY condition exist on the selected drive.

BIT 1 - NO CYLINDER ZERO. This indicates that during a RECALIBRATION command or if retries are enabled no CYLINDER 000 was detected. This error occurs after the controller issues 2048 step pulses towards cylinder 000 and the selected drive does not respond with the TRACK 000 signal.

BIT 0 - NO DATA MARK FOUND. This indicates that the controller was able to locate the sector but was unable to locate the data mark associated with it.

3.3.3 SECTOR COUNT REGISTER 1F2(172)

This register contains the number of sectors to be processed and is decremented as each sector is processed. It can only be accessed while the controller is in the NOT BUSY state. This register is set to 1 after a RESET.

3.3.4 SECTOR NUMBER REGISTER 1F3(173)

This register contains the current sector number being processed by the controller. It can only be accessed while the controller is in the NOT BUSY state. If an error condition exist, this register contains the sector number in error. It is set to 1 after a RESET.

3.3.5 CYLINDER (LSB) REGISTER 1F4(174)

This register contains the least significant byte of the current cylinder number. It can only be accessed while the controller is in the NOT BUSY state. If an error condition exist, this register contains the least significant byte of the cylinder number in error. This register is set to 0 after a RESET.

3.3.6 CYLINDER (MSB) REGISTER 1F5(175)

This register contains the most significant byte of the current cylinder number. It can only be accessed while the controller is in the NOT BUSY state. If an error condition exist, this register contains the most significant byte of the cylinder number in error. This register is set to 0 after a RESET.

3.3.7 SDH REGISTER 1F6(176)

This register contains the controller ERROR CODE/SECTOR SIZE parameters along with the current DRIVE/HEAD select. It can only be accessed while the controller is in the NOT BUSY state. This register is set to 0 after a RESET. The bit definitions are:

BIT 7 - ERROR CODE. This bit indicates the error code selected. If this bit is set to ONE, the data field will be appended with an ECC field. If set to ZERO, the data field will be appended with a CRC field.

BITS 6, 5 - SECTOR SIZE. These bits indicate the sector size selected. Their definitions are:

BIT 6 5	
0 0 -	256 BYTE SECTOR
0 1 -	512 BYTE SECTOR
1 0 -	1024 BYTE SECTOR
1 1 -	128 BYTE SECTOR

BIT 4 - DRIVE SELECT. This bit reflects the selected drive. If this bit is set to ZERO, drive 0 is selected. If set to ONE, drive 1 is selected.

BITS 3-0 - HEAD SELECT. These bits indicate the selected head.

3.3.8 STATUS REGISTER 1F7(177)

This register contains the CONTROLLER/DRIVE STATUS. Reading this register de-asserts the INTRQ signal. The bit definitions are:

BIT 7 - BUSY. This bit indicates the state of the controller. If SET, the controller is busy executing the specified command and is NOT in a DATA TRANSFER state. While set, the STATUS REGISTER is gated on the BUS during any READ to the HOST READ/WRITE REGISTERS. Any WRITE to the HOST READ/WRITE REGISTERS while this bit is set will be ignored. If CLEARED, the controller is either in a NOT BUSY or a DATA TRANSFER state. The DRQ bit will be SET if the controller is in the DATA TRANSFER state.

BIT 6 - READY. This bit is an inverted copy of the ~READY signal of the selected drive.

BIT 5 - WRITE FAULT. This bit is an inverted copy of the ~WRITE FAULT signal of the selected drive.

BIT 4 - SEEK COMPLETE. This bit is an inverted copy of the ~SEEK COMPLETE signal of the selected drive.

BIT 3 - DATA REQUEST. This bit indicates that the controller is in a DATA TRANSFER mode. While this bit is SET, the BUSY bit will be CLEARED and the controller will wait for data to be transferred to or from the HOST.

BIT 2 - CORRECTED. This bit indicates if a DATA ERROR was corrected. If SET, an ECC error occurred but was corrected. A corrected ECC error will NOT terminate a multiple sector transfer. If CRC is selected, this bit has no meaning and is set to ZERO.

BIT 1 - INDEX. This bit is an inverted copy of the ~INDEX signal of the selected drive.

BIT 0 - ERROR. This bit indicates if an UNRECOVERABLE ERROR has occurred. If SET, an error condition exist and the ~~STATUS~~ ERROR REGISTER must be read to determine the error type.

3.3.9 FDC 765 MAIN STATUS REGISTER (OPTIONAL)

Reading this register selects the FDC 765 MAIN STATUS register (if available). For more information, consult the FDC 765 data sheet.

3.3.10 FDC 765 DATA REGISTER (OPTIONAL)

Reading this register selects the FDC 765 DATA register (if available). For more information, consult the FDC 765 data sheet.

3.3.11 SECONDARY STATUS REGISTER 3F6 (376)

This register contains the CONTROLLER/DRIVE STATUS. It is identical to the STATUS REGISTER at address 1F7(177). See section 3.3.8 for bit definitions.

3.3.12 HEAD/SELECT STATUS REGISTER 3F7(377)

This register contains the HEAD/DRIVE SELECT STATUS. The bit definitions are:

BIT 7 - DISKETTE CHANGE.	This bit indicates the state of the floppy ~DCHG signal. If SET, no diskette, door open or drive NOT READY condition exist.
BIT 6 - WRITE GATE.	This bit indicates the state of the winchester ~WRITE GATE signal.
BIT 5 - HEAD SELECT 3/RWC.	This bit indicates the state of HEAD SELECT 3/RWC.
BIT 4 - HEAD SELECT 2.	This bit indicates the state of HEAD SELECT 2.
BIT 3 - HEAD SELECT 1.	This bit indicates the state of HEAD SELECT 1.
BIT 2 - HEAD SELECT 0.	This bit indicates the state of HEAD SELECT 0.
BIT 1 - DRIVE SELECT 1.	This bit indicates the state of DRIVE SELECT 1. If set to ZERO, DRIVE 1 is selected. If set to ONE, DRIVE 1 is de-selected.
BIT 0 - DRIVE SELECT 0.	This bit indicates the state of DRIVE SELECT 0. If set to ZERO, DRIVE 0 is selected. If set to ONE, DRIVE 0 is de-selected.

3.4 HOST WRITE REGISTER DESCRIPTION

3.4.1 DATA REGISTER 1F0(170)

This register transfers controller data between the HOST and the 5098. In WORD MODE, 16 bits of data are transferred requiring ~IO_CS_16 to be asserted and possibly de-asserting IO_CH_RDY. In BYTE MODE, 8 bits of data are transferred leaving ~IO_CS_16 de-asserted and IO_CH_RDY asserted.

3.4.2 WRITE PRECOMPENSATION/RWC REGISTER 1F1(171)

This register determines the cylinder at which WRITE PRECOMPENSATION will be applied. The value written is 1/4 the actual precompensation cylinder. A value of 255 will result in no write precompensation/reduce write current. This register should be written prior to the COMMAND REGISTER being written with a WRITE/FORMAT command. It is set to 32 (128) after a RESET.

3.4.3 SECTOR COUNT REGISTER 1F2(172)

This register specifies the number of sectors to be processed. A value of 0 indicates 256 sectors. It should be written prior to the COMMAND REGISTER being written. This register is set to 1 after a RESET.

3.4.4 SECTOR NUMBER REGISTER 1F3(173)

This register specifies the starting sector number. It should be written prior to the COMMAND REGISTER being written. This register is set to 1 after a RESET.

3.4.5 CYLINDER (LSB) REGISTER 1F4(174)

This register specifies the least significant byte of the starting cylinder number. It should be written prior to the COMMAND REGISTER being written. This register is set to 0 after a RESET.

3.4.6 CYLINDER (MSB) REGISTER 1F5(175)

This register specifies the most significant byte of the starting cylinder number. It should be written prior to the COMMAND REGISTER being written. This register is set to 0 after a RESET.

3.4.7 SDH REGISTER 1F6(176)

This register specifies the controller ERROR CODE/SECTOR SIZE parameters along with the DRIVE/HEAD select. This register should be written prior to the COMMAND REGISTER being written. This register is set to 0 after a RESET. The bit definitions are:

BIT 7 - ERROR CODE. This bit specifies the error code to be selected. If this bit is SET the data field will be appended with an ECC field. If CLEARED, the data field will be appended with a CRC field.

BITS 6, 5 - SECTOR SIZE. These bits specify the sector size to be selected. The sector size definitions are:

BIT 6	5	
0	0	- 256 BYTE SECTOR
0	1	- 512 BYTE SECTOR
1	0	- 1024 BYTE SECTOR
1	1	- 128 BYTE SECTOR

BIT 4 - DRIVE SELECT. This bit selects the drive. If this bit is set to ZERO, drive 0 is selected. If set to ONE, drive 1 is selected.

BITS 3-0 - HEAD SELECT. These bits select the head.

3.4.8 COMMAND REGISTER 1F7(177)

This register specifies the command to be executed by the controller. It is set to 0 after a RESET. Writing to this register asserts the ~COMMAND signal.

3.4.9 FLOPPY SELECT/CONTROL REGISTER (OPTIONAL)

Writing this register selects the floppy select/control register (if available). This register is external to the OMTI 5098 and is selected by the ~FDD_REG signal.

3.4.10 FDC 765 DATA REGISTER (OPTIONAL)

Writing this register selects the FDC 765 DATA register (if available). For more information, consult the FDC 765 data sheet.

3.5 CONTROLLER READ/WRITE REGISTERS

The OMTI 5098 contains 8 registers by which the microcomputer can communicate with the HOST and 4 WRITE ONLY registers which control the internal/external special functions.

3.6 MICROCOMPUTER REGISTER ASSIGNMENT

ADDRESS	READ	WRITE
40 F0	INTRQ STATUS REGISTER	HEAD SELECT REGISTER
42 F1	PRECOMPENSATION REGISTER	ERROR REGISTER
44 F2	SECTOR COUNT REGISTER	SECTOR COUNT REGISTER
46 F3	SECTOR NUMBER REGISTER	SECTOR NUMBER REGISTER
48 F4	CYLINDER REGISTER (LSB)	CYLINDER REGISTER (LSB)
4A F5	CYLINDER REGISTER (MSB)	CYLINDER REGISTER (MSB)
4C F6	SDH REGISTER	SDH REGISTER
4E F7	COMMAND REGISTER	STATUS REGISTER
50 F8		INTERNAL CONTROL REGISTER
52 F9		DRIVE CONTROL REGISTER
54 FA		BUSY CONTROL REGISTER
56 FB		5098 IDENTIFIER REGISTER
REV C ONLY		
FC		ADDITIONAL CONTROL REGISTER

TABLE 2 MICROCOMPUTER REGISTER ASSIGNMENT

3.7 MICROCOMPUTER READ REGISTER DESCRIPTION

3.7.1 INTRQ STATUS REGISTER F0

This one bit register (BIT 0 ONLY) contains the status of the INTRQ bit. If this bit is SET, INTRQ is asserted. If CLEARED, INTRQ is de-asserted.

REV C:

This register has been expanded to include drive and command interface status. The bit definitions are:

BIT 2 - COMMAND. This bit is an inverted copy of the external -COMMAND input signal. When this status bit is set to '1', a write to HOST WRITE REGISTER 1F7(177) has occurred. This bit is set to '0' by writing the INTERNAL CONTROL REGISTER bit 2 with a '1' or a RESET.

BIT 1 - READY. This bit is an inverted copy of the external -READY input signal. When this status bit is set to '1', the selected drive is ready. When set to '0' the selected drive is NOT ready.

3.7.2 WRITE PRECOMPENSATION REGISTER F1

This register contains the cylinder at which WRITE PRECOMPENSATION will be applied. The value read must be multiplied by 4. A value of 255 will result in no write precompensation/reduce write current. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.3 SECTOR COUNT REGISTER F2

This register contains the number of sectors to be processed. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.4 SECTOR NUMBER REGISTER F3

This register contains the starting sector number to be processed. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.5 CYLINDER (LSB) REGISTER F4

This register contains the starting (least significant byte) cylinder number to be processed. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.6 CYLINDER (MSB) REGISTER F5

This register contains the starting (most significant byte) cylinder number to be processed. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.7 SDH REGISTER F6

This register contains the controller ERROR CODE/SECTOR SIZE parameters along with the current DRIVE/HEAD select. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST). The bit definitions are:

BIT 7 - ERROR CODE. This bit specifies the error code to be used. If this bit is set to ONE, the data field will be appended with an ECC field If set to ZERO, the data field will be appended with a CRC field.

BITS 6, 5 - SECTOR SIZE. These bits specify the sector size to be used. The sector size definitions are:

BIT 6 5	
0 0 -	256 BYTE SECTOR
0 1 -	512 BYTE SECTOR
1 0 -	1024 BYTE SECTOR
1 1 -	128 BYTE SECTOR

BIT 4 - DRIVE SELECT. This bit specifies the drive to be selected. If this bit is set to ZERO, drive 0 is selected. If set to ONE, drive 1 is selected.

BITS 3-0 - HEAD SELECT. These bits specify the head to be selected.

3.7.8 COMMAND REGISTER F7

This register contains the command to be executed by the controller. It is read only after the ~COMMAND signal has been asserted.

3.8 MICROCOMPUTER WRITE REGISTER DESCRIPTION

3.8.1 HEAD SELECT REGISTER F0

This registers upper nibble (BITS 7,6,5,4) is written with the current head select (BIT 7 - HEAD 2^3, BIT 4 - HEAD 2^0) during head changes on multiple sector reads or writes. BIT 0 of this register enables or disables the 5098 identifier register. If a '1' is written to this bit, the identifier register will be accessed at HOST READ ADDRESS 3F1(371). If a '0' is written, the register is disabled.

3.8.2 ERROR REGISTER F1

This register is written with ERROR STATUS of the last command executed. The bit definitions are:

BIT 7 - BAD BLOCK FOUND. This indicates that the specified track has previously been formatted with the BAD TRACK flag set in the ID field. It is not possible to access data on this track and the command will be terminated.

BIT 6 - ECC ERROR. This indicates that a NON-ZERO syndrome was detected in a specified data field. If the data error was corrected by ECC, BIT 2 of the STATUS REGISTER will also be SET and the command will continue if more sectors are specified. If the data error was NOT corrected by ECC, BIT 0 of the STATUS REGISTER will be SET and the command terminated.

BIT 5 - NOT USED. Set to zero.

BIT 4 - ID NOT FOUND. This indicates that the controller was able to locate the correct cylinder and head numbers but was unable to locate the correct sector number. An ID CRC error can also generate this error condition.

BIT 3 - NOT USED. Set to zero.

BIT 2 - ABORTED COMMAND. The current command issued by the HOST has been aborted due to an undefined COMMAND OPCODE, or a WRITE FAULT/NOT READY condition exist on the selected drive.

BIT 1 - NO CYLINDER ZERO. This indicates that during a RECALIBRATION command or if retries are enabled no CYLINDER 000 was detected. This error occurs after the controller issues 2048 step pulses towards cylinder 000 and the selected drive does not respond with the TRACK 000 signal.

BIT 0 - NO DATA MARK FOUND. This indicates that the controller was able to locate the sector but was unable to locate the data mark associated with it.

3.8.3 SECTOR COUNT REGISTER F2

This register is written with the number of sectors processed. It is read by the host only after a command has been executed by the controller.

3.8.4 SECTOR NUMBER REGISTER F3

This register is written with the sector number that has an error by the controller. It is read by the host only after a command has been executed by the controller.

3.8.5 CYLINDER (LSB) REGISTER F4

This register is written with the cylinder LSB number that has an error by the controller. It is read by the host only after a command has been executed by the controller.

3.8.6 CYLINDER (MSB) REGISTER F5

This register is written with the cylinder MSB number that has an error by the controller. It is read by the host only after a command has been executed by the controller.

3.8.7 SDH REGISTER F6

This register is written with the size/drive/head number that has an error by the controller. It is read by the host only after a command has been executed by the controller. The bit definitions are:

BIT 7 - ERROR CODE. This bit indicates the error code selected. If this bit is set to ONE, the data field will be appended with an ECC field. If set to ZERO, the data field will be appended with a CRC field.

BITS 6, 5 - SECTOR SIZE. These bits indicate the sector size selected. Their definitions are:

BIT 6 5	
0 0 -	256 BYTE SECTOR
0 1 -	512 BYTE SECTOR
1 0 -	1024 BYTE SECTOR
1 1 -	128 BYTE SECTOR

BIT 4 - DRIVE SELECT. This bit reflects the selected drive. If this bit is set to ZERO, drive 0 is selected. If set to ONE, drive 1 is selected.

BITS 3-0 - HEAD SELECT. These bits indicate the selected head.

3.8.8 STATUS REGISTER F7

This register is written with the status by the controller. It is read by the host only after a command has been executed by the controller. The bit definitions are:

3.8.9 INTERNAL CONTROL REGISTER F8

This register is written by the controller and is used to control of the internal operations of the 5098. This register is set to 0 after a RESET. The bit definitions are:

BIT 7 - DMA_BUSY. This bit controls if DMA_INTRQ will cause BUSY status. Writing a '1' to this bit will enable DMA_INTRQ to cause the 5098 BUSY status. Writing a '0' will disable the DMA_INTRQ signal. Disabling DMA_INTRQ will not affect the BUSY state.

BIT 6 - SELECT. This bit controls the ~DS_0 or ~DS_1 output enable. If the DIS_SELECT (BIT 5) is not set, this bit has no meaning. Writing a '1' to this bit will enable the drive select signals. Writing a '0' will disable them.

BIT 5 - DIS_SELECT.

This bit enables or disables the drive select function. Writing a '1' to this bit will enable the drive select function. This causes the drive to be selected only during STATUS reads or the SELECT bit is set. Writing a '0' to this bit disables the drive select function leaving the drive select signals active at all times.

BIT 4 - DIS_MSB.

This bit enables or disables the most significant bit (MSB) of HOST REGISTER 3F7(377) during reads. Writing a '1' to this bit disables (tri-states) BIT 7 of HOST REGISTER 3F7(377). Writing a '0' enables (drives) it.

BIT 3 - DIS_WORD.

This bit enables or disables word (16 bit) data transfers. Writing a '1' to this bit enables word data transfers during read or writes to HOST REGISTER 1F0(170). While in WORD MODE, the ~IO_CS_16 and IO_CH_RDY signal are enabled. Writing a '0' causes byte (8 bit) data transfers during read or writes to HOST REGISTER 1F0(170). In this case, the ~IO_CS_16 and IO_CH_RDY signals are disabled.

BIT 2 - COMMAND

This bit is used to reset the ~COMMAND signal. Writing a '1' to this bit deasserts the ~COMMAND signal. Writing a '0' leaves the ~COMMAND signal in its current state.

BIT 1 - BUSY

This bit is used to set or reset the 5098 BUSY STATUS. Writing a '1' to this bit will set the BUSY STATUS. Writing a '0' will clear it.

BIT 0 - INTERRUPT

This bit is used to set or reset the INTRQ signal. Writing a '1' to this bit will set the INTRQ signal. Writing a '0' will clear it.

REV C: Writing a 0 to this bit has no effect on the INTRQ signal

3.8.10 DRIVE STATUS CONTROL REGISTER F9

This register is written by the controller and is used to control both the 5098 and the drive status. The bit definitions are:

BIT 7 - POLARITY. This bit specifies the polarity of the DMA_INTRQ input. Writing a '1' to this bit causes (if enabled) the 5098 BUSY STATUS to be set when DMA_INTRQ is a '1'. Writing a '0' causes BUSY STATUS when DMA_INTRQ is a '0'.

BITS 6 - DIS_BUSY. This bit enables or disables the 5098 BUSY STATUS. Writing a '1' to this bit disables BUSY. Writing a '0' enables BUSY.

BIT 5 - NOT_RDY_1. This bit allows the controller to override the ~READY signal for drive select 1. Writing a '1' to this bit will cause the 5098 to indicate DRIVE NOT READY status for drive select 1 regardless of the ~READY signal. Writing a '0' will allow the ~READY signal to indicate DRIVE NOT READY STATUS.

BIT 4 - WF_1. This bit specifies the WRITE_FAULT status for drive select 1. Writing a '1' to this bit will cause the 5098 to indicate WRITE FAULT status. Writing a '0' will signal no WRITE FAULT.

BIT 3 - SC_1. This bit specifies the SEEK COMPLETE status for drive select 1. Writing a '1' to this bit will cause the 5098 to indicate SEEK COMPLETE status. Writing a '0' will indicate NO SEEK COMPLETE status.

BIT 2 - NOT_RDY_0. This bit allows the controller to override the ~READY signal for drive select 0. Writing a '1' to this bit will cause the 5098 to indicate DRIVE NOT READY status for drive select 0 regardless of the ~READY signal. Writing a '0' will allow the ~READY signal to indicate DRIVE NOT READY STATUS.

BIT 1 - WF_0. This bit specifies the WRITE_FAULT status for drive select 0. Writing a '1' to this bit will cause the 5098 to indicate WRITE FAULT status. Writing a '0' will signal no WRITE FAULT.

BIT 0 - SC_0. This bit specifies the SEEK COMPLETE status for drive select 0. Writing a '1' to this bit will cause the 5098 to indicate SEEK COMPLETE status. Writing a '0' will indicate NO SEEK COMPLETE status.

3.8.11 BUSY COMMAND COMPARATOR REGISTER FA

This register is written by the controller and is used to allow for two commands that will not cause the 5098 to indicate BUSY status. It is organized into two nibbles. Bits 7,6,5,4 represent the first command, bits 3,2,1,0 represent the second. These nibbles correspond to bits 7,6,5,4 of HOST REGISTER 1F7(177). This register must be initialize prior to writing a command to the 5098.

3.8.12 5098 IDENTIFIER REGISTER FB

This register is written by the controller and is used to specify the controller type. It is accessed by the HOST (if enabled, see section 3.8.1) by reading HOST REGISTER 3F1(371).

3.8.13 ADDITIONAL CONTROL REGISTER FC (REV C ONLY)

This register allows extended control over the drive READY status and output signals IO_CH_RDY and ~IO_CS_16. The bit definitions are:

BITS 7-5 RESERVED. These bits are reserved.

BITS 4-3 SYS CLOCKS. These bits define the number of system clocks used to hold IO_CH_RDY de-asserted after the assertion of ~IO_CS_16. They are set to two clocks (01) on RESET. The clocks are defined as:

BIT	4	3	
	0	0	- zero clocks (disabled)
	0	1	- two clocks
	1	0	- three clocks
	1	1	- four clocks

BIT 2 - READY STATUS

This bit selects the origin of the drive ready status. It is set to '0' on RESET. Writing a '0' to this bit will cause the 5098 to operate in the REV B mode. Writing a '1' to this bit selects ready status from the internal register F9 bit 5 (drive 1) or bit 2 (drive 0). In this case, writing a '1' to bit 2 of internal register F9 will cause drive 0 to signal NOT READY status irrespective of the ~READY input signal. Writing a '0' to bit 2 of internal register F9 will cause drive 0 to signal READY status irrespective of the ~READY signal.

BIT 1 - DISABLE I/O READY.

This bit enables or disables the de-assertion of the IO_CH_RDY signal. Writing a '0' to this bit will enable the IO_CH_RDY logic. Writing a '1' to this bit will disable the IO_CH_RDY logic. In this case, the 5098C will not de-assert IO_CH_RDY even if data is NOT available. Use caution when disabling IO_CH_RDY.

BIT 0 - DISABLE ~IO_CS_16.

This bit enables or disables the assertion of the ~IO_CS_16 signal. Writing a '0' to this bit will enable the IO_CS_16 logic. Writing a '1' to this bit will disable the IO_CS_16 logic. In this case, the 5098C will not de-assert IO_CS_16 even if 16 bit data transfers are required. Use caution when disabling IO_CS_16.

SECTION 4

D. C. CHARACTERISTICS

4.1 Absolute Maximum Ratings:

* Voltages on all pins with respect to GND range from -0.3 V to +7.0 V.

* Ambient operating temperature is 0 degrees C. to +70 degrees C.

* Storage temperature ranges from -65 degrees C. to +150 degrees C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

4.2 Standard Test Conditions:

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

* +4.75 V < VCC < +5.25 V

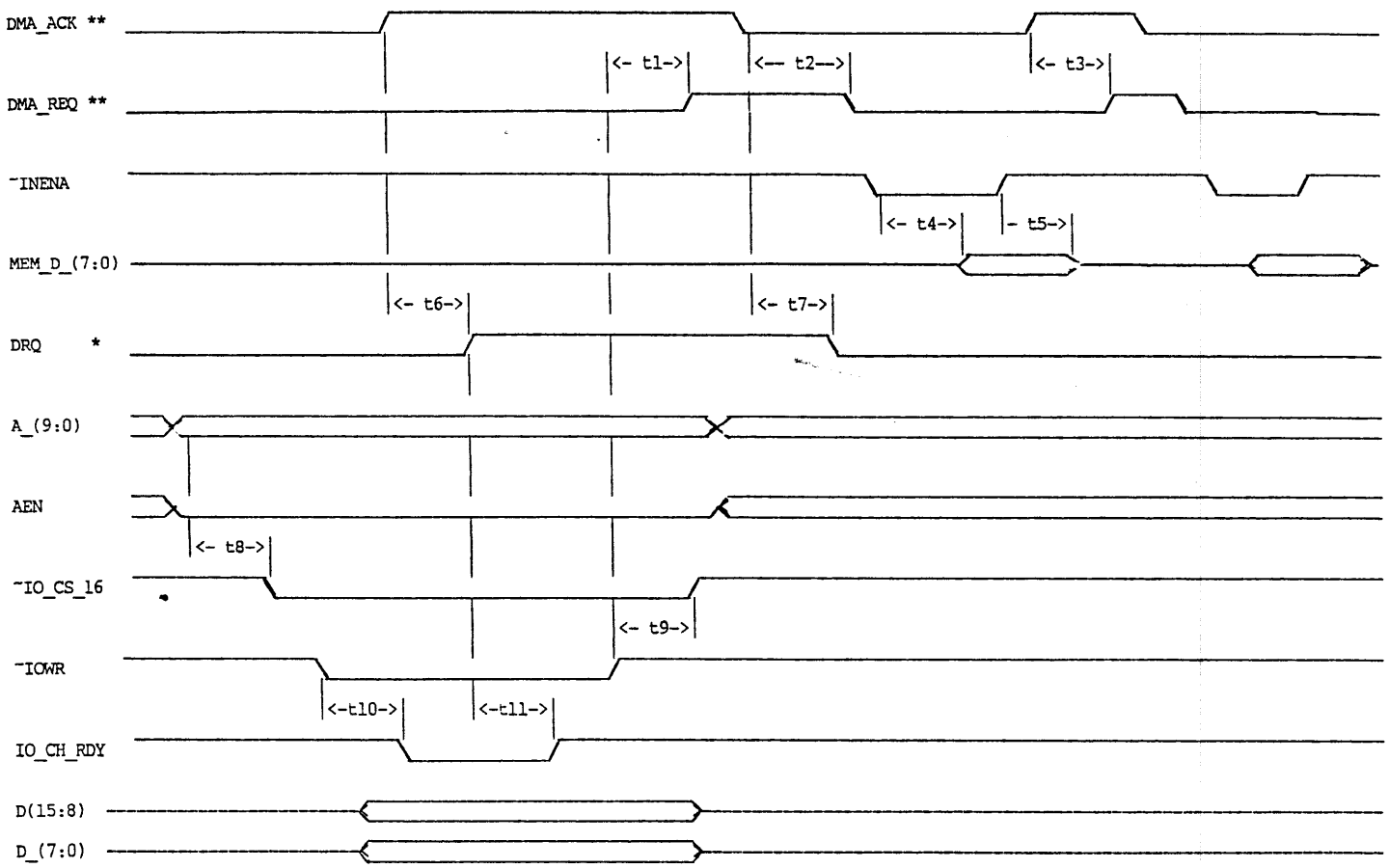
* GND = 0 V

* 0 degrees C. < TA < +70 degrees C.

4.3 D.C. Characteristics:

Parameter	Min	Max	Unit	Condition	Notes
Input High Voltage	2	VCC	V		
Input Low Voltage	-0.3	0.8	V		
Output High Voltage	2.4	VCC	V		
Output Low Voltage		0.4	V		
Output Low Current	4.0		mA		
Output High Current	-4.0		mA		
Output Low Current	12.0		mA		D_(15:0)
Output High Current	-12.0		mA		D_(15:0)
Output Low Current	24.0		mA		-DS_0&1 IO_CH_RDY -IO_CS_16
Input Leakage	-30	10	uA		
Output Leakage		10	uA		
VCC Supply Current		50	mA		

HOST DMA WRITE DATA TRANSFER (WORD MODE)



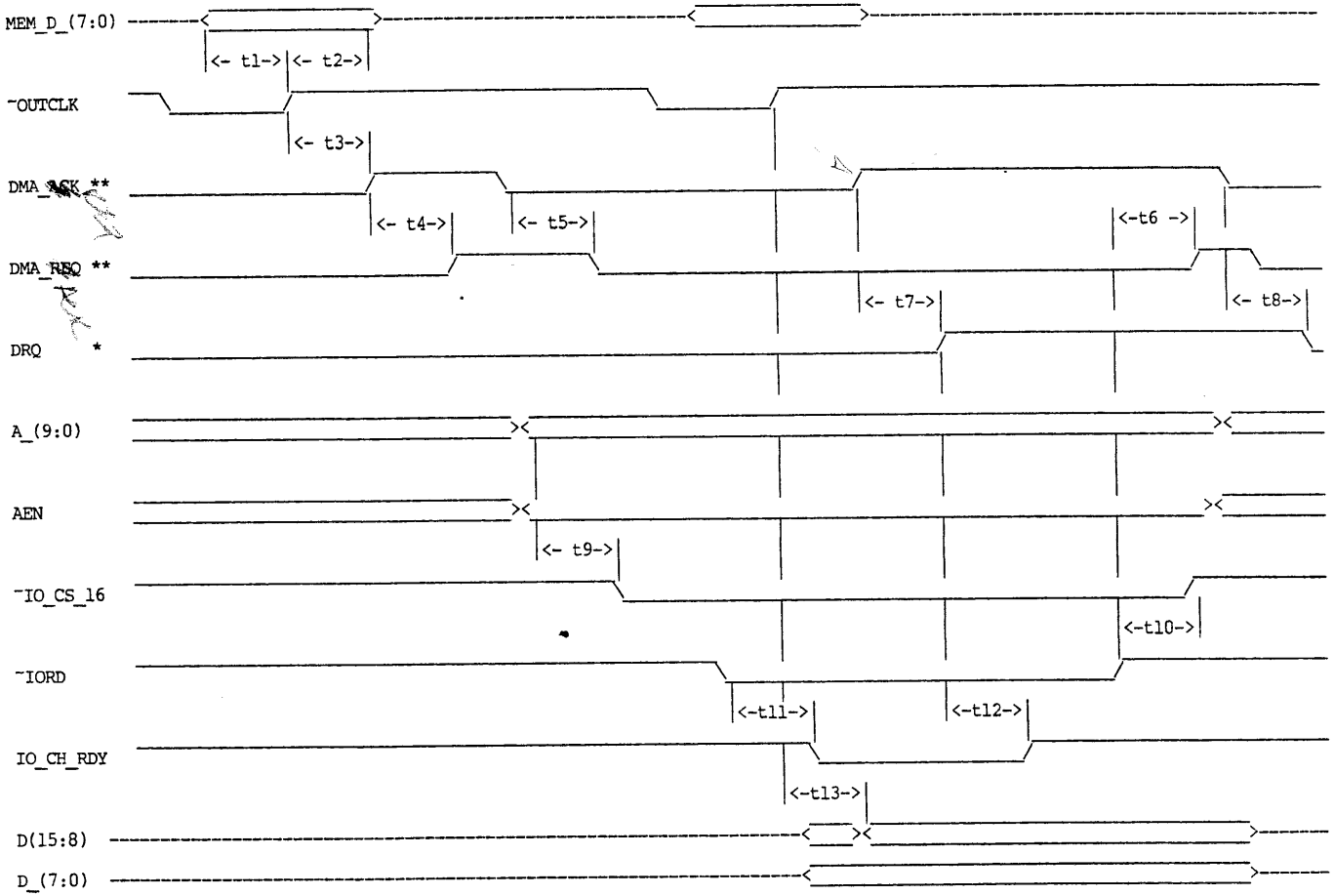
	DESCRIPTION	MIN	TYP	MAX	
t1	~IOWR DE-ASSERTED —> DMA_REQ ASSERTED			60	nS
t2	DMA_ACK ASSERTED —> DMA_REQ ASSERTED			25	nS
t3	DMA_ACK DE-ASSERTED —> DMA_REQ DE-ASSERTED			43	nS
t4	~INENA ASSERTED —> DATA VALID			48	nS
t5	MEM DATA HOLD	10			nS
t6	DMA_ACK ASSERTED —> DRQ ASSERTED			16	nS
t7	DMA_ACK DE-ASSERTED —> DRQ DE-ASSERTED			16	nS
t8	ADDRESS VALID —> ~IO_CS_16 ASSERTED			62	nS
t9	~IOWR DE-ASSERTED —> ~IO_CS_16 DE-ASSERTED	18		56	nS
t10	~IOWR ASSERTED —> IO_CH_RDY DE-ASSERTED			59	nS
t11	DRQ ASSERTED —> IO_CH_RDY ASSERTED			28	nS

** This timing diagram illustrates the SMS SCSI Mode of DMA Handshake, where these signals perform opposite of their nomenclature.[ie: DMA_ACK signal acts as the HOST REQUEST function,& the DMA_REQ signal acts as the HOST ACKNOWLEDGE function.]
See the SMS 5055 B (KOMBO) Technical Reference Manual for information on SCSI Mode of DMA.

* This signal is the DRQ STATUS BIT = BIT 3 of [illegible] REGISTER 1F7 (177).

20516B (5098B) TIMING SPECIFICATION

HOST DMA READ DATA TRANSFER (WORD MODE)



	DESCRIPTION	MIN	TYP	MAX	
t1	MEM DATA SETUP	40			nS
t2	MEM DATA HOLD	12			nS
t3	~OUTCLK ASSERTED-->DMA_ACK ASSERTED	25			nS
t4	DMA_ACK ASSERTED-->DMA_REQ ASSERTED			25	nS
t5	DMA_ACK DEASSERTED-->DMA_REQ DEASSERTED			25	nS
t6	~IORD DEASSERTED-->DRQ BIT CLEARED			20	nS

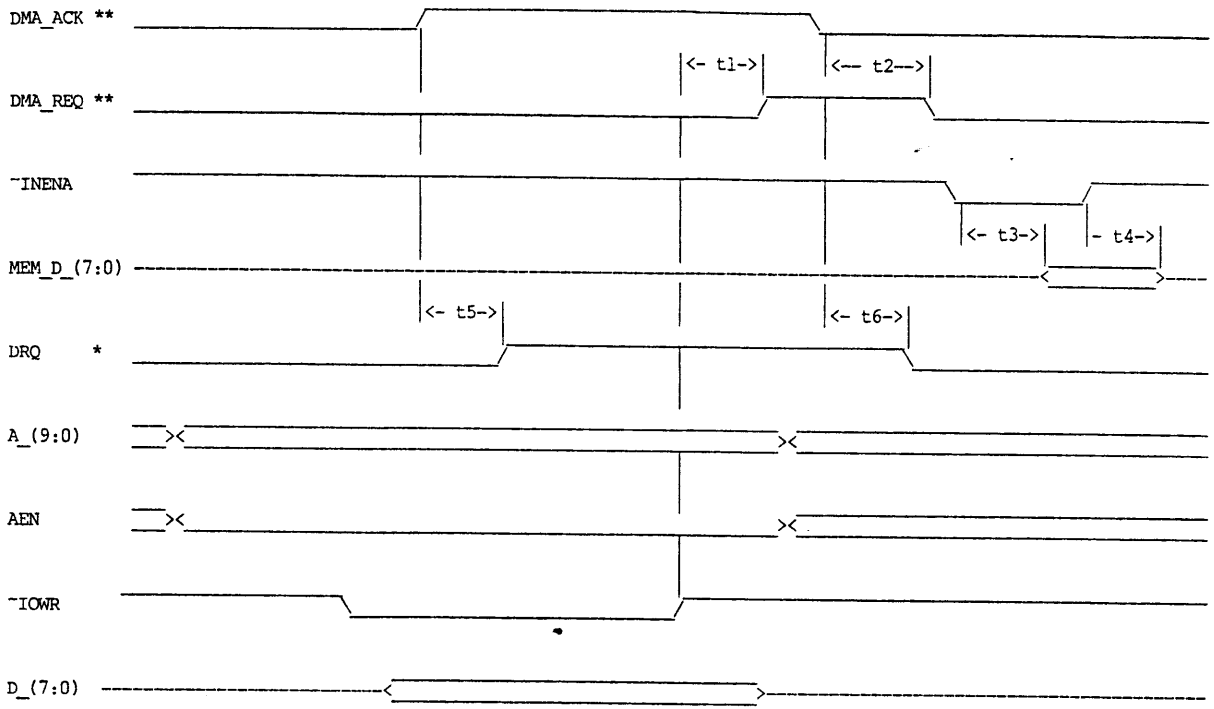
	DESCRIPTION	MIN	TYP	MAX	
t7	DMA_ACK ASSERTED --> DRQ ASSERTED			20	nS
t8	DMA_ACK DE-ASSERTED --> DRQ DE-ASSERTED			20	nS
t9	ADDRESS VALID --> ~IO_CS_16 ASSERTED			75	nS
t10	~IORD DE-ASSERTED --> ~IO_CS_16 DE-ASSERTED	18		70	nS
t11	~IORD ASSERTED --> IO_CH_RDY DE-ASSERTED			65	nS
t12	DRQ ASSERTED --> IO_CH_RDY ASSERTED			40	nS
t13	~OUTCLK DE-ASSERTED --> DATA (MSB) VALID			40	nS

** This timing diagram illustrates the SMS SCSI Mode of DMA Handshake, where these signals perform opposite of their nomenclature.[ie: DMA_ACK signal acts as the HOST REQUEST function,& the DMA_REQ signal acts as the HOST ACKNOWLEDGE function.]
See the SMS 5055 B (KOMBO) Technical Reference Manual for information on SCSI Mode of DMA.

* This signal is the DRQ STATUS BIT = BIT 3 of READ REGISTER 1F7 (177).

20516B (SMS 5098B) TIMING SPECIFICATION

HOST DMA WRITE DATA TRANSFER (BYTE MODE)



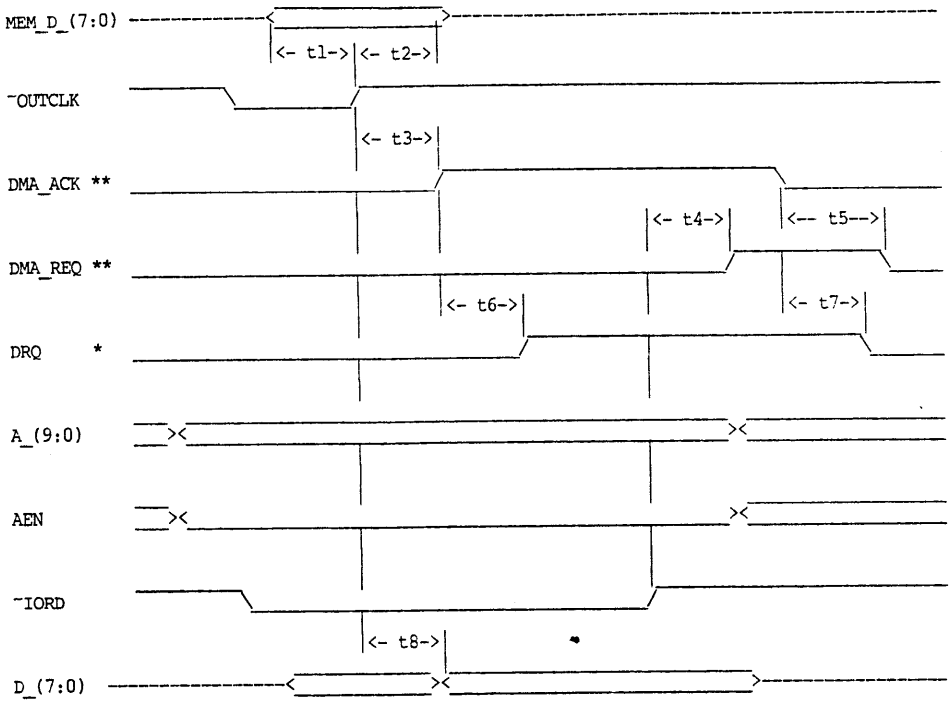
	DESCRIPTION	MIN	TYP	MAX
t1	~IOWR DE-ASSERTED --> DMA_REQ ASSERTED			60 nS
t2	DMA_ACK DE-ASSERTED --> DMA_REQ DE-ASSERTED			43 nS
t3	~INENA ASSERTED --> DATA VALID			48 nS
t4	MEM DATA HOLD	10		nS
t5	DMA_ACK ASSERTED --> DRQ ASSERTED			16 nS
t6	DMA_ACK DE-ASSERTED --> DRQ DE-ASSERTED			16 nS

** This timing diagram illustrates the SMS SCSI Mode of DMA Handshake, where these signals perform opposite of their nomenclature.[ie: DMA_ACK signal acts as the HOST REQUEST function,& the DMA_REQ signal acts as the HOST ACKNOWLEDGE function.]
See the SMS 5055 B (KOMBO) Technical Reference Manual for information on SCSI Mode of DMA.

* This signal is the DRQ STATUS BIT = BIT 3 of READ REGISTER 1F7 (177).

20516B (SMS 5098B) TIMING SPECIFICATION

HOST DMA READ DATA TRANSFER (BYTE MODE)



	DESCRIPTION	MIN	TYP	MAX	
t1	MEM DATA SETUP	40			nS
t2	MEM DATA HOLD	12			nS
t3	~OUTCLK ASSERTED --> DMA_ACK ASSERTED	25			nS
t4	~IORD DE-ASSERTED --> DMA_REQ ASSERTED			58	nS
t5	DMA_ACK DE-ASSERTED --> DRQ DE-ASSERTED			16	nS
t6	DMA_ACK ASSERTED --> DRQ ASSERTED			13	nS
t7	DMA_ACK DE-ASSERTED --> DMA_REQ DE-ASSERTED			30	nS
t8	~OUTCLK DE-ASSERTED --> DATA VALID			40	nS

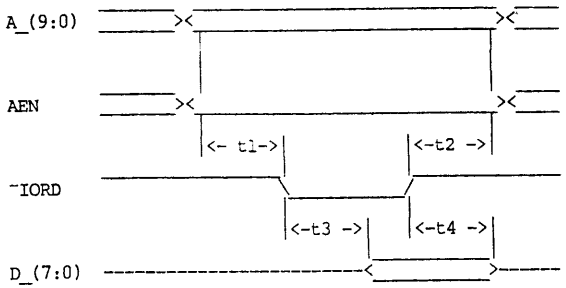
** This timing diagram illustrates the SMS SCSI Mode of DMA Handshake, where these signals perform opposite of their nomenclature.[ie: DMA_ACK signal acts as the HOST REQUEST function,& the DMA_REQ signal acts as the HOST ACKNOWLEDGE function.]
See the SMS 5055 B (KOMBO) Technical Reference Manual for information on SCSI Mode of DMA.

* This signal is the DRQ STATUS BIT = BIT 3 of READ REGISTER 1F7 (177).

[2 March 1988]

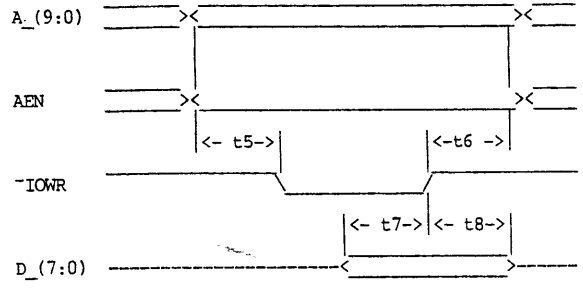
20516B (SMS 5098B) TIMING SPECIFICATION

HOST READ TIMING



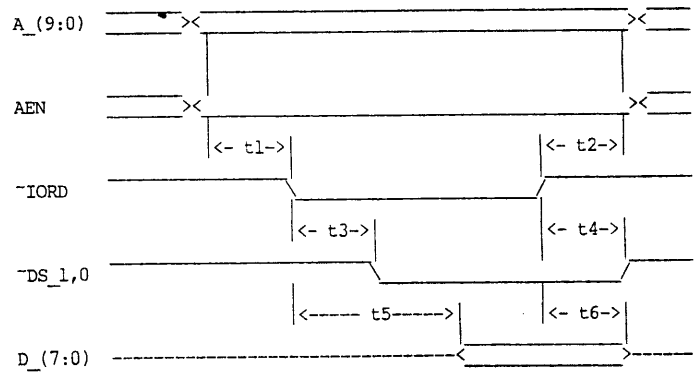
	DESCRIPTION	MIN	TYP	MAX	
t1	ADDRESS SETUP	20			nS
t2	ADDRESS HOLD	0			nS
t3	DATA VALID			75	nS
t4	DATA HOLD	12		50	nS

HOST WRITE TIMING



	DESCRIPTION	MIN	TYP	MAX	
t5	ADDRESS SETUP	20			nS
t6	ADDRESS HOLD	25			nS
t7	DATA SETUP	30			nS
t8	DATA HOLD	25			nS

HOST STATUS READ TIMING (NON-LATCHED)



	DESCRIPTION	MIN	TYP	MAX	
t1	ADDRESS SETUP	20			nS
t2	ADDRESS HOLD	0			nS
t3	~DS_1,0 ASSERTED			75	nS
t4	~DS_1,0 DE-ASSERTED			60	nS
t5	DATA VALID			90	nS
t6	DATA HOLD	12		50	nS

HOST WRITE TIMING