Oct 1968

UTS

Universal Time Sharing

1 INTRODUCTION

BPM -- the base for UTS

Why UTS

Elements of UTS

Components of the UTS Monitor

Building UTS from BPM

UTS Schedule

2 BPM -- THE BASE FOR UTS

Modern, General Purpose Batch Processing Monitor

Real Time Services concurrent with Batch

Concurrent Symbiont-Cooperative Peripheral I/O

New and Expanded BPM Services

3 WHY UTS ?

Success of experimental systems

Success of commercial systems

Need for Batch Processing plus on-line

Efficiency:

- Of CPU use by multiprogramming
- Of personnel by fast turn-around
- Of problem solving by on-line interaction

4 ELEMENTS OF UTS

Hardware Configuration

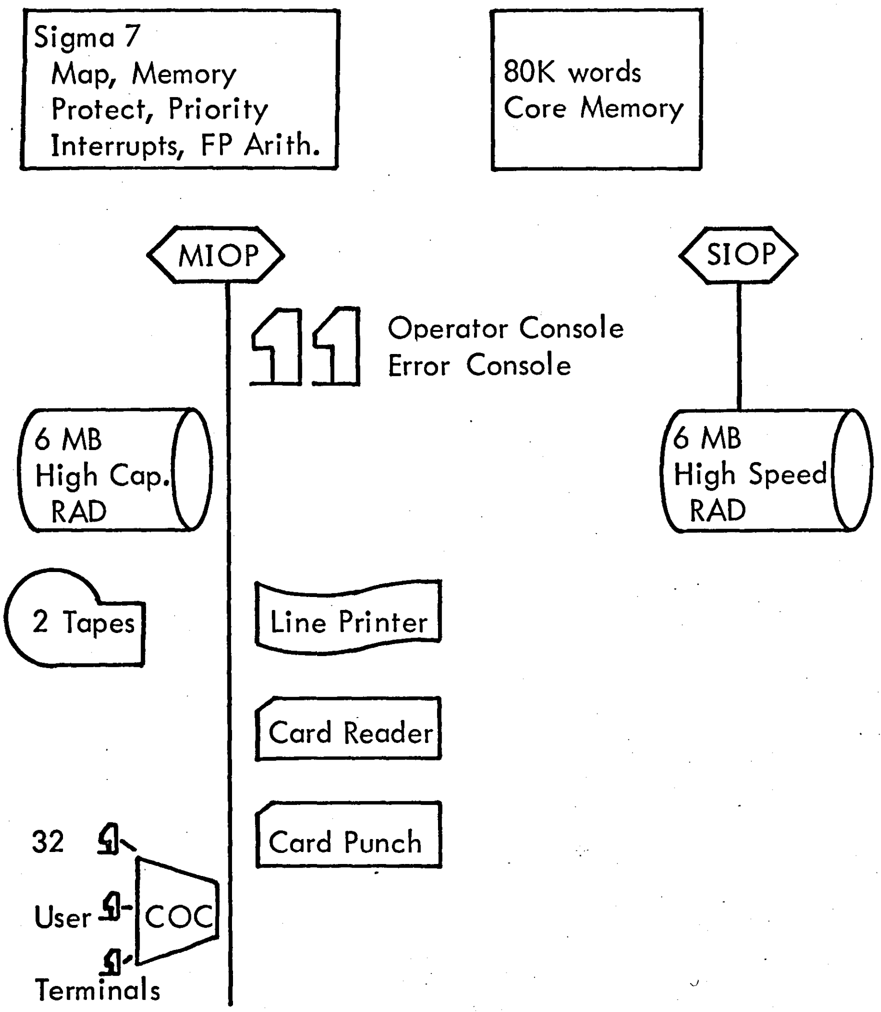
Shared Processors

UTM and related processors

Documentation

Coordination with other departments

5 HARDWARE CONFIGURATION



6 SHARED PROCESSORS

SDS FORTRAN	--	batch and on-line compatable
META SYMBOL	--	batch and on-line compatable
BASIC	--	batch and on-line interactive
FDP	--	on-line interactive
SDS MATH	--	on-line conversational

7 DOCUMENTATION

Functional Specs

User Manual

Implementation Specifications

Technical Manuals

8 COMPONENTS OF THE UTS MONITOR

Shared Processors
New Monitor Elements
Changes to BPM
Debugging Tools
Hardware Problem Defenses

9 UTM SHARED PROCESSORS

TEL	Terminal Executive Language
DELTA	Interactive Machine Language Debugger
EDIT	Context Editor for Text Files
PCL	Peripheral Interchange and Transformation
LINK	Program Leader supplying Symbol Tables

10 NEW MONITOR ELEMENTS

Console I/O Routines
Memory Management
Executive Scheduler
Swap Storage Manager
Performance Display
System Management

11 CHANGES TO BPM

Scheduler Communications
Virtual-Physical Address Translation
Interrupt and Trap Handlers
Accounting

12 DEBUGGING TOOLS

Executive DELTA
Event Count, Time, Mark
I/O Activity Recorder
Instruction Trace

13 HARDWARE PROBLEM DEFENSES

Error and Failure Reporting

Failure Recovery

Software Consistency Checks

Dynamic hardware reconfiguration

On-line diagnostics

14 BUILDING UTS FROM BPM

Base BPM System

Advantages for UTM development

Steps in UTM development

15 BASE BPM SYSTEM

BPM version B00

Symbiont

16K resident real-time area

Executive DELTA resident and "in control"

Resident monitor symbol table

16 BASE SYSTEM ADVANTAGES

BPM maintained and used continuously

UTM developed in RT area using RT services

Swapping and Scheduling algorithms are tested

System "efficiency" is measured

Early QA availability of partial systems

17a STEPS IN UTM DEVELOPMENT

Load "prototype" system into RT area

Execution scheduling, mapping, console I/O, DELTA

TRAP control, BREAK control, breakpoints

Clock controlled time slicing, batch background

User I/O, EDITOR, PCL

Swapping and memory management

17b STEPS IN UTM DEVELOPMENT (cont'd)

Log on, log off, processor calls

LINK loaded programs with symbol tables

Shared Processors

System Management displays and controls

SYSGEN - SYSMAK

18a UTS SCHEDULE

Assumptions

Status of UTM Elements

UTM Benchmarks

Pert Chart

18b UTS Project August Completion

12 programmers (full and part time)

9 man years of programmer time

11 months elapsed time

15,000 lines of code (new and changed)

1000 hours of machine time

18c Assumptions

25 - 100 lines of code/programmer/week

1 - 4 hours machine time/100 lines of code

Typical project time breakdown:

Design	40%
Coding	10%
Debugging	10%
Integration	30%
Documentation	10%

19 STATUS OF UTM ELEMENTS

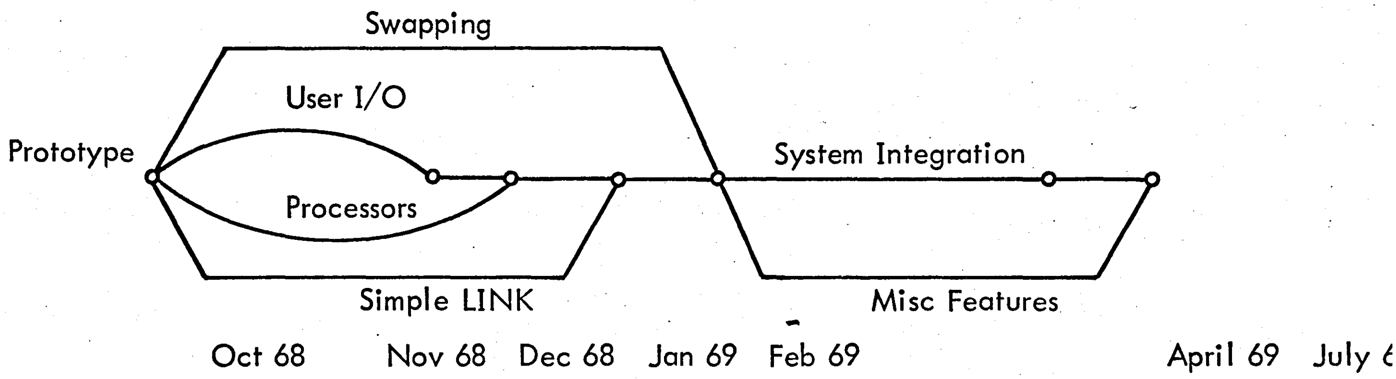
10/5/68 - Percent Complete

	Design	Coding	Stand Alone Check	System Integration
Exec DELTA	100	90	98	98
User DELTA	100	90	70	50
COC routines	75	50	50	20
EDIT	100	90	90	0
PCL	100	80	80	0
LINK	90	50	30	0
TEL	60	10	2	0
Memory Manage	90	20	2	2
Execution Scheduler	90	70	70	60
Swap Manage	80	5	0	0
Swap Scheduler	80	5	0	0
Traps & Interrupts	80	20	20	10
System Integration	80	0	0	0

20 UTM BENCHMARKS

Prototype -- DELTA, COC, simple scheduling & mapping	Oct 68
User I/O; Log on, Log off; processor calls	Nov 68
Processors -- PCL, EDITOR, TEL	Dec 68
Simple program loading - LINK	Jan 69
Swapping and advanced memory management	Feb 69
System integration	April 69
Misc -- Processor integration, System Mgmt, System Recovery	July 69

21 PERT CHART

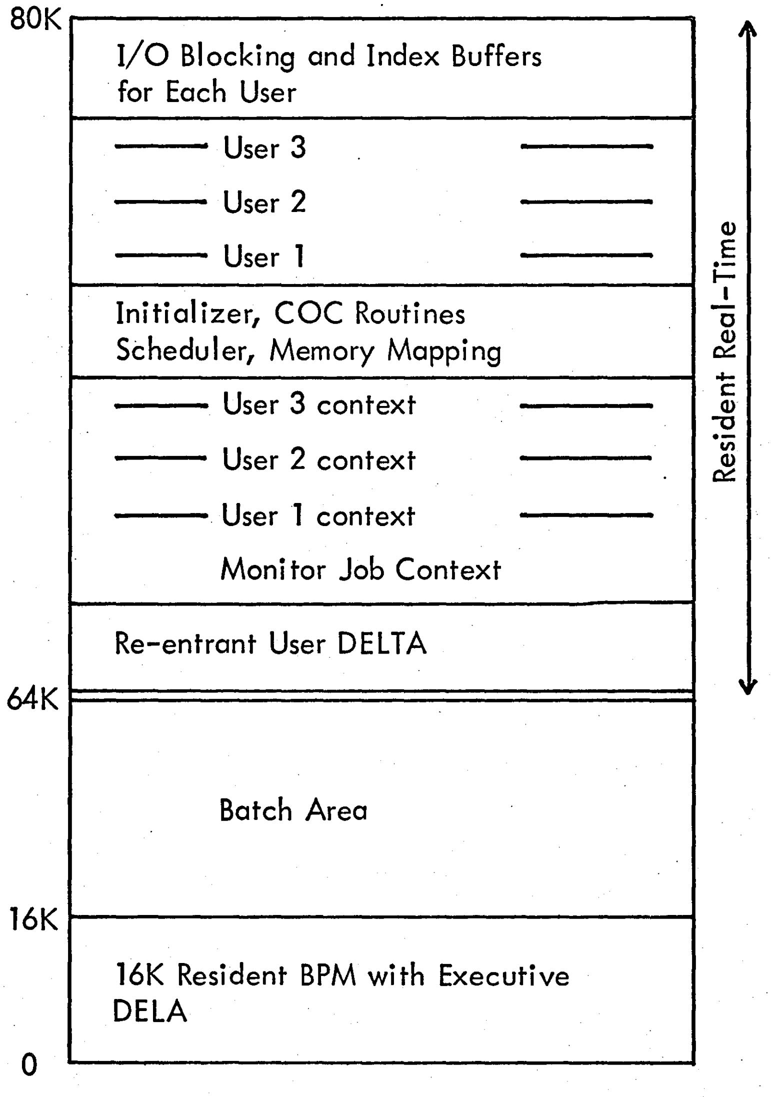


22 UTM IMPLEMENTATION SELECTED DETAILS

UTM Implementation Details .

- Proto-type physical core layout
- UTM Virtual memory layout
- Scheduler operation - states and state transitions
- RAD layout for swapping

23 PROTOTYPE UTS PHYSICAL CORE



80K

I/O Blocking and Index Buffers for Each User

User 3

User 2

User 1

Initializer, COC Routines Scheduler, Memory Mapping

User 3 context

User 2 context

User 1 context

Monitor Job Context

Re-entrant User DELTA

64K

Batch Area

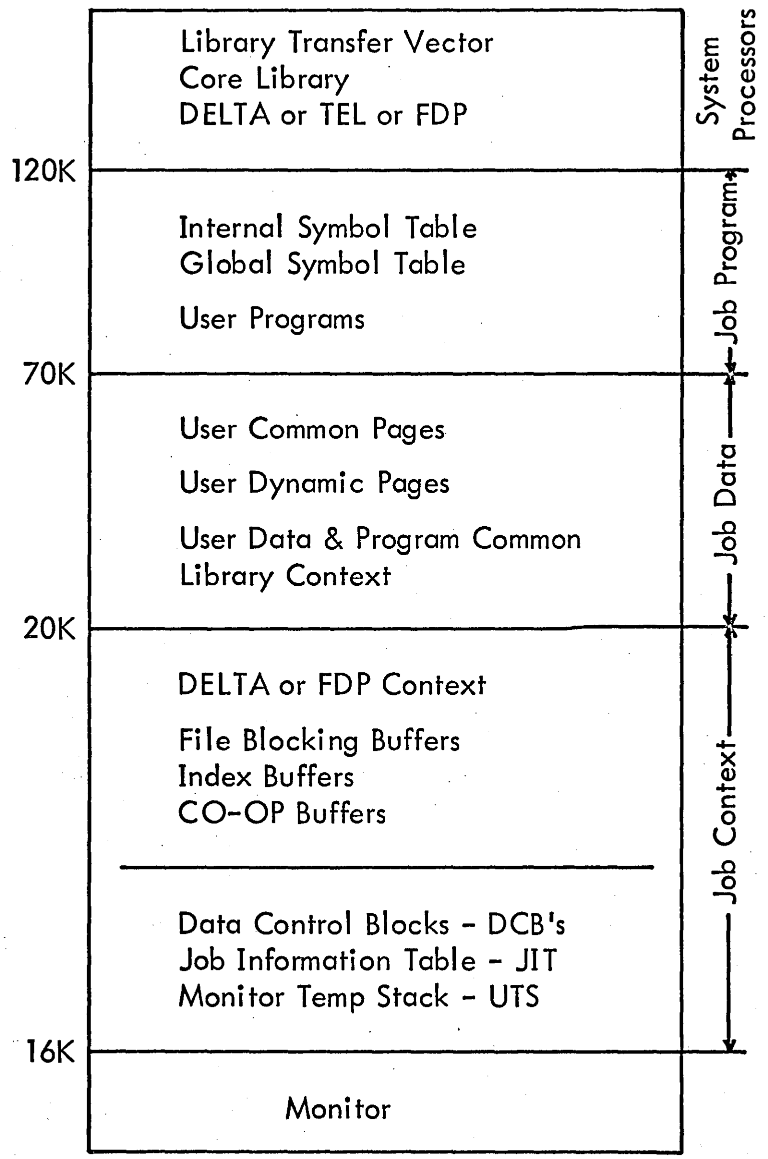
16K

16K Resident BPM with Executive DELA

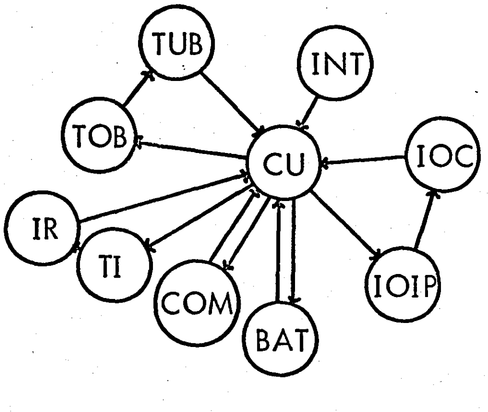
0

Resident Real-Time

24 UTM VIRTUAL MEMORY LAYOUT



25 SCHEDULER STATES AND TRANSITIONS



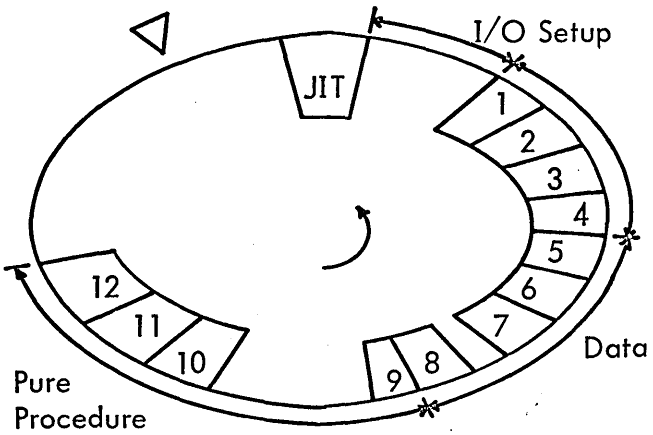
Execution Selection

INT	- interruptions
IR	- terminal input ready
TUB	- terminal output unblock
IOC	- file I/O complete
COM	- compute bound
BAT	- batch

Out Swap Selection

TI	- terminal inputting
TOB	- terminal output block
BAT	- batch
COM	- compute bound

26 RAD LAYOUT FOR SWAP



27 UTS SYSTEM RESPONSE

UTS System Response

Characteristics of users and programs

RAD utilization

CPU utilization

Response times under various loads

28a USAGE PROFILE

On-line users:

75% Typing commands
15% Terminal output bound
10% Compute bound

20 seconds between commands
5 char/sec/terminal total I/O rate
3 file I/O requests/terminal command
50 ms compute time per interactive command
4 K average user program size

28b Terminal Time:

50% Editor
30% Basic
10% FDP
5% DELTA
5% Other - compile, assemble, execute

28c USAGE PROFILE (cont'd)

Execution Time:

5%	Editor
10%	Basic
10%	FDP
5%	DELTA
70%	Other

29 RAD LOADS

	RAD transfers/sec
Card and Printer Symbiont	3.8
Batch File I/O	2.0
Terminal File I/O (30 Users)	4.5
Swaps for Interactive Users	3.0
Swaps for Time Slicing	6.7
Monitor File Activity	5.5
	25.5

7232 load 95%
7212 load 51%

30 CPU LOADS

	% of Sigma 7
Card and Printer Symbiont	5
Memory Interference	5
Swap I/O Management	1
File I/O Management	17
Terminal I/O (30 Users)	1
Interactive Service (30 Users)	8
	37%

Remaining for computation 63%

31 TERMINAL RESPONSE TIME

Case	1	2	3	4
Users	30	30	60	60
User size	4K	12K	12K	4K
CPU Load (RT + ouhd)	.29	.29	.32	.78
RAD Load	.54	.62	.79	.71
Interactive Load	.07	.07	.15	.15
Average delay (ms.)	149	188	241	540

32 DIFFERENCES FROM BTM

Differences from BTM

- Uses Map
- Multiple Users in Core
- Schedules on I/O
- Real-Time Available
- Shared Processors