N= 17473/002/00

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DATE 1 February 1962 PAGE 1 OF 1 PA

NOTE *an internal working paper*

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TWIN MODE WITH AOR, SOR, AND ATR

The XD-1A does NOT check for the "illegal" twin mode with AOR, SOR, and ATR, that is, it will twin. The twin process is such that twinning occurs EACH time the word passes from the exchange register to the A register.

For Example:

AØR, twin mode, bytes 0, 1, 2, 3, 4, 7 active, displacement 1

Original memory word	00112233	44556677
Original accumulator	01234567	76543210
New memory word	00112300	00556600
New accumulator	77001123	00000023

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TWIN MODE WITH AOR, SOR, AND ATR

This Note corrects the example in the original Note.

The XD-1A does NOT check for the "illegal" twin mode with AOR, SOR, and ATR, that is, it will twin. The twin process is such that twinning occurs EACH time the word passes from the exchange register to the A register.

For Example:

AØR, twin mode, bytes 0, 1, 2, 3, 4, 7 active, displacement 1		
Original memory word	00112233	44556677
Original accumulator	01234567	76543210
New memory word	00112377	00556677
New accumulator	77001123	77000023

(last page)

Active Notes

Store Class Instructions

001 Half-word mode with AOR, SOR, and ATR
002/01 Twin mode with AOR, SOR, and ATR

Miscellaneous Class Instructions

003 Use of U Modifier Codes with BSN and PER

Arithmetic Unit

001 Half-word mode with AOR, SOR, and ATR
002/01 Twin mode with AOR, SOR, and ATR