SAGE

COMPUTER TECHNOLOGY

SERVICE MANUAL

SAGE II

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35 N. EDISON SUITE #4

RENO, NV 89502

SAGE II SERVICE MANUAL VERSION I.0

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I DESCRIPTION OF DIAGNOSTIC AIDS :

The Service Kit contains several major diagnostic aids for the SAGE II user/dealer and are explained in detail in this document. Briefly, they are

The POWER-UP (OR BOOT) TEST resides in the PROMS of the SAGE II and is always executed on power-up or reset. It provides a good overall system checkout. Troubleshooting at this level is aimed at a user with good digital hardware experience.

The CYCLER test is a system exerciser. Tests of all major system components are repeatedly executed. The disk test is especially useful for identifying the true performance of a drive. This test can be run by any user but hardware experience will be necessary to isolate some types of problems and repair them.

The ALIGNMENT test is used to determine if a drive is misaligned. Simple, step-by-step instructions and a new philosophy of testing using a specially formatted diagnostic diskette make this test easy to run.

The CLEANER program is used with a diskette cleaning kit to clean the heads of a floppy drive. Often disk errors are due to simple dirt buildup.

The ERROR LOOKUP list is a list of error messages and what they mean.

Also available are descriptions of the system operation with some valuable trouble shooting hints.

II DIAGNOSTIC AIDS AVAILABLE :

In order to use some of the diagnostics described in this manual you will need either the software and/or hardware that goes with that test. These diagnostics aids are available from SAGE:

		Sage PN#
1	SAGE II User's manual	DC0000
1	Service Manual	DC0031
1	Test interface	SU0003
2	Test diskettes .. 80/80 40/40	SF0008
2	Scratch diskettes..(Box of 10)	DK0002
1	Alignment diskette	SF0009
	DYSAN #506-400 (80 trk) double density 16 sectors/256 bytes	
1	Diskette cleaning kit	DK0003
	VERBATIM #21145	

Additional equipment needed:

#1 or #2 Phillips head screw driver
Oscilloscope
heat gun
cans of "freeze" such as FREEZ-IT
Chemtronics
Hauppauge, NY 11788

An isolated soldering iron with a small tip. It is important that the soldering iron be no more than 25 Watts (or temperature controlled) with a small tip. A large iron will "lift" the traces and damage the board badly.

anti-static mat

ground straps for technician

The repair area must have an anti-static mat to place the CPU boards on and a ground strap for the technician as he is working on the board. The technician must always touch the mat to discharge himself before working on the unit.

III CARE AND HANDLING PROCEDURES :

Some components internal to the SAGE are sensitive to improper handling. Static especially is known to cause damage to both CMOS and LSI circuits. Industry quidelines have been established to reduce static damage and should be followed with no deviation. This section gives the procedures SAGE considers most important.

III.01 CIRCUIT BOARD HANDLING :

Circuit boards shall only be handled on or over anti-static mats.

Users shall ALWAYS be grounded to the mat.

Circuit boards shall only be stacked if a layer of conductive foam is placed between boards.

Circuit boards shall only be stacked 8 high.

III.02 CHIP HANDLING :

Chips shall ONLY be handled on anti-static mats with the user grounded to the mat.

III.03 DISK DRIVE HANDLING :

Disk drives shall be grasped only from the front plastic bezel.

Disk drives shall be very gently handled at all times.

Disk drives shall always be stored on edge.

Disk drives shall always be stored with cardboard shipping diskette in place.

Disk drive doors shall never ever be closed without either a diskette or cardboard shipping diskette in place.

Disk drives shall only be handled and placed on anti-static mats. Before touching any disk drive the handler shall discharge himself to the anti-static mat first.

III.04 MICROPOLIS DISK DRIVE HANDLING :

The MICROPOLIS disk drives are handled as above with these differences:

1. The door may be closed with nothing in the drive.
2. The disk drives are shipped without a packing diskette.

IV SOFTWARE INSTALLATION :

The SAGE II Diagnostic software is shipped on two diskettes, one 80 track and one 40 track. Each diskette has a complete set of code and source files. The diskettes boot to a menu program which runs each test as selected.

The master diskettes shipped from SAGE should be backed up using the Filer and safely stored. As bad systems tend to destroy diskettes, this is a very important safety precaution.

As the diskettes hold both source and code, it is advised that service personnel create work diskettes that hold only the code files. This is done by making a direct copy (boot area also) and then deleting all ".TEXT" files except "USERLIB.TEXT" from the new floppy.

A bridge system (one with an 80 track drive and a 40 track drive) can be tested by using SAGEUTIL to change the floppy parameters. For example:

Boot the 80 track diskette (usually in drive #4:) to the TEST MENU.
Then type "E" Exit to the command line.
"X" Xecute SAGEUTIL.
"C" Configure.
"O" change ON-LINE. (or "F" then "SYSTEM.MISCINFO <cr>" when building an 80/40 test diskette.)
"F" floppy change.
"5" the 40 trk floppy drive (or 4 if left drive).
"B" to set to 40 track SAGE format.
"Z" to set to non-standard parameters for CYCLER to run properly.
"F1 <cr>" set the number of retries =1
"J" set Read after write OFF.
<cr> type return until "Ready to write...?"
"Y" updates configuration
"Q" until back at command line.
"I" to re-init to test menu.

If desired, an 80/40 diskette can be made by duplicating an 80 track diskette and making the changes as above only changing SYSTEM.MISCINFO on the diskette itself instead of ON-LINE.

V SYSTEM LEVEL TROUBLE SHOOTING :

1. Connect the power cord and terminal. Turn the power switch on. During a normal power-on the front panel LED is RED for a fraction of a second. Then it turns green for the startup test until the boot from the floppy is finished. It should stay green except for flashes of red.

2. If LED stays dark then the power supply may not be working. If LED stays RED then the cpu board may not be working. If LED is blinking then the cpu cannot access the terminal chip.

3. If the LED is dark see the section on CHECK THE POWER SUPPLY.

4. Insert the boot diskette and press reset.

5. If no sign-on message appears or one of the following errors occur, replace the computer board.

   Exception error Parity error Memory error

   These errors can also be caused by a power supply with an intermittent problem or whose voltages need adjusting.

6. If the sign-on appears ok but there is an error in booting the diskette (such as an error reading a system file, a drive error, or a CRC error) try booting on the other drive using the debugger command "IF1".

7. If there are two drives and neither one will boot the system, try replacing the computer board.

8. If there is only one drive or the computer board has been replaced on a two drive system, try replacing the boot disk drive. On a SAGE II this is the left-hand drive (#4:).

9. Replace the disk drive ribbon cable and try booting with the new cable.

10. Next, check the voltage at the disk drive circuit board itself where it comes out of the connector. If the voltage is out of spec, check the power supply voltage. If it is correct, replace the power wiring harness.

VI CHECKING THE POWER SUPPLY :

Check power supply for these DC voltage ranges:

5.0V =	4.9V to	5.2V
+12.0V =	11.5V to	13.0V
-12.0V =	-10.0V to	-13.5V

If the voltages do not seem right, or some are not there, disconnect any external devices from the board including the terminal, printer, power supply, and disk drives.

Apply a dummy load to the power supply by connecting the following resistors from the supply to ground.

+ 5V =	1.2 ohm	50 watt
+12V =	8.0 ohm	50 watt
-12V =	16 ohm	25 watt

Check the power supply voltages again. If the voltages are outside of the ranges then the voltage should be adjusted. (On the Compower power supply change the R116 trimmer.)

Adjust: + 5V to between 5.0 to 5.1V

Replace the power supply if this is not possible.

Check +12V for	11.5 to	13.0V
-12V for	-10.0 to	-13.5V

If the other voltages fall outside the limits replace the Power supply.

If the power supply checks out ok, then a short exists on the board, or on a peripheral being powered from the board.

To determine which section(s) have the short(s), apply a 5.0V, 3 amp current limited voltage to each of the three power supply inputs on the cpu board. Be careful to observe correct polarity. The voltage will drop on the section that is shorted.

Using the appropriate (usually most sensitive) scale of a DVM, measure the voltage between the power rail under test, and ground at various points on the board. The points with the least voltage across them indicate the area where the short is. In a new board the fault is usually a trace short or a solder bridge; in a board from the field the fault is usually a bad chip.

VI.01 REPLACING THE POWER SUPPLY :

1. Disconnect the power cord.

2. Remove all the screws around the vent holes on the back panel.

3. Disconnect all cables connected to the computer board.

4. Remove the circuit board fastenings.

   Gently bend the back panel outward so that the circuit board may be moved back sufficiently that the LED on the front will clear the front panel. Tilt the front edge of the board until it clears the top of the front panel. Slide the board forward to remove it from the chassis.

   The board, whether in, or out, of the chassis must only be handled with anti-static materials and procedures.

5. Disconnect the fan power cord on units which have the fan mounted on the power supply shield.

6. Remove the screws on the underside of the chassis which attach the supply shield to the chassis. Note: only the older models with Tandon disk drives have power supply shields.

7. Disconnect power connector from power supply.

8. Remove the four screws which secure the power supply to the chassis and remove the power supply from the chassis.

9. Install the new power supply in the reverse order.

VII POWER-UP ROUTINE :

The power-up routine is a diagnostic aid within itself. This section explains how it works and how to use it for troubleshooting. If the early portions of the boot fail, no error messages are given but the processor LED will turn RED. An oscilloscope is necessary to isolate the problem.

Versions of the PROMS before 3-Jan-83 do not have all of the diagnostic features described here. The differences are explained in the release updates found in the front of your SAGE Users' Manual.

The power-up routine resides in an 8K byte boot ROM. It contains simplex non-interrupt drivers for self-test of memory, processor and devices. Normally, the PROMS reside in memory at address FE0000 but on reset they are switched to reside at 000000.

On power-up or when the processor is RESET, the processor starts executing the boot program at memory location 0. The processor reads the initial stack pointer and initial start vector from ROM locations 0 and 4 respectively. The start vector points to the address of the initialization code. After the initial tests, the execution of an address over FE0000 causes the hardware to switch the ROMs back to their high memory location. Program execution continues out of the new ROM location.

Descriptions of the initialization tests follow. Note that the entire initialization test sequence can be continuosly repeated by setting the switches as described at the end of this section.

VII.01 INITIALIZATION :
First all the I/O chips are initialized to an "idle" condition.

CHECK THE DATA SIGNALS:

0000 then FFFF are written to FC0FFE repeatedly for about 100 msec. This is long enough to use an oscilloscope to verify that all of the data lines are indeed going high and low. A line that does not change is in error. Check for shorts to another line or a bad buffer/driver. If two lines are shorted together, the signal may still change but the level of the signal will be too low.

CHECK THE ADDRESS SIGNALS:

Another loop toggles all the address lines between 0 and 1 by sequentially reading addresses 000000, FFC0FE and 7FFE for 100 msec.

CHECK THE I/O CHIP SELECTS:

A third loop sequentially reads all the I/O ports (FFC001, FFC011...FFC081). Use an oscilloscope to verify that all the chip select lines change. The test repeats for about 100 ms.

SWITCH SETTINGS ARE READ:

Next, the terminal baud rate is determined by reading GROUP-A DIP switches on the rear panel.

SW3	**SW2**	**SW1**	**Terminal baud rate**
dwn	dwn	dwn	19.2K baud
dwn	dwn	up	9600
dwn	up	dwn	4800
dwn	up	up	2400
up	dwn	dwn	1200
up	dwn	up	600
up	up	dwn	300
up	up	up	reserved, will default to 19.2K baud.

SW4	**Parity control**
dwn	even parity enabled
up	parity disabled

On startup, the remote serial channel defaults to 8 data bits, 1 stop bit, and even parity.

The floppy drive option switch is read to determine which type of drive is installed (always double-density, double-sided format).

SW7	**FLOPPY CONFIGURATION**
up	40 track (48 TPI) drive
dwn	80 track (96 TPI) drive

The terminal displays:

" Sage II":

At this point the terminal is initialized. The first part of the sign-on message "SAGE II" is displayed. If no message is displayed, and the LED is blinking rapidly the cpu cannot access the terminal controller chip. The system must be reset to get it out of this condition.

Now the ROMs are switched to their normal address location. The last part of the sign-on message "Startup test" is displayed. If the system always dies before completing the sign-on message, the switch has been unsuccessful. Check the address lines, switch hardware and the boot ROMS themselves.

At this point, the display should read:

" Sage II Startup Test"

PROM CHECKSUM TEST:

Both PROMs have simple checksums. The ROM test calculates the checksum of the ROMs to insure that the BOOTSTRAP program itself is ok. Messages "PROM 1 bad" or "PROM 2 bad" will display if possible otherwise the CPU will halt and the CPU light will be RED. Because this error and a CPU error are catastrophic, no further information can be given. PROM 1 refers to the EVEN memory addresses (package U17) while PROM 2 refers to the ODD memory addresses (package U18).

VII.02 RAM MEMORY TEST :

All RAM memory existing in the system is tested next.

> NOTE:If Switches 5,6 and 8 of GROUP A are set OFF,OFF,ON respectively then this test will be bypassed and a message "Bypassed Init" will display. The processor enters the debugger. This option is used to inspect memory after a program crash.

The test of the first 128K of RAM is run in the following manner:

Each long word (4 bytes) is set to 00000000 and read back.

Each long word (4 bytes) is set to FFFFFFFF and read back.

Then it is set to its own address and program goes on to next long word. When all 128K is done, each long word is read to see if it still contains its address.

Then the top word of each 128K bank is read to see if that bank exists. Once the size of the additional memory is determined, it is checked just as the first 128K was.

This test will take a few seconds. Then the message

"RAM SIZE = XXXXXX" will be displayed.

If a bad memory location was found then an error is displayed:

BAD memory @ (addr) is (8 digit value) instead of (8 digit value)

The program stops at the first bad location it finds. Because it re-reads the location to print out the error message, the error value may be the expected value if the RAM is intermittent and reads correctly the second time. The processor will attempt to enter the debugger after a memory error. If the failed memory occurs in the debugger stack area (working down from 400H), the debugger may fail to operate correctly after the memory error.

VII.03 DISK BOOTSTRAP :

Next, the bootstrap switches are read to determine what device/program to boot to:

SW6	SW5	BOOT DEVICE
dwn	dwn	boot to DEBUGGER
dwn	up	boot to Floppy drive 0.
up	dwn	reserved, defaults to DEBUGGER
up	up	reserved, defaults to DEBUGGER

If the rear panel switches are set to boot from a floppy the screen will display:

"Booting from Floppy"

Then the first 1K of the BOOT diskette (first 2 sectors of 512 bytes each) are read into memory at location 400 hex. The first 4 bytes of this area should be the ASCII string 'BOOT' = 42 4F 4F 54 hex. If this information is not there then an error message is displayed:

"Not BOOT disk"

If a timeout occurs while trying to access the diskette, the program assumes there is no diskette there and outputs:

"Put in BOOT disk and press a key"

Typing a "Q" will display

"Boot aborted on drive 0"

and control will go to the DEBUGGER. Typing any other key will cause a re-try to boot from the Floppy.

If the system appears to try to boot, but dies before displaying the prompt line for the operating system, the problem may lie in the interrupt system. All I/O up to this point was done using the polled drivers in the monitor ROM. Once the system is read from the floppy, the interrupt driven I/O routines in SYSTEM.BIOS are used. The system files can be verified if another working SAGE II is present. The floppy drive could also be reading the files incorrectly.

Usually, if a floppy disk error occurs, one of these error messages will be given:

"Drive error (code) on drive (0 or 1)" where codes are:

01	- controller failure
02	- invalid command
03	- recalibrate or seek failure
04	- timeout
05	- missing address mark
06	- no data found
07	- overrun
08	- CRC error
09	- end-of-cylinder
0A	- unknown
0B	- address out-of-range

VII.04 SPECIAL MONITOR COMMANDS :
There are several monitor commands specifically designed for hardware trouble shooting.

ERx and EWx

These commands cause 4K of data to be transfered from/to the specified drive and block number.A period ('.') is displayed for each successful transfer while an 'X' is displayed for each unsuccessful transfer.

All errors are ignored by the system. Signals to the Floppy drive or controller can be viewed with an oscilloscope to determine the problem. By starting the read on a block # that is a multiple of 4, the side select line can be observed to toggle.

ER0 bbbb	Block bbbb (hex) on Unit #4 (left floppy) is continuously read.
ER1 bbbb	Block bbbb (hex) on Unit #5 (right floppy) is continuously read.
EW0 bbbb	Block bbbb (hex) on Unit #4 (left floppy) is continuously written to with all zeros. Remember to use a scratch diskette.
EW1 bbbb	Block bbbb (hex) on Unit #5 (right floppy) is continuously written to with all zeros. Remember to use a scratch diskette.

VII.05 MAINTENANCE TESTS :

ROM program versions after 3-Jan-83 have additional diagnostics that are controlled by the GROUP A switches at the back of the SAGE:

SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	MAINTENANCE TEST:
up	dwn	dwn	dwn	...	...	...	...	Bypassed init
up	dwn	dwn	up	...	...	...	...	Looped test (PROM)
up	dwn	up	dwn	...	...	...	...	RAM write loop
						dwn	dwn	00000 to 1FFFE
						dwn	up	20000 to 3FFFE
						up	dwn	40000 to 4FFFE
						up	up	60000 to 7FFFE
up	dwn	up	up	...	...	...	...	Looped test (Reserved)

When the system is reset a message for the type of test will be displayed. For example:

"SAGE II Startup Tests"
"RAM write loop"

The **Bypassed Init** selection overrides the normal startup sequence. When the reset button is pressed the debugger is automatically entered. The memory can be inspected. Register contents are invalid as they cannot be saved on reset. Stack memory from 400H down is used by the debugger so these locations may have changed. The flag at 104H is also cleared so that the debugger will not attempt to use the BIOS.

The **Looped test** selection repeats the startup tests in PROM over and over again. This is useful when watching signal lines with the oscilloscope. If the tests are seccessful the LED remains green for the duration of each pass and blinks red at the end of each pass. If any test fails the processor is stopped and the LED is set RED. The switches must be changed back (Switch 8 to dwn and switches 5 & 6 to your desired bootstrap selection) and the system reset to get out of the exercise loop.

The **RAM write loop** continuously loops through a selected bank (128K) of memory writing 0000 or FFFF as determined by switch 3 of GROUP B:

SW3 (Group B is also used for the IEEE-488 address)
dwn 0000 is written to the bank
up FFFF is written to the bank

VIII CPU BOARD TROUBLESHOOTING :

NOTE: These procedures are intended for troubleshooting a "dead" system. If the system boots properly, run CYCLER, clean the disk heads etc. before starting this checkout.

When the power is turned on or the reset button is pressed, a "dead" system sends no output to the terminal (except perhaps a couple of @@ signs) and stops with the processor LED set RED.

Most field problems are due to the failure of a chip or a chip that is not properly seated in its socket. Intermittent operation may be due to any of several different problems. If the system will operate most of the time refer to the CHECKLIST FOR intermittence section of this manual.

When troubleshooting a "dead" system keep in mind these hints from our experienced factory technicians:

TROUBLESHOOTING HINTS:

1. Faulty CPUs are very rare.
2. Faulty EPROMs are fairly common.
3. Faulty RAM chips are fairly common.
4. A faulty RAM cannot keep the system from giving a sign-on message. A faulty EPROM will do it all most every time.
5. Faulty delay lines do occur.
6. Faulty chips in the I/O section are rare.
7. Faulty capacitors may work for awhile but eventually degrade and cause intermittent problems.

These parts and RAM should not effect the sign-on message:

U3	RN1	U10	U11	U12	RN5	RN4	RN3
Rn2	U63	U62	U46	U40	U30	U23	U64
U31	U49	U6	U7	U8	U39	U58	U59
U21	U5	U73	U74	U2	U29	U20	U28

Even a "dead" system will have signal activity for a short time after reset is pressed. A scope probe can be used to examine all data, address, and control lines. Start with the PROM signals as this code is the first to execute. Check the I/O section last even if the signals there look suspect. It is very unlikely that the problem is in the I/O as the cpu has no interaction with this section until much later in the BOOT routine.

Specific checks of the important system signals follow. It will also help to have a good understanding of the Boot program. Refer to the section on the BOOT TEST in this manual.

VIII.01 CHECKING THE SYSTEM CLOCK :

Check these points with an oscilloscope. If there is no 8 Mhz clock then look for the problem indicated.

Pin 8 of U66 .... shorted crystal oscillator.
Pin 3 of U69 .... short or bad counter U69
Pin 15 of U68 .... open trace from U69-pin 3.
Pin 14 of U44 .... short or bad buffer U44.
Pin 13 of U37 .... open trace from U44-pin 14.
Pin 10 of U37 .... short or bad inverter U37.
Pin 8 of U54 .... 120 ohm resistor missing or wrong value or a shorted line

Check for 64 Khz at pin 9 of U75. If it is not there then trouble shoot counter chain of U69 and U67 and/or check for short on 64 Khz line. Check for 64 Khz at pin 11 of U34. It should be there if it was at U75-pin 9.

VIII.02 CHECKING THE ADDRESS STROBE LINE :

Check to see if AS+ pin 13 of U44 is either low or toggling.

If AS+ is not right then check pin 6 of U68 where the signal originates. It should be high or floating (if the processor is halted). If it is low check for either shorts, a bad U44, or a bad processor. (Note: Bad processors are very rare.)

If U68-pin 6 is ok then check the input on pin 17 of U44 for a high or floating signal. If it is not the same as U68-pin 6 check for an open trace. Check for a low on Pin 3 of U44 as the signal should be inverted through U44. If the input on pin 17 is ok, but pin 3 is high, then either the output is shorted or U44 is bad. U44-pin 3 and U44-pin 13 are connected and should have the same signal. If not check for an open trace or a bad socket.

Check for high at pin 2 of U15. A low or floating state indicates that U44 may be bad, the resistor may not be 120 ohms, or the trace is open. U15 itself or a short to another line could be the problem.

VIII.03 CHECKING THE REFRESH SIGNALS :

Check for the 64 Khz refresh signal at pin 3 of U32. If this is not correct, or the timing is slightly off then the delay line (U42) is bad (known to happen). U34, U32 or a pc board fault can also cause problems for the refresh signal. At this point, no matter how dead the board is you should have refresh signals to the RAMs. To check this send nothing but refresh signals to the RAMs by holding the reset switch in. Check RA0 - RA7 for missing signals or a signal shorted to another line. Signals which are shorted together will show a mid-level voltage between 0 and +5V at intervals during the refresh. They may cause inconsistent errors. Good signals will change quickly between ground and +5V without pausing in the middle.

VIII.04 CHECKING THE RAM SIGNALS :

Proper functioning of the RAMs is not necessary for the system to display the sign-on message when using either the RAM test ROMs or the normal Boot ROMs. The RAM circuitry can only affect the system start-up if it interferes with the data bus. Check the MC6889 buffers to see if they are shorted to the data bus. If the read signal is faulty, the buffers will always drive the bus on the processor side. To test this remove buffers U63, U62, U30 and U23. Reset and see if the sign-on message appears.

The other possible point of interference with the data bus can be caused by the data lines being shorted to the parity decoder chips U64 and U31.

VIII.05 REPLACING THE COMPUTER BOARD :

1. Disconnect the power cord.

2. Remove all but the two bottom screws around the vent holes on the back panel.

3. Disconnect all cables connected to the computer board.

4. Remove the fastenings securing the circuit board to the chassis.

5. Gently bend the back panel outward so that the circuit board may be moved back sufficiently that the LED on the front will clear the front panel. Tilt the front edge of the board until it clears the top of the front panel. Slide the board foreward to remove it from the chassis.

6. The board, either in or out of the chassis, must only be handled with anti-static procedures.

IX TEMPERATURE TEST :

Ideally, a service center will have a temperature chamber in which to place the system and vary the temperature up and down to determine if the unit is truly sensitive to temperature variations. As this method is very expensive and somewhat time-consuming, this test outlines some general guidelines for checking for a temperature problem.

The technician needs only a heat gun and cans of "freeze" spray.

The test is somewhat of an art as the technician has little idea of the true measure of the temperature being applied to the board. Beginners tend to fry or frost-bite chips doing more damage than good. Remember that the customer who complained of the problem is probably not trying to program in adverse weather conditions. Slight variations from the normal room temperature of your service center should be enough to identify the problem as "temperature sensitive" or not.

Remember that all systems have some hot or cold limit where they will normally quit operating.

OPERATION:

1. Remove the lid from the system.

2. If the system will boot fairly consistently, boot to CYCLER and start the test. Otherwise, set the switches on the back to reboot over and over (See the writeup on the POWER-UP routine) while varying the temperature.

3. **HEAT:** Visually divide the board into sections. Apply heat with a heat gun evenly over the section. The chips should be hot enough to cause discomfort if touched but not enough to burn the skin. Let the board cool down between intervals so that expansion and contraction occurs within the chips and socket connections. Do all sections of the board. If a problem occurs try to narrow the cause down to a single chip (or socket or connector).

4. **COOL:** A can of "freeze" spray can be used to check for temperature sensitivity in the cold range. Again use caution. Holding the nozzle on a chip will usually make the system fail and may permanently damage the chip. Use short bursts over sections of the board. Let the board warm up between bursts so that expansion and contraction occurs within the chips and socket connections.

Loose cables or bad sockets may masquerade as a temperature problem.

X INTERMITTANCE CHECKLIST :

If the system is intermittent, perform this checklist, then re-test with CYCLER:

1. RAMs are suspect in intermittent failures. If RAMDISK is being used, try operating without it. If no problem occurs, isolate the bad RAM by swapping one by one with a good RAM.

2. Check all cables and connectors. The cables should not have been pinched. Posts for cable connectors in the pc boards should stand solid and not wiggle when touched.

3. Inspect for chips that are not seated completely into the socket. Press down firmly on all chips to insure that they are making good connection with the socket. Inspect the pins of all the chips to see if any are curled under the chip instead of going into the socket. Look for foreign matter jammed in with the pin of a socket.

4. Are the capacitors the right values? Check their voltage rating. Underrated capacitors (68 uf 6v) across the 12V power supplies may have worked for some time before the caps finally degraded enough to cause problems. Even if the voltages look ok, any of these caps MUST be replaced with 10uf 25V caps as they will cause problems sooner or later.

5. Check for temperature sensitive chips. Use the TEMPERATURE test.

6. Check for improper solder connections. Inspect the board for grayish solder areas on the pins. All feed-through holes should be filled. "Beads" of solder instead of a smooth base on a pin are also suspect. Touch up the board with a small solder tip and run the CYCLER test.

XI CYCLER TEST :

CYCLER is a test of overall system performance. It is used both to diagnose problems and to validate GOOD systems. It is especially useful for finding disk drives that are not operating properly.

CYCLER tests

RAM MEMORY	
DISK STRAPPING	
DISK DRIVES	
SERIAL PORT	(modem port)
PARALLEL PORT	(printer port)
REAL TIME CLOCK	
ATTACH PROCESS	(interrupt check)
SWITCHES	(an optional test)

These tests are run repeatedly over many cycles. Each of the tests is described in separate chapters of this section. The test criteria for each test has been carefully determined and should not be changed by service personnel unless advised to do so by SAGE.

EQUIPMENT NEEDED:

CYCLER diskettes (set of 2)

A printer (optional) to print test results for record keeping.

OPERATION NOTES:

See the Software Installation notes if this is the first time CYCLER is being run or if the system to be tested is a BRIDGE system which has both an 80 track and a 40 track drive.

XI.01 TEST OPERATION :

1. POWER UP the SAGE II. It asks you to insert the boot diskette.

2. TEST DISK: Select a test diskette for the type of drives (80 track or 40 track) and insert it into the LEFT (#4:) drive.

3. TEST INTERFACE: Connect the INTERFACE serial and parallel connectors to the SAGE modem and printer ports.

4. BOOT: Type any key to boot to the test menu and select CYCLER:

   SYSTEM CYCLER TEST:
   Remove cycler diskette, insert scratch diskettes. DISKETTES READY?

   BE SURE TO REMOVE THE CYCLER DISKETTE AT THIS POINT OR IT MAY BE DESTROYED! Insert scratch diskettes into the drive(s) to be tested. Type "Y" to continue. ("N" will exit.)

5. CONFIGURATION: CYCLER shows the size of the disks and memory:
   ATTACH TEST PASSED

   ```
   *   512K of RAM            --will be tested.
   *   DISK #4:  =  80 track  --will be tested.
   *   DISK #5:  =  80 track  --will be tested.   START TEST?
   ```

   Type "Y" to start the test. Type "N" to ALTER the test.

6. TESTING: As each test is done, the terminal will display:

   ```
   PASSES =  n      (Stops after xxxx passes.)
   RAM...PASSED   CLOCK...PASSED   SERIAL...PASSED   PARALLEL...PASSED
   DISK #4:      hard = x   soft = x   data =x
   DISK #5:      hard = x   soft = x   data =x
   ```

   The tests will be repeated 250 times. The processor LED will stay GREEN with brief flashes during the disk tests. When finished, the LED will blink RED_GREEN. If the system dies, the LED will be RED.

7. TEST DONE: Type the "ESC" key to display errors.

XI.02 TEST ERROR DISPLAY :

At the end of the tests or if the test is interrupted the test menu and errors will be displayed:

```
Select:
  1...Print all errors  A...Alter test            N...New test
  G...Graph errors      R...Raw Data              K...Keep data on file
  4...Disk 4 errors     S...check Switches        C...Continue test
  5...Disk 5 errors     2...Print soft err graph  E...Exit Cycler
```

```
RESULTS:              PASS=  2 TEST INCOMPLETE.
RAM TEST ..................... PASSED
CLOCK TEST.................... FAILED ***  was 333 should be 342
SERIAL TEST................... FAILED ***  DTR to DSR  = high XMT=  0 RCV=  0
PARALLEL TEST................. FAILED ***  PRIME  to CD= low  XMT=  1 RCV=192

TOTAL DISK ERRORS: hard= 35 FAILED ***
                   soft=102 FAILED ***
                   data=  0 PASSED

DISK #4:    ERRORS: hard= 11 FAILED ***
                    soft= 30 FAILED *** at Head=0 Cyl=1 Soft errs=5
                    data=  0 PASSED

DISK #5:    ERRORS: hard= 24 FAILED ***
                    soft= 72 FAILED ***
                    data=  0 PASSED
```

All tests must pass in order for the system to pass. Refer to the description of each test for an explanation of the errors.

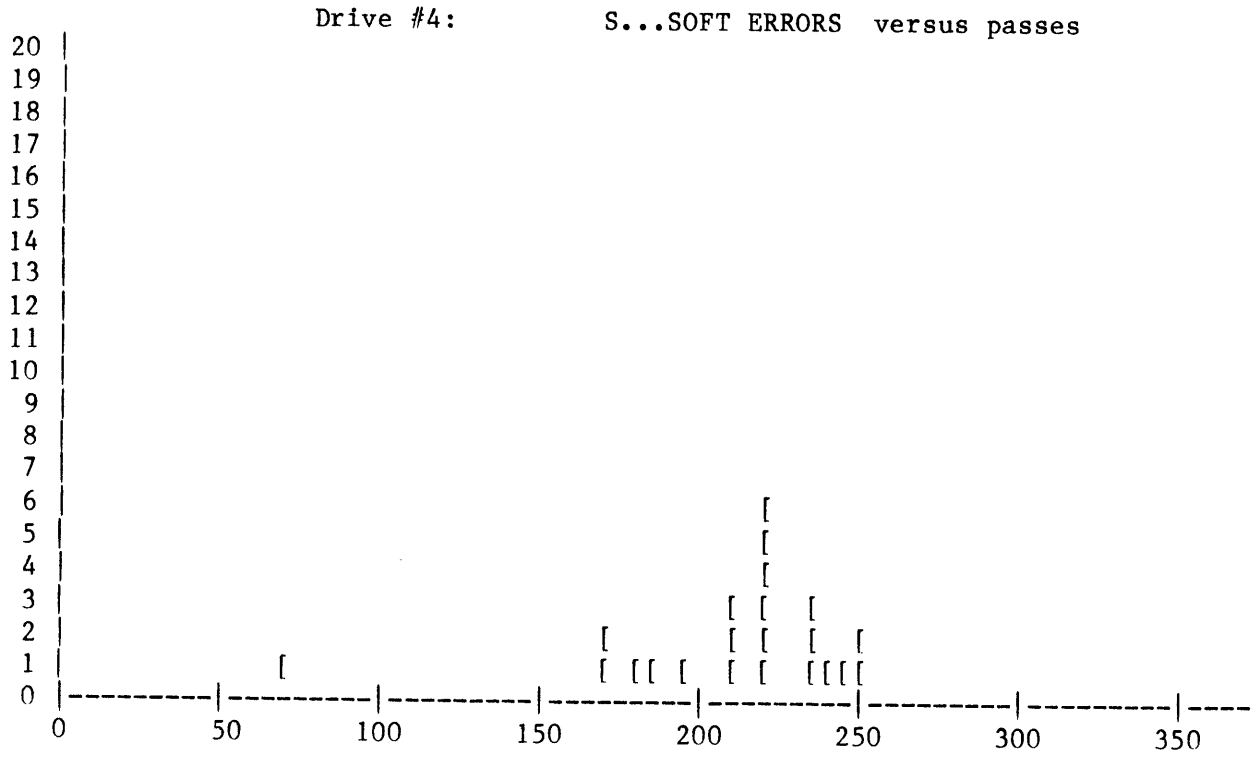
1...Print

The main error display, the soft err graph, the disk cylinder errors, and the disk head errors are printed just as they are displayed to the terminal. (3 pages of output). SAGEUTIL must be set for the correct printer and the system must have passed the SERIAL and PARALLEL tests for this to work. Changing the O...Output option in the Alter test selection will allow the information to be sent to a file. If the system has failed the disk tests sending the data to a file may not work.

G...Graph

This selection plots selected disk errors versus the test pass where the error(s) occurred. Choose the drive # (4=left or 5=right) and the type of error (hard, soft or data) to be plotted. Read or write errors can also be shown.

This graph shows that drive #4 is making more errors the longer it runs.



4...Disk #4 errors

5...Disk #5 errors

The total hard, soft and data errors are shown for each drive. #4: is the left drive and #5: is the right drive as you face the front of the SAGE.

```
DISK #4:   ERRORS: hard=  11 FAILED ***
                   soft=  30 FAILED *** at Head=0 Cyl=1 Soft errs=5
                   data=   0 PASSED
```

Then the soft errors for Head 0 and Head1 of each drive are shown where the values above the dashed line are for Head 0, the values below the line for Head 1. Disk #4 shows 4 soft errors on Head 0, cylinder 45 and 6 soft errors on Head 1, cylinder 52. More than 5 errors on any one head cylinder is unacceptable. The first such head cylinder found will be shown after the "FAILED ****' message on the main display.

```
      Disk #4   Head #0 (top) vs Head #1: (bottom)
                                                4
0---------1---------2---------3---------4---------5---------6-------
                                                  6
```

Next, the total hard soft and data errors per drive are shown with the hard, soft and data errors (in that order) for each cylinder.

Disk #4 shows 1 hard error on cylinder 70 and 8 soft errors on cylinder 2. Disk #4 has failed because no hard errors are acceptable. Also if more than 5 of the errors on cylinder 2 are on the same head, disk #4 has failed.

These errors are the sum of the errors on both heads. Remember that the failure criteria is PER HEAD so that the sum may show a cylinder with soft errors >5 that still passes. The disk HEAD errors display provides the individual errors for each cylinder/head.

```
 Dsk #4 Total errors per cylinder: (hard,soft,data)
 0:      1:      2: 8    3:      4:      5:      6:      7:
 8:      9:     10:     11:     12:     13:     14:     15:
16:     17:     18:     19:     20:     21:     22:     23:
24:     25:     26:     27:     28:     29:     30:     31:
32:     33:     34:     35:     36:     37:     38:     39:
40:     41:     42:     43:     44:     45:     46:     47:
48:     49:     50:     51:     52:     53:     54:     55:
56:     57:     58:     59:     60:     61:     62:     63:
64:     65:     66:     67:     68:     69:     70: 1   71:
72:     73:     74:     75:     76:     77:     78:     79:
```

A...ALTER

The ALTER option allows test parameters to be changed. Refer to section (undefined).

R...Raw data

The disk data is written in a raw form as it occurs with only the main drive totals added up during the test. This raw data is useful if information is needed on a particular error. It is displayed:

PASS=x drv=x WRT Cyl=x Hd=x Soft=x Hard=x Io=x Data=x

PASS = the number of the test pass that the error occurred on.
drv = either drive #4 (left) or drive #5 (right)
Cyl = the cylinder that had the error
WRT or RD = the error occurred on a write or read operation.
Soft = the number of soft errors
Hard = the number of hard errors
Io = the I/O error returned from the driver on a hard error.
Data = the number of data errors.

S...Check switches

This calls a routine which will display the values read from the 2 groups of dip switches on the back of the Sage II. The switch settings are displayed as if you were looking at the back:

GROUP A								GROUP B							
SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
dwn	dwn	dwn	dwn	up	dwn	dwn	dwn	up	up	up	dwn	dwn	dwn	dwn	dwn

The setting shown above has the system boot to the floppy with the IEEE-488 address set to 7.

To test a switch use the tip of a pen to "rock" the switch into position and type the space bar. The sense of the switch "up" or "dwn" should change.

Remember to return the switches to their initial settings or the SAGE II may not boot as expected. Type "R" to return to the error menu or "E" to exit the CYCLER program.

2...Print soft err graph

The soft errors for drive #4 and drive #5 are printed. This is a common option of the Graph errors selection and is included for

convenience.

N...New test

All error counters are cleared. A new test is started.

K...Keep data on file

This option asks for a data disk to be inserted into drive #4. It looks for a file called "CYC.DATA.text" and reads it in if it exists. If not it creates it. The current data is added to the file and the file is saved. The file can be printed with a program called DATAPAGE which simply lists the file, paging at each occurance of '####'. The data results of each "keep" takes about 18 blocks. This enables the results of many tests to be kept together on one diskette. If reading in the file becomes very slow, rename the file so that a new one will be started.

C...Continue test

The test is continued starting with the next test after the one that was interrupted. The memory test always completes unless an error was found. The disk tests always complete the Read or write function they were in.

E...Exit Cycler

The Cycler test finishes and the test menu is shown.

XI.03 ALTER :

```
-------------------------------------------------------------
Type key to set test:

 M....Memory test ..... ON      I....disk Inspection Test
 C....Clock test ...... ON      W....Write this screen
 4....DRIVE #4: ....... ON      Z....Zero test counts
 5....DRIVE #5: ....... ON      R....Return
 S....Serial ports ..... ON     E....EXIT CYCLER
 P....Parallel port .... ON
 H....Halt on error..... OFF
 #....Stop after passes  >= 250
      if hard errors are >=  20
      if soft errors are >= 200
      if data errors are >=  20
 F....Disk failed:
      if hard errors are >=   1
      if soft errors are >= 100
      if soft/cyl    are >=   5
      if data errors are >=   1
      U....Update parameter file.
      O....Output to         PRINTER:.TEXT
-------------------------------------------------------------
```

M...to H...Test controls

These selections are a "toggle" and turn the test ON or OFF. The Halt on error option stops the Parallel port test on the error condition so that the signals on the port can be probed.

#...Stop controls

Each of the values that may stop a test can be changed. Typing just a return will leave the current value alone. These values are read in from a file on the diskette called CYC.PARAM. The new values will exist only for this load of cycler. If the values are to be permanent an UPDATE (option U) must be done. An update should be done only at the request of SAGE engineers.

Changing the number of passes that the cycler makes will shorten the test. Since the failure values are set for the number of errors allowed for this number of passes, it is not a good idea to change this for the disk tests. If a long term check of memory only is desired, change the number of passes to a very high number (10000), shut all other tests OFF.

F...Disk failure parameters

These values determine if a disk has failed or not. The values given have been carefully determined for the disk vendor by SAGE and should NOT be changed unless authorized.

U...Update the parameter file.

File CYC.PARAM contains a table of information that CYCLER uses to determine when to stop a test and when a test fails. If CYC.PARAM does not exist on the disk, it will be created according to default parameters on the first load of CYCLER. Parameters for various test situations can be setup by renaming CYC.PARAM using the FILER. Run CYCLER, create new parameters in ALTER then Update. Exit and rename the new CYC.PARAM.

O...Output data to a printer or a file.

Changing the output option allows the error data to be saved in a file or transferred to a different device. If sent to a file on a floppy, one of the scratch diskettes must be removed, and the data floppy with a good directory inserted. The print options 1 or 2 from the main menu will write the data to the output device. Remember to put the scratch floppy back in or continuing the test will destroy all the data just written.

I...Disk Inspection parameters

The disk Inspection test turns off all tests except the Drive tests. The number of passes is set to 15. This is used to quickly check newly received disk drives before they are installed in a system.

W...Write this screen

This allows a printout or a file to be made of the parameters on which a test was run as CYC.PARAM cannot be printed with the Filer. (The file is a text file for viewing and cannot be used as an input parameter file. Use the UPDATE option to create a parameter file.)

Z...Zero all errors

All error counts are set to zero so that a new test can be run.

R...Return

Returns to the routine which called the ALTER program.

E...EXIT CYCLER

Testing is stopped and the Operating system command line is displayed. CAUTION: Save/print any test data needed before exiting. As CYCLER cannot be sure having either a printer or a good disk it cannot do this automatically.

XI.04 CYCLER RAM TEST :

On CYCLER startup, procedure TST_INIT is called. Memory location 100 (hex) is checked to determine how much ram the SAGE II is equipped with.

All of the RAM is tested, one 512 byte block at a time. The block test is done with a 68000 assembly code program called TST_RAM. It does this sequence of operations:

Supervisor mode is entered.
Interrupts are shut off.
Parity checking is shut off.
The original contents of the block are saved.
A pattern is written to all bytes of the block and read back.
The original contents are restored.
Interrupts are enabled.

The calling PASCAL routine RAMTEST will call the block test for all of memory. Then the test pattern will be changed for the next test.

If the test fails it will abort all other tests. The processor light will be RED. If a terminal is connected, "TYPE ESC" will be displayed. A "beep" will sound every 15 seconds.

All RAM memory is checked except for a small section of TST_RAM itself.

A RAM error may occur during other parts of the CYCLER test or during the BOOT initialization. An EXCEPTION error will be printed to the terminal. The CYCLER test will be aborted and any error information from the other tests will be lost.

XI.05 SERIAL TEST :

The connector provided in the service kit must be attached for the serial test to run. This connector has:

DTR (Data Transmit Ready)	connected to	DSR (Data Set Ready)
RTS (Request to Send)	connected to	CTS (Clear to Send)
RXD (Receive Data)	connected to	TXD (Transmit data)

This "wraps" the port so that the SAGE II is sending and receiving to itself.

All input and output is done through standard UNITREAD,UNITWRITE, and UNITSTATUS calls from the PASCAL procedure TST_SERIAL. It does these operations:

1. The current SERIAL port configuration is saved.

2. The test configuration is defined for the BIOS.

3. The channel is cleared of any leftover transmissions from a user program or from a previous failure.

4. The control line DTR is set low and DSR is checked to see that it goes low as they are tied together.

5. The control line DTR is set high and DSR is checked to see that it goes high.

6. The control line RTS is set low which should disable communications. RTS is connected to CTS, but CTS cannot be read directly with UNITSTATUS. 5 characters are transmitted and the receive buffer is checked to see that NONE of them arrive.

7. The control line RTS is set high which should enable communications. The 5 characters which were waiting in the transmit buffer are now sent and should be received.

8. The channel is cleared in case any of the previous tests failed. 255 bytes, 0-255 are send over the channel to insure that none of the data signals are interacting with one another.

9. The current configuration is restored.

If any operations fail, an error will be logged and the SERIAL test will be turned off. (The other tests will continue to run.)

At the end of the test, or when an "ESC" is typed, a serial test error will show as:

SERIAL TEST..... FAILED ***** err message XMT= x RCV= x

where the error message describes the first test that failed. XMT and RCV are the values of the byte being sent and received. Possible error messages are:

Bad buffer size — The size of the receive buffer should be 0-255. Anything else indicates a system error, possibly a bad BIOS or memory error.

DTR to DSR = low — DSR should be the same as DTR. Check U60 and U59 Check also to see that the service kit connector is mounted correctly and that the wire is not broken.

DTR to DSR = high — DSR should be the same as DTR. Check U60 and U59 Check also to see that the service kit connector is mounted correctly and that the wire is not broken.

RTS to CTS = low — With CTS disabled, no data can be received. A 5 byte transmission is set up. A timeout on receive should occur and test will continue. If this error occurs , CTS did not go low and data was received.

RST to CTS = high — CTS should be enabled, the check for receive should NOT timeout. The 5 bytes have arrived.

5 byte transfer — The 5 bytes sent when CTS was disabled are checked for their values. If they differ from what was sent, check for shorts on the RXD and TXD lines, replace the USART.

255 byte transfer — 255 bytes, values= 0-255, are sent and received. If the byte received does not match the byte sent then this error occurs, the XMT and RCV indicate the transmitted and received values.

The CD and RG connections of the port are tested in the PARALLEL test.

XI.06 PARALLEL TEST :

The connector provided in the service kit must be attached to run this test.

The PARALLEL test checks the parallel printer port and the CD (carrier detect) and RG (Ringing Detect) of the "MODEM" port. The data bits of the port connect to a 74LS157 multiplexer which will select between the odd and even bits depending on the status of PRIME. The output of the 74LS157 is to the BUSY, PAPER, SEL and FAULT input signals. An assembly code routine TST_CONT is used to change PRIME and STROBE for the test. UNITREAD, UNITWRITE, AND UNITSTATUS are used to transmit and read the data.

The parallel test does these operations:

1. The current parallel port configuration is saved.
2. The test configuration is defined for the BIOS.
3. PRIME is set low, CD is checked.
4. Bits 0,2,5 and 7 are tested through the 74LS157.
5. PRIME is set high, CD is checked.
6. Bits 1,3,4 and 6 are tested through the 74LS157.
7. STROBE is set low, RG is checked.
8. STROBE is set high, RG is checked.
9. The current configuration is restored.

If any of the tests fail, an error will be logged and the test will be turned off. At the end of the test, or when an "ESC" is typed, a parallel test error will show as:

PARALLEL TEST..... FAILED *** err message XMT= x RCV= x

where the error message describes the first test that failed. XMT and RCV are the values transmitted and received.

The error messages are:

PRIME to CD= low	PRIME is set low, CD should follow, the even bits on the data bus are selected.
B0 B2 B5 B7	All values 0-255 are sent and checked. An error here may mean two or more data lines connected together. Output lines BUSY, PAPER SEL and FAULT should also be checked.
PRIME to CD= high	PRIME is set high, CD should follow, the odd bits on the data bus are selected.
B1 B3 B4 B6	All values 0-255 are sent and checked. An error here may mean two or more data lines connected together. Output lines BUSY, PAPER SEL and FAULT should also be checked.
STROBE to RG= low	STROBE is set low, RG should follow.
STROBE to RG= high	STROBE is set high, RG should follow.

XI.07 FLOPPY DRIVE TEST :

Each floppy drive is tested according to the parameters defined for it in the BIOS. These parameters are read during startup. In this way the test can be set for different types of drives and formats with only minor changes. The scratch diskettes used for the test must be formatted to match the BIOS setup.

Drive #4 or #5 can be tested separately by using ALTER to shut off the other tests.

DRIVE FORMAT:

80 or 40	cylinders per diskette.
2	heads (tracks) per cylinder, one on each side
8	sectors/track (head)
512	bytes/sector
512	bytes/block: sectors size = block size.
1280	blocks per 80 "track" diskette.
640	blocks per 40 "track" diskette.
4096	bytes in one head of one cylinder.

Because there are really two tracks to each cylinder, the diskettes would be more properly called 80 "cylinder" and 40 "cylinder" drives but the older, single-sided nomenclature has carried over here.

The disk test does the following operations:

1. The entire diskette is written cylinder by cylinder (4096 bytes) with a code at the front of each cylinder and checked for hard and soft errors on the write.

2. The diskette is read cylinder by cylinder and checked for hard and soft errors on the read. If a hard error occurred the cylinder is not read. NUM_SCRIPT The data compared with the written data. If either a hard error or a soft error occurred this is not done.

Errors are logged and a major error will terminate the test on that drive. Testing of the other drive continues.

The test fails if a drive exceeds the failure parameters set in the parameter file CYC.PARAM. They can be changed by the ALTER option but SHOULD NOT BE CHANGED unless specified by SAGE.

At the end of the test or when an ESC is typed, the errors are added up so that the graphs and displays can be shown.

HARD I/O ERRORS:

0	No error.
-1	Floppy controller would not respond.
-2	Floppy controller returned invalid command error.
-3	Recalibrate or Seek Failure (equipment check).
-4	No diskette (as a result of read/write timeout.
-5	Missing address mark reported by floppy controller.
-6	No data Found reported by floppy controller.
-7	CRC Error reported by floppy controller.
-8	End of Cylinder reported by floppy controller.
-9	End of Cylinder reported by floppy controller.
-10	Write Protect Violation
-11	Address out of range
-12	Wrong Cylinder reported by floppy controller
-13	currently unused
-14	Illegal device number
-15	Illegal request.

SOFT ERRORS:

The BIOS interrupt driven driver returns the number of soft errors to the test program. Soft errors are tracked by the Head and cylinder that they occur on. A large number of soft errors may indicate that the drive is out of alignment or that imperfect diskettes are being used for the test. It is especially important that good media be used on the 80 track drives.

DATA ERRORS:

Data is NOT checked for cylinders that had hard or soft errors. A data error will only be shown if the data written does not match the data read and no hard or soft errors were reported.

SCRATCH DISKETTES:

It is important that the scratch diskettes be formatted on a KNOWN working system. DO NOT format the scratch diskette on the system being tested. This may reduce the number of errors found if the drive is out of alignment but will cause problems as the user will not be able to read updates from SAGE or diskettes from other systems. If alignment is wrong use the ALIGN program and an certified alignment diskette to correct the problem.

XI.08 DISK STRAP TEST :
On initialization, if CYCLER determines that there are two disk drives #4: and #5: to be tested, a quick check is made to determine if the strapping options of the floppy drives were set right. If incorrect, the system may confuse the two drives or think that there are two drives when really it is only equipped with one. The STRAP test writes 4's to drive #4: and writes 5's to drive #5:. Then it reads the drives, checking that the data coming back matches the drive number. An error shows incorrect strapping or a drive that is not working at all.

XI.09 SWITCH TEST :
The switch test reads the two groups of dip switches on the back panel and displays their position as "up" or "dwn". Each switch must be manually changed and a key typed to cause the new position to be read.

If a system will not automatically boot to the device specified, boot to the test diskette using either "IF0" or "IF1" and run this test to see that the switches work. The APPENDIX in the user manual defines the meaning of the switches. Note that GROUP B switches can be user defined if the IEEE-488 bus implementation is not needed.

XI.10 ATTACH TEST :
The attach test checks the timing hardware registers in U74 an 8253 and the bios interrupt structure for it. A .5 second timeout is setup with the Sage II ATTACH command to the first timed event. A loop in the main line of the program increments a counter. When .5 seconds is up, the ATTACHED process TIMER saves the status of the counter. The saved value of the counter should be 453 if the event was timed properly.

Problems with the clock, U71, U75, or U74 could cause the ATTACH test to fail. If it fails, the test may not continue properly and the system must be re-booted.

XI.11 REAL TIME TEST :
The system timer registers in U74 and U75 are checked using the Pascal TIME(HIGH,LOW) routine. The time is saved before the RAMTEST and checked once the RAMTEST is done. The interval actually measured is just the length of time taken to do the RAMTEST. The length of the RAMTEST will be determined by the amount of RAM in the system. Each bank (128K) of RAM takes about 114 clock ticks to test. A clock tick is 1/60th of a second. A 4 tick variance is allowed, so that the clock is tested to within +- .0664 seconds. This allowance is necessary for the refresh time.

Problems with the clock, U71, U75 or U74 can cause the TIME test to fail.

XI.12 BUILDING CYCLER :

The source diskette should have these files:

```
        CYC.68000.TEXT.....short assembly code routines
        CYC.RAM.TEXT ......assembly code ram test
        CYC.PLOT.TEXT......plots soft and hard errors
        CYC.MAIN.TEXT .....main program with menu selection
        CYC.SERIAL.TEXT....Modem serial port test
        CYC.PARALLEL.TEXT..Parallel port test
        CYC.ERRORS.TEXT....Displays errors
        CYC.PARAM..........Test parameter file

A ssemble......CYC.68000.TEXT ----> CYC.68000.CODE

A ssemble......CYC.RAM.TEXT   ----> CYC.RAM.CODE

C ompile.......CYC.PLOT.TEXT  ----> CYC.PLOT.CODE

C ompile.......CYC.MAIN.TEXT  ----> CYC.MAIN.CODE
  includes     CYC.SERIAL.TEXT
               CYC.PARALLEL.TEXT
               CYC.ERRORS.TEXT


L ink..........CYC.MAIN       ----> CYCLER.CODE
  lib files    CYC.68000
               CYC.RAM

E dit..........USERLIB.TEXT
  to include  "CYC.PLOT.CODE"

F iler
T ransfer......CYCLER.CODE    -----> service diskettes
```

The boot disk must not have RAMDISK enabled. A BIOS version newer than OCT 1, 1982 must be used.

Run SAGEUTIL to setup printer port. The number of retries for the disk drives should be 1. The "read after write" option must be turned off.

XII CLEANER PROGRAM :

CLEANER is not a test program but a process to clean the heads of a disk drive. If a drive is making many soft errors (as shown by CYCLER) but does not seem to be out of alignment or have any other problems it may just need cleaning. Run CLEANER as described and retest.

EQUIPMENT NEEDED:

CLEANER program (should be on Test diskette)
Diskette Cleaning Kit
VERBATIM #21145
Sunnyvale, Ca.

OPERATION:

The SAGE must be able to boot to the test menu. Select CLEANER.

The system will ask for the number of the drive to be cleaned. Type in "4" for the left-hand drive, "5" for the right-hand drive or "Q" to quit.

Put the solution on the cleaning diskette as recommended in the instructions. Insert into the drive. Type any key to start the test.

The program will take about 45 seconds. It should display "DONE".

DO NOT INTERRUPT THIS PROCESS WITH A CNTRL @. The disk drivers will be set up wrong for normal operation. If this happens, REBOOT!

XII.01 BUILDING CLEANER :

The source diskette should have this file:

CLEANER.TEXT.....Main program

C ompile.....CLEANER.TEXT ----> CLEANER.CODE

F iler
T ransfer.....CLEANER.CODE -----> service diskettes

XIII ALIGNMENT DIAGNOSTIC :

The ALIGN test is a diagnostic which determines if a floppy disk is properly aligned. It does NOT tell how to align a disk, since this differs slightly with each manufacturer. It help an end-user determine if the system must be sent back for calibration or help the service center validate their alignment process.

It takes about 4 minutes to run the entire 9 passes of the test with about 27 seconds for each pass.

EQUIPMENT NEEDED

506-400 (P/N 802010)
Alignment diskette -double density
16 sector/256 bytes sector

Dysan Corporation (408) 988-3472
5201 Patrick Henry Dr.
Santa Clara, CA 95050

OPERATION:

The SAGE must be able to boot to the command line. When booting from a Test diskette, select ALIGN from the test menu. The system displays:

"Remove test diskette. Insert DIAGNOSTIC diskette. DISKETTES READY?"

Put the alignment diskette into the drive. Type "Y" when ready or type "N" to go back to the test menu.

Next, the ALIGN menu is displayed:

```
DISK ALIGNMENT TEST

Select:

      4....test drive #4:   (Insert diagnostic disk first)
      5....test drive #5:   (Insert diagnostic disk first)

      D....Display results.
      P....Print results.
      R....Repeat test for  9 passes.
      O....Output data to:  A.SCRN
      W....Write this screen
      K....Keep results.
      E....EXIT
```

Type the key indicated to perform one of these functions:

4...DRIVE #4:
Testing begins on drive #4:. Make sure that the DIAGNOSTIC diskette is in this drive. When the test completes the number of passes, the results will be displayed.

5...DRIVE #5:
Testing begins on drive #5:. Make sure that the DIAGNOSTIC diskette is in this drive.When the test completes the number of passes, the results will be displayed.

D...Display results

The results of the last test are shown. If a test has not been run, the error message 'No data yet' will appear. Type any key to return to the menu. Below is an example of the results of a test of drive #4:.

```
DISK #4 ALIGNMENT: double density, 16 sectors/256 bytes

TK HD   Equal offset - ECCENTRICITY TEST
28  0   0 0  0 0  0 0  0 0  0 0  0 0  0 0  0 0
    1   0 0  0 0  0 0  0 0  0 0  0 0  0 0  0 0

TK HD   Progressive offset- ALIGNMENT TEST
 6  0   0 0  0 0  0 0  0 0  0 0  0 0  2 0  9 0
    1   0 0  0 0  0 0  0 0  0 0  0 0  0 0  8 4
10  0   0 0  0 0  0 0  0 0  0 0  1 0  3 0  9 0
    1   0 0  0 0  0 0  0 0  0 0  0 0  0 0  9 5
32  0   0 0  0 0  0 0  0 0  0 0  0 0  5 0  9 1
    1   0 0  0 0  0 0  0 0  0 0  0 0  0 0  9 9
36  0   0 0  0 0  0 0  0 0  0 0  1 0  9 0  9 0
    1   0 0  0 0  0 0  0 0  0 0  0 0  0 4  9 9
64  0   0 0  0 0  0 0  0 0  0 0  4 0  9 3  9 6
    1   0 0  0 0  0 0  0 0  0 0  2 1  4 9  9 9
74  0   0 0  1 0  0 0  0 0  1 1  0 8  9 9  9 9
    1   0 0  1 0  0 0  0 0  0 2  1 9  2 9  5 0
```

P...Print results.

The same information shown by the DISPLAY command is sent to the output file. Normally this is the printer. Using the O option to change the output file allows the information to be saved in a file.

R...Repeat test for 9 passes.

Running the test for many passes will take awhile. A quick check of a drive can be done by changing the repeat number to 1. This is normally not done unless an attempt to align the drive is being made.

O...Output data to: PRINTER:

This works with the P (print) option to allow the results of the test to be printed or written to a file. Type in the device or file name. Typing just a <cr> will restore the output option to PRINTER:.

Example:

```
Type "O"          for the output option.
     "DRV4.DATA"  for the file name
     "P"          to write the file
     "O"          to return to the output option.
     <CR>         a return restores output to PRINTER:
```

NOTE: The printer speed and type is configured using SAGEUTIL. See the SAGE owner's manual.

W...Write this screen

This writes the menu screen to the file or device set by the O (output) option. It is used to save the parameters that the test was run on.

K...Keep results.

If no test has been run the message "No data yet." will display. Type any key to restore the menu. Otherwise, the K option asks that the data diskette be inserted in drive #4:. It looks for file "A.DATA.text" and reads it if found or creates it if not. It then asks for information about the model and type of disk tested. The test results are added to the file A.DATA so that on-going records can be kept of disk problems. The program DATAPAGE can be used to print the file with one set of results per page.

E...EXIT

The program exits to the test menu.

XIII.01 TEST DESCRIPTION :
Currently, two types of test data field patterns are provided on the Digital Diagnostic Diskette. The ability of the drive to read specific patterns provides information which is used to calculate test results.

The normal format has been written on TRACK 0 both sides. This format has 16 sectors per TRACK with 256 bytes per sector. This is different from the standard SAGE format which has 8 sectors per TRACK with 512 bytes per sector. The floppy configuration is changed during the test to allow the DIAGNOSTIC format to be read and restored when the test is finished.

**** WARNING: DO NOT EXIT THIS TEST WITH CNTRL @ or the drive may be left set for the wrong format.

A data field contains bytes with binary pattern 01000000 or decimal value 64. (The data field is shown with a small "d" in the examples.)

Track 0 has a the data fields centered on the track as normal with the 16 sector/256 byte format and is ignored by the ALIGN test .

XIII.02 PATTERN 1 :

The ID information is written on track. Data fields (shown as "d") are written alternately displaced an equal amount on either side of track centerline. A read failure will indicate "eccentricity" where the drive failed to stay in the center of the track.

PATTERN 1

millinches:

```
      6 5 4 3 2 1 0 1 2 3 4 5 6
      + + + + + + + + + + + + +
      |_|_|_|_|_|_|_|_|_|_|_|_|
```

sector			offset
1		d	+3.0
2	d		3.0
3		d	+3.0
4	d		-3.0
5		d	+3.0
6	d		-3.0
7		d	+3.0
8	d		-3.0
9		d	+3.0
10	d		-3.0
11		d	+3.0
12	d		-3.0
13		d	+3.0
14	d		-3.0
15		d	+3.0
16	d		-3.0

XIII.03 PATTERN 2 :

Tracks 6,10,32,36,64 and 74 are written with PATTERN 2.

The track and sector ID information are written with track and sector ID fields centered on the track as normal. The data fields, however, are written with a radial displacement away from the centerline. Each sector's data is written a greater distance away as shown below. A positive value indicates an offset toward the spindle (center of the disk) and a negative value indicates an offset away from the spindle.

PATTERN 2
millinches:

sector	6	5	4	3	2	1	0	1	2	3	4	5	6	offset
1							d							0
2							d							0
3							|		d					+2.5
4				d			|							-2.5
5							|		d					+3.0
6			d				|							-3.0
7							|		d					+3.5
8		d					|							-3.5
9							|		d					+4.0
10		d					|							-4.0
11							|		d					+4.5
12		d					|							-4.5
13							|		d					+5.0
14	d						|							-5.0
15							|		d					+5.5
16	d						|							-5.5

The data has been written progressively away from the track centerline.

As the sectors are read, the drive WILL fail to read some sectors properly. (Even good drives cannot read 15 and 16 consistently). If the drive is aligned, the first two sectors that it FAILS to read should have data that is equally offset from the centerline. For example, BOTH sectors 15 and 16 should fail is the drive is aligned as they are both offset by 5.5 milli-inches. However, the drive is out of alignment if Sector 14 passes but 13 failed. (or 13 failed and 14 passed).

XIII.04 PATTERN 3 :
Resevered for third ALIGNMENT PATTERN.

XIII.05 BUILDING ALIGN :

The source diskette should have these files:

```
        A.MAIN.TEXT........main program
        A.DISK.TEXT........disk tests

C ompile.......A.MAIN.TEXT     ----> ALIGN.CODE
  includes      A.DISK.TEXT

F iler
T ransfer......ALIGN.CODE    -----> service diskettes
```

XIV REPLACING THE FLOPPY DISK DRIVE :

1. Disconnect the power cord

2. Remove all but the two bottom screws around the vent holes on the back panel.

3. Disconnect all cables connected to the computer board.

4. Remove the fasteners retaining the circuit board to the chassis.

5. Gently bend the back panel outward so that the circuit board may be moved back sufficiently that the LED on the front will clear the front panel and the front of the board tilted up. After the front of the board clears the top of the front panel the board may be slid forward to remove the connectors from the back panel. The board may then be removed from the chassis. The board whether in or out of the chassis must only be handled with anti-static procedures.

6. Remove the screws which attach the disk drive shield to the chassis, be sure not to forget the ones on the sides and bottom of the chassis.

7. Remove the disk drive shield.

8. Disconnect the cables from the drive(s) to be removed.

9. Remove the two screws which secure the drives to their mounting suspension through the clearance holes in the bottom of the chassis.

10. Carefully slide the drive out through the front of the computer.

11. Install the new drive in the reverse order.

XV SUBSYSTEM MODIFICATIONS :

SAGE has made the following modifications in-house. These changes are fully supported by SAGE.

MICROPOLIS DISK MODS

Install a jumper at position W22 on the disk drive circuit board.

MICROPOLIS DISK SETUP

For left hand drive install one shorting block at position W1 of connector J2.

For right hand drive install one shorting block at position W2 of connector J2.

There shall be only one SIP termination resistor pack (location RN1) per computer and it shall be installed in the right hand drive.

MITSUBISHI DISK MODS

None.

MITSUBISHI DISK SETUP

The seven resistor pullup straps should be removed on a drive which is closest to the cpu in a two drive system The head load jumper should be in the "HM" position. The drive should be selected for the appropriate position.

TANDON DISK MODS

A jumper wire is connected between pin 2 of J4 and TP13. Resistor (R49) has the end towards the strapping block moved to the adjacent pad (R50).

TANDON DISK SETUP

The strapping block determines the drive device number. Normally the left hand drive is device 4, the right hand drive is device 5. For the left hand drive count from the edge closest to the edge of the circuit board. Remove all but the first two straps.

For the right hand drive remove all but the first and third straps.

There shall be only one dip terminating resistor pack (2F) per computer and it shall installed in the right hand drive.

TEAC DISK MODS	None.
TEAC DISK SETUP	The resistor pack shall be removed from one drive in a two drive system. The head load jumper shall be placed in the "HM" position The drive select shall be jumpered for the appropriate position
POWER MOD FOR 220V	Remove jumper W101 for 220V, leave in for 110V.

XVI CABLE WIRING NOTES :

TERMINAL CABLE, TELEVIDIO 925, #CC0000, CC0001, & CC0002

```
SAGE II                    TERMINAL
  1 ------BROWN---------> 1
  2 ------BLACK---------> 2
  3 ------RED-----------> 3
  7 ------GREEN---------> 7
```

The sage part # shall be marked on both ends of the cable
SAGE TERMINAL shall be marked on the SAGE II end.
TERMINAL shall be marked on the terminal end.
Dummy pins shall be inserted in positions 1, 13, 14, 25 if these positions are unused.

TERMINAL CABLE, MULTIUSER, TELEVIDEO 925

```
SAGE II                    TERMINAL
  1 ------BROWN---------> 1
  2 ------BLACK---------> 3
  3 ------RED-----------> 2
  5-->6-->9
  7 ------GREEN---------> 7
```

The sage part # shall be marked on both ends of the cable
"SAGE MODEM" shall be marked on the SAGE II end.
"TERMINAL" shall be marked on the terminal end.
Dummy pins shall be inserted in positions 1, 13, 14, and 25.

INTEX TALKER CABLE

```
SAGE II                    INTEX TALKER
  1 ------BROWN---------> 1
  2 ------BLACK---------> 2
  3 ------RED-----------> 3
  5-->9
  6 ------WHITE---------> 4
  7 ------GREEN---------> 7
```

The sage part # shall be marked on both ends of the cable.
"SAGE MODEM" shall be marked on the SAGE II end.
"INTEX TALKER" shall be marked on the voice synthesizer end.
Dummy pins shall be inserted in positions 1, 13, 14, and 25.

PRINTER CABLE, TI, SERIAL, #CC0003 & CC0004

```
SAGE II                    PRINTER
  1 ------BROWN---------> 1
  2 ------BLACK---------> 3
  3 ------RED-----------> 2
  5-->9
                             6-->8-->9
  6 ------WHITE---------> 11
  7 ------GREEN---------> 7
```

The sage part # shall be marked on both ends of the cable
SAGE MODEM shall be marked on the SAGE II end.
TI PRINTER shall be marked on the printer end.
Dummy pins shall be inserted in positions 1, 13, 14, 25 if these positions are unused.

PRINTER CABLE, QUME, SERIAL

```
SAGE II                    PRINTER
  1 ------BROWN---------> 1
  2 ------BLACK---------> 3
  3 ------RED-----------> 2
  5-->9
  6 ------WHITE---------> 20
  7 ------GREEN---------> 7
```

The sage part # shall be marked on both ends of the cable.
SAGE MODEM shall be marked on the SAGE II end.
QUME PRINTER shall be marked on the printer end.
Dummy pins shall be inserted in positions 1, 13, 14, 25 if these positions are unused.

CABLE, PRINTER, DIABLO #630, SERIAL

```
SAGE II                    PRINTER
  2 ------BLACK---------> 3
  3 ------RED-----------> 2
  4 ------BROWN---------> 5-->6-->8
  5-->9
  6 ------WHITE---------> 11
  7 ------GREEN---------> 7
```

The sage part # shall be marked on both ends of the cable.
SAGE MODEM shall be marked on the SAGE II end.
DIABLO #630 PRINTER shall be marked on the printer end.
Dummy pins shall be inserted in positions 1, 13, 14, 25 if these positions are unused.

PARALLEL PRINTER CABLE, (# CC0005 6 ft. cable)

The parallel printer cable consists of :

A) #CN0012 36 pin Centronics connector AMP pn# 552931-1
B) #CN0000 34 pin Female header connector AMP pn# 499571-9
C) #CA0000 34 conductor ribbon cabe AMP pn# 499116-8

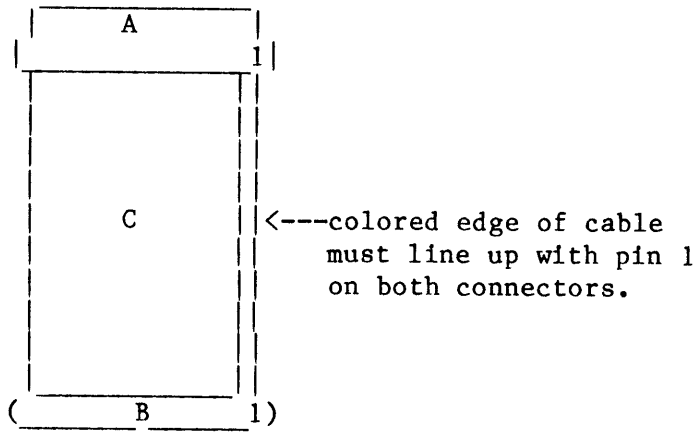
The ribbon cable has one edge colored differently to show the position of pin 1.

Pins 1-34 of Connector B must go to pins 1-34 of the cable and to pins 1-34 of Connector A. The last two pins of Connector A are unused.

The polarizing tabs of connector B must face the ribbon cable.

Trim the cable so that the edges are even and straight across.

Arrange the three parts in front of you as shown below with the connectors standing straight up from the cable. The main body of the connectors should be above the cable.



Line up the crimping pins of each connector with the wires in the cable and press fit to the cable.

Use an ohmmeter to verify good connectors on all 34 pins.

XVII CPU BOARD CIRCUIT DESCRIPTIONS :

This section is a description of the circuits on the SAGE II board. References to components on the circuit board are given as "U" followed by a number. A description of the signal names used is given at the end of this section.

XVII.01 PAGE 1 OF SCHEMATIC :

MC68000 PROCESSOR

U68 is the MC68000 microprocessor which is the heart of the SAGE II microcomputer. Refer to the Motorola MC68000 User's Manual for a detailed description of this processor.

23 address lines are brought out of the processor and buffered by U16, 26, and 35. These are 74LS240 inverted tri-state line driver/receivers. They are hard selected as drivers only. The output side which connects to J1 and other parts of the system is never in the high impedance state.

The 16 data lines are buffered through U55 and U43 which are 74LS245 bi-directional noninverted tri-state bus tranceivers. The high impedance output state is not used. The direction of U55 is switched by BRW+ and data is transferred to the processor when BRW+ is low and from the processor to J2 and the rest of the system when low. The direction of U43 is controlled by RW-. Data transfer is from the processor when low.

The system clock, 8 Mhz-, and control bus signals SRES+, RW-, LDS+, UDS+, and AS+ are buffered by U44. This Schottky tri-state buffer 74S240 is used as a bus driver without the tri-state mode.

SAGE BUS

The Sage interface bus is comprised of connectors J1 and J2. J1 includes the address lines inverted and buffered, FC2- the user/supervisor bit, and PRTY- which is the RAM parity exception interrupt line. The odd numbered pins of J1 are all connected to ground for signal isolation. J2 includes buffered and unbuffered signals. The buffered lines include the data lines, system clock 8 Mhz-, system reset SRES+, read/write RW-, lower data strobe LDS+, upper data strobe UDS+, and address strobe AS+. The unbuffered lines are the two external interrupt inputs I2- and I3-, and data transfer acknowledge DTACK-. The odd numbered pins 1 through 33 of J2 are connected to ground. Pins 35, 37, 39, 41, 43, and 45 are connected to +5 volts. Pin 47 is +12 volts and pin 49 is -12 volts.

PROCESSOR LIGHT EMMITING DIODE INDICATOR

The processor LED driver circuit is comprised of R1 and 2, C1, and three gates of U65, a 7406 Hex inverter buffer with open collector outputs. The LED is on whenever the computer is powered. The buffer, U65 pins 11 and 10, drives the green direction of the LED with pin 10 low whenever pins 6 and 8 are both inactive and pulled high by R1. When pin 6 or pin 8 are active, pin 11 is low and pin 10 is pulled high by R2. When this side of the LED is high the red diode is on and when the side toward R1 is high the green diode is on. C1 provides integration on the red side such that when the circuit is being driven by AS- from an active processor the LED will appear green. Pin 5 of U65 is LEDR+ which originates at U39-17 on page 6 of schematics. This signal can be controlled by software to set or toggle the LED to green. If LEDR+ is inactive then the LED will be green only when the processor is busy executing instructions.

INTERRUPT DECODER

Integrated circuit U36 is a 74LS148 and is the interrupt priority level decoder. The outputs are pins 6, 7, and 9. IPL0-, IPL1-, and IPL2- are the active low interrupt inputs to the processor and when any of these lines go low the interrupting device whose "priority address" appears on these lines will be serviced.

PROCESSING STATES

The processor outputs at pin 26 FC2, pin 27 FC1, and pin 28 FC0 are the code for the processing state reference classification. See the Motorola MC68000 Users Manual section 5 for a detailed explanation of the function of these pins. U27 looks at these lines in this system to generate VPA- valid peripheral address.

The 74LS04 buffer U1 pins 3 and 4 along with 74LS12 U52 pins 1, 2, 12, and 13 generate a bus error if system I/O is trespassed by user and the supervisor bit is not set.

RESET

The reset circuit is located at the lower right corner of page 1 of the schematics. When the reset switch is closed, pin 1 of U4 is held low. pin 2 is high and thus U1-2, U65-4, and U65-2 are all low. In this condition HALT- and RESET- are both active at the processor and the transparent boot flipflop U51-1 is cleared. When the switch is released the 68 uf capacitor at U4-1 begins to charge. At some positive voltage U4, which is a 74LS14 Schmitt trigger, will toggle. RESET- and HALT- both go inactive and the processor begins execution at address location 0.

The transparent boot circuit consists of U51 pins 1-6 and U45 pins 8-10. During reset a low at U51-1 clears U51 which is a 74LS74 D-type positive

edge triggered flip-flop. After reset the Q of the flip-flop U51-5 which is BRD- is low and the output of the 74LS00 U45-8 is high. The output of the inverting buffer U72-8 is low and thus the read only memory chips U17 and U18 are enabled. BRD- also goes to pin 1 of U14 on page 3 and disables the RAM. The effect of this circuit is to make the ROM appear to be located at address 0, which is normally the beginning of the RAM address. On the first occurrence of an address to the normal ROM location ROM- will go low and the transparent boot flip-flop will be preset Q=high. With BRD- high, ROM- selects the ROM's in the normal mode and the RAM + circuit of page 3 is enabled so that RAM is again addressable.

READ / WRITE

The data transfer acknowledge signal (DTACK-) is necessary for the completion of any read or write cycle by the processor. Normally, DTACK- is generated whenever any address in the Sage II memory map is decoded.

The DTACK- generation circuit consists mainly of U54, an 8 bit parallel out serial shift register, and the NAND gates U52 and U53. CPU boards CB0002 and later also include U76. This circuit is found in the upper right quadrant of schematic page 1. The function of this circuit is to tell the processor that the data lines have had enough time to settle after a peripheral device has been addressed, and that the read or write cycle can be completed. This is accomplished by taking the logical AND of the decoded select line for a device or group of devices and a time delay signal which is appropriate to the access speed of the device.

When upper data strobe (UDS-) and lower data strobe (LDS-) are inactive (high), then the output of U45-11 which is a 74LS00 NAND gate is low . All of the Q outputs of the 74LS164 shift register U54 are held low by clear at pin 9. When UDS- or LDS- go active low the clear at pin 9 of U54 goes high and the shift register is enabled. Provided that the refresh signal RF- is inactive high the shift register will be clocked by D8Mhz-. This is 8 Mhz- delayed through two 74LS04 inverting buffers U37. The QA output U54-3 is the first to go high. This output generates DTACK- at U52-8 when RAM+ is active high at pin 10 and bus error BE- is inactive high at pin 9. DTACK- generated from QA allows the processor to complete a cycle with no wait states. The QA output is also used in conjunction with the buffered read / write lines BRW- and BRW+ to generate WR- and RD- signals at the two 74LS00 NAND gates U45 pins 1 through 6. Output QB of the shift register and I/O+ are combined at NAND gate U53 pins 1,2,and 3 to produce DTACK- when input / output devices are addressed with cycle completion after 1 wait state. DTACK- is generated at U53-6 from QD with 3 wait states when ROM locations are addressed causing U45-8 to be high. The QC output at pin 5 of U54 would produce a DTACK- for a 2 wait state cycle.

The Sage II does not currently use 2 wait states but CPU boards CB0002 and later were laid out to facilitate a mod so that slower peripheral devices may be used.

If the serial input to the serial shift register U54 pin 2 is low due to RF- active, then DTACK will not be generated. This prevents the processor completing a cycle during refresh of the RAM and thus loading incorrect data.

Whenever a location is addressed which is not decoded in the Sage II memory map, DTACK- is not generated. This causes a bus timeout error which allows an orderly recovery from the addressing of nonexistent locations.

OPERATION OF BUS ERROR TIME OUT CIRCUIT

The watch dog timeout circuit is implemented in U67, a 74LS390 dual decade counter which is wired for BCD count sequence. QD goes high on the 8th count.

Address strobe (AS-) is applied to U67-pin 2 causing the counter to be cleared whenever AS- is inactive (high). A bus time out error is caused when AS- stays low for longer than 16 usec. This is caused by either a software or hardware condition which prevents DTACK- from being applied within ~ 16 usec.

When AS- becomes active (goes low) the counter is enabled and is clocked at pin 1 by the 500 KHZ signal from U70-12 of page 2. If DTACK- is not received within ~ 16 usec causing AS- to go high and reset the counter, then the QD output at pin 7 goes high on the eighth count and in turn causes BERR- to be generated by U65 at pin 12. The 7406 inverting buffer used at U65 is open collector output as is U52 of the user/supervisor violation circuit which was described earlier. Bus error exception processing can thus be initiated only by the watch dog timer or by user trespassing the system I/O. If a second bus error occurs while the first is being processed then the processor will halt assuming a hardware failure.

READ ONLY MEMORY

The read only memory sockets U17 and 18 have been wired with strap option pads on the printed circuit board so that they may be configured for a variety of ROM, PROM, EPROM, or EAROM in sizes from 16K bit to 256K bit. The straps P,Q,R,S,T,U,W,X, and Y are documented in the Sage II manual.

XVII.02 PAGE 2 OF SCHEMATIC DIAGRAMS :

Page 2 contains system clock generation, baud rate generation, an intelligent interrupt controller, an I/O port for the floppy drive controller and the DIP switches, address decoding, and buffers.

SYSTEM CLOCK

U66 is an integrated crystal oscillator circuit. The 16 Mhz output at U66-8 is divided by U69, a 74LS390 dual decade counter, to produce the 8 MHZ+ system clock at U69 pin 3. The output at U69-13 is the 4 Mhz+ clock. Two sections of U69 and one of U67 divide 8 Mhz+ to produce 64 KHZ+ at U67-9. The 4 MHZ+ is used by the IEEE 488 I/O port on page 6 and is the input at pin 2 to U70 a 74LS161. U70 is a synchronous 4 bit binary counter. The output QA at pin 14 is 2 MHZ which clocks the serial ports of page 6. 500 KHZ is output at QC pin 12 and this clock is used by the bus error timeout circuit and to generate WCK+ at the RIPPLE CARRY OUTPUT pin 15. MFM+ is received at pin 6 from the floppy disk circuit page 5. The RIPPLE CARRY OUTPUT is inverted by U72 74LS00 and input at pin 9 to LOAD the counter from pins 3,4,5,and 6 to begin the next count cycle. MFM+ at pin 6 determines whether the clock WCK+ is at a 250 Khz or 500 khz rate. Refer to the floppy disk circuit description for more detail of operation. U71 is also a 4 bit synchronous binary counter which can be preset, and is used in a similar configuration to U70. The parallel input pins 3,4,5,and 6 preset the count to start the cycle over again when the inverted RIPPLE CARRY OUT is applied to LOAD. The output QD at pin 11 is 615.38 KHZ .

ADDRESS DECODING

Address decoding for the ROM and I/O locations are accomplished by three 3-input NOR gates, three inverters, and two 4-input NAND gates. U25 is a 74LS27, U33 a 74LS04, and U24 a 74LS20. These gates decode A14- through A23- to generate the active low signal at U24-8 which is ROM-, and at U24-6 active low signal I/O- is decoded and becomes active high I/O+ at inverter U33-8. The individual chip select signals are generated by decoding address lines A4- through A13- and FC2+, which is a reference class function code output (user/supervisor) from the processor, and then gating with the I/O active low signal which is decoded from A14- through A23-. This is accomplished by U14 a 74LS21 4-input AND, U27 a 74LS20 4-input NAND, U19 a 74LS138 3 to 8 line decoder, and U47 a 74LS139 2 to 4 line decoder. This circuit completely decodes A4- through A23- so that the read only memory or input / output devices are never accessed by imaging.

ADDRESS BUFFERS

Address lines A1-, A2-, and A3- are buffered again by U1 a 74LS04 with outputs BA1+ at pin 12, BA2+ at pin 10, and BA3+ at pin 8. These signals go to the counters U75 and U74 and to I/O ports on this page and page 6.

I/O ADDRESSING

All of the I/O port device chip selects are generated at U19 and 47.

Two open collector NAND gates of U53 were added to CPU boards CB0002 and later to allow a mod to free up unused I/O address space.

The following table lists the I/O signals and their function.

SELECT:	OUTPUT:	INPUT:	DESCRIPTION:	SCHEMATIC
S1-	Y0 U19-15	U57-11	RS232 serial port	p.6
S2-	Y1 U19-14	U58-11	MODEM serial port	p.6
FD-	Y2 U19-13	U21-4	Floppy disk controller	p.5
HP-	Y3 U19-12	U6-3	IEEE 488 port	p.6
CN-	Y4 U19-11	U39-6	Parallel printer port	p.6
DS-	Y5 U19-10	U22-6	parallel port/floppy	p.2
IN-	Y6 U19-9	U73-1	Interrupt controller	p.2
BT-	Y7 U19-7	U75-21	Timer-baud rate	p.2
TM-	Y0 U47-12	U74-21	Timer	p.2

I/O BUS

The lower data lines are connected to the I/O devices through U56 a 74LS245 noninverted tri-state octal bus transceiver. The lines at the processor side are D0+ through D7+. The signals on the I/O data bus side are labeled BD0+ through BD7+. The I/O signal from the address decoder circuit enables the bus by going active low at pin 19. The direction of the I/O bus is determined by BRW+ which is applied to pin 1. BRW+ is from page 1 U37-2.

I/O PORT

U22 is a programmable peripheral interface integrated circuit type 8255A-5. This port has 24 I/O lines in three groups. Group A is used to read the DIP switches at J7 which are labeled group A on the back of the Sage II. Group B reads the switches at J6 labeled group B. Group C is utilized to send control signals to the floppy controller on page 5. Group A and B are programmable as a 16 bit bi-directional parallel port. In this configuration they are used as input only and group C for output only.

INTERRUPT CONTROLLER

The intelligent interrupt controller U73 is an 8259-5. When one or more of it's interrupt inputs, IR0-IR7, go active high it sends an interrupt to the processors interrupt encoder on page 1. This signal is called ICI- after it is inverted by the 74LS04 buffer U72 pins 5 and 6. The processor may access this device to determine the source of the interrupt or to program the priority mask.

TIMERS

Two 8253-5 programmable interval timers U75 and U74 are utilized in the Sage II. U75 generates the two baud rates for the USARTS. These signals are BR1+ and BR2+ and are used at the serial ports on page 6. Each device contains 3 independent 16-bit counters. Two of these counters are used to produce the baud rates. The use of the remaining counters is dependant on appropriate software. Typical uses are event scheduler and real time clock. Sections IV.4.6 and IV.4.7 of the SAGE II Owners' Manual describe the software available to access these timers.

XVII.03 PAGE 3 OF SCHEMATIC DIAGRAMS :

This section contains the RAM parity interrupt signal generation, RAM refresh and refresh arbitration, and RAM control circuitry.

PARITY INTERRUPT

The circuit in the upper left corner of this page is the parity error interrupt generation circuit. The parity reset signal PRES- comes from U39 pin 14 on page 6. PRES- goes low during initialization, is inverted at 74LS04 U37 pins 9 and 8, and appears high at the preset input pin 10 of the parity latch U51 which is a 74LS74 D-type positive edge triggered flip flop. This makes the Q output of U51 inactive high which is the normal state and inputs a high to 74LS00 U50 pin 12. In this normal state the NAND gate U50 pins 11-13 looks like an inverter between pins 13 and 11. The input at U50 pin 13 is RAM+ which goes low after a RAM access and thus causes a positive edge clock to U51 at pin 11. The inputs at U50 pins 4 and 5 originate at the ram circuit page 4. Parity flag low PFL- and parity flag high PFH- are both active low. The low and high refer to upper and lower bytes of RAM.

If either of these signals are active low then pin 6 of U50 goes high. If the buffered read / write signal BRW+ from page 1 is high indicating a read cycle then the output of U50 at pin 8 will go low. At the end of the cycle when RAM+ goes low the low at U51-12 gets clocked through to U51-9 and also appears at pin 4 of noninverting buffer U48 as active low PRTY-. This also places a low at U50 pin 12 and does not allow the flip flop U51 to be clocked again until it is preset by PRES- effectively latching the PRTY-. PRTY- goes to U36-4 on page 1 which is the interrupt decoder.

MEMORY BANK SELECTION

Memory bank selection is accomplished by decoding address lines A17, & A18 with one half of a 74LS139 (U47). The decoded outputs are gated to the RAS lines of the appropriate memory banks with 1/2 of an 74LS241 (U46) during the active time of RAM+. The other half is used to gate the RAS signal to the memories during refresh cycles.

MEMORY REFRESH CONTENTION ARBITRATION

Refresh cycles are initiated every 15.625 usec from the 64 Khz refresh clock. The refresh request is latched into the first section of the D flip flop (U34). The next falling edge of AS+ (gated with the 8 Mhz clock) clocks the refresh request into the refresh grant flip flop (U34-2) initiating a memory refresh. The output from the refresh grant flip flop (pins 5 & 6 of U34) goes to three places.

First it disables RAM+ generation with a low on pin 11 of U15.

Second it generates a high on the output (pin 6) of U41 which increments the refresh counter, generates a low on the output (pin 4) of U33 which enables the refresh address to the ROW address lines through U12 while simultaneously disabling both U10, & U11 from placing any addresses on the ROW address lines. This is a 260ns pulse generated when RF+ goes high setting the output (pin 6) of U41 (AND) high until the low signal propagates through the delay line (260ns) setting the output back low.

Third a 190 nsec pulse with a delay of 70 nsec from RF is generated with the 70 nsec, & 260ns tap on the delay line, one section of U33 (pins 1 to 2) and one section of U32 (pins 1, 2, & 3) which is the actual RAS signals to the rams for refresh. The Refresh RAS is always enabled to the RAS lines of the RAMS whenever RAM+ is low.

MEMORY ADDRESS SEQUENCE

All memory address cycles start with the rising edge of AS+. At this point the address bus has had a valid address for about 30 nsec. 4 main events start on the rising of AS+. First the appropriate read or write data buffers to the rams are enabled through pins 3 of U41, or 11 of U32. Second the signal for the eventual CAS is started through the 60 nsec delay line. Third the RAS buffer (U46) is switched from the refresh mode to the data mode sending a RAS- to the selected bank of memory. Fourth the low byte address buffer is disabled (U10) immediately followed by the high byte address buffer being enabled (U11) onto the Address lines of the RAM'S to wait for the eventual CAS signal when it gets through the delay line. The falling edge of AS+ clocks any parity error generated during the memory cycle to the parity interrupt.

RAM CONTROL SIGNALS

The write enable signals are produced by U41, U40 and RN3. LDS+ from U44-16 of page 1 and BRW- from 37-4 also on page 1 are combined at U41 a 74LS08 AND gate. The output of U41-11 is input at U40 pins 2 and 4 and produces the independently buffered low byte write enable signals LW0 and LW1. Similarly, the upper byte write enable signals UW0 and UW1 are produced at U41-8 by UDS+ upper data strobe from U44-18 page 1 which is logical AND'd with BRW- buffered read / write.

The RAM data bus control signals RRD+ and RWR- are generated from RAM+ and the buffered read / write lines. BRW+ from U37-2 page 1 is combined with RAM+ at pins 1 and 2 of U41 74LS08 AND gate making RRD+ at pin 3 active high for a read cycle. BRW- at U32-12 AND RAM+ at U32-13 make RWR- active low for a write cycle at pin 11 of U32 74LS00 NAND gate.

All of the signals on the right side of schematic page 3 except BE- and RAM+ are RAM control signals and go to page 4. BE- goes to U52-9 page 1 and RAM+ goes to U52-9 page 1.

BUS ERROR GENERATION FOR NONEXISTANT MEMORY LOCATIONS

Whenever a memory location is addressed which is not a decoded address in the SAGE memory map there is no DTACK- generated which causes a bus timeout error as described above. This allows an orderly recovery from the addressing of any nonexistent memory locations. A DTACK- is generated for all locations in the SAGE II memory map.

If the system had only 128K and a location between 128K & 512K were addressed, there would be no indication. To solve this problem the bank enables for banks 0, 1, 2, & 3 are fed through an noninverting open collector buffer (U48) to the bus error input of the processor through a dip shunt. With the proper connections in the dip shunt the addressing of any location in banks 1, 2, or 3 can cause a bus error indicating an invalid memory address.

XVII.04 PAGE 4 OF SCHEMATIC DIAGRAMS :

This section contains the RAM, the RAM bus transceivers, and the RAM parity circuit.

RAM ADDRESS LOCATION

The arrangement of the RAM schematic is mapped to match the actual parts placement on the printed circuit board, and thus it can be used to determine the physical location of a particular bit or address group. Refer to the parts location drawing for the following discussion. The row of IC's across the top of the page have RAS0 connected to pin 4 and are designated as ROW0 on the board. The second row down is ROW1 and the third row is ROW2 and the bottom row is ROW3. The ROW designations are sometimes referred to as BANKS of memory, ie. BANK0, BANK1, etc. The left side of the schematic has the low byte RAM IC's and the right side has the upper byte. The lowest order bits and the lowest order nibbles are toward the left. The two columns of parity IC's are down the middle. The bit columns are numbered across the top of the parts location drawing.

ADDRESS LOCATIONS BY ROW IN HEX

Row 0	from 00000	to 1FFFF
Row 1	from 20000	to 3FFFF
Row 2	from 40000	to 5FFFF
Row 3	from 60000	to 7FFFF

RAM CONTROL SIGNALS

The multiplexed address lines RA0- to RA7- are bussed to every integrated circuit in the array. The four column address strobe signals CAS0- through CAS3- are bussed to nibble wide groups of columns and the second and third nibbles include the parity columns. The lower byte write enable lines LW0 and LW1 are bussed similarly to the CAS as are the upper byte write enable lines UW0 and UW1.

The four 8T28 bus drivers U63, U62, U30, and U23 interface the RAM data bus to the system data bus. Anti-ringing resistors are used in the input lines. The RWR- signal is not used in this configuration so that the RAM data bus is always enabled toward the RAM. RRD- enables the bus for a read cycle.

PARITY CIRCUIT

Two 9-bit odd/even parity generators/checkers 74LS280 U64 and U31 are employed. BRW+ enables the output of the parity RAMs at the NAND gates U50 and U32 during a read cycle so that the contents can be combined with the data bus for parity check. If the parity is even then pin 5 of U64 and U32 will both be high and no parity interrupt will occur. If either PFL- or PFH- go low indicating odd parity the interrupt circuit on page 3 will latch.

During a write cycle the OD outputs U64-6 and U31-6 store a 1 if the data is odd and a 0 if even. The I inputs are low during a write. The bit stored is the inverse of that necessary to produce even parity when it is added into the parity check , however, the 74LS00 gates invert it back so that parity will be even when read back if there are no memory errors.

XVII.05 PAGE 5 OF SCHEMATIC DIAGRAMS :
FLOPPY DISK CONTROLLER

The floppy disk controller section uses an NEC 765 controller chip to take care of all the low level interface to the floppy disk. The chip is used in the interrupt driven mode with the processor responding to an asynchronous interrupt from the 765 for every byte transferred.

An FDC9216 digital data separator chip is used for the data separator. There are two disk drive selects provided from an I/O port. Single/Double density select is provided form another I/O port bit. Write precomp is enabled/disabled from another I/O port bit. The amount of write precomp is determined by the 765 as normal, early, or late in increments if 125 nsec. PS0, & PS1 from the 765 determine the select of multiplexer U29, which taps off the appropriate delay from the serial in parallel out shift register U20 to determine the amount of write precomp.

The signal FDIE+ is a software controlled bit from an I/O port which is used to enable or disable the interrupts generated from the 765. The RDY+ line which would normally come from an 8" disk drive has been connected to another I/O port bit so that the ready condition may be controlled under software.

The TC+ line which would normally come from a DMA controller to signify the end of a DMA transfer now also is generated from a bit from an I/O port so the transfers may be terminated under direct software commands.

WCK+ GENERATION

The 765 requires a write clock of 500 Khz for double density and 250 Khz for single density. Both clocks require a pulse width of 250 nsec. The presettable counter U70 page 2 is clocked with a 4 Mhz input which generates a ripple carry of duration of one input clock period (250 nsec). This ripple carry is used to preset the counter to either 0 or 8 depending on how the MFM+ bit is set on the input to D3 of the preset of the counter. The counter then counts up to 15 from either 0, or 8 causing the 4 Mhz input clock to be divided by either 8 or 16 generating either

500 Khz or 250 Khz clocks with the required pulse width of 250 nsec.

XVII.06 PAGE 6 OF SCHEMATIC DIAGRAMS :

This section is titled Communications Circuit and includes the four main input /output ports of the Sage II system. The other I/O devices in the system are used internally as software / hardware interface to generate control signals. However, the port for the dip switches could conceivably be used as a 16-bit parallel port. The ports in this section are the RS232, the serial printer, the parallel printer, and the IEEE 488 or HPIB.

RS 232 PORT

The serial terminal port is implemented using an 8251A programmable communication interface U57. The Receiver Ready RxRDY signal at pin 14 is inverted by 74LS04 buffer U37-5 to 6 producing RX1I, an interrupt signal which goes to U36-2 on page 1. Pin 15 of U57 is TX1I which is also an interrupt signal and goes to the intelligent interrupt controller U73-20 on page 2. The buffered data lines BD0 through BD7 are connected to U56 at the lower left corner on page 2. The read / write signals RD- and WR- are from page 1. The chip select pin 11 of U57 originates at U19 pin 15 on page 2. Concluding the system signals is SRES+ from U44-9 page 1, 2 MHz+ from page 2 U70-14, and BR1 from U75-1.

The port is connected to J10 through buffer gates U60 and U61. The transmit buffer U60 is an MC1488 or 75188 and is powered by positive and negative 12 volts to level shift the output for proper RS232 levels. U61 is an MC1489 or 75189.

MODEM OR SERIAL PRINTER PORT

J9 is the second serial port and is also implemented using an 8251A U58. Three gates of U60 are used as output for positive and negative signal levels as in the RS232 port. U59 and U61 are MC1488 packages. U53 a 74LS38 NAND is used to negative logic OR inputs CD- and RG-, the output of which clocks the Ring / carrier interrupt flipflop U38.

The signals on the system side of the port are the same as those for the other serial port with a few exceptions. The baud rate clock is BR2+ from U75 pin 17. TX2I+ is connected to U73-21 and RX2I to U73-19 on page 2 which is the interrupt controller. Also connected to U73 is the Ring / carrier interrupt signal MI+. The reset signal RMI- is from U39 of this page. The chip select pin 11 is from U19-14 on page 2.

PARALLEL PRINTER PORT

In the center of page 6 is U39 which is used as a printer port and to interface some hardware control signals to the software. U39 is an 8255A-5 programmable peripheral interface integrated circuit. U38 is the other half of 74LS74 flip flop used as an interrupt latch at the MODEM port and serves a similar function here. CNI+ goes to the intelligent interrupt controller U73-23 on page 2. Other connections to page 2 are the buffered address lines at pins 8 and 9, the chip select CN- from U19-11, and the buffered data lines (I/O data bus) from U56. SRES+, RD- and WR- are all from page 1.

The I/O control signals at U39 include the following. The outputs are PRES- to U37-9, SC+ to U8-1 this page, SI+ to U73-25 page 2, LEDR+ to page 1 U65-5, and RMI- to U38-13 this page. The input signals include FDI+ from U21-18 page 5, WP+ from U4-10 on page 5, RG- from U61-8 this page, and CD- from U59-11 also of this page.

IEEE 488

This is a standard port often referred to as the HPIB, GPIB, or IEEE 488. Implementation here comprises U6, 7, 8, and one gate of U3. U6 is a TMS9914 GPIB adapter. For more information on this device refer to the TMS9914 GPIB Adapter Data Manual from Texas Instruments Inc. semiconductor group. Connections to page 1 include HPI- to U36-1, WR- from U45-3, SRES- from U44-9, and RD-. Connections from page 2 are the I/O data bus, buffered address lines BA1 - BA3, chip select HP- from U19-12 and 4 Mhz+ clock from U69-13.

The data lines are buffered through U7, a 75160A octal general purpose interface bus transceiver. The control lines are routed through U8, a 75162A which is also a GPIB transceiver. SC+ U8-1 is from U39-15 of this page. both U7 and U8 are bi-directional and further information on them may be found in the Line Driver and Line Receiver Data Book from

Texas Instruments.

XVII.07 PAGE 7 OF SCHEMATIC DIAGRAMS :

POWER AND GROUND

This page includes all of the power and ground connections for jack connectors and integrated circuits on the main printed circuit board.

XVII.08 LIST OF SIGNAL ABBREVIATIONS :

A "-" OR "+" after a signal name signifies inverting or noninverting.

AS+	Address Strobe from 68000
A#	Address line from 68000
A#-	Buffered address line
BA1+	Buffered Address line 1 to I/O section
BA2+	Buffered Address line 2 to I/O section
BA3+	Buffered Address line 3 to I/O section
BT-	Baud rate time chip select (U10)
BR1+	Baud rate clock to terminal port
BR2+	Baud rate clock to modem port
BE-	Buss error
BD#+	Buffered data to peripheral chips
BRD-	Boot Ram Disable
BRW+	Buffered Read/Write, read is active high
BRW-	Buffered Read/Write, read is active low
CAS#-	Cas for bank #
CN-	Printer port chip select (U37)
CD-	Carrier detect from modem port
D8MHz-	Delayed 8 MHz clock
DTACK-	Data Transfer Acknowledge
DS-	Dip switch port chip select (U36)
FC2-	Function code 2 from CPU
FD-	Floppy disk controller chip select (U50)
FDI+	Interrupt direct from floppy disk controller (U50)
FDI-	FDC interrupt after software enable
FDIE+	Floppy disk interrupt enable
FRES+	Reset floppy disk controller
HPI-	IEEE 488 interrupt (U68)
HP-	IEEE 488 interface chip select (U69)
I/O+	High when in I/O address space
IC1-	Interrupt #1 to 68000
IN-	Interrupt Device chip select (U8)
I2-	Unassigned interrupt on expansion connector
I3-	Unassigned interrupt on expansion connector
LW0-	Lower byte Write nibble 0
LW1-	Lower byte Write nibble 1
LEDR+	LED enable
LDS+	Lower Data Strobe active high
MFM+	Output from FDC to select double density DD=1
MOT-	Motor on active low
MI+	Interrupt from Ring detect or Carrier detect
PCRMP-	Write precomp active low
PRTY-	Parity error signal active low
PFL+	Parity Flag Low active high (1=parity error)
PFH+	Parity Flag High active high.
RWR-	Write dir ram buffer enable. (Permanently enabled)
RRD+	Read direction ram buffer enable
ROM-	Rom chip select active low

RDY+	Floppy disk controller READY input
RD-	Read active low (delayed 1 T state)
RMI-	Software reset for Ring/carrier detect interrupt
RX2I+	Receive interrupt from modem port
RX1I+	Receive interrupt from terminal port
RW-	1 = Read, 0 = Write
RG-	Ring detect from modem port
RA#+	Ras outputs to rams
RF-	Refresh granted from arbitration active low
RF+	Refresh granted from arbitration active high
SC+	Control line for IEEE 488 buffer
SRES+	System reset from reset SW or CPU
S1-	Terminal port chip select (U25)
S2-	Modem port chip select (U26)
SL0-	Drive select 0 (decoded)
SL1-	Drive select 1 (decoded)
SI+	Software interrupt
TM-	Timer chip select (U9)
TX1I+	Transmit interrupt from terminal port
TX2I+	Transmit interrupt from modem port
TC+	Terminal count input to floppy disk controller
UDS+	Upper Data Strobe active high
UW0+	Upper byte write nibble 3
UW1+	Upper byte write nibble 4
WR-	Write active low (delayed 2 T states)
WCK+	Write clock for floppy disk controller
WP+	Write protect input from disk drive
64 Khz	Refresh clock. High 3.125 usec every 15.625 usec

XVIII ERROR LOOKUP LIST :

Generally, a problem is specific to only a part of the machine. This section lists the various run-time error codes and discusses probable causes and how to deal with them. Refer to the Operating System Manual for assembler and compiler errors.

XVIII.01 BIOS CHANNEL ERROR CODES :

Error codes are returned by the BIOS for the Initialize, Read, Write, and Status check commands. The errors are word values with negative numbers. Zero represents a no error (normal) condition. Most of the error codes pertain to the floppy driver. Codes -14. and -15. may come from any device.

SUMMARY OF BIOS CHANNEL ERROR CODES	
0	No error.
-1	Floppy controller would not respond.
-2	Floppy controller returned invalid command error.
-3	Recalibrate or Seek failure (equipment check).
-4	No diskette (as a result of read/write timeout).
-5	Missing address mark reported by floppy controller.
-6	No Data Found reported by floppy controller.
-7	Overrun reported by floppy controller.
-8	CRC Error reported by floppy controller.
-9	End of Cylinder reported by floppy controller.
-10	Write Protect Violation.
-11	Address out of range.
-12	Wrong Cylinder reported by floppy controller.
-13	currently unused
-14	Illegal device number
-15	Illegal request

XVIII.02 BOOT ERRORS :

Boot aborted on drive X. The user typed "Q" to quit the boot routine and go to the debugger. This is not really an error, but a notice to the user in case "Q" was typed accidentally.

CRT PROBLEMS See TERMINAL PROBLEMS.

Drive error (code) on drive X where X is 0 for the left-hand drive and 1 for the right-hand drive.

The code can be:

01	- controller failure
02	- invalid command
03	- recalibrate or seek failure
04	- timeout
05	- missing address mark
06	- no data found
07	- overrun
08	- CRC error
09	- end-of-cylinder
0A	- unknown
0B	- address out-of-range

GARBAGE TEXT See TERMINAL problems.

LED BLINKING If blinking on boot see TERMINAL PROBLEMS. A blinking LED in the CYCLER test indicates that the test is finished. Connect a terminal and type ESC to view the results of the test. Refer to the CYCLER section.

LED GREEN This indicates that the processor is happy with the boot and is busy. If no memory is being accessed, the LED will normally be RED. If Green and nothing is being displayed on the terminal, the processor may be stuck in a software loop.

LED RED The LED is normally RED if no memory is being accessed. However, if the LED is red on boot, the system is not working properly. Isolate the cause using the SYSTEM LEVEL TROUBLE SHOOTING section. If the CPU board is suspect replace it or repair it using CPU BOARD TROUBLE SHOOTING.

Not Boot disk

This error occurs on startup if the boot diskette does not have a boot program in the first 2 sectors. The boot can be copied from the master system diskette or another good boot diskette by using the boot copy routine in SAGEUTIL. SAGEUTIL also allows you to change some parameters of the boot.

The disk drive may also not be working right. If your system has other boot devices, try booting from them. For example, on a SAGE II:

Press Reset

type "Q" to get to the debugger

insert boot disk in the right drive

type "IF1" to boot to the right drive.

NO TEXT ON TERMINAL

See TERMINAL PROBLEMS.

WILL NOT START

The machine does not start up. The processor LED is red, no output is sent to terminal. In some cases the terminal will display @ signs. (If you do have an error message on the terminal go to the correct error description in this section.) Assuming that the board once worked, a completely dead system is generally the failure of a chip OR a power supply problem. Refer to the Boot test section for aid in finding the problem. If the processor light is blinking, the terminal chip is not working right. See TERMINAL PROBLEMS.

Try to localize the problem following the system trouble-shooting guide.

TERMINAL PROBLEMS

If the LED is RED you most likely do NOT have a terminal protocol problem. See LED RED.

No text or garbage text is most likely due to a configuration problem. If you have a non-Sage connector check to see if pins 2 and 3 are reversed. The SAGE II terminal is set up as Data Communications equipment. Refer to the CABLE WIRING NOTES on how the cable should be built.

Refer to the section on the POWER UP ROUTINE to see how the SAGE switches should be set. Refer to your terminal manual to set it up to the same protocol. Refer to the User's manual to find out how to SETUP a new terminal and how to use SAGEUTIL. Appendix A in the User's Manual also defines the switches.

XVIII.03 EXCEPTION ERRORS :
These errors are generally caused by software problems except for RAM parity errors.

When processing an exception error, interrupts are turned off and the BIOS is disabled, unless the user has re-directed the error to his own error handling routine. Non user-intercepted errors have this format:

EXCEPTION: <error type> 'Error at' <8 digit location>

Error types are defined:

Bus Error

The processor tried to read memory and there was no response. Memory may not exist. A hardware strapping option determines what memory is equipped. Additional information is displayed:

"Function:xxxx Access:xxxxxxxx Instr:xxxx"

Function is a 4 digit word with bits set:
0-2 ..are the state of the processor function code outputs FC0,FC1 and FC2
3 ..is 0 for an instruction, 1 for not an instruction.
4 ..is 0 for write, 1 for read.

Access is the 8 digit address of the attempt.
Instr is the 4 digit instruction word executed

Bus error on TIME OUT

A bus time out error is caused when AS- stays low for longer than 16 usec. This is caused by either a software or hardware condition which prevents DTACK- from being applied within ~ 16 usec. U3, a 74LS390 dual decade counter is used to count cycles of the 500 Khz clock, the QD output of the counter is fed through U7, an open collector inverting buffer to the BERR- input to the processor. AS- is applied to the clear input causing the counter to be cleared whenever AS- is inactive. Whenever AS- goes active (low) the counter starts counting and if AS- has not been removed by the 8th count, QD goes high generating a bus error signal.

BUS ERROR DUE TO ADDRESSING NONEXISTANT MEMORY LOCATIONS

Whenever a memory address is addressed which is not a decoded address in the SAGE II memory map there is no DTACK- generated which causes a bus timeout error as described above. This allows an orderly recovery from the addressing of any nonexistent memory locations. A DTACK- is generated for all locations in the SAGE II memory map which means that if the system had only 128K and a location between 128K & 512K were addressed, there would be no indication. To solve the problem the bank enables for banks 1, 2, & 3 are fed through an noninverting open collector buffer (U14) to the bus error input of the processor through a dip shunt. With the proper connections in the dip shunt the addressing of any location in banks 1, 2, or 3 can cause a bus error indicating an invalid memory address.

Address error

The processor attempted to access a word or long word on an odd address. Additional information is displayed with this error:

"Function:xxxx Access:xxxxxxxx Instr:xxxx"

Function is a 4 digit word with bits set:
- 0-2 ..are the state of the processor function code outputs FC0,FC1 and FC2
- 3 ..is 0 for an instruction, 1 for not an instruction.
- 4 ..is 0 for write, 1 for read.

Access is the 8 digit address of the attempt.
Instr is the 4 digit instruction word executed

Illegal Instruction

There are 2 unused opcodes (Axxx & Fxxx) in the 68000 which are currently undefined and will give this error if an attempt is made to use them. Also, any undefined instruction format or addressing mode will cause this error.

Arithmetic error

An attempt was made to divide by zero or a CHK instruction was executed (user needs to define vector) or a TRAPV instruction was executed (user needs to define vector).

Privilege error

User tried an instruction which requires SUPERVISOR mode.

Reserved TRAP

Certain TRAP locations have been reserved by Motorola for future use and should not be used. (This error should never occur.)

Unassigned TRAP

There are 16 trap locations in the 68000, 0-14 of which are normally unassigned by the Debugger. Trap 15 is used for breakpoints by the Debugger. Traps 8 to 14 are used by the BIOS.

Unassigned Interrupt

There are 6 auto-interrupt vectors. Normally all of them are unassigned by the debugger.

RAM Parity error

Remember when troubleshooting that the Parity chip itself could be the cause of this error. Note that the location shown is where the program was executing and is not necessarily the location with the error. Swapping a suspect ram chip into a different location can help isolate the error as it should follow the chip. If the system will boot to a floppy, run the CYCLER RAM test.

The 7th auto-interrupt vector is non-maskable and is used for RAM parity error reporting.

Unknown error

Either the program entered the TRAP handler illegally or the supervisor stack was not set to point to valid ram.

EXECUTION ERROR X

The number given with the execution error means:

0 System error
1 Invalid index, value out of range
2 No segment, bad code file
3 Procedure not present at exit time
4 Stack overflow
5 Integer overflow
6 Divide by zero
7 Invalid memory reference <bus timed out>
8 User break
9 System I/O error
10 User I/O error
11 Unimplemented instruction
(For example: no floating point pkg in interp.)
12 Floating point math error
13 String too long
14 Halt, Breakpoint
15 Bad Block
16
17 wrong arithmetic package
(2 word instead of 4 word) or
(4 word instead of 2 word)

XIX HARDWARE CHANGES ON SAGE II :

Various small changes have been made to the SAGE II model. To date these changes do not change the functional operation of the SAGE II with the possible exception of the CTS remote port changes and PROM updates. These changes are minor and can be done on site or at the SERVICE CENTER fairly quickly with little cosmetic effect.

XIX.01 PROM CHANGES :

Changes to the Boot PROMS and BIOS are well-documented in the RELEASE notes in the SAGE II Users' Manual.

XIX.02 CPU BOARD CHANGES :

The versions of the SAGE II CPU board have different part numbers:

CB0000 -Shipped Jun 1982 to Jul 1982
CB0001 -Shipped Jul 1982 to Dec 1982
CB0002 -Shipped Dec 1982 to ___ 1983
CB0002B -Shipped ___ 1983 to _____

Details of the changes follow.

XIX.03 CHANGES FROM CB0000 TO CB0001 :

The CB0000s were modified by the factory to be as nearly identical electrically as possible to the CB0001. Any problems with the CB0000 should be referred to the factory.

Both the CB0000 and CB0001 have 32K of address space decoded for I/O. Newer versions of the CPU board have a portion of this space mapped for the new SAGE IV products. The "MOD" page of the schematics shows the circuit layout added to the new boards which will allow the user to free up unused I/O space. CB000 and CB0001 do not have this circuit so they cannot be easily modified to be used in a SAGE IV.

Pin 8 of the fourth row of RAM was tied to ground instead of +5V.

A silkscreen of the parts location was added to CB0001.

A damping resistor was put in series on the D8mhz signal.

Changes were made to the Ground plane and +5V plane layouts.

A mounting screw was unconnected from ground plane.

Refresh counter circuit was changed. U13-6 was cut from U13-11 and connected to U13-13.

The delay line layout was changed to make mods easier for the different types of delay lines. (See the Delay line notes in this section.)

The parity circuit was changed:

U50-1 to U32-12 to U41-1 (BRW+)
U50-2 to pin 14 of Lower Parity RAM
U50-3 to U64-4
U32-13 to pin 14 of Upper Parity RAM
U32-11 to U31-4

Pin 2 of Lower Parity RAM to U64-6
Pin 2 of Upper Parity RAM to U31-6

U39-14 to U37-9
U37-8 to U51-10

XIX.04 CHANGES FROM CB0001 TO CB0002 :

The CB0001 was not modified to conform electrically with the CB0002 except where specifically detailed below.

One side of ground on the floppy ribbon connector (pin 34 of J4) was cut to remove a ground loop. Factory mod was done to some CB0001s.

The Reset switch layout had a ground loop which was removed.

CB0001 had these chips silkscreened wrong:

U35 was shown as LS245 should be LS240
U59,61 was shown as 75189 should be 1489
U60 was shown as 75188 should be 1488

The CB0001 had one factory mod to connect the terminal port CTS (J10-5) to U61-4.

The CB0002 changed the terminal port CTS layout. +5V was removed from pin 4 of terminal port U61. Pin 4 was connected to strap S06 input. +12V was connected to A of S06. Pin 5 (CTS) was connected to B of S06. This connects all three points of the strap so that CTS normally high. To drive CTS, the connection to B (+12V) must be cut first. (See the S06 strap mod for the CB0002 as the change for this was not quite right.)

The CB0002 changed the terminal port DSR layout. Pin 6 of the terminal port was connected to +12V. (User DSR) Pin 20 of the terminal port was connected to U61 pin 13. (SAGE DSR) This will allow a user cable to be made which holds DSR high by wiring pin 6 to 20 on the terminal connector. This was done as a convenience to the user so that it is not necessary to change an internal strap.

A pullup resistor was added to the IEEE488 (GPIB) interrupt line.

U66 was too close to U67. The can of U66 (clock) could short against U67, so U66 was moved up. When changing U66 on the CB0001 bend the clock leads so that U66 sits away from U67 slightly.

Series damping resistors were added on signals BA1, BA2, BA3 and AS+.

The CD+ and RG+ remote port interrupt circuit was changed. U59-11 was connected to U39-21 and U61-8 was connected to U39-20. Inputs to U52 go through a differentiator.

Pin 27 became an option (strap S05) on the parallel printer port and can be strapped either to +5V or Ground.

Various capacitors were repositioned.

The Straps were silkscreened and numbered.

U76 (LS00) was added to allow the user to make a mod to allow extra data hold time for slow peripheral chips. See the mod sheet of the schematics. Also one gate of U76 was used for the optional mod to allow ram to be the first 512K or the second 512K.

The mod sheet of the schematics also shows a mod to free up unused I/O ADDRESS space which is necessary to use the CB0002 in a SAGE IV.

The mod sheet also shows a mod to allow addressing the first 128K to cause a Buss error.

Chassis ground was removed from the mounting hole which was closest to the power connector.

The ground plane on the front edge was moved back slightly.

A layout for an extra unused chip was added.

XIX.05 CHANGES FROM CB0002 TO CB0002B :

The first 150 CB0002 boards needed U65 (7406) pin 7 wired to ground. All were modified in the factory.

Resistors R7 & R6 were located too close to a trace on the back of the board. Solder bridges were common so resistor pads were moved.

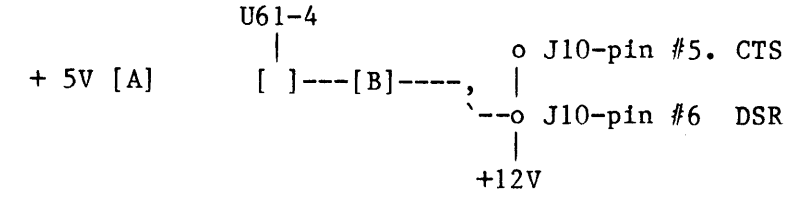
Mounting holes were slightly changed to work better with the Winchester board CB0003.

The floppy connectors were moved towards the rear of the board about 1/4 to 1/2 inch as the bay was too close to the mounting holes.

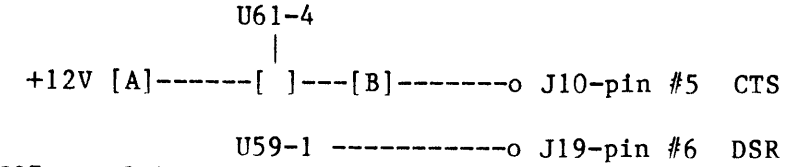
A few systems were shipped in December which may have had underrated capacitors (68 uf 6V) across the 12V supplies. These **MUST** be replaced with 10uf 25V capacitors **REGARDLESS** of whether they seem to cause problems or not.

The straps as shown in older Users' Manuals (before version [1.4]) and their schematics do not match this board. The main difference is in how the straps are named. However STRAP S06 for the CTS signal IS wrong.

> CB0002 was connected as shown below. If the user attempts to strap CTS high [A] (+5v) a short will exist to +12V. To drive CTS, cut the trace from pin 6 to pin 5. Cut the trace from [B] to pin 6. Rewire pin 5 to [B]. Also cut +12V from pin 6 and connect pin 6 to U59-1.

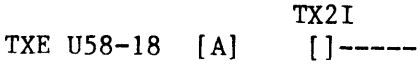


> CB002A was connected so that CTS is normally held high.
> To drive CTS, the strap from [A] must be cut.



U59-1 ----------o J19-pin #6 DSR

Strap S07 was labeled on the silkscreen:



XIX.06 DELAY LINE MODS :

Small quantities of different U42 DELAY lines were used due to delivery problems with the standard part. The other parts did not have the same pinouts so mods were made to various systems. The delay values also differed slightly. The table below is also shown on the schematic to help reference the pins while troubleshooting.

Delay values vs pin numbers:

U42	IN	(70	90)	(250	260)	(370	375)	IN	60	Shipped
DDU-7-8087-1	1	13			3	12		5	8	100
DDU-7-8087	1		13	3			12	5	8	10
DDU-4-8150	1	12			4	10		5	8	standard
ESC 98-61	1		12	4		10		6	8	15

The CB0000 boards have a slightly different layout in the U42 area which makes it more difficult to implement a change for a different delay line.

XIX.07 MECHANICAL CHANGES :

.....	About 50 machines were shipped with lids that were slightly tight. The newer lids are longer by 0.04 inches. The older lid may not fit on a new machine so it is not a good idea to mix and match lids.
Aug-82	The mechanics were changed to reduce the number of mounting holes. The old and new driveshields are interchangeable, but some holes will be left open. The old and new power shields are interchangeable but 4 hole positions at the back will not line up. A cosmetic problem only.
Jan 83	New style mechanics (as designed for SAGE IV and low-profile SAGE II) included a design for standard size SAGE II with removable front and back. Some AC-DC power wiring harnesses prior to Jan 1 will not reach to the connectors of all types of drives. The new harnesses (CB0006B) are longer and can be installed in older systems when necessary. On 220V systems shipped before Jan 1 83 the fans were hard-wired in. Some plug-in fans were shipped after that which require that a plug (CA0008B) be wired in to the power supply connector to connect the fan to.

XIX.08 GENERAL MECHANICAL NOTES :

Torin fans should not be used in Low profile systems. If these bronze bushing fans are mounted with the axle in a vertical position, the lubricant will run to the bottom and reduce the life of the fan.

INDEX

- D -

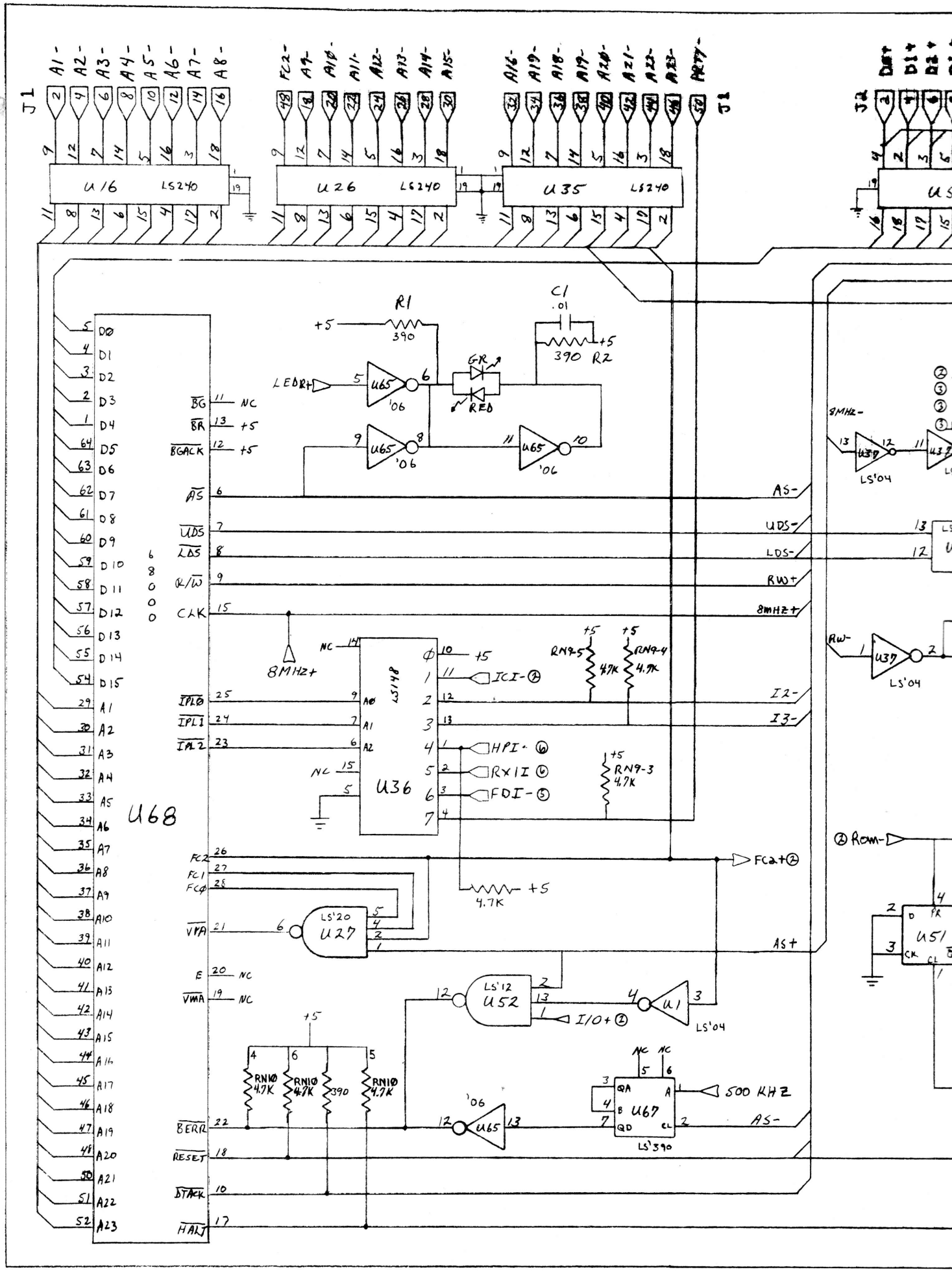
- E -

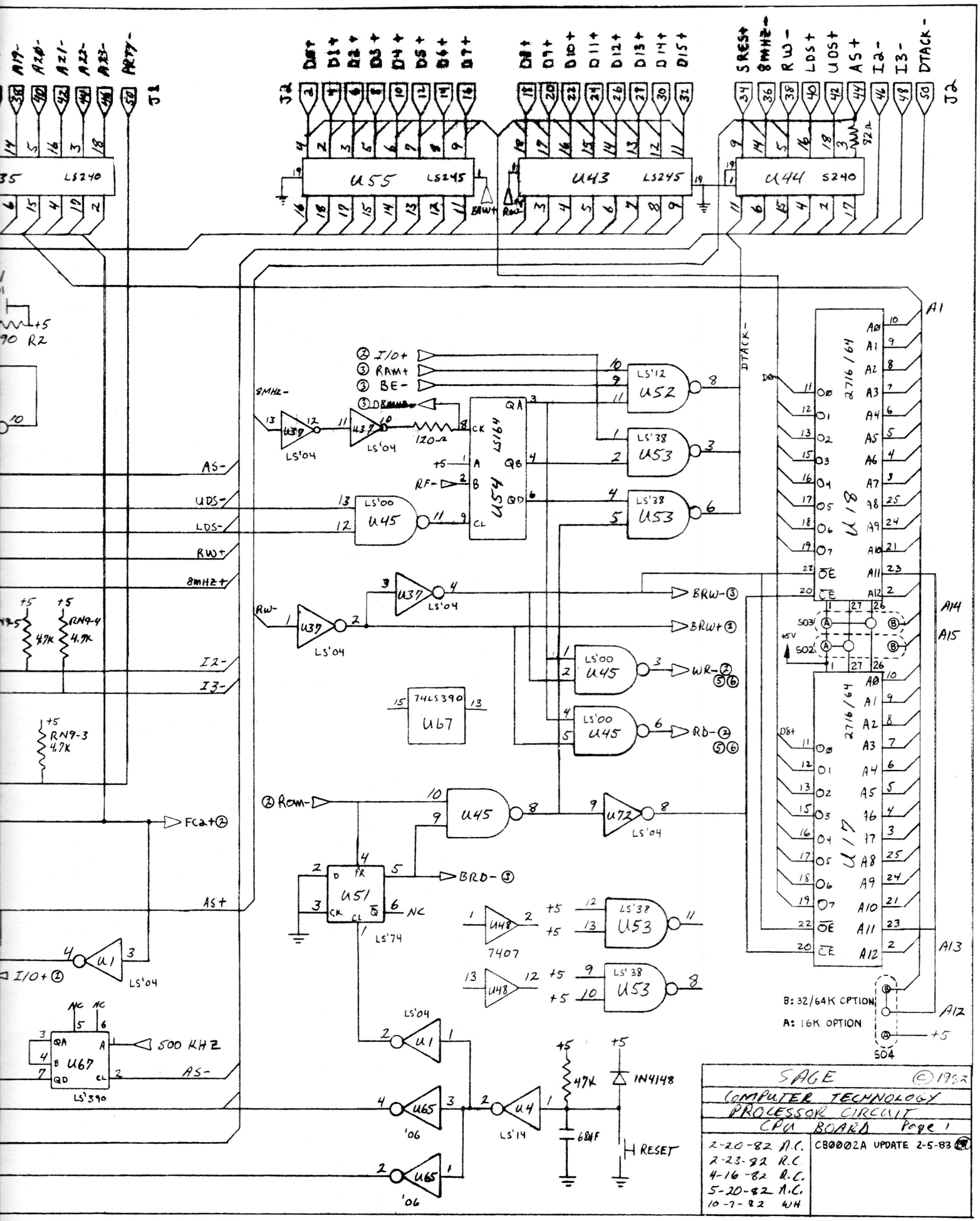
- F -

- T -

- U -

- W -


J1
A1-
A2-
A3-
A4-
A5-
A6-
A7-
A8-
U16 LS240
FC2-
A9-
A10-
A11-
A12-
A13-
A14-
A15-
U26 LS240
A16-
A19-
A18-
A17-
A20-
A21-
A23-
A22-
U35 LS240
J2
D0+
D1+
D2+
R1
390
+5
C1
.01
390 R2
LEDR+
U65 '06
GR
RED
U68
68000
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
BG NC
BR +5
BGACK +5
AS
UDS
LDS
R/W
CLK
BERR
RESET
DTACK
HALT
IPL0
IPL1
IPL2
E NC
VMA NC
VPA
FC2
FC1
FC0
8MHz+
U36 LS148
ICI-④
HPI-⑥
RXII⑥
FDI-⑤
RN9-5 4.7K
RN9-4 4.7K
RN9-3 4.7K
4.7K
U27 LS'20
U52 LS'12
I/O+②
U1 LS'04
RN10 4.7K
RN10 4.7K
390
RN10 4.7K
U67 LS'390
500 KHZ
AS-
AS+
UDS-
LDS-
RW+
8MHZ+
I2-
I3-
FCa+②
8MHz-
U39 LS'04
RW-
U37 LS'04
②Rom-
U51


J1
J2
U55 LS245
U43 LS245
U44 S240
U54 LS164
U52 LS'12
U53 LS'38
U45 LS'00
U37 LS'04
U67 74LS390
U51 LS'74
U48 7407
U1 LS'04
U65 '06
U4 LS'14
U72 LS'04
U67 LS'390
2716/64 U18
2716/64 U17
SO3
SO2
SO4
B: 32/64K OPTION
A: 16K OPTION
500 KHZ
RESET
IN4148
47K
.68MF
DTACK-
AS-
UDS-
LDS-
RW+
8MHZ+
I2-
I3-
AS+
FCa+②
BRW-③
BRW+③
WR-②⑤⑥
RD-②⑤⑥
BRD-③
NC
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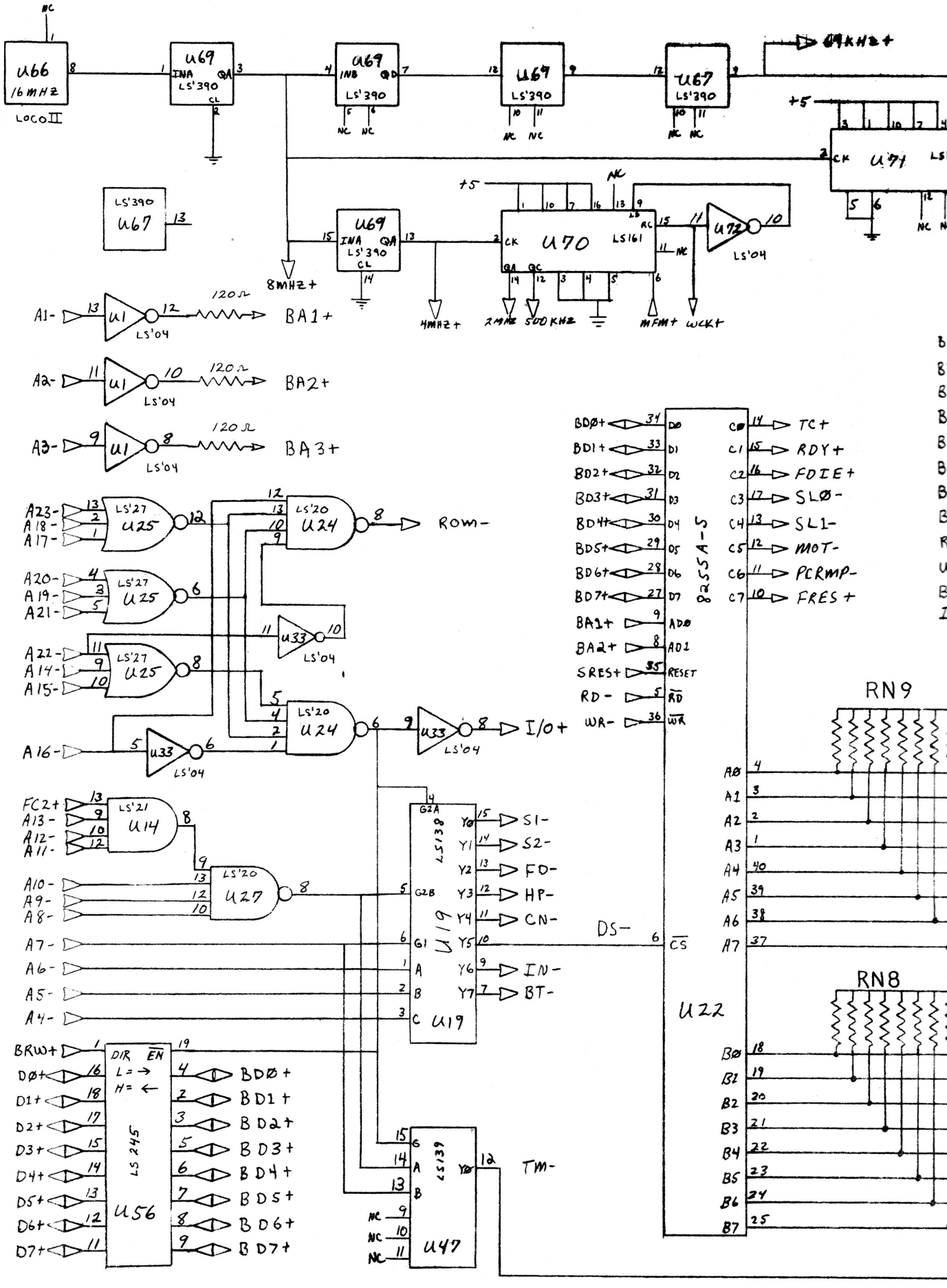
COMPUTER TECHNOLOGY
PROCESSOR CIRCUIT
CPU BOARD Page 1
2-20-82 R.C.
2-23-82 R.C.
4-16-82 R.C.
5-20-82 R.C.
10-7-82 WH
CB0002A UPDATE 2-5-83 ⓒ


U66
16MHZ
LOCO II
U69
LS'390
U67
LS'390
U71
U70
LS161
U72
LS'04
8MHZ+
4MHZ+
2MHZ
500KHZ
MFM+
WCK+
69KHZ+
+5
A1-
A2-
A3-
BA1+
BA2+
BA3+
120Ω
U1
A23-
A18-
A17-
A20-
A19-
A21-
A22-
A14-
A15-
A16-
LS'27
U25
LS'20
U24
U33
ROM-
I/O+
FC2+
A13-
A12-
A11-
A10-
A9-
A8-
LS'21
U14
U27
A7-
A6-
A5-
A4-
U19
LS138
S1-
S2-
FD-
HP-
CN-
IN-
BT-
DS-
BRW+
DØ+
D1+
D2+
D3+
D4+
D5+
D6+
D7+
DIR
EN
L=→
H=←
LS 245
U56
BDØ+
BD1+
BD2+
BD3+
BD4+
BD5+
BD6+
BD7+
U47
LS139
TM-
8254-5
U22
BDØ+
BD1+
BD2+
BD3+
BD4+
BD5+
BD6+
BD7+
BA1+
BA2+
SRES+
RD-
WR-
TC+
RDY+
FDIE+
SLØ-
SL1-
MOT-
PCRMP-
FRES+
RN9
RN8
AØ
A1
A2
A3
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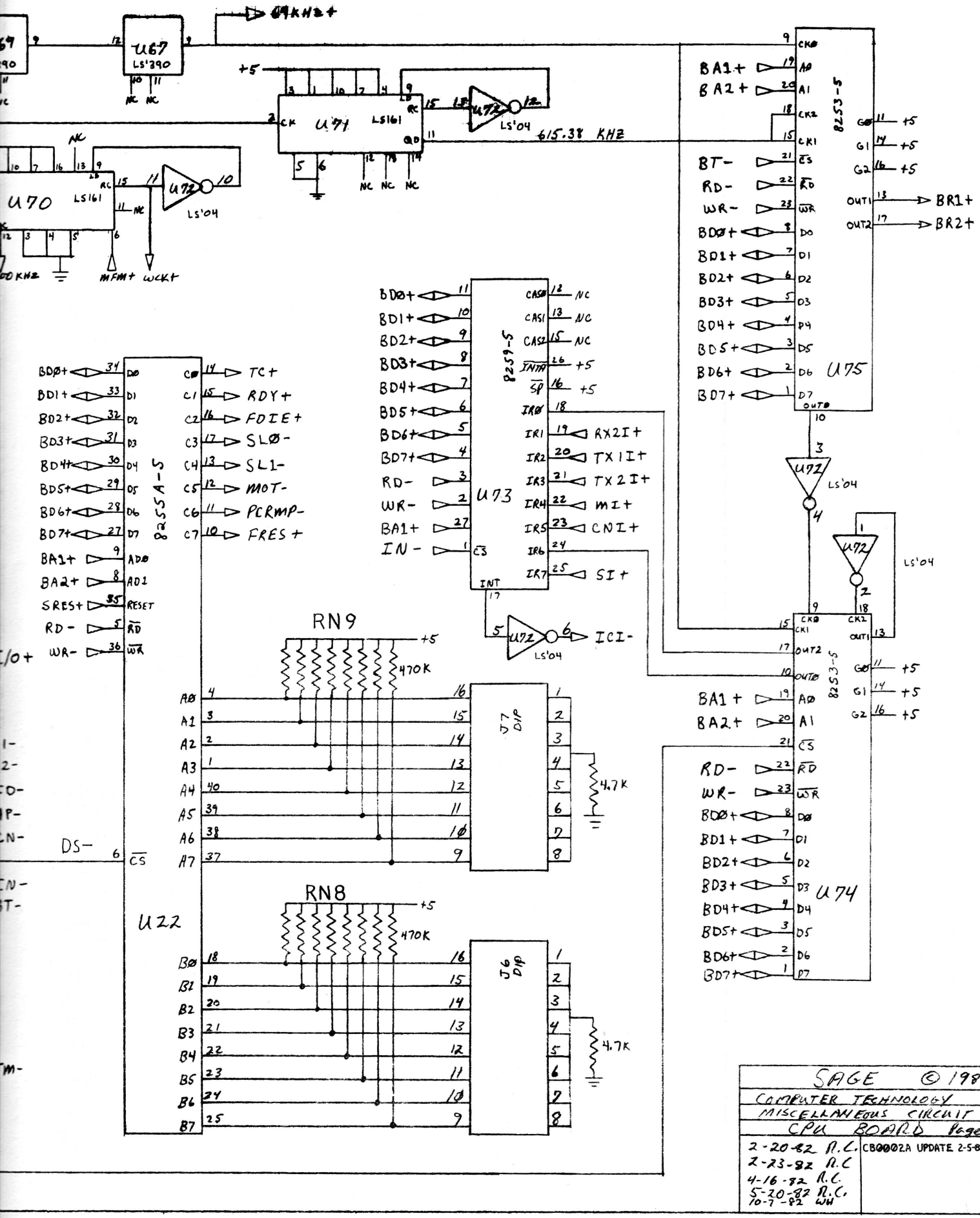
A7
BØ
B1
B2
B3
B4
B5
B6
B7



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MISCELLANEOUS CIRCUIT
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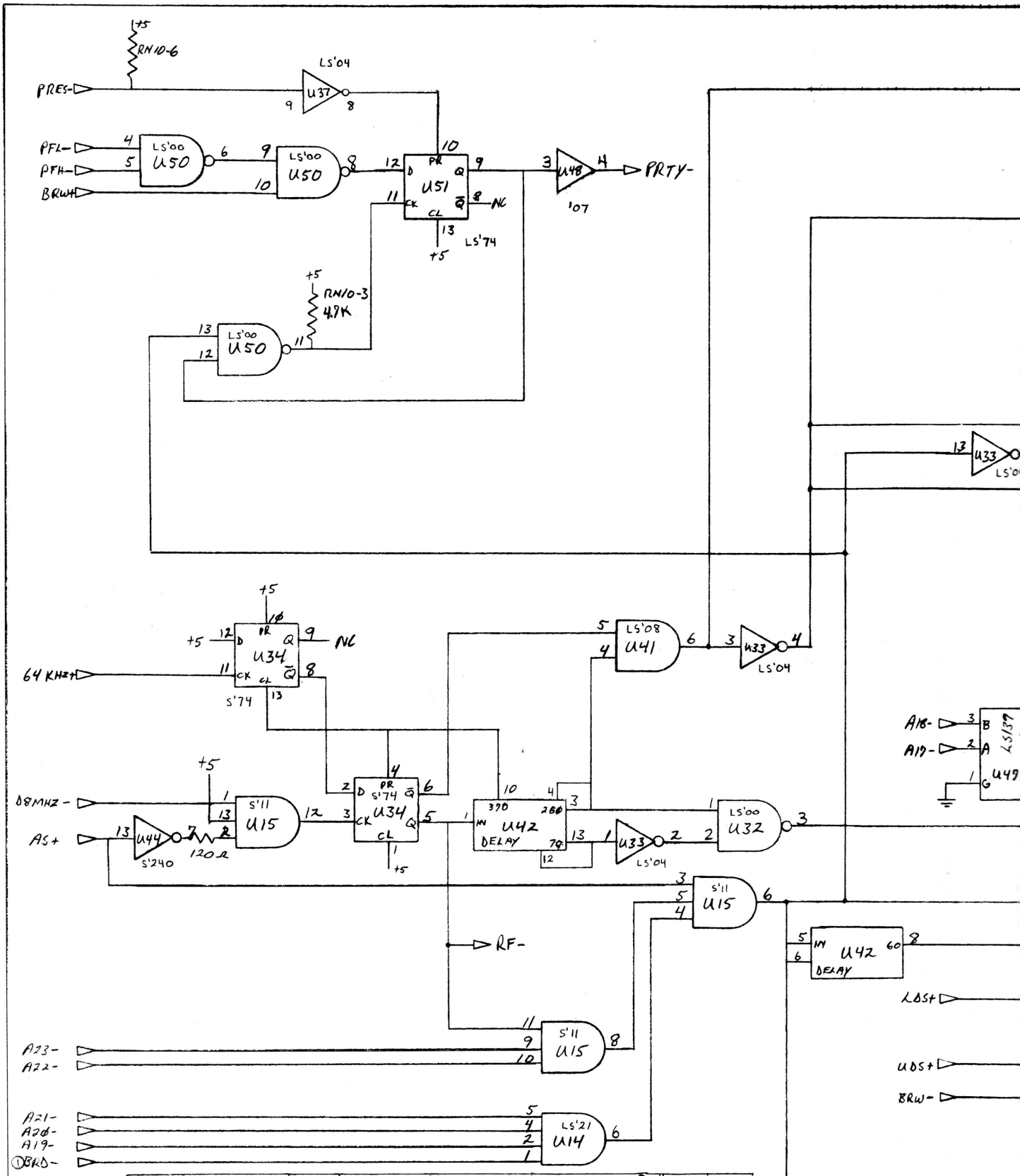
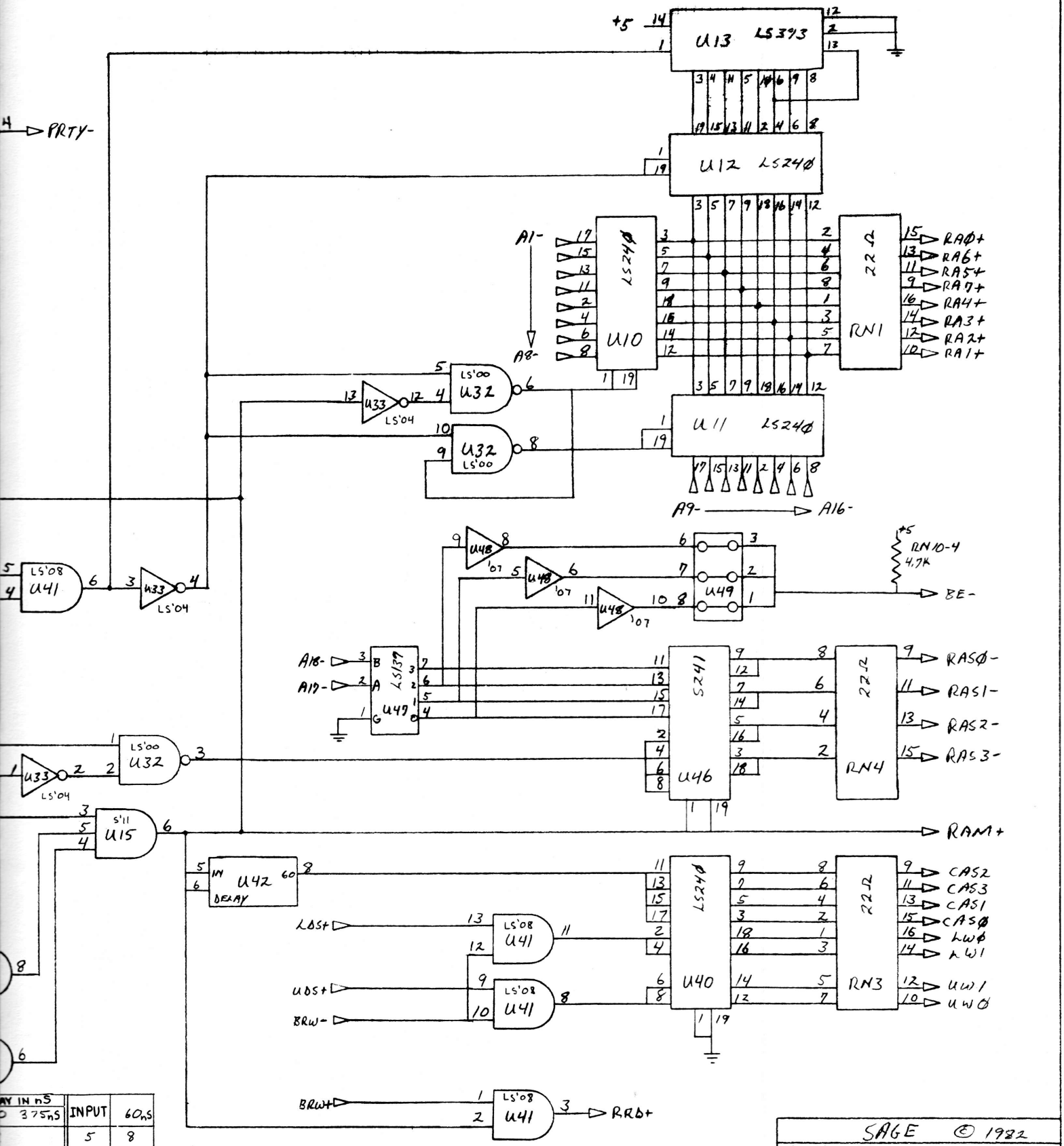
2-20-82 N.C.
2-23-82 N.C
4-16-82 N.C.
5-20-82 N.C.
10-7-82 WH

CB0002A UPDATE 2-5-83 GM



ALTERNATE DELAY LINE PINOUTS

U42 PART NUMBER	INPUT	PIN NUMBERS FOR COLUMN HEADING DELAY IN nS						INPUT	60nS
		70	90nS	250	260nS	370	375nS		
DDU-7-8087-1	1	13			3	12		5	8
DDU-7-8087	1		13	3			12	5	8
DDU-4-8150	1	12			4	10		5	8
ESC 98-61	1		12	4			10	6	8



AY IN nS		
0 375nS	INPUT	60nS
	5	8
12	5	8
	5	8
10	6	8

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RAM CIRCUIT
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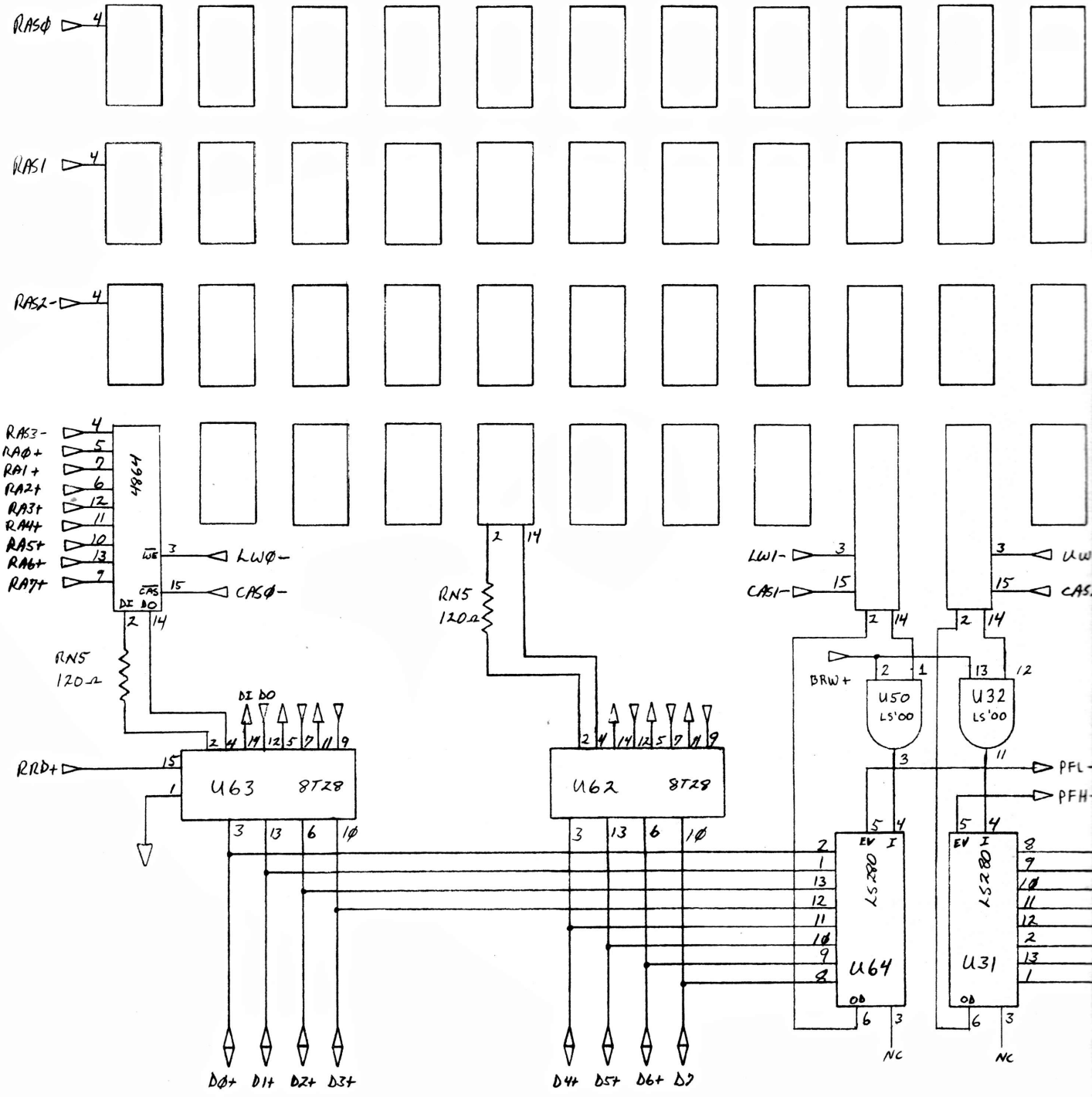
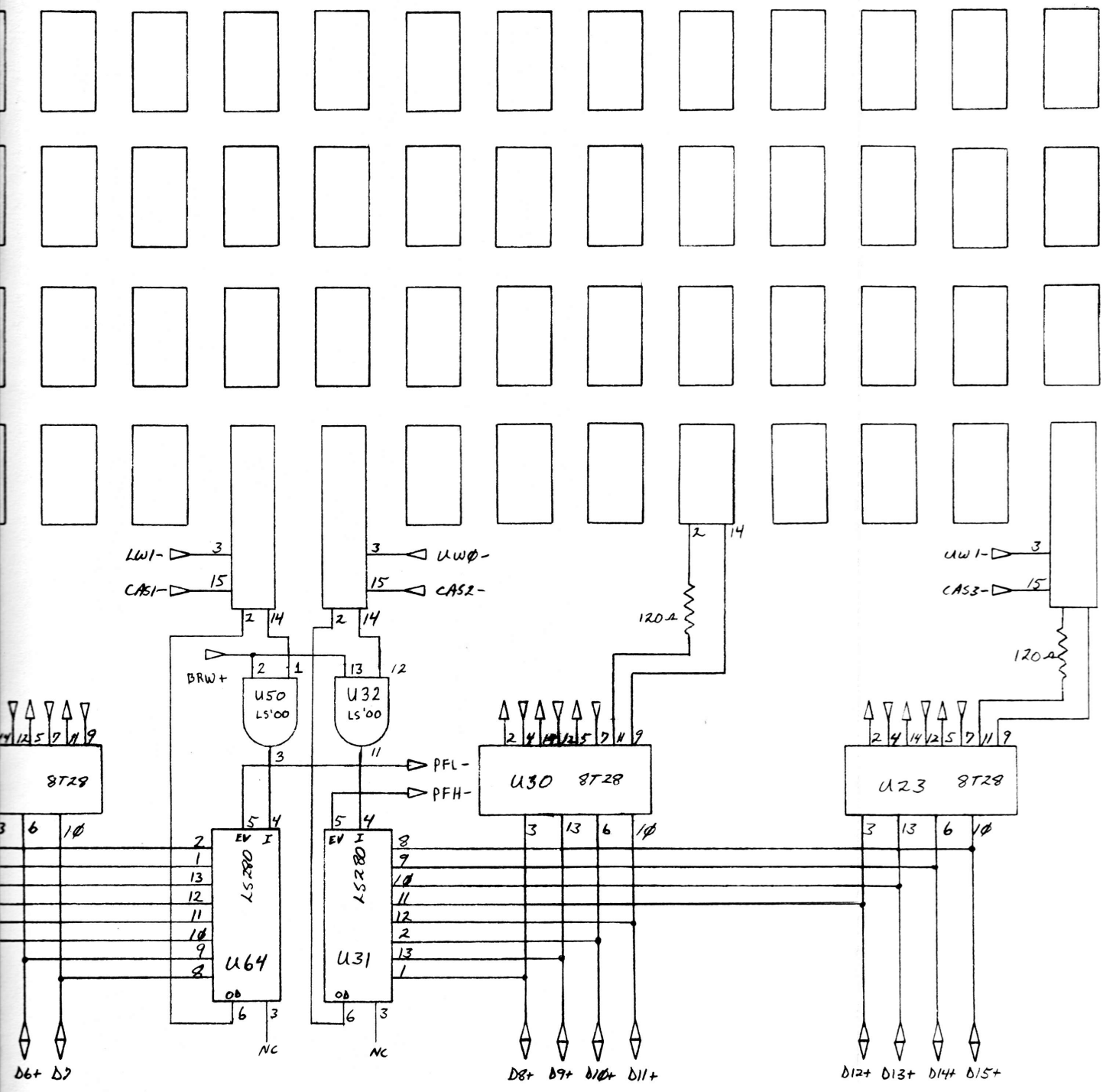
2-20-82 R.C.
2-23-82 R.C.
4-16-82 R.C.
5-20-82 R.C.
10-7-82 WH

CB0002A UPDATE 2-5-83 (80)


RAS0
RAS1
RAS2-
RAS3-
RA0+
RA1+
RA2+
RA3+
RA4+
RA5+
RA6+
RA7+
4464
WE
CAS
DI DO
LWØ-
CASØ-
RN5
120Ω
RRD+
U63 8T28
U62 8T28
DI DO
LWI-
CASI-
BRW+
U50 LS'00
U32 LS'00
PFL-
PFH-
U64
U31
LS280
EV I
OD
NC
DØ+ DI+ D2+ D3+
D4+ D5+ D6+ D7



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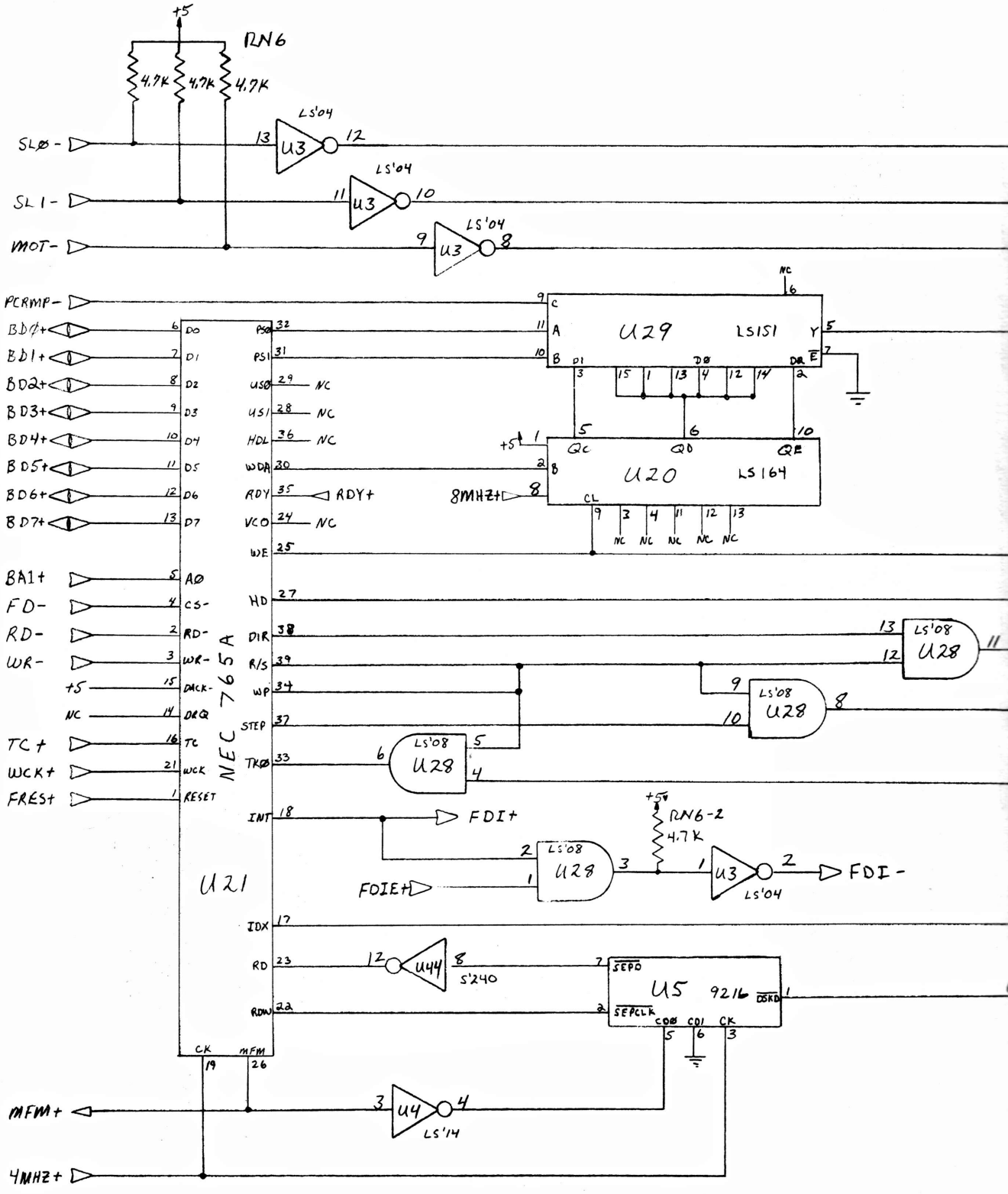
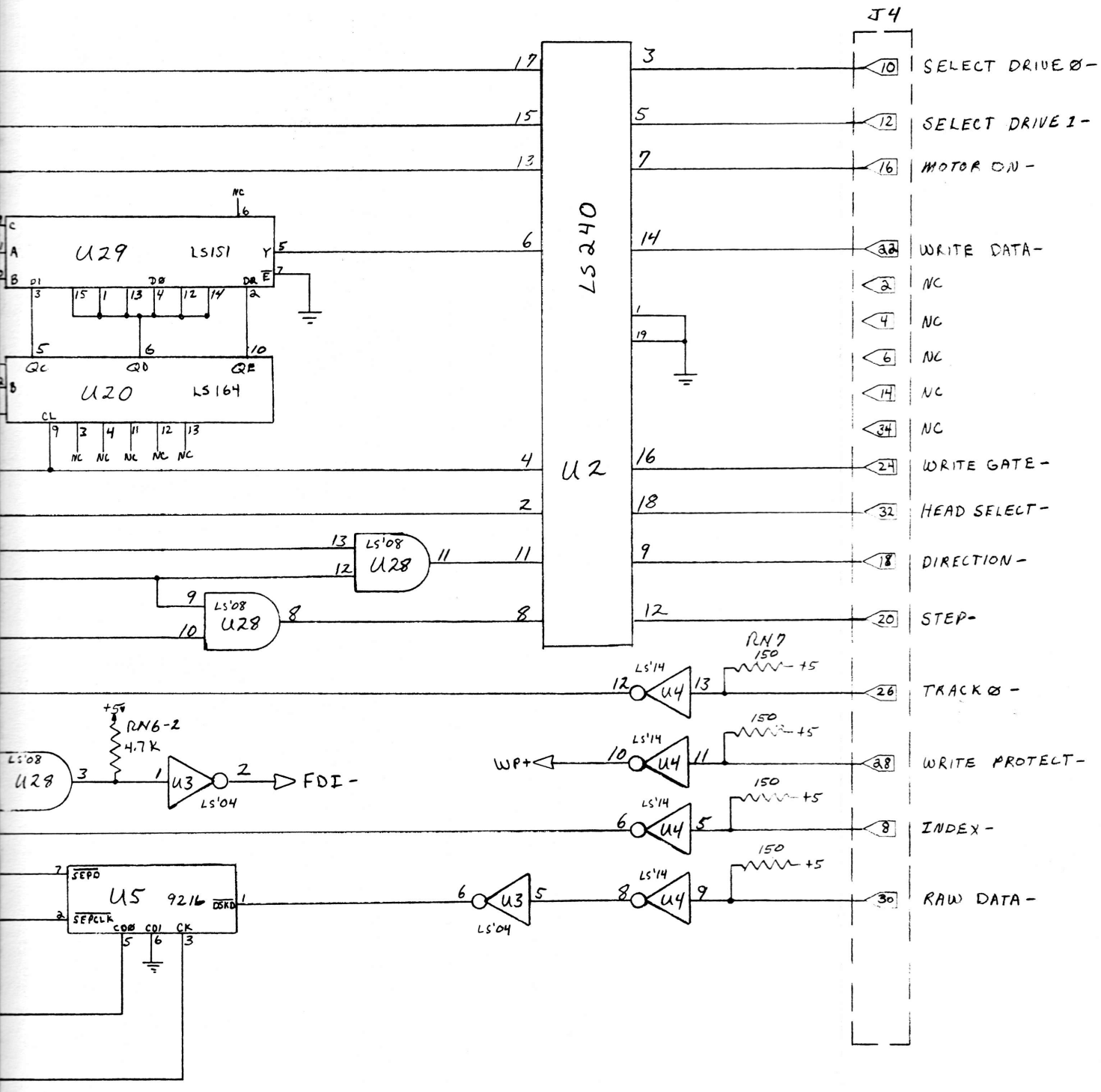
RAM ARRAY	
CRU BOARD page4	
2-20-82 N.C. 2-23-82 N.C. 4-16-82 N.C. 5-20-82 N.C. 10-7-82 WH	CXXXD2A-NOCHANGE-2-5-83 (RA)


+5
RN6
4.7K
4.7K
4.7K
LS'04
U3
SL0-
SL1-
MOT-
PCRMP-
BD0+
BD1+
BD2+
BD3+
BD4+
BD5+
BD6+
BD7+
BA1+
FD-
RD-
WR-
+5
NC
TC+
WCK+
FRES+
NEC 765A
U21
D0
D1
D2
D3
D4
D5
D6
D7
A0
CS-
RD-
WR-
DACK-
DRQ
TC
WCK
RESET
PS0
PS1
US0
US1
HDL
WDA
RDY
VCO
WE
HD
DIR
R/S
WP
STEP
TRK0
INT
IDX
RD
RDW
CK
MFM
NC
RDY+
U29
LS151
U20
LS164
8MHZ+
U28
LS'08
FDI+
FDI-
FDIE+
RN6-2
4.7K
U44
S'240
U5
9216
SEPD
SEPCLK
COD
CDI
CK
DSKD
U4
LS'14
MFM+
4MHZ+



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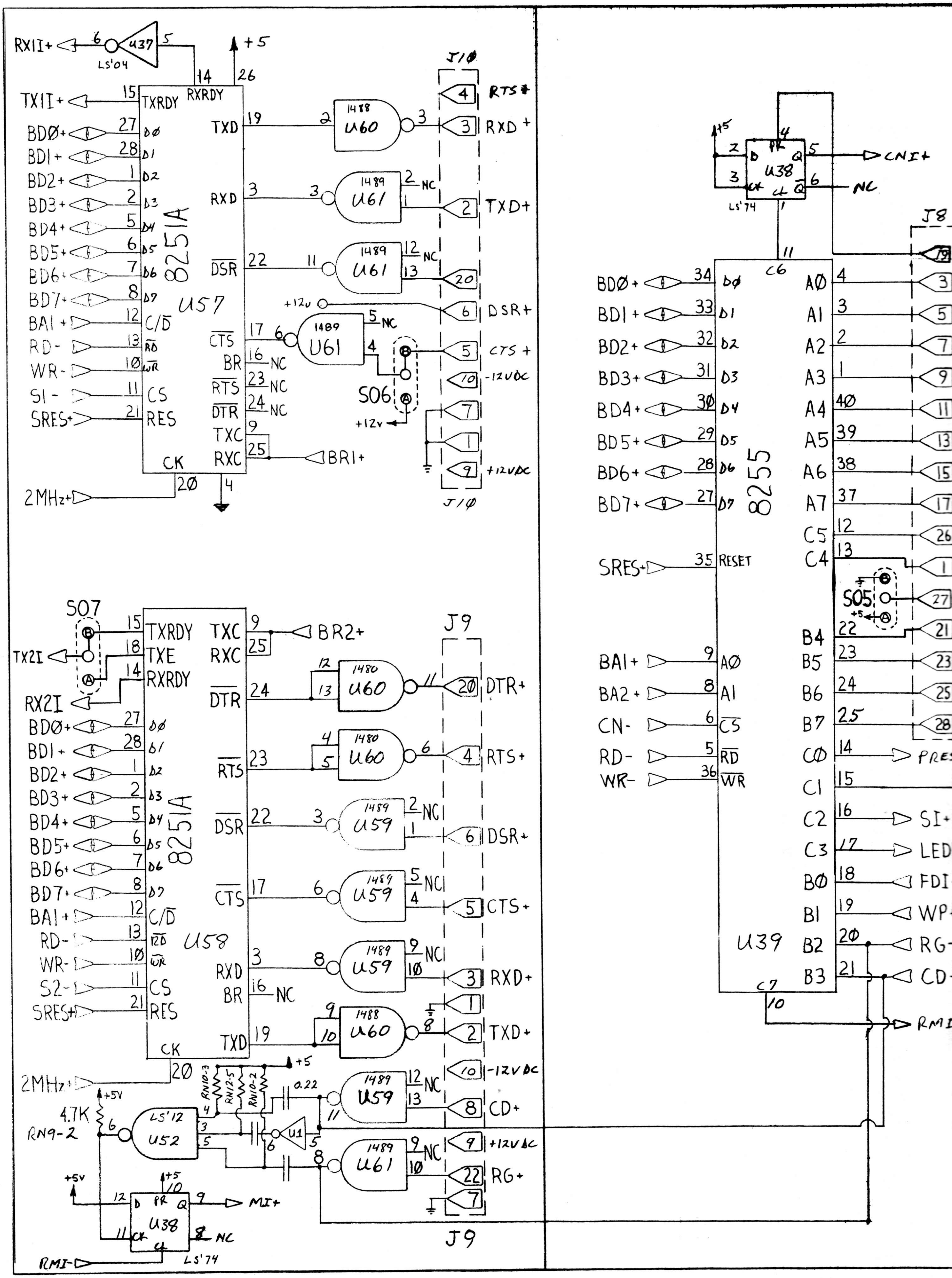
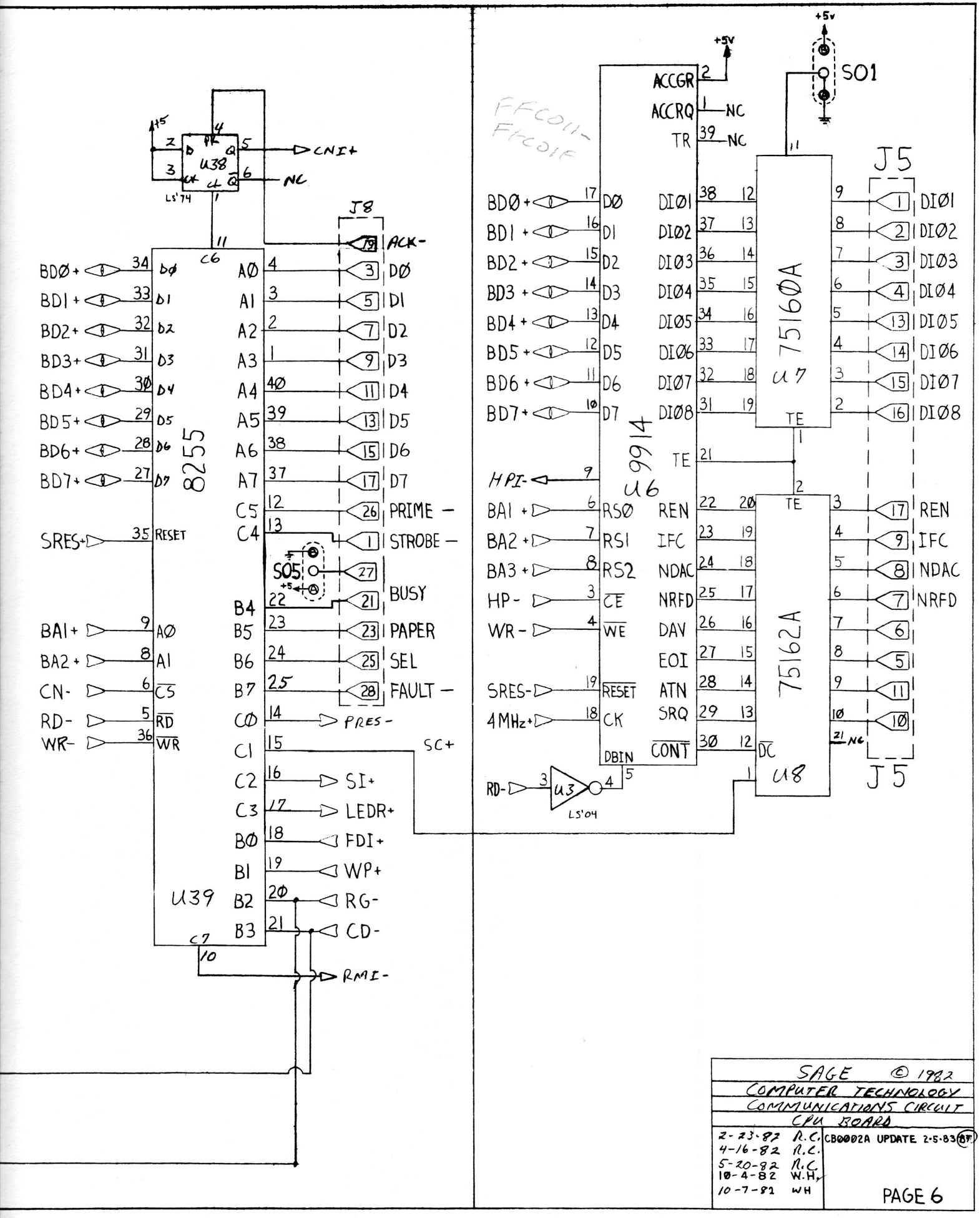
FLOPPY DISK CIRCUIT
CPU BOARD PAGE 5
5-20-82 R.C.
CB0002A- NO CHANGE 2-5-83 (BR)



8251A
U57
8251A
U58
8255
U39
U60
U61
U59
U38
U52
U37
J10
J9
J8
S06
S07
S05
TXRDY
RXRDY
TXD
RXD
DSR
CTS
RTS
DTR
TXC
RXC
BR
TXE
C/D
RD
WR
CS
RES
CK
RESET
RXI1+
TXI1+
RX2I
TX2I
BD0+
BD1+
BD2+
BD3+
BD4+
BD5+
BD6+
BD7+
BA1+
BA2+
RD-
WR-
S1-
S2-
SRES+
CN-
2MHz+
BR1+
BR2+
RTS+
RXD+
TXD+
DSR+
CTS+
DTR+
CD+
RG+
-12VDC
+12VDC
+12v
+5
+5V
NC
LS'04
LS'74
LS'12
1488
1489
0.22
4.7K
RN9-2
RN10-3
RN12-5
RN10-2
U1
MI+
RMI-
CNI+
SI+
LED
FDI
WP
RG
CD
RMI
PRES



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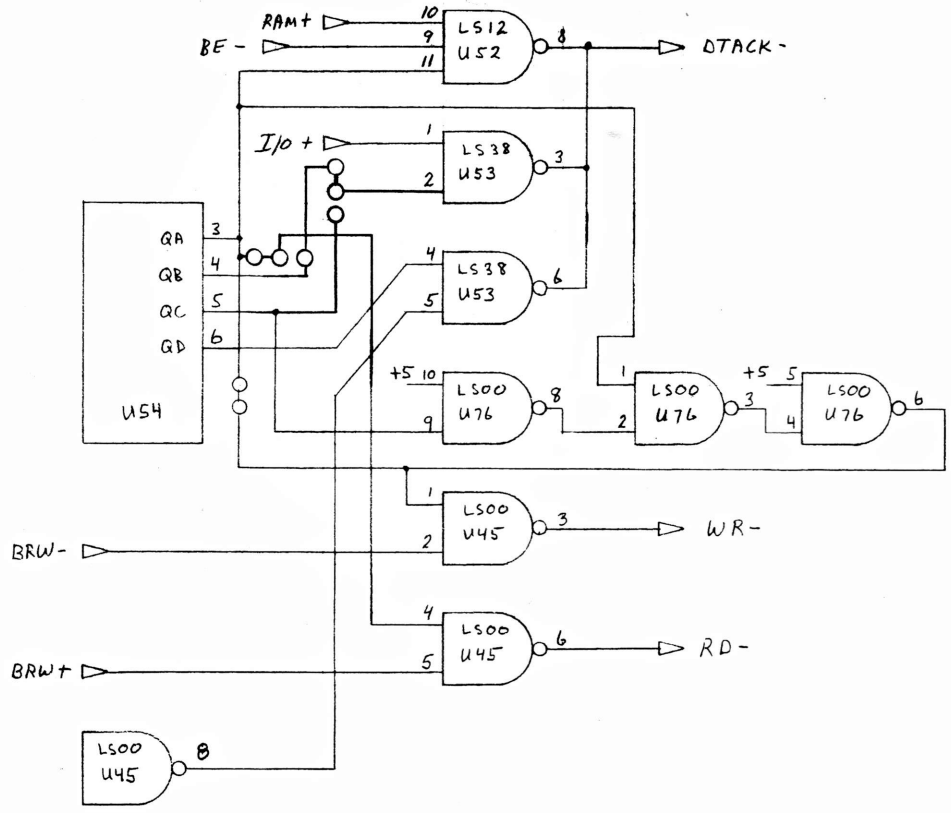
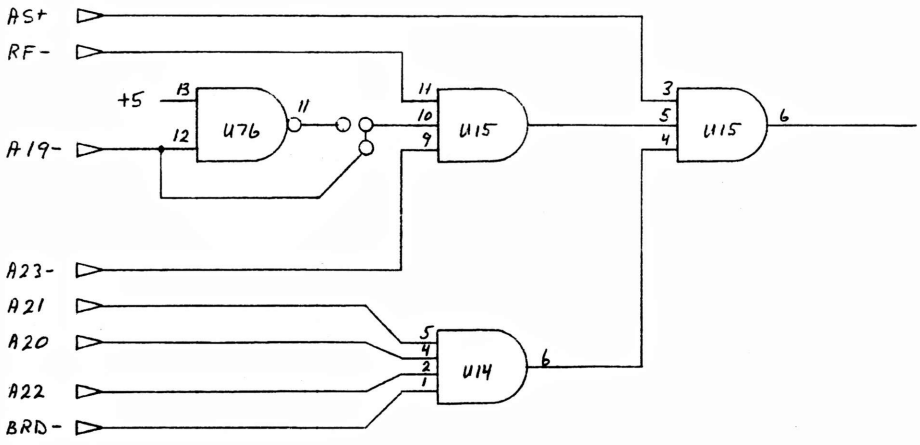
COMMUNICATIONS CIRCUIT		
CPU BOARD		
2-23-82	R.C.	CB0002A UPDATE 2-5-83 BT
4-16-82	R.C.	
5-20-82	R.C.	
10-4-82	W.H.	
10-7-82	WH	



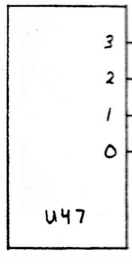
MOD TO ALLOW EXTRA DATA HOLD TIME FOR SLOW PERIPHERAL CHIPS

11-2-82

MOD TO FREE UP UA



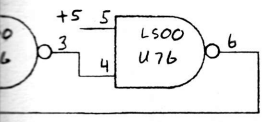
MOD TO ALLOW RAM TO BE FIRST 512K OR SECOND 512K



MOD TO ALLOW ADDR

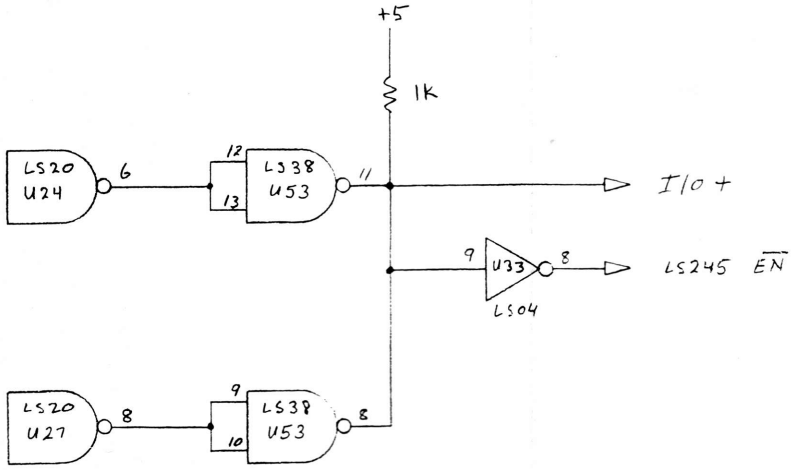
11-2-82

DTACK-



WR-

RD-

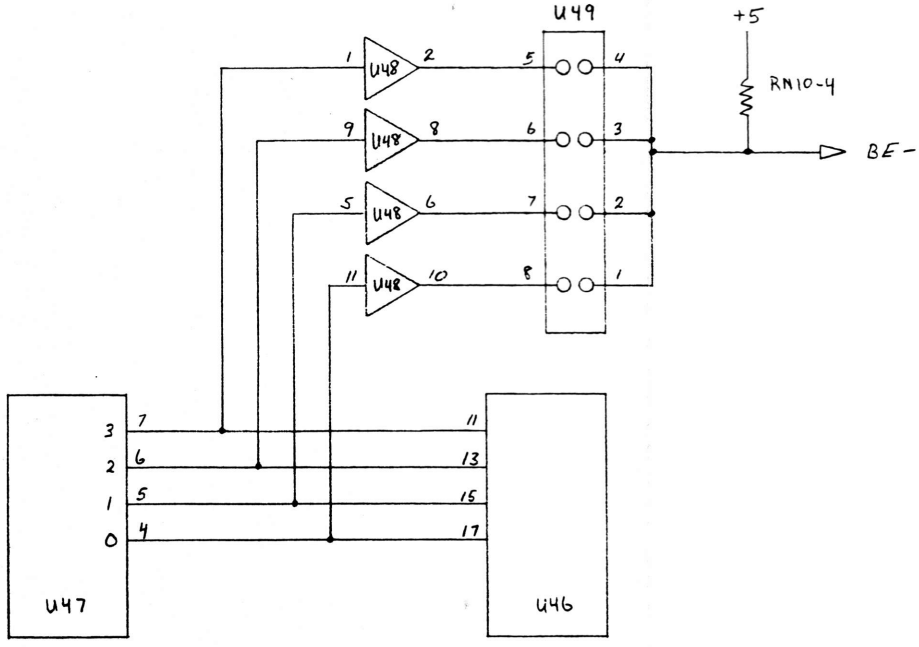


PIN 6 OF U24 STILL GOES TO U19 PIN 4 AND U47 PIN 15
U27 PIN 8 STILL GOES TO U19 PIN 5 AND U47 PIN 14
U27 PIN 8 DOES NOT GO TO U56 PIN 17

MOD TO FREE UP UNUSED I/O ADDRESS SPACE

11-2-82

11-2-82



MOD TO ALLOW ADDRESSING FIRST 128K TO CAUSE BUSS ERROR

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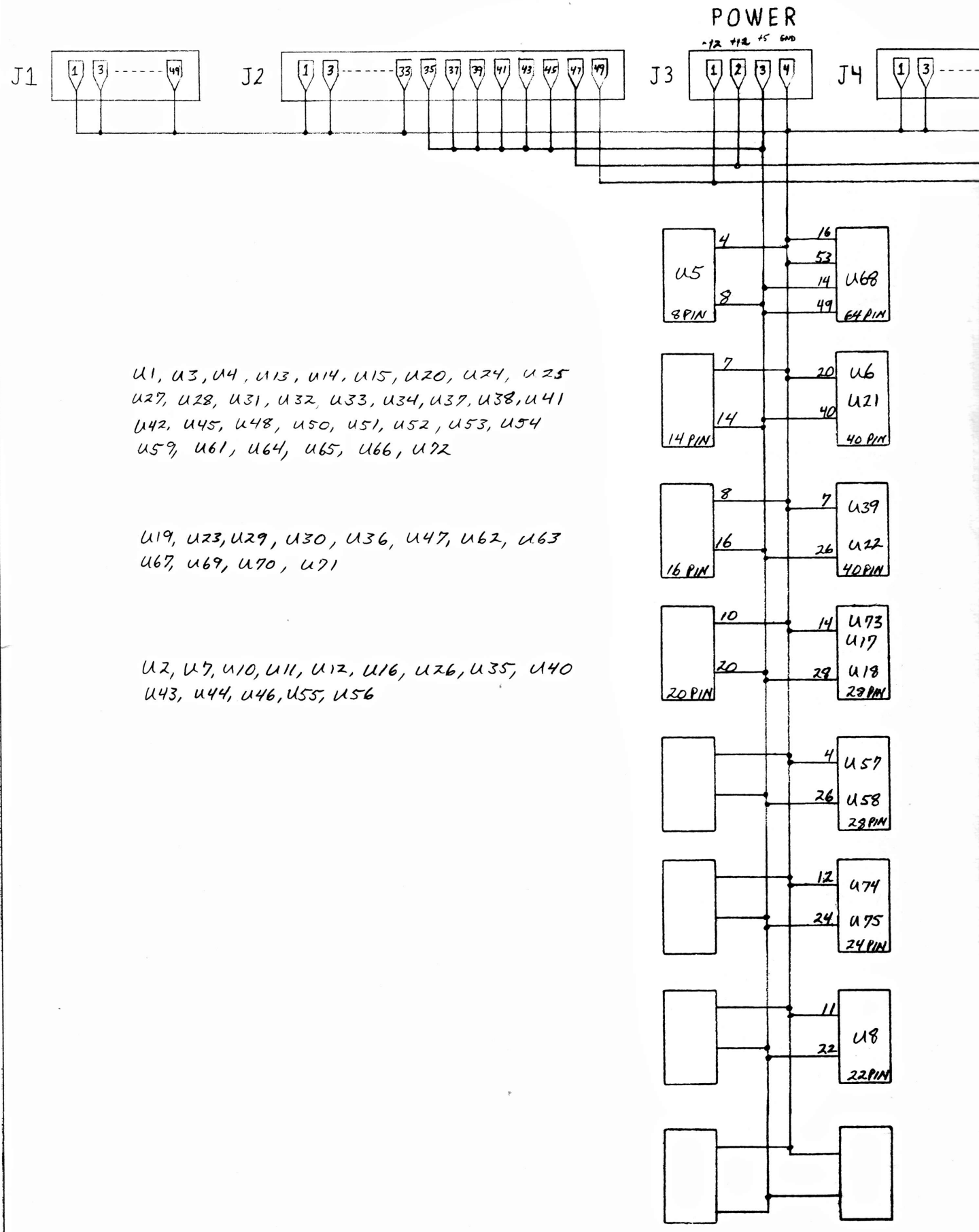
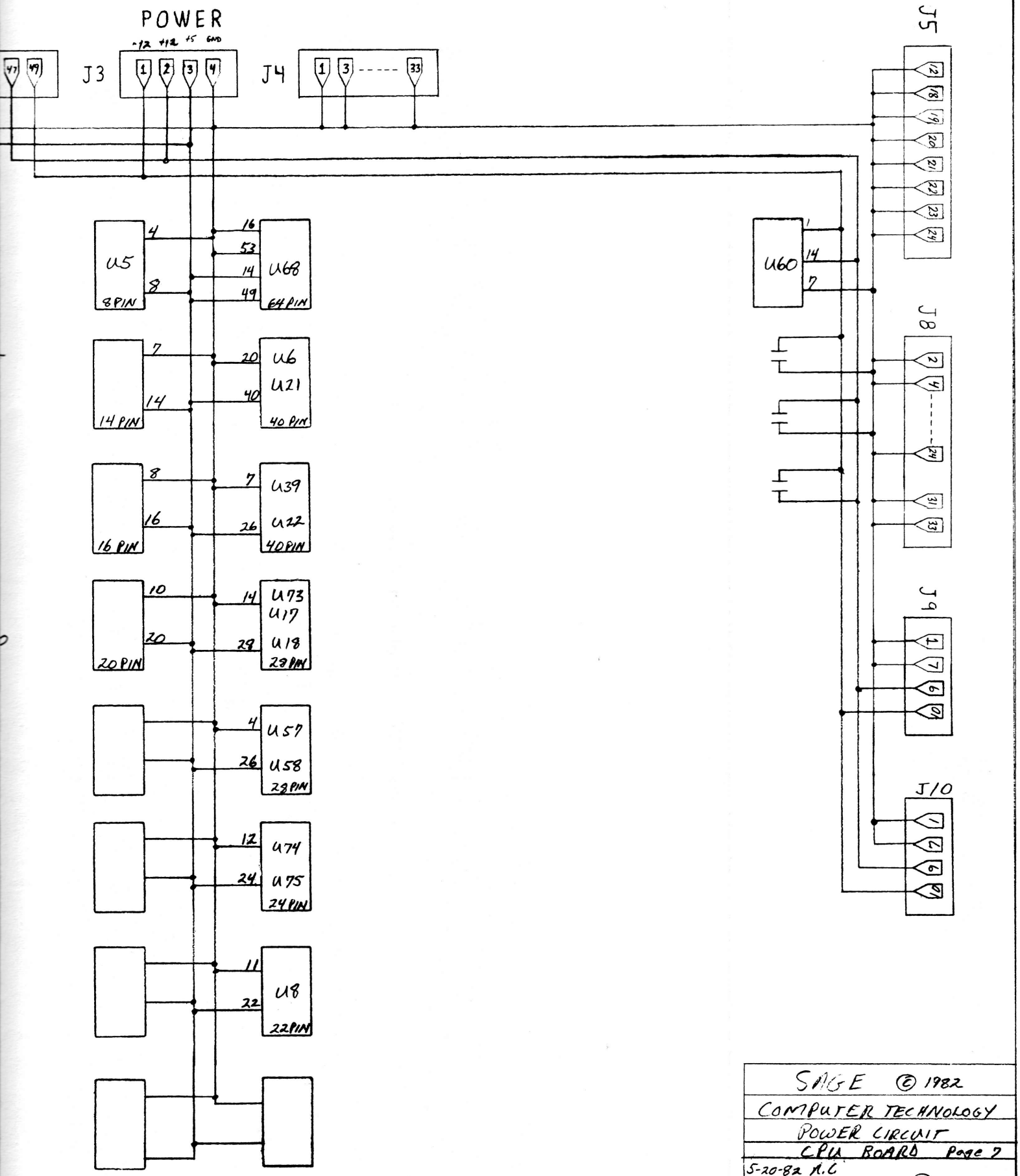
MODIFICATIONS TO CPU BOARD
11-2-82
CB0002A UPDATE 2-5-83 BM

11-2-82


POWER
-12 +12 +5 GND
J1
J2
J3
J4
U5
8 PIN
U68
64 PIN
U6
U21
40 PIN
14 PIN
U39
U22
40 PIN
16 PIN
U73
U17
U18
28 PIN
20 PIN
U57
U58
28 PIN
U74
U75
24 PIN
U8
22 PIN
U1, U3, U4, U13, U14, U15, U20, U24, U25
U27, U28, U31, U32, U33, U34, U37, U38, U41
U42, U45, U48, U50, U51, U52, U53, U54
U59, U61, U64, U65, U66, U72
U19, U23, U29, U30, U36, U47, U62, U63
U67, U69, U70, U71
U2, U7, U10, U11, U12, U16, U26, U35, U40
U43, U44, U46, U55, U56



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COMPUTER TECHNOLOGY
POWER CIRCUIT
CPU BOARD Page 7
5-20-82 A.C
CB0002A-NO CHANGES - 2-5-83 (870)