RCA 601

ELECTRONIC DATA PROCESSING SYSTEM

GENERAL DESCRIPTION

COMPUTER, MODEL 604

RADIO CORPORATION OF AMERICA

Electronic Data Processing Division
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GO 361

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INTRODUCTION

This description together with the RCA 601 General Information Manual provides a description of the Model 604 Computer.

The Model 604 Computer encompasses all of the features of the RCA 601 System and performs all of the functions of the Model 603 Computer.

In addition the Model 604 Computer increases the speed and enhances the scope of application of the system by the incorporation of the following features:

- Faster staticizing times
- Faster Address Modification times
- Floating Point Arithmetic

These additional features, provided by the Model 604 Computer, result in a significant increase in the overall performance of the RCA 601 System, and at the same time, compatibility is maintained between the Model 603 and the Model 604 Computers. Programs written for the Model 603 may be run on the Model 604 with no reprogramming required.

The Model 603 recognizes the Model 604 Floating Point Instructions by their class codes (the C digit of the Operation Half Word) and causes automatic transfer to fixed standard locations in memory. From these locations, control can be transferred to subroutines performing the same functions as are performed by Floating Point Instructions in the Model 604.

COMPUTER, MODEL 604

The Model 604 Computer is a high speed general purpose digital computer. It incorporates all of the features of the RCA 603, and it increases the overall performance of the RCA 601 System by the inclusion of the following features:

A. 1.5 to 4.5 μs staticizing times.

B. 1.25 μs Address Modification time.

C. Addition of Floating Point Arithmetic to the instruction complement.

FLOATING POINT ARITHMETIC

The Model 604 Computer provides instructions for performing floating point operations on both excess 50 decimal and excess 256 binary floating point data. Both single and double precision operations are permitted. The instructions included are:

Floating Add Decimal
Floating Add Binary
Floating Subtract Decimal
Floating Subtract Binary
Floating Multiply Decimal
Floating Multiply Binary
Floating Multiply and Accumulate Decimal
Floating Multiply and Accumulate Binary
Floating Divide Decimal
Floating Divide Binary

Floating Point Arithmetic Operations

Data Format

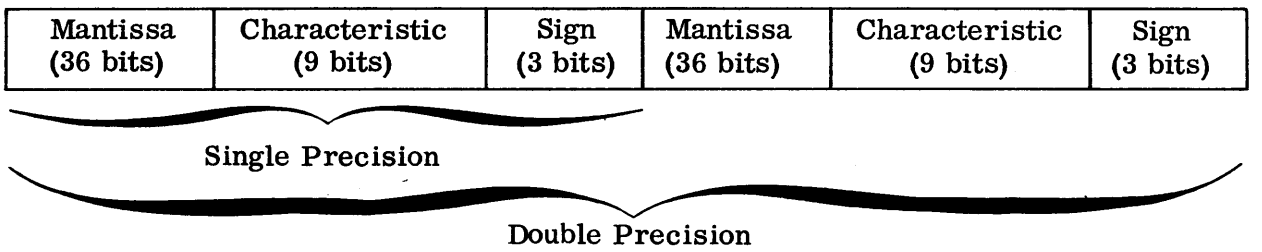
Decimal (4-bit characters only)

Mantissa (9 digits)	Characteristics (2 digits)	Sign (1 digit)	Mantissa (9 digits)	Characteristic (2 digits)	Sign (1 digit)

Single Precision

Double Precision

Binary



Note: The signs of both words of double precision data should agree; otherwise, the sign of the most significant word will be used.

The characteristic of the least significant word of double precision decimal data must be nine less than that of the most significant word.

The characteristic of the least significant word of double precision binary data must be thirty-six less than that of the most significant word.

ROUND OPTION AND OPERAND SIZE

The N digit of the Operation Half Word is used to specify whether or not a result is to be rounded. In addition, it is used to specify whether operands are single or double precision. The use of the N digit for these purposes is indicated in the following chart:

N Digit	Option Selected
0	Result not rounded; Operands single precision
1	Result not rounded; Operands double precision
4	Result rounded; Operands single precision
5	Result rounded; Operands double precision

The following chart summarizes the pertinent characteristics of the Model 604 Floating Point Arithmetic instructions:

Floating Point Arithmetic Operations

	Add or Subtract	Multiply	Multiply & Accumulate	Divide
Decimal	Yes, 4-bit only	Yes 4-bit only	Yes 4-bit only	Yes 4-bit only
Binary	Yes	Yes	Yes	Yes
Operand Size	Single or double precision	Single or double precision	Single or double precision	Single precision divisor; single or double precision dividend
Result Size	1 word in single precision 1 word in double precision if round option chosen; 2 words in double precision if round option not chosen.	1 word in single precision if round option is chosen 2 words otherwise	1 word in single precision if round option is chosen 2 words otherwise.	1 word quotient; (and 1 word remainder if round option not chosen)
Operands signed or unsigned	Signed only	Signed only	Signed only	Signed only
Operation algebraic or absolute	Either, depending on P digit	Either, depending on P digit	Either, depending on P digit	Either, depending on P digit.
Indicators Set	PRI's (and TCC if PRZ is set) Overflow Underflow Subsidiary Underflow	PRI's (and TCC if PRZ is set) Overflow Subsidiary Overflow Underflow Subsidiary Underflow	PRI's (and TCC if PRZ set) Overflow Subsidiary Overflow Underflow Subsidiary Underflow	PRI's (and TCC if PRZ is set) ZDI Overflow Underflow Subsidiary Underflow
Execution Time** (Decimal or Binary)	Single Precision: 4 μs (includes 1 shift) Double Precision: 10 μs	Single Precision: 10 μs Double Precision 40 μs	Single Precision: 15 μs Double Precision: 50 μs	Single Precision 25 μs Double Precision 25 μs

** Execution times include the memory access of one operand. For each additional operand memory access add 1.5 μs.

FLOATING ADD, DECIMAL OR BINARY

GENERAL DESCRIPTION

This instruction performs decimal (or binary) floating point addition in accordance with algebraic rules or with absolute rules as specified by the P digit of the Operation Half Word. It performs single precision addition (one word plus one word) or double precision addition (two words plus two words) as specified by the N digit of the Operation Half Word. At the conclusion of the operation the normalized result appears in the accumulator (MWA for a single precision result; MWA and LWA for a double precision result) and may also be stored in HSM (if the M digit of the Operation Half Word so indicates).

OPERATION HALF WORD

OO = 50 for Floating Add Decimal: 52 for Floating Add Binary

D = Standard

P = Absolute Control Digit

M = Accumulator Addressing Digit

N = Round/Operand Size Option

A = 7 (If no addresses are assumed)

C = 0

ADDRESSES

A = Address of least significant word of augend

B = Address of least significant word of addend

C = Address of least significant word of sum

OUTLINE OF OPERATION

The characteristics of the most significant words of the two operands are compared. The mantissa of the operand having the smaller characteristic is shifted to the right k places, where k is the difference between the characteristics. The mantissas are then added. The larger operand characteristic is assigned to the result. The result is then normalized by shifting the mantissa to the left one position for each leading zero it contains, and subtracting one from the characteristic for each position shifted. If the characteristic of the most significant word of the result becomes less than zero during this process, the Underflow Indicator is set, the characteristic becomes 00 for decimal, or $(000)_8$ for binary, and the process continues. The same is true of the least significant word, except that the Subsidiary Underflow

Indicator is set in this case. If the round option is chosen, the result is rounded to one word and renormalized. If N = 1, nine for decimal, or 36 for binary, is subtracted from the characteristic of the most significant word of the result. This number is placed into the characteristic portion of the least significant word of the result and both words are stored in HSM (if the M digit so indicates). In the case of overflow (characteristic greater than 99 for decimal or $(777)_8$ for binary) the Overflow Indicator is set and the characteristic of the result is set to 99 for decimal, or $(777)_8$ for binary.

FINAL REGISTER CONTENTS

$A_f = A_i$ - n words

$B_f = B_i$ - n words

$$C_f = \begin{cases} C_i - 1 \text{ word if round option chosen.} \\ C_i - n \text{ words otherwise} \end{cases}$$

Where n = Number of words in an operand.

If the accumulator is specified as an operand the corresponding address register is not altered.

INDICATORS SET

PRI's (and TCC if PRZ is set)

Overflow

Underflow

Subsidiary Underflow

ACCUMULATORS AFFECTED

MWA, LWA

FLOATING SUBTRACT, DECIMAL OR BINARY

GENERAL DESCRIPTION

This instruction performs decimal (or binary) floating point subtraction in accordance with algebraic rules or with absolute rules as specified by the P digit of the Operation Half Word. It performs single precision subtraction (one word minus one word) or double precision subtraction (two words minus two words) as specified by the N digit of the Operation Half Word. At the conclusion of the operation the normalized result appears in the accumulator (MWA for a single precision result; MWA and LWA for a double precision result) and may also be stored in HSM (if the M digit of the Operation Half Word so indicates).

OPERATION HALF WORD

OO = 51 for Floating Subtract Decimal; 53 for Floating Subtract Binary

D = Standard

P = Absolute Control Digit

M = Accumulator Addressing Digit

N = Round/Operand Size Option

A = 7 (if no addresses are assumed)

C = 0

ADDRESSES

A = Address of least significant word of minuend

B = Address of least significant word of subtrahend

C = Address of least significant word of difference

OUTLINE OF OPERATION

The characteristics of the most significant words of the operands are compared. The mantissa of the operand having the smaller characteristic is initialized by shifitng it to the right k places, where k is the difference between the characteristics. The mantissas are then subtracted. The larger operand characteristic is assigned to the result. The result is normalized by shifting the mantissa to the left one position for each leading zero it contains, and subtracting one from the characteristic for each position shifted. If the characteristic of the most significant word of the result becomes less than zero during this process the Underflow Indicator is set, the characteristic becomes 00 for decimal, or $(000)_8$ for binary, and the process continues. The same is true of the least significant word, except that the Subsidiary

Underflow Indicator is set in this case. If the round option is chosen, the result is rounded to one word and renormalized. If N = 1, nine for decimal, or 36 for binary, is subtracted from the characteristic of the most significant word of the result. This number is inserted into the characteristic portion of the least significant word of the result and both words are stored in HSM (if the M digit so indicates). In the case of overflow (characteristic greater than 99 for decimal or $(777)_8$ for binary) the Overflow Indicator is set and the characteristic of the result is set to 99 for decimal, or $(777)_8$ for binary.

FINAL REGISTER CONTENTS

$A_f = A_i$ - n words

$B_f = B_i$ - n words

$$C_f = \begin{cases} C_i \text{ - 1 word if round option chosen.} \\ C_i \text{ - n words otherwise} \end{cases}$$

where n = number of words in operand.

If the accumulator is specified as an operand the corresponding address register is not altered.

INDICATORS SET

PRI's (and TCC if PRZ is set)

Underflow

Subsidiary Underflow

Overflow

ACCUMULATORS AFFECTED

MWA, LWA

FLOATING MULTIPLY, DECIMAL OR BINARY

GENERAL DESCRIPTION

This instruction performs decimal (or binary) floating point multiplication in accordance with algebraic rules or with absolute rules as specified by the P digit of the Operation Half Word. It performs single precision multiplication (one word multiplied by one word) or double precision multiplication (two words multiplied by two words) as specified by the N digit of the Operation Half Word. At the conclusion of the operation the normalized result appears in the accumulator (MWA for a single precision result; MWA and LWA for a double precision result) and may also be stored in HSM (if the M digit of the Operation Half Word so indicates). The result is always two words in length. (If N = 1, or 5, the result is rounded to two words). If N = 4, the result is rounded to one word.

OPERATION HALF WORD

OO = 70 for Floating Multiply Decimal; 74 for Floating Multiply Binary

D = Standard

P = Absolute Control Digit

M = Accumulator Addressing Digit

N = Round/Operand Size Option

A = 7 (If no addresses are assumed)

C = 0

ADDRESSES

A = Address of least significant word of multiplicand

B = Address of least significant word of multiplier

C = Address of least significant word of product

OUTLINE OF OPERATION

The characteristics of the most significant words of the operands are added. Fifty for decimal, or 256 for binary, is subtracted from this number to give the characteristic of the result. The mantissas are then multiplied to form the mantissa of the result. This number is then normalized by shifting it to the left one position for each leading zero it contains, and subtracting one from the characteristic for each position shifted. If N = 4, the result is rounded to one word and renormalized. If N = 1 or 5, the result is rounded to two words. In the case of a two word result, nine for decimal, or 36 for binary, is subtracted from the characteristic of the most

significant word of the result and this number placed into the characteristic portion of the least significant word of the result.

FINAL REGISTER CONTENTS

$A_f = A_i$ - n words

$B_f = B_i$ - n words

$$C_f = \begin{cases} C_i \text{ - 1 word if N = 4.} \\ C_i \text{ - 2 words otherwise} \end{cases}$$

where n = Number of words in operand.

If the accumulator is specified as an operand, the corresponding address register is not altered.

INDICATORS SET

PRI's (and TCC if PRZ is set)

Overflow

Subsidiary Overflow

Underflow

Subsidiary Underflow

ACCUMULATORS AFFECTED

MWA, LWA

FLOATING MULTIPLY AND ACCUMULATE, DECIMAL OR BINARY

GENERAL DESCRIPTION

This instruction performs decimal (or binary) floating point multiplication of two operands and addition of the product to the initial contents of the field specified by the C address. The final normalized result appears in the accumulator (MWA for a single precision result; MWA and LWA for a double precision result) and may also be stored in HSM (if the M digit of the Operation Half Word so indicates). Algebraic or absolute rules are followed throughout, as specified by the P digit of the Operation Half Word. The final result is either one or two words in length depending upon the N digit of the Operation Half Word. Rounding takes place after the multiplication phase of the operation. The multiplication and addition may both be either single precision (one word by one word) or double precision (two words by two words), as specified by the N digit of the Operation Half Word.

OPERATION HALF WORD

OO = 76 for Floating Multiply & Accumulate Decimal; 77 for Floating Multiply & Accumulate Binary

D = Standard

P = Absolute Control Digit

M = Accumulator Addressing Digit

N = Round/Operand Size Option

A = 7 (If no addresses are assumed)

C = 0

ADDRESSES

A = Address of least significant word of multiplicand

B = Address of least significant word of multiplier

C = Address of least significant word of final result.

OUTLINE OF OPERATION

This instruction operates as a Floating Multiply of the operands, followed by a Floating Add of the product to the contents of the field specified by the C address (or to the original contents of the accumulator if the M digit of the Operation Half Word so specifies). The product is formed in the accumulator and is rounded if N = 4. The quantity to which this product is then added must of course be equal in number of words to the product after rounding. If this quantity is two words in length, the signs of both words must agree; otherwise, the sign of the most significant word is used.

FINAL REGISTER CONTENTS

$A_f = A_i$ - n words

$B_f = B_i$ - n words

$$C_f = \begin{cases} C_i \text{ - 1 word if N = 4} \\ C_i \text{ - 2 words otherwise} \end{cases}$$

where n = Number of words in operand.

If the accumulator is specified as an operand, the corresponding address register is not altered.

INDICATORS SET

PRI's (and TCC if PRZ is set)

Overflow

Subsidiary Overflow

Underflow

Subsidiary Underflow

ACCUMULATORS AFFECTED

MWA, LWA

FLOATING DIVIDE, DECIMAL OR BINARY

GENERAL DESCRIPTION

This instruction performs decimal (or binary) floating point division of one word by one word, or two words by one word, as specified by the N digit of the Operation Half Word. In either case the quotient is one word in length, and appears in the Most Significant Word Accumulator (and may be stored in HSM if the M digit of the Operation Half Word so specifies). The remainder appears in the Least Significant Word Accumulator. Albegraic or absolute rules are followed as specified by the P digit of the Operation Half Word.

OPERATION HALF WORD

OO = 71 for Floating Divide Decimal; 75 for Floating Divide Binary

D = Standard

P = Absolute Control Digit

M = Accumulator Addressing Digit

N = Round/Dividend Size Option

A = 7 (If no addresses are assumed)

C = 0

ADDRESSES

A = Address of least significant word of dividend.

B = Word address of divisor.

C = Word address of quotient.

OUTLINE OF OPERATION

The characteristic of the divisor is subtracted from the characteristic of the most significant word of the dividend. Fifty for decimal, or 256 for binary, is added to this difference to form the characteristic of the result. The mantissas are then divided to form the one word quotient and the one word remainder. If the divisor is zero, the Zero Divisor Indicator is set and the instruction terminates. If not, the quotient appears in the Most Significant Word Accumulator (and may be stored in HSM if the M digit so specifies) and the remainder in the Least Significant Word Accumulator. (It is not stored in HSM by this instruction but this may be accomplished by a Store Data Register instruction). If the round option is chosen and the remainder is greater than or equal to half the divisor, one is added to the quotient and the remainder is destroyed. The Overflow Indicator is set if the characteristic of the quotient exceeds 99 for decimal, or $(777)_8$ for binary, in which case the characteristic is set to 99 for decimal, or $(777)_8$ for binary.

The Underflow Indicator is set if the characteristic of the quotient becomes less than zero, in which case the characteristic is set to zero.

The Subsidiary Underflow Indicator is set if the characteristic of the remainder becomes less than zero, in which case the characteristic is set to zero.

FINAL REGISTER CONTENTS

$A_f = A_i$ - n words, where n is the number of words in the dividend.

$B_f = B_i$ - 1 word

$C_f = C_i$ - 1 word

If the accumulator is specified as an operand, the corresponding address register is not altered.

INDICATORS SET

PRI's (and TCC if PRZ is set)

ZDI

Overflow

Underflow

Subsidiary Underflow

ACCUMULATORS AFFECTED

MWA, LWA