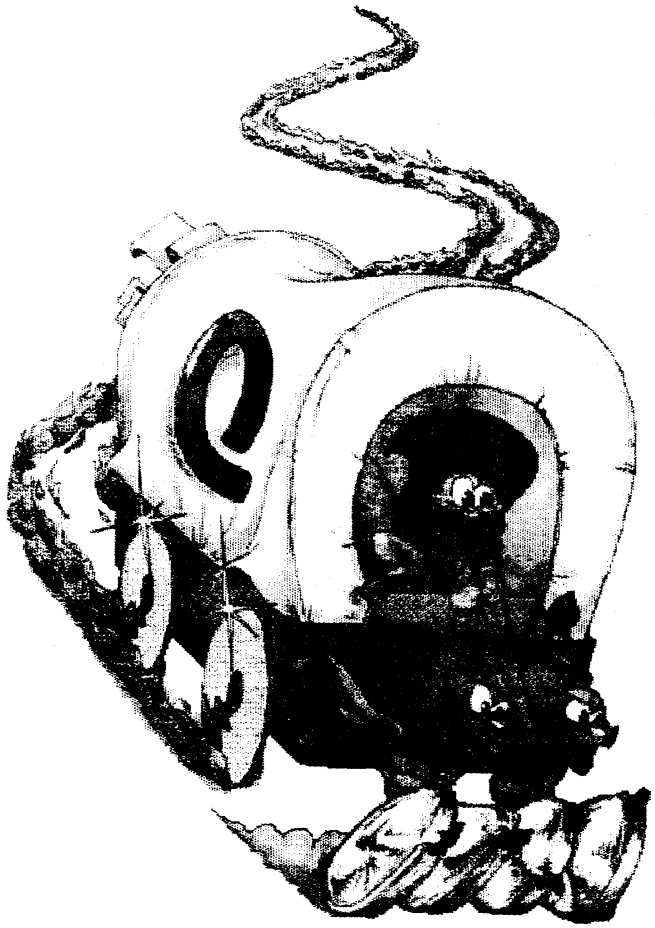
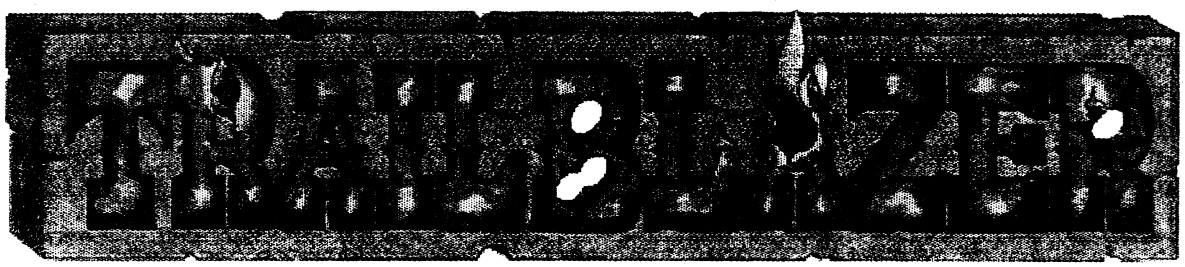




Trailblazer Product Training

Tuesday February 28, 1995

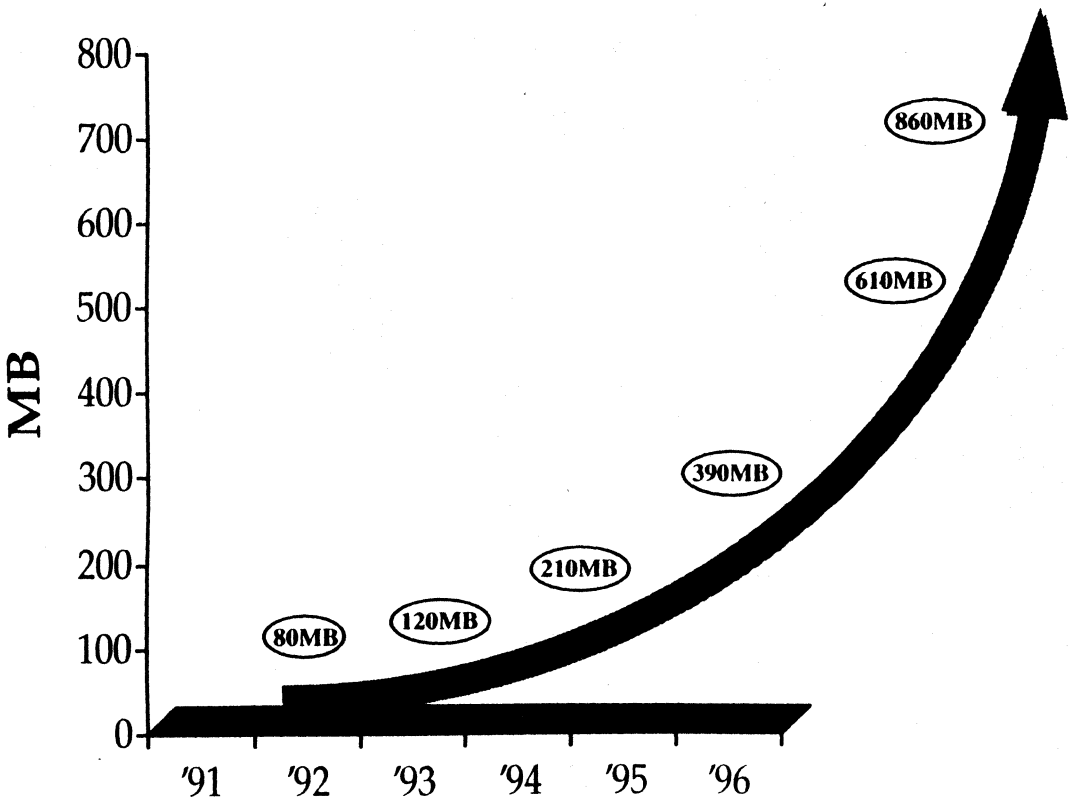
Quantum Confidential

TABLE OF CONTENTS

Agenda

- Market Trends
- Quantum Roadmap
- Program Overview
- Transition Plan
- Production Ramp
- Schedule Update

The average hard drive capacity continues to grow at a sustained 60% annual growth rate



Future growth spurred by:

- rapid migration of most markets to advanced processor/ multimedia systems
- increased storage requirements of O/Ss, applications and the number of software titles per system
- trend to a "Digitized World"
  - access to new media
  - more paths for data into the PC

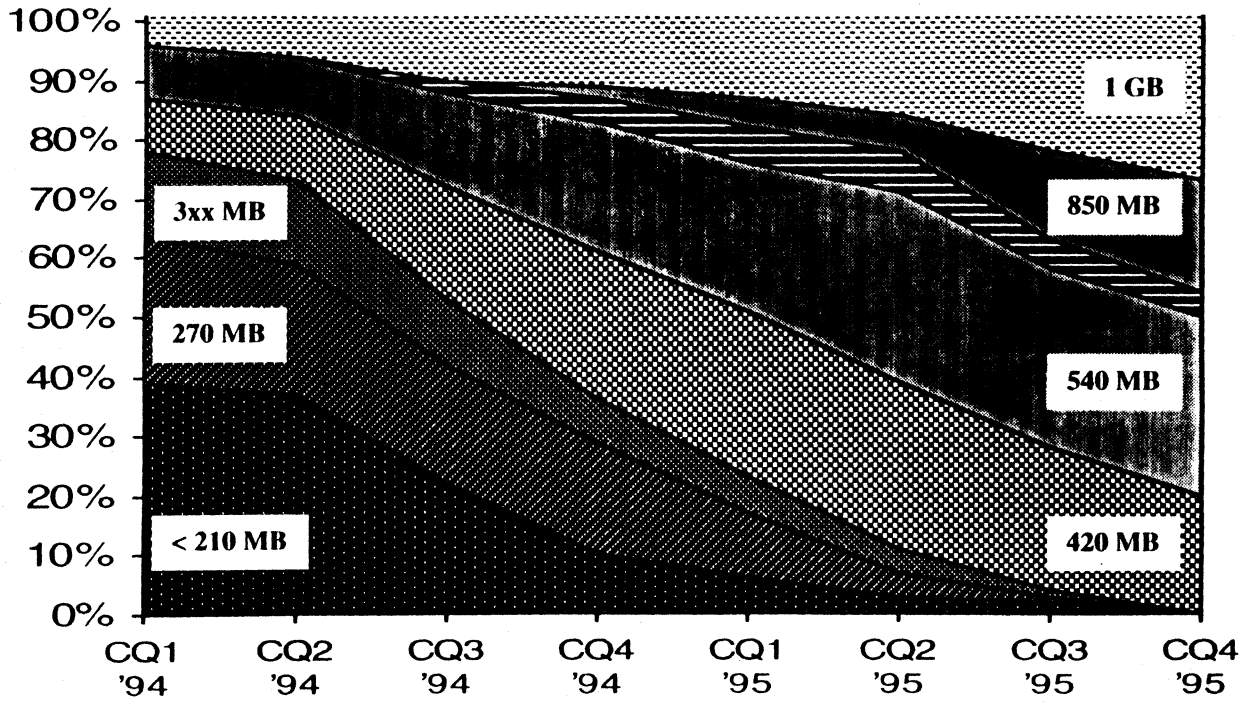
Source: Dataquest

Desktop Capacity Trends

Strong PC demand for advanced systems is driving a dramatic shift upward in 1995 desktop capacities

- 420 and 540 MB for entry level systems
- 635 MB capacity to be used as differentiator by leading OEMs
- 850 MB and 1 GB for mid-range and performance systems

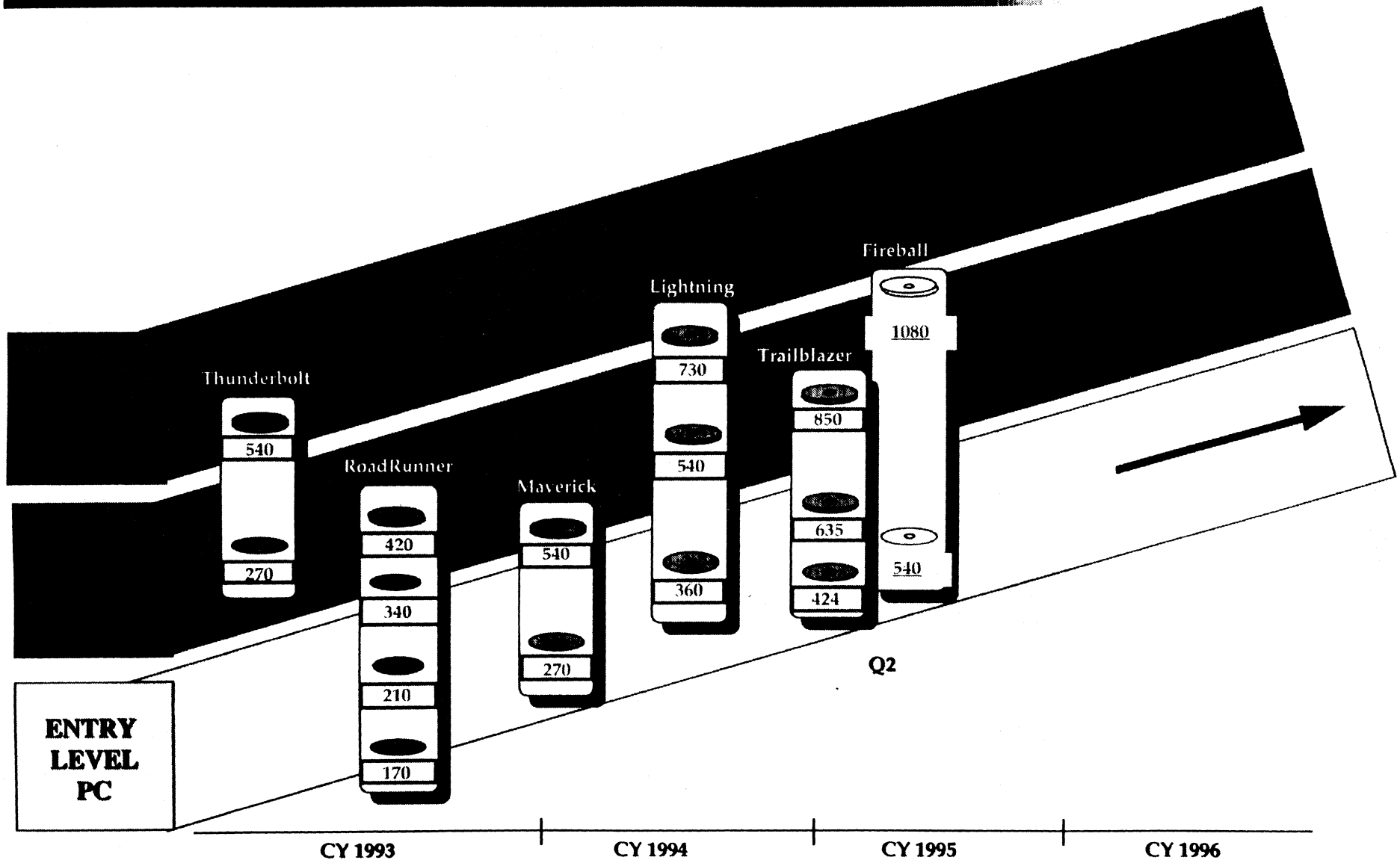
Desktop HDD Capacity Trends



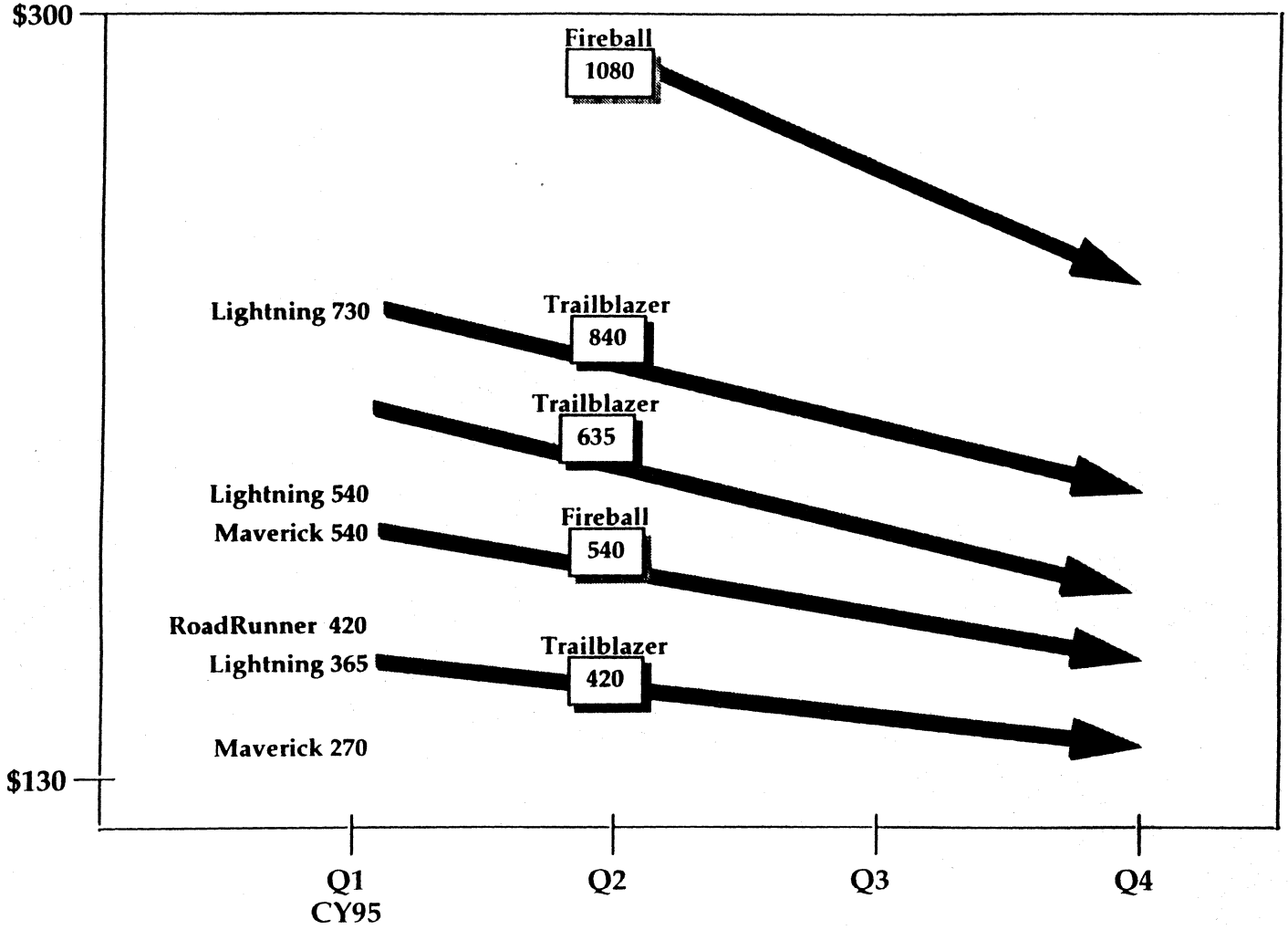
Source: IDC HDD Industry Model

Product Roadmap

Trailblazer 420/635/850



Price Point Transitions



Marketing Objectives

- **Aggressively grow share at key market capacity points: 420/635/850 MB**
  - Maintain position with RR 420 and LT 730 in CQ1 and early CQ2 until Trailblazer available
  - Lead market in emerging 635 MB capacity point with TR 635
- **Sell Trailblazer 420MB staying power at entry level throughout 1995, and Trailblazer 850MB as the critical capacity point between 540MB and 1GB**
- **Get customers qualified in preparation for fast ramp in CQ2**
  - P2.5 evals available mid-March
  - PMP evals available mid-April

Program Overview

Trailblazer 420/635/850

Product Concept

- Low cost, value products targeted toward entry-level PC market in CY '95 and early '96
- Three capacities allow coverage of the entry-level and mainstream multimedia PC markets through program life

Key Attributes

- Revolutionary mechanical design
- Highest value 420/635 /850 MB drives available in CY '95
- Feature set matched to entry-level market segment
- Quantum quality with fast production ramp

Product Specifications

- Capacity 420/635/850 MB
- Seek Time 14 ms
- RPM 4500
- Buffer 128 KB
- MiG Heads
- Firmware : Enhanced Roadrunner and Maverick
- Interface: AT and SCSI

Target Applications

- Small Office and Home Office (SOHO), Entry-level business systems
- Windows(95), OS/2, and Macintosh operating systems, word processing, spreadsheets, database, and edutainment apps.

Product Availability

- Eval Units March/April '95
- Volume Availability May/June '95

Design Leverage

Trailblazer 420/635/850

Thunderbolt/Roadrunner

- NEC Microprocessor
- Integrated Read Channel
- Integrated, hall-less motors
- Embedded servo format
- Buffer controller & sequencer
- SCSI Interface

Roadrunner

- Firmware
- Actuator voice coil design
- Balanced Airlock

Lightning

- SCSI Plug-and-Play

New Technology

- Mechanics
- AT interface
- Combo chip (VCM, motor & POR)
- Pre-amp, Read Channel
- Firmware : Multiple AutoRead/ AutoWrite, Double-burst ECC on-the-fly

Trailblazer 420/635/850

Product Comparisons

Trailblazer 420/635/850

Design Elecments	Trailblazer	Roadrunner/Maverick
Cost	▪ Stamped Al. Base ▪ Mig Heads ▪ Integrated Motor & Controller	▪ Cast Base ▪ Thin Film Heads ▪ Separate VCM, Controller
Performance	▪ PIO Mode 4 ▪ DMA Mode 2 ▪ 54 Mb/s Read Channel ▪ Multiple AutoRead/ AutoWrite ▪ Enhanced Adap. Seg. ▪ 48 bit ECC On The Fly ▪ Dual Top Cover	▪ PIO Mode 2 ▪ DMA Mode 1 ▪ 36 Mb/s Read Channel ▪ AutoRead, AutoWrite ▪ Adaptive Segmentation ▪ 24 bit ECC On The Fly ▪ Single Top Cover
Reliability	▪ Advanced Drive Diag. ▪ 5 ICs	▪ Self Diagnostics ▪ 7 + ICs

Product Comparisons

Trailblazer 420/635/850

	RoadRunner	Maverick	Trailblazer
Capacity (MB)	210/420	270/540	**420/635/850**
Interface	AT/SCSI	AT/SCSI	AT/SCSI
Seek Time (ms)	14/12	14	**14**
RPM	3600	3600	**4,500**
Buffer (KB)	128	128	**128**
Data Rate (Mb/sec)	31.5	36	**54**
Transfer Rate (MB/s)			
PIO	11	11	16
DMA	13	13	16
SCSI	6/10	6/10	6/10
Acoustics-Idle (dBA)	32	34	**30 / 3.5 Bels**
Power - Idle (W)	3.3	3.7	**3.3**
-R/W (W)	4.5	5.2	4.5
FCS	CQ4'93	CQ2'94	**CQ2' 95**

Update on Competitor Availability

		Capacities	Evals Avail.	Volume Avail.	Notes
Conner	*Steamboat*	850/1275	Shipping	Low Volume	Steamboat has mfging problems,
	Cabo-2	425/850/1275	Dec. '94	CQ1 '95	Cabo priced low to re-gain share
	La Paz	635/1275	Sept. '95	CQ3/4 '95	La Paz to be led by 3 headed Cabo635
WD	*Sturgeon*	425/850/1275	CQ4 '94	CQ1 '95	Drives in Disti channel and Tier 1 OEMs, New low cost mechanics
Seagate	*Decathlon*	420 ?, 850	CQ4 '94	CQ1 '95	Limited mktg rumored due to high cost structure, Lead qual is AT&T
Maxtor	*Excaliber*	425/850/1275	CQ4 '94	CQ1 '95	Just introduced low cost 7000AV line (135/270/405/540MB)
IBM	*Alladin*	540/1080	CQ4 '94	CQ1 '95	No plan to have 420/840MB

Trailblazer Qual Drive Allocation Matrix

As of 2/16/95

Customer	Feb (P2.0)					March (P2.5)					April (PMP)				
	420 AT	420 S	630 AT	850 AT	850 S	420 AT	420 S	630 AT	850 AT	850 S	420 AT	420 S	630 AT	850 AT	850 S
Compaq	24		24	24		30		30	30		100		100	100	
Apple	8	2		8	2	8	2		8	2	40	40		60	60
Digital						6			6		50			50	
HP				7		5			5		40			40	
Dell						2					30			30	
IBM						10			10		25			25	
AST						4			4		30			30	
Acer						5			5		10			10	
AT&T											20			20	
NA Region	7	2		8	2	7	2		8	2					
Packard Bell											10			10	
Gateway 2000						2			2		10	10		10	10
Leading Edge											12			12	
Intel											10			10	
Micron											5	5		5	5
Mitsuba											2	2		2	2
Comtrade											2	2		2	2
Epson											10			10	
Zenith						2			2		5	5		5	5
Micronet											5			5	
Zeos						2			2		10			10	
APAC Region	7	2		8	2	7	2		8	2					
Daewoo									5					5	
Trigem									5					5	
Goldstar									5					5	
Samsung									7					7	
Leading Edge									5					5	
Lucky Goldstar									5		5			5	
IPC						2			2						
ALR						1			1						
FIC						2			2						
Europe Region	7	2		8	2	7	2		8	2					
Olivetti						15			15		30			30	
SNI						5			5		10	10		5	
Apricot											12			12	
Peacock											2			2	
Escom											2			2	
Vobis														2	
Tulip											2			2	
ICL						2			2		10			10	
Elonex											2			2	
Japan Region						7	2		8	2					
Fujitsu						3	3		3	3	30	30		30	30
NEC											30			30	
LA Region						2	2		2	2	10	10		10	10
Distribution	3	3		3	3	15	14		18	26	20	20		20	20

TOTALS			**P2.0**			**Total**			**P2.5**			**Total**			**PMP**			**Total**
Total Tier 1	32	2	24	39	2		70	2	30	68	2		345	40	100	365	60	
Total NA Region	7	2	0	8	2		11	2	0	12	2		71	24	0	71	24	
Total APAC Region	7	2	0	8	2		7	2	0	40	2		5	0	0	32	0	
Total Japan Region	0	0	0	0	0		10	5	0	11	5		60	30	0	60	30	
Total Europe Region	7	2	0	8	2		29	2	0	30	2		70	10	0	67	0	
Total LA Region							2	2		2	2		10	10		10	10	
Total Qual Drives	56	11	24	66	11	**168**	151	29	30	188	41	**439**	591	134	100	635	144	**1604**
Total Available	58	8	19	77	8	**170**	166	40	38	154	40	**439**	600	200	100	650	200	**1750**

Specifications Update

	Trailblazer 420/635/850	Conner Cabo	Conner Steamboat	Maxtor 7425 / 7850AV	WD 1425 / 2850	Seagate Decathlon
Volume Shipment	Q2 CY95	Q1 CY95	Q1 CY95	Q2 CY95	Q1 CY95	Q1 CY95
Formatted Capacity	424 / 850	425/635/850	850	426 / 853	428/635/856	854
Head Technology	**MiG**	MiG	Thin-film	Thin-film	Thin-film	Thin-film
Interface	**Fast ATA-2 SCSI-2**	Fast ATA	Fast ATA SCSI-2	Fast ATA	Fast ATA	Fast ATA-2
Seek Time	14 ms	< 15ms	12ms	12ms	10ms	11ms
RPM	4500	3600	4500	3551	4500	5400
Buffer	**128K**	64K	256K	64K	64K	256K
Data Rate (Mbits/sec)	55	<50	60.4	43	42	61
Transfer Rate (MB/sec)						
AT PIO:	**Mode 4**	Mode 3	Mode 4	Mode 3	Mode 3	Mode 4
Fast DMA:	Mode 2	Mode 1	Mode 1	Mode 1	Mode 1	Mode 2
SCSI:	6 / 10	--	6 / 10	--	--	--
Acoustics (Idle)	**30dBA (1M)**	34 dBA (1M)	38 dBA (1M)	3.5 Bels	37 dBA (1M)	?
Power (Idle)	3.3W	3.8 / 3.9W	3.9W	3.5 / 3.8W	4.6W	3W
MTBF	300,000	250,000	300,000	300,000	300,000	500,000

Transition Plan

Trailblazer 420/635/850

Objectives

- Ramp aggressively to optimize DPSG gross margin
- Satisfy major OEM qual windows
- Maintain/grow share at Tier 1 and strategic regional accounts
- Maintain flexibility in Distribution to ship either new or old product as needed

Tactics

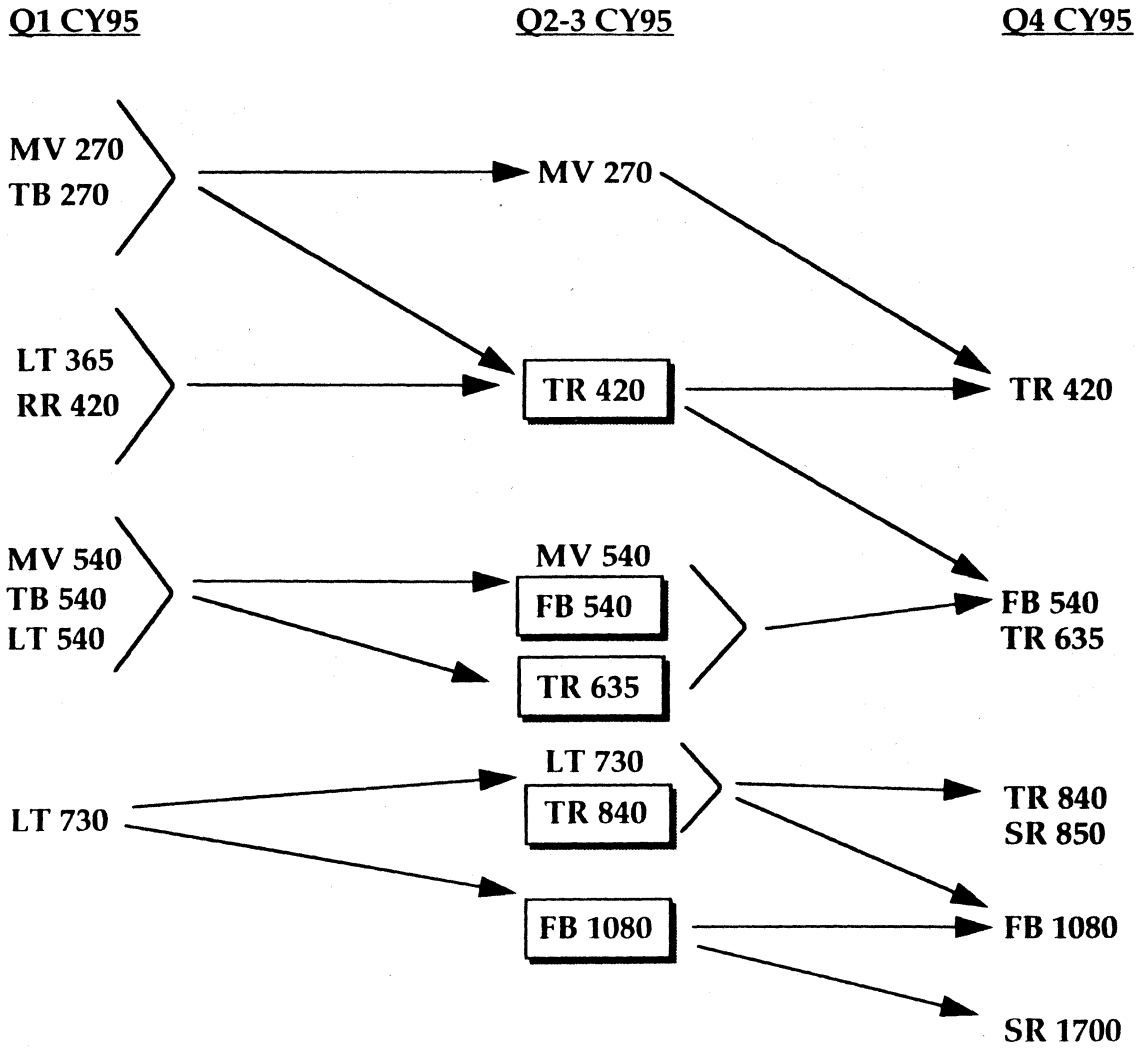
"What we will do differently to be able to transition faster than before"

- Prioritize key OEM accounts for early shipments & qual support
- Develop a strategy with Sales for seeding a limited quantity of "demo drives" (P2) at strategic regional accounts, based on drive maturity
- Start quals with smaller OEMs and regional accounts at PMP even if availability constrained
- Be ready to ship to Distribution at MP

Product Transitions

Trailblazer 420/635/850

Primary Transition Paths



Transition Plan Actions

Trailblazer 420/635/850

Next Steps	Who
Generate customer interest and qual commitments for Fireball & Trailblazer • Product introduction activities • Sales tools/presentation materials • Customer visits	**Field & Marketing**
Develop qual strategies & timelines for all OEM accounts • Feasibility/priority for simultaneous Fireball & Trailblazer quals • Strategies for starting strategic regional OEM quals ealier (P2 vs. PMP evals)	**Field, Account Management, & Regional Marketing**
Begin forecasting new product transitions for all customers • Distribute updated forecast assumptions	**Field**
Update detailed transition plan	**Marketing**
Issue Product Status Reports every two weeks **(via e-mail to sales offices)**	**Marketing**

Customer Priorities

TrailBlazer 420/635/850

Priorities for Evals

Criteria:	Strategic importance Qual windows Volume potential

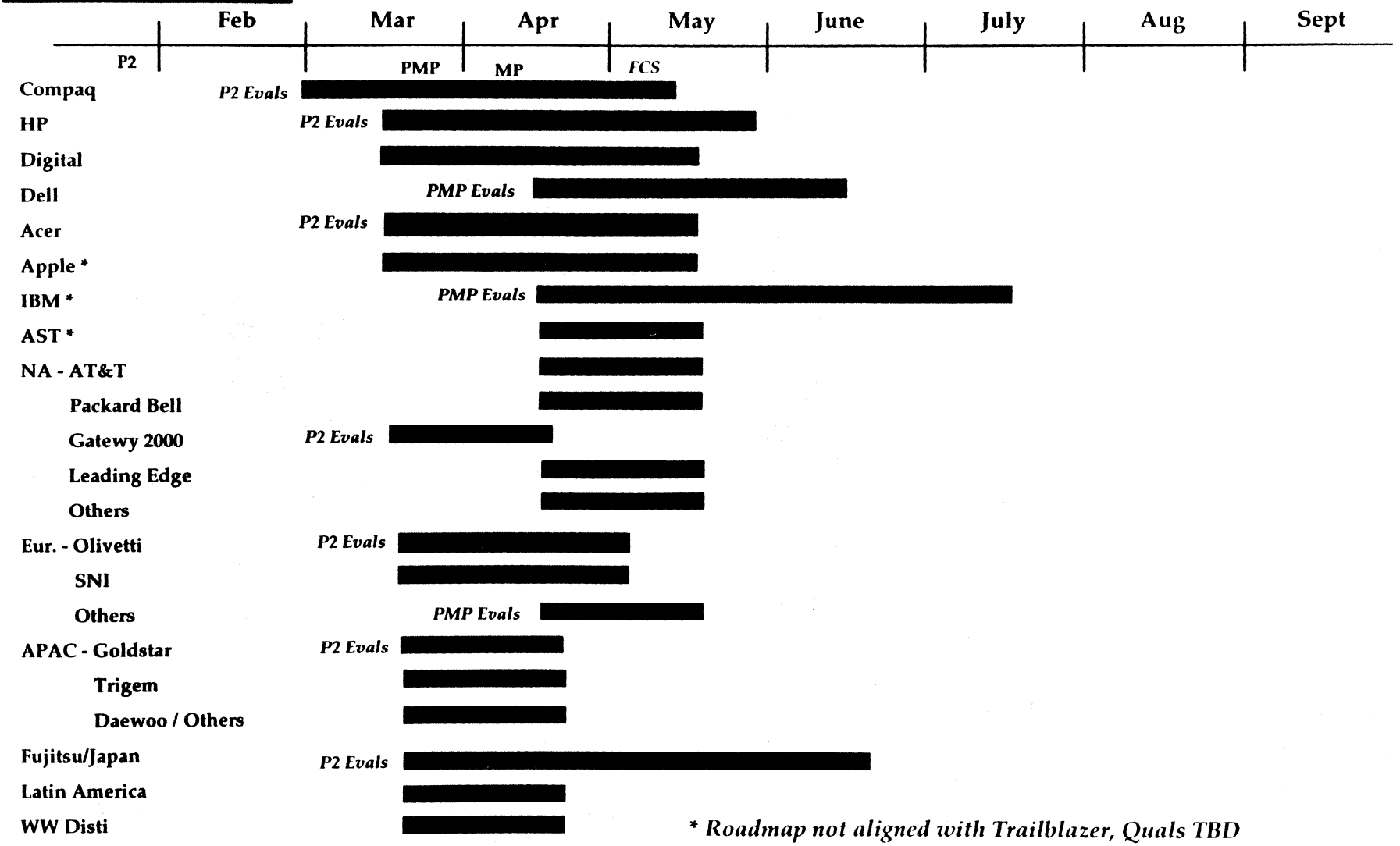
Customer	*TrailBlazer 420/840*
1. **Sponsor/Lead Customer** *(P2 Evals)*	**Compaq** **HP** **Digital** **Apple *** **Olivetti**
2. **Other Tier 1 OEMs** *(PMP Evals)*	**Dell** **Acer** **IBM *** **AST ***
3. **Strategic Regional OEMs** *(P2/PMP Evals)* • *N.A.* • *Europe* • *APAC* • *Japan*	**Gateway 2000, Packard Bell, AT&T** **ICL, SNI, Peacock, Escom, Vobis** **Goldstar, Trigem, FIC, Samsung** **Fujitsu, NEC**
4. **Other OEMs & Disti**	**Leading Edge, Ingram Micro, etc.**

* *Roadmap not aligned with TrailBlazer, Quals TBD*

Trailblazer Transition Plan

Trailblazer 420/635/850

Qual Schedules



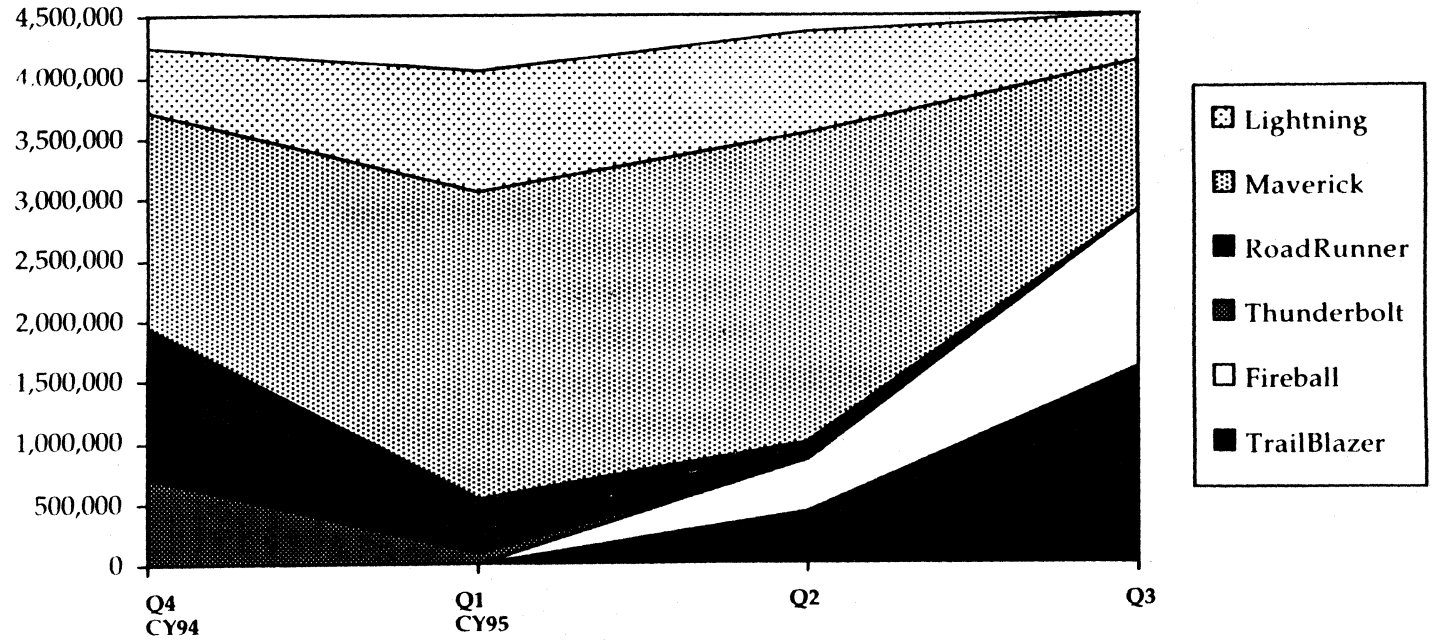
* *Roadmap not aligned with Trailblazer, Quals TBD*

Production Ramp

Trailblazer 420/635/850

New Product Production Ramps:

	Q2	Q3	Q4
Trailblazer	**700K**	**1.6MM**	**1.8 MM**



Transition Plan

Trailblazer 420/635/850

Plans For Meeting Production Ramp: Prelimary FQ1 Forecasts

	Planned		Contingency	
	Customers	*Volume*	*Customers*	*Volume*
Tier One	Compaq HP Digital Dell Olivetti	356K	Compaq HP Digital Olivetti	220K
Reg. Accts.	Acer Goldstar Apricot Peacock Leading Edge	92K	Goldstar Escom Peacock Mitsuba IPC	150K
Distribution		252K		330K
Preliminary FQ1 Forecast		700K		700K

Trailblazer Schedule

Program Status

P2 Results

- 61% Self Scan testing yields
- Scratches on the media found - MKE process issue to be resolved
- Actuator imbalance on TR 850 - fix with minor coil change at PMP
- Minor PCB layout change required - MKE process issue solved

Maturity Testing

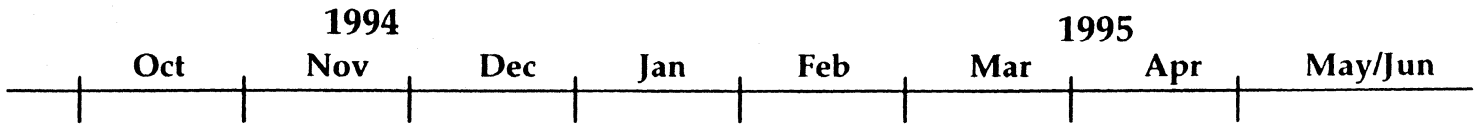
- DVT: Passed Acoustics, 4-corner, & power, Failed Vibration, fix in progress
- Compatibility : Leo V.3 testing passed, accelerated testing with P2 drives

Incremental Design Changes

- P2.5 : ComboV.5, Leo V.3
- PMP
  - Combo roll to V.6 - potential long-term reliability issue at high temperature (125 deg, C)
  - PCB layout change - re-location of discrete components
  - Actuator coil re-design

Trailblazer Schedule

Trailblazer 420/635/850



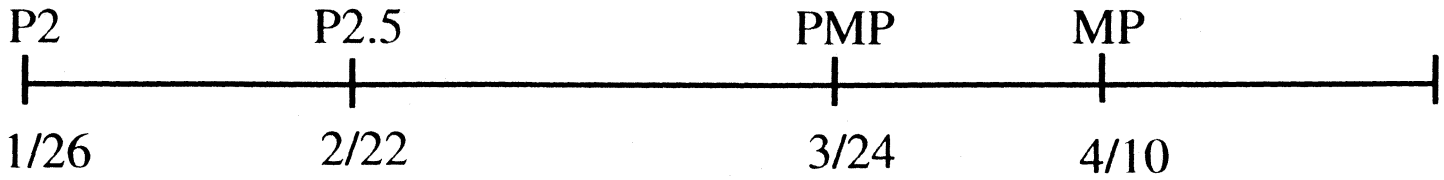
Build Schedule:	P1 Build	P2 Build	Pre Mass Pro	Mass Pro	
Maturity Testing:		DVT Complete	FMT Complete	DMT Complete	PMT
Availability:			Early Evals Avail.	Full Spec Evals Avail.	Volume Availability

Schedule Update

- 1200 drives built at P2.0 with 61% Self Scan yield and 95% Servowriter yield
- P2.5 build commencing on 2/24 : 979 drives with Leo V.3, Combo V.5
- 3000 drives at PMP build with final Combo V.6 and MKE process changes
- DVT testing complete, FMT testing beginning on P2.0 drives
- Compatibility testing on-schedule with all major OEM platforms being tested

Trailblazer Schedule

Build Start



Key Dates

3/5	3/17	4/10	5/8
Ship P2.0 Drives To Customers	Ship P2.5 Drives To Customers	Ship PMP Drives To Customers	Volume Production Available

Schedule Implications

- **Mktg to issue P2.5 & PMP design changes to field**
- **Need to design creative qual strategies by account with P2.5 drives**
- **If Tier One quals slip, quick turn PMP quals must pick up volume**

"Who to Call" Matrix

For Questions On ...	Contact
1. Evaluation Units	Chris Abate
2. Qualifications	Tom Lee
3. Transition/Availability	Chris Abate
4. Pricing	Account Champion
5. Competitive Specs & Benchmarks	Chris Abate
6. Operations and Logistics	Randy Filippuzzi
7. AE Support Issues	Tom Lee
8. Technical Issues	Charlie Helkenn
9. Failure Issues	Tom Lee

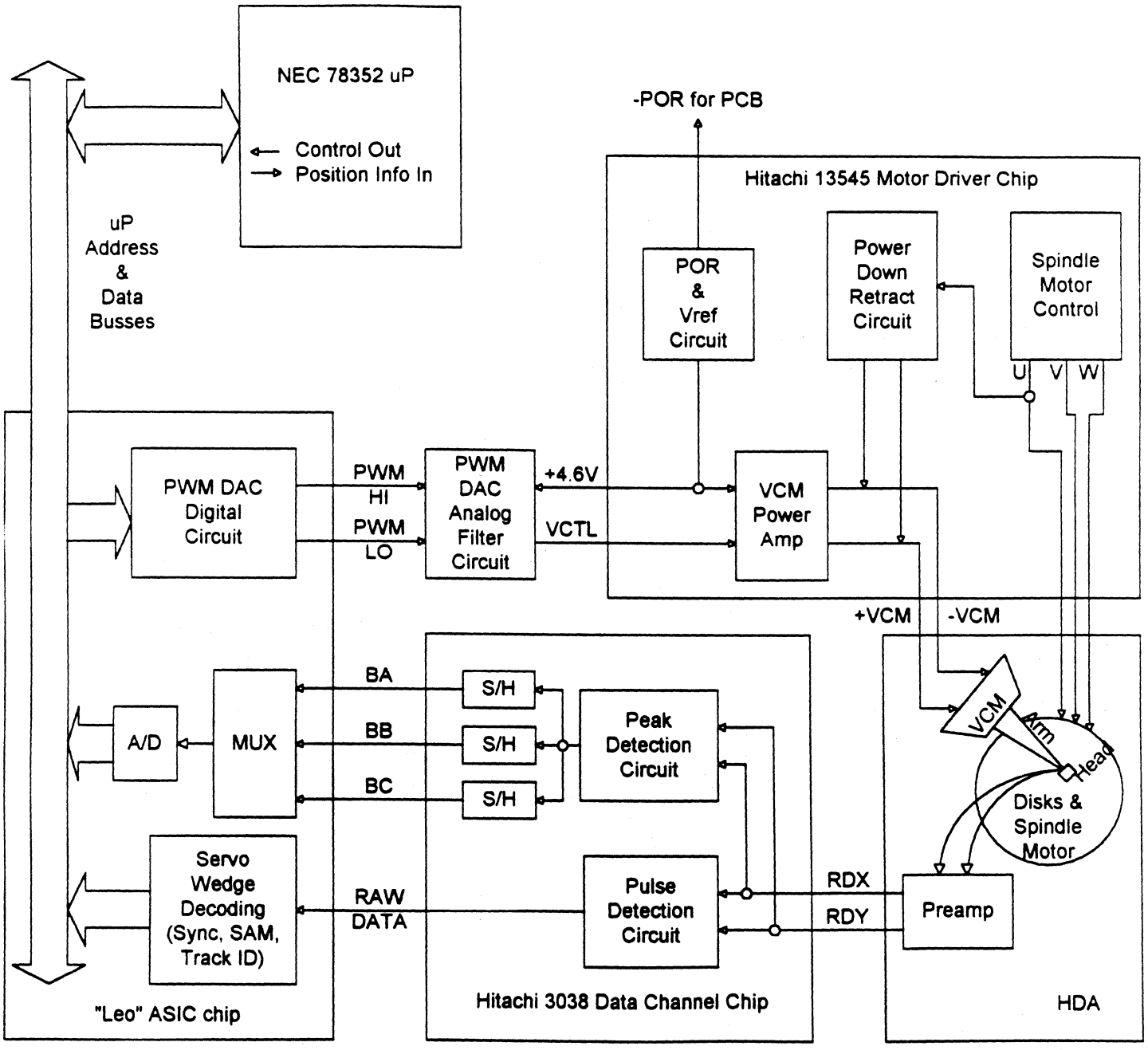
Trailblazer Servo

Trailblazer Product Training

February 28, 1995

Joe Lillig

Trailblazer Servo-Mechanical System: Hardware Block Diagram

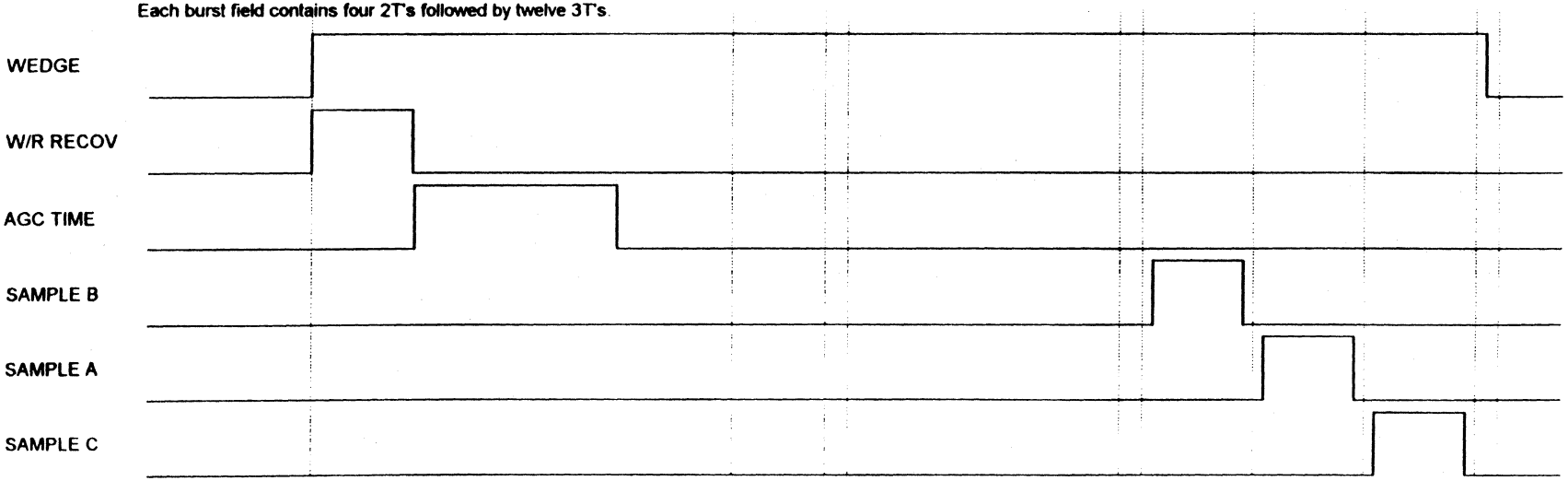


12/7/94 Joe Lillig

TRAILBLAZER SERVO WEDGE FORMAT

T TIME (T = 25 ns)	471T TOTALS	167T	37T	9T	108T	9T	44T	44T	44T	9T	
TIME IN uSEC	11.8 us	4.18 us	.925 us	.225 us	2.7 us	.225 us	1.1 us	1.1 us	1.1 us	.225 us	
FIELD	3T'S	3T'S	SAM	IND	TRACK NUMBER	GAP			C BURST	GAP	TRACK 0
FIELD	3T'S	3T'S	SAM	IND	TRACK NUMBER	GAP	B BURST	A BURST		GAP	TRACK 1
FIELD	3T'S	3T'S	SAM	IND	TRACK NUMBER	GAP			C BURST	GAP	TRACK 2
FIELD	3T'S	3T'S	SAM	IND	TRACK NUMBER	GAP	B BURST	A BURST	C BURST	GAP	TRACK 3

Notes:
3T pattern = 100. Fields filled with 3T's contain 100100100... etc.
Track number is gray coded. Binary to gray code conversion is Gmsb = Bmsb, and Gn = Bn XOR Bn+1. Example: Binary track number 00Ah = Gray code track number 00Fh. The gray code bits are encoded as:
Data bit "0" = disk 10 000 010 0,
Data bit "1" = disk 10 010 000 0.
SAM = Servo Address Mark = 14T pattern repeated 2 times followed by a data bit "0": 10000000000000 10000000000000 10 000 010 0
IND = Index = data bit "1" (10 010 000 0) for sector 0, and data bit "0" (10 000 010 0) for sectors 1 through 62.
Gap = 9T of DC erase = 000000000.
Each burst field contains four 2T's followed by twelve 3T's.



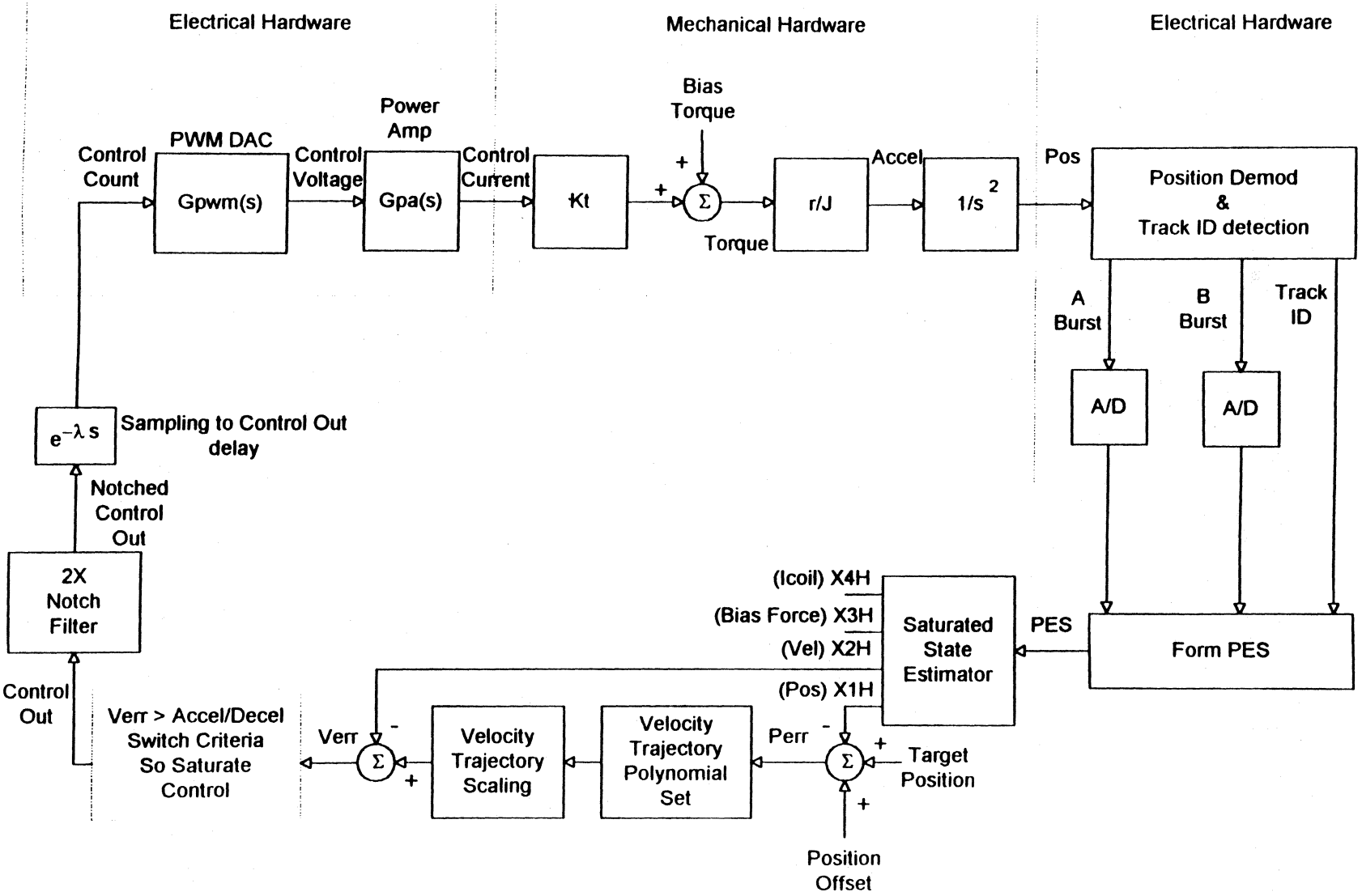
12/9/94 JOE LILLIG

Trailblazer Servo Related Parameters

TPI	3794
Track pitch	264 ui
Number of cylinders	3653
Disk rotation speed	4500 rpm
Servo samples/rev	63
Servo sample freq	4.73 KHz
Servo sample time	212 usec
Servo-mech loop bandwidth	350 Hz

12/9/94 Joe Lillig

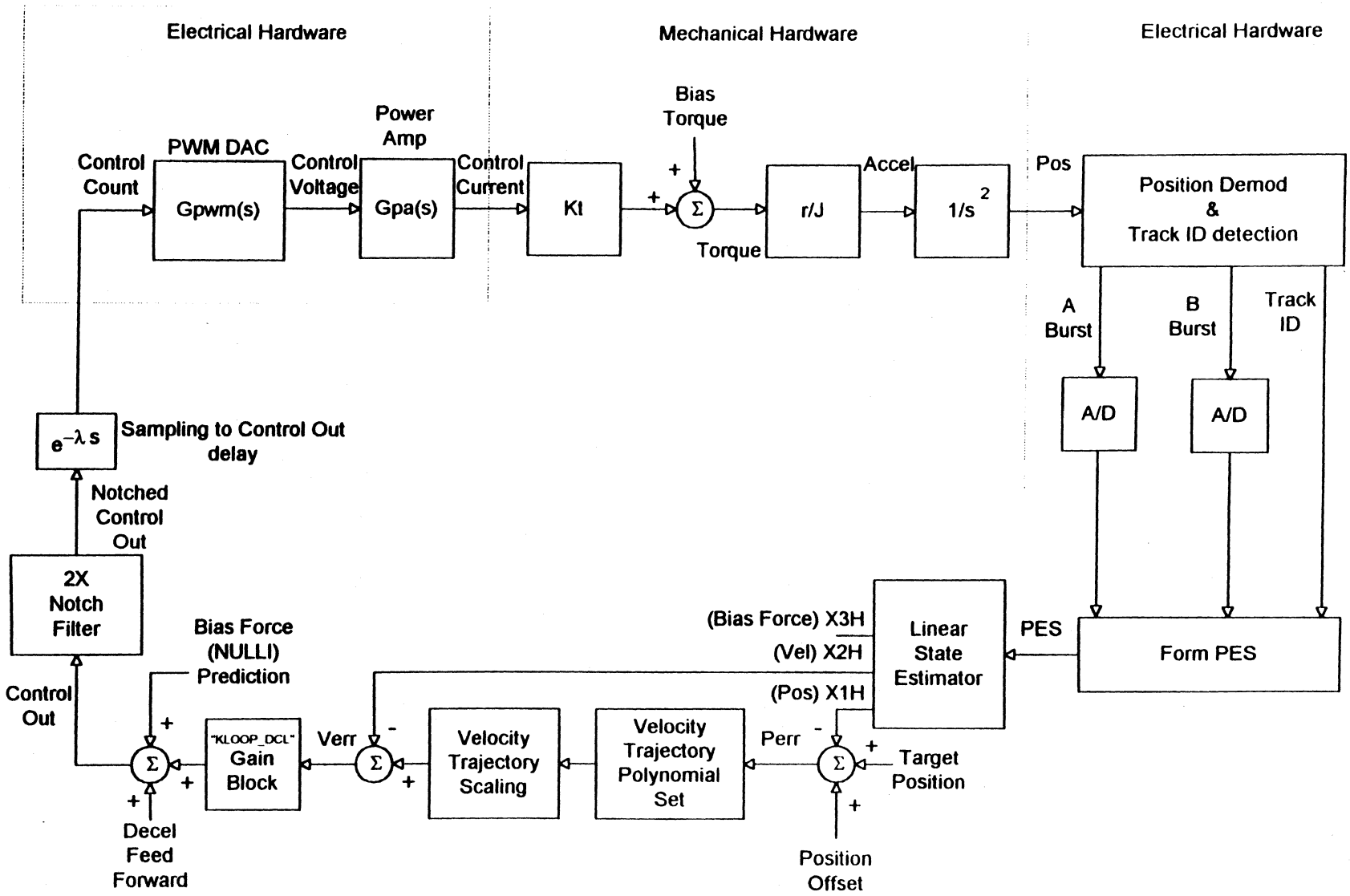
Trailblazer Servo-Mechanical System: "Long" Seek Mode - Acceleration Phase



Switch to Decel mode if Verr < Accel/Decel switch criteria

12/8/94 Joe Lillig

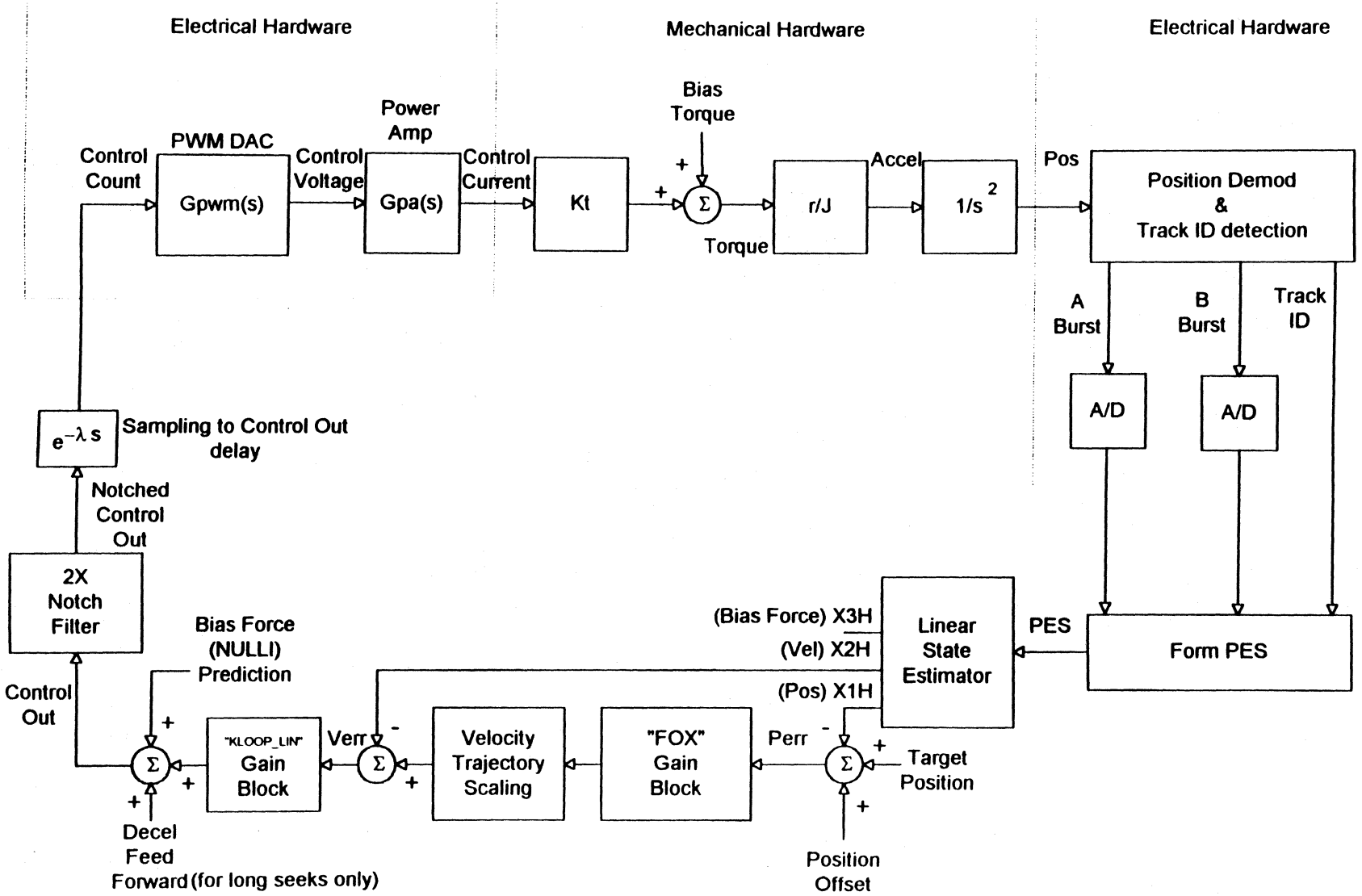
Trailblazer Servo-Mechanical System: "Long" Seek Mode - Deceleration Phase



Switch to Linear Range mode if Perr < Decel/LinearRange switch criteria

12/8/94 Joe Lillig

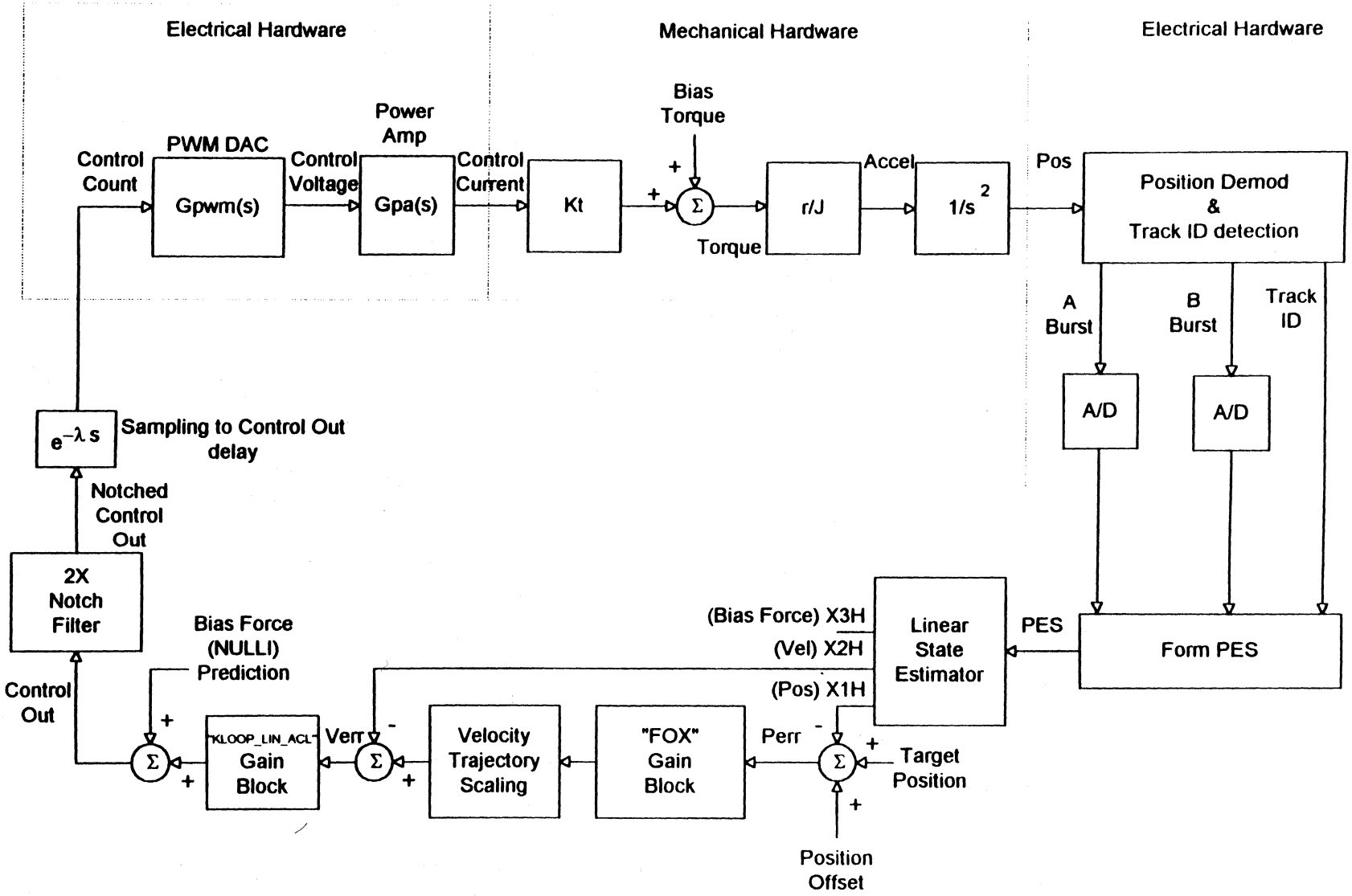
Trailblazer Servo-Mechanical System:
"Linear Range" Seek Mode - Last Mode for Short & Long Seeks



Switch to 1st (AB) settle mode if Perr & X2H are below Seek/Settle switch criteria

12/8/94 Joe Lillig

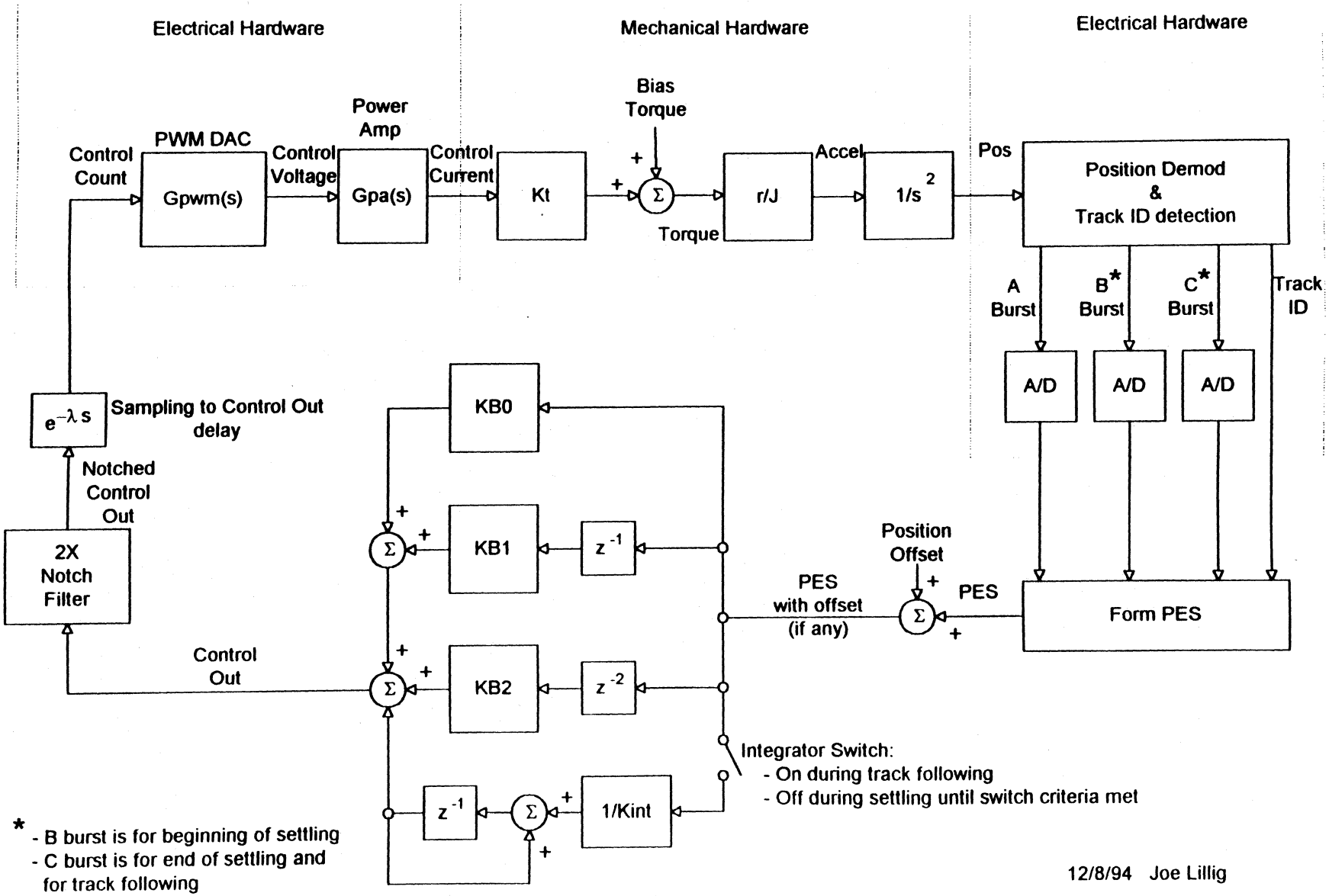
Trailblazer Servo-Mechanical System: "Short" Seek Mode - Acceleration Phase



Switch to Linear Range mode if Verr < ShortAccel/LinearRange switch criteria

12/8/94 Joe Lillig

Trailblazer Servo-Mechanical System: Track Follow & Settle Modes



Trailblazer Servo-mechanical System: Transfer Functions for 420 MB (1 disk) drive

The following 5 pages show open loop transfer functions of the servo-mechanical system for the 420 MB drive

1 Simulation: gain

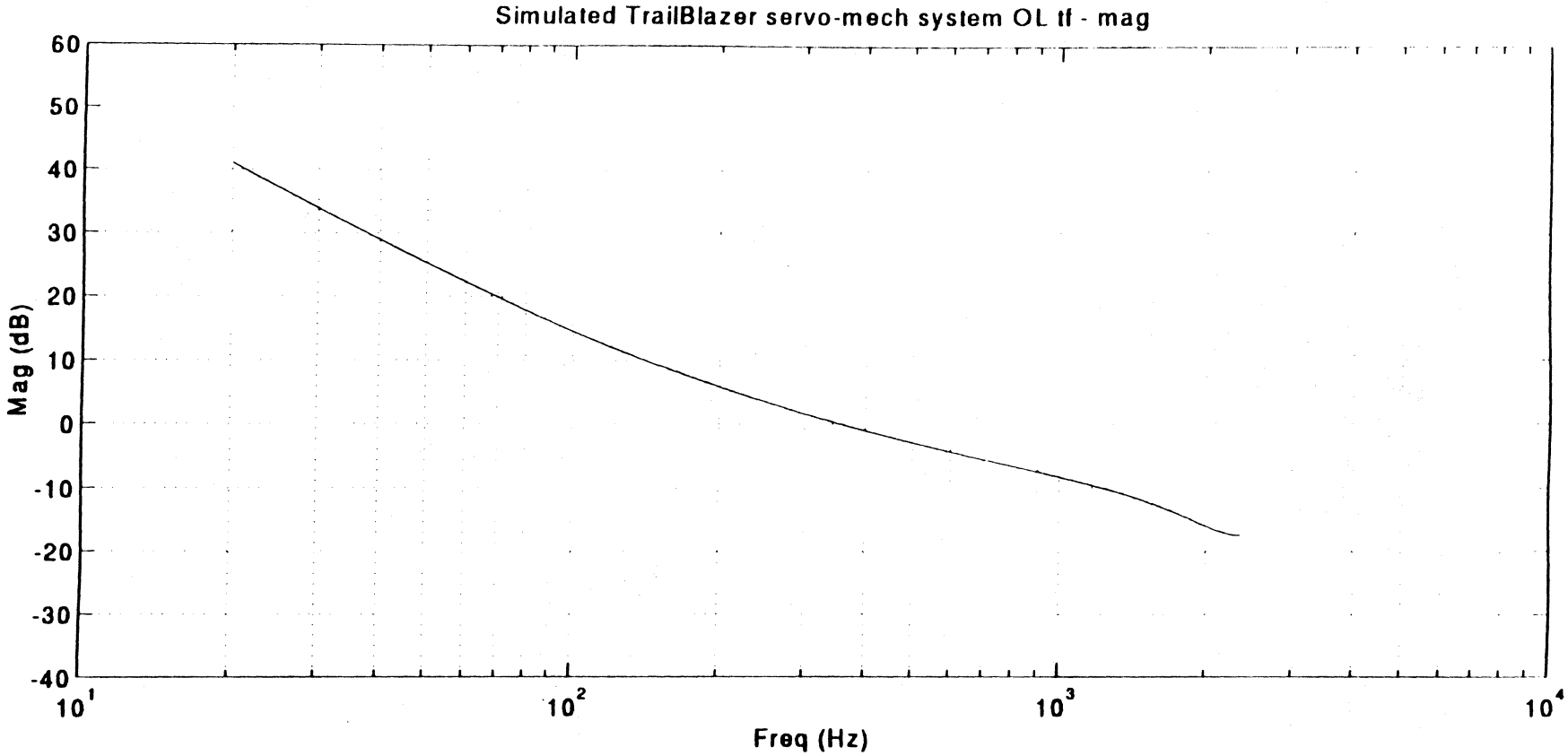
2 Simulation: phase

3 Measured: gain

4 Measured: phase

5 Measured: gain with special 4X sampling rate servo running

12/9/94 Joe Lillig



kb0 = 1.320 (KB0_BY_KLOOP = 0151)

kb1 = -1.492 (KB1_BY_KLOOP= FE83)

kb2 = 0.329 (KB2_BY_KLOOP = 0054)

kint = 768 (KINT = 0300)

Ts = 212 us

Gain crossover freq = 355 Hz

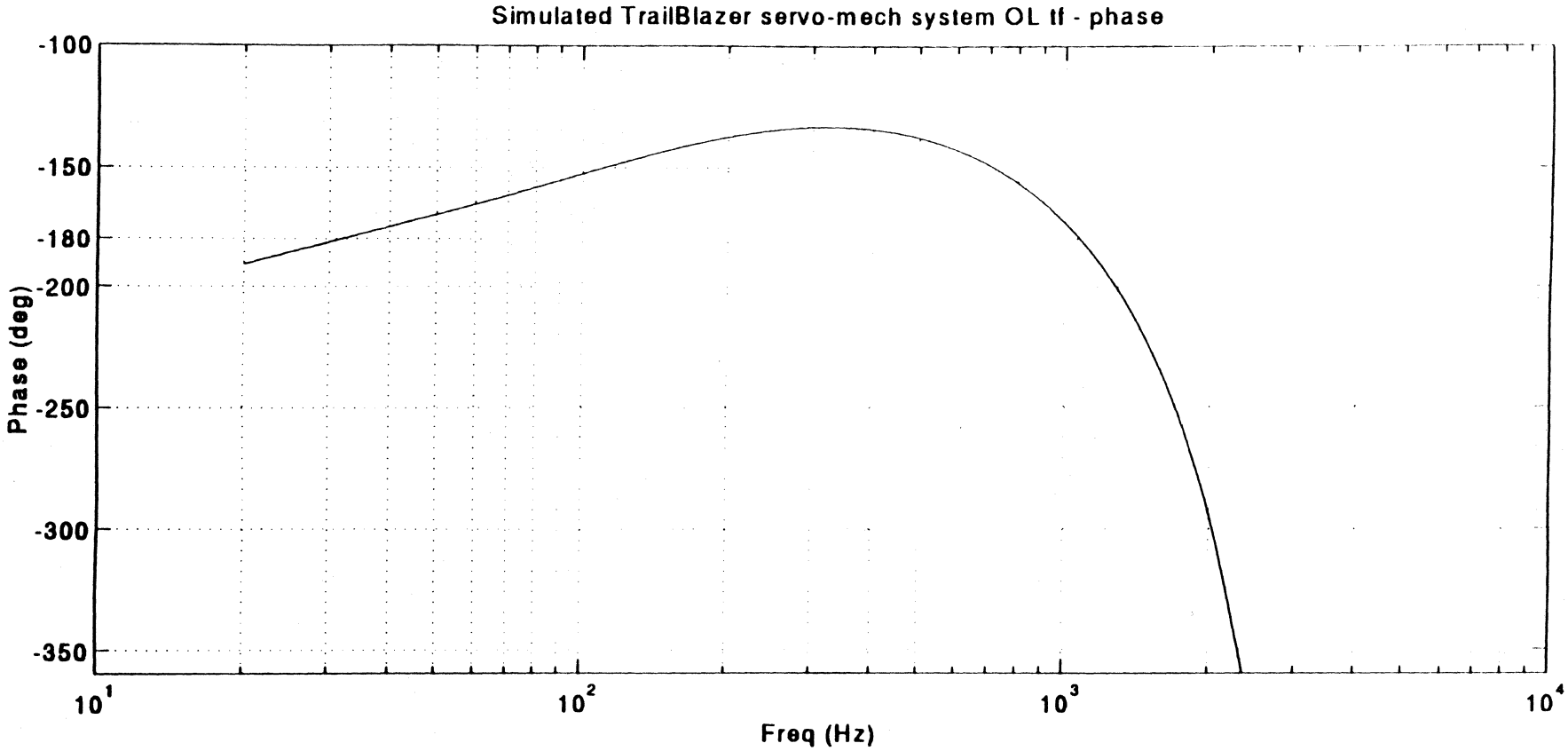
Phase crossover freq = 1071 Hz

Phase margin = 47 deg

Gain margin = 8.8 dB

1 disk, ac coeffs

7-Dec-94 Quanuah Pratt



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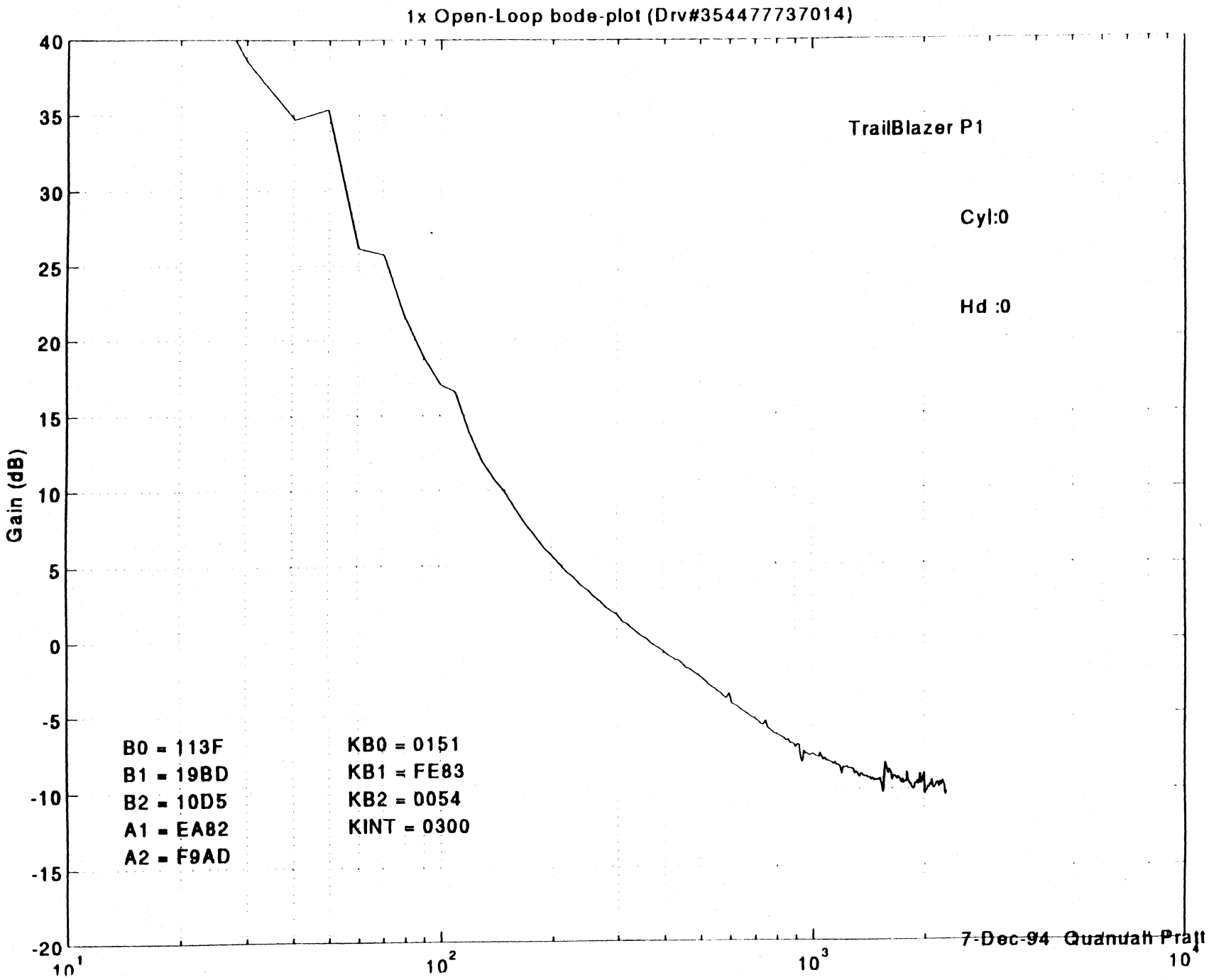
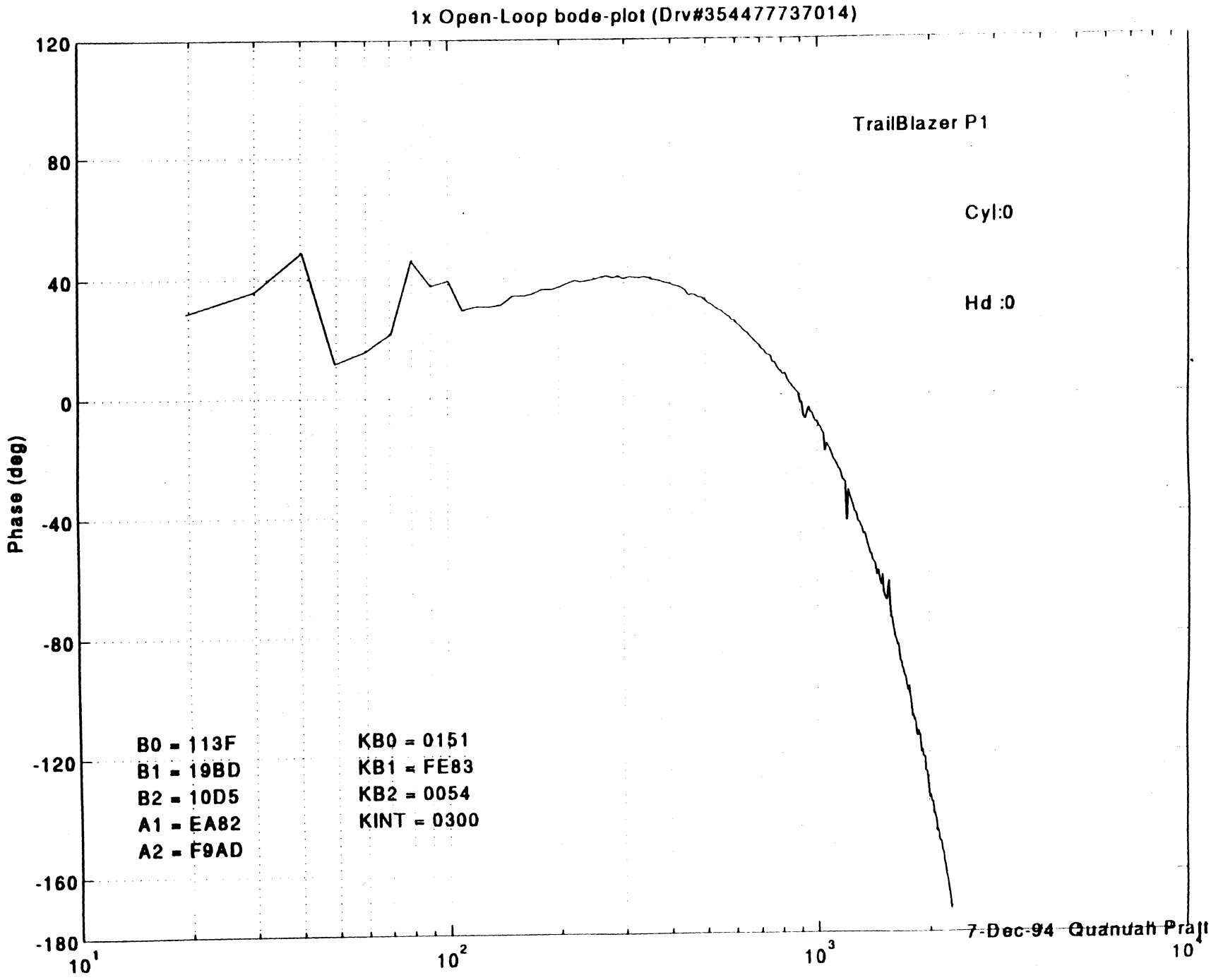
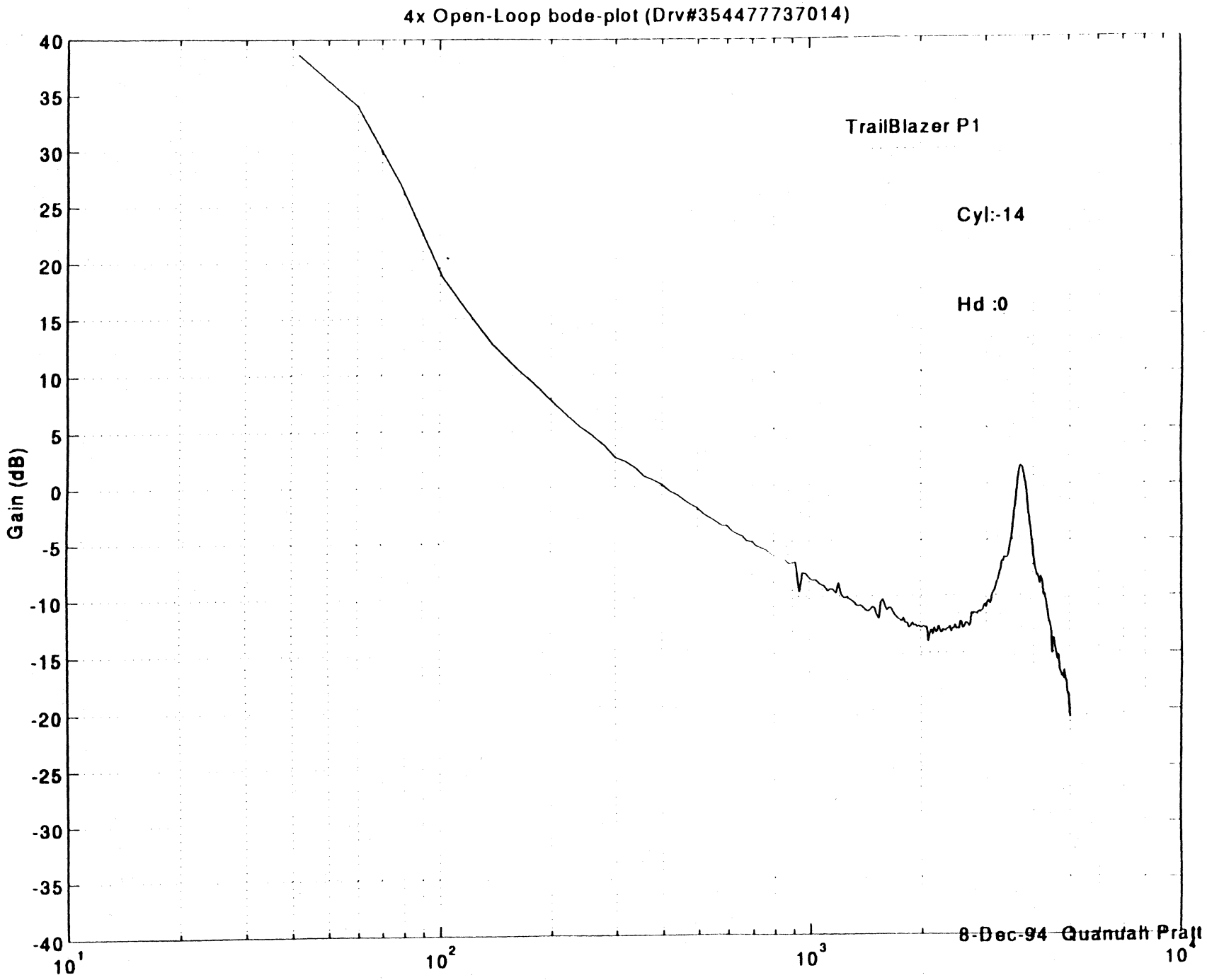
7-Dec-94 Quanuah Pratt


1x Open-Loop bode-plot (Drv#354477737014)
TrailBlazer P1
Cyl:0
Hd :0
Gain (dB)
40
35
30
25
20
15
10
5
0
-5
-10
-15
-20
10^1
10^2
10^3
10^4
B0 = 113F
B1 = 19BD
B2 = 10D5
A1 = EA82
A2 = F9AD
KB0 = 0151
KB1 = FE83
KB2 = 0054
KINT = 0300
7-Dec-94 Quantum Prat


1x Open-Loop bode-plot (Drv#354477737014)
TrailBlazer P1
Cyl:0
Hd :0
Phase (deg)
120
80
40
0
-40
-80
-120
-160
-180
10^1
10^2
10^3
10^4
B0 = 113F
B1 = 19BD
B2 = 10D5
A1 = EA82
A2 = F9AD
KB0 = 0151
KB1 = FE83
KB2 = 0054
KINT = 0300
7-Dec-94 Quantum Prajt


4x Open-Loop bode-plot (Drv#354477737014)
TrailBlazer P1
Cyl:-14
Hd :0
Gain (dB)
40
35
30
25
20
15
10
5
0
-5
-10
-15
-20
-25
-30
-35
-40
10^1
10^2
10^3
10^4
8-Dec-94 Quantah Pratt

Trailblazer Servo-mechanical System: Transfer Functions for 840 MB (2 disk) drive

The following 5 pages show open loop transfer functions of the servo-mechanical system for the 840 MB drive

1 Simulation: gain

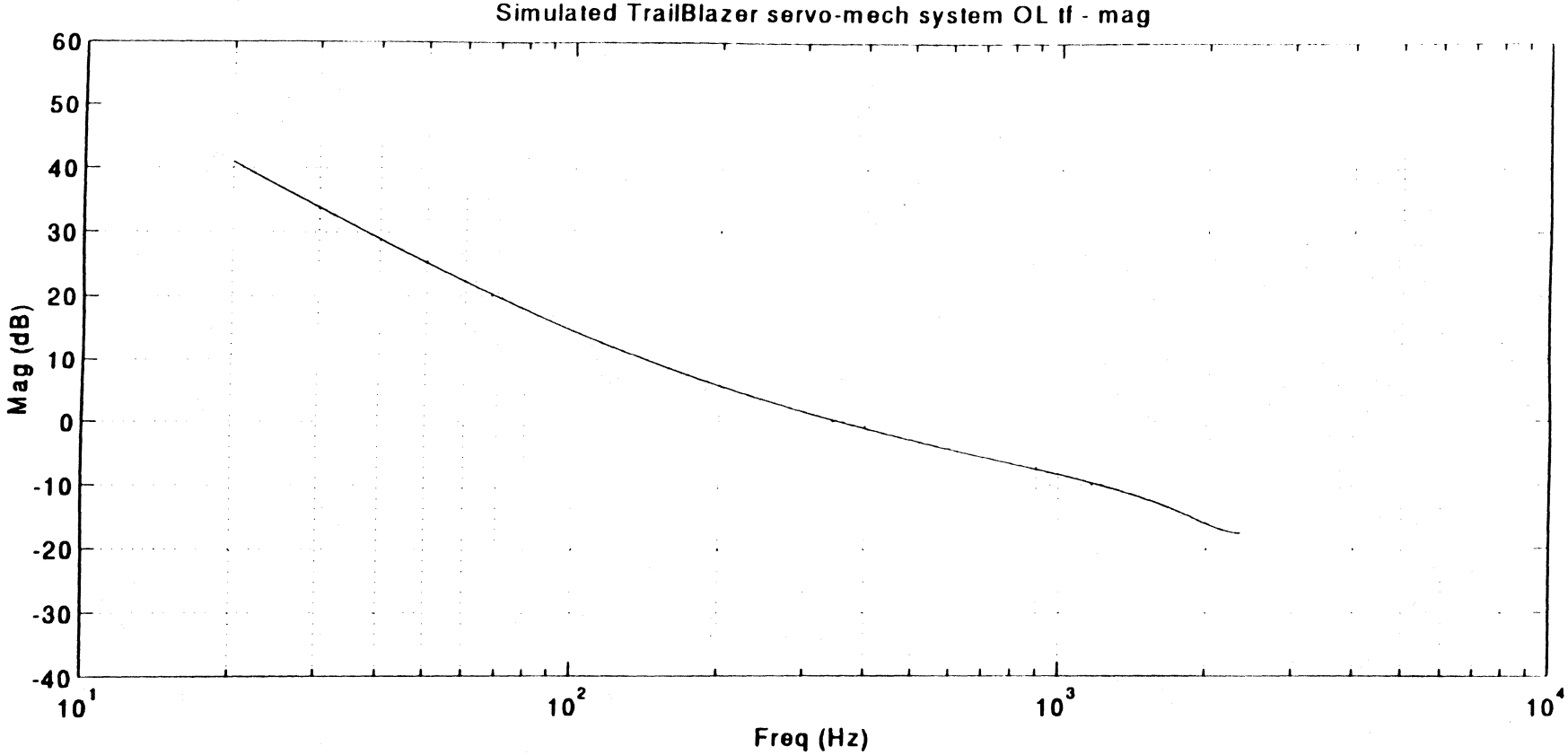
2 Simulation: phase

3 Measured: gain

4 Measured: phase

5 Measured: gain with special 4X sampling rate servo running

12/9/94 Joe Lillig



kb0 = 1.370 (KB0_BY_KLOOP = 015E)

kb1 = -1.548 (KB1_BY_KLOOP= FE74)

kb2 = 0.341 (KB2_BY_KLOOP = 0057)

kint = 768 (KINT = 0300)

Ts = 212 us

Mbytes = 840

Pes gain = 512

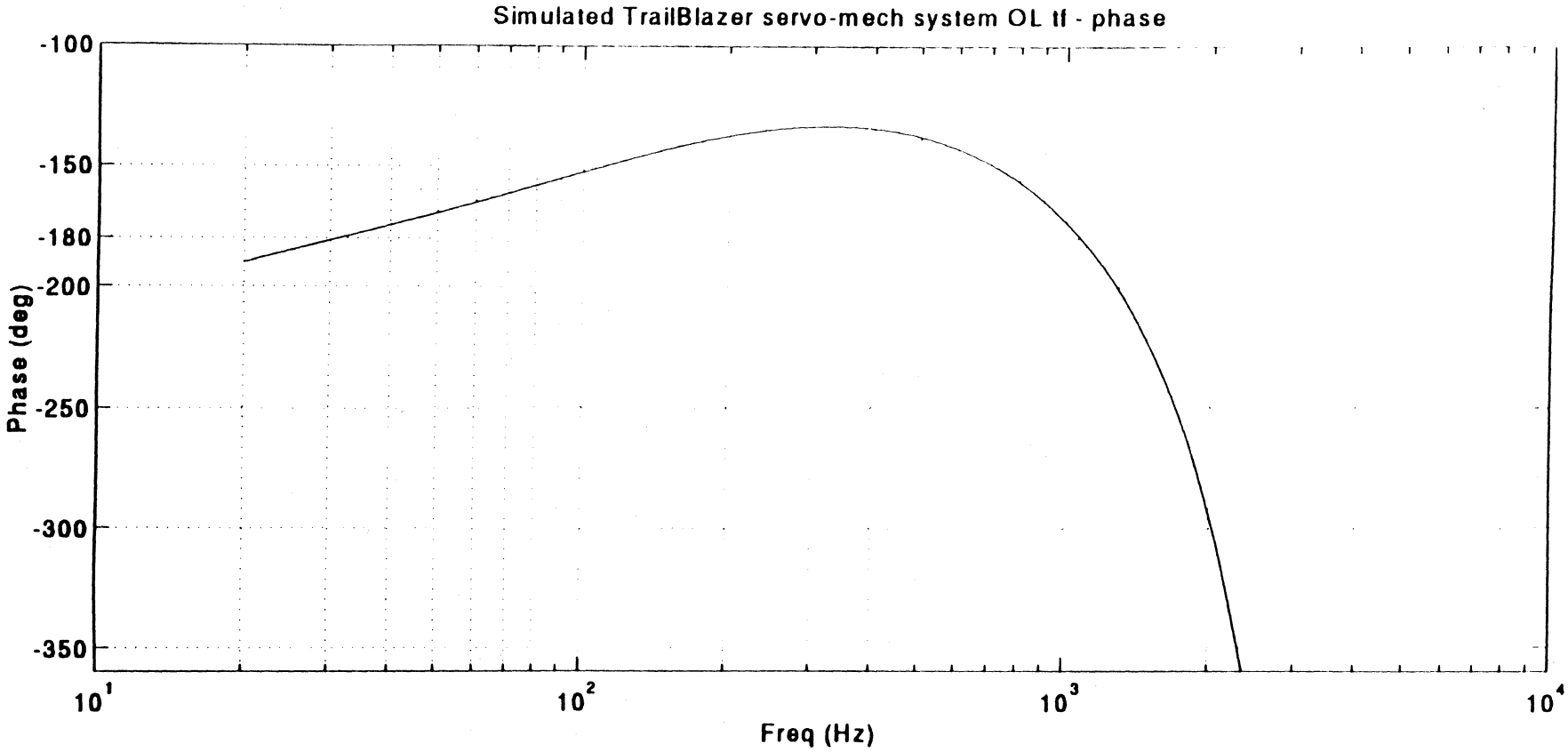
Gain crossover freq = 355 Hz

Phase crossover freq = 1071 Hz

Phase margin = 47 deg

Gain margin = 8.9 dB

9 Dec 04 Quanyah Pratt



kb0 = 1.370 (KB0_BY_KLOOP = 015E)

kb1 = -1.548 (KB1_BY_KLOOP= FE74)

kb2 = 0.341 (KB2_BY_KLOOP = 0057)

kint = 768 (KINT = 0300)

Ts = 212 us

Mbytes = 840

Pes gain = 512

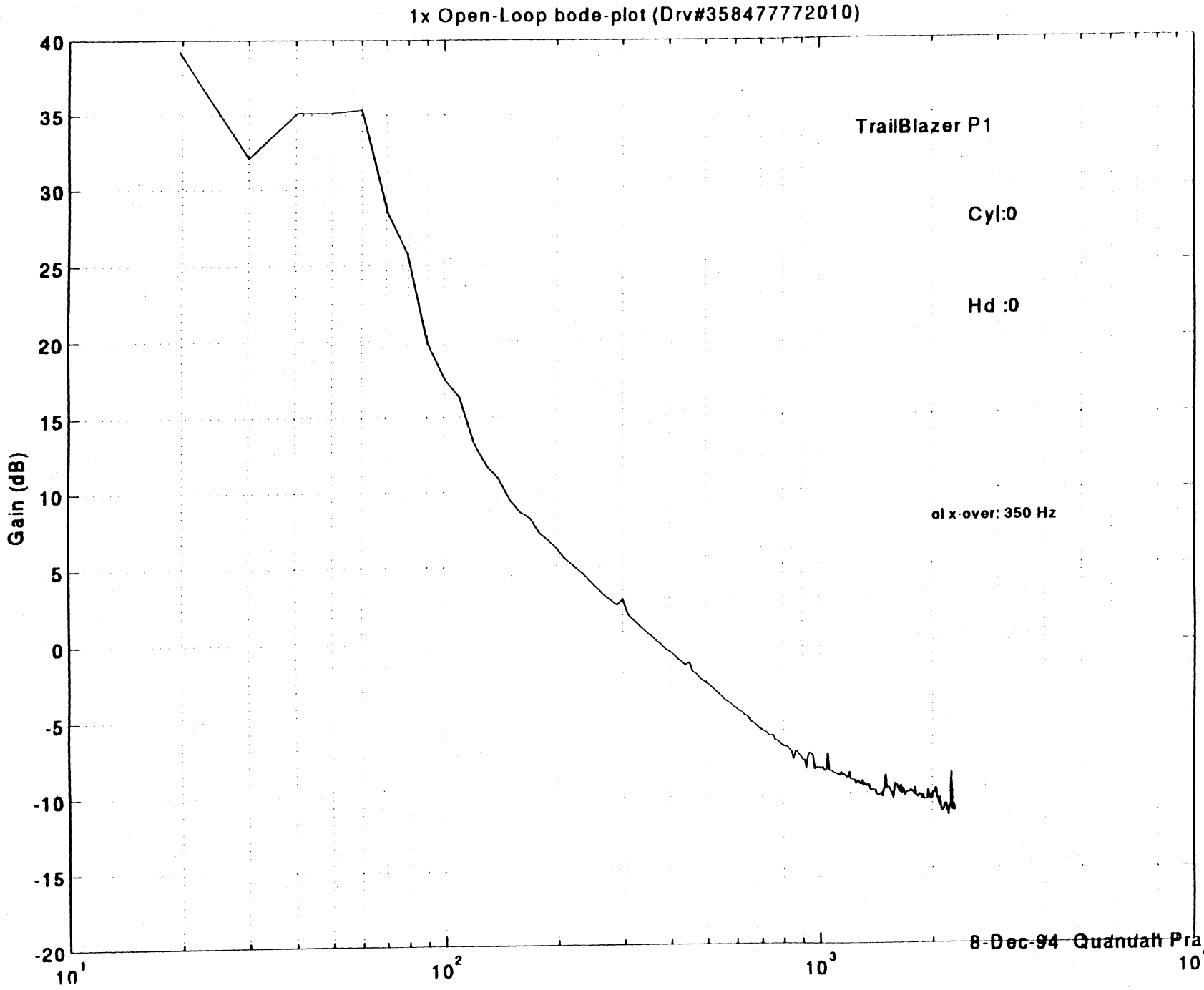
Gain crossover freq = 355 Hz

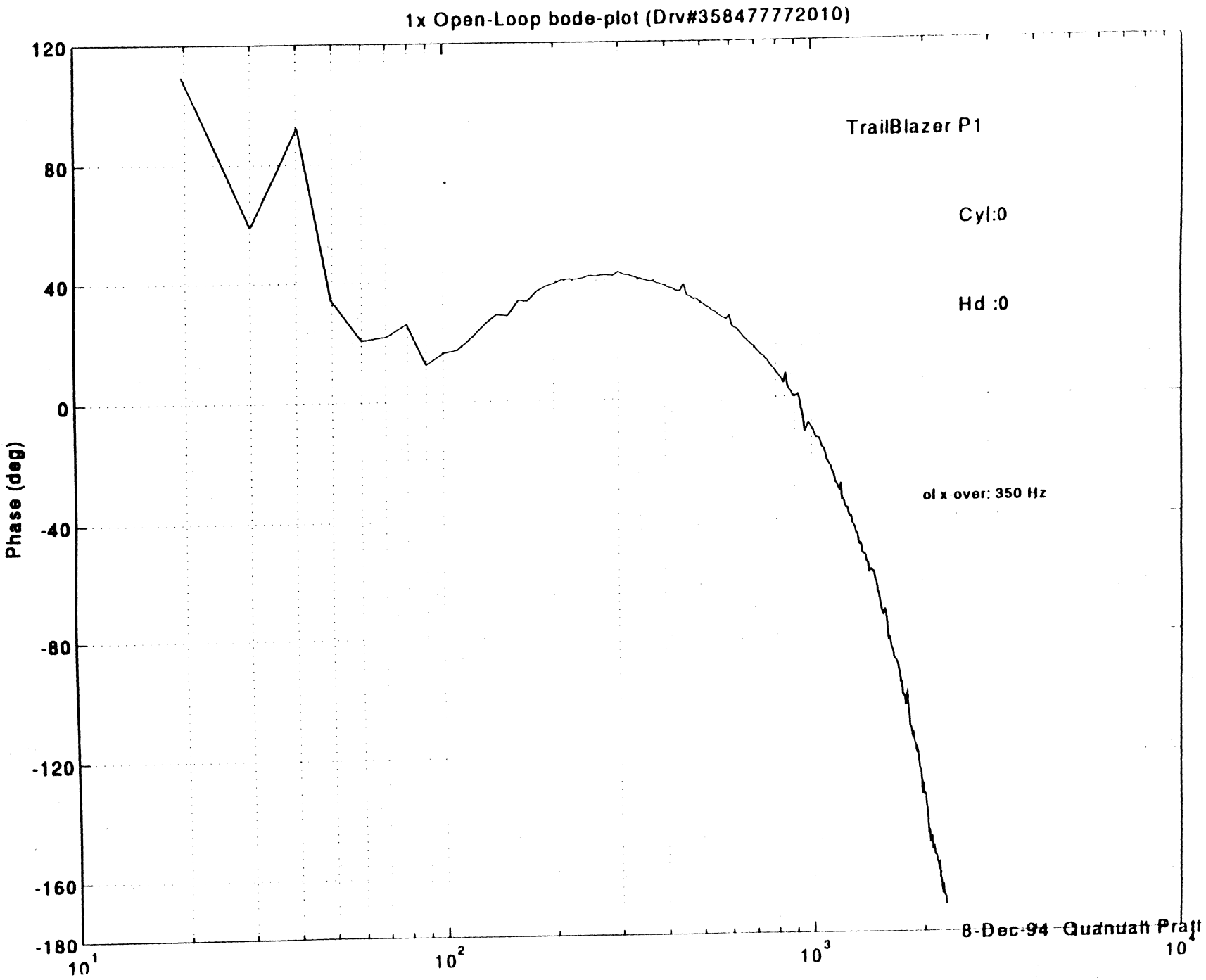
Phase crossover freq = 1071 Hz

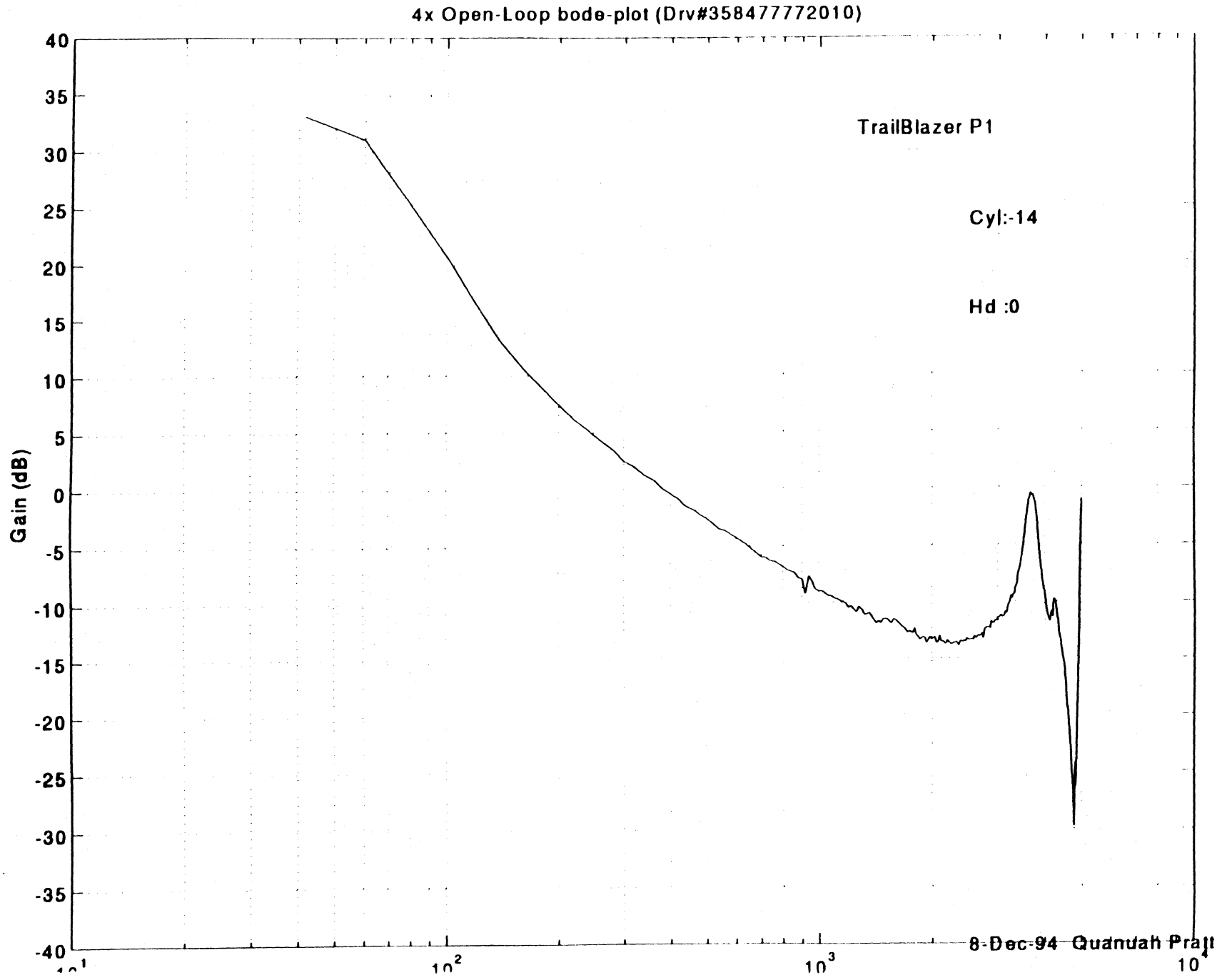
Phase margin = 47 deg

Gain margin = 8.9 dB

9 Dec 04 Quanyah Pratt


1x Open-Loop bode-plot (Drv#358477772010)
TrailBlazer P1
Cyl:0
Hd :0
ol x-over: 350 Hz
8-Dec-94 Quanuah Pratt
Gain (dB)
40
35
30
25
20
15
10
5
0
-5
-10
-15
-20
10^1
10^2
10^3
10^4


1x Open-Loop bode-plot (Drv#358477772010)
TrailBlazer P1
Cyl:0
Hd :0
ol x-over: 350 Hz
Phase (deg)
120
80
40
0
-40
-80
-120
-160
-180
10^1
10^2
10^3
8-Dec-94 Quanuah Pratt


4x Open-Loop bode-plot (Drv#358477772010)
TrailBlazer P1
Cyl:-14
Hd :0
Gain (dB)
40
35
30
25
20
15
10
5
0
-5
-10
-15
-20
-25
-30
-35
-40
10^2
10^3
8-Dec-94 Quanuah Pratt

Trailblazer Servo: Notch filter

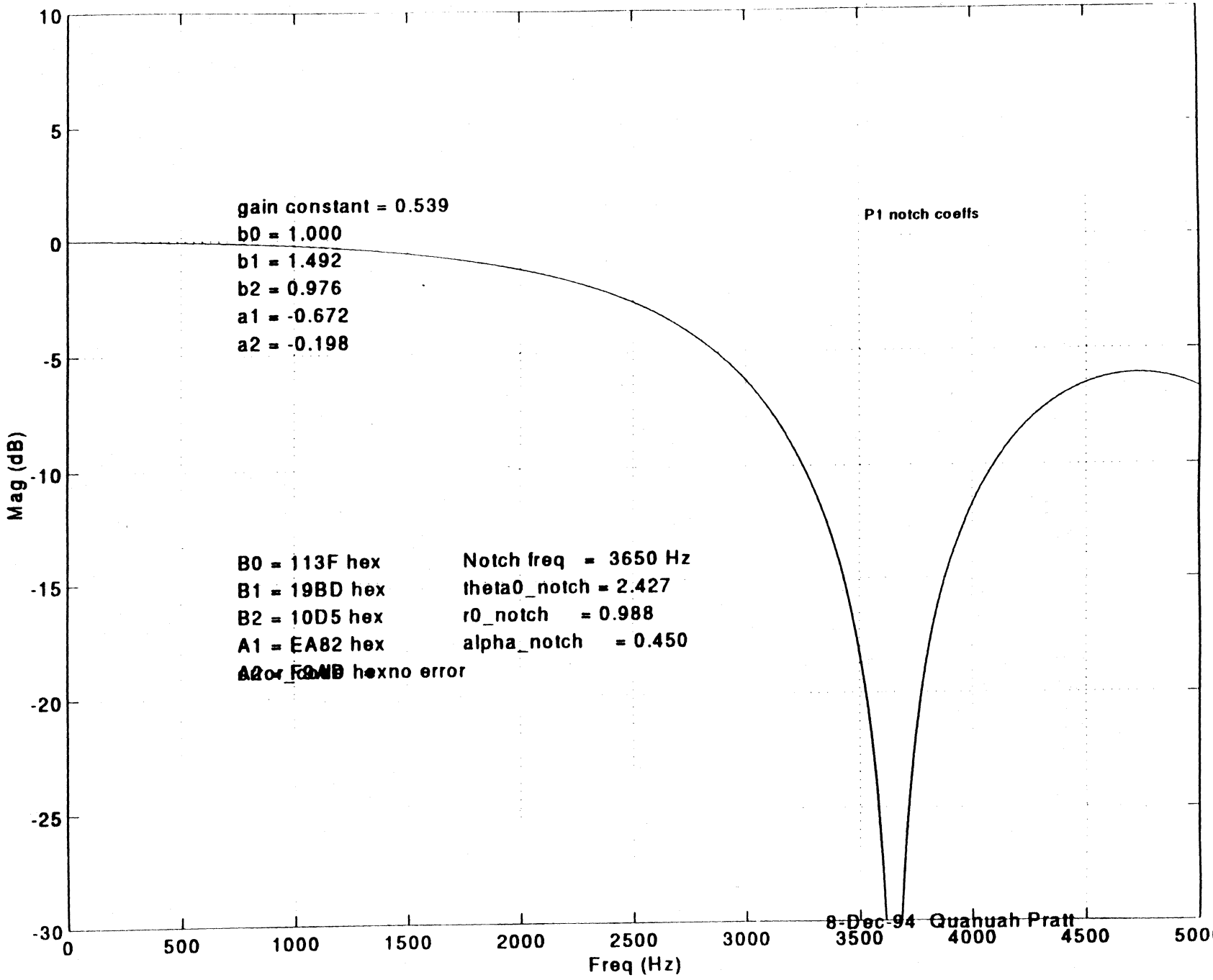
The following 2 pages show the transfer function of the servo's notch filter which runs at 2 times the servo sampling rate. (There are 2 control outputs for every position measurement.)

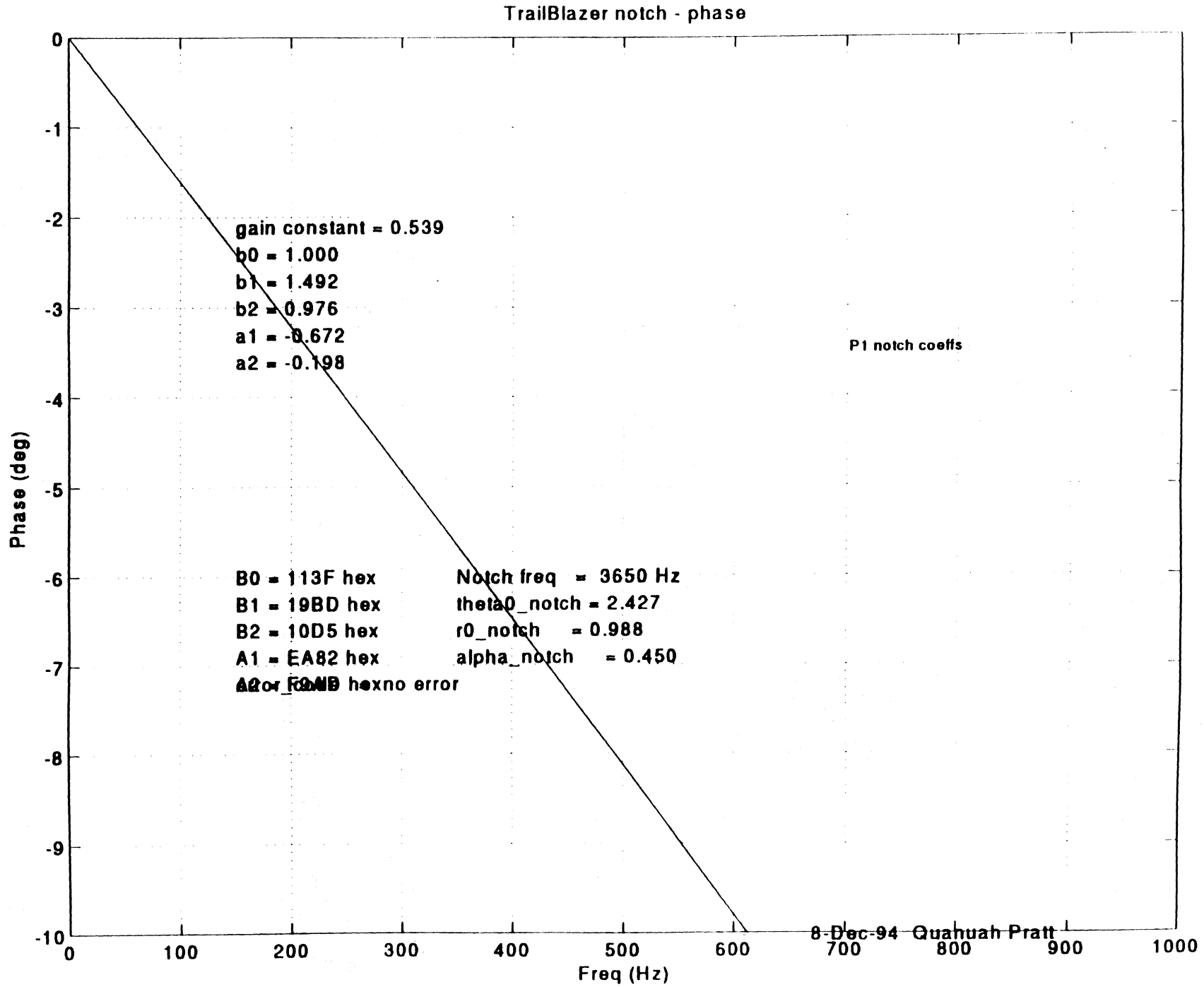
The notch filter is used to attenuate the VCM's 3.6KHz system mode

1 Simulation: gain

2 Simulation: phase

12/9/94 Joe Lillig


gain constant = 0.539
b0 = 1.000
b1 = 1.492
b2 = 0.976
a1 = -0.672
a2 = -0.198
P1 notch coeffs
B0 = 113F hex
B1 = 19BD hex
B2 = 10D5 hex
A1 = EA82 hex
A2 = F9AB hex
Notch freq = 3650 Hz
theta0_notch = 2.427
r0_notch = 0.988
alpha_notch = 0.450
no error
8-Dec-94 Quahuah Pratt
Mag (dB)
Freq (Hz)
10
5
0
-5
-10
-15
-20
-25
-30
0
500
1000
1500
2000
2500
3000
3500
4000
4500
5000


TrailBlazer notch - phase
gain constant = 0.539
b0 = 1.000
b1 = 1.492
b2 = 0.976
a1 = -0.672
a2 = -0.198
P1 notch coeffs
B0 = 113F hex
B1 = 19BD hex
B2 = 10D5 hex
A1 = EA82 hex
A2 = F2AB hex
Notch freq = 3650 Hz
theta0_notch = 2.427
r0_notch = 0.988
alpha_notch = 0.450
no error
8-Dec-94 Quahuah Pratt
Phase (deg)
Freq (Hz)
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
0
100
200
300
400
500
600
700
800
900
1000

Date: 02/24/95 **Memo**

To: **Tim Daffin (Trailblazer servowriter)**
Alfred Hwu (Test process)
Thomas Gemal (Test process)
Peter Butler (Analog parametrics)

cc: **T. S. Lee (Trailblazer firmware)**
John Goodman (Trailblazer PCB)
Steve Reed (Trailblazer drive engineering)
Rob Caldeira (Trailblazer program manager)
Tuan-Chau Ngo (Trailblazer servo)
Quanuah Pratt (Trailblazer servo)
Daniel Chan (Trailblazer servo)
Brian Bourke (Trailblazer servo)

From: **Joe Lillig (Trailblazer servo)**

Subject: Servowritten serial number format for Trailblazer - correction

The original version of this memo, dated 9/9, indicated there are 13 negative cylinders on a drive. There are actually 15. I have made the necessary corrections in "reverse video".

Serial number format

The serial number of a Trailblazer drive will be written on 10 cylinders at the ID, cylinders that are in the landing zone. The following table is a map of the cylinder usage near the ID. It shows exactly where the serial number cylinders are.

Servowritten cylinder number (starting at 0)	User oriented cylinder number (starting at -15)	Total number of cylinders in this area	Cylinder usage
3667	3652	---	Last customer data cylinder
3668 - 3675	3653 - 3660	8	Guard band
3676 - 3678	3661 - 3663	3	4x servo wedges
3679 - 3683	3664 - 3668	5	Guard band
3684 - 3693	3669 - 3678	10	Serial number
3694 - 3695	3679 - 3680	2	Guard band

The servo wedges in the serial number cylinders will have modified track id fields. The track id's will look like this:

Bit	11	10	9	8	7	6	5	4	3	2	1	0
Usage	1	1	1	1	4 bits of serial number				4 bits of track address			

The upper 4 bits will be set to all ones. This will uniquely identify the track id field as a serial number field because a track id of Fxx hex would translate to a track number greater than or equal to 3840 decimal, which is beyond the highest possible Trailblazer track number.

The next 4 bits will be one tenth of the serial number. It takes 40 binary bits to represent a 12 decimal digit serial number. The least significant bits of the serial number will be in the OD-most cylinder of the 10 serial number cylinders. The bits will continue in sequence through the 10 cylinders.

Subject: Servowritten serial number format for Trailblazer - correction

The 4 bits of track address will be the same as they would be on a normal track. They will be the 4 least significant bits of the true track address for those cylinders. The servo will use them to determine where it is within the 10 serial number cylinders.

The same modified track id fields will be written to all 63 wedges on a track, and to on all heads in a cylinder. So the number of copies of the serial number on a drive will be 63 times the number of heads in the drive.

The track id on the disk is gray coded. The ASIC decodes it before loading it into its track number register. It is the un-gray-coded value that is described above. Here is an example of what might be written in one track id field on a serial number track:

Actual servowritten track number if it was not a serial number track: 3682
Serial number of drive: 12345678901234

Last 4 bits of track number in binary: 0010
Last 4 bits of serial number in binary: 0010

Un-gray-coded modified track id field: 1111 0010 0010
Gray coded track id field to be servowritten: 1000 1011 0011

Test software and servo firmware issues

When the test process or analog parametrics test software wants to read the cylinder number, it should command the drive to seek to a user cylinder some distance away from the first serial number cylinder, such as the last customer data cylinder. It should then execute 1 track seeks to "ease" into the serial number area. This will make things easier for the servo firmware. We will not put anything in the "long seek code" that knows about the serial number tracks. We will only be able to handle the modified track id field while doing short (1 track seeks) and while track following.

When moving through the serial number cylinders, the test software should use normal target track addresses. The servo will recognize that the target cylinder is a serial number cylinder and it will use only the bottom 4 bits for positioning. The four 1's in the most significant bits of the modified track id fields will be used by the servo firmware to confirm that it is indeed in the serial number area.

MEMO

Date: Jan. 19, 1995
To: Trailblazer Team
From: Richard Hu
Subject: TBR S/W Serial Number

MKE has requested that the start date and time, station ID and position number be incorporate into our current serial number scheme. Greg Kahlert and I along with the MKE staff have come up with the following solution:

1. The current serial number format stays unchanged. This will minimize the chance of things going wrong since we are so close to P2.

2. The start date and time, station ID and position number will take an additional 9 tracks starting 4 tracks after the last serial number track. Since the serial number occupies physical tracks 3684 to 3693, tracks 3698 to 3706 will be taken up by the new data. There is a 4-track guard band between the serial number and new data tracks. This band ensures that there are no (1111) to (0000) transitions in the lower 4 bit cylinder number.

3. The following table shows the track layout:

Physical Track # (starting at 0)	Logical Track # (starting at -15)	Total # of Tracks	Track Usage
0 to 3	-15 to -12	4	4x Servo Wedges
4 to 3667	-11 to 3652	3663	Customer Data
3668 to 3675	3653 to 3660	8	Guard Band
3676 to 3678	3661 to 3663	3	4x Servo Wedges
3679 to 3683	3664 to 3668	5	Guard Band
3684 to 3693	3669 to 3678	10	Serial Number
3694 to 3697	3679 to 3682	4	Guard Band
3698 to 3706	3683 to 3691	9	*New Data
3707 to 3708	3692 to 3693	2	Guard Band
3709 to 3728	3694 to 3713	20	Extra Guard Band

* See appendix for detail.

APPENDIX

THE BIT LAYOUT FOR THE NEW DATA

Physical Track #	Logical Track #	Data
3698	3683	0FS2 ↑↑_____ last 4 bits of the track # |_____ upper 4 bits of the station ID
3699	3684	0FS3 ↑↑_____ last 4 bits of the track # |_____ lower 4 bits of the station ID
3700	3685	0FN4 ↑↑_____ last 4 bits of the track # |_____ xxOX ↑ ↑ ↑__5th bit of date (0 or 1) | |_____ always 0 |_____ position # (0 - 3)
3701	3686	0FT5 ↑↑_____ last 4 bits of the track # |_____ lower 4 bits of the starting date
3702	3687	0FM6 ↑ ↑_____ last 4 bits of the track # |_____ starting month
3703	3688	0FS7 ↑↑_____ last 4 bits of the track # |_____ starting year
3704	3689	0FH8 ↑↑_____ last 4 bits of the track # |_____ upper 4 bits of starting hour
3705	3690	0FN9 ↑↑_____ last 4 bits of the track # |_____ XOxx ↑ ↑ ↑_upper minute bits (0 - 3) | |___always 0 |_____lowest hour bit (0 or 1)
3706	3691	0FMA ↑↑_____last 4 bits of the track # |_____lower 4 bits of the starting minute

NON-FATAL SERVO ERROR CODES

The servo does not shut down and does not require a recal when a non-fatal servo error occurs. It reports the error to the read/write firmware and attempts to settle back on track. It sets SERVO_DISTRESS, the handshaking flag it uses to communicate with the read/write firmware. It also sets WR_GATE_DIS to disable write operations. See the document entitled "Trailblazer Servo Error Handling" for a complete description of the handling of non-fatal servo error codes by the servo and read/write firmware.

- **EC_BAD_SYNC**

  The ASIC's servo logic block could not detect a sync pattern in a wedge ... and the previous wedge had the first indication of a non-fatal servo error of any type. This means the previous wedge had a bad sync or bad SAM or any other type of error.

- **EC_BAD_SAM**

  The ASIC's servo logic block could not detect a SAM (Servo Address Mark) in a wedge ... and the previous wedge had the first indication of a non-fatal servo error of any type.

- **EC_BAD_TRKNUM_OR_INDEX**

  The ASIC's servo logic block reported a data error or a soft error in a wedge ... and the previous wedge had the first indication of a non-fatal servo error of any type. A data error is an illegal pattern in the track number field or the index bit field. A soft error is a missing data pulse in the track number field.

- **EC_OFF_TRACK**

  The ASIC's servo logic block reported a track address for a wedge that was not what the servo code expected ... and the previous wedge had the first indication of a non-fatal servo error of any type.

- **EC_OUT_SPEED**

  The ASIC's servo logic block reported a speed error. It does not matter what happened with the previous wedge.

- **EC_BUMPED**

  The burst amplitudes for two consecutive wedges indicate the drive was bumped. Or the burst amplitudes in a single wedge indicate a possible bump ... and the previous wedge had the first indication of a non-fatal servo error of any type. Or the head ran over a wedge which had a defect in the bursts ... and the previous wedge had the first indication of a non-fatal servo error of any type. See the document referenced above for a complete description of how the servo determines whether or not a bump has occurred.

- **EC_ERASED_BURST**

  A wedge's C burst amplitude was below the value used to test for C bursts which were erased at self scan ... and the previous wedge had the first indication of a non-fatal servo error of any type.

Note that there is no longer an EC_SERVO_DEFECT error code as there was on Roadrunner. The servo no longer attempts to distinguish between defects and bumps.

FATAL SERVO ERROR CODES

When a fatal servo error occurs the servo shuts down (it no longer goes through its interrupt routines), the VCM is disabled, and a recal is required to bring the servo back on line. SERVO_DISTRESS and WR_GATE_DIS are set. FATAL_SERVO_ERROR is also set to let the rest of the firmware know what is going on.

- **EC_LOST_LOCK**

  The ASIC's servo logic block reported any combination of five consecutive bad syncs, bad SAMs, or speed errors while the servo was attempting to sit on track.

- **EC_BUMP_TIMEOUT**

  The drive failed to recover from a non-fatal servo error within 1 second. The non-fatal servo error was most likely a bump so the error code is named that way.

- **EC_SEEK_TIMEOUT**

  The drive failed to complete a seek within 1 second.

- **EC_SEEK_LOST_LOCK**

  The ASIC's servo logic block reported any combination of five consecutive bad syncs, bad SAMs, or speed errors while the servo was attempting to seek.

To: Anyone interested in the subject below

From: Joe Lillig (Trailblazer servo) and Kevin Murphy (Trailblazer firmware)

Subject: Trailblazer servo error handling **Rev 2**

Note: All changes from the last rev of this document are shown in "reverse video".

General Introduction

The purpose of this memo is to document the proposed strategy for servo error handling in the Trailblazer drive. We have worked with Rick Ehrlich of the APE servo group and Dave Jeppson of the Fireball servo group to establish a strategy that is satisfactory for both the Trailblazer and Fireball programs. Some of the ideas evolved from discussions some time ago with Joe Humel of the Lightning servo group. Other drive programs being developed in the same time frame as Trailblazer and Fireball may want to adopt this strategy.

Both Trailblazer and Fireball are early in their development cycles so things may change as we gain experience with the drives. This is our starting point.

Servo Error Detection and Reporting Strategy (Joe Lillig)

Introduction

There are three primary goals of the servo code's error detection and reporting scheme. First, we must protect the customer's data. Second, if data sectors need to be reallocated in the vicinity of a servo wedge that is corrupted, we must give the interface code enough information to allow it to reallocate the minimum number of data sectors necessary to avoid the bad servo wedge. Third, the handshaking done with the interface code should be as simple as possible so that present and future interface and servo coders can easily understand it when they are adding new code features that deal with it.

Types of servo errors

Servo errors fall into three categories: (1) servo wedge pattern errors reported by the ASIC's servo logic block, (2) off track conditions detected by the servo code after examining the burst amplitudes, and (3) a spindle motor speed error that is also reported by the ASIC.

Wedge pattern error handling

There are four servo wedge pattern errors reported by the ASIC: sync error, SAM error, data error, and soft error. In addition, the ASIC may report a track address that does not match what we expected. We will also call that a wedge pattern error rather than a off track error because we suspect a defect or noise blip caused the bad track address. If we are wrong, the customer's data is still protected because the sequencer won't begin writing until it finds the data sector ID it is looking for.

If one of these wedge pattern errors occurs, and there is no indication of an off track condition, then we assume that either a defect in the media or a noise blip caused the problem, and that it can be ignored. We will use the current wedge's servo bursts for positioning.

To: Anyone interested in the subject below

From: Joe Lillig (Trailblazer servo) and Kevin Murphy (Trailblazer firmware)

Subject: Trailblazer servo error handling | Rev 2

If we see two consecutive wedges with any combination of these errors, then we believe there may truly be a problem. We will set our primary handshaking flag for the interface code which is called SERVO_DISTRESS. We will also disable writing and jump into our settling code to attempt to get back on track reliably.

In addition to the handshaking flag, there is an error status byte the servo code uses to tell the interface code what kind of servo error it detected. It is called SERVO_STATUS. If we get consecutive wedges with any combination of servo wedge pattern errors, we will load SERVO_STATUS with the current error, the one associated with the second wedge.

Speed error handling

If a speed error is reported by the ASIC, we will immediately set SERVO_DISTRESS, disable writing, and jump into our settling code. We will load the SERVO_STATUS error byte with a speed error code.

Off track error handling

When we first encounter what seems to be an off track condition, it can really be one of three things: a true bump, a defect (or noise blip) in the bursts, or an erased C burst.

(A C burst is erased at self scan time if a defect in the A and/or C burst causes a bump to occur while sitting on track doing a scan for servo wedge errors. Fireball will not erase C bursts at self scan. Instead they will create a map of bad servo wedges. So every reference to "erased C bursts" in the rest of this document should be translated to "mapped wedges" for Fireball.)

To be conservative, we will immediately disable writing when we detect an off track condition. We will set a second handshaking flag called POTENTIAL_BUMP. We will not use the current wedge's servo bursts for positioning because we are not sure if their amplitudes indicate true motion of the head or just a defect or an erased C burst. We will position the actuator using the burst information from the previous wedge. If we see an erased C burst we will load SERVO_STATUS with an erased C burst error code. If not we will load it with a bump error code.

(Fireball uses an estimator based servo while track following instead of a simple compensator. If there is an off track indication they will position the actuator with their estimated position instead of using position information from the previous wedge.)

At the next servo wedge we will look to see if there is an off-track indication again. If there is, we will set the SERVO_DISTRESS flag to let the read/write code know that we believe the drive has truly been bumped. We will overwrite the SERVO_STATUS byte with a bump error code and jump into our settling code. If there is no indication of an off track condition at the second wedge, we will not set SERVO_DISTRESS and will continue track-following using the burst information from the second wedge.

We will once again allow writing to take place.

We will not reset POTENTIAL_BUMP. In fact, we will never reset either of the two handshaking flags, POTENTIAL_BUMP or SERVO_DISTRESS. This is because the servo code is interrupt driven and runs

asynchronously to the interface (R/W) code. We will always let the interface firmware decide what to do when it sees the flags set and let it reset them when it is ready to do so.

Note that if a potential bump turns out to be an erased C burst, the interface code will be left with only the POTENTIAL_BUMP flag set and the SERVO_STATUS byte loaded with an erased C burst error code. If a potential bump turns out to be a defect in the wedge then the interface code will be left with POTENTIAL_BUMP set and SERVO_STATUS loaded with a bump error code. It would be more accurate in this case to report a defect in the servo wedge. However, we decided not to do this because of the possibility of misinterpreting a "one wedge bump" as a defect. If the actuator just barely hits the bump detect limit for one sample due to a light bump or a rough seek arrival it would be quite misleading to report a defect.

Reporting defects as bumps does not cause any problems anyway. When the wedges are scanned for wedge defects the first time during self scan, we will report bumps wherever there are burst defects. After self scan erases the C bursts of the defective wedges, we will report only erased C bursts. After that, only if a burst defect grows in the field will we erroneously report a bump instead of a defect when we set POTENTIAL_BUMP. But it doesn't really matter. The interface code will react the same way no matter what error code is in the SERVO_STATUS byte. It will map out the necessary data sectors around the wedge which is causing POTENTIAL_BUMP to be set without SERVO_DISTRESS being set.

(Since we never report anything as a defect on a Trailblazer drive, we will eliminate all the flag bits and error codes associated with wedge defects that exist in the code from previous products. We will no longer try to analyze position error to differentiate between bumps and defects. Fireball will be different. They will flag a defect if their on-track estimator error is too large. But they will treat it the same way as Trailblazer treats any off track indication.)

Interaction between different types of servo errors

How should the servo react and what error should be reported if various types of errors are detected in consecutive bursts? As was already mentioned, if two consecutive servo wedge pattern errors occur, the second one will be reported. We also already stated that if an off track condition is detected for two consecutive wedges, a bump will be reported.

What if an off track condition in one wedge is followed by a wedge pattern error in the next wedge, or vice-versa? The answer is: we will set SERVO_DISTRESS for two consecutive errors, no matter what types of errors they are. This is the most conservative approach. It does not cost anything in terms of performance because we should rarely see two wedge errors in a row. (Self scan will reject a drive that has two wedge errors in a row so only a bump or a grown defect can cause two in a row in the field.)

The next question is: what error code will be loaded into the SERVO_STATUS byte? The convention we will follow is this: we will only overwrite the SERVO_STATUS byte if SERVO_DISTRESS is not already set. (Note from the previous paragraphs that it is also true that we will only load the SERVO_STATUS byte when we are also setting either the POTENTIAL_BUMP flag or SERVO_DISTRESS flag.) Let's go through a few scenarios.

To: Anyone interested in the subject below

From: Joe Lillig (Trailblazer servo) and Kevin Murphy (Trailblazer firmware)

Subject: Trailblazer servo error handling | Rev 2

First wedge error	Second wedge error	SERVO_STATUS contents
Sync (wedge pattern error)	Sync (wedge pattern error)	Sync error
Sync (wedge pattern error)	SAM (wedge pattern error)	SAM
Erased C burst (off track error)	Bump (off track error)	Bump
Sync (wedge pattern error)	Potential Bump (off track error)	Bump
Potential Bump (off track error)	Sync (wedge pattern error)	Sync

We look at the wedge pattern information before we analyze the burst amplitudes. Therefore, if a second servo wedge pattern error occurs at the same time as a potential bump, we will set SERVO_DISTRESS due to the two consecutive servo wedge pattern errors, switch to our settling code, and not even read in the burst values. We will load the SERVO_STATUS byte with the wedge pattern error.

If different types of errors which can cause SERVO_DISTRESS to be set occur several wedges apart, and if the second one happens before the interface firmware has responded to the first one, the first error will be reported in the SERVO_STATUS byte. This just goes along with the convention of not overwriting SERVO_STATUS if SERVO_DISTRESS is already set.

As usual, there is one exception to the SERVO_STATUS overwriting rule. If we get 5 bad syncs or SAMs in a row we will overwrite the sync or SAM error already written in SERVO_STATUS with a "lost lock" error code. The lost lock error is a more severe error that obviously cannot occur unless you have already had the previous problem of two bad syncs or SAMs.

Disabling writing

We have mentioned disabling and re-enabling write operations but we have not discussed how we do those things. They are accomplished using the ASIC's servo and sequencer logic. For Trailblazer and Fireball the ASIC is "Leo". The servo disables writing by setting the FORCE_SVO_FLT bit in the TNACTL1 register (TNA Control Register 1) in the ASIC's servo logic block. If a write operation is in progress, this bit will get passed to the SERVO_FAULT bit in the SEQINT register (Sequencer Interrupt Control / Status Register) in the ASIC's sequencer logic block, and the write will be aborted. If there is not a write operation in progress the SERVO_FAULT bit will not get set. If FORCE_SVO_FLT is cleared before the sequencer tries to write, the write operation will be allowed to start.

When the servo encounters a potential bump that does not turn into a real bump it holds FORCE_SVO_FLT high only for one wedge-to-wedge time. When it encounters a true bump or any other error condition that causes SERVO_DISTRESS to be set, it sets FORCE_SVO_FLT high and leaves it high until it is finished settling back on track.

Summary

The error reporting passed from the servo code to the interface code can be summarized in the following paragraphs.

To: Anyone interested in the subject below

From: Joe Lillig (Trailblazer servo) and Kevin Murphy (Trailblazer firmware)

Subject: Trailblazer servo error handling | Rev 2

If the second of two consecutive servo wedge pattern errors (sync, SAM, data, soft, or track address mismatch) is detected, it will be reported and SERVO_DISTRESS will be set. (In this case we do not even bother to look at the burst values.)

If a speed error occurs, it will be reported immediately and SERVO_DISTRESS will be set.

If an off track condition (a bump, an erased C burst, or a burst defect) is detected, we will report either an erased C burst or a bump and set POTENTIAL_BUMP. If the off track condition continues for a second consecutive wedge we will report a bump and set SERVO_DISTRESS.

If two consecutive errors of any type occur, we will set SERVO_DISTRESS and report the second error. If two errors which can cause the setting of the SERVO_DISTRESS flag occur and are separated by a wedge or more, we will report the first error.

Conclusion

Have we achieved our three goals? Number one was to protect the customer's data. We do this because we immediately disable writes if we suspect any kind of off track condition.

Number two was to minimize the number of data sectors reallocated around a bad servo wedge. We achieve this by reporting only a potential bump at the first wedge that indicates an off track condition, and by using the burst information from the previous wedge to avoid inducing our own "bump" by reacting to the potentially bad information in that wedge. We will allow writing again immediately after the next wedge.

Number three was to keep the error reporting interface between the servo code and interface code as simple and efficient as possible. It looks OK. The servo code only controls the setting of two handshaking flags and the loading of an error status byte. The interface code controls the resetting of the flags and the clearing of the error status byte.

Read/Write Response to Servo Errors (Kevin Murphy)

Background

The POTENTIAL_BUMP flag was implemented to signal cases where the Servo ISR routine requires a subsequent wedge to distinguish erased C-bursts and servo defects from actual off-track (bump) situations. If the next wedge causes the servo code to determine that a bump has actually occurred, then the SERVO_DISTRESS (can be read as BUMP_DETECTED in previous code base) flag is set.

The read/write firmware does error processing only when the sequencer has STOPPED. The servo ISR does not terminate the sequencer on Reads, but will abort Writes on either SERVO_DISTRESS or POTENTIAL_BUMPs.

It is assumed for this discussion that the servo status flags are first checked (by R/W code) immediately following sequencer gone NOT_BUSY. In other words, at the end of the last sector of a set of sectors that

To: Anyone interested in the subject below

From: Joe Lillig (Trailblazer servo) and Kevin Murphy (Trailblazer firmware)

Subject: Trailblazer servo error handling | Rev 2

was either completely or partially read or written. (The sectors would be completely read or written if no errors occurred. They would be partially written if a servo error caused the writing to be disabled.)

Note that the POTENTIAL_BUMP flag is not cleared by the servo code. This is done so that read/write code is guaranteed not to miss any transitory status bits. POTENTIAL_BUMP, SERVO_DISTRESS and the SERVO_STATUS byte are cleared when the sequencer is started. This is done because only the servo conditions that occur during an actual read or write seem truly "interesting".

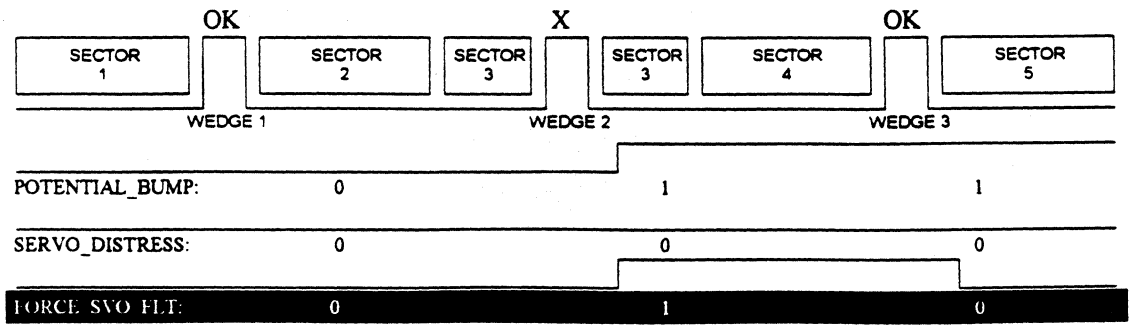
Examples

The following cases explore the determination of read/write errors due to servo conditions when the sequencer has gone not busy, either because the read/write operation is complete or a write has been disabled. (The subroutine that handles sequencer not busy is called Sequencer_Done.)

You will notice in the examples that when the read/write firmware detects that the sequencer has stopped, it usually waits for one or two servo wedges to go by before it has all the error information it needs. This is because, in the worst case, the servo may not detect a possible off track condition until the wedge after the data transfer is complete. Then it must wait for one more wedge to determine whether or not there really was motion due to a bump. It is critical to wait two wedges for a write operation because we need to find out if we got bumped while trying to write the last sector. If we did, we have to go back and rewrite it.

For a read operation, we wait for at most one wedge, never two. If the sequencer stops and POTENTIAL_BUMP is not set we just do an ECC check right away. If POTENTIAL_BUMP is set, we wait one wedge and check to see if SERVO_DISTRESS gets set. If not, we just do an ECC check and don't bother to wait around for the second wedge. In either case, we stop looking for a servo reported bump earlier than for a write because we have ECC bytes to validate the data. We are not so concerned that a bump may have occurred while reading the last sector.

- Case 1: Erased C-burst



Read Sector 2. No servo error codes set. Base errors on ECC Syndrome only.
Read Sector 3. Potential Bump. Wait 1 wedge to check for Distress. None. Check ECC Syndrome.
Read Sector 4. Potential Bump. Wait 1 wedge to check for Distress. None. Check ECC Syndrome.

To: Anyone interested in the subject below

From: Joe Lillig (Trailblazer servo) and Kevin Murphy (Trailblazer firmware)

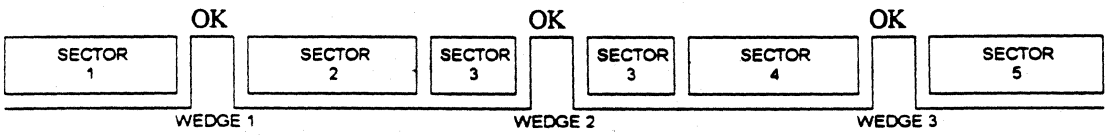
Subject: Trailblazer servo error handling **Rev 2**

Write Sector 2. No servo flags. Wait 1 wedge. POTENTIAL_BUMP. Wait 1 more wedge. No SERVO_DISTRESS. Update SECTORS_WRITTEN to include last sector that sequencer has successfully completed.

Write Sector 3. Potential Bump. Wait 1 wedge. No SERVO_DISTRESS. Wait 1 more wedge. No SERVO_DISTRESS. Update SECTORS_WRITTEN to include last sector that sequencer has SUCCESSFULLY completed. (Note that this will include Sector 2, but not Sector 3. This is done so as to reduce the number of reallocated sectors around erased C-burst wedges.)

Write Sector 4. Potential Bump. Wait 1 wedge. No SERVO_DISTRESS. Wait 1 more wedge. No SERVO_DISTRESS. Update SECTORS_WRITTEN to include last sector that sequencer has successfully completed (sector 2, but not sectors 3 or 4).

- Case 2: Erased C-burst before FIRST_SECTOR. (FIRST_SECTOR is that programmed to the sequencer as the starting sector for the read/write operation. An erased-burst may be encountered during disk rotation (latency) between the time the sequencer is started by r/w code, and the time the starting sector is seen under the head.)



POTENTIAL_BUMP:	1	1	1
SERVO_DISTRESS:	0	0	0
FORCE SVO FLT:	0	0	0

Read Sector 2. Potential Bump. Wait 1 wedge to check for Distress. None. Check ECC Syndrome.
Read Sector 3. Potential Bump. Wait 1 wedge to check for Distress. None. Check ECC Syndrome.
Read Sector 4. Potential Bump. Wait 1 wedge to check for Distress. None. Check ECC Syndrome.

For the following write examples we check the SERVO_DISTRESS flag two times after seeing POTENTIAL_BUMP set. This is because POTENTIAL_BUMP was already set when the sequencer started, and an impact during the last sector being written may cause a NEW potential bump situation. We have to wait to see if it develops into a true bump. (We always check the error flags for two wedges after the end of a write operation anyway, as explained earlier.)

Write Sector 2. Potential Bump. Wait 1 wedge. No SERVO_DISTRESS. Wait 1 more wedge. No SERVO_DISTRESS. Update SECTORS_WRITTEN to include last sector that sequencer has successfully completed.

To: Anyone interested in the subject below

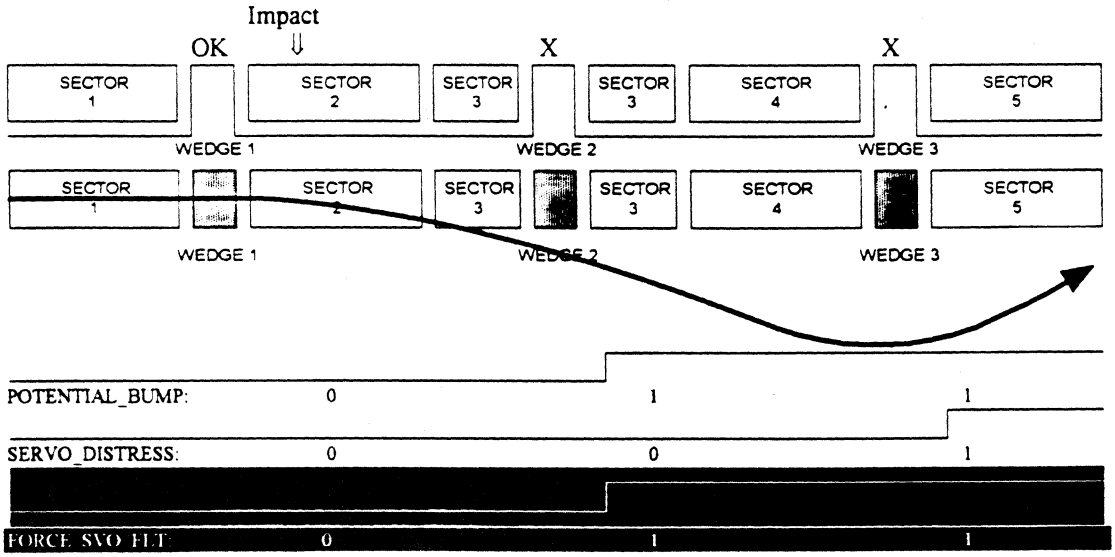
From: Joe Lillig (Trailblazer servo) and Kevin Murphy (Trailblazer firmware)

Subject: Trailblazer servo error handling | Rev 2

Write Sector 3. Potential Bump. Wait 1 wedge. No SERVO_DISTRESS. Wait 1 more wedge. No SERVO_DISTRESS. Update SECTORS_WRITTEN to include last sector that sequencer has successfully completed.

Write Sector 4. Potential Bump. Wait 1 wedge. No SERVO_DISTRESS. Wait 1 more wedge . No SERVO_DISTRESS. Update SECTORS_WRITTEN to include last sector that sequencer has successfully completed.

- Case 3: Potential, then Distress (a real bump)



Read Sector 2. No servo flags. Base errors on ECC Syndrome only.
Read Sector 3. Potential Bump. Wait 1 wedge to check for Distress. Distress. Retry read operation.
Read Sector 4. Potential Bump. Wait 1 wedge to check for Distress. Distress. Retry read operation.

Write Sector 2. No servo flags. Wait 1 wedge. Potential Bump. Wait 1 more wedge. SERVO_DISTRESS. Retry write operation.
Write Sector 3. Potential Bump. Wait 1 wedge. SERVO_DISTRESS. Retry write operation.
Write Sector 4. Potential Bump. Wait 1 wedge. SERVO_DISTRESS. Retry write operation.

Final notes

It should be an extremely rare event that two consecutive wedges have hard errors in drives in the field. The self scan process will reject such a drive. A bump will be a transitory error, not a hard one. So only new defects in the wedges could cause this problem. If so, what will happen?

To: Anyone interested in the subject below

From: Joe Lillig (Trailblazer servo) and Kevin Murphy (Trailblazer firmware)

Subject: Trailblazer servo error handling **Rev 2**

For writes, the read/write firmware will have a hard time writing to any data sectors on the track which has two consecutive hard wedge defects. This is because of the rotational latency between the time the sequencer is started and the time the first data sector to be written is found. If the head crosses over the bad wedges while it is looking for the first sector to write, the servo will set BUMP_DETECTED and the sequencer won't be allowed to write at all. If the bad wedges are within the data sectors to be written, writing will be stopped in the middle of the write. In the worst case, all the data sectors on the track will be re-allocated because at one time or another the sequencer will not be allowed to write to them. This is OK because we expect this to happen very rarely.

For reads ... TBD.

Trailblazer Firmware AT and SCSI

New TrailBlazer Firmware Features

TrB	RRR
* 20 Cross-check and ECC bytes.	* 14 bytes on RoadRunner
* Double burst correction on the fly.	* Single burst on the fly
* Triple burst offline correction.	* Double burst offline correction.
* Auto wiggle error recovery.	
* Bigger defect list. (426 entries)	* 365 defect entries.
* Up to 8 dynamic cache segments.	* 4 dynamic cache segments.
* Up to 2 random write command cache.	
* Concurrent read/write cache process.	* No concurrent read/write process.
* Dynamic read cache allocation up to 64K on sequential read.	

* Accu-write to buffer write data during spin up from sleep/standby mode.

* DPA phase 3 error logging and reporting. (AT only)

* AT auto-read/auto-write and auto TFR update. (AT only)

* AT LBA mode and DMA mode support. (AT only)

* SCSI-3 message & power mode support. (SCSI only)

* SCAM support. (SCSI only)

AT Data Transfer Modes

Read/Write Sectors (PIO)

Host
----I---XXXX---XXXX---XXXX---XXXX---XXXX---XXXXs
Drive
B--Di-----B--Di-----B--Di-----B--Di-----B--Di----B--Dis

Read/Write Multiple (PIO)

Host
----I-----XXXXXXXXXXXXXXXX---XXXXXXXXs
Drive
B---Di----------B-Dis
What is disadvantage ?

Read/Write DMA (DMA)

Host
----I----------s
Drive
B---XXXXXXXXXXXXXXXXXis

PIO Mode 4 : 16MB/S
DMA Mode 2 : 16MB/S

I : Host Issue command.
D : Drive set Data request.
s : Drive return Status
B : Drive set Busy
i : Drive generate iRQ14
X : Data Xfer

Auto Features

Auto Write Single Sector (KONI)

Host

----IXXXX---XXXX---XXXX---XXXX

Drive

D-------B-Di------B-Di-----B--Di-- ---

Auto Write Multiple Sectors (Leo)

Host

----IXXXXXXXXXXXXXXX---

Drive

Di-----Di------Di------Di------B--

*Write sector/Write multiple/Writre buffer

Auto Read Multiple Sectors (Leo)

Host

----IXXXXXXXXXXXXXXX---

Drive

Di-----Di-----Di-----Di------B--

*Cache prefetch hit.

Drive Parameter Analysis (DPA)

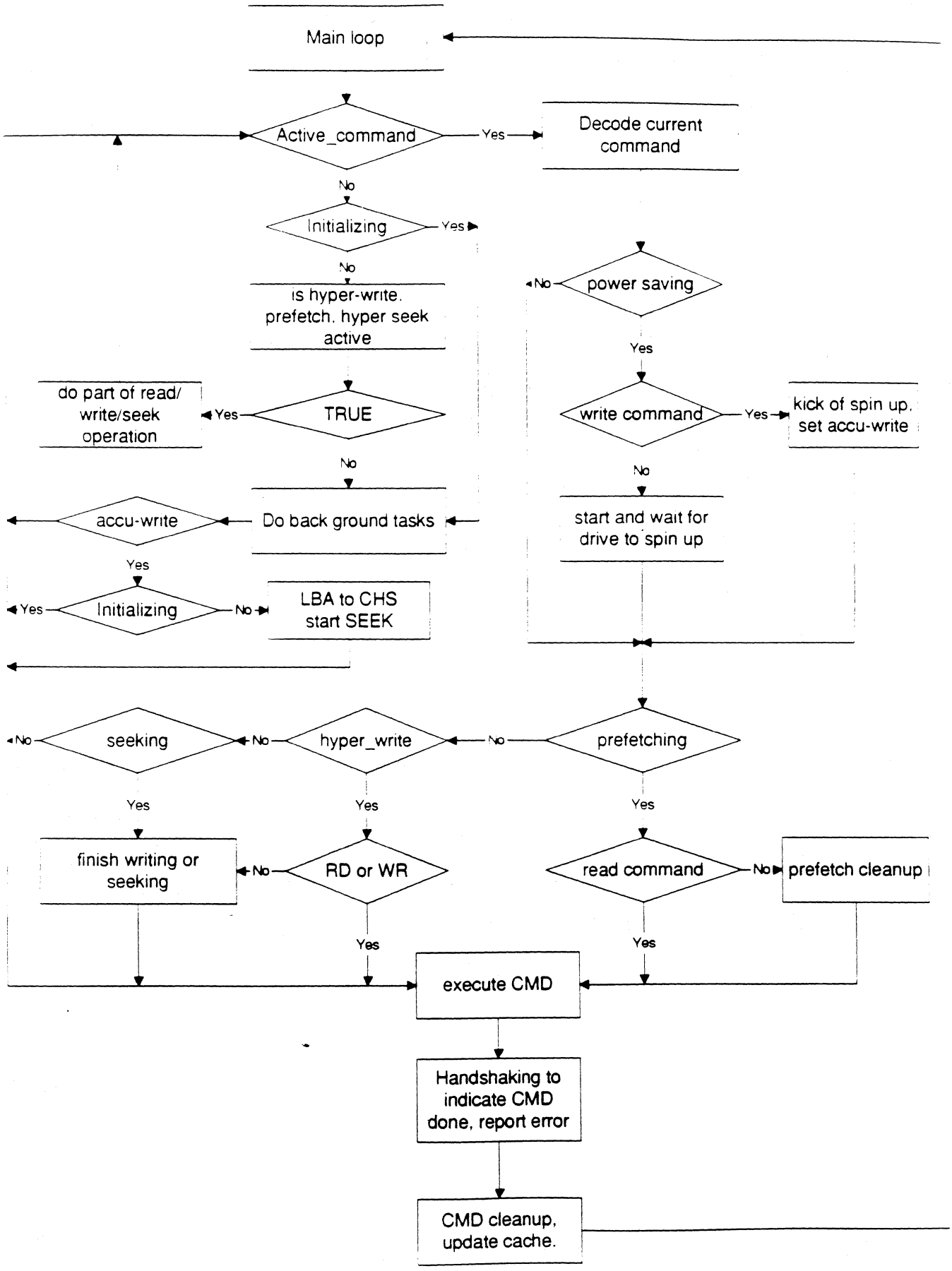
Following information are collected by F/W for drive failure analysis.

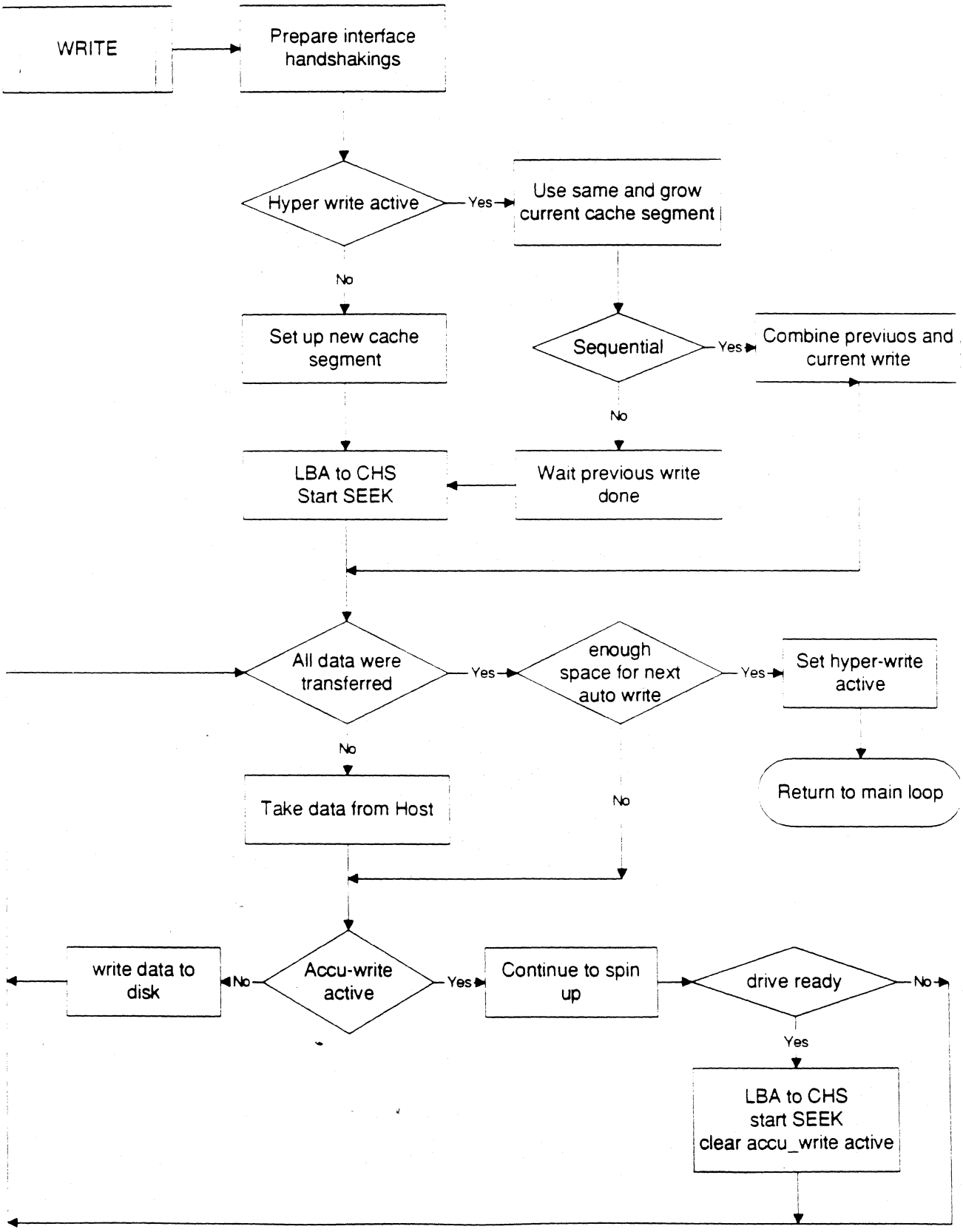
Number of CSS
Number of Power Cyles
Power On Hours
Grown Defects
Spin-up time
Number of recal retry count
Seek error rate
Read soft error rate

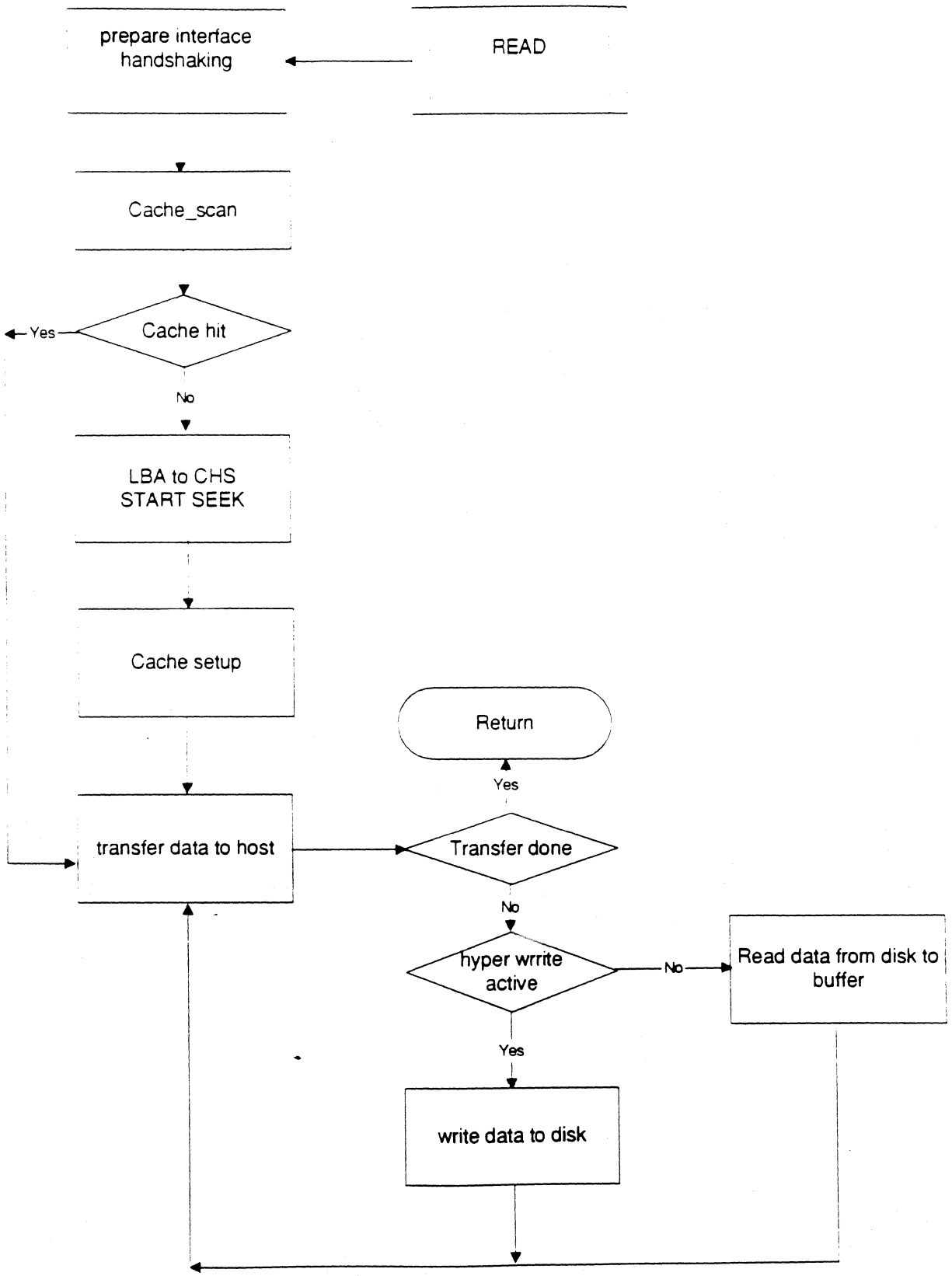
Scsi Configured AutoMagically (SCAM)

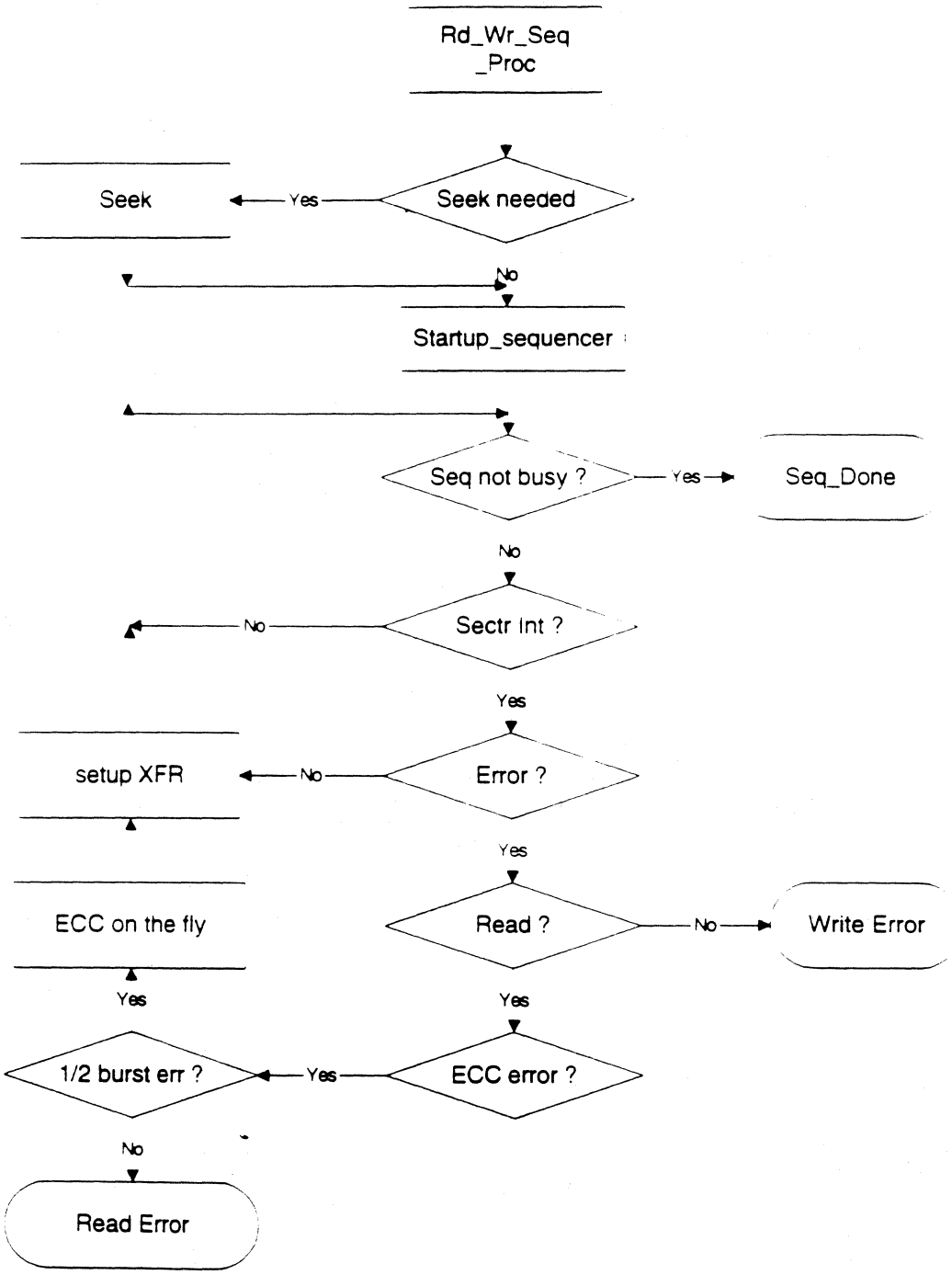
Terms

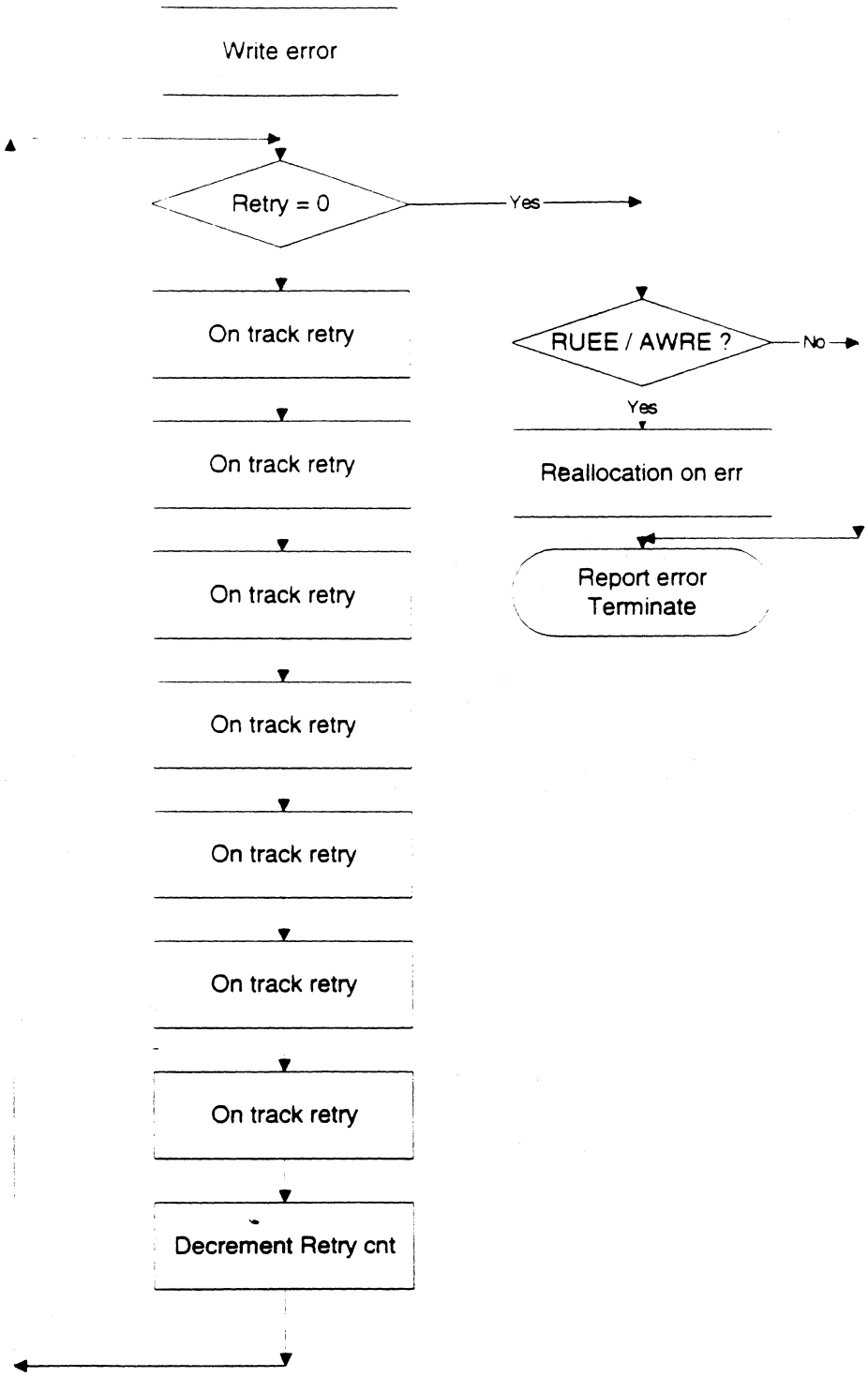
Hard ID : ID selected by jumper
Soft ID : ID Assigned by SCAM
Default ID : Default ID on NON-SCAM bus
SCAM Capable Bus : A SCSI bus has one or more SCAM Master device
SCAM Master Device : Controls SCAM soft ID assignment
SCAM Slave Device : Device responds to SCAM ID assignment

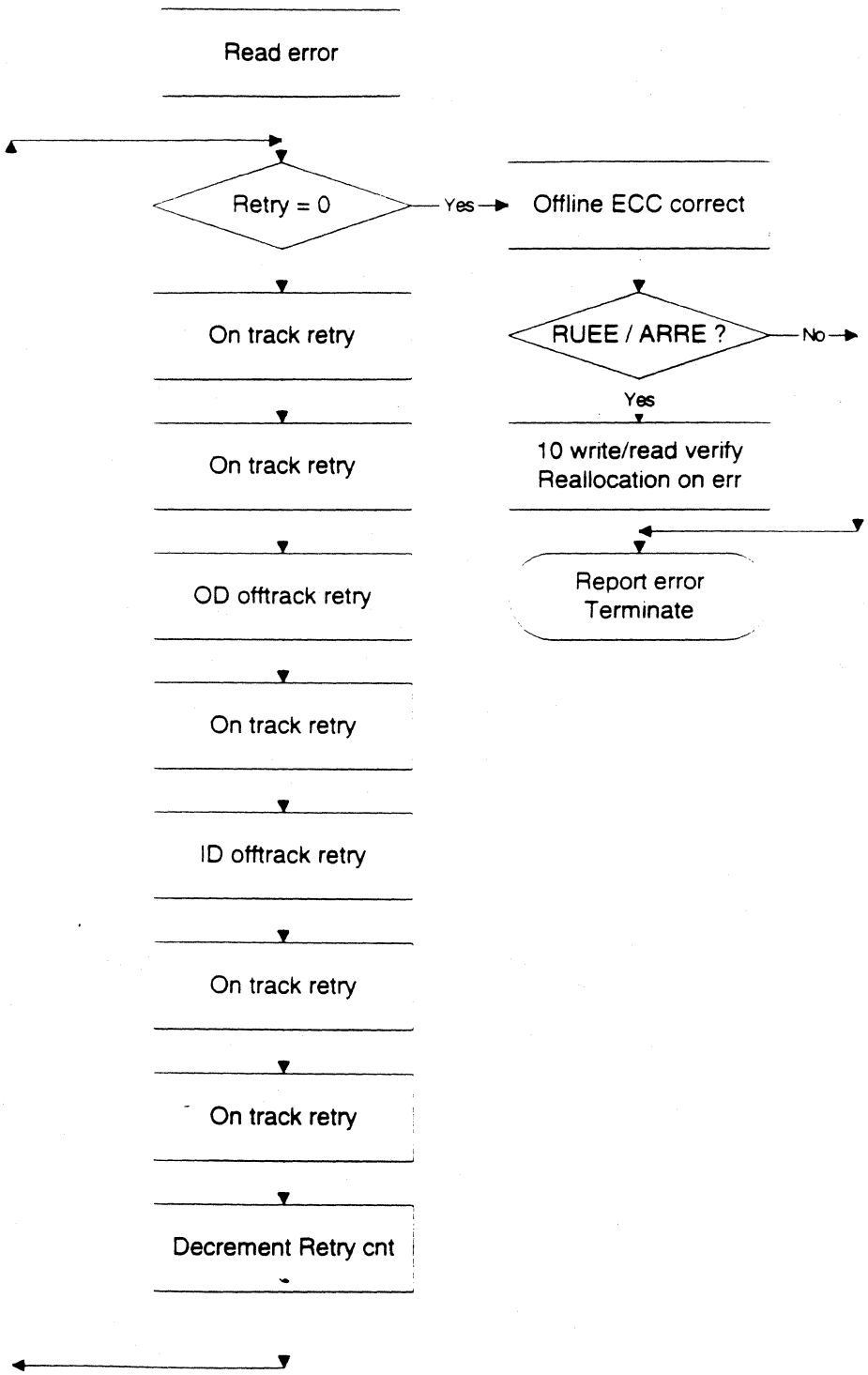

Main loop
Active_command
Yes
Decode current command
No
Initializing
Yes
No
is hyper-write. prefetch. hyper seek active
No
power saving
Yes
do part of read/ write/seek operation
Yes
TRUE
write command
Yes
kick of spin up, set accu-write
No
No
start and wait for drive to spin up
accu-write
Do back ground tasks
Yes
Yes
Initializing
No
LBA to CHS start SEEK
No
seeking
No
hyper_write
No
prefetching
Yes
Yes
Yes
finish writing or seeking
No
RD or WR
read command
No
prefetch cleanup
Yes
Yes
execute CMD
Handshaking to indicate CMD done, report error
CMD cleanup, update cache.


WRITE
Prepare interface handshakings
Hyper write active
Yes
Use same and grow current cache segment
No
Set up new cache segment
Sequential
Yes
Combine previuos and current write
No
LBA to CHS Start SEEK
Wait previous write done
All data were transferred
Yes
enough space for next auto write
Yes
Set hyper-write active
No
Take data from Host
Return to main loop
No
write data to disk
No
Accu-write active
Yes
Continue to spin up
drive ready
No
Yes
LBA to CHS start SEEK clear accu_write active


READ
prepare interface handshaking
Cache_scan
Cache hit
Yes
No
LBA to CHS
START SEEK
Cache setup
transfer data to host
Transfer done
Return
Yes
No
hyper wrrite active
No
Read data from disk to buffer
Yes
write data to disk


Rd_Wr_Seq
_Proc
Seek needed
Yes
Seek
No
Startup_sequencer
Seq not busy ?
Yes
Seq_Done
No
Sectr Int ?
No
Yes
Error ?
No
setup XFR
Yes
Read ?
No
Write Error
ECC on the fly
Yes
ECC error ?
Yes
1/2 burst err ?
Yes
No
Read Error


Write error
Retry = 0
Yes
On track retry
On track retry
On track retry
On track retry
On track retry
On track retry
On track retry
Decrement Retry cnt
RUEE / AWRE ?
No
Yes
Reallocation on err
Report error
Terminate


Read error
Retry = 0
Yes
Offline ECC correct
On track retry
RUEE / ARRE ?
No
Yes
On track retry
10 write/read verify
Reallocation on err
OD offtrack retry
Report error
Terminate
On track retry
ID offtrack retry
On track retry
On track retry
Decrement Retry cnt

PCB & Components

Product Comparison

	RoadRunner	Trailblazer
Capacity	210/420	420/850
Interface	AT/SCSI	AT/SCSI
MP	75352	78352
Buffer	128	128
Seek Time (ms)	14	14
RPM	3600	4500
Data rate (Mb/sec)		
Max	52	27.88
Min	29.14	16.67
Filter	8011 or 0896	Programable Integral to 3038 chip
Synthesizer	SAKANA	Integral to 3038 chip
Motor Driver	HA 13481	Hitachi Combo
VCM Driver	HA 13490	Hitachi Combo
Transfer Rate (MB/sec)		
PIO	11	16
DMA	13	16
SCSI	6/10	6/10

PCB Major Components

Description	Vendor Part Number	Vendors
Read Channel	HA153038	Hitachi
Controller & Interface	Leo-A (AT CF64675A) Leo-S (SCSI CF64674A)	T.I.
U-Processor	uP78352KK	NEC
Buffer RAM	TC511664BJ-80 LC321664AJ-80 MSM511664A80-JS EiC611160A-80 uPD421664LE-80	Toshiba Sanyo Oki ETRON NEC
Motor & VCM	HA13545	Hitachi
Terminator (SCSI only)	BH9595FP-Y	Rohm
EEPROM (SCSI only)	NMC93C14MB ST93C46AM1 AT93C46-10SC	NSemi SGS ATMEL

LEO AT AND LEO S

MAIN BLOCKS

- INTERFACE (AT OR SCSI)
- BUFFER CONTROL
- SERVO CONTROL
- MICROPROCESSOR INTERFACE
- READ/WRITE SEQUENCER
- MOTOR/VCM CONTROL
- A TO D CONVERTER
- ECC
- SERIAL INTERFACE

SCSI INTERFACE

- SAME AS KONI/NEKO ASICS

AT INTERFACE

- **SUPPORTS 16 MB/SEC TRANSFER RATE**
  - PIO MODE 4
  - DMA MODE 2
- **LBA AND EXTENDED CHS SUPPORTED**
- **8.33 MB/SEC SUSTAINED WITHOUT FLOW CONTROL**
- **AUTO READ CAPABILITY EXPANDED**
  - READ / WRITE MULTIPLES
  - AUTOMATIC MULTIPLE SECTOR TRANSFERS WITHOUT FIRMWARE INTERVENTION
  - AUTO READ ACROSS COMMAND CAPABILITY
- **AUTO CHS/LBA**

BUFFER CONTROL

- CPU PREFETCH CONTROL
- NON PREFETCH AREA
- 40.0 MBYTES/SEC MAX BANDWIDTH (60 MHZ CLOCK AND 4 MEG 70 NS DRAM)
  - 26.6 MBYTES/SEC ON TRAILBLAZER (40 MHZ CLOCK AND 1 MEG 80 NS DRAM)
- OPTIMIZED ARBITRATION
  - DISK FIFO INCREASED FROM 6 TO 8 WORDS
- PROGRAMMABLE NUMBER OF CLOCKS PER DRAM CYCLE
  - ALLOWS OPTIMUM PERFORMANCE AT VARIOUS BUFFER CLOCK FREQUENCY / DRAM SPEED COMBINATIONS

READ WRITE SEQUENCER

- **MODIFIED ADDRESS MARK DETECTION FOR COMPATIBILITY WITH HITACHI 3038**
  - NO "APPLE" BIT (IMPLEMENTED IN FIRMWARE)
- **INCREASED LOOP COUNTER TO 8 BITS TO ALLOW > 128 SECTORS / TRACK**
- **WCS RAM INCREASED**
  - WAS 32 x 28, NOW 36 x 30
- **REMOVE ENDEC**
  - ENDEC FUNCTION NOW IN HITACHI 3038
- **TWO BIT PARALLEL, NRZ, BIDIRECTIONAL DATA PATH BETWEEN LEO AND 3038 (45.5 MHZ MAX)**
  - TRAILBLAZER RUNS AT A MAXIMUM OF 26 MHZ

SERVO CONTROL

- GENERATES SIGNALS TO SHIVA TO CONTROL BURST SAMPLING
- OPTIONAL 2T OR 3T IN WEDGE SYNC FIELD
- 40 MHZ OPERATION ON TRAILBLAZER
- INCREASED TRACK NUMBER TO 13 BITS (NOW 8192 MAX)
  - WE PROGRAM IT TO 12 BITS
- INCREASED SAM TO SAM COUNTER TO 13 BITS

A TO D CONVERTER

- SAME A TO D CELL AS IN NEKO
- SUPPORTS SERIAL SAMPLE MODE

SERIAL INTERFACE

- OPERATES IN BOTH READ AND WRITE MODES
- SHIVA COMPATIBLE PROTOCOL

MOTOR / VCM CONTROL

- MOTOR CONTROL SAME AS KONI / NEKO
- PWM CIRCUIT REDESIGN
  - 13 EFFECTIVE BITS

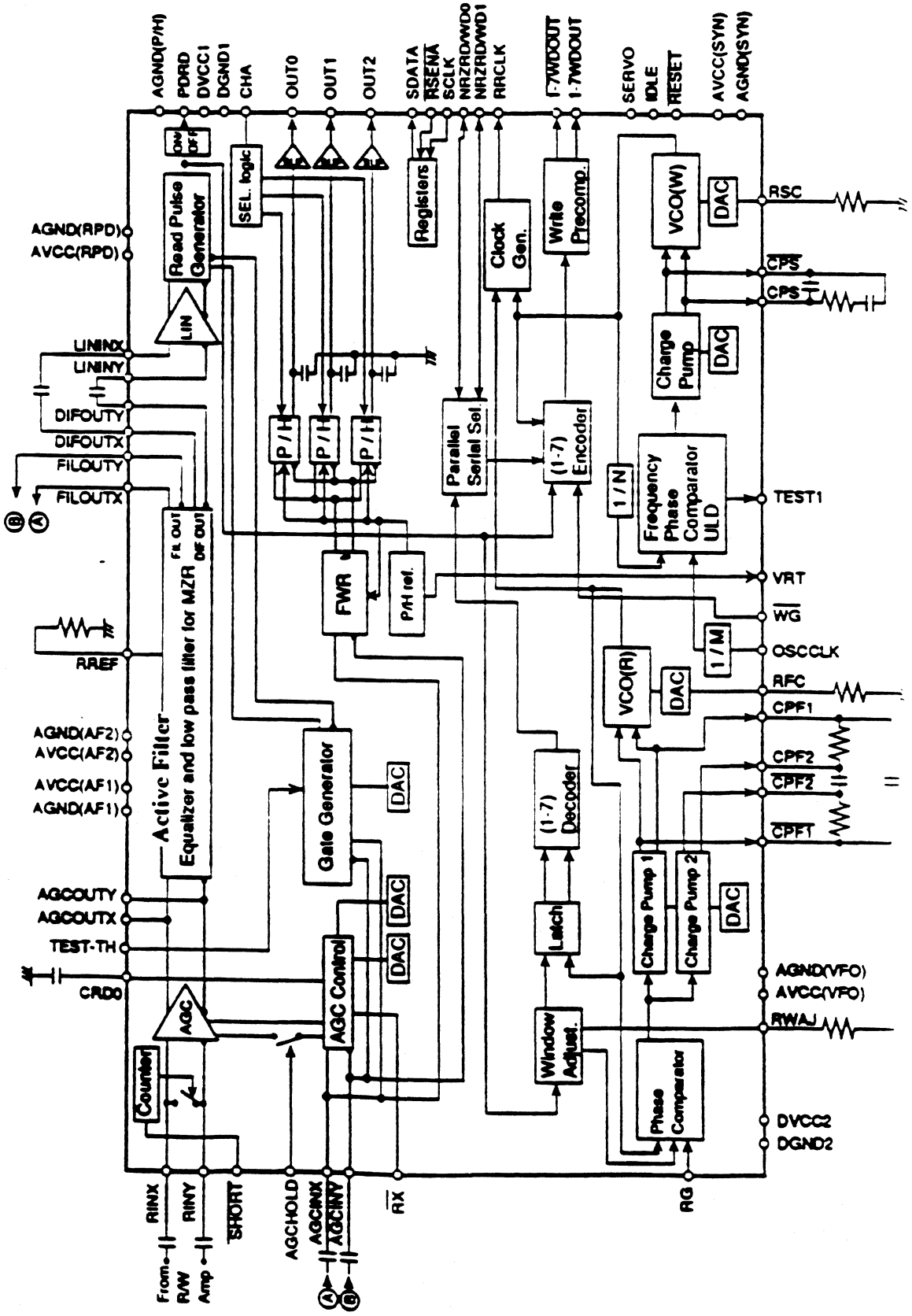
MICRO INTERFACE

- **NOW SUPPORTS BOTH 8 AND 16 BIT PROCESSORS**
  - **WE USE 8 BIT NEC 78352 ON TRAILBLAZER**

ECC BLOCK

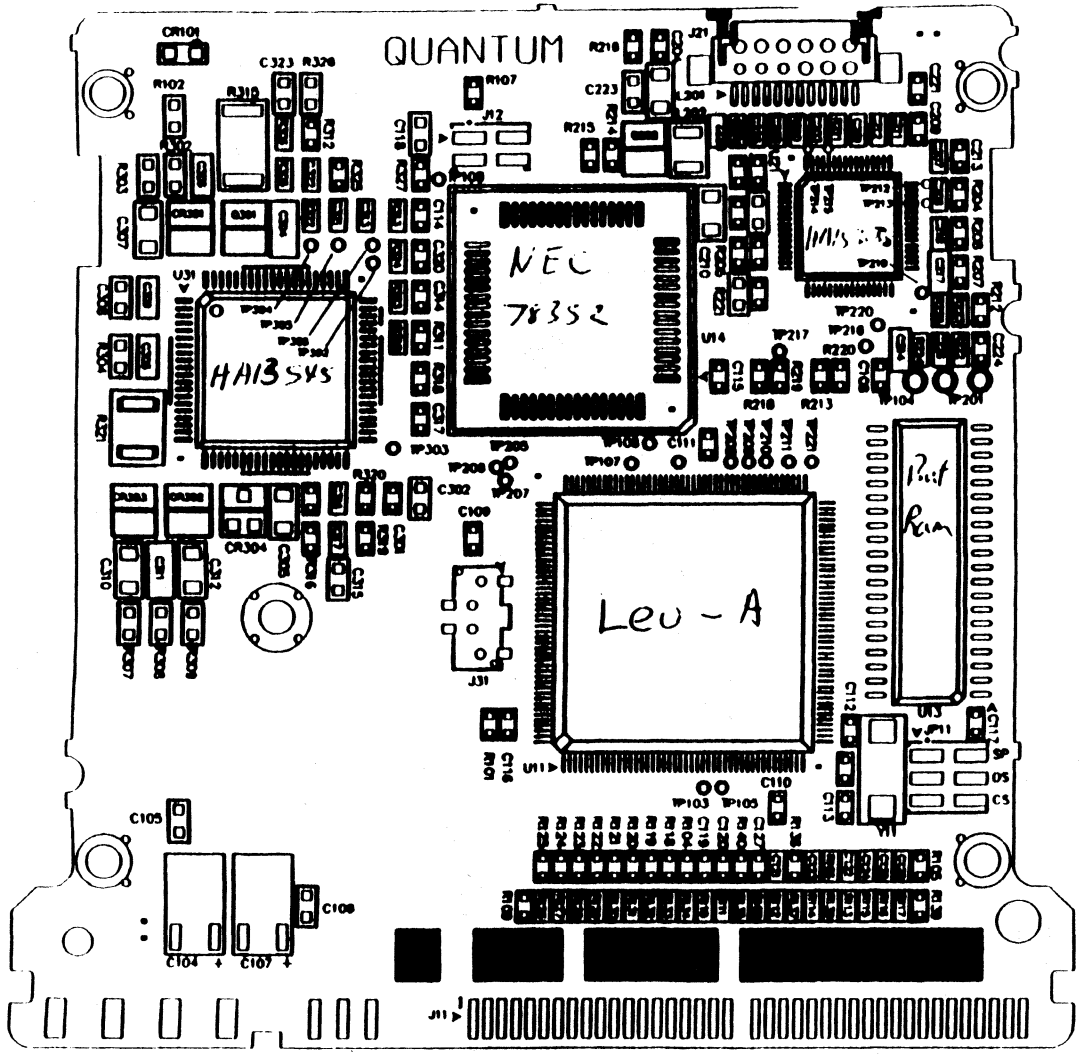
- 3 INTERLEAVES
- 18 ECC AND 2 CROSS-CHECK BYTES
- INCREASED CORRECTION CAPABILITY
  - GUARANTEED CORRECTION SPAN
    - SINGLE BURST - 17 BITS (ON THE FLY)
    - DOUBLE BURST - 41 BITS (ON THE FLY)
    - TRIPLE BURST - 65 BITS (OFFLINE)

Block diagram



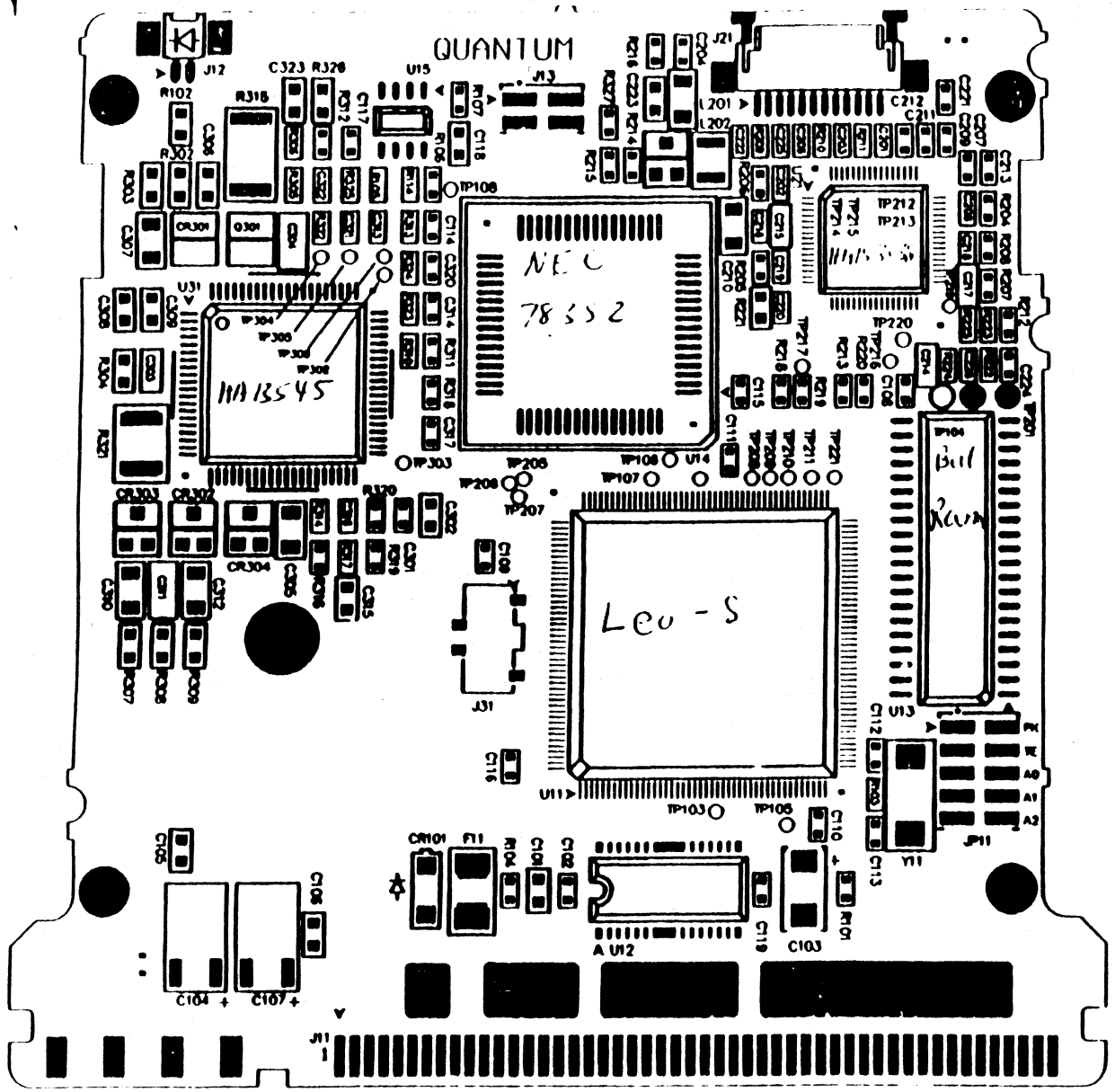
TRAILBLAZER CHANNEL ADAPTATION

PARAMETER	RANGE	STEP
Window Centering	+- 2.4 ns	0.3 ns
Write Current	4 to 16 ma	0.1 ma
Bandwidth	Per Zone	243 KHz
Boost	10 db	1 db
Write Precomp	1.6 ns	0.8 ns



1.2 Assembly Drawing
TRB AT PCB P1-

20-107770-01 ver2.0



TRB SCSI PCB P1

20-107780-01 ver 1.0

1.3 SYSTEM ENVIRONMENT

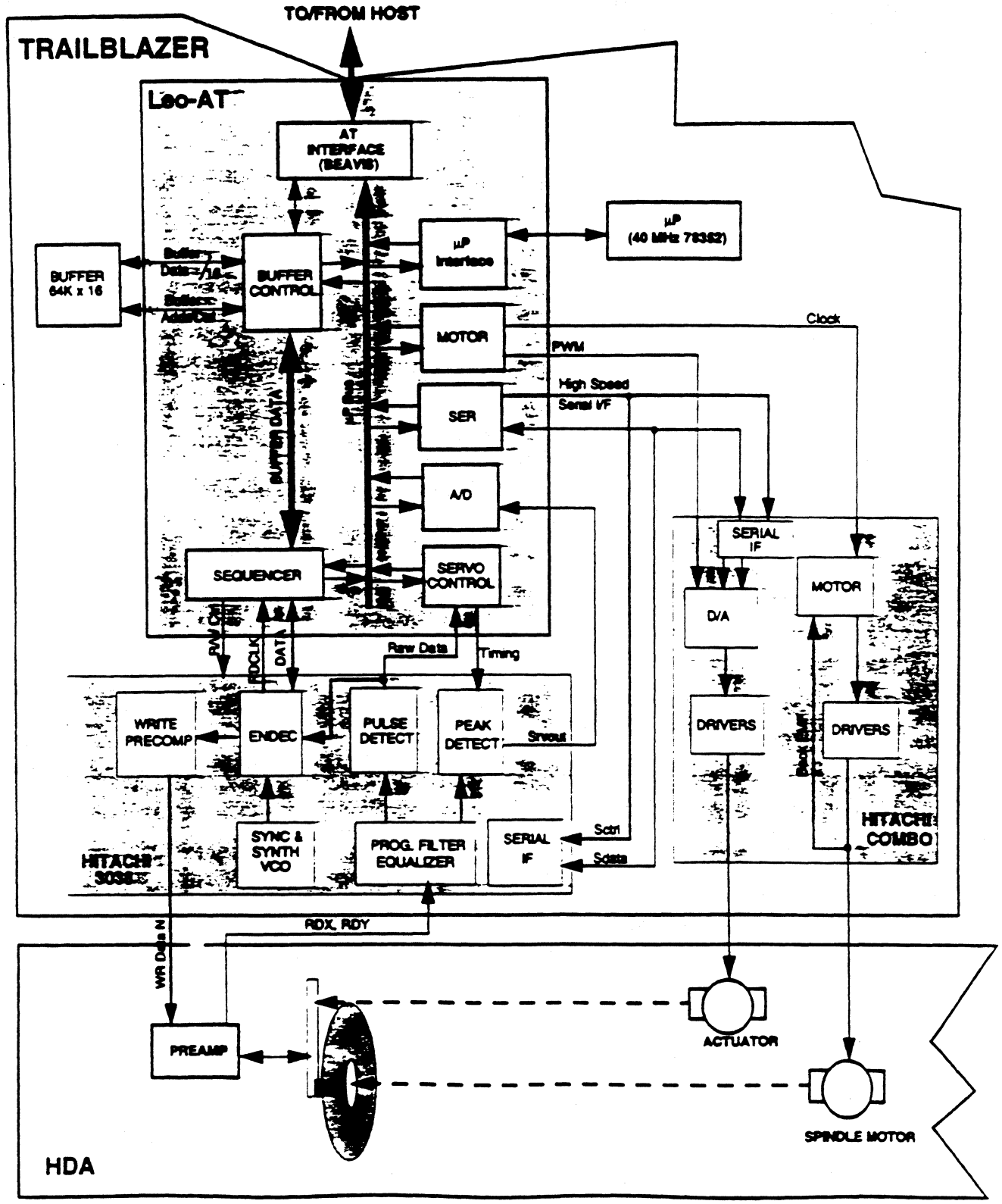
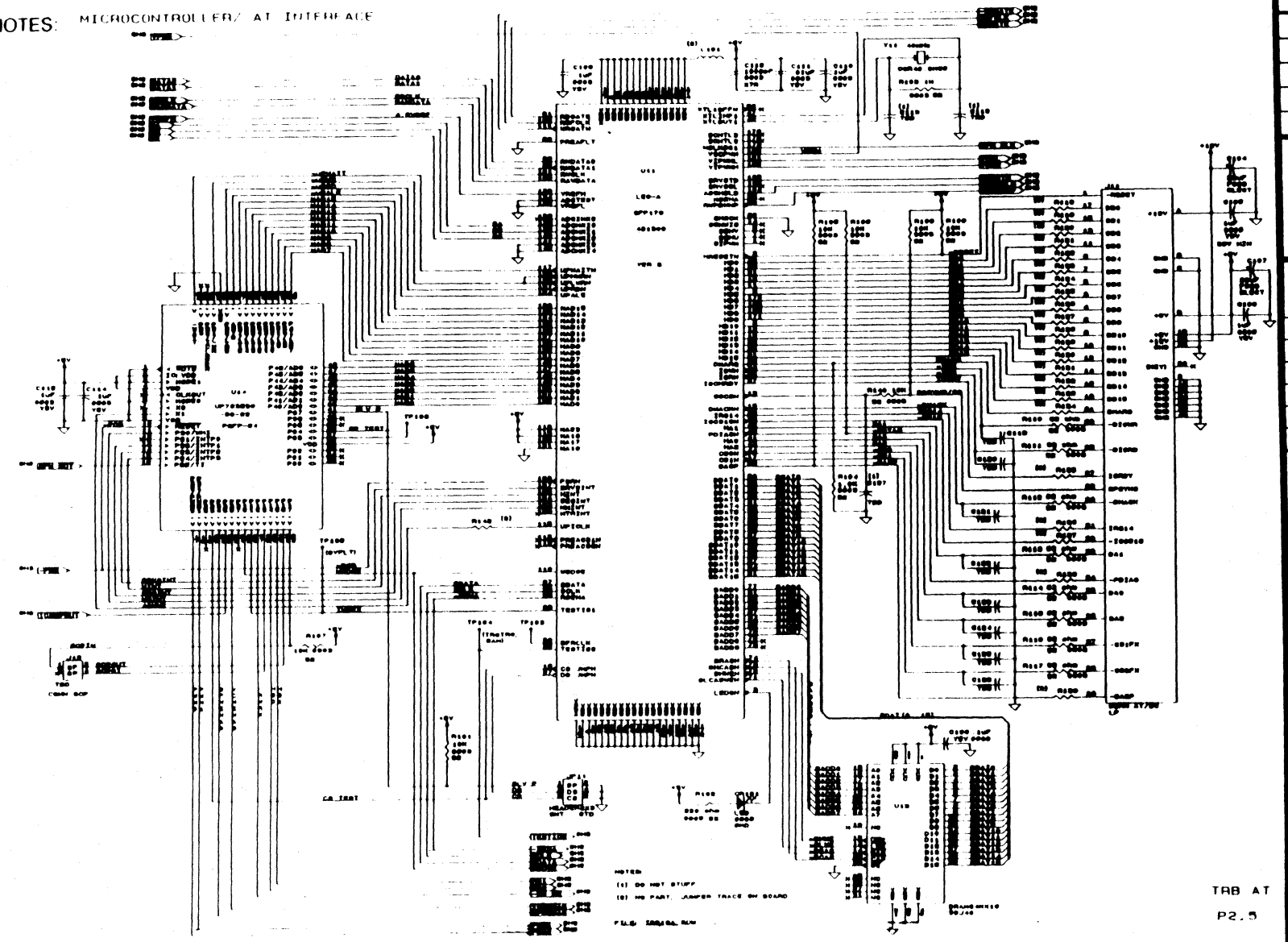


Figure 1-1. System Block Diagram

NOTES: MICROCONTROLLER/ AT INTERFACE



REV	EC	DATE	CK	SIGN

METRIC
TOLERANCES IN MILLIMETERS
THIRD ANGLE PROJECTION

LINEAR ≤4	± 0.10	
>4 ≤16	± 0.20	
>16 ≤63	± 0.30	
>63 ≤250	± 0.50	
>250	± 0.80	
ANGULAR	±1°	

MATERIAL

FINISH

DRAWN BY | DATE 21/7/95

Quantum

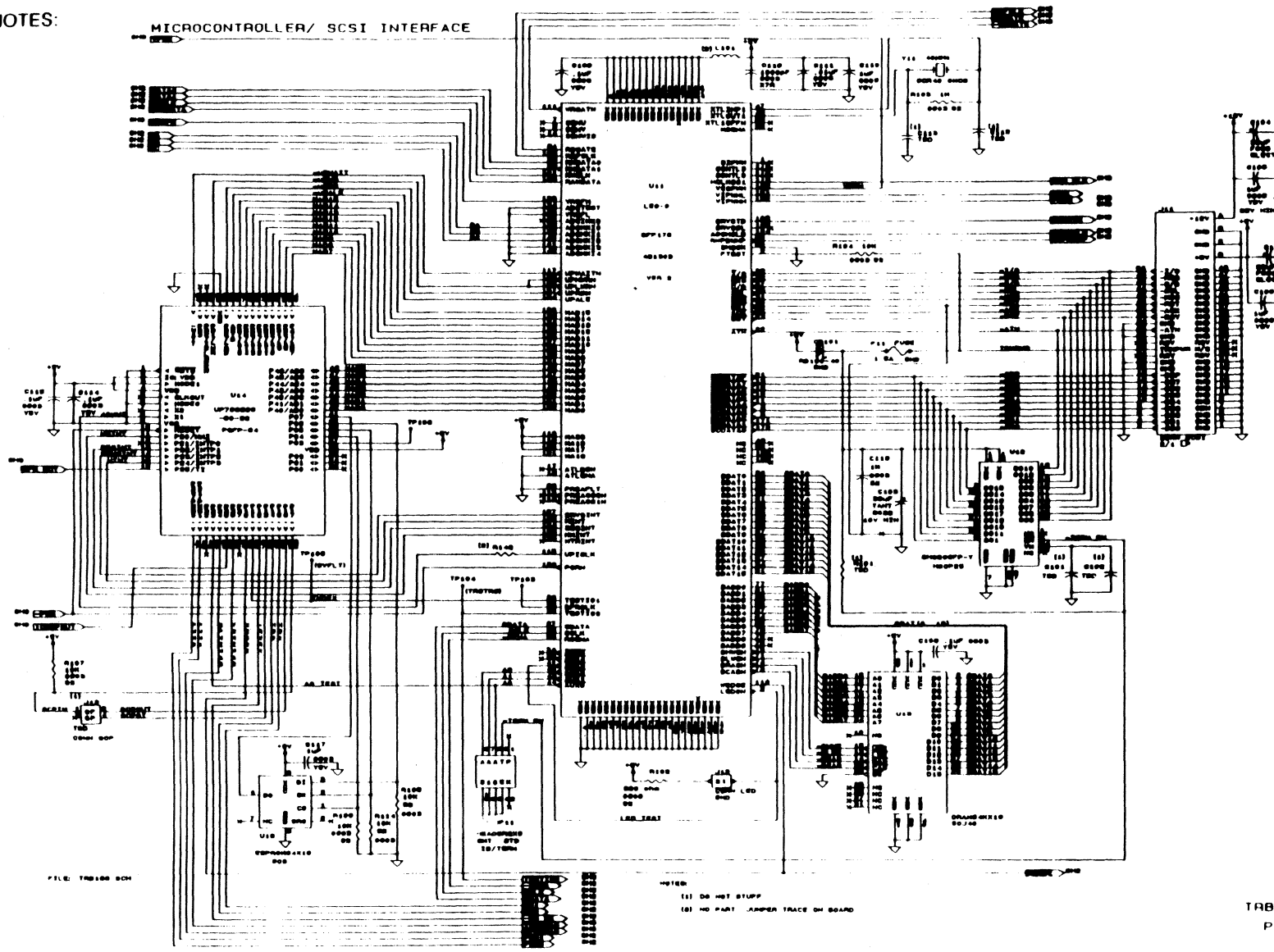
TITLE

TRB AT
P2.5

SIZE	SCALE	SHEET
B		1 OF 3

PART NUMBER 80-107710-05 | REV

NOTES:



REV	EC	DATE	CK	SIGN

METRIC
TOLERANCES IN MILLIMETERS
THIRD ANGLE PROJECTION

LINEAR ≤ 4	± 0.10
>4 ≤ 16	± 0.20
>16 ≤ 63	± 0.30
>63 ≤ 250	± 0.50
>250	± 0.80
ANGULAR	±1°

MATERIAL

FINISH

DRAWN BY

DATE 2/7/95

Quantum

TITLE

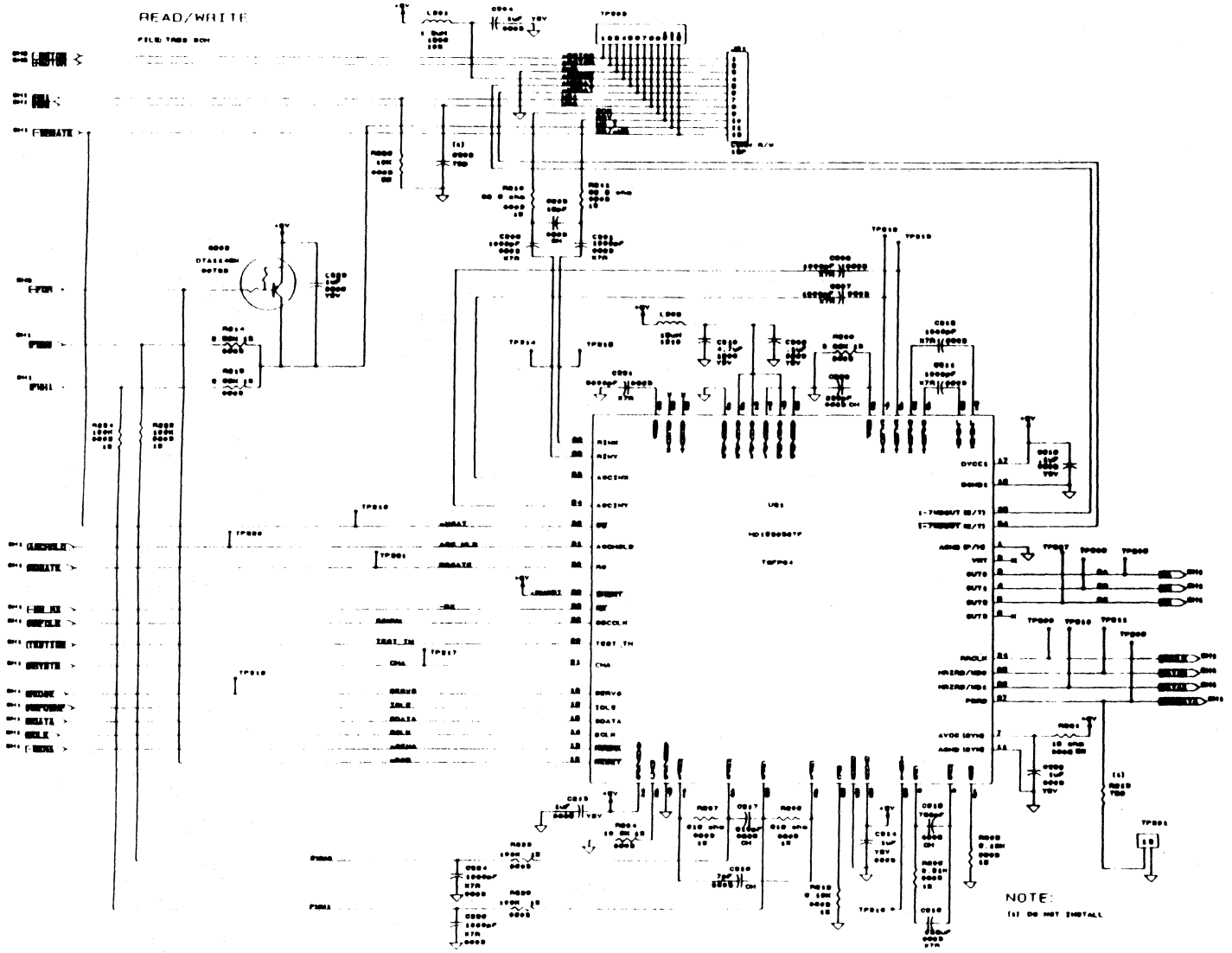
SIZE	SCALE	SHEET
B		1 OF 3

PART NUMBER 80-107780-03

REV 2.5

4 3 2 1

NOTES:



REV	EC	DATE	CK	SIGN

METRIC
TOLERANCES IN MILLIMETERS
THIRD ANGLE PROJECTION

LINEAR ≤4	± 0.10	
>4 ≤16	± 0.20	
>16 ≤63	± 0.30	
>63 ≤250	± 0.50	
>250	± 0.80	
ANGULAR	±1°	

MATERIAL

FINISH

DRAWN BY DATE
2/17/95

Quantum

TITLE

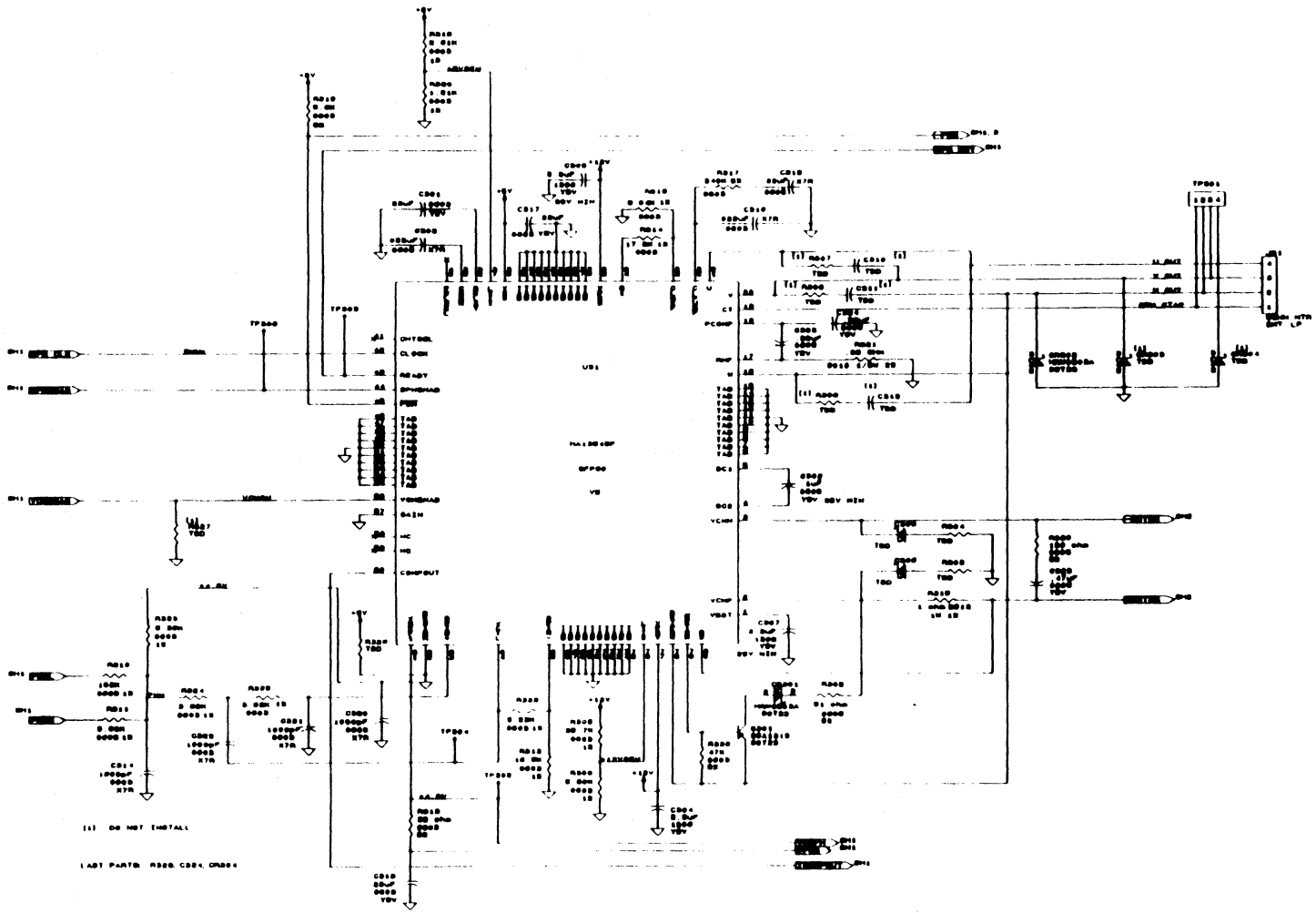
SIZE	SCALE	SHEET
B		2 OF 3

PART NUMBER
80 107770-05
80 107780-03

REV
A5

NOTES:

MOTOR/VCM



REV	EC	DATE	CK	SIGN

METRIC
TOLERANCES IN MILLIMETERS
THIRD ANGLE PROJECTION

LINEAR	≤ 4	± 0.10	
>4	≤ 16	± 0.20	
>16	≤ 63	± 0.30	
>63	≤ 250	± 0.50	
>250		± 0.80	
ANGULAR		±1°	

MATERIAL

FINISH

DRAWN BY

DATE 2/17/95

Quantum

TITLE

SIZE B | SCALE | SHEET 3 OF 3

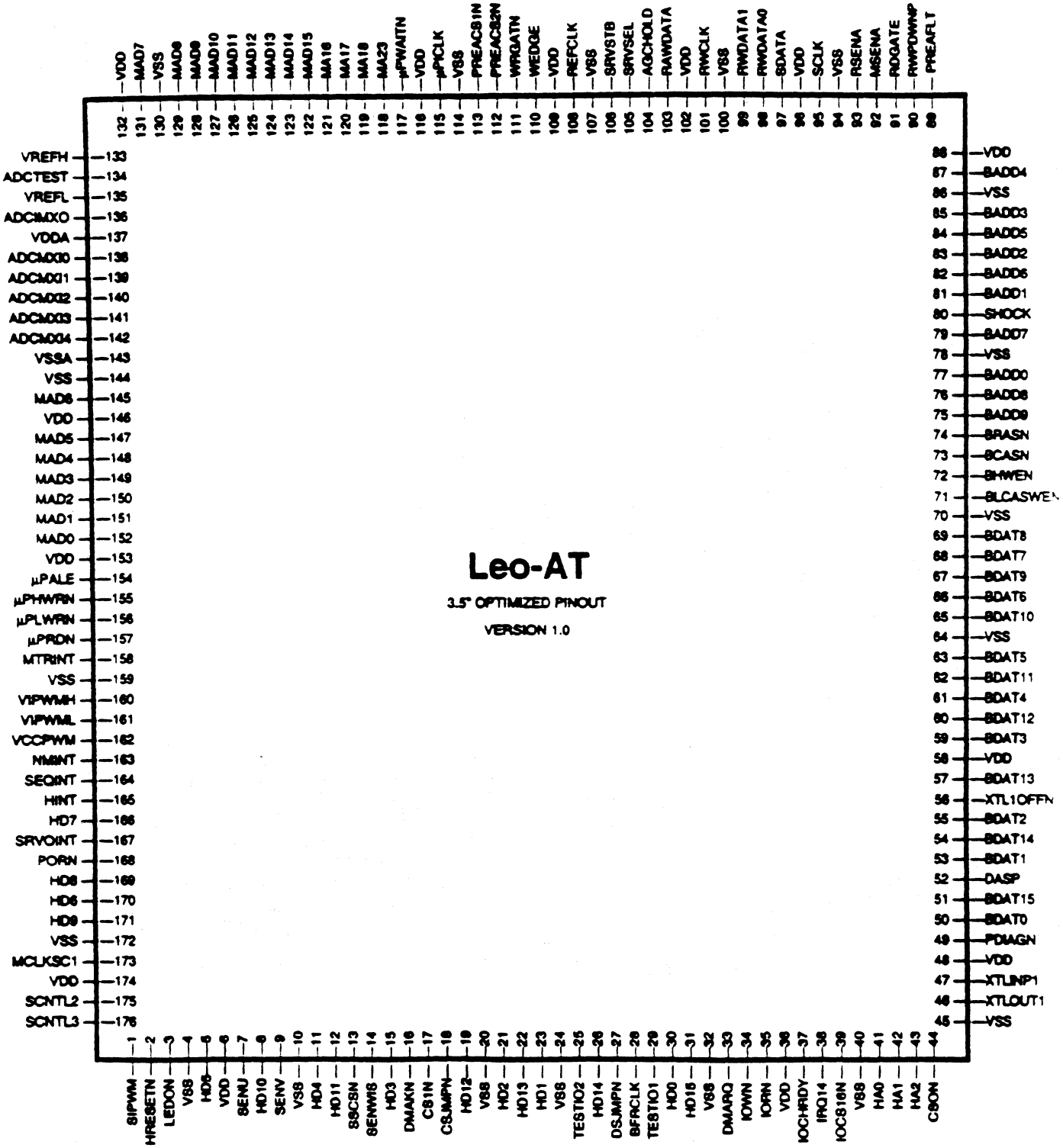
PART NUMBER 80-107770-05
80-107780-03

REV 25

Appendix A

TESTING POINTS LIST

Reference	Description	Comment
TP103	BFRCLK	Sheet 1of SCH
TP104	SAM, TRGTRG	
TP105	Index, SVFLT	
TP108	uP, P03	
TP201	For window margin measurement (with R213 installed)	Sheet 2of SCH
TP205	Servo Burst A	
TP206	Servo Burst B	
TP207	Servo Burst C	
TP208	Raw DATA	
TP209	Read Clock	
TP210	DATA1 of NRZ	
TP211	DATA0 of NRZ	
TP212	Differential output X after filter	
TP213	Differential output Y after filter	
TP214	Differential input Y after PreAmp	
TP215	Differential input X after PreAmp	
TP216	Output Test Signal of HD153038	
TP217	Sampling Control Signal of SA,SB,SC	
TP218	Servo mode/Read mode	
TP219	Write Gate	
TP220	AGCHOLD	
TP221	Read Gate	
TP303	Spindle Ready	Sheet 2of SCH
TP304	Control Signal for VCM driver	
TP305	Voltage Reference	
TP306	Spindle Enable	



Hung Nguyen R2 10/5/94

Table 5-1. Leo-AT Pin List

SIGNAL	QTY	I/O Type	IOL mA	IOH mA	RP uA	Load pf	Fmx Mhz	Pin #	DESCRIPTION
SYSTEM									Total 38 pins
XTLINP1	1	I A - - -					40	47	Crystal input 1 (40MHZ)
XTLOUT1	1	O A - - -					40	46	Crystal output 1 (40MHZ)
PORN	1	I T H - -			10		<1	168	Power On reset
LEDON	1	O - - O S	24			25	<1	3	24ma Open Drain LED driver, when this signal is low level the LED turn on
TESTIO1	1	B T H 3 S	4	4	10	25	20	29	Test input/output 1 can be used for trigger in or multiplex output signal SONCE, TESTCLK, SCI_TRIGGER, BRSTRDY, SAMFLT, SVOFLT, WFAULT.
TESTIO2	1	O - - 2 S	4	4		25	20	25	Test output 2 can be used for multiplex output signals SPDERR, SAM, ADCTSTO, TRGOUT, LSYNDN0, LCRCN0, LCM0N0, BDTEST.
VSS	21	O - - - -						--->	Ground at pins # 4, 10, 20, 24, 32, 40, 45, 64, 70, 78, 86, 94, 100, 107, 114, 130, 144, 159, 172.
VDD	11	I - - - -						--->	Power at pins #: 6, 36, 48, 58, 88, 96, 102, 109, 116, 132, 146, 153, 174.
A/D I/F									Total 12 pins
VREFH	1	I A - - -						133	Voltage reference high for A/D
VREFL	1	O A - - -						135	Voltage reference low for A/D
VSSA	1	O A - - -						143	Analog ground pin
VDDA	1	I A - - -						137	Analog power pin
ADCMXI(4:0)	5	I A - - -					<1	--->	A/D Mux inputs which are sequential vertially scanned. Pin # 142,141,140,139,138.
ADCIMXO	1	B A - - -					<1	136	A/D In and Mux out for testing.
SRVSEL	1	O - - 2 S	4	4		25	<1	105	Servo select signal to R/W SHIVA/LITE2.
ADCTEST	1	I T H - -			100D		<1	134	For ADC testing only. Note that this pin needs to connect to Ground for the Chip functioning.
AT I/F									Total 34 pins
HD(15:0)	16	B T H 3 S			10	200*	5	--->	Host data bus at pins # starting from MSB (HD-15). Pin # 31, 26, 22, 19, 12, 8, 171, 169, 166, 170, 5, 11, 15, 21, 23, 30.
HA(2:0)	3	I T H - -			10		<1	--->	Host address bus at pins # starting from MSB (HA-2). Pin # 43,42,41.
CS0N	1	I T H - -			10		<1	44	Host chip select 0.
CS1N	1	I T H - -			10		<1	17	Host chip select 1.
IORN	1	I T H - -			10		5	35	Host read strobe.
IOWN	1	I T H - -			10		5	34	Host write strobe.

Table 5-1. Leo-AT Pin List

SIGNAL	QTY	I/O Type	IOL mA	IOH mA	RP uA	Load pf	Fmx Mhz	Pin #	DESCRIPTION
IRQ14	1	O - - 3 S	[redacted]	[redacted]		200*	<1	38	Interrupt to Host.
IOCS16N	1	O - - O S	[redacted]			200*	<1	39	Indicates 16 bits IO.
IOCHRDY	1	O - - O S	[redacted]			200*	<1	37	I/O channel ready.
DMARQ	1	O - - 3 S	[redacted]	[redacted]		200*	5	33	DMA request to Host, this pin needs 1K external P.D.
DMACKN	1	I T H - -			10		5	16	Host DMA acknowledge.
HRESETN	1	I T H - -	[redacted]				<1	2	Host power on reset, this pin needs 10K external P.U.
PDIAGN	1	B T H O S	[redacted]			200*	<1	49	Passed diagnostics, this pin needs 10K external P.U.
SSCSN	1	I T H - -					<1	13	Spindle sync / Cable select, this pin needs 10K external P.U.
DASP	1	B T H O S	[redacted]			200*	<1	52	Drive active/slave present (24ma), this pin needs 10K external P.U.
DSJMPN	1	I T H - -			5	-	<1	27	Drive Select input port .
CSJMPN	1	I T H - -			5	-	<1	18	Cable select input port .
UP I/F									Total 32 pins
MAD(15:0)	16	B T H 3 S	4	4	100	25	5	--->	Microprocessor multiplexed address/data. Pin # starting from MSB (MAD-15). Pin # 122,123,124,125, 126,127,128,129,131,145,147,148,149,150, 151,152.
MA23	1	I T H			100	25	5	118	Microprocessor address 23
MA(18:16)	3	I T H			100	25	5	--->	Microprocessor address at pins # starting from MSB (MA-18). Pin # 119,120,121.
UPWAITN	1	O - - 2 S	4	4		25	5	117	Microprocessor wait.
UPALE	1	I T H - -			100d		5	154	Microprocessor Address latch.
UPRDN	1	I T H - -			10		5	157	Microprocessor I/O read.
UPLWRN	1	I T H - -			10		5	156	Microprocessor low byte I/O write.
UPHWRN	1	I T H - -			10		5	155	Microprocessor upper byte I/O write.
SEQINT	1	O - - 2 S	4	4		25	<1	164	Sequencer interrupt to Microprocessor (from SEQ).
NMINT	1	O - - 2 S	4	4		25	<1	163	NMI interrupt to Microprocessor (from ATIF or SCIF module, host reset to Microprocessor or sleep exit).
SRVOINT	1	O - - 2 S	4	4		25	<1	167	Servo interrupt to Microprocessor (from TNA).
HINT	1	O - - 2 S	4	4		25	<1	165	Host interrupt to Microprocessor (from ATIF and SCIF).
UPICLK	1	O - - 2 S	8	8		25	40	115	Microprocessor clock, programmable 8,16,10,20 or 32Mhz.
XTL1OFFN	1	O - - O S					<1	56	Turn off Crystal 1 (40MHZ).
REFCLK	1	O - - 2 S	4	4		25	40	108	Reference clock for R/W SHIVA/LITE2 (40 MHZ).
DRAM I/F									Total 31 pins

Table 5-1. Leo-AT Pin List

SIGNAL	QTY	I/O Type	IOL mA	IOH mA	RP uA	Load pf	Fmax Mhz	Pin #	DESCRIPTION
BLCASWEN	1	O - - 2 S	4	4		25	10	71	Buffer lower byte write enable.
BHWEN	1	O - - 2 S	4	4		25	10	72	Buffer higher byte write enable.
BRASN	1	O - - 2 S	4	4		25	5	74	Buffer row address strobe.
BHCASN	1	O - - 2 S	4	4		25	10	73	Buffer column address strobe.
BADD(9:0)	10	O - - 2 S	4	4		25	10	--->	Buffer address upto 256Kx16 DRAM at pins # starting from MSB (BADD-9). Pin # 75,76,79,82,84,87,86,83,81,77.
BDAT(15:0)	16	B T H 3 S	4	4	100d	25	10	--->	Buffer data for and interface chip at pin # starting from MSB (BDAT-15). Pin# 51,54,57,60,62,65, 67,69,68,66,63,61,59,55,53,50.
BFRCLK	1	I T H - -			10	-	50	28	External buffer clock.
MOTOR I/F									Total 11 pins
MCLKSC1	1	O C - 2 -					<1	173	Mux between PHASE1 signal which is the Spindle Phase1 CMOS output to Motor MIGHTY , using a six state phase commutation sequence (132645) and MCLK signal which is the Motor clock for Motor PEACHFUZZ , it can be Programmed to 1Mhz, 3Mhz, 5Mhz, 10Mhz or turn-off.
SCNTL2	1	O C - 2 -					<1	175	Spindle Phase2 CMOS output to MTR MIGHTY , using a six state phase commutation sequence (132645).
SCNTL3	1	O C - 2 -					<1	176	Spindle Phase3 CMOS output to MTR MIGHTY , using a six state phase commutation sequence (132645).
SENU	1	I T H - -			10		<1	7	Sense phase U is driven by MTR MIGHTY which is the output of BEMF or current sense comparator.
SENV	1	I T H - -			10		<1	9	Sense phase V is driven by MTR MIGHTY which is the output of BEMF or current sense comparator.
SENWIS	1	I T H - -			10		<1	14	Sense phase W is driven by MTR MIGHTY which is the output of BEMF or current sense comparator.
SIPWM	1	O C - 2 -					<1	1	The pulse width modulated CMOS output to MTR MIGHTY to control the motor current, which requires symmetrical rise & fall times at 30pf.
VIPWMH	1	O C - 2 -					<1	160	The pulse width modulated most significant bit CMOS output to MTR MIGHTY to control the voice coil current, which requires symmetrical rise & fall times at 30pf.
VIPWML	1	O C - 2 -					<1	161	The pulse width modulated least significant bit CMOS output to MTR MIGHTY to control the voice coil current, which requires symmetrical rise & fall times at 30pf.

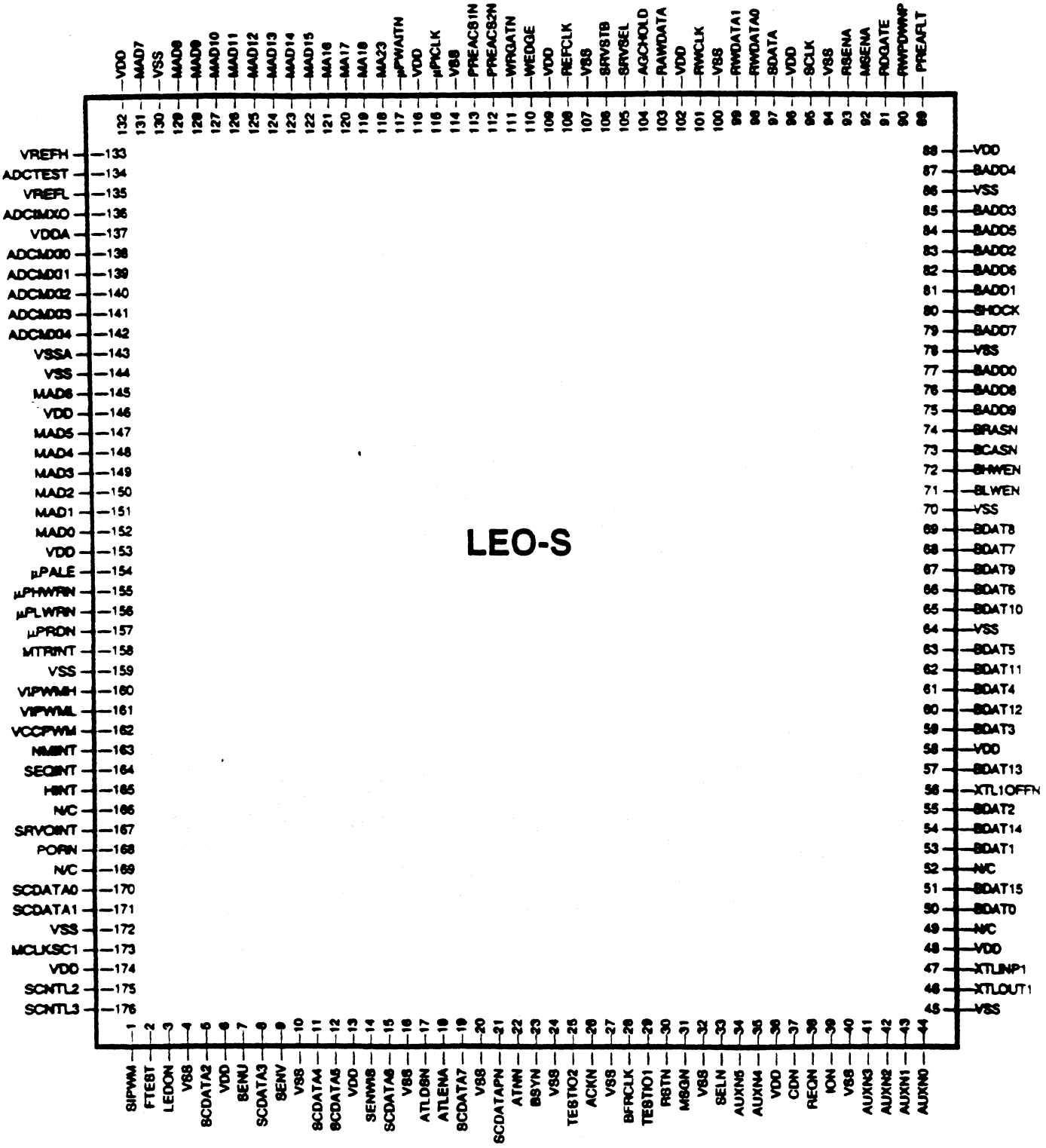
Table 5-1. Leo-AT Pin List

SIGNAL	QTY	I/O Type	IOL mA	IOH mA	RP uA	Load pf	Fmx Mhz	Pin #	DESCRIPTION
VCCPWM	1	I A - - -						162	Voltage reference high for The pulse width modulated.
MTRINT	1	O - - 2 S	4	4			<1	158	Motor Interrupt, occurs once per revolution for speed correction.
SERIAL I/F									Total 4 pins
SDATA	1	B T H 3 S	4	4		25	5	97	Serial data for MTR PEACHFUZZ & R/W SHIVA/LITE2.
SCLK	1	B T H 3 S	4	4		25	40	95	Serial clock for MTR PEACHFUZZ @ 10Mhz & R/W SHIVA/LITE2 @ 40Mhz.
MSENA	1	O - - 2 S	4	4			<1	92	Serial enable for MTR PEACHFUZZ.
RSENA	1	O - - 2 S	4	4			<1	93	Serial enable for R/W SHIVA/LITE2
SERVO I/F									Total 4 pins
WEDGE	1	O - - 2 S	4	4		25	<1	110	Servo field for R/W SHIVA/LITE2.
SRVSTB	1	O - - 2 S	4	4		25	<1	106	Servo strobe signal to R/W SHIVA/LITE2.
AGCHOLD	1	O - - 2 S	4	4		25	<1	104	The AGCHOLD will lock the AGC amplifier gain. This signal is active high for R/W SHIVA/LITE2.
RAWDATA	1	I T H - -			10	-	36	103	Raw data from the pulse detector of R/W SHIVA/LITE2.
SHOCK	1	B T H 3 S			100d		<1	80	Shock sensor input. Output for ADC test.
R/W I/F									Total 9 pins
RDGATE	1	O - - 2 S	4	4		25	<1	91	Read Gate for R/W SHIVA/LITE2.
RWDATA0	1	B T H 3 S			10	-	50	98	Write data 0 to PREAMP chip or synchronized Read Data 0 from PLL in R/W SHIVA/LITE2
RWDATA1	1	B T H 3 S			10	-	50	99	Write data 1 to PREAMP chip or synchronized Read Data 1 from PLL in R/W SHIVA/LITE2.
RWCLK	1	I T H - -			10	-	50	101	Read/Write data clock from R/W SHIVA/LITE2, RD/WR switch deglitched by LEO chip.
WRGATN	1	O - - 2 S	4	4		25	<1	111	Write Gate, active low for R/W SHIVA/LITE2 & PREAMP chip.
RWPDWNP	1	O - - 2 S	4	4		25	<1	90	Read/Write Power Down signal for R/W SHIVA/LITE2. This signal is enable when WEDGE changes high to low and disable before next WEDGE goes low to high, the time between RWPDWNP goes high to low and WEDGE is programmable
PREACS1N	1	O - - 2 S	4	4		25	<1	113	Preamp chip select 1. This pin is low active and can be set to a static mode, ie. the signal will stay high or low once it is set. OR it can be set to toggle in Sync as the RWPDWNP pin.
PREACS2N	1	O - - 2 S	4	4		25	<1	112	Preamp chip select 2. This pin is low active and can be set to a static mode, ie. the signal will stay high or low once it is set. OR it can be set to toggle in Sync as the RWPDWNP pin.

Table 5-1. Leo-AT Pin List

SIGNAL	QTY	I/O Type	IOL mA	IOH mA	RP uA	Load pf	Fmx Mhz	Pin #	DESCRIPTION
PREAFLT	1	I T H - -	4	4	10	25	<1	89	Preamp fault signal active high from the R/W preamplifier. In Read mode a fault is caused by thermal asperity, capacitance discharge etc. and in Write mode a fault is caused by WDI frequency out of spec., No write current etc.

0.0.1 LEO-S Pin List



Hung Nguyen 03/24/94

0.0.1 LEO-S Pin List

Leo Pin List

JDo 11/09/94 - REV B2

Table 5-2. LEO-S Pin List

SIGNAL	QTY	I/O TYPE	IOL mA	IOH mA	RP µA	LOAD pF	Fmx MHz	Pin No.	DESCRIPTION
SYSTEM									Total 45 pins
XTLINP 1	1	IA_ _ _					40	47	Crystal input 1 (40MHZ)
XTLOUT1	1	OA _ _ _					40	46	Crystal output 1 (40MHZ)
PORN	1	I TH_ _	10		10		<1	168	Power On Reset
LEDON	1	O_ _OS	24			25	<1	3	24 mA Open Drain LED driver, when this signal is low level the LED turns on.
TESTIO1	1	BTHSS	4	4	10	25	2.0	29	Test Input/Output 1 can be used for trigger in or multiplex output signals: SVOFLT, WFAULT, SONCE, TRGOUT, and SAM.
TESTIO2	1	BTHJS			10	25	20	25	Test Input/Output 2 can be used for trigger in or multiplex output signals: LSYNDN0, LCRCN0, LCMPN0, BDOP, and ADCTEST.
VSS	21	O_ _ _ _							Ground Pin #: 4, 10, 16, 20, 24, 27, 32, 40, 45,84, 70, 78, 86, 94, 100, 107, 114, 130, 144, 159, 172.
VDD	14	I_ _ _ _							Power Pin #: 6, 13, 36, 48, 58, 88, 96, 102, 109, 116,132,146, 153, 174
N/C	4								Spare pins (N/C) Pin #: 49, 52, 166, 169.
A/D I/F (ADC)									Total 12 pins
VREFH	1	IA_ _ _						133	Voltage reference high for the A/D
VREFL	1	IA _ _ _						135	Voltage reference low for the A/D
VSSA	1	IA_ _ _						143	Analog ground pin
VDDA	1	IA_ _ _						137	Analog power pin
ADCMDI(4:0)	5	IA_ _ _					<1		A/D Mux sequential inputs (vertically scanned) Pin #: 142, 141, 140, 139, 138.
ADCIMXO	1	BA_ _ _					<1	136	A/D In. and Mux out for test.
SRVSEL	1	OC_2S	4	4		25	<1	105	Servo select signal to R/W Shive/Lilit2
ADCTEST	1	ITH_ _ _			100d		<1	134	For ADC test only. Note: This pin needs to be connected to ground for proper chip operation.
SCSI I/F (SC IF)									Total 26 pins
SCDATA(7:0)	8	BTHOS	48			200*	5		SCSI Data Bus Pin #: 19, 15, 12, 11, 8, 5, 171, 170.
SCDATAPN	1	BTHOS	48			200*	5	21	SCSI Data Parity.
ATNIN	1	BTHOS	24			200*	<1	22	SCSI Attention.
BSYN	1	BTHOS	48			200*	<1	23	SCSI Busy.
REON	1	BTHOS	48			200*	10	38	SCSI Request.
ACKN	1	BTHOS	24			200*	10	28	SCSI Acknowledge.
RSTN	1	BTHOS	24			200*	< 1	30	SCSI Reset.
MSGN	1	BTHOS	48			200*	<1	31	SCSI Message.
SELN	1	BTHOS	48			200*	< 1	33	SCSI Select.
CDN	1	BTHOS	48			200*	<1	37	SCSI Command/Data.
ION	1	BTHOS	48			200*	<1	39	SCSI Input/Output.
AUXN(5:0)	6	BTHOS	4		100	85	<1		SCSI Auxiliary - Differential Control Pin #: 34, 35, 41, 42, 43, 44.

Table 5-2. LEO-S Pin List

SIGNAL	QTY	I/O TYPE	IOL mA	IOH mA	RP µA	LOAD pF	Fmax MHz	Pin No.	DESCRIPTION
FTEST	1	ITH_ _			100d		<1	2	SCSI fuse test.
µP I/F (µPI)									Total 33 pins
MAD(15:0)	16	BTH3S	4	4	100	25	5		Microprocessor Multiplexed Address/Data. Pin numbering starts from the MSB (MAD bit-15). Pin#: 122, 123, 124, 125, 126, 127, 128, 129, 131, 145, 147, 148, 149, 150, 151, 152.
MA23	1	ITH_ _			100	25	5	118	Microprocessor Address 23
MA(18:16)	3	ITH_ _			100	25	5		Microprocessor Address Pin numbering starts from MSB (MA bit-18) Pin#: 119,120,121.
µPWAITN	1	O_ _2S	8	8		25	5	117	Microprocessor wait.
µPALE	1	ITH_ _			100d		5	154	Microprocessor Address latch.
µPRDN	1	ITH_ _			100		5	157	Microprocessor I/O read.
µPLWRN	1	ITH_ _			100		5	156	Microprocessor low byte I/O write.
µPHWRN	1	ITH_ _			100		5	155	Microprocessor upper byte I/O write.
SEQINT	1	O_ _2S	4	4		25	<1	164	Sequencer interrupt to Microprocessor (from the SEQ).
NMINT	1	O_ _2S	4	4		25	<1	163	NMI interrupt to the Microprocessor (from the SC IF module, host reset to Microprocessor or sleep exit).
SRVOINT	1	O_ _2S	4	4		25	<1	167	Servo interrupt to the Microprocessor (from the TNA)
HINT	1	O_ _2S	4	4		25	<1	165	Host interrupt to the Microprocessor (from the SC IF)
µPCLK	1	O_ _2S	8	8		25	40	115	Microprocessor clock, programmable 10,20 or in 352 Mode and 10, 20 or 40 divide-by-6 in K7 Mode.
REFCLK	1	O_ _2S	4	4		25	40	108	Reference clock for R/W SHIVA/LITE2 (40 MHz).
XTL1OFFN	1	O_ _OS					<1	56	Turn off Crystal 1 (40 MHz).
ATLENA	1	ITH_ _			100d		<1	18	Micro Atlas enable.
ATLDSN	1	ITH_ _			100		<10	17	Micro Atlas data strobe.
DRAM I/F (BFR)									Total 31 pins
BLCASWEN	1	O_ _2S	4	4		25	10	71	Buffer low lower column address byte write enable.
BHWEN	1	O_ _2S	4	4		25	10	72	Buffer high byte write enable.
BRASN	1	O_ _2S	4	4		25	5	74	Buffer row address strobe.
BHCASN	1	O_ _2S	4	4		25	10	73	Buffer high column address strobe.
BADD(9:0)	10	O_ _2S	4	4		25	10		Buffer Address for up to 256Kx16 DRAM Pin numbering starts from MSB (BADD-9) Pin#: 75, 76, 79, 82, 84, 87, 85, 83, 81, 77.
BDAT (15:0)	16	BTH3S	4	4	100d	25	10		Buffer Data for LEO and interface chip. Pin numbering starts from MSB (BDAT bit-15). Pin#: 51,54, 57, 60, 62, 65, 67, 69, 68, 66, 63, 61, 58, 55, 53, 50
BFRCLK	1	ITH_ _			10		50	28	External buffer clock.
MOTOR I/F (MTR)									Total 11 pins
MCLKSC1	1	OC_2_					<l	173	Mux between PHASE1 signal which is the Spindle Phase 1 CMOS output to Motor MIGHTY, using a six state phase commutation sequence (132645) and MCLK signal which is the Motor clock for Motor PEACHFUZZ. It can be Programmed to 1 MHz, 3MHz, 5MHz, 10MHz or turned-off.
SCNTL2	1	OC_2_					<1	175	Spindle Phase2 CMOS output to MTR MIGHTY, using a six state phase commutation sequence (132645).
SCNTL3	1	OC_2_					<1	176	Spindle Phase3 CMOS output to MTR MIGHTY, using a six state phase commutation sequence (132645).
SENU	1	I T H_ _				100d	<1	7	Sense phase U is driven by MTR MIGHTY which is the output of BEMF or current sense comparator.

Table 5-2. LEO-S Pin List

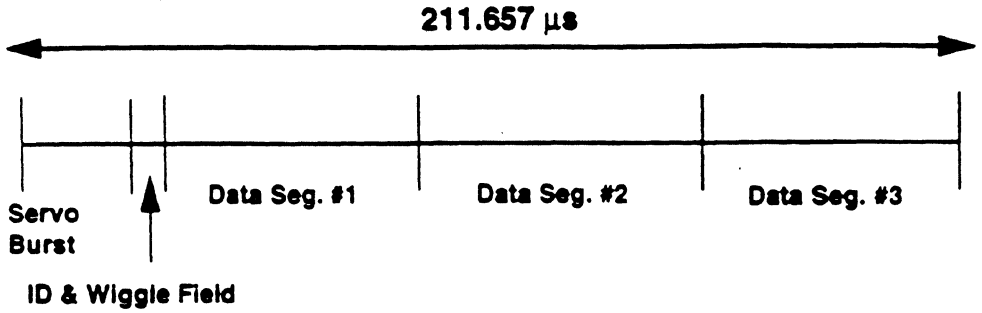
SIGNAL	QTY	I/O TYPE	IOL mA	IOH mA	RP µA	LOAD pF	Fmax MHz	Pin No.	DESCRIPTION
SENV	1	ITH__				100d	<1	9	Sense phase V is driven by MTR MIGHTY which is the output or BEMF or current sense comparator.
SENWS	1	ITH__				100d	<1	14	Sense phase W is driven by MTR MIGHTY which is the output of BEMF or current sense comparator.
SIPWM	1	OC_2_					<1	1	The pulse width modulated CMOS output to MTR MIGHTY to control the motor current. (Requires symmetrical rise & fall times at 30 pF.)
VIPWMH	1	OC_2_					<1	160	The pulse width modulated signal's most significant bit CMOS output to MTR MIGHTY to control the voice coil current. (Requires symmetrical rise & fall times at 30 pF.)
VIPWML	1	OC_2_					<1	161	The pulse width modulated signal's least significant bit CMOS output to MTR MIGHTY to control the voice coil current. (Requires symmetrical rise & fall times at 30 pF.)
VCCPWM	1	IA___	4	4				162	Voltage reference high for the pulse width modulation.
MTRINT	1	O__2 S	4	4			<1	158	Motor Interrupt, occurs once per revolution for speed correction
SERIAL I/F (SER)									Total 4 pins
SDATA	1	BTH3S	4	4		25	5	97	Serial data for MTR PEACHFUZZ and R/W SHIVA/LITE2.
SCLK	1	BTH3S	4	4		25	40	95	Serial clock for MTR PEACHFUZZ @ 10 Mhz and R/W SHIVA/LITE2 @ 40 Mhz.
MSENA	1	O__2 S	4	4			<1	92	Serial enable for MTR PEACHFUZZ.
RSENA	1	O__2 S	4	4			<1	93	Serial enable for R/W SHIVA/LITE2.
SERVO I/F (TNA)									Total 5 pins
WEDGE		O__2 S				25	< 1	110	Servo field for R/W S H IVA/LITE2.
SRVSTB	1	O__2 S	4	4		25	<1	108	Servo strobe signal to R/W SHIVA/LITE2.
AGCHOLD	1	O__2 S	4	4		25	<1	104	ACGHOLD will lock the AGC amplifier gain. This signal is active high for R/W SHIVA/LITE2.
RAWDATA	1	ITH__			10		36	103	Raw data from the pulse detector of the R/W SHIVA/LITE2.
SHOCK	1	ITH__			100d			80	Shock sensor (for Daytona program).
R/W I/F (SEQ)									Total 9 Pins
RDGATE	1	O__2S	4	4		25	<1	91	Read Gate for R/W SHIVA/LITE2.
RWDATA0	1	BTH3S			10		50	98	Write data 0 to PREAMP chip or synchronized Read Data 0 from PLL in R/W SHIVA/LITE2
RWDATA1	1	BTH3S			10		50	99	Write data 1 to PREAMP chip or synchronized Read Data 1 from PLL in R/W SHIVA/LITE2.
RWCLK	1	ITH__2S			10		50	101	Read/Write data clock from R/W SHIVA/LITE2. RD/WR switch deglitched by LEO chip.
WRGATN		O__2S	4	4		25	<1	111	Write Gate, active low for R/W SHIVA/LITE2 and the Preamp chip.
RWPDWNP	1	O__2S	4	4		25	<1	90	Read/Write Power Down signal for R/W SHIVA/LITE2 This signal is enabled when WEDGE changes high to low and disabled before the next WEDGE goes low to high, the time between RWPDWNP goes high to low and WEDGE is programmable.
PREACS1N		O__2S	4	4		25	<1	113	Preamp chip select 1. This pin is low active and can be set to a static mode, i.e. the signal will stay high or low once it is set. Or it can be set to toggle in Sync with the RWPDWNP pin.
PREACS2N	1	O__2S	4	4		25	<1	112	Preamp chip select 2. This pin is low active and can be set to a static mode, i.e. the signal will stay high or low once it is set. Or it can be set to toggle in Sync with the RWPDWNP pin.
PREAFLT	1	ITH__	4	4	10	25	<1	89	Preamp fault signal active high from the R/W preamplifier. In Read mode a fault is caused by thermal asperity, capacitance discharge etc. and in Write mode a fault is caused by WDI frequency out of spec. (No write current etc.)

0.0.1 LEO-S Pin List

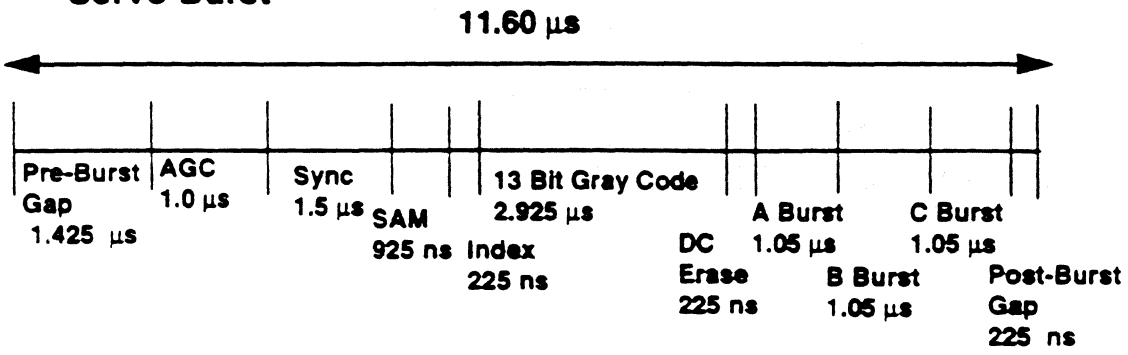
Notes: 1. LEO-S = 176pins.
2. I/O Type = a) I/O/B = In, Out, Bidirect. b) T = TTL; C = CMOS; A = Analog.
c) H = Hysteresis. d) O = Open Drain; 2/3 = 2 or 3 State.
e) S = Slew Lim.
3. IOL/IHH = Low/High Level DC current Drive (min).
4. RP = Resistance Pullup/Down (d = Down).
5. Load = Capacity load (max).
6. Fmx = Maximum frequency.
7. *= Host bus load is based on cable impedance, see separate Host Interface I/O Spec. document for bus model and maximum loads.
8. **= These pin must not sink current when the chip has been powered down (Vdd = Vss = 0V).
9. All signals name ended with an 'N' are negative true enable

Read / Write Channel

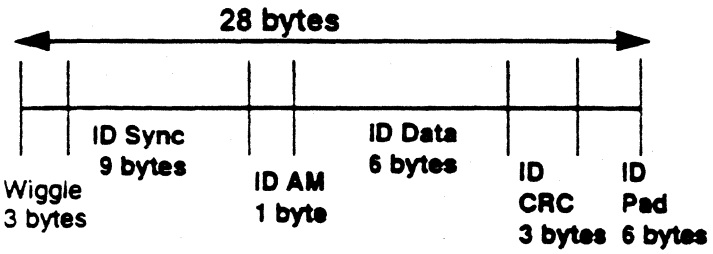
Wedge (63 x's per rev)



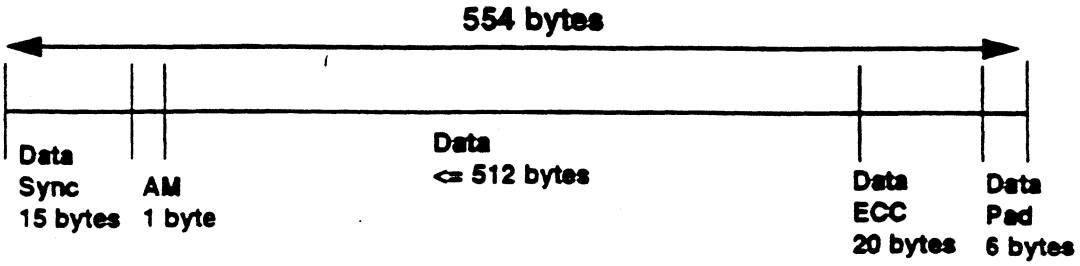
Servo Burst



ID Field



Data Segment



Product: Trail Blazer 420

Rev :3.0 9/29/94 P1 build

Req Cap	421.659	MBytes
Spare	1	per cyl
Surf	2	
Rod	1.7992	in
Rid	0.8310	in
Stroke	0.9682	in
Trk Den	3794	tpi
RPM	4499.64	rpm
Certified cyls	3672	
Data cyls	3653	
Servowritten cyls	3679	

ID as overhead

	Bytes	%
Speed Tol		0.30%
Wiggle	3	
ID Pre	9	
ID AM	1	
ID Data	6	
ID CRC	3	
ID Pad	6	
ID Gap	0	
ID Total	28	

Servo overhead

Srv Fq	40 MHz
Srv Clk	25 nSec
Srv N	464 Clocks
Nservos	63 samples
Wr-Wdg	1.5 uSec
Tservo	11.60 uSec
Tdata	199.42 uSec
Srv OH	5.48 %

AT CHS Set up

Logical Cylinders	1008
Logical Heads	16
Logical sectors	51
Logical Diag. Cyl.	2
Total sectors	824,160
Logical MegaBytes	421.970

Data overhead

Data Pre	15
Data AM	1
Data Pad	6
Data ECC	20
Data Total	42

Achieved Capacity =	828,323	Blocks
	424.10138	MBytes
	100.58	%
Excess Blocks =	4771	

Tinner	Zone	Rinner	Ntracks	Nsect	BPI	FCI	Rdata (Mbps)	FRcode (MHz)	Fmax (MHz)	Wndw/2 (nsec)	Num Blk	Eff (%)	Sct/Wdg whole
-13	4x Wdg	1.7987	3										
-1	16	1.7955	12	120	52,532	39,399	44.44	66.67	16.67	7.50			1
399	0	1.6901	400	141	65,296	48,972	52.00	78.00	19.50	6.41	56400	83.29	2
643	1	1.6258	244	138	66,357	49,767	50.83	76.25	19.06	6.56	33672	83.39	2
861	2	1.5683	218	135	67,250	50,437	49.70	74.55	18.64	6.71	29430	83.44	2
1007	3	1.5298	146	133	67,821	50,865	48.89	73.33	18.33	6.82	19418	83.57	2
1225	4	1.4724	218	129	68,637	51,478	47.62	71.43	17.86	7.00	28122	83.21	2
1530	5	1.3920	305	126	69,697	52,273	45.71	68.57	17.14	7.29	38430	84.67	2
1662	6	1.3572	132	121	70,130	52,597	44.85	67.27	16.82	7.43	15972	82.88	1
1832	7	1.3124	170	118	70,673	53,005	43.70	65.56	16.39	7.63	20060	82.94	1
2024	8	1.2618	192	114	71,235	53,427	42.35	63.53	15.88	7.87	21888	82.68	1
2233	9	1.2067	209	110	71,815	53,861	40.83	61.25	15.31	8.16	22990	82.75	1
2490	10	1.1389	257	105	72,463	54,347	38.89	58.33	14.58	8.57	26985	82.94	1
2735	11	1.0744	245	99	73,027	54,770	36.97	55.45	13.86	9.02	24255	82.26	1
2978	12	1.0103	243	94	73,519	55,139	35.00	52.50	13.13	9.52	22842	82.50	1
3211	13	0.9489	233	88	73,954	55,465	33.07	49.60	12.40	10.08	20504	81.75	1
3399	14	0.8994	188	84	74,253	55,689	31.47	47.20	11.80	10.59	15792	82.00	1
3652	15	0.8327	253	78	74,258	55,694	29.14	43.70	10.93	11.44	19228	80.13	1
Certified guard		0.8314	5										
Inner guard		0.8306	3										
4x Wdg		0.8298	3										

Product: Trail Blazer 840

Rev :3.0 9/29/94 P1 build

Req Cap	843.317	MBytes
Spare	1	per cyl
Surf	4	
Rod	1.7992	In
Rid	0.6310	In
Stroke	0.9682	In
Trk Den	3794	tpi
RPM	4499.64	rpm
Certified cyls	3672	
Data cyls	3653	
Servowritten cyls	3679	

ID as overhead

	Bytes	%
Speed Tol		0.30%
Wiggle	3	
ID Pre	9	
ID AM	1	
ID Data	6	
ID CRC	3	
ID Pad	6	
ID Gap	0	
ID Total	28	

Servo overhead

Srv Fq	40	MHz
Srv Clk	25	nSec
Srv N	464	Clocks
Nservos	63	samples
Wr-Wdg	1.5	uSec
Tservo	11.60	uSec
Tdata	199.42	uSec
Srv OH	5.48	%

AT CHS Set up

Logical Cylinders	1645
Logical Heads	16
Logical sectors	63
Logical Diag. Cyl.	2
Total sectors	1,660,176
Logical MegaBytes	850.010

Data overhead

Data Pre	15
Data AM	1
Data Pad	6
Data ECC	20
Data Total	42

Achieved Capacity = 1,660,299 Blocks
850.07309 MBytes
100.80 %
Excess Blocks = 13195

Tinner	Zone	Rinner	Ntracks	Nsect	BPI	FCI	Rdata (Mbps)	FRcode (MHz)	Fmax (MHz)	Wndw/2 (nsec)	Num Blk	Eff (%)	Sct/Wdg whole
-13	4x Wdg	1.7987	3										
-1	16	1.7955	12	120	52,532	39,399	44.44	66.67	16.67	7.50			1
399	0	1.6901	400	141	66,296	46,972	52.00	78.00	19.50	6.41	56400	83.29	2
643	1	1.6258	244	138	66,357	49,767	50.83	76.25	19.06	6.56	33672	83.39	2
861	2	1.5683	218	135	67,250	50,437	49.70	74.55	18.64	6.71	29430	83.44	2
1007	3	1.5296	146	133	67,821	50,865	48.89	73.33	18.33	6.82	19418	83.57	2
1225	4	1.4724	218	129	68,637	51,478	47.62	71.43	17.86	7.00	28122	83.21	2
1530	5	1.3920	305	126	69,697	52,273	45.71	68.57	17.14	7.29	38430	84.67	2
1662	6	1.3572	132	121	70,130	52,597	44.85	67.27	16.82	7.43	15972	82.88	1
1832	7	1.3124	170	118	70,673	53,005	43.70	65.56	16.39	7.63	20060	82.94	1
2024	8	1.2618	192	114	71,235	53,427	42.35	63.53	15.88	7.87	21888	82.68	1
2233	9	1.2067	209	110	71,815	53,861	40.83	61.25	15.31	8.16	22990	82.75	1
2490	10	1.1389	257	105	72,463	54,347	38.89	58.33	14.58	8.57	26985	82.94	1
2735	11	1.0744	245	99	73,027	54,770	36.97	55.45	13.86	9.02	24255	82.26	1
2978	12	1.0103	243	94	73,519	55,139	35.00	52.50	13.13	9.52	22842	82.50	1
3211	13	0.9489	233	88	73,954	55,465	33.07	49.60	12.40	10.08	20504	81.75	1
3399	14	0.8994	188	84	74,253	55,689	31.47	47.20	11.80	10.59	15792	82.00	1
3652	15	0.8327	253	76	74,258	55,694	29.14	43.70	10.93	11.44	19228	80.13	1
Certified guard		0.8314	5										
Inner guard		0.8306	3										
4x Wdg		0.8298	3										

Product: Trail Blazer 420

R/W CHANNEL SET UP

Setup Rev : 37 2/5/95 P2 build Write Current change

Format Rev :3.0 9/29/94 E3 build

				3036 Registers																		uP
				9	8	13	15	14	16	18	22	1	3	2	4	17	0	10	11	5	6	PWM
Zone	NCyl	Touter	Nsect	Syn-20*N/M		Data		Servo		Threshold		Precomp				HPF	VFC	Wndw Cntr		NCW	NDW	Iw
				N	M	Fc	Bst	Fc	Bst	Low	High	S	N	L	E	G/Bw		Step	Range	/Dsg	/LowZ	
16	12	3863	120	20	6	60	4	39	4	102	144	9	14	9	2	68	44	36	105	39	233	76
0	400	0	141	39	10	59	4	39	4	102	144	11	15	7	2	68	52	36	104	40	231	76
1	244	400	138	61	16	58	4	39	4	102	144	11	15	7	2	68	51	36	104	40	231	76
2	218	644	135	41	11	56	4	39	4	102	144	10	15	40	2	68	50	36	104	40	232	76
3	148	862	133	22	6	55	4	39	4	102	144	10	15	40	2	68	49	36	104	39	232	76
4	218	1008	129	25	7	54	4	39	4	102	144	9	15	41	2	68	48	36	104	39	233	76
5	305	1226	126	24	7	52	4	39	4	102	144	9	14	41	2	68	46	36	105	39	233	76
6	132	1531	121	37	11	51	4	39	4	102	144	8	14	42	2	68	45	36	105	38	234	76
7	170	1663	118	59	18	49	4	39	4	102	144	8	14	42	2	68	44	36	105	38	234	76
8	192	1833	114	54	17	48	4	39	4	102	144	7	14	43	2	68	42	36	106	38	235	76
9	209	2025	110	49	16	47	4	39	4	102	144	6	14	43	3	68	41	36	106	37	235	76
10	257	2234	105	35	12	45	5	39	4	102	144	6	13	44	3	68	39	36	107	37	236	76
11	245	2491	99	61	22	43	5	35	4	102	144	5	13	45	3	68	37	36	107	37	236	76
12	243	2736	94	21	8	41	5	31	4	102	144	5	13	46	3	68	35	36	108	36	237	76
13	233	2979	88	62	25	39	5	29	4	102	144	4	13	46	3	68	33	36	108	36	237	76
14	188	3212	84	59	25	37	5	27	4	102	144	3	13	47	3	68	31	36	109	35	238	76
15	253	3400	76	59	27	35	5	25	4	102	144	3	13	47	3	68	29	36	200	35	238	76

TailBrazer

Some Common Patterns in Hitachi RLL Code

00H	3T	BBH	2T
11H	6T	EEH	2T
22H	4T2T	00H	3T
33H	6T	AAH	3T
44H	6T	FFH	3T
55H	6T	70H OR 07H	4T
66H	2T4T	1CH OR C1H	4T
77H	2T4T	31 C5 14 53 4CH	5T
88H	4T2T	11H	6T
99H	2T4T	33H	6T
AAH	3T	44H	6T
BBH	2T	55H	6T
CCH	6T	CCH	6T
DDH	2T4T	66H	2T4T
EEH	2T	77H	2T4T
FFH	3T	99H	2T4T
70H OR 07H	4T	DDH	2T4T
1CH OR C1H	4T	22H	4T2T
31 C5 14 53 4CH	5T	88H	4T2T
2F BE F8 E2 8B	3T2T	2F BE F8 E2 8B	3T2T
55 13 D9 ACH	6T6T2T2T	2D 59H	2T6T
2D 59H	2T6T	93 AD 35 D9 5AH	2T2T6T
D5 92H	6T2T	AD 35 D9 5A 93H	2T6T2T
93 AD 35 D9 5AH	2T2T6T	D5 92H	6T2T
AD 35 D9 5A 93H	2T6T2T	55 13 D9 ACH	6T6T2T2T

TRAILBLAZER HEAD/MEDIA DESIGN SUMMARY

	ROAD RUNNER	TRAIL BLAZER
DRIVE DESIGN		
RPM	3600	4500
Channel	Peak Detection	Peak Detection
Areal Density (Mb/in2), Max (ID)	122	282
TPI	2670	3790
BPI, Max (ID)	45.7k	74.3k
FCI, Max (ID)	34.3k	55.7k
Data Rate (Mb/S), Max (OD)	29.7	52.0
HF Frequency (MHz), Max (OD)	10.5	19.5
HEAD DESIGN - SLIDER		
Head Type	Composite DMIG	Composite DMIG
Form Factor (Core/Slider)	70%	50%
Number of Turns	36 Monofilar	33 Monofilar
Inductance (uH)	≤ 2.5	≤ 1.5
Resistance (Ohm)	≤ 7.5	≤ 10.0
MIG Material	Fe-Al-Si (10-11 kG)	Fe-Ta-N (15-16 kG)
Track Width (um)	8.0 ± 0.8	5.5 ± 0.7
Gap Length (nm)	350 ± 50	250 ± 50
Air Bearing	Taper Flat	Offset Blend (TPC)
Flying Height (u")	3.4 ± 0.9	2.5 ± 0.75
Crown (nm)	37.5 ± 27.5	34.5 ± 16.5
HEAD DESIGN - SUSPENSION		
Suspension Type	HTI 870	HTI 850 LSF
Wire Tube OD (mm)	0.42 ± 0.02, Full Tube	0.30 Semi Tubeless
Z Height (mm)	0.860 ± 0.013	0.737
Gram Load (gram force)	7.0 ± 0.6	5.0 ± 0.5
DISK DESIGN		
Coercivity (Oe)	1450 ± 100	1800 ± 130
Remanence x Thickness (Gauss-um)	450 ± 30	290 ± 20
Glide Height (u")	≤ 2.0	≤ 1.5

Trailblazer™ Product Training

Mechanical/HDA

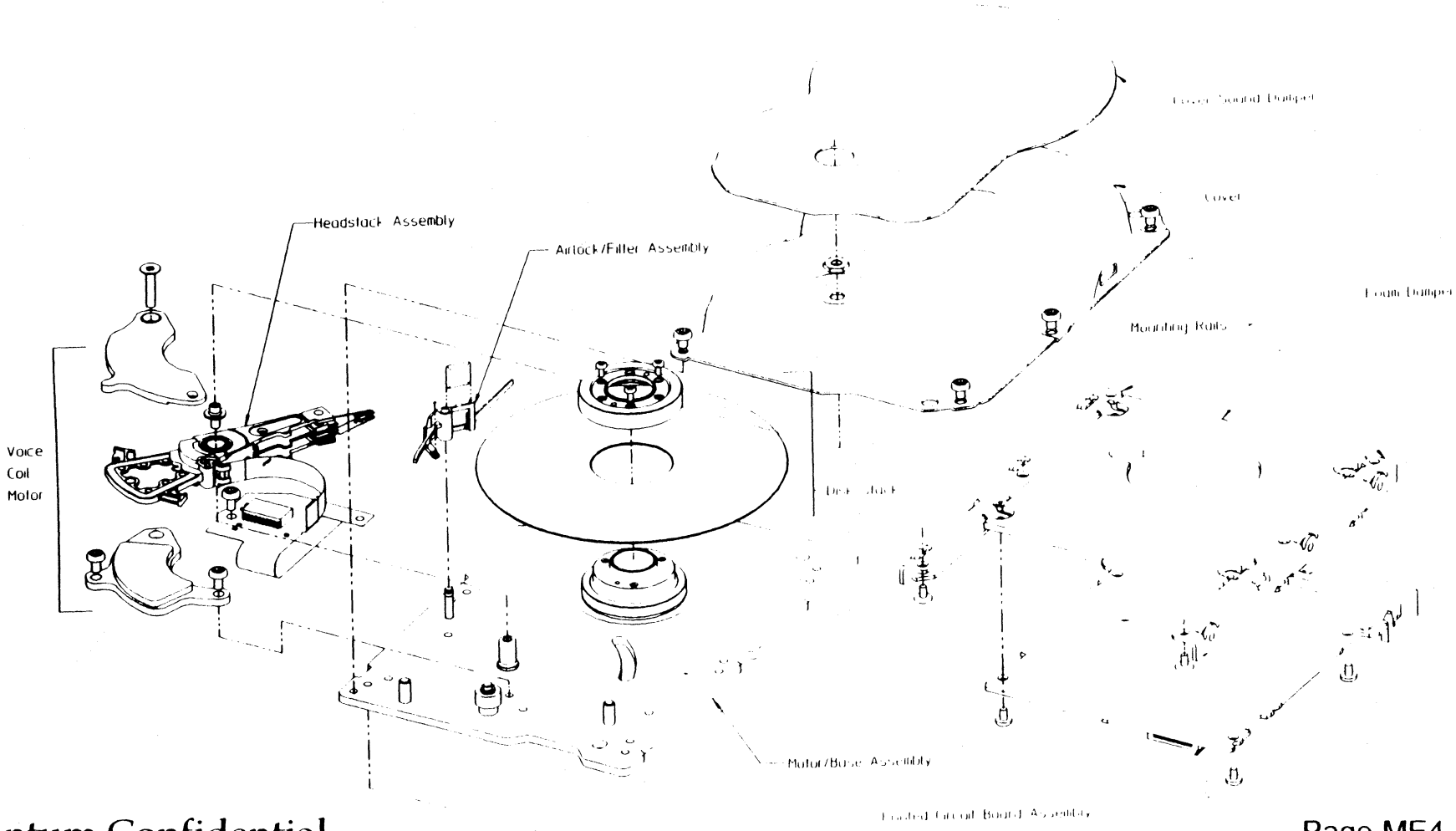
Product Specifications

	Trailblazer	Roadrunner
Capacity (MB)	420/630/840	210/420/+
Form Factor	1" high	1" high
Seek Time	14 ms	14 ms/12 ms
RPM	4500	3600
Ruggedness		
-Operational Shock (11 ms)	10 g	10 g
-Non-op shock (11 ms)	70 g	70 g
-Vibration (5-300 Hz, P-P)	2 g	2 g

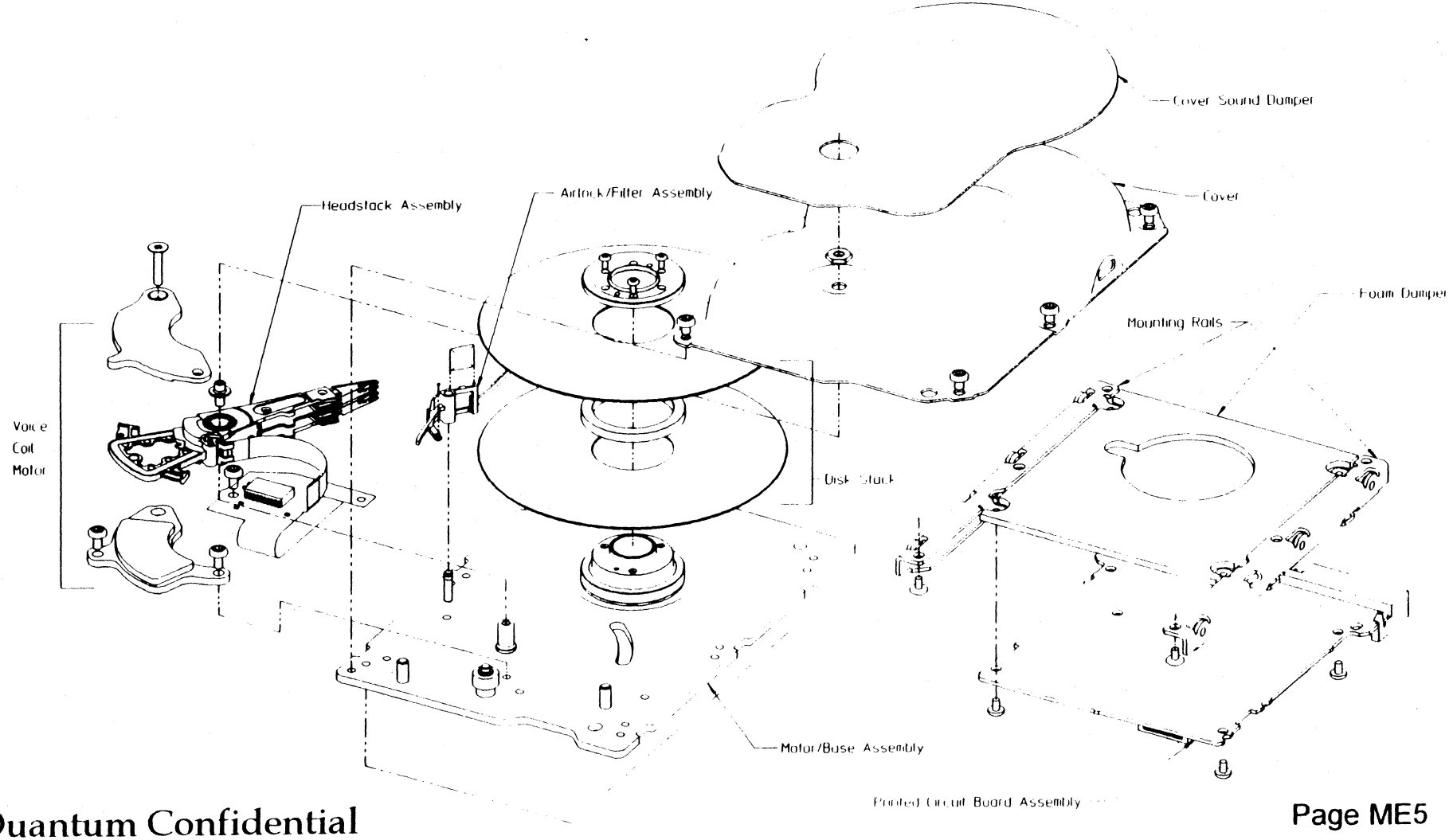
Product Specifications (cont.)

	Trailblazer	Roadrunner
Acoustics (Sound Pressure)		
-Idle	30 dBA	32 dBA
-Seeking	37 dBA	36 dBA
Acoustics (Sound Power)		
-Idle	3.5 bels	4.0 bels
-Seeking	4.2 bels	4.5 bels

1 Disk Exploded Assembly

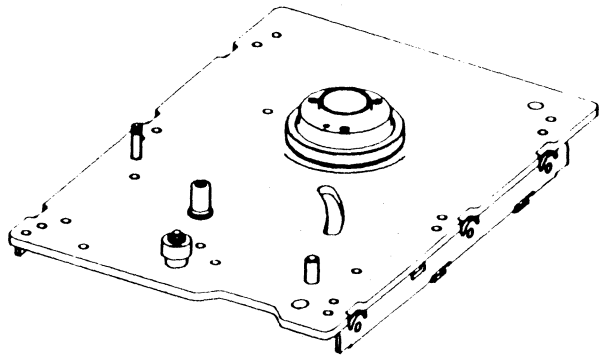


2 Disk Exploded Assembly



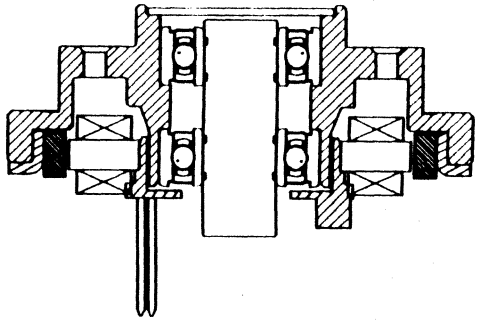
Base Assembly

- Stamped Aluminum plate
- Integral spindle motor
- Pressed in actuator and airlock shafts
- Steel stamped side rails
- Drive mounting
  - More critical because of base flexibility



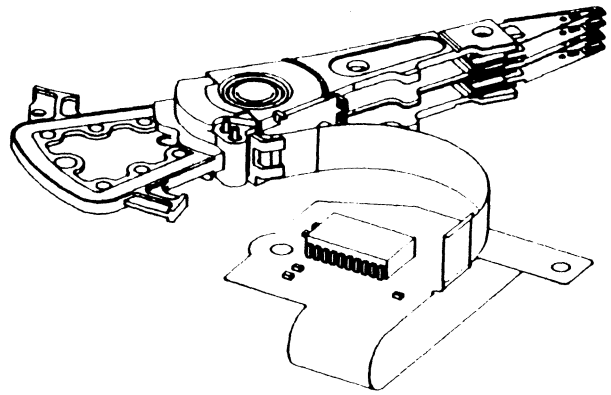
Spindle Motor Assembly

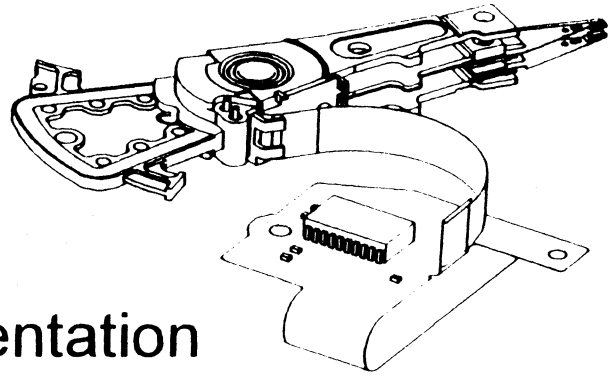
- Brushless DC type
- Hall-less driver
- 3-phase, 8-pole design
- Fixed shaft
- Counterclockwise rotation
- 4500 RPM
- Spin up time less than 5 seconds
- 4 pin motor connector



Headstack Assembly

- Capacities
  - 2 head/1 disk = 420 MB
  - 3 head/2 disk = 630 MB
  - 4 head/2 disk = 840 MB
- Actuator
  - Rotary positioner
  - Single phase coil
  - Voice coil motor
  - Balanced to operate in any orientation



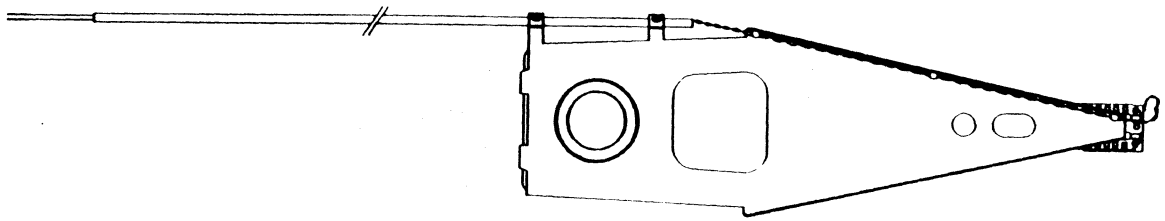


Headstack Assembly (cont.)

- Voice coil motor
  - Single lower magnet
  - Upper fluxplate
- E-Block
  - Die cast aluminum
  - Encapsulated coil
  - Discrete bearing arrangement

Headstack Assembly (cont.)

- Plastic flex-circuit guide
- Heads
  - 50% slider, 5.5 micron track width
  - Composite MIG core
  - Type 8 suspension
  - 1.75 µinch minimum flying height
  - Shorter wire capture

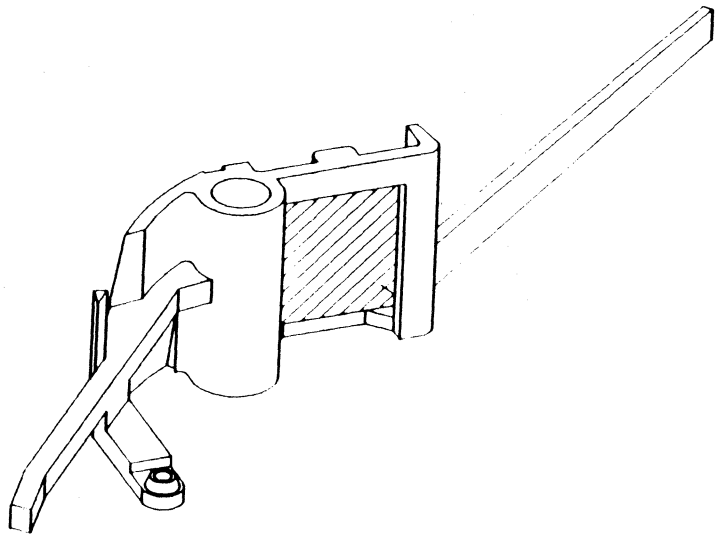


Disk Stack Assembly

- Thin film media
- 1.50 µinch glide height
- 1-disk version
  - Disk clamp
  - 3 screws
- 2-disk version
  - 'Flat' clamp design
  - Spacer
  - 3 screws

Airlock Assembly

- Magnetic return uses stray flux from the VCM magnet
- Integral recirculating filter
- Balanced to operate in any orientation



Cover Assembly

- Sealing gasket
- Drawn aluminum sheet cover
- Additional sound dampening cover