GENERAL PURPOSE MEMORY MODULE
GPM AND GPM - Sol

ASSEMBLY AND TEST INSTRUCTIONS

Processor Technology

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GENERAL PURPOSE MEMORY MODULE
GPM and GPM-Sol

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PROCESSOR TECHNOLOGY CORPORATION

GPM Contents

SECTION 1

INTRODUCTION AND GENERAL INFORMATION

GPM (General Purpose Memory) and GPM-Sol MODULES

1.1 INTRODUCTION

This manual provides all information necessary to assemble, test, and use the General Purpose Memory (GPM) Module. Before starting to assemble the kit, scan the entire manual, and be sure that you have all the parts and components in Table 2-1, GPM Parts List, page 2-2. All instructions are presented in the order in which you must assemble the module.

1.2 GENERAL INFORMATION

1.2.1 Description

The GPM is an S-100 bus compatible memory module available in kit or assembled form for use in 8080-based computers including the Processor Technology Sol, and models by several other manufacturers. It has a capacity of 10,240 8-bit bytes of read-only-memory (ROM) for storing programs as "firmware", and 1024 bytes of read-write-memory (RAM) which is normally used as a "scratch-pad" memory. The user can store any frequently-used programs on the GPM, or use the module to house a companion product, the ALS-8 program development system, a resident monitor-assembler system, available in ROM. GPM may be adapted for use with several types of ROMs and PROMs including types 9216B, 8316E, 34000P, and 2708. A switch-selectable automatic start-up mode is included, so that the system is "up" and ready to accept commands as soon as power is applied. All signal lines are fully buffered.

The GPM memory is available separately or as a component module in a system of five modules; "Subsystem B", by Processor Technology. Subsystem B includes CUTS, VDM-1, 3P+S, and a choice of RAM memory boards, as well as the GPM. CUTS provides cassette tape mass storage interface; VDM-1 provides a powerful video display interface; 3P+S provides parallel and serial data channels for keyboard, TTY, paper tape reader or other peripherals; the RAM memory provides working systems storage area. GPM fits into this system by providing the CUTER monitor program, and space for the ALS-8 program development system or other "firmware". Overall, Subsystem B turns the mainframe computer offered by many manufacturers into a powerful integrated computer system.

1.2.2 GPM and GPM-Sol Versions

Two versions of the product are available; GPM-Sol, for use in the Sol Terminal Computer by Processor Technology, and GPM, for use in other S-100 computers. The main differences between these two versions is illustrated in Figure 1-1, GPM and GPM-Sol Memory Map, page 1-3. This figure shows the full addressing capability, ØØØØ to FFFF (hex.), of the 8080 Central Processing Unit used in S-100 computers and how the subsections of the GPM and the GPM-Sol may be addressed within this range. The right-hand

figure shows the GPM-Sol sections mapped within the Sol addressing structure, and left-hand figure shows GPM mapped within other manufacturer's addressing structures. The main differences between the two maps are:

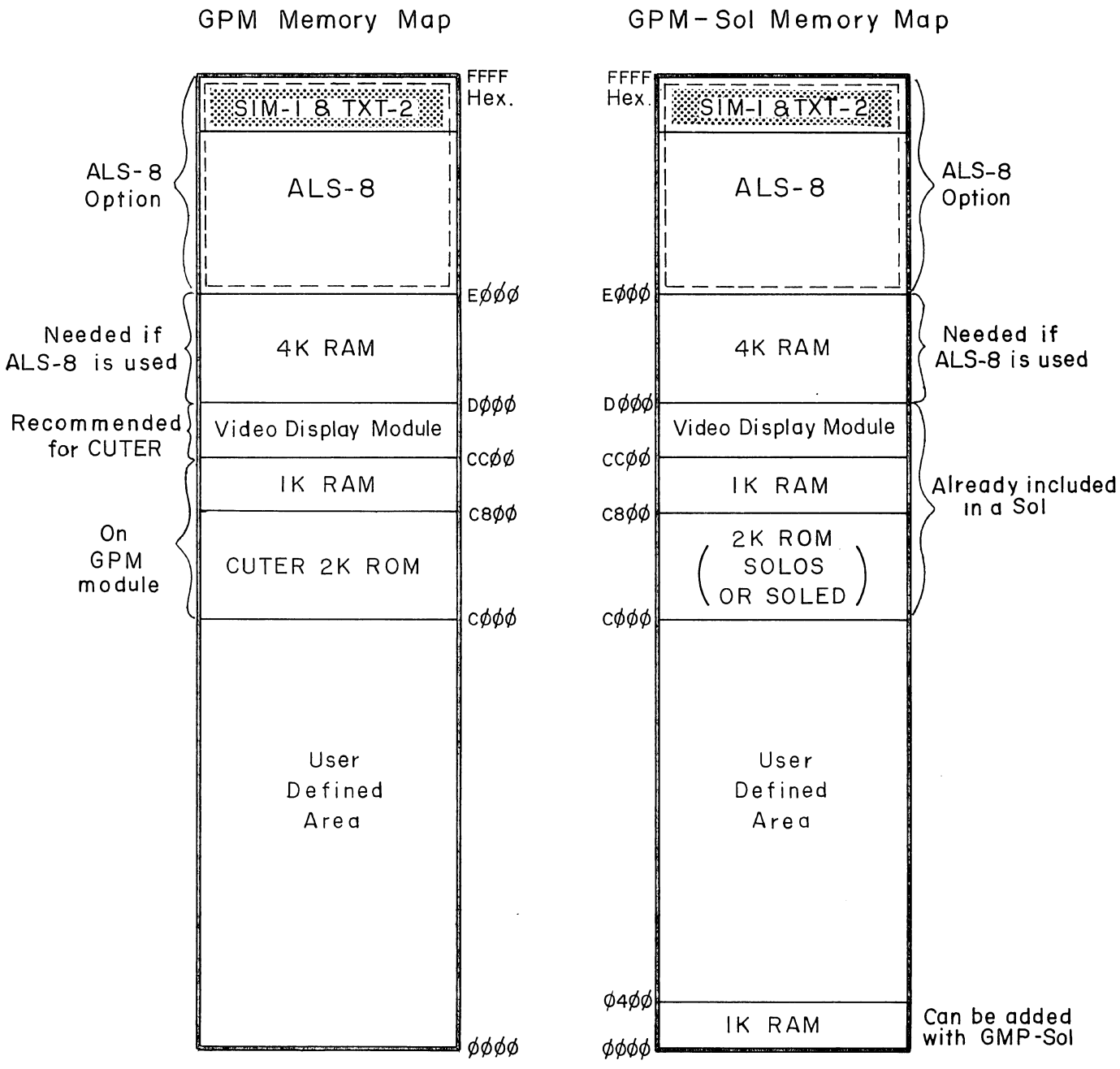
1. The GPM version contains 2K of ROM normally addressed at locations CØØØ to C8ØØ (hexadecimal) contain CUTER (Computer User's Tape Entry and Retrieval monitor program), a version of the SOLOS monitor program used in the Processor Technology Sol. The use of this program is covered in the SOLOS/CUTER User's Manual. Since the Sol already contains the SOLOS program, it is not included in the GPM-Sol version.

2. The GPM version includes 1K of RAM addressed C8ØØ to CBFF which is used by CUTER as systems memory area. The GPM-Sol version does not include the RAM, since this too is included in the Sol. However, 1K of RAM may be added to the GPM-Sol, and addressed ØØØØ to Ø3FF (hex).

3. The Sol includes a video display circuit addressed CCØØ to DØØØ. To ensure compatibility, it is recommended that the GPM version be used in conjunction with the VDM-1 Video Display Module, which is similar to the video section of the Sol, and is also addressed CCØØ to DØØØ.

4. Both the GPM and GPM-Sol versions contain space for 8K of ROM addressed at EØØØ to FFFF (hex). This area may be used to store programs as "firmware" in ROM or PROM. A companion product, the ALS-8 program development system is available in three or four ROMs which plug into the GPM or GPM-Sol board, and are addressed at these locations. This is shown on Figure 1-1 as the ALS-8 area within the dotted lines. An option is available with ALS-8: SIM-1, an 8080 simulator program, and TXT-2, a text editor program. The ALS-8 kit contains three ROMs with the ALS-8 program, an optional fourth ROM with SIM-1 and TXT-2, a software manual, and assembly instructions. A system which includes all three programs is a powerful program development system including an assembler,

Figure 1-1. GPM and GPM-Sol Memory Maps



an 8080 simulator, a text editor, and support routines for file-handling, program execution, and debugging. When ALS-8 is used on either GPM or GPM-Sol, 4K of RAM must be added at locations DØØØ to EØØØ.

1.2.3 GPM Voltage Requirements, Typical

The basic GPM board requires:	+7.5 to +10 V dc at	750 ma.,	
	+15 to +18 V dc at	50 ma.,	and
	-15 to -18 V dc at	50 ma.	
Each additional 2708 draws:	+7.5 to +10 V dc,	6 ma.,	
	+15 to +18 V dc,	50 ma.,	and
	-15 to -18 V dc,	30 ma.	
Each additional 9216 draws:	+7.5 to +10 V dc,	15 ma.,	and
	+15 to +18 V dc,	50 ma.	

1.3 WARRANTY AND REPLACEMENT INFORMATION

1.3.1 Receiving Inspection

When your kit arrives, examine the shipping container, noting any conditions that might indicate damage to the contents during transit. Then inspect the contents. (We suggest you save the shipping materials for use in returning the Kit to Processor Technology if it is necessary. If your GPM is damaged, please write us at once describing the condition of both the shipping container and the contents, so that we can take appropriate action.

1.3.2 Warranty Information

In brief, parts that fail because of defects in materials or workmanship are replaced at no charge for 3 months for kits, and one year for assembled products, following the date of purchase. Also, products assembled by the buyer are warranted for a period of 3 months after the date of purchase; factory assembled units are warranted for one year after the date of purchase. Refer to Appendix I for the complete "Statement of Warranty".

1.3.3 Replacement Parts

Order replacement parts by component nomenclature (DM8131 IC or 1N2222 diode, for example) and/or a complete description (680 ohm, 1/4 watt, 5% carbon resistor, for example).

1.3.4 Factory Service

In addition to in-warranty service, Processor Technology also provides factory repair service on out-of warranty products. Before returning the unit to Processor Technology, obtain authorization to do so by writing us a letter describing the problem. After you receive our authorization to return the unit, proceed as follows:

1. Write a description of the problem.

2. Securely pack the unit and the description in a shipping container.

3. Ship prepaid to Processor Technology Corporation, 6200 Hollis Street, Emeryville, CA. 94608

Your unit will be repaired as soon as possible after receipt and returned to you prepaid. (Factory service charges will not exceed $20.00 without prior notification and your approval).

SECTION 2

ASSEMBLY

GPM (General Purpose Memory) and GPM-Sol Modules

2.1 PARTS AND COMPONENTS

Check all parts and components against the "Parts List" (Table 2-1 on Page 2-2). If you have difficulty in identifying any parts by sight, refer to the Component Identification Illustrations, following page 2-2.

2.2 ASSEMBLY TIPS

1. Read Sections 2 and 3 before you start to assemble your GPM.

2. Assembly steps and component installations are preceded by a set of parentheses. Check off each installation and step as you complete them. This will minimize the chances of omitting a step or component.

3. When installing components, make use of the assembly aids that are incorporated on the GPM PC board and the assembly drawing. (These aids are designed to assist you in correctly installing the components.)

4. In assembling your GPM, follow the step-by-step integrated assembly-test procedure. FOLLOW THE INSTRUCTIONS IN THE ORDER GIVEN. The circuit reference (R3, C10, and U7, for example) for each component is silk screened on the PC board near the location of its installation. Both the circuit reference and value or nomenclature (1.5k and 74LS08, for example) for each component are included on the assembly drawing near the location of its installation.

5. To simplify reading resistor values after installation, install resistors so that their color codes read from left-to-right and top-to-bottom as appropriate (board oriented as defined in Paragraph 2.5 on Page 2-6).

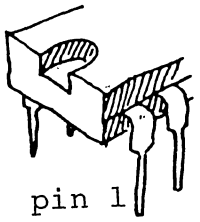
6. Unless specified otherwise in the instructions, install all components, especially disc capacitors, as close to the board as possible.

7. If you encounter any problem during the assembly, feel free to call on us for help.

Table 2-1. GPM Parts List

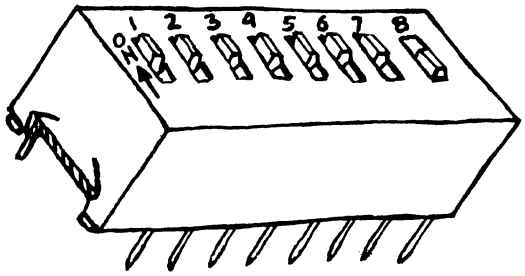
Quantity GPM	Quantity GPM-Sol	Part#	Designation(s)	Function	Acceptable Substitute
Integrated Circuits					
1	0	9216B (AMD)	U9	2Kx8 ROM	
8	0	91L02A (AMD)		1Kx1 RAM	2102L1PC or 21L02B
1	1	74LS04	U23	HEX INVERTER	
2	2	74LS74	U20-U21	DUAL FLIP-FLOP	7474
2	2	74LS132	U19-U22	QUAD NAND SCHMITT	
1	1	74LS138	U31	DECODER	
4	4	74367	U18,U28,U29, U32	HEX BUFFERS	8097 or 8T97
4	4	74LS367	U24-U27	HEX BUFFERS	8T97
1	1	82S129B(SIGNETICS) (Specially programmed)	U30	256X4 PROM	3601 (INTEL)
1	1	7812		+12V REG	
1	1	7805		+5V REG	
Resistors					
		(BOURNS)			
2	2	4308R-101-222	R1,R2	8 PIN 2.2K ARRAY	
6	6	1.5KΩ,1/4 WATT	R3-R8		
2	2	470Ω, 1/4 WATT	R10,R11		
1	1	10KΩ, 1/4 WATT	R9		
Capacitors					
23	23	.047μF DISC	C1-C12,C15, C16,C20-C28		
2	2	1μF TANT	C13,C29		
3	2	15μF TANT	C17,C19,(C30)		
DIP Sockets					
5	5	14 PIN			
18	18	16 PIN			
9	9	24 PIN			
DIP Switch					
1	1	206-8 (CTS)	SW1	8 POS DIP	
Transistors					
1	1	2N2907	Q1	PNP TRANSISTOR	
Miscellaneous					
1	1	210-001		P. C. BOARD	
1	1	680-5220		HEAT SINK	
1	1			HEAT SINK COMPOUND	
4	4	6-32x½ SCREW			
4	4	#6 LOCKWASHER			
4	4	6-32 NUT			

COMPONENT IDENTIFICATION ILLUSTRATIONS

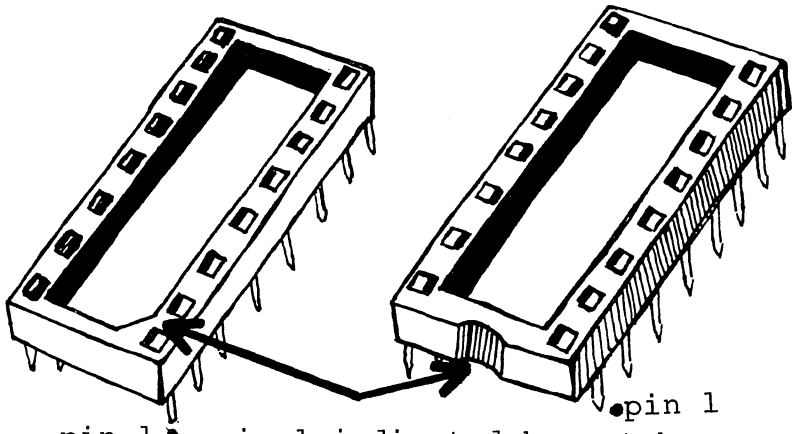


NOTE: Pin 1 may be indicated by corner dot or cut-out

Dual Inline Package (DIP) IC
(8,14,16,24 or 40 pins)



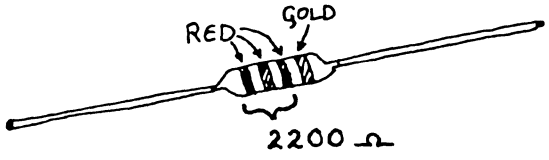
DIP Switch



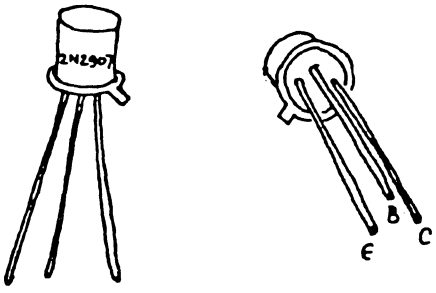
pin 1 indicated by notch
DIP Socket

positive (+) lead

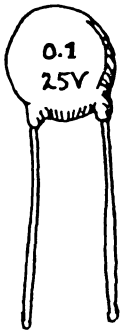
Dipped Tantalum
Electrolytic Capacitor



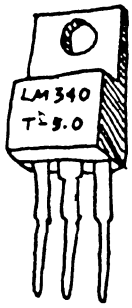
Carbon Film Resistor
5% (gold), 10% (silver)



Transistor
TO-18 Package (Metal Can)

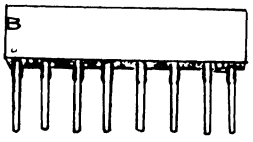


Disc Ceramic
Capacitor



TO-220 Regulator IC
or Power Transistor

Star Lockwasher



Resistor Network

2.3 ASSEMBLY PRECAUTIONS

2.3.1 Handling MOS Integrated Circuits

Many of the ICs used in the GPM are MOS devices. They can be damaged by static electricity discharge. Always handle MOS ICs so that no discharge will flow through the IC. Also, avoid unnecessary handling, and wear cotton--NOT synthetic--clothing when handling these ICs.

2.3.2 Soldering **IMPORTANT**

1. Use a fine tip, low-wattage iron, 25 watts maximum.

2. DO NOT use excessive amounts of solder. DO solder as neatly and as quickly as possible.

3. Use only 60-40 rosin-core solder. NEVER use acid-core solder or externally applied fluxes.

4. To prevent solder bridges, position iron tip so that it does not touch adjacent pins and/or traces simultaneously.

5. DO NOT rest tip of iron on pad or trace. To do so can cause the pad or trace to "lift" off the board and permanently damage it.

6. The GPM circuit board has plated-through holes. Solder flow through the component (front) side of the board can produce solder bridges. Check for such bridges after you install each component.

7. The GPM circuit board has an integral solder mask (a lacquer coating) that shields selected areas on the board. This mask minimizes the chances of creating solder bridges during the assembly. DO, however, check all solder joints for possible bridges.

8. Additional pointers on soldering are provided in Appendix 3 of this manual.

2.3.3 Installing and removing GPM Module.

NEVER install the GPM in, or remove it from the computer, with the power on. To do so can damage the module.

2.3.4 Installing and Removing Integrated Circuits.

NEVER install or remove integrated circuits while power is applied to the GPM. To do so can damage the IC.

2.3.5 Use of Clip Leads

NEVER attach clip leads to the top edge of the GPM circuit board. Clip leads so attached are apt to short the +8, +16, -16 V dc, and ground buses.

2.4 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment, and materials are recommended for assembling and testing the GPM Module:

1. Needle nose pliers
2. Diagonal cutters
3. Screwdriver
4. Sharp knife
5. Controlled heat fine tip soldering iron, 25 watts
6. 60-40 rosin-core solder (supplied)
7. Volt-ohm meter

2.5 ORIENTATION

The heat sink area (large foil area) will be located in the upper right hand corner of the board when the 100-pin edge connector is at the bottom. In this position the component (front) side of the board is facing up and the solder (back) side is facing down. Also, the IC legends (U1 through U9, U10 through U18, etc.) will read from left to right. The assembly drawing in Section 5 reflects this position. Subsequent position references in the instructions assume this orientation.

2.6 ASSEMBLY-TEST

Refer to the GPM assembly drawing, Figure 5-1, in Section 5. Note that the assembly drawing shows values, e.g. 1.5K, as well as circuit references, e.g. R3.

NOTE

Instructions preceded with an asterisk (*) do not apply to the GPM-Sol.

CAUTION

THIS DEVICE USES MOS MEMORY INTEGRATED CIRCUITS WHICH CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGES. HANDLE THESE ICs SO THAT NO DISCHARGE FLOWS THROUGH THE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON RATHER THAN SYNTHETIC CLOTHING WHEN HANDLING THESE ICs. (STATIC DISCHARGE PROBLEMS ARE MUCH WORSE IN LOW HUMIDITY ENVIRONMENTS.)

2.6.1 Circuit Board Check

( ) Visually check GPM circuit board for solder bridges (shorts) between traces, broken traces, and similar defects.

( ) Check board to ensure that the +8, +16, -16, +12, +5, -5 volt buses are not shorted to one another or to ground. Using an ohmmeter, make the following measurements (refer to GPM assembly drawing in Section 5). You should measure no continuity in any of these measurements.

( ) +8-volt Bus Test. Measure between edge connector pin 1 or 51 (left end of connector) and pin 50 or 100 (right end of connector).

( ) +16-volt Bus Test. Measure between edge connector pin 2 (second top, or front, pin from left end of connector) and pin 50 or 100.

( ) -16-volt Bus Test. Measure between edge connector pin 52 (second bottom, or back, pin from left end of connector) and pin 50 or 100.

( ) +5-volt Bus Test. Measure between positive (+) mounting pad for C13 and edge connector pin 50 or 100.

( ) +12-volt Bus Test. Measure between positive (+) mounting pad for C29 and edge connector pin 50 or 100.

( ) -5-volt Bus Test. Measure between negative (-) mounting pad for C14 and edge connector pin 50 or 100.

( ) 8/16/(-16)/5/(-5)/12 Volt Bus Test. Measure between:

A. Edge Connector pins 1 or 51 and--

( ) Edge connector pin 2

( ) Edge connector pin 52

( ) Positive (+) pad for C13

( ) Negative (-) pad for C14

( ) Positive (+) pad for C29

B. Edge Connector pin 2 and--

( ) Edge Connector pin 52

( ) Positive (+) pad for C13

( ) Negative (-) pad for C14

( ) Positive (+) pad for C29

C. Edge connector pin 52 and--

( ) Positive (+) pad for C13

( ) Negative (-) pad for C14

( ) Positive (+) pad for C29

D. Positive (+) pad for C13 and--

( ) Negative (-) pad for C14

( ) Positive (+) pad for C29

E. Negative (-) pad for C14 and--

( ) Positive (+) pad for C29

If you measure continuity in any of the preceding tests, recheck the measurement(s). If you still measure continuity, the board is defective. Return it to Processor Technology for replacement. If none of the measurements show continuity, go on to the next paragraph.

2.6.2 Assembly-Test Procedure

( ) Step 1. Install heat sink. Position the large, black heat sink (flat side to board) over the square foil area in the upper right corner. Orient the sink so that the two triangles of mounting holes in the board are under the two triangular cutouts in the sink. Using two 6-32 screws, lockwashers and nuts, attach heat sink to board. Insert the screws from back (solder) side of board.

( ) Step 2. Install U34 (7805). Position U34 over left hand cutout in heat sink and observe how the leads must be bent to fit the mounting pads. Note that the center lead (3) must be bent down at a point approximately 0.2 inches further from the body than the other two leads. Bend leads so that no contact is made with the heat sink when U34 is flat against the sink and its mounting hole is aligned with the hole in the sink. Coat both the bottom surface of U34 and the heat sink area to which U34 mates with a thin film of heat sink compound. Insert leads and fasten U34 to sink with a 6-32 screw, #6 lockwasher and nut. Insert screw from solder (back) side of board, place washer on screw and drive nut. Solder and trim leads.

NOTE

U35, the negative supply regulator, is not supplied with standard GPM modules. It is needed only when 2708 ROMs are used. (Refer to Section 3).

( ) Step 3. Install U33 (7812). Position U33 in the upper right hand corner of the board with the leads facing left. Observe how the leads must be bent down to fit the mounting pads and bend accordingly. U33 should lie flat against the board with its mounting hole aligned with the hole in the circuit board. Insert leads and fasten U33 to board with a 6-32 screw, #6 lockwasher and nut. Insert screw from solder (back) of board, place washer on screw and drive nut. Solder and trim leads.

( ) Step 4. Install DIP switch in location SW1. Position switch so Switch No. 1 (SW1-1) is at the left. (Refer to "Loading DIP Devices" in Appendix 4.)

( ) Step 5. Install all resistors in numerical order in the following locations. Bend leads down to fit distance between mounting holes, insert leads, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

	LOCATION	VALUE (ohms)	COLOR CODE
( )	R3	1.5k	brown-green-red
( )	R4	1.5k	brown-green-red
( )	R5	1.5k	brown-green-red
( )	R6	1.5k	brown-green-red
( )	R7	1.5k	brown-green-red
( )	R8	1.5k	brown-green-red
( )	R9	10K	brown-black-orange
( )	R10	470	yellow-violet-brown
( )	R11	470	yellow-violet-brown

( ) Step 6. Install resistor networks R1 and R2 (2.2k ohms) in their respective locations. Position R1 and R2 so that the dot on their packages is at the bottom right. Insert leads, solder and trim.

CAUTION

RESISTOR NETWORKS ARE DELICATE. HANDLE WITH CARE.

( ) Step 7. Install the five tantalum capacitors in the following locations. Take care to observe the proper value and orientation for each installation.

	LOCATION	VALUE (ufd)	ORIENTATION
( )	C13	1	"+" lead right
	C14 (not used)		
( )	C17	15	"+" lead bottom right
	C18 (not used)		
( )	C19	15	"+" lead right
( )	C29	1	"+" lead right
*( )	C30	15	"+" lead down

* C30 is not marked on the board. It is the unmarked capacitor to the right of IC socket U20.

NOTE

C14 and C18 are not supplied with standard GPM modules. They are needed only when ROMs that require -5 V dc are used. (Refer to Section 3.3.2, steps 2 and 3.)

( ) Step 8. Install all disc capacitors in numerical order in the following locations. Insert leads, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

NOTE

Disc capacitor leads are usually coated with wax during the manufacturing process. After inserting leads through mounting holes, remove capacitor and clear the holes of any wax. Re-insert and install.

	LOCATION	VALUE (ufd)	TYPE
( )	C1	.047	Disc Ceramic
( )	C2	.047	Disc Ceramic
( )	C3	.047	Disc Ceramic
( )	C4	.047	Disc Ceramic
( )	C5	.047	Disc Ceramic
( )	C6	.047	Disc Ceramic
( )	C7	.047	Disc Ceramic
( )	C8	.047	Disc Ceramic
( )	C9	.047	Disc Ceramic
( )	C10	.047	Disc Ceramic
( )	C11	.047	Disc Ceramic
( )	C12	.047	Disc Ceramic
( )	C15	.047	Disc Ceramic
( )	C16	.047	Disc Ceramic
( )	C20	.047	Disc Ceramic
( )	C21	.047	Disc Ceramic
( )	C22	.047	Disc Ceramic
( )	C23	.047	Disc Ceramic
( )	C24	.047	Disc Ceramic
( )	C25	.047	Disc Ceramic
( )	C26	.047	Disc Ceramic
( )	C27	.047	Disc Ceramic
( )	C28	.047	Disc Ceramic

( ) Step 9. Install DIP sockets. Install each socket in the indicated location with its end notch at the bottom. (Note that pin 1 is in the lower right corner of each location.) Take care not to create solder bridges between the pins and/or traces.

INSTALLATION TIP

Insert socket pins into mounting pads of appropriate location. On back (solder) side of board, bend pins at opposite corners of socket (e.g. pins 1 and 9 on a 16-pin socket) outward until they are at a 45° angle to the board surface. This secures the socket until it is soldered. Repeat this procedure with each socket until all are secured to the board. Solder the unbent pins on all sockets. Then straighten the bent pins to their original position and solder.

NOTE

If you intend to use eight 1K ROMs instead of four 2K ROMs, 24-pin sockets should be installed in these four locations.

LOCATION	SOCKET TYPE
( ) U1 through U9	24 pin
( ) U10 through U18	16 pin
( ) U19 through U23	14 pin
( ) U24 through U32	16 pin

( ) Step 10. Check regulator operation. This check is made to prevent potential damage to the ICs from incorrect voltages.

( ) Using an ohmmeter, make the following measurements:

SUPPLY	MEASUREMENT POINTS
+5 V dc	Positive (+) and negative (-) leads of C13
+12 V dc	Positive (+) and negative (-) leads of C29

You should measure some resistance in both measurements. Zero resistance indicates a short. If required, find and correct the problem before proceeding. Especially check for solder bridges.

( ) Install GPM in computer. (The use of a Processor Technology EXB Extender Board is recommended.)

CAUTION

NEVER INSTALL OR REMOVE GPM WITH POWER ON.

( ) Turn power on and make the following voltage measurements:

MEASUREMENT POINTS	VOLTAGE (±5%)
Across C13	+5 V dc
Across C29	+12 V dc

If either voltage is incorrect, determine and correct the cause before proceeding. If voltages are correct, turn power off, remove GPM from computer and go on to step 11.

( ) Step 11. Install the following ICs in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Pin 1 is positioned in the lower right corner of each IC location, and is indicated by a dot on the assembly drawing.

	IC NO.	TYPE
*( )	U9#	9216# (CUTER ROM)
*( )	U10 through 17#	91L02A, 2102L1PC or 21L02B#
( )	U18	74367, 8097 or 8T97
( )	U19	74LS132 or 74132
( )	U20 & 21	74LS74 or 7474
( )	U22	74LS132 or 74132
( )	U23	74LS04 or 7404
( )	U24 through 27	74LS367 or 8T97
( )	U28 & 29	74367, 8097, or 8T97
( )	U30	82S129 or 3601
( )	U31	74LS138 or 74158
( )	U32	74367, 8097, or 8T97

* #MOS devices. Refer to CAUTION on Page 2-8.

Assembly and test of the GPM General Purpose Memory or GPM-Sol is now complete and ready for use with appropriately programmed ROMs.

As presently assembled, the GPM is configured to operate with 9216B ROMs in locations U2, U4, U6, U8, and U9. Other 2K ROMs (34000 and 8316E) can also be used in these locations by reconfiguring the board via trace cutting and jumper options. In a similar manner the GPM can be reconfigured to use 1K ROMs (e.g. 2708) in locations U1 through U8. Instructions for making the required changes are given in Section 3.

( ) Step 12. Install transistor 2N2907 according to the following instructions. Place the middle lead of the transistor in the hole labeled B (right below and to the left of R4 on the component side). The small metal tab should point to the left; then the other two leads will fit into the appropriate holes. Install the transistor as close to the board as possible. Turn the board over, solder the leads and trim.

2.6.3 ALS-8, and ALS-8 with SIM-1 and TXT-2 Options

If you have purchased either the ALS-8 option alone, or the ALS-8 plus SIM-1 and TXT-2 option, and your GPM or GPM-Sol board is functioning correctly, you may proceed to install these ROMs according to the instructions enclosed with them.

2.6.4 Operation in Computers without Sense Switches

At start-up, after examining location CØØØ, the CUTER program inputs the sense switch data from port FF (hexadecimal) to determine the input and output pseudoports to be used during command mode. If the system has no sense switches, data from port FF will be input as FF which indicates that at locations C8ØØ and C8Ø2 the program will find the addresses of user-defined input and output routines. By putting the addresses of pre-written CUTER routines in these two locations, the desired command mode input and output routines are selected without sense switches. By entering the data in the table below before examining CØØØ and running, the desired input and output routines may be chosen. Entering these addresses is known as patching.

1. INPUT PATCH:

   at C8ØØ patch in: 35CØ for keyboard input
   3ECØ for serial input
   5ØCØ for parallel input

2. OUTPUT PATCH:

   at C8Ø2 patch in 77CØ for video display output
   46CØ for serial output
   59CØ for parallel output

SECTION 3

GPM OPTIONS

GPM (General Purpose Memory) and GPM-Sol MODULES

3.1 GPM OPTIONS

The eight-position DIP switch (SW1) located in the upper right corner of the PC board is used to configure the GPM for the various operating options. These include: the automatic start-up option; wait-state generation; and the ability to place portions of memory at different addresses.

Jumper arrangements are provided to permit accomodation of various types of ROM chips.

TABLE 3-1. SWITCH SETTINGS NECESSARY TO OPERATE THE GPM MODULE

SWITCH	DESCRIPTION ON	OFF	Sol	ALTAIR	IMSAI
S1-1	Disables EØØØ-FFFF during phantom start-up	EØØØ-FFFF is enabled during auto start	ON	ON if used with auto start at CØØØ OFF if used with auto start at EØØØ	ON if used with auto start at CØØØ OFF if used with auto start at EØØØ
S1-2	Imposes 1 wait state	No wait state imposed	OFF (normal operation) ON if slow PROMs are used	OFF (normal operation) ON if slow PROMs are used	OFF (normal operation) ON if slow PROMs are used.
S1-3	Disables CØØØ-C7FF during phantom start-up	CØØØ-C7FF is enabled during auto start	Not used	OFF for auto start to CØØØ (normal operation) ON for no auto start or auto start to EØØØ	OFF for auto start to CØØØ (normal operation) ON for no auto start or auto start to EØØØ
S1-4	Disables RAM at ØØØØ-Ø3FF when used in a Sol (i.e. if S1-7 is closed)	RAM is enabled @ ØØØØ-Ø3FF (provided S1-7 is closed)	ON if Sol already has memory @ ØØØØ-Ø3FF OFF if Sol does not already have memory @ ØØØØ-Ø3FF	OFF (1K RAM will appear at C8ØØ)	OFF (1K RAM will appear @ C8ØØ)
S1-5	Permits auto start in ALTAIRs only	Disconnects GPM from PRESET, Bus Pin 75	OFF	ON (for auto start) OFF (for non-auto start)	OFF
S1-6	Enables on-card phantom	Disables on-card phantom	OFF	ON for auto start with GPM OFF for non-auto start	ON for auto start with GPM OFF for non-auto start
S1-7	For Sol (disables PROM 9 & puts 1K RAM at ØØØØ	For ALTAIR, IMSAI (puts PROM 9 at CØØØ-C7FF & 1K RAM at C8ØØ-CBFF)	ON	OFF	OFF
S1-8	Allows control from external phantom	Disconnects GPM from pin 67 on bus	OFF	OFF	OFF

3.2 SWITCH OPTIONS

Table 3-1 "Switch Settings Necessary to Operate the GPM Module" summarizes the function of the different switchs in each of the three main types of computers: the Sol, the ALTAIR 8800, and the IMSAI 8080, in which the GPM is expected to be used. In each case, the first setting shown is the one that would normally be used and the second setting is the exception (i.e. S1-2 is normally OFF but should be switched to ON if slow memory chips are used).

If the GPM is to be used in any other computer, the switch functions should be studied and set according to the requirements of that computer.

3.3 READ ONLY MEMORY OPTIONS

When assembled according to the instructions in Section 2, your GPM is configured for use with 9216B (2Kx8) ROMs in locations U2, U4, U6, U8, and U9 and no memory chips in locations U1, U3, U5, and U7. By cutting specific traces and installing specific jumpers, you can configure your board to:

1. Replace any 9216B (2Kx8) ROM (U2, U4, U6, U8, and U9) with an 8316E or a 34000P ROM.

2. Replace any 9216B (2Kx8) ROM in locations U2, U4, U6, and U8 with two 2708 (1Kx8) PROMs (two 2708s in U1 and U2 to replace the 9216B in U2, two 2708s in U3 and U4 to replace the 9216B in U4, two 2708s in U5 and U6 to replace the 9216B in U6, or two 2708s in U7 and U8 to replace the 9216B in U8). In order to use 2708 PROMs, you must also add the -5 V dc regulator circuit.

3.3.1 Replacing 9216Bs With 8316Es or 34000Ps

A summary of traces to be cut and jumpers to be added to replace 9216B ROMs with 8316E or 34000P ROMs are given in Table 3-2. Figure 3-1 shows the locations of the traces to be cut and the jumpers to be installed.

Table 3-2. Replacing 9216B (2Kx8) ROMs With 8316E Or 34000P (2Kx8) ROMs

CHIP LOCATION	CUT TRACE	INSTALL JUMPER BETWEEN*
U2	M-P (component side) jj-kk (solder side)	M and GND kk and P
U4	Q-S (solder side) gg-hh (solder side)	Q and GND hh and S
U6	T-W (solder side) ee-ff (solder side)	T and GND ff and W
U8	X-Z (solder side) cc-dd (solder side)	X and GND dd and Z
U9	J-L (component side) aa-bb (solder side)	J and GND bb and L

*Install all jumpers on component side of board using #24 bare wire.

Your GPM is now configured to operate with 8316E or 34000P (2Kx8) ROMs. Return to Section II to complete assembly of your GPM module.

3.3.2 Replacing 9216Bs With Two 2708 PROMs

If 2708 PROMs are used on the GPM module, you must install a -5 V dc regulator circuit (U35, C14, and C18). You need the following components and hardware. This equipment can usually be purchased at any local electronics store.

1	7905 regulator (U35)
1	1 ufd tantalum dipped capacitor (C14)
1	15 ufd tantalum dipped capacitor (C18)
1	6-32 x ½ screw, Nylon
1	#6 lockwasher
1	6-32 hex nut
1	Insulator, mica
1	Heat sink compound

To add this circuit, proceed as follows: (See assembly drawing in Section 5, Page 5-1.)

( ) Step 1. Install U35 (7905). Position U35 over right hand cutout in heat sink and determine how the leads must be bent to fit the mounting holes. Note that the center lead (3) must be bent down at a point approximately 0.2 inches further from the body than the other two leads. Bend leads so that no contact is made with the sink when U35 is flat against the sink and its mounting hole is aligned with the hole in the sink. Coat both sides of the mica insulator and the mating surfaces on the sink and the bottom of U35 with a thin film of heat sink compound. Insert Nylon 6-32 x ½ screw from back (solder) side of board, place insulator over screw on front (component) side, lower U35 over screw and insert leads, place #6 lockwasher on screw and drive hex nut. Solder and trim leads.

( ) Step 2. Install C14 (1 ufd tantalum dipped capacitor) in its location below the heat sink, position C14 with its positive (+) lead to the left, insert leads, solder and trim.

( ) Step 3. Install C18 (15 ufd tantalum dipped capacitor) in its location in lower left corner of board (below U9). Position C18 with its positive (+) lead at the top, insert leads, solder and trim.

( ) Step 4. Check regulator operation. This check is made to prevent potential damage to the ICs from an incorrect voltage. Using an ohmmeter, measure between positive (+) and negative (-) leads of C14. You should measure some resistance. Zero resistance indicates a short. If required, find and correct the problem before proceeding. Especially check for solder bridges.

( ) Install the GPM in computer. (The use of a Processor Technology EXB Extender Board is recommended.)

CAUTION

NEVER INSTALL OR REMOVE GPM
WITH POWER ON.

( ) Turn power on and measure the voltage across C14 (positive lead is ground). You should measure -5 V dc ± 5%. If the voltage is incorrect, determine and correct the cause before proceeding. If the voltage is correct, turn power off, remove GPM from computer and configure the GPM for 2708 PROMs as subsequently described.

A summary of traces to be cut and jumpers to be added to replace a 9216B (2Kx8) ROM (U2, U4, U6, and U8) with two 2708 (1Kx8) PROMs are given in Table 3-3. Figure 3-1 shows the locations of the traces to be cut and the jumpers to be installed. These locations are also printed on the circuit board legend.

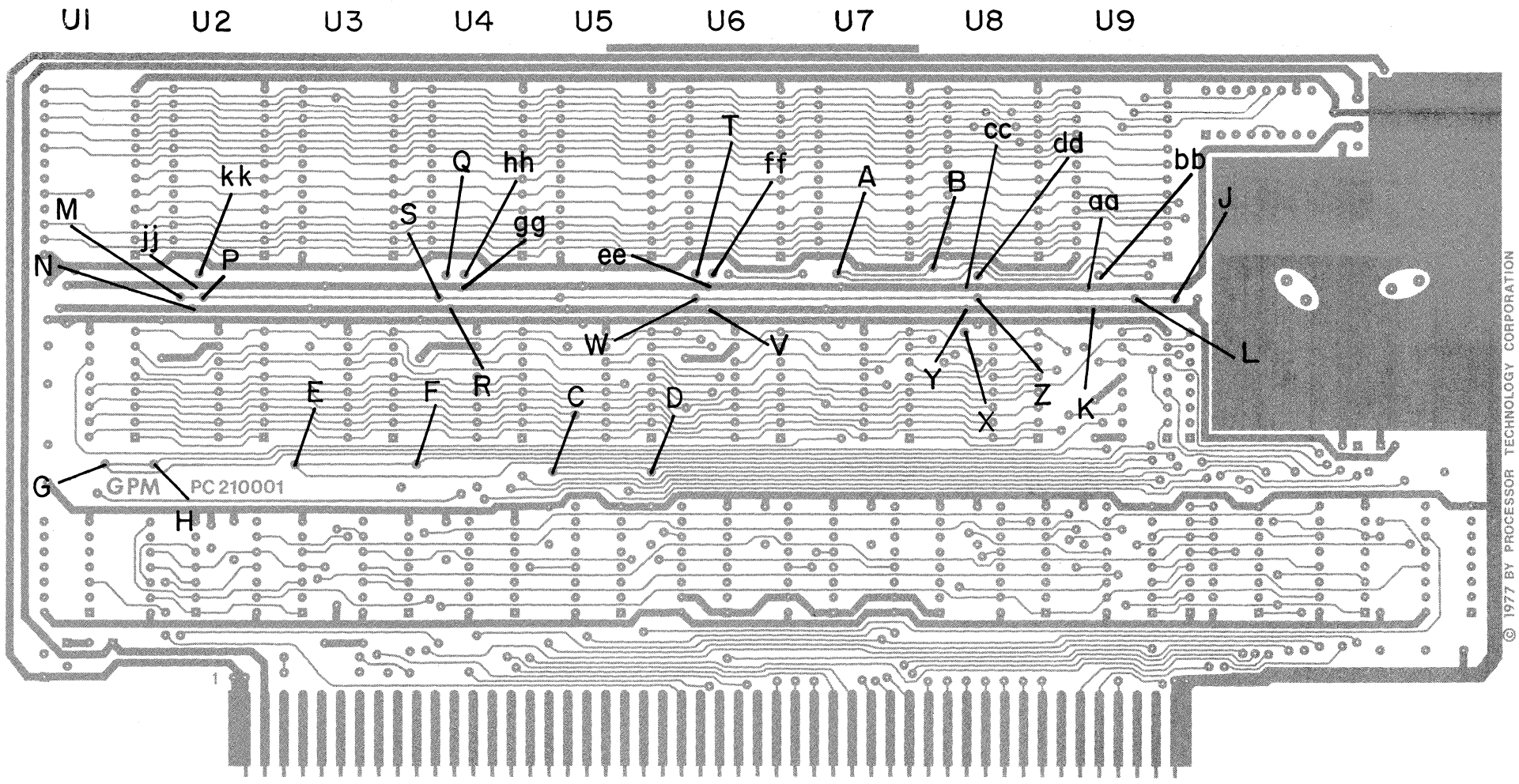
Table 3-3. Replacing 9216B (2Kx8) ROMs With 2708 (1Kx8) ROMs

CHIP LOCATION	CUT TRACE	INSTALL JUMPER BETWEEN*
U1, U2	M-P (component side) G-H (component side)	M and N
U3, U4	Q-S (solder side) E-F (component side)	Q and R
U5, U6	T-W (solder side) C-D (component side)	T and V
U7, U8	X-Z (solder side) A-B (component side)	X and Y

*Install all jumpers on component side of board using #24 bare wire.

Your GPM is now configured to operate with 2708(1Kx8) EPROMs. Return to Section 2 to complete assembly of your GPM module.

Component (front) Side



Solder (back) Side

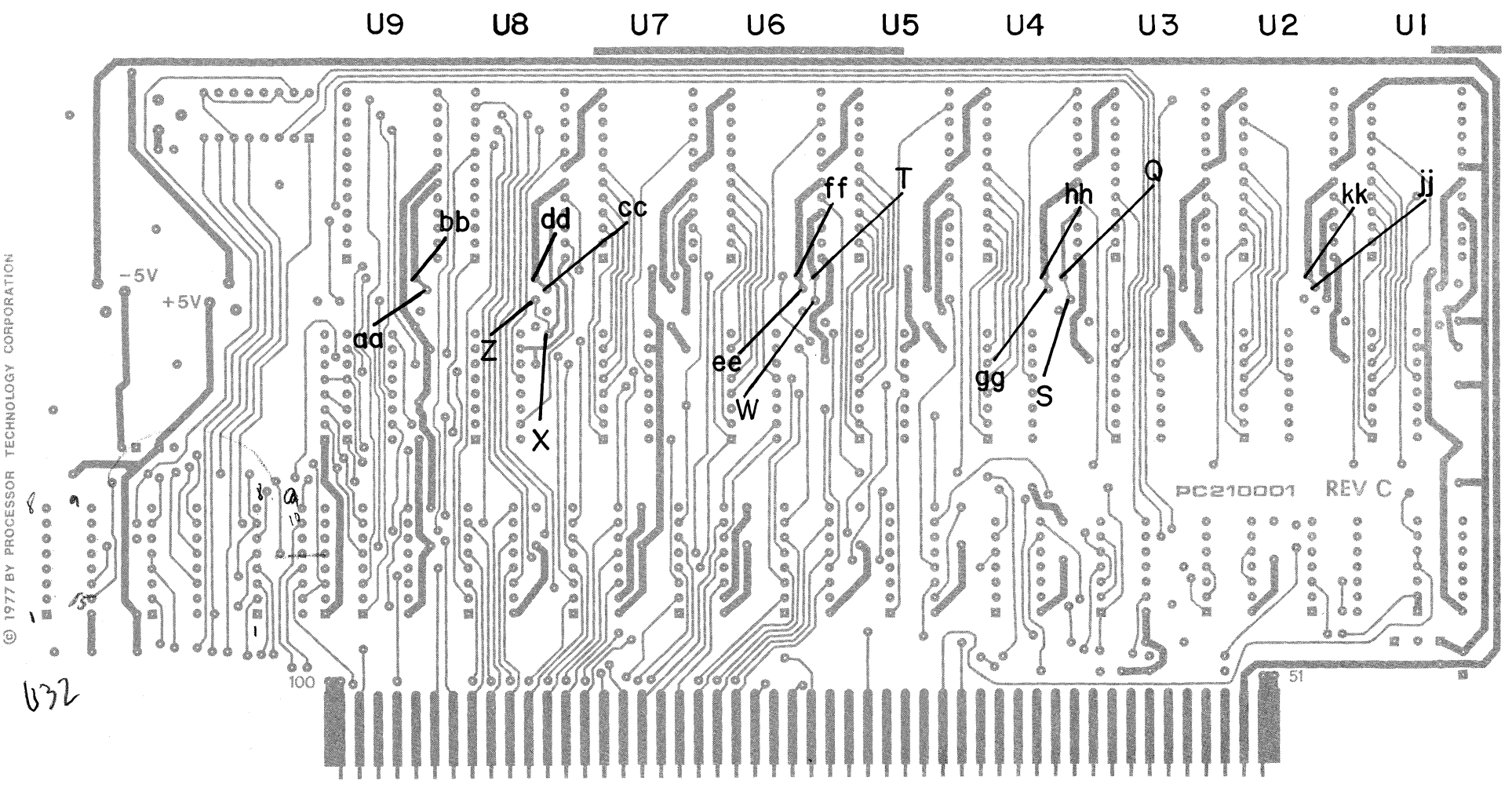


Figure 3-1. Locations for Trace Cuts and Jumpers

SECTION 4

THEORY OF OPERATION

GPM (General Purpose Memory) and GPM-Sol MODULES

4.1 OVERVIEW

The GPM consists of up to 10K of ROM, 1K of RAM, an address decoder, a phantom (automatic) start-up circuit, a wait state circuit, and on-board voltage regulator circuits. While reading the circuit description, pull out the schematic in Section V, Figure 5-2. Also refer to the GPM and GPM-Sol Memory Map in Section 1, Figure 1-1.

4.2 CIRCUIT DESCRIPTION

4.2.1 Address Decoding

Address lines A0 through A9 are buffered from the bus through U25 and U26 to the 10 address pins on each RAM chip (U10 through U17) and ROM/PROM chip (U1 through U9). A10, buffered through U24, is applied to the A10 input to U2, U4, U6, and U8. A10 also appears on pin 21 of U9, and A0 input to U30 and the A input to U31. In addition, A10 provides the enables for ROM chip select drivers U18 and PROM chip enable drivers U29.

The address decoding is done with an 82S129 256x4 PROM (U30), and a small amount of support circuitry. The four outputs of the 82S129 are $\overline{\text{CARD SELECT}}$, ROM C, $\overline{\text{ROM EF}}$, and $\overline{\text{RAM}}$. Any time the 82S129 gets an address that one of the memories on the card should respond to, both $\overline{\text{CARD SELECT}}$ and the appropriate memory line (ROM C, $\overline{\text{ROM EF}}$, or $\overline{\text{RAM}}$) are activated. Whenever $\overline{\text{CARD SELECT}}$ is activated (active low), the buffers from both the wait state circuitry (which outputs to the PRDY line and will be discussed below) and from pin 11 of U22 are activated. Since the inputs to this NAND gate are PDBIN and SMEMR, output 11 will go low whenever the processor is requesting data from memory. Thus, when CARD SELECT is low pin 13 of U32 will go low whenever the processor is requesting data. This signal goes to both U20 (the phantom start-up circuitry which will be discussed later) and to enable the data bus drivers, U28 and U29. So, whenever data is requested from one of the memories on the GPM, the appropriate memory line (ROM C, $\overline{\text{ROM EF}}$, or $\overline{\text{RAM}}$) is activated as well as $\overline{\text{CARD SELECT}}$ which in turn activates both the wait state output driver and the data bus drivers.

The question that arises here is: which addresses does each memory respond to? The answer is that it depends on whether or not it is during phantom start-up (pin 15 of the 82S129 is pulled low thru either S1-6 or S1-8) and whether or not the GPM is being used in a Sol (pin 1 of the 82S129 is pulled low thru S1-7). The following table summarizes the address to which each memory will respond under the four basic conditions:

Table 4-1. Memory Allocation Table

Memory Line	Sol (S1-7 is ON)		Non-Sol	
	PHANTOM	NORMAL OPERATION	PHANTOM	NORMAL OPERATION
ROM C	None	None	ØØØØ-Ø3FF (if S1-3 is open)	CØØØ-C7FF
ROM EF	None	EØØØ-EFFF	ØØØØ-Ø3FF (if S1-1 is open)	EØØØ-FFFF
RAM	None	ØØØØ-Ø3FF	None	C8ØØ-CBFF

4.2.2 Memory Allocation

The memory block EØØØ to FFFF consists of either four 2K ROMs (U2, U4, U6, and U8) or eight 1K PROMs (U1 through U8). Memory allocations for this block are as follows:

ROM CONFIGURATION

SOCKET	4-2K CHIPS	8-1K CHIPS
U1	---	F8ØØ - FBFF
U2	F8ØØ - FFFF	FCØØ - FFFF
U3	---	FØØØ - F3FF
U4	FØØØ - F7FF	F4ØØ - F7FF
U5	---	F80Ø - EBFF
U6	E8ØØ - EFFF	ECØØ - EFFF
U7	---	EØØØ - E3FF
U8	EØØØ - E7FF	E4ØØ - E7FF

Memory block CØØØ - C7FF is assigned to U9, a 2K ROM.

The 1K of RAM (U10 through U17) can be addressed at either C8ØØ - CBFF when the GPM is used with non-Sol computers at ØØØØ - Ø3FF when it is used with the Sol.

4.2.3 Read Operation

In a GPM read operation, data is read from either ROM/PROM or RAM, as requested, to the Data In Bus (DIØ-7) via buffers U28 and U29. The Data Out (DO) outputs of the RAM and ROM/PROM chips are tri-stated types that float in a high impedance state when they are not selected. They are therefore connected in parallel. As a result, only the bits in the addressed memory can be gated to DI0-7.

Assuming the processor requests data from the GPM (PDBIN and SMEMR are both high on Bus Pins 78 and 47 respectively and it is appropriately addressed), $\overline{\text{CARD SELECT}}$ and the applicable memory line are activated.

$\overline{\text{CARD SELECT}}$ (active low) enables the PRDY (Bus pin 72) line driver, U32-11, and enables U32-13. With S1-2 open, PRDY will be high and the processor will be in the run state. One wait state is imposed if S1-2 is closed. (Refer to Paragraph 4.2.6) Since PDBIN and SMEMR are low when the GPM is accessed, the low on pin 13 of U32 enables the DI Bus drivers U28 and U29.

Should the RAM be addressed, $\overline{\text{RAM}}$ is low to enable U10 through U17 to present data to U18 and U29, the DI Bus drivers. Note that $\overline{\text{RAM}}$ also enables U24-9 which gates the inverted MEM WR (Bus pin 68) to the $\overline{\text{WE}}$ inputs of each RAM chip. MEM WR is low for a read operation, so the $\overline{\text{WE}}$ input is high. $\overline{\text{RAM}}$ can also be applied to pin 15 of U30 through S1-3. This disables the RAM at ØØØØ - Ø3FF.

If U9 is addressed, ROM C will be active (high), and providing $\overline{\text{PHANTOM}}$ is not low on U22-9 through S1-3, U22-8 is low to enable U9 to present data to the DI Bus drivers.

With $\overline{\text{ROM EF}}$ active (low), U31 decodes address lines A10, A11, and A12 to determine which of U1 through U8 is to be accessed. The enables for U2, U4, U6, and U8 are gated when A10 is high by U18, and the enables for U1, U3, U5, and U7 are gated when A10 is low by U29. Switch S1-1 determines whether or not EØØØ - EFFF is disabled (S1-1 closed) during automatic start-up.

4.2.4 Write Operation

The GPM write operation is similar to a read operation. Data is written from the Data Out (DO) Bus (DO0-7) into the RAM memory. Each DO line is buffered (U26 and U27) to the Data In (DI) of one RAM chip. Thus, each RAM chip stores one bit of the word written into Ram.

The main difference between a read and a write operation is that in a write operation MEM WR is high instead of SMEMR and only the RAM will be active. In this case the low on pin 6 of U19 is gated to the WE input of each RAM so that the data on the DO Bus can be written into U10 through U17.

4.2.5 Phantom (Automatic) Start-Up

The phantom start-up circuitry (see GPM Schematic, Section 5, Figure 5-2) consists of flip-flop U20 and one-half of U21. When the power is turned on, $\overline{\text{POC}}$ (Bus pin 99) resets the R-S flip-flop which consists of two (2) gates from U22 pulling pin 3 low. This, in turn, resets the phantom flip-flops. As C30 charges up, it turns Q1 off. With Q1 off, R11 pulls pin 1 low, which sets the R-S flip-flop (U22-3) high. Pin 5 of U21, which has been reset to zero (0), pulls pin 15 of the 82S129 ROM (U30) low from pin 11 of U18 (provided S1-6 is closed). Thus, the memories on the board will respond as indicated under PHANTOM start-up in Table 3-1.

If $\overline{\text{PRESET}}$ is pulled low (either through S1-5 in an ALTAIR 8800 or from the front panel of an IMSAI 8080), the processor begins executing code at ØØØØ. The first four bytes in ROM C or ROM EF will be typically one byte NOOP (ØØ) and a three byte JMP (C3 XX XX). As the processor reads these four bytes, U20 counts the memory access pulses from pin 13 of U32. Pin 5 of U21 goes high on the fourth access, the GPM goes into normal operation, and the processor jumps to address XX XX to begin executing code.

4.2.6 Wait State Circuit

The Q output of wait state flip-flop, U21-9, is reset low by PSYNC (Bus pin 76) at the start of each machine cycle. An inverted 2 from pin 3 of U19 clocks U21-9 back to a high at the end of each machine cycle. Consequently U21-9 generates a wait state that is one machine cycle in duration.

If S1-2 is closed, this wait state is placed on the PRDY line (Bus pin 72) via U32-11 each time the GPM is accessed. This causes the processor to enter the wait condition and allows the GPM two cycles, rather than one, to respond.

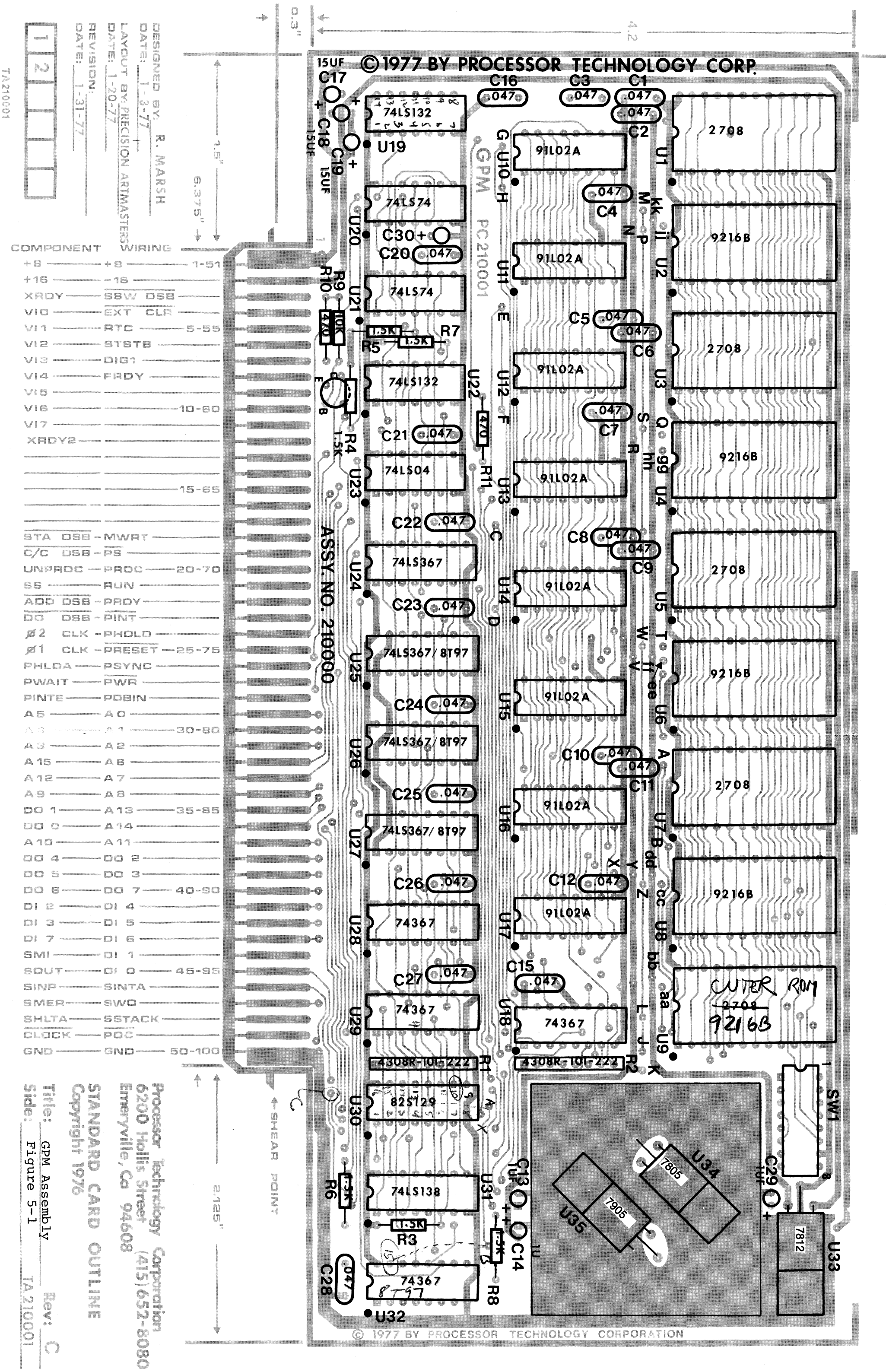
4.2.7 Regulators

U33 and U34, series voltage regulators, supply on-card regulation to maintain constant +12 V and +5 V dc outputs respectively. (If installed, U35 provides on-card regulation to maintain a constant -5 V dc output.) Input capacitor C17 provides additional filtering of the +8 V dc input, as does C19 for the +18 V dc input. The output bypass capacitors C13 and C29 improve transient response. (C18 and C14 in the -5 V dc regulator, if installed, serve the same functions as their counterparts in the +12 and +5 V dc supplies.)

SECTION 5

DRAWINGS

GPM (General Purpose Memory) and GPM-Sol MODULES


© 1977 BY PROCESSOR TECHNOLOGY CORP.
GPM PC210001
ASSY. NO. 210000
© 1977 BY PROCESSOR TECHNOLOGY CORPORATION
COMPONENT WIRING
+8 +8 1-51
+16 -16
XRDY SSW DSB
VI0 EXT CLR
VI1 RTC 5-55
VI2 STSTB
VI3 DIG1
VI4 FRDY
VI5
VI6 10-60
VI7
XRDY2
15-65
STA DSB - MWRT
C/C DSB - PS
UNPROC PROC 20-70
SS RUN
ADD DSB - PRDY
DO DSB - PINT
ø2 CLK - PHOLD
ø1 CLK - PRESET 25-75
PHLDA PSYNC
PWAIT PWR
PINTE PDBIN
A5 A0
A4 A1 30-80
A3 A2
A15 A6
A12 A7
A9 A8
DO 1 A13 35-85
DO 0 A14
A10 A11
DO 4 DO 2
DO 5 DO 3
DO 6 DO 7 40-90
DI 2 DI 4
DI 3 DI 5
DI 7 DI 6
SMI DI 1
SOUT DI 0 45-95
SINP SINTA
SMER SWO
SHLTA SSTACK
CLOCK POC
GND GND 50-100
DESIGNED BY: R. MARSH
DATE: 1-3-77
LAYOUT BY: PRECISION ARTMASTERS
DATE: 1-20-77
REVISION:
DATE: 1-31-77
TA210001
1 2
0.3"
4.2
1.5"
6.375"
2.125"
SHEAR POINT
Processor Technology Corporation
6200 Hollis Street (415)652-8080
Emeryville, Ca 94608
STANDARD CARD OUTLINE
Copyright 1976
Title: GPM Assembly
Side: Figure 5-1
Rev: C
TA210001
C17 15UF
C18 15UF
C19 15UF
C16 .047
C3 .047
C1 .047
C2 .047
C4 .047
C5 .047
C6 .047
C7 .047
C8 .047
C9 .047
C10 .047
C11 .047
C12 .047
C15 .047
C20 .047
C21 .047
C22 .047
C23 .047
C24 .047
C25 .047
C26 .047
C27 .047
C28 .047
C30+
C13 1UF
C14 1UF
C29 1UF
U19 74LS132
U20 74LS74
U21 74LS74
U22 74LS132
U23 74LS04
U24 74LS367
U25 74LS367/8T97
U26 74LS367/8T97
U27 74LS367/8T97
U28 74367
U29 74367
U30 82S129
U31 74LS138
U32 74367 8T97
U33 7812
U34 7805
U35 7905
U1 2708
U2 9216B
U3 2708
U4 9216B
U5 2708
U6 9216B
U7 2708
U8 9216B
U9 OUTER ROM 2708 9216B
U10 91L02A
U11 91L02A
U12 91L02A
U13 91L02A
U14 91L02A
U15 91L02A
U16 91L02A
U17 91L02A
U18 74367
R1 4308R-101-222
R2 4308R-101-222
R3 1.5K
R4 1.5K
R5 1.5K
R6 1.5K
R7 1.5K
R8 1.5K
R9 10K
R10 470
R11 470
SW1

LTR	REVISION DESCRIPTION	DATE	APPROVED
C	REV'D PER ENG'NG MARK-UP		

NOTES: UNLESS OTHERWISE SPECIFIED:
1. R1 & R2 VALUES ARE 2.2K RESISTOR PACK
2. OTHER RESISTORS VALUE ARE 1.5K, 1/4W, ±5%
3. ALL CAPACITORS VALUE ARE IN MICROFARAD

REF DES.	FIRST USED	LAST USED	NOT USED
U	1	35	
R	1	8	
C	1	30	
S	1	1	
Q	1	1	

REF. DES.	PART OR DWG. NO.	PART DESCRIPTION
NEXT ASSY.	USED ON	
210000	GPM	

Processor Technology Corporation
6200 Hollis Street
Emeryville, CA 94608

DRAWN: S TONG | ENGR:
DATE: 4/30/77 | DATE:
CHECKED: | RELEASED:
DATE: | DATE:

SCHEMATIC, GPM MODULE

Figure 5-2

C REV. | 210002 DRAWING NO. | SCALE: NONE | SHEET 1 OF 1 | D SIZE

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-8893

APPENDICES

GPM (General Purpose Memory) and GPM-Sol MODULES

Warranty

PROCESSOR TECHNOLOGY CORPORATION, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by **Processor Technology Corporation** are purchased through normal factory distribution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 3 months for kits, and one year for assembled modules, following the date of purchase. The defective part must be returned postpaid to **Processor Technology Corporation** within the warranty period.

Any malfunctioning module, purchased as a kit directly from **Processor Technology** and returned to the factory within the three-month warranty period, which in the judgement of **PTC** has been assembled with care and not subjected to electrical or mechanical abuse, will be restored to proper operating condition and returned, regardless of cause of malfunction, without charge. Kits purchased from authorized **PTC** dealers should be returned to the selling dealer for the same warranty service.

Any modules purchased as a kit and returned to **PTC,** which in the judgement of **PTC** are not covered by the above conditions, will be repaired and returned at a cost commensurate with the work required. In any case, this charge will not exceed $20.00 without prior notification and approval of the owner.

Any modules, purchased as assembled units are guaranteed to meet specifications in effect at the time of manufacture for a period of at least one year following purchase. These modules are additionally guaranteed against defects in materials or workmanship for the same one year period. All warranted factory assembled units returned to **PTCO** postpaid will be repaired and returned without charge.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.

JUMP

C3	JMP	Adr
C2	JNZ	
CA	JZ	
D2	JNC	
DA	JC	
E2	JPO	
EA	JPE	
F2	JP	
FA	JM	
E9	PCHL	

CALL

CD	CALL	Adr
C4	CNZ	
CC	CZ	
D4	CNC	
DC	CC	
E4	CPO	
EC	CPE	
F4	CP	
FC	CM	

RETURN

C9	RET
C0	RNZ
C8	RZ
D0	RNC
D8	RC
E0	RPO
E8	RPE
F0	RP
F8	RM

RESTART

C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7

ROTATE†

07	RLC
0F	RRC
17	RAL
1F	RAR

CONTROL

00	NOP
76	HLT
F3	DI
FB	EI

MOVE (cont)

58	MOV	E,B	
59	MOV	E,C	
5A	MOV	E,D	
5B	MOV	E,E	
5C	MOV	E,H	
5D	MOV	E,L	
5E	MOV	E,M	
5F	MOV	E,A	
60	MOV	H,B	
61	MOV	H,C	
62	MOV	H,D	
63	MOV	H,E	
64	MOV	H,H	
65	MOV	H,L	
66	MOV	H,M	
67	MOV	H,A	
68	MOV	L,B	
69	MOV	L,C	
6A	MOV	L,D	
6B	MOV	L,E	
6C	MOV	L,H	
6D	MOV	L,L	
6E	MOV	L,M	
6F	MOV	L,A	
70	MOV	M,B	
71	MOV	M,C	
72	MOV	M,D	
73	MOV	M,E	
74	MOV	M,H	
75	MOV	M,L	
	---	---	
77	MOV	M,A	
78	MOV	A,B	
79	MOV	A,C	
7A	MOV	A,D	
7B	MOV	A,E	
7C	MOV	A,H	
7D	MOV	A,L	
7E	MOV	A,M	
7F	MOV	A,A	

ACCUMULATOR*

80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
87	ADD	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
8F	ADC	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
97	SUB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
9F	SBB	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
A7	ANA	A
A8	XRA	B
A9	XRA	C
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
AF	XRA	A
B0	ORA	B
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
B7	ORA	A
B8	CMP	B
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
BF	CMP	A

CONSTANT DEFINITION

0BDH	Hex
1AH	
105D	Decimal
105	
72O	Octal
72Q	
11011B	Binary
00110B	
'TEST'	ASCII
'A' 'B'	

OPERATORS

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\+ −

MOVE IMMEDIATE

06	MVI	B,	D8
0E	MVI	C,	
16	MVI	D,	
1E	MVI	E,	
26	MVI	H,	
2E	MVI	L,	
36	MVI	M,	
3E	MVI	A,	

Acc IMMEDIATE*

C6	ADI		D8
CE	ACI		
D6	SUI		
DE	SBI		
E6	ANI		
EE	XRI		
F6	ORI		
FE	CPI		

LOAD IMMEDIATE

01	LXI	B,	D16
11	LXI	D,	
21	LXI	H,	
31	LXI	SP,	

STACK OPS

C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW*
E3	XTHL	
F9	SPHL	

MOVE

40	MOV	B,B	
41	MOV	B,C	
42	MOV	B,D	
43	MOV	B,E	
44	MOV	B,H	
45	MOV	B,L	
46	MOV	B,M	
47	MOV	B,A	
48	MOV	C,B	
49	MOV	C,C	
4A	MOV	C,D	
4B	MOV	C,E	
4C	MOV	C,H	
4D	MOV	C,L	
4E	MOV	C,M	
4F	MOV	C,A	
50	MOV	D,B	
51	MOV	D,C	
52	MOV	D,D	
53	MOV	D,E	
54	MOV	D,H	
55	MOV	D,L	
56	MOV	D,M	
57	MOV	D,A	

DOUBLE ADD†

09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP

SPECIALS

EB	XCHG	
27	DAA*	
2F	CMA	
37	STC‡	
3F	CMC‡	

INPUT/OUTPUT

D3	OUT	D8
DB	IN	D8

INCREMENT**

04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3C	INR	A
03	INX	B
13	INX	D
23	INX	H
33	INX	SP

DECREMENT**

05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
3D	DCR	A
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP

LOAD/STORE

0A	LDAX	B
1A	LDAX	D
2A	LHLD	Adr
3A	LDA	Adr
02	STAX	B
12	STAX	D
22	SHLD	Adr
32	STA	Adr

PSEUDO INSTRUCTION

ORG	Adr	
END		
EQU	D16	
DS	D16	
DB	D8	[ ]
DW	D16	[ ]

STANDARD SETS

A	SET	7
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
SP	SET	6
PSW	SET	6

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

* = all Flags (C,Z,S,P) affected

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

† = only CARRY affected

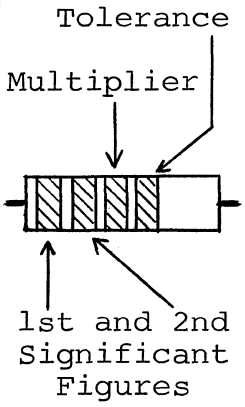
Adr = 16 bit address

** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)

The electrical value of many types of resistors and capacitors is printed on the component. Other types, however, are identified by color coding which gives all the information needed to correctly identify the component. In most cases color coding conforms with the EIA (Electronic Industries Association) Standard Color Code. In other cases a manufacturer will adapt the standard to fit his particular requirement. Both the Standard Color Code and a code used to identify tantalum dipped capacitors are provided below.

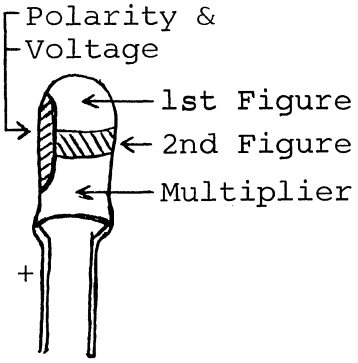
STANDARD COLOR CODE FOR RESISTORS AND CAPACITORS

COLOR	1st FIGURE	2nd FIGURE	MULTIPLIER	TOLERANCE (%)	VOLTAGE RATING*
Black	0	0	1		--
Brown	1	1	10		100
Red	2	2	100		200
Orange	3	3	1,000		300
Yellow	4	4	10,000		400
Green	5	5	100,000		500
Blue	6	6	1,000,000		600
Violet	7	7	10,000,000		700
Gray	8	8	100,000,000		800
White	9	9	1,000,000,000		900
Gold	-	-	0.1	5	1000
Silver	-	-	0.01	10	2000
None	-	-	---	20	500



*Applies only to capacitors.

RATED VOLTAGE VDC 25°C	COLOR	CAPACITANCE IN PICOFARADS		
		1st Figure	2nd Figure	Multiplier (uuF)
3-4	Black	0	0	1
3-6	Brown	1	1	10
3-10	Red	2	2	100
3-15	Orange	3	3	1,000
3-20	Yellow	4	4	10,000
3-25	Green	5	5	100,000
3-35	Blue	6	6	1,000,000
3-50	Violet	7	7	10,000,000
--	Gray	8	8	---
3	White	9	9	---



LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

(1) Sockets. DIP sockets are marked to indicate the correct orientation for the IC which will be inserted. This mark may be a notch at the end of the socket, or a filled-in corner on the inside of the socket as shown in the Component Ientification Illustrations in Section II.

Orient the socket so that pin 1 lines up with the indication for pin 1 printed on the printed circuit board legend, which may be a white dot. Insert the socket into the board, and while pressing the socket into place to ensure that it is fully seated, bend two diagonally opposite pins to retain the socket in its fully seated position while soldering.

(2) ICs. Many DIP devices have their leads spread so that they may not be inserted directly into their sockets. They must be "walked in" using the following procedure.

Orient pin 1 of the device so that it lines up with pin 1 on the socket and the printed circuit board legend. Insert the pins from one row only into the socket until they barely engage. Push the device using both hands with even pressure to bend this first row of pins until the second row of pins lines up with the holes in the socket, then push the second row of pins into the socket. After all ICs are inserted, examine each to make sure that no pins are bend out or under. Careful examination might prevent hours of unnecessary troubleshooting later.

SOLDERING TIPS

(1) Use a low-wattage iron--25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.

(2) Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.

(3) Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

NOTE: DO NOT press the top of the iron on the pad or trace. This will cause the trace to "lift" off of the board which will result in permanent damage.

(4) In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder

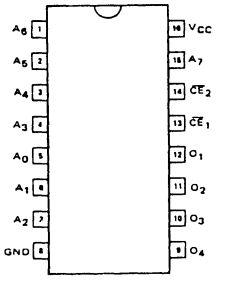
melts the rest of the joint will be hot enough for the solder to "take", (i.e., form a capillary film).

(5) Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.

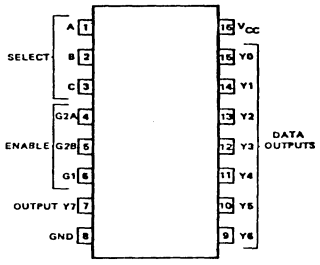
(6) Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.

(7) To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.

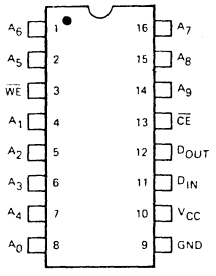
82S129B



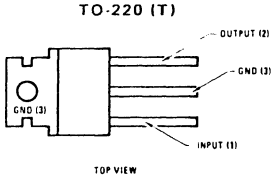
74LS138



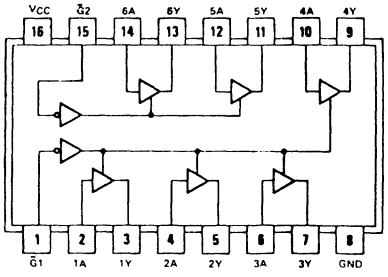
91L02A (AMD)



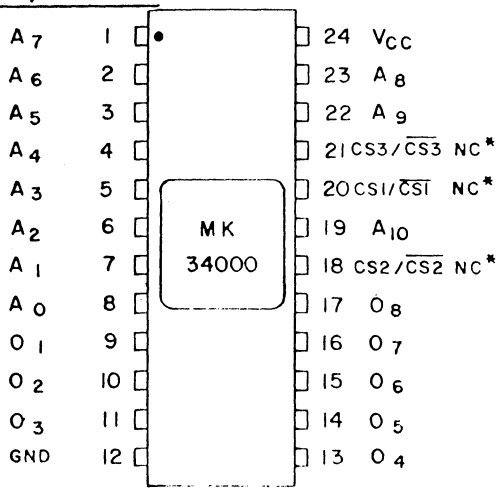
7805, 7812



74367, 74LS367

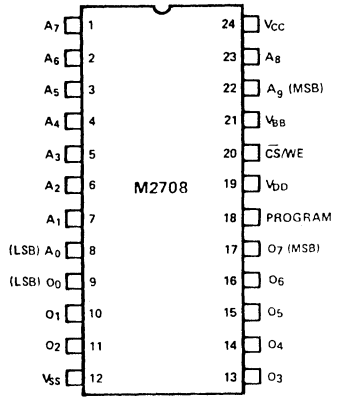


34000P, 8316E

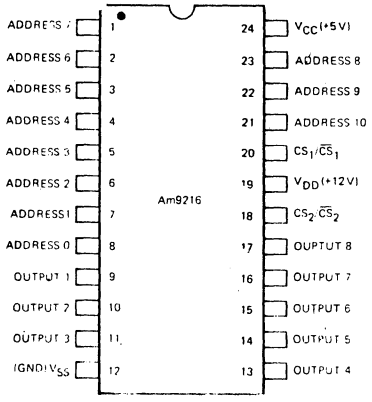


*Programmable Chip Selects

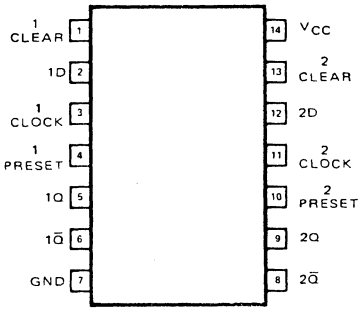
2708



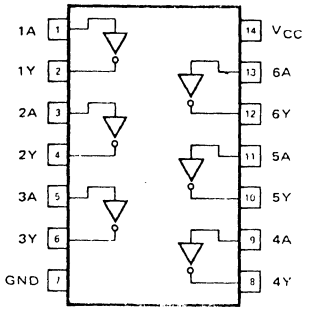
9216B (AMD)



74LS74

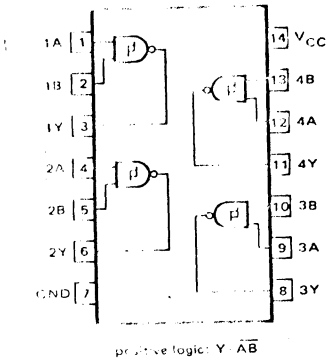


74LS04



Positive logic: $Y = \overline{A}$

74LS132



positive logic: $Y = \overline{AB}$

Processor Technology

Change Notice #1A

A set of three or four ROMs containing the ALS-8 program development system may be used on the GPM and GPM-Sol boards. Alternative procedures are given below for entering the ALS-8 program from the SOLOS monitor program in the Sol Terminal Computer with GPM-Sol, and from the CUTER monitor program in ROM on GPM. The procedure differs also depending on whether serial data input is used, as from a teletype or CRT terminal, or parallel data input is used, as from a keyboard. The procedures assume that a VDM-1 video display module is in use.

1) Serial Data Input

   a) From the CUTER command mode, type EXEC EØ24 (Carriage Return).

   b) Type Control-Z (CR), i.e., depress Z and CTRL key simultaneously. This initializes the ALS-8 video display driver, clearing parameters.

   c) Next type Control-S. The ALS-8 program will respond: SPEED?

   d) Lastly, type one key from 1 to 9 (CR) to set the rate at which new characters are added to the video display. Normally type 1 for the fastest speed. ALS-8 is now ready to use.

   e) To exit to CUTER from ALS-8, type EXEC CØØ3 (CR).

2) Parallel Data Input

   a) From the SOLOS/CUTER command mode, type EXEC EØ24 (CR). This moves the ALS-8 input and output driver from ROM into RAM, where they may be modified.

   b) In a Sol, with GPM-Sol, Press Upper Case and Repeat keys simultaneously. In other computers, first stop the computer from running, then start up CUTER again, at location CØØØ. The video display will respond with a prompt.

   c) Enter the data shown below. The underline indicates characters which are responses from SOLOS/CUTER:

ENTRIES FOR CUTER	ENTRIES FOR SOLOS
ENTR DØ9F (CR)	ENTR DØ9F (CR)
: 03 (CR)	: FC (CR)
: DØA6: 2F E6 Ø1 C9 (CR)	: DØA5: FA 2F E6 Ø1 C9 (CR)
: DØDØ: 77 FE (CR)	: DØDØ: 77 FE (CR)
: DØ96: 77 FE / (CR)	: DØ96: 77 FE / (CR)

SOLOS/CUTER should again respond with a prompt: ⟩ . The above entries modify the standard input and output drivers, which are written for a serial console interface, to work with a parallel console interface, as for a keyboard. You may want to record these entries on tape for later use.

e) Type EXEC EØ6Ø to transfer control to the ALS-8. Do not try to start the ALS-8 at EØ24 as this will reinitialize the drivers, erasing the entries just made.

f) Do steps b, c, and d from Serial Data Input procedure above.

g) To exit to SOLOS/CUTER from ALS-8, type EXEC CØØ3 (CR).

Processor Technology

Change Notice #2

1) Refer to Section 2, page 2-7, Step 3.

   This step calls for the installation of U33, a 7812 voltage regulator IC. Please note that this regulator does not go on the heat sink. It goes on the top the board above the heat sink, with the leads facing to the left, as described in this assembly step. Only U34, a 7805 goes on the heat sink. The heat sink is designed for two parts, and there are pads for an additional regulator on the heat sink, but these are for the optional regulator U35, which is not supplied with this kit. U35, a negative regulator, is only used if the GPM is later set up for 2708 ROMs. Two other parts, C14 and C18, are not included in the kit and are only needed if U35 is installed. Mark Step 3 to refer you to this page, so that when you come to this point in the assembly procedures, you will be reminded to reread this information.

2) Refer to Section 3, page 3-4, Step 4.

   It is recommended that the check procedure in this step be repeated for C18, to ensure there is no short accross the -17 volt supply. Note this step is only necessary if the optional negative regulator U35 is installed. Make a note below step 4 containing this information.

3) Refer to Section 3, page 3-4, Step 3.

   In the second line of this step, change "(below U9)" to read, "(below U19)".

PROCESSOR TECHNOLOGY CORPORATION 6200 HOLLIS STREET EMERYVILLE CA 94608 (415) 652-8080

Users of Processor Technology's General Purpose Memory Module (GPM) board, part of the widely advertised Subsystem B, will find that they can not load or use the cassette tape version of the ALS-8 Assembler without first modifying the GPM board.

The problem is caused by the fact that the GPM board responds to memory addresses in the range of E000H to FFFFH, whether or not any ROM chips are installed on the board.

The following modification to the board disables this response and allows locating a standard 8K RAM board in this address space, so that the ALS-8 tape can be loaded. The modification does not affect operation of the CUTER monitor or of the PHANTOM startup feature to the CUTER monitor.

IN THE FOLLOWING INSTRUCTIONS, ALL LOCATION DESCRIPTIONS ASSUME THE BOARD TO BE HELD WITH THE COMPONENT SIDE FACING YOU AND THE EDGE CONNECTOR DOWN AS SHOWN IN THE CARD OUTLINE DRAWING (FIG 5-1) IN THE GPM MANUAL

1) On the front (component side of the board), cut the thin trace connecting the pad located near the top end of U30 and the pad located under the body of R8.

NOTE 1: This is the first thin trace just above the top end of U31. This trace carries the card select signal from pin 12 of U30 to pin 15 of U32. By cutting the trace between these pads, the board can easily be returned to its original state should you ever install ROM chips for the ALS-8.

2) On the rear (copper side of the board), connect the following seven wire jumpers:

FROM	TO	
pin 10 of U30	pin 1 of U23	NOTE 2
pin 2 of U23	pin 12 of U19	
pin 10 of U19	pin 11 of U19	
top end of R3	pin 13 of U19	NOTE 3
pin 12 of U30	pin 11 of U23	NOTE 4
pin 10 of U23	pin 9 of U19	
pin 8 of U19	pin 15 of U32	NOTE 5

NOTE 2: Pin 10 of U30 is available at a pad below U30. This pad may be located by following the thin trace, on the rear of the board, from this pin down to the pad adjacent to the "1"

digit of the number "100" located near the bottom edge connector.

NOTE 3: The PHANTOM signal is available at several locations on the board. The most convenient one from a wiring standpoint seems to be at the top end of R3.

NOTE 4: Pin 12 of U30 is available at the pad above U30 refered to in step 1.

NOTE 5: Pin 15 of U32 is available at the pad under the body of R8, refered to in step 1.

The overall circuit will look as in the attached logic diagram

The following GPM manual errors, discovered during the course of the above design, may also be of interest:

Table 3-1 The S1-8 description should read "allows phantom signals from auto start (on GPM) to S-100 bus". Switch settings should show S1-8 "ON" for an IMSAI, if auto start from the GPM is desired.

Figure 5-1 (card outline drawing) and figure 5-2 (schematic) both identify U9 as a Prom B, a 2708. U9 is really ROM C, the OUTER ROM, a 9216B.

Figure 5-2 (schematic) has several other errors:

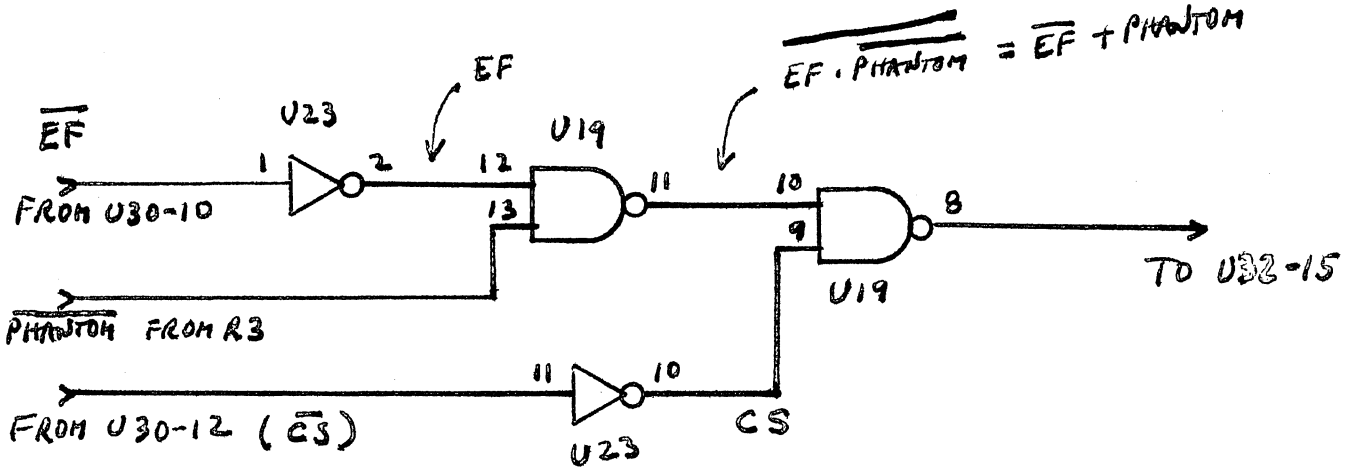
The signal at U30 pin 12 (CARD SELECT) should be shown as active low.

The signal at U30 pin 9 (ROM C) should be shown as active high.

The unlabeled dual input gate shown connected to bus pin 76, is really an inverter (U23) with pin 9 as input and pin 8 as output.

Ed Elizondo
6 Cypress Court
East Windsor, N.J. 08520

21 April 1978



GPM FIX FOR ALS-8

EE 1/9/78

00	NOP		28	---		50	MOV	D,B	78	MOV	A,B	A0	ANA	B	C8	RZ		F0	RP				
01	LXI	B,D16	29	DAD	H	51	MOV	D,C	79	MOV	A,C	A1	ANA	C	C9	RET		F1	POP	PSW			
02	STAX	B	2A	LHLD	Adr	52	MOV	D,D	7A	MOV	A,D	A2	ANA	D	CA	JZ		F2	JP	Adr			
03	INX	B	2B	DCX	H	53	MOV	D,E	7B	MOV	A,E	A3	ANA	E	CB	---		F3	DI				
04	INR	B	2C	INR	L	54	MOV	D,H	7C	MOV	A,H	A4	ANA	H	CC	CZ	Adr	F4	CP	Adr			
05	DCR	B	2D	DCR	L	55	MOV	D,L	7D	MOV	A,L	A5	ANA	L	CD	CALL	Adr	F5	PUSH	PSW			
06	MVI	B,D8	2E	MVI	L,D8	56	MOV	D,M	7E	MOV	A,M	A6	ANA	M	CE	ACI	D8	F6	ORI	D8			
07	RLC		2F	CMA		57	MOV	D,A	7F	MOV	A,A	A7	ANA	A	CF	RST	1	F7	RST	6			
08	---		30	---		58	MOV	E,B	80	ADD	B	A8	XRA	B	D0	RNC		F8	RM				
09	DAD	B	31	LXI	SP,D16	59	MOV	E,C	81	ADD	C	A9	XRA	C	D1	POP	D	F9	SPHL				
0A	LDAX	B	32	STA	Adr	5A	MOV	E,D	82	ADD	D	AA	XRA	D	D2	JNC	Adr	FA	JM	Adr			
0B	DCX	B	33	INX	SP	5B	MOV	E,E	83	ADD	E	AB	XRA	E	D3	OUT	D8	FB	EI				
0C	INR	C	34	INR	M	5C	MOV	E,H	84	ADD	H	AC	XRA	H	D4	CNC	Adr	FC	CM	Adr			
0D	DCR	C	35	DCR	M	5D	MOV	E,L	85	ADD	L	AD	XRA	L	D5	PUSH	D	FD	---				
0E	MVI	C,D8	36	MVI	M,D8	5E	MOV	E,M	86	ADD	M	AE	XRA	M	D6	SUI	D8	FE	CPI	D8			
0F	RRC		37	STC		5F	MOV	E,A	87	ADD	A	AF	XRA	A	D7	RST	2	FF	RST	7			
10	---		38	---		60	MOV	H,B	88	ADC	B	B0	ORA	B	D8	RC							
11	LXI	D,D16	39	DAD	SP	61	MOV	H,C	89	ADC	C	B1	ORA	C	D9	---							
12	STAX	D	3A	LDA	Adr	62	MOV	H,D	8A	ADC	D	B2	ORA	D	DA	JC	Adr						
13	INX	D	3B	DCX	SP	63	MOV	H,E	8B	ADC	E	B3	ORA	E	DB	IN	D8						
14	INR	D	3C	INR	A	64	MOV	H,H	8C	ADC	H	B4	ORA	H	DC	CC	Adr						
15	DCR	D	3D	DCR	A	65	MOV	H,L	8D	ADC	L	B5	ORA	L	DD	---							
16	MVI	D,D8	3E	MVI	A,D8	66	MOV	H,M	8E	ADC	M	B6	ORA	M	DE	SBI	D8						
17	RAL		3F	CMC		67	MOV	H,A	8F	ADC	A	B7	ORA	A	DF	RST	3						
18	---		40	MOV	B,B	68	MOV	L,B	90	SUB	B	B8	CMP	B	E0	RPO							
19	DAD	D	41	MOV	B,C	69	MOV	L,C	91	SUB	C	B9	CMP	C	E1	POP	H						
1A	LDAX	D	42	MOV	B,D	6A	MOV	L,D	92	SUB	D	BA	CMP	D	E2	JPO	Adr						
1B	DCX	D	43	MOV	B,E	6B	MOV	L,E	93	SUB	E	BB	CMP	E	E3	XTHL							
1C	INR	E	44	MOV	B,H	6C	MOV	L,H	94	SUB	H	BC	CMP	H	E4	CPO	Adr						
1D	DCR	E	45	MOV	B,L	6D	MOV	L,L	95	SUB	L	BD	CMP	L	E5	PUSH	H						
1E	MVI	E,D8	46	MOV	B,M	6E	MOV	L,M	96	SUB	M	BE	CMP	M	E6	ANI	D8						
1F	RAR		47	MOV	B,A	6F	MOV	L,A	97	SUB	A	BF	CMP	A	E7	RST	4						
20	---		48	MOV	C,B	70	MOV	M,B	98	SBB	B	C0	RNZ		E8	RPE							
21	LXI	H,D16	49	MOV	C,C	71	MOV	M,C	99	SBB	C	C1	POP	B	E9	PCHL							
22	SHLD	Adr	4A	MOV	C,D	72	MOV	M,D	9A	SBB	D	C2	JNZ	Adr	EA	JPE	Adr						
23	INX	H	4B	MOV	C,E	73	MOV	M,E	9B	SBB	E	C3	JMP	Adr	EB	XCHG							
24	INR	H	4C	MOV	C,H	74	MOV	M,H	9C	SBB	H	C4	CNZ	Adr	EC	CPE	Adr						
25	DCR	H	4D	MOV	C,L	75	MOV	M,L	9D	SBB	L	C5	PUSH	B	ED	---							
26	MVI	H,D8	4E	MOV	C,M	76	HLT		9E	SBB	M	C6	ADI	D8	EE	XRI	D8						
27	DAA		4F	MOV	C,A	77	MOV	M,A	9F	SBB	A	C7	RST	0	EF	RST	5						

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

Adr = 16 bit address

HEX-ASCII TABLE

Non-Printing

00	NULL
07	BELL
09	TAB
0A	LF
0B	VT
0C	FORM
0D	CR
11	X-ON
12	TAPE
13	X-OFF
14	
1B	ESC
7D	ALT MODE
7F	RUB OUT

HEX-ASCII TABLE

Printing		Characters	
30	0	40	@
31	1	20	space
32	2	21	!
33	3	22	"
34	4	23	#
35	5	24	$
36	6	25	%
37	7	26	&
38	8	27	'
39	9	28	(
		29	)
41	A	2A	*
42	B	2B	+
43	C	2C	,
44	D	2D	-
45	E	2E	.
46	F	2F	/
47	G	3A	:
48	H	3B	;
49	I	3C	<
4A	J	3D	=
4B	K	3E	>
4C	L	3F	?
4D	M	5B	[
4E	N	5C	\
4F	O	5D	]
50	P	5E	↑ _ (^)
51	Q	5F	← (-)
52	R		
53	S		
54	T		
55	U		
56	V		
57	W		
58	X		
59	Y		
5A	Z		

Processor Technology Corp.

APPENDIX II