7387

FLOPPY-DISK CONTROLLER CARD

PRO-LOG
CORPORATION

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FOREWORD

This manual explains how to use Pro-Log's 7387 Floppy-Disk Controller Card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7387. We welcome your suggestions on how we can improve our instructions.

The 7387 is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of utilizing his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use, microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: Microprocessor User's Guide and the Series 7000 STD BUS Technical Manual. If you would like a copy of these documents, please submit your request on your company letterhead.

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Purpose

The 7387 is suitable for use in small-to-medium sized microprocessor systems requiring disk storage. It is designed for simplicity of hardware, cost effectiveness, and reliability. The 7387 is completely self-contained and fully buffered. It has its own clock, data separator, and interrupt capability. It can be used with most popular floppy disk drives. The card is based on an intelligent controller chip that is thoroughly documented in this manual. This, along with the control software examples provided in this manual make the user's interface task relatively easy.

Features

- **Controls up to four disk drives, either single- or double-sided**
- **Accomodates either 8" or 5-1/4" disk drives**
- **Supports soft-sectored disk format**
- **Supports single-density disk format; requires no DMA**
- **Interrupt via INTRQ*, NMIRQ*, or interrupt controller card**
- **Compatible with 8085, Z80, 6800/09, 8088 and other processors**
- **Uses single +5V power supply**

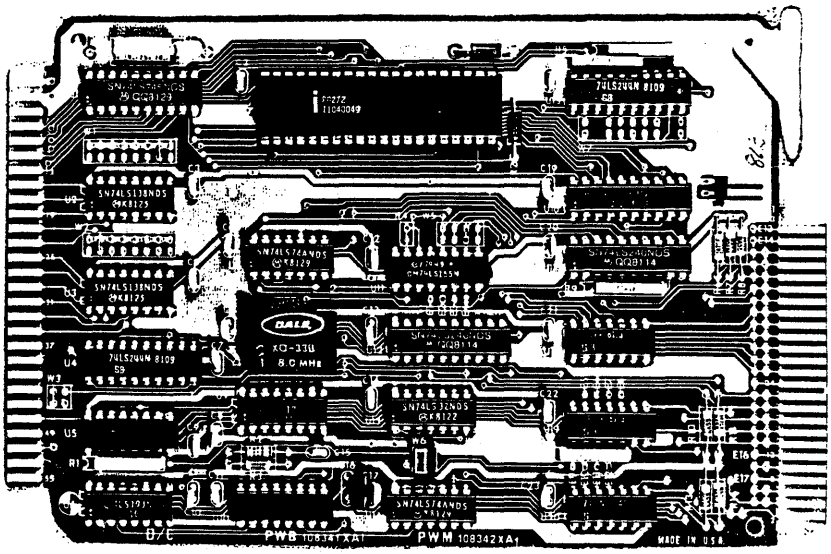
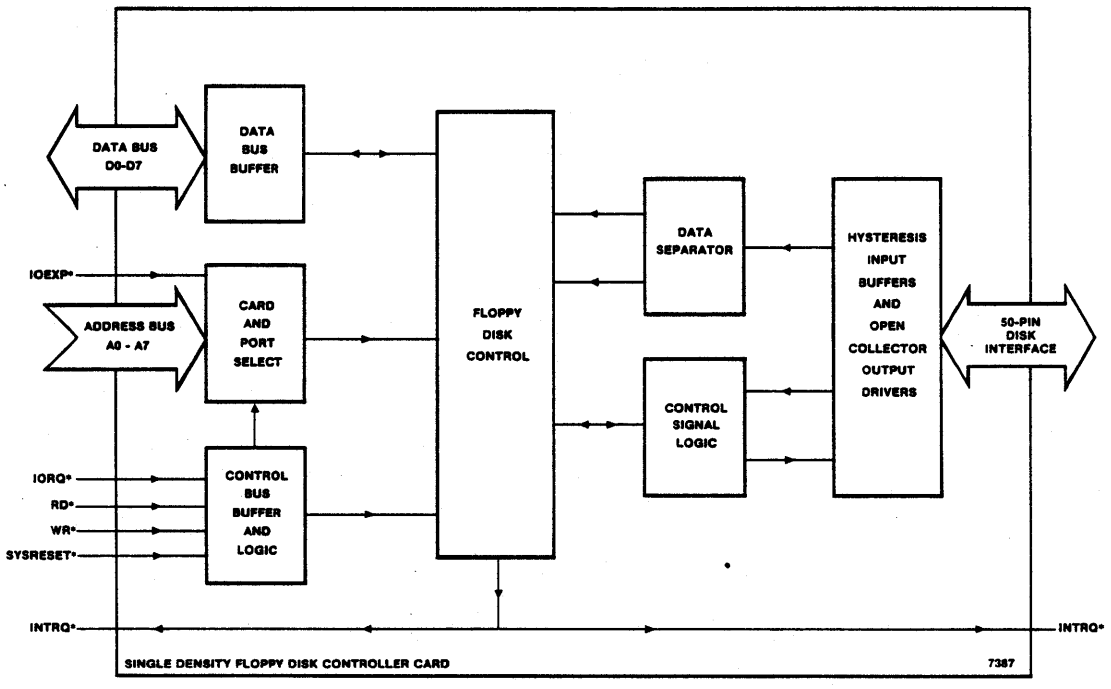


Fig. 1-1, 7387 Floppy Disk Controller Card



* Active low-level logic

Fig. 1-2, 7387 Block Diagram

SECTION 2
Installation and Specifications

Introduction

This section describes the installation and cabling of the 7387 Floppy Disk Controller card. Optional functions which should be considered before the card is installed are also described. At the end of this section are detailed specifications of the card.

Installation

The 7387 operates as part of an STD BUS card rack system. It should be installed with the white card ejector tab at the top as shown in Fig. 2-1. The card normally should be installed directly into the card rack. It can be made accessible for testing by use of an extender card.

The 7387 can generate an interrupt directly to the STD BUS or to a connector on the front of the card for connection to an interrupt controller card. The location of the connector, connector J2, is shown in Fig. 2-4. Its pin-out is given in Fig. 2-18. It consists of two 0.025" square pins, 0.10" apart. Connection should be made with a twisted pair cable, one signal and one ground line. The Pro-Log RC704 cable can be used for this purpose.

The 7387 can be connected via an RC704 cable to a Pro-Log 7320 Priority Interrupt card. This card, or a similar interrupt controller card, may be used in conjunction with the 7387. The 7320 can accept and prioritize up to eight interrupts and provide either restart vectors or the user's own vectors. It can also be used in polled interrupt systems.

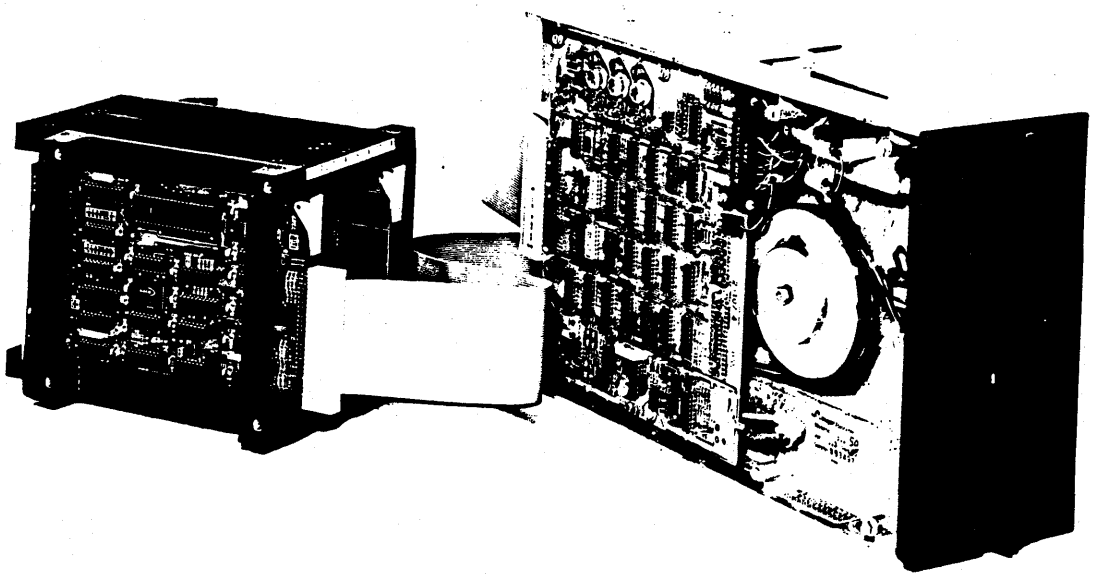


Fig. 2-1, 7387 Installation

Cabling

The 7387 is connected to the floppy disk drives via a 50 conductor cable with card edge type connectors. The cable connections consist of alternating signal and ground lines; the even numbered pins on the component side of the card being signals, and the odd numbered pins on the circuit side of the card being ground.

The connector type used for the 7387 card edge is the same as the type commonly used for connection on the floppy disk drives. The pinout matches the pinout of Shugart or equivalent 8" disk drives. The contacts for the connectors are on 0.1" centers. The cable is connected to multiple disk drives in daisy chain fashion.

The Pro-Log RC50-6 cable can be used to connect the 7387 to one disk drive. See Fig. 2-1. Additional connectors can be added by the user to this cable for additional disk drives. Some sources for these connectors and for cables ready-made for up to four disk drives are shown in Fig. 2-2.

Type of Cable	Manufacturer	Conn. Part #	Contact Part#
Twisted pair, crimp or solder connection	Amp	1-583717-1	583616-5 (crimp) 58354-3 (solder)
Twisted pair, solder connection	Viking	3VH25/1JN-5	-
Flat Cable	Anseley	609-5015M	-
Flat Cable	Winchester	53-50-0	-
Flat Cable	3M	3415-0001	-

Fig. 2-2, 7387 Cabling Sources

Wire Jumpers

The 7387 has several optional functions that are selected by wire jumpers. When removing and replacing these jumpers, cut the jumper in half, and then desolder and remove each half individually. Remaining solder should be removed, and new jumpers installed in the appropriate places. This procedure will prevent damage to circuit traces.

Alternately, permanent 0.025 in. square posts can be installed which can be connected by slip on, slip off connectors. Recommended connectors and headers are listed in Fig. 2-3. Fig. 2-4, shows the location of these jumpers and some of the other features of the 7387.

Part	Manufacturer Part Number	
	Elco Corp.	Berg Electronics
2 Pin Header	00 8261 02 32 00 852	65611-102
4 Pin Header	00 8261 04 32 00 852	65611-104
6 Pin Header	00 8261 06 32 00 852	65611-106
8 Pin Header	00 8261 08 32 00 852	65611-108
Connector	00 8261 02 42 00 870	

Fig. 2-3, 7387 Replacements for Wire Jumpers

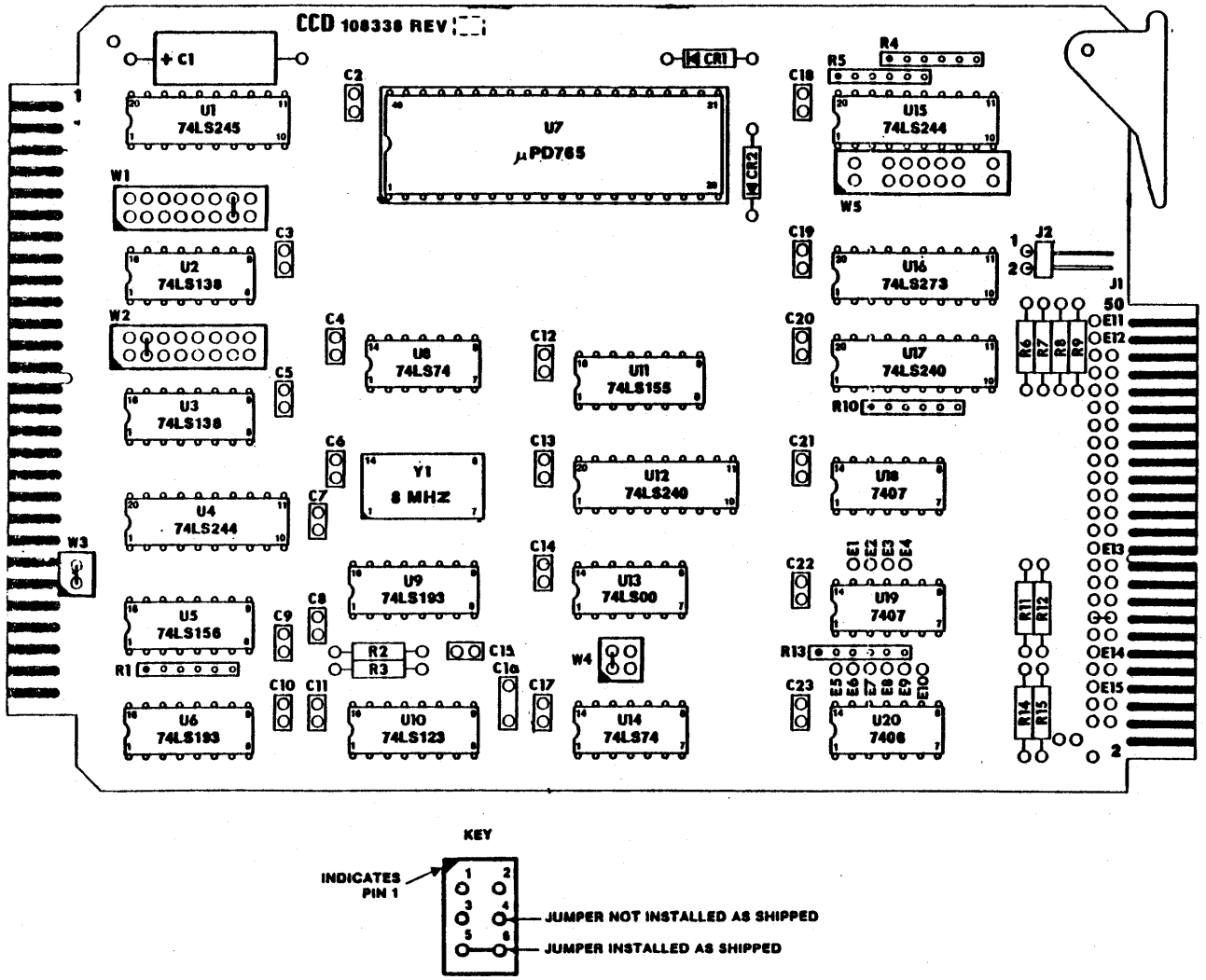


Fig. 2-4, 7387 Physical Locations of Main Features

I/O Port Addressing

The 7387 Card is accessed through I/O ports. As shipped, the card occupies I/O addresses C4 through C7. It can be remapped anywhere within the 256 port I/O address range. The remapping is done with wire jumpers. The physical location of these jumpers is shown in Fig. 2-4. The jumpers are labeled W1 and W2. Figure 2-5 is a table of all the possible combinations of the jumpers and the resulting I/O address mapping.

PORT	JUMPERS
00	W1 1-2
01	
02	W2 1-2
03	
04	W1 1-2
05	
06	W2 3-4
07	
08	W1 1-2
09	
0A	W2 5-6
0B	
0C	W1 1-2
0D	
0E	W2 7-8
0F	
10	W1 1-2
11	
12	W2 9-10
13	
14	W1 1-2
15	
16	W2 11-12
17	
18	W1 1-2
19	
1A	W2 13-14
1B	
1C	W1 1-2
1D	
1E	W2 15-16
1F	
20	W1 3-4
21	
22	W2 1-2
23	
24	W1 3-4
25	
26	W2 3-4
27	
28	W1 3-4
29	
2A	W2 5-6
2B	
2C	W1 3-4
2D	
2E	W2 7-8
2F	
30	W1 3-4
31	
32	W2 9-10
33	
34	W1 3-4
35	
36	W2 11-12
37	
38	W1 3-4
39	
3A	W2 13-14
3B	
3C	W1 3-4
3D	
3E	W2 15-16
3F	

PORT	JUMPERS
40	W1 5-6
41	
42	W2 1-2
43	
44	W1 5-6
45	
46	W2 3-4
47	
48	W1 5-6
49	
4A	W2 5-6
4B	
4C	W1 5-6
4D	
4E	W2 7-8
4F	
50	W1 5-6
51	
52	W2 9-10
53	
54	W1 5-6
55	
56	W2 11-12
57	
58	W1 5-6
59	
5A	W2 13-14
5B	
5C	W1 5-6
5D	
5E	W2 15-16
5F	
60	W1 7-8
61	
62	W2 1-2
63	
64	W1 7-8
65	
66	W2 3-4
67	
68	W1 7-8
69	
6A	W2 5-6
6B	
6C	W1 7-8
6D	
6E	W2 7-8
6F	
70	W1 7-8
71	
72	W2 9-10
73	
74	W1 7-8
75	
76	W2 11-12
77	
78	W1 7-8
79	
7A	W2 13-14
7B	
7C	W1 7-8
7D	
7E	W2 15-16
7F	

PORT	JUMPERS
80	W1 9-10
81	
82	W2 1-2
83	
84	W1 9-10
85	
86	W2 3-4
87	
88	W1 9-10
89	
8A	W2 5-6
8B	
8C	W1 9-10
8D	
8E	W2 7-8
8F	
90	W1 9-10
91	
92	W2 9-10
93	
94	W1 9-10
95	
96	W2 11-12
97	
98	W1 9-10
99	
9A	W2 13-14
9B	
9C	W1 9-10
9D	
9E	W2 15-16
9F	
A0	W1 11-12
A1	
A2	W2 1-2
A3	
A4	W1 11-12
A5	
A6	W2 3-4
A7	
A8	W1 11-12
A9	
AA	W2 5-6
AB	
AC	W1 11-12
AD	
AE	W2 7-8
AF	
B0	W1 11-12
B1	
B2	W2 9-10
B3	
B4	W1 11-12
B5	
B6	W2 11-12
B7	
B8	W1 11-12
B9	
BA	W2 13-14
BB	
BC	W1 11-12
BD	
BE	W2 15-16
BF	

PORT	JUMPERS
C0	W1 13-14
C1	
C2	W2 1-2
C3	
C4	W1 13-14
C5	
C6	W2 3-4
C7	
C8	W1 13-14
C9	
CA	W2 5-6
CB	
CC	W1 13-14
CD	
CE	W2 7-8
CF	
D0	W1 13-14
D1	
D2	W2 9-10
D3	
D4	W1 13-14
D5	
D6	W2 11-12
D7	
D8	W1 13-14
D9	
DA	W2 13-14
DB	
DC	W1 13-14
DD	
DE	W2 15-16
DF	
E0	W1 15-16
E1	
E2	W2 1-2
E3	
E4	W1 15-16
E5	
E6	W2 3-4
E7	
E8	W1 15-16
E9	
EA	W2 5-6
EB	
EC	W1 15-16
ED	
EE	W2 7-8
EF	
F0	W1 15-16
F1	
F2	W2 9-10
F3	
F4	W1 15-16
F5	
F6	W2 11-12
F7	
F8	W1 15-16
F9	
FA	W2 13-14
FB	
FC	W1 15-16
FD	
FE	W2 15-16
FF	

Fig. 2-5, 7387 I/O Port Mapping Options

Interrupt Option

The 7387 can generate an interrupt to either the INTRQ* line on the STD BUS, or to an interrupt controller card, such as Pro-Log's 7320 card, through a connector on the front of the card. The physical location of the connector is shown in Fig. 2-4, and its pinout is given in Fig. 2-18.

If you will be using the interrupt via this connector, you will want to prevent the signal from also occuring on the backplane, since the interrupt controller card will take care of interrupting the processor. To do this, remove the jumper labeled W3. The jumper is shown in Fig. 2-4.

8" or 5.25" Option

The 7387 card can be used to control 8" or 5.25" disk drives. Since the 5.25" disk is smaller, the bits per inch density is greater. To adjust to this, 5.25" disk drives are normally used with a slower data transfer rate in order to reduce data density and thereby increase reliability. The data rate used for 5.25" disks is half that used for 8" disks.

Jumper W4, shown in Fig. 2-4, is used to adapt the data rate for 5.25" or 8" disks. In position 1-2, as shipped, the onboard clock generates an 8 MHz signal. This clock is used by the FDC (Floppy Disk Controller) chip, the write data timer, and the data separator. If this jumper is removed and a jumper is placed at position 3-4, the clock speed is reduced to 4 MHz.

Additional I/O Lines

Several of the interface lines to the disk drive may be used for additional, or customized purposes. You may want software control of the "In Use" indicator LED on the front of the disk drive for instance. Or you may want to input the "Disk Change" signal. Several jumper options on the 7387 allow for just such modifications.

There are 7 output and 7 input port bits of port C6 which are unused. As shipped, each output bit is connected to its corresponding input bit, i.e., output bit 0 to input bit 0. These lines are connected to each other through jumpers W5, 1-2 through 13-14. The locations of these jumpers are shown in Fig. 2-4. Position 1-2 corresponds to data bit 6, position 13-14 corresponds to data bit 0. These jumpers allow you to separate these lines from each other and use them to output to, or input from, the disk drive through port C6.

Outputs to the disk drive are generally required to be open collector. There are several spare open collector drivers on the 7387. The schematic, Fig. 5-1, shows these spare buffers and the labels of the solder pads for connection to them. These labels also appear on the silk screen on the card.

To use one of the output port bits, connect the output line to one of the open collector buffers or inverters, then connect its output to the interface line to the disk drive. Each of the interface lines has either a jumper pad with a cutable trace, or a solder pad, for connection to these lines.

Outputs from the disk drives are generally open collector as well. These lines require pull-up resistors on the controller card. The input port bits accessible at jumper W5 have 1K pull-ups on them.

Software Controlled Stepper Motors

The additional I/O lines described in the previous subsection may be used to give you software control of the stepper motor in each disk drive. This may be desirable in order to reduce the amount of power required of the power supply for the stepper motors.
Normally each disk drive must have its stepper motor engaged at all times. This is because the FDC chip on the 7387 constantly changes the Drive Select lines. It does this in order to scan the status of each drive. This scanning action, however, prevents the stepper motor from having enough time to become fully engaged and perform the step when requested. Hence, there is the need for having it engaged at all times so that it can perform the step as soon as commanded.
You may therefore wish to use the additional I/O lines previously described to have software control of engaging these stepper motors. By this method the processor could engage the stepper motor it wishes to access just prior to requesting the FDC chip to step the motor. Only one motor would need to be engaged at a time, reducing the power required to run these motors by as much as 75%.

Configuring the Disk Drive

Inside your floppy disk drive you will find a number of jumpers. These jumpers are described in the user's manual for your drive. All of these jumpers should be reviewed when you set up your disk system. Here we will discuss the jumper options which you should take into account when using your disk drives with the 7387 card.

Head Load

Your floppy disk drive will probably come configured so that the head will be loaded onto the disk whenever the drives Disk Select line is active. This should be changed so that the head is loaded only when the Disk Select line and the Head Load line are active.

Enabling Stepper Motor

The FDC constantly scans all four possible drives to keep track of their status. It does this by constantly changing the Drive Select lines. Since they are constantly changing, the stepper motor does not have a chance to get fully engaged when a step or seek command is given. Therefore, the stepper motors must be engaged at all times.

Your disk drive will probably come configured so that the stepper motor is engaged whenever the head is loaded. It may also have a jumper for engaging the stepper motor when the drive is selected. Both of these should be checked and configured so that the stepper motor is engaged at all times.

Having several stepper motors engaged at once will demand more power from your stepper motor power supply. Be sure to take this into account when figuring your power and cooling requirements.

Soft Sectoring

Your floppy disk drive may come configured for hard-sectored disks. The 7387 only operates with soft-sectored disks. Check the jumpers in your disk drive that configure it for soft-sectored disks.

Special Considerations for 5-1/4" Disk Drives

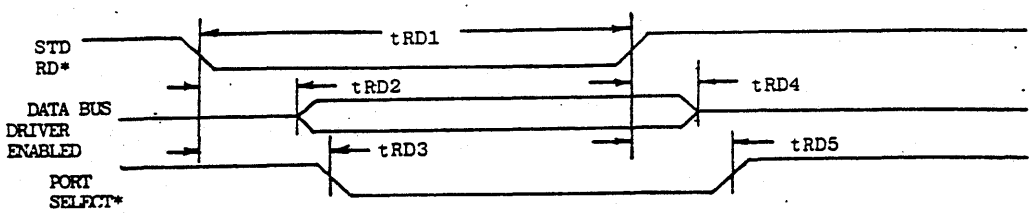
Most 5-1/4" disk drives do not provide either a Two-Sided* line or a Ready* line. The 7387 will not operate if the Ready* line is in the inactive state. For this reason it is necessary to tie the line to ground either on the card or at the disk drive. If your disk drive is two-sided you should also tie this line to ground or the 7387 will not operate on the second side of the disk.

Specifications

Figures 2-6 through 2-20 show timing specifications, electrical and environmental specifications and characteristics, and pinouts of connectors for the 7387.

Mechanical Specifications

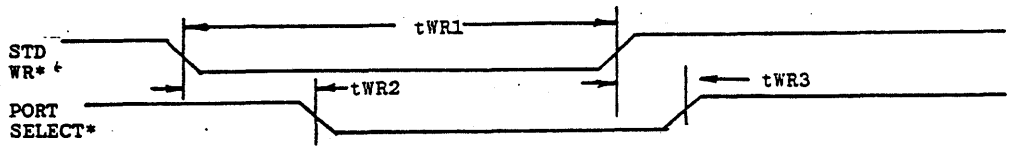
The 7387 card meets all general STD BUS mechanical specifications.



SYMBOL	PARAMETER	NANOSECONDS MIN	TYP	MAX
tRD1	Minimum Read pulse width	255		
tRD2	Read low till Data Bus driver enabled for read		45	65
tRD3	Read low till port selected		55	75
tRD4	Read high till Data Bus driver disabled for Read		35	50
tRD5	Read high till port deselected		45	95

The above parameters are true if all other signals are valid

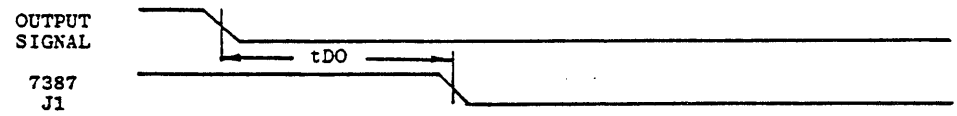
Fig. 2-6, 7387 Read Timing



SYMBOL	PARAMETER	NANOSECONDS MIN	TYP	MAX
tWR1	Minimum Write pulse width	255		
tWR2	Write low till port selected		55	75
tWR3	Write high till port deselected		30	45

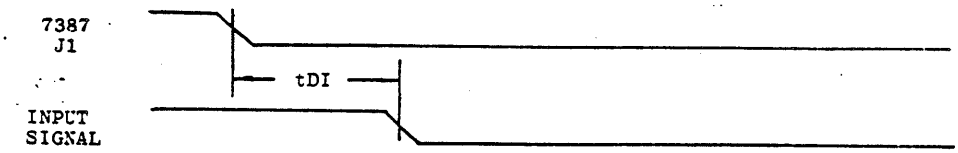
The above parameters are true if all other signals are valid

Fig. 2-7, 7387 Write Timing



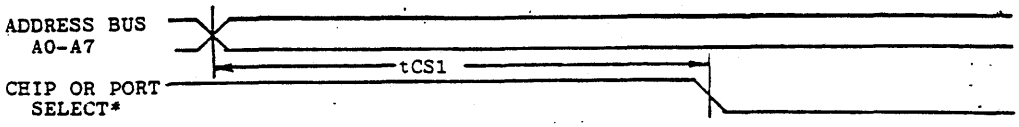
SYMBOL	PARAMETER	NANOSECONDS TYP	MAX
tDO	Disk interface output buffer delay	25	35

Fig. 2-8, 7387 Disk Drive Interface Output Timing



SYMBOL	PARAMETER	NANOSECONDS TYP	MAX
tD1	Disk interface input buffer delay	20	25

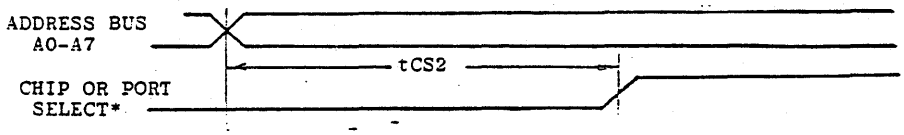
Fig. 2-9, 7387 Disk Drive Interface Input Timing



SYMBOL	PARAMETER	NANOSECONDS TYP	MAX
tCS1	Time address valid till port select low	100	150

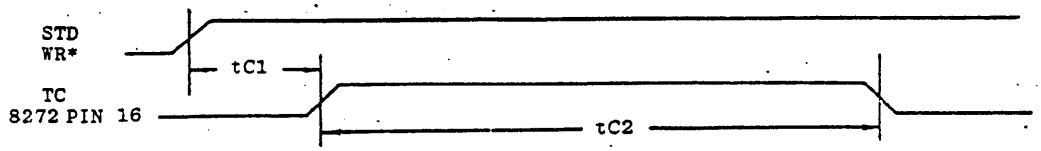
The above parameter is true if all other signals are valid

Fig. 2-10, 7387 Port Select Address Timing



SYMBOL	PARAMETER	NANOSECONDS TYP	MAX
tCS2	Time address invalid till port Select* high	80	145

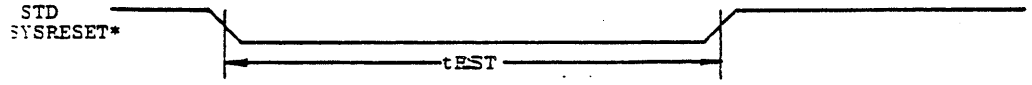
Fig. 2-11, 7387 Port Deselect Address Timing



SYMBOL	PARAMETER	NANOSECONDS TYP	MAX
tC1	Time WR* high till Terminal Count high	55	115
tC2	Terminal Count pulse width	405	455

The above parameters are true if all other signals are valid

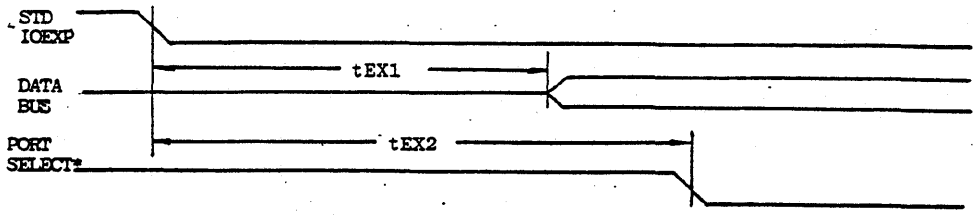
Fig. 2-12, 7387 Terminal Count Timing



SYMBOL	PARAMETER	NANOSECONDS MIN	TYP
tRST	Minimum reset pulse width for 8-inch floppy disk drive	2000	
tRST	Minimum reset pulse width for 5-1/4 Floppy disk drive	4000	

The above parameters are true if all other signals are valid

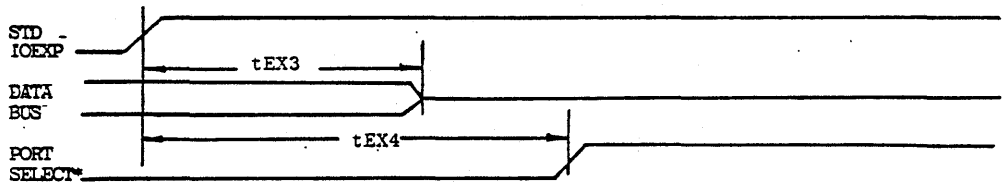
Fig. 2-13, 7387 Reset Timing



SYMBOL	PARAMETER	NANOSECONDS TYP	MAX
tEX1	Time IOEXP Low till Data Bus Driver Enabled	85	125
tEX2	Time IOEXP Low till Port Select* low	100	150

The above parameters are true if all other signals are valid

Fig. 2-14, 7387 IOEXP Enable Timing



SYMBOL	PARAMETER	NANOSECONDS TYP	MAX
tEX3	Time IOEXP high till Data Bus disabled	55	85
tEX4	Time IOEXP high till ports deselected	75	145

The above parameters are true if all other signals are valid

Fig. 2-15, 7387 IOEXP Disable Timing

		RECOMMENDED OPERATING LIMITS			ABSOLUTE NON-OPERATING LIMITS		
MNEM.	PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
V_{CC}	Supply Voltage	4.75	5.00	5.25	0	5.50	Volts
—	Free Air Temperature	0	+25	+55	-40	+75	°C
—	Humidity	5		95(1)	0	95(1)	%RM

(1) Non condensing

Fig. 2-16, 7387 Electrical and Environmental Specifications

MNEM.	PARAMETER	MIN	TYP	MAX	UNITS
I_{CC}	V_{CC} Supply Current		752	1157.7	Milliamps

Fig. 2-17, 7387 Electrical Characteristics Over Recommended Operating Range

PIN NUMBER			PIN NUMBER		
OUTPUT			OUTPUT (LSTTL DRIVE)		
MNEMONIC					MNEMONIC
GROUND	GND	1	2	55	INTRQ* #

* Designates low level logic
# Designates open collector drive

Fig. 2-18, 7387 J2 Interrupt Output Connector Pin List

PIN NUMBER			PIN NUMBER			
OUTPUT			OUTPUT 40mA Pull Down			
INPUT			INPUT 150 Ω Pullups			
MNEMONIC						MNEMONIC
GROUND	GND		1	2	.	LOW CURRENT*
	"		3	4	.	FAULT RESET*
	"		5	6	.	FAULT*
	"		7	8		ALT I/O
	"		9	10	.	TWO SIDED*
	"		11	12		DISK CHNG*
	"		13	14	.	SIDE SELECT
	"		15	16	1	TEST
	"		17	18	.	HEAD LOAD*
	"		19	20	.	INDEX*
	"		21	22	.	READY*
	"		23	24		HARD SECTOR*
	"		25	26	.	DRIVE SELECT 1*
	"		27	28	.	DRIVE SELECT 2*
	"		29	30	.	DRIVE SELECT 3*
	"		31	32	.	DRIVE SELECT 4*
	"		33	34	.	DIRECTION*
	"		35	36	.	STEP*
	"		37	38	.	WRITE DATA*
	"		39	40	.	WRITE GATE*
	"		41	42	.	TRACK 00*
	"		43	44	.	WRITE PROTECT*
	"		45	46	.	READ DATA*
	"		47	48		SEP DATA*
	"		49	50		SEP CLOCK*

* Designates Active Low Level Logic
1 4 MHz LSTTL output for testing only
All outputs are open collector
All inputs pulled up with 150 Ω resistors

Fig. 2-19, 7387 J1 Disk Drive Interface Connector Pin List

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)				OUTPUT (LSTTL DRIVE)			
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5 VOLTS	IN		2	1		IN	+5 VOLTS
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31		2	WR*
MEMRQ			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*#		55	44	43			INTAK*
NMIRQ*#		55	46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Designates Active Low Level Logic
# Designates Open Collector Driver

Fig. 2-20, STD/7387 Interface Connector Pin List

SECTION 3
OPERATION AND PROGRAMMING

Introduction

This section deals with the interfacing between the 7387 and the processor. It includes a description of the floppy disk controller chip, the commands it uses, and the I/O ports used by the 7387.

Floppy Disk Controller

The Floppy Disk Controller chip, or FDC, simplifies interfacing to a floppy disk drive. It manipulates the control lines and takes care of timing requirements for reading from and writing to the disk drive.

There are 15 fixed commands to which the FDC responds. The commands are delivered to the FDC by writing to one of the output ports associated with it. The FDC performs the function and responds by making available to the processor status information about the floppy disk drive and the FDC itself. Data also is written to and read from the FDC through I/O ports.

Figure 3-1 gives the pinout of the FDC chip. A review of this may aid in understanding the functions of the chip.

Pin No.	Symbol	Name	Input/ Output	Connection to	FUNCTION
1	RST	Reset	Input	Processor	Places FDC chip in idle state. Resets the output lines to the disk drive to a logic 0. The Step Rate Time and Head Load and Unload Times are not affected. If the RDY (disk drive ready) pin is high during reset the FDC chip will generate an interrupt 1 to 25ms later. The interrupt can be cleared by using the Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input	Processor	Data is transfered from the FDC chip to the data bus when the Read line is low.
3	$\overline{WR}$	Write	Input	Processor	Data is transfered from the data bus to the FDC chip when the Write line is low.
4	$\overline{CS}$	Chip Select	Input	Processor	Transfer of data to and from the data bus is enabled when Chip Select is low.
5	A0	Data/Status Register Select	Input	Processor	Connects to address line A0. Selects the Data Register for data transfer when high, Status Register when low.
6-13	DB0-DB7	Data Bus	Input/ Output	Processor	Bi-Directional eight bit data bus. All transfer of commands, status, and data take place on this bus.
14	DRQ	Data DMA Request	Output	Processor or DMA Controller	Equivelant to BUSRQ* line on STD BUS. Indicates the FDC chip wishes to transfer data in the DMA mode. Not used on the 7387.
15	$\overline{DACK}$	DMA Acknowledge	Input	Processor or DMA Controller	Equivelant to BUSAK* on the STD BUS. Indicates the bus is free for data transfer in the DMA mode. Not used on the 7387.
16	TC	Terminal Count	Input	Processor or DMA Controller	Read, Write, and Scan commands can be terminated with this line. The FDC chip immediately goes into the Result phase. Convenient for stopping the FDC from reading or writting after you have read or written all the data you intended to.
17	IDX	Index	Input	Disk Drive	The disk drive strobes this line whenever the index hole in the disk passes the index hole sensor in the disk drive. This indicates to the FDC chip that the head is positioned over the beggining of Track 0.
18	INT	Interrupt	Output	Processor	Interrupt signal to processor.
19	CLK	Clock	Input	Clock Circuit	Clock input, single phase TTL. 8MHz for 8" disks, 4MHz for 5.25" disks.
20	GND	Ground	Output	D.C. Return	D.C. power return.

Pin No.	Symbol	Name	Input, Output	Connection to	FUNCTION
21	WCK	Write Clock	Input	Clock Circuit	Provides timing for data written to the disk. The 7387 provides a 500KHz signal to this pin with a pulse with of 250ns. This is standard for single density recording.
22	RDW	Read Data Window	Input	Data Separator	This signal is generated by the data separation logic and indicates to the FDC chip the period during which a data pulse may occur.
23	RDD	Read Data	Input	Disk Drive	This signal comes from the data read from the disk and includes both clock and data pulses. If a data pulse occurs during the period of the Read Data Window the FDC chip interprets it as a logic one. If no data pulse occurs during this period it is interpretedas a logic 0.
24	VCO	VCO Sync	Output	Data Separator	Enables the VCO in a phase locked loop based data separator. Usually used for double density data seperation. Not used on the 7387.
25	WE	Write Enable	Output	Disk Drive	Enables the write logic in the disk drive when in the low state.
26	MFM	MFM Mode	Output	Data Separator	Selects single or double density data separation in a phase locked loop based data separator. Not used on the 7387.
27	HD	Head Select	Output	Disk Drive	Indicates to the disk drive which head is to be accessed on double sided disk drives. First side selected when 0, second side selected when 1.
28	US0	Unit Select	Output	Drive Select Decoder Circuit	A two bit address used to select the drive to be accessed. The 7387 decodes these bits and outputs four individual select lines to the disk drives.
29	US1				
30	WDA	Write Data	Output	Disk Drive	Data to be written on the disk is sent to the disk drive via this line. The data on this line includes data and clock pulses and is of the proper data rate and pulse width to be written directly on the disk.
31	PS1	Precompensation	Output	Disk Drive	These lines are used in the double density mode to ensure the proper timing of data being written on the disk. Not used on the 7387.
32	PS0				
33	FLT/TR0	Fault/Track 0	Input	Disk Drive	A multiplexed line, the 7387 performs the demultiplexing. The disk drive can indicate an error condition to the FDC chip in the read and write modes on the Fault line. The disk drive indicates to the FDC chip wether the read/write head is over track 0 by the Track 0 line.
34	WP/TS	Write Protect/ Two-Sided	Input	Disk Drive	A multiplexed line, the 7387 performs the demultiplexing. The Write Protect line indicates to the FDC chip wether the write protect notch in the disk sleeve is covered. The Two-Sided line indicates to the FDC chip wether a single sided or double sided disk is installed.
35	RDY	Ready	Input	Disk Drive	Indicates to the FDC chip that the disk drive is ready to read or write. Ready conditions include, disk installed, door closed, disk rotation up to speed, and the index hole has been encountered twice since the drive was selected.
36	HDL	Head Load	Output	Disk Drive	Causes the read/wrire head to be loaded onto the disk. The head is only loaded on the drive that is presently selected, and only during the course of a read or write operation.
37	FR/STP	Fault Reset/ Step	Output	Disk Drive	A multiplexed line, the 7387 performs the demultiplexing. The Fault Reset line reset the fault line out of the disk drive. The Step line supplies step pulses to the stepper motor in Seek or Recalibrate modes.
38	LCT/DIR	Low Current/ Direction	Output	Disk Drive	A multiplexed line, the 7387 performs the demultiplexing. The Low Current line decreases the write current to the recording head on the inner tracks to compensate for the increased bit density on the inner tracks. The Direction line indicates to the disk drive in which direction to move the stepper motor in Seek or Recalibrate modes.
39	$\overline{RW}$/SEEK	Read Write/ Seek	Output	Demultiplexer	This line does not connect to the disk drive, it is used on the 7387 for control of the demultiplexeing of the multiplexed lines. Indicates a Read/Write command when in the logic one state, and a Seek or Recalibrate command in the logic 0 state.
40	Vcc	+5	Input	+5v Supply	+5V supply

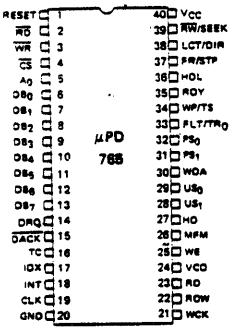


Fig. 3-1, Pinout of the 7387 FDC Chip

I/O Ports

The 7387 occupies eight I/O ports, four input ports and four output ports. One input port and one output port are unused. Three ports are integral functions of the FDC chip, the other three are extra functions of the 7387 card. Fig. 3-2 is a table of the ports.
The ports internal to the FDC chip are the Main Status Register port, the Read Data port, and the Write Data port. The three ports that the 7387 provide are the Interrupt Status port, the Interrupt Mask port, and the Terminate port.

Port Name	Standard Port Address	Input Output	Description
Main Status Port	C4	Input	Accesses Main Status Register in FDC chip.
Terminate Port	C4	Output	Output to this port causes the Terminal Count pin on the FDC chip to be strobed. Data written out is inconsequential, just the act of writing out to this port generates a 400ns. pulse to the pin.
Read Data Port	C5	Input	During read operations, this port is used to read data out of the FDC. During the Result Phase of a command, this port is used to read the Result bytes out of the FDC.
Write Data Port	C5	Output	During the Command Phase of a command, this port is used to write the Command bytes to the FDC. During write operations, this port is used to write data to the FDC.
Interrupt Status	C6	Input	Bit 7 of this port is used to read the interrupt output of the FDC chip. When the bit is set to 1, the interrupt is active. The other bits are spares.
Interrupt Mask Port	C6	Output	Bit 7 of this port is used to control the interrupt mask. The interrupt is masked after power-up or reset. To Enable the interrupt, set the bit to a one. The mask does not affect the Interrupt Status port's ability to monitor the interrupt output pin of the FDC. The other bits are spares.
	C7	Input	Invalid
	C7	Output	Invalid

Fig. 3-2 7387 Table of I/O Ports

Main Status Register Port

The sole purpose of the Main Status Register Port is to read the Main Status Register. It is available to be read at anytime and contains eight flags indicating the present state of the FDC. These flags are shown in Fig. 3-4.

Terminate Port

The Terminate port is used to prematurely stop any function that the FDC may be carrying out. The data you write out to this port is inconsequential. Just the act of writing to this port causes a 400ns. pulse to be applied to the Terminal Count pin of the FDC chip.

Read Data Port

The Read Data Port is used to retrieve status information at the end of a command, and to read data that is being transfered during a command.

Write Data Port

The Write Data Port is used to write the commands and their associated parameters to the FDC at the begining of a command, and to write data to the FDC during a command.

Interrupt Status Port

The Interrupt status port serves two functions. First, it can be read to determine if the FDC chip is generating an interrupt. The most significant bit of the port is used for this purpose. The other bits of this port can also be used for inputing optional signals from the floppy disk drive. These optional signals are described in Section 2 under the "Additional I/O Lines" heading.

Interrupt Mask Port

The Interrupt Mask port also serves two functions. The most significant bit is used as an interrupt mask. When this bit is low, the interrupt is disabled. Therefore, the interrupt is disabled at power up or reset. This bit must be set for the interrupt to be enabled. This interrupt mask bit does not prevent the FDC chip from generating an interrupt, it merely prevents the interrupt from appearing on either the STD BUS backplane, or on the interrupt connector J2 on the front of the card. Whether the mask bit is set or not, the Interrupt Status port can still be read to determine if the FDC chip is generating an interrupt.
The second use of this port is to output optional signals to the floppy disk drive. These optional signals are described in Section 2 under the "Additional I/O Lines" heading.

Command Format

All interfacing to the FDC is done by way of its 15 commands. The commands have three phases to them. What follows is a description of those phases.

Command Phase

The command consists of several bytes that must be written out to the FDC. The first byte is the command itself. It is followed by several bytes of additional data such as the track to be accessed, the sector to be accessed, etc.

Execution Phase

After all the bytes associated with the command have been written out, the FDC will perform the function requested of it. If the commands require data to be transfered, i.e. read or write commands, the data will be transfered during this phase. For other commands, the processor does not need to have any interaction with the FDC during this phase.

Result Phase

At the end of most commands, the FDC makes available to the processor a series of bytes containing detailed information about the status of the floppy disk drive and the FDC . You may want the processor to examine all of this information, or more likely, you will only want the processor to examine a few essential status bits. In either case, you must extract all of the result bytes before the FDC chip will accept the next command.

Instruction Set

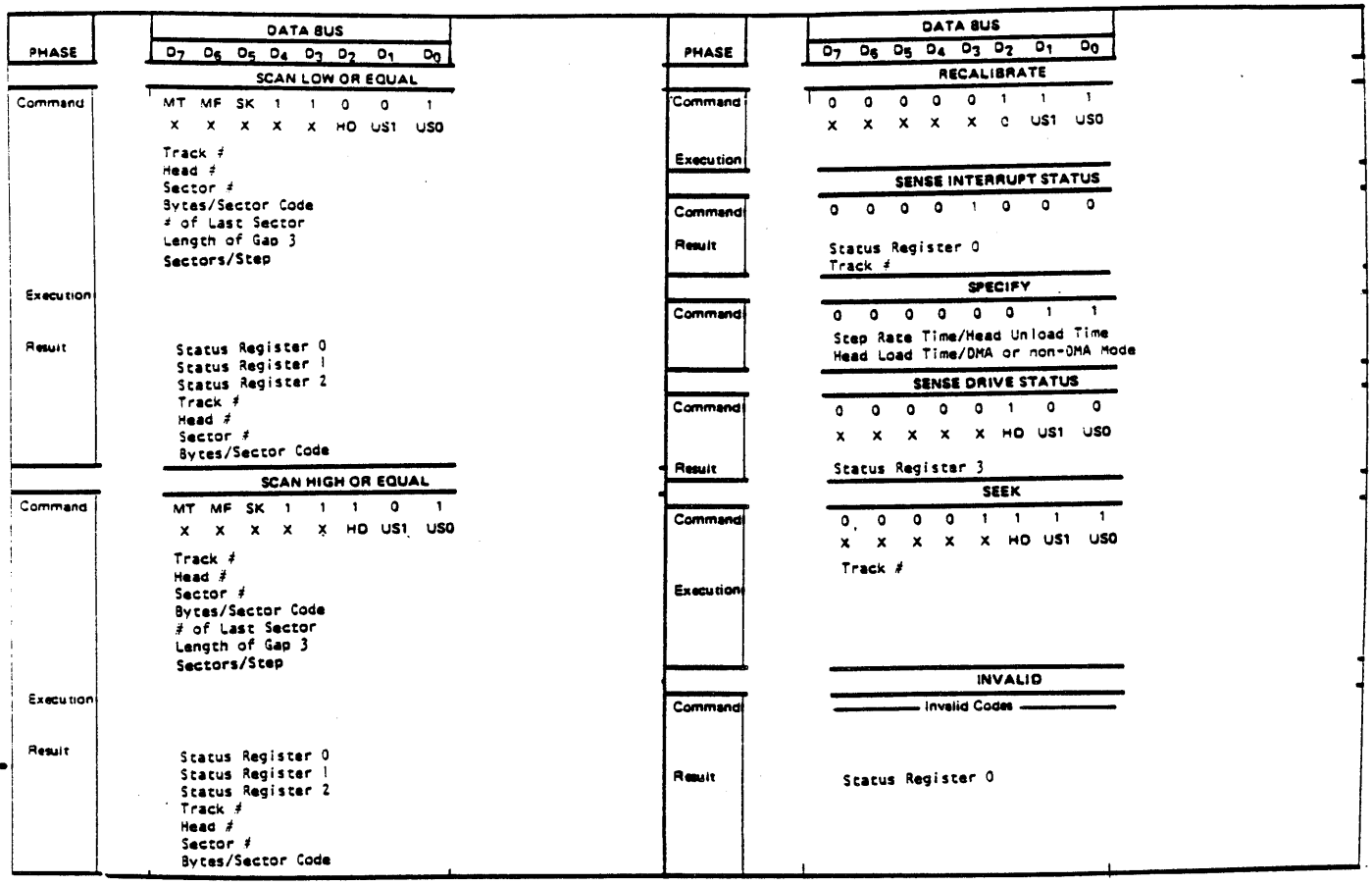
Each command has a particular number of bytes and set of parameters that must be sent to the FDC. Likewise, each command has a particular number of bytes of status information which must be read back from the FDC. Figure 3-3 shows what must be written to and read from the FDC for each command.

The status registers in the Result Phase should not be confused with the Main Status Register. These status registers are only available as part of the Result Phase and are read out of the Read Data Port, not the Main Status Port.

Figures 3-5 through 3-11 are descriptions of the bytes in the Command and Result Phases and of the status registers.

PHASE	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
READ DATA	
Command	MT MF SK 0 0 1 1 0
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
READ DELETED DATA	
Command	MT MF SK 0 1 1 0 0
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
WRITE DATA	
Command	MT MF 0 0 0 1 0 1
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
WRITE DELETED DATA	
Command	MT MF 0 0 1 0 0 1
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code

PHASE	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
READ A TRACK	
Command	0 MF SK 0 0 0 1 0
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
READ ID	
Command	0 MF 0 0 1 0 1 0
	X X X X X HD US1 US0
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
FORMAT A TRACK	
Command	0 MF 0 0 1 1 0 1
	X X X X X HD US1 US0
	Bytes/Sector Code
	Sectors/Track
	Length of Gap 3
	Filler Data Byte
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
SCAN EQUAL	
Command	MT MF SK 1 0 0 0 1
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	Sectors/Step
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code



PHASE	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
SCAN LOW OR EQUAL	
Command	MT MF SK 1 1 0 0 1
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	Sectors/Step
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
SCAN HIGH OR EQUAL	
Command	MT MF SK 1 1 1 0 1
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	Sectors/Step
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code

PHASE	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
RECALIBRATE	
Command	0 0 0 0 0 1 1 1
	X X X X X 0 US1 US0
Execution	
SENSE INTERRUPT STATUS	
Command	0 0 0 0 1 0 0 0
Result	Status Register 0
	Track #
SPECIFY	
Command	0 0 0 0 0 0 1 1
	Step Rate Time/Head Unload Time
	Head Load Time/DMA or non-DMA Mode
SENSE DRIVE STATUS	
Command	0 0 0 0 0 1 0 0
	X X X X X HD US1 US0
Result	Status Register 3
SEEK	
Command	0 0 0 0 1 1 1 1
	X X X X X HD US1 US0
	Track #
Execution	
INVALID	
Command	Invalid Codes
Result	Status Register 0

Fig. 3-3. 7387 FDC Instruction Set

Bit	Name	Description
0	FDD 0 BUSY	Bit set means Disk Drive 0 is in the Seek mode. The FDC cannot accept a Read or Write Command while this bit is set.
1	FDD 1 BUSY	Bit set means Disk Drive 1 is in the Seek mode. The FDC cannot accept a Read or Write Command while this bit is set.
2	FDD 2 BUSY	Bit set means Disk Drive 2 is in the Seek mode. The FDC cannot accept a Read or Write Command while this bit is set.
3	FDD 3 BUSY	Bit set means Disk Drive 2 is in the Seek mode. The FDC cannot accept a Read or Write Command while this bit is set.
4	FDC BUSY	Bit set means a Read or Write command is in process. FDC cannot accept any other command.
5	EXECUTION MODE	Bit set means FDC is in the Execution Phase of a command.
6	DATA INPUT/ OUTPUT	Bit set means data transfer should be from Read Data Port to processor. Bit reset means data transfer should be from processor to Write Data Port.
7	REQUEST FOR MASTER	Indicates the FDC is ready for a data transfer between the Read or Write Data Ports and the processor.

Fig. 3-4, 7387 Main Status Register

NAME	DESCRIPTION
MT	If MT is set, a double-sided operation is to be performed. After finishing a Read or Write operation on Side 0, the FDC will automatically start searching for Sector 1 on Side 1.
MF	Selects FM or MFM mode. On 7387 it should always be reset, indicating FM mode.
SK	If SK is set, sectors with Deleted Data Address Masks will be skipped, otherwise the command will terminate.
HD	If reset selects side 0. If set selects side 1.
US1, US0	A two bit binary number indicating the drive to be selected.
TRACK #	Binary number of track to be accessed. Must match the track number in the ID field of the sector to be accessed. As a Result byte, it may be incremented from the number given in the command. For the Read ID command, it is the track number read from the ID field of the first sector encountered.
HEAD #	Number of side to be accessed, 0 or 1. Must match head number in ID field of the sector to be accessed. As a Result byte, its least significant bit may be complemented from the number in the command.
SECTOR #	Number of sector to be accessed. Must match sector number in ID field of sector to be accessed. As a Result byte, it reflects the FDC internal sector counter. For the Read ID command, it is the sector number read from the ID field of the first sector encountered.

Fig. 3-5, 7387 Command and Result Bytes (1)

BYTES/ SECTOR CODE	Code indicating the number of bytes per sector. Must match Bytes/Sector Code in ID field of sector to be accessed. However, if you will not be reading all the data from the sector the Bytes/Sector Code should be 00 The last command byte, "# of Data Bytes to be Transferred," then defines the number of bytes transferred. Refer to Fig. 3-12 for the proper code.
# OF LAST SECTOR	The command will end after the sector with this number has been operated on. The number is a binary number. If you are performing a double-sided operation, the sectors operated on will start with the starting sector you specify, read through the sector on side 0 that equals the # of Last Sector, then start reading side 1 at sector 1, and finish when it reads the sector on side 1 equal to the # of Last Sector.
LENGTH OF GAP 3	A binary number specifying the length of Gap 3, which in the IBM 3740 format, is the gap between the end of one sector and the beginning of the next. See Fig. 3-12.
FILLER DATA BYTE	When formatting a track, the entire data field of each sector will be filled with this data byte.
SECTOR/ STEP	During Scan commands, if this byte = 0 consecutive sectors are scanned. If = 1 every other sector is scanned. Scan commands should only be used on one sector per command, so this byte has no real meaning. It is suggested it be set = 0.
SECTOR/ TRACK	A binary number specifying the number of sectors to be placed on a track during the Format a Track command.
STEP RATE TIME	The most significant 4 bits of this byte specify the time delay between step pulses issued to the stepper motor during Seek or Recalibrate commands. The time may vary from 1 to 16ms. in 1ms. increments. F=1ms., 0=16ms.

Fig. 3-6, 7387 Command and Result Bytes (2)

HEAD UNLOAD TIME	The least significant 4 bits of this byte specify the length of time the head will remain loaded on the disk after the Execution Phase of an operation has been completed. The time may vary from 16 to 240ms. in 16ms. increments. 1=16ms., F=240ms.
HEAD LOAD TIME	The most significant 7 bits of this byte specify the head settling time. This is the time between the head load signal being issued and the FDC beginning the operation. The time may vary from 2 to 254ms. in 2ms. increments. 01=2ms., 7F=254ms.
DMA OR NON-DMA MODE	The least significant bit of the byte selects the DMA or Non-DMA mode of operation. On the 7387 this bit should always be set to a 1, indicating the Non-DMA mode.

Fig. 3-7, 7387 Command and Result Bytes (3)

BIT	NAME	DESCRIPTION
7 AND 6	INTERRUPT CODE	7=0, 6=0 Command was completed without error.
		7=0, 6=1 Command terminated early because of some error.
		7=1, 6=0 Invalid command was issued.
		7=1, 6=1 Command terminated early because the Ready line from the disk drive changed state.
5	SEEK END	When set, this flag indicates a Seek command has been completed.
4	EQUIPMENT CHECK	When set, this flag indicates a Fault signal was received from the disk drive, or no Track 0 signal was received from the disk drive after 77 step pulses had been issued during a Recalibrate command.
3	NOT READY	When set, this flag indicates a command was issued to a disk drive whose Ready line is inactive, or a command was issued to operate on the second side of a single-sided disk.
2	HEAD	This flag indicates whether side 0 or side 1 was selected when the command terminated or an interrupt occurred.
1 AND 0	DRIVE	A two bit binary number indicating the disk drive that the other status flags pertain to.

Fig. 3-8, 7387 Status Register 0

BIT	NAME	DESCRIPTION
7	LAST SECTOR ERROR	During Scan commands, if the FDC is scanning every other sector and it skips over the sector equal to the "# of Last Sector" this flag will be set. Scan commands should only be used on one sector per command, so this bit has no real significance.
6		Not used, this bit is always 0.
5	CRC ERROR	When a CRC error is detected in either the ID Field or the Data Field, this flag is set.
4	OVER RUN	If the processor does not perform a data transfer in time during the Execution Phase of a command, this flag is set.
3		Not used, this bit is always 0.
2	SECTOR NOT FOUND	If the FDC cannot find a sector it is looking for after it has encountered the index hole twice, it sets this flag. For the Read a Track command: If during the course of the command the specified sector was not found, this flag will be set. For the Read ID command: If the FDC cannot read an ID Field without an error, it sets this flag.
1	NOT WRITEABLE	Any time you request data to be written on the disk and the disk is write-protected, this flag is set.
0	MISSING ADDRESS MARK	If the FDC cannot find an ID Address Mark after encountering the index hole twice, or if it cannot find a Data Address Mark or Deleted Data Address Mark for the sector it is trying to operate on, this flag is set.

Fig. 3-9, 7387 Status Register 1

BIT	NAME	DESCRIPTION
7		Not used, this bit is always 0.
6	CONTROL MARK	If a Deleted Data Address Mark is encountered during the Read Data command or during a Scan command, this flag is set. If a Data Address mark is encountered during the Read Deleted Data command, this flag is set.
5	DATA CRC ERROR	If a CRC error is detected in the data field, this flag is set.
4	WRONG TRACK	If the track number read from the ID Field does not agree with the FDC's internal track counter, this flag is set.
3	SCAN HIT	During Scan commands, if the scan was successful, this flag is set.
2	SCAN MISS	During Scan commands, if the scan was not successful, this flag is set.
1	BAD TRACK	If the track number read from the ID Field is FF Hex, this flag is set. In the IBM format, tracks with hard errors are labeled with a track number FF Hex.
0	MISSING DATA FIELD ADDRESS MARK	If the FDC cannot find the Data Address Mark or Deleted Data Address Mark, this flag is set.

Fig. 3-10, 7387 Status Register 2

BIT	NAME	DESCRIPTION
7	FAULT	Indicates the status of the Fault line from the disk drive.
6	WRITE PROTECTED	Indicates the status of the Write-Protected line from the disk drive.
5	READY	Indicates the status of the Ready line from the disk drive.
4	TRACK 0	Indicates the status of the Track 0 line from the disk drive.
3	TWO SIDED	Indicates the status of the Two-Sided line from the disk drive.
2	SIDE SELECT	Indicates the status of the Side-Select line to the disk drive.
1 AND 0	UNIT SELECT	Indicates the status of the Unit Select 1 and Unit Select 0 lines to the disk drive. These should match the drive number specified when the Sense Drive Status command was issued.

Fig. 3-11, 7387 Status Register 3

BYTES/ SECTOR	BYTES/ SECTOR CODE	SECTORS/ TRACK	LENGTH[1] OF GAP 3 R/W	LENGTH[2] OF GAP 3 FORMAT
		8" DISKS		
128	00	26	07	1B
256	01	15	OE	2A
512	02	8	1B	3A
1024	03	4	47	8A
2048	04	2	C8	FF
4096	05	1	C8	FF
		5-1/4" DISKS		
128	00	18	07	09
128	00	16	10	19
256	01	8	18	30
512	02	4	46	87
1024	03	2	C8	FF
2048	04	1	C8	FF

(1) Suggested Hex values for Gap Length 3 for commands other than Format.

(2) Suggested Hex values for Gap Length 3 for Format command.

Fig. 3-12, 7387 Bytes/Sector Code & Gap Length 3 Values

FDC Commands

Figures 3-13 and 3-14 give a brief description of the FDC commands.

Command	Description
Specify	Provides the FDC chip with several variables which remain fixed thereafter. Variables are: Head Load Time, Head Unload Time, Step Rate Time, DMA/NON-DMA Mode.
Recalibrate	Resets the FDC chip's internal track counter and sets the read/write head over Track 0 of the disk.
Sense Interrupt Status	When an interrupt occurs, this command can be used to extract status information from the FDC as to why the interrupt occurred and what, if any, problems there are.
Sense Drive Status	This command can be used to extract status information from the FDC about the disk drive, i.e., is the drive ready, is it on Track 0, etc.
Seek	Moves the read/write head to a different track.
Read Data	Causes data from the data field of a sector to be read from the disk. Depending on certain variables issued with the command, you can read one sector, or several sectors, or a whole track, or a track from both sides 0 and 1.
Write Data	Similar to Read Data but data is written onto the disk. Data is automatically configured in the IBM 3740 single-density, soft-sectored format.

Fig. 3-13, 7387 Command Descriptions (1)

Command	Description
Read Deleted Data	Reads only sectors preceded by a Deleted Data Address mark. Otherwise, the same as Read Data.
Write Deleted Data	This command is the same as Write Data except that a Deleted Data Address mark is written in place of a Data Address mark. It is used to mark faulty sectors on the disk.
Format a Track	Writes the ID fields, sector numbers, gaps, etc. on a track.
Read a Track	Similar to Read Data but reads the sectors on a track consecutively, starting with the first sector after the index mark.
Read ID	Reads the first ID field encountered. The processor is given the track number, sector number, head number, and bytes per sector code.
Scan Equal	Compares data from a sector on the disk with data supplied by the processor and sets a flag in a status register if it compared.
Scan Low or Equal	Same as Scan Equal but looks for data numerically equal to or less than data supplied by the processor.
Scan High or Equal	Same as Scan Equal but looks for data numerically equal to or greater than data supplied by the processor.

Fig. 3-14, 7387 Command Descriptions (2)

FDC Command Descriptions

What follows is a detailed description of the FDC commands.

Specify

The Specify command is used to set several variables in the FDC chip. These variables are:

Head Load Time:
The Read/Write head is loaded onto the disk during Read or Write commands. The head must be given a certain amount of time to load and settle before reading or writing can begin. The Specify command sets the amount of time allowed for this.

Head Unload Time:
After a Read or Write function, the head remains loaded on the disk for preset amount of time. The Specify command sets this amount of time. The idea is, if the head is still loaded from the last Read or Write when you issue a new command to Read or Write, the FDC does not have to wait for the head to settle before it can begin the new command.

Step Rate Time:
This is the amount of time between step pulses to the stepper motor. The stepper motor is used to move the read/write head from one track to another.

Recalibrate

The FDC chip has an internal counter that holds the track number the head is currently positioned over. This counter is cleared to 0. Also, the head is stepped outward towards the edge of the disk until the Track 0 signal from the disk drive goes active. If the FDC does not get a Track 0 signal after 77 steps, it sets an error flag and terminates the command.

With most commands, only one command can be performed at a time. With the Seek and Recalibrate commands however, you can perform either on up to four drives at a time. You can do this by issuing Seek or Recalibrate commands one after the other, one to each drive. Each time a command is completed for one of the drives the FDC will generate an interrupt.

When a Seek or Recalibrate command is completed the Sense Interrupt Status command must be performed before the FDC will accept another command.

Sense Interrupt Status

This command simply requests two bytes of information from the FDC. The first byte is status information which includes information about why an interrupt has been generated, i.e., has the disk drive door been opened, was an error detected during the execution of a command, etc. From this information, the processor can decide how to respond to the interrupt. The command also resets the interrupt output. The second byte is the the track number currently held in the FDC's internal track counter.

Sense Drive Status

This command requests one byte of data containing information on the status of the disk drive, i.e., is there a double-sided disk installed, is the disk write-protected, etc. The FDC takes these conditions into account automatically as it interfaces to the drive. This command merely gives the processor direct access to this status information.

Seek

This command causes the FDC to move the read/write head to a new position. The FDC moves the head in the proper direction until its own internal track counter matches the track number you gave it with the command.

Multiple Seek commands can be performed simultaneously in the same manner described for the Recalibratre command. When a Seek command is finished, indicated by an interrupt, a Sense Interrupt Status command must be performed before the FDC will accept any other command.

Read Data

The Read Data command causes data to be read off the disk. The head is loaded on the track it is presently over and the track is searched for the correct sector. In the command you specify the side of the disk, the track, the sector, and the bytes per sector code. All four of these factors are also contained in the ID field of each sector. The FDC must find a sector in which all four of these factors match before it will start to read data. When it is found, the FDC reads the data from the data field and delivers it to the processor byte by byte. Each time a byte is ready to be read by the processor, an interrupt will be generated. Also, a flag will be set in the Main Status Register in the FDC. The entire sector may be read out, or only part of it, as specified by the command. In either case, the FDC will read the entire sector and the CRC (Cyclic Redundancy Check) to check for errors.

The FDC will go on to search for and read out the next sector until it reads the last one. What sector is considered last is defined by two factors, both defined in the command.

First, in the command, you give the number of the last sector. You may, for instance, define sector 20 as the last one, even if there are 26 sectors on the track.

Second, you may specify a double-sided read. That is, you may request the FDC to automatically start reading the second side of the disk after it has reached the end of the first side. If you define sector 20 as the last one, and sector 10 of side zero as the sector to start with, the FDC will read sectors 10-20 of side 0 and sectors 1-20 of side 1.

If the FDC chip encounters a Deleted Data Address Mark, it will either skip over that sector and go on to the next, or it will terminate the command. Which action it will take is specified in the command by you. In either case, a flag will be set in a status register to indicate a Deleted Data Address Mark has been encountered.

The Read command may be stopped either by letting it reach its natural conclusion or by strobing the Terminal Count pin of the FDC chip. This can be done through an output port on the 7387. Simply read the sector or sectors you want and then strobe the Terminal Count pin.

The command will also stop if any one of a variety of errors occur. Possible error conditions are discussed later in this section under the "Execution of Commands" heading. It will also help to review the error flags in the status registers.

Read ID

This command causes the FDC to read the first valid ID field it encounters. This information is stored in the FDC. When the FDC completes the command, it generates an interrupt and sets a flag in a status register. The processor can then read the ID field information out of the FDC. If the FDC cannot find a valid ID Address Mark after it has encountered the index hole twice it will terminate the command.

Write Data

The Write Data command is very similar to the Read Data command. The correct sector is searched for and the CRC bytes associated with the ID field are read and checked. Data is then written onto the data field and the CRC calculated and written on the disk. The FDC will indicate its request for data by generating an interrupt and by setting a flag in the Main Status Register.

The Write Data command, like the Read Data command, can operate on multiple sectors and both sides of the disk. The command will terminate when the Terminal Count pin is strobed, the last sector has been written, or if some error condition has occured.

The number of data bytes written to the sector or sectors can also be controlled. For instance, if your disk is formatted with 128 byte sectors, you may specify in the command that you only wish to write 100 bytes on it. The FDC will automatically fill in the remaining bytes with zeros. The CRC will then be calculated on the entire data field.

Format a Track

This command will format a track of a disk with the IBM 3740 format. After encountering the index hole, the FDC will begin to write the ID fields, gaps and address marks, etc., necessary to format the track. It will also load the data field with a byte of data specified in the command and generate a CRC for the data field based on that data. The side of the disk, the bytes per sector, the sectors per track, and the length of Gap 3 are also specified in the command. As each ID Record is written on the disk, the FDC will request from the processor four bytes of information. These are the Track Address, Head Address, Sector Address, and Bytes per Sector Code. The FDC will request each of these by generating an interrupt and by setting a flag in the Main Status Register. These bytes should be able to be written to the FDC at the same rate as in the Write Data command.

Read Deleted Data

This command is identical to the Read Data command, except that only sectors with a Deleted Data Address Mark will be read. If a sector without a Deleted Data Address Mark is encountered, the FDC will either terminate the command or skip over that sector and search for the next numerically sequential sector. Which action is taken when this occurs is specified in the command.

Write Deleted Data

This command is identical to the Write Data command except that a Deleted Data Address Mark is written in place of a Data Address Mark. This command is normally used to mark physically defective sectors on the disk.

Read a Track

This command is similar to the Read Data command. It does have several differences though, beside the fact that it is intended for reading a track of data rather than a particular sector or sectors. First, it does not start reading data at the sector you specified in the command. Rather, it starts with the first sector after the index hole. It will continue to read out sectors in physically consecutive order until it has read the number of sectors you specified in the command. It does, however, look for the sector you specified as it is reading out these sectors. If it does not find it, a flag will be set in a status register.

Second, as mentioned, it does not search for the next numerically sequential sector after it has finished reading the previous one. Rather, it reads the sector which is physically next on the track.

Third, the command is not terminated for as many error conditions. It does not stop if it does not find the specified sector, it merely sets a flag. Also, it does not stop if it finds a CRC error, nor does it set a flag.

It responds to Deleted Data Address Marks the same way the Read Data command does. It will either terminate the command or skip the sector, depending on what you specified in the command.

The Read a Track command can only be used to read one side of the disk per command. It will terminate when it finishes reading the track, when the Terminal Count pin is strobed, or if an error condition occurs.

Scan Equal

Note: Some literature on the FDC chip indicates that the Scan commands can be used to scan more than one sector per command. However, these commands cannot be guaranteed to work correctly unless only one sector is scanned per command as described below.

The Scan Equal command reads a sector from the disk and compares it byte by byte with data supplied by the processor. The comparison is done with the binary data as is, i.e., there is no conversion from ASCII to HEX. When the command is completed, flags are set in a status register to indicate whether the data compared. Data must be provided by the processor at the same rate as a Write Data command. When using any of the Scan commands, only one sector should be scanned per command. This should be done by specifying the last sector to be read to be the same as the first sector, both of which are specified in the command.

If the sector has a Deleted Data Address Mark it will either scan it or terminate the command as soon as the Deleted Data Address Mark is encountered. Which action it takes is specified in the command.

During the comparison operation an FF Hex always compares. No matter what the data provided by the processor, if the data on the disk is an FF the FDC considers it a comparison. Likewise, no matter what the data on the disk, if the data provided by the processor is an FF the FDC considers it a comparison. FF can therefore be used as a mask during comparison.

Scan Low or Equal

Note: Some literature on the FDC chip indicates that the Scan commands can be used to scan more than one sector per command. However, these commands cannot be guaranteed to work correctly unless only one sector is scanned per command.

This is the same as the Scan Equal command except that data on the disk that is equal to or less than the data supplied by the processor is considered a comparison.

Scan High or Equal

Note: Some literature on the FDC chip indicates that the Scan commands can be used to scan more than one sector per command. However, these commands cannot be guaranteed to work correctly unless only one sector is scanned per command.

This is the same as the Scan Equal command except that data on the disk that is equal to or greater than the data supplied by the processor is considered a comparison.

Execution of Commands

Read Data
Write Data
Write Deleted Data
Read Deleted Data
Read a Track

Command Phase

Write out all bytes associated with the command to the FDC. One way for the processor to handle this is to have the command bytes in RAM in the form of a look-up table. Before you issue a command you would modify the contents of the table, i.e., sector number, track number, etc., then simply write the bytes out in consecutive order.

The Main Status register must be read before each command byte is written out. This is a requirement of the FDC chip. After a command byte has been written, it may take as much as 15us. for the flags in the Main Status register to become stable. Therefore, the processor should wait 15us. between writing a command byte and reading the Main Status register. The processor may use this much time taking care of the "housekeeping" between command bytes. You should check your program to be sure.

It is assumed that you have already performed a Seek command to position the head over the desired track. Also, anytime the processor is powered up or reset, a Specify command and a Recalibrate command should be performed before any other commands are performed.

Execution Phase

When the FDC is ready for a data transfer, it will signal the processor in one of three ways. If you have enabled the 7387's interrupt, The FDC will interrupt the processor. If the interrupt has not been enabled, you can monitor the interrupt output from the FDC chip by checking bit 7 of the Interrupt Status port. The third method is to monitor the Request for Master bit, bit 7, of the Main Status register.

Whichever method you use, it is best to also check the Execution Mode bit, bit 5, of the Main Status Register. This bit will tell you if the FDC is requesting a data transfer or if an error has occurred and the FDC has entered the Result Phase.

The average data rate is one byte every 32us. However, under worst case conditions the FDC chip may make a data byte available to the processor for only 27us. For this reason the processor must be able to perform a data transfer every 27us. for 8" disks (54us. for 5.25" disks) or an overrun error may occur and the command will be terminated. The Main Status register does not need to be read before each data transfer as it does in the Command and Result phases.

The processor can terminate the command in one of two ways. It can let the command reach its natural conclusion or it can perform an output instruction to the Terminate port.

Result Phase

When the FDC enters the Result Phase, the Execution Mode flag, bit 5, in the Main Status register will no longer be set. Also the FDC will generate an interrupt. It will not generate an interrupt for each Result byte.

All of the bytes associated with the Result Phase must be read before the FDC will accept another command. One method of ensuring that you have read all the Result bytes is to monitor the Data Input/Output flag in the Main Status register. When the flag goes low, the FDC is through providing Result bytes.

As with the Command Phase, the Main Status register must be read before each Result byte is read. The Main Status register will take up to 15us. to settle after each Result byte is read.
The status information should be checked to determine if there is an error condition. The two Interrupt Code bits of Status Register 0, bits 6 and 7, can be used for this purpose. If it is determined that there is an error the other status information can be analyzed to determine the source of the error.

The status register flags that may be affected are:

Status Register 0		Status Register 1		Status Register 2	
Bit	Name	Bit	Name	Bit	Name
6&7	Interrupt Code	5	CRC Error	6	Control Mark
4	Equipment Check	4	Overrun	5	Data CRC Error
3	Not Ready	2	Sector Not Found	4	Wrong Track
2	Head	1	Not Writeable	1	Bad Track
1&0	Drive	0	Missing Address Mark	0	Missing Data Field Address Mark

Read ID
Sense Drive Status

Command Phase

Write out the Command bytes in the manner previously described.

Execution Phase

There is no data transfer during the Execution Phase for these commands.

Result Phase

Read all Result bytes in the manner previously described.

The status register flags that may be affected for the Read ID command are shown below. The Sense Drive Status command affects all of Status Register 3.

Status Register 0		Status Register 1		Status Register 2	
Bit	Name	Bit	Name	Bit	Name
6&7	Interrupt Code	2	Sector Not Found		
4	Equipment Check	0	Missing Address Mark		
3	Not Ready				
2	Head				
0&1	Drive				

Scan Equal
Scan Low or Equal
Scan High or Equal

Command Phase

Write out the Command bytes in the manner previously described.

Execution Phase

The FDC will request data from the processor for comparison, in the same manner described for the Write command. After you have provided the FDC with an entire sector of data, check the Main Status register to determine if there was a comparison. This can be determined by checking either the Execution Mode bit or the Data Input/Output bit, bits 5 and 6. If the Execution Mode bit goes low, or the Data Input/Output bit goes high, the FDC has entered the Result phase.

The FDC may have entered the Result phase because there was a comparison, the Scan was completed without finding a comparison, or an error occurred. Which of these has occurred can be determined by checking the flags in the status registers extracted during the Result phase.

Result Phase

Read in all the Result bytes in the manner previously described. Check the Interrupt Code bits of Status Register 0. Be sure to check the Scan Hit flag in Status Register 2.

The status register flags which may be affected are:

Status Register 0		Status Register 1		Status Register 2	
Bit	Name	Bit	Name	Bit	Name
6&7	Interrupt Code	5	CRC Error	6	Control Mark
4	Equipment Check	4	Overrun	5	Data CRC Error
3	Not Ready	2	Sector Not Found	4	Wrong Track
2	Head	0	Missing Address Mark	3	Scan Hit
0&1	Drive			2	Scan Miss
				1	Bad Track
				0	Missing Data Field Address Mark

Sense Interrupt Status

Command Phase

This command has only one Command byte. Read the Main Status Register once and write out the command byte.

Execution Phase

This command has no Execution Phase.

Result Phase

Read the Result bytes in the manner previously described for the Read and Write commands.

The Sense Interrupt Status command is used for two reasons. The first is to extract status information after the completion of a Recalibrate or Seek command. The Sense Interrupt Status command **must** be performed after a Recalibrate or Seek command.

The second reason to use this command is to determine the reason for an interrupt which occurs at an odd time, i.e., an interrupt which occurs when no FDC commands are in process.

The FDC generates an interrupt whenever any of the Ready lines from the disk drives change state. Therefore, an interrupt may occur at anytime, provided that the 7387's interrupt is enabled. If you do not have it enabled, and you issue a command to a drive whose Ready line has gone inactive, the command will terminate.

It is possible for an interrupt to occur for more than one reason. Therefore, when this command is used, it is best to issue it repeatedly until all interrupting conditions have been found and responded to. When there are no more interrupt conditions, the FDC will treat the Sense Interrupt Status command as an invalid command. It will respond with only one Result byte, Status register 0, and its contents will be 80 Hex.

The status register flags that may be affected include all of Status Register 0.

Recalibrate
Seek

Command Phase

Write out the Command bytes in the manner previously described.

Execution Phase

The Execution phase of these commands requires no interaction with the processor.

Result Phase

The FDC will generate an interrupt when the Execution phase is completed. These two commands have no Result phase. Rather, they **must** be followed by a Sense Interrupt Status command. The Result bytes of the Sense Interrupt Status command can then be checked by the processor for error conditions.

Specify

Command Phase

Write out the Command bytes in the manner previously described.

Execution Phase

The Specify command has no Execution Phase.

Result Phase

The Specify command has no Result phase. It will not generate an interrupt and it does not need to be followed by a Sense Interrupt Status command.

Format a Track

Command Phase

The head must be positioned over the proper track by use of the Seek command before the Format a Track command is issued.
Write out the command bytes in the manner described for the Read and Write commands.

Execution Phase

The FDC will request four bytes of data for every sector it formats. These four bytes are Track number, Head number, Sector number and Bytes per Sector code, in that order. These numbers should agree with the track, head, etc., you are formatting. Otherwise, when a Read or Write command is performed, the FDC won't be able to find the sector requested. The sector numbers may be in consecutive order, or they may be interleaved.
One way to provide these four bytes for each sector is to form a look-up table in RAM, and write them out sequentially.
Writing these bytes out should be handled in the same way writing data during a Write Data command is handled.

Result Phase

The FDC will generate an interrupt when it enters the Result phase. The Result bytes should be read in the manner previously described for Read and Write commands. The Status registers can be checked to ensure that there were no errors. The rest of the Result bytes, however, have no meaning.

The status register flags that may be affected are:

Status Register 0		Status Register 1		Status Register 2	
Bit	Name	Bit	Name	Bit	Name
6&7	Interrupt Code	1	Not Writeable		
4	Equipment Check				
3	Not Ready				
2	Head				
0&1	Drive				

SECTION 4
Operating Software

Introduction

This section contains hardware-level subroutine modules with which to operate the 7387 card. The software in this section can be used without license from Pro-Log. Although tested and believed correct, this software is not represented to be free from errors or copyright infringement, or appropriate for any specific application.
The subroutines are in STD instruction mnemonics, using 8080 assembly codes. They execute in 8080, 8085, Z80, NSC 800, and other code-compatible microprocessor systems. The coding forms are grouped at the end of this section, following the flowcharts.
Flowcharts, which do not refer to microprocessor characteristics, allow the subroutines to be easily adapted to other microprocessor types.

Memory Addresses

Full memory addresses are given. They are preferred addresses that allow the subroutines to work with those provided for other Series 7000 STD BUS cards from Pro-Log. The program addresses correspond to the Series 7800 processor cards' onboard ROM/EPROM and RAM sockets.
If your system can not use the memory addresses in the 7387's software package, simply change the memory page addresses, as required, when loading these modules into your system.

I/O Port Addresses

The 7387's I/O ports are assigned preferred hexadecimal addresses C4-C7 for compatibility with other Series 7000 cards. Section 2 shows how to remap these addresses if necessary. This software can be used by simply changing the port addresses when loading the program modules into your system.

Description of Subroutines

This section provides software subroutine modules that can be used as a base for writing a disk operating system, or as examples from which to write your own subroutines. You will need to write some software of your own since these subroutines in themselves do not make up a disk operating system. Fig. 4-1 shows the level of complexity that these subroutines occupy.

They do not make use of all the FDC commands, or all of the capabilities of the card. They are intended to provide the necessary control to transfer data to and from the disks and to simplify the task of writing a disk operating system. They allow you to transfer data using a few simple commands and yet give you access, when desired, to detailed status information on both the FDC and disk drive.

There are 22 subroutines provided in this section. Most of these you will not need to use directly, they are subroutines within subroutines. There are only 10 subroutines that you will need to use directly. The other subroutines can be used if desired. Documentation of all the subroutines is provided later in this section. Figure 4-2 lists the 10 main subroutines.

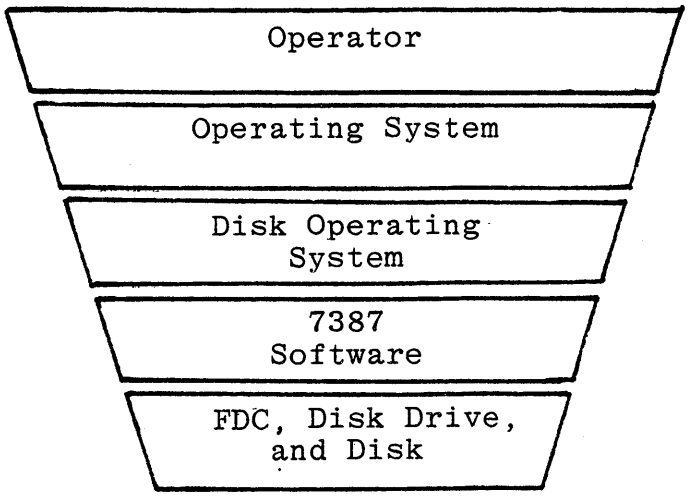


Fig. 4-1, Function of 7387 Software

Subroutine	Entry Address	Entry Requirements	Previously Run Subroutines
Set 8"	1A00	-	-
Set 5"	1A06	-	-
Recalibrate	1C00	-	Set 8" or Set 5" Set Drive
Set Trans Buf	1A63	Starting Buffer Address in Reg. Pair BC.	-
Set Drive	1A6C	Drive Number in Reg. C	-
Set Track	1A88	Track Number in Reg. C	Set Drive
Set Sector	1AC0	Sector number in Reg. C	-
Format	1B2E	-	Set Trans Buf, Set Drive
Write Sector	1B00	-	Set Trans Buf, Set Drive, Set Track, Set Sector
Read Sector	1ACF	-	Set Trans Buf, Set Drive, Set Track, Set Sector

Comments
Sets Head Load time and other variables for 8" Shugart or equivalent disk drive. This or Set 5" must be used once after reset.
Sets Head Load time and other variables for 5.25" Shugart or equivalent disk drive. This or Set 8" must be used once after reset
Sets the head over Track 0, and sets the FDC track counter to 0. This must be used once for each disk drive after reset.
Defines the starting address of the RAM area you will use for transferring data to and from the disk
Selects the drive to be accessed.
Selects the track to be accessed.
Selects the sector to be accessed.
Formats the entire disk, both sides if double-sided, in the IBM 3740 format. Data byte written into data fields is E5.
Writes a sector of data from the transfer buffer to the disk. Buffer address, drive, track, and sector must be preselected.
Reads a sector of data to the transfer buffer in RAM from the disk. Buffer address, drive, track, and sector must be preselected.

Fig. 4-2, 7387 Main Subroutines

Ram Mapping

Two sections of RAM must be supplied for use with these subroutines. The first is the Transfer Buffer. This is an area of RAM equal in size to one sector of data, which is used as a data buffer for moving data to and from the disk. This software uses 128 byte sectors. This section can be anywhere in memory, and is specified by way of the "Set Trans Buf" subroutine.

The second section of RAM is a "scratch pad" area. It is used by the software for look-up tables for sending commands to the FDC and for storing status information recieved from the FDC. This section is 30 bytes long and must start on the first address of a page of memory. That is, it must start on address 00 of the page of your choice. If you use page 40, it would occupy addresses 4000 Hex through 401D Hex. In the program listings, all references to the page address have been left blank. They must be supplied by the user. Figure 4-3 is a list of all the locations where you must supply this address.

Status Information

After running the Format, Recalibrate, Read Data, or Write Data subroutines, status information is left in the scratch RAM. The status information will consist of several bytes of information, all of which are defined in Section 3 under the "Instruction Set" heading.

The detailed descriptions of the subroutines later in this section list what status information each subroutine leaves and its position in RAM.

The lists take the form of:

Address	Status
XX00	Status Reg. 0
XX01	Status Reg. 1

etc.

The XX indicates your page address for the scratch pad RAM. The rest of the address is the line number in RAM. The status information always begins at line address 00.
The number of status bytes left in the scratch pad RAM is contained in Register C upon exiting one of these subroutines.

Interrupt Considerations

During the course of the Read Data, Write Data, and Format commands you will likely want to disable the processor's maskable interrupt. This is because the data transfers that take place during these commands must take place within a given time frame, and there is no time for the processor to perform other functions.
This software takes care of this problem by disabling the processor's interrupt just before it sends a command to the FDC. This means that the interrupt will be disabled upon entering the Read Data, Write Data, Format, or Recalibrate commands. The interrupt is not reenabled. If you are using the processor's interrupt you should reenable it when the processor returns from these subroutines.
If your interrupts have a higher priority than the disk interface, you can eliminate the "Disable Interrupt" command from this software. It is located at address 1C6C. In this case, if an interrupt occurs during a data transfer an error will most likely occur. The processor can then simply reperform the command.

1A0B	1B0E	1BB7
1A67	1B36	1BC1
1A74	1B39	1BC5
1A7E	1B40	1C02
1A83	1B45	1C1B
1A8A	1B4C	1C2C
1AC2	1B58	1C39
1AD4	1B62	1C4A
1AD9	1B77	1C5B
1ADD	1B99	1C98
1B05	1BA4	1CA3
1B09	1BB1	

Fig. 4-3, 7387 User Supplied RAM Page Addresses

Set 8"

Entry Address: 1A00
Entry Requirements: None
Registers Used: A,B,C,D,E,H,L
Status Information: None

This subroutine or the Set 5" subroutine must be used once after power-up or reset before any of the other subroutines are used.

The subroutine initializes the FDC with the time between stepper motor pulses, the time allowed for head loading and the time delay between completion of a command and the unloading of the head. The time delays used are those recommended for Shugart 8" disk drives. They are:

Head load time = 36ms
Head unload time = 240ms
Step rate time = 8 ms

If you wish to change these parameters they are located in addresses 1A37 and 1A38 of the program listing at the end of this section.

Set 5"

Entry Address: 1A06
Entry Requirements: None
Registers Used: A,B,C,D,E,H,L
Status Information: None

This subroutine or the Set 8" subroutine must be used once after power-up or reset before any of the other subroutines are used.

This subroutine initializes the FDC with the time between stepper motor pulses, the time allowed for head loading, and the time delay between completion of a command and the unloading of the head. The time delays used are those recommended for Shugart 5-1/4" disk drives.

They are:
Head load time = 508ms
Head unload time = 480ms
Step rate time = 32ms
If you wish to change these parameters, they are located in addresses 1A47 and 1A48 of the program listing at the end of this section.

Recalibrate

Entry Address: 1C00
Entry Requirements: None
Registers Used: A,B,H,L
Status Information:

ADDRESS	STATUS
XX 00	Status Reg. 0
XX 01	Track #

Zero flag set (1) no error occurred.
Zero flag reset (0) an error occurred.

This subroutine must be performed once for each disk drive after power-up or reset and must be preceeded by the Set Drive and either the Set 8" or Set 5" subroutines.

This subroutine causes the head to be positioned over Track 0 and causes the FDC's internal track counter to be reset to 0.

Set Trans Buf

Entry Address: 1A63
Entry Requirements: Starting address of Transfer Buffer in Register pair BC.
Registers Used: B,C,H,L
Status Information: None

This routine specifies the location of the transfer buffer, the area of RAM where data is moved on and off the disk. Normally this subroutine will only be used once. The usual method of moving data on and off the disk is to have an area of RAM the size of a sector dedicated to storing data that is being transfered. Data is moved into this buffer before it is written on the disk, and data read from the disk is received into this buffer and then moved to its proper location.
Alternately, the transfer buffer can be redefined before each sector is read allowing the data to be received directly into its proper location. Data can be written out in a similar fashion, even from ROM.

Set Drive

Entry Address: 1A6C
Entry Requirements: Drive number, in Hex, in Register C.
Registers Used: A,C
Status Information: None

This subroutine specifies the disk drive you wish to access. Once you have selected a drive, you do not need to use this subroutine again until you access a different drive. If you have more than one 7387 card and you enter this subroutine with a drive number greater than four, the processor can be directed to service the second 7387 card. A jump instruction is provided in the subroutine for this purpose. The additional service routine and the address for the jump instruction must be provided by the user. If you do not need this feature simply replace the jump instruction with a series of three NOP instructions, 00 Hex. The jump instruction is located at address 1A6F.

Set Track

Entry Address: 1A88
Entry Requirements: Track number, in HEX, in Register C. Drive must be preselected.
Registers Used: A,C,H,L
Status Information: None

This subroutine specifies the track to be accessed. Once a track has been selected, this subroutine does not need to be used again until you wish to access a different track. The Set Track subroutine can also be used to specify which side of a two-sided disk you wish to access. By selecting track numbers 0 through 76 you access the first side of the disk, side 0. Selecting track numbers 77 through 153 you access the second side of the disk, side 1. The subroutine can detect if the track number you provided is to large to be valid. Also, if you give it a track number between 77 and 153 the program will determine if there is a two-sided disk and a two-sided disk drive. To do this the FDC must know which drive to check, this is why the drive must be preselected via the Set Drive subroutine. Jump instructions have been placed in the subroutine to direct the processor to an error routine should either of these errors occur. The error routine and the addresses for the jump instructions must be supplied by the user. If you will not require the error routine, simply replace the jump instructions with a series of three NOP instructions, 00 Hex. The jump instructions are located at addresses 1AA2 and 1AAC.

Set Sector

Entry Address: 1AC0
Entry Requirements: Sector number, in HEX, in Register C.
Registers Used: A,C,H,L
Status Information: None

This subroutine selects the sector to be accessed. Once a sector is selected, the subroutine does not need to be used until you wish to access a different sector.

The subroutine can detect if the sector number you provide is too large to be valid. A jump instruction is provided in the subroutine to direct the processor to an error routine should this occur. The error routine and the address for the jump instruction must be provided by the user. If you will not require the error routine simply replace the jump instruction with a series of three NOP instructions, 00 Hex. The jump instruction is located at address 1AC5.

Write Sector

Entry Address: 1B00

Entry Requirements: Transfer Buffer, Drive, Track, and Sector must be preselected by their respective subroutines. The data to be written must be in the Transfer Buffer.

Registers Used: A,B,C,D,E,H,L

Status Information:

ADDRESS	STATUS
XX 00	Status Reg. 0
XX 01	Status Reg. 1
XX 02	Status Reg. 2
XX 03	Track #
XX 04	Head #
XX 05	Sector #
XX 06	Bytes/Sector Code

Zero flag set (1) no error occurred.
Zero flag reset (0) an error occurred.

This subroutine writes a sector of data, 128 bytes, from the transfer buffer onto the disk. It will select the disk drive, move the head to the correct track if necessary, find the right sector and write the data.

The Write Sector subroutine was written to work with either the 4MHz Z80 or the 8085 processor. It will not work with the 2.5MHz Z80 because it cannot keep up with the required data transfer rate. Figure 4-4 shows a modification to the program listing using the Z80's special Jump Relative instructions. This will allow the program to be used with the 2.5MHz Z80.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
	0					
	1					
	2					
	3					
	4					
1B	15	DB	WRITE LOOP	IPA		← WAIT FOR RQM
	16	C4		—	MAW STATUS	
	17	17		RLAC		
	18	30		JPR	CO	
	19	FB		—	WRITE LOOP	↓
	1A	17		RLAC		← FETCH RESULT INFO. IF THERES AN ERROR
	1B	38		JPR	C1	
	1C	0A		—	FETCH RESULT	↓
	1D	1A		LDAN	(DE)	← GET DATA BYTE + SEND TO FDC
	1E	D3		OPA		
1B	1F	C5		—	DATA	↓
1B	20	13		ICP	DE	← INC POINTER
	21	0D		DCC		← DEC COUNTER
	22	C2		JP	ZO	← GO SEND NEXT BYTE IF NOT FINISHED
	23	15		—	WRITE LOOP	
	24	1B		—		↓
	25	D3		OPA		← SEND TERMINAL COUNT WHEN FINISHED
	26	C4		—	TC	↓
1B	27	CD	FETCH RESULT	JS		← GET EXECUTION RESULTS + SET FAIL FLAG
	28	92		—	(RESULT FLAG)	
	29	1C		—		↓
	2A	C9	———	RTS		← RETURNS Z=1 PASS Z=0 FAIL
	B					
	C					
	D					
	E					
	F					

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Fig. 4-4, 7387 "Write Data" Modification for 2.5MHz Z80

Read Sector

Entry Address: 1ACF
Entry Requirements: Transfer Buffer, drive, track, and sector must all be preselected by their respective subroutines.
Registers Used: A,B,C,D,E,H,L
Status Information:

ADDRESS	STATUS
XX 00	Status Reg. 0
XX 01	Status Reg. 1
XX 02	Status Reg. 2
XX 03	Track #
XX 04	Head #
XX 05	Sector #
XX 06	Bytes/Sector Code

Zero flag set (1) no error occurred.
Zero flag reset (0) an error occurred.

This subroutine reads a sector of data, 128 bytes, from the disk into the transfer buffer. It will select the disk drive, move the head to the correct track if necessary, find the right sector and read the data.
The Read Sector subroutine was written to work with either the 4MHz Z80 or the 8085 processor. It will not work with the 2.5MHz Z80 because it cannot keep up with the required data transfer rate. Fig. 4-5 shows a modification to the program listing using the Z80's special Jump Relative instructions. This will allow the program to be used with the 2.5MHz Z80.

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS
	0					
	1					
	2					
	3					
	4					
	5					
1A	E 6	DB	READ LOOP	IPA		- WAIT FOR RQM
	7	C4		—	MAIN STATUS	
	8	17		RLAC		
	9	30		JPR	CO	
	A	FB		—	READ LOOP	↓
	B	17		RLAC		- GET RESULT INFO. IF THERE'S AN ERROR
	C	17		RLAC		
	D	30		JPR	CO	
	E	0A		—	GET RESULT	↓
	E F	DB		IPA		- INPUT ONE DATA BYTE
	F 0	C5		—	DATA	↓
	1	12		STAN	(DE)	← STORE
	2	13		ICP	DE	← INC POINTER
	3	0D		DCC		← DEC COUNTER
	4	C2		JP	Z0	- GO GET NEXT CHARACTER IF NOT FINISHED
	5	E6		—	READ LOOP	
	6	1A		—		↓
	7	D3		OPA		- SEND TERMINAL COUNT WHEN FINISHED
	8	C4		—	TC	↓
1A	F 9	CD	GET RESULT	JS		- GET EXECUTION RESULTS & SET FAIL FLAG
	A	92		—	(RESULT FLAG)	
	B	1C		—		↓
	C	C9		RTS		← RETURNS Z=1 PASS Z=0 FAIL
	D					
	E					
	F					

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Fig. 4-5, 7387 "Read Data" Modification for 2.5MHz Z80

Format

Entry Address: 1BD0
Entry Reguirements: Transfer Buffer and drive must be preselected by their respective subroutines. Buffer size must be equal to 4 x the number of sectors per track, i.e. 104 bytes for 26 sectors per track.
Registers Used: A,B,C,D,E,H,L
Status Information:

ADDRESS	STATUS
XX 00	Status Reg. 0
XX 01	Status Reg. 1
XX 02	Status Reg. 2
XX 03	Track #
XX 04	Head #
XX 05	Sector #
XX 06	Bytes/Sector Code

Zero flag set (1) no error occurred.
Zero flag reset (0) an error occurred.

The Format subroutine formats the entire disk, both sides if it's two-sided, in the IBM 3740 single density format. The data fields are filled with the data byte E5 Hex. The format uses 26 sectors per track and 128 bytes per sector. If you wish to change any of these parameters, they are located in the Format Command table, address 1A30 for 8" disks, address 1A50 for 5-1/4" disks.
The sectors are numbered sequentially, sector one following immediately after the index hole. If you wish to interleave sectors, you can do so by modifying the table at address 1BD0.
The Format subroutine was written to work with either the 4MHz Z80 or the 8085 processor. It will not work with the 2.5MHz Z80 because it cannot keep up with the required data transfer rate. Fig. 4-6 shows a modification to the program listing using the Z80's special Jump Relative instructions. This will allow the program to be used with the 2.5MHz Z80.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
	70					
	1					
1B	72	CD	(FORMAT TRACK)	JS		← GENERATE FORMAT COMMAND TABLE
	3	97		—	(FORM TABLES)	
	4	1B		—		↓
	5	21		LDPI	HL	← POINT TO FORMAT COMMAND TABLE
	6	10		—	FORMAT CMDTABLE	
	7	XX		—		↓
	8	06		LDBI		← 6 COMMAND BYTES
	9	06		—	06	↓
	A	CD		JS		← SEND COMMAND TO FDC
	B	65		—	(COMMAND)	
	C	1C		—		↓
1B	7D	DB	TRACK LOOP	IPA		← WAIT FOR RQM
	E	C4		—	MAIN STATUS	
1B	7F	17		RLAC		
1B	80	30		JPR	CO	
	1	FB		—	TRACK LOOP	↓
	2	17		RLAC		← EXTRACT RESULTS IF THERE'S AN ERROR
	3	38		JPR	C1	
	4	0A		—	EXTRACT RESULTS	↓
	5	1A		LDAN	(DE)	← OUTPUT DATA BYTE
	6	D3		OPA		
	7	C5		—	DATA	↓
	8	13		ICP	DE	← INC POINTER
	9	0D		DCC		← DEC COUNTER
	A	C2		JP	Z0	← LOOP UNTIL ALL CHARACTERS ARE SENT
	B	7D		—	TRACK LOOP	
	C	1B		—		↓
	D	D3		OPA		← SEND TERMINAL COUNT
	E	C4		—	TC	↓
1B	8F	CD	EXTRACT RESULTS	JS		← EXTRACT RESULTS
	90	92		—	(RESULT FLAG)	STORE IN RESULT TABLE
	1	1C		—		↓
	2	C9	———	RTS		← RETURNS Z=1 PASS Z=0 FAIL
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

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Fig. 4-6, 7387 "Format" Modification for 2.5MHz Z80

Flowcharts and Listings

Figures 4-7 through 4-23 are flowcharts for the 22 subroutines provided in this section. Following these are the program listings for the subroutines.

SPECIFY (COMMAND)

The Specify Command is used to initialize the FDC after RESET before any other commands can be issued.

Registers used H,L,B,A

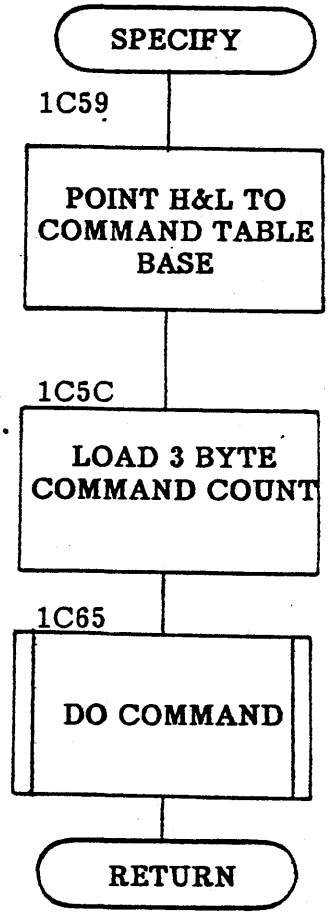


Fig. 4-7, 7387 "Specify" Flowchart

(Recalibrate) This routine allows the user to home a selected drive.

Registers used H,L,B,A

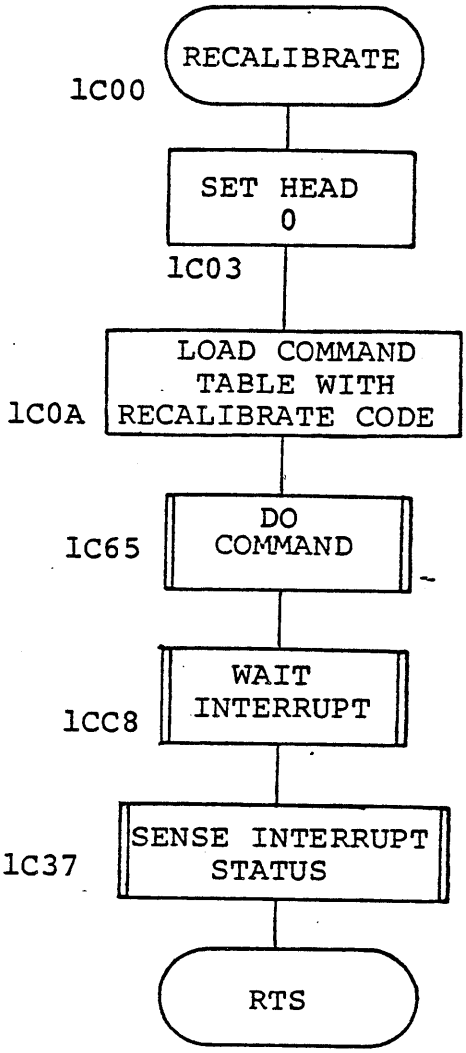
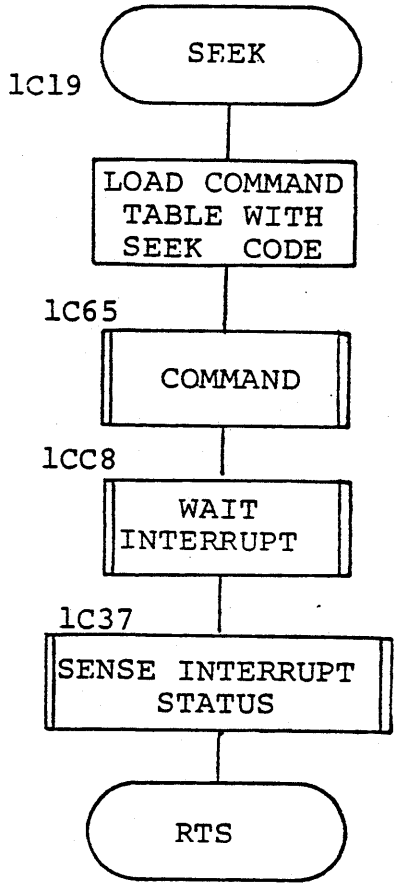


Fig. 4-8, 7387 "Recalibrate" Flowchart

(Seek) This routine allows the user to position the head over desired track.

Registers used H,L,B,A



Z = 0, Fail Z = 1, Pass

Fig. 4-9, 7387 "Seek" Flowchart

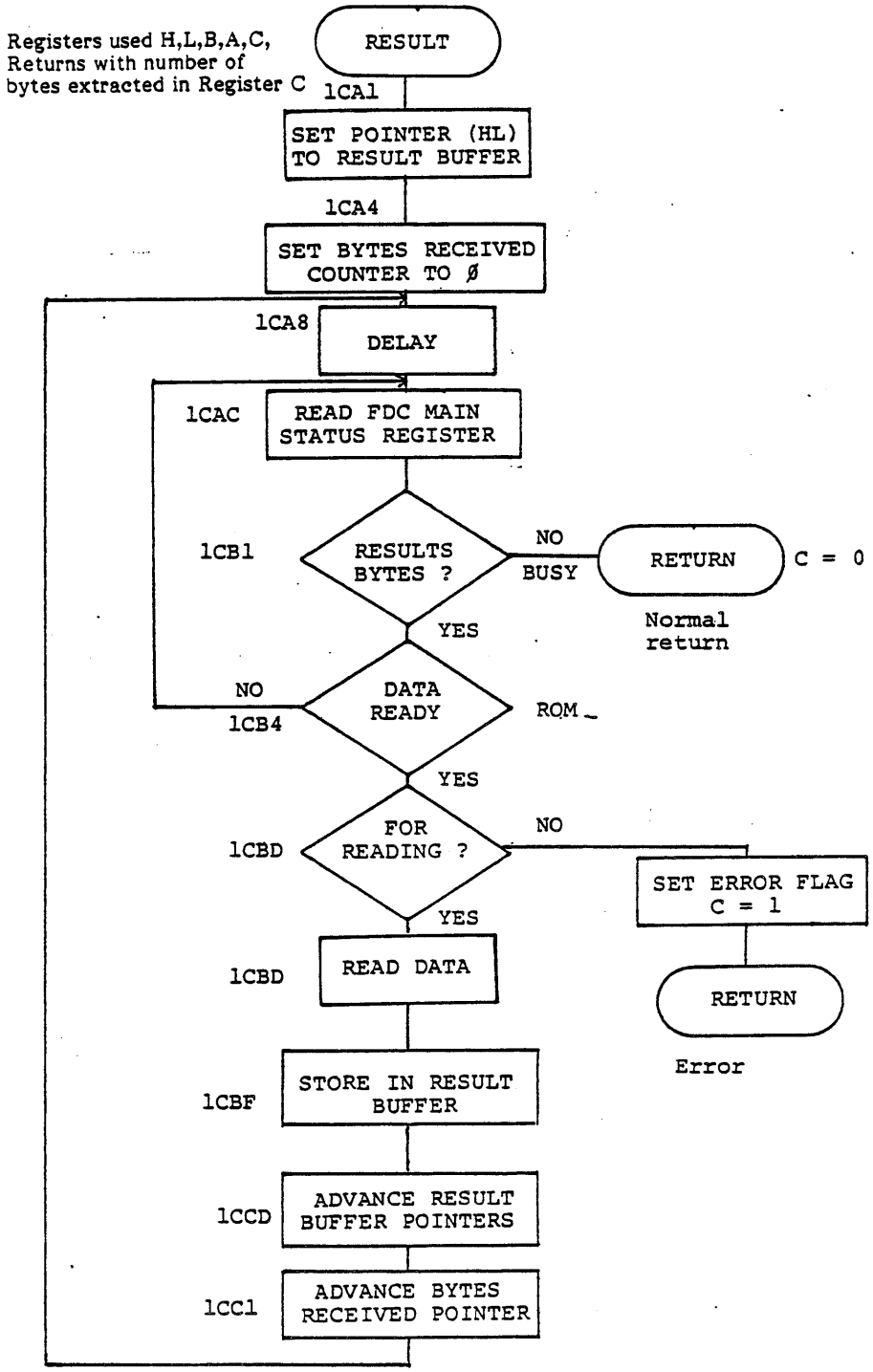


Fig. 4-10, 7387 "Result" Flowchart

(Format) This routine allows the user to format a disk single or double-sided.

Registers used H,L,D,E,B,C,A

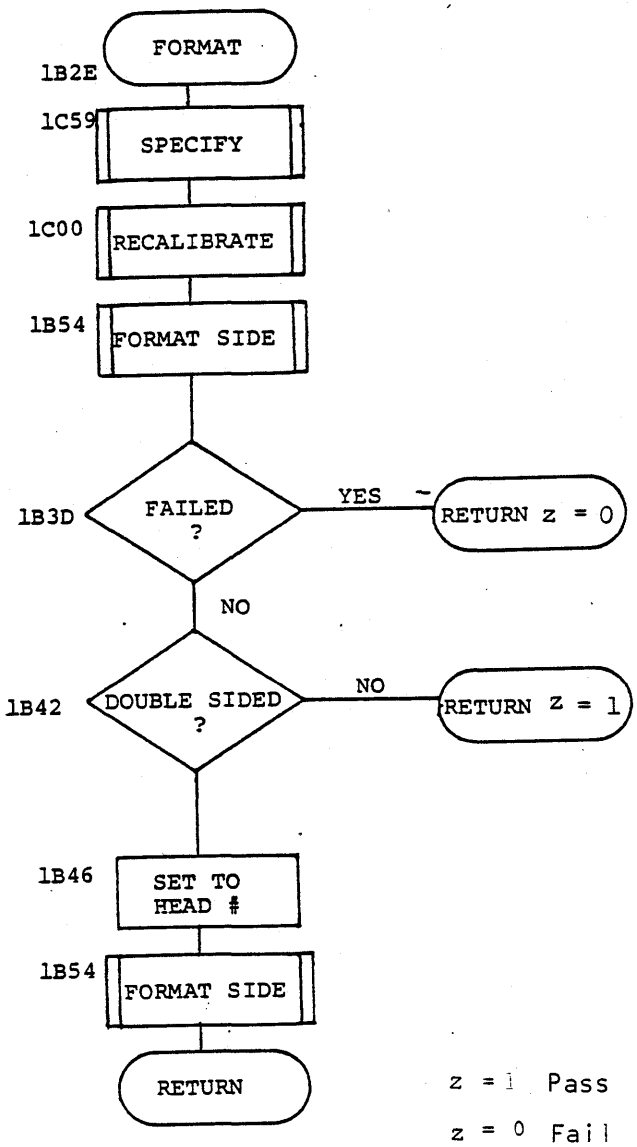


Fig. 4-11, 7387 "Format" Flowchart

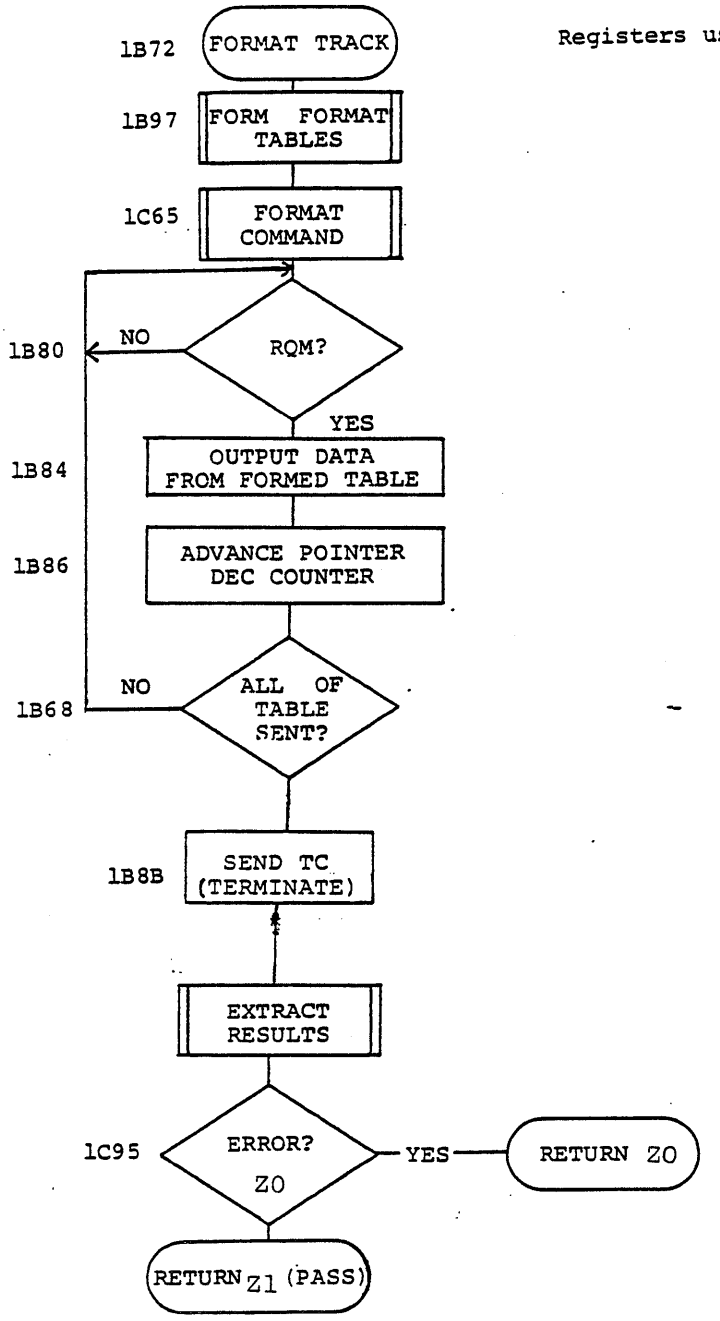
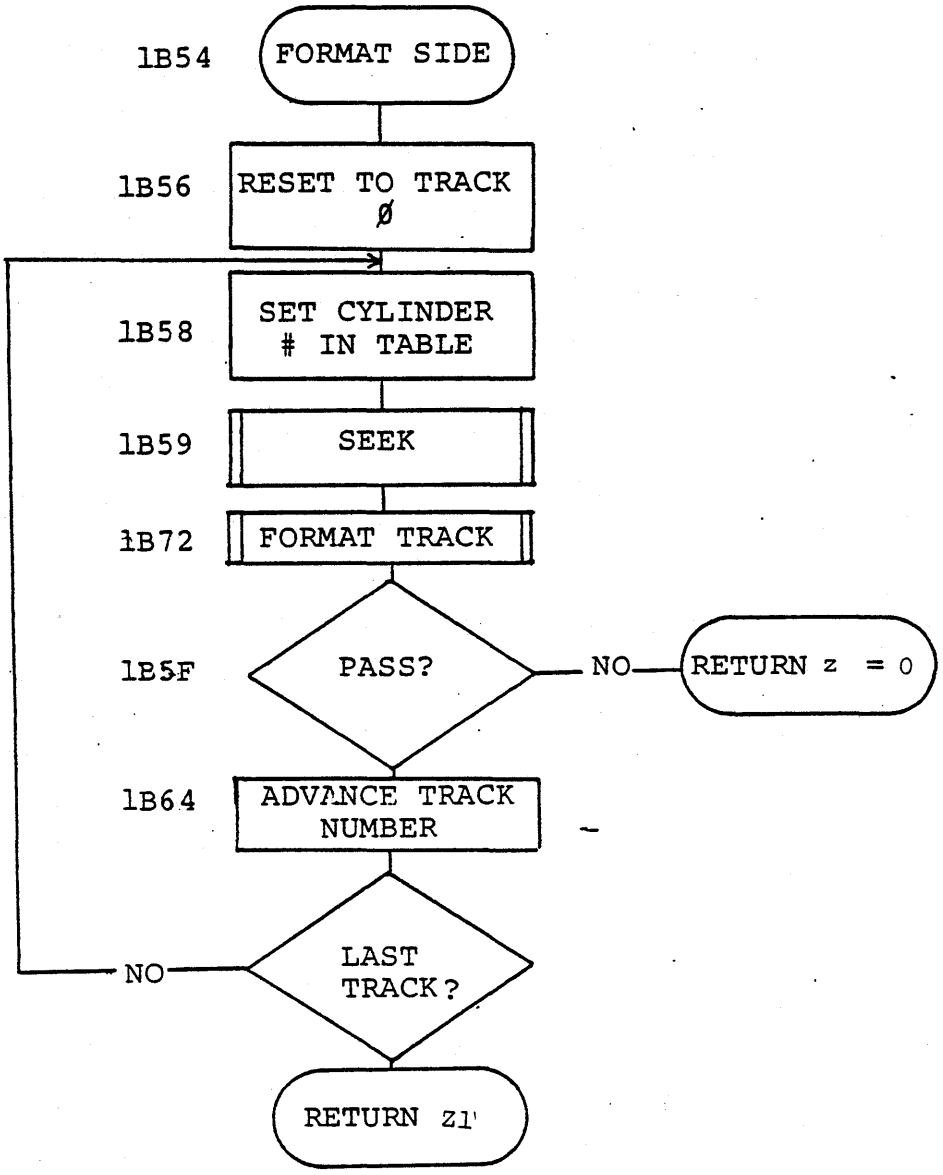


Fig. 4-12, 7387 "Format Track" Flowchart

Registers used H,C,D,E,B,C,A



Side formatted

Fig. 4-13, 7387 "Format Side" Flowchart

Registers used H,L,D,E,B,C,A

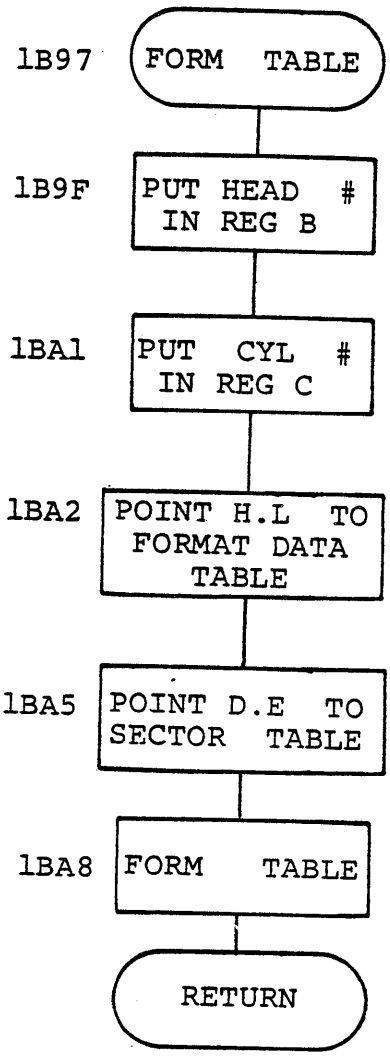


Fig. 4-14, 7387 "Form Table" Flowchart

(Write Sector) Ths routine allows the user to write the data in the transfer buffer to selected track and sector.

Registers used H,L,D,E,C,B,A.

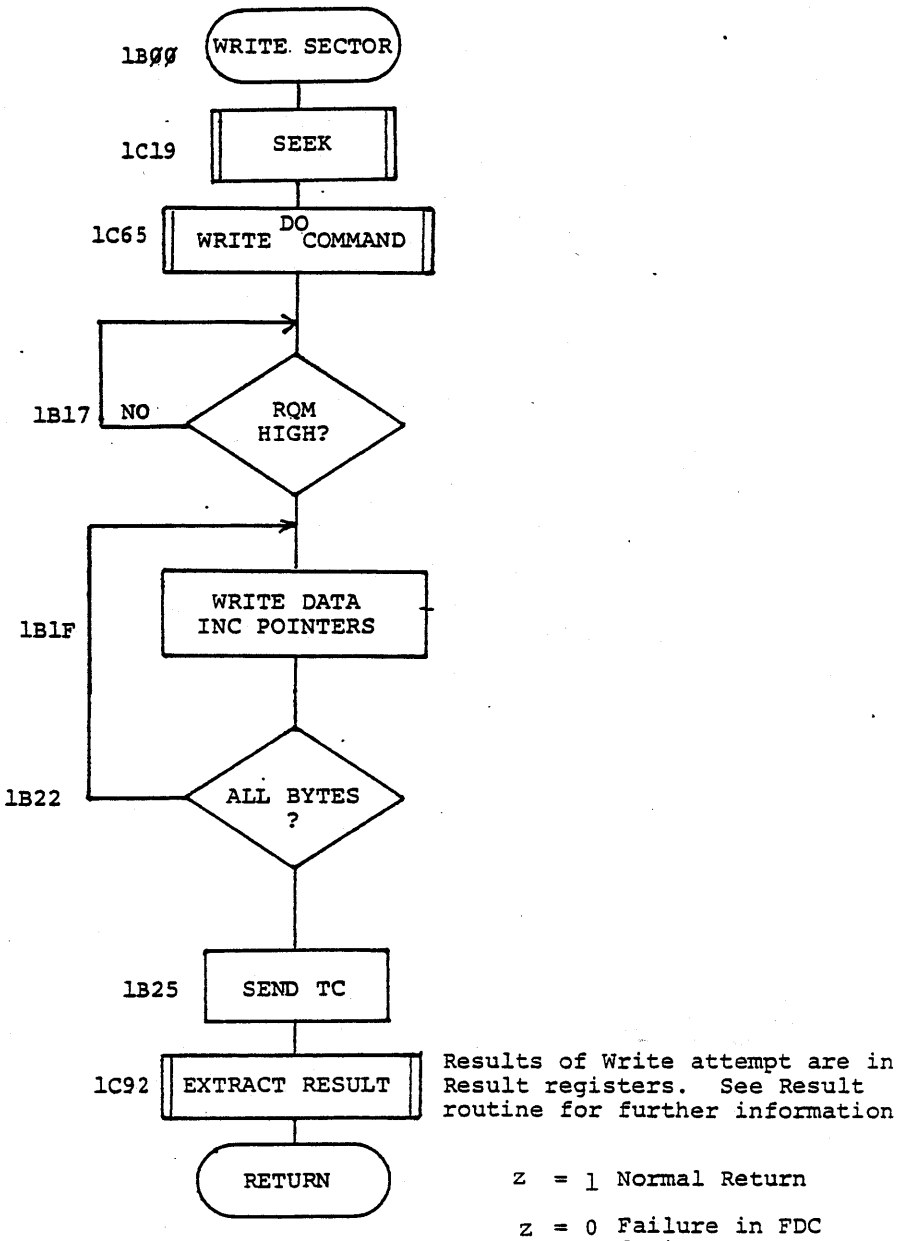


Fig. 4-15, 7387 "Write Sector" Flowchart

(Read Sector) This routine allows the user to read a sector of data and store it in the transfer buffer.

Registers used H,L,D,E,B,C,A.

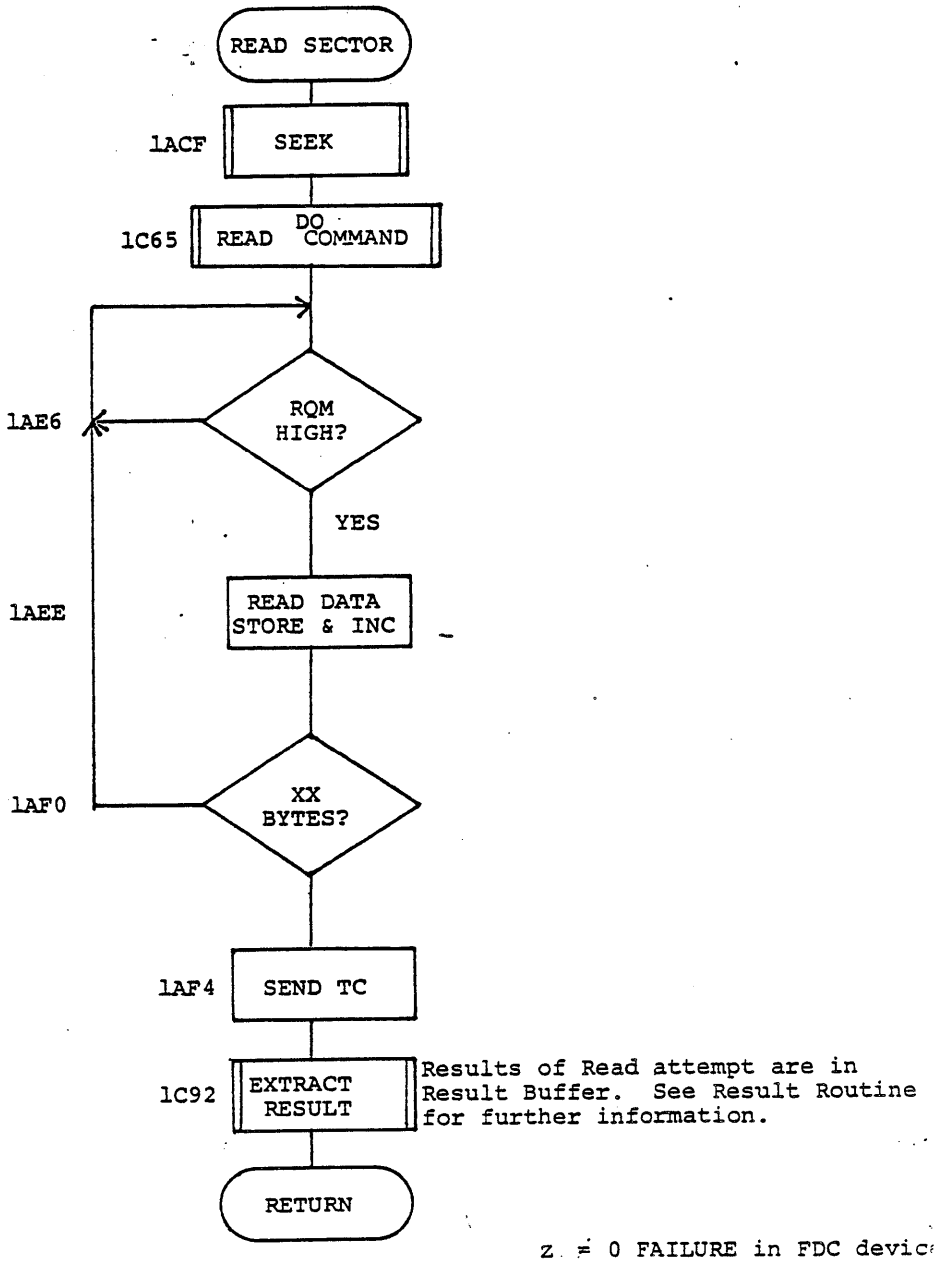


Fig. 4-16, 7387 "Read Sector" Flowchart

SENSE DRIVE STATUS (Command)

The Sense Drive Status Command is used to obtain the status of the Disk Drives.

Registers used
H,L,B,A

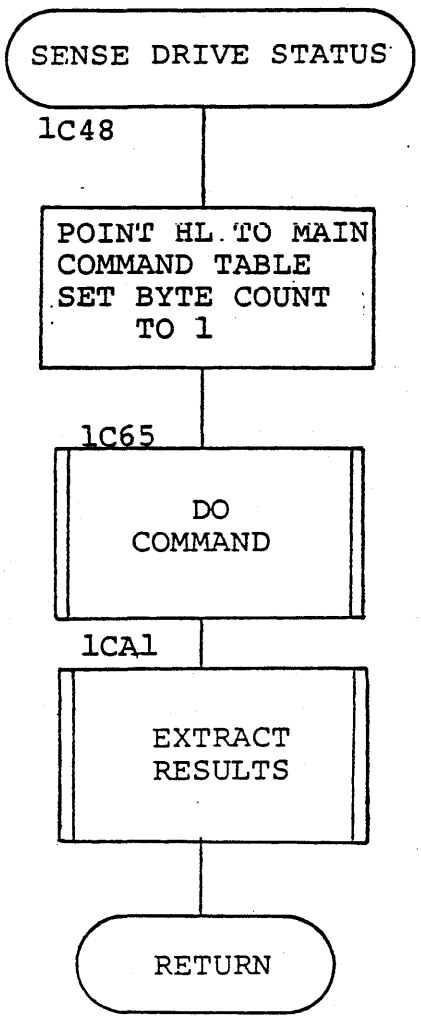


Fig. 4-17, 7387 "Sense Drive Status" Flowchart

SENSE INTERRUPT STATUS

This command is used to determine the cause of an interrupt signal from the FDC.

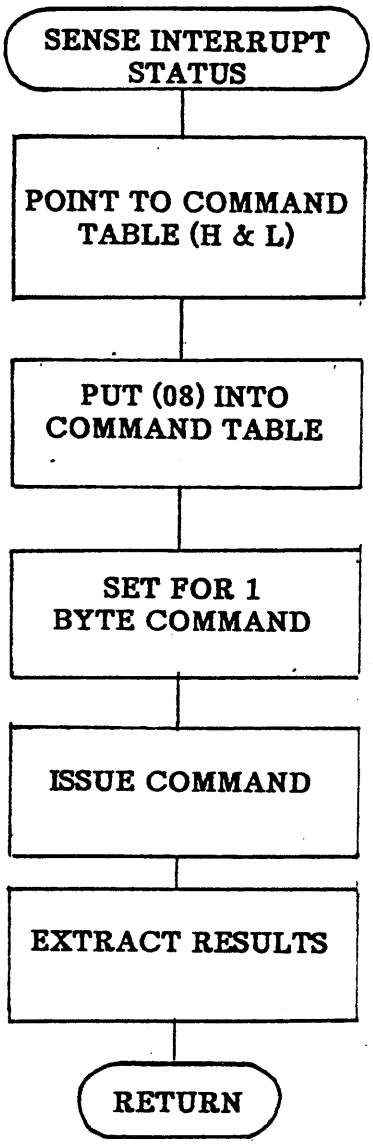
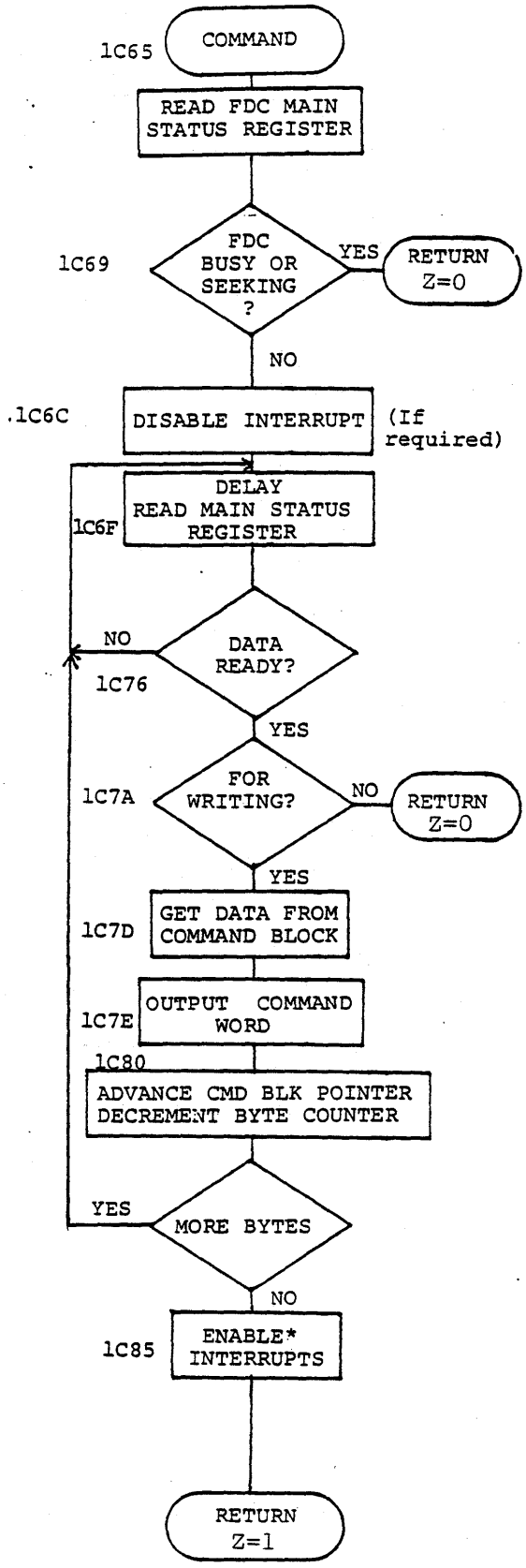


Fig. 4-18, 7387 "Sense Interrupt Status" Flowchart

Registers used H,L,B,A

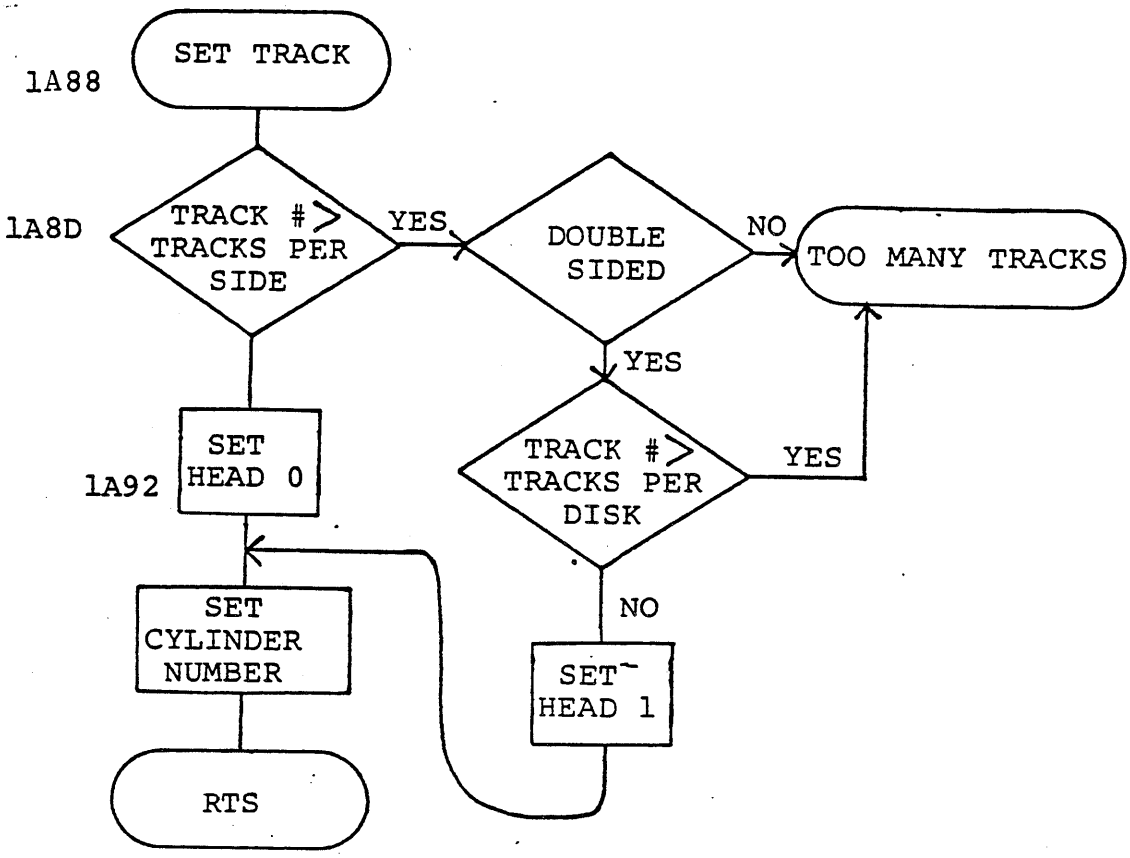


*Do not enable unless enabled when entering command subroutine.

Fig. 4-19, 7387 "Command" Flowchart

(Set Track) This routine allows user to select a particular track for subsequent operations.

Registers used H,L,C,A.



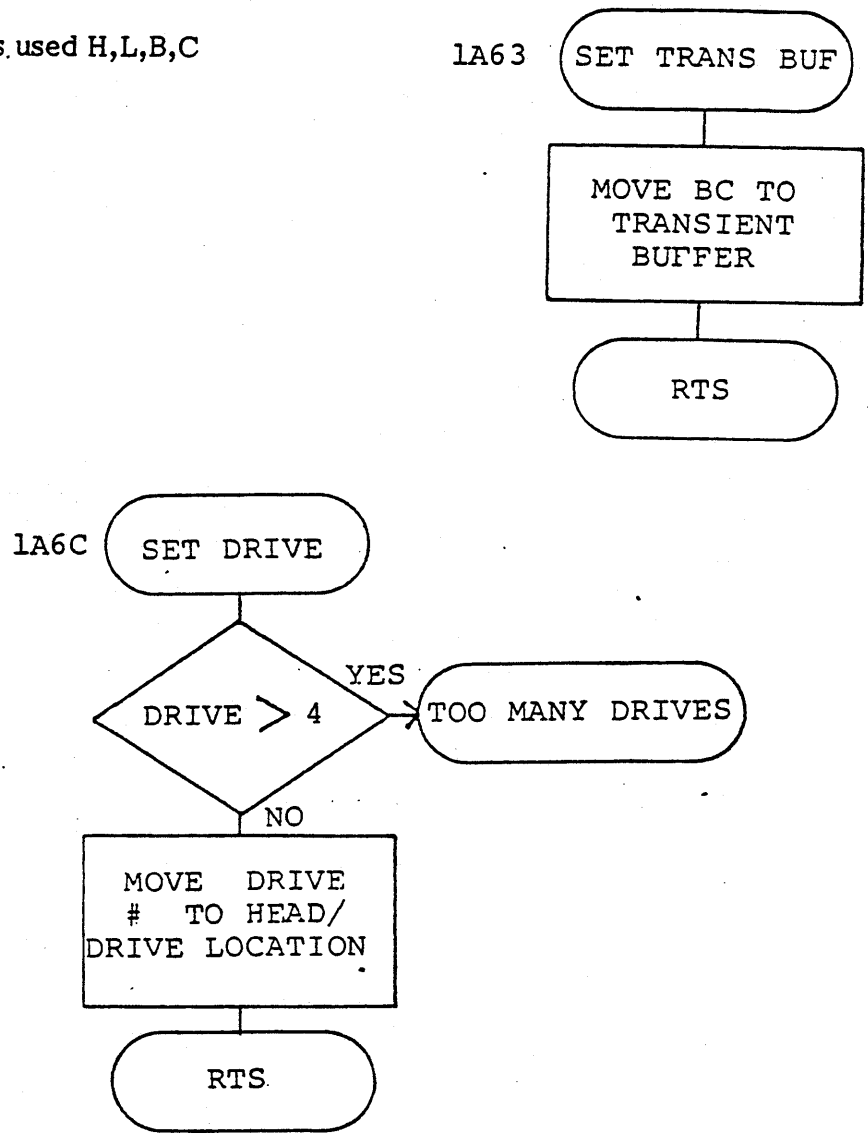
(Too Many Tracks) is a user supplied error handling routine

Fig. 4-20, 7387"Set Track" Flowchart

(Set Trans Buf) This routine allows user to set pointers for RAM data transfer location.

(Set Drive) This routine allows user to select one of four drives for subsequent operations.

Registers used H,L,B,C

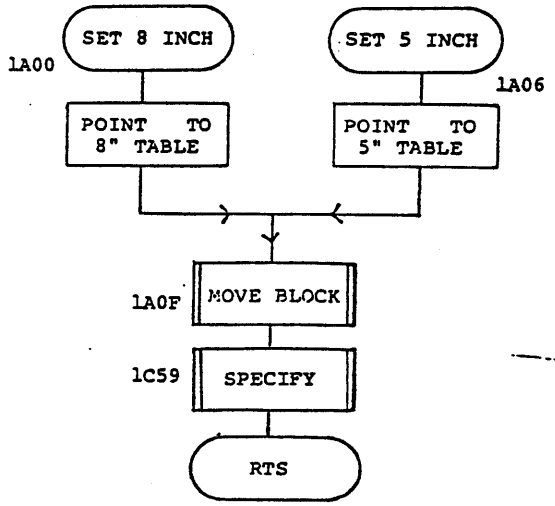


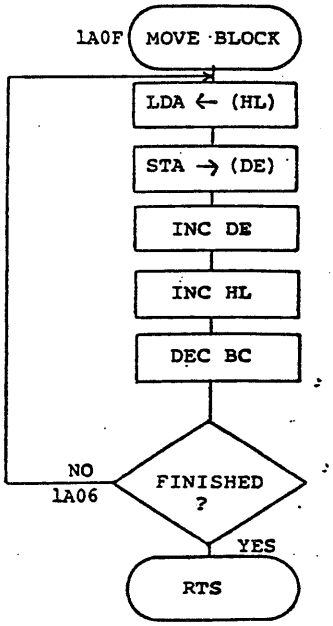
(Too Many Drives) is a user supplied error routine.

Fig. 4-21, 7387 "Set Trans Buf" & "Set Drive" Flowcharts

(Set 8 Inch) This routine sets up the command tables to deal with 8" drives.

(Set 5 Inch) This routine sets up the command tables to deal with 5 1/4" drives.





This routine moves a block of Data.

Before Entering:

HL = from Address

DE = to Address

BC = BYTE Count

Fig. 4-22, 7387 "Set 8"", "Set 5"", & "Move Block" Flowcharts

(Set Sector) This routine allows the user to select a particular sector for subsequent read or write operations.

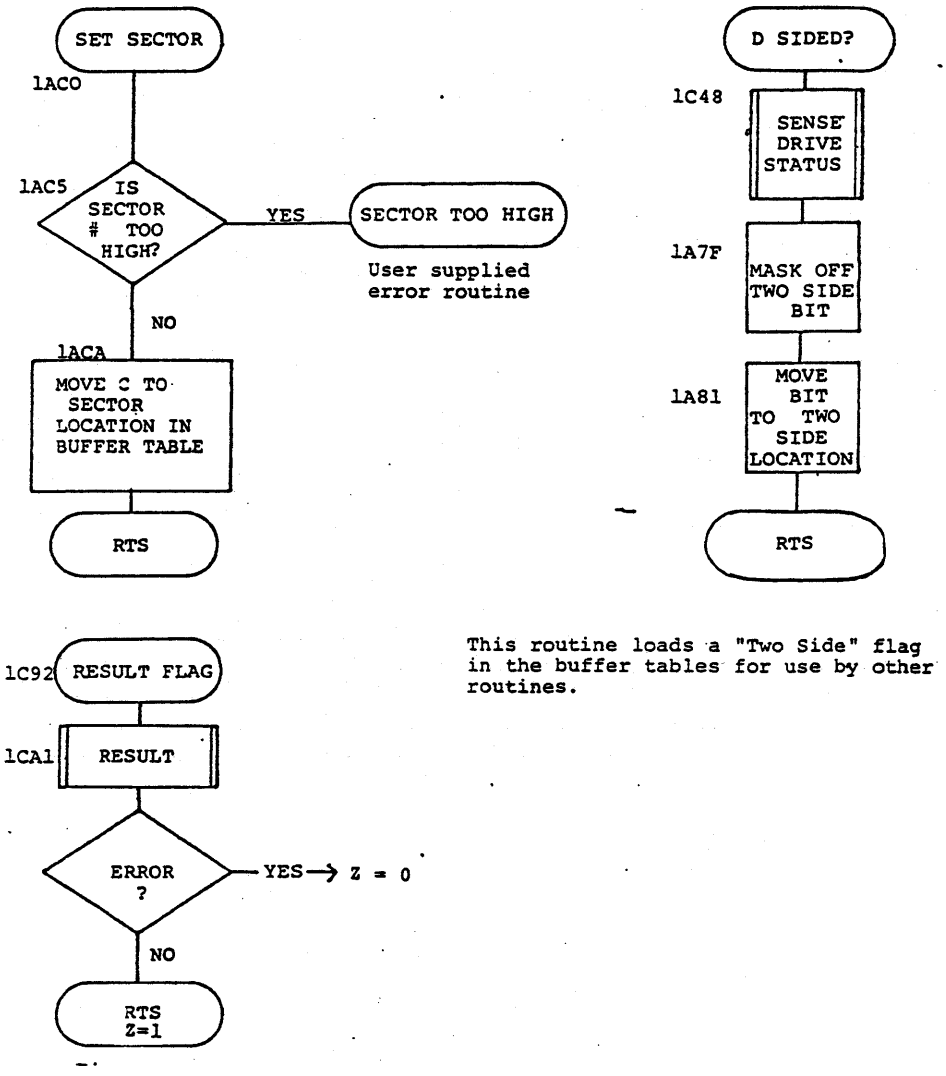


Fig. 4-23, 7387 "Set Sector", "D Sided", & "Result Flag" Flowcharts

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PROGRAM ASSEMBLY FORM

TITLE

DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MODIFIER	COMMENTS
XX	00		RESULT BUFFER		STATUS REG 0	← STATUS 0 EXCEPT AFTER (DRIVE STATUS) THEN STATUS 3
	1				1	STATUS 1
	2				2	STATUS 2
	3				CYLINDER (TRACK)	C
	4				HEAD	HD
	5				SECTOR	R
	6		↓		FORMAT #	N
	7		MAIN COMMAND		COMMAND CODE	
	8		TABLE		HEAD / DRIVE	
	9				CYLINDER (TRACK)	
	A				HEAD	
	B				SECTOR	
	C				N	
	D				EOT	
	E				R/W GPL	
	0F				BYTES / SECTOR	
	10		FORMAT COMMAND		COMMAND CODE	
	1		TABLE		F HEAD / DRIVE	
	2				F N	
	3				F EOT	
	4				F GPL	
	5		↓		DATA	
	6		SPECIFY COMMAND		COMMAND CODE	
	7		TABLE		SRT / HUT	
	8		↓		HLT / ND	
	9		# OF TRACKS		# OF TRACKS	
	A					
	B		DOUBLE/SINGLE*		TWO SIDED ?	
	C		TRABUF		TRABUF LSD	
	D		↓		MSD	
	E					
	1F					
	20					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	2F					
	30					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
XX	3F					

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DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	COMMENTS
1A	00	21	(SET 8 INCH)	LDPI	HL	POINT TO 8" TABLE
	1	20		-	8" TABLE	
	2	1A		-		
	3	C3		JP		
	4	09		-	8 ENTER	
	5	1A		-		
1A	06	21	(SET 5 INCH)	LDPI	HL	POINT TO 5¼" TABLE
	7	40		-	5" TABLE	
	8	1A		-		
1A	09	11	8 ENTER	LDPI	DE	MOVE PARAMETERS TO RESULT. COMMAND TABLE
	A	00		-	RAM TABLE	
	B			-		
	C	01		LDPI	BC	SET BYTE COUNT TO 32 RAM BUFFER LENGTH
	D	20		-	20 BYTE COUNT	
	E	00		-	00	
1A	0F	7E	MOVE BLOCK	LDAN	(HL)	← GET DATA FROM TABLE
	10	12		STAN	(DE)	← LOAD DATA TO RAM
	1	23		ICP	HL	INCREMENT POINTERS
	2	13		ICP	DE	
	3	0B		DCP	BC	← DECREMENT COUNT
	4	78		LDA	B	
	5	B1		ORA	C	CHECK FOR LAST CHARACTER
	6	C2		JP	20	
	7	0F		-	MOVE BLOCK	
	8	1A		-		
	9	CD		JS		INITIALIZE FLOPPY DISK CONTROLLER
	A	59		-	SPECIFY	
	B	1C		-		
	C	C9	——	RTS		RETURN
	D					
	E					
1A	1F					(WRITE, READ, FORMAT) (INTERRUPT SENSE STATUS) (DRIVE SENSE STATUS)
1A	20	FF	RESULT TABLE	8"	ST0	ST0 ST3
	1	FF			ST1	PCN X
	2	FF			ST2	X X
	3	FF			C	X X
	4	FF			H	X X
	5	FF			R	X X
	6	FF	↓	↓	N	X X
	7	FF	COMMAND TABLE		COMMAND CODE	COMMAND TABLE
	8	00			HEAD - DRIVE	
	9	00			C	
	A	00			H	
	B	01			R	
	C	00			N	
	D	1A			EOT	
	E	07			R/W GPL	
	2F	80	↓		BYTES/SECTOR	
	30	0D	FORMAT COMMAND		FORMAT COMMAND	FORMAT COMMAND TABLE
	1	FF			HEAD DRIVE	
	2	00			N	
	3	1A			EOT	
	4	1B			F GPL	
	5	E5	——		DATA	
	6	03	SPECIFY COMMAND		SPECIFY COMMAND	
	7	8F			SRT/HUT	SPECIFY COMMAND TABLE
	8	25			HLT/ND	
	9	4D	——		# OF TRACKS	
	A	FF				RESERVED AREA
	B	00			TWO SIDED?	
	C	FF			TRA BUF	
	D	FF			"	
	E	FF				
1A	3F	FF	——	——		

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HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE READ (WRITE FORMAT)	SENSE DATE (INTERRUPT STATUS)	SENSE (DRIVE STAT.)
							ST0	ST3
1A	40	FF	RESULT TABLE	5¼"	ST0		PCN	X
	1	FF			ST1		X	X
	2	FF			ST2		X	X
	3	FF			C		X	X
	4	FF			H		X	X
	5	FF			R		X	X
	6	FF			N		X	X
	7	FF	COMMAND TABLE		COMMAND CODE	COMMAND TABLE		
	8	00			HEAD - DRIVE			
	9	00			C			
	A	00			H			
	B	01			R			
	C	00			N			
	D	10			EOT			
	E	10			R/W GPL			
	4F	80	↓		BYTES/SECTOR	↓		
	50	00	FORMAT TABLE		FORMAT COMMAND	FORMAT COMMAND TABLE		
	1	FF			HEAD - DRIVE			
	2	00			N			
	3	10			EOT			
	4	19			F GPL			
	5	E5			DATA			
	6	03			SPECIFY COMMAND			
	7	DF			SRT/HUT			
	8	FF			HLT/ND			
	9	22	↓		# OF TRACKS	↓		
	A	FF				RESERVED BYTES		
	B	00			TWO SIDED?			
	C	FF			TRA BUF			
	D	FF			"			
	E	FF				—		
1A	5F	FF	↓	↓		↓		
	60							
	1							
	2							
1A	63	69	(SET TRANS BUF)	LDL	C	← MOVE BC TO TRANSIENT BUFFER LOCATION		
	4	60		LDH	B			
	5	22		STPD	HL			
	6	1C		—	TRA BUF			
	7	XX		—		↓		
	8	C9	——	RTS				
	9							
	A							
	B							
1A	6C	79	(SET DRIVE)	LDA	C	← PUT DRIVE # IN C		
	D	FE		CPAI		← JUMP IF # GREATER THAN 4 DRIVES		
	E	04		—	04			
	6F	D2		JP	CO	*IF MORE THAN 4 DRIVES ARE USED THIS CAN		
	70			—	(TOO MANY DRIVES).	JUMP TO THE SECOND 7387 ROUTINE		
	1			—		↓		
	2	32		STAD		← MOVE DRIVE NUMBER TO HEAD/DRIVE LOCATION		
	3	08		—	08 HEAD/DRIVE			
	4	XX		—	XX	↓		
	5	C9	——	RTS				
	6							
	7							
	8							
1A	79	CD	(D SIDED?)	JS		← GET DRIVE STATUS (FOR 8" ONLY)		
	A	48		—	(SENSE DRIVE STATUS)			
	B	1C		—		↓		
	C	3A		LDAD		← PUT STATUS IN ACCUMULATOR		
	D	00		—	STATUS			
	E	XX		—		↓		
1A	7F	E6		ANAI		← CHECK TWO SIDE FLAG		

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HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
1A	80	08		-	08	
	1	32		STAD		← STORE RESULT
	2	1B		-		
	3	XX		-		
	4	C9	———	RTS		
	5					
	6					
	7					
1A	88	21	(SET TRACK)	LDPI	HL	← LOAD A WITH TRACKS/SIDE
	9	19		-	# OF TRACKS	
	A	XX		-		
	B	7E		LDAN	(HL)	
	C	B9		CPA	C	← JUMP IF C IS GREATER THAN # OF
	D	DA		JP	C1	TRACKS/SIDE (C = NEW TRACK #)
	E	9D		-	OTHER SIDE?	
	8F	1A		-		
	90	2E		LDLI		← SET HEAD BYTE TO HEAD 0
	1	0A		-	HEAD	
	2	36		LDMI		
	3	00		-	00	
	4	2E		LDLI		← SET HEAD BIT TO HEAD 0
	5	08		-	HEAD/DRIVE	
	6	7E		LDAN	(HL)	
	7	E6		ANAI		← MASK OFF HEAD BIT LEAVE
	8	03		-	03	← DRIVE #
1A	99	77	OUT TRACK	STAN	(HL)	← STORE HEAD/DRIVE #
	A	23		ICP	HL	← STORE CYLINDER # (TRACK)
	B	71		STCN	(HL)	
	C	C9	———	RTS		
1A	9D	C3	OTHER SIDE?	JP	UN	← CHECK "TWO-SIDED" LINE FROM
	E	79		-	(D SIDED?)	- DISK DRIVE
	9F	1A		-		
	A0	00		NOP		
	1	CA		JP	Z1	← JUMP IF NOT A TWO-SIDED DISKETTE
	2	—		-	TOO MANY TRACKS	(USER SUPPLIED ERROR
	3	—		-		ROUTINE)
	4	2E		LDLI		
	5	19		-	# OF TRACKS	
	6	79		LDA	C	← PUT TRACK # IN A
	7	96		SUA	M(HL)	← SUBTRACT # OF TRACKS PER SIDE
	8	3D		DCA		← 1 → 45 = 0 → 44
	9	4F		LDC	A	← PUT CYLINDER # IN C
	A	7E		LDAN	(HL)	← LOAD # OF TRACKS PER SIDE
	B	B9		CPA	C	← JUMP IF TOO MANY TRACKS
	C	DA		JP	C1	
	D			-	TOO MANY TRACKS	*USER SUPPLIED ERROR ROUTINE
	E			-		
	AF	00		NOP		
	B0	2E		LDLI		SET HEAD BYTE TO HEAD 1
	1	0A		-	HEAD	
	2	36		LDMI		
	3	01		-	01	
	4	2E		LDLI		← SET HEAD BIT TO HEAD 1
	5	08		-	HEAD/DRIVE	
	6	7E		LDAN	(HL)	
	7	F6		ORAI		
	8	04		-	04	
	9	C3		JP		STORE HEAD - DRIVE INFORMATION
	A	99		-	OUT TRACK	
	B	1A	———	-		
	C					
	D					
	E					
1A	BF					

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
1A	C0	21	(SET SECTOR)	LDPI	HL	← GET MAX SECTOR #
	1	0D		–	EOT	
	2			–		
	3	7E		LDAN	(HL)	↓
	4	B9		CPA	C	← JUMP IF SECTOR IS TOO HIGH
	5	DA		JP	C1	C = SECTOR #
	6			–	(SECTOR TOO HIGH)	(USER SUPPLIED ERROR ROUTINE)
	7			–		↓
	8	2B		DCP	HL	← STORE SECTOR #
	9	2B		DCP	HL	
	A	71		STCN	(HL)	↓
	B	C9	———	RTS		
	C					
	D					
	E					
1A	CF	CD	(READ SECTOR)	JS		← MOVE HEAD TO PROPER LOCATION
	0	19		–	(SEEK)	
	1	1C		–		↓
	2	2A		LDPD	HL	← POINT DE TO THE ADDRESS CONTAINED
	3	1C		–	TRA BUF	IN TRA BUF
	4			–		
	5	EB		XCP	HL, DE	↓
	6	00		NOP		
	7	21		LDPI	HL	← SET C REGISTER TO # OF BYTES/SECTOR
	8	0F		–	BYTES, SECTOR	
	9			–		
	A	4E		LDCN	(HL)	↓
	B	21		LDPI	HL	← PUT READ COMMAND IN COMMAND TABLE
	C	07		–	COMMAND TABLE	
	D			–		
	E	36		LDMI	(HL)	
1A	DF	26		–	26	↓
1A	E0	00		NOP		
	1	06		LDBI		← SET COUNT FOR 9 COMMAND BYTES
	2	09		–	09	
	3	CD		JS		← SEND COMMAND TO FDC
	4	65		–	(COMMAND)	
	5	1C		–		
1A	E6	DB	READ LOOP	IPA		← WAIT FOR RQM
	7	C4		–	MAIN STATUS	
	8	17		RLAC		
	9	D2		JP	C0	
	A	E6		–	READ LOOP	
	B	1A		–		
	C	17		RLAC		← GET RESULT INFO. IF THERE'S AN ERROR
	D	17		RLAC		
	E	D2		JP	C0	
	EF	FB		–	GET RESULT	
	F0	1A		–		
	1	DB		IPA		← INPUT ONE DATA BYTE
	2	C5		–	DATA	↓
	3	12		STAN	(DE)	← STORE
	4	13		ICP	DE	← INC POINTER
	5	0D		DCC		← DEC COUNTER
	6	C2		JP	Z0	← GO GET NEXT CHARACTER IF NOT FINISHED
	7	E6		–	READ LOOP	
	8	1A		–		
	9	D3		OPA		← SEND TERMINAL COUNT WHEN FINISHED
	A	C4		–	TC	
1A	FB	CD	GET RESULT	JS		← GET EXECUTION RESULTS + SET FAIL FLAG
	C	92		–	(RESULT FLAG)	
	D	1C		–		↓
	E	C9		RTS		← RETURNS Z=1 PASS Z=0 FAIL
1A	FF					

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HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / DATE / COMMENTS
1B	00	CD	(WRITE SECTOR)	JS		- MOVE HEAD TO PROPER POSITION
	1	19		—	(SEEK)	
	2	1C		—		↓
	3	2A		LDPD	HL	- POINT DE TO THE ADDRESS CONTAINED
	4	1C		—	TRA BUF	IN TRA BUF
	5	XX		—		
	6	EB		XCP	HL, DE	↓
	7	21		LDPI	H'L	- SET REGISTER C =TO# OF BYTES PER SECTOR
	8	0F		—	BYTES/SECTOR	
	9	XX		—		
	A	4E		LDCN	(HL)	↓
	B	21		LDPI	HL	- PUT WRITE COMMAND IN TABLE
	C	07		—	COMMAND TABLE	
	D	XX		—		
	E	36		LDMI	(HL)	
	0F	05		—	05	↓
	10	06		LDBI		- SET COMMAND BYTE COUNT TO 9
	1	09		—	09	↓
	2	CD		JS		- SEND COMMAND TO FDC
	3	65		—	(COMMAND)	
	4	1C		—		↓
1B	15	DB	WRITE LOOP	IPA		- WAIT FOR RQM
	6	C4		—	MAIN STATUS	
	7	17		RLAC		
	8	D2		JP	C0	
	9	15		—	WRITE LOOP	
	A	1B		—		↓
	B	17		RLAC		- FETCH RESULT INFO. IF THERE'S AN ERROR
	C	DA		JP	C1	
	D	29		—	FETCH RESULT	
	E	1B		—		↓
1B	1F	1A		LDAN	(DE)	- GET DATA BYTE + SEND TO FDC
1B	20	D3		OPA		↓
	1	C5		—	DATA	↓
	2	13		ICP	DE	← INC POINTER
	3	0D		DCC		← DEC COUNTER
	4	C2		JP	Z0	- GO SEND NEXT BYTE IF NOT FINISHED
	5	15		—	WRITE LOOP	
	6	1B		—		↓
	7	D3		OPA		- SEND TERMINAL COUNT WHEN FINISHED
	8	C4		—	TC	↓
1B	29	CD	FETCH RESULT	JS		- GET EXECUTION RESULTS + SET FAIL FLAG
	A	92		—	(RESULT FLAG)	
	B	1C		—		↓
	C	C9	———	RTS		← RETURNS Z=1 PASS Z=0 FAIL
	D					
1B	2E	CD	(FORMAT)	JS		- SPECIFY HEAD LOAD + UNLOAD TIMES
	2F	59		—	(SPECIFY)	
	30	1C		—		↓
	1	CD		JS		- MOVE HEAD TO TRACK 0
	2	00		—	(RECALIBRATE)	
	3	1C		—		↓
	4	3A		LDAD		- GET HEAD DRIVE INFORMATION
	5	08		—	HEAD/DRIVE	
	6	XX		—		↓
	7	32		STAD		- PUT HEAD DRIVE INFORMATION IN FORMAT TABLE
	8	11		—	F HEAD/DRIVE	COMMAND TABLE
	9	XX		—		↓
	A	CD		JS		- FORMAT ONE SIDE
	B	54		—	(FORMAT SIDE)	
	C	1B		—		↓
	D	C0		RTS	Z0	← RETURN IF FAILED
	E	3A		LDAD		- CHECK FOR DOUBLE SIDED
1B	3F	1B		—	TWO SIDED?	

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

TITLE

DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	COMMENTS
1B	40			-		
	1	A7		ORA	A	
	2	C8		RTS	Z1	← RETURN IF ONE SIDED
	3	21		LDPI	HL	SET POINTER TO HEAD DRIVE LOCATION
	4	08		-	HEAD/DRIVE	
	5			-		
	6	7E		LDAN	(HL)	SET TO HEAD 1
	7	F6		ORAI		
	8	04		-	04	
	9	77		STAN	(HL)	
	A	32		STAD		
	B	11		-	F HEAD/DRIVE	
	C	XX		-		
	D	CD		JS		FORMAT OTHER SIDE
	E	54		-	(FORMAT SIDE)	
	4F	1B		-		
	50	C9	———	RTS		
	1					
	2					
	3					
1B	54	3E	(FORMAT SIDE)	LDAI		CYLINDER 0 (TRACK 0)
	5	00		-	00	(H,L,D,E,B,C,A)
	6	32		STAD		STORE IN CYLINDER NUMBER LOCATION
	7	09		-	CYLINDER (TRACK)	
	8			-		
1B	59	CD	SIDE LOOP	JS		MOVE HEAD TO CYLINDER (TRACK)
	A	19		-	SEEK	
	B	1C		-		
	C	CD		JS		FORMAT ONE TRACK
	D	72		-	(FORMAT TRACK)	
	E	1B		-		
1B	5F	C0		RTS	Z0	← RETURN Z = 0 FOR FAIL
1B	60	21		LDPI	HL	
	1	09		-	CYLINDER (TRACK)	
	2			-		
	3	7E		LDAN	(HL)	INCREMENT CYLINDER NUMBER
	4	34		ICM	(HL)	
	5	00		NOP		
	6	2E		LDLI		LOOP UNTIL LAST SECTOR
	7	19	0	-	# OF TRACKS	
	8	00		NOP		
	9	BE		CPA	M	
	A	DA		JP	C1	
	B	59		-	SIDE LOOP	
	C	1B		-		
	D	AF		CLAC		
	E	C9	———	RTS		← RETURN Z = 1 IF PASS
	6F					
	70					
	1					
1B	72	CD	(FORMAT TRACK)	JS		GENERATE FORMAT DATA TABLE
	3	97		-	(FORM TABLES)	
	4	1B		-		
	5	21		LDPI	HL	POINT TO FORMAT COMMAND TABLE
	6	10		-	FORMAT CMD TABLE	
	7			-		
	8	06		LDBI		6 COMMAND BYTES
	9	06		-	06	
	A	CD		JS		SEND COMMAND TO EDC
	B	65		-	(COMMAND)	
	C	1C		-		
1B	7D	DB	TRACK LOOP	IPA		WAIT FOR RQM
	E	C4		-	MAIN STATUS	
1B	7F	17		RLAC		

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / DATE / COMMENTS
1B	80	D2		JP	C0	
	1	7D		—	TRACK LOOP	
	2	1B		—		
	3	17		RLAC		EXTRACT RESULTS IF THERE'S AN ERROR
	4	DA		JP	C1	
	5	91		—	EXTRACT RESULTS	
	6	1B		—		
	7	1A		LDAN	(DE)	OUT PUT DATA BYTE
	8	D3		OPA		
	9	C5		—	DATA	
	A	13		ICP	DE	← INC POINTER
	B	0D		DCC		← DEC COUNTER
	C	C2		JP	ZO	LOOP UNTIL ALL CHARACTERS ARE SENT
	D	7D		—	TRACK LOOP	
	E	1B		—		
	8F	D3		OPA		SEND TERMINAL COUNT
	90	C4		—	TC	
1B	91	CD	EXTRACT RESULT	JS		EXTRACT RESULTS
	2	92		—	(RESULT FLAG)	STORE IN RESULT TABLE
	3	1C		—		
	4	C9	———	RTS		← RETURNS Z=1 PASS Z=0 FAIL
	5					
	6					
1B	97	21	(FORM TABLES)	LDPI	HL	GET HEAD DRIVE INFO (LEAVE HEAD #)
	8	08		—	HEAD / DRIVE	
	9			—		(H, C, D, E, B, C, A)
	A	7E		LDAN	(HL)	
	B	E6		ANAI		MASK OUT DRIVE INFO
	C	04		—	04	
	D	OF		RRA		PUT HEAD # IN B BIT 0
	E	OF		RRA		
1B	9F	47		LDB	A	
1B	A0	23		ICP	HL	GET CYLINDER # PUT IN C
	1	4E		LDCN	(HL)	
	2	2A		LDPD	HL	POINT TO START OF FORMAT DATA TABLE
	3	1C		—	TRA BUF	
	4			—		
	5	11		LDPI	DE	POINT TO START SECTOR TABLE
	6	DO		—	SECTOR TABLE	
	7	1B		—		
1B	A8	71	TABLE LOOP	STCN	(HL)	← PUT CYLINDER # (C) IN TABLE
	9	23		ICP	HL	← INC POINTER
	A	70		STBN	(HL)	← PUT HEAD # (H) IN TABLE
	B	23		ICP	HL	← INC POINTER
	C	1A		LDAN	(DE)	← LOAD SECTOR NUMBER
	D	77		STAN	(HL)	← PUT SECTOR # (R) IN TABLE
	E	23		ICP	HL	← INC POINTER
	AF	3A		LDAD		PUT BYTES PER SECTOR CODE (N) IN TABLE
	B0	∝		—	N	
	1			—		
	2	77		STAN	(HL)	
	3	23		ICP	HL	← INC POINTER
	4	13		ICP	DE	
	5	3A		LDAD		LOOP UNTIL TABLE IS FINISHED
	6	OD		—	EOT	LOAD A WITH LAST SECTOR #
	7			—		
	8	C6		ADAI		ADD SECTOR TABLE ADDRESS TO SECTOR # TO
	9	DO		—	SECTOR TABLE	GET LAST LOCATION IN TABLE BY ADDING
	A	00		NOP		FIRST ADDRESS OF SECTOR TABLE TO LAST
	B	BB		CPA	E	← COMPARE A WITH ADDRESS IN E
	C	D2		JP	C0	LOOP UNTIL A = E
	D	A8		—	TABLE LOOP	
	E	1B		—		
1B	BF	ZA		LDPD	HL	POINT TO START OF FORMAT DATA TABLE

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL			MNEMONIC			TITLE / DATE / COMMENTS
PAGE ADR	LINE ADR	INSTR	LABEL	INSTR	MODIFIER	
1B	C0	1C		-	TRA BUF	
	1			-		
	2	EB		XCP	DE, HL	
	3	3A		LDAD		PUT # OF SECTORS TIMES 4 IN C REGISTER
	4	0D		-	EOT	SET A WITH LAST SECTOR #
	5			-		
	6	B7		CLC		MULTIPLY A TIMES 4
	7	17		RLAC		
	8	B7		CLC		
	9	17		RLAC		
	A	4F		LDC	A	PUT NUMBER IN C REGISTER
	B	C9	———	RTS		
	C					
	D					
	E					
	CF					
1B	D0	01	SECTOR TABLE	1		
	1	02		2		THE SECTOR TABLE WILL BE USED IN
	2	03		3		SEQUENTIAL ORDER IF SECTOR SKEWING
	3	04		4		IS DESIRED USER CAN REARRANGE ORDER
	4	05		5		OF SECTORS ON DISK
	5	06		6		
	6	07		7		
	7	08		8		
	8	09		9		
	9	0A		A		
	A	0B		B		
	B	0C		C		
	C	0D		D		
	D	0E		E		
	E	0F		F		
1B	DF	10		10		
1B	E0	11		11		
	1	12		12		
	2	13		13		
	3	14		14		
	4	15		15		
	5	16		16		
	6	17		17		
	7	18		18		
	8	19		19		
	9	1A		1A		
	A					
	B					
	C					
	D					
	E					
	EF					
	F0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
1B	FF					

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

TITLE

DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
IC	00	21	(RECALIBRATE)	LDPI	HL	POINT TO HEAD DRIVE # (H,L,B,A)
	1	08		-	HEAD / DRIVE	
	2			-		
	3	7E		LDAN	(HL)	SET TO HEAD 0
	4	E6		ANAI		
	5	03		-	03	
	6	77		STAN	(HL)	
	7	2B		DCP	HL	← POINT TO COMMAND TABLE
	8	36		LDMI	(HL)	PUT RECAL CODE IN TABLE
	9	07		-	07	
	A	06		LDBI		SET B FOR 2 BYTES
	B	02		-	02	
	C	CD		JS		SEND COMMAND
	D	65		-	(COMMAND)	
	E	IC		-		
	0F	CD		JS		WAIT FOR COMPLETION
	10	C8		-	(WAIT FOR INT)	
	1	IC		-		
	2	CD		JS		GET STATUS
	3	37		-	(SENSE INTR STATUS)	
	4	IC		-		
	5	C9	———	RTS		
	6					
	7					
	8					
IC	19	21	(SEEK)	LDPI	HL	MOVE HEAD TO PROPER POSITION (H,L,B,A
	A	07		-	MAIN COMMAND	SET POINTER TO COMMAND TABLE
	B			-	TABLE	
	C	36		LDMI	(HL)	PUT COMMAND IN TABLE
	D	0F		-	0F	
	E	06		LDBI		SET NUMBER OF BITES
IC	1F	03		-	03	
IC	20	CD		JS		SEND COMMAND TO FDC
	1	65		-	(COMMAND)	
	2	IC		-		
	3	CD		JS		WAIT FOR INTERRUPT
	4	C8		-	(WAIT INTR)	(FDC INTERRUPTS WHEN SEEK IS FINISHED)
	5	IC		-		
	6	CD		JS		TERMINATE SEEK COMMAND
	7	37		-	(SENSE INTR STATUS)	
	8	IC		-		
	9	C0	———	RTS	Z0	← RETURN IF FAIL Z = 0
	A	3A		LDAD		LOAD STATUS
	B	00		-	STATUS REG 0	
	C			-		
	D	2F		CMAL		← COMPLIMENT FLAGS
	E	E6		ANAI		CHECK SEEK # FLAG
	2F	20		-	20	
	30	C8		RTS	Z1	← RETURN Z = 1 FOR PASS
	1	3E		LDAI		
	2	01		-	01	
	3	C9	———	RTS		← RETURN Z = 0 FOR FAIL
	4					
	5					
	6					
IC	37	21	(SENSE INTR STATUS)	LDPI	HL	POINT TO COMMAND TABLE (H,L,B,A)
	8	07		-	MAIN COMMAND	
	9			-	TABLE	
	A	36		LDMI	(HL)	PUT CODE IN TABLE
	B	08		-	08	
	C	06		LDBI		SET B FOR . BYTE
	D	01		-	01	
	E	CD		JS		SEND COMMAND
IC	3F	65		-	(COMMAND)	

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PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	TITLE / DATE / COMMENTS
IC	40	IC		-		
	1	CD		JS		GET RESULTS & SECTOR CLEAR FAIL FLAG
	2	92		-	(RESULT FLAG)	
	3	IC		-		
	4	C9	———	RTS		
	5					
	6					
	7					
IC	48	21	(SENSE DRIVE STATUS)	LDPI	H,L	POINT TO COMMAND TABLE (H,L, B,A
	9	07		-	MAIN COMMAND	
	A			-	TABLE	
	B	36		LDMI	(HL)	PUT SENSE DRIVE STATUS CODE IN TABLE
	C	04		-	04	
	D	06		LDBI		SEND COMMAND
	E	02		-	02	
	4F	CD		JS		
	50	65		-	(COMMAND)	GET RESULT
	1	IC		-		
	2	CD		JS		
	3	A1		-	(RESULT)	
	4	IC		-		
	5	C9	———	RTS		
	6					
	7					
	8					
IC	59	21	(SPECIFY)	LDPI	HL	POINT TO SPECIFY TABLE (H,L(B,A)
	A	16		-	SPECIFY COMMAND	
	B			-	TABLE	
	C	06		LDBI		SET B FOR 3 BYTES
	D	03		-	03	
	E	CD		JS		SEND SPECIFY BYTES
IC	5F	65		-	(COMMAND)	
IC	60	IC		-		
	1	C9	———	RTS		
	2					
	3					
	4					
IC	65	DB	(COMMAND)	IPA		GET STATUS INFO (H,L,B,A)
	6	C4		-	MAIN STATUS REG	
	7	E6		ANAI		RETURN WITH Z=0 IF BUSY
	8	10		-	10	
	9	C2		JP	20	
	A	8A		-	ERROR C	
	B	IC		-		
	C	F3		DIN		← DISABLE INTERRUPT
IC	6D	3E	NOT YET	LDAI		DELAY
	E	10		-	10	
	6F	3D	⚠	DCA		
	70	C2		JP	20	
	1	6F		-	⚠	
	2	IC		-		
	3	DB		IPA		GET STATUS INFO
	4	C4		-	MAIN STATUS REG	
	5	17		RALC		WAIT FOR NOT BUSY
	6	D2		JP	C0	
	7	6D		-	NOT YET	
	8	IC		-		
	9	17		RLAC		RETUEN WITH CARRY SET IF READ (FDC→µP)
	A	DA		JP	C1	
	B	8A		-	ERROR C	
	C	IC		-		
	D	7E		LDAN	HL	SEND BYTE
	E	D3		OPA		
IC	7F	C5		-	DATA	

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

TITLE _____ DATE _____

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	COMMENTS
1C	80	23		ICP	HL	← INCREMENT POINTER
	1	05		DCB		⊢ LOOP UNTIL ALL CHARACTERS SENT
	2	C2		JP	20	
	3	6D		–	NOT YET	
	4	1C		–		
	5	00		NOP		← ENABLE INTERRUPT (OPTIONAL)
	6	00		NOP		
	7	00		NOP		
	8	AF		CLAC		⊢ RETURN Z = 1 IF PASS
	9	C9	———	RTS		
1C	8A	00	ERROR C	NOP		(A)
	B	3E		LDAI		⊢ RETURN Z = 0 IF FAIL
	C	01		–	01	
	D	A7		ORA	A	
	E	C9	———	RTS		
	8F					
	90					
	1					
1C	92	CD	(RESULT FLAG)	JS		⊢ GET RESULTS (H,C,B,A
	3	A1		–	(RESULT)	
	4	1C		–		
	5	C0		RTS	Z=0	
	6	3A		LDAD		CHECK ERROR
	7	00		–	STATUS REG 0	
	8			–		
	9	E6		ANAI		
	A	D0		–	D0	
	B	C8		RTS	Z1	RETURN IF PASS ACC=0 Z=1
	C	3E		LDAI		
	D	01		–	01	
	E	C9	———	RTS		– RETURN IF FAIL ACC=1 Z=0
1C	9F					
1C	A0					
1C	A1	21	(RESULT)	LDPD	HL	⊢ INPUT POINTER (H,L,B,A)
	2	00		–	RESULT BUFFER	
	3			–		
	4	0E		LDCI		⊢ SET COUNT TO ZERO
	5	00		–	00	
1C	A6	3E	MORE	LDAI		⊢ DELAY
	7	10		–	10	
1C	A8	3D	△	DCA		
	9	C2		JP	20	
	A	AB		–	△	
	B	1C		–		
1C	AC	DB	NOT READY	IPA		⊢ INPUT STATUS
	D	C4		–	MAIN STATUS REG	
	E	47		LDB	A	
	AF	E6		ANAI		⊢ RETURN IF NOT BUSY WITH CARRY CLEAR
	B0	10		–	10	(FINISHED) A=0 Z=1
	1	C8	—	RTS	Z1	
	2	78		LDA	B	⊢ WAIT FOR RQM
	3	17		RLAC		
	4	D2		JP	C0	
	5	AC		–	NOT READY	
	6	1C		–		
	7	17		RLAC		⊢ JUMP IF READ
	8	D2		JP	C0	
	9	8A		–	ERROR C	
	A	1C		–		
	B	00		NOP		⊢ RETURN WITH CARRY SET IF WRITE (ER
	C	00		NOP		
1C	BD	DB	RD DATA	IPA		⊢ INPUT STATUS BYTE
	E	C5		–	DATA	
1C	BF	77		STAN	(HL)	← PUT STATUS IN RESULT TABLE

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PROGRAM ASSEMBLY FORM

TITLE

DATE

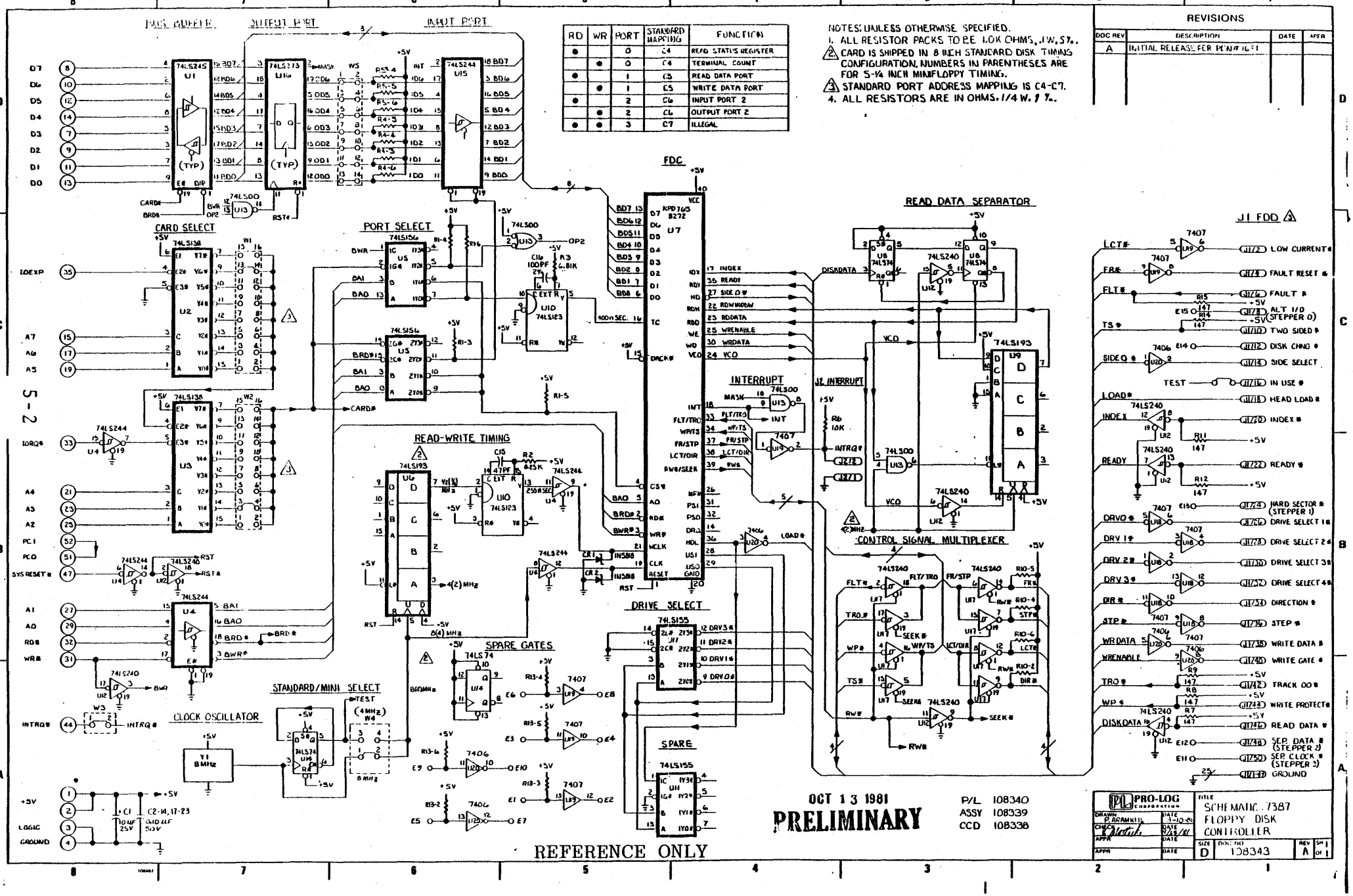
HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	COMMENTS
1C	C0	23		ICP	HL	←INCREMENT POINTER
	1	0C		ICC		←INCREMENT COUNT
	2	C3		JP	UN	← GO GET NEXT BYTE
	3	A6		-	MORE	
	4	1C	———	-		
	5					
	6					← INPUT INTERRUPT STATE
	7					
1C	C8	DB	(WAIT INT)	IPA		← CHECK INTERRUPT BIT (A)
	9	C6		-	C6	
	A	E6		ANAI		← WAIT FOR INTERRUPT
	B	80		-	80	
	C	CA		JP	Z1	
	D	C8		-	(WAIT INT)	
	E	1C		-		
	CF	C9	———	RTS		
	D0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
1C	DF					
1C	E0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	EF					
	F0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
1C	FF					

SECTION 5
Maintenance

Reference Drawings

The schematic (Fig. 5-1) and assembly drawing (Fig. 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. They may differ in some respects from the card and documentation that the user receives from Pro-Log.

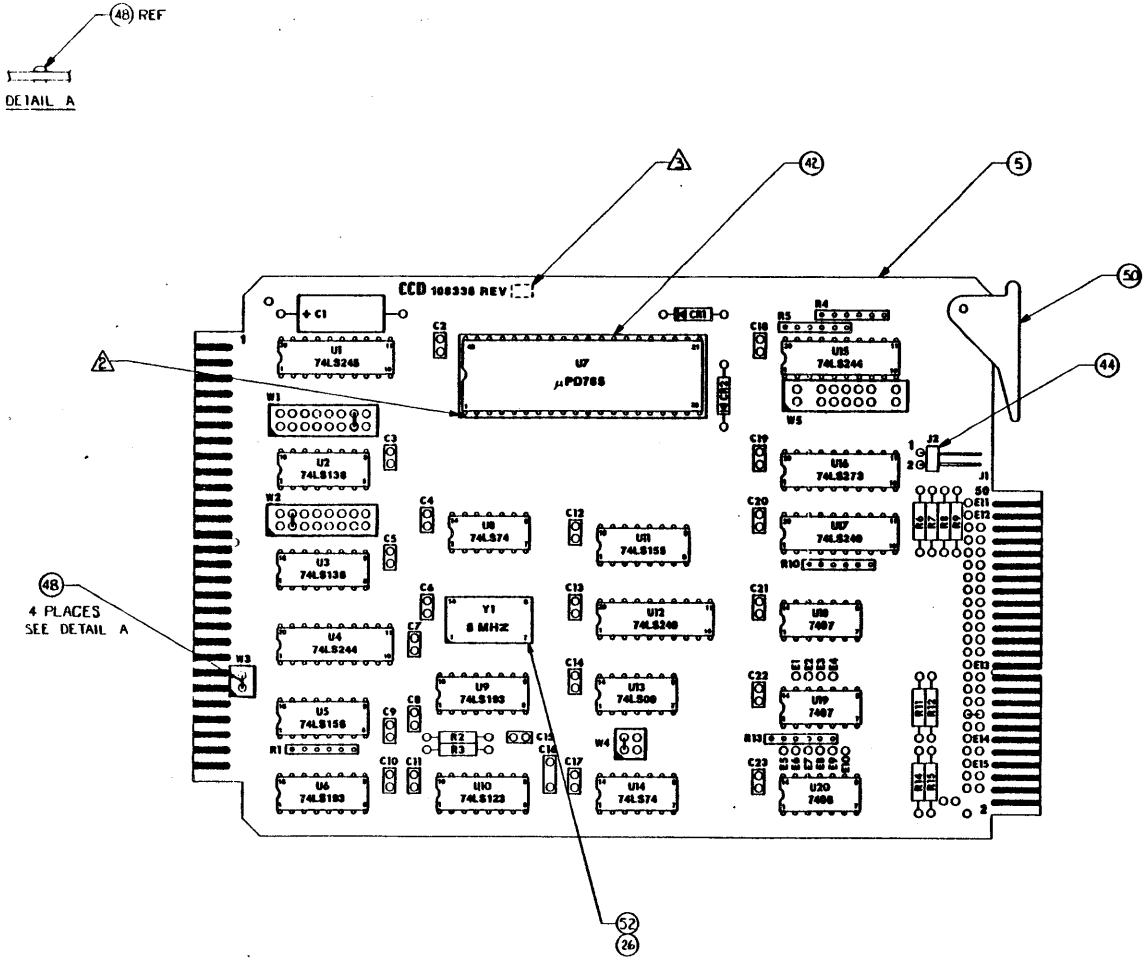
The schematic and the assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.



RD	WR	PORT	STANDARD MAPPING	FUNCTION
●		0	C4	READ STATUS REGISTER
	●	0	C4	TERMINAL COUNT
●		1	C5	READ DATA PORT
	●	1	C5	WRITE DATA PORT
●		2	C6	INPUT PORT 2
	●	2	C6	OUTPUT PORT 2
●	●	3	C7	ILLEGAL

DOC REV	DESCRIPTION	DATE	APPR
A	INITIAL RELEASE PER PCN #6371		

Fig. 5-1, 7387 Schematic



REVISION				
	A	INITIAL RELEASE PER PCN # 1054		

NOTES: UNLESS OTHERWISE SPECIFIED.

1. REF. DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND MAY NOT APPEAR ON ACTUAL PART.
2. DENOTES PIN 1 OF IC SOCKETS.
3. IDENTIFY WITH CCD REV LETTER USING RUBBER STAMP.
4. BOARD TO CONFORM WITH ASSEMBLY STANDARDS AS1004.

OCT 13 1981

OCT 13 1981

PRELIMINARY

ITEM	DESCRIPTION	REF DESIGNATION
26	8.0 MHZ	Y1
20	IN5818	CR1,2
19		
18	10K, 1/4W, CF, 5%	R6
17	8.25K, 1/4W, MF, 1%	R2
16	6.81K, 1/4W, MF, 1%	R3
15	147Ω, 1/4W, MF, 1%	R7,8,9,11,12,14,15
14	1.0K, NETWORK	R1,4,5,10,13
13		
12		
11	.1μF, 50V	C2-14,17-23
10	100pF, 500V, 2%	C16
9	47pF, 50V	C15
8	10μF, 25V	C1
7		
6		
5	108341	PWB

CCD	108338	PRO-LOG CORPORATION	
SCHEMATIC	108343		
PARTS LIST	108340		
Gene Pippa 8 4 81		ASSY, 7387 FLOPPY DISK CONTROLLER	
		D 108339 REV A SHT 1 OF 1	

101357

Fig. 5-2, 7387 Assembly

Return for Repair Procedures

Domestic Customers:

1. Call our factory direct at (408) 372-4593, and ask for CUSTOMER SERVICE.

2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, reason for return, and the name and telephone number of the person we should contact (preferably the user), if we have any further questions.

4. Package the equipment in a solid cardboard box secured with packing material.

   CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, CA 93940

   Reference CRO # _____.

International Customers:

Equipment repair is handled by your local Pro-Log Distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty:

Seller warrants that the articles furnished hereunder are free fom defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part, whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

APPENDIX A
Quick Reference

INTRODUCTION

This appendix is a compilation of tables and figures which appear elswhere in the manual. They are presented here for quick access to information you will need to refer to frequently. These figures can also be found at the page number included at the end of the title of each figure, along with additional information.

Port Name	Standard Port Address	Input Output	Description
Main Status Port	C4	Input	Accesses Main Status Register in FDC chip.
Terminate Port	C4	Output	Output to this port causes the Terminal Count pin on the FDC chip to be strobed. Data written out is inconsequential, just the act of writing out to this port generates a 400ns. pulse to the pin.
Read Data Port	C5	Input	During read operations, this port is used to read data out of the FDC. During the Result Phase of a command, this port is used to read the Result bytes out of the FDC.
Write Data Port	C5	Output	During the Command Phase of a command, this port is used to write the Command bytes to the FDC. During write operations, this port is used to write data to the FDC.
Interrupt Status	C6	Input	Bit 7 of this port is used to read the interrupt output of the FDC chip. When the bit is set to 1, the interrupt is active. The other bits are spares.
Interrupt Mask Port	C6	Output	Bit 7 of this port is used to control the interrupt mask. The interrupt is masked after power-up or reset. To Enable the interrupt, set the bit to a one. The mask does not affect the Interrupt Status port's ability to monitor the interrupt output pin of the FDC. The other bits are spares.
	C7	Input	Invalid
	C7	Output	Invalid

Fig. A-1, 7387 Table of I/O Ports (pg 3-5)

Bit	Name	Description
0	FDD 0 BUSY	Bit set means Disk Drive 0 is in the Seek mode. The FDC cannot accept a Read or Write Command while this bit is set.
1	FDD 1 BUSY	Bit set means Disk Drive 1 is in the Seek mode. The FDC cannot accept a Read or Write Command while this bit is set.
2	FDD 2 BUSY	Bit set means Disk Drive 2 is in the Seek mode. The FDC cannot accept a Read or Write Command while this bit is set.
3	FDD 3 BUSY	Bit set means Disk Drive 2 is in the Seek mode. The FDC cannot accept a Read or Write Command while this bit is set.
4	FDC BUSY	Bit set means a Read or Write command is in process. FDC cannot accept any other command.
5	EXECUTION MODE	Bit set means FDC is in the Execution Phase of a command.
6	DATA INPUT/ OUTPUT	Bit set means data transfer should be from Read Data Port to processor. Bit reset means data transfer should be from processor to Write Data Port.
7	REQUEST FOR MASTER	Indicates the FDC is ready for a data transfer between the Read or Write Data Ports and the processor.

Fig. A-2, 7387 FDC Main Status Register (pg. 3-12)

PHASE	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
READ DATA	
Command	MT MF SK 0 0 1 1 0
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
READ DELETED DATA	
Command	MT MF SK 0 1 1 0 0
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
WRITE DATA	
Command	MT MF 0 0 0 1 0 1
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
WRITE DELETED DATA	
Command	MT MF 0 0 1 0 0 1
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code

PHASE	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
READ A TRACK	
Command	0 MF SK 0 0 0 1 0
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	# of Data Bytes to be Transfered
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
READ ID	
Command	0 MF 0 0 1 0 1 0
	X X X X X HD US1 US0
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
FORMAT A TRACK	
Command	0 MF 0 0 1 1 0 1
	X X X X X HD US1 US0
	Bytes/Sector Code
	Sectors/Track
	Length of Gap 3
	Filler Data Byte
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code
SCAN EQUAL	
Command	MT MF SK 1 0 0 0 1
	X X X X X HD US1 US0
	Track #
	Head #
	Sector #
	Bytes/Sector Code
	# of Last Sector
	Length of Gap 3
	Sectors/Step
Execution	
Result	Status Register 0
	Status Register 1
	Status Register 2
	Track #
	Head #
	Sector #
	Bytes/Sector Code

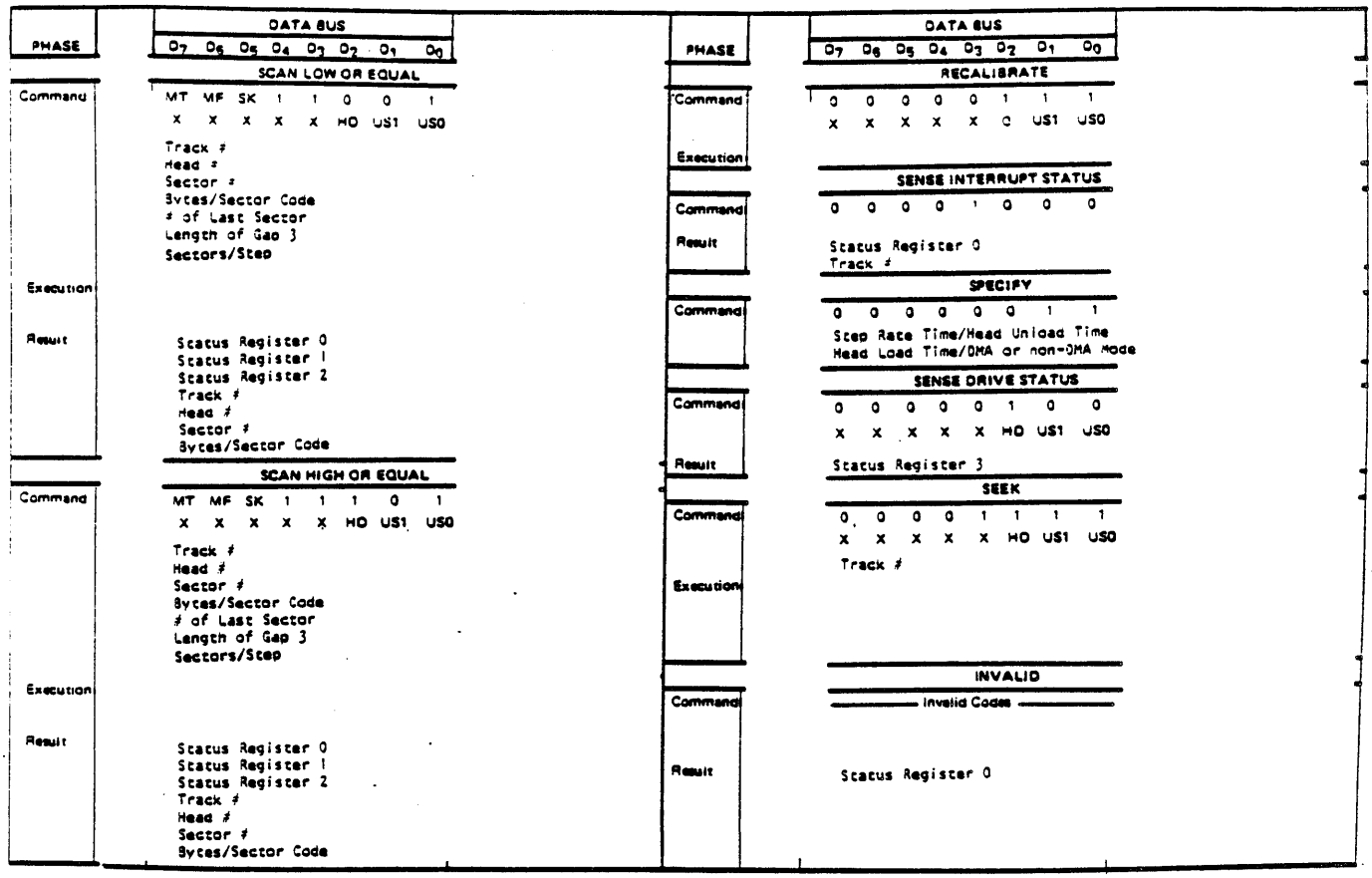


Fig. A-3, 7387 FDC Instruction Set (pg. 3-11)

NAME	DESCRIPTION
MT	If MT is set, a double-sided operation is to be performed. After finishing a Read or Write operation on Side 0, the FDC will automatically start searching for Sector 1 on Side 1.
MF	Selects FM or MFM mode. On 7387 it should always be reset, indicating FM mode.
SK	If SK is set, sectors with Deleted Data Address Masks will be skipped, otherwise the command will terminate.
HD	If reset selects side 0. If set selects side 1.
US1, US0	A two bit binary number indicating the drive to be selected.
TRACK #	Binary number of track to be accessed. Must match the track number in the ID field of the sector to be accessed. As a Result byte, it may be incremented from the number given in the command. For the Read ID command, it is the track number read from the ID field of the first sector encountered.
HEAD #	Number of side to be accessed, 0 or 1. Must match head number in ID field of the sector to be accessed. As a Result byte, its least significant bit may be complemented from the number in the command.
SECTOR #	Number of sector to be accessed. Must match sector number in ID field of sector to be accessed. As a Result byte, it reflects the FDC internal sector counter. For the Read ID command, it is the sector number read from the ID field of the first sector encountered.

Fig. A-4, 7387 Command and Result Bytes (1) (pg. 3-13)

BYTES/ SECTOR CODE	Code indicating the number of bytes per sector. Must match Bytes/Sector Code in ID field of sector to be accessed. However, if you will not be reading all the data from the sector the Bytes/Sector Code should be 00 The last command byte, "# of Data Bytes to be Transferred," then defines the number of bytes transferred. Refer to Fig. 3-12 for the proper code.
# OF LAST SECTOR	The command will end after the sector with this number has been operated on. The number is a binary number. If you are performing a double-sided operation, the sectors operated on will start with the starting sector you specify, read through the sector on side 0 that equals the # of Last Sector, then start reading side 1 at sector 1, and finish when it reads the sector on side 1 equal to the # of Last Sector.
LENGTH OF GAP 3	A binary number specifying the length of Gap 3, which in the IBM 3740 format, is the gap between the end of one sector and the beginning of the next. See Fig. 3-12.
FILLER DATA BYTE	When formatting a track, the entire data field of each sector will be filled with this data byte.
SECTOR/ STEP	During Scan commands, if this byte = 0 consecutive sectors are scanned. If = 1 every other sector is scanned. Scan commands should only be used on one sector per command, so this byte has no real meaning. It is suggested it be set = 0.
SECTOR/ TRACK	A binary number specifying the number of sectors to be placed on a track during the Format a Track command.
STEP RATE TIME	The most significant 4 bits of this byte specify the time delay between step pulses issued to the stepper motor during Seek or Recalibrate commands. The time may vary from 1 to 16ms. in 1ms. increments. F=1ms., 0=16ms.

Fig. A-5, 7387 Command and Result Bytes (2) (pg. 3-14)

HEAD UNLOAD TIME	The least significant 4 bits of this byte specify the length of time the head will remain loaded on the disk after the Execution Phase of an operation has been completed. The time may vary from 16 to 240ms. in 16ms. increments. 1=16ms., F=240ms.
HEAD LOAD TIME	The most significant 7 bits of this byte specify the head settling time. This is the time between the head load signal being issued and the FDC beginning the operation. The time may vary from 2 to 254ms. in 2ms. increments. 01=2ms., 7F=254ms.
DMA OR NON-DMA MODE	The least significant bit of the byte selects the DMA or Non-DMA mode of operation. On the 7387 this bit should always be set to a 1, indicating the Non-DMA mode.

Fig. A-6, 7387 Command and Results Bytes (3) (pg. 3-15)

BIT	NAME	DESCRIPTION
7 AND 6	INTERRUPT CODE	7=0, 6=0 Command was completed without error.
		7=0, 6=1 Command terminated early because of some error.
		7=1, 6=0 Invalid command was issued.
		7=1, 6=1 Command terminated early because the Ready line from the disk drive changed state.
5	SEEK END	When set, this flag indicates a Seek command has been completed.
4	EQUIPMENT CHECK	When set, this flag indicates a Fault signal was received from the disk drive, or no Track 0 signal was received from the disk drive after 77 step pulses had been issued during a Recalibrate command.
3	NOT READY	When set, this flag indicates a command was issued to a disk drive whose Ready line is inactive, or a command was issued to operate on the second side of a single-sided disk.
2	HEAD	This flag indicates whether side 0 or side 1 was selected when the command terminated or an interrupt occurred.
1 AND 0	DRIVE	A two bit binary number indicating the disk drive that the other status flags pertain to.

Fig. A-7, 7387 Status Register 0 (pg. 3-16)

BIT	NAME	DESCRIPTION
7	LAST SECTOR ERROR	During Scan commands, if the FDC is scanning every other sector and it skips over the sector equal to the "# of Last Sector" this flag will be set. Scan commands should only be used on one sector per command, so this bit has no real significance.
6		Not used, this bit is always 0.
5	CRC ERROR	When a CRC error is detected in either the ID Field or the Data Field, this flag is set.
4	OVER RUN	If the processor does not perform a data transfer in time during the Execution Phase of a command, this flag is set.
3		Not used, this bit is always 0.
2	SECTOR NOT FOUND	If the FDC cannot find a sector it is looking for after it has encountered the index hole twice, it sets this flag. For the Read a Track command: If during the course of the command the specified sector was not found, this flag will be set. For the Read ID command: If the FDC cannot read an ID Field without an error, it sets this flag.
1	NOT WRITEABLE	Any time you request data to be written on the disk and the disk is write-protected, this flag is set.
0	MISSING ADDRESS MARK	If the FDC cannot find an ID Address Mark after encountering the index hole twice, or if it cannot find a Data Address Mark or Deleted Data Address Mark for the sector it is trying to operate on, this flag is set.

Fig. A-8, 7387 Status Register 1 (pg. 3-17)

BIT	NAME	DESCRIPTION
7		Not used, this bit is always 0.
6	CONTROL MARK	If a Deleted Data Address Mark is encountered during the Read Data command or during a Scan command, this flag is set. If a Data Address mark is encountered during the Read Deleted Data command, this flag is set.
5	DATA CRC ERROR	If a CRC error is detected in the data field, this flag is set.
4	WRONG TRACK	If the track number read from the ID Field does not agree with the FDC's internal track counter, this flag is set.
3	SCAN HIT	During Scan commands, if the scan was successful, this flag is set.
2	SCAN MISS	During Scan commands, if the scan was not successful, this flag is set.
1	BAD TRACK	If the track number read from the ID Field is FF Hex, this flag is set. In the IBM format, tracks with hard errors are labeled with a track number FF Hex.
0	MISSING DATA FIELD ADDRESS MARK	If the FDC cannot find the Data Address Mark or Deleted Data Address Mark, this flag is set.

Fig. A-9, 7387 Status Register 2 (pg. 3-18)

BIT	NAME	DESCRIPTION
7	FAULT	Indicates the status of the Fault line from the disk drive.
6	WRITE PROTECTED	Indicates the status of the Write-Protected line from the disk drive.
5	READY	Indicates the status of the Ready line from the disk drive.
4	TRACK 0	Indicates the status of the Track 0 line from the disk drive.
3	TWO SIDED	Indicates the status of the Two-Sided line from the disk drive.
2	SIDE SELECT	Indicates the status of the Side-Select line to the disk drive.
1 AND 0	UNIT SELECT	Indicates the status of the Unit Select 1 and Unit Select 0 lines to the disk drive. These should match the drive number specified when the Sense Drive Status command was issued.

Fig. A-10, 7387 Status Register 3 (pg. 3-19)

BYTES/ SECTOR	BYTES/ SECTOR CODE	SECTORS/ TRACK	LENGTH(1) OF GAP 3 R/W	LENGTH(2) OF GAP 3 FORMAT
		8" DISKS		
128	00	26	07	1B
256	01	15	OE	2A
512	02	8	1B	3A
1024	03	4	47	8A
2048	04	2	C8	FF
4096	05	1	C8	FF
		5-1/4" DISKS		
128	00	18	07	09
128	00	16	10	19
256	01	8	18	30
512	02	4	46	87
1024	03	2	C8	FF
2048	04	1	C8	FF

(1) Suggested Hex values for Gap Length 3 for commands other than Format.

(2) Suggested Hex values for Gap Length 3 for Format command.

Fig. A-11, 7387 Bytes/Sector Code and Gap Length 3 Values (pg. 3-20)

Subroutine	Entry Address	Entry Requirements	Previously Run Subroutines
Set 8"	1A00	-	-
Set 5"	1A06	-	-
Recalibrate	1C00	-	Set 8" or Set 5" Set Drive
Set Trans Buf	1A63	Starting Buffer Address in Reg. Pair BC.	-
Set Drive	1A6C	Drive Number in Reg. C	-
Set Track	1A88	Track Number in Reg. C	Set Drive
Set Sector	1AC0	Sector number in Reg. C	-
Format	1B2E	-	Set Trans Buf, Set Drive
Write Sector	1B00	-	Set Trans Buf, Set Drive, Set Track, Set Sector
Read Sector	1ACF	-	Set Trans Buf, Set Drive, Set Track, Set Sector

Comments
Sets Head Load time and other variables for 8" Shugart or equivalent disk drive. This or Set 5" must be used once after reset.
Sets Head Load time and other variables for 5.25" Shugart or equivalent disk drive. This or Set 8" must be used once after reset
Sets the head over Track 0, and sets the FDC track counter to 0. This must be used once for each disk drive after reset.
Defines the starting address of the RAM area you will use for transferring data to and from the disk
Selects the drive to be accessed.
Selects the track to be accessed.
Selects the sector to be accessed.
Formats the entire disk, both sides if double-sided, in the IBM 3740 format. Data byte written into data fields is E5.
Writes a sector of data from the transfer buffer to the disk. Buffer address, drive, track, and sector must be preselected.
Reads a sector of data to the transfer buffer in RAM from the disk. Buffer address, drive, track, and sector must be preselected.

Fig. A-12, 7387 Main Subroutines (pg. 4-5)

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