DISKOS 1070 PRODUCT
SPECIFICATION

INDEX

## FIGURES

# I. INTRODUCTION

## A. Purpose

This specification describes the performance and the physical and electrical characteristics of the PRIAM DISKOS 1070 disc drive. It provides the necessary information to connect a DISKOS 1070 to a disc drive controller through a microprocessor type of interface. This document provides the reference technical specifications required by OEM users. Interface and detailed timing data are not included in the short form of this specification.

## B. General Description

The DISKOS 1070 uses advanced Winchester and microprocessor technologies to provide users with a low-cost disc drive having high capacity and long-term reliability. A stepper motor driven positioner enables the DISKOS 1070 to position Winchester type heads quickly and precisely. These low-force heads assure high data reliability. An advanced 8-inch Winchester-technology disc is driven by a brushless DC motor. The head positioner and carriage, heads, and disc are enclosed in a sealed, contamination-resistant chamber to assure high reliability.

A microprocessor provides interface flexibility and monitors drive operation. For example, it controls the power up and down sequencing and a self-test program checks drive performance during each power up sequence. Any malfunction detected by these tests will prevent drive start-up, reducing the chance of loss of data or damage to the drive.

## C. Features

1. 10 megabytes of mass storage at low cost for small system usage.

2. Advanced Winchester technology discs and heads provide efficient and cost-effective data density.

3. Brushless DC spindle drive motor improves reliability by:

   a. Accelerating and braking the disc quickly, extending disc and head life and improving data reliability.

   b. Elimination of the belts, pulleys, switches and starting capacitors.

   c. Elimination of brushes so that brush wear and noise problems do not occur.

4. Reserved area on disc surface for head landing and takeoff protects data integrity.

5. Package size identical to the "Industry Standard" 8-inch floppy.

6. Light weight--only 20 pounds--reduces cost of installation.

7. Flexible, microprocessor-based interface:

   a. Eliminates handshake protocols, freeing valuable processor time.

   b. Supports daisy-chained drives and overlapping seeks.

   c. Simplifies controller design and allows up to a 25-foot controller cable without the need for additional line drivers and receivers.

8. Microprocessor-controlled self-test protects data and the drive and aids troubleshooting.

9. DC operation permits flexibility of prime power source and ease of battery backup.

10. Skip defect data is stored within the drive, eliminating the need for defect record keeping and manual insertion of data during system integration.

11. VFO/data separator provided.

12. Selectable sector size: 256 to 1024 bytes, for data area (formatted).

Application notes to aid users in design of controllers for the DISKOS 1070 are available upon request.

## II. PRODUCT DESCRIPTION

### A. Operational Specifications

Operational specifications of the DISKOS 1070 disc drive are shown in Table 1 below.

TABLE 1. DISKOS 1070 OPERATIONAL SPECIFICATIONS

| | DISKOS 1070 |
|---|---|
| Capacity (unformatted) | 10.8 Mbytes |
| Bytes per track (unformatted) | 15,000 |
| Bytes per cylinder (unformatted) | 60,000 |
| Bytes per track (formatted) | 11,264 |
| Bytes per cylinder (formatted) | 45,056 |
| Number of cylinders | 190 |
| Single Track Access Time (includes head setting time) | 23 ms |
| Average Track Access Time | 73 ms |
| Maximum Track Access Time | 140 ms |
| Average Rotational Latency Time | 8.4 ms |
| Recording Density | 7,475 BPI |
| Track Density | 180 TPI |
| Data Transfer Rate | 0.9 Mbytes/sec |
| Recording Code | MFM |
| Interface Code | NRZ |
| Start Time | 30 sec |
| Stop Time | 30 sec |

B. Physical Characteristics

The physical characteristics of the DISKOS 1070 disc drive are shown in Table 2 below.

TABLE 2. DISKOS 1070 PHYSICAL CHARACTERISTICS

| CHARACTERISTIC | BASIC DRIVE |
|---|---|
| Height (inches) | 4.62 |
| Width (inches) | 8.55 |
| Depth (inches) | 14.25 |
| Weight (pounds) | 20 |

Mounting attitudes of the drive are as follows:

1. Horizontal: Spindle motor down.

2. Vertical: On edge; positioner motion horizontal.

The physical appearance of the drive is shown in Figure 1.

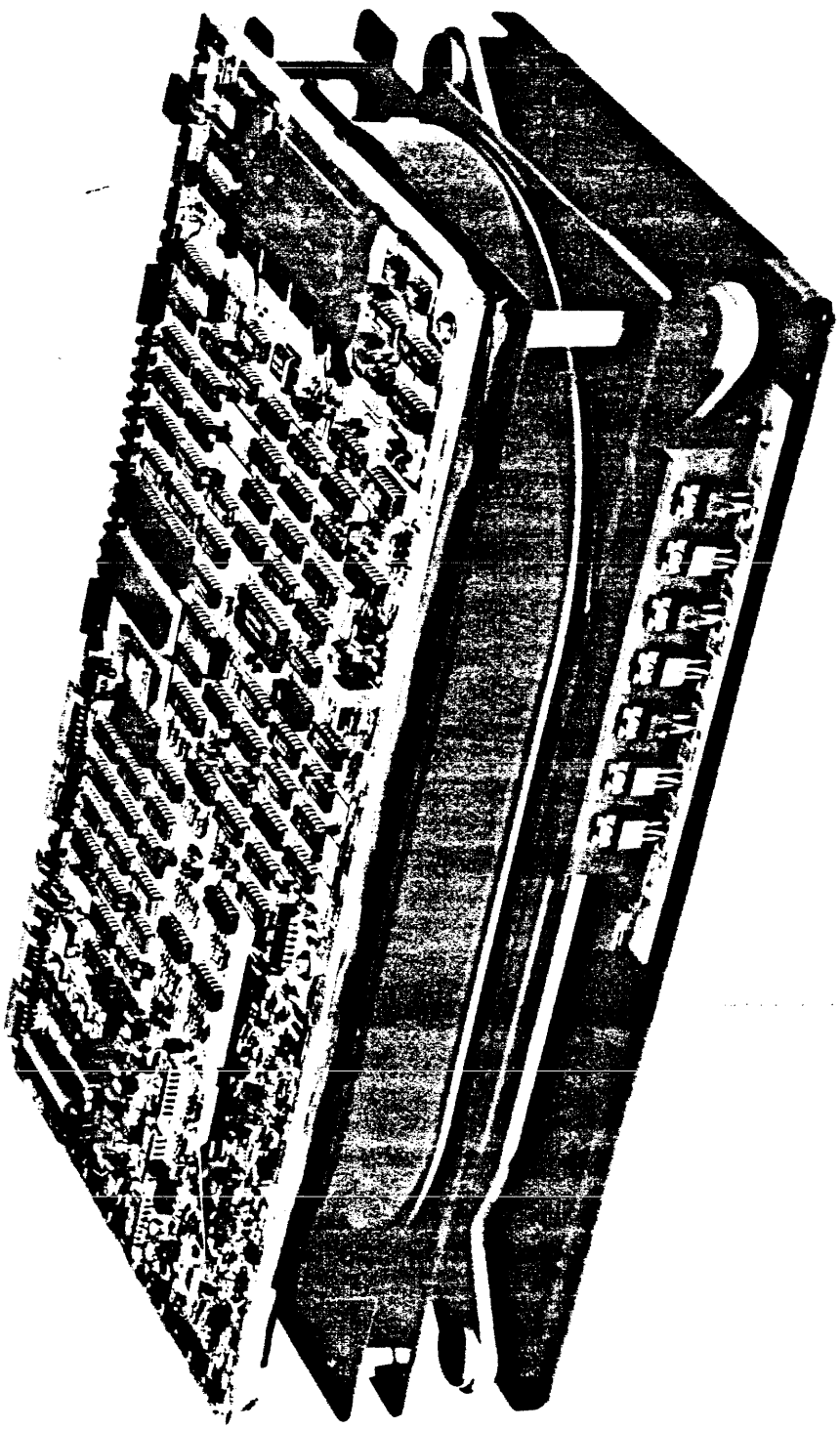


Figure 1. DISKOS 1070 Disc Drive

C. Controls

1. PANELS

The DISKOS 1070 drive is normally supplied without a front panel. There are no front panel controls or indicators.

There is no rear panel. All connections are made directly to the printed circuit board via ribbon cable type connectors.

2. INTERNAL CONTROLS

Mini-dip type switches are provided to select drive address, sector length, and write protect functions, as shown below.

TABLE 3. DISKOS 1070 INTERNAL CONTROLS

| | | |
|---|---|---|
| Switch | DSEL1 | Select Drive Address 1 |
| Switch | DSEL2 | Select Drive Address 2 |
| Switch | DSEL3 | Select Drive Address 3 |
| Switch | DSEL4 | Select Drive Address 4 |
| Switch | WP0 | Write Protect for Head 0 |
| Switch | WP1 | Write Protect for Head 1 |
| Switch | WP2 | Write Protect for Head 2 |
| Switch | WP3 | Write Protect for Head 3 |
| Switch | RSW-1 ON and RSW-2 ON | 44 Sectors per track |
| Switch | RSW-1 OFF and RSW-2 ON | 22 Sectors per track |
| Switch | RSW-1 ON and RSW-2 OFF | 11 Sectors per track |

D. Environmental Characteristics

1. TEMPERATURE

a. Equipment Operational: 10° C to 45° C. (57° F to 113° F)

100 feet per minute air velocity must be maintained through the drive (end to end).

b. Equipment Non-operational: -40° C to 60° C. (-40° F to 140° F)

2. HUMIDITY

a. Equipment Operational: 10% to 80% relative humidity, with a wet bulb temperature limit of 26° C (78° F) without condensation.

b. Equipment Non-operational: 10% to 90% without condensation.

3. ALTITUDE

a. Equipment Operational: From 1000 feet below sea level to 7000 feet above sea level.

b. Equipment Non-operational: From 1000 feet below sea level to 40,000 feet above sea level.

E. Reliability

1. MTBF

The DISKOS 1070 has an expected Mean Time Between Failures (MTBF) of 10,000 power-on hours.

2. MTTR

The DISKOS 1070 is designed so that the Mean Time to Repair (MTTR) is less than 1/2 hour.

3. PREVENTIVE MAINTENANCE

No preventive maintenance is required.

F. Power Requirements

1. DC POWER REQUIREMENTS

The DISKOS 1070 is provided without a power supply and with the standard microprocessor interface, the following power is required from the system:

+24 VDC, $\pm$ 5%,5.1 maximum; ripple 500 mv MAX P-P

+ 5 VDC, $\pm$ 5%,2.5 maximum; ripple 100 mv MAX P-P

-12 VDC, $\pm$ 5%, 0.7A maximum; ripple 150 mv MAX P-P

## III. DATA INTEGRITY

### A. Seek Errors

Seek errors result when the head does not reach the correct track, which can be verified by reading the ID field. Whenever such an error occurs, the drive's track counter must be reset to zero by issuing a RESTORE command to the drive, which will move the head back to cylinder zero. Then a new SEEK command may be issued.

The seek error rate is less than one error in $10^6$ SEEK executions.

### B. Recoverable Data Errors

Recoverable read errors result from transient conditions and are usually corrected by simply re-reading. Errors are normally detected by using cyclic redundancy checking (CRC), performed in the disc drive controller. Each field should be terminated with CRC information.

The recoverable read error rate is less than one error in $10^{10}$ bits.

### C. Non-Recoverable Data Errors

A non-recoverable error is one which persists after several attempts to read the record. This error may be a write error, in which case rewriting the record clears the error. Or, the error may be a disc defect, in which case the error may persist even though the record is rewritten.

The non-recoverable error rate is less than one error in $10^{13}$ bits. Errors that are detected and flagged (either by alternate track or skip defect methods) during initialization are not included in determining this error rate.

### D. Skip Defect

Recorded on each track between index and the first sector pulse is a short data record containing skip defect information. This record contains the addresses of up to three known defects on the addressed track. Each defect is defined by a two-byte binary address of the byte in which the defect is located; zero indicates no defect.

This information is accessed by initiating a read, coincident with the front edge of the index pulse, and reading until the leading edge of the first sector pulse. Use of this technique allows automatic defect mapping and alternate sector allocation, rather than the more commonly used method of providing the user with a written record of the defective areas. The latter method makes it necessary for the user to enter the defective area information manually. A written record is also provided by PRIAM, but it is needed only by customers who wish to retain defect records in their files.

These specifications are subject to change without notice.

## IV. INTERFACE

### A. General

PRIAM offers a basic 8-bit bidirectional bus control interface designed to be readily connected to popular 8-bit and 16-bit microprocessors. Across this interface all spindle motor and head positioning controls are passed.

Read and Write Data is passed via synchronous serial-bit NRZ signal lines. The interface provides for the following synchronization signals; INDEX, SECTOR MARK, READ/REFERENCE CLOCK, and WRITE CLOCK.

Up to four drives may be daisy chained along a single 50 conductor flat ribbon cable. Power is provided via a separate cable.

Each of these interface areas is discussed in the balance of this section in terms of:

1. Address and Command Control
2. Serial Data Transfer
3. Physical Interface

The information contained in the balance of the section is sufficient for the design of a controller for attachment of the DISKOS 1070.

### B. Address and Command Control

All cylinder addresses, status information and commands are transferred over the three-state bidirectional DBUS 0 through 7 lines. These eight lines present an open circuit (tri-state) to the controller's bus until activated by DRIVE SELECT. An active DRIVE SELECT combined with RD (Read) sets the DBUS into the transmit mode while DRIVE SELECT combined with an active WR (Write) sets the DBUS into the receive mode. The information to control the DISKOS 1070 resides in five accessible 8-bit registers. These are:

1. Control Command Register which receives and stores commands from the controller.

2. Target Address Register which Receives the eight bits of the desired cylinder address.

3. Status Register which contains pertinent information about present operation.

4. Current Address Register Lower Byte which contains the eight bits of the current cylinder address or other requested drive parameters.

5. Current Address Register, Upper Byte which is always zero for current address and drive ID information and contains the upper eight bits defining the selected sector size.

Accessing of the registers is accomplished by a combination of active levels on DRIVE SELECT, RD or WR, and register address lines A1 and A0, as shown in Table 4. The Command and Target Address Registers can only receive information and the Status and Current Address Registers can only transmit information.

TABLE 4. REGISTER SELECTION

| A1 | A0 | WR | RD | Selected Register |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | Status Register |
| 0 | 0 | 1 | 0 | Command Register |
| 0 | 1 | 0 | 1 | Current Address, Upper Byte (Used for Sector size reporting |
| 1 | 0 | 0 | 1 | Current Address, Lower Byte |
| 1 | 0 | 1 | 0 | Target Address-Diagnostic Test Select) |

Seven Control Commands are used. All are single byte commands and are listed in Table 5.

TABLE 5. COMMAND SUMMARY

| COMMAND | BITS 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SEQUENCE UP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| SEQUENCE DOWN | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| RESTORE | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| SEEK | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| FAULT RESET | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| READ DRIVE ID | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| READ SELECTED SECTORS SIZE | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

1. SEQUENCE UP

The SEQUENCE UP Command causes the disc drive spindle motor to power up. The rotational speed of the disc is monitored, and when the drive is up to speed, the heads are positioned to cylinder zero. The drive will present BUSY status while the SEQUENCE UP is in process. CYLINDER ZERO, SEEK COMPLETE and READY status is set at the successful completion of this command. WRITE PROTECT and DRIVE FAULT are set if the SEQUENCE UP was unsuccessful.

2. SEQUENCE DOWN

The SEQUENCE DOWN command causes the heads to be positioned to the landing zone and the spindle motor is braked to a stop. WRITE PROTECT status will be set at the completion of this command.

3. RESTORE

The RESTORE command causes the drive carriage to be repositioned to cylinder zero. The drive RESTORES automatically on SEQUENCE UP, or when a SEEK FAULT is detected. Upon failure of the RESTORE command, the heads will be positioned to the landing zone area and DRIVE FAULT status will be set.

4. SEEK

The SEEK command uses the contents of the Target Address Register for desired cylinder address information. Upon receipt of this command, the drive will go NOT READY and BUSY while moving the carriage to the desired cylinder. When this is complete, the drive will again become READY and SEEK COMPLETE status will be posted. Upon failure of the SEEK command, the drive will RESTORE to cylinder zero and present READY, CYLINDER ZERO and SEEK FAULT status.

5. FAULT RESET

The FAULT RESET command clears both fault condition flip-flops (SEEK FAULT and DRIVE FAULT).

6. READ ID

This command sets the Drive ID code (10 hex) in the Current Address Register. READY status will be reset to the not ready state. In order to bring the drive to the READY state a SEQUENCE UP or RESTORE command must be executed. Thus, the Current Address Register contains the valid current cylinder address if the drive is READY and last requested parameter information if not READY.

7. READ BYTES PER SECTOR

This command sets the switch selected number of bytes per sector in the Current Address Registers. There are three possible settings:

1. 340 Bytes per Sector (44 Sectors per Track) Switch RSW-1 ON and RSW-2 ON.

2. 680 Bytes per Sector (22 Sectors per Track) Switch RSW-1 OFF and RSW-2 ON.

3. 1,360 Bytes per Sector (11 Sectors per Track) Switch RSW-1 ON and RSW-2 OFF.

Table 6 is a definition of the various bits in the Current Address Registers and Target Address Register.

TABLE 6. ADDRESS REGISTER BIT DEFINITION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Current Address Reg. Upper Byte | 0 | 0 | 0 | 0 | 0 | $C_{10}$ | $C_9$ | $C_8$ |
| Current Address Reg. Lower Byte | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ |
| Target Address Reg. Lower Byte | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ |

where . . .

| | $C_{10}$ | $C_9$ | $C_8$ | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Cylinder 000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Cylinder 001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| : | | | | | | | | | | | |
| : | | | | | | | | | | | |
| : | | | | | | | | | | | |
| : | | | | | | | | | | | |
| Cylinder 188 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| Cylinder 189 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |

and ....

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Sector Length 340 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Sector Length 680 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| Sector Length 1,316 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

The following is a definition of the various bits of the Status Register.

TABLE 7. STATUS REGISTER BIT DEFINITION

| Bit | Name | Description |
|---|---|---|
| 0 | READY | The drive is up to speed, no fault condition exists and the unit is in a state to read, write, or seek. |
| 1 | SEEK COMPLETE | This bit is set when seek operation is completed. |
| 2 | SEEK FAULT | A fault was detected during a seek operation. |
| 3 | CYLINDER ZERO | Access arm is set to Cylinder 0. |
| 4 | BUSY | Drive is in process of executing a command. |
| 5 | DRIVE FAULT | A fault was detected during a write operation or a drive unsafe condition was detected. |
| 6 | WRITE PROTECT | The head selected is write protected. Write protection is set by a switch on the drive by the WRITE PROTECT command, or when the drive is not sequenced up. |
| 7 | COMMAND REJECT | Control or Register Load command received while drive is not ready, or improper command received. |

The timing and electrical details are described in the Physical Interface part of this section.

C. Serial Data Transfer

Several individual signal lines provide timing and status information to facilitate the serial data transfer between the drive and controller. These signals are:

1. INDEX

A 1.9-microsecond pulse that occurs whenever the mechanical index mark is encountered to indicate the beginning of a track. The timing is discussed in the Physical Interface section.

2. READY

This signal indicates that the selected drive is ready to read, write, or seek. When this line is false, WRITE, READ and SEEK commands should not be initiated by the controller. However, READY will go false whenever a SEEK command is initiated and remain false until the seek is completed, at which time it will become true again.

READY will be true when the drive is at speed, on cylinder and no fault condition exists.

3. SECTOR MARK

SECTOR MARK is a 960 nanosecond pulse that occurs at the beginning of each sector. The sector size is selectable by setting mini-dip type switches on the drive. Two mini-dip switches are provided to select sector length. See Table 8 for switch assignment.

TABLE 8. SECTOR LENGTH SWITCH

| Switch RSW-1 | Switch RSW-2 | Sector Length |
|---|---|---|
| ON | ON | 340 bytes (44 sectors/track) |
| OFF | ON | 680 bytes (22 sectors/track) |
| ON | OFF | 1360 bytes (11 sectors/track) |

4. HEAD SELECT 1, HEAD SELECT 2

These logic level signals are used to select the appropriate head. These signals are low active and gated by DRIVE SELECT.

TABLE 9. HEAD SELECTION

| Head Select 1 | Head Select 2 | Selected Head |
|---|---|---|
| HIGH | HIGH | HEAD ZERO |
| LOW | HIGH | HEAD ONE |
| HIGH | LOW | HEAD TWO |
| LOW | LOW | HEAD THREE |

5. WRITE GATE

WRITE GATE enables data to be written on the disc when in the active state. READY must be valid before signaling WRITE GATE. An attempt to write between trailing edge of INDEX and the leading edge of first SECTOR MARK will be negated because the prerecorded skip defect information is write protected. DRIVE FAULT will be set if any of the following error conditions occur during writing.

TABLE 10. DRIVE FAULT CONDITIONS

1 - WRITE GATE without write current at the head
2 - Write current at the head without WRITE GATE
3 - More than one head selected

Normally, for full sector write, WRITE GATE is activated at the leading edge of SECTOR MARK and terminated with the last byte of the postamble or the leading edge of the next SECTOR MARK or INDEX.

6. WRITE CLOCK

Provides clocking and synchronization for WRITE DATA. WRITE CLOCK is generated by the controller by echoing the REFERENCE CLOCK signal back to the drive through a similar delay path. Thus, it is both frequency and phase locked to WRITE DATA. The timing of these signals is shown in the Physical Interface section.

7. WRITE DATA

Provides the data to be stored on the track. The required format is NRZ (non-return to zero). READ/REFERENCE CLOCK (received from the drive) is used by the controller to clock WRITE DATA on the positive edge. READ/REFERENCE CLOCK is retransmitted back to the drive as WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe WRITE DATA into the drive's encoder circuitry. Detailed timing diagrams are shown in the Physical Interface section.

8. READ GATE

This signal must be enabled in a gap area (all 0's recorded) and at least 8 microseconds before the sync byte. READ GATE enables the VFO clock to synchronize with the information from the read head. Raising READ GATE during a data record may cause the VFO to spuriously lock in incorrect phase relationship for correct decoding of recorded information.

7.5 ± 0.5 microseconds after the leading edge of READ GATE the READ CLOCK is gated to the READ/REFERENCE CLOCK signals.

9. READ/REFERENCE CLOCK

Provides clocking and synchronization for reading and writing data. When READ GATE is not active this signal is the REFERENCE CLOCK which is derived from the crystal oscillator.

7.5 ± 0.5 microseconds after the leading edge of READ GATE, READ/REFERENCE CLOCK is switched to the VFO which is phase locked to READ DATA. A change in the READ/REFERENCE CLOCK phase or a spurious pulse may occur when it is switched between the crystal oscillator and VFO clocks.

10. READ DATA

Data from the drive is in serial bits NRZ (non-return to zero) and is synchronized with READ/REFERENCE CLOCK 7.5 ± 0.5 microseconds after the leading edge of READ GATE. READ DATA may not be valid for the first 8 microseconds after the leading edge of READ GATE.

D. Physical Interface

All drive signal connections are made via a single 50-pin ribbon cable connector J1. A second 50-pin connector, J2, is provided for daisy chaining to another drive or for a terminator attachment at the last drive in the string. Up to four drives may be daisy chained.

Terminator must be installed in connector J2.

A separate connector for DC power is provided.

1. J1 and J2 CONNECTOR

J1 and J2 are a 50-pin ribbon cable connector. The pins are numbered 1 through 50. A recommended mating connector is Spectra-Strip 802-050-004 or Scotchflex 3425-6000.

J1 and J2 Connector

| Pin | Signal |
|---|---|
| 1 | Ground |
| 2 | + DBUS 0 |
| 3 | + DBUS 1 |
| 4 | + DBUS 2 |
| 5 | + DBUS 3 |
| 6 | + DBUS 4 |
| 7 | + DBUS 5 |
| 8 | + DBUS 6 |
| 9 | + DBUS 7 |
| 10 | Ground |
| 11 | - READ GATE |
| 12 | Ground |
| 13 | - RESET |
| 14 | Ground |
| 15 | - WRITE GATE |
| 16 | Ground |
| 17 | - RD |
| 18 | - WR |
| 19 | + AD 1 |
| 20 | + AD 0 |
| 21 | Ground |
| 22 | - DRIVE SELECT 1 |
| 23 | - DRIVE SELECT 2 |
| 24 | - DRIVE SELECT 3 |
| 25 | - DRIVE SELECT 4 |
| 26 | Ground |
| 27 | Ground |
| 28 | + 5 VOLTS DC (TERMINATOR POWER) |
| 29 | Reserved (No connection) |
| 30 | - HEAD SELECT 2 |
| 31 | - HEAD SELECT 1 |
| 32 | Ground |
| 33 | - INDEX |
| 34 | Ground |
| 35 | - READY |
| 36 | Ground |
| 37 | - SECTOR MARK |
| 38 | Ground |
| 39 | + WRITE DATA |
| 40 | - WRITE DATA |
| 41 | Ground |
| 42 | + WRITE CLOCK |
| 43 | - WRITE CLOCK |
| 44 | Ground |
| 45 | + READ/REFERENCE CLOCK |
| 46 | - READ/REFERENCE CLOCK |
| 47 | Ground |
| 48 | + READ DATA |
| 49 | - READ DATA |
| 50 | Ground |

2. J3 CONNECTOR

This connector is used to supply DC power to the drive. J3 is a 6-pin AMP MATE-N-LOK Connector, and the recommended mating connector is an AMP 1-480270-0 socket using AMP 60619-1 pins.

J3 CONNECTOR

| PIN | VOLTAGE |
|---|---|
| 1 | GND |
| 2 | +24 VDC |
| 3 | Not Used |
| 4 | -12 VDC |
| 5 | +5 VDC |
| 6 | GND (+ 24 return) |

3. INTERFACE SIGNALS

Following is an electrical description of each interface signal.

a. +DBUS 0-7

A high active 8-bit wide bus used to transfer commands and status between drive and controller. These lines connect directly to an 8304B (or 8286) bus transceiver as shown in Figure 2.

If long cables are used, these lines should be terminated at each end.

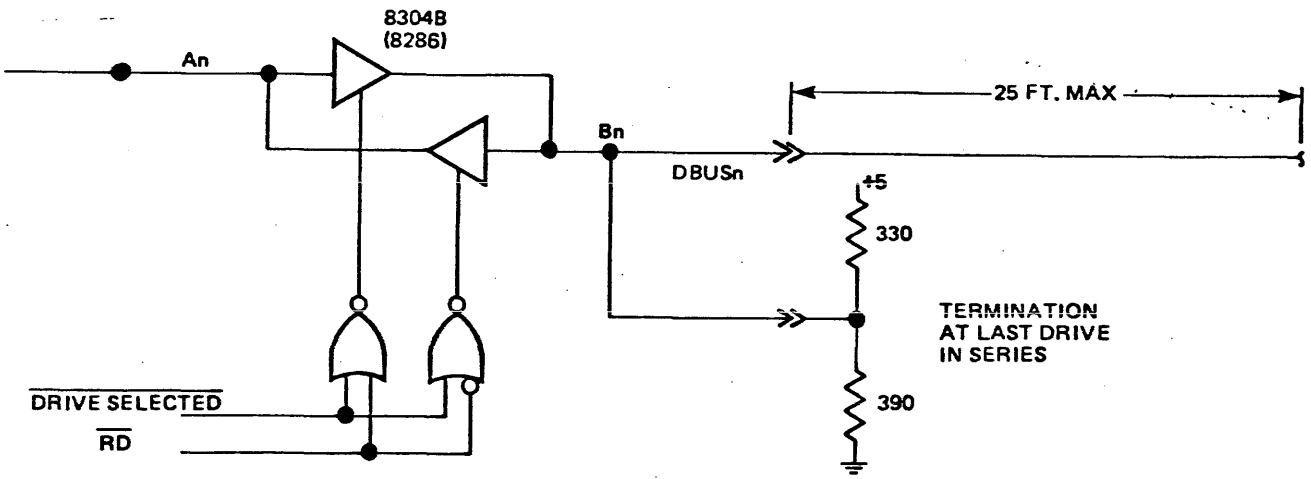



Figure 2. DBUS Transceiver

TABLE 11. DBUS DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Level | | 0.5 | V | $I_{OL}$ = 32 MA |
| $V_{OH}$ | Output High Level | 2.4 | | V | $I_{OH}$ = -5 MA |
| $I_{OFF}$ | Output Off Current | | -0.2 | mA | $V_{OFF}$ = 0.45 V |
| | | | 50 | mA | $V_{OFF}$ = 5.25 V |
| $V_{IL}$ | Input Low Level | | 0.9 | V | |
| $V_{IH}$ | Input High Level | 2.0 | | V | |

b. + AD0-1

A high active 2-bit wide address bus, whose function is to select one of three registers in which data is stored or from which it is read. These lines connect directly to a 74LS244 Schmitt-Triggered Receiver enabled by DRIVE SELECTED as shown in Figure 3.

These lines should be terminated at the drive end. PRIAM provides an optional terminator.

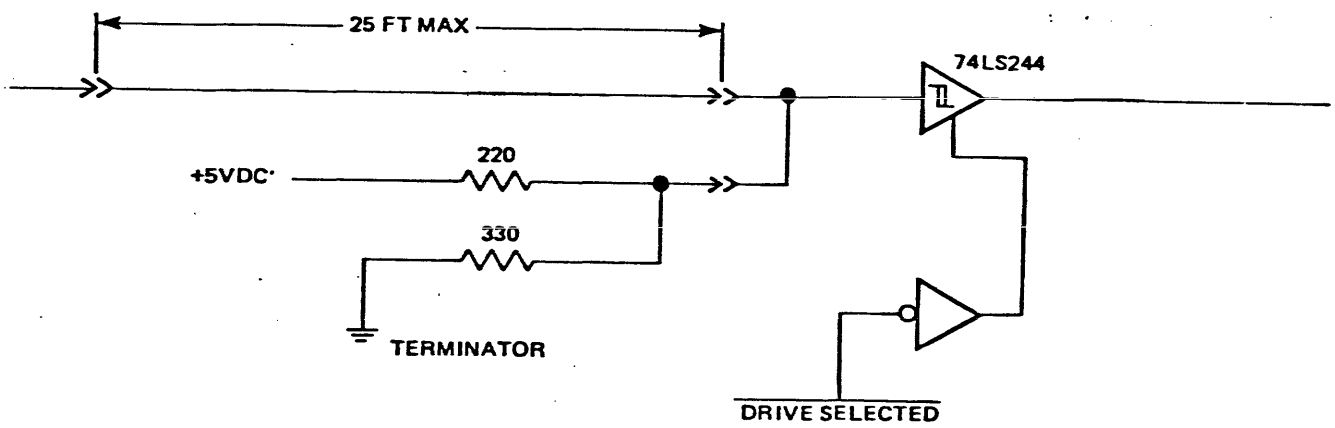



Figure 3. Single Line Receiver Gated By Drive Select

TABLE 12. SINGLE LINE RECEIVER GATED BY DRIVE SELECT
DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | 2 | | V | |
| $V_{IL}$ | Input Low Level | | 0.8 | V | |
| $I_{IH}$ | High Level Input Current | | 0.02 | mA | $V_I$ = 2.7V |
| $I_{IL}$ | Low Level Input Current | | -0.2 | mA | $V_I$ = 0.4V |

c. - RD

This low active signal is used to gate the contents of the selected register (decode of AD1,AD0) onto the DBUS. This line is connected to a 74LS244 as shown in Figure 3. Also, the DC characteristics are listed in Table 12.

Cables should be terminated at the drive end. PRIAM provides an optional terminator as shown in Figure 3.

d. - WR

This low active signal is used to gate the contents of the DBUS into the selected register. This line is connected to a 74LS244 as shown in Figure 3 and its DC characteristics are listed in Table 12.

Cables should be terminated at the drive end. PRIAM provides an optional terminator as shown in Figure 3.

e. - RESET

This low active signal resets the drive logic. If the drive is Sequenced Down when RESET occurs it will remain sequenced down. If the drive is Sequenced Up, the operation is terminated and the drive becomes Sequenced Down. This line is connected to a 74LS244 as shown in Figure 3 and its DC characteristics are listed in Table 12.

Cables should be terminated at the drive as shown in Figure 3.

f. - DRIVE SELECT 1-4

These low active signals enable drive response. No reading, writing, register selection, or command response will occur unless the drive is selected. These single-ended receiver lines are shown in Figure 4. Cables should be terminated as shown in Figure 4.

Long cable connections should be terminated at the drive. See Figure 4.

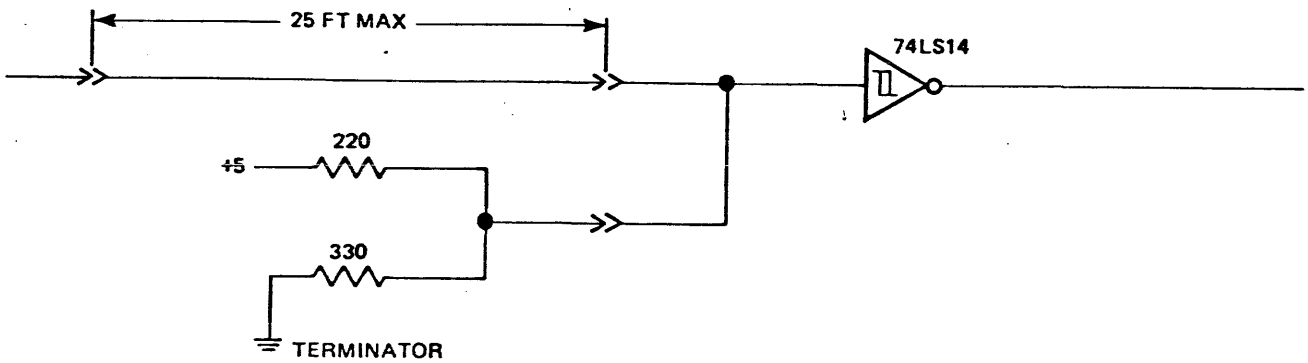



Figure 4. Single End Line Receiver

TABLE 13. SINGLE LINE RECEIVER DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $V_{T+}$ | Positive-going threshold | 1.4 | 1.9 | V | |
| $V_{T-}$ | Negative-going threshold | 0.5 | 1 | V | |
| $I_{IH}$ | High level input current | | .020 | mA | $V_I$ = 2.7V |
| $I_{IL}$ | Low level input current | | -0.400 | mA | $V_I$ = 0.4V |

g. -HEAD SELECT 1-2

These low active signals are used to select the desired head for reading or writing. The head selection decoding is shown in Table 9. These lines are connected to a 74LS14 as shown in Figure 4 and its DC characteristics are listed in Table 13.

Cable connections should be terminated as shown in Figure 3.

h. -READY

This low active signal from the drive indicates that it is up to speed and ready to read, write or seek. It is driven by a 75462 open collector driver as shown in Figure 5.

This line must be terminated at the controller.

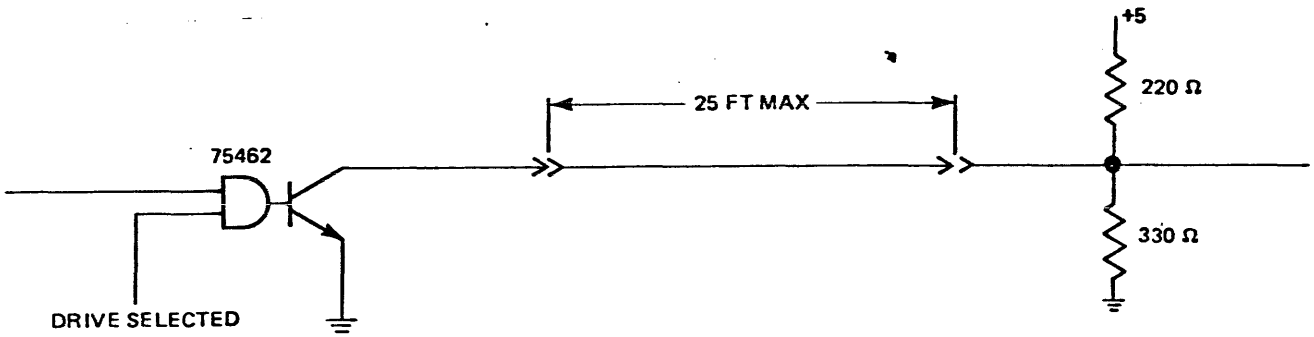



Figure 5. Single Line Driver

TABLE 14. SINGLE LINE DRIVER DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $I_{OH}$ | High level output current | | 0.10 | mA | |
| $I_{OL}$ | Low level output current | 300 | | mA | |
| $V_{OL}$ | Low level output voltage | | 0.8 | V | $I_{OL}$ = 300mA |

i. -INDEX

This low active signal indicates the beginning of a track. The INDEX pulse is 1.9 microseconds wide. It is driven by a 75462 open collector driver as shown in Figure 5 and has the DC characteristics listed in Table 14. This line must be terminated at the controller.

j. -SECTOR MARK

This low active signal indicates the beginning of a sector. The SECTOR MARK pulse is 960 nanoseconds wide. It is driven by a 75462 open collector driver as shown in Figure 5 and has the DC characteristics listed in Table 14. This line must be terminated at the controller.

k. -WRITE GATE

This low active signal enables the writing of data by the selected head. This signal is received by a 74LS244 as shown in Figure 3 and its DC characteristics are listed in Table 12. Cable connections should be terminated at the drive as shown in Figure 3.

l. -READ GATE

This low active signal initiates synchronization of the drive's phase lock loop for data separation. READ GATE must be enabled during a gap. This signal is received by a 74LS244 as shown in Figure 3 and its DC characteristics are listed in Table 12. Long cable connections should be terminated at the drive as shown in Figure 3.

m. +, - WRITE DATA

WRITE DATA is an NRZ serial data signal synchronous with WRITE CLOCK. It is received by a 75116 type differential line receiver section as shown in Figure 6.

The DC characteristics are listed in Table 15. The last drive in a string should be terminated. PRIAM offers an optional terminator.

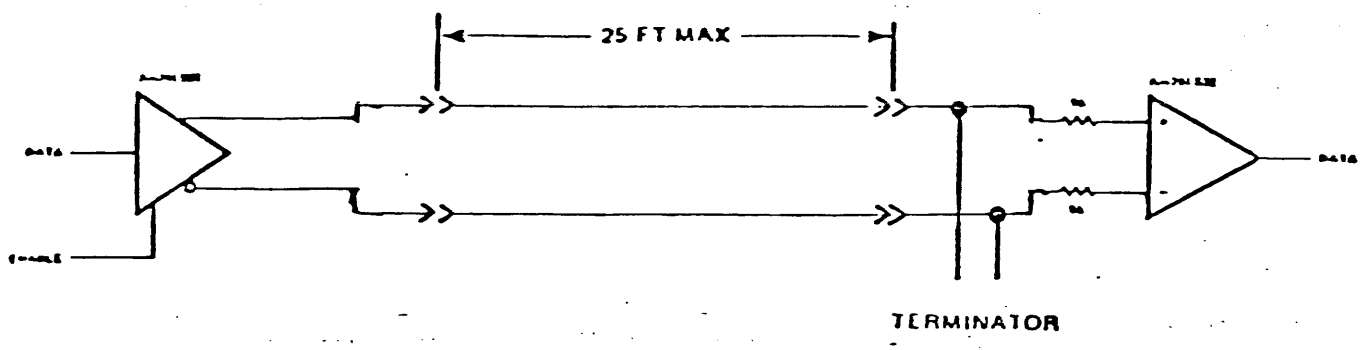



Figure 6. Differential Line Drivers & Receivers

TABLE 15. DIFFERENTIAL LINE RECEIVER DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $V_{TH}$ | Differential input high-threshold | | 0.2 | V | |
| $V_{ICR}$ | Common-mode input range | +15 to -15 | | V | |
| $I_{I(REC)}$ | Receiver input current | | 2.3 | mA | |

n. +, - WRITE CLOCK

This square wave signal from the controller is phase locked to the WRITE DATA. It must be stable from 120 nanoseconds before WRITE GATE and remain stable during WRITE GATE. The nominal period of WRITE CLOCK is 139 nanoseconds. It is received by a 75116 type differential line receiver as shown in Table 15 and Figure 6. These lines should be terminated by the optional terminator.

TABLE 16. DIFFERENTIAL LINE DRIVER DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $V_{OH}$ | High level output voltage | 2.5 | | V | $I_{OH}$ = -20mA |
| $V_{OL}$ | Low level output voltage | | 0.32 | V | $I_{OL}$ = 20mA |
| $I_{OZ}$ | Off-state (non-selected) output current | | $\pm$0.02 | mA | |
| $I_{OH}$ | High-level output current | | -20 | mA | |
| $I_{OL}$ | Low-level output current | | 20 | mA | |
| $I_{OS}$ | Short circuit output current | -30 | -150 | mA | |

o. +, - READ/REFERENCE CLOCK

This square wave signal provides clocking and synchronization for reading and writing data. It is derived from either the crystal oscillator or the VFO synchronized to READ DATA. The nominal period is 139 nanoseconds. It is driven by a 75113 type differential line driver as shown in Figure 6 and its DC characteristics are listed in Table 16.

p. +, - READ DATA

This serial NRZ signal is used to transmit data from the drive to the controller. This output is valid 8 microseconds after READ GATE is enabled. It is driven by a 75113 type differential line driver as shown in Figure 6 and its DC characteristics are listed in Table 16.

In the following section, timing requirements are discussed. Register load timing is shown in Figure 7 and the AC characteristics are listed in Table 17.

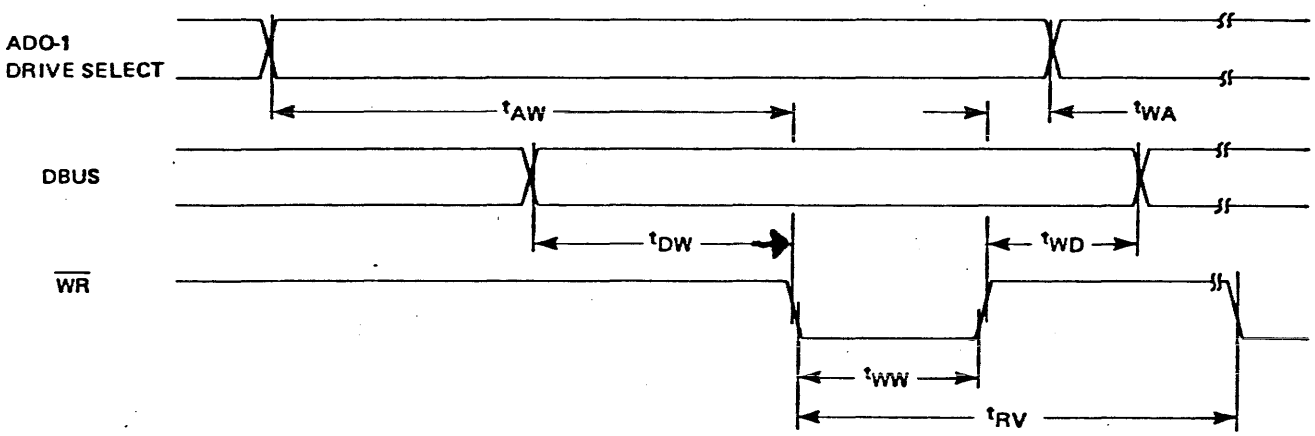



Figure 7. Register Load Timing

TABLE 17. REGISTER LOAD AC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{AW}$ | Address stable before WR | 60 | | ns |
| $t_{WA}$ | Address hold time for WR | 30 | | ns |
| $t_{WW}$ | WR pulse width | 100 | | ns |
| $t_{DW}$ | Data set up time for WR | 60 | | ns |
| $t_{WD}$ | Data hold time for WR | 30 | | ns |
| $t_{RV}$ | Recovery time between WR | 200 | | ns |

Register read timing is shown in Figure 8 and the AC characteristics are listed in Table 18.

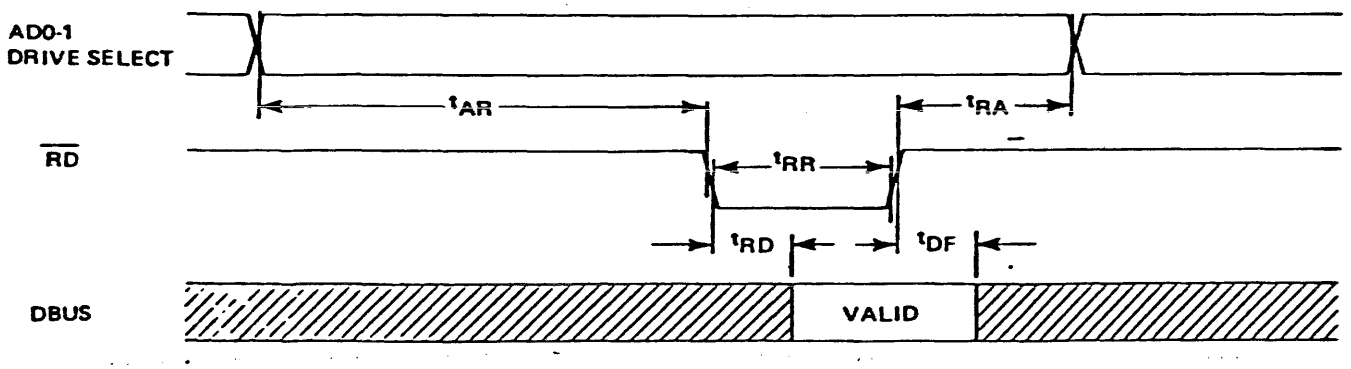



Figure 8. Register Read Timing

TABLE 18. REGISTER READ AC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{AR}$ | Address stable before RD | 60 | | ns |
| $t_{RA}$ | Address hold time for RD | 30 | | ns |
| $t_{RR}$ | RD pulse width | 100 | | ns |
| $t_{RD}$ | Data delay from RD | | 60 | ns |
| $t_{DF}$ | RD to data floating | 10 | 40 | ns |

RESET timing is shown in Figure 9 and the AC characteristics are listed in Table 19.

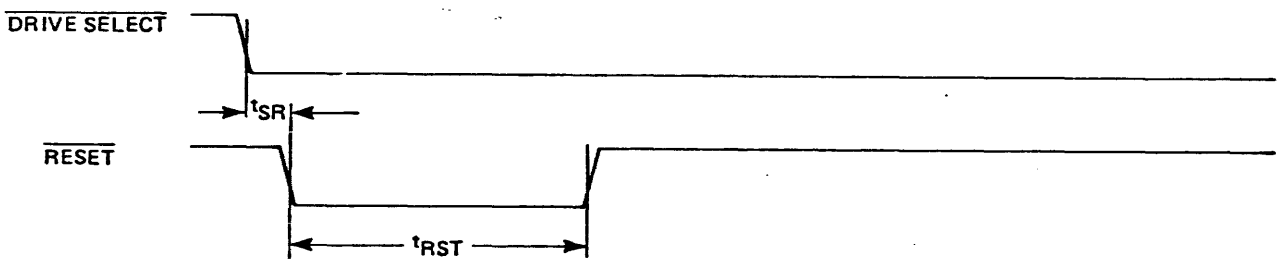



Figure 9. Reset Pulse Width Timing

TABLE 19. RESET AC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{RST}$ | Reset pulse width | 100 | | ms |
| $t_{SR}$ | DRIVE SELECT to RESET | 0 | | ns |

INDEX and SECTOR MARK timing are shown in Figure 10 and their AC characteristics are listed in Table 20.

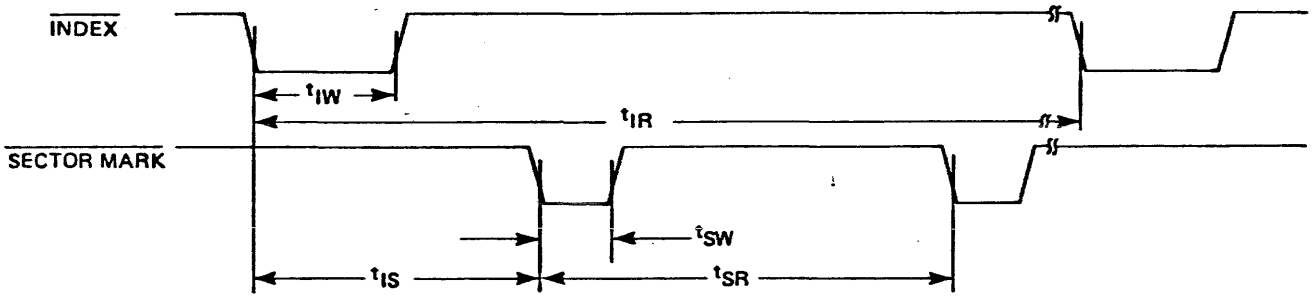



Figure 10. INDEX and SECTOR MARK Timing

TABLE 20. INDEX AND SECTOR MARK AC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{IW}$ | INDEX pulse width | 1.6 | 1.9 | 2.2 | us |
| $t_{IR}$ | INDEX period | 16.5 | 16.8 | 17.2 | ms |
| $t_{SW}$ | SECTOR MARK pulse width | 816 | 960 | 1100 | ns |
| $t_{IS}$ | INDEX to first SECTOR MARK | 179 | 187 | 195 | us |
| $t_{SR}$* | Sector width | | | | |
| | for 44 sectors | 366 | 374 | 382 | us |
| | for 32 sectors | 733 | 748 | 764 | us |
| | for 11 sectors | 1466 | 1496 | 1527 | us |

WRITE DATA and WRITE CLOCK timing relationship is shown in Figure 11 and their AC characteristics are listed in Table 21.

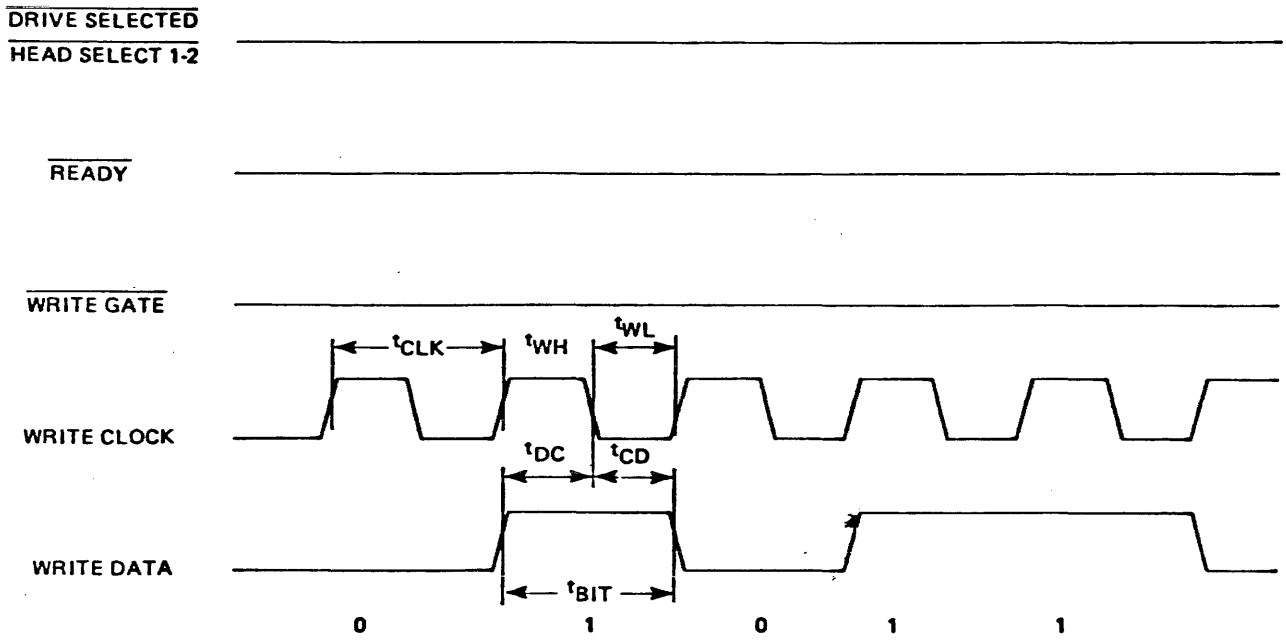



Figure 11. WRITE DATA and WRITE CLOCK Timing

TABLE 21. WRITE DATA AND WRITE CLOCK AC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CLK}$ | WRITE CLOCK period | 137 | 139 | 141 | ns |
| $t_{WH}$ | WRITE CLOCK high pulse width | 59 | 69.5 | 80 | ns |
| $t_{WL}$ | WRITE CLOCK low pulse width | 59 | 69.5 | 80 | ns |
| $t_{BIT}$ | WRITE DATA bit period | 137 | 139 | 141 | ns |

READ DATA and READ CLOCK timing relationship is shown in Figure 12 and their AC characteristics are listed in Table 22.

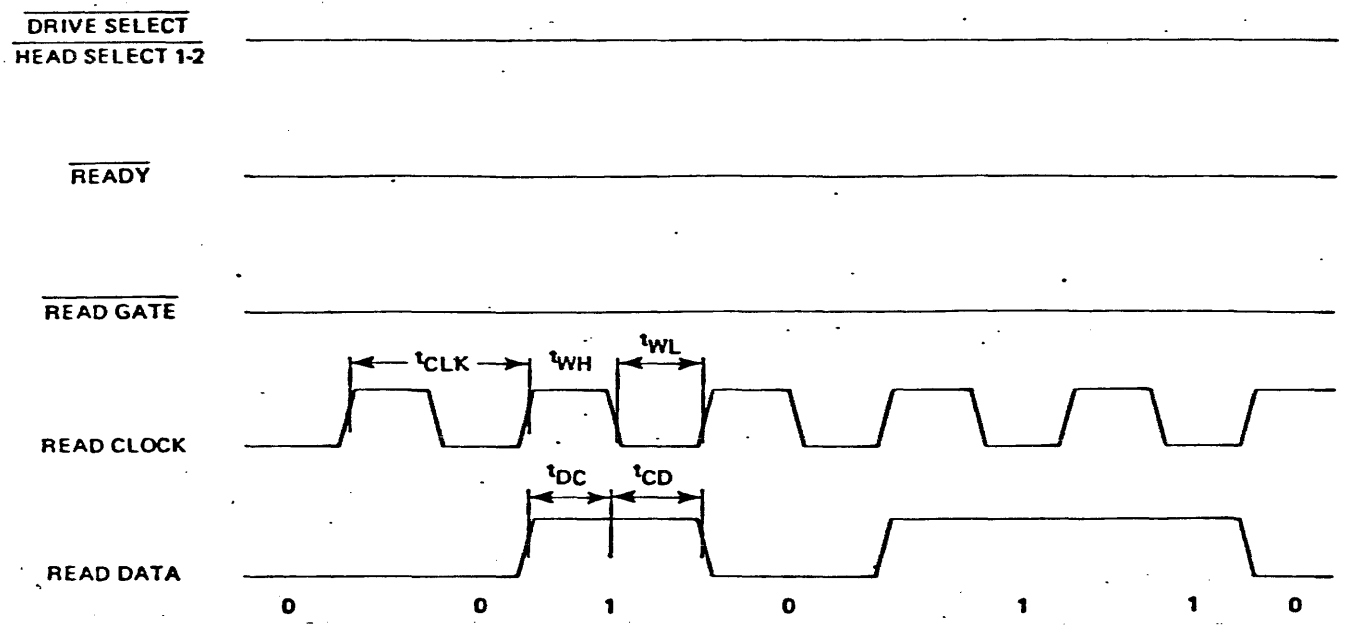



Figure 12. READ DATA and READ CLOCK Timing

TABLE 22. READ DATA AND READ CLOCK AC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CLK}$ | READ CLOCK period | 129 | 139 | 149 | ns |
| $t_{WH}$ | READ CLOCK high pulse width | 59 | 69.5 | 80 | ns |
| $t_{WL}$ | READ CLOCK low pulse width | 59 | 69.5 | 80 | ns |
| $t_{BIT}$ | READ DATA bit period | 129 | 139 | 149 | ns |

Figure 13 shows timing requirements for writing full sectors (ID and data fields) and also for writing sector data fields only.

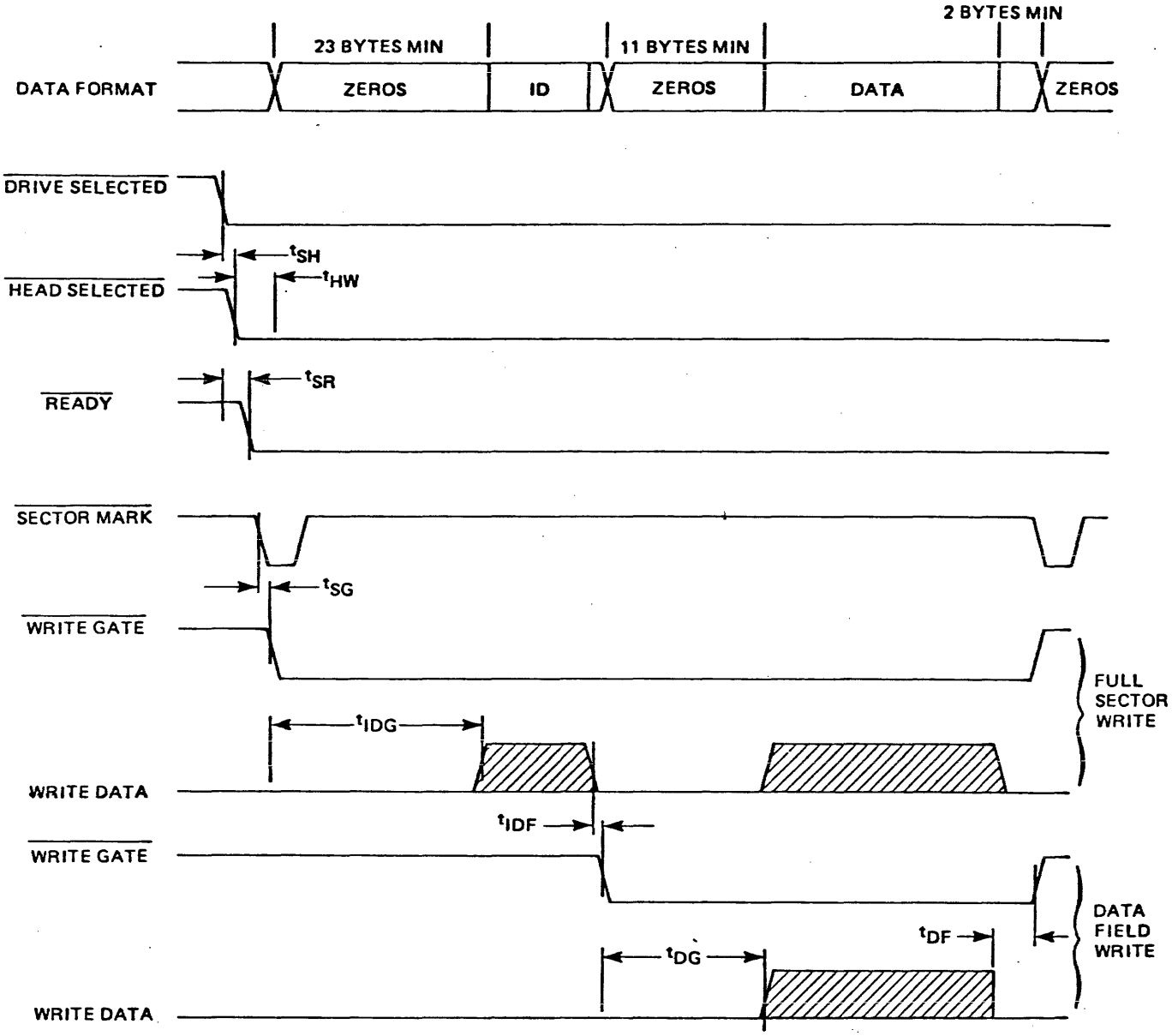



Figure 13. Record Writing Timing

TABLE 23. RECORD WRITING CONTROL AC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{SH}$ | DRIVE SELECTED to HEAD SELECTED | 20 | | | us |
| $t_{SR}$ | DRIVE SELECTED to READY | 100 | | | ns |
| $t_{SG}$ | SECTOR MARK TO WRITE GATE | -1 | 0 | 1 | us |
| $t_{IDG}$ | ID gap timing (23 bytes min) | 18.8 | 22.1 | | us |
| $t_{IDF}$ | ID fill (2 Byte min) | 1.63 | 1.92 | | us |
| $t_{DG}$ | Data gap (no WRITE to READ transitions (11 byte min) | 8.98 | 10.56 | | us |
| $t_{DF}$ | Data fill (2 Byte min) | 1.63 | 1.92 | | us |
| $t_{HW}$ | Head Select to WRITE GATE | 100 | | | ns |

Figure 14 shows timing requirements for reading ID and data fields and for reading data fields only.

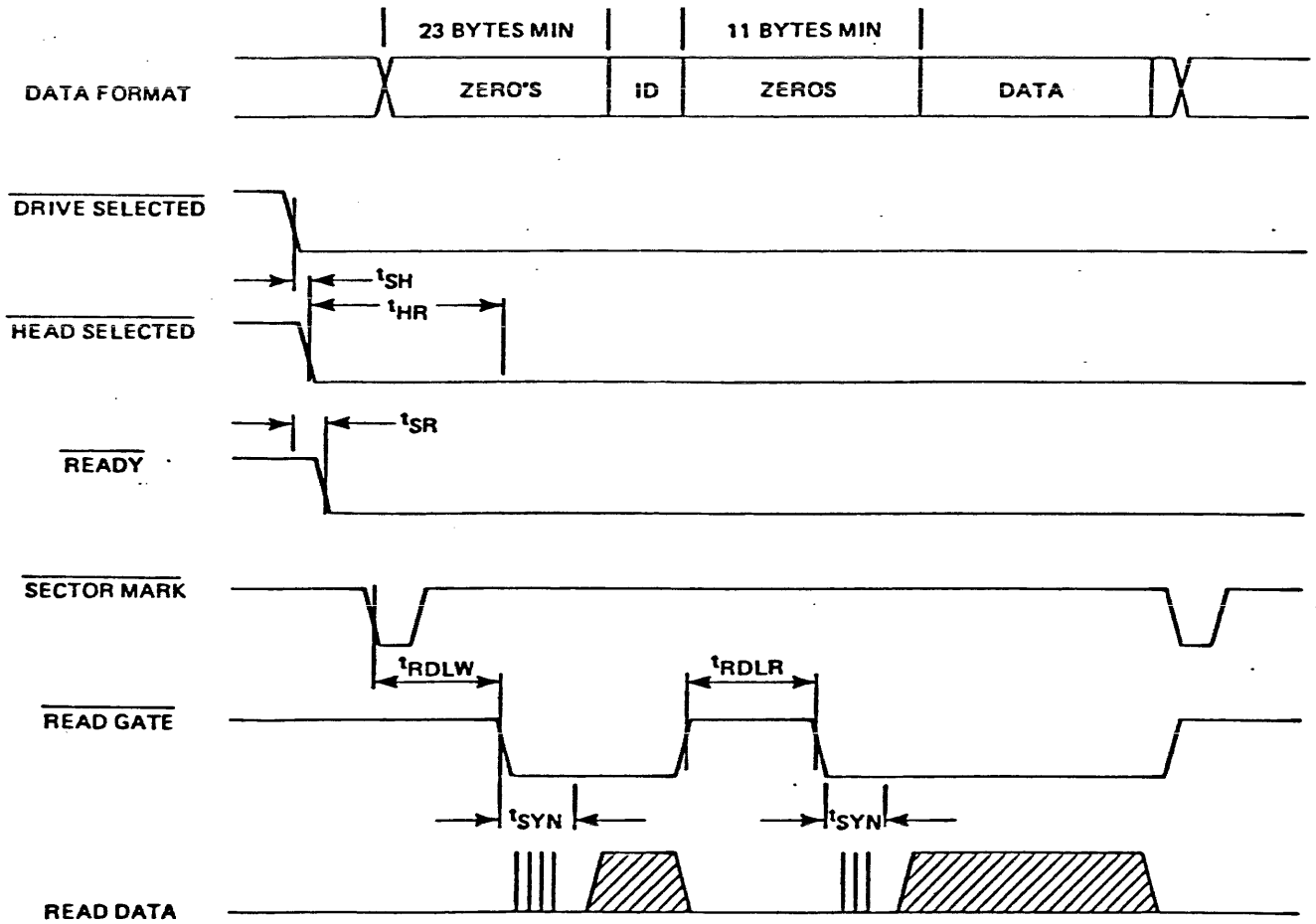



Figure 14. Record Reading Timing

TABLE 24. RECORD READING CONTROL AC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{SH}$ | DRIVE SELECTED to HEAD SELECTED | 20 | | us |
| $t_{SR}$ | DRIVE SELECTED to READY | 100 | | ns |
| $t_{RDLW}$ | READ GATE DELAY for gaps allowing WRITE to READ transitions | 10 | | us |
| $t_{RDLR}$ | READ GATE DELAY for gaps limited to READ to READ or READ to WRITE transitions | 1 | | us |
| $t_{SYN}$ | READ PLO SYNCHRONIZATION (Data not valid for this period) | | 8 | us |
| $t_{HR}$ | HEAD SELECT to READ GATE | 10 | | us |

The combined operations are shown in Figure 15.

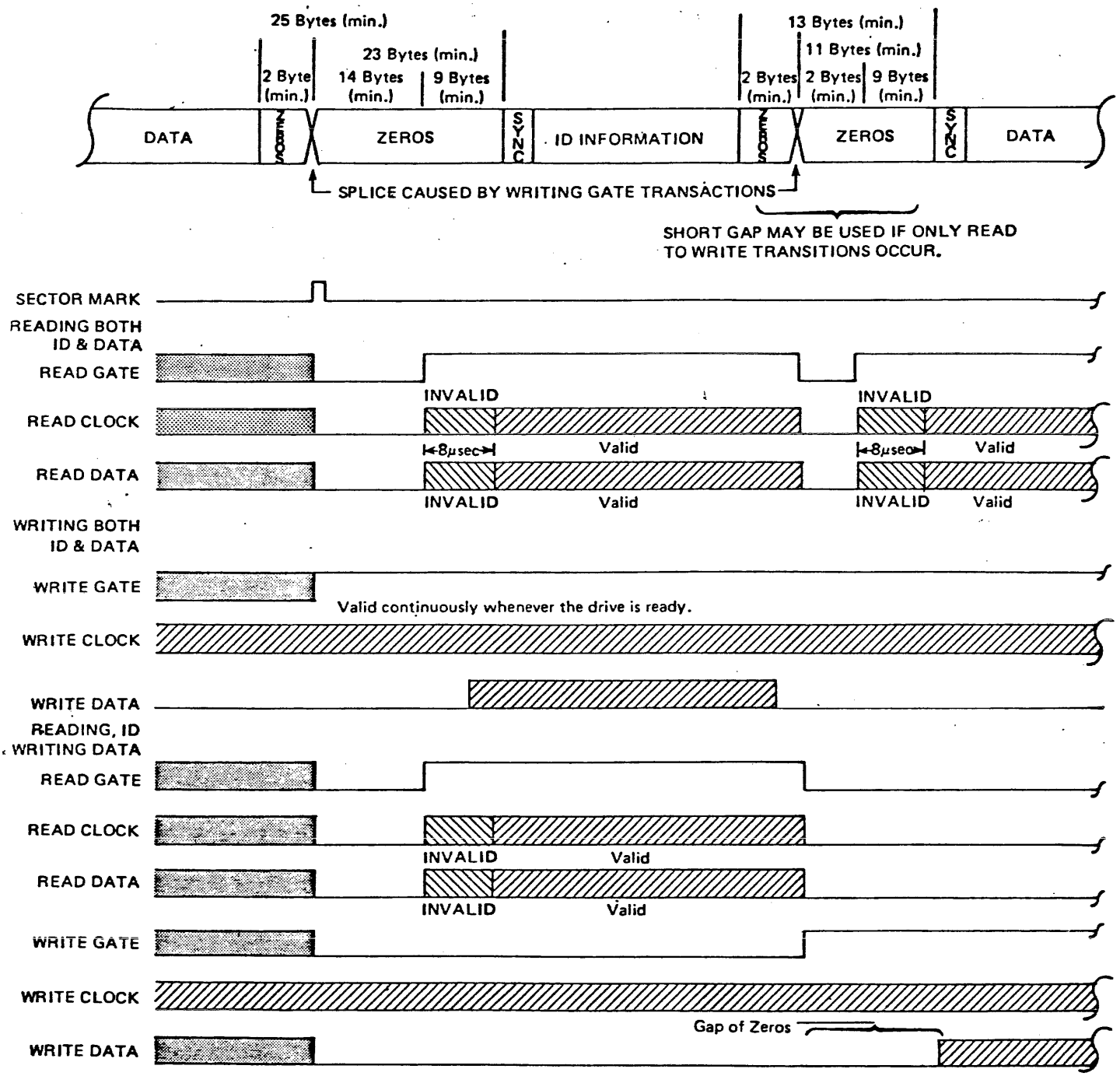



Figure 15. Read and Write Transitions During Gaps.

## V. SUGGESTED DATA FORMAT

### A. Format Definitions

The suggested format is similar to the soft sectored format used on flexible discs.

This format has the sector ID field and the data field separated by a gap. This allows reading of the ID field to verify position, and subsequently switching to write mode during the gap and writing a new data field.

The soft sector format is shown in Figure 16 and is described below.

Each track starts with an INDEX pulse, which corresponds to a certain area of the index ring. Also, the index ring provides rotational position information for the generation of SECTOR MARK pulses. A sector pulse precedes each record and successive records are separated by gaps within which the sector pulses occur.

#### 1. PRE-RECORD GAP (GAP 1)

The Pre-Record Gap, or Gap 1, appears at the beginning of every record. It consists of 23 bytes of zeros. The length of Gap 1 never varies. The first Gap 1 after INDEX is followed by the Skip Defect Record. All other Gap 1's, after SECTOR MARKS, are followed by ID records.

#### 2. SKIP DEFECT RECORD

The Skip Defect Record consists of 11 bytes: a Data Sync using the hexadecimal pattern FB, the physical address of the first defect using two bytes, the physical address of the second defect using two bytes, the physical address of the third defect using two bytes, a check sum across the previous six bytes using two bytes, and fill characters of zeros using two bytes.

#### 3. ID FIELD

This Identification Field uses nine bytes: an ID sync of one byte, the head address and high order cylinder address of one byte, the low order cylinder address of one byte, the sector number of one byte, a sector length and flag bytes, two CRC (cyclic redundancy check) bytes, and two bytes of zeros for filling. The cylinder and head address, along with the sector number, verify that the drive has addressed the correct track and sector.

#### 4. ID GAP (GAP 2)

The ID Gap, or Gap 2, separates each successive Identification Field from its Data Field. It contains 11 bytes of zeros.

5. DATA FIELD

Following Gap 2, the Data Field may consist of any number of bytes but lengths of 261, 517, or 1029 bytes are common for 256, 512 or 1024 data lengths. The first byte is a data sync, while the last four bytes consist of two bytes of CRC and two bytes of zeros for filling.

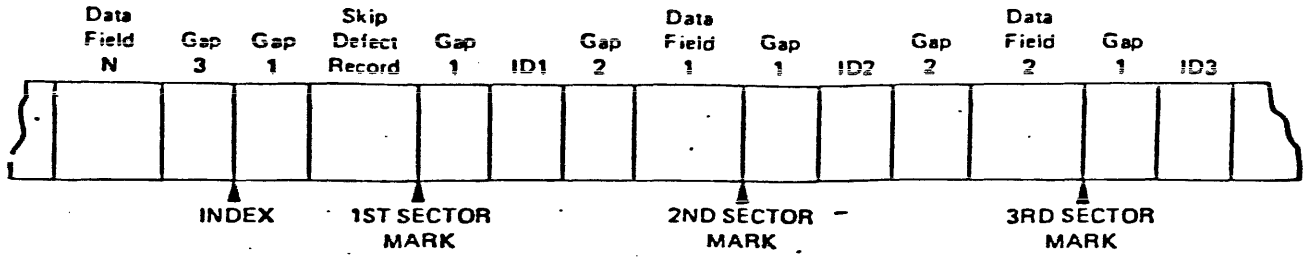
6. PRE-INDEX GAP (GAP 3)

The Pre-Index Gap, or Gap 3, is used only once on a track. It appears at the end of the last data field and persists until INDEX. This gap contains zeros.

Table 25 lists a few of the various available soft sector track formats.

TABLE 25. HARD SECTOR FORMAT INFORMATION

| Data Field Length (bytes) | Sector Length | Sectors Per Track | Gap 1 (bytes) | Gap 2 (bytes) | Gap 3 (bytes) | Data Per Track (bytes) | Data Capacity (bytes) | Percent Utilization (bytes) |
|---|---|---|---|---|---|---|---|---|
| 256 | 304 | 44 | 23 | 11 | 28 | 11,264 | 8,560,640 | 75.1% |
| 512 | 560 | 22 | 23 | 11 | 524 | 11,264 | 8,560,640 | 75.1% |
| 1024 | 1072 | 11 | 23 | 11 | 540 | 11,264 | 8,560,640 | 75.1% |




| | | |
|---|---|---|
| Gap 1: | Zeros | 23 Bytes |
| Skip Defect Record: | Data sync X'FB | 1 Byte |
| | 1st defect address | 2 Bytes |
| | 2nd defect address | 2 Bytes |
| | 3rd defect address | 2 Bytes |
| | Check sum | 2 Bytes |
| | Fill characters - zeros | 2 Bytes |
| Sector Mark: | Derived from INDEX and servo clock | |
| Gap 1: | Zeros | 23 Bytes |
| ID Field: | ID sync | 1 Byte |
| | Head and high order cylinder address | 1 Byte |
| | Low order cylinder address | 1 Byte |
| | Sector address | 1 Byte |
| | Sector length & flag | 1 Byte |
| | CRC | 2 Bytes |
| | Fill characters - zeros | 2 Bytes |
| Gap 2: | Zeros | 11 Bytes |
| Data Field | Data sync | 1 Byte |
| | Data | n Bytes |
| | CRC | 2 Bytes |
| | Fill characters - zeros | 2 Bytes |
| Gap 3: | Zeros | Size depends on data field size |

Figure 16. Soft Sector Format